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Electromagnetic Launcher Control Using Finite State Machines

1Lt Jeffrey M. Gay, Mark W. Heyse, James B. Cornette

Wright Laboratory, Armament Directorate
Analysis and Strategic Defense Division
Electromagnetic Launcher Technology Branch (WL/MNSH)
Eglin AFB FL 32542-5000

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1Lt Jeffrey M. Gay, James B. Cornette, Mark W. Heyse,WL/MNSH

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This paper shows the continued viability of sequential Finite State Machines (FSM s) as a means to control the sequencing of Electromagnetic Launcher (EML) systems. While computer controlled sequencing is an attractive alternative, FSM s are easy to design, inexpensive and reliable. Several FSM controllers are currently in use for the long duration EML experiments at the Hypervelocity Research Facility, Eglin AFB, FL. This paper discusses the basic system design with reference to design procedure and systems interfacing, flexibility, and the fail-safe nature of the FSM (i.e., system interrupt capability) are also discussed. Where requirements include repeatability, reliability, ease of operation, relative low cost, and flexibility, the FSM is presented as a reasonable alternative to more expensive computer-based systems.

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1LT Jeffrey M. Gay
James B. Cornette
Mark W. Heyse

Wright Laboratory Armament Directorate (WL/MNSH)
Eglin Air Force Base, Florida 32542-5434

Abstract- This paper shows the continued viability of sequential Finite State Machines (FSMs), as a means to control the sequencing of Electromagnetic Launcher (EML) systems. While computer controlled sequencing is an attractive alternative, FSMs are easy to design, inexpensive and reliable.

Several FSM controllers are currently in use for the long duration EML experiments at the Hypervelocity Research Facility, Eglin Air Force Base, Florida. This paper discusses basic system design, with reference to design procedure and systems interfacing. Flexibility, and the fail-safe nature of the FSM (i.e., system interrupt capability) are also discussed. Where requirements include repeatability, reliability, ease of operation, relative low cost, and flexibility, the FSM is presented as a reasonable alternative to more expensive computer based systems.

INTRODUCTION

Before making the decision to sink lots of money into the computers, and associated hardware and software, necessary to control repeated sequencing of Electromagnetic Launchers (EMLs), discrete hardware controllers should be considered. Working from an algorithm describing a sequence of events; a simple, reliable, systems controller can be designed. The number of steps allowed in a complete sequence is unlimited, allowing for flexibility in design, and sequence modification as needed. The heart of any Finite State Machine (FSM) is a memory device, such as a flip-flop, decoder, programmable logic array, or ROM. This allows the designer to choose the device best suited for a given application. The controllers used at the Eglin Hypervelocity Research Facility are based on decoders, sequenced by counters. Here again, there are many devices available for sequence control, with the optimum device determined by the application.

Interfacing a controller to the outside world is another area where the FSM excels. The designer isn't limited to off the shelf devices. At the Eglin facility, interfacing techniques utilize standard electrical connections (BNC) and fiber-optic links, as well as magnetic and inductive pick-ups. The sequences of the machine can also be made available for triggering data acquisition systems, other controllers, video equipment, or any device operating in conjunction with the controller.

FINITE STATE MACHINES

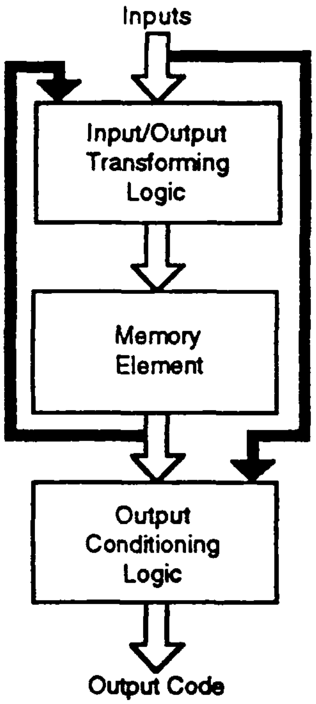


Fig. 1. General model of a finite state machine.

The heart of any FSM is the memory element. As shown in Fig. 1, it's used to store information related to the past history of the inputs to the system [1]. Fig. 1 also serves as a basic block diagram for the Multiple Sequence Interface/Controller (MSI/C) described in this paper. Designed and built at the Eglin facility, the MSI/C employs a 74LS138 3-line to 8-line Decoder as the memory element. In conjunction with the decoder, Multiplexers (MUXs), combinational logic elements, and flip-flops, are used in the input/output transforming logic. Designing the input/output transforming logic represents most of the work involved in FSM design. However, careful use of Karnaugh maps (K-maps) simplifies the task, yielding a design that minimizes gate usage.

Devices for sequencing the memory element of a FSM include counters, and shift registers. Sequencing of the MSI/C is accomplished with a 74LS160 synchronous 4-bit counter. The normal count rate is 10 MHz, with count and load operations controlled by separate 74LS151 8-bit MUXs. Whenever possible, some form of unit distance code should be employed in the count sequence of a FSM in order to avoid flashing during state changes. This makes the 'LS160 ideal for sequencing applications, since it has independent count and load functions. In order for a FSM to function properly, the present state, or count, of the machine must be fed back to the input transforming logic. Through this logic, the next state information for the machine is generated. For the MSI/C, this information is presented to the counter inputs. Thus, using the MUXs to either load the counter, or allow it to count normally, any sequence can be formed. Design of the output conditioning logic depends heavily upon the application at hand. For example, the MSI/C uses numerous fiber-optic transmitters. With each transmitter pulling 30 mA to 60 mA, buffers and line drivers are employed as drivers and predrivers before final output.

DESIGNING A FSM

Designing a FSM can be difficult unless a structured approach is taken. However, following some basic rules will result in a system that works with little to no debugging. Reference [1] suggests a 10 phase algorithm for FSM design. This can usually be cut to 7 phases, as follows: (1) Define the purpose and role of the system, (2) Define the basic operations and limitations of the system, (3) Using timing diagrams, define the timing and frequency of the system level input and output control signals, (4) Detail the sequential behavior of the system controller, (5) Develop a Mnemonic Documented State (MDS) diagram for controller operation using phases 1, 2, 3, and 4 as reference, (6) Choose a system controller architecture and, (7) Use suggested rules and constraints to make state assignments [1], [2].

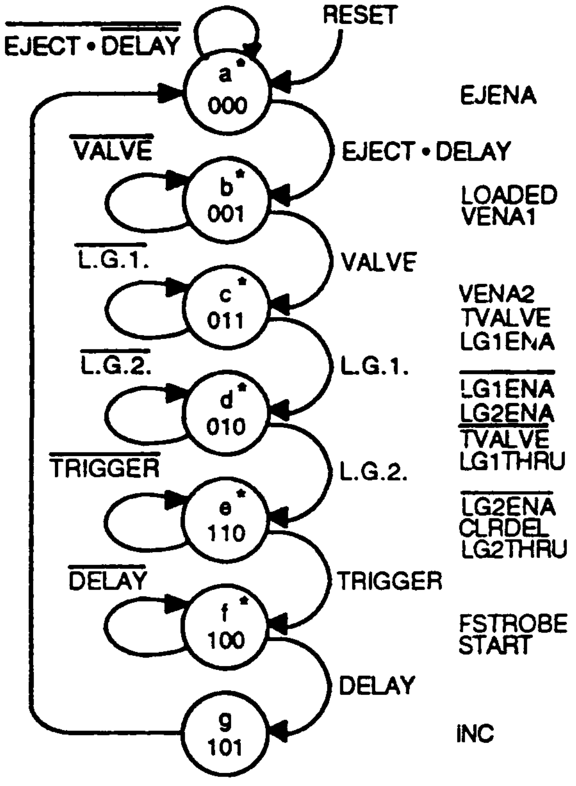


Fig. 2. MDS diagram for the MSI/C.

ACTUAL CONTROLLER DESIGN

The MSI/C arose from the requirement for multiple discharges of the Eglin 5 MJ power supply, with adjustable inter-discharge delay times from 200 ms to 5 s. From this requirement, and working with the test engineer, an algorithm for the controller was developed. Since the events that take place before, during, and after the discharge of the power supply are sequential and repeating in nature, a FSM was the logical choice for controlling the process. Originally designed to be an interface, the unit is a fully functional controller that performs as an interface.

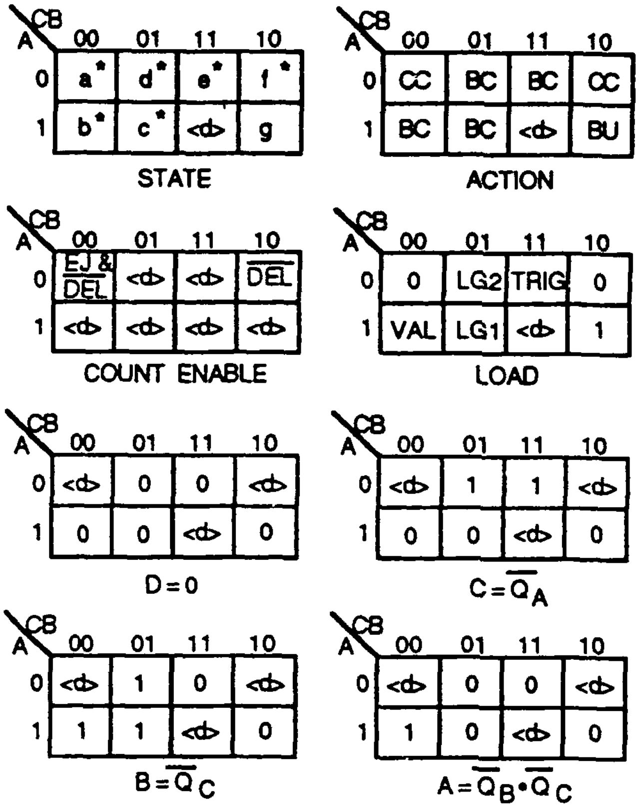
Following the previously mentioned design phases, block diagrams, flow diagrams, and timing diagrams were constructed to determine the sequential behavior of the controller. In designing a system of any kind, elegance and simplicity mean reliability. With that in mind, a go-no-go construct was sought, to reduce the possibility of timing problems in the final product. Put simply, the go-no-go structure is the epitome of sequential machine design. In such a system, all actions are predicated on the completion of a previous action (or actions). If the conditions for transitioning to the next machine state are not met, the machine simply idles until they are. This is especially attractive where EMLs are concerned, as the energy levels used can be quite destructive if not properly controlled. For example, at the Eglin facility, in order to avoid voltage breakdown at the breech of a launcher, or system discharge at the instant a projectile reaches the breech, the velocity of the projectile is used to determine a delay time before energy transfer. Delay time calculation is handled by the controller, and energy transfer cannot take place until the delay is satisfied. Past experience has shown that transferring energies in the Megajoule range can be catastrophic for an empty launcher, making this FSM capability invaluable.

Fig. 2 shows the MDS diagram for the MSI/C. The go-no-go construct is evident where the states (each bubble represents a machine state) loop back on themselves. This represents an idle condition, where the machine is waiting for the conditions for transitioning to be met. Note the unit distance sequencing, as only one bit changes for any given transition (except the last one). The mnemonic at each transition arrow indicates the action causing the transition, while the information to the right of each bubble indicates actions taking place while in a given state. Each state is also given a letter. These letters are used in the "state" K-map, as an aid in filling out the rest of the K-maps. Some of the actions in a FSM of this type will be asynchronous and/or conditional in nature. These are indicated with an asterisk in the MDS diagram. It is easy to see the value of the MDS diagram as a design or troubleshooting aid. A well documented MDS diagram completely explains the operation of the machine. Fig. 3 shows the three sets of K-maps needed to complete the design of the MSI/C. This set of maps is typical for any FSM of similar architecture. In Fig. 3, the "action" and "state" maps are used as aids in completing the rest of the maps. The "state" map is a 2-by-4 map with the letters from the state bubbles entered as determined by the sequencing code. The "action" map contains descriptors for the operations that cause state to state transitions in the machine. For example, a conditional count takes the machine from state 000 to 001. Thus, a CC is entered in the 000 box of the 2-by-4 K-map. Similarly, since the transition from 001 to 011 in a conditional branch, a BC is entered in the 001 box. Unconditional branching is indicated with a BU.

Since the MSI/C employs two MUXs in generating its sequence, each requires a K-map to determine the proper MUX inputs. Using the action map as a guide, the "count enable" and "load" maps are constructed. The count enable map is built by replacing all CC entries with the logic function desired before the count can be allowed. Similarly, all BC entries are replaced with the proper logic function, in a separate "load" map. The logic functions are taken directly from the MDS diagram.

Finally, parallel data maps are generated to determine the logic needed to convert the present state of the machine into next state information. This is fed to the counter inputs, insuring that the desired sequence is generated. A single K-map is made for each counter bit. Since only three bits are used in the MSI/C sequence, one of the maps is redundant. However, it takes little time to construct, and may come in handy for future system modifications. Filling in the parallel data maps is started by entering "don't cares" (<d>) for all CC entries from the action map. When a transition results in a change in any given bit (e.g., 1 to 0, or 0 to 1), a "1" is entered into the map. If no change occurs, a "0" is entered. As shown under each map, solving the parallel data maps yields the minimized logic needed for generation of the next state information. Thus, by following the phases discussed earlier, the controller design is complete (except for interfacing), and easily read from the K-maps, in conjunction with the chosen system architecture. Note that, by cascading counters, MUXs, and decoders, any length sequence can generated. Indeed, devices can be inserted for future expansion, and strapped in as needed. For the MSI/C, many of the MUX inputs are unused. Thus, as future needs arise, there is built in flexibility to expand. Such flexibility is characteristic of a FSM designed around the go-no-go construct. If the controller is a wire-wrapped prototype, changes can be made on the spot. Once the prototype is a proven performer, circuit boards can be made, still leaving room for modifications.

With the FSM, interfacing options are also unlimited. In the MSI/C, all inputs are fiber-optic. Outputs reaching the high energy environment of the launchers are also fiber-optic. Electrical signals used to trigger the DAS and record controller state information are optically isolated from the controller, and battery powered on the DAS side. Such optical isolation keeps the control electronics separate from the noisy EML environment. However, to insure compatibility with older systems, parallel electrical connections are available for critical input, and output functions.



A\CB	00	01	11	10
0	a*	d*	e*	f*
1	b*	c*	<d>	g

STATE

A\CB	00	01	11	10
0	CC	BC	BC	CC
1	BC	BC	<d>	BU

ACTION

A\CB	00	01	11	10
0	EJ & $\overline{DEL}$	<d>	<d>	$\overline{DEL}$
1	<d>	<d>	<d>	<d>

COUNT ENABLE

A\CB	00	01	11	10
0	0	LG2	TRIG	0
1	VAL	LG1	<d>	1

LOAD

A\CB	00	01	11	10
0	<d>	0	0	<d>
1	0	0	<d>	0

$D=0$

A\CB	00	01	11	10
0	<d>	1	1	<d>
1	0	0	<d>	0

$C=\overline{Q}_A$

A\CB	00	01	11	10
0	<d>	1	0	<d>
1	1	1	<d>	0

$B=\overline{Q}_C$

A\CB	00	01	11	10
0	<d>	0	0	<d>
1	1	0	<d>	0

$A=\overline{Q}_B \bullet \overline{Q}_C$

Fig. 3. MSI/C K-maps.

The basic controller portion of the MSI/C is shown in Fig. 4. The MUX inputs are taken directly from the count enable, and load K-maps. For each "0," the input is grounded. Where a "1" appears, the input is tied to +5 V. The rest of the inputs, interfaced from the outside world, are applied either directly to the MUXs or routed through the appropriate logic ahead of the MUX inputs.

This structured approach to FSM design results in an elegant, easy to understand documentation package. Referring to the MDS diagram (Fig. 2), the sequence of events is easily traced on the controller schematic (Fig. 4). By monitoring the states of the controller during launcher operation, a time reference is established for every event. If problems arise during launcher sequencing, correlation of the machine state with the suspicious event can often lead to quick solutions of problems that might otherwise be difficult to troubleshoot. By the same token, such signal monitoring may indicate the need for sequence modifications within the controller. This synergistic relationship between the controller and the outside world is probably the best reason for using FSMs to control EML operations.

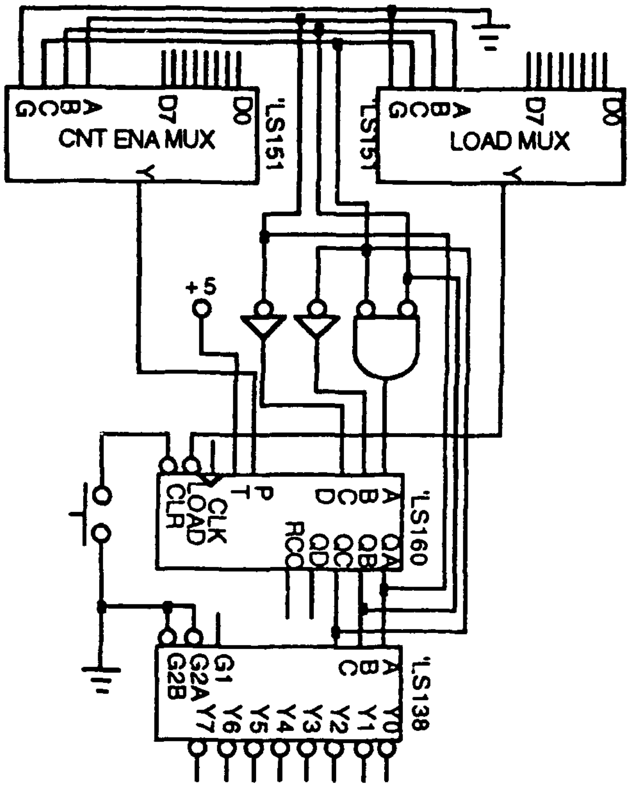


Fig. 4. Basic controller section of the MSI/C.

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[2] Clare, Christopher R., "Designing logic systems using finite state machines." New York: McGraw-Hill, 1973.

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