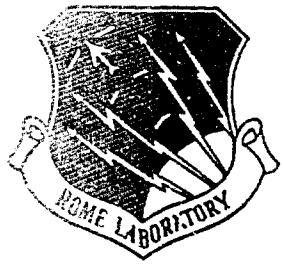
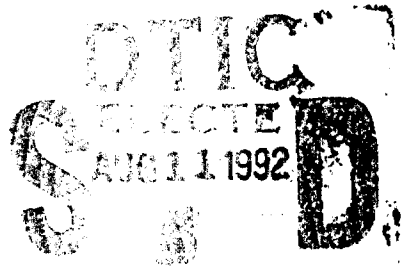
RL-TR-92-12, Vol II (of two)
Final Technical Report
February 1992



TESTABILITY DESIGN RATING SYSTEM: Analytical Procedure

Raytheon Company

Ronald E. Press, Michael E. Keller, Gregory J. Maguire



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RL-TR-92-12, Vol II (of two) has been reviewed and is approved for publication.

APPROVED: Roy F. Stratton

ROY F. STRATTON
Project Engineer

FOR THE COMMANDER: Anthony J. Feduccia

ANTHONY J. FEDUCCIA
Acting Director
Electromagnetics & Reliability Directorate

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REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY (Leave Blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	February 1992	Final Jun 89 - Feb 91

4. TITLE AND SUBTITLE
TESTABILITY DESIGN RATING SYSTEM Analytical Procedure

5. FUNDING NUMBERS
C - F30602-89-C-0121
PE - 62702F
PR - 2338
TA - 02
WU - 4F

6. AUTHOR(S)
Ronald Press, Michael E. Keller, Gregory J. Maguire

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Raytheon Company
Equipment Division
Marlborough MA 01752

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Rome Laboratory (ERSR)
Griffiss AFB NY 13441-5700

10. SPONSORING/MONITORING AGENCY REPORT NUMBER
RL-TR-92-12, Vol II (of two)

11. SUPPLEMENTARY NOTES
Rome Laboratory Project Engineer: Roy F. Stratton/ERSR(315) 330-4205

12a. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT (Maximum 200 words)

This effort provides a means of rating the testability of an electronic design at any stage in the design life.

Volume I, Testability Handbook, discusses the particulars of the circuit design and how they relate to testability. It also discusses the software developed in this program and how to obtain the software. The software, which will run on any IBM compatible PC having 512 k of available memory and a hard disk, asks a number of questions, and based on the answers, will provide a testability rating and a credibility rating.

Volume II provides means of doing the testability analysis without the computer.

14. SUBJECT TERMS
Testability, Ratings, Design, Test & Evaluation

15. NUMBER OF PAGES
494

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	U/L

EXECUTIVE SUMMARY

The purpose of the Testability Design Rating System (TDRS) contract was to develop a method of rating a design's inherent testability and provide recommendations on how to improve the design's testability. The TDRS was developed by creating a methodology, implemented in a Personal Computer (PC) program which rates the testability of a design and a corresponding TDRS testability handbook which has recommendations on how to improve a design's testability.

The TDRS Testability Handbook is a two volume set. Volume One contains this TDRS executive summary, a TDRS introduction, and recommendations on how to improve the testability aspects of a design. Volume One, Section 1 is an introduction to Volume One and contains a description of each section within Volume One (pages 1-8 and 1-9). Volume One includes a list of acronyms and abbreviations before the main sections. It also includes a Bibliography and Glossary after the main sections.

Volume Two contains a copy of this executive summary and a listing of all the parameters and equations that are used in the TDRS computer program to rate a design's testability. It also contains the instructions and data needed to manually generate a testability rating.

The TDRS contract requirements were fulfilled in four phases, Each phase fulfills a major part of the TDRS development. These four phases are as follows:

PHASE ONE;

The objectives of Phase One were to determine the specific design-related parameters, associated with state-of-the-art designs, which impact testability.

Testability parameters were gathered by interviewing testability experts specializing in various technologies and by reviewing several hundred articles from technical proceedings, technical journals, books, and manuals. All of the resources used to gather testability data are included in the Bibliography of the TDRS: Volume I, Testability handbook.

PHASE TWO;

The objectives of Phase Two were to determine the relative impact of each parameter identified in phase one on the testability of a design.

Each parameter gathered in Phase One was assigned a testability weight based on the parameters relative overall impact on a design's testability.

PHASE THREE;

The objectives of Phase Three were to develop a rating system software package and a corresponding handbook which can measure the relative testability of a design and provide recommendations to improve the inherent testability of that design.

The rating system was developed as an executable PC program. A relational data base development tool, R:BASE, was used to generate the rating system code. The generation of the TDRS code used an R:BASE Compiler and does not require a licence from the R:BASE manufacturer. Since the TDRS program is executable, it can be run on any IBM compatible PC with DOS revision 3.1 or greater. A testability rate can also be generated manually by using the procedure and data in the TDRS testability handbook, volume two.

Recommendations on how to improve a design's testability are included in the TDRS Testability Handbook, Volume One. Each testability parameter used to generate a rate has an action associated with it. Each action refers to a section of the TDRS testability handbook which describes testability recommendations for that parameter. If a parameter is considered unresolvable, then the corresponding action is not applicable.

PHASE FOUR;

The objectives of Phase Four were to validate the TDRS by applying it to at least three (3) different Air Force designs and have an independent panel of testability experts verify the rates.

Nine MKXV designs were independently analyzed by both the TDRS program and a panel of testability experts. MKXV is an Air Force IFF (Information Friend or Foe) program. The designs consisted of three (3) MKXV Line Replaceable Units (LRUs) and six Module/Circuit Card Assemblies (CCAs) within the LRUs.

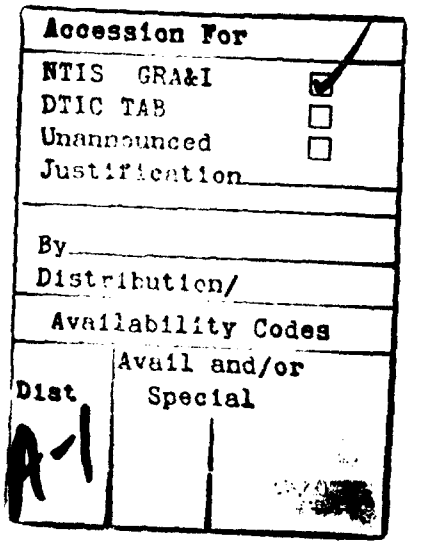
The independent MKXV analyses were performed by testability experts from Raytheon using a customized version of MIL-STD-2165. The testability experts also provided a testability rating for each design based on their own personal opinions.

The MKXV designs were then analyzed using the TDRS software. The results of the TDRS analysis was compared to the customized 2165 analysis and the expert opinions. The variance between the TDRS and customized 2165 analyses were within 17 %. The variance between the TDRS and the testability experts opinions were within 12 %.

CONTENTS

PREFACE

This is the final technical report delivered by Raytheon Company to Rome Air Development Center as required by the Testability Design Rating System (TDRS) contract (#F30602-89-0121). This is Volume Two (2) of a two (2) volume set. The title of this volume is the Testability Design Rating System: Volume Two, Analytical Procedure. The executive summary, included in both volumes, describes the TDRS project.



SECTION 1. INTRODUCTION

1.0 OVERVIEW.

The Testability Design Rating System (TDRS) can analyze the testability of a design. This handbook describes the process used to perform a TDRS analysis.

A design can be analyzed with the Testability Design Rating System using the TDRS computer program or a manual procedure described in section 3 of this handbook. The analytical process used in the TDRS project is geared toward use in the TDRS computer program. All of the algorithmic calculations are completely automated in the TDRS software. A design can be manually analyzed using the same process as the software but many manual calculations are required.

A TDRS user answers various questions about a design asked either automatically (TDRS software) or manually. The TDRS software can provide various testability reports on a design which was analyzed using the TDRS software. A brief description of the TDRS software is contained in section 2 of this handbook.

The remainder of this handbook describes the analytical process used in the TDRS project. This process is automated in the TDRS software or can be manually approached.

1.1 TDRS Testability Rating and Credibility Factor.

The purpose of a TDRS testability analysis is to generate a numerical value which represents the testability of a design. This number is referred to as a Testability Rating (TR). The relevance of a Testability Rating as calculated by the TDRS software or manual analyses is as follows:

Testability Rating	Relevance
85 - 100	Excellent testability
70 - 84	Good testability
50 - 69	Minor testability problems exist
0 - 49	Major testability problems exist

Every TR has a corresponding Credibility Factor (CF) which represents how credible or reliable the TR is. A CF is a weighted measure of the number of testability questions which a user answered during a TDRS analysis versus the total number of testability questions. A low CF indicates that unanswered testability questions can have a significant impact on the associated Testability Rating. The relevance of a CF is as follows:

Credibility Factor	Relevance
80 - 100	The amount of input data is excellent
60 - 79	The amount of input data is sufficient
40 - 59	More input data should be provided
0 - 39	Input data is deficient

1.2 Testability Parameters and Subjects.

The TDRS program uses independent aspects of a design referred to as TESTABILITY PARAMETERS. Appendix B of this handbook lists the testability parameters and associated subjects used by the Testability Design Rating System. Related testability parameters are grouped into 16 SUBJECTS. The TDRS subjects are as follows:

1. General Digital
2. VLSI
3. Processors
4. Memory
5. Scan
6. General Analog
7. High Power
8. High Frequency
9. BIT
10. Electro-Optics
11. Incircuit
12. System
13. System BIT
14. Top Level
15. Module
16. Others

During a TDRS analysis, a separate TR and CF is generated for each subject analyzed and used to generate a Final TR and CF for the design.

1.3 TDRS Analysis Flow.

A subset of the sixteen subjects is analyzed during a user session. A separate analysis flow path is taken when analyzing a system/subsystem or a module.

1.3.1 System/subsystem Analysis Flow. If a system or subsystem is analyzed, then only three subjects are analyzed - Top Level, System, and System BIT. The analysis procedure for a system or subsystem is described in Section 2.

1.3.2 Module Analysis Flow. If the design being analyzed is a module, then several software flow options are possible. The user will always analyze the subjects - Top Level and Module. The user then has a choice to analyze the subjects BIT and/or Scan. Next, the type of module analysis to be performed is chosen. The user can choose to perform four types of analyses:

1. Incircuit.
2. Functional with subjects weighted by failure rates of components within each subject.
3. Functional with subjects weighted by the number of components within each subject.
4. A combination of 1 and 2 or 1 and 3 above.

If an incircuit analysis is chosen, then the subject Incircuit is analyzed and the final TR and CF are generated as presented in Section 2.

If a functional analysis is chosen, then a subset of nine functional analysis subjects is automatically chosen. These nine subjects are :

1. General Digital	2. VLSI	3. Processors
4. Memory	5. General Analog	6. High Power
7. High Frequency	8. Electro-Optics	9. Others.

They are chosen and weighted by using either the failure rates of components in the module (Failure Rate Table in Appendix D) or the number of module components within each subject (Subject Value Table in Appendix E).

A detailed flow diagram of the TDRS software is included as Appendix A of this report.

SECTION 2. TDRS ANALYTICAL PROCESS

2.0 OVERVIEW.

This section describes the analytical process used by the Testability Design Rating System to analyze a design for testability. All of the equations used in the TDRS software and manual analyses are presented in this section.

A TDRS analysis is performed by answering testability questions for specific testability subjects, generating a testability rating for each subject, weighting each subject, and generating a final rating based on subject ratings and weights.

The symbols used in all equations contained in this handbook to indicate the arithmetical function of that operation are as follows:

* = Multiplication
\- = Subtraction
/ = Division
\+ = Addition

2.1 TDRS Subject Analysis.

During a TDRS analysis each subject is independently analyzed and a testability rate (TR) and credibility factor (CF) is generated for each subject. The process used to analyze a subject is the same for every subject. The only variations from subject to subject are the testability parameters and questions associated with each subject.

2.1.1 Parameter Questions. The information used to generate a TR and CF is entered by the user by responding to questions. A question is asked for each parameter within a subject when the subject is analyzed. The question can appear in one of two standard forms - a ratio question or a true/false question. A listing of every TDRS parameter grouped by subject is included as Appendix B of this report. Each page in Appendix B represents the screen that would appear if the subject that the parameter is in was analyzed in the TDRS computer program.

In the TDRS software, each parameter is displayed in a window along with its CONCERN (why the parameter is important), an ACTION (referenced to a section of the TDRS Testability Handbook for testability recommendations for the parameter), data requests (two values for ratio parameters or a '0' or '1' for true/false parameters), and an applicability/STATUS question.

The STATUS question asks the user if the parameter is applicable. If the parameter is applicable (Y) then the user will type a Y (yes) as a response to the STATUS question. If the parameter is not applicable (N) then the user will type N as a response to the STATUS question. If the parameter cannot be addressed by the user but it is applicable, then the user enters C (cannot answer).

The parameters which have a user input of both STATUS = N and C are not used in generating a TDRS rating but the STATUS = C parameters are used to lower the TDRS Credibility Factor.

2.1.2 Subject TR and CF. The two standard parameter questions are as follows:

1. RATIO PARAMETERS:

   Ratio parameter questions ask for two numbers; The first number is the number of positive occurrences of an aspect (e.g. # of controllable clocks) and the second is the total number of occurrences of the aspect (e.g. total # of clocks). These two numbers are used in a standard ratio type of algorithm and parameters which use them are referred to as ratio parameters.

2. TRUE/FALSE PARAMETERS:

   The second type of question is a true/false question. The user responds to the question by entering a '1' for TRUE/YES or a '0' for FALSE/NO. Parameters with true/false questions are referred to as true/false parameters.

SUBJECT TR & CF:

Each parameter has two associated weights, an "A WEIGHT" and a "B WEIGHT". Parameters which are more important will have higher A and B weights. Each parameter type (ratio or true/false) has two standard algorithms which use A and B weights, referred to as ALG A and ALG B, respectively. The standard algorithms for ratio and true/false parameters are:

RATIO PARAMETERS

$$\text{ALG A} = (\text{A Weight}) * (\text{response1} / \text{response2}) \quad (1)$$

$$\text{ALG B} = (\text{B Weight}) * (\text{response2} - \text{response1}) \quad (2)$$

TRUE/FALSE PARAMETERS (response equals '1' for true, '0' for false)

$$\text{ALG A} = (\text{A Weight}) * (\text{response}) \quad (3)$$

$$\text{ALG B} = (\text{B Weight}) * (1 - (\text{response})) \quad (4)$$

The subject TR and CF use the ALG A and ALG B results along with the A Weights. The algorithms used to generate subject TRs and CFs are as follows:

SUBJECT TESTABILITY RATE (TR)

$$= 100 * \left(\frac{(\text{ALG A RESULTS})}{(\text{ALG A WEIGHTS})} - (\text{ALG B SUM}) \right) \quad (5)$$

WHERE:
(ALG A RESULTS) = (SUM of all ALG A results for STATUS = Y)
(ALG A WEIGHTS) = (SUM of all A Weights for STATUS = Y)
(ALG B SUM) = (SUM of all ALG B results for STATUS = Y)

SUBJECT CREDIBILITY FACTOR (CF)

$$= 100 * \frac{\text{(ALG A WEIGHTS)}}{\text{(ALG A WEIGHTS STATUS =Y and C)}} \qquad (6)$$

WHERE:

(ALG A WEIGHTS) = (SUM of all A Weights for STATUS = Y)

(ALG A WEIGHTS STATUS = Y and C) = (SUM of all A Weights for STATUS = Y and C (can't answer))

2.2 System/Subsystem Analysis.

When a design is analyzed using the TDRS software it is logged by the design's part number and the analysis run number. If a part number is being analyzed by the TDRS software for the first time, then the user is prompted to enter what type of design the part number is - a module or a system/subsystem. (See Appendix A page A-4).

If a design is considered a system, subsystem, Line Replaceable Unit (LRU), or any other assembly larger than a module, the system analysis path of the software flow is taken. A system analysis has only three (3) applicable subjects that will be analyzed. They are Top Level, System, and System BIT. The TDRS program will display windows for each parameter in these three subjects during a system analysis.

2.2.1 System/Subsystem TR and CF. TRs and CFs will be generated for the three subjects and will be used in the Final TR and Final CF for a system analysis. The algorithms used for a system Final TR and CF are as follows:

SYSTEM FINAL TESTABILITY RATE (TR)

$$= 0.1*(\text{Top Level Rate}) + 0.4*(\text{System Rate}) + 0.5*(\text{System BIT Rate}) \quad (7)$$

SYSTEM FINAL CREDIBILITY FACTOR (CF)

$$= 0.1*(\text{Top Level CF}) + 0.4*(\text{System CF}) + 0.5*(\text{System BIT CF}) \quad (8)$$

2.3 Module Testability Rating and CF.

If a design is considered a module, the module analysis path of the software flow is taken. The user has the option to perform a functional or in-circuit test analysis or both.

The user decides which type of analysis to perform by choosing the desired analysis in the Type of Analysis Menu in the TDRS software (see Appendix A, page A-6).

2.3.1 Module Functional Analysis. Nine subjects in the module functional analysis flow are technology based and are individually weighted for use in generating the MODULE FINAL TESTABILITY RATE and CF. The nine subjects which are assigned weights are as follows:

1) General Digital
2) VLSI
3) Processors
4) Memory
5) General Analog
6) High Power
7) High Frequency
8) Electro-Optics
9) Others

Two methods are used to weight these nine subjects; failure rate, and subject value. One of the these two methods is chosen in the Type of Analysis Menu (see Appendix A, page A-11). These methods are defined as follows:

FAILURE RATE;

Each subject is weighted based on the failure rates of the components that exist in each subject.

SUBJECT VALUE;

Each subject is weighted based on a preassigned value and the number of components that exist in each subject.

One of the two methods is chosen by the user during an analysis. and a table, corresponding to the chosen method, is filled out. The table entries are used to generate weights for the nine technology based subjects. These table-entry generated weights, Failure Rate Table weights and Subject Value Table weights, are defined as follows:

2.3.1.1 Failure Rate Table. The Failure Rate Table (FRT) which exists in the TDRS software is included as Appendix D of this report. The same process is used to fill out the FRT manually or by the TDRS software. A user merely enters the number of generic components that exist in the module for each component type listed in the FRT. The algorithm used to generate subject weights based on FRT entries is as follows:

FAILURE RATE TABLE WEIGHTS;

SUBJECT(i) WEIGHT

= Sum of [(component (i) failure rate) * (# of components (i))] (9)
where (i) consists of each component type within a subject.

where: SUBJECT(i) is any one of nine technology based subjects.

2.3.1.2 Subject Value Table. The Subject Value Table (SVT) which exists in the TDRS software is included as Appendix E of this report.

SUBJECTIVE VALUE TABLE WEIGHT;

SUBJECT(I) WEIGHT
= [(SUBJECT(i) value) * (# of components in subject (i))] (10)

where: SUBJECT(i) is any one of nine technology based subjects.

2.3.1.3 Testability Rate Weighting Factors.

2.3.1.3.1 Positive Weighting Factors. The subjects Scan and BIT are analyzed if the user chooses to do so. Since these two subjects will usually improve a design's testability, they are considered POSITIVE WEIGHTING FACTORS in the FINAL MODULE TESTABILITY RATE.

2.3.1.3.2 Negative Weighting Factors. The subjects Top Level and Module are always analyzed. Since these two subjects contain parameters that often negatively effect a design's testability, they are considered NEGATIVE WEIGHTING FACTORS in the FINAL MODULE TESTABILITY RATE.

2.3.2 Module Incircuit Analysis. If a module incircuit Analysis is chosen, then the analysis is similar to a module functional analysis. The major difference is that during an incircuit analysis, the nine technology based subjects (section 2.3.1) and subject weights are not analyzed, an Incircuit subject is analyzed instead. However, the user is able to perform both an incircuit and functional analysis concurrently by proceeding with a normal functional analysis and also analyzing the Incircuit subject. The final testability rate and CF for both an incircuit or concurrent incircuit and functional analysis are calculated using equations (11) and (12), respectively.

2.3.3 Final Module TR and CF Calculations If a subject was not analyzed then the subject TR and CF are set to '0' as a default. The Final Module TR and CF are as follows:

FINAL MODULE TESTABILITY RATE

$$= \left[\sum_{i=1}^{9} \left\{ ((\text{SUBJECT(i) RATE}) * \frac{(\text{SUBJECT(i) WEIGHT})}{(\text{sum of nine weighted subjects weights})} \right\} \right.$$

$$+ (\text{Incircuit Rate})) * \frac{1}{Y}$$

$$\left. + (\text{positive weighting factors}) - (\text{negative weighting factors}) \right] \qquad (11)$$

where: i = the nine weighted subjects (see section 2.3.1).

Y = 2 if both the functional and Incircuit analyses are done
Y = 1 if either a functional or Incircuit analysis is done

$$\text{Positive Weighting Factors} = \frac{(\text{Scan Rate}) + (\text{BIT Rate})}{10}$$

$$\text{Negative Weighting Factors} = \frac{(\text{Top Level Rate}) + (\text{Module Level Rate})}{20}$$

FINAL MODULE CF

$$= (\text{BASE MODULE CF}) * \left(1 - \frac{x}{10}\right) + ((\text{Scan CF}) + (\text{BIT CF})) * \frac{1}{10} \qquad (12)$$

where: x = 0 if Scan or BIT were not analyzed.
x = 1 if either Scan or BIT was analyzed.
x = 2 if both Scan and BIT were analyzed.

BASE MODULE CF

$$= \sum_{i=1}^{9} \left\{(\text{SUBJECT(i) CF}) * \frac{(\text{SUBJECT(i) WEIGHT})}{(\text{sum of nine weighted subjects weights})} * 0.9\right\}$$

$$+ \frac{(0.1 * (\text{Top Level CF}) + (\text{Module CF}))}{2}$$

where: i = the nine weighted subjects (see section 2.3.1).

SECTION 3. MANUAL TESTABILITY ANALYSIS

3.0 OVERVIEW.

The analysis procedure described in Section 2 can be used to perform a manual testability analysis. Several forms are included in Appendix C to facilitate a manual analysis. The remainder of this section described how to use the manual analysis forms, Failure Rate forms, and Subject Value forms with the testability parameter listing in Appendix B, to generate a testability rate.

3.1 System/Subsystem Analysis.

To complete a manual TDRS system/subsystem analysis, only the subjects Top Level, System, and System BIT need to be analyzed.

Copy the following forms from Appendix C for use during a manual analysis:

1) Top Level TR and CF Form (pages C-4 and C-5)
2) System TR and CF Form (pages C-6 to C-8)
3) System BIT TR and CF Form (pages C-9 to C-11)

3.1.1 Subject TR and CF Generation The subject TR and CF forms can be filled out by answering the questions for each corresponding parameter in Appendix B (Parameter Listing). Each parameter in the Parameter Listing sheets and in the subject TR and CF forms are referenced by a parameter number.

The user should go to the parameter listing sheets corresponding to the subject being analyzed. For each parameter, the user would make a decision whether the parameter is applicable or not. If it is not applicable, then an N is entered in the Status column of the subject form. If the parameter is applicable, but for some reason, cannot be answered, then a C is entered in the Status column. If either an N or C is entered then the parameter questions are skipped and the next parameter is checked. If the parameter is both applicable and can be answered, then an Y is entered in the Status column.

The responses to the two ratio question (in parameter listing) should be entered in the corresponding response 1 and response 2 columns in the subject forms. The response to the true/false question should be entered in the corresponding response column in the subject form.

After all of the parameter status and applicable parameter questions for a subject are answered, then the Alg A and Alg B results are calculated. An Alg A and Alg B result is calculated for every parameter with a Status of 'Y'. The columns exist to enter the Alg A and Alg B results in the subject form for each parameter. Alg A & B results are calculated using the following equations for ratio and true/false parameters:

For Ratio Parameters:

$$\text{Alg A Result} = (\text{AWeight}) * (\text{Response 1} / \text{Response 2}) \quad (1)$$

$$\text{Alg B Result} = (\text{BWeight}) * (\text{Response 2} - \text{Response 1}) \quad (2)$$

For True/False Parameters:

$$\text{Alg A Result} = (\text{AWeight}) * (\text{Response}) \quad (3)$$

$$\text{Alg B Result} = (\text{BWeight}) - (\text{Response} * \text{BWeight}) \quad (4)$$

Next the following columns are totaled at the bottom of the subject form:

1) Alg A Result
2) Alg B Result
3) AWeight (for Status = Y)
4) AWeight (for Status = Y or C)

These totals are applied to the two equations at the bottom of the subject form to generate a subject testability rate (TR) and credibility factor (CF).

This process is repeated for every subject that is analyzed.

3.1.2 System/Subsystem Final TR and CF. The results of the subject analyses (TR and CF) for Top Level, System, and System BIT are applied to the equations in the System/Subsystem Final TR and CF Form in Appendix C, page C-40.

To get recommendations on how to improve the final TR refer to the action for each parameter in Appendix B where the Alg A Result is less than the AWeight in the subject form (from Appendix C).

3.2 Module Incircuit Analysis.

A module can be analyzed for incircuit test testability by the process in this section. Complete the Top Level, Module, and Incircuit forms from Appendix C using the parameter listing in Appendix B. The process to complete a subject form is described in Section 3.1.1.

If the user wants to analyze the module for BIT, then the subject BIT is also analyzed using the BIT form in Appendix C.

The subject analysis results calculated above are applied to the equations in the Module Incircuit Analysis TR and CF Form of Appendix C, pages C-41 and C-42, to generate the final TR and CF.

To get recommendations on how to improve the final TR refer to the action for each parameter in Appendix B where the Alg A Result is less than the AWeight in the subject form (from Appendix C).

3.3 Module Functional Analysis.

To complete a module functional analysis, a subset of the module subjects is analyzed. This subset is chosen either by using a Failure Rate or Subject Value Table.

3.3.1 Subject Selection and Weighting. The user must choose either the Failure Rate or Subject Value Table (SVT) to select and weight functional subjects.

If the Failure Rate Table (FRT) is chosen, then copy the FRT in Appendix D. Enter the number of each component type that exists in the module under the '# of components' column in the FRT.

After completing the FRT, multiply the '# of components' times the failure rate for each component. Sum this result for every component for each subject. Enter this sum for each subject in a copy of the Failure Rate Table Form in Appendix C, page C-2.

If the SVT is chosen, then copy the SVT in Appendix E and enter the number of module components that exist in each subject category. Multiply the number of components times the subject value for each subject and enter the results in a copy of the Subject Value Table Form in Appendix C, page C-3.

3.3.2 Module Functional TR and CF Analysis. Analyze the subjects Top Level, Module, and every subject which has a positive weight in the FRT or SVT form. The user can choose whether to analyze the subjects BIT and/or Scan.

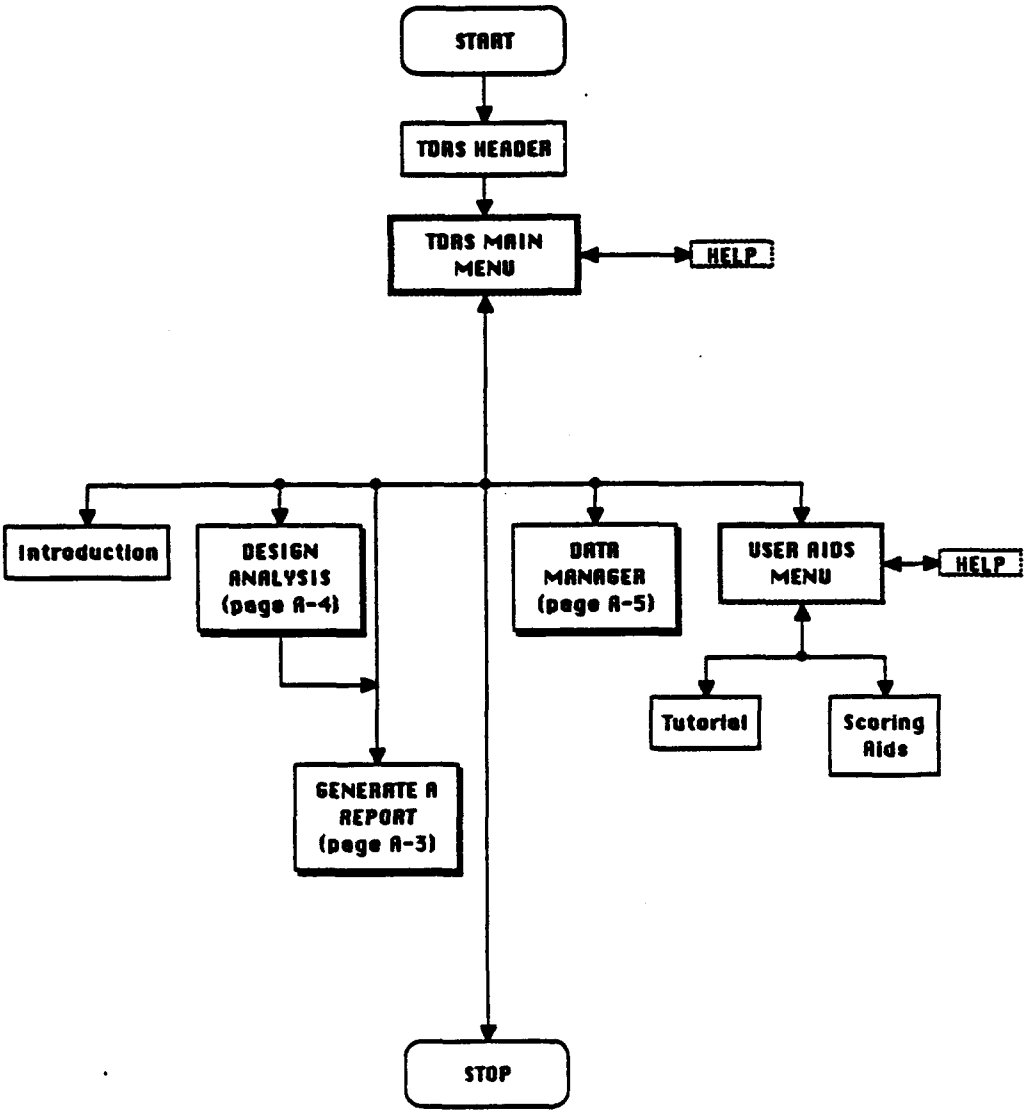
After each subject is analyzed using the procedure described in Section 3.1.1, the Module Functional Analysis Form in Appendix C, pages C-43 and C-44, is used to calculate a Final Functional TR and CF.

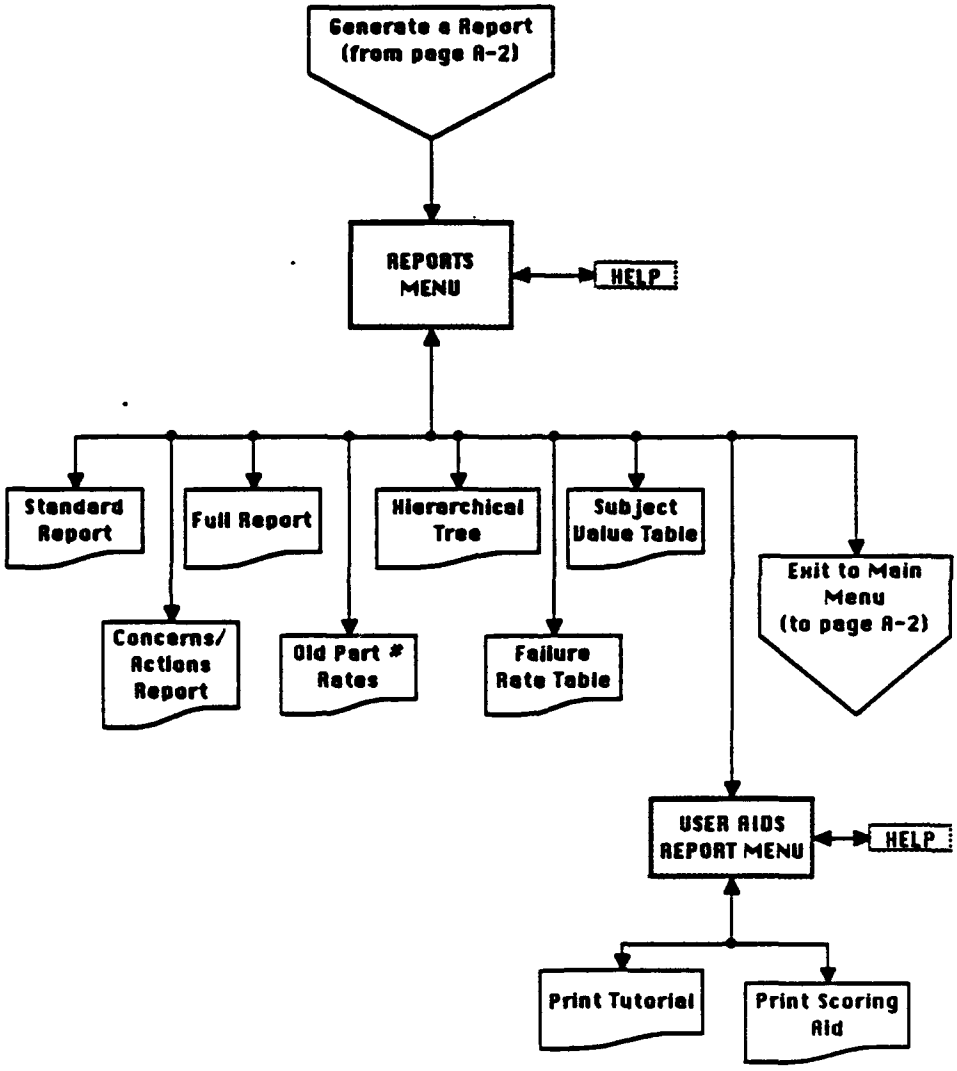
3.4 Concurrent Functional and Incircuit Module Analysis.

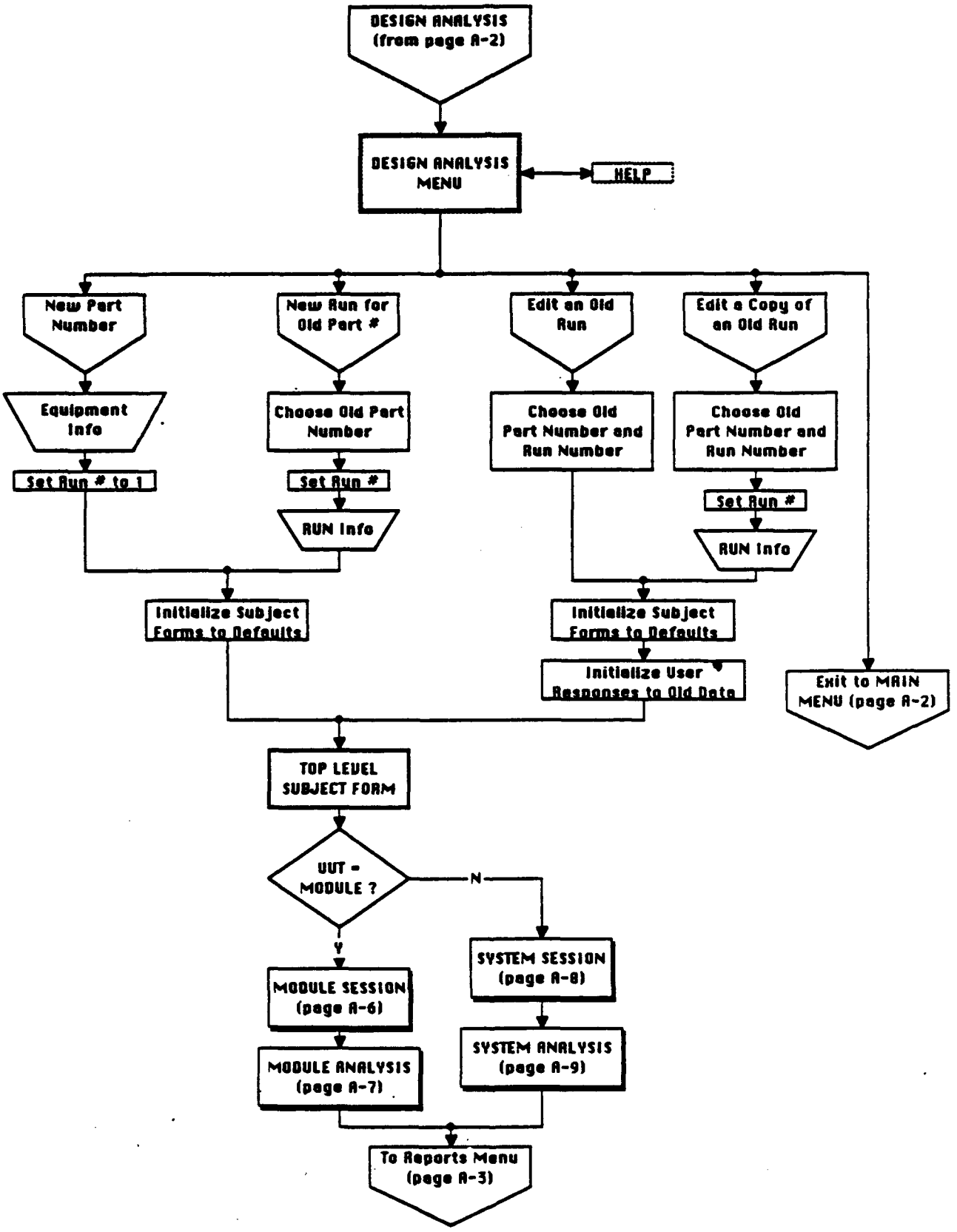
A module can be analyzed for both a functional and incircuit test analysis to generate a Final TR. The same process is followed as in the Module Functional Analysis (Section 3.3), however, the subject Incircuit is also analyzed and the Concurrent Functional and Incircuit Module Analysis Form in Appendix C, pages C-45 and C-46, is used to generate the final TR anc CF.

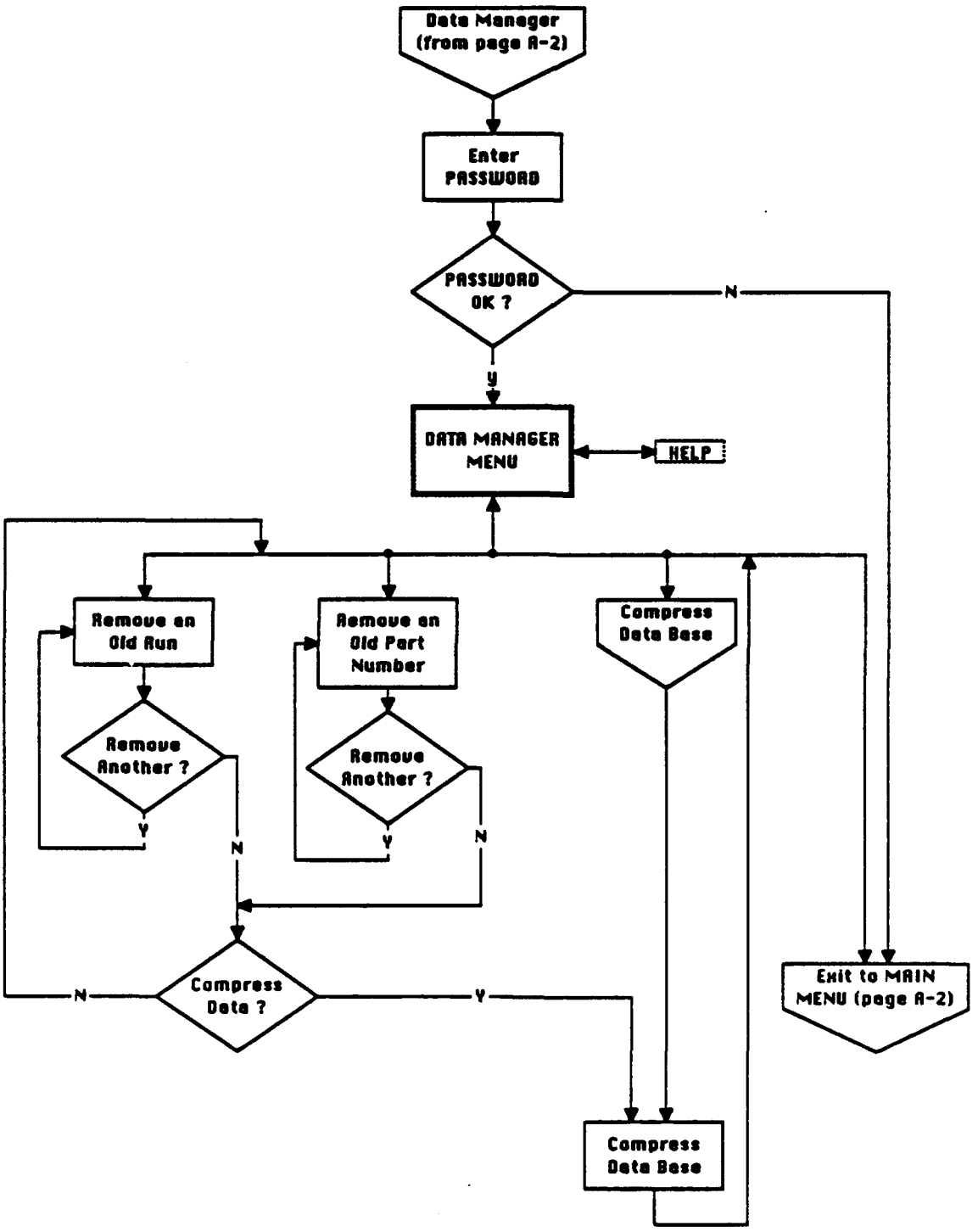
APPENDIX A

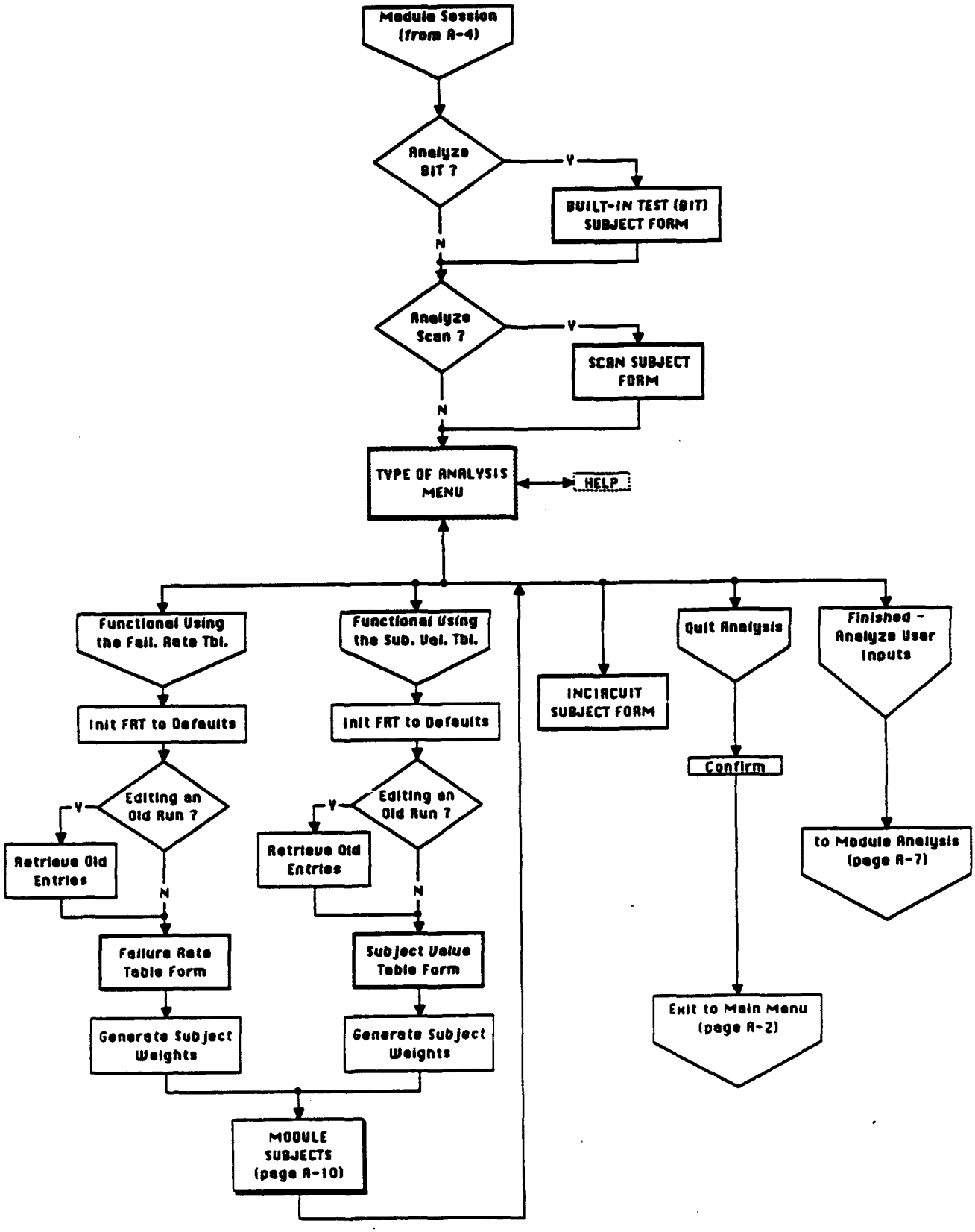
TDRS SOFTWARE FLOW DIAGRAM

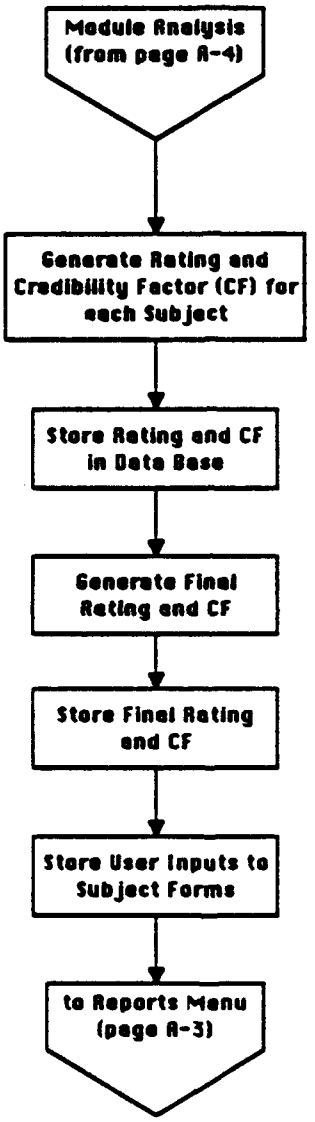

START
TDRS HEADER
TDRS MAIN MENU
HELP
Introduction
DESIGN ANALYSIS (page A-4)
DATA MANAGER (page A-5)
USER AIDS MENU
HELP
Tutorial
Scoring Aids
GENERATE A REPORT (page A-3)
STOP

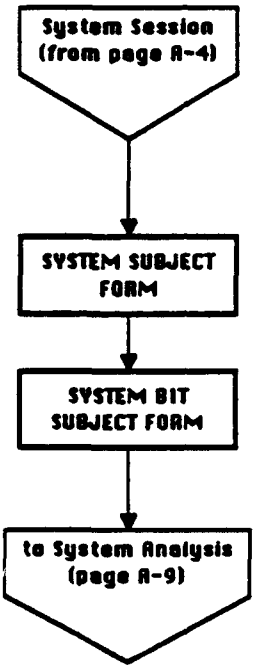

Generate a Report
(from page A-2)
REPORTS
MENU
HELP
Standard
Report
Full Report
Hierarchical
Tree
Subject
Value Table
Exit to Main
Menu
(to page A-2)
Concerns/
Actions
Report
Old Part #
Rates
Failure
Rate Table
USER AIDS
REPORT MENU
HELP
Print Tutorial
Print Scoring
Aid

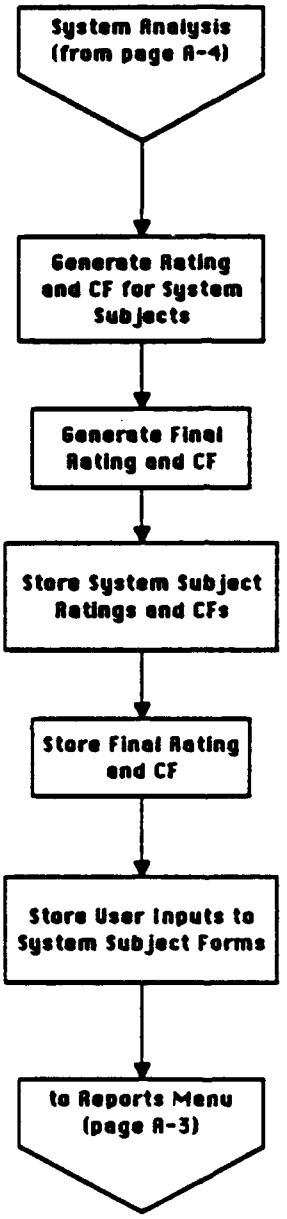

DESIGN ANALYSIS (from page A-2)
DESIGN ANALYSIS MENU
HELP
New Part Number
New Run for Old Part #
Edit an Old Run
Edit a Copy of an Old Run
Equipment Info
Choose Old Part Number
Choose Old Part Number and Run Number
Choose Old Part Number and Run Number
Set Run # to 1
Set Run #
RUN Info
Set Run #
RUN Info
Initialize Subject Forms to Defaults
Initialize Subject Forms to Defaults
Initialize User Responses to Old Data
Exit to MAIN MENU (page A-2)
TOP LEVEL SUBJECT FORM
UUT = MODULE ?
N
Y
MODULE SESSION (page A-6)
SYSTEM SESSION (page A-8)
MODULE ANALYSIS (page A-7)
SYSTEM ANALYSIS (page A-9)
To Reports Menu (page A-3)

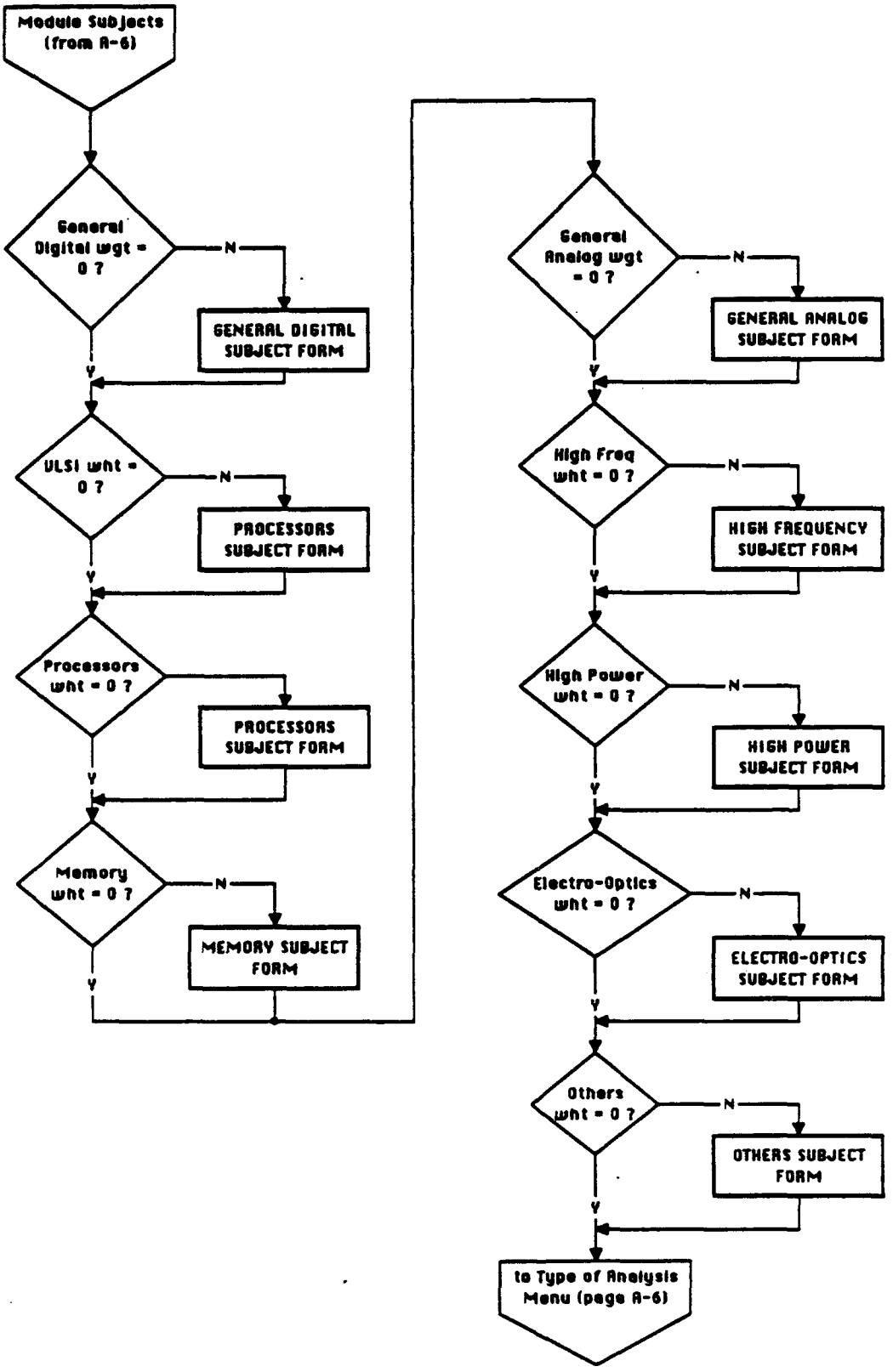

Data Manager
(from page A-2)
Enter
PASSWORD
PASSWORD
OK ?
N
Y
DATA MANAGER
MENU
HELP
Remove an
Old Run
Remove an
Old Part
Number
Compress
Data Base
Remove
Another ?
Remove
Another ?
Y
N
Y
N
Compress
Data ?
N
Y
Exit to MAIN
MENU (page A-2)
Compress
Data Base


Module Session (from A-4)
Analyze BIT ?
Y
N
BUILT-IN TEST (BIT) SUBJECT FORM
Analyze Scan ?
Y
N
SCAN SUBJECT FORM
TYPE OF ANALYSIS MENU
HELP
Functional Using the Fail. Rate Tbl.
Functional Using the Sub. Val. Tbl.
INCIRCUIT SUBJECT FORM
Quit Analysis
Finished - Analyze User Inputs
Init FRT to Defaults
Init FRT to Defaults
Confirm
Editing an Old Run ?
Editing an Old Run ?
Retrieve Old Entries
Retrieve Old Entries
to Module Analysis (page A-7)
Failure Rate Table Form
Subject Value Table Form
Exit to Main Menu (page A-2)
Generate Subject Weights
Generate Subject Weights
MODULE SUBJECTS (page A-10)


Module Analysis
(from page A-4)
Generate Rating and
Credibility Factor (CF) for
each Subject
Store Rating and CF
in Data Base
Generate Final
Rating and CF
Store Final Rating
and CF
Store User Inputs to
Subject Forms
to Reports Menu
(page A-3)


System Session
(from page A-4)
SYSTEM SUBJECT
FORM
SYSTEM BIT
SUBJECT FORM
to System Analysis
(page A-9)


System Analysis
(from page A-4)
Generate Rating
and CF for System
Subjects
Generate Final
Rating and CF
Store System Subject
Ratings and CFs
Store Final Rating
and CF
Store User Inputs to
System Subject Forms
to Reports Menu
(page A-3)


Module Subjects (from A-6)
General Digital wgt = 0 ?
N
GENERAL DIGITAL SUBJECT FORM
Y
ULSI wht = 0 ?
N
PROCESSORS SUBJECT FORM
Y
Processors wht = 0 ?
PROCESSORS SUBJECT FORM
Y
Memory wht = 0 ?
N
MEMORY SUBJECT FORM
Y
General Analog wgt = 0 ?
N
GENERAL ANALOG SUBJECT FORM
Y
High Freq wht = 0 ?
N
HIGH FREQUENCY SUBJECT FORM
Y
High Power wht = 0 ?
N
HIGH POWER SUBJECT FORM
Y
Electro-Optics wht = 0 ?
N
ELECTRO-OPTICS SUBJECT FORM
Y
Others wht = 0 ?
N
OTHERS SUBJECT FORM
Y
to Type of Analysis Menu (page A-6)

APPENDIX B

PARAMETER LISTING

Subject: Top Level

Parameter Number: t251

Parameter:

Design finalized (not undergoing changes).

Concern:

Testability designed into a changing design may be worthless after a design undergoes later design changes. Clear documentation of changes and how they will affect the design testability need to be available.

Data Request:

Is the design finalized?

A Weight: 50 B Weight: 10

Action: N/A

Subject: Top Level

Parameter Number: t252

Parameter:

Testability technical requirements plan.

Concern:

A testability technical requirements plan includes testability requirements with their relative importance to each other.

Data Request:

Does a testability technical requirements plan exist?

A Weight: 40 B Weight: 0

Action: See sections 3.1 and 3.2

Subject: Top Level

Parameter Number: t253

Parameter:

Design documentation available.

Concern:

Documentation such as schematics, parts lists, memory maps, and applicable specifications (calibration and alignment) enable test personnel to understand the functions of a design more fully.

Data Request:

Is all design documentation available?

A Weight: 50 B Weight: 10

Action: See sections 2.1.1 and 3.4.7

Subject: Top Level

Parameter Number: t254

Parameter:

Typical failure mode specification available.

Concern:

A typical failure mode specification allows complex faults to be traced quickly.

Data Request:

Is a typical failure mode specification available?

A Weight: 10 B Weight: 0

Action: See section 2.1.1.9

Subject: Top Level

Parameter Number: t255

Parameter:

Use of unavailable parts.

Concern:

Use of unavailable (obsolete) parts greatly complicates test development and testing a design because of lack of documentation and parts.

Data Request:

Are only available or non-obsolete parts used in the design?

A Weight: 35 B Weight: 0

Action: See section 2.2

Subject: Top Level

Parameter Number: t256

Parameter:

All critical measurements flagged and critical timing diagrams supplied with documentation package.

Concern:

Identifying critical measurements and critical timing diagrams save the test engineer considerable time and effort otherwise needed to understand the critical signal functions and relationships.

Data Request:

Are all critical signals and timing diagrams available?

A Weight: 45 **B Weight:** 4

Action: See section 2.1.1.2

Subject: Top Level

Parameter Number: t257

Parameter:

Testing time an insignificant part of design total expected lifetime.

Concern:

Occasionally a design may only have a total "mission" time of a few minutes or a few hours. Testing one of these designs for an hour or longer may degrade total lifetime.

Data Request:

Is the testing time less than 5% of the total expected life of the design?

A Weight: 25 B Weight: 0

Action: N/A

Subject: Top Level

Parameter Number: t258

Parameter:

Test procedure/diagram inter-sheet connections marked with consistent signal names and page reference designators.

Concern:

Calling the same signal by several names complicates test program development. Also, if page reference designators do not exist, schematics and other diagrams are difficult to read.

Data Request:

Are consistent names used for signals in all diagrams and documentation with page ref. designators?

A Weight: 30 B Weight: 0

Action: See section 2.1.1.1

Subject: Top Level

Parameter Number: t259

Parameter:

Documentation on purpose and rational of testability features of the design included in the design package.

Concern:

In a UUT designed with testability features, documentation of required measurements and the design rational simplifies test development.

Data Request:

Are the purpose and rational of testability features of the design documented?

A Weight: 40 B Weight: 2

Action: See section 2.1.1.5

Subject: Top Level

Parameter Number: t260

Parameter:

Vertical testability concept used (similar test program used for depot and production testing).

Concern:

The concept of vertical testability is to use the same test program developed for factory production test in the depot. As a result, only one test program must be developed. Also, a factory test program usually undergoes frequent updates and improvements due to the quantity of designs tested.

Data Request:

Is the concept of vertical testability used in this design?

A Weight: 5 **B Weight:** 0

Action: See section 2.3

Subject: Top Level

Parameter Number: t261

Parameter:

Design complies with MIL-STD-2165.

Concern:

MIL-STD-2165 outlines general testability programs for electronic systems and equipments and should be a requirement for any avionic system.

Data Request:

Does the design comply with MIL-STD-2165?

A Weight: 20 **B Weight:** 0

Action: See section 3.3

Subject: Top Level

Parameter Number: t262

Parameter:

UUT contains voting circuitry for mission/personnel critical functions.

Concern:

"Voting circuitry" often exists in critical UUT functions to provide more reliable circuitry and fault tolerance.

Data Request:

Is voting circuitry employed in all critical functions?

A Weight: 15 **B Weight:** 0

Action: See section 4.8

Subject: System

Parameter Number: r001

Parameter:

Use of standard commercial electronic modules.

Concern:

Standard off-the-shelf commercially available electronic modules such as power supplies and controllers, are easy to interchange or replace.

Data Request 1:

Enter the number of standard electronic modules used.

Data Request 2:

Enter the total number of electronic modules used.

A Weight: 20 **B Weight:** 0

Action: N/A

Subject: System

Parameter Number: r002

Parameter:

Redundant elements independently testable.

Concern:

Often critical circuits will require redundant circuits for fault tolerance. The outputs of the redundant circuits feed a voting circuit that masks faults. Redundant circuits need to be independently tested so that a fault within a redundant circuit can be isolated to that circuit.

Data Request 1:

Enter the total number redundant circuits that can be individually tested.

Data Request 2:

Enter the total number of redundant circuits.

A Weight: 45 B Weight: 2

Action: See section 3.4.3

Subject: System

Parameter Number: r003

Parameter:

Number of different standard connector types.

Concern:

Avionic and ground systems incorporate "standard" connectors as a matter of course, but the number of "different" standard connectors should be kept low. The same connector type with different keying should be used wherever possible.

Data Request 1:

Enter the number of standard connectors used.

Data Request 2:

Enter the total number of connectors used.

A Weight: 35 B Weight: 0

Action: See sections 13.3.9 and 3.4.1

Subject: System

Parameter Number: r004

Parameter:

Direct access to system level address and data buses.

Concern:

Direct access to address/data buses is necessary for test equipment to read data directly from the system.

Data Request 1:

Enter the number of system level address and data buses accessible at a connector(s).

Data Request 2:

Enter the total number of system level address and data buses.

A Weight: 50 B Weight: 8

Action: See section 3.4.3

Subject: System

Parameter Number: r005

Parameter:

Use of standard communications signals between systems and subsystems.

Concern:

Using standard communication signals between systems and subsystems (such as 1553B) enable dissimilar systems and test equipment to communicate without using costly adapters.

Data Request 1:

Enter the number of standard communication buses in the system/subsystem.

Data Request 2:

Enter the total number of communication buses in the system/subsystem.

A Weight: 40 B Weight: 0

Action: See section 3.4.3

Subject: System

Parameter Number: r006

Parameter:

Critical nodes routed to a connector and are accessible during test.

Concern:

All system/subsystem critical nodes (and test points) need to be accessible at a connector during test to prevent the need for internal probing. These nodes assist in controlling or observing major system functions.

Data Request 1:

Enter the number of critical nodes that are accessible at a connector during test.

Data Request 2:

Enter the total number of critical nodes.

A Weight: 50 B Weight: 3

Action: See section 3.4.1

Subject: System

Parameter Number: r007

Parameter:

System level feedback loops controllable by test equipment.

Concern:

System level feedback loops need to be broken and controlled by test equipment to isolate faults to individual sections within the feedback loops.

Data Request 1:

Enter the number of controllable system level feedback loops.

Data Request 2:

Enter the total number of system level feedback loops.

A Weight: 50 B Weight: 6

Action: See section 3.4.7

Subject: System

Parameter Number: t001

Parameter:

Use of standard power (115 v, 60 Hz, +28 v, +/-15 v).

Concern:

Using standard power on avionic and ground systems, makes interconnection to test equipment easier, reducing test times and cost.

Data Request:

Is standard power used for this system/subsystem?

A Weight: 40 B Weight: 0

Action: See section 3.4.2

Subject: System

Parameter Number: t002

Parameter:

Automatic self calibration available.

Concern:

Automatic self calibration of system functions, especially government calibration standards, verifies the accuracy of system measurements and does not require external calibration equipment.

Data Request:

Does an automatic self calibration routine exist in the system/subsystem?

A Weight: 20 **B Weight:** 0

Action: N/A

Subject: System

Parameter Number: t003

Parameter:

Ability to replace power supply signal on power failure.

Concern:

On main power failures, a system should incorporate an emergency air powered generator or uninterruptible power supply to keep critical electronic circuits running (especially for airplane/missile platforms).

Data Request:

Is a system/subsystem uninterruptible power supply provided on a main power failure?

A Weight: 20 B Weight: 0

Action: See section 3.4.2

Subject: System

Parameter Number: t004

Parameter:

Use of a standard test and maintenance bus that is accessible through a test connector.

Concern:

"Standard" test and maintenance buses (such as IEEE-STD-1149.1) that are accessible through a test connector improve system controllability and observability and greatly simplify system troubleshooting.

Data Request:

Is a system/subsystem standard test and maintenance bus accessible through a connector?

A Weight: 50 B Weight: 3

Action: See section 3.4.3

Subject: System

Parameter Number: t005

Parameter:

Modular design of system (MIL STD-2076, AFLC/AFSCP 800-39, 3960-9A).

Concern:

Modular system design means that each subassembly is a functionally complete entity. If this were not the case then test equipment would need custom circuitry to simulate missing subassembly functions.

Data Request:

Is the system/subsystem designed in a modular approach?

A Weight: 40 B Weight: 0

Action: See section 3.4.5

Subject: System

Parameter Number: t006

Parameter:

Manual interactions required, such as "select at test".

Concern:

Manual system interactions such as select at test and manual adjustments tend to slow down system test, debug, and repair.

Data Request:

Are manual interactions unnecessary during test?

A Weight: 45 B Weight: 3

Action: See sections 13.1.1 and 3.4.5

Subject: System

Parameter Number: t007

Parameter:

Ability to replace subassemblies in less than 30 minutes without the use of special tools.

Concern:

Replacing subassemblies in < 30 minutes (without special tools) can help reduce test times and costs. Good design for repairability can achieve this (use fewer screws, 1/4 turn screws, and do not hard wire removable covers to the unit under test).

Data Request:

Can all system/subsystem subassemblies be replaced in less than 30 minutes?

A Weight: 10 B Weight: 0

Action: See section 3.4.5

Subject: System

Parameter Number: t008

Parameter:

Ground points accessible by an instrument ground clip.

Concern:

All systems/subsystems need good measurement instrument ground terminals on their structures. Otherwise, the ground reference of the system/subsystem and test equipment may vary.

Data Request:

Does the system/subsystem provide ground points for test instrument ground clips?

A Weight: 15 B Weight: 0

Action: See section 3.4.7

Subject: System

Parameter Number: t009

Parameter:

Test points and readouts in close proximity.

Concern:

During system test, test points for I/O and readouts should be in close proximity to each other so that one test engineer can run the entire test.

Data Request:

Are test points and readouts in close enough proximity so that one person can use both of them?

A Weight: 5 **B Weight:** 0

Action: See section 3.4.4

Subject: System

Parameter Number: t010

Parameter:

Access to fuses and transient protectors.

Concern:

Test times can be reduced when fusses, transient protectors (for lightening strikes), desiccants, etc. are quickly accessible without having to remove subassemblies or covers.

Data Request:

Are fuses and transient protectors accessible without removing subassemblies?

A Weight: 10 **B Weight:** 0

Action: See section 3.4.7

Subject: System

Parameter Number: t011

Parameter:

Subsystems mounted on drawer slides, extender racks, etc.

Concern:

Subsystems mounted on extender slides or extender racks provide much easier accessibility during integration, testing, debug, and repair (especially while the subsystem is in the system).

Data Request:

Is the subsystem(s) mounted on drawer slides or extender racks?

A Weight: 40 B Weight: 3

Action: See section 3.4.5

Subject: System

Parameter Number: t012

Parameter:

Cables clearly marked and keyed on both ends and middle.

Concern:

Systems/subsystems containing a dozen to hundreds of cables are difficult to integrate, test, debug, or repair without each end of all cables clearly marked (and keyed). Markings should include the connector number that it attaches to and a cable identification number.

Data Request:

Are all cables marked on both ends with the number of the mating connectors and a cable ID number?

A Weight: 40 B Weight: 1

Action: N/A

Subject: System

Parameter Number: t013

Parameter:

Ability to remove and replace cables in < 3 min.

Concern:

Removing and replacing cables in less than 3 minutes can be accomplished with good mechanical design of system hardware interconnects. Quick release cables and cable access can shorten the time required to remove and replace a cable.

Data Request:

Can all system/subsystem cables be removed and replaced in less than 3 minutes?

A Weight: 10 B Weight: 0

Action: See section 3.4.1

Subject: System

Parameter Number: t014

Parameter:

Empty card slots used for operational test points.

Concern:

There is no better way to gain access to a subsystem backplane than through an empty card slot, if any are available.

Data Request:

If empty card slots exist, are they used for access to operational test points?

A Weight: 5 B Weight: 0

Action: See section 3.4.7

Subject: System

Parameter Number: t015

Parameter:

Defeatable keying used on subsystem modules.

Concern:

Defeatable keying on subsystem connectors reduces the number of unique interface adapters needed for an automated test system.

Data Request:

Is defeatable keying used in subsystem modules?

A Weight: 35 B Weight: 0

Action: See section 3.4.1

Subject: System

Parameter Number: t016

Parameter:

Ability to trace cables in assembly visually.

Concern:

Visually inspecting and tracing all assembly cables rather than having hidden cables (cables behind other cables) enable a system and cable integrity check. It also aids in overall system integration and debug, providing quick access for manipulative actions.

Data Request:

Can all cables be traced in the system/subsystem visually?

A Weight: 10 B Weight: 0

Action: N/A

Subject: System

Parameter Number: t017

Parameter:

Ability to disconnect high power section and independently test other portion without interlock problem.

Concern:

Having the ability to disconnect a high power section from the rest of a system/subsystem while testing low power sections results in added test engineer safety.

Data Request:

Can the high power section(s) be disconnected from the system during test?

A Weight: 40 B Weight: 0

Action: See section 3.4.2

Subject: System

Parameter Number: t018

Parameter:

All subsystems marked with ID numbers, generic English identifiers, and location reference designators.

Concern:

Multiple subsystems within systems should be marked with ID numbers, generic English identifiers, and location reference designators. This makes proper location and connections of subsystems less confusing.

Data Request:

Are all subsystems marked with ID number, generic English identifiers, and location references?

A Weight: 35 B Weight: 0

Action: See section 3.4.5

Subject: System

Parameter Number: t019

Parameter:

Use of VLSI circuitry or fiber optic cables been to reduce the number of system interconnects.

Concern:

Faulty interconnects usually cause 40 to 90% of all system problems. VLSI and fiber-optic use can reduce the number of cables and interconnects needed in a system and thus reduce system fault possibilities.

Data Request:

Is VLSI or fiber optic circuitry employed in this design?

A Weight: 5 B Weight: 0

Action: See section 3.4.1

Subject: System

Parameter Number: t020

Parameter:

Critical control portions of the system contain redundant (fail safe) modules for fault tolerance.

Concern:

Redundant circuits used for critical system functions enable testing of off line redundant sections without interruption of the main functions.

Data Request:

Are redundant circuits employed in all critical system control portions?

A Weight: 20 B Weight: 0

Action: See section 3.4.3

Subject: System

Parameter Number: t021

Parameter:

System externally asynchronously initializable by using a "master" reset.

Concern:

Every system/subsystem must have the ability to be reset at any time either remotely or by a reset switch or push-button. This allows test equipment to initiate a reset, which will usually put the system/subsystem in a known state.

Data Request:

Can the system/subsystem be reset externally?

A Weight: 50 B Weight: 15

Action: See section 3.4.3

Subject: System

Parameter Number: t022

Parameter:

Ability to bypass system computer externally.

Concern:

If a system computer is faulty, then test equipment must have the ability to replace the computer signals to operate system tests.

Data Request:

Can test equipment signals bypass and replace the system computer?

A Weight: 50 B Weight: 10

Action: See section 3.4.3

Subject: System

Parameter Number: t023

Parameter:

Factory (non-deliverable) mock-up system available to simulate complex faults.

Concern:

Often inaccessible systems develop specific faults that cannot be diagnosed without access to an identical "non-flight" system or mock-up. The mock-up simulates the error and debugs the problem before a line of action can be recommended.

Data Request:

Is a factory mock-up system available to assist in complicated diagnostics?

A Weight: 10 B Weight: 0

Action: See section 3.4.7

Subject: System

Parameter Number: t024

Parameter:

System warm-up time before test commencement < 20 minutes.

Concern:

If system has to warm up for more than 20 minutes then test times will be relatively long.

Data Request:

Is the system warm-up time less than 20 minutes?

A Weight: 15 B Weight: 0

Action: See section 3.4.7

Subject: System

Parameter Number: t025

Parameter:

Ability to inspect and manipulate internal system modules or LRUs.

Concern:

Manipulating/inspecting internal system modules allows an operator to check for obvious faults before exhaustive testing or disassembly.

Data Request:

Are the internal system/subsystem modules/LRUs accessible for inspection and manipulations?

A Weight: 25 B Weight: 0

Action: See section 3.4.1

Subject: System

Parameter Number: t026

Parameter:

Standard test point impedance levels of 50, 75, 130 ohm, or > 1 megaohm.

Concern:

Incorporating standard impedance levels at test points enable test equipment to access them directly without additional impedance matching circuitry.

Data Request:

Are standard test point impedance levels used?

A Weight: 30 B Weight: 0

Action: See section 3.4.4

Subject: System

Parameter Number: t027

Parameter:

System/subsystem functionally independent.

Concern:

If a system/subsystem is not functionally independent, then test equipment must simulate or provide the missing functions.

Data Request:

Is the system(s)/subsystem(s) functionally independent?

A Weight: 30 B Weight: 0

Action: See section 3.4.7

Subject: System

Parameter Number: t028

Parameter:

System includes a "battle-short" override switch with audible/visual display for test engineer safety.

Concern:

Often systems will include a "battle short" switch, which allows a system to continue running despite catastrophic internal problems that can result in fires or explosions. Using an audible and visual display to warn test engineer that it has engaged, is absolutely necessary.

Data Request:

Does a "battle-short" override switch exist with an audible/visual alarm?

A Weight: 40 B Weight: 2

Action: See section 3.4.6

Subject: System

Parameter Number: t029

Parameter:

Code sequence necessary to activate any explosive circuitry in the system with a deactivation switch.

Concern:

Missiles, etc. contain self destruct mechanisms on adjustable time fuses. It is essential that these self-destruct sequences are only available through a special multi-sequence code to prevent accidental turn on during test.

Data Request:

If explosive circuitry exists, is a sequential code needed to activate the explosion?

A Weight: 50 B Weight: 30

Action: See section 3.4.6

Subject: System

Parameter Number: t030

Parameter:

System internally coated or filled with a solidifying gel or inert gas.

Concern:

Systems/subsystems filled with a gel or inert gas can greatly increase integration, test, debug, and repair times.

Data Request:

Is the system/subsystem free from any internal coating or internal fillings (gels, gases, etc.)?

A Weight: 40 B Weight: 0

Action: See section 3.4.7

Subject: System

Parameter Number: t031

Parameter:

System testing requires a laminar flow bench or a clean room.

Concern:

A laminar flow bench or a clean room (class 100 to 100,000) requirement complicates system integration, test, debug and repair. (Clean rooms have many hidden costs.) Systems can be designed to minimize or eliminate these requirements.

Data Request:

Can the system/subsystem be tested in a normal environment (not requiring a clean room, etc.)?

A Weight: 45 B Weight: 3

Action: See section 3.4.7

Subject: System

Parameter Number: t032

Parameter:

All hazards clearly marked and contain protective covers (toxic chemicals, gases, high power, radiation, etc.).

Concern:

Test engineer safety during test is the prime concern and outweighs all other testability requirements. Clearly marking hazardous or hazard emitting systems in English and international symbols and providing protective covers is only prudent.

Data Request:

Are all hazards in the system/subsystem clearly marked and include protective covers?

A Weight: 35 B Weight: 0

Action: See section 3.4.6

Subject: System

Parameter Number: t033

Parameter:

Test points include protection barriers/covers to help prevent contamination or moisture from entering system.

Concern:

System test points are susceptible to contamination if not protected by covers or a covering. Also, depending on contamination type, test points can become functionally useless with time reducing system testability.

Data Request:

Are all system/subsystem test points protected from contaminants by protective covers?

A Weight: 5 B Weight: 0

Action: See section 3.4.4

Subject: System

Parameter Number: t034

Parameter:

Higher order software language(s) employed to simplify operator/system interchange for testing and debug.

Concern:

Higher order software languages employed in a system make it much easier to integrate, test, and debug since test engineering is often familiar with them.

Data Request:

Are any high order software languages used in the system control port(s)?

A Weight: 30 B Weight: 0

Action: See section 3.4.3

Subject: System

Parameter Number: t035

Parameter:

Remote system used to provide a data link for remote diagnostics and maintenance.

Concern:

Using a standard like the ARINC Communications and Reporting System for remote diagnostics/maintenance requires less customized test equipment (especially for satellites, etc.).

Data Request:

If the system is remote, does a remote data link exist for test?

A Weight: 45 B Weight: 0

Action: See section 3.4.3

Subject: System

Parameter Number: t036

Parameter:

System contains fire/smoke detectors, fire control circuitry, or a sprinkler system.

Concern:

Fire/smoke detectors and sprinkler systems protect not only the system but also the test engineer during integration, test and debug.

Data Request:

Does the system contain fire/smoke detectors, fire control circuitry, and sprinkler system?

A Weight: 10 B Weight: 0

Action: See section 3.4.6

Subject: System

Parameter Number: t037

Parameter:

All weapons system interfaces comply with MIL-STD-1760.

Concern:

Many avionic platforms use MIL-STD-1760, including: B1-1, B-52, F-15, and F-16. It provides I/O standards including plug/connector socket and pin connection types, power levels, dual MIL-STD-1553B, data buses, and others. Use of MIL-STD-1760 ensures compatibility with USAF ATE.

Data Request:

If the design is a weapons system, does it conform to MIL- STD-1760?

A Weight: 25 B Weight: 0

Action: See section 3.4.7

Subject: System

Parameter Number: t038

Parameter:

Exhaustive system heating during test.

Concern:

Some systems heat up considerably during test and tests should not occur without auxiliary temperature monitors and cooling equipment available.

Data Request:

Is it unnecessary to cool the system while testing?

A Weight: 25 B Weight: 0

Action: See section 3.4.7

Subject: System

Parameter Number: t039

Parameter:

System software divided into common software modules/ structures for fault isolation by function.

Concern:

Dividing system software (s/w) into common s/w modules/ structures by system function can greatly enhance testability of individual functions for both s/w and hardware.

Data Request:

Is the system software divided into common software modules?

A Weight: 30 B Weight: 0

Action: See section 3.4.3

Subject: System

Parameter Number: t040

Parameter:

All system/subsystem specifications available, such as operators manuals and software flow diagrams.

Concern:

A total specification and documentation package needs to be available for maximum expediency of integrating, testing, debugging, and repairing systems.

Data Request:

Are all system/subsystem specifications available?

A Weight: 35 B Weight: 0

Action: See section 3.4.7

Subject: System

Parameter Number: t041

Parameter:

System "operator monitor" circuit supplied with visual and audible warnings when it is about to engage.

Concern:

Complex systems contain operator monitors to take evasive or other action if operator fails to respond in a given amount of time after warning. (Such situations arise in battle: approaching obstruction, altitude too low, etc.). Test engineers need to control "operator monitors".

Data Request:

If "operator monitors" exist, can they be externally controlled?

A Weight: 45 B Weight: 4

Action: See section 3.4.6

Subject: System BIT

Parameter Number: r051

Parameter:

Percent faults detected by built-in test (BIT).

Concern:

Like any test, BIT should detect as high a percent of possible faults as feasible. Estimate the percentage of faults detected by BIT.

Data Request 1:

Enter the number of faults detected by BIT.

Data Request 2:

Enter the total number of possible faults.

A Weight: 45 B Weight: 0

Action: See section 4.7

Subject: System BIT

Parameter Number: r052

Parameter:

Environmental data used to analyze if BIT failure occurred during an over-stressed condition.

Concern:

Many false alarms (fault report when system is healthy) occur due to environmental conditions. These conditions should be monitored. If BIT reports a fault, the environmental conditions can be checked for an over-stress state and, if so, ignore the fault report.

Data Request 1:

Enter the number of environmental conditions that are monitored (temperature, shock, etc.).

Data Request 2:

Enter the total number of environmental conditions that could affect the system/subsystem.

A Weight: 50 B Weight: 2

Action: See section 4.7.5

Subject: System BIT

Parameter Number: t051

Parameter:

Failure information recorded in memory device with the time it occurred.

Concern:

BIT failures should be recorded on a memory device with the time of occurrence. At least 20 failures should be able to be stored. This enables the maintenance equipment or personnel to make a knowledgeable repair decision based on the failure sequence, reoccurrences, etc.

Data Request:

Is failure information and the time of occurrence recorded in a memory device?

A Weight: 45 B Weight: 5

Action: See section 4.7.6.1

Subject: System BIT

Parameter Number: t052

Parameter:

BIT hierarchically structured (BIT circuitry used to test a level of configuration is resident on that level).

Concern:

In hierarchically structured BIT each level of configuration (module, LRU, subsystem, system) runs its own BIT and reports the results to a higher level. Therefore, test equipment can run the same built-in test on a subassembly that the system ran.

Data Request:

Is the system/subsystem BIT hierarchically structured?

A Weight: 45 B Weight: 3

Action: See section 4.8

Subject: System BIT

Parameter Number: t053

Parameter:

Standardized BIT architecture and algorithms.

Concern:

Use of standard BIT architecture and algorithms makes the BIT system easier to understand since they employ only a few standard concepts. Also, the standard architecture and algorithm development occurs only once but can be used in many places.

Data Request:

Are standard BIT architectures and algorithms used?

A Weight: 7 B Weight: 0

Action: See section 4.8

Subject: System BIT

Parameter Number: t054

Parameter:

Independent control and observability of fault tolerant voting circuitry for independent test of each redundancy.

Concern:

Fault tolerance circuits usually consist of multiple redundant circuits with outputs feeding a voting circuit. If a fault exists in one of the redundant circuits, it will be masked from appearing at an output. BIT should have a means of independently testing each redundant circuit.

Data Request:

Are all redundant circuits independently tested by BIT?

A Weight: 40 B Weight: 0

Action: See section 4.8

Subject: System BIT

Parameter Number: t055

Parameter:

On board BIT designed such that faulty BIT circuitry will give a fail indication.

Concern:

If a BIT hardware failure does not appear as a failure indication, then BIT may not be able to report a fault in functional circuitry.

Data Request:

Will a fault in BIT circuitry cause a fail indication?

A Weight: 45 B Weight: 3

Action: See section 4.8

Subject: System BIT

Parameter Number: t056

Parameter:

Visual fault indicators exist to report faults in the main fault reporting device(s).

Concern:

If the main fault reporting device fails, then that failure should be reported. For instance, if a CRT normally reports a fault but the CRT fails, then a light near the CRT should be used to identify the CRT failure.

Data Request:

Do visual fault indicators exist to report a failure in the main fault reporting device(s)?

A Weight: 40 B Weight: 3

Action: See section 4.8

Subject: System BIT

Parameter Number: t057

Parameter:

Subsystem level BIT control located on one board.

Concern:

If subsystem level BIT control circuitry is present on several boards, then isolation of faulty BIT control circuitry is difficult. If the BIT control circuitry exists on one board alone, then BIT failures can be isolated to that board.

Data Request:

Is the subsystem level BIT control circuitry located on one circuit board?

A Weight: 35 B Weight: 0

Action: See section 4.8

Subject: System BIT

Parameter Number: t058

Parameter:

Manuals have procedures for faults not covered by BIT (for example, system will not power-up).

Concern:

Maintenance manuals should include a section of repair or test actions for all faults not tested by BIT. For example, if a fault causes the system not to power-up, BIT cannot report the fault. A procedure should exist to instruct maintenance personnel in an action to take.

Data Request:

Do the system/subsystem maintenance manuals cover faults not covered by BIT?

A Weight: 40 B Weight: 2

Action: See section 4.8

Subject: System BIT

Parameter Number: t059

Parameter:

Use of a BIT building-block approach. (Verify all inputs to a function before testing the function).

Concern:

If several functions are dependent, then BIT should test the function that provides inputs to the others first and the function at the end of the chain last. This approach detects faults at their earliest stages and avoids reporting a fault in a later state/function due to a faulty input.

Data Request:

Is a BIT building block approach used?

A Weight: 15 B Weight: 0

Action: See section 4.8

Subject: System BIT

Parameter Number: t060

Parameter:

Self-test routines stored separately from functional firmware.

Concern:

Test routines should be separate from any functional routines so that a test routine alteration does not affect functional firmware.

Data Request:

Are all self-test routines stored separately from functional firmware?

A Weight: 10 B Weight: 0

Action: See section 4.8

Subject: System BIT

Parameter Number: t061

Parameter:

Failure rate contribution of BIT circuitry.

Concern:

The addition of BIT circuitry decreases a system's reliability since BIT failure rates increase the overall system failure rate. The failure rate of BIT circuitry should be much lower than the function tested so that it will not significantly impact system reliability.

Data Request:

Is the failure rate contribution of BIT circuitry less than 10% of the function being tested?

A Weight: 40 B Weight: 0

Action: See section 4.8

Subject: System BIT

Parameter Number: t062

Parameter:

Failure of BIT circuitry isolated from disrupting system operation.

Concern:

A failure in BIT circuitry should not disrupt system operation and the operability of the system.

Data Request:

Is a failure in BIT circuitry isolated from disrupting the system's normal operation?

A Weight: 40 B Weight: 0

Action: See section 4.0

Subject: System BIT

Parameter Number: t063

Parameter:

BIT threshold values incorporated in software or easily modified firmware.

Concern:

BIT parameters, such as threshold values, which are subject to frequent change, should be located in easy to modify firmware or software. Otherwise, modifications due to operational experience require extra time and maintenance.

Data Request:

Are all BIT threshold values subject to change located in software or easily modified firmware?

A Weight: 30 B Weight: 0

Action: See section 4.5.1

Subject: System BIT

Parameter Number: t064

Parameter:

Use of processing or filtering of BIT sensor data to minimize false alarms.

Concern:

Filtering or processing circuits can be used to analyze BIT fault reports and make a judgement if a report is real. They can be a statistical filter, bayesian processor, or a filter that requires "m" faults out of "n" reports. These help limit incorrect fault reports such as false alarms.

Data Request:

Is BIT data filtered or processed prior to reporting a fault?

A Weight: 45 B Weight: 3

Action: See section 4.7.6.2

Subject: System BIT

Parameter Number: t065

Parameter:

Device used to monitor processor activity (clock activity watchdog timer).

Concern:

Processors are often difficult to test and often used to control BIT of other circuits. A simple circuit can be used to monitor a processor and report a "no-activity" fault. This same signal can be used to reset the processor.

Data Request:

Is a processor activity monitoring device used?

A Weight: 35 B Weight: 0

Action: See section 4.8

Subject: System BIT

Parameter Number: t066

Parameter:

Results of BIT reported to the system operator and brought out to a connector for monitoring.

Concern:

All BIT faults should be brought to a connector that test equipment can access at the LRU and higher levels of configuration. Also, the system operator should receive a BIT fault report.

Data Request:

Are the BIT results reported to the system operator and also accessible at a connector?

A Weight: 25 B Weight: 0

Action: See sections 4.7.6.2 and 4.10

Subject: System BIT

Parameter Number: t067

Parameter:

BIT exercise I/O between lower levels of assembly (signals in cables).

Concern:

Interconnects and I/Os need to be tested by BIT. If BIT circuitry tests each LRU individually and does not test connections between LRUs, then tests will not cover many faults.

Data Request:

Does BIT exercise I/O between LRUs?

A Weight: 45 B Weight: 5

Action: See section 4.5.1

Subject: System BIT

Parameter Number: t068

Parameter:

Allocation of BIT capability to each item reflects the relative failure rate and criticality of the item.

Concern:

A properly completed Failure Modes and Effects Analyses (FMEA) can verify this parameter. The FMEA results should show if BIT was properly allocated. BIT circuitry is more important in critical areas and areas more likely to fail.

Data Request:

Is a function's/item's criticality and failure rate taken into account in BIT allocation?

A Weight: 10 B Weight: 0

Action: See section 4.7.1

Subject: System BIT

Parameter Number: t069

Parameter:

Ability to load system diagnostics into the system computer.

Concern:

Alterations to system diagnostic routines are very difficult unless a means of porting this data into the system exists, such as a floppy disk or tape drive.

Data Request:

Can the system computer externally load system diagnostics?

A Weight: 30 B Weight: 0

Action: See section 4.5.1

Subject: System BIT

Parameter Number: t070

Parameter:

Mechanical system conditions and battle damage monitoring functions integrated with general system BIT.

Concern:

The device used to report BIT failures to the operator also should report monitored physical parameters. Battle damage reports should be included in the BIT report. This will make analysis of the system's health by the operator more comprehensive.

Data Request:

Are system physical conditions reported with the BIT report?

A Weight: 20 B Weight: 0

Action: See section 4.2.1

Subject: System BIT

Parameter Number: t071

Parameter:

Built-in Self Test (BIST) runs on power-up and controllable by user manually without the use of external equipment.

Concern:

The system operator should have a simple means of initiating power-up BIST, such as a switch or button, without the use of external hardware. Otherwise, a simple BIST check may require cost and time to connect and operate external equipment to the system.

Data Request:

Is the built-in self test (BIST) controllable by a simple means, such as a button or switch?

A Weight: 30 B Weight: 0

Action: See section 4.6.1

Subject: System BIT

Parameter Number: t072

Parameter:

Ground maintenance BIT disabled when the system is operational.

Concern:

Ground maintenance BIT (initiated BIT) should be disabled while the system is operational. Otherwise, BIT could be initiated and interfere with a critical system function, such as a terrain following radar in an aircraft.

Data Request:

Is ground maintenance BIT disabled when the system is operating?

A Weight: 30 B Weight: 0

Action: See section 4.8

Subject: System BIT

Parameter Number: t073

Parameter:

Next lower level of assembly average ambiguity group size for BIT failure report.

Concern:

The size of an ambiguity group directly affects the Mean Time to Repair (MTTR) a system. The ideal size of an ambiguity group for an LRU fault is one Shop Replaceable Unit (SRU).

Data Request:

Does the BIT isolate to 1 item more than 90% of the time?

A Weight: 45 B Weight: 1

Action: See section 4.8

Subject: System BIT

Parameter Number: t074

Parameter:

Manual calibration of BIT circuitry.

Concern:

Manual calibration of BIT circuitry requires error prone manual actions to be taken. Also, it complicates and slows down BIT.

Data Request:

Is manual calibration of BIT circuitry unnecessary?

A Weight: 20 B Weight: 0

Action: See section 4.8

Subject: System BIT

Parameter Number: t075

Parameter:

BIT test itself (residue codes, checksum of firmware, etc.).

Concern:

If BIT circuitry fails, it is unable to detect a functional fault. Therefore, BIT hardware needs to be checked by BIT before testing functional circuitry.

Data Request:

Does the BIT circuitry test itself before it tests any functional hardware?

A Weight: 20 B Weight: 0

Action: See section 4.8

Subject: System BIT

Parameter Number: t076

Parameter:

System/subsystem contains a lamp check button.

Concern:

In order to verify any lamps in a system, a button(s) or switch(s) should exist that can turn on the lamps for visual inspection.

Data Request:

Does a lamp check button exist to test each lamp in the system/subsystem?

A Weight: 5 B Weight: 0

Action: See section 4.8

Subject: System BIT

Parameter Number: t077

Parameter:

All system critical faults sent to operator's "head-up display"?

Concern:

Critical faults usually require immediate decisions and the operator should be informed via a "head-up display".

Data Request:

Are all critical faults sent to the operator's "head-up display"?

A Weight: 20 B Weight: 0

Action: See section 4.8

Subject: System BIT

Parameter Number: t078

Parameter:

"Safe-to-turn-on" interlocks provided for all high power sections.

Concern:

High power portions of a design require interlocks to guarantee that potential system hazards are not present. For instance, an interlock should initiate if a cooling system fails.

Data Request:

Do "safe-to-turn-on" interlocks exist at all high power sections of the system/subsystem?

A Weight: 10 B Weight: 0

Action: See sections 4.8 and 14

Subject: Module

Parameter Number: r651

Parameter:

Percent nodes accessible for probing (for hermetic hybrid-access to open package).

Concern:

Ideally every function node on a module should be accessible for manual probing during test and diagnostics. This simplifies fault isolation using a manual probe.

Data Request 1:

Enter the number of nodes that are accessible for probing.

Data Request 2:

Enter the total number of nodes on the module.

A Weight: 50 B Weight: 0

Action: See section 5.3

Subject: Module

Parameter Number: r652

Parameter:

Percent nodes accessible at a connector or module lead.

Concern:

Nodes that are accessible at a connector or module lead can be connected directly to a test fixture and not require manual probing. The greater the percent of nodes on connectors or leads the more automated a test can be.

Data Request 1:

Enter the number of nodes that are accessible at a connector or module lead.

Data Request 2:

Enter the total number of nodes on the module.

A Weight: 45 B Weight: 0

Action: See section 5.3

Subject: Module

Parameter Number: r653

Parameter:

Number of complex external feedback loops (feedback loops completed through another module).

Concern:

If a module requires the connection of complex feedback loops, then ATE must imitate the feedback loops during test.

Data Request 1:

Enter the total number of module external feedback loops that are required during test.

Data Request 2:

Enter the total number of module external feedback loops.

A Weight: 50 B Weight: 5

Action: See section 5.1.1.2

Subject: Module

Parameter Number: r654

Parameter:

Number of sequential devices.

Concern:

In general, sequential devices are more difficult to test than combinational devices. Steps need to be taken to initialize sequential devices and sequential device test vectors are difficult to generate.

Data Request 1:

Enter the number of sequential devices that are fully tested with BIT.

Data Request 2:

Enter the total number of sequential devices.

A Weight: 30 B Weight: 0

Action: See section 5.1.2

Subject: module

Parameter Number: r655

Parameter:

Control of oscillators.

Concern:

Oscillators that are not controllable force test equipment to synchronize to the oscillator signal. This is difficult and the test equipment may not even be able to operate at the oscillator frequency.

Data Request 1:

Enter the number of oscillators that are controllable and replaceable by an external ATE signal.

Data Request 2:

Enter the total number of oscillators on the module.

A Weight: 50 B Weight: 10

Action: See Sections 5.1.8 and 7.4.2

Subject: module

Parameter Number: r656

Parameter:

Control of internal module feedback loops.

Concern:

Faulty devices within a feedback loop are impossible to isolate without being able to break the feedback loop.

Data Request 1:

Enter the number of breakable feedback loops on the module.

Data Request 2:

Enter the total number of feedback loops on the module.

A Weight: 48 B Weight: 8

Action: See Sections 5.1.1.1 and 7.4.4

Subject: Module

Parameter Number: t651

Parameter:

Component IDs ('U' numbers) visible on component side (marked on board or device) and solder side of board.

Concern:

Component IDs on the component side of a board provide quick and easy device location during test diagnostics and test development. Component IDs on the solder side of a board enable easy device pin location while debugging fixture contact problems and manual probing.

Data Request:

Are component IDs marked on the solder and component sides of the module?

A Weight: 25 B Weight: 0

Action: See section 5.2.2

Subject: Module

Parameter Number: t652

Parameter:

Pin 1 of each device and connector visibly marked on components or boards.

Concern:

A pin one reference should exist for each device and connector to simplify locating a pin during test development, test, and diagnostics. Also, connectors should be marked every ten pins to ease locating pins.

Data Request:

Is pin 1 of each device and connector identified on the module or components?

A Weight: 35 B Weight: 0

Action: See section 5.2.2

Subject: Module

Parameter Number: t653

Parameter:

Use of standard connector(s).

Concern:

Non-standard connectors are more difficult to procure and manufacture than standard ones.

Data Request:

Are all connectors used, standard connector types?

A Weight: 20 B Weight: 0

Action: See section 5.2.3

Subject: Module

Parameter Number: t654

Parameter:

Spacing of connectors >250 mils apart to allow easy connection.

Concern:

Placing connectors too close to each other makes connecting a test fixture to the module unnecessarily difficult.

Data Request:

Are all connectors spaced more than 250 mils from other connectors or module extrusions?

A Weight: 20 B Weight: 0

Action: See section 5.2.3

Subject: Module

Parameter Number: t655

Parameter:

Undefined logic states.

Concern:

All logic states of a design should be tested. If any undefined states exist, then the output response to these states cannot be determined and as a result, cannot be tested.

Data Request:

Are all outputs and internal states in the module defined?

A Weight: 45 B Weight: 8

Action: N/A

Subject: Module

Parameter Number: t656

Parameter:

Use of wired-OR or wired-AND circuitry.

Concern:

Wired-OR and -AND circuitry often leads to ambiguity groups of every device that is wired-OR or -AND. A better approach is to use a multiple input AND or OR gate device.

Data Request:

Is the module free from the use of wired-OR or AND circuitry?

A Weight: 30 B Weight: 0

Action: See section 5.1.6

Subject: Module

Parameter Number: t657

Parameter:

All redundant elements independently testable.

Concern:

Fault tolerant designs often use redundant circuits. If a fault occurs in a redundant circuit, a voting circuit masks it from appearing at an output. If a redundant circuit is faulty and each redundant element cannot be tested independently, then the fault cannot be determined.

Data Request:

Are all redundant circuits in the module independently testable?

A Weight: 40 B Weight: 0

Action: See section 5.1.5

Subject: Module

Parameter Number: t658

Parameter:

Test points adequately buffered or isolated from the main signal path.

Concern:

Test points should be protected from accidental shorts to power or ground by a test technician. A short of a test point to power or ground could cause damage to module devices. A few simple mechanisms to achieve this are: buffers, isolators, couplers, and diodes.

Data Request:

Are all test points isolated from the main signal paths?

A Weight: 20 B Weight: 0

Action: See section 5.1.4

Subject: Module

Parameter Number: t659

Parameter:

Multiple phase related or time related signals.

Concern:

Sophisticated and costly test equipment is required to supply or monitor complex signals (multiple phase or time related).

Data Request:

Are all signals that need to be supplied or monitored by the test equipment non-complex?

A Weight: 45 **B Weight:** 5

Action: See section 5.1.3

Subject: Module

Parameter Number: t660

Parameter:

Use of nominal or select-at-test components.

Concern:

The use of nominal or select-at-test components require operator intervention, which is fault prone. Such components should be avoided.

Data Request:

Is the module free from the use of nominal and select-at-test components?

A Weight: 45 B Weight: 5

Action: See sections 5.6 and 12.1.5

Subject: Module

Parameter Number: t661

Parameter:

Standard connector and pin positions used for power, ground, and clock signals.

Concern:

All modules tested from an LRU should use the same standard power, ground, and clock signal pins. This allows several modules to be tested on the same fixture connector if each module uses a standard connector.

Data Request:

Are standard module connector and pin locations used for power, ground, and clock signals?

A Weight: 35 B Weight: 0

Action: See section 5.2.3

Subject: Module

Parameter Number: t662

Parameter:

Components oriented in the same direction. (Pin 1 in same position for each device).

Concern:

It is easier to identify component pins if all components have pin #1 oriented in the same direction. A standard orientation is for pin 1 to be at the top left corner of each device.

Data Request:

Are all components oriented with pin #1 in the same position?

A Weight: 10 B Weight: 0

Action: See section 5.2.2

Subject: Module

Parameter Number: t663

Parameter:

Special setup requirements (warm-up time > 10 minutes, cooling, etc.)

Concern:

Cooling, heating, gas flow, and other design requirements complicate test equipment and increases test equipment costs.

Data Request:

Are special setup requirements unnecessary, such as heating, cooling, and warm-up times?

A Weight: 30 B Weight: 0

Action: See section 5.5

Subject: Module

Parameter Number: t664

Parameter:

Each function placed wholly on the board (including bias voltages and pull-ups).

Concern:

All functions on a module should be complete, not requiring bias voltages, pull-up resistors, or any other circuitry needed for the function to operate properly. Otherwise, the test equipment or an adapter has to provide this circuitry.

Data Request:

Are all functions on the module complete?

A Weight: 15 B Weight: 0

Action: See section 5.1.7

Subject: Module

Parameter Number: t665

Parameter:

Components listed by their generic part numbers in module documentation.

Concern:

All components should be identified by their generic part numbers on themselves, the module, or in module documentation. Component documentation is easy to obtain for standard parts using the generic part numbers.

Data Request:

Are the module components listed by their generic part numbers?

A Weight: 5 B Weight: 0

Action: See section 5.2.2

Subject: Module

Parameter Number: t666

Parameter:

Devices that are very difficult to remove.

Concern:

Some devices are very difficult to remove and module expected to undergo repairs frequently should not use them. Some examples are: Chip on Board (COB) technology, Tape Automated Bonding (TAB), and thermally bonded devices.

Data Request:

Are all the devices removable?

A Weight: 30 B Weight: 0

Action: See section 5.2.1

Subject: Module

Parameter Number: t667

Parameter:

Test vectors provided for all custom devices.

Concern:

If test vectors do not exist for a custom device, then a custom device test usually needs to be manually generated by a test engineer. The test engineer usually will not be familiar with the device. It could take many weeks to generate test vectors for a custom VLSI chip.

Data Request:

Do test vectors exist for all custom devices on the module?

A Weight: 45 B Weight: 10

Action: N/A

Subject: Module

Parameter Number: t668

Parameter:

Module ID resistor.

Concern:

Before initiating a test sequence on a module, it is desirable to verify that the correct module is mounted on the test fixture. This can be done by checking an identifying resistor (unique for each similar design) prior to power up.

Data Request:

Does the module have an ID resistor?

A Weight: 5 B Weight: 0

Action: See section 5.4

Subject: BIT

Parameter Number: r751

Parameter:

Number of VLSI/ASIC/microprocessors with BIT controllable by automated test equipment (ATE).

Concern:

Complex devices, such as a VLSIs, ASICs, and microprocessors are difficult to test. If Built-in Test (BIT) exists for any of these devices then it can be used in module test and ease the test program development task.

Data Request 1:

Enter the number of VLSI, ASIC, & processors with BIT controllable and observable by ATE.

Data Request 2:

Enter the total number of VLSI, ASIC, & processor devices.

A Weight: 50 B Weight: 2

Action: N/A

Subject: BIT

Parameter Number: r752

Parameter:

Thoroughness of BIT.

Concern:

BIT or Built-in Self Test (BIST) can be used to aid in module testing. However, the effectiveness of running any BIT test is dependent on the thoroughness of the BIT test - % pin faults detected. A pin fault is the inability of the pin to change from a high to low or a low to high signal state.

Data Request 1:

Estimate the number of device pin faults detected by BIT.

Data Request 2:

Enter the total number of device pin faults (two possible pin faults per pin).

A Weight: 50 B Weight: 0

Action: N/A

Subject: BIT

Parameter Number: r753

Parameter:

Amount of sequential logic (applicable to BIT using signature analysis only).

Concern:

In order to propagate test data through sequential circuitry a series of dependent vectors needs to be input to it. During signature analysis, input test vectors are random and independent. Therefore, it is very difficult to propagate random data through sequential circuits.

Data Request 1:

Enter the number of devices with < 8 sequential states that are analyzed by signature analysis.

Data Request 2:

Enter the total number of devices that are analyzed by signature analysis.

A Weight: 40 B Weight: 3

Action: See section 6.2.2

Subject: BIT

Parameter Number: r754

Parameter:

High power supply voltages monitored by BIT.

Concern:

Any module driving or receiving high voltage or current should have continuous BIT monitoring the signal that will shut down the driver/receiver after detecting a fault. Otherwise, damage to circuits receiving the signal is possible if the signal driver fails.

Data Request 1:

Enter the number of high power supply voltages that are monitored & disabled by BIT on a fault.

Data Request 2:

Enter the total number of high power supply voltages.

A Weight: 35 B Weight: 0

Action: See section 6.3.1

Subject: BIT

Parameter Number: t751

Parameter:

On-board BIT control processor used to exercises and report BIT.

Concern:

An on-board BIT control processor enables ATE to exercise the same BIT that a higher level configuration may run, which helps limit false alarms. Often, it enables at-speed BIT (testers usually cannot test at-speed).

Data Request:

Does an on-board BIT control processor exist that can be controlled by ATE?

A Weight: 30 **B Weight:** 0

Action: See section 6.1.3

Subject: BIT

Parameter Number: t752

Parameter:

BIT controllable/observable at a connector.

Concern:

In order for test equipment to make use of BIT circuitry, the BIT control circuitry must be accessible by the test equipment at a connector.

Data Request:

Is the BIT circuitry controllable and observable at the connector(s)?

A Weight: 50 B Weight: 20

Action: N/A

Subject: BIT

Parameter Number: t753

Parameter:

Failure rate of BIT circuitry does not increase the failure rate of the tested function.

Concern:

The addition of BIT circuitry to a design increases the failure rate of the design due to the BIT circuitry failure rate contribution. Therefore, if BIT circuitry significantly increases the failure rate of a design, the design will be more apt to fail due to the BIT circuitry.

Data Request:

Is the BIT circuitry failure rate less than 10% of the failure rate of the tested function?

A Weight: 45 B Weight: 2

Action: See section 6.4

Subject: BIT

Parameter Number: t754

Parameter:

Ability to execute portions of BIT.

Concern:

The ability to operate portions of BIT independently simplifies fault isolation and test program development. This is similar to partitioning.

Data Request:

Can the module BIT be executed in functional portions?

A Weight: 20 B Weight: 0

Action: See section 6.1.3

Subject: BIT

Parameter Number: t755

Parameter:

Allocation of BIT to each item reflect the relative failure rate and criticality of each item's function.

Concern:

Critical functions and circuits with high failure rates should have more BIT circuitry allocated to them as compared with non-critical low failure rate functions.

Data Request:

Does the allocation of BIT reflect the relative failure rates and criticality of each item?

A Weight: 15 B Weight: 0

Action: See section 6.4

Subject: BIT

Parameter Number: t756

Parameter:

BIT circuitry or failure of BIT circuitry interfere with main operational functions.

Concern:

If BIT circuitry fails, then that failure should not disrupt any functional operations. A simple method of achieving this is to isolate signals monitored by BIT.

Data Request:

Is the failure of BIT circuitry isolated from interfering with any main functional operations?

A Weight: 40 B Weight: 2

Action: See section 6.1.3

Subject: BIT

Parameter Number: t757

Parameter:

Average size of BIT ambiguity group.

Concern:

Smaller BIT ambiguity groups require fewer diagnostic tests to isolate a fault to one or several components. If a BIT ambiguity group is very large, then it is only useful in determining that a fault exists and cannot aid in fault isolation.

Data Request:

Is the average size of a BIT failure ambiguity group less than 5 devices?

A Weight: 45 B Weight: 8

Action: N/A

Subject: BIT

Parameter Number: t758

Parameter:

Time needed to run BIT.

Concern:

Excessive time needed to run BIT (> 3 minutes) increases the Mean Time to Repair (MTTR) and slows down production test.

Data Request:

Is the time required to run BIT less than 3 minutes?

A Weight: 15 B Weight: 0

Action: See section 6.1.3

Subject: BIT

Parameter Number: t759

Parameter:

Ability of BIT to report multiple faults.

Concern:

Modules with multiple faults need to go through the test and repair cycle several times if multiple fault reporting does not exist.

Data Request:

Can multiple faults be detected and reported by BIT?

A Weight: 20 B Weight: 0

Action: N/A

Subject: BIT

Parameter Number: t760

Parameter:

BIT check itself before checking functional circuitry.

Concern:

BIT should be able to check itself before testing a function so that faulty BIT circuitry will not incorrectly report a functional circuitry fault.

Data Request:

Does BIT circuitry perform a self-test of itself before checking functional circuitry?

A Weight: 30 B Weight: 0

Action: See section 6.5

Subject: BIT

Parameter Number: t761

Parameter:

Coding schemes used in transmission and storage of data (hamming codes, residue codes, syndrome word, etc.)

Concern:

Coding schemes can be used to test data transmission and storage errors.

Data Request:

Are coding schemes used to test data transmission and storage?

A Weight: 30 B Weight: 0

Action: See section 6.2.4

Subject: BIT

Parameter Number: t762

Parameter:

Fault in BIT circuitry observed and reported as a fault.

Concern:

A fault within BIT circuitry should be propagated as a fault. Otherwise, BIT circuitry may not have the ability to report a fault when one occurs or it may report a fault in functioning circuitry.

Data Request:

Is a fault within the BIT circuitry observed and reported as a fault?

A Weight: 45 B Weight: 8

Action: See section 6.1.3

Subject: BIT

Parameter Number: t763

Parameter:

Deterministic module outputs for circuitry tested by BIT signature analysis.

Concern:

During signature analysis, vectors (usually random) are input to circuitry and the responses compressed into a word. This word is validated against a known correct signature. If outputs are not deterministic, then a functional circuit may have several signatures and make analysis impossible.

Data Request:

If signature analysis is used, are all outputs analyzed deterministic?

A Weight: 45 B Weight: 20

Action: See section 6.2.2

Subject: BIT

Parameter Number: t764

Parameter:

Fan-in circuitry count (for circuits analyzed by signature analysis only).

Concern:

High fan-in circuits are difficult to test with random number inputs and should be divided. An example of a problem fan-in circuit would be a 20 input AND gate. When testing this gate with random patterns, the chances of outputting a logic ONE are 1 to 2E-20 or 1 to 1 million.

Data Request:

If signature analysis is used, do all circuits analyzed have fan-ins of less than 6?

A Weight: 30 B Weight: 0

Action: N/A

Subject: BIT

Parameter Number: t765

Parameter:

Use of modularized BIT "building-blocks" for like functions.

Concern:

In modularized BIT, the design of BIT circuits such as envelope detectors, gated video buffers and video detectors, only occurs once as a BIT "module" and can be used repeatedly.

Data Request:

Are BIT "building blocks" used for similar functions?

A Weight: 5 B Weight: 0

Action: N/A

Subject: BIT

Parameter Number: t766

Parameter:

Fault indicators shielded from noise.

Concern:

Noise spikes often trigger unprotected BIT circuitry through some form of cross coupling causing false BIT error reports. Using sufficient detection delay circuitry greatly reduces the amount of false BIT signals due to these problems.

Data Request:

Are BIT fault indicators shielded from noise?

A Weight: 15 B Weight: 0

Actior: See section 6.3

Subject: BIT

Parameter Number: t767

Parameter:

Design contains BIT LEDs to identify the presence or absence of critical voltages.

Concern:

LEDs used as BIT to show the absence or presence of critical voltages in a design greatly decreases test and debug times. They give a quick overview of where faults may exist.

Data Request:

Does the module have BIT LEDs to display presence or absence of critical voltages?

A Weight: 15 B Weight: 0

Action: See section 6.1.3

Subject: BIT

Parameter Number: t768

Parameter:

BIT protection for UUT power-on and power-off.

Concern:

Many designs are protected with power-on circuitry. However, during power-off, faults can still occur due to stored charges or noise cross coupled from adjacent modules. BIT circuitry to critical main circuit functions may need battery back-up to continue monitoring during power-off.

Data Request:

Has the module been designed with BIT protection for power-on and power-off situations?

A Weight: 5 B Weight: 0

Action: N/A

Subject: General Digital

Parameter Number: r101

Parameter:

Control of module initialization.

Concern:

Control of initialization (setting a starting state or value) for general digital modules is necessary prior to testing. It allows a module to be put into a known state or starting point before applying test vectors. Without this control, modules cannot be tested for repeatability.

Data Request 1:

Enter the number of sequential devices that can be initialized from a connector.

Data Request 2:

Enter the total number of sequential devices.

A Weight: 45 B Weight: 5

Action: See section 7.1

Subject: General Digital

Parameter Number: r102

Parameter:

Control of device tri-state and enable lines.

Concern:

Control of tri-state and enable lines of a device allow the device to be disabled during the testing of other devices. Therefore, devices on a bus that are tri-stateable can be individually tested while tri-stating the other devices.

Data Request 1:

Enter the number of devices with outputs that can be disabled from a connector.

Data Request 2:

Enter the total number of devices with tri-state outputs on the module.

A Weight: 40 B Weight: 1

Action: See section 7.4.3.3

Subject: General Digital

Parameter Number: r103

Parameter:

Control of set/reset/halt logic lines.

Concern:

Control of set/reset and halt lines in general digital devices allows test equipment to end a given test and set up for a new one.

Data Request 1:

Enter the number of set/reset, and halt lines controllable from a connector.

Data Request 2:

Enter the total number of set/reset and halt lines used on the module.

A Weight: 50 B Weight: 2

Action: See section 7.1.3

Subject: General Digital

Parameter Number: r104

Parameter:

Glue logic node accessibility.

Concern:

Glue logic refers to Small Scale Integration (SSI) devices between Large or Very large Scale Integration devices (LSI & VLSI). Access to glue logic nodes simplifies testing. Otherwise, test signal would have to travel though the LSI and VLSI devices during glue logic test.

Data Request 1:

Enter the number of glue logic signals that are accessible from a connector.

Data Request 2:

Enter the total number of glue logic signals.

A Weight: 40 B Weight: 0

Action: See section 7.2

Subject: General Digital

Parameter Number: r105

Parameter:

Control of asynchronous devices (such as monostables/"one-shots").

Concern:

When asynchronous devices (pulse generators, one shots, etc.) must be used in a module, their outputs must be controllable by Automatic Test Equipment (ATE). Otherwise, testing these devices is very difficult.

Data Request 1:

Enter the number of asynchronous devices controllable from a connector.

Data Request 2:

Enter the total number of asynchronous devices.

A Weight: 40 B Weight: 3

Action: See section 7.4.8

Subject: General Digital

Parameter Number: r106

Parameter:

Breakup of long sequential logic chains (counters, etc.).

Concern:

Sequential devices are considered more difficult to test than combinational devices. Long sequential chains should be divided into several smaller chains during test. Unbroken chains require long test patterns and should be avoided.

Data Request 1:

Enter the number of sequential devices that can be tested in sequential chains of 4 or less.

Data Request 2:

Enter the total number of sequential chains.

A Weight: 50 B Weight: 3

Action: See sections 7.4.6 and 7.2.1

Subject: General Digital

Parameter Number: t101

Parameter:

Number of technologies used.

Concern:

Most technologies (TTL, ECL, CMOS, etc.) have different input and output signal characteristics, such as output signal levels. A tester must be able to supply and monitor signal levels for each technology resident on a module. Therefore, tester requirements increase with technology count.

Data Request:

Are three (3) or fewer technologies used on the module?

A Weight: 5 B Weight: 0

Action: See section 7.4.3.1

Subject: General Digital

Parameter Number: t102

Parameter:

UUT functionally partitioned.

Concern:

Partitioning simplifies testing and trouble shooting by dividing a circuit's complexity into several smaller less complex circuits during test.

Data Request:

Are sections of the module partitioned or functionally separated?

A Weight: 45 B Weight: 3

Action: See section 7.4.5

Subject: General Digital

Parameter Number: t103

Parameter:

Number of supply voltages required.

Concern:

Each supply voltage required for a module must be provided by power supplies in the test equipment during test. As a result, the test equipment and adapter(s) requirements for a module increase with the number of supply voltages needed by the module.

Data Request:

Are less than four (4) supply voltages required for the module?

A Weight: 10 B Weight: 0

Action: N/A

Subject: General Digital

Parameter Number: t104

Parameter:

Complex timing signals/relationships required (rise times, propagation delays, etc.).

Concern:

Complex timing relationships designed into in a module increase the time to develop a test program and usually require costly test equipment capable of making timing related measurements.

Data Request:

Is the design free from signals dependent on timing relationships?

A Weight: 40 B Weight: 5

Action: See section 5.1.3

Subject: General Digital

Parameter Number: t105

Parameter:

Use of multilevel logic.

Concern:

Multilevel logic devices have more than two logic level states. Multilevel logic causes reduced noise immunity due to tighter tolerances on more than two thresholds.

Data Request:

Is the module free from the use of multilevel logic?

A Weight: 15 B Weight: 0

Action: N/A

Subject: General Digital

Parameter Number: t106

Parameter:

Use of asynchronous circuits.

Concern:

Asynchronous devices are difficult to control and test and should be avoided.

Data Request:

Is the design free from the use of asynchronous circuits?

A Weight: 40 B Weight: 2

Action: See section 7.6.8

Subject: General Digital

Parameter Number: t107

Parameter:

Unused logic input gates tied high or low.
(Not applicable for ECL devices).

Concern:

Non terminated or floating unused logic inputs for TTL introduce noise into module circuitry if not held to a high or low state. ECL devices are an exception.

Data Request:

Are all unused devices inputs tied high or low?

A Weight: 10 B Weight: 0

Action: See section 7.4.3.4

Subject: General Digital

Parameter Number: t108

Parameter:

Ambiguity groups of functions contained in the same package.

Concern:

For multi-device IC packages, same devices in an ambiguity group should be located in the same IC package. If an ambiguity group fails then only one IC package needs to be replaced for the same devices in the ambiguity group.

Data Request:

Do all equivalent devices in each ambiguity group exist in one multi-device IC?

A Weight: 5 **B Weight:** 0

Action: See section 7.4.5.2

Subject: General Digital

Parameter Number: t109

Parameter:

Use of discrete transistors for digital logic implementation.

Concern:

Discrete transistors used as digital logic devices make it difficult to isolate to a single faulty transistor.

Data Request:

Is the module free from the use of discrete transistors for digital logic implementation?

A Weight: 10 **B Weight:** 5

Action: N/A

Subject: General Digital

Parameter Number: t110

Parameter:

Control of multiplexers.

Concern:

Several multiplexed signals may only exist at one output pin. In order to select the multiplexer output signal, access to the multiplexer select line must exist at an edge connector pin.

Data Request:

Are all multiplexers controllable at connectors pins?

A Weight: 20 B Weight: 0

Action: See sections 7.2.1 and 7.3

Subject: General Digital

Parameter Number: t111

Parameter:

Enough component spacing to allow the use of test clips.

Concern:

Test clips can be used to access the signals from individual ICs. Some modules are so dense that test clips will not fit over the ICs limiting the techniques available to access internal signals.

Data Request:

Does component spacing allow the use of test clips?

A Weight: 10 B Weight: 0

Action: See section 7.4.5.2

Subject: General Digital

Parameter Number: t112

Parameter:

Invalid sequences and indeterminate outputs identified.

Concern:

If invalid or indeterminate states are possible, they must be identified so test equipment can avoid them and not accidently generate them.

Data Request:

Are all invalid and indeterminate states identified?

A Weight: 30 B Weight: 0

Action: N/A

Subject: General Digital

Parameter Number: t113

Parameter:

Latches or buffers present at inputs where skew problems could result during test.

Concern:

Skew problems result when slight offsets in input signal state transitions affect functional circuitry. Input signals from test equipment will often have a skew of 20 nS or more. Latches placed at sensitive inputs can protect input signals from skew problems.

Data Request:

Are latches or buffers present at all inputs that are susceptible to skew problems?

A Weight: 10 B Weight: 0

Action: See section 7.4.3.2

Subject: VLSI

Parameter Number: r901

Parameter:

Internal functions divisible into 'modules' that are controllable and observable during test.

Concern:

The complexity of a VLSI device should be divided into individual functions. The test development and test for each function individually is less complex than that of the entire device.

Data Request 1:

Enter the number of VLSIs with the main functions of the device divisible.

Data Request 2:

Enter the total number of VLSI devices used.

A Weight: 10 B Weight: 0

Action: See section 8.6

Subject: VLSI

Parameter Number: r902

Parameter:

Initialization by a few vectors (<20 Vectors).

Concern:

Initialization is the setting of sequential states to predefined values. To test any sequential device, the sequential states must be known prior to test. Otherwise, a definite response to a test vector cannot be predicted.

Data Request 1:

Enter the number of VLSIs with sequential states that can be initialized in less than 20 vectors.

Data Request 2:

Enter the total number of VLSIs with sequential states (not including scan VLSIs).

A Weight: 50 B Weight: 4

Action: See section 8.5

Subject: VLSI

Parameter Number: r903

Parameter:

Number of combinational devices between test points and VLSI device pins.

Concern:

Sometimes input pins to VLSI devices cannot be accessed directly by test equipment. As more combinations/devices are in series between test points (or connector pins) and VLSI pins, the process of controlling the VLSI pins gets more complicated.

Data Request 1:

Enter the number of VLSI signal pins that can be accessed from a connector.

Data Request 2:

Enter the total number of VLSI signal pins.

A Weight: 45 B Weight: 0

Action: N/A

Subject: VLSI

Parameter Number: r904

Parameter:

Percent VLSI device pins controllable/observable by test equipment.

Concern:

Controllability and observability are two of the most important factors in module testing. VLSI pins that are not controllable or observable are usually difficult or impossible to test.

Data Request 1:

Enter the number of VLSI signal pins that are controllable/observable.

Data Request 2:

Enter the total number of VLSI signal pins.

A Weight: 50 B Weight: 1

Action: N/A

Subject: VLSI

Parameter Number: r905

Parameter:

Percent VLSI device pins probeable.

Concern:

It is necessary to manually probe VLSI device pins during test development and often during diagnostic testing. Therefore, VLSI device pins should not be difficult to probe.

Data Request 1:

Enter the number of VLSI pins that are accessible for manual probing.

Data Request 2:

Enter the total number of VLSI pins.

A Weight: 40 B Weight: 0

Action: N/A

Subject: VLSI

Parameter Number: r906

Parameter:

Complexity of devices that do not have manufacturer test patterns, or structured design-for-test technique.

Concern:

It is difficult to develop test patterns for VLSI devices. Structured Design-for-Test (DFT) techniques, such as boundary scan, reduce the problem of test pattern generation. If a VLSI does not have patterns or a structured test technique, then test pattern development can be a huge effort.

Data Request 1:

Enter the number of VLSI devices with >30K gates or >10 sequential states with patterns or DFT.

Data Request 2:

Enter the total number of VLSI devices with >30K gates or >10 sequential states.

A Weight: 50 B Weight: 4

Action: See section 8.1

Subject: VLSI

Parameter Number: r907

Parameter:

Sequential chains within VLSI devices that cannot be broken or controlled.

Concern:

Sequential states that are not controllable within a VLSI device complicate testing and test generation. Each state must be initialized and test signals must be propagated through sequential states by a series of vectors. Large sequential chains within a device should be breakable.

Data Request 1:

Enter the number of VLSI devices with sequential chains of >4 states that can be broken or scanned.

Data Request 2:

Enter the total number of VLSI devices with sequential chains of >4 states.

A Weight: 40 B Weight: 2

Action: See sections 8.1.2.1 and 8.9

Subject: VLSI

Parameter Number: r908

Parameter:

Direct access to disable, reset, and other control lines.

Concern:

Test equipment should have direct access to VLSI control lines from a connector because these lines need to be exercised during most test routines.

Data Request 1:

Enter the number of VLSI control lines directly accessible from a connector.

Data Request 2:

Enter the total number of VLSI control lines.

A Weight: 35 B Weight: 2

Action: See section 8.3

Subject: VLSI

Parameter Number: r909

Parameter:

Buses and indicator lines accessible by the test equipment.

Concern:

If VLSI bus or indicator lines are present, test equipment will usually need to constantly monitor or control these lines during VLSI testing.

Data Request 1:

Enter the number of VLSI bus and indicator lines directly accessible by the test equipment.

Data Request 2:

Enter the total number of VLSI bus and indicator lines.

A Weight: 45 B Weight: 0

Action: See sections 8.1.1.2 and 8.2

Subject: VLSI

Parameter Number: r910

Parameter:

Length of sequential chains within VLSI. Applicable only if VLSI tests use pseudo-random numbers.

Concern:

Outputs of sequential circuitry depend on a series of vectors propagated through sequential states. The length of the series of vectors increases with the length of sequential chains. As a result, pseudo-random number generators do not produce efficient tests of VLSIs with sequential chains.

Data Request 1:

Enter the number of VLSIs with serial chains less than four states long.

Data Request 2:

Enter the total number of VLSI devices in the module.

A Weight: 35 B Weight: 0

Action: See section 8.9

Subject: VLSI

Parameter Number: r911

Parameter:

Tri-stateability of functional VLSI pins on a bus.

Concern:

Device pins that are bidirectional or can be tri-stated during normal operation need to be controlled during test. Test equipment should have control to tri-state any such pins while testing. Otherwise, several devices may be active on the same bus and damage could result.

Data Request 1:

Enter the number of VLSI bus pins that are tri-stateable by 4 or fewer vectors.

Data Request 2:

Enter the total number of VLSI bus pins.

A Weight: 35 B Weight: 0

Action: See section 8.1.1

Subject: VLSI

Parameter Number: r912

Parameter:

Number of non-controllable internal VLSI feedback loops (for devices without test patterns).

Concern:

If a VLSI device does not have test patterns and the device contains uncontrollable internal feedback loops, then these loops make test vector generation very difficult.

Data Request 1:

Enter the number of VLSI devices that either have test patterns or do not have feedback loops.

Data Request 2:

Enter the total number of VLSI devices.

A Weight: 55 B Weight: 5

Action: See sections 8.1.2.3 and 8.6

Subject: VLSI

Parameter Number: t901

Parameter:

Every input to the circuit generates a definite output (deterministic outputs).

Concern:

In order to test a circuit, a vector is input and a response observed and compared to a known correct response. If a functional circuit does not generate a definite output, then a response to a test vector could vary. Thus, verifying it against a known correct response is not possible.

Data Request:

Does every VLSI on the module generate deterministic outputs?

A Weight: 30 B Weight: 0

Action: See section 8.9

Subject: VLSI

Parameter Number: t902

Parameter:

Sequential states between test points and VLSI signal pins.

Concern:

Sequential circuitry exists between VLSI pins and test points (or connectors) greatly complicates the complexitv of controlling VLSI devices. To propagate a signal to through sequential devices requires a series of vectors dependent on the length of the sequential chain.

Data Request:

Is the number of sequential states between VLSI signals and connector pins less than 8?

A Weight: 40 B Weight: 10

Action: See section 8.9

Subject: VLSI

Parameter Number: t903

Parameter:

All Elements of custom VLSI device functions placed in the same device package.

Concern:

Functions of custom designed devices, such as Application Specific ICs (ASICs), should be designed so that separate SSI devices do not need to be added to a module to complete the function of an ASIC. An example is an ASIC requiring pull-up resistors externally.

Data Request:

Do all VLSI custom devices not require external SSI or discrete devices to complete a function?

A Weight: 20 B Weight: 0

Action: See section 8.9

Subject: VLSI

Parameter Number: t904

Parameter:

Do any VLSI devices have refresh requirements?

Concern:

A VLSI device can be designed so that memory within the device requires a refresh signal. This signal repeats after a certain period to retain the contents of the memory. If the test program has to maintain a memory refresh signal, it complicates test generation.

Data Request:

Are all VLSI devices free from refresh requirements?

A Weight: 15 B Weight: 0

Action: See section 8.3

Subject: VLSI

Parameter Number: t905

Parameter:

Clear description of device functions and any associated memory maps provided.

Concern:

During test development for VLSI devices, it is necessary to have descriptions of the device functions and any other descriptive materials (such as memory maps.)

Data Request:

Is a clear description of each VLSI device function available?

A Weight: 30 B Weight: 0

Action: See section 8.9

Subject: VLSI

Parameter Number: t906

Parameter:

Analog and digital portions of devices separately controllable and observable.

Concern:

It is much easier to test a mixed signal device if the digital and analog sections can be tested independently.

Data Request:

Are the digital and analog signals of mixed signal VLSIs separately controllable and observable?

A Weight: 30 B Weight: 0

Action: See section 12.1.3

Subject: VLSI

Parameter Number: t907

Parameter:

Computer aided design (CAD) system support test generation and evaluation.

Concern:

Some CAD databases are compatible with software that can automatically generate test vectors for a circuit design and analyze the thoroughness of test vectors.

Data Request:

Is a CAD system available to generate test vectors or check for testability problems?

A Weight: 40 B Weight: 0

Action: See section 8.9

Subject: VLSI

Parameter Number: t908

Parameter:

All internal oscillators completely controllable by test equipment.

Concern:

If a device contains an internal oscillator, it should be replaced by a test equipment oscillator during test. Otherwise, the test equipment will have to synchronize to the device oscillator.

Data Request:

Are all internal VLSI oscillators completely controllable by test equipment?

A Weight: 45 B Weight: 15

Action: See section 8.4

Subject: Processors

Parameter Number: r801

Parameter:

Access to microprocessor control signals (reset, wait, halt, single step, interrupt lines, etc.).

Concern:

Control of processor signals used for internal data/address manipulations is essential if external test programs will manipulate its various functions.

Data Request 1:

Enter the number of processor control signals that are accessible from a connector.

Data Request 2:

Enter the total number of processor control signals.

A Weight: 45 B Weight: 5

Action: See section 9.2.1.2

Subject: Processors

Parameter Number: t801

Parameter:

Control of microprocessor clock.

Concern:

Without control of the processor(s) clock(s), test equipment is unable to control the processor rendering the module practically untestable.

Data Request:

Is the processor(s) clock(s) controllable from a connector pin?

A Weight: 50 **B Weight:** 20

Action: See section 9.2.1.4

Subject: Processors

Parameter Number: t802

Parameter:

Knowledge of processor minimum clock frequency.

Concern:

Many of today's processors run at speeds that are too fast for most module testers. These processors have minimum clock speeds at which they can operate. Manufacturing faults are best diagnosed at slow speed, pervasive timing at single step speeds, and subtle timing faults at module clock rate.

Data Request:

Is the processor minimum clock speed specified or known?

A Weight: 10 B Weight: 0

Action: N/A

Subject: Processors

Parameter Number: t803

Parameter:

Control of all microprocessor buses (address, data).

Concern:

Control/access to all data/address lines is necessary for most microprocessor tests. (Some microcontrollers, however, have only internal address and data lines and would not be applicable here).

Data Request:

Are the processor address and data buses controllable and observable from a connector?

A Weight: 50 B Weight: 10

Action: See section 9.2.1.1

Subject: Processors

Parameter Number: t804

Parameter:

Ability to reset/interrupt microprocessor.

Concern:

Control of reset/interrupt lines of a processor is necessary during test. It enables test equipment to initialize or halt the processor before or during tests.

Data Request:

Can the processor(s) be reset and interrupted from a connector pin(s)?

A Weight: 50 B Weight: 10

Action: See section 9.2.1.2

Subject: Processors

Parameter Number: t805

Parameter:

Ability to tri-state all microprocessors.

Concern:

Tri-stating a processor allows for processor emulation by the test equipment, and allows other ICs or processors on the bus to be tested.

Data Request:

Can all processors on the module be individually disabled?

A Weight: 40 B Weight: 3

Action: See section 9.2.1.2

Subject: Processors

Parameter Number: t806

Parameter:

Ability to load random access memory (RAM) externally with a test program.

Concern:

Externally loading a test program into (on board module) RAM allows for faster module test.

Data Request:

Can the processor(s) RAM be loaded externally?

A Weight: 30 B Weight: 0

Action: See section 9.2.1.2

Subject: Processors

Parameter Number: t807

Parameter:

Monitor microprocessor/status lines without hanging up processor.

Concern:

Many processors have certain sequences in which status lines can be accessed. This knowledge is necessary in order to avoid hanging up the processor. (Also, a hung up processor often has a re-starting sequence).

Data Request:

Can processor(s) status lines be monitored without hanging up the processor(s)?

A Weight: 45 B Weight: 5

Action: See section 9.2.1.1

Subject: Processors

Parameter Number: t808

Parameter:

32 bit microprocessors (and higher) self-test or diagnostics available in accompanying firmware or on processor.

Concern:

Without self-test or diagnostics, a microprocessor of 32 bits (or higher) becomes a mammoth to test completely. It could require millions of test vectors and possibly months to generate test programs. Avoid processors with little or no diagnostics of this bit size.

Data Request:

Do all 32 bit or higher processors have >70% self-test available in ROM or on the processor?

A Weight: 50 B Weight: 2

Action: N/A

Subject: Processors

Parameter Number: t809

Parameter:

16 bit processors (or less) have self-test/diagnostics available.

Concern:

Self-test/diagnostics for processors of 16 bits or fewer, aids in test program development. Self-test can partially validate a complex IC (processor) quickly and easily at the start of a test program.

Data Request:

Do all processors of 16 bits or less have a self-test of >70% coverage available?

A Weight: 35 B Weight: 0

Action: N/A

Subject: Processors

Parameter Number: t810

Parameter:

Full processor product specifications and documentation available.

Concern:

Without full product specifications on the processor, it is difficult to generate accurate test vectors, or test programs in a short time.

Data Request:

Is full product specifications and documentation available for the processor(s)?

A Weight: 45 B Weight: 8

Action: See section 9.2.1.5

Subject: Processors

Parameter Number: t811

Parameter:

All processor frequencies required (clocks) from one controllable master oscillator.

Concern:

Using one controllable master oscillator (instead of several) to generate all processor frequencies required simplifies test equipment requirements.

Data Request:

Are all input clock signals to the processor from one controllable oscillator?

A Weight: 40 B Weight: 0

Action: See section 9.2.1.4

Subject: Processors

Parameter Number: t812

Parameter:

Micro-code of processor available including flow chart and memory map.

Concern:

Micro-code, flow charts, and memory map availability for a processor, makes a test engineer's task of generating a test program with test vectors much easier.

Data Request:

Is the processor micro-code available?

A Weight: 45 B Weight: 2

Action: See section 9.2.1.5

Subject: Processors

Parameter Number: t813

Parameter:

Electrical and mechanical emulator access to processor.

Concern:

All processors should be designed to make it easy to electrically and mechanically hook up a processor emulator. Difficult processor access can increase test times using an emulator.

Data Request:

Does electrical and mechanical access to the processor exist for emulation?

A Weight: 30 B Weight: 0

Action: See section 9.2.1.1

Subject: Processors

Parameter Number: t814

Parameter:

Use of multilevel output processors.

Concern:

Presently, only a few processors and controllers allow for multilevel outputs (more than two logic level states) such as Intel 43203, IAPX432, and Intel 8087. Avoid these scenarios since these circuits have more critical tolerances and reduced noise immunity.

Data Request:

Are only non-multilevel processors used?

A Weight: 10 B Weight: 0

Action: N/A

Subject: Processors

Parameter Number: t815

Parameter:

Ability to check microcode location when processor stops on an error.

Concern:

Module design has to be done so that when a processor halts due to error detection, test equipment can determine the microcode step the processor stopped at. One approach is to log the code address location in a status register on a failure.

Data Request:

Can the microcode location be checked when the processor fails on an error?

A Weight: 40 B Weight: 0

Action: N/A

Subject: Processors

Parameter Number: t816

Parameter:

Non-multiplexed processor address/data lines.

Concern:

It is always easier for test equipment to access address and data lines separately rather than have these lines multiplexed. Non-multiplexing allows test equipment to set address lines and simultaneously check the data lines.

Data Request:

Does the processor(s) have separate address and data lines (non-multiplexed)?

A Weight: 10 **B Weight:** 0

Action: N/A

Subject: Processors

Parameter Number: t817

Parameter:

Emulator/pod available for the specific processor used.

Concern:

Module troubleshooting can take months rather than days without access to an emulator and pod for a specific processor.

Data Request:

Is an emulator/pod available for processor testing?

A Weight: 30 B Weight: 0

Action: N/A

Subject: Processors

Parameter Number: t818

Parameter:

Microcode implemented with test instructions for easy debug (use of breakpoints, flags, single step, etc.)

Concern:

Software design and development for processor(s) can greatly enhance the ease of creating test programs for them, even without processor self-test.

Data Request:

Does processor microcode include instructions to aid in debug?

A Weight: 45 B Weight: 2

Action: N/A

Subject: Memory

Parameter Number: r851

Parameter:

Programmable devices tri-stateable (designed with tri-state).

Concern:

Without tri-state control of individual tri-stateable devices it is difficult to isolate to one of many devices connected on a bus.

Data Request 1:

Enter the number of memory devices that are tri-stateable.

Data Request 2:

Enter the total number of memory devices on the module.

A Weight: 45 B Weight: 1

Action: See sections 10.3 and 10.2.7

Subject: Memory

Parameter Number: r852

Parameter:

Direct access to chip control lines (RAS, CAS, etc.).

Concern:

Access to Row Address Strobe (RAS), Column Address Strobe (CAS), and other chip control lines is necessary. These signals enable various test pattern reading and writing to and from memory devices.

Data Request 1:

Enter the number of memory device control lines that are accessible at a connector.

Data Request 2:

Enter the total number of memory device control lines on the module.

A Weight: 50 B Weight: 2

Action: See section 10.3

Subject: Memory

Parameter Number: r853

Parameter:

Access to all memory locations (even spare locations).

Concern:

Access to all device locations (including spare or unused ones) is necessary to completely check the device contents. Erroneous data and spare locations can be verified during device tests.

Data Request 1:

Enter the number of accessible memory locations.

Data Request 2:

Enter the total number of memory locations.

A Weight: 30 B Weight: 0

Action: See sections 10.2.7 and 10.3

Subject: Memory

Parameter Number: r854

Parameter:

Checksum value stored on memory devices.

Concern:

The simplest memory test for a Read Only Memory (ROM) device is a checksum test. A checksum is the sum of all device memory locations. This value is easy to compute during an automated test and can be compared to a correct checksum value in the device.

Data Request 1:

Enter the number of ROMs with a checksum value stored on the ROM.

Data Request 2:

Enter the total number of ROM devices.

A Weight: 45 B Weight: 1

Action: See sections 10.2.1 and 10.3

Subject: Memory

Parameter Number: t851

Parameter:

Have direct access to all memory address and data lines.

Concern:

Without access to all address and data lines of a device, it is impossible to test it completely.

Data Request:

Can all memory address and data lines be accessed at a connector?

A Weight: 50 B Weight: 10

Action: N/A

Subject: Memory

Parameter Number: t852

Parameter:

Control of memory address generator (such as a demultiplexer).

Concern:

Without control to the address generator specific tests of a memory device are impossible.

Data Request:

If an address generator exists, is it controllable at connector pins?

A Weight: 45 B Weight: 4

Action: See section 10.3

Subject: Memory

Parameter Number: t853

Parameter:

Ability to tri-state or disable all programmable logic devices (PLDs) driving ROMs.

Concern:

Without tri-stating these upstream PLD's, it is difficult, if not impossible, to test specific "downstream" memory devices.

Data Request:

Can all PLDs driving memory devices be disabled?

A Weight: 35 B Weight: 0

Action: See section 10.2.7

Subject: Memory

Parameter Number: t854

Parameter:

Ability to enter illegal states for test purposes. (Depends on application).

Concern:

If illegal states are possible in the memory/PLD device, a tester needs the ability to access them. In doing so, the tester can see if they can influence the module functional operation, such as causing a logic "lock up".

Data Request:

Can illegal states in memory devices be entered during test?

A Weight: 20 B Weight: 0

Action: See section 10.3

Subject: Memory

Parameter Number: t855

Parameter:

PLD designed to eliminate untestable bridging faults.

Concern:

The compact structure of a PLD invites shorts between adjacent lines known as "bridging faults". PLDs can be laid out (designed) to minimize the probability of these types of faults.

Data Request:

Are all PLDs designed to limit untestable bridging faults?

A Weight: 40 B Weight: 0

Action: See section 10.3

Subject: Memory

Parameter Number: t856

Parameter:

Known output for every ROM word (unused words should output known error state).

Concern:

By having an output for every ROM word, the device can be tested by just reading and verifying each ROM location. Therefore, no unknown error states can occur in unused memory locations.

Data Request:

Does a known output exist for each ROM location?

A Weight: 40 B Weight: 3

Action: See section 10.3

Subject: Memory

Parameter Number: t857

Parameter:

Access to strobe lines in dynamic RAMs.

Concern:

Dynamic RAMs require refreshing every few milliseconds to renew the present state of the memory using a strobe line. Access to this line is essential when testing these devices. If possible, strobe circuitry should be disabled.

Data Request:

Can all strobe lines be accessed?

A Weight: 30 B Weight: 0

Action: N/A

Subject: Memory

Parameter Number: t858

Parameter:

Automatic Test Pattern Generator (ATPG) available to test engineer for PLDs.

Concern:

Programmable Logic Devices (PLDs) such as PALs and PLAs are custom designed and require unique test vectors for each PLD design. Manual generation of test vectors can be costly and time consuming. If an ATPG can be used for test pattern development than time and money can be saved.

Data Request:

Is an automatic test pattern generator available for PLD test generation?

A Weight: 50 B Weight: 3

Action: N/A

Subject: Memory

Parameter Number: t859

Parameter:

Use of internal PLD oscillators without a dedicated enable pin.

Concern:

Oscillators can be "buried" in PLD designs without external access to them making these devices almost impossible to test. Dedicated oscillator enable pins need to be designed into such circuitry that allow the oscillator to be replaced by an external clock.

Data Request:

If an oscillator exists in a PLD, can it be disabled?

A Weight: 45 B Weight: 10

Action: N/A

Subject: Memory

Parameter Number: t860

Parameter:

Use of simple memory elements created by using 3-state type of combinational outputs.

Concern:

Memory elements created by feedback around a 3-state type of combinational output (0, 1, high impedance) may necessitate tester and PLD to be simultaneously active. This facilitates reliable latching of data (especially in CMOS parts).

Data Request:

Are simple memory elements avoided?

A Weight: 20 B Weight: 0

Action: See section 10.2.7

Subject: Memory

Parameter Number: t861

Parameter:

Complex memory internal to a PLD.

Concern:

Feedback loops with more than one output or overlapping two feedback loops create complex memory elements. They can cause race conditions in many testers.

Data Request:

Do all PLD designs avoid complex memory and have less than 30 sequential states?

A Weight: 45 B Weight: 5

Action: N/A

Subject: Memory

Parameter Number: t862

Parameter:

Initialization of memory by a short sequence of test vectors (preloading, etc.).

Concern:

Memory/PLD designs need to be executed in such a way that they can be initialized by only a few test vectors. The preferred method to test an uninitializable device is to devote unused input pins to load initial states.

Data Request:

Can all memory/PLD devices be initialized by less than 5 vectors? (Not including RAM).

A Weight: 45 B Weight: 0

Action: See section 10.3

Subject: Memory

Parameter Number: t863

Parameter:

PLD power-up state information available.

Concern:

PLDs power up state is not standard. It is often all ZEROs or all ONEs. Knowledge of this initial state is necessary for programming, testing, and testability purposes.

Data Request:

Is the power-up state known or available for all PLDs?

A Weight: 35 B Weight: 0

Action: see section 10.2.7

Subject: Memory

Parameter Number: t864

Parameter:

Use of older Programmable ROMs (PROMs) requiring 2 voltages for readout.

Concern:

Some older PROMs require 2 voltages for readout. Avoid these models since they increase the tester requirements.

Data Request:

Is the module free from older PROMs requiring 2 voltages?

A Weight: 20 B Weight: 0

Action: N/A

Subject: Memory

Parameter Number: t865

Parameter:

Access to ROM security bit preventing memory readout.

Concern:

Occasionally ROMs contain "proprietary" information. Without access to the security bit, complete memory readout during test is impossible.

Data Request:

If "secure" ROMs are used, is the security accessible at a connector pin?

A Weight: 40 B Weight: 0

Action: N/A

Subject: Memory

Parameter Number: t866

Parameter:

Electronically Erasable PROMs (EEPROMs) write cycle "lifespan" information available.

Concern:

EEPROM write-cycle lifespan can range from 100 rewrites to over one million rewrites. Before "long" test cycles begin, this information is important because the device lifespan may be significantly reduced by certain types of tests.

Data Request:

Is lifespan information available for EEPROMs?

A Weight: 10 B Weight: 0

Action: N/A

Subject: Memory

Parameter Number: t867

Parameter:

All device documentation and specifications available, including logic equations and truth tables.

Concern:

Device documentation, specifications, logic equations, and truth tables all aid the test engineer in understanding the device operation during test program development.

Data Request:

Is all memory/PLD device documentation available?

A Weight: 50 B Weight: 10

Action: See section 10.2.1

Subject: Memory

Parameter Number: t868

Parameter:

PLD test vectors available.

Concern:

Test vectors may be available from the PLD designer that can be used in the module test program. As a result, the test engineer needs to develop fewer test vectors for the PLD.

Data Request:

Do test vectors exists for all PLD devices?

A Weight: 20 B Weight: 0

Action: N/A

Subject: Memory

Parameter Number: t869

Parameter:

Use of WORM CD/ROMs.

Concern:

Avoid using Write Once Read Many (WORM) Compact Disk (CD)/ ROMs since corrections of faults or memory testing is impossible.

Data Request:

Are only non WORM CD/ROM devices used?

A Weight: 10 B Weight: 0

Action: N/A

Subject: Memory

Parameter Number: t870

Parameter:

Use of core memory.

Concern:

Memory technology has progressed to the point where core memory is no longer necessary. Core memory is heavy, fragile, and often difficult to access with present day testers (not set up for core).

Data Request:

Is the module free from the use of core memory?

A Weight: 15 B Weight: 0

Action: N/A

Subject: Scan

Parameter Number: r701

Parameter:

Use of boundary scan devices.

Concern:

Boundary scan is the only technique that can be efficiently used during module test (not including scan used in BIT such as BILBO). Boundary scan enables devices to be tested individually and can verify interconnections similar to incircuit testing.

Data Request 1:

Enter the number of boundary scan devices on the module.

Data Request 2:

Enter the total number of devices on the module.

A Weight: 45 B Weight: 1

Action: See sections 11.2 and 11.3.3

Subject: Scan

Parameter Number: r702

Parameter:

Percent pins of all devices with boundary scan.

Concern:

Implementing boundary scan allows interconnect testing between several device pins and between device pins and test points. Therefore, if every device on a module is a boundary scan device, then every interconnect can be tested.

Data Request 1:

Estimate the total number of device pins with boundary scan.

Data Request 2:

Enter the total number of device pins.

A Weight: 50 B Weight: 0

Action: N/A

Subject: Scan

Parameter Number: r703

Parameter:

Percent scan devices with a BYPASS instruction available.

Concern:

Usually during scan testing, tests of individual devices occur. Input and output vectors to and from the scan cells of the device travel through scan cells of other devices on the scan chain. However, a BYPASS instruction can set the scan chain to one cell in devices not undergoing tests.

Data Request 1:

Enter the number of devices with a BYPASS or compatible instruction.

Data Request 2:

Enter the total number of scan devices.

A Weight: 15 B Weight: 0

Action: See section 11.2.4.3.2

Subject: Scan

Parameter Number: r704

Parameter:

Scan test patterns (from the device vendor) available.

Concern:

In order to test any device, a set of test vectors must exist. If a manufacturer tests devices scan chains individually, then module tests can use the same vectors. This could make scan test pattern generation unnecessary and ease test program development.

Data Request 1:

Enter the number of scan devices with test patterns from the device vendor.

Data Request 2:

Enter the total number of scan devices.

A Weight: 50 B Weight: 2

Action: See section 11.2.6

Subject: Scan

Parameter Number: t701

Parameter:

Scan devices controlled by a standard testability bus (such as IEEE-STD-1149.1 and ETM bus).

Concern:

Any testability bus used on scan devices should follow a standard. An example of a well written standard is IEEE standard 1149.1. Standards reduce test development time and make the design compatible with other hardware and test equipment.

Data Request:

Does the scan design conform to a standard testability bus?

A Weight: 50 B Weight: 4

Action: See section 11.2.2

Subject: Scan

Parameter Number: t702

Parameter:

Tester access to testability bus or a test bus controller.

Concern:

In order for test equipment to control and monitor scan devices, it needs easy connection to the test bus.

Data Request:

Is the scan test bus or bus controller accessible from a connector?

A Weight: 50 B Weight: 20

Action: See section 11.3.1

Subject: Scan

Parameter Number: t703

Parameter:

Scan test control and serial data signals only used for test and BIT (especially the test clock).

Concern:

It is good practice to use scan control and data signals only during test and BIT. Otherwise, there is not a clear separation between scan test operations and functional circuitry.

Data Request:

Are the scan control signals only used for testing and Built-in Test (BIT)?

A Weight: 25 B Weight: 0

Action: See section 11.3.2

Subject: Scan

Parameter Number: t704

Parameter:

Devices have identification data accessible from test lines (ID register).

Concern:

Some scan devices can be designed with a register that contains device identification data. This register would typically have a manufacturer code, part number, and rev. This information could be used during test to identify wrong parts and revisions before applying test vectors.

Data Request:

Is device identification data accessible from the scan control circuitry?

A Weight: 5 B Weight: 0

Action: See section 11.2.4.3.6

Subject: Scan

Parameter Number: t705

Parameter:

Scan/boundary scan devices conform to a standard.

Concern:

Every scan device should conform to a standard. Standards reduce test development time and make the design compatible with other hardware and test equipment.

Data Request:

Do the scan devices conform to a scan standard?

A Weight: 50 B Weight: 3

Action: See section 11.2.2

Subject: Scan

Parameter Number: t706

Parameter:

Scan cells should initialize to known state of two logic levels for scan path integrity check.

Concern:

Scan test circuitry should be validated prior to test by reading known data from the scan chain and verifying it. Initializing data within each scan device enables isolation of a fault within the scan path or a device's scan control circuitry to one device.

Data Request:

Do several cells within each device's scan chain initialize to a know state?

A Weight: 30 B Weight: 0

Action: See section 11.2.4.3

Subject: Scan

Parameter Number: t707

Parameter:

Control of IC internal and external tri-states during scan testing.

Concern:

If any tri-state control signal within a scan device is not controllable during scan testing, test development, and test may be impossible. Attempting scan testing might enable two drivers on the same bus at the same time and cause device damage.

Data Request:

Is every internal and external tri-state enable controllable during scan testing?

A Weight: 50 B Weight: 10

Action: See section 11.2.4.4

Subject: Scan

Parameter Number: t708

Parameter:

Scan support software to run test, translate, and interpret scan test data.

Concern:

If a module is to be tested by a scan technique, then module scan test support software should be used to interpret test results. Otherwise, software has to be manually generated to interpret results and report failures.

Data Request:

Does scan test support software exist for the test run time system?

A Weight: 45 B Weight: 8

Action: N/A

Subject: Scan

Parameter Number: t709

Parameter:

Scan test patterns directly used during board test without needing to be simulated through other devices.

Concern:

In some scan techniques such as boundary scan and In-Situ Testability Design (INSTD), individual device tests occur similar to an incircuit test. This allows testers to use device scan test patterns with minor alterations during module test.

Data Request:

Can individual device scan test patterns be used during module test?

A Weight: 50 B Weight: 10

Action: See section 11.3.3

Subject: Scan

Parameter Number: t710

Parameter:

Documentation of scan technique and design.

Concern:

All scan techniques used needs to be well documented for test pattern generation. A testability scan standard is a good source of documentation and any design specifics and options should be documented.

Data Request:

Is the scan technique and design used well documented?

A Weight: 50 B Weight: 10

Action: See section 11.3.4

Subject: Scan

Parameter Number: t711

Parameter:

Ability to control and observe individual functions in scan devices from the connector.

Concern:

Test generation and debug get easier as the test equipment gains more control of test functions. For scan testing, test equipment should be able to control and observe functions and instructions within individual scan devices from a test or edge connector.

Data Request:

Can scan functions and instructions within scan devices be controlled from a connector?

A Weight: 30 B Weight: 0

Action: See section 11.3.1

Subject: Scan

Parameter Number: t712

Parameter:

Size of ambiguity group of an observed fault.

Concern:

The isolation of a fault to the smallest group of devices that could have generated it is called an ambiguity group. Ideally, an ambiguity group should be one device. If the ambiguity group isolated during scan testing is very large, then extra tests are needed to improve fault isolation.

Data Request:

Is the smallest scan ambiguity three (3) devices or less?

A Weight: 20 B Weight: 0

Action: N/A

Subject: Scan

Parameter Number: t713

Parameter:

All scan chips have a compatible control interface to test bus or controlled by a test controller.

Concern:

Every scan device on a test bus should have the same bus interface. This enables test equipment to use the same set of instruction codes and control sequences for every device on the test bus.

Data Request:

Is the control interface the same for every scan device?

A Weight: 45 B Weight: 2

Action: See section 11.3.1

Subject: Scan

Parameter Number: t714

Parameter:

Software available to test non-scan devices through boundary scan devices.

Concern:

On a module that contains both boundary scan devices and non-boundary scan devices, it is possible to use the boundary scan device cells during the test of other devices. Software exists that can do this automatically. The software simplifies tests of non-boundary scan devices.

Data Request:

Is software available to test non-boundary scan devices using the boundary scan chain?

A Weight: 10 B Weight: 0

Action: See section 11.3.3

Subject: Scan

Parameter Number: t715

Parameter:

Signals must not invert at any point when they are shifted through a scan chain.

Concern:

Any signals can invert during shifting of data through the boundary scan chain immensely complicate tester interpretations of scan test output data.

Data Request:

Do signals shift through the scan chain without inverting at any point?

A Weight: 40 B Weight: 5

Action: See section 11.3.2

Subject: General Analog

Parameter Number: r551

Parameter:

Test points at macro boundaries. (Macro I/O and control pins should be accessible).

Concern:

Test points at macro boundaries (macro I/O and control pins), simplify fault isolation to a single cascaded macro.
NOTE: a macro is a functional analog circuit.

Data Request 1:

Enter the number of macro boundaries accessible at a test point or connector.

Data Request 2:

Enter the total number of macro boundaries.

A Weight: 50 B Weight: 2

Action: See section 12.1.2

Subject: General Analog

Parameter Number: r552

Parameter:

Test points accessible at connector pins (or output leads).

Concern:

Test point signals resident on an external connector (or to output lead of a hybrid) can be accessed directly by automatic test equipment (ATE). Otherwise, a technician has to manually probe the board or attach test clips for each test.

Data Request 1:

Enter the number of test points on a connector pin or lead.

Data Request 2:

Enter the total number of test points.

A Weight: 35 B Weight: 0

Action: See sections 12.1.2.1 and 12.1.2.2

Subject: General Analog

Parameter Number: r553

Parameter:

Number of complex waveforms measured and supplied.

Concern:

Test equipment and test development costs increase with the number of complex waveforms measured and supplied during module test. A complex signal can be described as multiple phase or time related signal or an exotic modulation signal with or without unique timing patterns.

Data Request 1:

Enter the number of non-complex input/output signals on the module.

Data Request 2:

Enter the total number of input/output signals on the module.

A Weight: 45 B Weight: 1

Action: See section 12.1.2.3

Subject: General Analog

Parameter Number: r554

Parameter:

Ability to break feedback loops between macros.

Concern:

Feedback loops between several macros make fault isolating to one macro impossible unless the tester has the ability to break these loops.

Data Request 1:

Enter the number of feedback loops between macros that can be broken.

Data Request 2:

Enter the total number of feedback loops between macros.

A Weight: 50 B Weight: 4

Action: See section 12.1.1

Subject: General Analog

Parameter Number: r555

Parameter:

Ability to inject own oscillator.

Concern:

As in digital circuitry, free running oscillators in analog circuits are a nightmare for synchronization in most present day testers. Oscillators must be disablable and replaceable by an off-card oscillator, such as one supplied by test equipment.

Data Request 1:

Enter the number of disablable/replaceable oscillators.

Data Request 2:

Enter the total number of oscillators on the module.

A Weight: 50 B Weight: 10

Action: See section 5.1.8

Subject: General Analog

Parameter Number: t551

Parameter:

Use of discrete devices.

Concern:

Discrete parts have higher failure rates, take up more space, and are more expensive than analog integrated circuits. Resistor packs are more reliable and provide for "matched" resistors compared to discrete resistors.

Data Request:

Are less than 25 discrete devices used in the module? (Not including pull-ups or pull-downs).

A Weight: 10 B Weight: 0

Action: N/A

Subject: General Analog

Parameter Number: t552

Parameter:

Long time constant macro controllability.

Concern:

Macros with long time constants increase test times, thus the ability for the tester to control and reduce them decreases test times.

Data Request:

Can every time constant (length of time of a function) be reduced to under 30 seconds?

A Weight: 25 B Weight: 0

Action: See sections 12.1.4 and 12.1.1

Subject: General Analog

Parameter Number: t553

Parameter:

Tolerances of all signals known.

Concern:

Test program development requires a knowledge of the tolerances of all signals to be tested. If they do not exist, a test program may have tolerances that pass out-of-tolerance boards or fail in-tolerance boards.

Data Request:

Are all signal tolerances defined or known?

A Weight: 45 B Weight: 3

Action: See section 12.1.4

Subject: General Analog

Parameter Number: t554

Parameter:

Control of digital signals feeding analog (such as Digital to Analog Converters (DACs)).

Concern:

Often analog circuits receive digital signals through DACs. These conversion circuits need to be controllable so that the test equipment can completely exercise the analog sections.

Data Request:

Can all digital signals feeding analog circuits be controlled at test points?

A Weight: 40 B Weight: 10

Action: See section 12.2.2

Subject: General Analog

Parameter Number: t555

Parameter:

Use standard 50, 75, 130 ohm, or greater than 1 megaohm system.

Concern:

Standard 50, 75, 130 ohm, > 1 megaohm system refers to a standard impedance used for outputs and test points. The most common impedance used in test equipment is 50 ohms. Impedance matching circuitry is unnecessary if the tester, module, and tester interface have the same impedance.

Data Request:

Does the module use an impedance of 50, 75, 130, or >1Mohm for inputs, outputs, and test points?

A Weight: 50 B Weight: 7

Action: See section 12.1.2.2

Subject: General Analog

Parameter Number: t556

Parameter:

Analog/RF control system uses a standard bus (such as IEEE-488).

Concern:

Use of standard buses, such as IEEE-488 or RS432, in analog/RF control circuitry, provides an easy tester interface. Thus, reducing both test times and cost.

Data Request:

Is the analog/RF control bus a standard control bus?

A Weight: 40 B Weight: 1

Action: N/A

Subject: General Analog

Parameter Number: t557

Parameter:

Ability to inject own signals when normal signal levels are Very high or low (<1 mV or >80 volts).

Concern:

For very high or very low signal levels, a tester needs to access and inject a range of input signals directly for troubleshooting purposes.

Data Request:

Can every signal < 1 mV and > 80 Volts be replaced by a tester signal?

A Weight: 20 B Weight: 0

Action: See section 12.1.2

Subject: General Analog

Parameter Number: t558

Parameter:

Use of wired-OR for error bits.

Concern:

Wired-OR (wiring several devices together) does not allow a tester to isolate a fault to one device. Placing diodes at each wired-OR signal enables detection of a faulty device.

Data Request:

Is the design free from the use of wired-OR circuits?

A Weight: 10 B Weight: 0

Action: See section 12.1.2.1.2

Subject: General Analog

Parameter Number: t559

Parameter:

Circuits functionally complete (bias networks or loads on other assemblies not required).

Concern:

If circuits are not functionally complete on one circuit card then the additional circuits required have to be provided by the tester. These additional circuits must be provided in a more complex adapter or tester, raising test costs and complexity.

Data Request:

Are all circuits functionally complete (not requiring external circuitry)?

A Weight: 45 B Weight: 1

Action: See section 12.1.3

Subject: General Analog

Parameter Number: t560

Parameter:

All selected parts well characterized in terms of failure modes.

Concern:

By selecting parts well characterized in terms of failure modes, the types of failures can be more easily predicted. As a result, the test program can more accurately check for possible faults.

Data Request:

Are all parts well characterized in terms of failure modes?

A Weight: 30 B Weight: 0

Action: See section 12.1.2.1

Subject: General Analog

Parameter Number: t561

Parameter:

Ability to separate functional blocks (separate output of one block to input of next block).

Concern:

Separating blocks of different functions simplifies testing and debug of analog circuits. Blocks can be separated by breaking feedback loops or separating output of one block to the input of the next.

Data Request:

Can module functional blocks (independent functions) be separated during test?

A Weight: 45 B Weight: 3

Action: See sections 12.1.1 and 12.1.3

Subject: General Analog

Parameter Number: t562

Parameter:

Number of analog and digital signal pins.

Concern:

Today's analog circuit cards can be so complex that the number of signal pins can be over one thousand. If a tester cannot provide enough signal pins, then the test adapter will need to include multiplexors. A typical tester will not be able to provide/monitor over 200 signals to a module.

Data Request:

Do less than 200 signals exist as inputs and outputs on the module?

A Weight: 45 B Weight: 8

Action: See sections 12.1.2 and 12.1.3

Subject: General Analog

Parameter Number: t563

Parameter:

Statistical failure analysis available.

Concern:

Statistical failure analysis greatly reduces the complexity of analog debug time after test by analyzing those sections most likely to have failed first.

Data Request:

Is a statistical failure analysis of the module available?

A Weight: 10 B Weight: 0

Action: N/A

Subject: General Analog

Parameter Number: t564

Parameter:

Test points isolated from the main signal path.

Concern:

By isolating test points from the main signal path through buffers, etc., noise and other problems such as accidental shorts can be isolated from affecting main circuit functions.

Data Request:

Are all test points isolated from the main signal path(s)?

A Weight: 30 B Weight: 0

Action: See section 12.1.2

Subject: General Analog

Parameter Number: t565

Parameter:

Test points designed with drive capability and impedance match for ATE load.

Concern:

Automatic test equipment will load any test point connected to it. The UUT must be designed to be able to impedance match and drive the ATE load.

Data Request:

Are all test points capable of impedance matching and driving an ATE load?

A Weight: 40 B Weight: 2

Action: See sections 12.1.2.2 & 12.1.2.3

Subject: High Freq

Parameter Number: r451

Parameter:

Ability to monitor all active components and frequency conversion stages.

Concern:

Test points should exist at all frequency stages and the output of all active components. This will ease fault isolation and the complexity of signal conversions between test points. For mixers, test points should be placed before filtering.

Data Request 1:

Enter the number of test points at different frequency stages.

Data Request 2:

Enter the total number of frequency stages.

A Weight: 45 B Weight: 3

Action: See section 13.1.1

Subject: High Freq

Parameter Number: r452

Parameter:

Test points have common impedances and connector types (preferably 50 or 70 ohms; BNC OR SMA connectors).

Concern:

As a signal frequency increases the problem of impedance matching becomes more severe. Impedances need to be matched for all high frequency signals. Most test equipment and high frequency designs use 50 ohm impedances. Also, standard connectors ease test fixturing.

Data Request 1:

Enter the number of standard impedances and connectors used.

Data Request 2:

Enter the total number of impedances and connectors used.

A Weight: 50 B Weight: 6

Action: See sections 12.1.2.2 and 13.1.1

Subject: High Freq

Parameter Number: t451

Parameter:

GHz test pads meet layout rules. (Minimum pad pitch of 50 um, 50 X 50 um minimum pad size, etc.).

Concern:

Large GHz test pads introduce parasitics and small pads are difficult to probe. The recommended size is 100 x 100 um with 150 um pitch (distance from pad edge to pad edge). Pads also should be of equal height (max. variance of 0.5 um) and oriented in a straight line.

Data Request:

Do all test pads for GHz probing meet standard GHz layout rules?

A Weight: 40 B Weight: 5

Action: See section 13.3.3

Subject: High Freq

Parameter Number: t452

Parameter:

Ground pads provided with each GHz signal pad. (Not applicable for differential MMIC layouts).

Concern:

Each GHz signal pad should have an adjacent common ground provided with it. Common ground inductance can cause cross-talk. Ground-signal-ground pad layout is recommended for signals over 16 GHz (NOTE: ground-signal-ground should be required for frequencies above 18 GHz).

Data Request:

Are ground pads provided with each GHz signal pad?

A Weight: 45 B Weight: 4

Action: See sections 13.3.3 and 13.3.5

Subject: High Freq

Parameter Number: t453

Parameter:

Difficult test requirements (> 18 GHz, <-70 dBm, >60 dBm).

Concern:

Some test requirements (>18 GHz, <-70 dBm, >60 dBm) require costly test equipment and interfaces. For example, automated network analyzers above 18 GHz usually are not readily available without frequency conversion and its associated errors.

Data Request:

Are all signals to be measured and supplied < 18 GHz, > -70 dBm, & < 60 dBm?

A Weight: 45 B Weight: 7

Action: N/A

Subject: High Freq

Parameter Number: t454

Parameter:

Ability to observe complex signal health based on indirect parameters.

Concern:

Often, RF, microwave, or a complex signals health can be verified by an easy to measure indirect parameter. For instance, supply current or a DC level dependent on frequency can verify a frequency.

Data Request:

Can indirect parameters be used to verify complex signals?

A Weight: 20 B Weight: 0

Action: See section 13.2.6

Subject: High Freq

Parameter Number: t455

Parameter:

Manual interactions.

Concern:

Required operator interactions are time consuming and error prone. Any type of manual frequency alignment should be avoided since it requires operator interactions. Active multipliers requiring frequency alignment can be replaced with division schemes or phase lock technology.

Data Request:

Is the design free from any manual user interactions?

A Weight: 30 B Weight: 0

Action: See section 13.1.1

Subject: High Freq

Parameter Number: t456

Parameter:

Filters or buffers used to protect comparators and "sample & hold" circuits from ATE injected noise.

Concern:

Comparators and "sample & hold" circuits are highly susceptible to noise and often fail test due to injected noise from the test system. Using filters or buffers ac these devices lessens the effects of noise.

Data Request:

Are all comparators and "sample & hold" circuits protected from noise with filters or buffers?

A Weight: 10 B Weight: 0

Action: See section 13.1.1

Subject: High Freq

Parameter Number: t457

Parameter:

Test fixture heat dissipation required.

Concern:

Many high frequency devices heat up rapidly and require cooling during test. This forces the test fixture to be made more complex and costly.

Data Request:

Can the module be tested without having to provide heat dissipation?

A Weight: 15 B Weight: 0

Action: See section 13.3.8

Subject: High Freq

Parameter Number: t458

Parameter:

Calibration of circuitry to be tested required.

Concern:

When a circuit requires calibration, operator interactions are necessary, which are time consuming and error prone. In automatic calibration, test time and accuracy are also affected.

Data Request:

Can the module be tested without performing a module calibration?

A Weight: 30 B Weight: 0

Action: See sections 13.3.3.2 and 13.3.4

Subject: High Freq

Parameter Number: t459

Parameter:

Frequencies and waveforms specified at all interface points.

Concern:

Knowledge of high frequency signals at all interface points must be provided for test development and test. These frequencies and waveforms must be documented in some form of literature.

Data Request:

Are all module frequencies and waveforms documented at all interface points?

A Weight: 45 B Weight: 4

Action: See section 13.1.1

Subject: High Freq

Parameter Number: t460

Parameter:

Test points designed not to degrade the test signal.

Concern:

Signals at test points can be degraded due to transmission line effects, poorly matched impedances, and resistance and capacitance of devices on the test signal line. For example, resistive attenuators at test points should have low series impedance and shunt capacitance.

Data Request:

Are all test points designed so that test signals are not degraded?

A Weight: 10 B Weight: 0

Action: See section 13.1.1

Subject: High Freq

Parameter Number: t461

Parameter:

Similar frequency ranges and components grouped together on the same module.

Concern:

Similar frequencies ranges and components should be partitioned on the same module to ease module test equipment requirements to a small frequency range.

Data Request:

Are similar frequency ranges and components partitioned on the module?

A Weight: 20 B Weight: 0

Action: N/A

Subject: High Freq

Parameter Number: t462

Parameter:

Signals isolated at test points to avoid disturbing any functional signals.

Concern:

Test points should be designed not to disturb functional signals using isolation devices, couplers, or matched impedances. Matched impedances should be designed for MINIMUM power transfer. Also, reflections from open test points are possible then they should be terminated.

Data Request:

Are all test points designed not to disturb any functional signals?

A Weight: 45 B Weight: 5

Action: See section 13.1.1

Subject: High Freq

Parameter Number: t463

Parameter:

Complex input test signals required.

Concern:

This parameter refers to signals that are not DC, simple AM, or simple FM signals as "complex signals". Test points should be located at points on the module where simple inputs generate the complex signals. Complex signals require high cost signal generators in test equipment.

Data Request:

Are all required test input signals non-complex?

A Weight: 35 B Weight: 4

Action: N/A

Subject: High Freq

Parameter Number: t464

Parameter:

Test point leads and transmission lines kept as short as possible.

Concern:

Test point leads and transmission lines are susceptible to noise and should be minimized.

Data Request:

Are all test points and transmission lines as short as possible?

A Weight: 30 B Weight: 0

Action: N/A

Subject: High Power

Parameter Number: t401

Parameter:

Independent control of parallel power supplies.

Concern:

If independent control of parallel supplies does not exist, then a faulty parallel supply cannot be isolated.

Data Request:

Are parallel power supplies be independently controllable and observable?

A Weight: 35 B Weight: 0

Action: See section 14.5

Subject: High Power

Parameter Number: t402

Parameter:

Power supplies designed to drive non-linear loads.

Concern:

Linear loads are easy to model and much easier for test equipment to emulate than non-linear loads.

Data Request:

Is the power supply(s) designed to drive only linear loads?

A Weight: 40 B Weight: 2

Action: See section 14.5

Subject: High Power

Parameter Number: t403

Parameter:

Test equipment access to connect to and provide input voltage signals.

Concern:

To test a power module, power and voltage signals must be input from test equipment. The ease with which test equipment can connect to the module and provide these signals affects the test fixturing and test times.

Data Request:

Is a standard or simple connector used for input power supply signals?

A Weight: 40 B Weight: 1

Action: See section 14.3

Subject: High Power

Parameter Number: t404

Parameter:

Linear voltage regulated power supplies avoided or stabilized.

Concern:

Linear power supplies (P.S.) are less efficient than switching P.S.s and often require extensive cooling. Switching P.S.s are more popular and have better ripple and dynamic response.

Data Request:

Are only non-linear or stabilized linear power supplies used?

A Weight: 10 B Weight: 0

Action: See sections 14.1 and 14.4.2

Subject: High Power

Parameter Number: t405

Parameter:

Large potential gradients between adjacent pins or test points.

Concern:

If a large voltage or power gradient exists between two pins (such as one 300 volt signal and one 50 millivolt signal), then the higher power signal could induce noise or glitches in the smaller one. Test points should not exist next to high power signal/power pins.

Data Request:

Are all signal levels within 1% of the power of each adjacent pin's signal levels?

A Weight: 10 B Weight: 0

Action: N/A

Subject: High Power

Parameter Number: t406

Parameter:

Hazardous voltages, high level, or RF level signals at test points.

Concern:

Any potentially hazardous signals brought to test points for use during test cause a safety problem. Often special test procedures, test equipment, or extra fixturing need to be used or developed if a potential hazard exists.

Data Request:

Are only non-hazardous signals brought to test points?

A Weight: 45 B Weight: 5

Action: See section 14.1

Subject: High Power

Parameter Number: t407

Parameter:

Accessibility of internal nodes of the supply (potted and oil filled supplies are not accessible).

Concern:

If a component within a power supply fails, then the component may need to be physically probed and will need to be replaced. The ease of accessing internal nodes and replacing components affects test times and test complexity.

Data Request:

Are all power supply internal nodes accessible?

A Weight: 45 B Weight: 3

Action: N/A

Subject: High Power

Parameter Number: t408

Parameter:

Ability to remove magnetic components (transformers, inductors) during test.

Concern:

Magnetic components, such as transformers and inductors, are often removed from a power supply during a portion of power supply testing.

Data Request:

Are all magnetic components removeable during test?

A Weight: 10 B Weight: 0

Action: See section 14.5

Subject: High Power

Parameter Number: t409

Parameter:

Temperature of parts subject to operator contact.

Concern:

If any exposed part of a module that an operator may contact exceeds 60 degrees C, then operator injury could occur, requiring additional safety measures during test.

Data Request:

Does every part subject to operator contact heat up to less than 60 degrees centigrade?

A Weight: 20 B Weight: 0

Action: See section 14.5

Subject: High Power

Parameter Number: t410

Parameter:

Non-self-powered equipment external surfaces at ground potential.

Concern:

External surfaces of externally powered equipment (line power) should be at ground reference for operator safety (excluding antennas and transmission line terminals).

Data Request:

Is the surface of the power supply at ground potential?

A Weight: 25 B Weight: 2

Action: See section 14.3.1

Subject: High Power

Parameter Number: t411

Parameter:

Standard safety protection.

Concern:

Safety protection is a critical factor during the test of high power equipment. The levels of protection listed in the manual are from MIL-STD-454G (reference latest version).

Data Request:

Does standard safety protection exist for high power signals?

A Weight: 50 B Weight: 10

Action: See section 14.3

Subject: High Power

Parameter Number: t412

Parameter:

Storage devices designed to discharge within 2 seconds of power removal.

Concern:

All storage devices in excess of 30 volts should be designed with bleeder resistors or an automatic shorting bar to discharge power within 2 seconds of power removal. Otherwise, an operator may assume that no potential hazards exist while power is off and contact a charged device.

Data Request:

Do all storage devices of >30 volts discharge within 2 seconds of power removal?

A Weight: 40 B Weight: 5

Action: See sections 14.3 and 14.5

Subject: High Power

Parameter Number: t413

Parameter:

High voltage dividers have two equal parallel resistors on the "bottom" of voltage divider.

Concern:

All high voltage signals should be divided and brought to test points through two equal parallel resistors at the "bottom" of a voltage divider. Otherwise, if only one resister were present and it failed open, then the voltage at the test point would be the original high voltage.

Data Request:

Do all high voltage dividers have two equal parallel resistors at the "bottom" of the divider?

A Weight: 35 B Weight: 0

Action: See section 14.3

Subject: High Power

Parameter Number: t414

Parameter:

Access to all high voltage and cascaded transformer taps.

Concern:

If high voltage transformer taps exist, then they can be used as monitoring points. The taps isolate the monitored signal from the main signal (usually at safer voltage levels).

Data Request:

Are all high voltage and cascaded transformer taps accessible?

A Weight: 20 B Weight: 0

Action: N/A

Subject: High Power

Parameter Number: t415

Parameter:

Manipulation of power supply controls at connector pins.

Concern:

If power supply controls, such as gain and safety signals, can be manipulated from signals at a connector, then a test procedure can be made more automated. Thus, requiring fewer operator actions.

Data Request:

Can power supply controls be manipulated from connector signals?

A Weight: 40 B Weight: 0

Action: See section 14.5

Subject: High Power

Parameter Number: t416

Parameter:

Test points at all amplifier stages.

Concern:

Multi-stage amplifiers should have test points at every stage. Otherwise, a failing stage cannot be isolated.

Data Request:

Do test points exist at all amplifier stages?

A Weight: 35 B Weight: 0

Action: See section 14.5

Subject: High Power

Parameter Number: t417

Parameter:

High voltage reversal controls interlocked and accessible.

Concern:

If high voltage reversal controls exist, then they should be exercised during test. Easy access to the reversal controls improves test times and an interlock on the control prevent a powered voltage reversal causing device damage.

Data Request:

Are all high voltage reversal controls interlocked and accessible?

A Weight: 20 B Weight: 0

Action: See section 14.5

Subject: Incircuit

Parameter Number: r951

Parameter:

Tester able to override clocks.

Concern:

Incircuit testers test each component individually by supplying all input signals and monitoring outputs on each chip individually. If a clock signal is not disablable, then clock inputs to downstream devices cannot be controlled by the tester.

Data Request 1:

Enter the number of controllable clocks on the module.

Data Request 2:

Enter the total number of clocks on the module.

A Weight: 50 B Weight: 10

Action: See section 15.5.2

Subject: Incircuit

Parameter Number: r952

Parameter:

Percent of functional nodes accessible by test equipment.

Concern:

Access to functional nodes by test fixture pins is the most important parameter for incircuit test. Device leads and points on components should not act as points for nodal access. Fixture pin pressure on device leads could make a cold solder joint (open) appear functional.

Data Request 1:

Enter the number of functional nodes accessible by test equipment fixture pins.

Data Request 2:

Enter the total number of functional nodes on the module.

A Weight: 50 B Weight: 1

Action: See sections 15.1.2 and 15.5.1

Subject: Incircuit

Parameter Number: r953

Parameter:

Percent access to unused pins of devices (for used and unused devices).

Concern:

An ideal test will test all possible faults of all devices, whether functionally used or not. Unused devices and unused pins in used devices should be tested. Future design changes may use theme or an unused device failure may interfere with a functional device.

Data Request 1:

Enter the number of accessible unused pins on the module.

Data Request 2:

Enter the total number of unused pins on the module.

A Weight: 25 B Weight: 0

Action: See section 15.5.2

Subject: Incircuit

Parameter Number: r954

Parameter:

Number of device pins tied directly to VCC or ground.

Concern:

If a node is hard-wired to VCC or ground (GND), then that node cannot be controlled or observed during incircuit test. Pull-up or pull-down resistors can be used on nodes that must be terminated. Pull-ups are recommended since it is easier for a tester to drive a signal low than high.

Data Request 1:

Enter the number of device pins not tied directly to VCC or ground.

Data Request 2:

Enter the total number of device pins on the module.

A Weight: 30 B Weight: 0

Action: See section 15.5.2

Subject: Incircuit

Parameter Number: r955

Parameter:

Number of uncontrollable feedback loops between components or on individual components.

Concern:

Uncontrollable feedback loops cause a problem in any type of testing. During incircuit testing, they can be made controllable by using tri-states.

Data Request 1:

Enter the number of controllable feedback loops on the module.

Data Request 2:

Enter the total number of feedback loops.

A Weight: 50 B Weight: 5

Action: See section 15.5.2

Subject: Electro-Optics

Parameter Number: t306

Parameter:

UUT requires a clean room or laminar flow bench for aligning, debugging, or testing.

Concern:

A UUT requirement of a clean room or laminar flow bench complicates testing and alignment and may require special training.

Data Request:

Does the UUT not require a clean room or laminar flow bench during debug or testing?

A Weight: 30 B Weight: 0

Action: See section 16.2.1

Subject: Incircuit

Parameter Number: r957

Parameter:

Number of programmable logic devices (PLDs) that are not tri-stateable.

Concern:

PLDs are custom devices that are difficult to manipulate outside of running software generated patterns. Therefore, to disable a PLD, a single tri-state control pin should exist.

Data Request 1:

Enter the number of programmable devices that can be disabled from an accessible pin.

Data Request 2:

Enter the total number of programmable devices.

A Weight: 35 B Weight: 0

Action: See section 15.5.2

Subject: Electro-Optics

Parameter Number: t308

Parameter:

UUT filled with a gas other than air (inert gases such as nitrogen and argon).

Concern:

A UUT filled with a gas other than air requires gas purging before opening and debugging the UUT.

Data Request:

Is the UUT filled only with air and no other gas?

A Weight: 40 B Weight: 3

Action: See section 16.2.1

Subject: Incircuit

Parameter Number: r959

Parameter:

Number of ASICs/microprocessors not tri-stateable.

Concern:

ASICs and microprocessors should have a one pin control for tri-stating their outputs while testing other devices.

Data Request 1:

Enter the number of ASICs and processors that can be tri-stated from an accessible pin.

Data Request 2:

Enter the total number of ASICs and processors.

A Weight: 45 B Weight: 5

Action: See section 15.5.2

Subject: Incircuit

Parameter Number: r960

Parameter:

Number of device types without test patterns or thorough self-tests (excluding PLDs).

Concern:

Many non-custom devices have pre-developed test patterns in an incircuit tester library. A large portion of test development time can be spent on devices without test patterns in the tester library or without patterns accompanying it.

Data Request 1:

Enter the number of device types with tests patterns in the tester library or elsewhere.

Data Request 2:

Enter the total number of device types on the module.

A Weight: 45 B Weight: 2

Action: N/A

Subject: Incircuit

Parameter Number: r961

Parameter:

Number of PLDs without JEDEC files, ABEL files, or fuse equations.

Concern:

In order to develop tests for PLDs, JEDEC files, fuse equations, or ABEL files are necessary.

Data Request 1:

Enter the number of PLDs with JEDEC files, ABLE files, or fuse equations.

Data Request 2:

Enter the number of PLDs on the module.

A Weight: 45 B Weight: 2

Action: N/A

Subject: Incircuit

Parameter Number: r962

Parameter:

Percent device pins on the component side of the module that are accessible by manual probing.

Concern:

If a device fails a test, the next action is usually for the operator to probe the device pins to verify the net and solder connection. Therefore, all device pins should be accessible for manual probing on the component side of the board.

Data Request 1:

Enter the number of device pins accessible for manual probing on the module component side.

Data Request 2:

Enter the total number of device pins on the module.

A Weight: 43 B Weight: 0

Action: See sections 15.1.2 and 15.5.1

Subject: Incircuit

Parameter Number: t951

Parameter:

Board to be conformally coated.

Concern:

All incircuit testers probe points on the surface of a board. In a conformally coated board, test points are covered with a dielectric after passing test. If the board fails in the future, then special preparation to remove the conformal coating is required prior to retest.

Data Request:

Is the module free from conformal coating?

A Weight: 35 B Weight: 0

Action: See sections 15.1.2 and 15.5.1

Subject: Incircuit

Parameter Number: t952

Parameter:

0.25 inch minimum clearance around the module perimeter, free of components or hardware.

Concern:

Components on the perimeter of a board interfere with the gasket used on a vacuum fixture.

Data Request:

Does a 0.25 inch minimum clearance exist on the module perimeter?

A Weight: 20 B Weight: 0

Action: See section 15.5.1

Subject: Incircuit

Parameter Number: t953

Parameter:

Unused ECL component outputs either pulled down on the module or by a programmable load.

Concern:

Unused ECL outputs need to be terminated with a pull down in order for them to be tested. When unterminated ECL device outputs exist, a logic ONE is essentially a tri-stated output and cannot be verified by a tester without a pull-down. (Some testers automatically provide pull-downs).

Data Request:

Do all unused ECL outputs have a pull-down or can pull-downs be supplied by the tester?

A Weight: 25 B Weight: 0

Action: See section 15.5.2

Subject: Incircuit

Parameter Number: t954

Parameter:

No open via or other holes on the module (for vacuum suction).

Concern:

Any open holes on a module that allow air to flow from one side to the other and can interfere with a vacuum fixture. Usually a module with holes is covered with a sheet of plastic to improve the vacuum fixture actions but blocks nodes during manual probing.

Data Request:

Is the module free from any open vias or other holes?

A Weight: 40 B Weight: 2

Action: See section 15.5.1

Subject: Incircuit

Parameter Number: t955

Parameter:

Distribute test pads/components evenly across board (to distribute test fixture pin pressure).

Concern:

If test pads are not evenly distributed, then pin force from the fixture will vary. This could cause board bending or warping and degrade the effectiveness of the fixture.

Data Request:

Are the test pads and component pins that are probed by the fixture, evenly distributed?

A Weight: 40 B Weight: 0

Action: See section 15.5.1

Subject: Incircuit

Parameter Number: t956

Parameter:

Module warp or bend.

Concern:

A warped module may have a less effective vacuum seal and some fixture pins may not make good contact. Stiffeners on the module can negate this problem.

Data Request:

Is any bending or warpage of the module less than 0.25 inches?

A Weight: 10 B Weight: 0

Action: See section 15.5.1

Subject: Incircuit

Parameter Number: t957

Parameter:

Test of ceramic substrates on a vacuum fixture.

Concern:

Ceramic substrate boards are susceptible to damage when placed on a vacuum fixture due to their rigidity. A ceramic substrate usually requires a custom fixture for incircuit test.

Data Request:

If a vacuum fixture is used, is the module substrate a material other than ceramic?

A Weight: 10 B Weight: 0

Action: See section 15.5.1

Subject: Incircuit

Parameter Number: t958

Parameter:

Total node count under 2700.

Concern:

Some incircuit testers cannot test boards with more than 2700 nodes. Even if the tester can handle the node count, fixture wiring and rework become much more difficult with more than 2700 nodes.

Data Request:

Does the module have less than 2700 nodes?

A Weight: 15 B Weight: 0

Action: See section 15.5.1

Subject: Incircuit

Parameter Number: t959

Parameter:

Module size limited to 10 x 12 inches.

Concern:

Modules larger than 10 x 12 inches are difficult to fixture using a standard fixture assembly. Odd shaped boards also need to be within 10 x 12 inches.

Data Request:

Are the dimensions of the module less than 10 x 12 inches?

A Weight: 25 B Weight: 0

Action: See section 15.5.1

Subject: Incircuit

Parameter Number: t960

Parameter:

Lead trimming device leads that contact the test fixture.

Concern:

Incircuit test points usually use soldered dip legs on the solder side of a board. Care should be taken to trim the device legs properly so they do not extend significantly past the solder. Otherwise, probe pins of the test fixture could be damaged.

Data Request:

Are all dip and other device leads that contact the test fixture trimmed?

A Weight: 20 B Weight: 0

Action: See section 15.5.1

Subject: Incircuit

Parameter Number: t961

Parameter:

Use at least two diametrically opposed 0.125 inch diameter tooling holes registered to the artwork.

Concern:

Usually, module alignment to a fixture during incircuit test uses the module tooling holes. If tooling holes are not accurate, then the reliability of fixture pins making contact with test points is poor. Also, small diameter tooling hole pins bend easily.

Data Request:

Do at least two diametrically opposed 0.125 inch diameter tooling holes exist?

A Weight: 50 B Weight: 10

Action: See section 15.5.1

Subject: Incircuit

Parameter Number: t962

Parameter:

Tooling hole locations and all test points included on a drill tape.

Concern:

Fixture development requires knowledge of the exact locations of tooling holes and points to be probed. Most fixture drill tools can load this data from a drill tape, which is less error prone than manual data entry.

Data Request:

Are the tooling hole locations and test points included on a drill tape?

A Weight: 40 B Weight: 0

Action: See section 15.5.1

Subject: Incircuit

Parameter Number: t963

Parameter:

Wires routed on the solder side of the module.

Concern:

Wires placed on the solder side of a module create a potential probe problem. Placement of the wires or adhesive used to tack down the wires might block a test point. If such wires must be used, process documentation should be specific to avoid this problem.

Data Request:

Is the solder side of the module free from any wire routing?

A Weight: 30 B Weight: 0

Action: See section 15.5.1

Subject: Incircuit

Parameter Number: t964

Parameter:

All components on one side of the module (for normal bed-of-nails fixturing).

Concern:

All components should be located on one side of a module to ease manual probing.

Data Request:

Are all components located on one side of the module?

A Weight: 45 B Weight: 5

Action: See section 15.5.1

Subject: Incircuit

Parameter Number: t965

Parameter:

Every node to contact test fixture pins located on the solder side of the module.

Concern:

Every node test point (test pad, dip solder side leg, via, etc.) should be located on the side of the board opposite from components (solder side). This allows the use of a standard bed-of-nails single-sided vacuum fixture - the most inexpensive and practical fixture type.

Data Request:

Is every node that will contact the test fixture located on the solder side of the module?

A Weight: 50 B Weight: 5

Action: See section 15.5.1

Subject: Incircuit

Parameter Number: t966

Parameter:

Provide individual pull-up or pull-down resistors on all terminated or unused control lines.

Concern:

Terminated control lines need to have a pull-up or pull-down resistor so the tester can manipulate them. Caution should be taken to ensure that each control line is the only signal on its pull-up/down to avoid accidentally settling it during other tests.

Data Request:

Do all terminated and unused control lines have individual pull-up or pull-down resistors?

A Weight: 40 B Weight: 3

Action: See section 15.5.2

Subject: Incircuit

Parameter Number: t967

Parameter:

Test points exist at connector pins.

Concern:

It is desirable to locate test points on nodes containing a connector at the connector via rather than locating them at component vias. The connection of the run at the connector to components on the module can be verified by using this approach.

Data Request:

Do test fixture probe points for nodes with connector pins exist at the connector pins?

A Weight: 10 B Weight: 0

Action: N/A

Subject: Incircuit

Parameter Number: t968

Parameter:

Evenly distributed ground and power test points.

Concern:

During incircuit test, fixture probe pins make power and ground connections. Many power and ground connections should exist to properly supply them and so excessive current will not travel through any probe pin. They also should be evenly distributed to help limit noise.

Data Request:

Do power and ground test points exist within 1 inch of every device on the module?

A Weight: 25 B Weight: 0

Action: N/A

Subject: Incircuit

Parameter Number: t969

Parameter:

Isolation of analog and digital circuits.

Concern:

Some means of isolating analog and digital circuits is necessary so that they can be independently tested. Circuits can be isolated by using resistors or tri-stateable devices between them.

Data Request:

Are analog and digital circuits isolated on the module? (Can they be tested independently?)

A Weight: 35 B Weight: 0

Action: See section 15.5.2

Subject: Incircuit

Parameter Number: t970

Parameter:

Use of the maximum device fan-out capability in the module.

Concern:

When test equipment monitors a signal, it acts as an extra load on that node. Therefore, nodes should be designed to handle at least 1 additional fan-out.

Data Request:

Are all devices designed to handle at least one additional fan-out?

A Weight: 10 B Weight: 0

Action: See section 15.5.2

Subject: Incircuit

Parameter Number: t971

Parameter:

Test points at least 200 mils from components >200 mils tall and 18 mils from anything else.

Concern:

Often devices > 200 mils tall require milling or routing of an incircuit test fixture. To allow for this, test points should be located outside the milling region - 200 mils away from tall devices. (Devices over 255 mils tall should be avoided).

Data Request:

Are all test points at least 200 mils from components >200 mils tall & 18 mils from anything else?

A Weight: 30 B Weight: 0

Action: See section 15.5.1

Subject: Incircuit

Parameter Number: t972

Parameter:

Memory initializable by a single or several pins in 16 or fewer clock pulses.

Concern:

Every memory device needs to be initialized before supplying test vectors. A single pin for initialization should exist at all sequential devices. If a power-up reset exists, it should be designed so that the tester can control it.

Data Request:

Can all memory or sequential devices be initialized by one or several accessible pins in <16 pulses?

A Weight: 45 B Weight: 10

Action: See section 15.5.2

Subject: Incircuit

Parameter Number: t973

Parameter:

Test pads and all points to be accessed reside on a 100 mil grid array.

Concern:

Placing all points to be probed by a tester on a 100 mil grid array simplifies fixturing and makes it more reliable. Also, 100 mil probes can be used, which are much more reliable, less expensive, more accurate, and last longer than smaller probes.

Data Request:

Are all test pads and test points on a 100 mil grid array?

A Weight: 50 B Weight: 5

Action: See section 15.5.1

Subject: Incircuit

Parameter Number: t974

Parameter:

Test points covered with solder and test points/via holes have a minimum diameter of 35 mils.

Concern:

A minimum diameter of 35 mils for all points to be probed by 100 mil probes and 45 mils for all points to be probed by smaller probes is required. These values take into account tolerances of the probes, fixture, artwork, etc. to achieve less than 1 probe miss per 1000 attempts on average.

Data Request:

Do all test points have a minimum diameter of 35 mils and do they have a solder covering?

A Weight: 25 B Weight: 0

Action: See section 15.5.1

Subject: Incircuit

Parameter Number: t975

Parameter:

LEDs easy to test visually with the board in the fixture.

Concern:

If LEDs exist, they should be able to be checked visually while the board is in the fixture.

Data Request:

Can all LEDs on the module be checked visually while the module is in the test fixture?

A Weight: 45 B Weight: 3

Action: N/A

Subject: Incircuit

Parameter Number: t976

Parameter:

Ability to initialize non-disablable PLD, LSI, and VLSI TTL devices to all ONEs and ECL outputs to all logic ONEs.

Concern:

If a complex device cannot be tri-stated, then all the device outputs should be able to be set high during the test of down-stream devices. This is especially true for ECL devices. Forcing a device's output to a logic ZERO requires less current to backdrive it.

Data Request:

Can all PLD, LSI, and VLSI TTL non-tristateable devices be preset to logic ONE?

A Weight: 10 B Weight: 0

Action: See section 15.5.2

Subject: Incircuit

Parameter Number: t977

Parameter:

Current at any test point under 1 amp.

Concern:

Most text fixture pins are designed for currents under 1 amp.

Data Request:

Is the current at every test point under 1 amp?

A Weight: 35 B Weight: 0

Action: N/A

Subject: Electro-Optics

Parameter Number: r301

Parameter:

Accessibility of UUT optical signals.

Concern:

Some UUTs have optical signals that are not accessible when the UUT covers are on. Unaccessible signals increase the times required to align, integrate, debug, and test the UUT.

Data Request 1:

Enter the number of electro-optic signals that are accessible.

Data Request 2:

Enter the total number of electro-optic signals in the UUT.

A Weight: 50 B Weight: 1

Action: See section 16.2.1

Subject: Electro-Optics

Parameter Number: r302

Parameter:

Access to individual electro-optic module signals.

Concern:

Access to individual electro-optic sub-modules such as photo-multipliers, vidicons, and CCDs is necessary for isolation of electro-optic components.

Data Request 1:

Enter the number of electro-optic modules that are individually accessible.

Data Request 2:

Enter the total number of electro-optic modules in the module assembly.

A Weight: 45 B Weight: 2

Action: See section 16.2.1

Subject: Electro-Optics

Parameter Number: t301

Parameter:

Design reviewed for UUT safety.

Concern:

Every electro-optic circuit should be designed with safety precautions to prevent functional or test operator injury. Some areas of concern are: high power, toxic gases, dyes, radiation, high temperature, and accidental contact with a high power beam.

Data Request:

Has the design been reviewed for safety?

A Weight: 50 B Weight: 7

Action: See section 16.2.1

Subject: Electro-Optics

Parameter Number: t302

Parameter:

Access to electro-optic source beam.

Concern:

Module alignment can be seriously hampered if there is no means of viewing the beam at each aperture. This is especially true for invisible and high power beams.

Data Request:

Is the source beam accessible and visible for beam alignment?

A Weight: 45 B Weight: 5

Action: See section 16.2.1

Subject: Electro-Optics

Parameter Number: t303

Parameter:

Correct operation of UUT with covers removed.

Concern:

Often UUT covers designs include interlocks or have optics mounted to them. Removal of these covers requires test equipment to supply any missing functions or the UUT will not work properly.

Data Request:

Will the UUT operate correctly with the covers removed?

A Weight: 35 B Weight: 0

Action: See section 16.2.1

Subject: Electro-Optics

Parameter Number: t304

Parameter:

UUT specifications available.

Concern:

Besides the regular required documentation for electrical systems, electro-optic UUTs need alignment instructions, optical criteria specifications, and error analysis specifications.

Data Request:

Are all the required electro-optic specifications available?

A Weight: 40 B Weight: 4

Action: N/A

Subject: Electro-Optics

Parameter Number: t305

Parameter:

UUT optics and electronics partitioned.

Concern:

Partitioning helps to isolate problems to individual parts, especially if external activation is possible.

Data Request:

Has the UUT been partitioned to separate source, optic train, sensor, and electronics?

A Weight: 50 B Weight: 5

Action: See section 16.2

Subject: Incircuit

Parameter Number: r956

Parameter:

Percent disablable devices and devices on a bus that are tri-stateable.

Concern:

Every tri-stateable device or device on a bus should have a tri-state control line accessible by the tester. This makes disabling devices connected to the device being tested much simpler.

Data Request 1:

Enter the number of devices that have a disable signal or are on a bus that are tri-stateable.

Data Request 2:

Enter the total number of devices that have a disable signal or are on a bus.

A Weight: 45 B Weight: 2

Action: See section 15.5.2

Subject: Electro-Optics

Parameter Number: t307

Parameter:

UUT spatial response measurement possible.

Concern:

UUT spatial response adjustments can be done quickly by using automated measurement circuits.

Data Request:

Can UUT spatial response be measured?

A Weight: 20 B Weight: 0

Action: See section 16.2.1

Subject: Electro-Optics

Parameter Number: t308

Parameter:

UUT filled with a gas other than air (inert gases such as nitrogen and argon.)

Concern:

A UUT filled with a gas other than air requires gas purging before opening and debugging the UUT.

Data Request:

Is the UUT filled with a gas other than air?

A Weight: 40 B Weight: 3

Action: See section 16.2.1

Subject: Electro-Optics

Parameter Number: t309

Parameter:

Temperature compensator available for optics.

Concern:

Some modules need to operate at temperatures that require temperature compensation to maintain the optical alignment.

Data Request:

Does the UUT have a temperature compensator for the UUT optics?

A Weight: 20 B Weight: 0

Action: See section 16.2.1

Subject: Electro-Optics

Parameter Number: t310

Parameter:

Auto-focus available.

Concern:

After electro-optic UUT alignment, the image or signal may still require focusing on the sensor. An auto-focusing module greatly reduces the effort to do so manually.

Data Request:

Does the UUT have an auto-focus?

A Weight: 20 B Weight: 0

Action: See section 16.2.1

Subject: Electro-Optics

Parameter Number: t311

Parameter:

External course and fine focus adjustment availability.

Concern:

External course and fine focus adjustments allow an operator to over-ride a faulty auto-focus or set the auto-focus into its mid-range.

Data Request:

Are external course and fine focus adjustments available?

A Weight: 30 B Weight: 0

Action: See section 16.2.1

Subject: Electro-Optics

Parameter Number: t312

Parameter:

UUT Internal reference or built-in calibration.

Concern:

Internal references (used in Doppler modules) or built-in calibration, such as a black body (with an emissivity of unity), provide a measurement reference during test.

Data Request:

Does the UUT have an internal reference signal or built-in calibration?

A Weight: 35 B Weight: 0

Action: See section 16.2.1

Subject: Electro-Optics

Parameter Number: t313

Parameter:

Ability to align internal components elsewhere and place in electro-optic UUT without UUT re-alignment.

Concern:

Electro-optic component alignment is simpler if done external to the UUT. However, even if external alignment of the components is possible, the UUT may need re-alignment after replacing the components.

Data Request:

Can optical components be externally aligned and placed in the UUT without UUT re-alignment?

A Weight: 40 B Weight: 0

Action: See sections 16.2.1.1 and 16.4.1

Subject: Electro-Optics

Parameter Number: t314

Parameter:

Device mobility requirements.

Concern:

Devices with more then two degrees of freedom complicate the alignment procedure.

Data Request:

Do all devices require two degrees of freedom or less?

A Weight: 20 B Weight: 0

Action: See section 16.2

Subject: Electro-Optics

Parameter Number: t315

Parameter:

Automatic UUT alignment.

Concern:

Automated UUT alignment will reduce the test time of a UUT. A quadrant detector can make automatic UUT alignment possible.

Data Request:

Does the UUT have automated alignment?

A Weight: 25 B Weight: 0

Action: See sections 16.2.1 and 16.4.1

Subject: Electro-Optics

Parameter Number: t316

Parameter:

Systematic optical adjustments and alignment.

Concern:

Optical UUT should be able to be aligned in "one pass". If more than one pass is necessary to align the UUT, then more adjustment errors are possible.

Data Request:

Can all optic adjustments and alignment be completed in one pass?

A Weight: 40 B Weight: 4

Action: See section 16.2.1.1

Subject: Electro-Optics

Parameter Number: t317

Parameter:

Adjustment mechanisms fine tuning.

Concern:

Adjustment mechanisms need to be designed for slow and smooth movements for fine adjustments. If mechanisms are not properly designed for fine tuning, then alignment time may be long.

Data Request:

Is fine tuning possible for all adjustable mechanisms?

A Weight: 20 B Weight: 0

Action: N/A

Subject: Electro-Optics

Parameter Number: t318

Parameter:

Laser discharge current sensor.

Concern:

The only way to see all lit discharges is to have a separate sensor on each discharge.

Data Request:

Does each discharge have a separate current sensor?

A Weight: 45 B Weight: 0

Action: N/A

Subject: Electro-Optics

Parameter Number: t319

Parameter:

Ability to measure source/laser voltage.

Concern:

A key parameter in determining the health of a source/laser is the measurement of its voltage while operating. Usually this is a high voltage measurement and a voltage divider network is necessary.

Data Request:

Can each source/laser voltage be measured?

A Weight: 20 B Weight: 0

Action: N/A

Subject: Electro-Optics

Parameter Number: t320

Parameter:

Laser/source power-on check.

Concern:

A test point at a source output in the form of a beam splitter or detector can check if a laser is on.

Data Request:

Does the laser/source have a power-on check signal or lamp?

A Weight: 20 B Weight: 0

Action: N/A

Subject: Electro-Optics

Parameter Number: t321

Parameter:

Ability to sample a flowed gas laser mixture of gases.

Concern:

Flowed gas lasers need very precise gas combinations to work properly. A scheme to sample the mixture at the module level periodically can ease laser troubleshooting.

Data Request:

Can the mixture be sampled in the flowed gas laser?

A Weight: 25 B Weight: 0

Action: N/A

Subject: Electro-Optics

Parameter Number: t322

Parameter:

Visual inspection of optics.

Concern:

Visual inspection for gross external and internal optical defects decrease troubleshooting time.

Data Request:

Can all optics be visually inspected after installation?

A Weight: 20 **B Weight:** 0

Action: See sections 16.3.5 and 16.4.1

Subject: Electro-Optics

Parameter Number: t323

Parameter:

High pressure ARC/sources shielding.

Concern:

High pressure ARC/sources often have gas fillings with pressures of 250 atmospheres or more. They are extremely fragile and present an explosion hazard even when cold. Shielding and warning labels are necessary.

Data Request:

Are all high pressure ARC/sources shielded?

A Weight: 50 B Weight: 8

Action: See sections 16.3.1 and 16.3.5

Subject: Electro-Optics

Parameter Number: t324

Parameter:

UUT process condition monitoring.

Concern:

A module containing source/optics/sensors require test points or BIT to measure various conditions, such as output power, high/low temperature, and liquid/gas flow rates and temperatures.

Data Request:

Does process condition monitoring exist?

A Weight: 40 B Weight: 3

Action: See section 16.3.5

Subject: Electro-Optics

Parameter Number: t325

Parameter:

Ability to monitor output beam at source (alignment, mode structure, spot size, diameter).

Concern:

Monitoring a source beam for mode structure, spot size, diameter, and alignment (with respect to the module) can quickly isolate individual source problems.

Data Request:

Can the output beam be monitored at its source for beam characteristics?

A Weight: 45 B Weight: 5

Action: See section 16.2.1

Subject: Electro-Optics

Parameter Number: t326

Parameter:

Ground reference on laser mirror mounts (safety during test).

Concern:

Laser mirror mounts that can reach a high voltage are dangerous and should be avoided. They represent an extreme risk to the operator during alignment.

Data Request:

Do the laser mirror mounts have a ground reference?

A Weight: 45 B Weight: 5

Action: See section 16.3.5

Subject: Electro-Optics

Parameter Number: t327

Parameter:

Ability to test with hazards removed (laser off during current regulator test, etc.).

Concern:

A high power laser with optics and detectors should have provisions to test optics and detectors with the laser turned off.

Data Request:

Can UUT be tested with all hazards removed?

A Weight: 35 B Weight: 0

Action: See section 16.3.5

Subject: Electro-Optics

Parameter Number: t328

Parameter:

Laser/source beam direction manipulation.

Concern:

A source beam may need to be aligned to the module chassis before mounting optical components. This usually is done with the optic components removed.

Data Request:

Have provisions been made for directing the laser/source beam out of module without all optics?

A Weight: 35 B Weight: 0

Action: See section 16.4.3

Subject: Electro-Optics

Parameter Number: t329

Parameter:

Avoid opaque optic components.

Concern:

Optics that are visibly transparent allow much easier alignment than opaque optics, such as geranium.

Data Request:

Are all optics visibly transparent?

A Weight: 15 B Weight: 0

Action: See sections 16.4.1 and 16.4.3

Subject: Electro-Optics

Parameter Number: t330

Parameter:

Ability to align optics manually.

Concern:

Modules designed for manual unaided eye alignments are easier and faster to align then those requiring micrometers.

Data Request:

Can optics be aligned manually?

A Weight: 25 B Weight: 0

Action: See section 16.4.3

Subject: Electro-Optics

Parameter Number: t331

Parameter:

Zoom lense focus without power.

Concern:

The optic train is much easier to focus when any zoom lenses can be focuses without module power on, especially when main system has a problem.

Data Request:

Can the zoom lense be focused with the UUT power turned off?

A Weight: 35 B Weight: 0

Action: See section 16.4.3

Subject: Electro-Optics

Parameter Number: t332

Parameter:

Use of prisms.

Concern:

A prism has fewer optic parts than individual optics used to perform the same function. As a result, prisms take less time to align.

Data Request:

Are prisms used rather than separate optical components?

A Weight: 25 B Weight: 0

Action: See section 16.4.1.1

Subject: Electro-Optics

Parameter Number: t333

Parameter:

Ability to test aspherics independently.

Concern:

Aspherics are optical components that are not spherical on either or both surfaces. These components are difficult to test if they are not tested independently.

Data Request:

Can aspherics be independently tested?

A Weight: 20 **B Weight:** 0

Action: See section 16.4.1.1

Subject: Electro-Optics

Parameter Number: t334

Parameter:

Use of prefocused optics at I/O ends of fiber-optics.

Concern:

Fiber-optics with prefocused lenses attached make fiber alignment easier (lenses do not need to be aligned to fiber). They also allow for more light to enter directly into the fiber.

Data Request:

Have prefocused optics been used at I/O ends of the fiber- optics?

A Weight: 35 B Weight: 0

Action: See section 16.4.2

Subject: Electro-Optics

Parameter Number: t335

Parameter:

Fiber-optics conform to a present standard (including EIA FO-6 + FO-2, ANSI, and IEEE).

Concern:

Fiber-optics need to conform to a standard to guarantee quality and compatibility to existing test equipment.

Data Request:

Do the fiber-optics conform to a standard?

A Weight: 45 B Weight: 5

Action: See section 16.4.2

Subject: Electro-Optics

Parameter Number: t336

Parameter:

Fiber-optic connectors conform to an industry standard (such as biconic, FC, PC, and DIN/IEC).

Concern:

Fiber-optic connectors need to conform to a standard to ensure compatibility with existing test equipment.

Data Request:

Do the fiber-optic connectors conform to a standard?

A Weight: 40 B Weight: 3

Action: N/A

Subject: Electro-Optics

Parameter Number: t337

Parameter:

Detector/sensor assembly mechanical constraints.

Concern:

UUTs are much easier to align using side looking detector assemblies mounted inside dewars rather than bottom looking detectors.

Data Request:

Has the detector assembly been made so the detector looks from the side?

A Weight: 35 B Weight: 0

Action: N/A

Subject: Electro-Optics

Parameter Number: t338

Parameter:

Detector lense window construction.

Concern:

Detector lenses, which are part of the detector assembly, are easier to align because one less component needs to be aligned.

Data Request:

Is the detector lense or window part of the detector assembly?

A Weight: 35 B Weight: 0

Action: See section 16.5.1

Subject: Electro-Optics

Parameter Number: t339

Parameter:

Beam steering during detector alignment.

Concern:

Moving an entire detector assembly for alignment is much more difficult and risky than only moving a source beam.

Data Request:

Can the beam be steered to the detector by optics during detector alignment?

A Weight: 25 B Weight: 0

Action: See section 16.5.1

Subject: Electro-Optics

Parameter Number: t340

Parameter:

Size of detector chip entrance window.

Concern:

Detector chips, which are smaller than the optical dewar window, are difficult to align (make sure beam covers entire detector chip). Alignment is easier if the detector chip is as large as the entrance window.

Data Request:

Is the detector chip larger than the entrance window?

A Weight: 15 B Weight: 0

Action: N/A

Subject: Electro-Optics

Parameter Number: t341

Parameter:

Ability to remove the sensor/detector electrically.

Concern:

A problem can quickly be isolated to the pre-amp or detector if a test signal can electrically remove and replace the sensor or detector.

Data Request:

Can the sensor/detector be electrically removed from the circuit?

A Weight: 45 B Weight: 3

Action: See section 16.5.1

Subject: Others

Parameter Number: r351

Parameter:

Number of critical signals brought to the exterior of the top assembly or to test points for quick ATE connection.

Concern:

Critical signals (I/O, power, ground, input, pick-off points in servo loops, etc.) should be accessible at a connector so test equipment can directly access them. With direct access to these signals many tests can be automated and may not require manual probing.

Data Request 1:

Enter the number of critical signals that are accessible at a connector.

Data Request 2:

Enter the total number of critical signals.

A Weight: 50 B Weight: 3

Action: N/A

Subject: Others

Parameter Number: r352

Parameter:

Panels available to provide visual and manual access to components.

Concern:

Panels provide visual and manual access to critical UUT areas. This enables periodic checking of mechanical loading such as engine mounts, wing struts, chains, and ropes that are subject to wear and difficult to test by BIT.

Data Request 1:

Enter the number of components subject to wear that are visually and manually accessible.

Data Request 2:

Enter the total number of components that are subject to wear.

A Weight: 45 B Weight: 2

Action: See section 17.8.2

Subject: Others

Parameter Number: r353

Parameter:

Critical controls provided with (non-bypassable) visual and audible alarms when manually set to unsafe limits.

Concern:

During test and test development, an operator could accidently set critical control signals or switches to levels that are unsafe and possible cause operator injury or material damage. An audible and visual alarm can warn the operator of this situation.

Data Request 1:

Enter the number of critical control signals with alarms.

Data Request 2:

Enter the total number of critical control signals that can cause injury or material damage.

A Weight: 50 B Weight: 4

Action: See section 17.10

Subject: Others

Parameter Number: r354

Parameter:

Operator protected from all accessible moving parts (gears, chain and conveyor drives, levers, shafts, etc.).

Concern:

Moving parts that the operator may come in contact with must have a means to protect the operator from possible injury. An operator guard, shield, or some type of physical barrier can be used to protect an operator from contacting the moving part.

Data Request 1:

Enter the number of moving parts that the operator is protected from contacting.

Data Request 2:

Enter the total number of moving parts.

A Weight: 45 B Weight: 3

Action: See section 17.1.1

Subject: Others

Parameter Number: t351

Parameter:

Access to liquid and gas test points, valves, and filters for physical measurements.

Concern:

Access to liquid and gas test points, valves, and filters decreasing test times needed for pressure, level, contamination, and other measurements. These test points may be accessible through filtered and quick disconnect (no-spill) ports.

Data Request:

Is physical access available to all liquids and gases for measurements?

A Weight: 45 B Weight: 0

Action: See section 17.2

Subject: Others

Parameter Number: t352

Parameter:

Modifications to UUT while running tests.

Concern:

Some UUTs require modifications such as clamps, fitting removals or additions when manipulating access points during test. Such modifications increase the test times and costs.

Data Request:

Are any UUT modifications required while running a UUT test?

A Weight: 40 B Weight: 0

Action: See section 17.10

Subject: Others

Parameter Number: t353

Parameter:

Access to motor shafts or extensions in UUTs with transmissions or gears.

Concern:

Backlash and compliance measurements are critical tests for transmission and geared uuts (fixed and adjustable). Motor shafts/extensions need to be accessible at I/O and intermediate points for these tests.

Data Request:

If the UUT contains transmissions or gears, are motor shafts/extensions accessible?

A Weight: 35 B Weight: 0

Action: See section 17.4

Subject: Others

Parameter Number: t354

Parameter:

UUT accessible for alignment (nulling) and calibration.

Concern:

UUTs such as gyros/accelerometers (in inertial guidance systems) that require alignment or calibration must provide access to all control points needed to calibrate or align.

Data Request:

Are all control points needed for calibration and alignment accessible?

A Weight: 40 B Weight: 0

Action: See section 17.7

Subject: Others

Parameter Number: t355

Parameter:

Access to test points and adjustments without introducing contamination.

Concern:

UUTs need to have their test points designed in such a way as not to introduce contamination.

Data Request:

Are test points protected from introducing contaminants when being used?

A Weight: 45 B Weight: 2

Action: See section 17.10

Subject: Others

Parameter Number: t356

Parameter:

Bearing race support.

Concern:

Precision bearings have run-in, spin-up, and spin-down test requirements. Inner and outer bearing races must have enough strength, stiffness, and dimensional stability to support themselves without using a mounting structure or support. Otherwise, they require test adapter supports

---

Data Request:

Are bearing races self supporting and not have to use a mounting or other structure for support?

A Weight: 30 B Weight: 0

Action: See sections 17.8 and 17.10

Subject: Others

Parameter Number: t357

Parameter:

Use of VLSI digital synchro/resolvers tachometers.

Concern:

Digital VLSI synchro/resolvers tachometers are easier to test (no moving parts) and more accurate than their analog counterparts.

Data Request:

If tachometers are used, are they digital as opposed to analog?

A Weight: 20 B Weight: 0

Action: See section 17.10

Subject: Others

Parameter Number: t358

Parameter:

External temperature monitor test points located before pressure reducing valve.

Concern:

Placing external temperature test points after pressure reducing valves reduces gas pressure and may give incorrect or inconsistent temperature readings.

Data Request:

Are all external temperature monitor test points located before pressure reducing valves?

A Weight: 20 B Weight: 0

Action: See section 17.10

Subject: Others

Parameter Number: t359

Parameter:

Software/firmware has a modular top-down structure with comments.

Concern:

Modular top-down structured software/firmware with comments should meet any one of several industry standards including MIL-STD-2167A, 2168, or internal company standards if any. This avoids confusion in interpreting code and decreases test development and debug times.

Data Request:

Does all software/firmware have a modular top-down structure with comments?

A Weight: 40 B Weight: 2

Action: See section 17.9.2

Subject: Others

Parameter Number: t360

Parameter:

UUTs with air flow use filter/regulator/lubricator as a single package module.

Concern:

UUTs with air flow use filters, regulators (for pressure), and lubricators. These elements can be obtained in one package with independently testable units. They are easy to replace and reduce the need for separate circuits to implement these parts.

Data Request:

If UUT contains air flow, is a single package filter/-regulator/lubricator used?

A Weight: 25 B Weight: 0

Action: See section 17.10

Subject: Others

Parameter Number: t361

Parameter:

Use of pneumatic actuators.

Concern:

When compressed air is available, pneumatic actuators should be used rather than electronic actuators. Unlike electronic actuators, pneumatic actuators do not require power and are not susceptible to the problems associated with electronic devices.

Data Request:

If actuators are used and compressed air is available, are pneumatic actuators used?

A Weight: 15 B Weight: 0

Action: See section 17.3

Subject: Others

Parameter Number: t362

Parameter:

Periodic fluid contamination level inspection.

Concern:

Visual inspection (besides quick removal) and pressure indicators are needed in a non-bypass filter. Tests for periodic fluid contamination level inspection (especially in pressure fittings for recirculating systems) use them.

Data Request:

Are visual fluid contamination level inspections possible?

A Weight: 20 B Weight: 0

Action: See section 17.2

Subject: Others

Parameter Number: t363

Parameter:

Use of toxic substances.

Concern:

Toxic substances always provide hazards for personnel that work on the UUT. They require test adapter and program warning messages and precautions, which increase adapter and test program costs.

Data Request:

Is the UUT free from the use of any toxic substances?

A Weight: 50 B Weight: 10

Action: See section 17.1.1

Subject: Others

Parameter Number: t364

Parameter:

Ability to test explosive UUTs repeatedly without a danger of explosion.

Concern:

Squibs, igniters/detonators, and Safety and Arming devices (S&A) can cause fatal injury if accidently triggered during a UUT test.

Data Request:

Are all potentially explosive devices prevented from accidental detonation during test?

A Weight: 50 B Weight: 10

Action: see section 17.1.2

Subject: Others

Parameter Number: t365

Parameter:

All explosive devices designed not to detonate due to mis-assembly during integration, test, or debug.

Concern:

This requirement results in more design time, but is essential to protect assembly and test personnel.

Data Request:

Are all explosive devices designed so that they cannot detonate if improperly assembled?

A Weight: 45 B Weight: 5

Action: See section 17.1.2

Subject: Others

Parameter Number: t366

Parameter:

UUT complies with OSHA safety standards.

Concern:

OSHA standards protect test personnel and UUT operators from hazardous conditions. Every UUT should comply with these standards as a minimum requirement.

Data Request:

Does the UUT comply with all OSHA safety standards?

A Weight: 50 B Weight: 10

Action: See section 17.1.1

APPENDIX C

MANUAL ANALYSIS FORMS

FAILURE RATE TABLE FORM

Subject Weight

= Sum of [(component(i) Failure Rate) * ('# of components(i)')]

Where (i) consists each component type within a subject.

SUBJECT WEIGHTS

General Digital Weight.. _____
VLSI Weight..... _____
Processor Weight..... _____
Memory Weight..... _____
General Analog..... _____
High Power..... _____
High Frequency..... _____
Electro-Optics..... _____
Others..... _____

SUBJECT VALUE TABLE FC.....

Subject Weight

= [(Subject Value) * ('# of components')]

(Note: Subject Values can be found in Appendix E, page E-2)

SUBJECT WEIGHTS

General Digital Weight.. _____
VLSI Weight..... _____
Processor Weight..... _____
Memory Weight..... _____
General Analog..... _____
High Power..... _____
High Frequency..... _____
Electro-Optics..... _____
Others..... _____

SUBJECT TR AND CF FORM
TOP LEVEL

Top Level Ratio Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
-	.....	.....	.....	-	-	.....	.....

Top Level True/False Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
T251	.....	.....	.....	50	10	.....	.....
T252	.....	.....	.....	40	0	.....	.....
T253	.....	.....	.....	50	10	.....	.....
T254	.....	.....	.....	10	0	.....	.....
T255	.....	.....	.....	35	0	.....	.....
T256	.....	.....	.....	45	4	.....	.....
T257	.....	.....	.....	25	0	.....	.....
T258	.....	.....	.....	30	0	.....	.....
T259	.....	.....	.....	40	2	.....	.....
T260	.....	.....	.....	5	0	.....	.....
T261	.....	.....	.....	20	0	.....	.....
T262	.....	.....	.....	15	0	.....	.....

AWeight Total = ____ for status = Y Alg A = _____ Results Total

AWeight Total = _____ for status = Y or C Alg B = _____ Results Total

SUBJECT TR AND CF FORM
TOP LEVEL
(continued)

Top Level Testability Rate (TR)

$$= \frac{\text{(Alg A Result Total)}}{\text{(AWeight Total for status = Y)}} * 100 - \text{(Alg B Results Total)}$$

$$= \frac{.....}{.....} * 100 - ..... = ...$$

Top Level Credibility Factor (CF)

$$= \frac{\text{(AWeight Total for status = Y)}}{\text{(AWeight Total for status = Y or C)}} * 100$$

$$= \frac{.....}{.....} * 100 = ...$$

SUBJECT TR AND CF FOR... SYSTEM

System Ratio Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
R001	.....	.....	.....	20	0	.....	.....
R002	.....	.....	.....	45	2	.....	.....
R003	.....	.....	.....	35	0	.....	.....
R004	.....	.....	.....	50	8	.....	.....
R005	.....	.....	.....	40	0	.....	.....
R006	.....	.....	.....	50	3	.....	.....
R007	.....	.....	.....	50	6	.....	.....

System True/False Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
T001	.....	.....	.....	40	0	.....	.....
T002	.....	.....	.....	20	0	.....	.....
T003	.....	.....	.....	20	0	.....	.....
T004	.....	.....	.....	50	3	.....	.....
T005	.....	.....	.....	40	0	.....	.....
T006	.....	.....	.....	45	3	.....	.....
T007	.....	.....	.....	10	0	.....	.....
T008	.....	.....	.....	15	0	.....	.....
T009	.....	.....	.....	5	0	.....	.....
T010	.....	.....	.....	10	0	.....	.....
T011	.....	.....	.....	40	3	.....	.....
T012	.....	.....	.....	40	1	.....	.....
T013	.....	.....	.....	10	0	.....	.....
T014	.....	.....	.....	5	0	.....	.....
T015	.....	.....	.....	35	0	.....	.....

SUBJECT TR AND CF FORM SYSTEM
(continued)

System True/False Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
T016	.....	.....	.....	10	0	.....	.....
T017	.....	.....	.....	40	0	.....	.....
T018	.....	.....	.....	35	0	.....	.....
T019	.....	.....	.....	5	0	.....	.....
T020	.....	.....	.....	20	0	.....	.....
T021	.....	.....	.....	50	15	.....	.....
T022	.....	.....	.....	50	10	.....	.....
T023	.....	.....	.....	10	0	.....	.....
T024	.....	.....	.....	15	0	.....	.....
T025	.....	.....	.....	25	0	.....	.....
T026	.....	.....	.....	30	0	.....	.....
T027	.....	.....	.....	30	0	.....	.....
T028	.....	.....	.....	40	2	.....	.....
T029	.....	.....	.....	50	30	.....	.....
T030	.....	.....	.....	40	0	.....	.....
T031	.....	.....	.....	45	3	.....	.....
T032	.....	.....	.....	35	0	.....	.....
T033	.....	.....	.....	5	0	.....	.....
T034	.....	.....	.....	30	0	.....	.....
T035	.....	.....	.....	45	0	.....	.....
T036	.....	.....	.....	10	0	.....	.....
T037	.....	.....	.....	25	0	.....	.....

SUBJECT TR AND CF FORM
SYSTEM
(continued)

System True/False Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
T038	.....	.....	.....	25	0	.....	.....
T039	.....	.....	.....	30	0	.....	.....
T040	.....	.....	.....	35	0	.....	.....
T041	.....	.....	.....	45	4	.....	.....

AWeight Total = ____ for status = Y

Alg A = _____ Results Total

AWeight Total =_____ for status = Y or C

Alg B = _____ Results Total

System Testability Rate (TR)

$$= \frac{\text{(Alg A Result Total)}}{\text{(AWeight Total for status = Y)}} * 100 - \text{(Alg B Results Total)}$$

$$= \frac{.....}{.....} * 100 - ..... = ...$$

System Credibility Factor (CF)

$$= \frac{\text{(AWeight Total for status = Y)}}{\text{(AWeight Total for status = Y or C)}} * 100$$

$$= \frac{.....}{.....} * 100 = ...$$

SUBJECT TR AND CF FORM
SYSTEM BIT

System BIT Ratio Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
R051	.....	.....	.....	45	0	.....	.....
R052	.....	.....	.....	50	2	.....	.....

System BIT True/False Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
T051	.....	.....	.....	45	5	.....	.....
T052	.....	.....	.....	45	3	.....	.....
T053	.....	.....	.....	7	0	.....	.....
T054	.....	.....	.....	40	0	.....	.....
T055	.....	.....	.....	45	3	.....	.....
T056	.....	.....	.....	40	3	.....	.....
T057	.....	.....	.....	35	0	.....	.....
T058	.....	.....	.....	40	2	.....	.....
T059	.....	.....	.....	15	0	.....	.....
T060	.....	.....	.....	10	0	.....	.....
T061	.....	.....	.....	40	0	.....	.....
T062	.....	.....	.....	40	0	.....	.....
T063	.....	.....	.....	30	0	.....	.....
T064	.....	.....	.....	45	3	.....	.....
T065	.....	.....	.....	35	0	.....	.....
T066	.....	.....	.....	25	0	.....	.....
T067	.....	.....	.....	45	5	.....	.....
T068	.....	.....	.....	10	0	.....	.....
T069	.....	.....	.....	30	0	.....	.....
T070	.....	.....	.....	20	0	.....	.....

SUBJECT TR AND CF FORM
SYSTEM BIT
(continued)

System BIT True/False Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
T071	.....	.....	.....	30	0	.....	.....
T072	.....	.....	.....	30	0	.....	.....
T073	.....	.....	.....	45	1	.....	.....
T074	.....	.....	.....	20	0	.....	.....
T075	.....	.....	.....	20	0	.....	.....
T076	.....	.....	.....	5	0	.....	.....
T077	.....	.....	.....	20	0	.....	.....
T078	.....	.....	.....	10	0	.....	.....

AWeight Total = ____ for status = Y Alg A = _____ Results Total

AWeight Total = _____ for status = Y or C Alg B = _____ Results Total

SUBJECT TR AND CF FORM
SYSTEM BIT
(continued)

System BIT Testability Rate (TR)

$$= \frac{\text{(Alg A Result Total)}}{\text{(AWeight Total for status = Y)}} * 100 - \text{(Alg B Results Total)}$$

$$= \frac{\text{.....}}{\text{.....}} * 100 - \text{.....} = \text{.....}$$

System BIT Credibility Factor (CF)

$$= \frac{\text{(AWeight Total for status = Y)}}{\text{(AWeight Total for status = Y or C)}} * 100$$

$$= \frac{\text{.....}}{\text{.....}} * 100 = \text{.....}$$

SUBJECT TR AND CF FORM
MODULE

Module Ratio Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
R651	.....	.....	.....	50	0	.....	.....
R652	.....	.....	.....	45	0	.....	.....
R653	.....	.....	.....	50	5	.....	.....
R654	.....	.....	.....	30	0	.....	.....
R655	.....	.....	.....	50	10	.....	.....
R656	.....	.....	.....	48	0	.....	.....

Module True/False Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
T651	.....	.....	.....	25	0	.....	.....
T652	.....	.....	.....	35	0	.....	.....
T653	.....	.....	.....	20	0	.....	.....
T654	.....	.....	.....	20	0	.....	.....
T655	.....	.....	.....	45	8	.....	.....
T656	.....	.....	.....	30	0	.....	.....
T657	.....	.....	.....	40	0	.....	.....
T658	.....	.....	.....	20	0	.....	.....
T659	.....	.....	.....	45	5	.....	.....
T660	.....	.....	.....	45	5	.....	.....
T661	.....	.....	.....	35	0	.....	.....
T662	.....	.....	.....	10	0	.....	.....
T663	.....	.....	.....	30	0	.....	.....
T664	.....	.....	.....	15	0	.....	.....
T665	.....	.....	.....	5	0	.....	.....
T666	.....	.....	.....	30	0	.....	.....
T667	.....	.....	.....	45	10	.....	.....
T668	.....	.....	.....	5	0	.....	.....

SUBJECT TR AND CF FORM
MODULE
(continued)

AWeight Total = ____ for status = Y Alg A = _____ Results Total

AWeight Total = _____ for status = Y or C Alg B = _____ Results Total

Module Testability Rate (TR)

$$= \frac{\text{(Alg A Result Total)}}{\text{(AWeight Total for status = Y)}} * 100 - \text{(Alg B Results Total)}$$

$$= \frac{.....}{.....} * 100 - ..... = ...$$

Module Credibility Factor (CF)

$$= \frac{\text{(AWeight Total for status = Y)}}{\text{(AWeight Total for status = Y or C)}} * 100$$

$$= \frac{.....}{.....} * 100 = ...$$

SUBJECT TR AND CF FORM
BIT

BIT Ratio Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
R751	.....	.....	.....	50	2	.....	.....
R752	.....	.....	.....	50	0	.....	.....
R753	.....	.....	.....	40	3	.....	.....
R754	.....	.....	.....	35	0	.....	.....

BIT True/False Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
T751	.....	.....	.....	30	0	.....	.....
T752	.....	.....	.....	50	20	.....	.....
T753	.....	.....	.....	45	2	.....	.....
T754	.....	.....	.....	20	0	.....	.....
T755	.....	.....	.....	15	0	.....	.....
T756	.....	.....	.....	40	2	.....	.....
T757	.....	.....	.....	45	8	.....	.....
T758	.....	.....	.....	15	0	.....	.....
T759	.....	.....	.....	20	0	.....	.....
T760	.....	.....	.....	30	0	.....	.....
T761	.....	.....	.....	30	0	.....	.....
T762	.....	.....	.....	45	8	.....	.....
T763	.....	.....	.....	45	20	.....	.....
T764	.....	.....	.....	30	0	.....	.....
T765	.....	.....	.....	5	0	.....	.....
T766	.....	.....	.....	15	0	.....	.....
T767	.....	.....	.....	15	0	.....	.....
T768	.....	.....	.....	5	0	.....	.....

SUBJECT TR AND CF FORM
BIT
(continued)

AWeight Total = ____ for status = Y

Alg A = _____ Results Total

AWeight Total = _____ for status = Y or C

Alg B = _____ Results Total

BIT Testability Rate (TR)

$$= \frac{\text{(Alg A Result Total)}}{\text{(AWeight Total for status = Y)}} * 100 - \text{(Alg B Results Total)}$$

$$= \frac{.....}{.....} * 100 - ..... = ...$$

BIT Credibility Factor (CF)

$$= \frac{\text{(AWeight Total for status = Y)}}{\text{(AWeight Total for status = Y or C)}} * 100$$

$$= \frac{.....}{.....} * 100 = ...$$

SUBJECT TR AND CF FORM
GENERAL DIGITAL

General Digital Ratio Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
R101	.....	.....	.....	45	5	.....	.....
R102	.....	.....	.....	40	1	.....	.....
R103	.....	.....	.....	50	2	.....	.....
R104	.....	.....	.....	40	0	.....	.....
R105	.....	.....	.....	40	3	.....	.....
R106	.....	.....	.....	50	3	.....	.....

General Digital True/False Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
T101	.....	.....	.....	5	0	.....	.....
T102	.....	.....	.....	45	3	.....	.....
T103	.....	.....	.....	10	0	.....	.....
T104	.....	.....	.....	40	5	.....	.....
T105	.....	.....	.....	15	0	.....	.....
T106	.....	.....	.....	40	2	.....	.....
T107	.....	.....	.....	10	0	.....	.....
T108	.....	.....	.....	5	0	.....	.....
T109	.....	.....	.....	10	5	.....	.....
T110	.....	.....	.....	20	0	.....	.....
T111	.....	.....	.....	10	0	.....	.....
T112	.....	.....	.....	30	0	.....	.....
T113	.....	.....	.....	10	0	.....	.....

AWeight Total = ____ for status = Y Alg A = _____ Results Total

AWeight Total = _____ for status = Y or C Alg B = _____ Results Total

SUBJECT TR AND CF FOKM
GENERAL DIGITAL
(continued)

General Digital Testability Rate (TR)

$$= \frac{\text{(Alg A Result Total)}}{\text{(AWeight Total for status = Y)}} * 100 - \text{(Alg B Results Total)}$$

$$= \frac{.....}{.....} * 100 - ..... = ...$$

General Digital Credibility Factor (CF)

$$= \frac{\text{(AWeight Total for status = Y)}}{\text{(AWeight Total for status = V or C)}} * 100$$

$$= \frac{.....}{.....} * 100 = ...$$

SUBJECT TR AND CF FORM
VLSI

VLSI Ratio Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
R901	.....	.....	.....	10	0	.....	.....
R902	.....	.....	.....	50	4	.....	.....
R903	.....	.....	.....	45	0	.....	.....
R904	.....	.....	.....	50	1	.....	.....
R905	.....	.....	.....	40	0	.....	.....
R906	.....	.....	.....	50	4	.....	.....
R907	.....	.....	.....	40	2	.....	.....
R908	.....	.....	.....	35	2	.....	.....
R909	.....	.....	.....	45	0	.....	.....
R910	.....	.....	.....	35	0	.....	.....
R911	.....	.....	.....	35	0	.....	.....
R912	.....	.....	.....	55	5	.....	.....

VLSI True/False Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
T901	.....	.....	.....	30	0	.....	.....
T902	.....	.....	.....	40	10	.....	.....
T903	.....	.....	.....	20	0	.....	.....
T904	.....	.....	.....	15	0	.....	.....
T905	.....	.....	.....	30	0	.....	.....
T906	.....	.....	.....	30	0	.....	.....
T907	.....	.....	.....	40	0	.....	.....
T908	.....	.....	.....	45	15	.....	.....

AWeight Total = ____ for status = Y Alg A = _____ Results Total

AWeight Total = _____ for status = Y or C Alg B = _____ Results Total

SUBJECT TR AND CF FORM
VLSI
(continued)

VLSI Testability Rate (TR)

$$= \frac{\text{(Alg A Result Total)}}{\text{(AWeight Total for status = Y)}} * 100 - \text{(Alg B Results Total)}$$

$$= \frac{.....}{.....} * 100 - ..... = ...$$

VLSI Credibility Factor (CF)

$$= \frac{\text{(AWeight Total for status = Y)}}{\text{(AWeight Total for status = Y or C)}} * 100$$

$$= \frac{.....}{.....} * 100 = ...$$

SUBJECT TR AND CF FORM
PROCESSORS

Processors Ratio Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
R801	.....	.....	.....	45	5	.....	.....

Processors True/False Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
T801	.....	.....	.....	50	20	.....	.....
T802	.....	.....	.....	10	0	.....	.....
T803	.....	.....	.....	50	10	.....	.....
T804	.....	.....	.....	50	10	.....	.....
T805	.....	.....	.....	40	3	.....	.....
T806	.....	.....	.....	30	0	.....	.....
T807	.....	.....	.....	45	5	.....	.....
T808	.....	.....	.....	50	2	.....	.....
T809	.....	.....	.....	35	0	.....	.....
T810	.....	.....	.....	45	8	.....	.....
T811	.....	.....	.....	40	0	.....	.....
T812	.....	.....	.....	45	2	.....	.....
T813	.....	.....	.....	30	0	.....	.....
T814	.....	.....	.....	10	0	.....	.....
T815	.....	.....	.....	40	0	.....	.....
T816	.....	.....	.....	10	0	.....	.....
T817	.....	.....	.....	30	0	.....	.....
T818	.....	.....	.....	45	2	.....	.....

AWeight Total = for status = Y ____ Alg A = Results Total _____

AWeight Total = for status = Y or C _____ Alg B = Results Total _____

SUBJECT TR AND CF FOR VI PROCESSORS
(continued)

Processors Testability Rate (TR)

$$= \frac{\text{(Alg A Result Total)}}{\text{(AWeight Total for status = Y)}} * 100 - \text{(Alg B Results Total)}$$

$$= \frac{.....}{.....} * 100 - ..... = ...$$

Processors Credibility Factor (CF)

$$= \frac{\text{(AWeight Total for status = Y)}}{\text{(AWeight Total for status = Y or C)}} * 100$$

$$= \frac{.....}{.....} * 100 = ...$$

SUBJECT TR AND CF FOR[illegible]
MEMORY

Memory Ratio Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
R851	.....	.....	.....	45	1	.....	.....
R852	.....	.....	.....	50	2	.....	.....
R853	.....	.....	.....	30	0	.....	.....
R854	.....	.....	.....	45	1	.....	.....

Memory True/False Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
T851	.....	.....	.....	50	10	.....	.....
T852	.....	.....	.....	45	4	.....	.....
T853	.....	.....	.....	35	0	.....	.....
T854	.....	.....	.....	20	0	.....	.....
T855	.....	.....	.....	40	0	.....	.....
T856	.....	.....	.....	40	3	.....	.....
T857	.....	.....	.....	30	0	.....	.....
T858	.....	.....	.....	50	3	.....	.....
T859	.....	.....	.....	45	10	.....	.....
T860	.....	.....	.....	20	0	.....	.....
T861	.....	.....	.....	45	5	.....	.....
T862	.....	.....	.....	45	0	.....	.....
T863	.....	.....	.....	35	0	.....	.....
T864	.....	.....	.....	20	0	.....	.....
T865	.....	.....	.....	40	0	.....	.....
T866	.....	.....	.....	10	0	.....	.....

SUBJECT TR AND CF FORM
MEMORY
(continued)

Memory True/False Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
T867	.....	.....	.....	50	10	.....	.....
T868	.....	.....	.....	20	0	.....	.....
T869	.....	.....	.....	10	0	.....	.....
T870	.....	.....	.....	15	0	.....	.....

AWeight Total = ____ for status = Y Alg A = _____ Results Total

AWeight Total = _____ for status = Y or C Alg B = _____ Results Total

Memory Testability Rate (TR)

$$= \frac{\text{(Alg A Result Total)}}{\text{(AWeight Total for status = Y)}} * 100 - \text{(Alg B Results Total)}$$

$$= \frac{.....}{.....} * 100 - ..... = ...$$

Memory Credibility Factor (CF)

$$= \frac{\text{(AWeight Total for status = Y)}}{\text{(AWeight Total for status = Y or C)}} * 100$$

$$= \frac{.....}{.....} * 100 = ...$$

SUBJECT TR AND CF FORM
SCAN

Scan Ratio Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
R701	.....	.....	.....	45	1	.....	.....
R702	.....	.....	.....	50	0	.....	.....
R703	.....	.....	.....	15	0	.....	.....
R704	.....	.....	.....	50	2	.....	.....

Scan True/False Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
T701	.....	.....	.....	50	4	.....	.....
T702	.....	.....	.....	50	20	.....	.....
T703	.....	.....	.....	25	0	.....	.....
T704	.....	.....	.....	5	0	.....	.....
T705	.....	.....	.....	50	3	.....	.....
T706	.....	.....	.....	30	0	.....	.....
T707	.....	.....	.....	50	10	.....	.....
T708	.....	.....	.....	45	8	.....	.....
T709	.....	.....	.....	50	10	.....	.....
T710	.....	.....	.....	50	10	.....	.....
T711	.....	.....	.....	30	0	.....	.....
T712	.....	.....	.....	20	0	.....	.....
T713	.....	.....	.....	45	2	.....	.....
T714	.....	.....	.....	10	0	.....	.....
T715	.....	.....	.....	40	5	.....	.....

AWeight Total = ____ for status = Y

Alg A = _____ Results Total

AWeight Total = _____ for status = Y or C

Alg B = _____ Results Total

SUBJECT TR AND CF FOR VI SCAN
(continued)

Scan Testability Rate (TR)

$$= \frac{\text{(Alg A Result Total)}}{\text{(AWeight Total for status = Y)}} * 100 - \text{(Alg B Results Total)}$$

$$= \frac{.....}{.....} * 100 - ..... = ...$$

Scan Credibility Factor (CF)

$$= \frac{\text{(AWeight Total for status = Y)}}{\text{(AWeight Total for status = Y or C)}} * 100$$

$$= \frac{.....}{.....} * 100 = ...$$

SUBJECT TR AND CF FORM
GENERAL ANALOG

General Analog Ratio Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
R551	.....	.....	.....	50	2	.....	.....
R552	.....	.....	.....	35	0	.....	.....
R553	.....	.....	.....	45	1	.....	.....
R554	.....	.....	.....	50	4	.....	.....
R555	.....	.....	.....	50	10	.....	.....

General Analog True/False Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
T551	.....	.....	.....	10	0	.....	.....
T552	.....	.....	.....	25	0	.....	.....
T553	.....	.....	.....	45	3	.....	.....
T554	.....	.....	.....	40	10	.....	.....
T555	.....	.....	.....	50	7	.....	.....
T556	.....	.....	.....	40	1	.....	.....
T557	.....	.....	.....	20	0	.....	.....
T558	.....	.....	.....	10	0	.....	.....
T559	.....	.....	.....	45	1	.....	.....
T560	.....	.....	.....	30	0	.....	.....
T561	.....	.....	.....	45	3	.....	.....
T562	.....	.....	.....	45	8	.....	.....
T563	.....	.....	.....	10	0	.....	.....
T564	.....	.....	.....	30	0	.....	.....
T565	.....	.....	.....	40	2	.....	.....

AWeight Total = ____ for status = Y Alg A = _____ Results Total

AWeight Total = _____ for status = Y or C Alg B = _____ Results Total

SUBJECT TR AND CF FORM1
GENERAL ANALOG
(continued)

General Analog Testability Rate (TR)

$$= \frac{\text{(Alg A Result Total)}}{\text{(AWeight Total for status = Y)}} * 100 - \text{(Alg B Results Total)}$$

$$= \frac{.....}{.....} * 100 - ..... = ...$$

General Analog Credibility Factor (CF)

$$= \frac{\text{(AWeight Total for status = Y)}}{\text{(AWeight Total for status = Y or C)}} * 100$$

$$= \frac{.....}{.....} * 100 = ...$$

SUBJECT TR AND CF FORM
HIGH FREQUENCY

High Frequency Ratio Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
R451	.....	.....	.....	45	3	.....	.....
R452	.....	.....	.....	50	6	.....	.....

High Frequency True/False Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
T451	.....	.....	.....	40	5	.....	.....
T452	.....	.....	.....	45	4	.....	.....
T453	.....	.....	.....	45	7	.....	.....
T454	.....	.....	.....	20	0	.....	.....
T455	.....	.....	.....	30	0	.....	.....
T456	.....	.....	.....	10	0	.....	.....
T457	.....	.....	.....	15	0	.....	.....
T458	.....	.....	.....	30	0	.....	.....
T459	.....	.....	.....	45	4	.....	.....
T460	.....	.....	.....	10	0	.....	.....
T461	.....	.....	.....	20	0	.....	.....
T462	.....	.....	.....	45	5	.....	.....
T463	.....	.....	.....	35	4	.....	.....
T464	.....	.....	.....	30	0	.....	.....

AWeight Total = ____ for status = Y Alg A = _____ Results Total

AWeight Total = _____ for status = Y or C Alg B = _____ Results Total

SUBJECT TR AND CF FORMI
HIGH FREQUENCY
(continued)

High Frequency Testability Rate (TR)

$$= \frac{\text{(Alg A Result Total)}}{\text{(AWeight Total for status = Y)}} * 100 - \text{(Alg B Results Total)}$$

$$= \frac{.....}{.....} * 100 - ..... = ...$$

High Frequency Credibility Factor (CF)

$$= \frac{\text{(AWeight Total for status = Y)}}{\text{(AWeight Total for status = Y or C)}} * 100$$

$$= \frac{.....}{.....} * 100 = ...$$

SUBJECT TR AND CF FORM
HIGH POWER

High Power Ratio Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
-	.....	.....	.....	-	-	.....	.....

High Power True/False Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
T401	.....	.....	.....	35	0	.....	.....
T402	.....	.....	.....	40	2	.....	.....
T403	.....	.....	.....	40	1	.....	.....
T404	.....	.....	.....	10	0	.....	.....
T405	.....	.....	.....	10	0	.....	.....
T406	.....	.....	.....	45	5	.....	.....
T407	.....	.....	.....	45	3	.....	.....
T408	.....	.....	.....	10	0	.....	.....
T409	.....	.....	.....	20	0	.....	.....
T410	.....	.....	.....	25	2	.....	.....
T411	.....	.....	.....	50	10	.....	.....
T412	.....	.....	.....	40	5	.....	.....
T413	.....	.....	.....	35	0	.....	.....
T414	.....	.....	.....	20	0	.....	.....
T415	.....	.....	.....	40	0	.....	.....
T416	.....	.....	.....	35	0	.....	.....
T417	.....	.....	.....	20	0	.....	.....

AWeight Total = ____ for status = Y Alg A = _____ Results Total

AWeight Total = _____ for status = Y or C Alg B = _____ Results Total

SUBJECT TR AND CF FOR M1
HIGH POWER
(continued)

High Power Testability Rate (TR)

$$= \frac{\text{(Alg A Result Total)}}{\text{(AWeight Total for status = Y)}} * 100 - \text{(Alg B Results Total)}$$

$$= \frac{.....}{.....} * 100 - ..... = ...$$

High Power Credibility Factor (CF)

$$= \frac{\text{(AWeight Total for status = Y)}}{\text{(AWeight Total for status = Y or C)}} * 100$$

$$= \frac{.....}{.....} * 100 = ...$$

SUBJECT TR AND CF FORM
INCIRCUIT

Incircuit Ratio Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
R951	.....	.....	.....	50	10	.....	.....
R952	.....	.....	.....	50	1	.....	.....
R953	.....	.....	.....	25	0	.....	.....
R954	.....	.....	.....	30	0	.....	.....
R955	.....	.....	.....	50	5	.....	.....
R956	.....	.....	.....	45	2	.....	.....
R957	.....	.....	.....	35	0	.....	.....
R958	.....	.....	.....	45	3	.....	.....
R959	.....	.....	.....	45	5	.....	.....
R960	.....	.....	.....	45	2	.....	.....
R961	.....	.....	.....	45	2	.....	.....
R962	.....	.....	.....	45	0	.....	.....

Incircuit True/False Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
T951	.....	.....	.....	35	0	.....	.....
T952	.....	.....	.....	20	0	.....	.....
T953	.....	.....	.....	25	0	.....	.....
T954	.....	.....	.....	40	2	.....	.....
T955	.....	.....	.....	40	0	.....	.....
T956	.....	.....	.....	10	0	.....	.....
T957	.....	.....	.....	10	0	.....	.....
T958	.....	.....	.....	15	0	.....	.....
T959	.....	.....	.....	25	0	.....	.....
T960	.....	.....	.....	20	0	.....	.....

SUBJECT TR AND CF FORM
INCIRCUIT
(continued)

Incircuit True/False Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
T961	.....	.....	.....	50	10	.....	.....
T962	.....	.....	.....	40	0	.....	.....
T963	.....	.....	.....	30	0	.....	.....
T964	.....	.....	.....	45	5	.....	.....
T965	.....	.....	.....	50	5	.....	.....
T966	.....	.....	.....	40	3	.....	.....
T967	.....	.....	.....	10	0	.....	.....
T968	.....	.....	.....	25	0	.....	.....
T969	.....	.....	.....	35	0	.....	.....
T970	.....	.....	.....	10	0	.....	.....
T971	.....	.....	.....	30	0	.....	.....
T972	.....	.....	.....	45	10	.....	.....
T973	.....	.....	.....	50	5	.....	.....
T974	.....	.....	.....	25	0	.....	.....
T975	.....	.....	.....	45	3	.....	.....
T976	.....	.....	.....	10	0	.....	.....
T977	.....	.....	.....	35	0	.....	.....

AWeight Total = ____ for status = Y Alg A = _____ Results Total

AWeight Total = _____ for status = Y or C Alg B = _____ Results Total

SUBJECT TR AND CF FORM
INCIRCUIT
(continued)

Incircuit Testability Rate (TR)

$$= \frac{\text{(Alg A Result Total)}}{\text{(AWeight Total for status = Y)}} * 100 - \text{(Alg B Results Total)}$$

$$= \frac{.....}{.....} * 100 - ..... = ...$$

Incircuit Credibility Factor (CF)

$$= \frac{\text{(AWeight Total for status = Y)}}{\text{(AWeight Total for status = Y or C)}} * 100$$

$$= \frac{.....}{.....} * 100 = ...$$

SUBJECT TR AND CF FORM
ELECTRO-OPTICS

Electro-Optic Ratio Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
R301	.....	.....	.....	50	1	.....	.....
R302	.....	.....	.....	45	2	.....	.....

Electro-Optic True/False Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
T301	.....	.....	.....	50	7	.....	.....
T302	.....	.....	.....	45	5	.....	.....
T303	.....	.....	.....	35	0	.....	.....
T304	.....	.....	.....	40	4	.....	.....
T305	.....	.....	.....	50	5	.....	.....
T306	.....	.....	.....	30	0	.....	.....
T307	.....	.....	.....	20	0	.....	.....
T308	.....	.....	.....	40	3	.....	.....
T309	.....	.....	.....	20	0	.....	.....
T310	.....	.....	.....	20	0	.....	.....
T311	.....	.....	.....	30	0	.....	.....
T312	.....	.....	.....	35	0	.....	.....
T313	.....	.....	.....	40	0	.....	.....
T314	.....	.....	.....	20	0	.....	.....
T315	.....	.....	.....	25	0	.....	.....
T316	.....	.....	.....	40	4	.....	.....
T317	.....	.....	.....	20	0	.....	.....
T318	.....	.....	.....	45	0	.....	.....
T319	.....	.....	.....	20	0	.....	.....
T320	.....	.....	.....	20	0	.....	.....

SUBJECT TR AND CF FORM
ELECTRO-OPTICS
(continued)

Electro-Optic True/False Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
T321	.....	.....	.....	25	0	.....	.....
T322	.....	.....	.....	20	0	.....	.....
T323	.....	.....	.....	50	8	.....	.....
T324	.....	.....	.....	40	3	.....	.....
T325	.....	.....	.....	45	5	.....	.....
T326	.....	.....	.....	45	5	.....	.....
T327	.....	.....	.....	35	0	.....	.....
T328	.....	.....	.....	35	0	.....	.....
T329	.....	.....	.....	15	0	.....	.....
T330	.....	.....	.....	25	0	.....	.....
T331	.....	.....	.....	35	0	.....	.....
T332	.....	.....	.....	25	0	.....	.....
T333	.....	.....	.....	20	0	.....	.....
T334	.....	.....	.....	35	0	.....	.....
T335	.....	.....	.....	45	5	.....	.....
T336	.....	.....	.....	40	3	.....	.....
T337	.....	.....	.....	35	0	.....	.....
T338	.....	.....	.....	35	0	.....	.....
T339	.....	.....	.....	25	0	.....	.....
T340	.....	.....	.....	15	0	.....	.....
T341	.....	.....	.....	45	3	.....	.....

AWeight Total = ____ for status = Y

Alg A = _____ Results Total

AWeight Total = _____ for status = Y or C

Alg B = _____ Results Total

SUBJECT TR AND CF FORM
ELECTRO-OPTIC
(continued)

Electro-Optic Testability Rate (TR)

$$= \frac{\text{(Alg A Result Total)}}{\text{(AWeight Total for status = Y)}} * 100 - \text{(Alg B Results Total)}$$

$$= \frac{.....}{.....} * 100 - ..... = ...$$

Electro-Optic Credibility Factor (CF)

$$= \frac{\text{(AWeight Total for status = Y)}}{\text{(AWeight Total for status = Y or C)}} * 100$$

$$= \frac{.....}{.....} * 100 = ...$$

SUBJECT TR AND CF FORM
OTHERS

Others Ratio Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
R351	.....	.....	.....	50	3	.....	.....
R352	.....	.....	.....	45	2	.....	.....
R353	.....	.....	.....	50	4	.....	.....
R354	....	.....	.....	45	3	.....	.....

Others True/False Parameters

Parameter #	Status	Response 1	Response 2	AWeight	BWeight	Alg A Result	Alg B Result
T351	.....	.....	.....	45	0	.....	.....
T352	.....	.....	.....	40	0	.....	.....
T353	.....	.....	.....	35	0	.....	.....
T354	.....	.....	.....	40	0	.....	.....
T355	.....	.....	.....	45	2	.....	.....
T356	.....	.....	.....	30	0	.....	.....
T357	.....	.....	.....	20	0	.....	.....
T358	.....	.....	.....	20	0	.....	.....
T359	.....	.....	.....	40	2	.....	.....
T360	.....	.....	.....	25	0	.....	.....
T361	.....	.....	.....	15	0	.....	.....
T362	.....	.....	.....	20	0	.....	.....
T363	.....	.....	.....	50	10	.....	.....
T364	.....	.....	.....	50	10	.....	.....
T365	.....	.....	.....	45	5	.....	.....
T366	.....	.....	.....	50	10	.....	.....

SUBJECT TR AND CF FORM
OTHERS
(continued)

AWeight Total = ____ for status = Y

Alg A = _____ Results Total

AWeight Total = ____ for status = Y or C

Alg B = _____ Results Total

Others Testability Rate (TR)

$$= \frac{\text{(Alg A Result Total)}}{\text{(AWeight Total for status = Y)}} * 100 - \text{(Alg B Results Total)}$$

$$= \frac{.....}{.....} * 100 - ..... = ...$$

Others Credibility Factor (CF)

$$= \frac{\text{(AWeight Total for status = Y)}}{\text{(AWeight Total for status = Y or C)}} * 100$$

$$= \frac{.....}{.....} * 100 = ...$$

SYSTEM/SUBSYSTEM ANALYSIS FORM

System/Subsystem Final Testability Rate (TR)

= 0.1 * (Top Level TR) + 0.4 * (System TR) + 0.5 * (System TR)

= (0.1 * .....) + (0.4 * .....) + (0.5 * .....)

= .....

System/Subsystem Credibility Factor (CF)

= 0.1 * (Top Level CF) + 0.4 * (System CF) + 0.5 * (System CF)

= (0.1 * .....) + (0.4 * .....) + (0.5 * .....)

= .....

MODULE INCIRCUIT ANALYSIS FORM

Module Incircuit Testability Rate (TR)

= (Incircuit TR) + (Positive Weighting Factors)

- (Negative Weighting Factors)

= ..... + ... - .....

= .....

where:

$$\text{Positive Weighting Factors} = \frac{(\text{Scan TR}) + (\text{BIT TR})}{10}$$

Negative Weighting Factors =

$$10 - \frac{(\text{Top Level TR}) + (\text{Module TR})}{20}$$

MODULE INCIRCUIT ANALYSIS FORM
(continued)

Module Incircuit Credibility Factor (CF)

$$= \text{(BASE CF)} * (1 - X/10) + [(\text{Scan CF}) + (\text{BIT CF})] * 0.1$$

where X = 0 for Scan and BIT not analyzed
= 1 for either Scan or BIT analyzed
= 2 for both Scan and BIT analyzed

= ..... * (1 - ..... /10) + (..... + ...) * 0.1

= .....

Where BASE CF

$$= \text{(Incircuit CF)} + \left[(0.1) * \left[\frac{\text{(Top Level CF)} + \text{(Module CF)}}{2} \right] \right]$$

= ..... + [0.1 * (..... + ...) / 2]

= .....

Module Testability Rate (TR)

$$= \left[\sum_{i=1}^{9} \left[(\text{Subject(i) TR}) * \frac{(\text{Subject (i) Weight})}{\sum_{j=1}^{9} (\text{Subject (j) Weight})} \right] \right]$$

+ (Positive Weighting Factors) - (Negative Weighting Factors)

= ..... + ... - .....

= .....

where:

$$\text{Positive Weighting Factors} = \frac{(\text{Scan TR}) + (\text{BIT TR})}{10}$$

Negative Weighting Factors =

$$10 - \frac{(\text{Top Level TR}) + (\text{Module TR})}{20}$$

Module Credibility Factor (CF)

$$= \text{(BASE CF)} * (1 - X/10) + [(\text{Scan CF}) + (\text{BIT CF})] * 0.1$$

where X = 0 for Scan and BIT not analyzed
= 1 for either Scan or BIT analyzed
= 2 for both Scan and BIT analyzed

= ..... * (1 - ..... /10) + (..... + ...) * 0.1

= .....

Where BASE CF

$$= \sum_{i=1}^{9} \left[(\text{Subject(i) CF}) * \frac{(\text{Subject (i) Weight})}{\sum_{j=1}^{9} (\text{Subject (j) Weight})} * 0.9 \right]$$

$$+ \left[(0.1) * \left[\frac{(\text{Top Level CF}) + (\text{Module CF})}{2} \right] \right]$$

= ..... + ... = ...

MODULE CONCURRENT FUNCTIONAL AND INCIRCUIT ANALYSIS FORM

Module Testability Rate (TR)

$$= \left[\sum_{i=1}^{9} \left[(\text{Subject(i) TR}) * \frac{(\text{Subject (i) Weight})}{\sum_{j=1}^{9} (\text{Subject (j) Weight})} \right] \right]$$

$$+ (\text{Incircuit TR}) \Big] * 1/2$$

$$+ (\text{Positive Weighting Factors}) - (\text{Negative Weighting Factors})$$

$$= (\ldots\ldots\ldots\ldots + \ldots\ldots\ldots\ldots) * 1/2 + \ldots\ldots\ldots\ldots - \ldots\ldots\ldots\ldots$$

$$= \ldots\ldots\ldots\ldots\ldots\ldots$$

where:

$$\text{Positive Weighting Factors} = \frac{(\text{Scan TR}) + (\text{BIT TR})}{10}$$

Negative Weighting Factors =

$$10 - \frac{(\text{Top Level TR}) + (\text{Module TR})}{20}$$

MODULE CONCURRENT FUNCTIONAL AND INCIRCUIT ANALYSIS FORM
(continued)

Module Credibility Factor (CF)

= (BASE CF) * (1 - X/10) + [(Scan CF) + (BIT CF)] * 0.1

where X = 0 for Scan and BIT not analyzed
= 1 for either Scan or BIT analyzed
= 2 for both Scan and BIT analyzed

= ..... * (1 - ..... /10) + (..... + ...) * 0.1

= .....

where BASE CF

$$= \sum_{i=1}^{9} \left[(\text{Subject(i) CF}) * \frac{(\text{Subject (i) Weight})}{\sum_{j=1}^{9} (\text{Subject (j) Weight})} * 0.9 \right]$$

$$+ \left[(0.1) * \left[\frac{(\text{Top Level CF}) + (\text{Module CF})}{2} \right] \right]$$

APPENDIX D

FAILURE RATE TABLE

TESTABILITY DESIGN RATING SYSTEM 03/24/91
FAILURE RATE TABLE 17:02:17
(failures/10e6 hrs.)

COMPONENT	SUBJECT	FAILURE RATE	NUMBER OF COMPONENTS
1-100 gate bipolar*	General Digital	0.037	.....
1-100 gate bipolar	General Digital	0.0408	.....
1-100 gate MOS*	General Digital	0.0408	.....
1-100 gate MOS	General Digital	0.0834	.....
100-1k gate bipolar*	General Digital	0.0655	.....
100-1k gate bipolar	General Digital	0.073	.....
100-1k gate MOS*	General Digital	0.073	.....
100-1k gate MOS	General Digital	0.1583	.....
1-1k OTHERS (guestimate)	General Digital	0.2	.....
1k-3k gate bipolar*	VLSI	0.126	.....
1k-3k gate bipolar	VLSI	0.1409	.....
1k-3k gate MOS*	VLSI	0.1409	.....
1k-3k gate MOS	VLSI	0.3116	.....
3k-10k bipolar*	VLSI	0.4151	.....
3k-10k bipolar	VLSI	0.4449	.....
3k-10k MOS*	VLSI	0.4449	.....
3k-10k MOS	VLSI	0.7863	.....
10k-30k bipolar*	VLSI	0.6805	.....
10k-30k bipolar	VLSI	0.74	.....

* Components with asterics (*) are hermetically sealed.

COMPONENT	SUBJECT	RATE	COMPONENTS
10k-30k MOS*	VLSI	0.74	.....
10k-30k MOS	VLSI	1.4228	.....
30k-90k others (estimate)	VLSI	1.8	.....
30-90k MOS (estimate)	VLSI	3.4	.....
>90k OTHERS (estimate)	VLSI	4.5	.....
>90k MOS (estimate)	VLSI	8.2	.....
8 bit bipolar*	Processors	0.1132	.....
8 bit bipolar	Processors	0.1057	.....
8 bit MOS*	Processors	0.1244	.....
8 bit MOS	Processors	0.2337	.....
16 bit bipolar*	Processors	0.2102	.....
16 bit bipolar	Processors	0.1992	.....
16 bit MOS*	Processors	0.2325	.....
16 bit MOS	Processors	0.4552	.....
32 bit bipolar*	Processors	0.4664	.....
32 bit bipolar	Processors	0.4329	.....
32 bit MOS*	Processors	0.511	.....
32 bit MOS	Processors	0.945	.....
64 bit OTHERS (estimate)	Processors	2.5	.....
64 bit MOS (estimate)	Processors	4.	.....
PLD, 1-100 gate bipolar*	Memory	0.1011	.....
PLD, 1-100 gate bipolar	Memory	0.1235	.....
PLD, 1-100 gate MOS*	Memory	0.1235	.....

* Components with asterics (*) are hermetically sealed.

COMPONENT	SUBJECT	RATE	COMPONENTS
PLD, 1-100 gate MOS	Memory	0.3795	.....
PLD, 100-1k gate bipolar*	Memory	0.1937	.....
PLD, 100-1k gate bipolar	Memory	0.2383	.....
PLD, 100-1k gate MOS*	Memory	0.2383	.....
PLD, 100-1k gate MOS	Memory	0.7504	.....
PLD, 1k-5k gate bipolar*	Memory	0.3824	.....
PLD, 1k-5k gate bipolar	Memory	0.4717	.....
PLD, 1k-5k gate MOS*	Memory	0.4717	.....
PLD, 1k-5k gate MOS	Memory	1.4959	.....
SRAM, <1k bipolar*	Memory	0.1054	.....
SRAM, <1k bipolar	Memory	0.124	.....
SRAM, 16k-64k MOS*	Memory	0.3836	.....
DRAM, <16k MOS*	Memory	0.0656	.....
ROM, <16k MOS*	Memory	0.0978	.....
SRAM, <1k MOS*	Memory	0.124	.....
SRAM, <1k MOS	Memory	0.3374	.....
SRAM, 4k-16k bipolar*	Memory	0.181	.....
SRAM, 4k-16k bipolar	Memory	0.2182	.....
SRAM, 4k-16k MOS*	Memory	0.2132	.....
SRAM, 4k-16k MOS	Memory	0.6391	.....
SRAM, 16k-64k MOS	Memory	1.2371	.....
SRAM, 64k-256k MOS*	Memory	0.7204	.....
SRAM, 64k-256k MOS	Memory	2.4273	.....

* Components with asterics (*) are hermetically sealed.

COMPONENT	SUBJECT	RATE	COMPONENTS
DRAM, <16k MOS	Memory	0.1723	.....
DRAM, 16k-64k MOS*	Memory	0.1107	.....
DRAM, 16k-64k MOS	Memory	0.3241	.....
DRAM, 64k-256k MOS*	Memory	0.1934	.....
DRAM, 64k-256k MOS	Memory	0.6201	.....
DRAM, 256k-1M MOS*	Memory	0.3627	.....
DRAM, 256k-1M MOS	Memory	1.2161	.....
OTHERS (estimate)	Memory	3.5	.....
ROM, <16k MOS	Memory	0.2471	.....
ROM, 16k-64k MOS*	Memory	0.164	.....
ROM, 16k-64k MOS	Memory	0.4621	.....
ROM, 64k-256k MOS*	Memory	0.2798	.....
ROM, 64k-256k MOS	Memory	0.8772	.....
ROM, 256k-1M MOS*	Memory	0.5378	.....
ROM, 256k-1M MO	Memory	1.7327	.....
PROM, <16k MOS*	Memory	0.1391	.....
PROM, <16k MOS	Memory	0.3952	.....
PROM, 16k-64k MOS*	Memory	0.2457	.....
PROM, 16k-64k MOS	Memory	0.7588	.....
PROM, 64k-256k MOS*	Memory	0.4451	.....
PROM, 64k-256k MOS	Memory	1.4693	.....
PROM, 256k-1M MOS*	Memory	0.8686	.....
PROM, 256k-1M MOS	Memory	2.917	.....

* Components with asterics (*) are hermetically sealed.

COMPONENT	SUBJECT	RATE	COMPONENTS
ROM/PROM, <16k bipolar*	Memory	0.1357	.....
ROM/PROM, <16k bipolar	Memory	0.1387	.....
ROM/PROM, 16-64k bipolar*	Memory	0.2126	.....
ROM/PROM, 16-64k bipolar	Memory	0.2375	.....
Resistor,RB,RZ,RBR,RWR,RE	General Analog	0.4	.....
Res., OTHERS (estimate)	General Analog	0.03	.....
1-100 gate bipolar*	General Analog	0.0481	.....
Var. Res., wirewound(RTR)	General Analog	0.11	.....
Var. Res., trimmer (RT)	General Analog	0.54	.....
Var. Res., W. W. Prec(RR)	General Analog	10.	.....
Var. Res., W. W. Semi(RA)	General Analog	4.5	.....
Var. Res., Precision(RK)	General Analog	4.5	.....
Var. Res., Non W.W. (RJR)	General Analog	0.1	.....
Var. Res., trimmer (RJ)	General Analog	0.52	.....
Var. Res., compstn (RV)	General Analog	9.7	.....
Var. Res., Non W.W.(RQ)	General Analog	0.84	.....
Var. Res., film (RVC)	General Analog	0.78	.....
1-100 gate bipolar	General Analog	0.1192	.....
1-100 gate MOS*	General Analog	0.0481	.....
1-100 gate MOS	General Analog	0.1192	.....
100-300 gate bipolar*	General Analog	0.0831	.....
100-300 gate bipolar	General Analog	0.2253	.....
100-300 gate MOS*	General Analog	0.0831	.....

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COMPONENT	SUBJECT	RATE	COMPONENTS
100-300 gate MOS	General Analog	0.2253	.....
300-1K gate bipolar*	General Analog	0.1501	.....
300-1k gate bipolar	General Analog	0.4344	.....
300-1k gate MOS*	General Analog	0.1501	.....
300-1k gate MOS	General Analog	0.4344	.....
Analog Proc, 1-100bit bi*	General Analog	0.2102	.....
An. Proc., 1-100 bit MOS*	General Analog	0.2325	.....
Analog Proc, 1-100bit bip	General Analog	0.2325	.....
An. Proc., 1-100 bit MOS	General Analog	0.4885	.....
Transistor, Si NPN	General Analog	0.069	.....
Transistor, Si PNP	General Analog	0.11	.....
Transistor, Ge NPN	General Analog	3.4	.....
Transistor, Ge PNP	General Analog	1.3	.....
Transistor, Si FET	General Analog	2.	.....
Transistor, unijunction	General Analog	4.8	.....
Diode, Si	General Analog	0.26	.....
Diode, Ge	General Analog	0.36	.....
Diode, Zener & Avalanche	General Analog	0.088	.....
Diode, Thyristor	General Analog	0.73	.....
Capacitors, General (est)	General Analog	0.01	.....
Caps, Al Oxide	General Analog	1.4	.....
Caps, Al dry	General Analog	2.2	.....
Var. Caps, Ceramic (CV)	General Analog	4.6	.....

* Components with asterics (*) are hermetically sealed.

COMPONENT	SUBJECT	RATE	COMPONENTS
Var. Piston (PC)	General Analog	0.63	.....
Var. Caps, Air trim(CT)	General Analog	8.5	.....
Var. Caps, Vacuum (CG)	General Analog	17.	.....
OTHER DEVICES (estimate)	General Analog	4.	.....
OTHERS (est)	High Power	5.	.....
Resistor, Power (RW)	High Power	0.67	.....
Resistor, OTHERS (est)	High Power	1.	.....
Var. Res., W.W.Power (RP)	High Power	3.8	.....
Var. Res., OTHERS (est)	High Power	4.5	.....
Tramsistors, Power	High Power	4.	.....
Capacitors (est)	High Power	2.5	.....
Resistor, Power film (RD)	High Power	0.071	.....
Microwave Detector, Ge	High Freq	36.	.....
Microwave Mixer, Si	High Freq	16.	.....
Microwave Mixer, Ge	High Freq	62.	.....
Varactor, Step recov. tun	High Freq	8.2	.....
Gunn & Impact	High Freq	15.	.....
Pin semiconductor	High Freq	11.	.....
LED	High Freq	0.14	.....
Single Isolator	High Freq	1.2	.....
Bipolar Micro. Pow Trans.	High Freq	4.	.....
Single isolator	High Freq	1.2	.....
Micro. Diode, JANTXV	High Freq	0.3	.....

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COMPONENT	SUBJECT	RATE	COMPONENTS
Micro. Diode, JANTX	High Freq	0.6	.....
Micro. Diode, JAN	High Freq	1.	.....
Micro. Diode, non-MIL*	High Freq	1.4	.....
Micro. Diode, JANTXV	High Freq	0.3	.....
Micro. Transistor JANTXV	High Freq	0.25	.....
Micro. Transistor JANTX	High Freq	0.5	.....
Micro. Transistor JANT	High Freq	1.	.....
Micro. Transistor NonMIL*	High Freq	2.5	.....
Microwave Detector, Si	High Freq	12.	.....
OTHERS (estimate)	High Freq	10.	.....
estimate for any device	Electro-Optic	20.	.....
estimate for any device	Others	10.	.....

* Components with asterics (*) are hermetically sealed.

APPENDIX E

SUBJECT VALUE TABLE

TESTABILITY DESIGN RATING SYSTEM 03/24/91
SUBJECT VALUE TABLE 17:02:50

SUBJECT	VALUE	# OF COMPONENTS
General Digital	1	.....
VLSI	12	.....
Processors	10	.....
Memory	3	.....
General Analog	4	.....
High Power	4	.....
High Freq	8	.....
Electro-Optics	5	.....
Others	1	.....

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