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GaAs Heterojunction Device Based A/D Converter Development

Final Report for Period: August 1987 - March 1992
CDRL No. A007

Contract No: N00014-87-C-0315

TRW Sales No: 50279

April 1992

Prepared For:

Defense Advanced Research Projects Agency
Defense Sciences Office
3701 N. Fairfax Drive
Arlington, Virginia 22217

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By:

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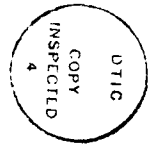

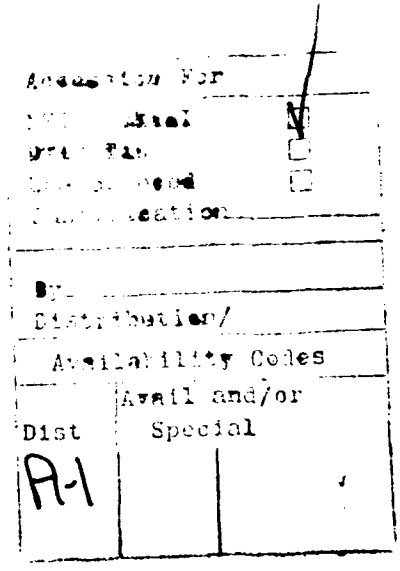

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SECURITY CLASSIFICATION OF THIS PAGE

REPORT DOCUMENTATION PAGE

Form Approved OMB No. 0704-0188

1a. REPORT SECURITY CLASSIFICATION Unclassified	1b. RESTRICTIVE MARKINGS
2a. SECURITY CLASSIFICATION AUTHORITY N/A	3. DISTRIBUTION/AVAILABILITY OF REPORT Approved for public release; distribution unlimited.
2b. DECLASSIFICATION/DOWNGRADING SCHEDULE N/A	
4. PERFORMING ORGANIZATION REPORT NUMBER(S)	5. MONITORING ORGANIZATION REPORT NUMBER(S)
6a. NAME OF PERFORMING ORGANIZATION TRW Electronics Systems Group 6b. OFFICE SYMBOL (If applicable)	7a. NAME OF MONITORING ORGANIZATION Office of Navel Research Electronics Division
6c. ADDRESS (City, State, and ZIP Code) One Space Park Redondo Beach, CA 90278	7b. ADDRESS (City, State, and ZIP Code) 800 N. Quincy Street Arlington, Virginia 22217-5000
8a. NAME OF FUNDING/SPONSORING ORGANIZATION 8b. OFFICE SYMBOL (If applicable)	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER N00014-87-C-0315
8c. ADDRESS (City, State, and ZIP Code)	10. SOURCE OF FUNDING NUMBERS PROGRAM ELEMENT NO. / PROJECT NO. / TASK NO / WORK UNIT ACCESSION NO.
11. TITLE (Include Security Classification) GaAs Heterojunction Device Based A/D Converter Development	
12. PERSONAL AUTHOR(S) de Graaf, Ken: Custer, Clark; Bui, Stacey	
13a. TYPE OF REPORT Final	13b. TIME COVERED FROM 87/8 TO 92/3
14. DATE OF REPORT (Year, Month, Day) 92/4	15. PAGE COUNT
16. SUPPLEMENTARY NOTATION	
17. COSATI CODES FIELD / GROUP / SUB-GROUP	18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number) GaAs Heterojunction Bipolar (HBT) Analog-to-Digital Converters (ADC)

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

This final report summarizes the technical work performed on the development of a GaAs Heterojunction analog-to-digital converter. The program goal was to develop a.12 bit 20 Msps, <1 Watt/20 Msps ADC implemented as a single monolithic chip or at most 2 chips. The part developed on this program is a single chip monolithic GaAs Heterojunction Bipolar Transistor (HBT) ADC that includes a sample-and-hold (S/H) and all of the active circuitry required for stand alone operation. The ADC development was taken to the point of fabricating one lot of 3" wafers, wafer probing, and packaging a few of the best candidate ADCs. Yield on the first (and only) lot was 18% for 4 MBE wafers. Three MOCVD wafers had low beta and were not finished. Several parts were packaged. Electrical trimming was accomplished on the first 5 most significant bits (msbs) and triangle and sine waveforms processed through the ADC. The chip demonstrated the highest reported SNR of 49.7 dB for a GaAs ADC (8 bit theoretical SNR=49.9dB).

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20. DISTRIBUTION/AVAILABILITY OF ABSTRACT ☐ UNCLASSIFIED/UNLIMITED ☐ SAME AS RPT. ☐ DTIC USERS	21. ABSTRACT SECURITY CLASSIFICATION Unclassified
22a. NAME OF RESPONSIBLE INDIVIDUAL Max N. Yoder	22b. TELEPHONE (Include Area Code) (703) 696-4218 22c. OFFICE SYMBOL 1114

DD Form 1473, JUN 86 *Previous editions are obsolete.* SECURITY CLASSIFICATION OF THIS PAGE

Block #19 (Continuation)

Features of the ADC include:

- Successive approximation architecture
- 1 bit error (overrange) correction
- Electrically and laser trimmable
- 6 on-board operational amplifiers
- On-board bandgap voltage reference
- 1855 transistors, 48 diodes, 1.2 Watts power consumption
- 4.15 X 3.40 mm die size

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ACRONYMS

ADC	analog-to-digital converter
BCLK	bit clock
BGAP	bandgap circuit
BITCLOCK	bit clock
CCLK	coarse comparator clock
CCMR	common mode rejection ratio
CERMET	ceramic/metal
CVD	chemical vapor deposition
DAC	digital-to-analog converter
DACOUT	DAC output
DREADY	data ready
ECL	emitter-coupled logic
EOC	end of conversion
FFT	fast Fourier transform
GaAs	gallium arsenide
HBT	heterojunction bipolar transistor
IC	integrated circuit
LEC	liquid-encapsulated Czochralski
lsb	least significant bit
MBE	molecular beam epitaxy
MHz	megahertz
MIM	metal insulator metal
MMIC	monolithic microwave integrated circuits
MOCVD	metallo-organic chemical vapor desposition
MOM	metal-oxide-metal
msb	most significant bit
Msps	megasamples per second
MTTF	mean time to failure
NSA	non-self aligned
OPAMP	operational amplifier
PSRR	power supply rejection ratio
R/2R	resistor/two times value resistor
S/H	sample and hold
SABM	self-aligned base ohmic metal

ACRONYMS (Continued)

SHCLK	sample and hold clock
SNR	signal-to-noise ratio
TTL	transistor-tansistor logic
WCLK	word clock
WORDCLOCK	word clock

1. INTRODUCTION

This is the final report for the GaAs Heterojunction Device Based A/D Converter Development program (Contract No. N00014-87-C-0315). The original program goal was to develop a 14-bit, 10 Msps, <5 W ADC implemented as a single monolithic chip or at most two chips. The requirements were changed early in the program to 12 bits, 20 Msps, and <1 W/20 Msps. This program developed a single chip monolithic GaAs Heterojunction Bipolar Transistor (HBT) ADC that includes a sample-and-hold (S/H) and all of the active circuitry required for stand alone operation (Figure 1-1). Although less than 60 percent of the definitized contract value was funded, the ADC development was taken through design, layout, fabrication of one lot, wafer probe, packaging of several parts, and initial ADC trimming. Electrical trimming was accomplished on the first 5 most significant bits (msbs) and triangle and sine waveforms were processed through the ADC. Excellent signal to noise (SNR) performance was obtained with only the 5 msbs trimmed. Considerably higher performance is anticipated with further ADC checkout and trim. Significant accomplishments that were achieved include:

- ADC design and layout completed
- Processed one lot of 7 wafers. All 4 MBE wafers had good circuits with an average yield of 18 percent (34 percent for best wafer). Three MOCVD wafers had low beta.
- Wafer probed 4 wafers
- Packaged several ADCs
- Demonstrated working ADCs in GaAs HBT process with laser trimmable CERMET (500 ohms/sq.) resistors
- Demonstrated highest reported SNR of 49.7 dB for a GaAs ADC

ADC features include:

- Successive approximation architecture
- 1 bit digital error (overrange) correction
- Electrically and laser trimmable

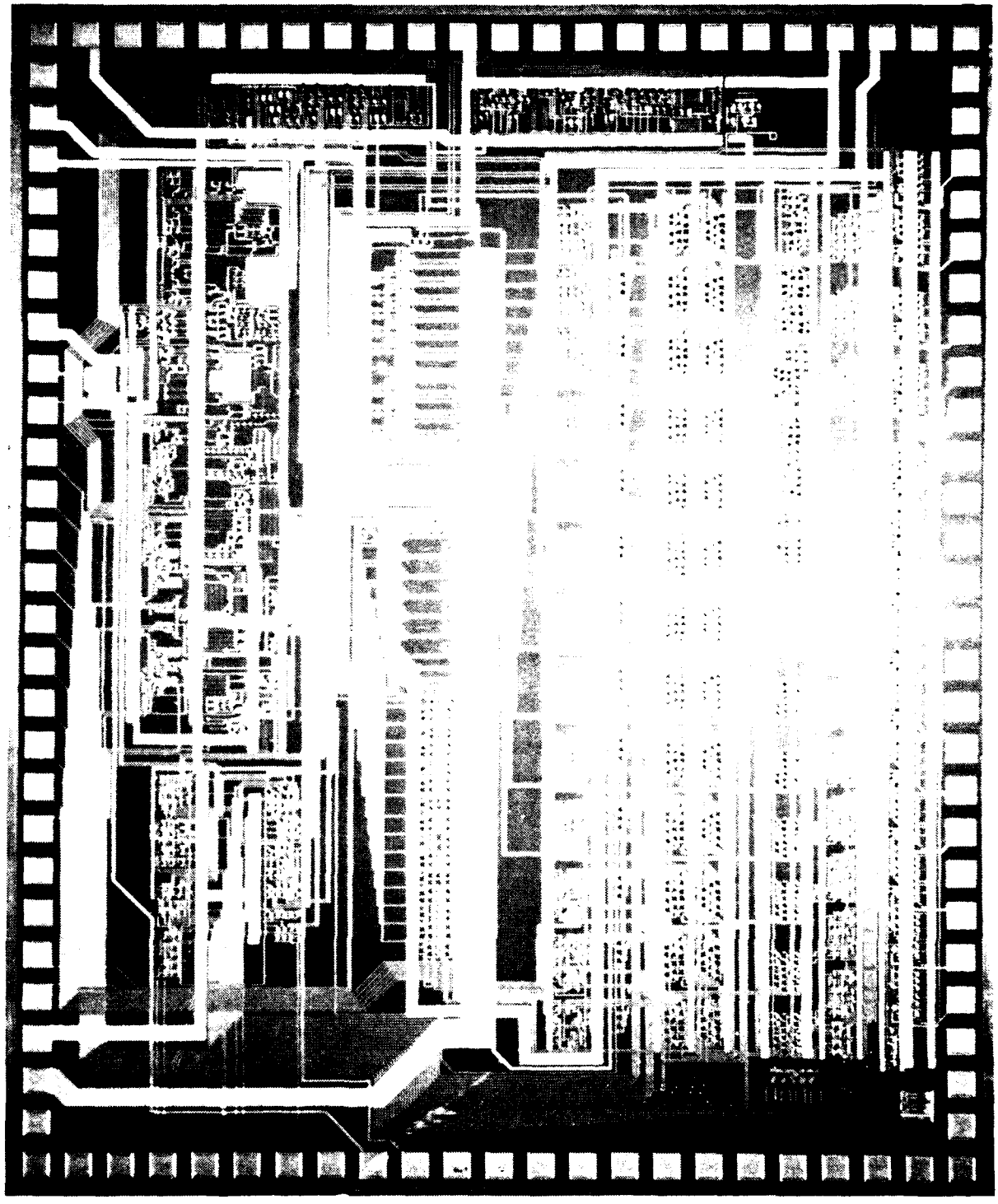


Figure 1-1. GaAs HBT 12-bit, 20 Msps, 1.2 W ADC

- 6 on-chip operational amplifiers
- On-chip bandgap voltage reference
- 1855 transistors, 48 diodes, 1.2 W power consumption
- 4.15 X 3.40 mm die size

Figure 1-2 lists the ADC program goals. ADC design and analysis showed that all of the goals are achievable, however a front-end self-calibration function is required to correct ADC gain and offset drift error. A study was performed on the contract to determine the feasibility of adding a front-end capability to the ADC including: analog multiplexing, auto-ranging, and self-calibration. The study concluded that such a front-end function was possible, and that it should be fabricated on a separate chip for highest yield and application flexibility.

ADC testing at both wafer probe and as packaged parts was curtailed by limited funding, however, significant performance was achieved. ADC performance is demonstrated by the digital-to-analog conversion of the ADC chip's output shown in Figure 1-3 for a triangle input waveform, and by Figure 1-4 which shows the ADC output for a 15 MHz sinewave input. The ADC has flat frequency response from 10 KHz to 15 MHz. The complete ADC test results are covered in Section 4.

Parameter	Goal
A. Accuracy	
1. resolution	12 bits
2. relative accuracy	±1.0 LSB
3. gain error	±1.0 LSB
4. gain error drift	≤2.0 ppm/°C
5. offset error	±0.5 LSB
6. offset error drift	≤2.0 ppm/°C
7. noise	≤0.5 LSB
B. Speed	20 MHz word rate
C. Input bandwidth	8 MHz at -3 dB
D. Input resistance	1 M ohm
E. Input voltage range	5.25 V
F. Output	Capable of driving TTL load 12 bits parallel Data valid or EOC signal
G. Power	1 W/20 Msps
H. Monotinicity	No missing codes to 12 bits
	Every code combination must appear in a monotonically increasing sequence as the analog input is increased.

Figure 1-2. ADC Program Goals

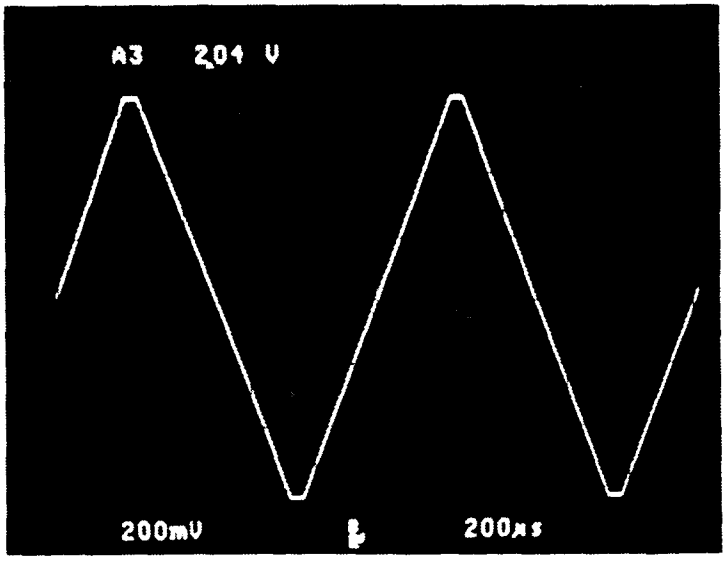


Figure 1-3. Digital to Analog Conversion of ADC Output for Triangle Wave Analog Input (Bit Clock = 90 MHz, Word Clock = 2 MHz)

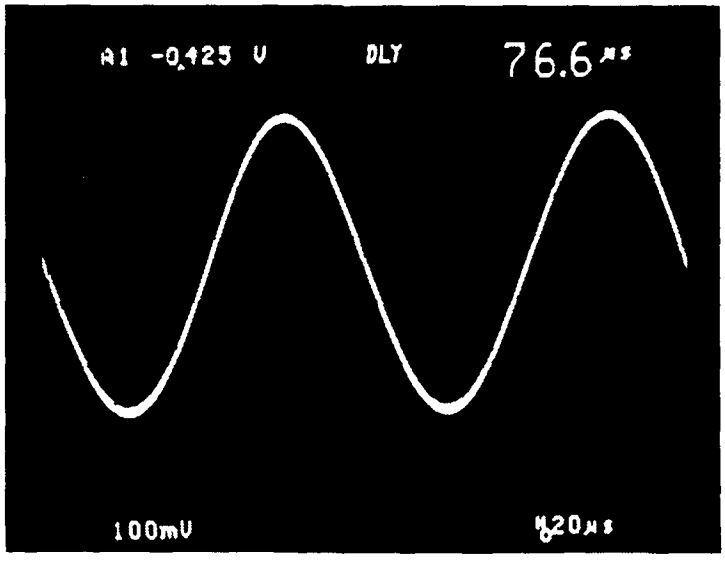


Figure 1-4. Digital to Analog Conversion of ADC Output for 15 MHz Sinewave Analog Input (Bit Clock = 90 MHz, Word Clock = 5 MHz)

2. ADC DESIGN

The ADC is a single chip GaAs HBT circuit that includes a sample and hold as well as all active circuitry required for stand alone operation. It requires four power supplies and two clocks. The ADC employs a modified successive approximation architecture with digital error correction and thus uses 13 conversion cycles + 5 cycles for sample-and-hold (S/H) acquisition. Laser trimming of CERMET resistors is used to compensate for device match limitations and guarantees 12-bit accuracy. Provision for electrical trimming is made through the use of optional package pins.

2.1 OVERVIEW

Several ADC architectures were considered and the choices narrowed to feedback algorithms. Feedforward architectures were rejected due to their difficulty of achieving the low power goal. Figure 2-1 lists the major factors in selecting between single bit feedback (successive approximation) and multibit feedback architectures. The preponderance of the factors favor the single bit approach and it was therefore selected. The ADC block diagram is shown in Figure 2-2. The ADC is wholly self- contained including both a S/H and voltage reference on the chip. The ADC consists of two successive approximation stages of 7 msbs and 6 least significant bits (lsbs) with a 1-bit overlap to allow for digital error correction. The two stages have separate comparators and DAC circuits which are wired together such that the two comparators see the same analog input and a common DAC output. The first 3 bits of the msb DAC are segmented and the remaining 4 msb and 6 lsb bits are a conventional R/2R configuration. The fine comparator, which determines the 6 lsbs, is gated off during the 7 msb conversion cycles such that its front-end stage does not develop a thermal offset due to the analog input signal and DAC voltages. Therefore, when the lsb comparator decisions are made there is no thermal history affecting those decisions.

Droop in this ADC architecture is canceled to a first-order by a droop correction DAC which generates a staircase of increasing currents to create a "droop" in the DAC output voltage to match the S/H droop. This technique has the drawback of limiting the bit clock rate to a limited range, nominally 360 MHz. The digital error correction also provides correction for S/H droop, S/H settling error, and coarse comparator hysteresis.

Feature	Single Bit Feedback (Successive Approximation)	Multi-Bit Feedback
Architecture Characteristics	Low Speed High Accuracy (Few Error Sources)	Medium Speed Medium Accuracy (Numerous Error Sources)
DAC Accuracy	Critical	Critical
Comparator Accuracy	No Effect	Critical
Amplifier Accuracy	None Required	Critical
Conversion Clock Speed	360 MHz	Lower
S/H Droop	Critical (But can be easily calibrated along with Gain and Offset)	Less Sensitive
Complexity (Transistors)	Low	Medium - High
Power Consumption	Low	Medium

Figure 2-1. Architecture Tradeoff

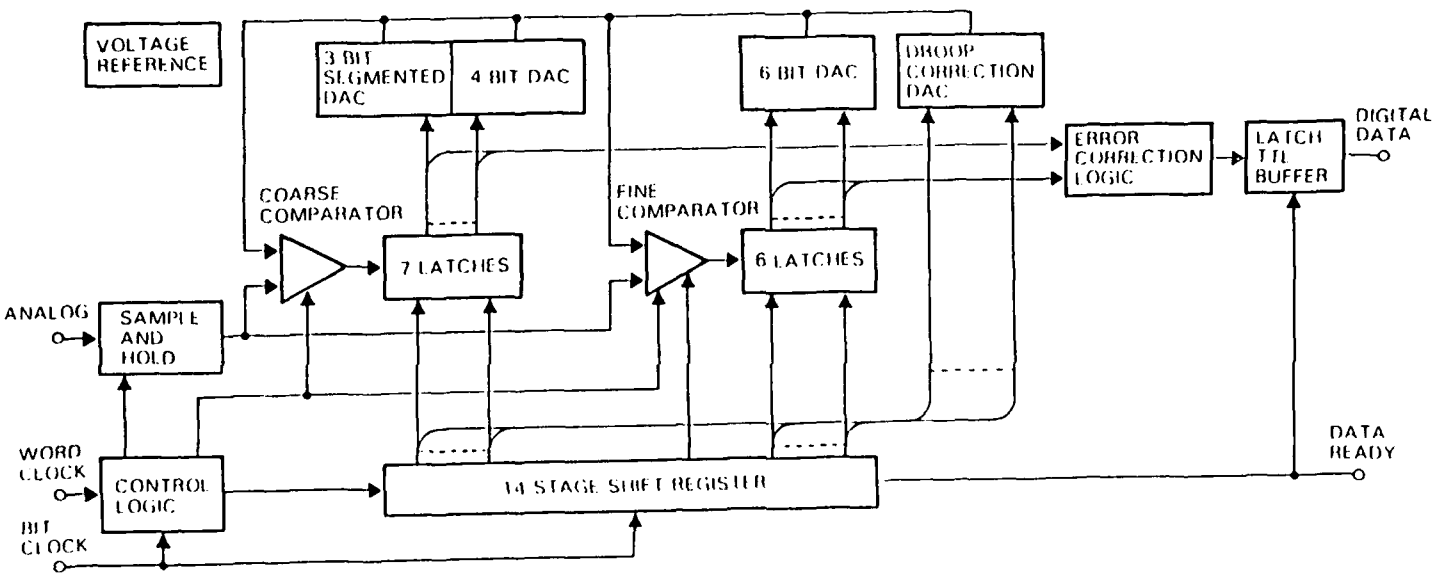
The ADC operates on 360 MHz clock and requires 18 cycles per conversion to obtain 20 Msps. Reduced conversion rates can be obtained by reducing the word clock below 20 Msps while maintaining the bit clock at a nominal 360 MHz for proper droop correction.

The parts count and power for the major circuit blocks of the ADC is shown in Figure 2-3. The ADC has been designed to operate over a -25 to +100°C temperature range with ± 5 percent variation on the supply voltages.

2.2 CIRCUIT DESIGN

2.2.1 Sample and Hold (S/H)

The Sample and Hold (S/H) circuit performs the function of tracking the analog input signal and periodically holding samples of that signal for the ADC quantizer section to digitize. The ADC is then only required to quantize what is essentially a dc signal during the conversion period. The S/H output is not actually constant but droops approximately 20 mV per cycle. Droop compensation is achieved by generating a corresponding droop in the DAC.



- ► Power 1.2 W
- ► Analog range ±1.6 V
- ► Distortion −84 dBc
- ► Thermal noise 400 uV RMS
- ► Signal-to-noise ratio 68 dB (at 25°C)

Figure 2-2. 20-Msps 12-Bit ADC Block Diagram

032/92-WP-175

Circuit Block	Transistors	Diodes	Power (mW)
Sample-and-Hold	108	38	250
DAC Circuits	409	0	324
Comparators	109	5	128
SAR	432	2	102
Droop Compensation	81	1	56
Offset Control	56	2	58
Voltage Reference	41	0	42
Gain Control	26	0	63
I/O	593	0	185
Totals	**1855**	**48**	**1208**

Figure 2-3. 20-Msps 12-bit ADC Device Count and Power Summary

The S/H circuit consists of pre and post amplifiers connected around a Schottky diode bridge switch driving a metal-oxide-metal (MOM) hold capacitor. Additional support circuitry is required for bootstrapping, bias control, and clock buffering. The S/H block diagram appears in Figure 2-4.

Preamplifier

The S/H preamplifier (preamp) is a single-emitter follower with compensation circuitry to eliminate thermal error and reduce high frequency dynamic distortion. The emitter follower is bootstrapped using a differential amplifier for level shifting. Bootstrapping the input stage forces the input transistor to dissipate constant power eliminating thermal V_{be} modulation by the signal. A major source of dynamic distortion for the preamp arises from the signal current that must be supplied to the hold capacitor at high frequency. This distortion is nearly eliminated by feeding forward an approximation of that current so that it is not supplied directly from the preamp transistor. The feedforward current is supplied by the bootstrapping amplifier to conserve power.

Bridge

The bridge circuit uses a Schottky diode balanced bridge biased by constant current sources. The current source on the negative side is a single transistor source while the positive side uses bootstrapped resistors to generate constant current. The voltage across the resistors is held at approximately 4 V (varying slightly with power supply and temperature) by driving them with a level shifted replica of the output signal.

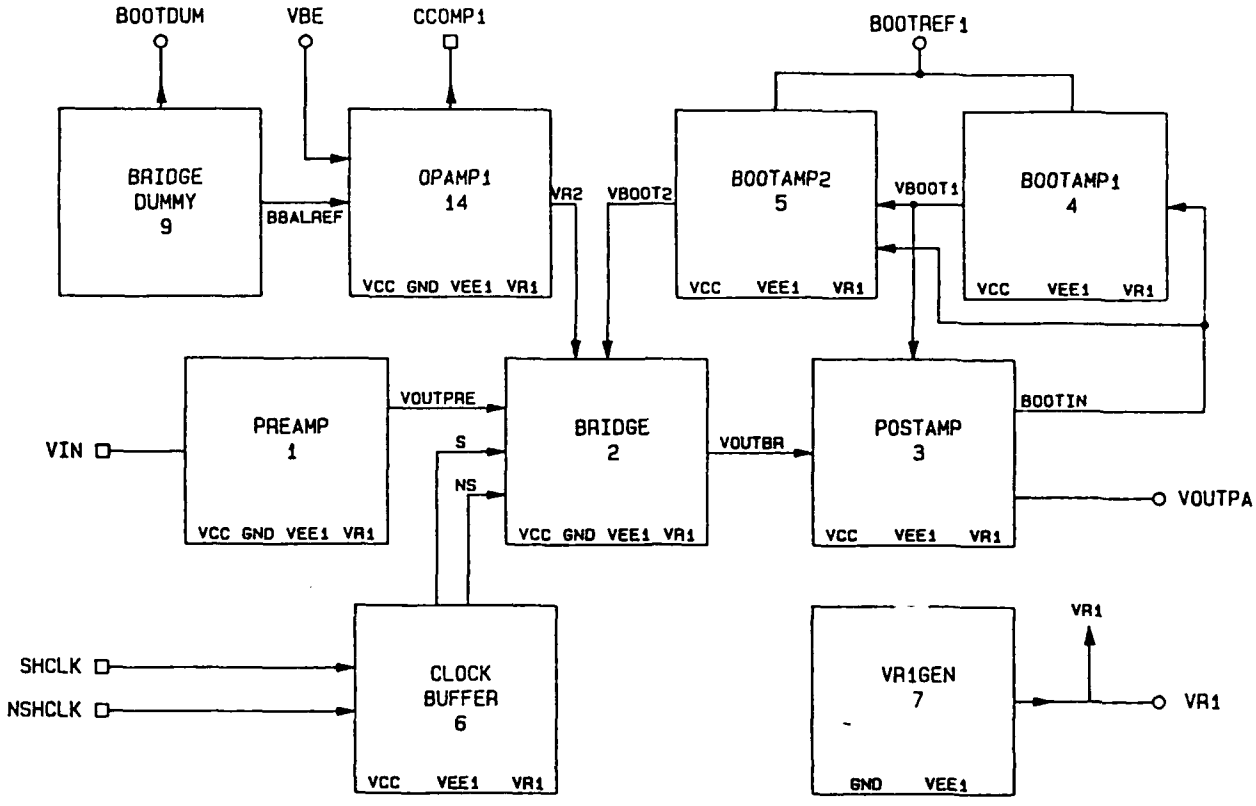


Figure 2-4. Sample and Hold

Biasing the bridge this way allows the switch to float with respect to ground so that no signal current flows through the diodes except the small ac current supplied to the hold capacitor. When the bridge is switched-off, the constant current nature of the resistors is lost and their respective currents are signal dependent.

The bridge is required to be clamped to some voltage when turned-off to ensure subsequent changes in input voltage cannot forward bias any of the diodes causing excessive feed through. Normally, the top and bottom of the bridge are clamped at fixed voltages above and below the held value. This requires the source of the clamp voltages to follow the hold voltage through a buffer and level shifter. This type of clamp uses significant power and circuitry as well as requiring voltage swings in the bridge that are twice as large as the signal swing. A much simpler clamp, which is used in this design, has two permanently fixed voltages (one high and one low) for the top and bottom of the bridge. This method has the undesirable effect of a signal dependent hold jump resulting from unequal charges being dumped onto the hold capacitor by the

switch diodes, which produces gain errors and distortion. In the HBT process however, the shunt capacitance of the Schottky diode is very small compared to the value of the hold capacitor and the effect of the hold jump is reduced. More importantly, in this application, the S/H and quantizer are both on the same chip which allows the S/H errors to be trimmed out along with the quantizer errors during calibration. As a result, the undesirable effect of using the simple clamp are eliminated.

Postamplifier

The postamplifier (postamp) is a bootstrapped double emitter follower driving a positive level shift and output emitter follower. The input stage is biased at extremely low current to minimize input bias current for lowest possible droop. Bootstrapping all emitter followers eliminates thermal errors and reduces input capacitance. Positive level shift is accomplished by generating a positive current from a bootstrapped resistor to bias a string of two transistors and Schottky diodes. This positive shift added to the -4 V_{be} level shift through the emitter followers has the net result of yielding a S/H output voltage of -1.8 V at 25°C . The temperature coefficient of offset is approximately -1.8 mV/°C for an offset voltage spread of -1.66 to -1.89 V over temperature. This range conveniently allows the relative offset between S/H and DAC to be adjusted by sourcing current from the DAC.

Bootstrap Amplifiers

The bootstrap amplifiers are emitter degenerated differential pairs that drive resistive loads tied to V_{CC}. Separate amplifiers are used for the bridge and the postamp to provide isolation from the quantizer (S/H output) and the hold capacitor, and to prevent distortion induced in the postamp level shift from feeding back to the bridge. Because the bootstrap amplifier's load resistor is connected to V_{CC}, common mode output voltage is power supply dependent causing bridge balance and S/H offset to demonstrate poor power supply rejection. The rejection problem is eliminated by using operational amplifier control loops for bridge balance and offset that compensate for supply drift and noise.

Bridge Dummy and Operational Amplifiers

The bridge dummy, an abbreviated and scaled version of the actual bridge, generates an output voltage equal to -1 V_{be} when the bridge is balanced. Balance is adjusted by carrying the negative current source via VR2. When the negative source

value is equal to the positive source value, VR2 has reached its correct voltage and properly biases the bridge. OPAMP1 uses a negative V_{be} reference for the loop and has sufficient gain for required accuracy and power supply rejection. C_{comp1} is an external connection to a 0.01 µF compensation capacitor.

2.2.2 Droop Compensation

Droop compensation is required to cancel the effects of hold capacitor discharge during conversion. The discharge of the S/H hold capacitor is very linear due to the constant beta and emitter current of the postamp input transistor. S/H droop is expected to run at about 1.88 lsb per bit clock cycle which must be compensated during all comparator decisions after the error correction redundant DAC cycle. Because of noise and power considerations, it was determined that the best approach is to induce a linear droop into the DAC output voltage that equals the S/H hold capacitor droop thereby causing the droop error to be rejected by the high common mode rejection ratio (CMRR) of the comparator. The droop is induced by connecting a linear, fully segmented current DAC to the main DAC R/2R ladder. The droop compensation DAC is an array of 12 current switches whose digital inputs are connected to the successive approximation register in a staggered fashion such that one switch turns on per bit clock cycle and stays on for the duration of the conversion period. The droop compensation DAC taps into the R/2R ladder at "DAC5". There is an attenuation factor of 16 from "DAC5" to the main DAC output. The selection of this tap point is chosen to optimize the current in the DAC switches at about 50 µA which represents low power but reasonable current density for high beta in the switch transistors.

The current in the droop compensation DAC is made to track the input current of a postamp dummy circuit by an operational amplifier servo loop as shown in Figure 2-5. Droop is assumed to be a linear function of this single parameter since the origin of droop is the drain of charge off of the hold capacitor by the constant current loading of the postamp input. This requires that the droop compensation current be initially trimmed since the hold capacitor must be matched by the product of a conductance and bit clock period. The stability of capacitance, bit clock frequency, and resistor conductance allow the tracking requirements of those parameters to be unimportant. Input bias current tracking of the postamplifier and its dummy is then the only requirement for droop compensation accuracy over time and temperature.

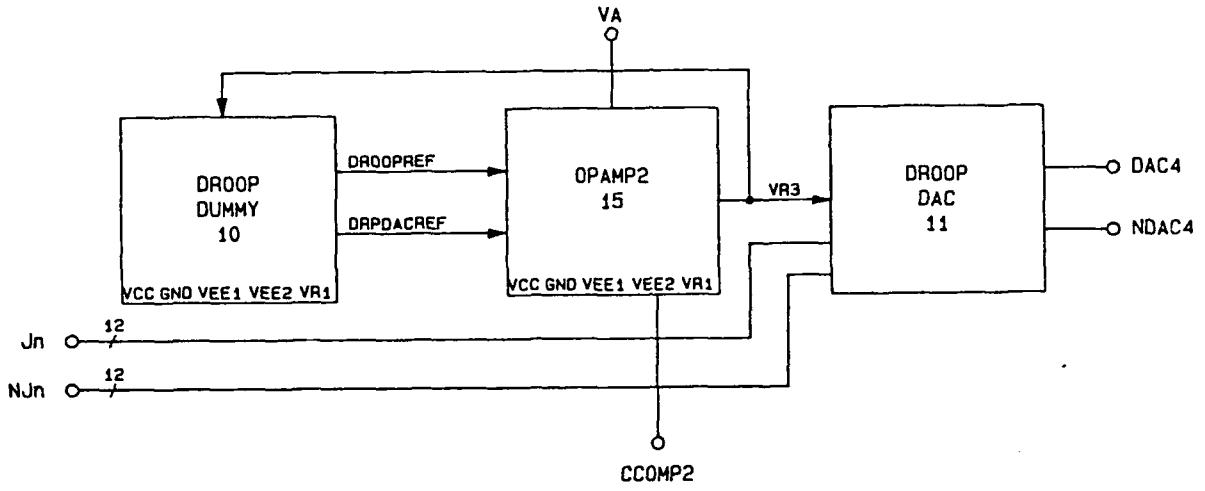


Figure 2-5. Droop Compensation Control

2.2.3 ADC Offset Control

ADC offset control (Figure 2-6) is accomplished by sourcing current from the dummy DAC until its mid-scale voltage is equal to the output voltage of the dummy S/H with its input grounded. The same current (actually, a multiple thereof) is sourced from the main DAC to force its mid-scale voltage to the same level. Offset voltage is then reduced to the mismatch between the dummy circuit and actual circuit. The mismatch is laser trimmed at calibration and maintained over temperature and supply voltage by the circuit tracking. Offset can be externally controlled by driving the input of the dummy S/H from an external voltage source.

Offset Generator

The offset generator is a current source nearly identical to the main DAC current sources, and is tied to the output of the main DAC. A common base transistor is inserted between the current source and the DAC to prevent any DAC transients from upsetting the operational amplifier loop. The common base stage also avoids possible breakdown problems as under extreme temperature and supply conditions the collector-base voltage could reach 10.6 V. With the common base stage the collector-base voltage is limited to 5.5 V.

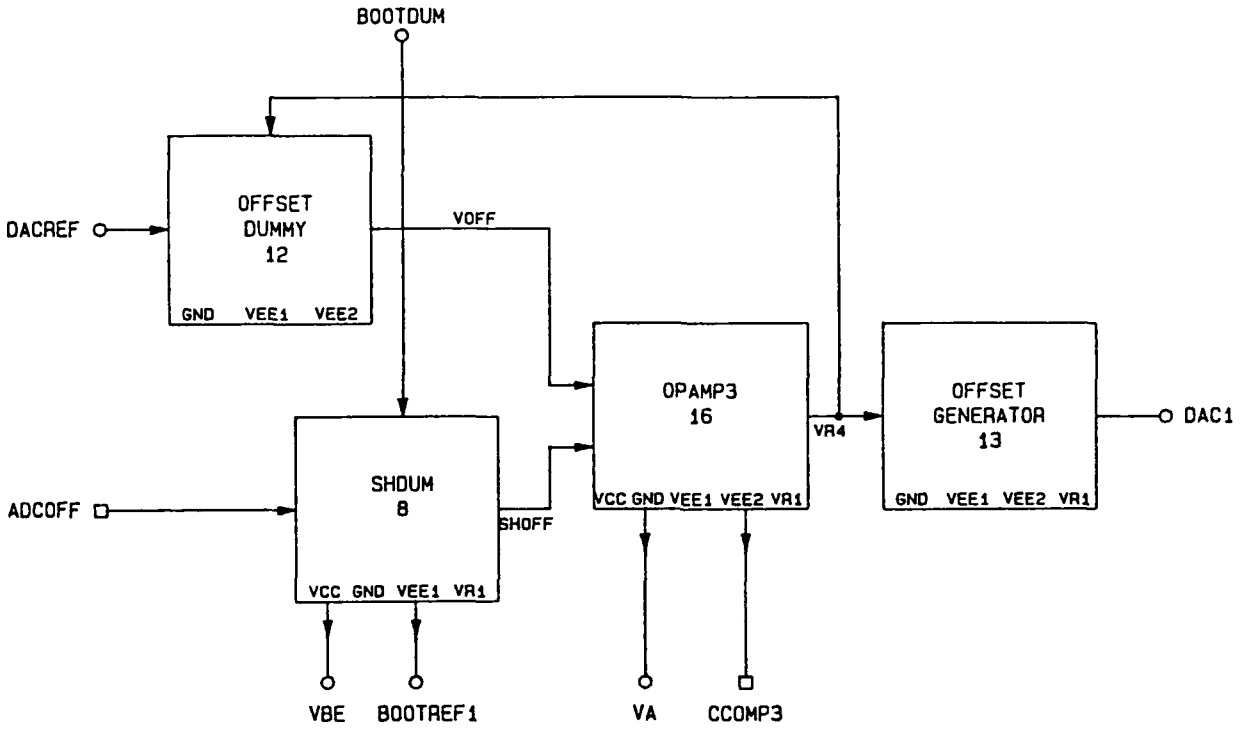


Figure 2-6. ADC Offset Control

Offset Dummy

The offset dummy consists of a cascaded current source modeling the main DAC and another cascaded current source modeling the offset generator both driving a common load resistor connected to ground. It was not necessary to model the R/2R ladder and an array of current sources to generate a replica of the mid-scale DAC voltage because of the high HBT transistor output impedance. High output impedance means that output current is independent of voltage and thus a single current source driving a single load is an accurate model of an array of current sources driving a network of resistor loads. The load and current source resistors are trimmable to calibrate offset to zero.

S/H Dummy

The S/H dummy generates an output voltage equal to the S/H level shift and provides a bias voltage for the bootstrap amplifiers. There is some difficulty power scaling this dummy as the actual postamp has a single emitter 3x3 μm transistor in the signal path that cannot be scaled down. The output stage is scaled by a factor of four

so that the intermediate stage (the level shift) is split into two with one side scaled by 4 and the other by 1.33. The small level shift drives the scaled output stage correctly while the larger level shift conveniently provides the necessary reference for the bootstrap amplifiers. An external pad is connected to the input of the S/H dummy for external offset control.

OPAMP3

The operational amplifier drives the current sources in the offset generator and main DAC. It uses an external capacitor for compensation and has sufficient gain for power supply rejection.

2.2.4 Gain Control

Gain control is accomplished by driving the current sources of the DAC with an operational amplifier that has as its input the outputs of the bandgap voltage reference and the DAC dummy circuit (Figure 2-7).

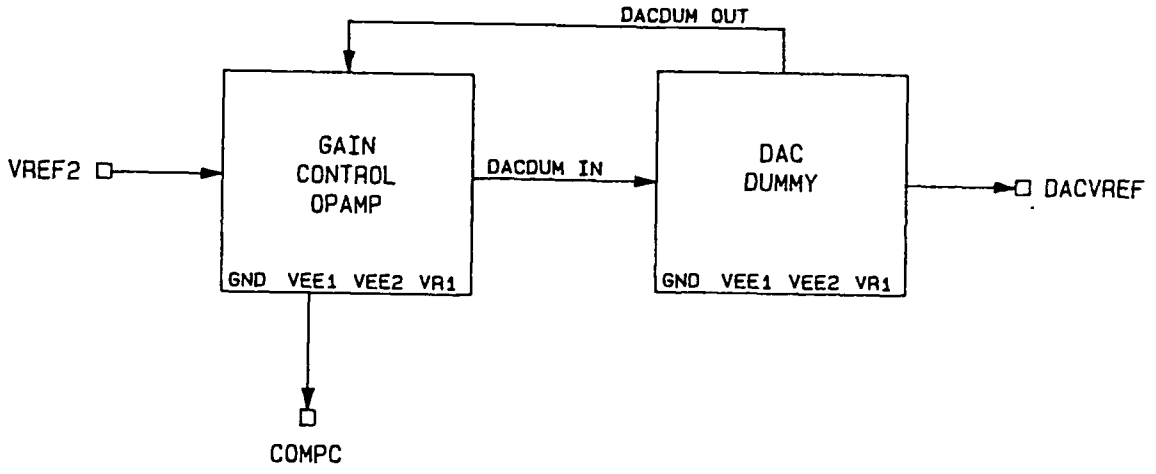


Figure 2-7. ADC Gain Control

The DAC dummy is a quarter-scale representation of the DAC. By using an appropriately sized resistor as the DAC dummy load, the full scale DAC output voltage is modeled. The operational amplifier forces the output of the DAC dummy to be equal to the bandgap reference voltage thereby ensuring that the gain of the ADC is correct within processing parameter variations. The final ADC gain adjustment is made by laser trimming the DAC dummy's load resistor. Gain Control Circuit performance for the DAC operating at midscale is shown in Figure 2-8.

Parameter	Value
DACOUT (midscale)	-1.6 V
ΔDACOUT -25 to +100°C	100 μV
Noise Density at 10 KHz	11.6 nV/ √Hz
Total noise to 2 GHz	158 μV
V_{EE1} Power Supply Rejection Ratio	-74.4 dB
V_{EE2} Power Supply Rejection Ratio	-64.4 dB
Gain Control Circuit Input Current	271 nA

Figure 2-8. Gain Control Circuit and Midscale DAC Specifications

2.2.5 Comparators

The ADC relies on two comparators for quantization. The first is a coarse comparator that is used for the first seven conversion cycles and has a thermal hysteresis limited accuracy of ~2 mV. Comparator errors up to 12 mV from the coarse quantization are corrected by an additional quantization cycle. The fine comparator is employed for the quantization cycles after the error correction and exhibits thermal hysteresis below 10 μV.

The fine comparator is preceded by a preamplifier to greatly reduce thermal errors and the probability of comparator indecision. The preamp has a gain of 35 and is designed to be turned off during coarse quantization to prevent saturation of the input transistors and nearly eliminates thermals since the differential input voltage is below 20 mV when switched on. The preamp also conditions the signal to eliminate the 3.2 V common mode swing to normal current mode logic levels at the fine comparator.

2.2.6 Digital-to-Analog Converter

The ADC uses a 12 bit-DAC to convert the digital approximation of the analog input signal back to analog for comparison to the input analog signal. The 3 msbs of the DAC are segmented into 7 separate current generators and switches. The remaining 10 bits of the DAC are binary weighted by virtue of an R/2R ladder. Segmenting the 3 msbs provides improved DAC linearity at the expense of increased parts count. The DAC is comprised of a 13-bit data register (which provides for one bit of error correction), 3-bit segmenting logic, 17 current switches, and a 10-bit R/2R ladder as shown in Figure 2-9.

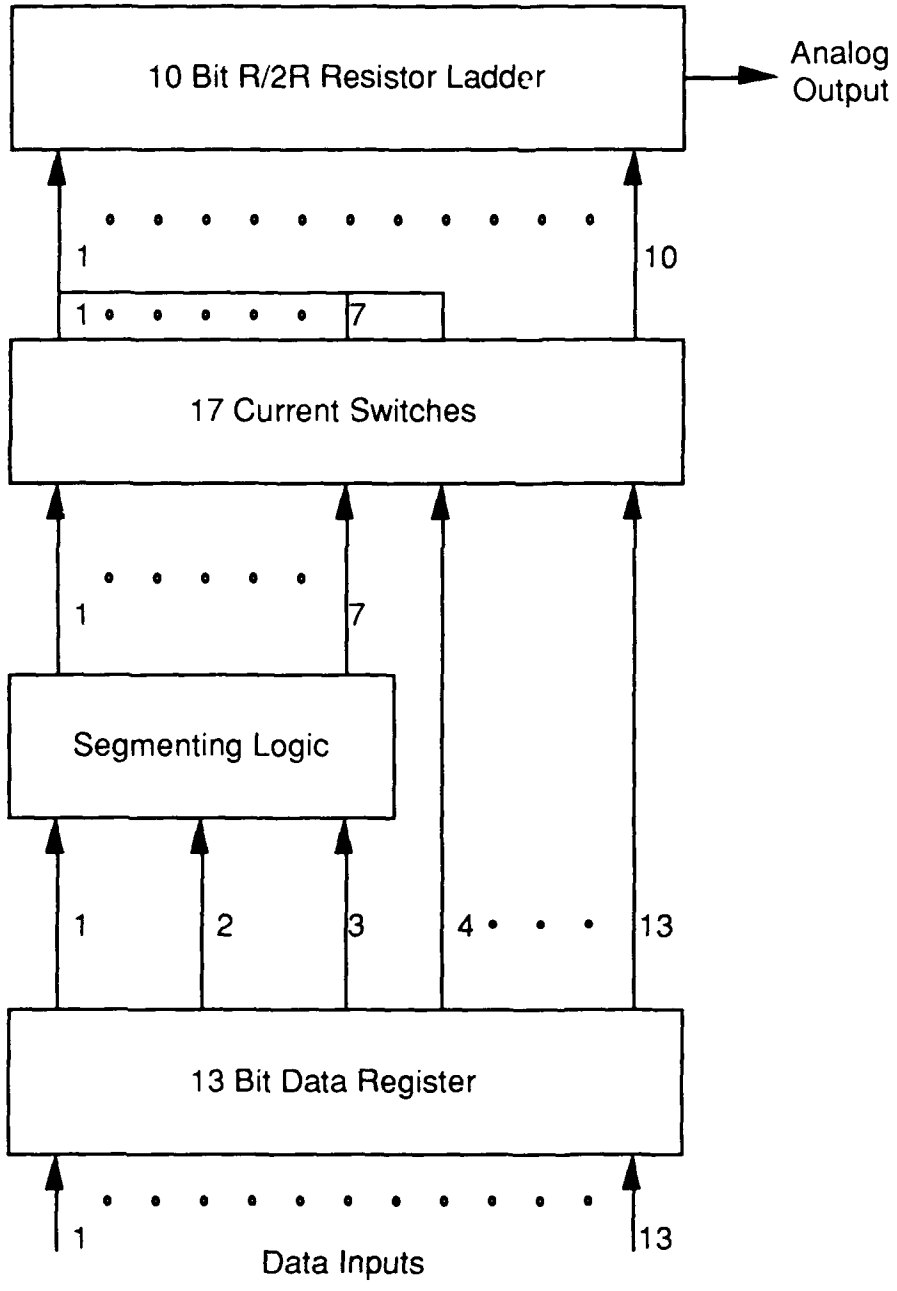


Figure 2-9. Partially Segmented DAC

2.2.7 Voltage Reference

The voltage reference is a bandgap circuit capable of driving at least 10 ADCs. The output reference voltage is -3.2 V which is also the full scale DAC output voltage and ADC voltage range. The voltage reference uses two operational amplifiers, as shown in Figure 2-10. One operational amplifier ensures the proper operation of the bandgap circuit (BGAP OPAMP) and the other provides level shift (BGAP OPAMP2). Separating these functions allows the temperature coefficient and offset of the voltage reference to be adjusted independently. Two resistors in the bandgap circuit are laser trimmable to either increase or decrease the temperature coefficient of the reference voltage. A laser trimmable resistor in the second operational amplifier is used to set the output voltage. Performance of the voltage reference is given in Figure 2-11.

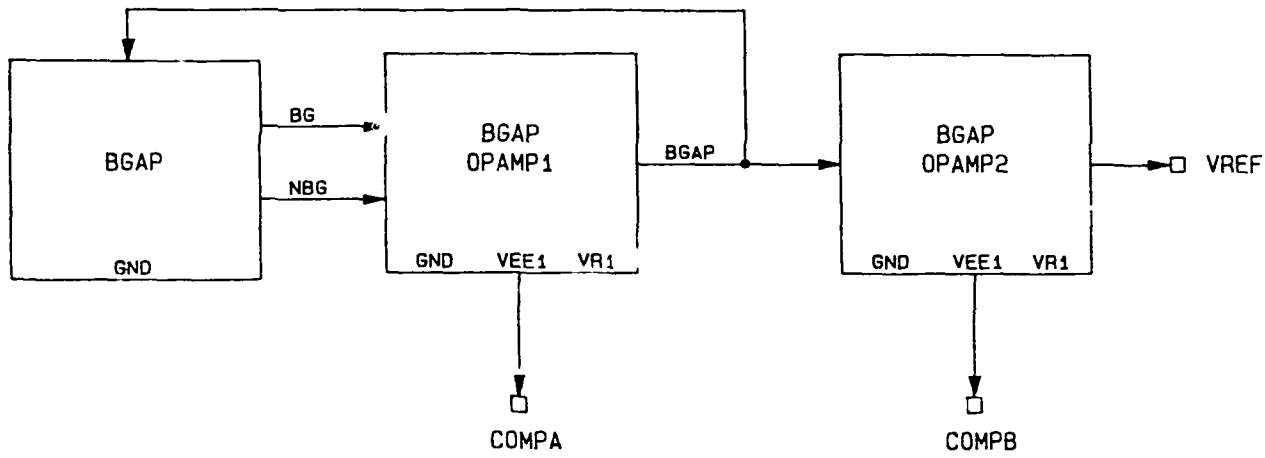


Figure 2-10. Bandgap Voltage Reference

2.2.8 Operational Amplifiers

There are six operational amplifiers used in the A/D: two in the bandgap reference, and one each in the control loops for droop compensation, offset, gain, and bridge balance. Operational amplifiers in the bandgap are inaccessible and must operate correctly for that circuit to work. If necessary, the bandgap circuit can be replaced with an off-chip reference. The four other loops can use external operational amplifiers in case of internal amplifier failure. Three package pins are dedicated to each control loop. An external capacitor (0.01µf) is required on the output of each internal operational amplifier used.

Parameter	Value
Vref	-3.2 V
ΔVref -25 to +100°C (after trim)	40 mμV
ΔVref	
10 loads	200 μV
50 loads	1.2 mV
100 loads	2.2 mV
Noise Density at 10 KHz	89.1 nV/√Hz
Total noise to 2 GHz	74 μV
Short Circuit Protection	Yes
V_{EE1} Power Supply Rejection Ratio	-50.4 dB
Phase Margin	
C_{LOAD} = 0.001 μF	85°
C_{LOAD} = 0.01 μF	55°

Figure 2-11. Bandgap Voltage Reference Predicted Performance

2.2.9 HBT Models

The HBT models used in the simulations of the ADC were established in 1987 and are illustrated in Figure 2-12. Model parameters are based on geometrical considerations as well as experimental results.

The collector-base capacitance was calculated for a 7000 Å epitaxial thickness and Nd = 6.3 x 10^{15}CM $^{-3}$. This profile and doping level combine to give a fully depleted epitaxial region near zero bias. Since the epitaxy is fully depleted, the collector-base capacitance is linear.

2.3 ADC SYSTEM CONSIDERATIONS

2.3.1 Error Correction

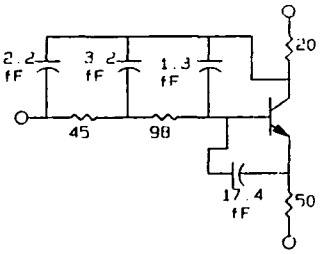
The A/D uses digital error correction to compensate for S/H settling, thermal hysteresis, and droop compensation limitations among other error sources. The correction technique is implemented by modifying the normal successive approximation algorithm such that two successive DAC bits are equal in magnitude. This establishes an allowable error range equal to the extra range of the DAC. Figure 2-13 shows the 13 decisions and DAC changes for the error corrected 12-bit converter. With an LSB of

LSI 3 x 3

Spice Model

```
.subckt lsi3x3bo 1 2 3
q 4 5 3 hbt
rbx 2 6 45
rbi 6 5 98
cjx1 2 4 2.2f
cjx2 6 4 3.2f
cjx3 5 4 1.3f
rcx 1 4 20
.model hbt npn(va=150 vje=1.4 mje=.5 br=.001
+ tf=4p re=50 cje=17.4f nf=1.07 ne=1.66 is=2.1e-25
+ bf=1e6 ise=1.3e-19)
.ends
```

BF = 50



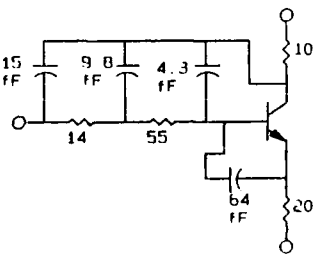
TF=4p
BF=50 @ 0.25mA
WB=1500 A
Na=6E18 cm^{-3}
xd=7000 A
Pc=3E-6 ohm cm^2
RSH=650 ohm/sqr
lt=0.68 um

SE 3 x 10

Spice Model

```
.subckt se3x10bo 1 2 3
q 4 5 3 hbt
rbx 2 6 14
rbi 6 5 55
cjx1 2 4 15f
cjx2 6 4 9.8f
cjx3 5 4 4.3f
rcx 1 4 10
.model hbt npn(va=150 vje=1.4 mje=.5 br=.001
+ tf=4p re=20 cje=64f nf=1.07 ne=1.66 is=8.4e-25
+ bf=1e6 ise=.52e-18)
.ends
```

BF = 50



TF=4p
BF=25 @ 1mA
WB=1500 A
Na=6E18 cm^{-3}
xd=7000 A
Pc=3E-6 ohm cm^2
RSH=650 ohm/sqr
lt=0.68 um

SD 5 x 5

Spice Model

```
model sd5x5 d(is=4.3e-17 cj0=20ff rs=12 pb=1.25)
```

Figure 2-12. GaAs HBT SPICE Models

	2 0 4 8	1 0 2 4	5 1 2	2 5 6	1 2 8	6 4	3 2	3 2	1 6	8	4	2	1	Delta
	1	0	0	0	0	0	0	0	1	0	0	0	0	
1	XC1	1	0	0	0	0	0	0	1	0	0	0	0	± 1024
2	XC1	XC2	1	0	0	0	0	0	1	0	0	0	0	± 512
3	XC1	XC2	XC3	1	0	0	0	0	1	0	0	0	0	± 256
4	XC1	XC2	XC3	XC4	1	0	0	0	1	0	0	0	0	± 128
5	XC1	XC2	XC3	XC4	XC5	1	0	0	1	0	0	0	0	± 64
6	XC1	XC2	XC3	XC4	XC5	XC6	1	0	1	0	0	0	0	± 32
7	XC1	XC2	XC3	XC4	XC5	XC6	XC7	1	0	0	0	0	0	± 16
8	XC1	XC2	XC3	XC4	XC5	XC6	XC7	XF8	1	0	0	0	0	± 16
9	XC1	XC2	XC3	XC4	XC5	XC6	XC7	XF8	XF9	1	0	0	0	± 8
10	XC1	XC2	XC3	XC4	XC5	XC6	XC7	XF8	XF9	XF10	1	0	0	± 4
11	XC1	XC2	XC3	XC4	XC5	XC6	XC7	XF8	XF9	XF10	XF11	1	0	± 2
12	XC1	XC2	XC3	XC4	XC5	XC6	XC7	XF8	XF9	XF10	XF11	XF12	1	± 1
13	XC1	XC2	XC3	XC4	XC5	XC6	XC7	XF8	XF9	XF10	XF11	XF12	XF13	

XC = Course Comparator decision
XF = Fine Comparator decision

Figure 2-13. Algorithm for Error Corrected A/D

781 μV, the error correction range of the A/D is ± 25 mV. The decisions made at and after the redundant DAC bit are performed by the fine comparator. The offset mismatch of the coarse and fine comparators is also corrected by the digital error correction logic by making the comparator swap at the redundant cycle. At the end of the conversion, the DAC holds a 13-bit word representing a 12-bit approximation of the ADC input. The logical conversion of this 13-bit word to a 12 binary representation is performed by the error correction logic. Figure 2-14 shows the logic function that takes place.

Coarse DAC Code	XC1	XC2	XC3	XC4	XC5	XC6	XC7	0	0	0	0	0
Add Fine DAC	0	0	0	0	0	0	XF8	XF9	XF10	XF11	XF12	XF13
Subtract 32	0	0	0	0	0	0	0	1	0	0	0	0
	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1
		MSB								LSB		

Figure 2-14. Error Correction Logic

2.3.2 Trimming and Calibration

Trimming the A/D requires adjustment for offset, gain, droop, and level errors. Offset, gain and droop are trimmed by annealing resistors or electrically by summing currents in their respective operational amplifier control loops. Level errors are trimmed by directly altering the value of the DAC current sources either by resistor annealing or current summing. All DAC current sources are laser trimmable while electrical trims are possible only for the first 9 current sources representing the 5 msbs. The purpose of the electrical trim is threefold. First, electrical trimming is preferred for laboratory analysis since it is fast, simple, and nondestructive. Second, electrical trims can make the laser anneal trim process easier. The laser trim can be performed upon a part that is being continuously electrically trimmed by a computer. The part is therefore properly trimmed when the computer indicates that the required electrical trim has reduced to zero. This ability to replace electrical trims with laser trims eliminates the need for subsequent trim iterations. Performing electrical trims also tells the operator in advance how much trimming will be necessary, as well as whether the part will be trimmable at all.

2.3.3 Timing

The ADC requires two external clocks, WORDCLOCK (WCLK) and BITCLOCK (BCLK). For normal operation, WCLK is nominally 20 MHz and BCLK is 360 MHz. S/H settling and track times are controlled by the phase between WCLK and BCLK. The S/H settling time is two BCLK periods, and the S/H track time is four BCLK periods as drawn in the ADC timing diagram Figure 2-15.

S/H settling and track times are affected by the frequency relationship between WCLK and BCLK. Increasing the frequency of BCLK relative to WCLK decreases the S/H settling time and increases the S/H track time. The S/H goes into track between the thirteenth and fourteenth BCLK periods. The Data ready (DREADY) signal becomes true as the output data changes. On the falling edge of DREADY, the output data is ready to be latched.

The coarse comparator clock (CCLK) is enabled at the start of the ADC cycle and disabled at the end of the coarse conversion cycle. The CCLK is disabled after the coarse conversion so that transients from the coarse comparator do not upset the ADC.

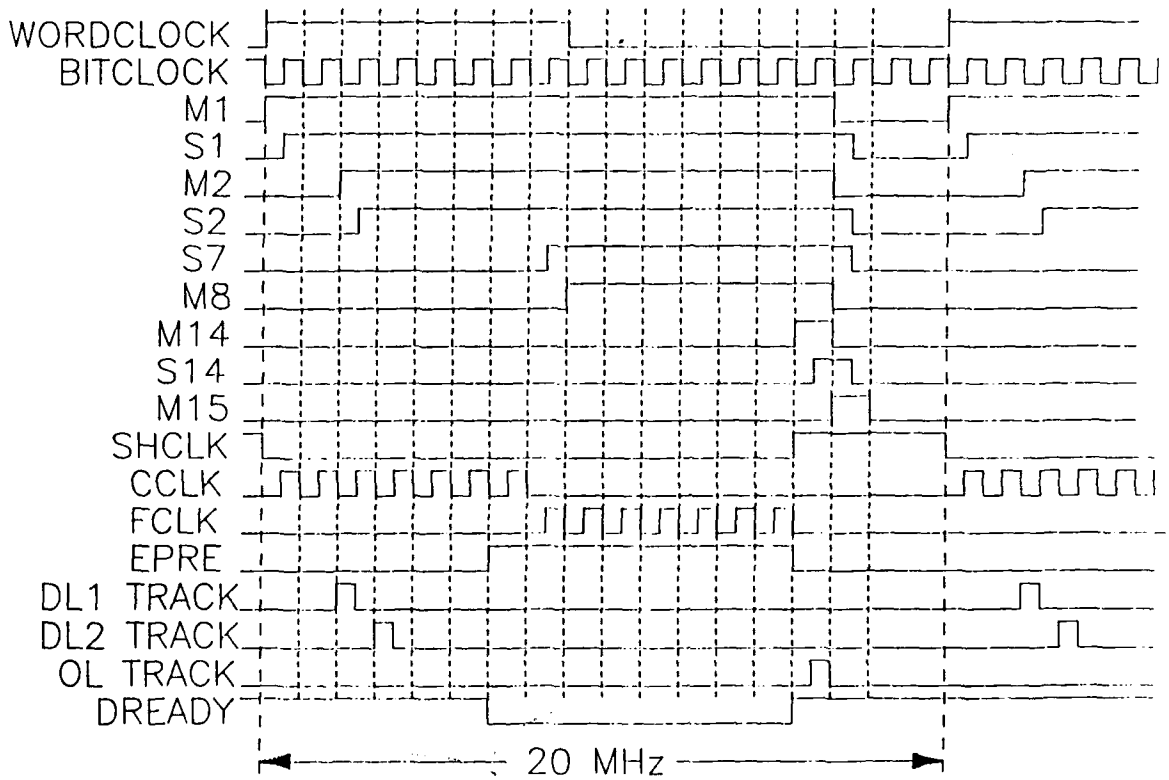


Figure 2-15. ADC Timing Diagram

The fine comparator clock is disabled after the fine conversion for a similar reason. The fine comparator's preamp is enabled 1.5 BCLK periods before the fine comparator to give the preamp ample settling time. The fine comparator's preamp is disabled during the coarse conversion so that its input transistor pair is not subjected to a differential voltage which would lead to thermal errors.

2.3.4 Test Mode

There is a pin named TEST that floats during normal ADC operation and is grounded when ADC operation in the test mode is desired. In the test mode, the S/H clock (SHCLK) is determined solely by the WCLK, the fine comparator is clocked through a pin named INTCLK, and the fine comparator's output is buffered and sent to an output pin named FCOMPOUT. INTCLK has a logic threshold -1 V_{be} and can float during mode operation. FCOMPOUT is disabled in normal mode and swings from 0 to -1V in the test mode.

Another option is available through a pin named SUBSAMP. Through this pin, the output latches can be subsampled in normal or test mode. When SUBSAMP floats, the output latches operate normally. When SUBSAMP is above a -1V threshold, the output latches hold the data and are not updated.

Since there is an overlap of 1 bit between the coarse and fine DAC's, there are two possible DAC latch sequences for each output code. Output signal D13 is the buffered version of signal DL6 which is the output of the last DAC latch in the coarse conversion. Through D13, the DAC latch sequence can be uniquely determined to aid testing.

2.4 PERFORMANCE PREDICTIONS

2.4.1 Accuracy

Accuracy requirements for the ADC are expressed as several parameters including resolution, relative accuracy, gain and offset error, gain and offset drift, and noise. The ADC resolution is 12 bit by design. The relative accuracy (linearity) is determined principally by trimming the ADC. Finite output impedance in the DAC current switches which would limit the DAC (and therefore ADC) linearity is significantly reduced with the high early voltage GaAs HBT devices.

The gain and offset requirements of ± 1 lsb for the ADC are met by using laser trimming. The proposed front-end analog multiplexer chip incorporates gain and offset calibration circuitry to meet the ±2 ppm/°C gain and offset drift requirement. Without this chip the ADC gain and offset drift is estimated to be ±50 ppm/°C.

Noise in the A/D is the sum of three dominant noise sources: the first is noise in the preamp; the second is the noise at the filtered output of the S/H postamp with the S/H in track; the third is the noise at the output of the fine comparator preamp and includes DAC noise with the DAC input simulated by a 400 ohm source impedance driven by half the major current sources. The noise breakdown is as follows (25°C):

S/H preamp	73 μV	
S/H postamp	99 μV	
DAC/Comparator	195 μV	
TOTAL	230 μV	RMS

2.4.2 Speed and Bandwidth

The critical sample rate timing budget is show in Figure 2-16 for two transistor geometries. The ADC was fabricated with 3x5 μ emitter transistors. The program plan was to replace these with 3x3 μ emitter transistors in the design revision. The program was not fully funded and the design revision never happened. The 3x5 μ devices result in a sample rate ~21 percent short of the 20 Msps/W goal, while the 3x3 devices were projected to exceed the goal by 25 percent based on the ADC power of 1.2 W. The ADC input bandwidth is estimated to be 50 MHz, far exceeding the 8 MHz requirement.

Circuit	Transistor Emitter Size	
	3 x 3 μm	3 x 5 μm
SAR	90 ps	150 ps
DAC Latch	270 ps	390 ps
DAC	1200 ps	2050 ps
Preamp	200 ps	240 ps
Fine Comparator	110 ps	100 ps
Total bit clock cycle time	1870 ps	2930 ps
Maximum sample rate	30 MHz	19 MHz

Figure 2-16. ADC Timing Budget

2.4.3 Interface Requirements

Input resistance is expected to exceed the 1 MΩ requirement tenfold. The high input resistance is the result of using a bootstrapped emitter follower input stage. Input voltage range for the ADC was selected to be lower than the 5.25 V specification. The input range of 3.2 V was chosen as a compromise between the higher power consumption and distortion that would result from a larger input voltage, and the increased relative magnitude of thermal noise for a smaller input voltage range. The digital data output of the ADC has been designed to have a TTL compatible interface.

2.4.4 Distortion

Distortion in the ADC was calculated using Spice (computer aided circuit analysis) for both static and dynamic performance. Static distortion results from curvature in the dc transfer characteristic while dynamic distortion only occurs in the presence of large fast moving input signals. The S/H has a curvature in its dc transfer curve that results in a -80 dB third harmonic. Trimming of the DAC will compensate this error to a practical limit of -90 dB. Dynamic distortion is calculated by Spice simulation of the S/H which is the only source of dynamic error. Analysis with a full scale 7 MHz signal applied to the S/H input and a DFT calculated from the output data shows ADC performance better than -85 dB for any spur.

2.4.5 Performance Prediction Summary

The ADC characteristics and predicted performance are given in Figure 2-17.

Parameter	Performance	Units
Resolution	12	Bits
LSB Weight	781	μv
Accuracy		
Monotonicity	Guaranteed	
Offset TC	50	PPM/°C
Gain TC	50	PPM/°C
Dynamic Characteristics		
Distortion (fully loaded)		
500 KHz input	90	dB BFS
7 MHz input	85	dB BFS
Thermal Noise	270	μV rms
Jitter	0.4	ps rms
SNR	70	dB
Conversion Time	18	Bit Clock Cycles
Conversion Rate	19 / 30	Msps (max)
Acquisition Time (1/5 LSB)	10	nsec
Settling Time (1 LSB)	2.8	nsec
Input Bandwidth		
Small Signal 3dB	350	MHz
Large Signal 3dB	50	MHz
Analog Input		
Range	±1.6	V
Range Adjust	±5	%
Bias Current	20	μA
Impedance	10	M Ω
Clock Input		
Differential ECL Input		
Common Mode Range	0 to -2	V
Minimum DIff Voltage	0.3	V
Bit Clock		
Frequency	360	MHz
Duty Cycle	50	%

Figure 2-17. ADC Characteristics and Predicted Performance

Parameter	Performance	Units
Word Clock		
Frequency	20	MHz
Pulse Width	5	nsec min
Rise/Fall Times	2	nsec min
Digtial Output		
Format	12 parallel; NRZ	Bits
Logic levels TTL Compatible	0 = 0.6 1 = 2.5	V
Drive		
Source	100	µA
Sink	1	mA
Coding	Binary	
Data Ready Output		
Logic Levels TTL Compatible	0"= 0.6 1 = 2.5	V
Drive		
Source	100	µA
Sink	1	mA
Rise/Fall Time	5	nsec min
Pulse Width	22	nsec min
Performance Requirements		
+8.4V ±5%	19.7	mA
+6V ±5%	8.4	mA
-8.4V ±5%	82.1	mA
-12.0V ±5%	26.5	mA
Power Consumption	1.22	W
PSSR (any supply to 1 MHz)	50	dB min
Temperature Range		
Operation	-25 to +100	°C

Figure 2-17. ADC Characteristics and Predicted Performance (Continued)

3. FABRICATION

High circuit yields on the recently completed wafer lot was obtained using the Self-Aligned Base ohmic Metal (SABM) process. Stepper alignment photolithography was chosen for high process yield. The molecular beam epitaxy (MBE) structures were also optimized to improve performance margin. InGaAs emitter cap reduced emitter contact resistance, which in turn improved V_{be} uniformity. The modified graded AlGaAs emitter layer at the emitter-base junction was proven to increase the current gain (ß).

3.1 MBE MATERIAL

The key to the high dc current gain and high cutoff frequency (f_t) of npn HBT transistors and Schottky diodes is a high quality epitaxial starting material. MBE was used to grow uniform, reproducible GaAs/AlGaAs heterostructures on 3-inch semi-insulating undoped liquid-encapsulated Czochralski (LEC) GaAs substrates. Silicon was used for n-type doping and beryllium for p-type doping.

Figure 3-1 illustrates the baseline MBE profile (Profile 9) used for the SABM HBT technology. This profile includes linearly-graded aluminum at the emitter-base interface to suppress the heterojunction barrier spike and maximize the current gain. The thin base layer (1400Å thick) reduces base transit time (high f_t), and the high doping concentration (1×10^{19} cm^{-3}) reduces base contact and bulk resistance (high f_{max}). The thick lightly-doped collector layer (7000Å thick, 7×10^{15} cm^{-3}) significantly reduces the collector-base capacitance.

In addition to the profile enhancements, significant improvements in material reliability have been made over the past two years. The MBE growth process has been optimized to minimize beryllium out diffusion into the emitter layer – an industry-wide problem. We have used a combination of increased As/Ga flux ratio and reduced substrate temperature to control Be incorporation and minimize Be^+ interstitial generation during MBE growth. Over 2000 hours at 240°C of lifetest data confirm that the profile provides a dramatic improvement in the reliability of HBT devices. This high reliability MBE profile has a projected mean time to failure (MTTF) of $>1.0 \times 10^8$ hours at 125°C junction temperature with a failure criteria of 10 percent decrease in ß. We were the first in the world to report high reliability HBT.

The ADC process lot was composed of 4 TRW-grown MBE wafers and 3 vendor MOCVD wafers. The n^+ GaAs emitter contact layer on TRW wafers is replaced by a

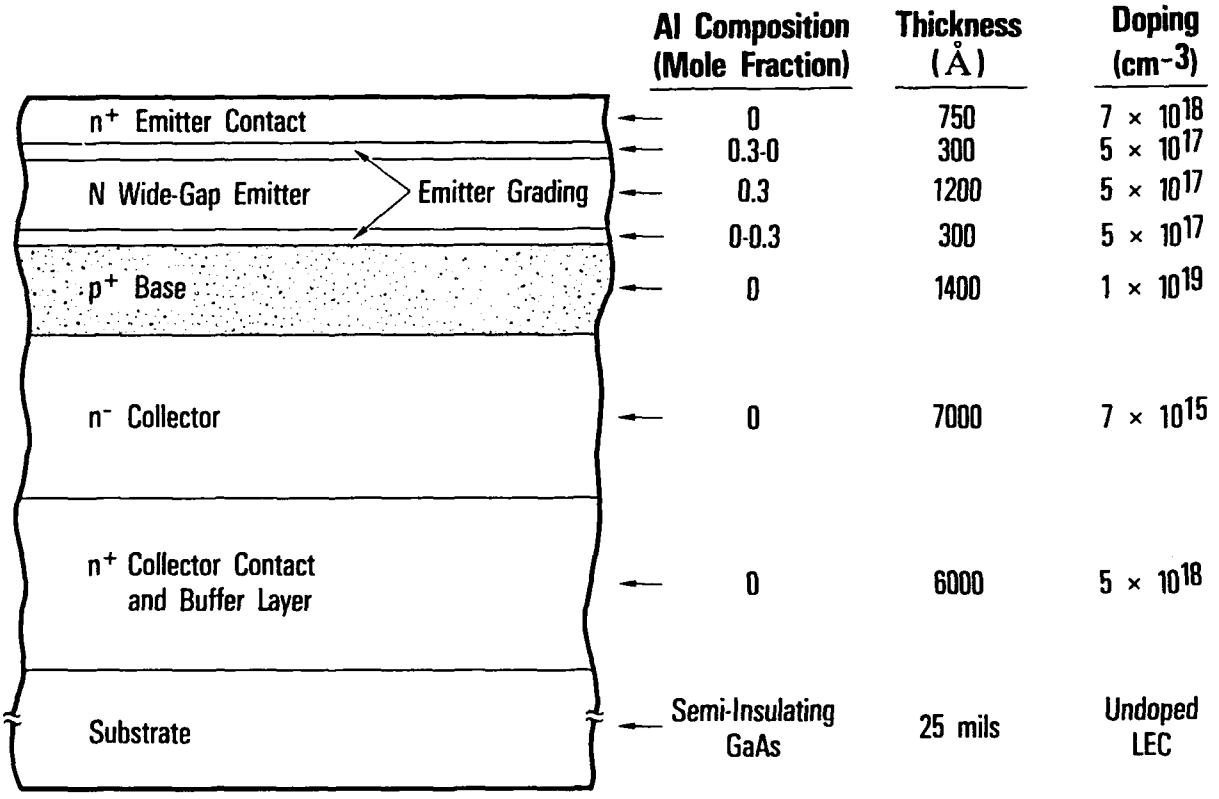


Figure 3-1. MBE Profile 9

$In_{0.5}Ga_{0.5}As$ graded to GaAs layer. This InGaAs layer enables us to use a non-alloyed refractory metal contact (Ti/Pt/Au). Not only do refractory contacts to InGaAs provide low emitter contact resistance, but they are also extremely thermally stable. The graded AlGaAs emitter layer at the emitter-base junction of TRW wafers has also been modified to reduce the emitter-base depletion capacitance and to increase dc current gain. The performance impact from this advanced profile is described in the following subsection.

3.2 3 μm EMITTER SABM HBT IC PROCESS

The SABM process is a simple modification of the non self-aligned (NSA) HBT process available at the beginning of this program. The NSA process used contact photolithography to access the collector, base, and emitter contact layers. The base ohmic contact and the emitter mesa were defined by two separate masking steps. The SABM HBT IC process structure shown in Figure 3-2 is aimed at significantly increasing the device f_{max} and circuit switching speed by essentially eliminating the parasitic inactive base resistance. This is achieved by using a double-photoresist lift-off technique to self-align the base ohmic metal to within ≈ 0.2 micron of the emitter mesa edge. Yield

for this process step is essentially 100 percent. A cleaved cross-section of the self-aligned base ohmic metal is shown in Figure 3-3. The rest of the process uses the same optical lithography used in the NSA HBT process, except that stepper alignment (vs. contact alignment) and 3-inch (vs. 2-inch) wafers are used to increase circuit yield.

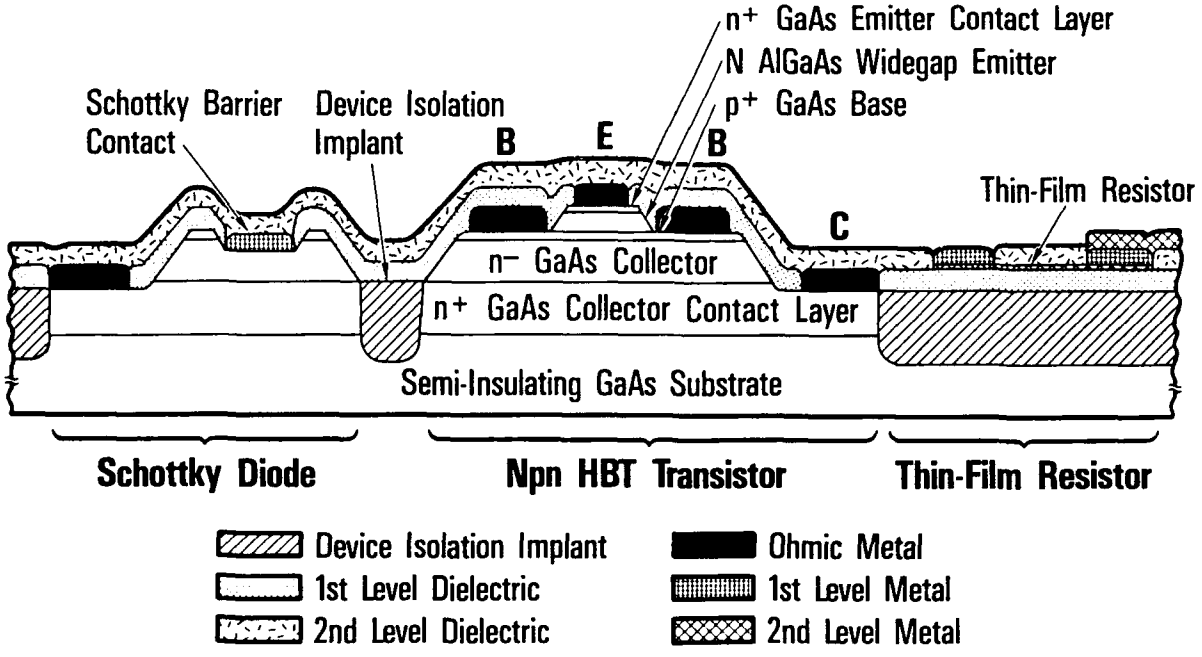
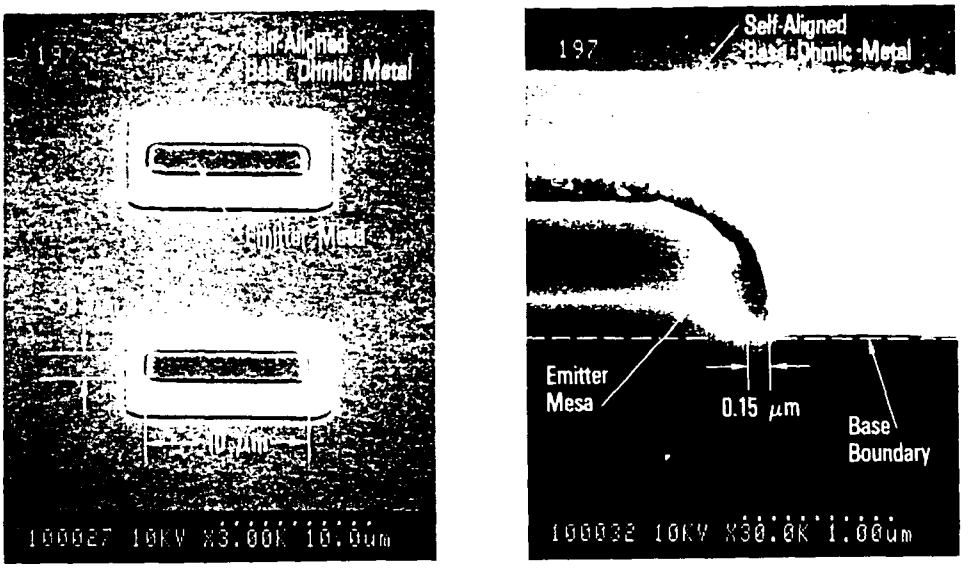


Figure 3-2. Self-Aligned Base Ohmic Metal HBT IC Structure

A flowchart describing the SABM MMIC processing sequence is shown in Figure 3-4. There are fourteen masking steps in this process. This process uses a series of selective and non-selective wet chemical etches to access the base and collector layers. The photoresist used to define the emitter mesa self-aligns the base ohmic metal deposition to within 0.2 μm of the emitter mesa edge, significantly reducing the external parasitic base resistance and increasing f_{max}. AuBe/Pd/Au and AuGe/Ni/Ti/Au are used for the p-type and n-type ohmic contacts, respectively. Recently processed wafers all use Ti/Pt/Au non alloyed contacts to graded n-type InGaAs. Isolation is provided by multiple boron implants. Plasma-enhanced CVD silicon nitride is used for surface passivation.

Scanning Electron Microscope Photographs



$3 \times 10\ \mu m^2$ Emitter HBTs
(Differential Transistor Pair)

Cleaved Cross-Section

Figure 3-3. Self-Aligned Base Ohmic Metal Process Structure

Other device components integrated with the HBT device are a Schottky barrier diode, a laser trimmable CERMET thin film resistor, and a MIM capacitor. The active and passive components are interconnected using a two level metal (8000Å Ti/Pt/Au first metal and a 2.0 μm thick Ti/Au second metal), and plasma-enhanced CVD silicon nitride for the interlevel dielectric.

3.3 FABRICATION RESULTS

In addition to numerous detailed process refinements (particularly metalization and nitride deposition procedures), the following SABM HBT process features have improved device performance and increased fabrication yield:

- Use of an optimized InGaAs cap layer has resulted in low emitter contact resistance
- Use of a higher base doping has resulted in low base contact resistance
- Use of optimized MBE growth conditions has produced very high reliability combined with high dc current gain
- Use of 3-inch GaAs substrates and stepper alignment photolithography has improved wafer yield significantly.

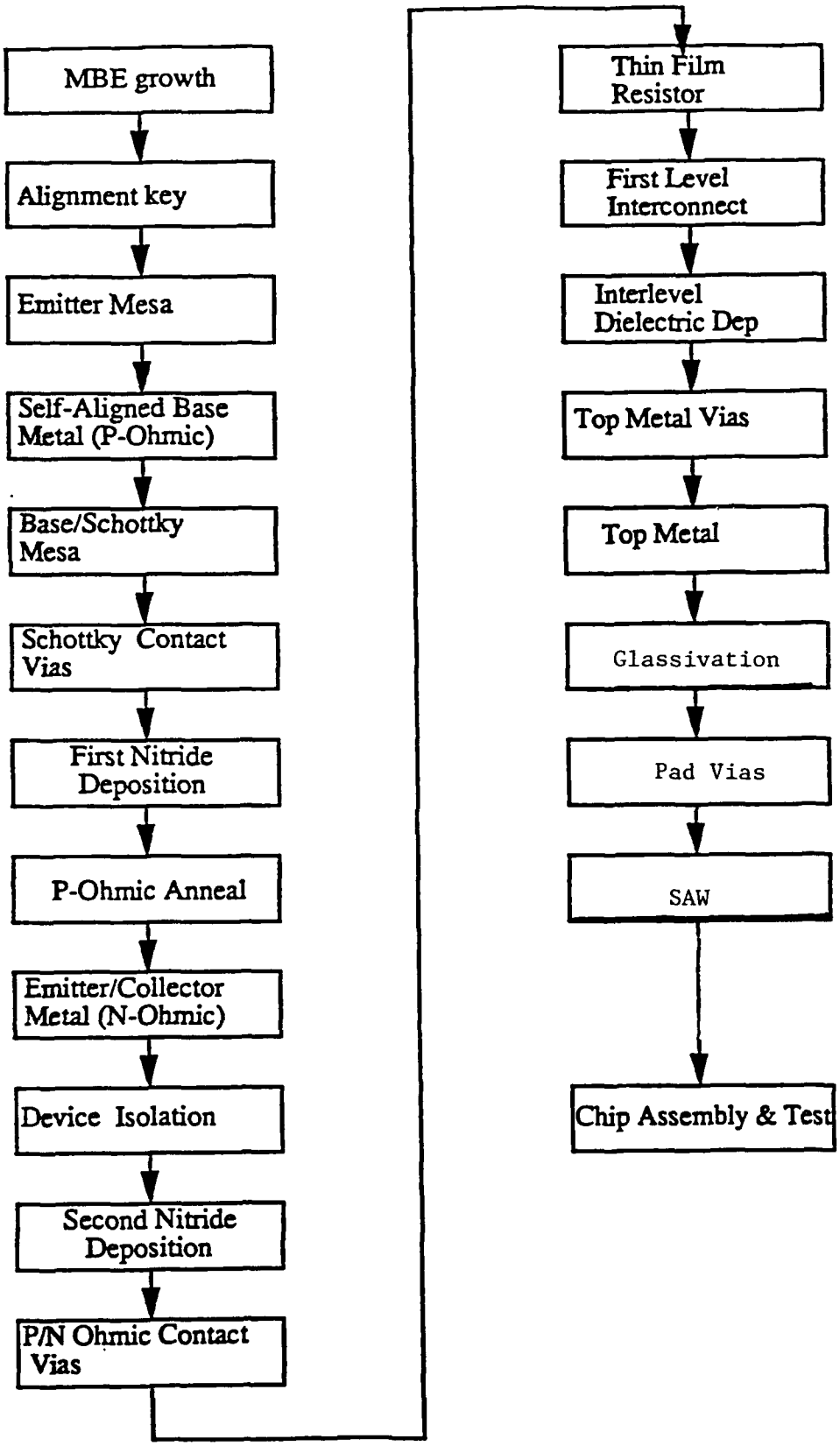


Figure 3-4. HBT Process Flow Chart

Implementation of the high yield SABM IC process with optimized MBE profile provides high f_{max}, providing increased speed margin for the ADC devices (Figure 3-5).

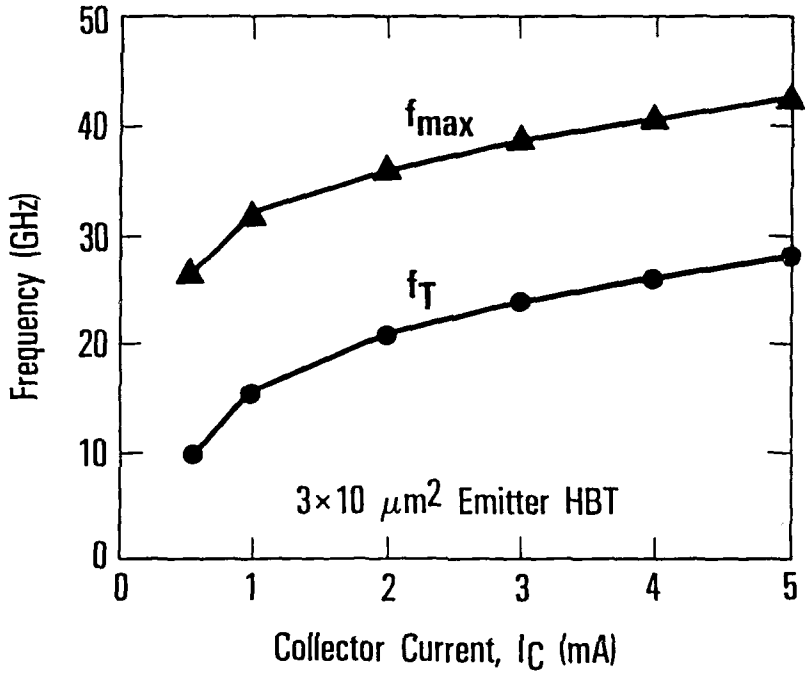


Figure 3-5. Self-Aligned Base Ohmic Metal (SABM) HBT

The ADC wafer lot was fabricated in our class 10 fabrication line. The wafers encountered no problems in the process and were successfully completed. The only poor wafers were the vendor MOCVD. All of the MOCVD wafers had low current gain (less than 10), and were not completed.

Only one wafer lot was processed for the program. The success in the first lot processing of 4 MBE wafers allowed replacing the second wafer lot originally planned with packaging, packaged parts laser trim, and test tasks.

3.4 DEVICE TEST RESULTS

The wafer lot consisted of four TRW grown MBE wafers with InGaAs contacts and three vendor MOCVD wafers. As shown in Figure 3-6, the TRW MBE wafers have high beta (65 to 74 at 1 mA collector current), and very low emitter contact resistance. The low Re is the result of the incorporation of an optimized InGaAs contact layer. The high

Wafer Spec ⇒	Beta	Re 4-25Ω	Rb 20-65Ω	Rc 1-40Ω	TFR 425-525Ω/sq
175-047	65	5.2	29.2	4.9	415
175-063	71	5.7	30.2	3.0	482
175-084	72	7.1	28.2	3.5	460
175-085	74	7.7	27.1	4.3	508

Figure 3-6. MBE Wafer Process Parameters

ß is the result of the improved emitter profile. This data confirms the improvement made in device parametrics as a result of the overall MBE enhancements. The base and collector contact resistance remain low with this advanced profile.

The ADC wafers were measured to have excellent V_{be} matching, which is critical to ADC threshold level errors. Excellent circuit yield of 18% averaged over the 4 MBE wafers has been achieved. We have successfully delivered the 12-bit ADC with only one wafer lot fabricated.

4. TEST RESULTS

Wafer probe and preliminary packaged part testing of the ADC was performed. Wafer probe testing concentrated on determining functionality. Packaged part testing focused on SNR and level error tests.

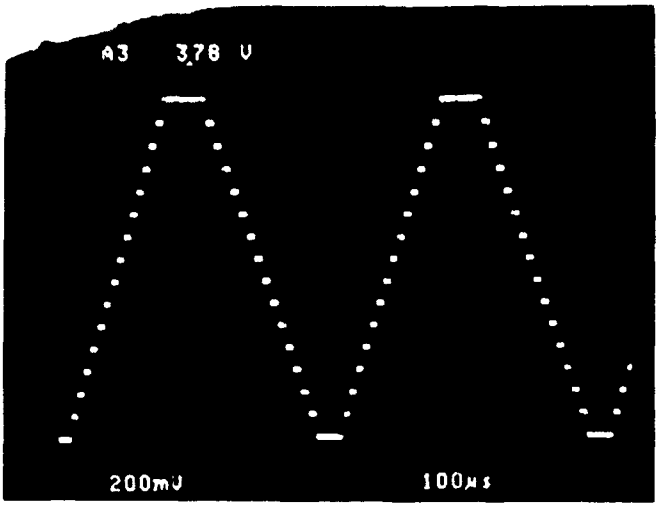
4.1 WAFER PROBE TESTING

The method used to assess ADC functionality was the triangle test. The ADC was driven by a triangle waveform. ADC output was then viewed on a oscilloscope after being reconstructed via a DAC. This test uncovered a resistor that had an incorrect value in a dc bias circuit. The effect of this error was easily corrected by using an external power supply. Using the triangle test, the processed wafers were probed for functionality. The yield is shown in Figure 4-1.

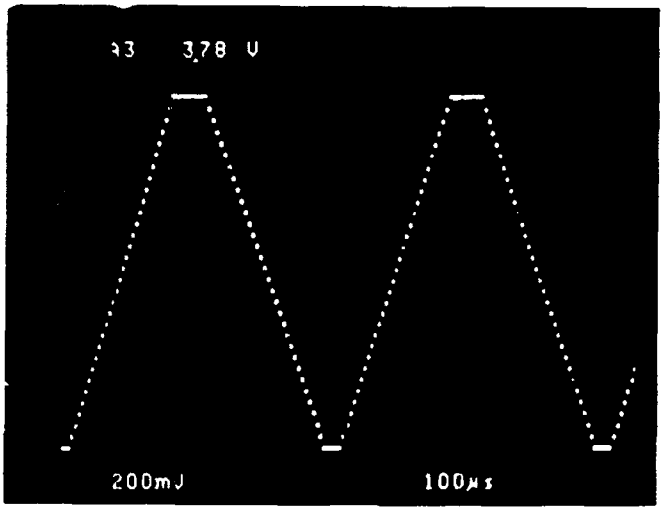
Wafer No.	Functional Yield (%)
175-047	9/167 = 5.4
175-063	28/167 = 16.8
175-084	26/167 = 15.6
175-085	57/167 = 34.1
Average	30/167 = 18.0

Figure 4-1. ADC Yield for MBE Wafers in Lot 1

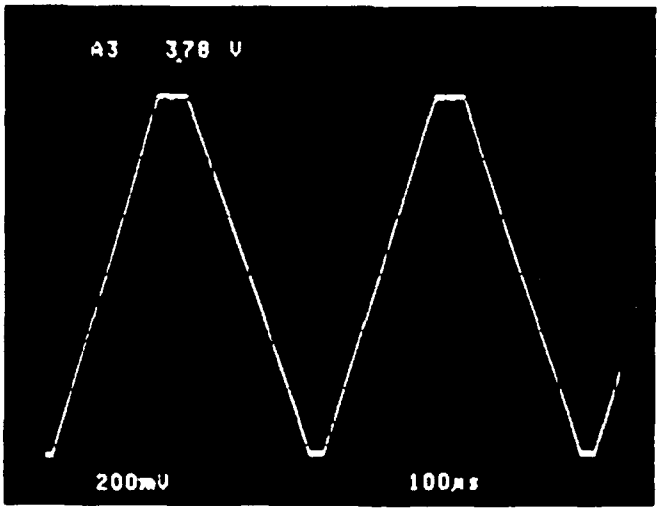
The results of the triangle test were very encouraging. All 12 bits were verified to be functional and untrimmed linearity appeared to be very reasonable. Figure 4-2 shows oscilloscope photos of the triangle output as bits of the DAC are progressively turned on beginning with the 4 msbs. In these photos, no visible difference is discernible in the output after the eighth bit is turned on. Figure 4-3 shows expanded views of the triangle output with 8 and 12 bits of the DAC turned on. In this figure the difference between the ADC output with 8 and 12 bits turned on is more readily apparent.



4 Bits

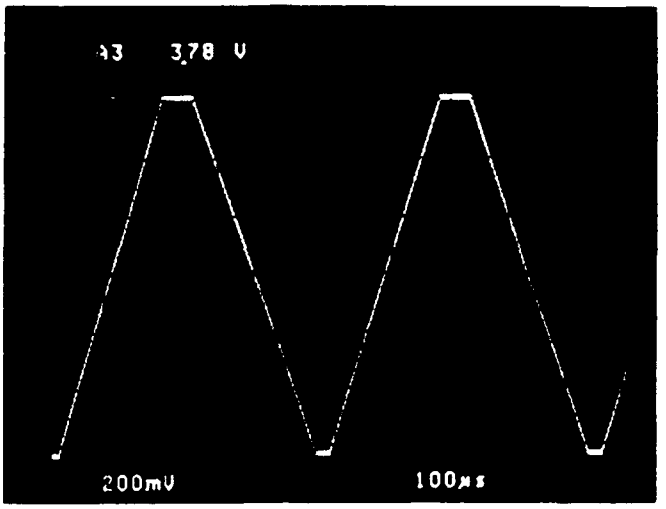


5 Bits

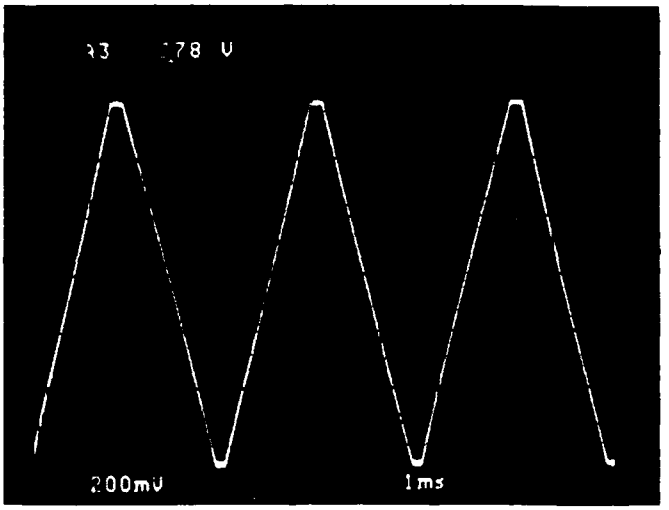


6 Bits

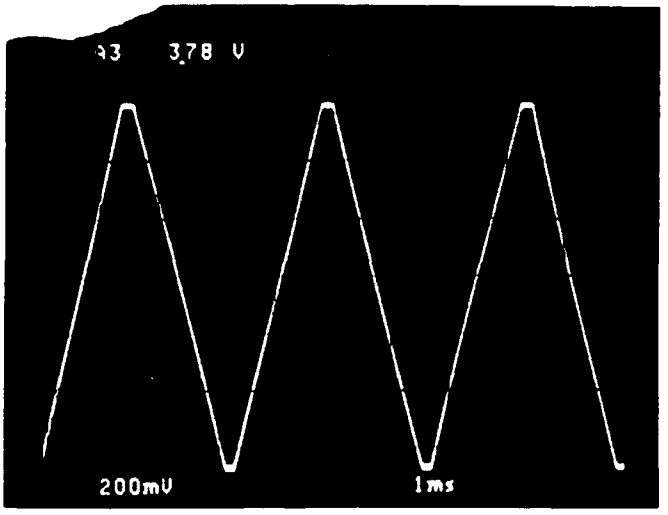
Figure 4-2 D/A Conversion of ADC Output for 4-12 Msbs
(f_B = 100 MHz, f_W = 1 MHz)



7 Bits

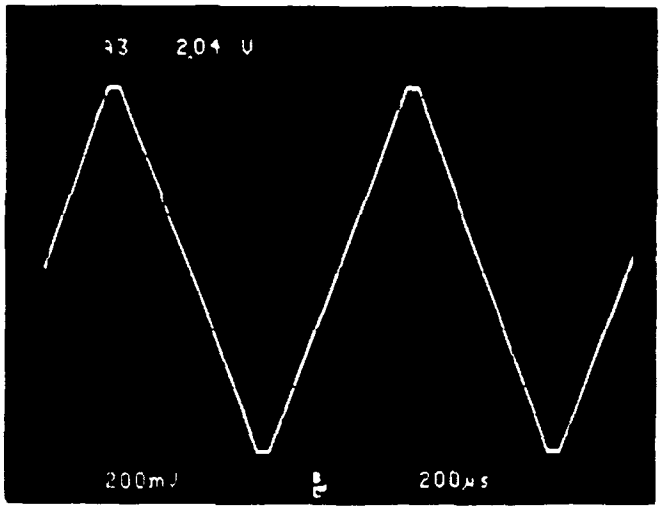


8 Bits

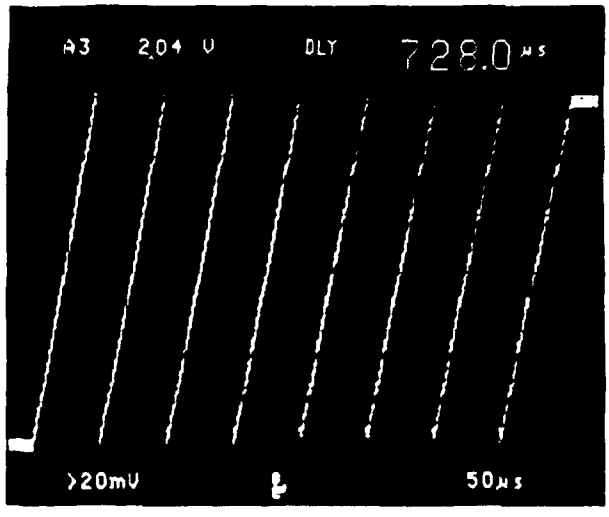


All 12 Bits

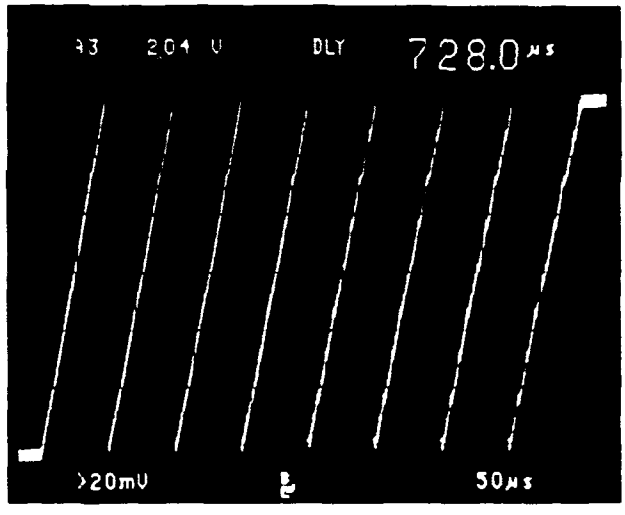
Figure 4-2. D/A Conversion of ADC Output for 4-12 Msbs (f_B = 100 MHz, f_W = 1 MHz) (Continued)



Full Scale Reconstructed 12-Bit Output



Expanded View
8-Bit Resolution



Expanded View
12-Bit Resolution

Figure 4-3. Wafer Probe Data: Functional Triangle Test

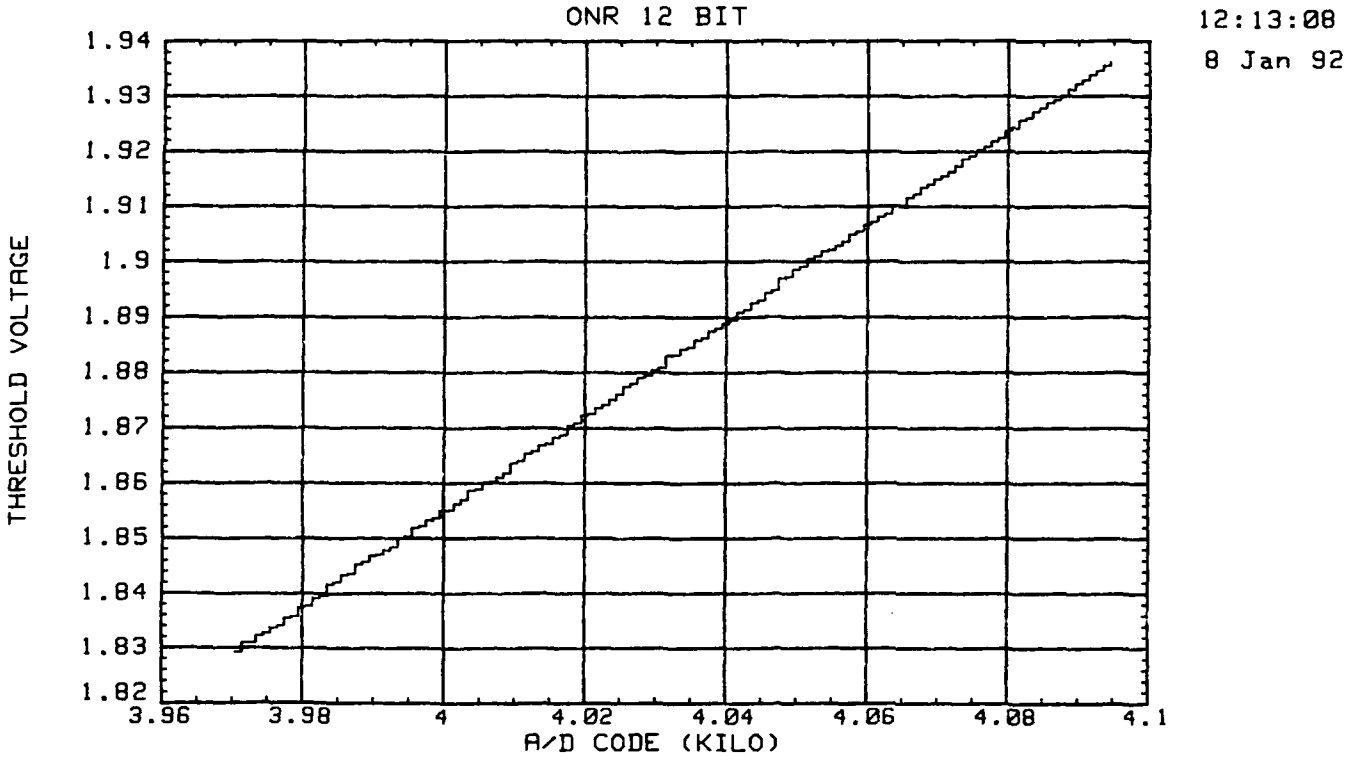
The lsbs were examined at wafer probe using a TRW-developed threshold level error tester. The level error tester finds ADC thresholds by teasing each threshold and recording the analog input voltage that causes equal occurrences of the ADC output digital code above and below the threshold. The transfer function determined by the level error tester for the 7 lsbs of an untrimmed ADC is shown in Figure 4-4. This transfer function has no missing codes. The level errors associated with this transfer function are shown in Figure 4-5. The level errors plotted are the deviation of each threshold from a best-fit straight line of the transfer function. Several of the thresholds (untrimmed) are greater than 1 lsb from the best fit straight line.

Another test performed at wafer probe was a beat frequency test. Reconstructed DAC outputs of the ADC response for sinusoidal inputs from 10 KHz to 15 MHz in 2.5 MHz steps are shown in Figures 4-6. These photos demonstrate that the ADC has a flat frequency response up to at least 15 MHz inputs.

4.2 PACKAGED PARTS TESTING

After wafer probe testing several chips were mounted in a commercial 84-pin package (Figure 4-7) for packaged part testing. Packaged part testing is preferable to testing at wafer probe because of the lower parasitics associated with packaged parts. Before the packaged part testing, laser trim and electrical trim capabilities for the ADC were established. The ADC can be electrically trimmed by adjusting power supplies connected to trim points in the ADC. However, to limit the pads dedicated to electrical trimming, only the 5 msbs of the ADC were made electrically trimmable. With laser trimming all bits of the ADC can be trimmed.

The advantage of trimming the ADC DAC can be seen by a comparison of the untrimmed transfer function of the 7 lsbs shown in Figure 4-4 to the trimmed transfer function of the 7 msbs shown in Figure 4-8. The noise problems with the ADC and test setup prevented us from trimming the entire 12-bit range of the ADC. An FFT was run on the 7 msbs of the ADC and the spectrum is shown in Figure 4-9. SNR performance extracted from several such FFTs run with different analog input frequencies is plotted in Figure 4-10. The SNR results reflect good static and dynamic linearity. A similar FFT run on all 12 bits of the ADC is shown in Figure 4-11. The ADC achieved an SNR of 49.7 dB with a low frequency analog input. represents the highest reported SNR for a GaAs ADC.



OFFSET: -1.589 V
SLOPE: 861.0E-6 V/Q

Figure 4-4. Transfer Function of 7 Least Significant Bits (Untrimmed)

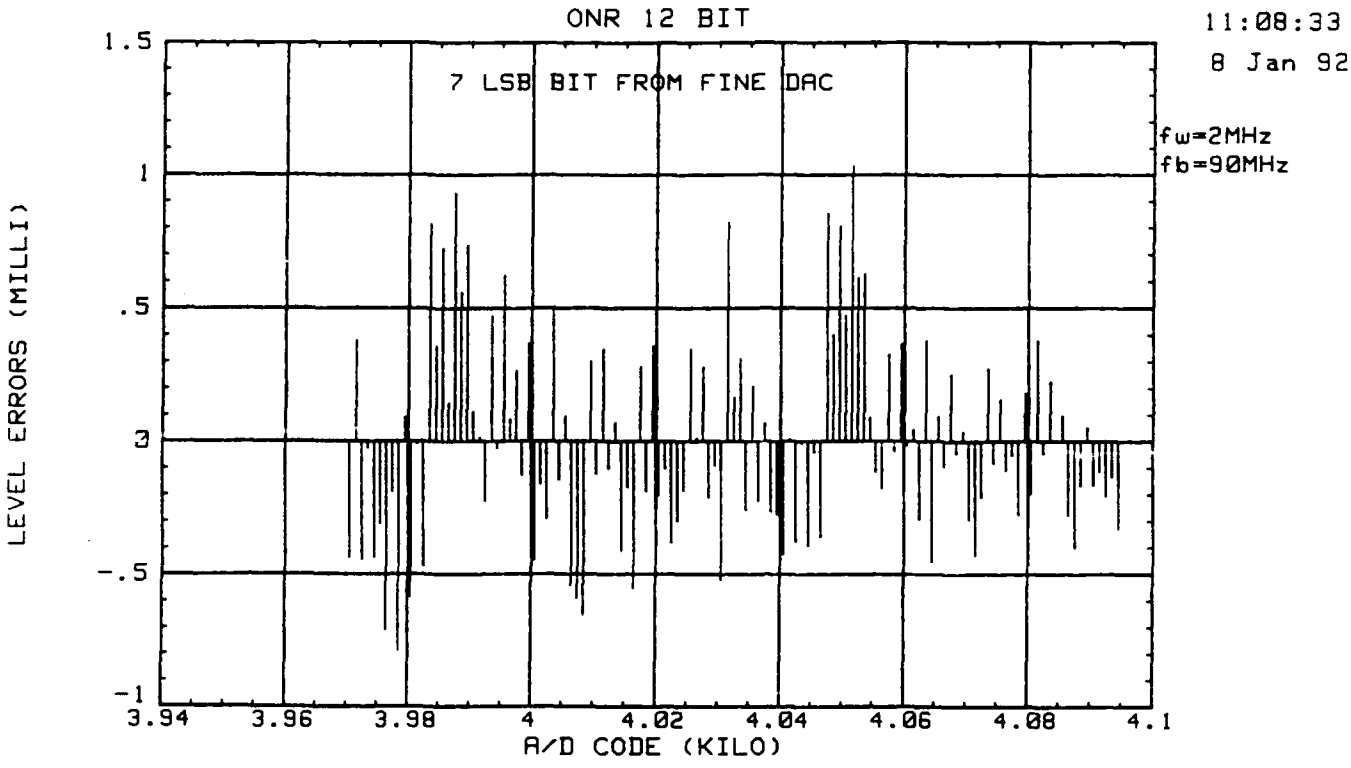
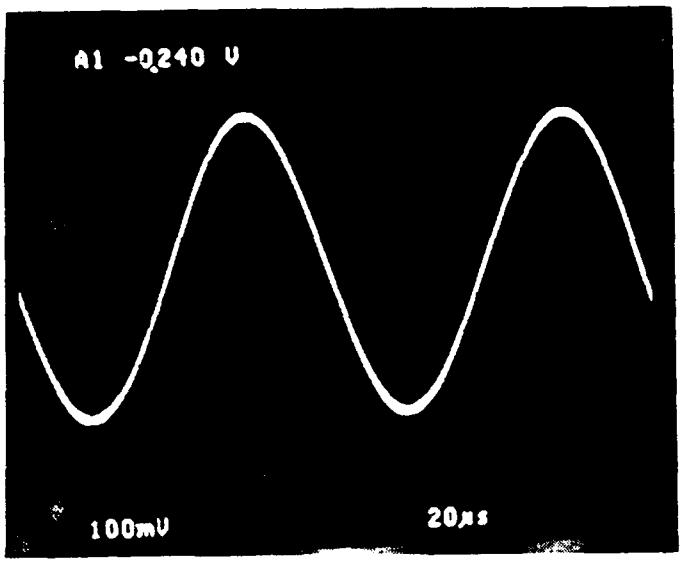
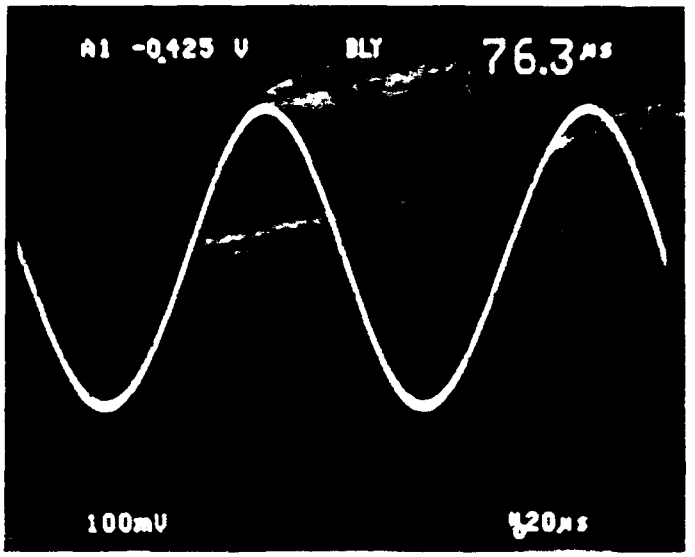
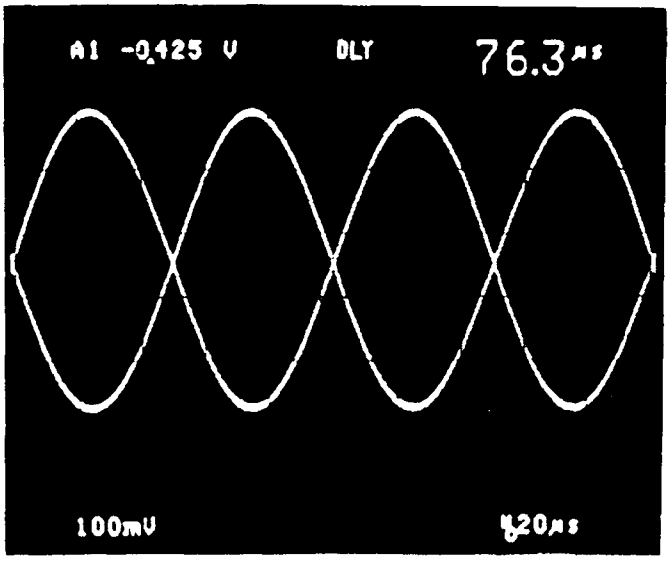
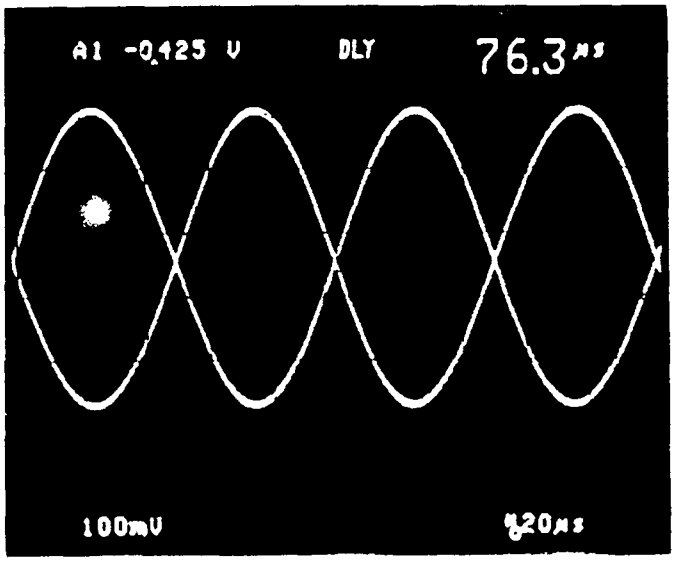


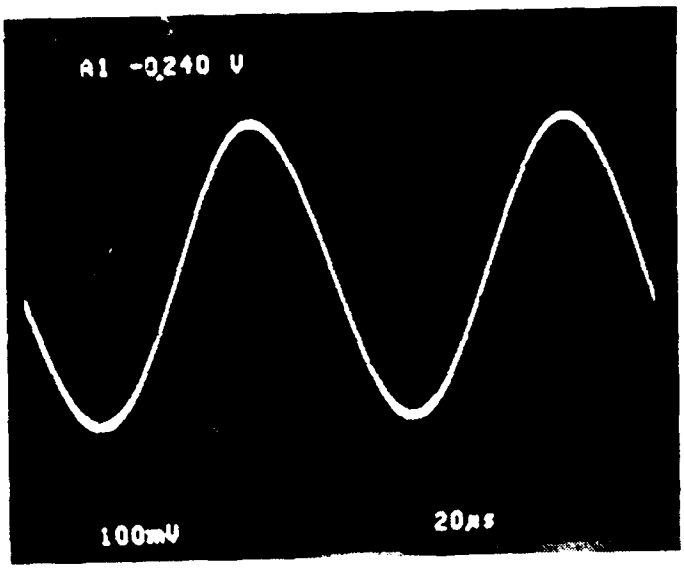
Figure 4-5. Level Errors of 7 Least Significant Bits (mV)
(1 lsb = ~ 0.8 mV)

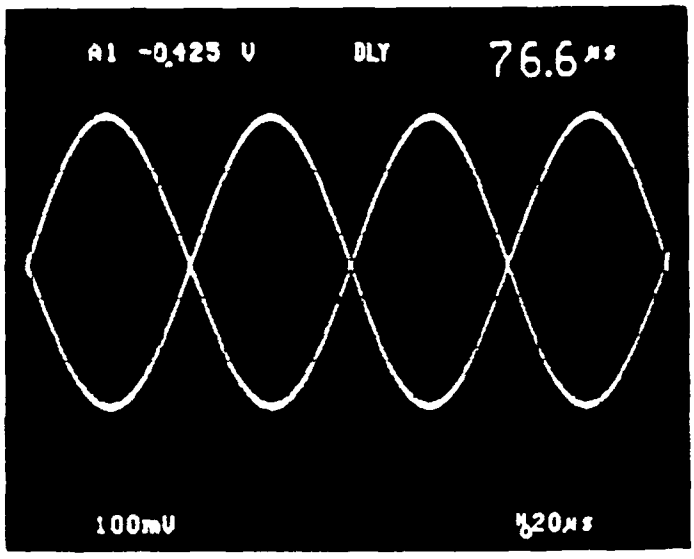

A1 -0.240 V
100mV
20μs

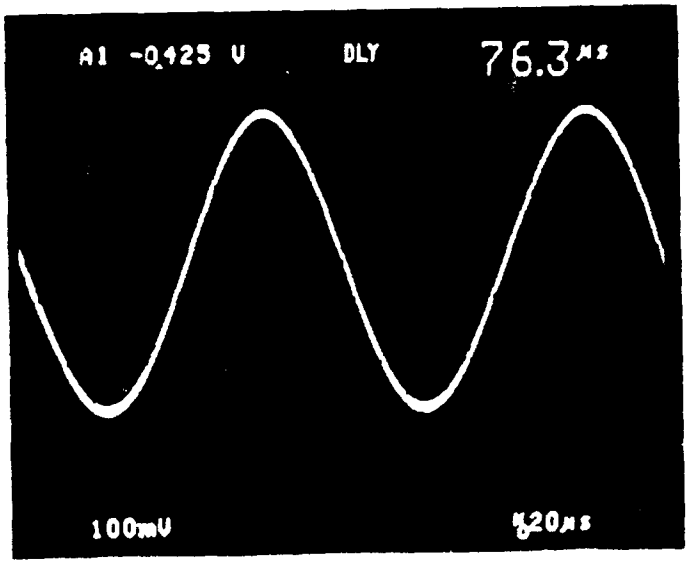

A1 -0.425 V
DLY
76.3μs
100mV
20μs

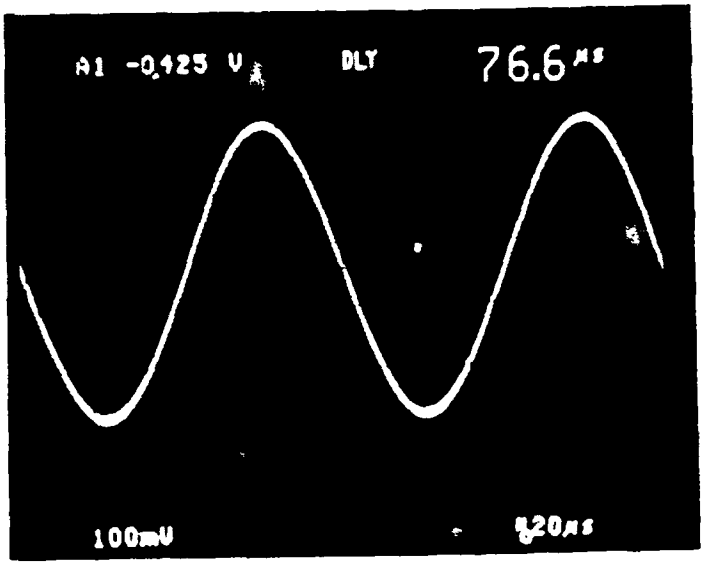

A1 -0.425 V
DLY
76.3μs
100mV
20μs


A1 -0.425 V
DLY
76.3μs
100mV
20μs


A1 -0.240 V
100mV
20μs


A1 -0.425 V
DLY
76.6μs
100mV
20μs


A1 -0.425 V
DLY
76.3μs
100mV
20μs


A1 -0.425 V
DLY
76.6μs
100mV
20μs

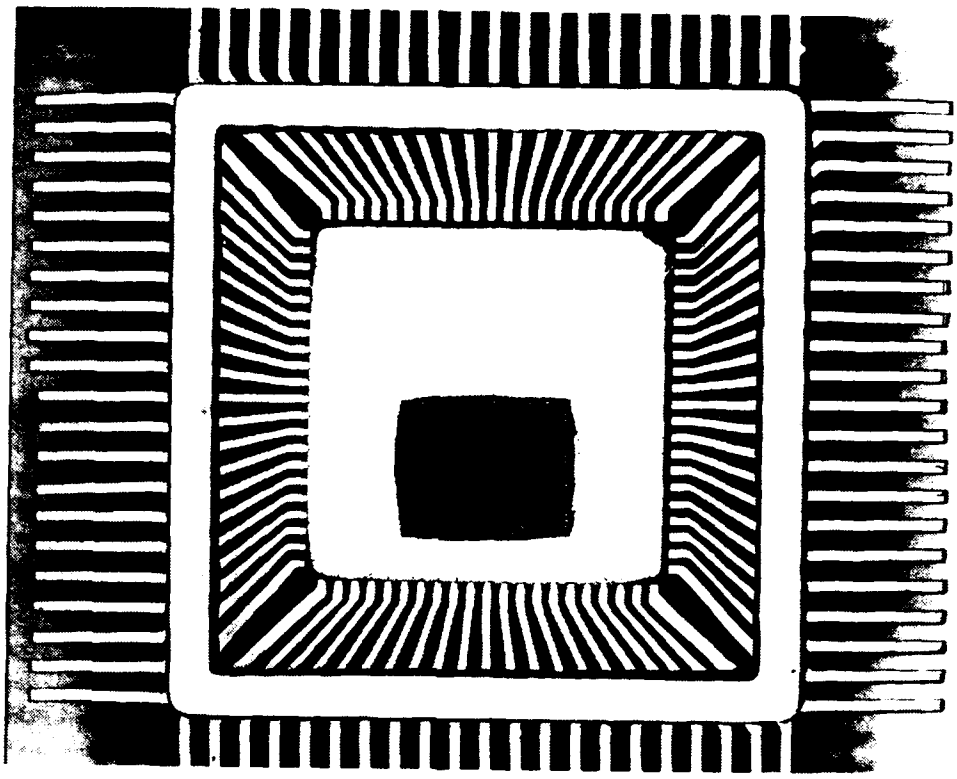


Figure 4-7. ADC in Test Package

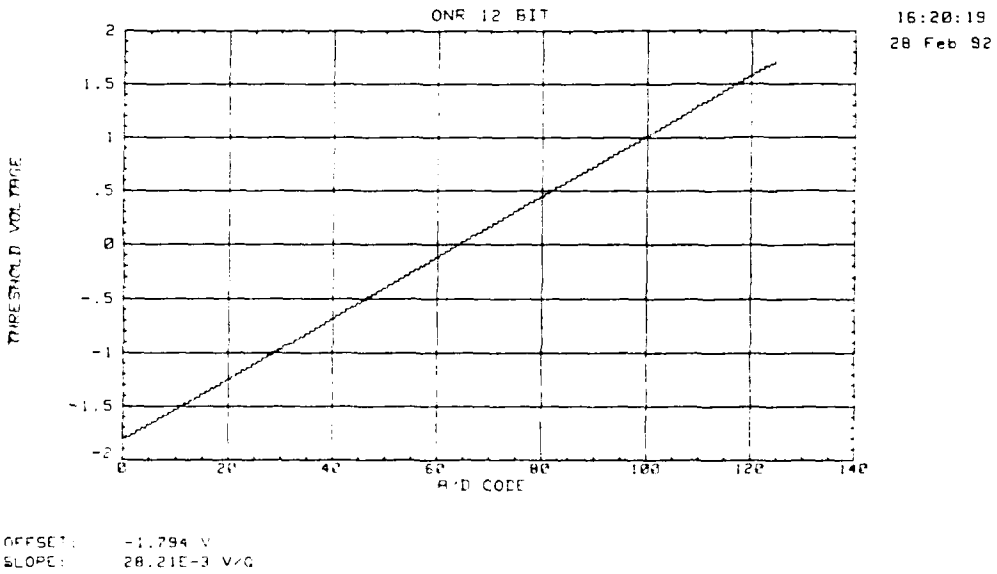


Figure 4-8. ADC Transfer Function - 7 Msbs
(5 Msbs Trimmed)

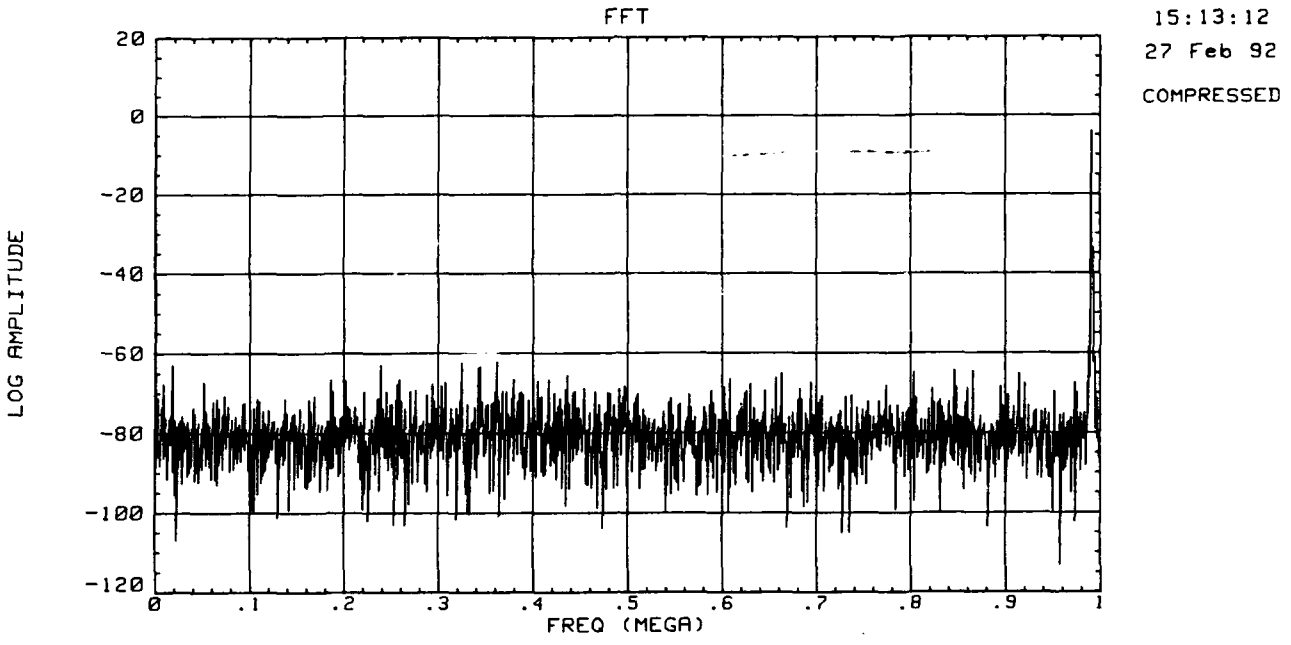


Figure 4-9. FFT Spectrum Run on 7 Msbs
(5 Msbs Trimmed)

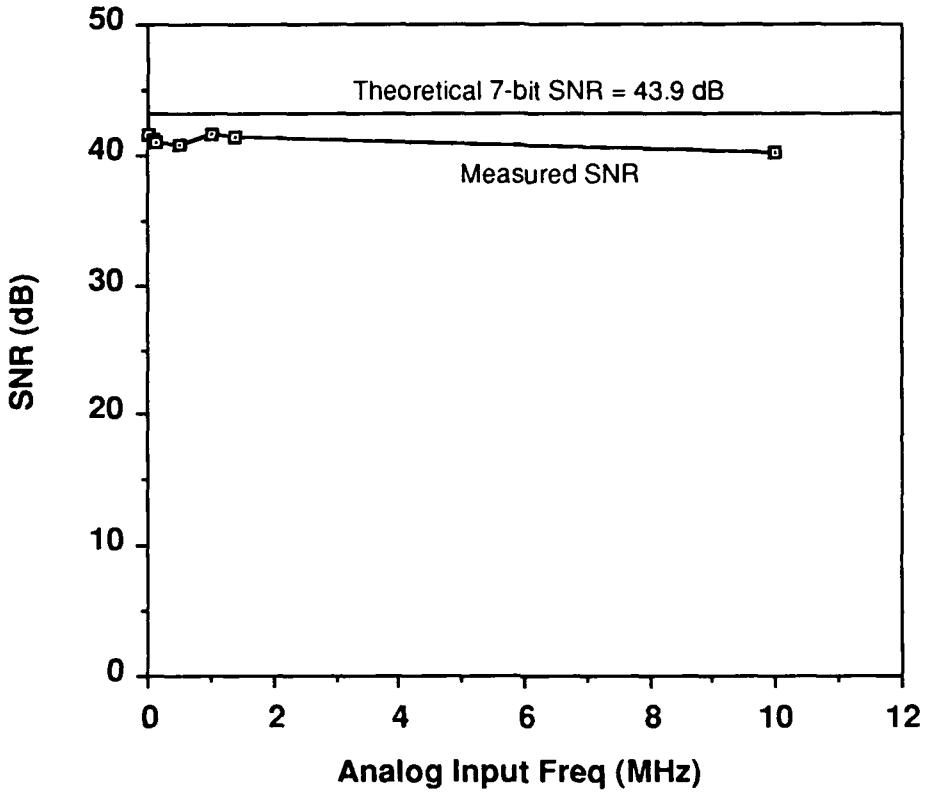


Figure 4-10. SNR vs. Input Frequency for 7 Msbs (Fs=2 Msps)

In summary, the preliminary test results indicate the following:

- 12-bit functionality of the ADC was verified. Average functional yield on four wafers was 18 percent
- The ADC has a flat frequency response up to at least 15 MHz inputs
- Near ideal SNR was achieved for the coarse section of the ADC (the 7 msbs)
- The fine section of the ADC exhibited no missing codes and good untrimmed linearity in level error tests.

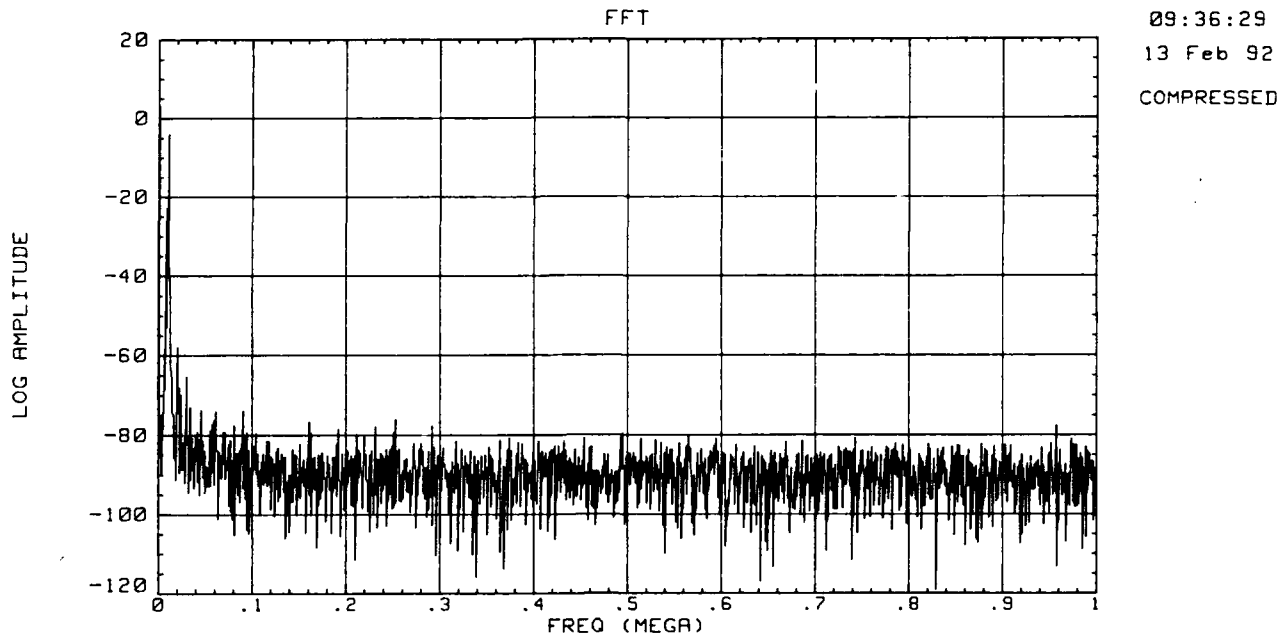


Figure 4-11. FFT Spectrum Run on All 12 Bits of ADC (5 Msbs Trimmed)

5. SUMMARY AND CONCLUSIONS

The ADC design is straight forward and was pulled heavily from eight previous TRW silicon bipolar, single chip, monolithic, successive approximation ADC designs. NevertheLess, the ADC incorporates several unique features including:

- 1-bit digital error (overrange) correction
- On-chip S/H
- Provision for electrical trim
- Use of 2 comparators, power gating, and error correction to eliminate thermal signal dependent modulation of the ADC thresholds

To maximize program success, TRW chose to delay processing on the program to solved the industry wide beryllium migration problem and significantly improve our HBT ADC technology which is reflected in terms of improved device parameter stability, reproducibility, yield, and reliability. During this period a 3-inch class 10 GaAs pilot line was established and the process matured significantly – to the point that when the ADCs were processed, good ADC wafer probe yield was achieved on the first lot run. This capability has now been demonstrated on several GaAs HBT ADC projects.

Although less than 60 percent of the negotiated contract value was funded, we were able to complete the ADC design, layout, fabrication, and wafer probing of one lot. Fully functional ADCs were found at wafer probe and the ADC chips were packaged for trim and test. Electrical trimming of the ADC was completed for the first 5 msbs, at which time work was halted for lack of funds.

ADC test results showed excellent linearity on the 7 msbs (trimmed) and good linearity on the untrimmed 6 lsbs. The tasks yet to be done are:

1) Process additional wafer lots
2) Solve the test fixture/ADC noise problem
3) Complete the electrical/ laser trimming
4) Explore the ADC speed capability
5) Revise the design if necessary to meet requirements. The estimated cost to finish the development is less than the remaining ~40 percent of contract value not funded.

Although only preliminary testing of ADC wafers and packaged parts was performed, the results offer encouraging indications of the potential for TRW's GaAs HBT technology to implement high resolution, low power ADCs. This ADC represents a significant advance in GaAs ADC performance and has already demonstrated the highest reported SNR for a GaAs ADC.