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Multichip Module Study

V.J. Sferrino

20 March 1992

Lincoln Laboratory
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON, MASSACHUSETTS

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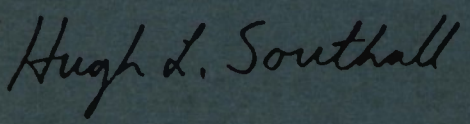
This technical report has been reviewed and is approved for publication.

FOR THE COMMANDER



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MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LINCOLN LABORATORY

MULTICHIP MODULE STUDY

V.J. SFERRINO
Group 27

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ABSTRACT

Multichip module (MCM) technology addresses the large gap that exists between the speed and circuit densities achieved in monolithic integrated circuits versus those achieved at the board and subsystem level using conventional through-hole and surface mount package technology. Multichip modules promise not only to improve board-level circuit densities but also to support dramatic increases in clock rate and reductions in overall power dissipation. This new technology is driven by the realization that current printed circuit board technologies are inadequate to achieve the speed and system throughput capabilities inherent in the chips that are now becoming available.

Multichip module technology centers on the high-density interconnection of bare die on a suitable substrate, resulting in a module with up to 95% of the substrate area devoted to active circuits. The technology features substrates that are generally made of silicon or ceramic with insulating layers of polyimide. Various other materials are employed by a host of vendors, and the technology, which is available now, is continuing to mature at a rapid rate. MCM technology is supplanting printed circuit board technology for most high-performance applications and will provide a vehicle for leading-edge digital systems in the 1990s.

The advantages of MCM technology over conventional packaging schemes include very high packaging densities, clock speeds in excess of 500 MHz, lower power due to reduced capacitances, higher reliability, and better thermal matching of the die to the substrate material. The current disadvantages include the high cost of substrates, limited availability of bare die, and difficulties in testing at speed. These disadvantages are being addressed and are expected to improve. This report includes a discussion of the state of the art of MCM technology, MCM vendors, and emerging CAD tools for the design and manufacturing of MCMs.

ACKNOWLEDGMENTS

The author would like to acknowledge the contributions made by Gary Shaw of Group 27 and Fred Vote of Group 28 in the form of many helpful discussions and contributions of reference material for this study. Further thanks are due to John Milne of Group 72 who accompanied me on the trip to the West Coast to visit a number of MCM vendors and shared his analysis of each visit with me.

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1. INTRODUCTION

1.1 GOALS OF STUDY

This report focuses on some of the important aspects of multichip module (MCM) technology. The advent of MCM technology is driven by the realization that current printed circuit board (PCB) technology is no longer adequate to accommodate the speeds that the chips used in the modules are capable of achieving. MCM technology is gaining wide acceptance in the electronics industry and will play a vital role in next-generation military and commercial systems.

The major goals of the study are listed below.

1. Identify Lincoln Laboratory programs with the potential for MCM insertion.
2. Identify and evaluate current vendor capability.
3. Evaluate process and packaging technologies.
4. Evaluate available and emerging CAD design tools.
5. Evaluate test technology.
6. Explore working arrangements with vendors.
7. Determine cost bases for MCM designs.

1.2 WHAT IS A MULTICHIP MODULE?

Multichip modules are devices that consist of a collection of integrated circuit (IC) chips or die that are mounted on a high-density interconnect substrate that is fabricated using a process resembling the process employed for ICs. Figure 1 shows a generalized sketch of a multichip module.

This structure leads to a very efficient packing of the die on the substrate with a high utilization ratio of die area to substrate area. Utilization ratios in the range of 50 to 80% are common, while size-driven designs can result in ratios of 90 to 95%. This new technology breaches the widening gap between the increasing complexity and speed of monolithic integrated circuit devices and the ability to package them in a system environment that preserves the inherent speed and throughput of the devices. The current methods of packaging devices center around PCB technology, which is incapable of providing the speed and packaging density required for many current system applications.

1.3 HISTORICAL PERSPECTIVE

At first glance, MCM technology appears to be merely an extension of the hybrid technologies that have existed for more than 30 years. Although this is partially true, MCM technology requires a significantly higher level of integrated design disciplines and often employs significantly different interconnect materials. Inherent in the design requirements, to an extent never before required in

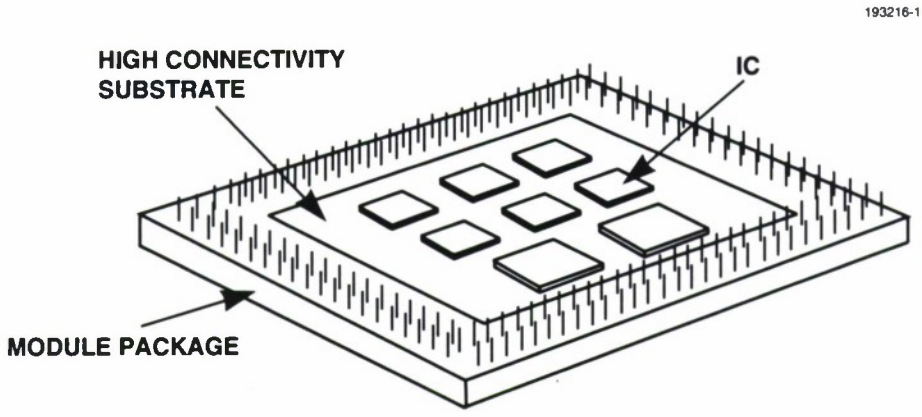

Figure 1. What is a multichip module?

a single package design, are elements of thermal management, high speed, low noise, reliability, testability, small size, and cost considerations.

Most of the early efforts to create high-density interconnect mediums were made by mainframe manufacturers. In 1980, IBM used a multilayered cofired alumina ceramic substrate for their thermal conduction module (TCM) [19]. In 1984 NEC and Mitsubishi used a similar technology to create modules for their mainframe computers. These efforts established the notion of achieving improved performance through the use of increased density and decreased size of architectural components. However, one of the disadvantages of the ceramic multilayer technology was that the dielectric constant of the alumina was too high, resulting in lower speed performance. Thus, the new thrust of MCM technology was to utilize a suitable material with a lower dielectric constant. This thrust gave rise to the use of silicon on silicon with a silicon dioxide insulating layer and aluminum metalization. The use of this method marked the transition to substrate processing similar to IC technology. This approach was explored by Hitachi, Honeywell, Mosaic, nCHIP, and IBM. Although this system provided a lower dielectric constant, it had some deficiencies. The higher resistance of aluminum metalization was found to limit high-speed performance, and multiple layers of silicon dioxide were found to be difficult to process. These realizations led to the use of organic polymer dielectric layers. These materials permit the use of copper instead of aluminum conductors. The copper-polyimide system leads to better speed performance. Furthermore, the use of copper facilitates solder-bonded tape automated bonding (TAB) connections for easier repair and rework of modules. In view of the expense involved in discarding an assembled MCM, this feature was afforded a high priority.

Although these process changes were evolutionary in nature, a variety of material systems are currently utilized by various vendors to address specific customer requirements for MCMs. Thus, the choice of an MCM technology requires a careful match of the interconnect and substrate medium to user requirements such as cost, speed, ease of repair, reliability, turnaround time, and so on.

2. MCM TECHNOLOGIES

2.1 TECHNOLOGY OVERVIEW

A substantial number of different approaches to MCM design are in evidence among the various vendors in the field. Each of these approaches was chosen for the particular advantages relevant to the goals and capabilities of the various vendors or for the diverse user requirements. Each vendor has settled on one or two methods of MCM design that make use of prior expertise with some of the materials involved in the MCM process. Tables 1 and 2 provide an overview of the principal features of the technologies employed by various merchant and captive MCM vendors. These tables support the notion of a wide variety of process choices among the various vendors. This lack of standardization complicates vendor selection and serves to underscore the need for an understanding of all aspects of the MCM process in order to make intelligent choices tailored to specific system requirements.

TABLE 1

Merchant Thin Film MCM Technologies

Company	Substrate	Conductor	Dielectric	Track Widths	Layers	Contact
APS	Si/Al_2O_3	Al	Pi	25/30/35 μm	7	WB/TAB
Alcoa	Al_2O_3	Cu	Pi	20/25/20 μm	9	WB/TAB
Hughes	Si/Al_2O_3	Al	Pi	20/40/35 μm	5	WB/TAB
nCHIP	Si	Al/Cu	SiO_2	25 μm	5	WB
Polycon	Si/AlNi	Al	Pi/BCB	20/50/35 μm	5	WB
Polylithics	Glass/qtz	Cu	Pi	15/35/5 μm	7	Solder Bump
Rogers	Moly	Cu	Flpoly	50/15/75 μm	-	TAB
Tektronix	Al_2O_3	Au	Pi	10/10/10 μm	8	TAB
Uni Structure	Mo/AlNi	Cr/Cu	Pi/epoxy	50/50/50 μm	6	Bump TAB
MCC	Al_2O_3	Cr/Cu/Cr	Pi	15/35 μm	5	TAB
MCNC	Al_2O_3/AlNi	Cu/Al	Pi/BCB	8/24/8 μm	-	Dry Etch
GE/TI	Al_2O_3	Ti/Cu/Ti	Pi	35/65/35 μm	5	Sputtered

TABLE 2

Captive Thin Film MCM Technologies

Company	Substrate	Conductor	Dielectric	Track Widths	Layers	Contact
AT&T	Si	Ti/Cu/Ti	Pi/SiO_2	10/10 μm	3x2	Solder Bump
DEC	-	Cu	Pi	18/57 μm	9	TAB
Honeywell	Si/Al–$2O_3$	Ti/Cu/Ti	Pi	25/100/100 μm	5	Bump/TAB
IBM	Si	Al	Pi	15/10/5 μm	4	Solder Bump
Rockwell	Si/AlNi	Al	Pi/BCB	20/60 μm	6	WB/TAB
HP	Si/AlNi	Cr/Cu/Cr	Pi	15/35/6 μm	7	Solder Bump
NEC	Saph	Cr/Cu/Cr	Pi	25/50/30 μm	7	TAB
NTK	Al_2O_3	Cu	Pi	25/40 μm	-	TAB
NTT	Al_2O_3	Cu	Pi	25/25/30 μm	6	Solder Bump
Toshiba	Si	Ti/Cu/Ti	Pi	50/150/50 μm	8	Solder Bump
Hitachi	Si	Al	SiO_2	-	-	Solder Bump
Thompson/CSF	Si	Si	Silica	20/20/8 μm	4	WB/TAB

MCM substrates are typically made of a silicon or ceramic material with an overlay pattern of conductors separated by an insulating material. Figure 2 shows a sectional view of a generic MCM.

This device contains two signal conduction layers and a power and ground plane. A surface layer contains the pad and die attachment areas. A system of "vias" joins selected points on the intervening layers. One of the important goals of MCM technology is to ensure that the substrate has a coefficient of thermal expansion similar to that of the semiconductor. This similarity reduces thermal stresses in the packaged MCM and enhances reliability. The die can be attached to the substrate face up, as in Figure 2, or face down, termed the flip-chip implementation. In the face-up mode some mechanism must be provided to transfer the heat generated at the junctions of the devices to some heat sink. In the case shown, "thermal vias" are provided through the use of low thermal resistance fill materials that transfer the heat from layer to layer on the substrate, and finally, to the substrate and package boundaries. The conduction levels are interspersed with an insulating material consisting of high dielectric strength materials with relatively low vapor absorption properties. Polyimide is used in a majority of cases for the insulating layers. Connections from the die I/O pads to the top layer metal pads are made using various techniques such as the tape automated bonding (TAB) depicted in Figure 2, wire bonding, or flip-chip methods.

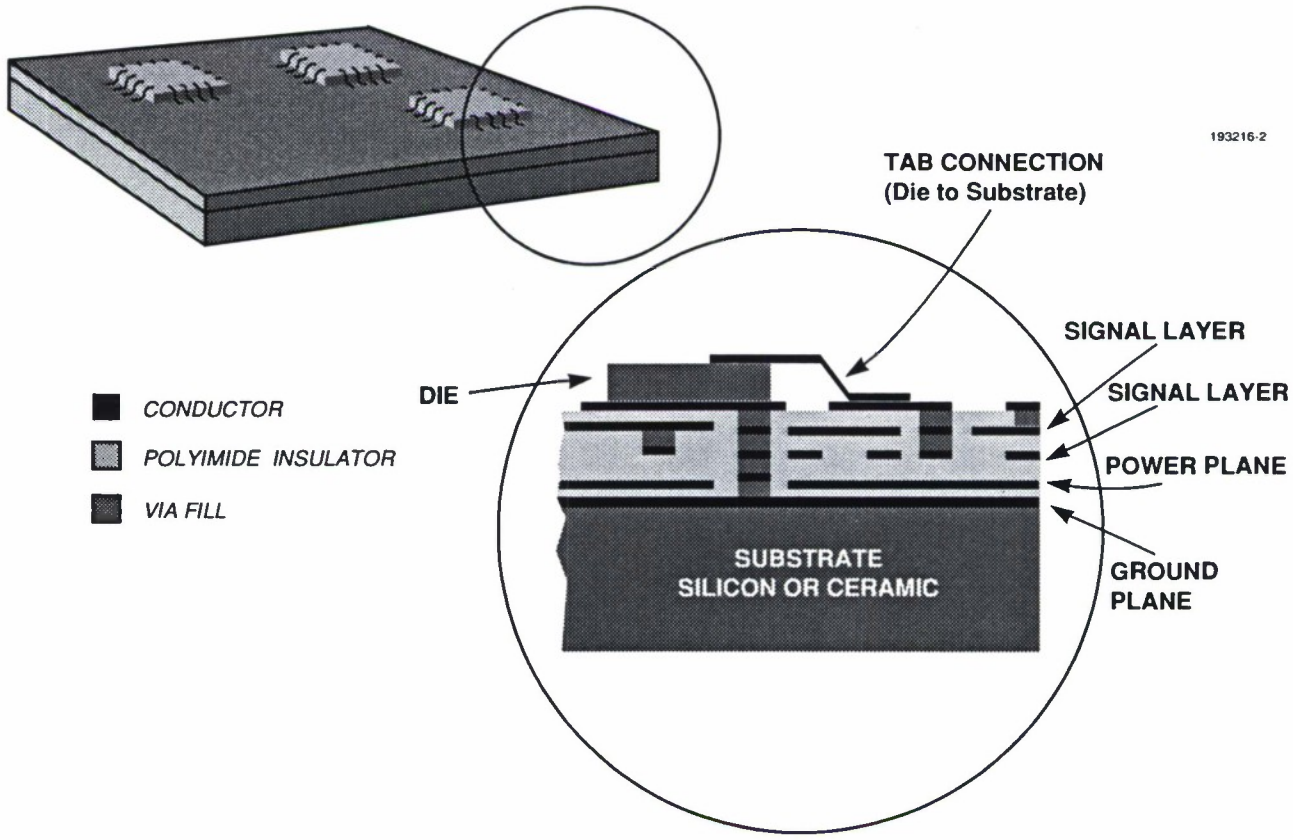

Figure 2. Sectional view of generic MCM.

Average interconnect line widths of MCM devices span the gap from 1 micron for ICs to 1000 microns for thick film hybrids and PCBs. Figure 3 gives a comparison [20] between average wire lengths and line widths for various technologies.

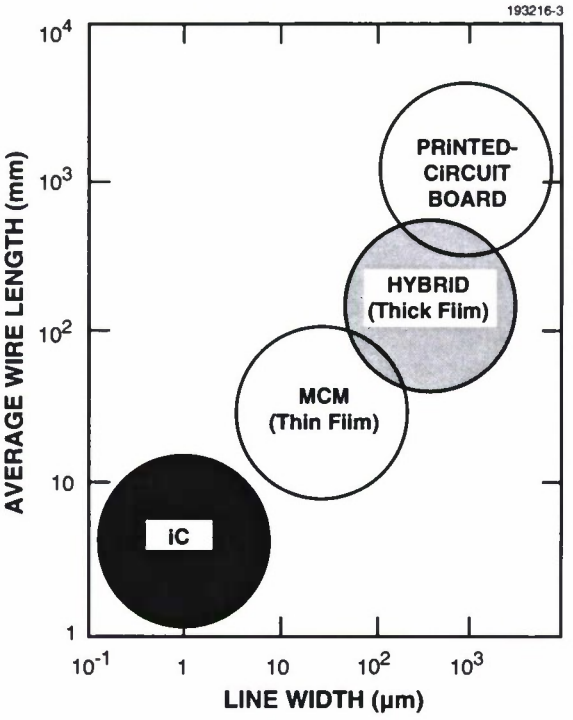

Figure 3. Average wire length vs line width.

Average wire lengths for MCM designs are more than an order of magnitude lower than for similar PCB designs, which accounts in part for the superior speed performance of MCMs. Figure 4 provides a perspective of where MCMs lie in the spectrum of interconnect technologies.

Some overlap exists between MCM and PCB technologies in terms of interconnection density. MCMs generally use smaller track widths than PCBs. Interconnect densities achieved for MCMs are about an order of magnitude higher than for PCBs. Most important, however, is the fact that the number of signal layers required to achieve high interconnect densities is considerably lower for an MCM than for a PCB because of the smaller line and space widths.

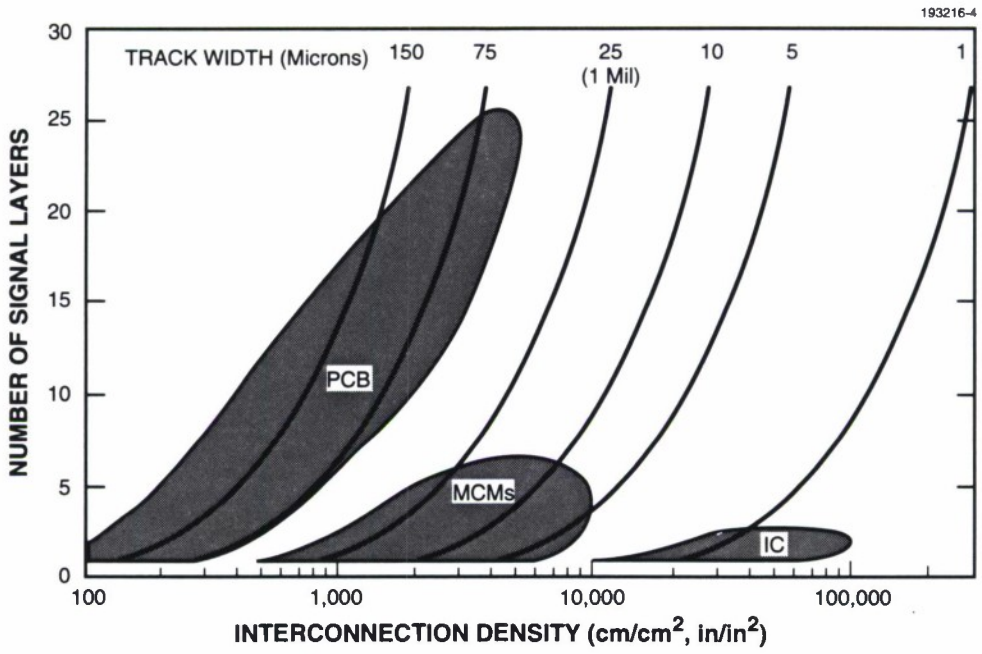

Figure 4. MCM domain in the interconnect spectrum.

2.2 MCM SUBSTRATES

MCM substrates are made in a variety of materials. Table 3 lists substrates according to several categories that have been developed for the MCM industry.

The categories are an attempt to provide some standard method of delineation between different process technologies. The MCM-D, D/C deposited thin film (DTF) technologies, and the MCM-Si technologies are high-performance processes that support very high system clock speeds (300 to 500 MHz) and pad densities. Substrates are the pacing item in MCM designs, and substrate processing costs account for the major fraction of the cost of a fully packaged MCM (not including the cost of the die).

A summary of the salient features of each MCM category follows. MCM-L represents a laminated PCB high-density technology. This low- cost technology has low line resistance, fair heat transfer through the substrate material, and 100- to 150-μm metal pitches. Pad density is very low for this technology.

MCM-C is a cofired ceramic technology that can be viewed as an extension of single chip ceramic packages and is therefore the most mature substrate technology. Metal pitches are 250 to 450μm. It is characterized by a poor (high) dielectric constant that limits the speed performance

TABLE 3

Substrate Technology Features

MCM Category	MCM-L	MCM-C	MCM-D	MCM-D/C	MCM-Si
Technology	Laminated HD PCB	Cofired Ceramic	Organic DTF on Si/Cer/Met	DTF on Co-fired Ceramic	SiO_2 on Si Substrate
Maturity	Good	Very Good	Limited	Limited	Limited
Cost Range	Medium	Medium	High	High	Medium
Metal Layers	>15	> 50	5	>50	5
Metal Pitch	$100 - 150\mu m$	$250 - 450\mu m$	$25 - 75\mu m$	$50 - 75\mu m$	$25\mu m$
Heat Transfer	Fair	Poor	Good	Poor	Good
Dielectric Constant	3.0-3.5	9.7	<3.0-3.5	<3.0-3.5	3.5
Frequency Range	<70 MHz	<100 MHz	500+ MHz	300+ MHz	400+ MHz
Pads/in	90	250	500	500	500
Suppliers	Rogers Ibiden	Alcoa, NTK Kyocera	APS, Alcoa Polycon, Dow	Kyocera NTK	nCHIP Mosaic

due to high propagation delays. Another limiting factor in the use of this technology is the relatively poor heat transfer characteristics.

MCM-D technology consists of metal conductors (such as copper), separated by an organic deposited thin film (DTF) layer (such as polyimide), which form signal and power planes. This structure is placed over a base material that consists of silicon, ceramic, or metal. This system features a low dielectric constant, high pad density, and good heat transfer characteristics. This high-end technology is relatively costly and has not reached full maturity. MCM-D provides the best speed performance of all categories.

MCM-D/C combines the MCM-C and MCM-D processes through the use of a thin film copper polyimide deposited over a cofired ceramic base material. The characteristics of this technology are very similar to those of MCM-D, except that it has poor heat transfer through the substrate. This alternative technology is used by Kyocera and NTK to provide their users with a higher speed performance option than is provided by their standard MCM-C cofired ceramic product.

MCM-Si technology uses silicon with a deposited metal for the substrate in a manner similar to that employed by IC manufacturers. This technology features high pad density, reasonable speed performance, and good heat transfer characteristics. Silicon dioxide is used for the insulating layer in this technology. Its low thermal conductivity helps to provide good thermal properties for

MCM-Si. nCHIP is one of the major users of this technology. MCM-Si satisfies the low cost, high volume corporate goals of nCHIP.

2.2.1 Chip-Substrate Interconnect Technology

Methods used for connecting die to the substrate range from conventional wire bonding techniques to exotic flip-chip technologies. Figure 5 illustrates the major chip-substrate connection options.

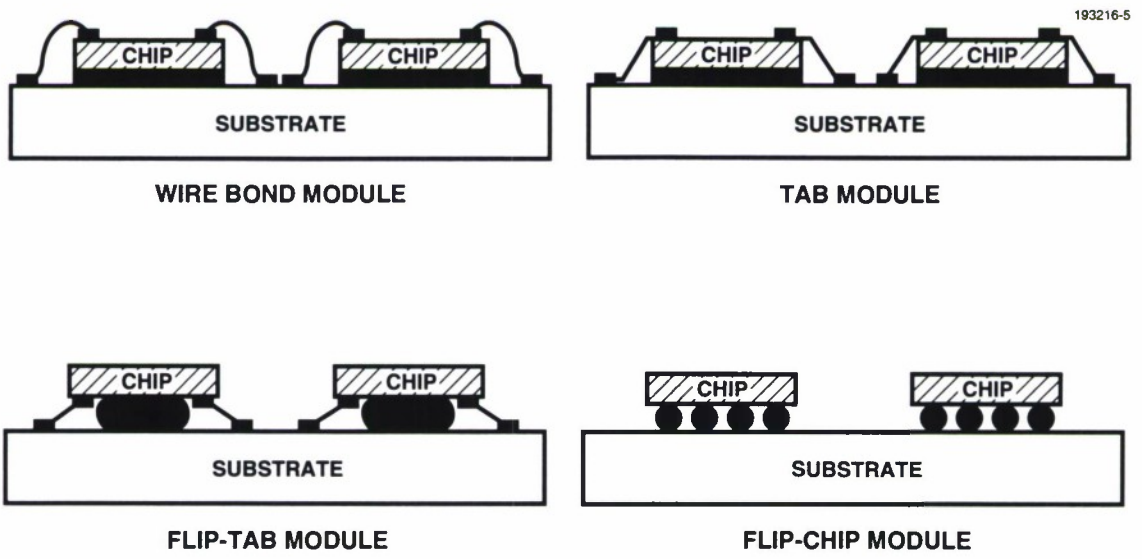

Figure 5. Chip interconnect options.

Wire bonding is used in many cases because of the manufacturer's experience with this connection method and the investment in bonding machines. Because one of the compelling reasons for using MCM is speed, wire bonding poses limitations for high-speed devices due to long wire loop lengths and associated inductance. Flip-chip technology, where the device is flipped over and connected to solder pads or solder bumps on the substrate, provides a higher speed interconnect technology but complicates the testing of attached die. Because testing is a critical requirement for very complex devices, a considerable amount of research effort is being invested in testing strategies for the flip-chip interconnect method. Table 4 summarizes the principal features of the various interconnect methods.

TABLE 4

Chip-Substrate Interconnect Technology Features

Technology Features	Wire Bonding	TAB	Flip-TAB	Flip-Chip
Maturity	Very Good	Good	Limited	Good
Chip Availability	Very Good	Fair	Fair	Poor
Peripheral Bond Pitch	4-7 mils	3-4 mils	3-4 mils	10 mils
Maximum I/O Count	300-500	500-700	500-700	>700
Footprint	20-100 mils	80-600 mils	80-600 mils	Clearance
Repairability	Poor	Fair	Good	Good
Thermal Path	Substrate	Substrate	Module Lid	Lid/Substrate
Chip Burn-in	Poor	Good	Good	Fair

One of the current difficulties in using the TAB or flip-chip connection methods is the limited number of available die compatible with these interconnect methods. This limitation is being addressed by the die vendors. One of the most compelling arguments for the use of TAB bonding methods for MCM is that it facilitates the burn-in and testing at speed of bare die prior to final connection to the substrate. Because testing is such a critical issue with regard to MCM technology, it weighs heavily in favor of this interconnect method for many vendors. The excess interconnect area penalty that is characteristic of the various chip-substrate interconnect methods [24] is depicted in Figure 6.

2.3 MCM PACKAGING

Once the die are attached to the substrate material, some external package and lead frame must be provided to the assembled MCM. Although several MCM manufacturers choose to provide this final packaging as part of their total MCM design, many have chosen to use outside vendors to complete the MCM. The packaging methods range from the conventional to the exotic. Because isolation materials that absorb water are used in some MCMs, hermeticity of packages becomes an issue that is particularly important for space applications. Polyimide insulating layers absorb moisture to a significant degree, which compromises the hermeticity of MCM devices using this material. nCHIP uses silicon dioxide for their insulating layers because of its low moisture absorption properties, which allows hermetically sealed packages to be employed.

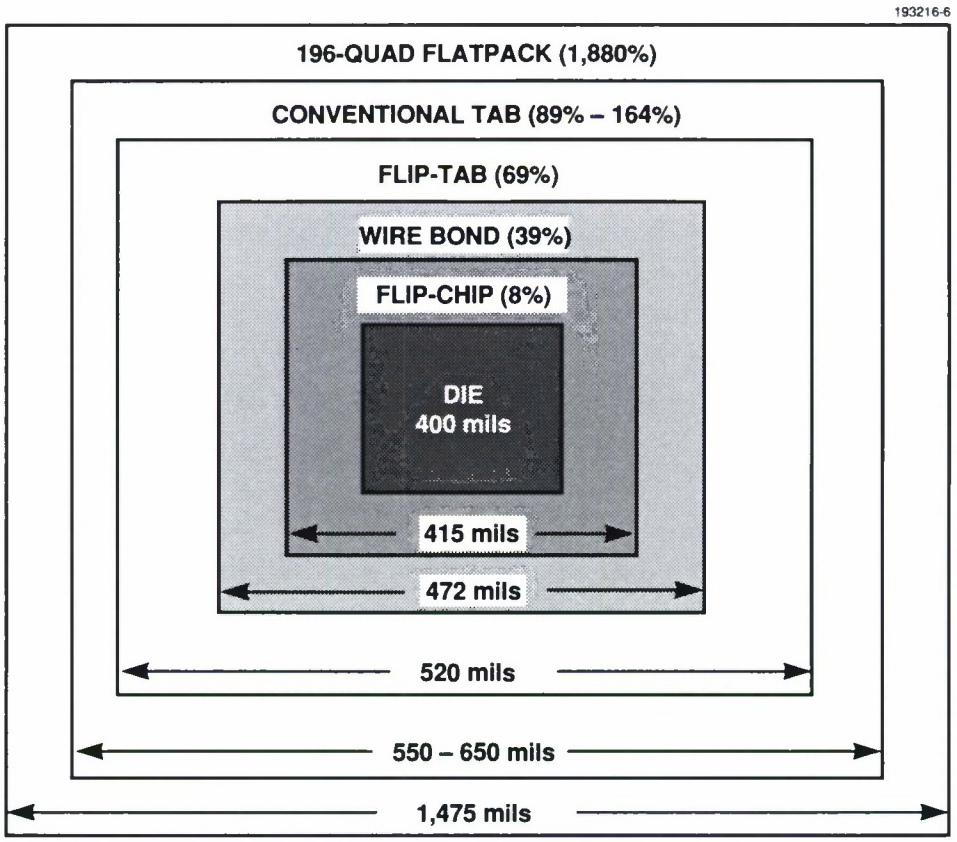

Figure 6. Package penalties: excess interconnect area.

3. MCM VENDOR TRIP

After a preliminary investigation of MCM vendors and researchers, a number of contacts were made in order to establish an agenda for a trip to various MCM vendors that would contribute to our assessment of the state of the art of MCM technology. The participants covered a broad spectrum including manufacturers of substrates, packages, or fully packaged MCMs; a potential MCM broker; and a research-oriented industry consortium leader. A list of the firms visited follows.

1. Alcoa Electronic Packaging – San Diego, CA
2. Hughes Microelectronic Circuits Division – Newport Beach, CA
3. USC Information Sciences Institute (ISI) – Marina Del Rey, CA
4. Interconnect Systems Inc. – Simi Valley, CA
5. Advanced Packaging Systems Inc. (APS) – San Jose, CA
6. nCHIP – San Jose, CA
7. Microelectronics and Computer Technology (MCC) – Austin, TX

The trip provided some of the technical detail included in this report. In addition, vendor-specific cost information and assessment of capability was obtained and is discussed in associated literature. [1]

[1] V.J. Sferrino (private communication, 1991).

4. CRITICAL MCM ISSUES

4.1 RELIABILITY AND YIELD

MCM devices have the potential to be inherently more reliable than the conventional subsystem packaging that generally involves larger numbers of solder joints. Given that the techniques for connecting the die to the MCM substrate are reliable, the overall reliability of the packaged MCM is considerably higher than that of more conventional PCB methods. This fact is a primary consideration in the use of MCMs in systems that require exceptionally high reliability. Because the MCM concept involves the use of a collection of die that might be very expensive, special significance is attached to providing a certain amount of rework capability. This capability varies with vendors but, in general, some provision is made for rework. Three separate rework epochs are often quoted as a reasonable proviso. The need to rework a particular module has some impact upon its final reliability, but none of the MCM vendors have offered to quantify this relationship.

Reliability and yield of the final assembled MCM are highly dependent upon the yield of the die used to assemble the module. It is imperative that the die used in the module be pretested (preferably at speed) and burned in prior to assembly. Figure 7 presents curves [25] of the final MCM test yield as a function of yield of the die used in the module for three different MCM sizes (8, 20, and 36 die).

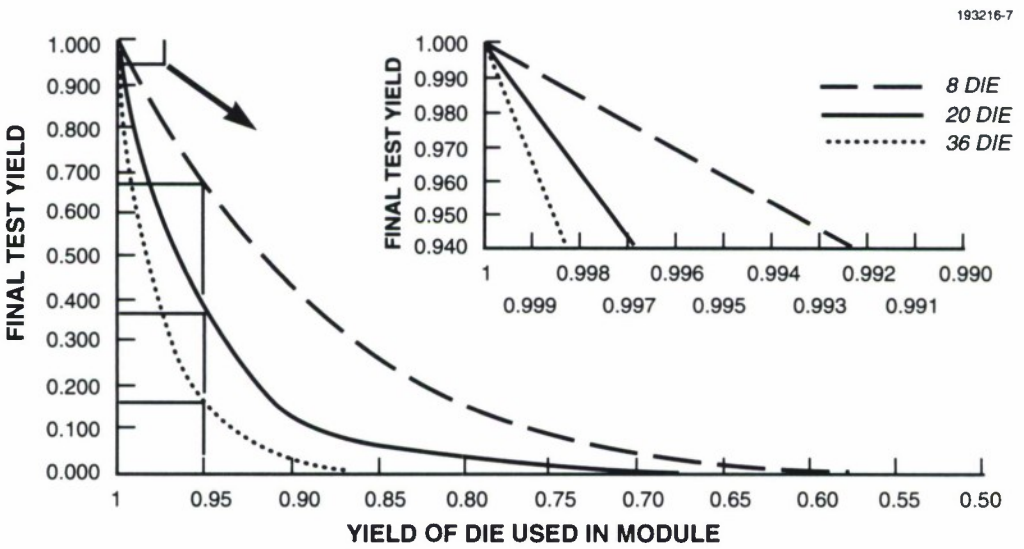

Figure 7. Effect of die yield on final MCM test yield.

These curves accentuate the premium that must be attached to die burn-in and test prior to assembly. For a module containing 36 die, a 95% die yield results in only a 15% final MCM yield. For an MCM with only 8 die, the same die yield will result in a final yield of only 68%. If the die yield is 100%, then the final yield will be determined by other factors such as the interconnect yield.

4.2 RADIATION HARDNESS

The question of radiation hardness for MCM packages is primarily dependent upon the hardness of the die attached to the MCM substrate. Generally, no active components are employed in the MCM design other than the die, although some MCM processes incorporate decoupling and pull-up resistors as an integral part of the substrate. Radiation effects on passive components are generally very minimal. However, the fact that very small geometries prevail on the higher performance substrates, such as deposited thin film copper on silicon, suggests that parameters of passive elements may be affected to some extent. This effect should not have any substantial impact on system performance in the case of passive decoupling elements; however, some effects on signal quality may be noted as a result of radiation-induced changes in termination resistor values. The radiation hardness of the interconnect substrate should generally exceed that of the die attached to it and, therefore, is not an issue in establishing hardness of the assembled MCM.

One of the subtler advantages of the use of MCMs in radiation-hardened systems is derived from increased packaging density. One of the most effective methods of providing radiation hardening to a system is through the use of adequate shielding. In a spacecraft environment the penalty attached to increased shielding is increased weight, which adversely impacts the spacecraft system. By supplanting a large number of individually packaged die with a single package containing a large number of die, the possibility for adding shielding to a functional segment or electronic subsystem is considerably enhanced with a minimal contribution to the total system weight.

4.3 SIZE

Size is an issue in many system applications and is especially critical in satellite environments where added package size adds weight that translates into extra booster requirements. It is also an issue in workstations that must package a large amount of electronic throughput into a small area for convenience and work space efficiency. Laptop computers have similar space conservation requirements, as do a host of other commercial applications such as automobile microprocessors and factory robotics. Several examples of packaged MCM designs follow.

1. Nixdorf Information Systems, Munich, Germany: 4 x 4-in module containing 16 or 25 LSI chip sites. The module features more than 1000 I/O signals and can handle more than 500 W of power using an external liquid cold plate attached to the metal lid of the package. Flip-TAB bonding is used. A schematic of this design [17] is shown in Figure 8.

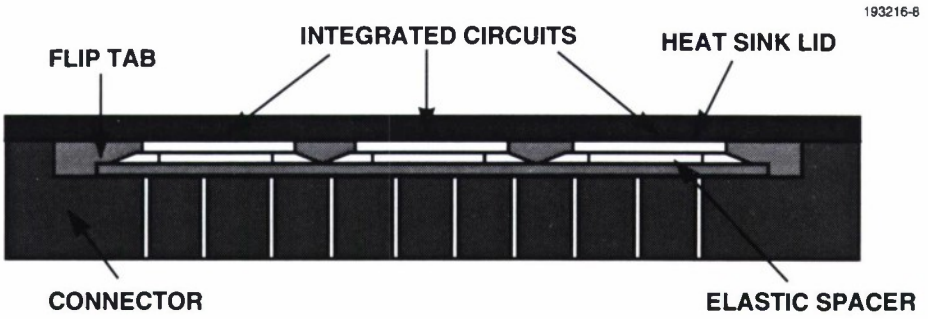

Figure 8. Nixdorf Information Systems MCM.

2. nCHIP, San Jose, California: nCHIP has produced a module comprising a complete SPARC processor. It houses five VLSI components that utilize a 0.8-micron CMOS process. The module was produced by nCHIP for Ross Technologies, a division of Cypress Semiconductor, for use in workstation applications. This module uses a silicon substrate with a silicon dioxide insulating material and aluminum wedge wire bonds. There are two signal layers, a surface pad layer, and power and ground layers. The module is packaged in a 224-pin ceramic quad flat pack. The module consists of five chips that include a central processing unit, floating point unit, memory management unit, and two cache memories and contains approximately three million transistors. The chips sizes are 292 x 330 mils (two chips), 420 x 393 mils, 421 x 445 mils, and 337 x 269 mils. A total of 852 pads are on the five chips. The substrate size is 0.9 x 1.2 in and is housed in a 1.5 x 1.5-in package. This processor was previously implemented on a 3.3 x 7.25-in PCB. Figure 9 is a photograph of the SPARC processor MCM.

   Figure 10 is a blow up of a wire bond interconnect region [12] of the SPARC processor MCM.

   The wire bond pitch is 4 mils, and the interchip spacing is of the order of 72 mils. This module is produced in the nCHIP NC-1000 [24] series of modules. Figure 11 shows a sectioned view of this process with the main features outlined.

   Silicon dioxide is used as an isolation material because of its thermal properties and its low moisture absorption. nCHIP specializes in low cost, high volume business, and this is also a factor in the choice of silicon dioxide because it is cheaper to process. The use of integral decoupling capacitors in the substrate reduces noise coupling and improves signal quality for high-speed operation.

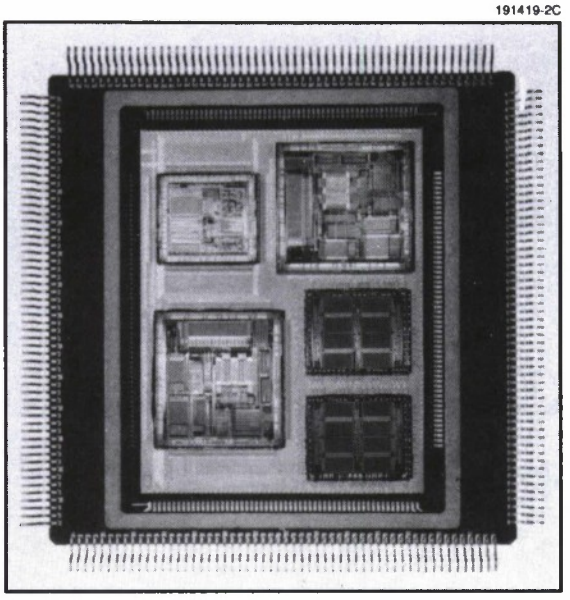

Figure 9. Photograph of nCHIP/Ross SPARC processor MCM.

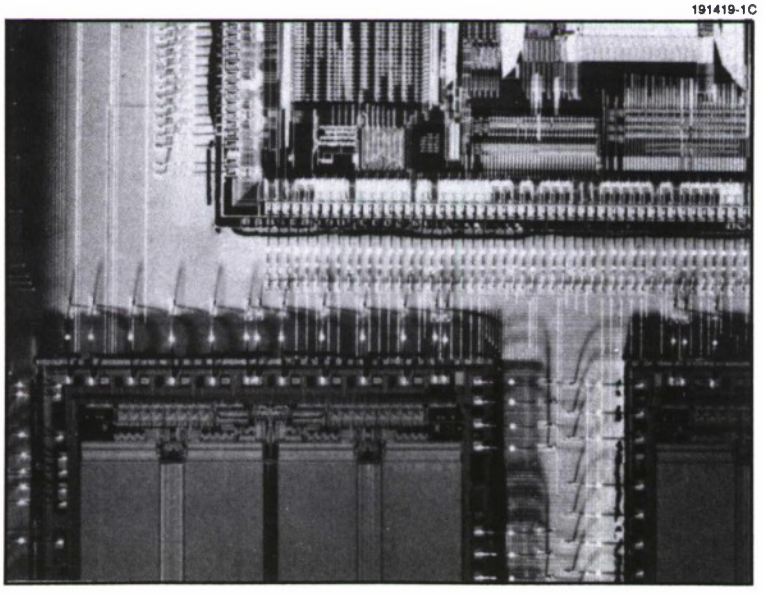

Figure 10. Photograph of wire bond area of nCHIP/Ross MCM.

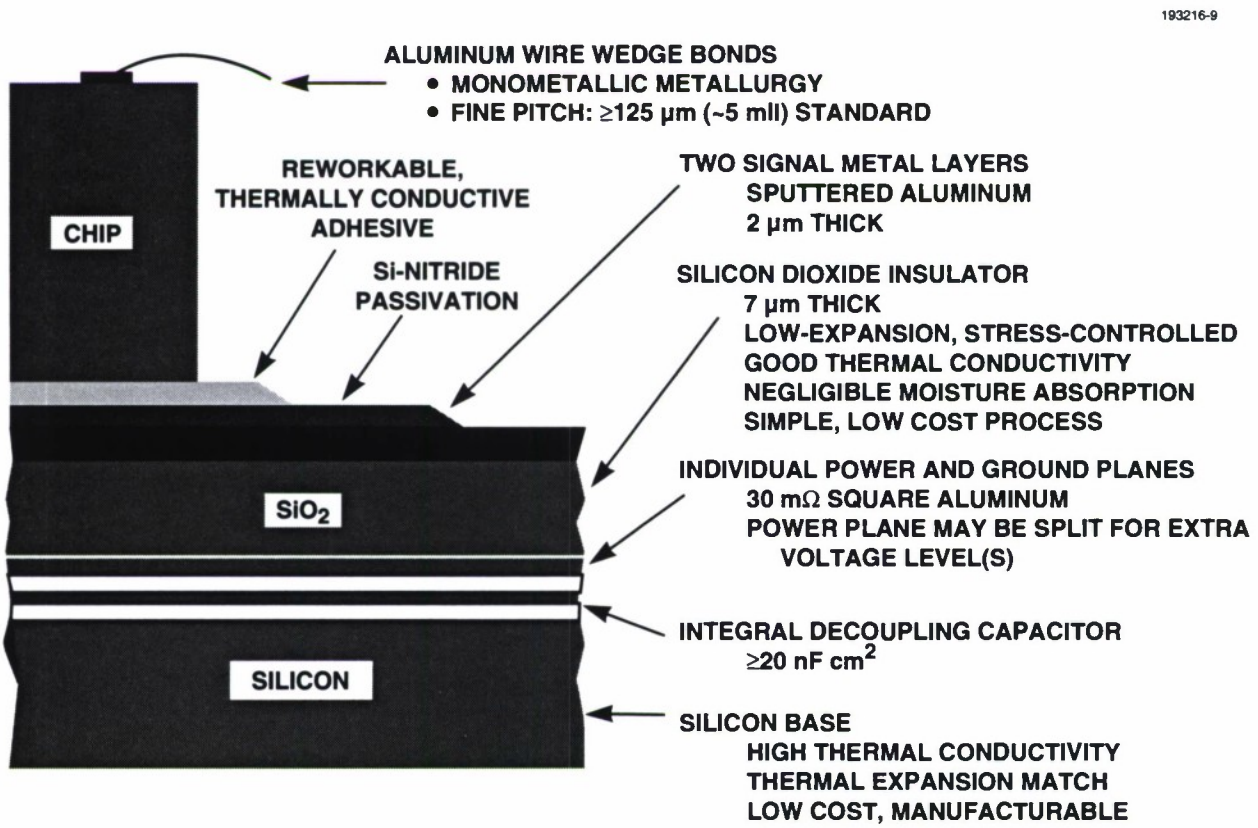

Figure 11. Sectioned view of nCHIP NC-1000 series MCM.

3. Microelectronics and Computer Technology Corporation (MCC), San Jose, California: MCC has developed an MCM for Harris Semiconductor. The substrate is 2 x 2 in and contains 16 large die and 6 smaller die that constitute a cross-bar switch. Figure 12 is a photograph showing the assembled substrate.

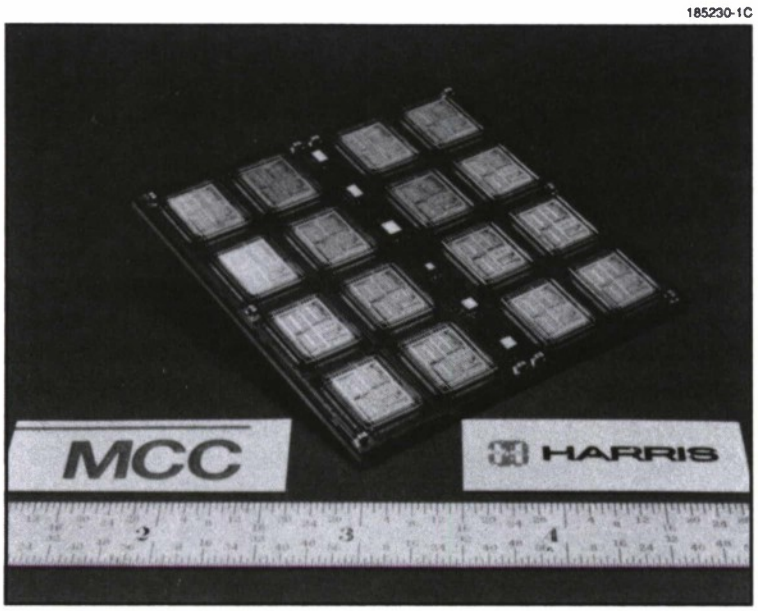

Figure 12. Photograph of MCC/Harris MCM.

The substrate is produced on a 5-in wafer that contains four substrates and a number of test sites. Figure 13 shows a photograph of an MCM substrate area of a wafer.

This photograph shows a section of the wafer with a number of substrate pad areas and package outlines for providing a heat sink frame for the die. Thermal vias connect this area to the outside package for efficient thermal conduction away from the die.

4.3.1 Three-Dimensional Packaging

A number of vendors [22] package MCMs in a three-dimensional framework. IBM has used three-dimensional packaging for various mainframe modules. Quadrant Technology and Electrochem have jointly developed a patented three-dimensional MCM package [16]. The package

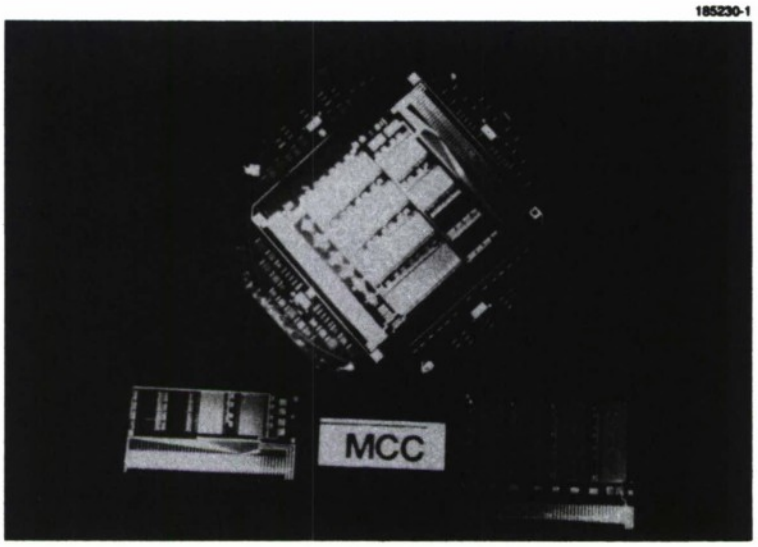

Figure 13. Photograph of MCC substrate on a 5-in wafer.

consists of a stack of substrates that are interconnected through a vertical interplane connector composed of thin-film-sputtered copper on polyimide. This packaging scheme provides 8-megabyte SRAMS. Figure 14 illustrates the main features of this package.

4.4 SPEED

Speed is perhaps the most vital factor driving current MCM technology. The ever-increasing throughput and clock speed of large, complex chips has fostered the development of MCM technology as an answer to the speed limitations imposed by the more conventional methods of packaging (such as PCBs). Figure 15 quantifies the projected increases in clock speeds [5] of leading-edge computer technology areas.

Figure 16 shows curves [24] that project an ever-widening performance gap between bare chip clock speeds and conventionally packaged (PCB) single IC clock speeds.

For 50-MHz bare chip clock speeds, the packaging penalty is 25%. This penalty is projected to grow to 75% by 1996 when typical bare chip clock speeds are expected to be 135 MHz. This projection reinforces the speculation that PCB technology is incapable of keeping up with the speed capability of future bare die clock speeds. Figure 17 shows results of an IBM case study [24] of package vs circuit speed for circuits packaged for the IBM 3033 computer using PCB technology and for circuits packaged for the 3081 computer using MCM technology [the IBM thermal conduction module (TCM)].

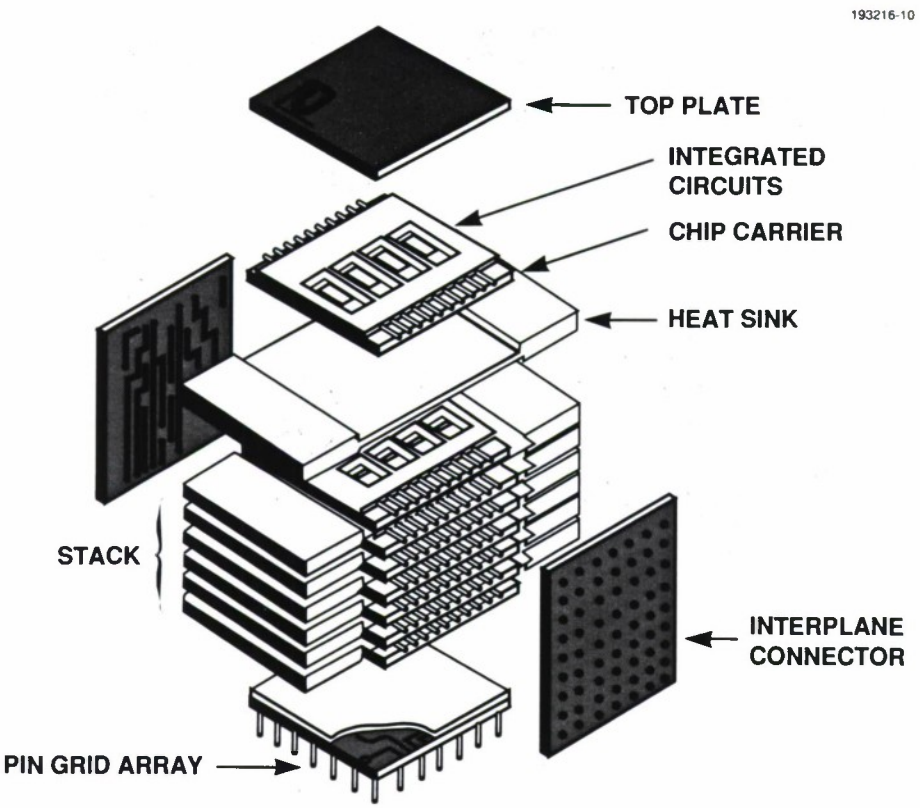

Figure 14. Quadrant Technology three-dimensional MCM package.

The study disclosed that package delays accounted for roughly 50% of the total cycle time for the PCB approach and roughly 33% of the total cycle time for the MCM approach. This quantitative study supports the rationale for using MCM packaging to significantly increase the clock cycle times of high-speed systems.

4.5 POWER

The development of CMOS technology was significant because it allowed a substantial reduction of power dissipation in most systems that had been formerly using bipolar devices. This was certainly true during the early days of CMOS development because the speeds that could be achieved with bipolar or CMOS devices were relatively modest by today's standards. CMOS power dissipation is a function of clock frequency, whereas bipolar power dissipation is relatively independent of clock frequency. Early CMOS devices were relatively slow and considered to be low in power. The crossover point for power dissipation was not reached until very high-speed CMOS devices became available and system clock speeds were raised significantly.

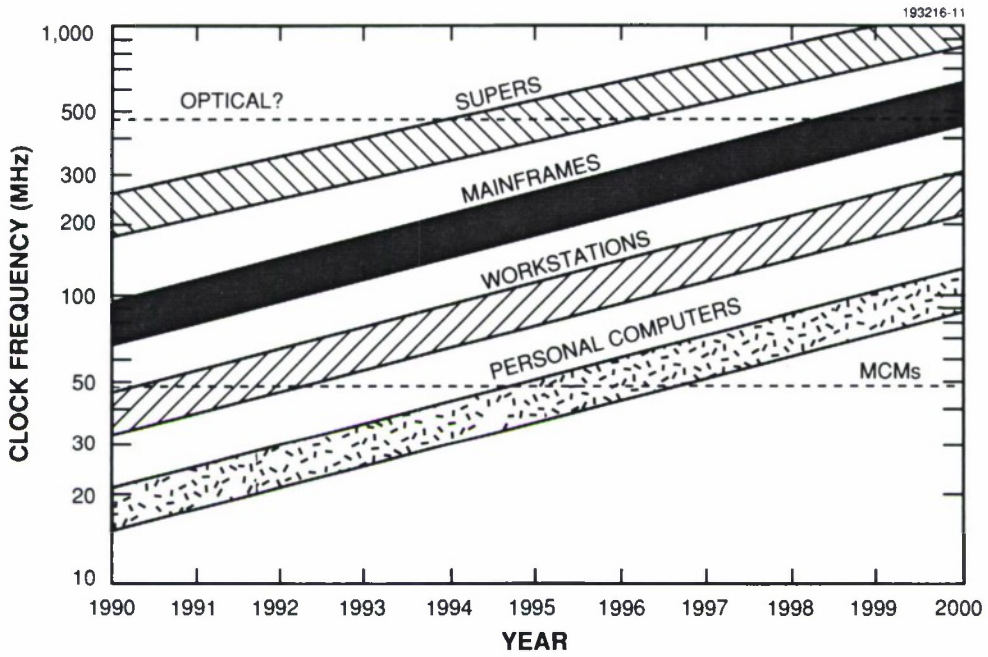

Figure 15. Clock speeds (leading edge).

The development of MCM packages has brought with it a new set of power-related packaging problems. Increased utilization ratios of die area to substrate area through the use of MCM technology have resulted in very close proximity of adjacent die and have thereby created the necessity for more efficient methods of getting the heat away from the die that are attached to the substrate. A number of novel methods [4] of facilitating heat transfer away from the die to the outside package have been generated during the development of MCMs. These methods include the use of low thermal resistance materials and thermal vias to transfer the heat from the die out to some dissipative package frame or heat sink.

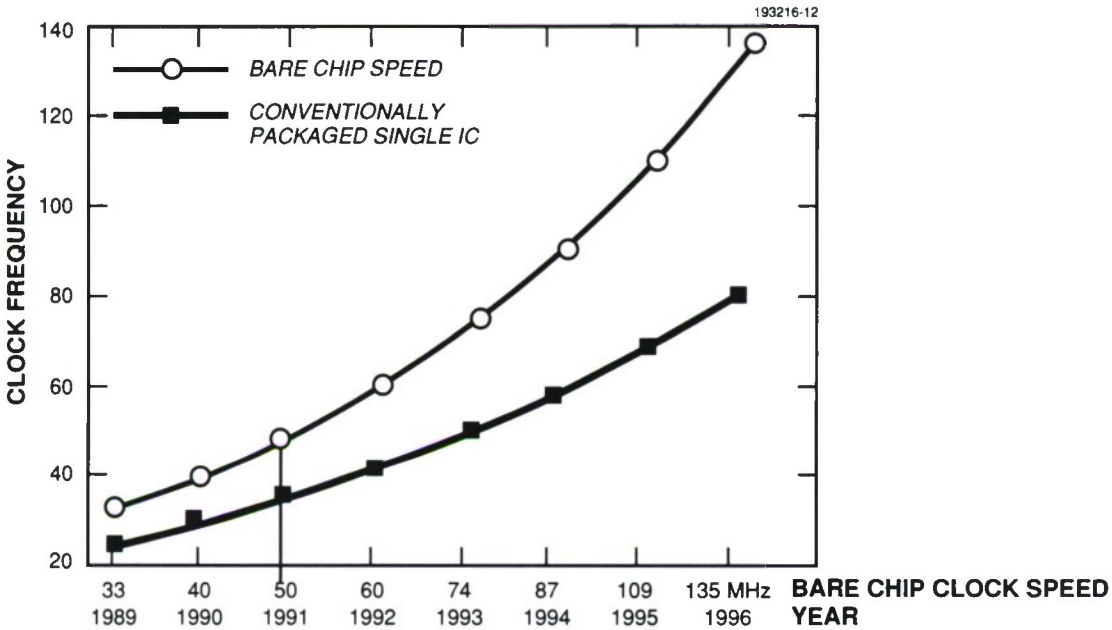

Figure 16. Interconnect performance gap.

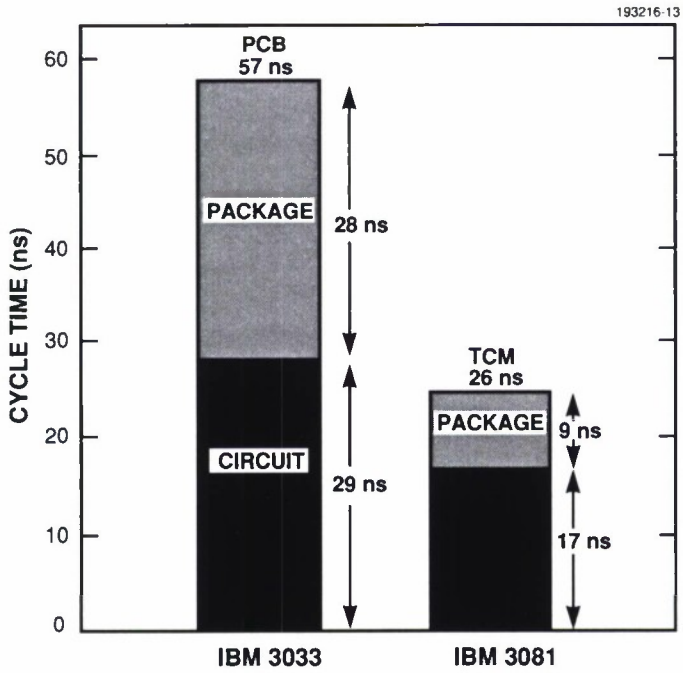

Figure 17. IBM case study: CPU cycle times.

5. MCM VENDORS

The fabrication technologies for multichip modules have evolved over a number of years. Because it is primarily an outgrowth and extension of thin and thick film hybrid IC technologies, some elements of the current MCM technology have existed for several decades. Several of the current vendors of MCMs have adapted their earlier processes to encompass MCM technology. In addition to many long-standing vendors of ICs such as Hughes, Harris, TI, GE, etc., a substantial number of start-up companies have entered the field. Figure 18 is a plot of forecasts for future MCM production and development.

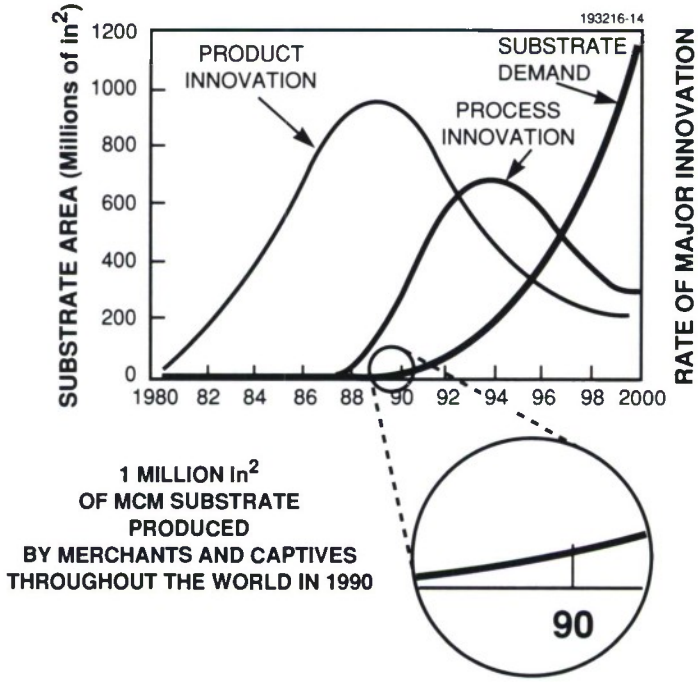

Figure 18. MCM forecast (BPA).

Other forecasts indicate similar trends and present a rationale for the explosion of MCM vendor activity. This graph was prepared by BPA, a management survey firm, which projected the manufacture of MCM substrates through the turn of the century. Clearly, the projected growth is exponential over this period with an expected increase, in terms of square inches of substrate area, of more than three orders of magnitude in the current decade to more than 1 x 10^9 in^2 of substrate by the year 2000. Assuming an average substrate area of 4 in^2, this growth translates into 250

million substrates. Two other curves provide indications of trends in MCM product and process innovations. The curves present relative rates of growth for these general categories and indicate that the innovations in types of MCM product offerings occurred at a maximum rate in 1989, whereas innovations in MCM processes are still occurring at an increasing rate that is expected to reach maximum growth rate in 1994.

5.1 SUBSTRATE MANUFACTURERS

Because the substrate is currently the most expensive item in the MCM assembly process, some manufacturers have concentrated their efforts in this area in order to maximize their profits in the MCM market. Some high-volume substrate suppliers have emerged as a result of this philosophy. Alcoa Electronic Packaging and Kyocera are both providers of MCM substrates. Advanced Packaging Systems has been a substrate manufacturer but has been moving toward producing fully packaged MCMs.

5.2 PACKAGING VENDORS

Because the final packaging of the assembled MCM substrate involves techniques that are a standardized part of intergrated circuit technology, many vendors have chosen to subcontract this portion of the MCM total design. This is the least critical portion of the MCM design cycle in terms of risky technology, and many packaging houses are available to fill this requirement if it is not provided by the MCM vendor.

5.3 VENDORS OF FULLY PACKAGED MCMs

A number of vendors that have in-house expertise in IC packaging have chosen to provide fully packaged MCM devices to their customers. These vendors are primarily large companies, although a few of the smaller start-up MCM companies have undertaken the total design approach. nCHIP is an example of a start-up enterprise that provides complete MCM packages.

5.4 MAINFRAME MANUFACTURERS

Mainframe computer manufacturers are perhaps the predominate current users of MCM designs. The race to provide speed and throughput to large-scale computers has necessitated the development of new packaging technologies to house the fast complex chips that are being developed for this new generation of computers and processors. MCM designs appear in nearly every new mainframe computer on the market and in many of the airborne and space-based processors being developed for the military. The following is a representative list of commercial and military systems that employ MCM technology.

1. DEC – VAX 9000
2. UNISYS – SCAMP Mainframe Data Processor

3. NEC – Mainframe Computers
4. CDC – 444R Space Computer
5. Hughes – Common Integrated Processor (YF-22 ATF)
6. TI – Aladdin Signal Processor
7. Space Computer Corporation – SCC-100 Parallel Processor [11]
8. Honeywell, GE – Generic VHSIC Space Computer (GVSC) [2]
9. Sun – SPARC Workstations

5.5 WORKSTATION MANUFACTURERS

With the advent of CAD workstations, a need has arisen for fast, reliable, small, low-power packages. This requirement is fulfilled through the use of MCMs that embody all of the characteristics necessary to meet the aforementioned objectives. As a result, engineering workstations comprise the second largest user sector in need of MCM designs.

5.6 MCM FOUNDRIES

The Defense Advanced Research Projects Agency (DARPA) has been instrumental in sponsoring research in areas relating to MCM design and implementation. DARPA is supporting technology and infrastructure creation in the MCM area [15]. These initiatives include MCM foundries, software tools (CAD and CAE), testing, packaging, manufacturing equipment, and systems integration. One such initiative is the creation of at least two MCM foundry operations [9]. These efforts are cooperative industry ventures by Texas Instruments and General Electric, and by nCHIP and E-Systems. Both of these efforts are slated to create an MCM foundry resource by the end of 1992. An initiative is under way by USC Information Sciences Institute that is expected to lead to a brokerage service, similar to the MOSIS foundry, that will facilitate the interface between intended MCM users and various MCM foundries.

6. CAD SUPPORT FOR MCMs

6.1 CAD OVERVIEW

The use of CAD tools for MCM development is an imperative. The fact that MCMs can use a large number of very expensive chips in a single design, and the high cost of the MCM design process, demands that a high priority be assigned to "right-the-first-time" design principles. CAD is an essential element in ensuring this level of design performance. In view of this requirement there has been a rapid growth in CAD support tools for MCM design. In most cases these tools have been developed as extensions of current CAD packages from either PCB or IC design disciplines, although a few new contracts have been awarded for the development of complete CAD software packages with direct application to MCM designs starting from fundamentals. One of the unique aspects of CAD support tools for MCM design and manufacture is that they require a large number of interdependent disciplines that must reside in a concurrent engineering framework. These disciplines encompass such diverse areas as thermal analysis, signal noise (crosstalk) analysis, signal quality analysis, signal propagation delay analysis, and multilayer automated routing as well as system testing and simulation.

6.2 SUPPORT TOOLS FOR MCM DESIGN AND MANUFACTURING

VALID Logic Systems has an MCM CAD design package called Allegro-MCM. The software includes design rule checks, placement and routing, thermal analysis, and signal noise analysis and provides direct manufacturing outputs with output formats that can drive various photoplotting machines.

Mentor Graphics offers a similar MCM support package known as MCM Station [8]. The Mentor software provides all of the features included in the VALID package with a few minor differences in implementation procedures.

Cadence Design Technology has developed MCM support tools that were derived from their IC CAD design package. Cadence has recently acquired VALID and will seek to integrate the best of each of their MCM design tools.

Dazix-Intergraph has a set of MCM tools called MCM Engineer [23] and MCM Engineer Plus. MCM Engineer features interactive placement and routing. MCM Engineer Plus provides a complete suite of tools that allows for all stages of MCM design including MCM manufacture.

Cadisys has a set of tools called Hybrid MCM Station, which handles both hybrid and MCM designs.

Table 5 presents a checklist summary of tools that are incorporated in several MCM support packages on the market.

Costs of CAD support tools for MCM design and manufacture are in the range of $100 K to $200 K depending upon platforms and licensing arrangements.

TABLE 5

CAD Support Tools for MCM Design and Manufacture

Vendor	Schem-atic	Place/ Route	Rule Check	Elec-trical	Noise	Thermal	Manu-facture
VALID	√	√	√	√	√	√	√
Mentor	√	√	√	√	√	√	√
Cadence	√	√	√	√	√	√	√
Quad Design	√	-	-	√	√	-	-
Contec	√	-	-	√	√	-	-
Dazix	√	√	√	√	√	√	√

6.2.1 Signal Noise Analysis

Most of the MCM design packages incorporate a signal noise analysis package such as the Quad Design Technology Crosstalk (XTK) toolkit. This package was developed to support PCB designs but works well with MCM designs using scaled parameters. The signal noise analysis tools can simulate signal propagation as a function of process parameters and routing, display signal shapes, and provide measures of signal quality. Figure 19 shows an example of I/O signal quality for two different implementations of an Intel 486 processor.

This figure demonstrates the dramatic speed performance improvements that can accrue from the use of an MCM. Technology Modeling Associates offers an interconnect analysis tool known as Raphael. Raphael simulates the electrical characteristics of arbitrary three-dimensional nonplanar interconnect structures and determines their contributed resistance, inductance, and capacitance to circuit performance. It automatically generates SPICE models for circuit analysis.

6.2.2 Thermal Analysis

Thermal analysis is another strict requirement for reliable MCM design. Closer MCM die placement and higher power dissipations in chips due to increased speed of operation combine to make die placement critically dependent not only on signal crosstalk properties but also on the elimination of thermal hot spots. This proximity adds another level of complexity to the automatic placement and routing design rules. All of the major MCM CAD packages take cognizance of this fact and include thermal analysis in the design suite for MCM design software. As in the case of signal noise analysis, some CAD vendors have adapted stand-alone thermal analysis tools and have integrated them into their MCM design suite.

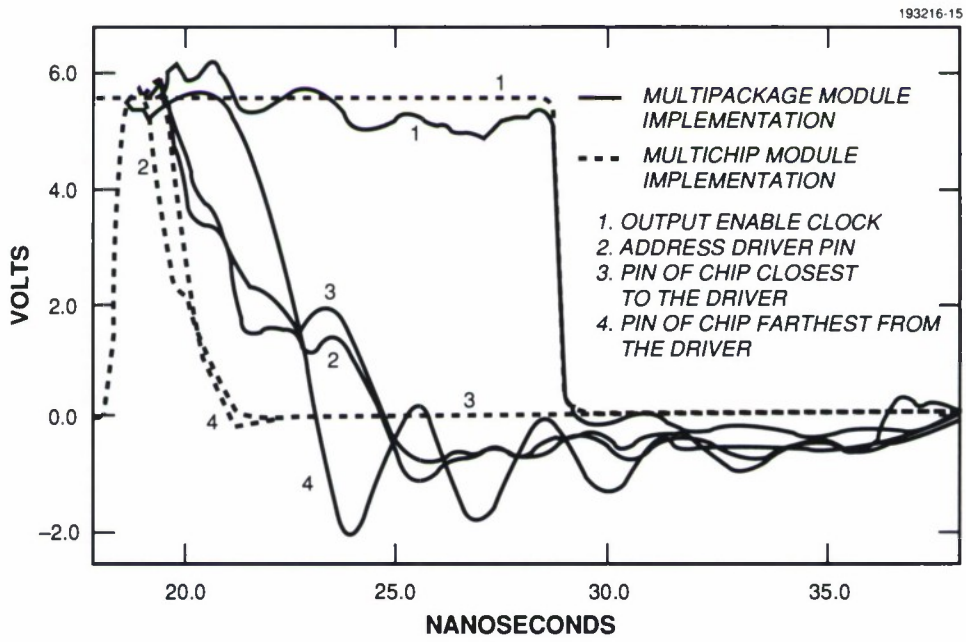

Figure 19. 486 I/O performance at 100 MHz.

7. TESTING ISSUES

7.1 TESTING OVERVIEW

The development of MCMs has brought with it a special set of requirements for the testing of fully packaged MCM systems. The testing is complicated by the increased density and proximity of the assembled die on the substrate and by the inaccessibility of the die/substrate connections. Several levels of testing are required for an MCM design. Probing of the bare die prior to connection of the substrate is a necessity. Similarly, testing of the interconnections made between the various module pins must be done on the substrate before and after the assembly of the die to the substrate. Finally, testing of the assembled die on the substrate material at speed is a critical step to ensure that the entire MCM works properly, in a system sense, over all parameter variations. Because of the nature of the compact MCM design, probing of the interconnections becomes increasingly difficult and various manufacturers and researchers are investing considerable time and effort in finding novel ways to satisfy the testing requirements for the packaged MCM.

7.1.1 Availability of Bare Die

One of the crucial factors affecting the MCM industry is the availability of bare die. In general, the die manufacturers prefer to provide packaged die because their profit margins are greater and because they can better safeguard yield and process information. A related problem is the difficulty of obtaining detailed information on the unpackaged die. Such information is vital in generating libraries for use with CAD support tools. Die manufacturers seem reluctant or unable to provide such information. The proliferation of MCM users is pressuring the industry to resolve this issue.

7.2 MCM TEST METHODS

Test methods for MCM designs are not standardized and are often left to the system designers who purchase the MCMs. Many different approaches to testing are in evidence, and a number of esoteric methods such as electron-beam "probing" are under investigation. The use of boundary scan testing is very much in evidence on the newer and more complex devices. Boundary scan [21] refers to special test hardware that is built into the device to allow access to most, or all, of the critical nodes of the device. The access is provided by means of a long shift register that is connected to the nodes of interest. Critical device states are serially shifted to output pins of the device for test analysis and comparison with known states in response to input conditions. The assembled MCM may be tested in a similar fashion if special test circuits employing the boundary scan principle are included as part of the overall MCM design. This design requires the addition of one or more test circuits to the MCM complex to perform the test function. Figure 20 shows an example of boundary scan for a digital device [7]. Boundary scan test methods have been standardized by the IEEE and are embodied in the IEEE 1149.1 test standard.

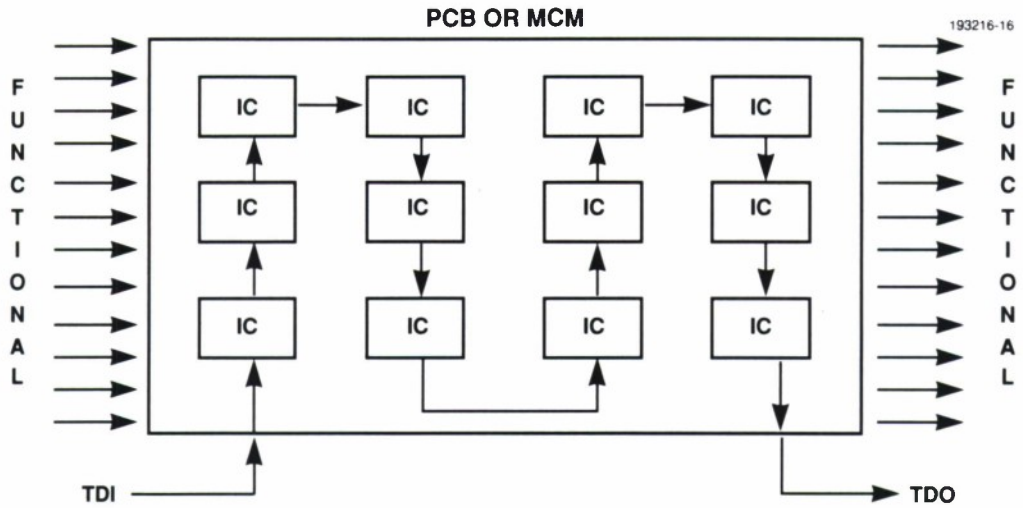

Figure 20. Boundary scan.

The primary lesson to be learned from current vendor MCM design experiences is that a great deal of planning and effort must be invested in providing adequate MCM test capability during the preliminary stages of the design. This enhanced level of test planning is required to ensure that satisfactory testing of the entire MCM system can be accomplished within the limits of the capability of the hardware and software test complex to be employed. Some degree of built-in self-test (BIST) must be incorporated in the design of the MCM from the outset.

7.3 TESTING FOR MILITARY APPLICATIONS

Because most of the current uses of MCMs are for commercial applications, MIL-STD tests are not generally applied to MCMs, with some notable exceptions. The Hughes Microelectronic Circuits Division does a majority of their MCM work for the military and therefore subjects all parts of their manufacturing process to full military test standards of MIL-STD Class B to Class S levels as required. GE is also involved in a large number of military programs that require MIL-STD tests that are applied to their completed MCM packages. GE uses a proprietary MCM process that is called high-density interconnect (HDI) [3]. The process involves the use of chips placed in tailored cavities formed in a ceramic blank. A computer-controlled pick-and-place machine puts the chips as close as 0.01-in apart. Silicon die densities can exceed 90%. The chips are bonded in the cavities using thermoplastic resin. Thin film metal interconnect layers are sputtered on the surface and into laser-generated via holes formed with the use of an excimer laser.

nCHIP is a start-up enterprise that uses silicon dioxide dielectric rather than polyimide, as most others do. Functional MCMs made by nCHIP have passed all MIL-STD-883C tests. nCHIP provides an hourly test flow for their process line, which is shown in Figure 21. Although they have not produced any MCM products for military applications, their normal process flow would appear to be capable of qualification for space applications.

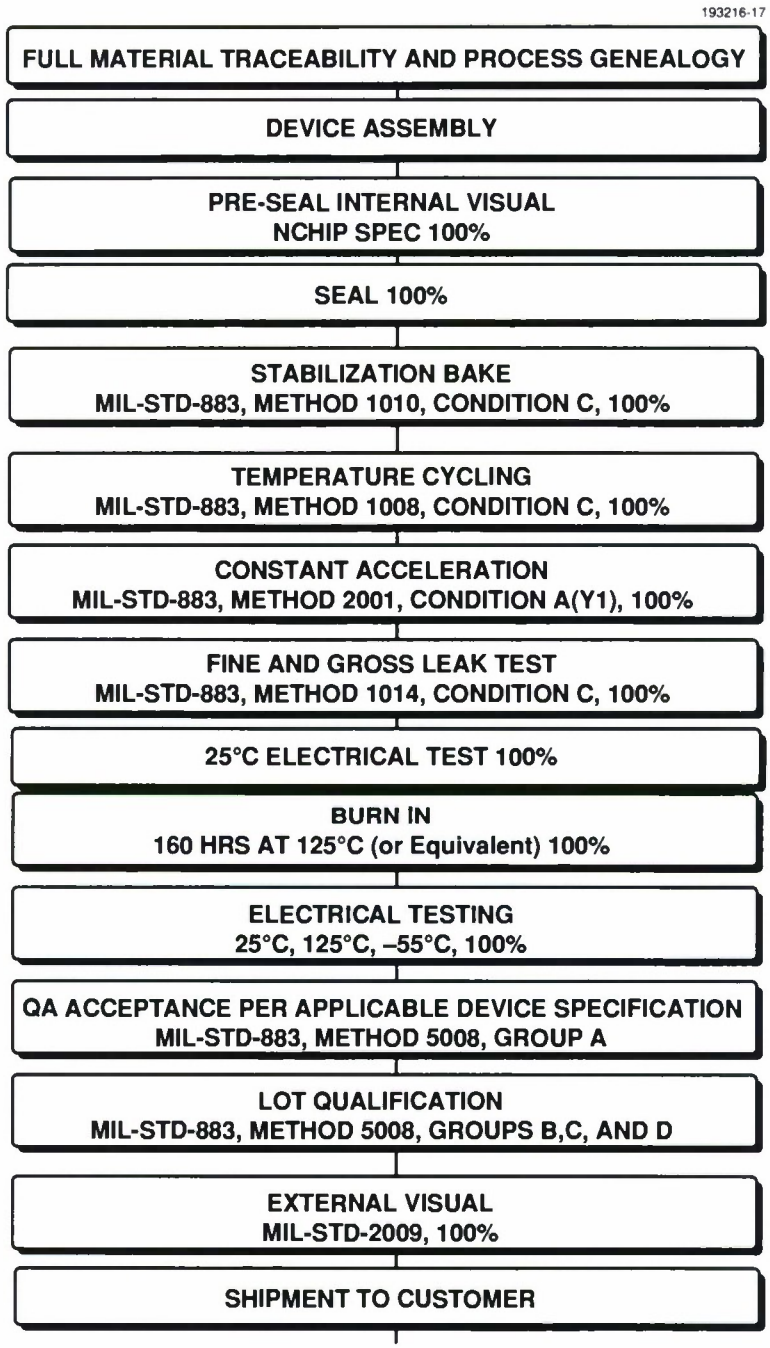

Figure 21. nCHIP hourly MCM test flow.

8. COST ISSUES

8.1 COST OVERVIEW

The current cost structure for MCMs is high compared to most PCB development costs [18]. Prospects for cost reductions are improving because process innovations are still on the rise. Figure 22 shows cost curves for a number of packaging systems including MCMs.

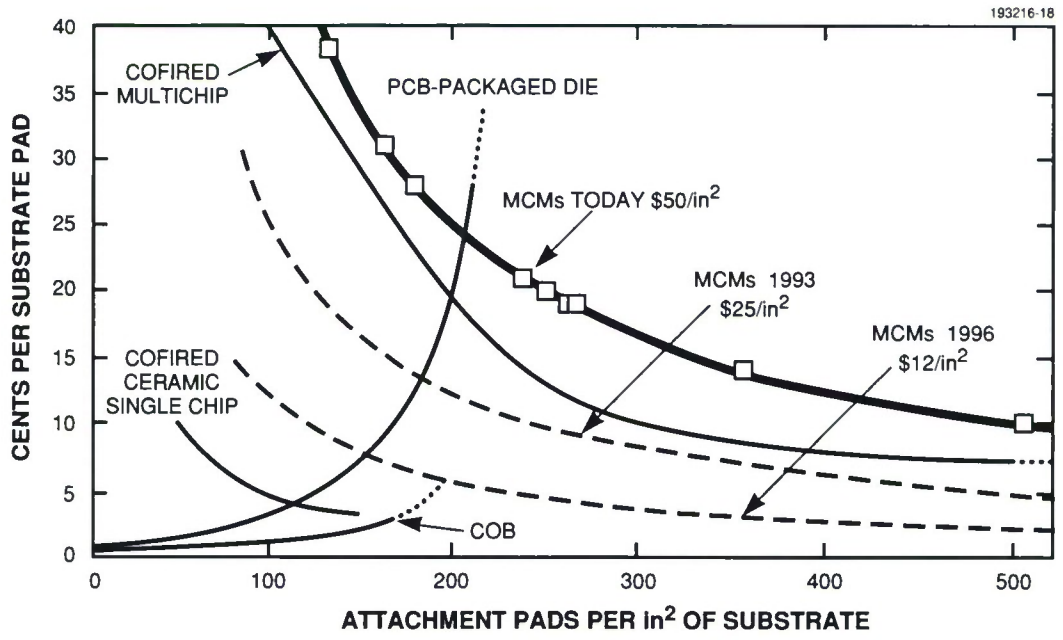

Figure 22. Cost per interconnect substrate pad (BPA).

These curves represent current costs and projections of future costs for MCMs [5]. The curves were prepared by BPA, as were the earlier curves for MCM sales forecasts. BPA used a special metric for comparing costs (cost per interconnection substrate pad). These pads are the attachment pads on the interconnect substrate. The value of this metric is that it is process independent. The curves show a projected reduction in cost by a factor of 2 in 1993 and again in 1996. The use of an MCM implementation in preference to a PCB implementation currently is cost effective at about 200 pads/in^2, which appears to be the limit of PCB pad density. By 1996 this cost-effective point will be reached at a pad density of 150 pads/in^2. These comparisons are for PCB implementations

using individually packaged die. The chip-on-board (COB) approach provides somewhat higher density but is still not as cost effective as MCMs for high pad densities. The current status of MCM technology is that low volume requirements are burdened by substantial nonrecurring engineering (NRE) costs. Although this is also true for PCB designs, the NRE costs are comparatively lower.

If MCM designs are to be generated in-house, the cost of a compatible CAD system is an issue. The current cost of a suitable MCM CAD package can range between $100 K and $200 K.

9. DESIGN FLOW

The MCM design flow [10] is similar to the one used for hybrid devices. Figure 23 shows a typical design flow.

The MCM design can be presented to the MCM vendor at one of several junctures of the flow depending on the vendor entry-level options available. Most vendors will allow a schematic diagram or net list entry level, while others prefer to take the MCM design from a block diagram conceptual level. Although this flowchart does not explicitly call out the thermal and signal noise analyses, they are embodied as part of the prelayout and postlayout AC simulation and static timing analysis steps. After all design rule checks have been satisfied, the desired manufacturing output file is generated.

9.1 CAD DESIGN FLOW

The CAD design flow uses different approaches from those used for the development of an IC or PCB. Each stage of the process is interactively coupled to analytical blocks so that changes in routing or process parameters produce new outputs that must be reanalyzed to remain within predetermined performance metrics. This process can be done in a design rule check format or interactively for the fine-tuning of signal characteristics. Simulation of the MCM design is an important aspect of the CAD design flow that follows the placement and routing step in the design process. Back annotation of intermediate results during simulation is done in an iterative process until all design criteria are satisfied.

9.2 MCM PROCESS FLOW

The MCM process flow is similar to many semiconductor process flows because most substrates are made in processes that mimic IC production. Figure 24 shows a typical process sequence [6] for multilayer ceramic substrates.

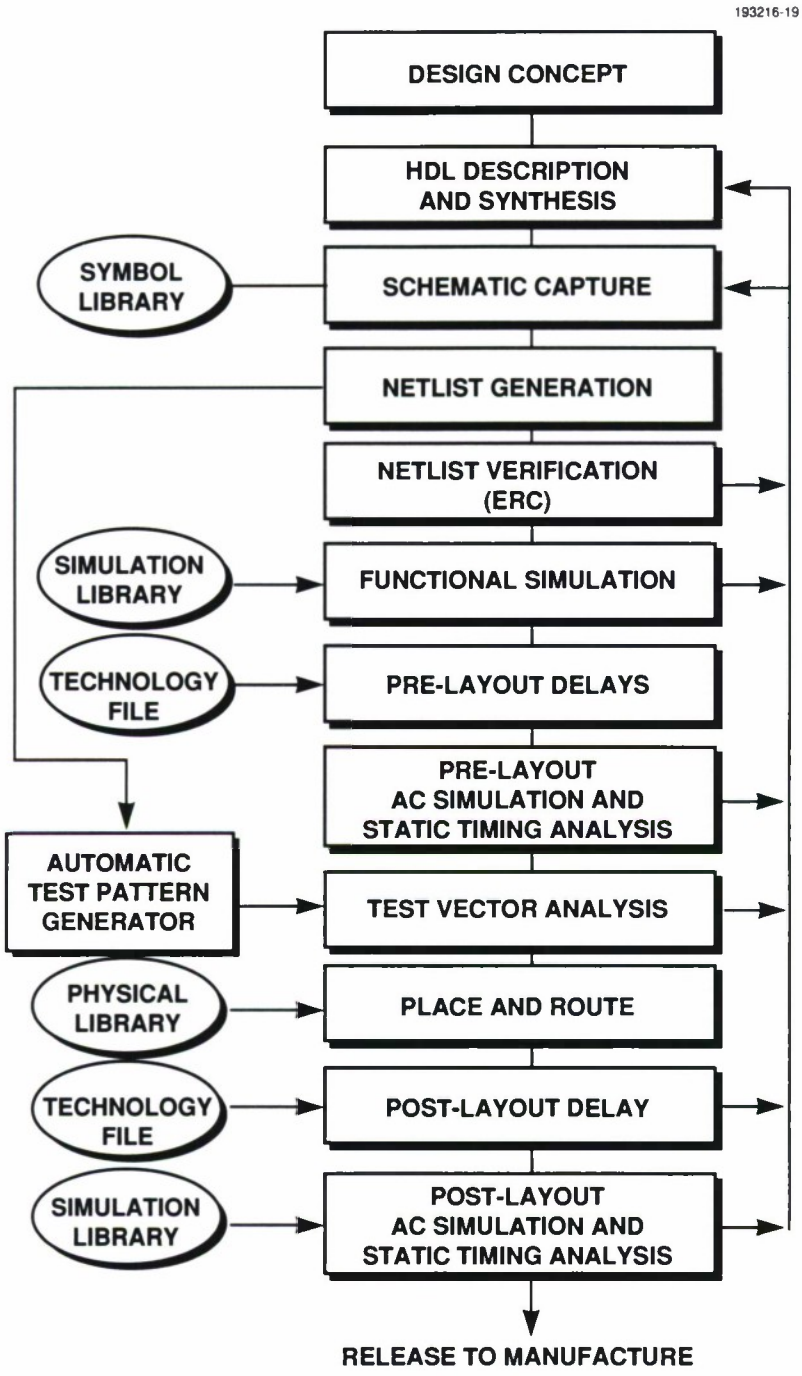

Figure 23. Typical MCM design flow.

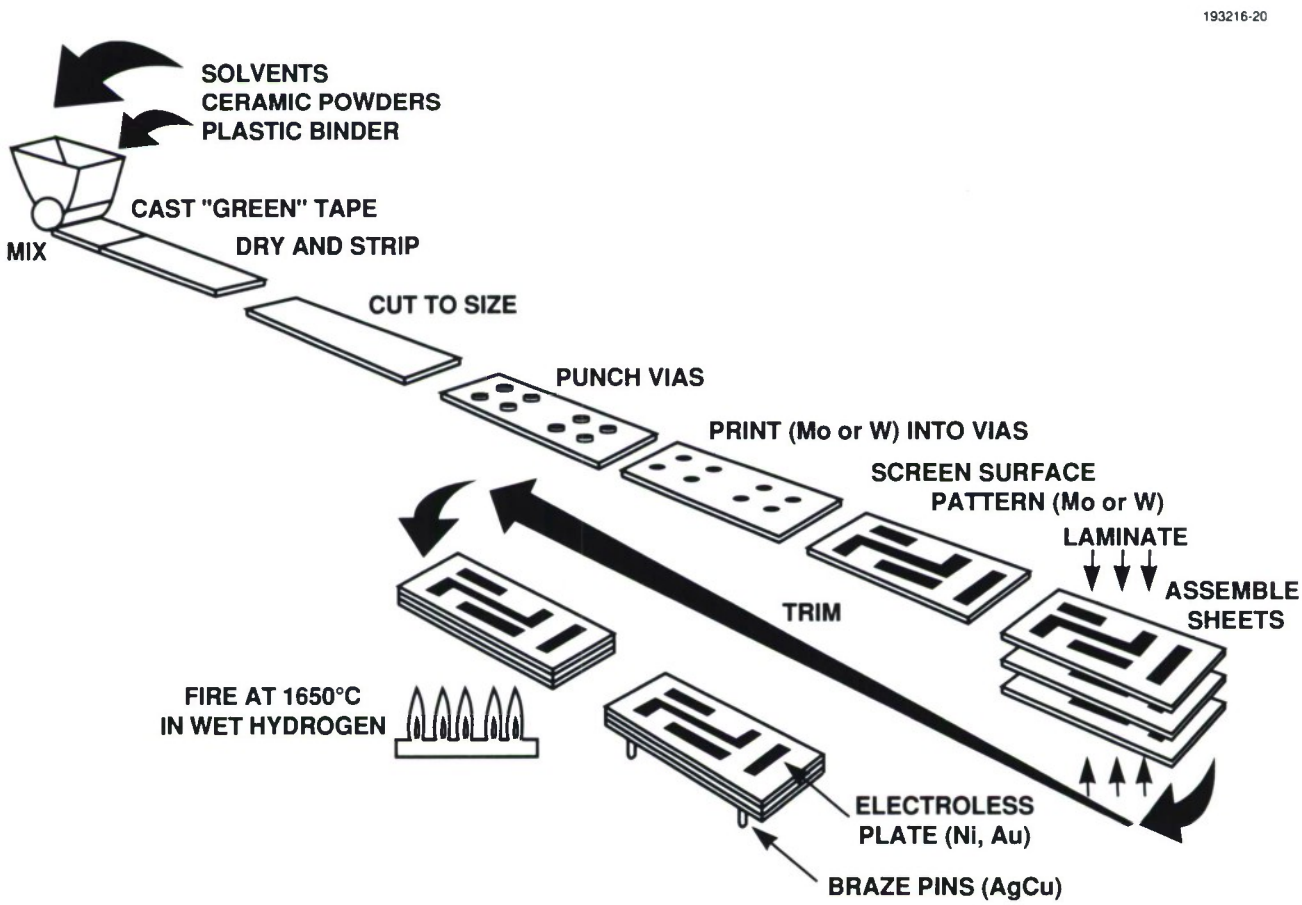

Figure 24. MCM process flow for ceramic substrates.

10. ADVANCED MCM DEVELOPMENT PROGRAMS

A substantial amount of work is under way to extend the range of usefulness for MCMs and to solve existing problems related to MCM technology. An industry consortium under the direction of Microelectronics and Computer Corporation has initiated a host of advanced MCM development programs. Among these are

1. Reliability without hermeticity (RWOH)
2. Low cost interconnect
3. Laser bonding
4. Noncontact electron beam testing
5. CAD support tool development
6. Advanced packaging technology

The following is a summary of MCM research and development programs in other companies that hold a similar promise for improvements in critical MCM technology areas.

1. Optoelectronic MCM – Advanced Packaging Systems (APS) is developing an MCM technology [13] that involves the use of optical fibers embedded into grooves in the MCM substrate to allow high-speed interconnection to other MCMs or external system packages. The technology employs optical waveguides deposited on the substrate and creates various beam-splitting junctions. A schematic of a substrate containing this technology is shown in Figure 25.

   The module is a beam splitter using both evanescent and Y junctions. The evanescent junction is formed by placing two waveguides in close proximity (approximately 1 micron) where the vanishing fields surrounding the waveguide sections can provide signal coupling. Similarly, the Y junction makes use of tapered waveguide sections to distribute signals to several different taps. A great deal of activity is noted in the area of optical interconnect technology for MCMs [1].

2. Bonded interconnect pin (BIP) – APS has developed BIP [14] for use in providing the close alignment necessary to ensure adequate coupling between optical fibers and the pins of the chips attached to the substrate. An array of gold wire posts that are approximately 2 mils in diameter and 20 mils high are attached to the die pads through solder wells. This array forms a compliant frame that can be adjusted to provide optimum coupling to the optical fibers. Figure 26 shows a schematic of the BIP process.

3. Copper-on-glass ceramic substrate – IBM is developing a copper-on-glass substrate technology that offers enhanced speed performance and matched die-substrate thermal properties. Figure 27 shows a curve of propagation delay vs dielectric constant

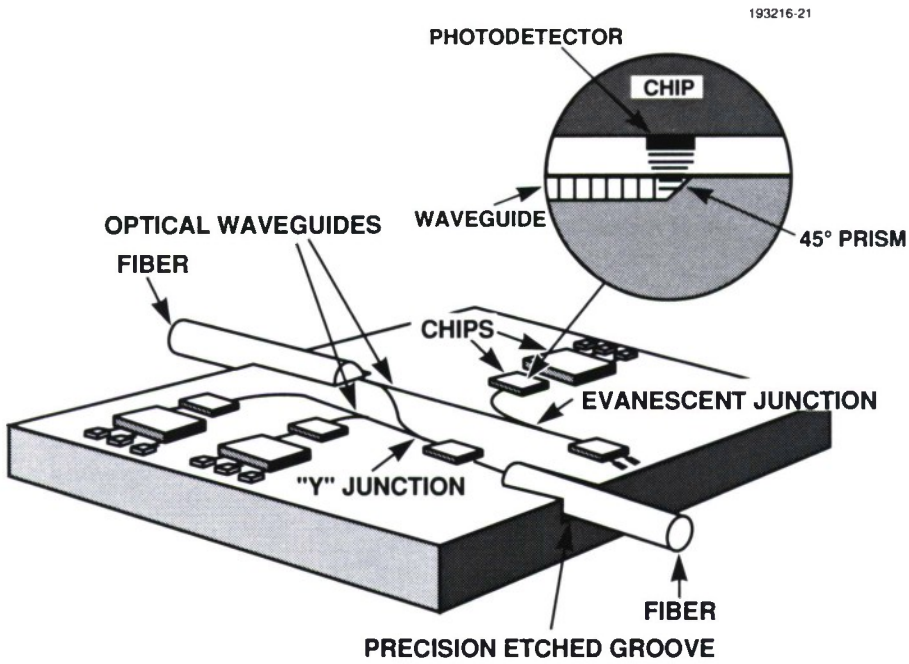

Figure 25. Optoelectronic MCM.

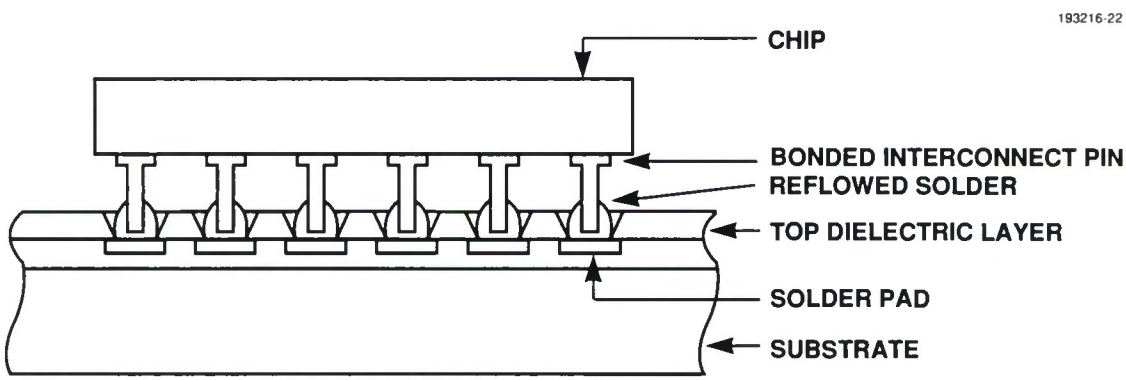

Figure 26. Bonded interconnect pin (BIP) schematic.

[20] for various substrate materials. The low dielectric constant of the glass ceramic substrate engenders lower propagation delays than most other substrate materials.

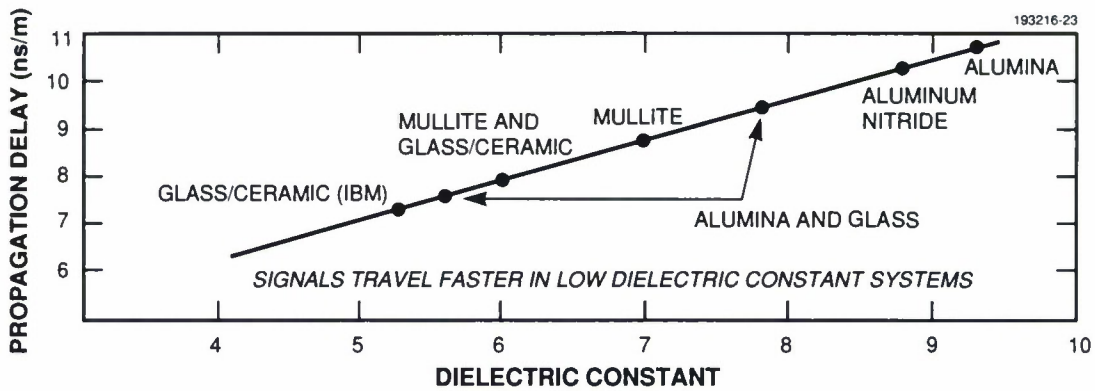

Figure 27. Propagation vs dielectric constant.

Figure 28 shows a curve of the Coffin-Mason relationship [20] of fatigue life vs coefficient of thermal expansion. Silicon and glass substrates are shown to have very similar coefficients of thermal expansion. This similarity provides a very low stress level for the die-substrate interface, which leads to higher reliability for the matched material system.

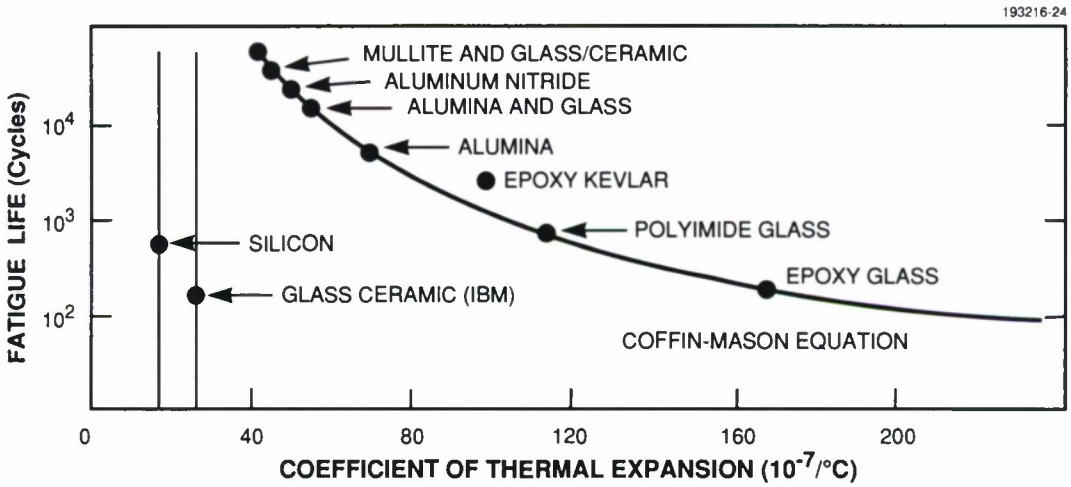

Figure 28. Fatigue life vs coefficient of thermal expansion.

11. TECHNOLOGY ASSESSMENTS

A large number of alternative methods exist for producing MCM designs. In this section some of these alternatives are sorted out and some measure of relative worth is attached to each. Tables 6 through 8 provide comparative value judgments on the major technology features inherent in MCM designs. Table 6 presents relative value judgments for thin film substrate materials.

TABLE 6

Value Judgments for Thin Film MCM Substrate Materials

Type	Substrate (Electrical)	Conductor (Electrical)	Thermal	Density	Flexi-bility	CTE	Cost	Avail-ability
Silicon	E	G/E	G/E	E	E	E	H	F
Aluminum	E	G/E	E	E	E	P	M/H	P
Alumina	F/P	G/E	G	G/E	E	G	M/H	G
Organic	G/E	G/E	F/P	G/E	E	F/P	M/H	P

E= Excellent, F= Fair, G= Good, P= Poor, M= Medium, H= High

Thin film substrates are considered to be the best choice for high-performance applications. The best electrical properties are found in silicon and aluminum substrate materials. The electrical properties of the conductors on the various substrates are all good to excellent. Organic substrates are not well suited to high power applications because of their relatively poor thermal characteristics. The high density capability and flexibility are generally excellent for all thin film substrate materials. Aluminum and organic substrates have a generally poor coefficient of thermal expansion (CTE) and are not good choices for applications requiring high power levels and high reliability. Silicon substrates possess the best overall set of characteristics for high- performance applications, but their cost is generally very high and their availability is fair.

Packaging techniques for MCM designs should be matched to the application requirements of the overall MCM system. Table 7 provides a relative scale for comparison of thermal and electrical characteristics for the various techniques used to package MCM designs. Maturity of the various package types is also rated on a relative scale.

TABLE 7

High-Density MCM Package Comparisons

	Thermal (1=Best)	Electrical (1=Best)	Maturity (1=Most Mature)
Chip-On-Board	3	4	1
TAB	2	3	4
Flip-TAB	4	2	4
Plastic QFP	8	8	1
Metal QFP	5	5	3
Ceramic QFP	7	7	2
Pad Grid Array	6	6	4
Flip-Chip	1	1	5

Flip-chip packaging is the most advantageous for both thermal and electrical properties, but it is the least mature technology for MCM packaging. The availability of bare die suitable for flip-chip packaging schemes is very limited but is improving. Quad flat packaging (QFP) is the most mature package technology, but it can only be used for low-end applications. Table 8 provides a comparative summary of module packaging features for plastic and ceramic flat packs, which represent the low-end packaging choices versus standard and high-performance MCM packages.

The tables presented in this and earlier sections of this report can be consulted by the intended user to select a process, package, or interconnect technology that satisfies particular requirements dictated by the MCM system.

11.1 CHOICE OF VENDORS

Many factors enter into choosing vendors for an MCM design effort. Numerous vendors use a wide variety of methods to implement MCM designs. One advantage of this situation is that a vendor can be chosen to satisfy specific sets of system requirements in an optimum way. Section 2.1 of this report presented tables of comparisons between different implementations used by various vendors. These tables may be consulted by the user to achieve a best fit of vendor capabilities to MCM system requirements. Vendors are divided between suppliers of substrates, fully tested MCMs, and MCM package houses, which simplifies the task of choosing a vendor, once a project assessment is made to determine which level of design involvement should be undertaken.

TABLE 8

Module Packaging Features

Technology Feature	Plastic QFP	Ceramic QFP	Module	High-Performance Module
Cost	Low	Low	Medium	High
Size	Limited	Limited	Large	Very large
Substrate I/O	Peripheral	Peripheral	Array	Array/Peripheral
Module I/O	Peripheral	PGA/Peripheral	Array	Array/Peripheral
Thermal	Poor	Fair	Good	Very Good
Repairability	Poor	Poor	Fair	Good
Hermetic	No	Yes	Yes	Optional

11.2 CHOICE OF TECHNOLOGY

Many different technologies are employed in the manufacture of MCMs. Trade-offs that must be made in the choice of MCM technology for particular applications may involve cost, reliability, speed, size, testability, and performance. Any high-performance technology is certain to involve cost penalties that must be placed in the framework of the user's assets.

11.3 CHOICE OF CAD DESIGN TOOLS

Current CAD design tool choices are relatively limited, and this makes the choice of a vendor for support tools somewhat easier. A great deal of competitive activity exists among a large number of CAD vendors to produce MCM design support tools. This competition gives testimony to the fact that MCM technology is growing rapidly and will supplant PCB technology for a majority of newly emerging high-throughput system applications. Because MCM design involves several technical disciplines in a concurrent interactive framework, a CAD support package for MCM design should incorporate this design philosophy rather than one that merely patches together individual thermal, signal noise, and signal quality analysis packages.

11.4 VENDOR INTERFACE

Because of the large number of choices for MCM involvement, the high cost of tooling for MCM development, and the limited funding available for initiating new research efforts, the type of interface that should be made with the chosen vendor involves a large number of complex decisions. Costs for designing and producing MCMs vary markedly as a function of entry level into the MCM process. Because CAD tools for MCM designs are sophisticated in view of the many design disciplines involved, costs for creating an MCM from a block diagram input level are high.

Providing a net list input to the MCM vendor should be the lowest entry level considered. Entry at this level assumes that one either rents or purchases a CAD support package for MCM designs. Figure 29 portrays a host of factors and options that might be involved in the decision of how to interface with the vendor [25].

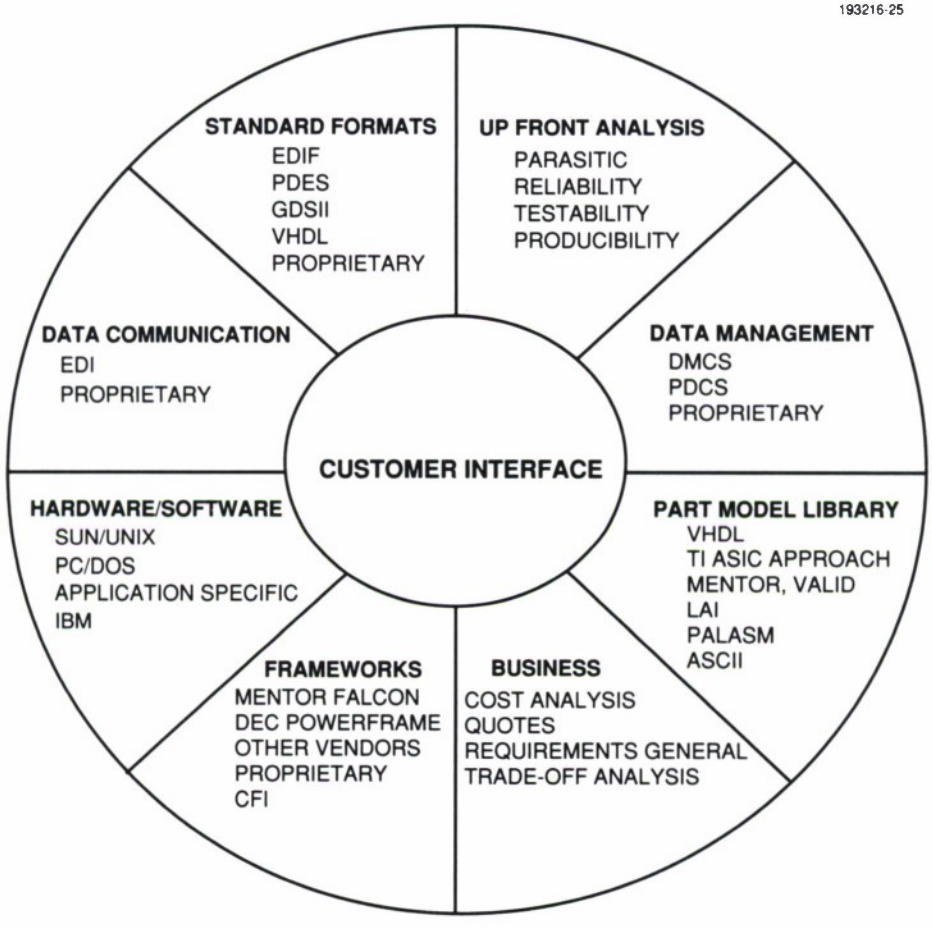

Figure 29. Customer interface perspectives.

12. SUMMARY

MCM technology is growing at a rapid rate that should reach full maturity within a few years. Current capabilities are real enough to provide significant improvements to systems that have already been designed or are under development. The improvements include increased speed and throughput, smaller size and weight, and higher reliability. Areas that are in need of improvement or further development include CAD support tools, testing, and reduced cost.

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13. ABSTRACT (*Maximum 200 words*)

Multichip module (MCM) technology addresses the large gap that exists between the speed and circuit densities achieved in monolithic integrated circuits versus those achieved at the board and subsystem level using conventional through-hole and surface mount package technology. Multichip modules promise not only to improve board-level circuit densities but also to support dramatic increases in clock rate and reductions in overall power dissipation. This new technology is driven by the realization that current printed circuit board technologies are inadequate to achieve the speed and system throughput capabilities inherent in the chips that are now becoming available.

Multichip module technology centers on the high-density interconnection of bare die on a suitable substrate, resulting in a module with up to 95% of the substrate area devoted to active circuits. The technology features substrates that are generally made of silicon or ceramic with insulating layers of polyimide. Various other materials are employed by a host of vendors, and the technology, which is available now, is continuing to mature at a rapid rate. MCM technology is supplanting printed circuit board technology for most high-performance applications and will provide a vehicle for leading-edge digital systems in the 1990s.

The advantages of MCM technology over conventional packaging schemes include very high packaging densities, clock speeds in excess of 500 MHz, lower power due to reduced capacitances, higher reliability, and better thermal matching of the die to the substrate material. The current disadvantages include the high cost of substrates, limited availability of bare die, and difficulties in testing at speed. These disadvantages are being addressed and are expected to improve. This report includes a discussion of the state of the art of MCM technology, MCM vendors, and emerging CAD tools for the design and manufacturing of MCMs.

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cofired ceramic	silicon	interconnect substrate	TAB	thermal via	
computer-aided design (CAD)	copper				

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