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Professor Hadis Morkoc

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Univ of Illinois @ Urbana-Champaign
Coordinated Science Laboratory
101 W. Springfield Avenue
Urbana, IL 61801

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13. ABSTRACT *(Maximum 200 words)*

Growth conditions have been established for GaAs, InGaAs, InP and InGaP using the newly installed Gas Source Molecular Beam Epitaxy apparatus. A study was conducted on the pseudomorphic epitaxy of Si on GaAs. MIS structures were pursued through various SiN_x and $SiGe_x$ interlayers.

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FINAL

~~ANNUAL~~ PROGRESS REPORT

Covering the Period of
January 1, ~~1991~~ ? through December 31, 1991

III- V HETEROJUNCTION STRUCTURES

AND HIGH SPEED DEVICES

U.S. Air Force AFOSR 89-0239

March 2, 1992

Principal Investigator

Hadis MORKOÇ

University of Illinois at Urbana-Champaign
Coordinated Science Laboratory
1101 W. Springfield Avenue
Urbana, IL 61801

I. SUMMARY

Our accomplishments for the past funding period can be grouped into four categories. These deal with the issues related to two dimensional phenomenon, some of which are germane to heterostructure growth, heterojunction bipolar transistors, MIS structures, and ohmic contacts and quantum wells, the last is grouped under miscellaneous. The laboratory facilities which were under installation during the last reporting period are all complete and have been is use for the projects funded by the AFOSR.

In what follows, we address the progress in each one of the four categories mentioned above. Following a brief introduction, abstracts of publications resulting from research carried out under the AFOSR sponsorship are enclosed for more details. In case elaboration beyond what is provided is required, the publication list provided will guide the inquirer to the appropriate journal citation.

II. PROGRESS MADE

II a. Hetrostructure Growth:

Safety has been a major concern for the custom Gas Source MBE system in the Epicenter. Considerable care has been taken for the safe use of the toxic gases. The integrated safety system consists of a network of interlocks and continuous toxic gas monitoring to provide multiple levels of protection against the toxic gases. A well designed air flow pattern has been incorporated to assure good air quality in the laboratory and in the gas storage facility.

The growth conditions have been established for GaAs, InGaAs, InP and InGaP, with recent emphasis on InGaP grown on (100) GaAs substrates. The low temperature photoluminescence linewidth is as narrow as 6.7 meV. Hall measurements show a room temperature electron mobility of 1500 cm^2/Vs and an unintentionally doped n-type carrier concentration of $1.7 \times 10^{16} cm^{-3}$.

Ultra thin Si layers between GaAs layers have been grown by MBE and characterized by cross sectional transmission electron microscopy. The lattice relaxation and antiphase annihilation have been investigated via the thickness of the Si layers. It has been found that a 9 Å Si layer grown on GaAs is pseudomorphic while an 18 Å Si layer is relaxed. Annihilation occurred within 100 Å of the interface for the 9 Å Si layer and about 1500 Å for the 18 Å Si layer.

The first epitaxial growth of GaAs on Si without the need for a high temperature (>850°C) oxide desorption step was demonstrated. This novel low temperature Si surface treatment utilizes a final HF treatment whereby the Si surface dangling bonds are terminated by hydrogen atoms. High quality GaAs epitaxial layers were successfully grown on the Si substrates with the pre-growth substrate preparation temperatures as low as 600°C.

II b. Field Effect Transistors:

Few years back we made the decision not to pursue research in conventional MODFETs that is industrial by nature and began MIS structures. We feel that the present MODFET structures suffer to a large extent from the induced parallel conduction in the barrier layer which essentially limit the sheet charge that can be modulated by the gate. Our group published two seminal papers on the subject (later a couple of other groups dubbed the name -lack of gate control- for the same phenomenon) We believe that this is the remaining barrier which keeps the community from obtaining the ultimate performance from FETs.

The structure that will alleviate the problem of charge accumulation in the barrier that cause the upper limit in the charge that can be controlled by the gate is the MIS structure. However, compound semiconductors have not yet have an MIS structure with interface properties good enough for such a device. We are attempting to break this by creating in situ deposited MIS structures which we believe will have the necessary properties for high performance FETs. Once accomplished the applications are not limited to the microwave/millimeter area with limited focus. Commercial world which to a large extent relies on the digital devices will also benefit from this technology as the MIS device would only require the control of only a few parameters and provide an interface which can handle large gate potentials.

MIS capacitor structures to be discussed below is in answer to the problem presented above:

We demonstrated the deposition of single crystal homoepitaxial Si at temperatures as low as 400°C using silane. It was observed that the plasma assisted deposition process at low temperatures was inhibited by the presence of hydrogen at the growing surface. An equilibrium between the rate of hydrogen desorption and generation of reactive radical participating in the deposition was reached at 460°C with 60 W of microwave power. For a 1000 Å thick epi-Si layer a background n-type doping concentration of less than 5×10^{16} cm^{-3} was measured. We have used this deposition technique to obtain a Si_3N_4/epi-Si metal-insulator-semiconductor capacitor (both the Si and Si_3N_4 layers were deposited in the same chamber) with an interface trap density of 2×10^{10} $eV^{-1}cm^{-2}$. The dielectric breakdown field of Si_3N_4 deposited on Si substrates and epitaxial Si/GaAs samples was found to be greater than 10 MV/cm for both cases. The I-V characteristics of the Si_3N_4 films at high fields are best represented by Fowler-Nordheim tunneling. Hole inversion of the n-GaAs layer was clearly seen in the quasi-static C-V curve. From the high-low C-V method we estimated the interface trap density to be of the order 4×10^{11} $eV^{-1}cm^{-2}$ and from the conductance measurements we found a value of 10^{12} $eV^{-1}cm^{-2}$.

We obtained an interface trap density of 3×10^{11} $eV^{-1}cm^{-2}$ in Si_3N_4/Si_xGe_{1-x} metal-insulator-semiconductor capacitors. We observed no significant change in the fast interface trap density for samples with 50 Å of Si grown on top of the Si_xGe_{1-x} before the deposition of Si_3N_4. This is in contrast to results obtained with SiO_2 as the gate dielectric.

We demonstrated the use of methane in an electron cyclotron resonance (ECR) plasma source to obtain very high carbon delta-doping in GaAs. By changing the deposition conditions sheet carrier density as high as 7 X 1012 cm-2 with a hole mobility of 75 cm2/V-s were obtained. All the layers obtained under different deposition conditions had good surface morphologies. It was also observed that the deposition was limited by mass transport.

Ga outdiffusion into Ge layers grown epitaxially by MBE was observed by secondary ion mass spectroscopy (SIMS), X-ray photoemission spectroscopy (XPS), capacitance-voltage, and temperature dependent Hall-effect measurements. The amount of Ga outdiffusion was greatest for films initially grown at 300°C. No direct evidence of As outdiffusion at any temperature or of Ga outdiffusion at initiation temperatures below 300°C was found. Hall-effect measurements showed higher hole concentrations and greater levels of compensation in films initiated at 300°C, consistent with outdiffusion of both Ga and As at this temperature. No degradation in the electrical characteristics of Ge-GaAs diodes was observed when the initial Ge growth temperature was reduced from 300°C to 200°C.

II c. Heterojunction Bipolar Transistor:

We applied the demonstrated carbon delta-doping by ECR activated methane to Npn AlGaAs/GaAs heterojunction bipolar transistors. The delta-doped base region had an average doping density of 5×10^{17} cm^{-3}. The device exhibited common emitter current gains of about 50, with the highest being about 75, at a collector current density of 4×10^3 A/cm^2 and collector voltage of 3 V. The devices were subjected to a 700°C anneal in H_2 for 20 minutes. The current gain and other characteristics obtained before and after anneal were very similar. In addition, the emitter-base junction ideality factor did not exhibit any change with the anneal.

We pursued a detailed investigation of the collector-emitter voltage corresponding to zero collector current. Single and double heterojunction bipolar transistors with graded and abrupt emitter-base heterojunctions were studied. The cause of large offset voltage in abrupt GaAs/AlGaAs SHBT and its reduction using a DHBT structure were clarified.

Also the effect of valence band offset on high frequency characteristics at high current density was modeled. It was shown that near Kirk effect a barrier may form at the collector. The variation of barrier height with collector current density and the degradation of current gain and frequency performance was studied. The results were particularly relevant to Si/SiGe HBT's.

Minority charge storage in single and double heterojunction bipolar transistors was modeled. The effect of band offsets, base grading and recombination lifetimes was described. The application of HBT's to I^2L circuits was considered. An improved Schottky coupled I^2L circuit was proposed for obtaining a small gate delay.

A unique device design incorporating 22 emitter fingers was used to give an AlGaAs/GaAs on Si power HBT a junction temperature spread across the entire device of less than 1°C. The device exhibited a common emitter current gain of 20, a maximum collector current of 0.6 A, and a collector base junction breakdown voltage of 25 V.

A 2-D modeling including the effective barrier effect was presented for describing the f_T roll-off at high current density in SiGe DHBT's. The calculated result is confirmed by experimental work. An analytical formula for the base transit time for SiGe base HBT's was presented including the doping grading, the compositional grading, and especially the retarding field effect.

A double layer collector with appropriate profiles was proposed and shown to increase the maximum collector current by 60% without compromising the breakdown voltage.

We analyzed the effect of the conduction band offset in the collector heterojunction in NpN GaAs/Ge/GaAs DHBT's. A modified collector design was proposed to increase the collection efficiency.

II d. Miscellaneous:

Non-alloyed Al contacts were deposited by molecular beam epitaxy on both n- and p-type $In_{0.53}Ga_{0.47}As$ layers prior to air exposure. The contacts were shown to be ohmic, with specific contact resistances in the range of mid 10^{-6} Ω-cm^2 by the transmission line model method. The thermal stability was tested by annealing at temperatures between 350 and 450°C for 30 minutes and at 300°C for 500 hours, and both experiments showed stable specific contact resistances. AuBe contacts to p-$In_{0.53}Ga_{0.35}Al_{0.12}As$ (Be: 5 x10^{18} cm^{-3}) formed by rapid thermal annealing (RTA) were studied and compared with those formed by conventional alloying. Using thermally evaporated AuBe, specific contact resistances in the range of low 10^{-6} Ω-cm^2 were achieved by both methods. However, contacts made by RTA demonstrated good thermal stability while the contacts made by conventional alloying degraded more than one order of magnitude at 250°C for 100 hours.

Considerable modulation ratio was achieved for GaAs multiple quantum well reflector modulators grown on Si by inserting an AlAs/AlGaAs dielectric mirror into the device structure. Modulation ratios of up to 4:1 were attained as the external bias voltage was increased to 9 V. This was achieved by taking advantage of the quantum confined Stark effect and the cavity effects arising from the front surface reflection and that of the embedded mirror.

III. REPRESENTATIVE PAPERS

GaAs Multiple Quantum Well Reflector Modulators Grown on Si.

by

A. Salvador, K. Adomi[+], K. Kishino*, M. S. Ünlü

and H. Morkoç

Coordinated Science Laboratory

and Materials Research Laboratory

University of Illinois at Urbana-Champaign

1101 W. Springfield Avenue, Urbana, Illinois 61801

Abstract

Considerable modulation ratios are achieved for GaAs multiple quantum well reflector modulators grown on Si by inserting an AlAs/AlGaAs dielectric mirror into the device structure. Modulation ratios of up to 51.4 percent is attained as the external bias voltage is increased to 8.5 Volts and the 1C-1HH exciton absorption peak undergoes quantum confined Stark shift. Measurements also indicate that cavity effects arising from the front surface reflection and that of the imbedded dielectric mirror strongly modify the reflectivity spectra.

Sh[illegible] Handotai Co Ltd.

[illegible]

* On leave from Sophia University, [illegible], Japan

COLLECTOR - EMITTER OFFSET VOLTAGE IN HETEROJUNCTION BIPOLAR TRANSISTORS

B. Mazhari, G. B. Gao* and H. Morkoç

Coordinated Science Laboratory and Materials Research Laboratory

University of Illinois at Urbana-Champaign

1101 W. Springfield Avenue

Urbana, IL 61801, USA.

Abstract

Collector-emitter offset voltage in heterojunction bipolar transistors is studied in detail. Based on an in-depth analysis of junction characteristics at zero collector current, a general model for offset voltage applicable to homojunction, single heterojunction and double heterojunction bipolar transistors is obtained. For an abrupt SHBT, the conduction band discontinuity at e-b heterojunction is found to be the main cause of large offset voltages. For DHBT's it is found that even when emitter and collector base junctions are identical in all respects, they will have an offset voltage with a magnitude dependent on the current gain of the transistor. Appropriate grading of emitter-base junction is shown to reduce the offset voltage in HBT's to values obtained in homojunction bipolar transistors.

* On leave from the Beijing Polytechnic University, Reliability Physics Laboratory, Beijing, China

MBE Grown Npn AlGaAs/GaAs Bipolar Transistors with C p-doping by Electron Cyclotron Resonance Source Activated Methane

G. Liu, D. Mui, S. Fang, G. Gao and H. Morkoç

University of Illinois at Urbana-Champaign

Coordinated Science Laboratory and

Materials Research Laboratory

1101 W. Springfield Avenue

Urbana, IL 61801

Abstract

Using an electron cyclotron resonance source in an UHV system, vacuum connected to adjacent molecular beam epitaxy, carbon doping in GaAs was obtained and applied to the b of a heterojunction Npn bipolar transistor. The devices fabricated on the heterostructures grc as described exhibited current gains of about 50. After subjecting the layers to a 700°C/20 n anneal cycle, the newly fabricated devices yielded current gains of about 50 demonstrating tl stability.

UNIFORM JUNCTION TEMPERATURE AlGaAs/GaAs POWER HETEROJUNCTION BIPOLAR TRANSISTORS ON SILICON SUBSTRATES

Guang-bo Gao, Zhi-fang Fan, D.L. Blackburn†, M.S.Ünlü

J. Chen, K. Adomi, H. Morkoç,

University of Illinois at Urbana-Champaign

Coordinated Science Laboratory and

Materials Research Laboratory

1101 W. Springfield Avenue

Urbana, IL 61801

Abstract

AlGaAs/GaAs power heterojunction bipolar transistors on Si substrates exhibiting uniform junction temperature distribution are reported. Owing to a unique device design, the temperature spread across the entire device area is about 1°C. The device exhibits a common emitter current gain of 20, a maximum collector current of 0.6 A and a collector base junction breakdown voltage of 25V.

† **National Institute of Standards and Technology, at Gaithersburg, MD 20899.**

STRAINED LAYER LASERS IN THE InGaAs/GaAs/AlGaAs HETERO-STRUCTURE SYSTEM

H. Morkoç

University of Illinois
Coordinated Science Laboratory and Materials Research Laboratory
1101 West Springfield Avenue
Urbana, Illinois 61801

ABSTRACT

Recent developments in the technology and fundamentals of strained layer epitaxial systems have generated overwhelming interest in the exploitation of such hetero-structures for optical and electronic device applications. This is in part due to the additional degrees of freedom provided for device structures to be tailored for the particular application and in many cases improved performance over what is possible with the lattice matched systems alone. For example, quantum well lasers with strained InGaAs active layers have achieved threshold currents comparable to those with GaAs channels but with much less edge losses due to the smaller surface recombination velocity in InGaAs and very stable power outputs. Reduced threshold currents and increased differential gains are expected to lead to modulation at higher frequencies.

I. INTRODUCTION

With the recently introduced epitaxial growth schemes such as Molecular Beam Epitaxy and Organometallic Vapor Deposition, it has become possible to grow multi-component epitaxial hetero-structures with excellent compositional and thickness control. This precise control, along with UHV in the case of MBE, paved the way for the investigation of growth mechanisms in a previously impossible amount of detail. Armed with an improved understanding of crystal growth, scientists were able to begin investigating strained layer hetero-epitaxy in detail. For SL structures, the constraint of having a lattice matched layer on a suitable substrate is relaxed, up to critical thickness. Material scientists and the device designers were able to choose a stack of various layers on a substrate without worrying about the immediate lattice matching problem. In a sense, an additional degree of freedom is provided for the optimization of the experiment and/or the device structure. The electronic and optical properties such as the band gap can be designed beyond what is already made available by [illegible] quantum wells structures.

Following the early work of Matthews and Blakeslee [1] who primarily concentrated on the materials aspects of the lattice mismatched systems, Osbourn [2] diligently was able to revive the field by pointing out the interesting optical and electrical properties of these systems. The Matthews and Blakeslee work had shown that dislocation free material could be grown up to a critical thickness below which the strain is taken up coherently by the crystal. Osbourn and colleagues, initially with GaAsP and later on with InGaAs and InAsSb, were able to show the advantages to be gained by the exploitation of these strained systems for both devices and [illegible] merit.

GROWTH OF GALLIUM ARSENIDE ON HYDROGEN PASSIVATED Si WITH LOW-TEMPERATURE TREATMENT (~ 600°C)

S.F.Fang, A.Salvador, and H. Morkoç

University of Illinois at Urbana-Champaign

Coordinated Science Laboratory & Material Research Laboratory

1101 W. Springfield Avenue

Urbana, IL 61801

ABSTRACT

Epitaxial growth of GaAs on Si commonly employs a high temperature (> 850°C) oxide desorption step. In this letter, we report the first epitaxial growth of GaAs on Si without the need for this high temperature treatment. This method utilizes a final HF treatment whereby the Si surface dangling bonds are terminated by hydrogen with a resultant (1x1) bulk-like surface structure. Upon medium temperature heat treatment (~500°C), hydrogen leaves the surface leading to the common orthogonal 2x1 surface reconstruction. High quality GaAs epitaxial layers were successfully grown on these 2x1 reconstructed Si surfaces with the pre-growth substrate preparation temperatures of as low as 600°C.

Use of Methane in an Electron Cyclotron Resonance Plasma Source for Carbon Delta-Doping in GaAs Molecular Beam Epitaxy

D. S. L. Mui, [a]K. R. Evans, S. F. Fang, D. Biswas, and H. Morkoc

University of Illinois at Urbana-Champaign
Coordinated Science Laboratory
1101 West Springfield Avenue
Urbana, Illinois 61801

[a]Wright Research and Development Center
Electronic Technology Laboratory (WRDC/EL)
Wright Patterson Air Force Base, Ohio 45433

Abstract

An electron cyclotron resonance (ECR) plasma source has been used with methane gas to perform carbon delta-doping in GaAs grown by molecular beam epitaxy. The ECR plasma source is installed on a chemical vapor deposition chamber which is vacuum connected to a conventional MBE apparatus. Good surface morphologies, high sheet carrier densities ($1\text{-}7\times10^{12}cm^{-2}$), and reasonable hole mobilities (75-110 cm^2/Vs) are obtained.

Analysis of cut-off frequency roll-off at high currents in SiGe double-heterojunction bipolar transistors

Guang-bo Gao, Zhi-fang Fan, and H. Morkoç
University of Illinois at Urbana–Champaign, Coordinated Science Laboratory and Materials Research Laboratory, 1101 West Springfield Avenue, Urbana, Illinois 61801

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Roll-off of the current gain cut-off frequency in *NpN* double-heterojunction bipolar transistors for large collector currents has been analyzed. The analysis includes such effects as the electron barrier formed at the collector base junction due to electron accumulation. Included in this investigation is also lateral electron diffusion before injection into the collector space-charge region at the base-collector heterointerface once the barrier is formed. The available data obtained in SiGe heterojunction bipolar transistors are in good agreement with this model.

It is well known that double-heterojunction bipolar transistors (DHBTs) have advantages such as (a) suppression of hole injection from base into collector in digital switching integrated circuits under saturation conditions, (b) emitter/collector interchangeability that means that the device can work as an emitter up or an emitter down, (c) reduction of the emitter/collector offset voltage, and (d) separate optimization of the base and collector.[1]

AlGaAs/GaAs/AlGaAs, AlInAs/InGaAs/AlInAs, and Si/SiGe/Si DHBTs have been investigated. In particular, $Si/Si_{1-x}Ge_x/Si$ DHBTs have received much attention lately with SiGe as the base. In separate efforts, dc current gains[2] of 5000 and a maximum current gain cut-off frequency[3] (f_T) of 75 GHz have been obtained. However, the current gain and cut-off frequency fall-off in SiGe heterojunction bipolar transistors (HBTs) for large collector currents is faster than that in AlGaAs/GaAs single HBTs and Si BJTs (bipolar junction transistors).

High current gain cut-off frequency at high current densities is very important for integrated circuits such as emitter coupled logic gates with large fan-out, and microwave applications. It is the values of current gain or cut-off frequency at high current densities, not some peak value for low injection levels, that determines the power output level in microwave power transistors and the switching response in circuits with large fan-out. Therefore, a discussion of high current behavior of $Si/Si_{1-x}Ge_x/Si$ DHBTs is imperative and timely.

Tiwari[4] and Yu *et al.*[5] have shown that a retarding potential barrier for the electrons forms at high current densities at the base-collector junction of *NpN* AlGaAs/GaAs/AlGaAs, and Si/SiGe/Si DHBTs, respectively. This barrier leads to an increase in minority-carrier charge storage time in the base and decreases the current gain as well as the current gain cut-off frequency.

Recently, Cottrell and Yu[6] developed an analytical model for calculating the aforementioned barrier height. Barrier height causes saturation of the transconductance, early onset of high level injection in the base, and rapid decrease of f_T for $J_c > J_K$, with J_K being the Kirk effect limited current density,[7] in both *NpN* and *PnP* SiGe base DHBTs.

In this letter, we present an analysis which includes an additional base delay term precipitated by the potential barrier at the base collector junction in DHBTs structures at high currents. Using this added base delay time and lateral diffusion of carriers [dubbed the two-dimensional (2D) effect], we can elaborate on the mechanisms for the observed rapid roll-off of the cut-off frequency in DHBTs at high currents. This analysis has been applied to the available experimental data for $Si/Si_{1-x}Ge_x/Si$ DHBTs with good agreement.

In homojunction transistors and wide gap emitter single HBTs, when $J_c > J_K$ the base-collector (*b-c*) junction shifts into the collector space-charge region, while the original base-collector (*b-c*) junction becomes forward biased. As a result more holes are injected into the collector from the base to compensate the mobile electron charge, resulting in the formation of a current induced base, W_{CIB}.

The picture is quite different for DHBTs having a sizable valence-band discontinuity in the *b-c* junction as in the case of SiGe/Si devices, see Fig. 1. This valence-band discontinuity suppresses the hole injection into the collector as electron injection is increased. These mobile electrons together with localized holes form a dipole layer and in turn a field opposite to that caused by the base-collector applied bias. This can be simply thought of as a barrier at the heterojunction against electrons giving rise to increased minority-carrier storage in the base. The build up of excess carriers under the active device area causes a lateral diffusion before injection into the collector which is the basis for the 2D effect. This essentially increases the effective area through which the current flows. This concept was initially introduced by Van der Ziel and Agouridis[8] to explain the Kirk effect. Obviously the barrier and 2D effects take place simultaneously and before the onset of the Kirk effect.

Taking into account the 2D effect, the cut-off frequency f_T at $I_c > I_K$ is[9]

$$f_T^{-1} = 2\pi\left(\frac{kT}{qI_c}C_{TE} + \frac{W_B^2}{nD_{nB}} + \frac{W_C}{2V_s} + r_c C_{TC} + \frac{(I_c/I_K - 1)^2 S_E^2}{4nD_{nB}}\right). \quad (1)$$

At high currents, Eq. (1) reduces to

MODFETs REACH NEW HEIGHTS WITH CUT-OFF FREQUENCIES OVER 400 GHz

by
Hadis Morkoç
University of Illinois
Material Research Laboratory and
Coordinated Science Laboratory
1101 W. Springfield Avenue
Urbana, Illinois 61801

ABSTRACT

Field Effect Transistors based on the heterojunction concept progressed over the past decade to the point where their presence is making waves in high speed digital (functional) circuits, and high performance millimeter wave low noise and power amplifiers. Device performance has recorded tremendous progress with switching delays under 5 ps, frequency division up to 26 GHz, current gain cut-off frequencies of about 250 GHz, and maximum oscillation frequencies in excess of 400 GHz. Although device performance alone does not automatically lead to blazing speed circuit performance, the rapid development in devices precipitated a flurry of activity to push back the fringes of high performance circuits. This paper will discuss the most recent developments in Modulation Doped FETs (MODFETs) based on compound semiconductor technology.

A Safety System for Gas Source Molecular Beam Epitaxy

by

Dhrubes Biswas and Hadis Morkoç

University of Illinois

Materials Research Laboratory and Coordinated Science Laboratory

104 S. Goodwin

Urbana, IL 61801

ABSTRACT

Gas Source Molecular Beam Epitaxy (GSMBE) is one of the newest development in epitaxial growth technology wherein the group V sources such as arsine and phosphine are gaseous and in the form of hydrides while the Group III sources such as indium, aluminum, gallium are all solids. However, the gases involved are very hazardous, extremely toxic, highly inflammable and explosive at elevated temperatures. Adequate care must be taken for the safe use of these gases so that this attractive technique can be properly utilized. This paper discusses the salient safety features of one such GSMBE (installed in the Epicenter at the University of Illinois) consisting of a gas delivery system with its robust piping assembly, gas manifold and a scrubber. The system is integrated with a Multiple Point Toxic Gas Monitor (MPTGM) acting as the central alarm command system based on the concept of fail safe total safety. This alarm system is equipped with audio-visual alarms for a variety of monitored conditions and interlocks for automatic shutdown. A well designed air flow pattern has been incorporated to provide good air quality in the laboratory and in the gas storage facility. Additionally a set of good laboratory practices ensured by administrative and personal control are instituted to reduce the hazards to an acceptable risk level.

c

Electron cyclotron resonance assisted low temperature ultrahigh vacuum chemical vapor deposition of Si using silane

D. S. L. Mui, S. F. Fang, and H. Morkoç
University of Illinois, Materials Research Laboratory and Coordinated Science Laboratory, 1101 West Springfield Ave., Urbana, Illinois 61801

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Deposition of single-crystal homoepitaxial Si at low temperatures assisted by an electron cyclotron resonance (ECR) generated plasma using a mixture of helium and silane gases in an ultrahigh vacuum chemical vapor deposition (UHVCVD) chamber is reported. The pure silane gas is introduced into the UHVCVD chamber through a showerhead located above the substrate and is excited indirectly by the helium plasma brought downstream from the ECR chamber. At a chamber pressure of 5×10^{-4} Torr epitaxial single-crystal Si can be obtained at a substrate temperature T_s as low as 400 °C. Variation of the deposition rate with respect to the microwave power, P_μ, at different temperatures suggests a hydrogen inhibited deposition process at low temperatures. At 460 °C the deposition rate increases with P_μ below 60 W and saturates for P_μ beyond this value. On the other hand, at a T_s of 610 °C, this saturation effect is not observed and the deposition rate increases linearly with P_μ. In this plasma-assisted deposition, a much reduced T_s dependence of the deposition rate is observed. We have used this deposition technique successfully in obtaining a Si_3N_4/(epi-Si) metal-insulator-semiconductor capacitor with an interface trap density of 2×10^{10} eV^{-1} cm^{-2} as determined by the conductance method.

Uniformity and abrupt doping profiles necessitated by large scale integration and ever decreasing device dimensions have led to the exploration of deposition of Si at very low temperatures and under ultrahigh vacuum conditions.[1-3] At high pressures, especially in a hot-wall reactor, where deposition takes place through the homogeneous decomposition of silane, it was found that depletion of the source gas around the growing surface led to nonuniform deposition of the epitaxial layer. In a cold-wall chamber and when low pressures are used, due to the steep temperature gradient of the vapor phase at the growing surface, the deposition becomes surface dependent and a much more uniform deposition is achieved. It was found that[4] the deposition of Si under these conditions is driven by silane surface diffusion limited by surface hydrogen desorption. Depending on the substrate temperature, which determines the hydrogen desorption rate, two different activation energies were obtained. Above 650 °C an activation energy of 33 kcal/mol is measured, while below this temperature it increases to 52 kcal/mol.[5]

Although sharper interfaces result from low temperature epitaxy,[1-3] the incorporation of O and C is enhanced. As a result the deposition chamber must be free, to the extent possible, of these contaminants. This necessitates the employment of ultrahigh vacuum techniques.[1,2] In addition, the use of plasma[1,3] and ultraviolet light[6] as excitation sources during deposition can increase the reduced deposition rates for low substrate temperatures. In this letter an ultrahigh vacuum chemical vapor deposition (UHVCVD) system where an electron cyclotron resonance (ECR) source is employed for plasma assisted deposition of single-crystal homoepitaxial Si using helium and silane gases is described. The crystal quality of the epitaxial layer is monitored by reflection high energy electron deflection (RHEED) and the thickness measured by a step height profiler. The deposition rate dependence on the microwave power and substrate temperatures is reported. We have used this deposition technique successfully in obtaining a Si_3N_4/(epi-Si) metal-insulator-semiconductor (MIS) capacitor with very low interface trap density.

The cross-sectional diagram of the UHVCVD chamber is shown in Fig. 1. Briefly, it is a stainless-steel cold-wall chamber consisting of an ECR source mounted on an 8 in flange putting the aperture of the source about 12 in. above the substrate. The chamber is pumped by an ion and turbomolecular pump combination achieving a base pressure of 1×10^{-9} Torr. Helium is introduced at the top of the ECR chamber where the plasma is generated. Helium metastables thus created have extremely long mean free paths (tens of cm) in the pressure range (mid-10^{-4} Torr) employed. This allows for the positioning of the substrate stage far away from the ECR chamber where the plasma is localized. Silane is introduced into the CVD chamber through a showerhead located halfway between the aperture of the ECR chamber and the substrate. The helium metastables impinging on the surface assist in the complex process of surface heterogeneous pyrolysis of silane and the hydrogen desorption from the surface.

The Si substrates used for the study of the epitaxial growth were *p*-doped (100) misoriented 4° toward the (001) plane. The substrates were etched in a 1:10 HF:H_2O solution followed by a 5:3:3 HCL:H_2O_2:H_2O solution. This procedure was repeated three times to remove the contaminants on the Si surface. The substrates were then etched in the same HF solution for 1 min before rinsing in deionized water. The substrates were then blown dry in dry N_2 and immediately loaded into the introchamber. After the substrates had been loaded into the vacuum system, they showed a (1×1) RHEED reconstruction, indicating a hydrogen passivated surface.[7] The shutter in the UHVCVD

Effect of collector-base valence-band discontinuity on Kirk effect in double heterojunction bipolar transistors.

B. Mazhari and H. Morkoç

Coordinated Science Laboratory and Materials Research Laboratory

University of Illinois at Urbana-Champaign

1101 W. Springfield Avenue

Urbana, IL 61801, USA.

Abstract

The effect of valence-band discontinuity at the collector base heterojunction on the current gain and base charge storage is modelled. It is shown that the onset of Kirk effect is accompanied by a sharp drop in the current gain and f_t due to the formation of a potential barrier. The variation of barrier height with collector current density is determined and its effect on current gain and base transit time described. The results discussed here are applicable to Si/SiGe double heterojunction bipolar transistors.

Base Transit Time for SiGe-Base Heterojunction Bipolar Transistors

Guang-bo Gao and Hadis. Morkoç

University of Illinois at Urbana-Champaign

Coordinated Science Laboratory and

Materials Research Laboratory

1101 W. Springfield Avenue

Urbana, IL 61801

Abstract

The base transit time expressions for SiGe base heterojunction bipolar transistors are presented including the accelerating field effects due to the base bandgap grading and the doping grading as well as the retarding field (opposing drift field) effect from the graded boron profile down towards the emitter. It is found that the retarding field exhibit 40 - 80% contribution to the base transit time, depending on the boron concentration near the emitter. The results of base transit time from these analytic expressions are unambiguously supported by the published simulation data.

PROPERTIES OF SI_3N_4/SI_xGE_{1-x} METAL INSULATOR SEMICONDUCTOR CAPACITORS

Abstract: The density of fast interface states was studied in $Si_3N_4/Si_{0.8}Ge_{0.2}$ Metal-Insulator-Semiconductor (MIS) capacitors. The interface state density does not appear to be strongly affected by the presence of a thin Si interlayer between the nitride and SiGe alloy. This is contrast to the results when SiO_2 is used as the insulator material in similiar structures.

Electrical characteristics of $Si_3N_4/Si/GaAs$ metal–insulator–semiconductor capacitor

D. S. L. Mui, H. Liaw, A. L. Demirel, S. Strite, and H. Morkoç

University of Illinois at Urbana–Champaign

Coordinated Science Laboratory

and

Materials Research Laboratory

1101 W. Springfield Ave.

Urbana, IL 61801

Abstract

We report on the electrical characteristics of as-grown $Si_3N_4/Si/n$–GaAs metal–insulator–semiconductor capacitor (MIS). The GaAs layer is grown by molecular beam epitaxy and both the Si_3N_4 and the 10 Å Si layers are deposited using silane in a vacuum connected ultrahigh vacuum chemical vapor deposition chamber driven by an electron cyclotron resonance (ECR) plasma source. Fowler–Nordheim tunneling through the barrier is observed at high fields for the first time in the Si_3N_4 films. Hole inversion of the n–GaAs layer is clearly seen in the quasi–static capacitance–voltage curve. Despite past reports on the presence of a large amount of bulk traps in Si_3N_4, a hysteresis of less than 100 meV is observed in the high–frequency capacitance–voltage curves with a bias voltage swing of ± 4V. From the high–low capacitance method we estimated the interface trap density to be of the order of 4×10^{11} eV^{-1} cm^{-2} and from the conductance measurements we found a value of 10^{12} eV^{-1} cm^{-2}.

Molecular-Beam-Epitaxy-Deposited Nonalloyed Al Contacts to n-type and p-type InGaAs

T.C. Shen, Z.F. Fan, G.B. Gao, H. Morkoç and A. Rockett

The Coordinated Science Laboratory and The Materials Research Laboratory

University of Illinois, 1101 W. Springfield Ave., Urbana, IL 61801

Nonalloyed Al contacts were deposited by molecular beam epitaxy on both n- and p-type $In_{0.53}Ga_{0.47}As$ layers prior to air exposure. These were shown to be ohmic, with specific contact resistances in the range of 1.7 to 5.0 $\mu\Omega\ cm^2$ by the transmission line model method. The thermal stability of these contacts was tested by annealing at temperatures between 350 and 450°C for 30 min and at 300°C for 500 hrs. Both experiments showed stable specific contact resistances.

SITE SYMMETRY APPROACH TO LATTICE DYNAMICS OF SEMICONDUCTOR SUPERLATTICES

B. H. Bairamov, R. A. Evarestov, Yu. E. Kitaev
A. F. Ioffe Physical-Technical Institute, Leningrad 194021, USSR

E. Jahne
Zentralinstitut fur Elektronenphysik, Akademie der Wissenschaften der DDR,
Berlin, DDR - 1086

M. Delaney, T. A. Gant*, M. V. Klein, D. Levi, J. Klem**+, H. Morkoc**
Department of Physics and Materials Research Laboratory
University of Illinois at Urbana-Champaign, (UIUC),
1110 W. Green Street, Urbana, IL 61801, USA

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We present here the site symmetry approach to lattice dynamics of superlattices which permits us to connect by symmetry the local atomic displacements and normal vibrational modes over the entire Brillouin zone. The atomic arrangements over the Wyckoff positions for $(GaAs)_m(AlAs)_n$ and $(Si)_m(Ge)_n$ superlattices oriented along [001] for different sets of m and n are determined. We obtained the phonon symmetry for $k \neq 0$ using the developed theory of the band representations of space groups and derived the selection rules for the first and second-order infrared and Raman spectra. Raman spectra obtained for the $(GaAs)_7(AlAs)_{18}$ and $(Si)_3(Ge)_3$ superlattices are interpreted in terms of the presented theory.

1. Introduction

Success in growing $(GaAs)_m(AlAs)_n$ and $(Si)_m(Ge)_n$ superlattices (SL's) with varying primitive cell, consisting of m and n monolayers of GaAs and AlAs (Si and Ge), respectively, by molecular beam epitaxy have been recently demonstrated by several groups [1-19]. Raman scattering techniques have proved to be an excellent tool for studing electronic properties and lattice dynamics of these SL's and for obtaining a detailed information on crystalline quality and strain field distribution. To analyze the experimental data on first and second-order Raman scattering we have to study the SL's phonon symmetry and the corresponding selection rules for Raman scattering.

In SL's the new periodicity has consequences both in a reduction of point group symmetry with respect to constituent bulk materials and in an increase of the number of atoms per primitive cell resulting in a new space group symmetry. The $(GaAs)_m(AlAs)_n$ SL's grown along [001] constitute two single crystal families with space groups D^5_{2d} (m+n=2k) and D^9_{2d} (m+n=2k+1) depending on even or odd total number of monolayers (m+n) per primitive cell [20]. The $(Si)_m(Ge)_n$ [001] SL's constitute five single crystal families with symmetries D^5_{2d} (m+n=4k; m,n odd); D^9_{2d} (m+n=4k+2; m,n odd); D^5_{2h} (m+n=4k; m,n even); D^{28}_{2h} (m+n=4k+2; m,n even) and D^{19}_{4h} (m+n=2k+1) [10].

The atomic arrangement over the Wyckoff positions in the primitive cell for the SL's is governed by the specific values of m and n for each SL-family being a series of single crystals with the same space group. Thus, in terms of symmetry SL's belonging to the same family are distinct crystals differing by the arrangement of atoms in the primitive cell. We have derived general formulae for the atomic arrangements for the SL's in question [17-19]. To obtain

* Present address: Division of Physics, National Research Council, Ottawa K1aOR6, Canada

** Coordinated Science Laboratory, UIUC

+ Present address: Sandia National Laboratory, Albuquerque NM 87185-5800, USA

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AuBe OHMIC CONTACTS TO *p*-InGaAlAs FORMED BY RAPID THERMAL ANNEALING

Abstract

AuBe ohmic contacts to *p*-$In_{0.53}Ga_{0.35}Al_{0.12}As$ (Be: $5x10^{18}cm^{-3}$) formed by rapid thermal annealing (RTA) have been studied and compared with those formed by conventional alloying. Using thermally evaporated AuBe, specific contact resistances in the low $\mu\Omega$-cm^2 range have been achieved by both methods. However, contacts made by RTA demonstrated good thermal stability while the contacts by conventional alloying degraded more than one order of magnitude at 250°C for 100 hours.

DOUBLE LAYER COLLECTOR FOR HETEROJUNCTION BIPOLAR TRANSISTORS

G.B. Gao†, M.S. Ünlü, J. Chen, B. Mazhari

K. Adomi, G.X. Liu, Z.F. Fan and H. Morkoç,

University of Illinois at Urbana-Champaign

Coordinated Science Laboratory and

Materials Research Laboratory

1101 W. Springfield Avenue

Urbana, IL 61801

Abstract

A double layer collector with appropriate profiles has been shown to increase the maximum collector current without compromising the breakdown voltage. Power HBT's with emitter ballasting resistors were grown on Si and GaAs substrates and fabricated to test the various collector designs. A maximum collector current density of 3.5×10^4 A/cm^2 and a collector-emitter breakdown voltage of 28 V were realized for a double layer collector HBT with ten 5×25 μm^2 emitter fingers. This high current density obtained by the novel collector design represents a 60% improvement over the conventional HBT with slightly higher breakdown voltage which is in agreement with predictions.

† On leave from the Beijing Poly[illegible]ersity, Reliability Physics Laboratory, Beijing, China.

Reduction of Outdiffusion at the Ge/GaAs (100) Interface by Low Temperature Growth

A. L. Demirel, S. Strite, A. Agarwal, M. S. Ünlü, H. Morkoç and A. Rockett

The Coordinated Science Laboratory and The Materials Research Laboratory

University of Illinois, 1101 W. Springfield Avenue, Urbana, IL 61801

ABSTRACT

Ga outdiffusion into Ge layers grown epitaxially by molecular beam epitaxy (MBE) was observed by secondary ion mass spectroscopy (SIMS), X-ray photoemission spectroscopy (XPS), capacitance-voltage, and temperature dependent Hall-effect measurements. Films were initially grown at low rates (0.03-0.04 nm/s) and low temperatures (150-300°C) on GaAs buffer layers on GaAs (100) substrates. The temperature and rate were then increased to 500°C and 0.1 nm/s. The amount of Ga outdiffusion was greatest for films initially grown at 300°C. No direct evidence of As outdiffusion at any temperature or Ga outdiffusion for initiation temperatures below 300°C was found. Hall-effect measurements showed higher hole concentrations and greater levels of compensation in films initiated at 300°C, consistent with outdiffusion of both Ga and As at this temperature. No degradation in the electrical characteristics of Ge-GaAs diodes was observed when the initial Ge growth temperature was reduced from 300°C to 200°C.

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Figures to Follow

A collector design study for GaAs/Ge/GaAs double heterojunction bipolar transistors

S. Strite, M. S. Ünlü, A. L. Demirel, D. S. L. Mui, and H. Morkoç

Materials Research Laboratory and Coordinated Science Laboratory

1101 W. Springfield Avenue

University of Illinois at Urbana-Champaign, Urbana, IL 61801

Abstract

We analyze the effect of the conduction band offset in the collector heterojunction in NpN GaAs/Ge/GaAs double heterojunction bipolar transistors (DHBT). Despite excellent diode characteristics in both the emitter-base and base-collector diodes, the GaAs/Ge/GaAs DHBTs exhibit relatively low common-emitter dc current gains and a lack of collector current saturation with increasing collector-emitter bias. Simulations indicate that this is at least in part attributable to a reduction in collection efficiency caused by the large collector-base conduction band offset (0.26 eV) between the Ge base and the GaAs collector. A modified collector design which incorporates higher doping in the region of the GaAs conduction band spike is proposed to decrease the width of the barrier to electrons. Simulations predict that the collection efficiency will be greatly improved with the incorporation of a modified collector.

Recent Developments in Ohmic Contacts for III-V Compound Semiconductors

T.C. Shen, G.B. Gao, and H. Morkoç
University of Illinois
Materials Research Laboratory
and Coordinated Science Laboratory
1101 West Springfield Avenue
Urbana, IL 61801

Abstract

Recent advances in the technology and understanding of ohmic contacts for a variety of III-V compound semiconductor material systems are reviewed. Special attention is focused on factors and critical issues involved in making low resistance and reliable ohmic contacts. The solid-phase regrowth mechanisms of key metallization systems are described. In addition, special techniques to improve the ohmic contacts are discussed. Finally, the reliability issues of ohmic contacts are addressed.

Minority charge storage characteristics of HBT in saturation

B. Mazhari and H. Morkoç

Coordinated Science Laboratory and Materials Research Laboratory

University of Illinois at Urbana-Champaign

1101 W. Springfield Avenue

Urbana, IL 61801, USA.

Abstract

An analytical model is developed to study the minority charge storage characteristics of heterojunction bipolar transistors in saturation. The model is used to compare the performance of single and double heterojunction bipolar transistors in a Schottky coupled I^2L logic circuit. A DHBT with a weak collector-base heterojunction is proposed as an optimum structure.

IV. LIST OF PAPERS RESULTING FROM AFOSR FUNDING

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