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EXPERIMENTAL EVALUATION OF INCORPORATING DIGITAL AND ANALOG INTEGRATED CIRCUIT DIE ON A COMMON SUBSTRATE UTILIZING SILICON-HYBRID WAFER-SCALE INTEGRATION TECHNOLOGY

THESIS

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Wright-Patterson Air Force Base, Ohio

AFIT/GE/ENG/92M-07

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THESIS

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Philip C. Reamy, Captain, USAF

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Preface

The purpose of this research was to evaluate the use of Wafer Scale Integration (WSI) techniques with analog circuits. Although most WSI research has focused on digital applications, the potential benefit of employing these techniques in systems containing analog circuits, for example, spacecraft and avionics systems, is significant.

Initial investigations in this research effort were focused at refining the WSI fabrication process developed through previous research. These preliminary studies investigated the potential application of alternative techniques and materials. While the procedure used in fabricating the actual test samples did produce repeatable results, problems encountered in the processing limited the numbers and types of testable samples. The interconnects which were evaluated indicated that the design was promising for digital CMOS applications, which are tolerant of low-level signal attenuation and can be characterized with high impedance loads. However, continued research is necessary to improve the interconnect design to a level suitable for analog applications.

I would like to express my appreciation for those whose efforts aided in the completion of this thesis. I would like to thank my thesis advisor, Lt Col Edward S. Kolesar. His guidance and suggestions throughout this research effort were motivational. In addition, Captain Mark Mehalic's assistance in design and submission of the test circuits for fabrication were invaluable. I also wish to thank Captain Tom Jenkins for his advise and assistance in the laboratory and throughout this research effort. I would like to express my appreciation for the assistance given by Mr. Donald Smith and Mr. William Trop of the AFIT Electronics and Materials Cooperative Laboratory. Additionally, I thank the members of the devices sequence for all of their support throughout this effort.

I would like to thank the Phillips Laboratory for the support and funds which made this research effort possible. In addition, I greatly appreciate the technical assistance and materials support from Mr. Herbert Newhouse and Amoco Chemical Company.

Finally, I cannot fully express my gratitude to my family for their unselfish support. I thank my wife, Kathy, for her patience and sacrifice (not to mention her typing skills), and my children whose boundless energy was inspirational. Lastly, I dedicate this thesis to the memory of my father, Richard Reamy Sr., who inspired my career in engineering, and who taught me so much more.

Phil Reamy

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Abstract

The objective of this research effort was to investigate the implementation of analog circuits in a WSI system. A test circuit composed of analog and digital subsystems was designed and tested through simulation. IC die containing this test circuit were utilized in the WSI system fabrication. Preliminary investigations were conducted to evaluate the potential improvements to the IC die mounting procedure, a key step in fabricating functional WSI systems. These investigations demonstrated a procedure which produced repeatable results in achieving acceptable planarization of IC die and host substrate surfaces. These investigations also demonstrated the successful application of Teflon® spray coating as a barrier material on the IC die mounting reference flat. An evaluation of candidate polyimides to be used as the interlevel dielectric in the WSI systems was also performed. Test samples for each of the WSI configurations were fabricated and tested for interconnect continuity. Additional electrical characterization measurements were conducted on two of the test samples.

The original goal of the research was to evaluate interconnect networks for three WSI configurations. However, because of difficulties in processing, the only useful test articles produced were the single IC die WSI configurations.

Specifically, difficulties with the IC die adhesive viscosity resulted in uneven and incomplete filling of the regions between the IC die and host substrate in the WSI assembly. These void regions resulted in insufficient planarization by the polyimide coating and subsequent fractures in the aluminum interconnects.

Electrical evaluation tests focused on parametric studies of interconnects on the single IC die test samples. With high impedance loads, these interconnects demonstrated minimal attenuation and propagation delays at frequencies up to 10 MHz. Therefore, these interconnects would be suitable for CMOS digital applications. These interconnects did demonstrate significant attenuation in the presence of low impedance loads.

Further research is recommended in the identification and evaluation of alternative IC die mounting adhesives. Critical characteristics of the IC die mount adhesive include: high processing temperature limitations, high bond strength, consistent viscosity during cure, and low voiding. In addition, investigations of alternative dielectric materials and processing techniques are recommended for application in further research. Research in the metallization processing is also recommended to characterize the interconnect failure mechanisms and to identify alternative processing techniques.

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I. Introduction

Background

Wafer scale integration (WSI) refers to a family of technologies which packages integrated circuits (ICs) to efficiently utilize the available surface area of a host silicon wafer substrate. These technologies offer substantial improvements in size, weight, power consumption, and operating speeds compared to conventional printed circuit board (PCB) systems. The space-utilization aspect of WSI technology is critical to many applications in commercial and military systems. Aircraft avionic systems are a prime example. As avionic systems become computationally intensive, the ability to pack more circuitry into a smaller volume is required. In spacecraft, the ability to reduce power consumption pays dividends by reducing the size of the power support systems. Achieving weight reductions of the microelectronic and power systems results in substantial launch cost reductions. WSI is a potential technology for achieving these reductions.

Current WSI programs focus on digital systems. WSI techniques have limited implementations involving analog circuits. However, the example systems cited above typically interface with analog devices or transducers. That is, aircraft avionic and spacecraft control systems routinely process analog sensor signals as inputs, and they correspondingly generate control signals to analog actuators. To maximize the payoffs of WSI, the ability to integrate analog devices and signals into a WSI system is critical. An investigation of implementing analog devices in WSI is necessary to answer questions concerning the capabilities of such systems.

Problem Statement

The purpose of this research effort is to investigate the implementation of analog circuits in a WSI system. This thesis addresses the feasibility of implementing a mixed digital and analog circuit, the special fabrication or design techniques required, and the corresponding electrical performance measured from the WSI circuit. This investigation includes a comparison of the different WSI fabrication technologies in terms of yield (in a limited sense), ease of fabrication, and electrical performance. The intended outcome of this effort is an evaluation of the performance of a combined digital and analog system implemented using WSI techniques.

Scope

This project continues the research accomplished by previous Air Force Institute of Technology (AFIT) thesis students (10,21,24,39). The focus of this research is to identify an appropriate WSI fabrication technique for implementing a hybrid analog and digital circuit. The goal of the preliminary test and evaluation program is to improve the IC die mounting procedure, reduce the fabrication process complexity, and produce a more planar wafer-to-die transition region. Compatibility of candidate polyimide dielectric materials, photolithography, and metallization processing were also investigated.

Test and evaluation of the fabricated circuits in this research effort focused on measuring certain electrical characteristics of the interconnects. Interconnect attenuation, crosstalk and coupling have a greater potential impact on analog signals compared to digital signals. These measurements were used to evaluate the effectiveness of the WSI techniques in implementing the candidate digital and analog circuit.

Assumptions

This research effort assumes that the process and material recommendations of previous AFIT researchers provides a sound foundation for the WSI process used in this project (10,21,24,39). The qualified success reported from the earlier efforts justifies this assumption. Refinements to this fabrication process focus on investigating alternative materials and processing techniques recommended by the previous researchers to improve interconnect yield.

It is also assumed that the IC die fabricated by the Metal-Oxide Semiconductor Implementation System (MOSIS) using the same design are functionally identical. Therefore, the functionality of the IC design used in this effort can be verified through the test and evaluation of a packaged control chip. Given that the design is verified, the functionality of additional circuits fabricated using the WSI techniques is assumed once the continuity of the WSI interconnects is demonstrated. This assumption is made because it is impractical to completely measure the functionality of the unpackaged WSI circuits with the limited testing resources available.

The final assumption is that the processing, test equipment, and materials required to perform this research are available at the appropriate times. Essential equipment located at AFIT has been identified and evaluated as being suitable to perform this research.

Approach

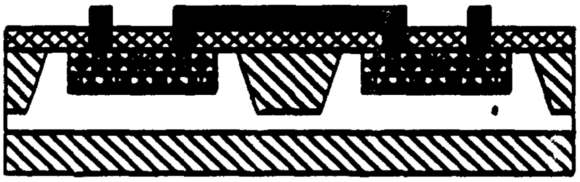
The research begins with preliminary testing to verify the basic process developed by previous AFIT researchers and to evaluate recommended alternatives. These investigations focus on the IC die mounting procedure and the selection of a dielectric material and patterning process.

Next, a candidate electrical system is designed which contains a number of well-defined digital and analog subsystems with the required subsystem interconnections. The investigation of different WSI techniques focuses on four configurations, as illustrated in Figure 1.1. The first configuration, shown in Figure 1.1(a), consists of a system fabricated entirely by MOSIS, including the subsystem interconnects and IC die packaging. This configuration serves as a control circuit for comparison with those fabricated using WSI processes. The second configuration begins with a MOSIS IC die containing all of the subsystems with no subsystem interconnects. After the subsystems are individually tested, functional elements are interconnected with a metallization process to produce a working circuit. As Figure 1.1(b) illustrates, discrete IC die planarization is not a critical issue for this method because the entire circuit resides on a single IC die.

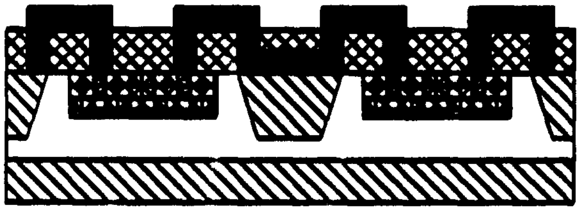
To produce the two multichip hybrid WSI configurations, four MOSIS-fabricated IC die, identical to the second IC die described above, are mounted into a host silicon wafer substrate. Two different interconnect techniques are utilized: patterned overlay hybrid WSI and patterned substrate hybrid WSI.

(a) Control circuit

(b) Patterned overlay monolithic circuit



(c) Patterned overlay hybrid circuit



(d) Patterned substrate hybrid circuit

Legend

Die ▩ Dielectric ▦ Metal ●

Epoxy ○ Substrate ▨

Figure 1.1. Cross-sectional views of the WSI configurations to be experimentally evaluated.

A cross-sectional view of a patterned overlay wafer is depicted in Figure 1.1(c). After the IC die are mounted in the host wafer, a planarizing dielectric layer is deposited on the surface of the host wafer and die. Vias to input and output pads are created, and the metal interconnects are patterned on the dielectric's surface. Because the aluminum interconnects are on a dielectric surface, incomplete surface planarization may lead to interconnect failures.

An alternative method, the patterned substrate hybrid WSI, is illustrated in Figure 1.1(d). In this method, a metallization layer is deposited and patterned directly on the host wafer's surface. The planarizing dielectric is then applied, and the vias are created to the IC die contact pads and aluminum connection points. The metal links across the transition regions are intentionally kept short to provide the necessary connections. By depositing the majority of the required interconnect lengths on the host wafer's planar surface, the possibility of interconnect failure should be reduced.

Test and evaluation during assembly focuses on characterizing the planarity of the assembly, using the stylus profilometer to perform the measurements. In the hybrid WSI fabrication process, planarity measurements are accomplished after the IC die bonding step. The surface profile is also measured for the hybrid circuits and the second monolithic configuration after the dielectric is applied and cured. These measurements are used to predict the capability for fabricating successful interconnects.

Electrical test and evaluation focuses on measuring a common set of parameters for comparison of the different configurations. The first step is verification of the circuit functions. Other parameters that are measured include: signal propagation delays, attenuation, crosstalk and coupling, as well as the affect of varying clock rates.

Presentation

This report documents this research effort and presents conclusions and recommendations for further research. Chapter II reviews the developing requirement for WSI technologies and research concerning the development of WSI fabrication processes. Based on the results of this research, a fabrication process for this research effort is proposed. Chapter III presents the design specification for the mixed analog/digital integrated circuit used in this effort. This chapter also documents the design process and the resulting IC layout. Procedures for implementing the proposed process with this IC and evaluating the electrical characteristics of the resulting circuits are outlined in Chapter IV. Detailed results of this fabrication process and test procedure are presented in Chapter V, followed by conclusions and recommendations for future research in Chapter VI.

II. Literature Review

Wafer scale integration (WSI) refers to a family of technologies which package integrated circuits (ICs) to efficiently cover the surface area of a host substrate (typically a silicon wafer). These technologies offer substantial improvements in size, weight, power consumption, and operating speeds compared to the IC systems that are common today (22:1). However, issues of yield, thermal management, packaging and electrical performance have yet to be fully resolved, which has prevented the full realization of WSI. The intent of this chapter is to provide an overview of the evolving requirement for WSI and a discussion of two approaches used to implement it. An explanation of the fabrication process for realizing hybrid WSI is provided, which focuses on the results of related research efforts that have used different materials and techniques. The summary outlines the materials and techniques selected for this thesis.

Background

Interest and research in WSI has fluctuated over the past 25 years. It was initially pursued in the late 1960s by Texas Instruments as a possible solution to the low yield associated with early silicon integrated circuits (25:62). However, these early attempts at implementing WSI resulted in a further yield reduction, while the silicon monolithic IC fabrication technology rapidly evolved to satisfy industry needs (25:62). That is, individual IC design and fabrication research succeeded in reducing the minimum feature size, from 20 microns in the early 1960s, to 0.5 microns today. Thus, with relatively small increases in IC die size, complexities have correspondingly increased from discrete devices to those with approximately 100,000 gates per die over the same period of time, while computational speed has increased by a factor of 100 with the passage of each decade (13:9). Until just recently, all of this success has acted to hinder interest in seriously pursuing WSI research.

Today, however, there are fundamental limitations associated with the silicon monolithic IC fabrication technique. The minimum feature size that can be achieved is on the order of 0.2 microns; current commercial technology is only a factor of two to four times larger than this limit, and rapidly converging upon it (34:22). Also, conventional packaging is still required, which degrades the overall active device density of the system. In current systems, the ICs are individually packaged and interconnected on PCBs. Minimum pin spacing in conventional IC packaging technologies increases the area required for an IC to be approximately two to ten times larger than the actual active device area. Because minimum line widths are on the order of 300 microns for PCBs, the space used to route interconnects, which contain no active elements, is quite significant (34:17). This "wasted" space translates into larger and more massive systems with limited electrical performance (24:Sec 1,2). In addition, the propagation delay associated with PCB interconnects limits the maximum operating speeds which can be achieved to less than 100 MHz (36:22).

A new technology is needed to continue the advances achieved in microelectronics over the past two decades. One possibility is wafer scale integration (WSI). Silicon WSI does not attack the problem by further reducing device feature size; instead, the goal is to increase the size of the overall IC, ultimately utilizing an entire silicon wafer as a single IC. Line widths in conventional ICs are typically on the order of 2-3 microns, and multilevel interconnects are easily achievable. With the WSI technology, devices will be closer together, which will reduce signal transit times. Thus, WSI purports to increase active device density and switching speeds for a given system (24:Sec 1,1-2).

In WSI, the electrical circuits are fabricated using the same processes currently used to produce discrete IC die which are common today. Although it might seem that WSI could be developed by simply increasing the overall size of a particular IC design, factors of yield and cost effectiveness represent significant barriers (40:23). When fabricating an IC, a certain number of failures are anticipated on each wafer, and these failures occur at random locations on the wafer's surface. These failures may be caused by point defects in the substrate's crystal structure or by a variety of fabrication failure mechanisms. In current IC fabrication, the IC die size is limited to allow a large number of duplicate circuits to be realized on each wafer. Certain defects may only affect the IC die in which they occur. Those IC die are identified through electrical performance testing and discarded. The remaining IC die are separated from the wafer and packaged for use. Cost effective yields are routinely achieved for these smaller IC die.

One simple model of IC die yield predicts an exponential decay in yield as the IC die area increases. This first order approximation is a function of the average number of critical defects per unit area and the number of photolithographic mask levels required (38:435). That is,

$$Y = \exp(-NDA) \tag{2.1}$$

where

Y is the IC die yield
N is the number of mask levels
D is the critical defect density
A is the area of the IC die.

Figure 2.1 illustrates the expected yield for a ten mask process with a defect density of 0.1 defects/cm^2. Typical IC die sizes are between 1 and 10 mm on a side. It should be

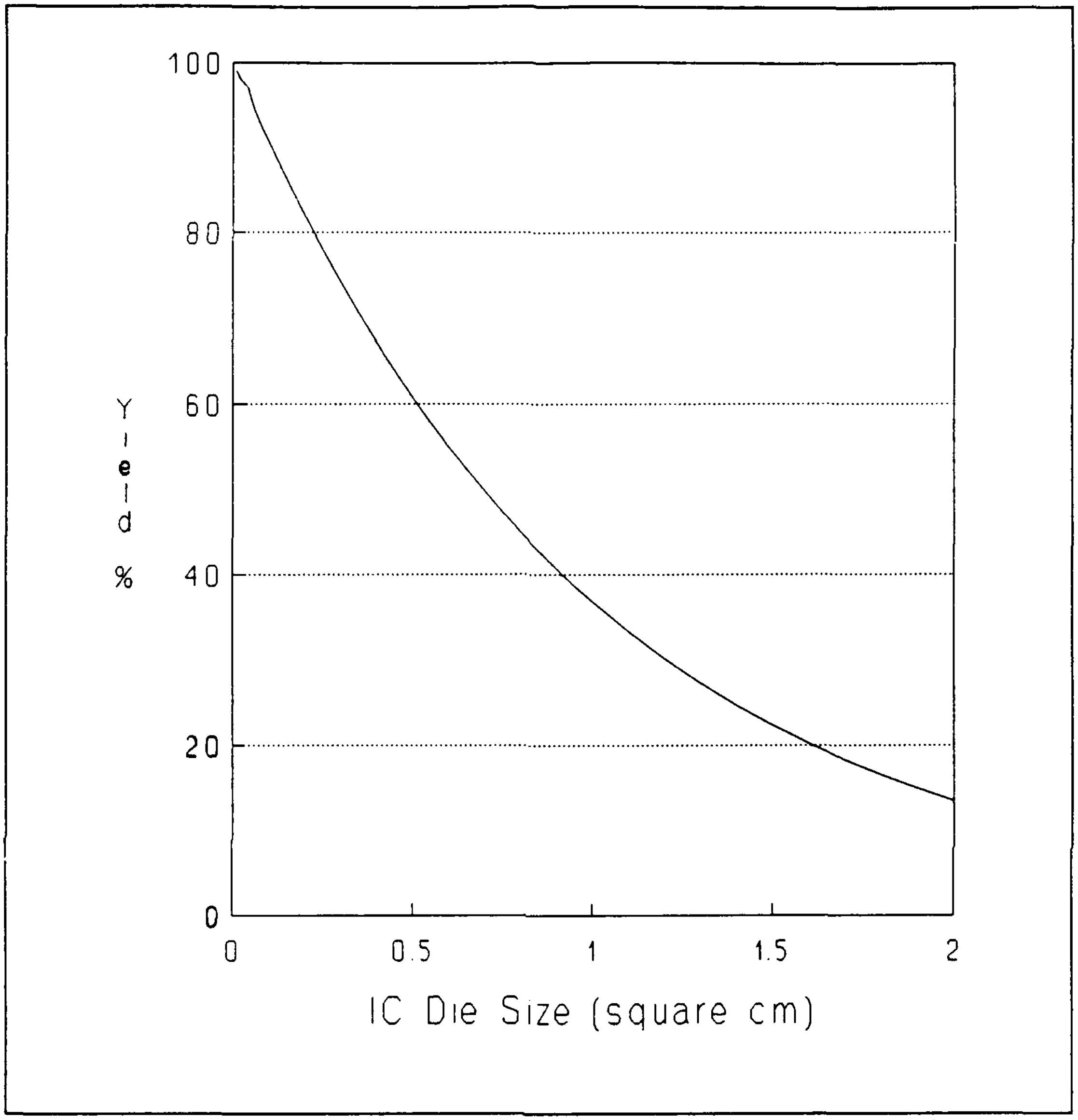


Figure 2.1. Yield of a ten mask process with 0.1 defects/cm^2.

noted that the useable area of wafer sizes commonly used in industry are 100 cm^2 for a six-inch diameter wafer and 25 cm^2 for a three-inch diameter wafer (38:469). Because whole wafers would have to be discarded in the case of a single critical defect, simply extending current IC die design and fabrication processes does not produce a cost effective WSI technique. However, two different approaches to WSI are being developed which are focused on producing acceptable yields in the presence of wafer defect densities in the range of 0.1 to 0.5 defects/cm^2, which are common today (25:65).

WSI Approaches

Monolithic WSI. Wafer scale integration fabrication techniques can be categorized into two major technologies: monolithic and hybrid WSI (16:845). Each method has its own distinctive implementation process, advantages and limitations. Monolithic WSI wafers are fabricated as a single IC die, with redundant copies of each subsystem incorporated on the wafer. Faulty subsystems are identified through testing, and they are bypassed with the resulting circuit interconnect scheme. The primary advantage of this method, relative to hybrid WSI, is that the fabrication process is the same as that currently used to manufacture ICs, with the addition of post-fabrication test and reconfiguration. The primary disadvantage of this technology is the requirement for redundant subsystems, which reduces the effective device density. Key concerns associated with this technology involve the test and reconfiguration of complex circuits, along with yield due to random and process defects.

Research in monolithic WSI has fluctuated since the early attempts by Texas Instruments (25:62). Most of the efforts aimed at applying monolithic WSI to complex circuits, such as microprocessors, have been disappointments. The most widely reported example of these "failures" was the Trilogy project which sought to implement a defect-tolerant 25,000 gate computer processor on a wafer. Although the IC proved functional, the level of redundancy required resulted in little improvement in device density, and the long interconnects on the wafer caused clock skew problems at high operating frequencies. Wafers with reduced redundancy were produced which exhibited improved performance in operating speeds. However, the reduction in redundancy also resulted in lower yield, making the product economically unfeasible, and the project was discontinued in 1984 (4:1743).

Efforts at less complex, array-type systems have shown more promise. These systems include large size memory modules and computational logic arrays, also known as systolic arrays. Massachusetts Institute of Technology (MIT), Lincoln Laboratories, and TRW have all reported research concerned with systolic array applications. The MIT and Lincoln Laboratory effort demonstrated the feasibility of laser programmable restructuring and an effective device density of approximately 45 percent, a modest increase over similar VLSI systems. The TRW effort demonstrated a system with device densities in the 30 percent range. The emphasis of this research was to demonstrate self-test and self-reconfiguration methods for WSI systems (4:1744). Nippon Telephone and Telegraph, Hughes and Sinclair Research have investigated the application of monolithic WSI for large memory modules (4,8). All three efforts demonstrated the feasibility of configurable wafer size modules with device densities in the 30 to 40 percent range (4:1744). In Europe, a consortium of universities together with British Telecom have begun an ambitious monolithic WSI program called ESPRIT 824 (41:17). The initial objectives of this program are to develop a large monolithic memory, followed by a systolic array system. The ultimate goal of this effort is to develop a defect-tolerant 16-bit microprocessor using WSI techniques (41:17).

Efforts in monolithic WSI research have already produced a commercial product, the large semiconductor computer memory. In mid-1989, a British firm, Anarmartic Ltd., began marketing a 160 Mbyte memory storage module (7:51). This memory module contains a stack of eight six-inch diameter silicon wafers. Each wafer contains more than the required 20 Mbytes of memory to allow for fabrication defects or subsequently induced failures. The device is tested to determine functional unit locations, and configuration circuitry on the wafer is programmed to provide a functional data path. By reducing the smallest unit which can be isolated to four thousand bytes, the typical yield of usable memory per wafer is approximately 80 percent (7:53). The success of this particular product can be attributed to the ability to extend the design and repair techniques already employed with the conventional memory ICs used today (40:22).

Hybrid WSI. Hybrid WSI is initiated with pretested, discrete ICs which are mounted into or onto a common substrate and interconnected using standard metallization or wire bonding processes (39:3). The primary advantage of this method results from subsystem pretesting. The discrete ICs, which are fabricated using standard, high-yield processes, are individually screened to eliminate faulty devices before they are incorporated in a WSI configuration. Higher device density can be correspondingly achieved because the need for redundant subsystems is either minimized or totally eliminated. Another advantage of hybrid WSI is the ability to mix IC die which have been fabricated from different materials or those derived from different fabrication technologies (for example, CMOS, NMOS, ECL, etc.). Although hybrid WSI was initially pursued as an intermediate alternative to monolithic WSI, the ability to mix materials and technologies with a common substrate may insure a more permanent role for the hybrid approach. High speed digital systems would benefit by using GaAs technology for key components; mixed digital/analog systems could include high-quality bipolar components for amplifiers, while still taking advantage of CMOS technology for the digital devices. The primary disadvantage of hybrid WSI is the more complicated fabrication process. The alignment, registration, and planarization requirements of the ICs mounted in the host wafer substrate are difficult to simultaneously achieve. The Air Force Institute of Technology (AFIT) has focused its research program on hybrid WSI because of its advantages, as described above.

Hybrid WSI Process

A number of different implementations for hybrid WSI are being pursued. Hybrid WSI techniques can be characterized by the mounting technique used for the pretested IC die. They can be either located on the surface of or mounted in cavities micromachined in the host substrate. Surface mount techniques usually pattern the interconnects on the host substrate, producing a micro-circuit board. The unpackaged IC die are then mounted on the substrate's surface and electrically connected. The large IC formed using these techniques is commonly referred to as a multichip module (MCM). In the alternative approach, the IC die are first mounted into micromachined cavities in the substrate, resulting in a planar surface on which the interconnects are fabricated. This method is known as patterned overlay hybrid WSI (22:2).

Select characteristics of each technique have been reported. In MCM manufacture, the fabrication of the interconnect pattern on the substrate employs non-stressing, automated photolithographic techniques already proven in the IC industry. The resulting interconnect lines and line spacing on these micro-circuit boards are approximately ten times narrower than those available on PCBs (11:171). Denser interconnects and smaller, unpackaged IC die result in smaller and less massive systems. A number of IC die attachment and electrical interconnection methods are available, many of which are currently automated. Mounting can be accomplished using epoxies or solders. Electrical connection of the IC die is commonly accomplished using wire bonding, tape automated bonding or solder bumps on the IC die contact pads. This latter technique has the advantage of accomplishing bonding and interconnection in the same processing step, while simultaneously promoting denser IC die packing (37:47).

In recent years, the applications of MCMs have been rapidly increasing, with much of the effort focused on aircraft avionic and spacecraft computational applications. Rockwell International Corporation has developed MCM memory modules, flight computer processors and a number of avionic modules, including a Global Positioning System (GPS) receiver and a redundancy manager unit (12). Unisys and the Digital Equipment Corporation have each integrated MCMs into their latest mainframe-level workstations (15:34). Honeywell developed an MCM version of their MIL-STD 1750A space flight computer which is one-third the size and has less than one-fifth the number of I/O pins required by the equivalent PCB system (28). Many other examples of MCM products exist which involve a large number of researchers and manufacturers (1,15,23,29,44). In addition to the avionic and computer examples cited above, researchers see the applications of MCMs broadening into telecommunication, medical, robotic and automotive systems (18,36).

The alternative approach, patterned overlay hybrid WSI, has not yet moved out of the laboratory, although a number of research efforts have reported some degree of success (5,16). Researchers at Auburn University developed a patterned overlay hybrid WSI technique which they demonstrated by mounting and interconnecting twelve IC die using a silicon wafer substrate. The fabrication technique proved successful and demonstrated the feasibility of their approach (16). A similar program at General Electric (GE) was also successful in producing a patterned overlay hybrid WSI circuit. The GE study also demonstrated the use of computer controlled lasers in dielectric and metal patterning as a method of automating the process, as well as the ability to repair a WSI module. The researchers removed the patterned overlay, removed and replaced select IC die, and re-patterned the interconnects without damaging the other IC die or the substrate (5).

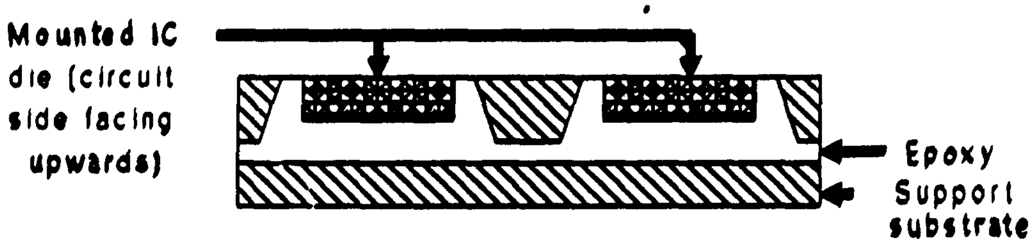
Application of patterned overlay hybrid WSI lags behind MCM technology because of the more complicated fabrication process, which tends to increase costs and reduce yields. Nevertheless, this technique continues to be pursued because it offers the potential for producing ICs with reduced size, higher reliability interconnects, and the ability to stack wafers, resulting in denser, three-dimensional ICs (16:845). Although the exact procedures vary in the different research efforts, the fundamental fabrication process can be analyzed with respect to four major steps: IC die cavity etching, IC die mounting, dielectric deposition, and interconnect patterning. These fundamental fabrication process steps are illustrated in Figure 2.2.

In surface mount and patterned overlay hybrid WSI, materials and processing issues must be addressed, many of which are common to both techniques. Selection of the host substrate, conductor and dielectric materials, as well as interconnect patterning and die bonding techniques, are crucial to all hybrid WSI processes. A number of candidate materials and processes have been applied to each of these areas. The physical and electrical characteristics of the candidates can be used to select the best suited materials and processes for a specific application.

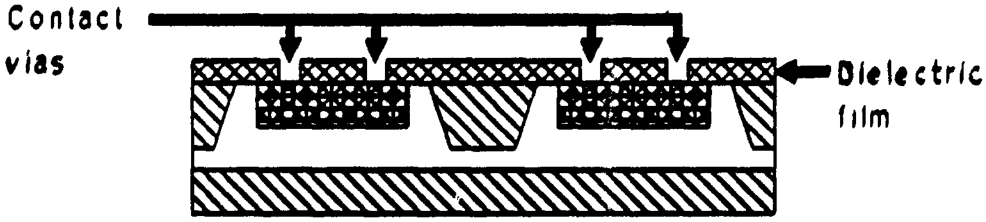
Host Substrate Material. The important parameters involved in selecting the host substrate material include: coefficient of thermal expansion (CTE), dielectric constant, thermal conductivity, mechanical strength and cost. A number of materials have been used as substrates, including:

(a) Host substrate before processing

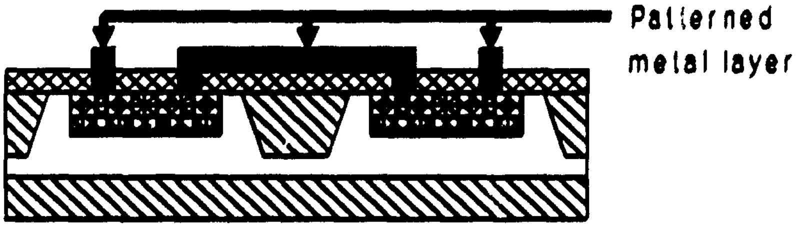
(b) Host substrate with etched IC die wells



(c) Host substrate with IC die mounted and attached to the support substrate



(d) Host substrate with planarizing dielectric applied and patterned for the metal interconnects



(e) Host substrate with patterned metal interconnects

Figure 2.2. Cross-sectional view during the hybrid WSI fabrication process.

silicon, alumina, and co-fired ceramics (34:18). Co-fired ceramics being investigated as host substrates include: aluminum nitride, beryllium oxide and silicon carbide. The characteristics of each of these materials with respect to the aforementioned parameters have been documented to facilitate the material's selection for a specific application. Typical parameter values for the candidate substrate materials are presented in Table 2.1.

Silicon. Single crystal silicon substrates possess many advantages relative to the other materials for both MCM and patterned overlay WSI. The most important advantage is the perfect match of the CTE with silicon IC die. The CTE match tends to reduce mechanical stress in the final WSI assembly (11:171). Also, photolithographic and micromachining techniques are well established for silicon, and additional passive elements, such as resistors and capacitors, can be fabricated in the substrate itself. Finally, as illustrated in Table 2.1, silicon exhibits reasonable thermal conductivity and a small-valued relative dielectric constant which favors reducing parasitic capacitances in the final WSI system (2:103). One disadvantage of silicon substrates is their fragility (37:45). AFIT, Auburn University, Hughes, Anamertek and Lincoln Laboratories have each pursued WSI research using silicon substrates (7,10,11,16,24,39).

Table 2.1. Typical Properties of Substrate Materials. From (34,45)

Material	CTE (ppm/ °C)	Relative Dielectric Constant	Thermal Conductivity (W/m·K)	Young's Modulus (Mpsi)	Cost
Silicon	3.5	12.0	120	29	1
Alumina	6.5	8.8	20	52	2
Beryllium Oxide	7.5	6.5	250	45	5
Aluminum Nitride	4.1	8.8	100-220	39	3
Silicon Carbide	3.8	40	270	83	4

NOTE: Entries in the Cost column are a rank ordering of the relative costs for each material, 1 being the least expensive, and 5 being the most expensive.

<u>Alumina</u>. Alumina has been considered as a substrate material because it is relatively inexpensive, as documented in Table 2.1, with a well established history as a conventional hybrid microelectronic substrate (2:102). Although alumina exhibits superior thermal conductivity, mechanical support and reduced line width and separation constraints compared to standard PCB materials, alumina has a poor CTE match with silicon, and a large-valued relative dielectric constant which tends to increase the parasitic capacitances in the resulting WSI circuit (2:102). Alumina does provide better mechanical support than silicon, and it can be machined to provide IC die cavities (5:340). General

Electric, Dupont and National Telephone and Telegraph of Japan have reported on WSI research using alumina substrates (4:528).

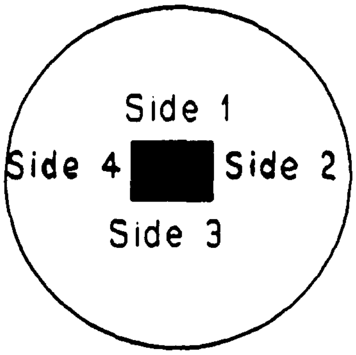
Co-Fired Ceramics. A co-fired ceramic is a multilayer material comprised of alternating layers of metal and ceramic material which are sandwiched together and sintered at a high temperature (15:35). Several co-fired ceramics are being investigated as substrate materials. Three examples are aluminum nitride, beryllium oxide and silicon carbide. The key advantage of these three ceramics is their large-valued thermal conductivity, which is important in very dense circuits and higher power applications. However, beryllium oxide exhibits an incompatible CTE match with silicon compared with alumina or single crystal silicon, and it requires special handling because of the toxicity of the substrate material (30:82). The special handling requirements for beryllium oxide increase the associated cost of using this material. As Table 2.1 illustrates, the other two candidates have CTEs compatible with silicon, and they are easy to machine. Both of these ceramics exhibit large-valued relative dielectric constants, resulting in higher parasitic capacitances. For these reasons, aluminum nitride and silicon carbide are usually selected only when the thermal load requires their use (2:102).

IC Die Cavity Etching. In the patterned overlay hybrid WSI technology, the next step in the process is to form wells or cavities in the host substrate to accommodate the IC die. When ceramic substrates are used, these cavities are formed with a mechanical machining process (5:340). When silicon substrates are used, the cavities are formed using a wet chemical or dry plasma etching process.

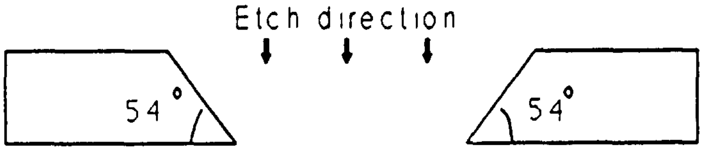
Wet chemical etching a single crystal silicon substrate requires a silicon dioxide mask, with appropriately etched windows, to mask select areas of the substrate from the etchant. The wafer is then immersed in the etchant which chemically dissolves the exposed silicon surfaces. Etching is terminated by rinsing the etchant from the wafer after a specified period of time. Etching is precisely controlled to produce the desired IC die cavity geometry. The host silicon wafer crystal orientation and dopant type, as well as the etchant concentration, temperature, and the etch duration time are all critical factors which control the etch process. Silicon wafer crystal orientation determines the planar atomic density which affects the etch rate. The properties of the etchant determine the advantageous exposure temperature and time necessary to produce the desired IC die cavities (24:Sec 4,20).

To minimize the size and step-height differential of the transition region between the IC die and the host substrate, vertical or near-vertical cavity walls are desired. For a wet chemical etch process, an etchant must be selected which will preferentially etch the silicon in a direction perpendicular to the surface. Two chemical solutions have been found to produce orientation-dependent etch rates: potassium hydroxide (KOH) and ammonium hydroxide (19,35). Both of these solutions exhibit faster etch rates in the (100)-plane of single crystal silicon compared to the (111)-planes. An etchant composed of 20%wt KOH and water at 75°C will produce an etch rate on the order of 0.5 microns per minute in the (100)-plane and approximately 10 Angstroms per minute in the (111)-plane (19:110). Similarly, an etchant composed of 3.7%wt ammonium hydroxide and water at 75°C will produce an etch rate on the order of 0.4 microns per minute in the (100)-plane and approximately 10 Angstroms per minute in the (111)-plane (35:2). The effect of these anisotropic etch rates, combined with the orientation of the crystal planes with respect to the wafer's surface, produces different cavity geometries.

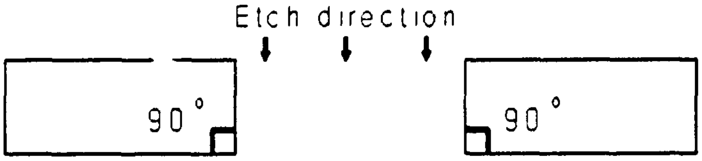
In his WSI research at AFIT, Mainger studied the effects of crystal orientation on cavity etching, comparing the cavities etched in (100)- and (110)-oriented silicon wafers (24:Sec 4,20). He recommended (100)-oriented wafers for a number of reasons. First, the walls and bottoms of the cavities etched in the (100)-oriented wafers were smoother than those found in the (110)-oriented wafers. The effects of the anisotropic etch rate of the KOH solution used by Mainger, combined with the crystallographic orientation of the test wafers, are illustrated in Figure 2.3. Although the



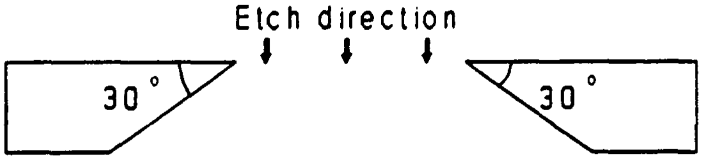
(a) Top view of either a (100)- or (110)-oriented silicon wafer with an etched window



(b) (100)-oriented etch results (sides 1,2,3,4)



(c) (110)-oriented etch results (sides 1,3)



(d) (110)-oriented etch results (sides 2,4)

Figure 2.3. Results of etching silicon wafers with different crystal orientations.

perpendicularity of two of the walls in the (110)-oriented wafers matches what is desired, the severe undercutting on the other two walls required significant spacing between mounted IC die. Thus, the (100)-oriented wafers require less surface area to produce a cavity with a given size opening (24: Sec 4,18).

In dry plasma etching, the wafer surface is bombarded with a stream of ionized gas molecules. The collision of the gas ions with the wafer's surface results in a momentum exchange with the substrate's atoms. Substrate atoms, which are sufficiently excited, are released from the wafer's surface. Specific gas mixtures have been found to etch different materials at different rates. Silicon is typically etched with a mixture of sulfur hexafluoride and chlorine. Silicon dioxide can be used as the mask material because this gas mixture etches silicon up to 80 times faster compared to silicon dioxide (38:463).

Dry plasma etching can produce cavities in silicon substrates with tightly controlled geometries and near-vertical walls. However, etching a cavity completely through a 500 micron thick wafer would require a silicon dioxide mask layer thickness in excess of six microns. An additional disadvantage of dry plasma etching is the high cost of the required etching equipment (38:463).

<u>IC Die Mounting</u>. The second step of the patterned overlay hybrid WSI process consists of mounting the pretested

IC die in the host substrate. Two approaches to this step have been employed in WSI research at AFIT. One approach used a host silicon wafer in which the IC die cavities were not etched completely through the wafer. The cavity bottoms, which were parallel to the top surface of the host silicon wafer, provided a smooth surface upon which to mount the IC die (24: Sec 4,20). An alternative method, initially reported by Auburn University researchers, utilizes a substrate with IC die cavities etched completely through the host wafer. Die bonding is performed by positioning the IC die in the etched windows with the circuit side contacting an optical flat, resulting in a planarized wafer and IC die surface (16:847). Consequently, this method requires that a second wafer be attached to the backside of the assembly to provide mechanical support.

The first approach described above has a number of key disadvantages. First, Mainger reported that it "was difficult to dispense the correct (and a consistent) amount of epoxy" (24: Sec 3,17). The excess or lack of bonding material results in degraded planarization of the IC die and wafer surfaces, as well as their transition region. Also, as Takahashi points out, this method requires host wafers which are approximately twice as thick as the thickest IC die to maintain structural integrity. The IC die available to AFIT through the Metal-Oxide Semiconductor Implementation System (MOSIS) are generally too thick to be utilized in this approach (39:59). As a result, recent WSI efforts at AFIT have employed a technique similar to that used by Auburn University (16).

One complication with the Auburn approach that has been noted in past research efforts is the tendency of the bonding material to stick to the optical flat, the host silicon wafer, and the IC die during the cure process. Figure 2.4 illustrates the cure process apparatus. To prevent permanent adhesion between the optical flat and the WSI assembly, Takahashi introduced a labor and time intensive process of forming a cured epoxy barrier across the transition region, by repeatedly cleansing the optical flat to prevent sticking (39:154-155). Gaughan attempted to avoid this problem by substituting a Teflon® block in place of the optical flat, which eliminated the need for its repetitious cleansing. Although this method succeeded in eliminating the sticking problem, Gaughan indicated that the Teflon® block failed to maintain its flatness at curing temperatures above 50°C. The heat-induced Teflon® deformation caused poor planarization between the IC die and the host silicon wafer surface (10:23).

A number of solutions to this problem have been proposed. Proposed solutions under consideration include: coating the optical alignment flat with a thin film of Teflon® or a dry lubricant, coating the optical flat with a thin sacrificial layer of polyimide or photoresist,

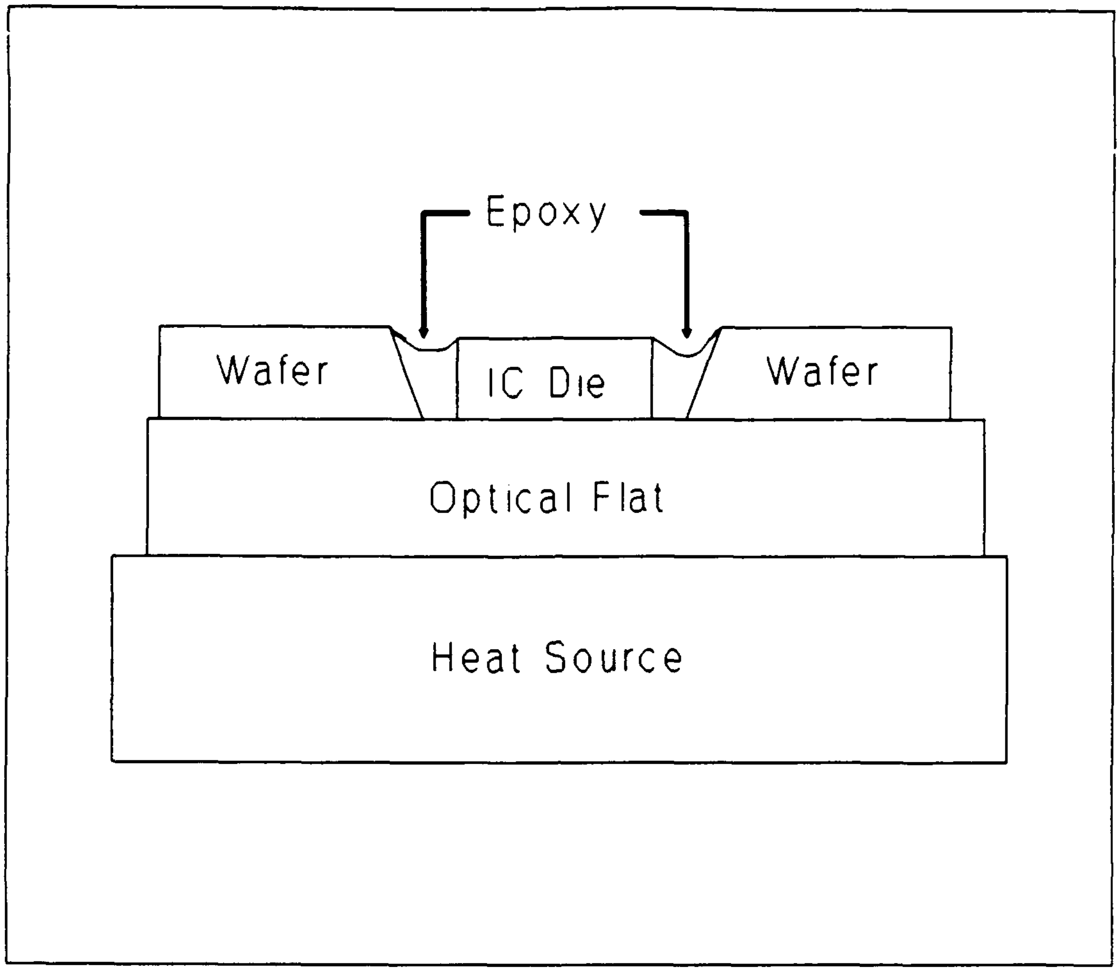


Figure 2.4. Cross-sectional view during epoxy cure.

substituting polyimide as the die bonding material, or substituting an epoxy which can be cured using an ultra-violet light source rather than a heat source. The Auburn University research reports the successful use of a "metal release film" on the optical flat surface (16:847).

Adhesive Material. The choice of adhesive is important, because a number of key characteristics will affect the success of the WSI assembly. The adhesive must exhibit minimal shrinkage during cure to prevent voids from forming in the IC die-to-host silicon wafer transition region. The adhesive must also be sufficiently strong to absorb the stress of thermal expansion relative to the silicon IC die and the host silicon wafer substrate. The maximum temperature to which this material can be exposed establishes a limit on the temperature to which the assembly can be exposed during subsequent processing and actual operation. Materials which have been used as the die mount adhesive include: polyimide, gold eutectic pre-forms, silver glass epoxy, and two component epoxies. Selection of one of these materials for a specific application can be made based upon its characteristics.

Polyimide. A number of IC die attachment materials have been tested in previous research efforts. The Auburn researchers have tested two polyimides as the bond material. The primary advantage of a polyimide in this application is the high post-cure exposure temperature (400°C) to which these materials can be exposed. However, the polyimides evaluated were found to be unacceptable because of the large density of voids that were formed within the polyimide during its cure (16:848). These voids, which are caused by solvent evaporation, could result in bond failures or latent stresses, as well as hot spots because of a lack of proper heat conduction.

Gold Eutectic Pre-Forms. Gold eutectic pre-forms have also been evaluated as an IC die attachment material. In his research, Mainger reported that gold eutectic pre-forms failed to provide a reliable bond and required a high processing temperature (350°C). This latter quality could be detrimental to the IC die circuitry (24: Sec 4,29). Nguyen indicated that the occurrence of a poor bond was the result of the high sintering rate of gold eutectics, which causes excessive stress in the bond during its cure. This stress was distributed over a large bond area, and it caused cracking and poor adhesion in the bonds (32:478).

Silver Glass Epoxy. Mainger also evaluated a silver glass epoxy IC die bonding material. Although this epoxy provides a reliable bond, a number of undesirable characteristics were observed. First, the silver glass epoxy requires the highest processing temperature of the adhesives evaluated. This processing temperature (435°C) could adversely affect the circuitry fabricated on the IC die. Also, the silver glass epoxy bond exhibits large voids, which could affect the circuit's heat dissipation (24: Sec 4,30). In another research effort, Nguyen reported success in producing void-free, large area die bonds with a silver glass adhesive; however, the material tested requires processing temperatures in excess of 400°C (32:479).

Two Component Epoxy. Two component epoxy adhesives have also been used as IC die attachment materials in MCM and hybrid WSI research. One advantage of the epoxies is that they are solventless, which leads to minimal shrinkage and voiding during cure. Mixtures can be tailored to meet a variety of specifications, such as thermal and electrical conductivity, thermal expansion, and post-cure temperature limits. Both AFIT and Auburn have used a common two-component epoxy in their research, Master Bond EP34CA (10,16,21,24).

Dielectric Coating. In the third step of the patterned overlay hybrid WSI process, a planarizing dielectric is applied to the surface of the wafer. This dielectric layer serves two primary functions. First, the dielectric provides a smooth layer over the IC die-to-substrate transition regions. Subsequent metal layers require a smooth surface to ensure interconnects with no cracks or breaks. The dielectric also provides electrical insulation between the interconnects and devices. Vias are etched through the dielectric layer to the IC die contact pads using either a masking process similar to conventional photolithography or plasma etching (16:847).

The dielectric layer thickness is an important factor to consider. The ability of the dielectric layer to smooth the topology of the IC die and the IC die-to-substrate transition region increases with a thicker layer. Also, thicker dielectrics will improve certain electrical characteristics of the circuit by providing better electrical insulation and reducing parasitic capacitances. There are limits to these improvements, however. Takahashi indicated that the most significant improvements in electrical characteristics, such as line loss and parasitic capacitance, occur for thicknesses less than 20 microns (39:50). The relationship between parasitic capacitance and dielectric thickness can be expressed as (39:24):

$$C=\epsilon_o\epsilon_r[1.15(\frac{w}{h})+2.8(\frac{d}{h})^A+[0.06(\frac{w}{h})+1.66(\frac{d}{h})-0.14(\frac{d}{h})^A](\frac{s}{h})^B] \tag{2.2}$$

where

C is the capacitance per unit length (pF/cm)
h is the dielectric thickness (cm)
w is the conductor line width (cm)
s is the adjacent conductor separation (cm)
d is the conductor thickness (cm)
ϵ_r is the relative dielectric constant of the dielectric
ϵ_o is the free space permittivity (pF/cm)
A is an exponential fitting parameter equal to 0.222
B is an exponential fitting parameter equal to -1.34.

This expression was utilized to derive a relationship between the capacitance and the dielectric thickness for a typical WSI assembly. A conductor line width, w, of 0.003 cm was utilized, based on dimensions reported in MCM and WSI research (11,25,39). Adjacent conductor separation, s, was 0.02 cm, in accordance with the typical IC die bond pad pitch (25,39). Conductor thickness, d, of 0.0001 cm was selected, to provide adequate step coverage over via regions. A relative dielectric constant equal to 3.0 was selected, as an approximate mean for the majority of the candidate dielectric materials (3,6,17,21,39,45). For these constant dimensions, the resulting relationship between the capacitance and the dielectric thickness is presented in Figure 2.5.

As Figure 2.5 illustrates, increases in dielectric thicknesses greater than 20 microns result in minimal improvements. One key disadvantage of the thicker layers must also be considered. As the dielectric layer becomes thicker, it becomes more difficult to produce reliable metal interconnects through the dielectric to the IC die.

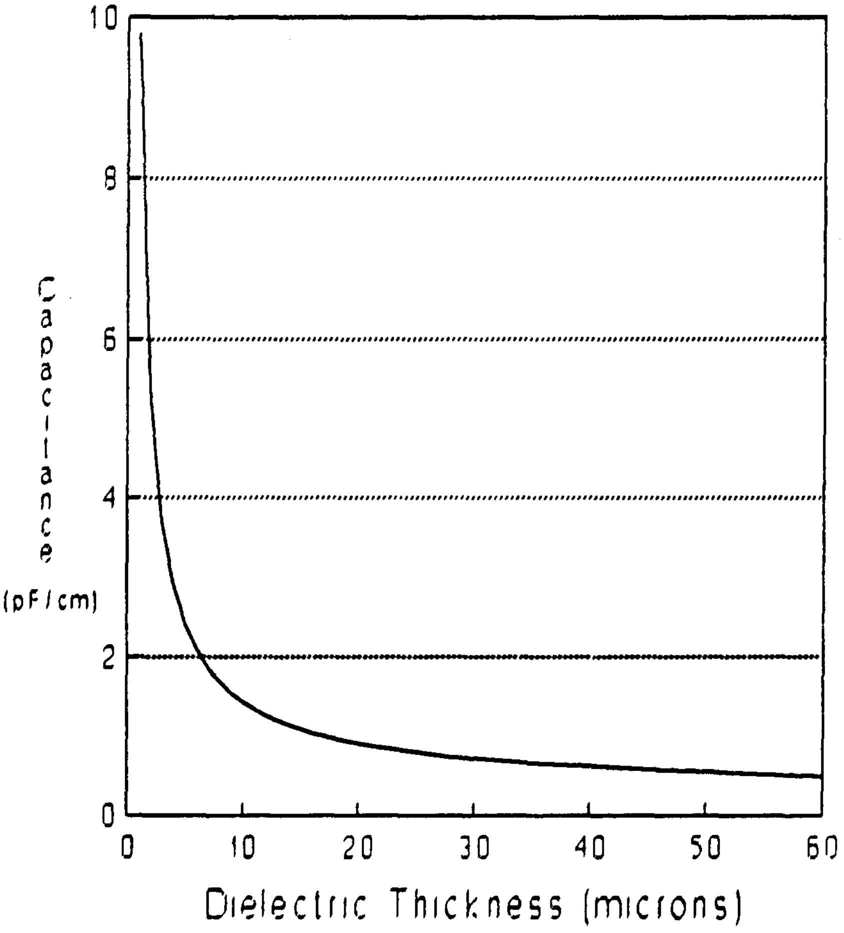


Figure 2.5. Parasitic capacitance as a function of dielectric thickness.

Dielectric Materials. A number of materials have been used in the IC industry as interlevel dielectrics. The most common examples are: silicon dioxide, silicon nitride, spin-on glass (SOG), benzocyclobutene (BCB), and the polyimides. Each candidate exhibits specific characteristics which can be matched to the requirements of a specific application. Table 2.2 lists typical values for the candidate materials.

Silicon Compounds. Silicon dioxide and silicon nitride have enjoyed popularity as electrical insulating materials in the IC industry because of their compatibility with the monolithic silicon fabrication process and the ease by which they can be thermally grown or deposited onto a silicon substrate using chemical vapor deposition (CVD). The primary disadvantage of using these materials in hybrid WSI fabrication is that the high processing temperatures required to apply these dielectrics could damage the adhesive bond between the mounted IC die and the host substrate (24: Sec 4,29). Other disadvantages of these dielectrics include the difficulty in producing sufficiently thick layers (2), and the tendency of these layers to be deposited without planarizing the topology (6:60).

Spin-on Glass. Spin-on glass (SOG) dielectrics are silicon-based coatings which are often used in conjunction with oxide CVD dielectrics to improve planarization. SOGs are not used alone to produce the dielectric layer because SOG films thicker than five microns tend to crack, and SOG in

Table 2.2 Typical Properties of Dielectric Materials. From (3,6,17,21,39,45).

Material	Dielectric Constant	Dielectric Strength (MV/cm)	CTE (ppm/°C)	Water Absorption (%)
Silicon Dioxide	3.9	1-10	0.6	-
Silicon Nitride	9	1-10	2.8-3.2	-
Spin-on Glass	3.0	0.2-0.5	-	0.9
BCB	2.75	2.5	30-60	0.2-0.3
Polyimide	3.4	3	5-60	0.5-1.5

the area of vias tend to absorb moisture which adversely affects metal interconnects (6:62). Thus, SOG is only applied as a thin planarization layer prior to the CVD application of silicon dioxide. Although this technique exhibits improved planarization, its disadvantages include an increased number of processing steps and the requirement for an accompanying high temperature CVD process (6:62).

Benzocyclobutene. A number of polymer materials are available which can be used as thick film planarizing dielectrics. Benzocyclobutene (BCB) is a typical polymer being evaluated as an alternative to the more common polyimides used today. As Table 2.2 depicts, BCB exhibits a lower-valued relative dielectric constant which reduces the inter-conductor capacitances in the resulting circuit. The primary advantage of BCB is low water absorption compared to most polyimides (3). The water absorbed by the dielectric tends to oxidize the metal conductors, reducing their conductance (2:107). One disadvantage of BCB is that dry etching is required to fabricate via holes for interlevel connections. The equipment required for dry etching is more costly compared to that required to support wet chemical etching, which can be used for polyimides. In addition, BCB demonstrates poorer adhesion to aluminum compared to that demonstrated with the polyimides. This adhesion can be improved using thin adhesion layers (17:348) or with sputtering techniques (3).

Polyimides. Polyimides are organic polymers which contain a phtalimide structure as part of the polymer chain. This structure results in a polymer which exhibits high thermal stability, solubility and processibility compared to other polymers (11:34). Polyimides exhibit a number of characteristics which are desirable for a dielectric material. First, polyimides exhibit a number of advantages, including a low-valued relative dielectric constant, good electrical insulation, and good adhesion with the substrate materials. Second, the cure process temperature required for polyimides is lower than the temperature limits common to the epoxies used in the IC die mounting process. Finally, polyimides have a high modulus of elasticity and good step coverage. The latter quality is important for planarizing the IC die-to-substrate transition regions (16:848). An important disadvantage of polyimides is that they exhibit poor thermal conductivity. Because of this quality, the bulk of heat produced by the circuit must be removed through the backside of the wafer.

Prior to the application of metal to the polyimide's surface for the interconnects, vias must be patterned in the polyimide layer to the bond pads on the IC die. A number of methods for producing these vias may be used. They include: wet etching, dry etching, photosensitive polyimide, and laser ablation (20:42).

Wet etching involves the use of a chemical etchant to pattern a partially cured polyimide layer. A photoresist layer must first be deposited and patterned on the surface of the polyimide. The disadvantages of this process include: the potential interaction between the photoresist processing chemicals and the polyimide, and low resolution due to polyimide shrinkage during final cure and the inherent limitations of a wet process (20:43). One advantage is that the equipment, materials and processes are common to other WSI processing steps.

Dry etching, using a plasma or reactive ions, is one method which provides improved resolution and aspect ratios. This method requires a protective mask to be deposited on the polyimide prior to implementing the via etching process. Often metals or silicon dioxide masks are required because a photoresist mask will etch at nearly the same rate as the polyimide. The deposition and patterning of these masks requires additional equipment and processes. Another disadvantage is the added expense of the plasma etch system (20:45).

To reduce the number of processing steps, polyimide complexes have been developed which include photosensitive materials. These photosensitive polyimides can be patterned directly, eliminating the need for a supplemental mask. Photosensitive polyimides require only four patterning steps (one half the number required for the dry or wet etch processes). One disadvantage with current photosensitive polyimides is the high energy absorption requirements of these materials, which requires long exposure times and limits the thickness which can be patterned. To produce a thick film patterned layer, thinner multi-layers may be required. Another disadvantage is that, currently, only negative-type photosensitive polyimides are available, which exhibit poorer resolution than those patterned with positive photoresists (20:45-46).

The most recent development in polyimide patterning is a technique known as laser ablation (20:46). In this technique, a small diameter laser beam is passed through a pinhole, and it is used to evaporate the polyimide in small areas to form the vias. This technique does not require the application of a mask pattern on the wafer. Instead, the laser is controlled by a computer which identifies contact pad locations through an image scan, and then positions the pinhole and fires the laser beam. Feature sizes as small as 0.4 microns have been etched in polyimide using this technique. Beam penetration is limited by the contact pad, which reflects the beam and dissipates the heat generated on its surface (5:340). The primary disadvantage of this technique is the high cost of the processing equipment; however, laser ablation shows significant promise for production-level WSI fabrication.

Interconnect Patterning. The final step of the patterned overlay hybrid WSI fabrication process is the metal deposition and patterning. This metal patterned layer provides the IC die interconnects. This step in the procedure requires the selection of a conductor material and a patterning technique.

The most common conductor materials found in hybrid WSI systems are aluminum, copper and gold. The characteristics which are important in choosing the appropriate conductor material include: good adhesion to the substrate, dielectric and contact pads, low resistivity, good corrosion resistance and chemical inertness (34:19). Table 2.3 summarizes the typical characteristics of the conductor candidate materials.

The key advantages for aluminum include: good adhesion to most dielectric and substrate materials, low cost, and well established IC fabrication processes. The major disadvantage is that aluminum has the highest resistivity of

Table 2.3. Typical Properties of Interconnect Metals. From (21,39,45).

Metal	Resistivity (10^{-6} ohm·cm)	CTE (ppm/°C)	Thermal Conductivity (W/m·K)
Aluminum	2.7	23.5	250
Copper	1.7	17	166
Gold	2.2	14	142

the three candidates (34:19). Copper is inexpensive, and exhibits good solderability and electrical conductivity. The primary disadvantage of copper is that polyimide precursors, used with the most common dielectrics, tend to oxidize copper, causing migration into the polyimide, which increases the conductor's resistivity (34:19). This effect also increases the polyimide's relative dielectric constant which, in turn, increases the parasitic capacitances (2:106) and degrades adhesion. This oxidation can be prevented by placing barrier layers between the copper and the dielectric; materials such as chromium, nickel or titanium have been utilized (34:19).

Each of the three candidate interconnect metals can be deposited on the substrate's surface using either thermal evaporation or sputtering. Patterning is accomplished using standard photolithographic techniques, with a wet etch process of the metal itself, or lift-off of the metal covering the patterned photoresist.

The alignment of the IC die in the attachment step affects the success of the metallization process. The polyimide vias must be aligned with the contact pads on the IC die for the interconnects to function properly. Any translational or rotational misalignment of the IC die in the cavity may place the contact pads under dielectric rather than an open via, resulting in a malfunctioning circuit. This problem can be prevented by maintaining tight tolerances on the IC die and etched cavity dimensions. This verification technique limits the amount of possible misalignment, thereby increasing the yield of the functional interconnects. An alternative method involves measuring the IC die alignment on a particular wafer prior to applying the planarizing dielectric. Via and metal patterning masks for individual wafers are produced based upon these measurements (16:848).

Summary

This chapter discussed the evolving requirement for WSI technology, the two primary approaches to implementing WSI, and the fabrication process and materials used to realize the hybrid WSI technology. Literature concerning the characteristics of alternative materials and approaches was reviewed to establish the foundation for the baseline approach to be used in this thesis.

An approach similar to the Auburn University method will be used to mount the IC die. A number of anti-adhesive coatings applied to a glass optical flat will be evaluated for improving the previously reported results. Silicon (100)-oriented wafers will be used as the host substrates. The Master Bond EP34CA epoxy will continue to serve as the primary adhesive material, based upon previous success with this epoxy.

Three candidate polyimides will be evaluated for use as the planarizing interlevel dielectric. The criteria for this evaluation will focus on the patternability of these three candidates. The primary material will be the photosensitive polyimide used in the previous AFIT WSI efforts. Although this material has been used successfully, difficulties concerning adhesion and patterning have been reported. A second photosensitive polyimide has been identified which has a purported higher photospeed. The third candidate will be a non-photosensitive polyimide developed for thick film applications, such as WSI and multichip modules.

Aluminum will be used in the metallization steps for this effort. Aluminum was chosen based primarily on availability and cost. In addition, previous AFIT research has demonstrated the compatibility of aluminum with one of the candidate polyimides, and a suitable processing procedure (21).

III. Integrated Circuit Design

An integrated circuit (IC) was designed to provide the test article to be used in the WSI configurations. This chapter describes the design process used to develop this IC. The specifications for the IC are outlined in the first section of this chapter. A detailed discussion of the floorplan considerations for the IC and the design process for each major component follows the discussion of the specifications. The major components are: the Counter, the Digital-to-Analog (D/A) Converter, the Comparator, and the 555 Timer. Descriptions of the specific functions of each of these components is included in the design process section. The chapter summary outlines the key characteristics of the final circuit design.

Project Design Specification

The circuit designed for this project is known as a successive approximation analog-to-digital (A/D) converter. The baseline approach is illustrated in the block diagram in Figure 3.1. This A/D converter has one external input signal: the analog signal (Analog In) to be evaluated, and two external output signals: the eight bit digital signal (Digital Out) equivalent of the analog input, and a Data Ready signal which indicates when the digital signal is valid. The Clock signal is internally generated via the 555

Timer circuit. The Analog Out signal represents the analog equivalent of the Digital Out signal, as generated by the D/A Converter. The X signal is the signal resulting from the comparison between the Analog In and Analog Out signals, which indicates to the Counter circuit whether to count up or down in the next approximation. The R1 and R2 nodes for the 555 Timer are provided to connect an external RC circuit which controls the Clock signal frequency and pulse width. The Reset input is used to initialize the 555 Timer circuit, and the Control provides the capability for maintaining a high or low clock signal. A sample timing diagram is shown in Figure 3.2.

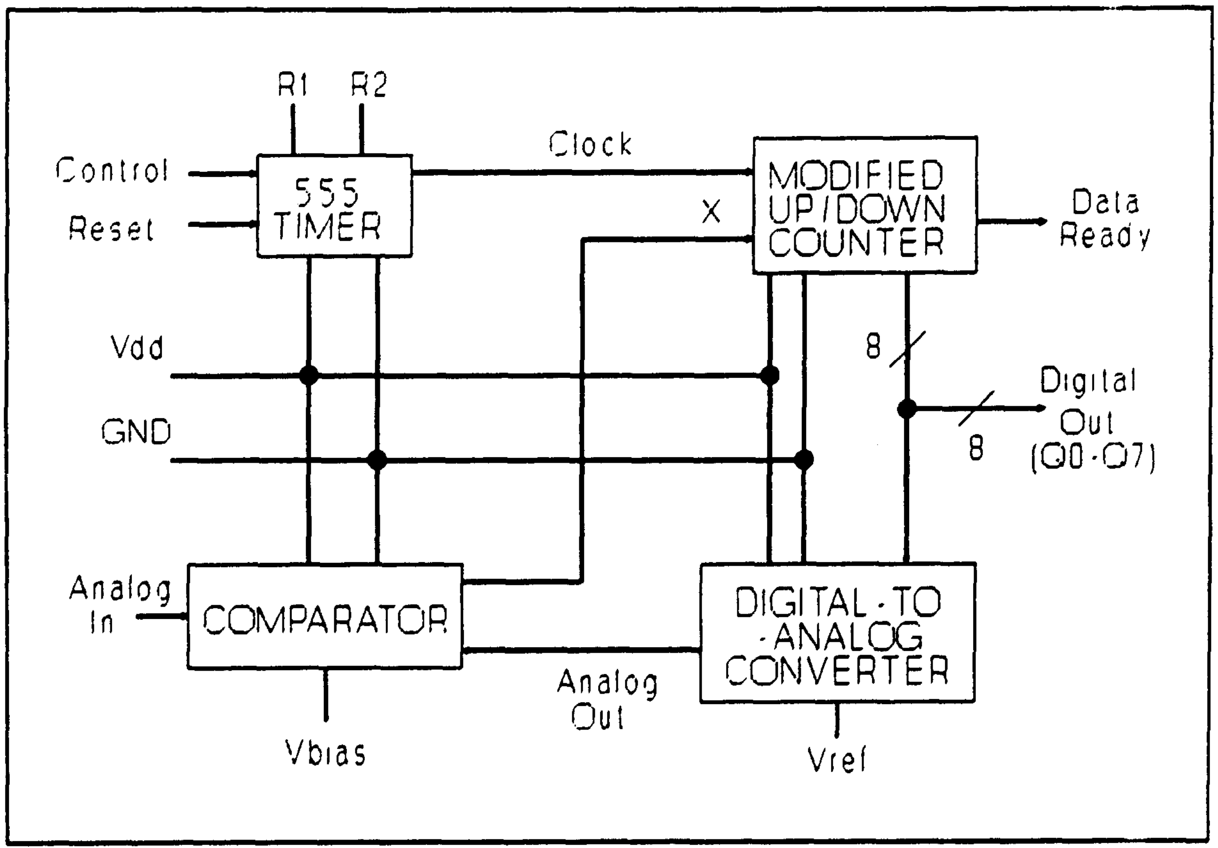


Figure 3.1. Baseline electrical circuit design block diagram.

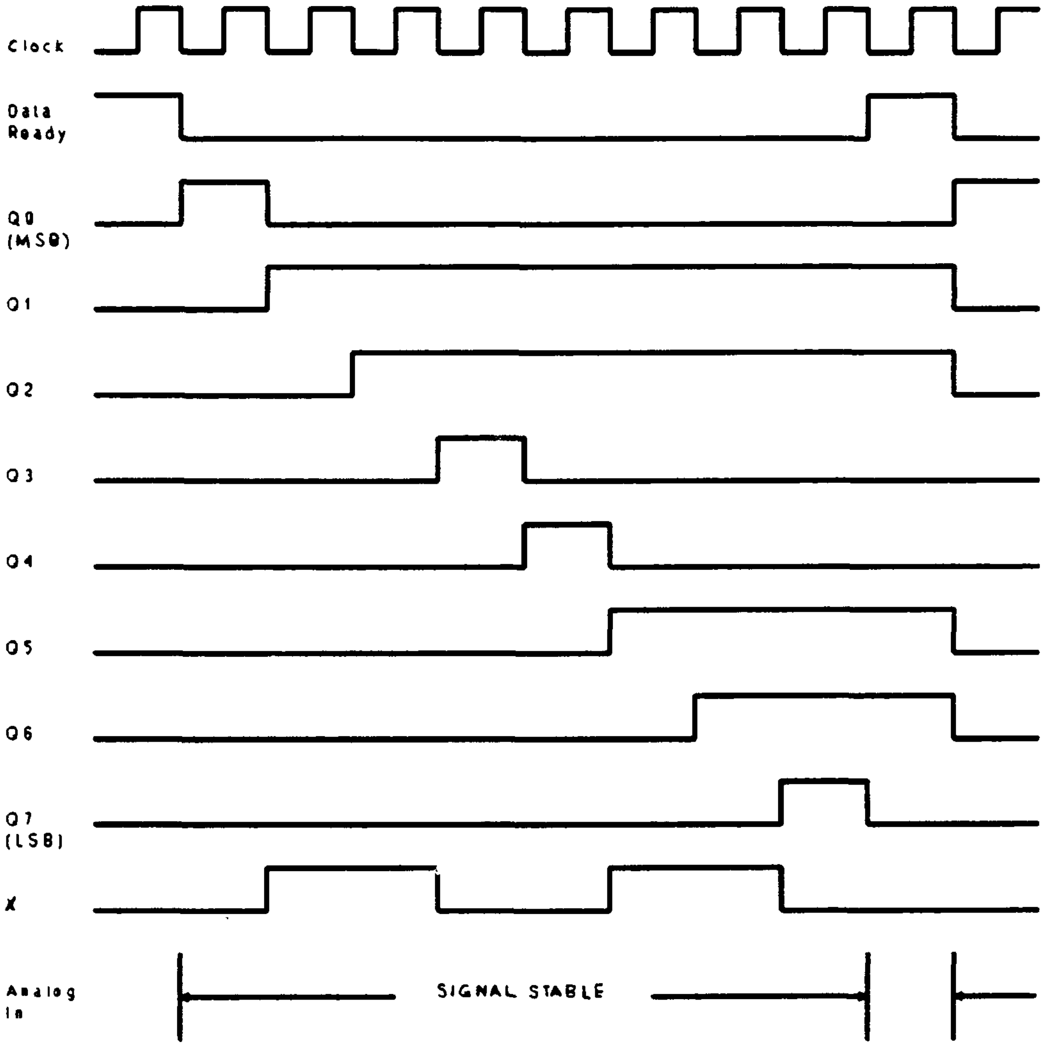


Figure 3.2. Ideal timing diagram of the proposed A/D Converter design.

The basic theory of operation is that a series of digital approximations will be compared to the analog input. The digital signal generator, or Counter, begins each comparison sequence with the most significant bit (Q0) set to one and all other bits set to zero. This digital vector is then converted to an analog signal and compared with the analog input. If the analog input is larger, Q0 remains a one, otherwise it is reset to zero. In the next clock sequence, the next most significant bit is set to one, the digital vector is converted to an analog signal and again compared with the analog input. This sequence is repeated for eight clock cycles for each analog input signal. The resulting digital equivalent signal is available on the ninth clock cycle, when the Data Ready signal is established. The internal clock signal is generated by the 555 Timer circuit.

The primary design specification for this project is minimal transistor sizes and equivalent rise and fall times for each gate design. The eight bit digital signals represent 256 different voltage values, from 0 volts, represented by '00000000', to Analog Out_{max}, represented by '11111111'. The magnitude of Analog Out_{max} is a function of the magnitude of V_{ref}. This functional relationship is determined in the D/A Converter design. The analog voltages corresponding to each digital increment are equally spaced. Each subsystem should be capable of operation in a stand-alone mode, with the provision of appropriate input signals.

Design Process

As previously stated, the approach was to design the four major subsystems separately, followed by integration of the components into the A/D converter system design. Although each subsystem was separately designed, loading between subsystems was taken into account in the circuit simulations, and an overall floorplan was developed prior to the layout of each subsystem. The Counter, Digital-to-Analog Converter and Comparator circuit designs were all created specifically for this project. The 555 Timer circuit design is a modification of an existing design. Capt Robert Fitch (GE-90D) designed a 555 Timer for his thesis project. This design has been fabricated and verified (9:Sec 4,13). Modifications to the Timer focused on integrating the layout with the design of the other subsystems.

The baseline floorplan is illustrated in Figure 3.3. This plan is based on the fact that the Counter and D/A Converter subsystems have the eight-bit interconnects, and that both would be designed using a bit slice approach. The bit slices in both of these subsystems were designed to approximately the same width for uniformity and to facilitate routing interconnects. The 555 Timer is configured to match the profile of these two subsystems and an interconnect channel. The 555 Timer is placed on the end of the Counter where the Counter's clock input is located. The Comparator is placed on the other end of the layout, such that it is

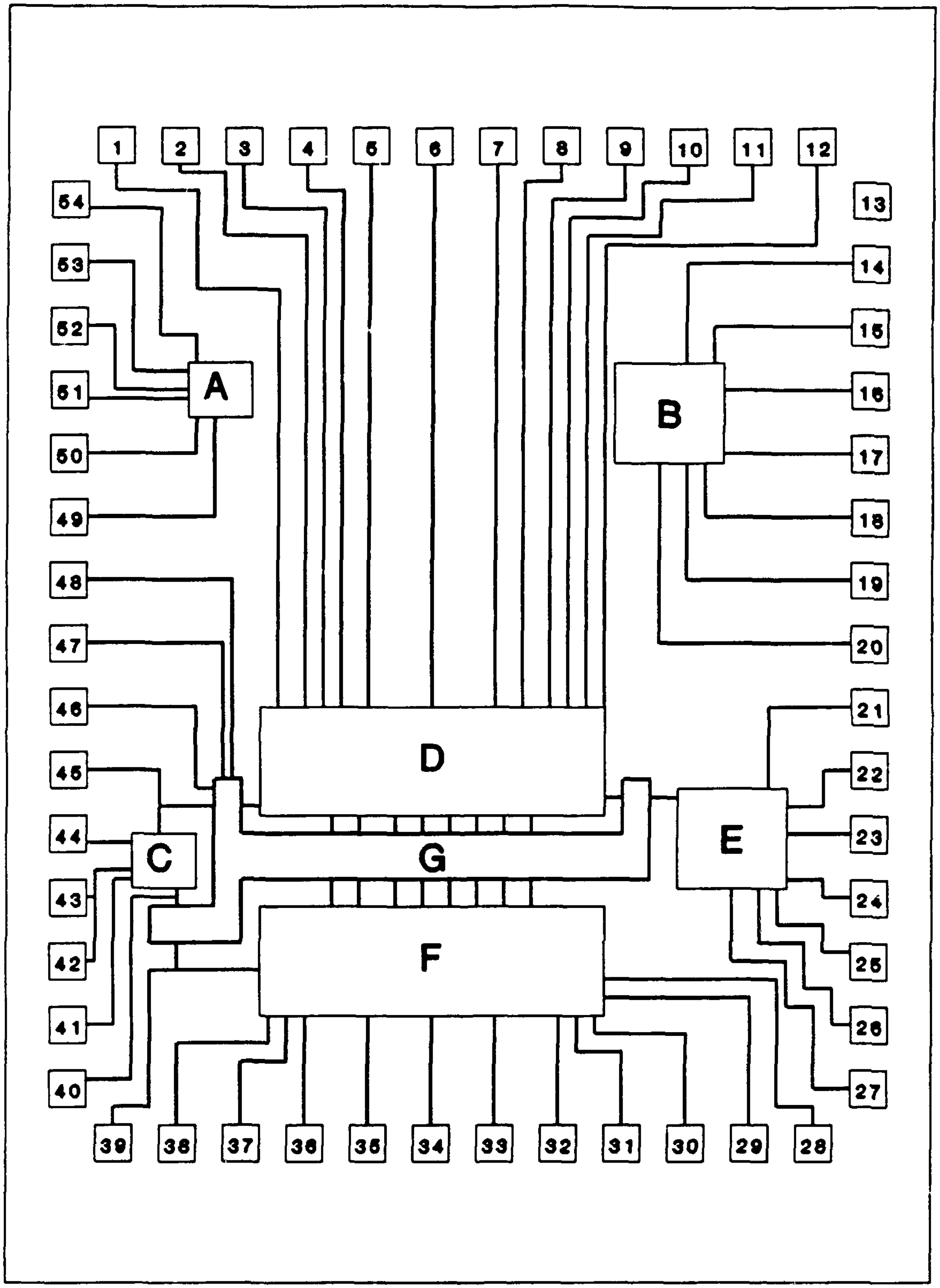


Figure 3.3. Baseline electrical circuit design floorplan. (A) Comparator, (B) 555 Timer, (C) Comparator, (D) Counter, (E) 555 Timer, (F) D/A Converter, (G) Isolator.

close to the analog output of the D/A Converter circuit. This feature should minimize the noise which is coupled to this signal. The fact that the Comparator output must be routed to the other end of the Counter is not as critical because it is a digital signal. Placing the Timer and Comparator on opposite ends of the layout also uniformly distributes the I/O pad requirements. The total pad requirements are listed in Table 3.1. Transmission gate Isolators controlled by an Enable signal are used to electrically isolate the subsystems on each IC die. This capability facilitates subsystem testing and characterization, and it also allows the same IC die to be used in the different WSI configurations. Second Comparator and 555 Timer circuits were added to the IC layout to provide the duplicate subsystems required for the single chip implementation variant of this WSI investigation. The square pads have a 200 micron length to accommodate limited misalignment, and the pads are separated by 100 microns. The resulting IC die size is 4.5 by 5.0 millimeters.

Counter Circuit Design. The Counter circuit design is a modified up-down counter to be used in an analog-to-digital (A/D) converter. The purpose of this circuit is to provide an eight bit digital signal that is compared through other circuitry to the analog input signal. The circuit has two inputs and two outputs. One input is the Clock signal. The other input, X, indicates whether the Counter should

Table 3.1. IC Bond Pad Requirements.

Bond Pad	Component	Signal Name	Bond Pad	Component	Signal Name
1	Counter	X	28	D/A Converter	Vdd
2	Counter	GND	29	D/A Converter	Vref
3	Counter	Q0	30	D/A Converter	Q7
4	Counter	Q1	31	D/A Converter	Q6
5	Counter	Q2	32	D/A Converter	Q5
6	Counter	Q3	33	D/A Converter	Q4
7	Counter	Q4	34	D/A Converter	Q3
8	Counter	Q5	35	D/A Converter	Q2
9	Counter	Q6	36	D/A Converter	Q1
10	Counter	Q7	37	D/A Converter	Q0
11	Counter	Data Ready	38	D/A Converter	GND
12	Counter	Clock	39	D/A Converter	Analog Out
13	Counter	Vdd	40	Comparator 1	Vdd
14	555 Timer 1	Vdd	41	Comparator 1	Analog Out
15	555 Timer 1	Reset	42	Comparator 1	Analog In
16	555 Timer 1	Control	43	Comparator 1	GND
17	555 Timer 1	R2	44	Comparator 1	Vbias
18	555 Timer 1	R1	45	Comparator 1	X
19	555 Timer 1	GND	46	Isolator	Vdd
20	555 Timer 1	Clock	47	Isolator	GND
21	555 Timer 2	Clock	48	Isolator	Enable
22	555 Timer 2	GND	49	Comparator 2	X
23	555 Timer 2	R1	50	Comparator 2	Vbias
24	555 Timer 2	R2	51	Comparator 2	GND
25	555 Timer 2	Control	52	Comparator 2	Analog In
26	555 Timer 2	Reset	53	Comparator 2	Analog Out
27	555 Timer 2	Vdd	54	Comparator 2	Vdd

increment up or down. By starting each conversion sequence with the Counter set to '10000000', each sequence requires only nine clock periods to perform the conversion. One output is the eight bit Counter value. The other output is a Data Ready bit that indicates when a result is available and the next input analog signal should be made available. Figure 3.2 illustrates the timing of the circuit. At the end of the first clock cycle, the second bit is set. Simultaneously, the first bit is cleared, if the input signal is low, or it is set, if the input is high. The second clock cycle results in setting the third bit and using the input to decide whether to set or clear the second bit. This sequence continues through the eighth clock cycle, where the input determines the state of the eighth bit, and the Data Ready bit is set. The Data Ready bit is cleared at the end of the ninth clock cycle, the Counter is reset to '10000000', and the overall sequence repeats itself for the next analog input signal.

The Counter circuit was designed using a state table approach, with the goal of determining a standard bit slice design. With a standard bit slice design, it is easy to adjust the resolution of the A/D converter by adding or subtracting bits. The basic building blocks of the Counter circuit include: the two-input NAND and NOR gates, the inverter, and the controlled inverter. From these basic gates, AND, OR and negative edge-triggered D flip-flop gates are constructed. Using state diagrams and Karnaugh maps, a standard bit cell composed of the gates described above was devised, called the LSB. The most significant bit required a unique cell, called the MSB. The original design required one MSB, 7 LSBs, one AND gate, and a D flip-flop. The AND gate and flip-flop provide the Data Ready circuitry.

Once this design was verified through VHDL, SPICE and ESIM simulations, the critical delay paths were examined to determine where improvements could be made. Two critical delay paths existed in the original circuit: a feedback loop with one AND gate from each bit slice connected in series, and a similar feedback loop composed of eight OR gates. It was found that by incorporating NAND and NOR gates in both of these feedback loops, the worst case propagation delay was reduced from 18 gate delays to 12. This modification required a slight deviation from the simple bit slice design. Instead of one standard bit slice, the modified design consisted of an odd bit slice and an even bit slice, as well as unique most significant bit and least significant bit microcells. The logic diagrams for the odd and even bit slices are presented in Figures 3.4 and 3.5, respectively. Figures 3.6 and 3.7 illustrate the logic diagrams for the most significant and least significant bit slices. A block diagram of the circuit is shown in Figure 3.8.

Table 3.2 describes the input signal designators utilized in the bit slice logic diagrams and the Counter circuit component block diagram. These diagrams also include three common output signal designators. Each of these signals is directly related to an input signal of a neighboring bit slice. For instance, the output QXP of each bit slice connects directly to the QXN input for the next lower significant bit. The outputs QORN and NQANDN connect directly to the QORP and NQANDP inputs, respectively, for the next higher significant bit.

Table 3.2. Input Signal Designators for Bit Slice Diagrams.

Signal	Description
Clock	Externally generated clock signal from Clock circuit
QORP	OR gate feedback path from lower significant bit
NQANDP	AND gate feedback path from lower significant bit
QXN	Bit value from next higher significant bit
QDR	Data Ready signal
NQDR	Complement of the Data Ready signal
X	External input to Counter circuit from Comparator circuit

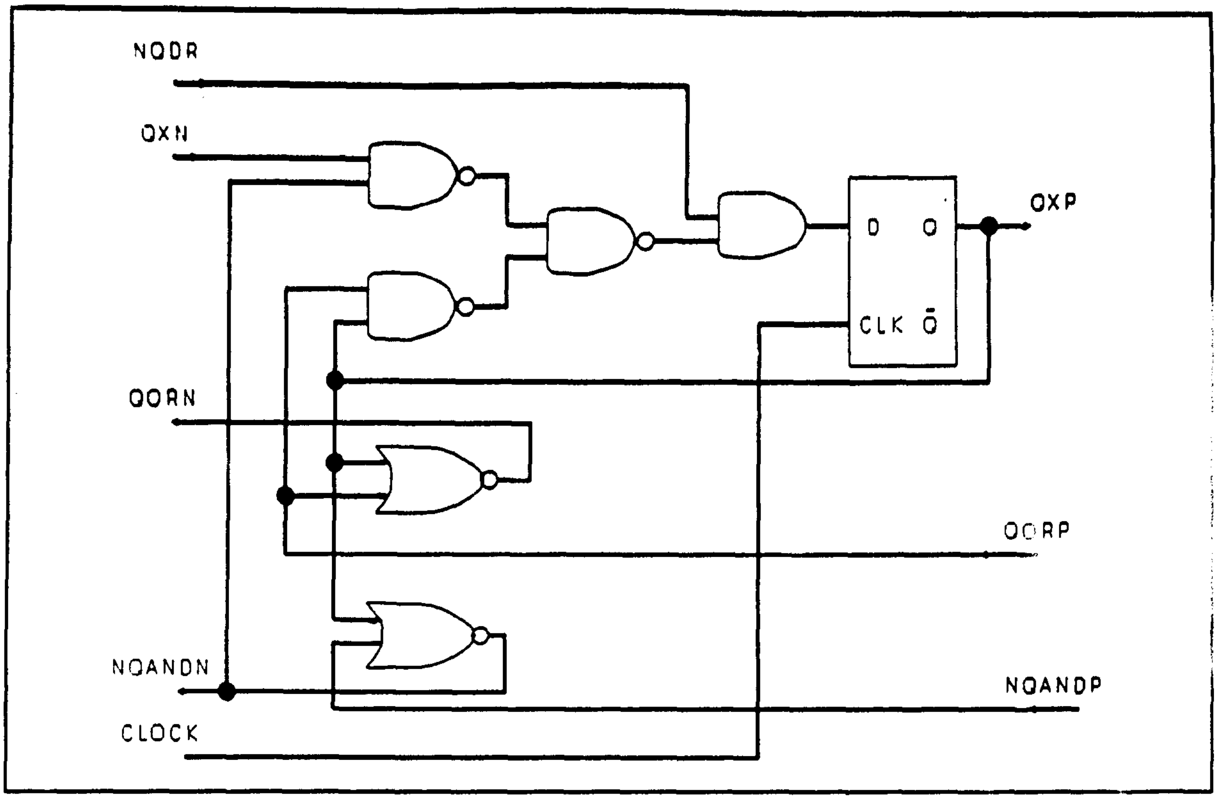


Figure 3.4. ODDBIT bit slice logic diagram.

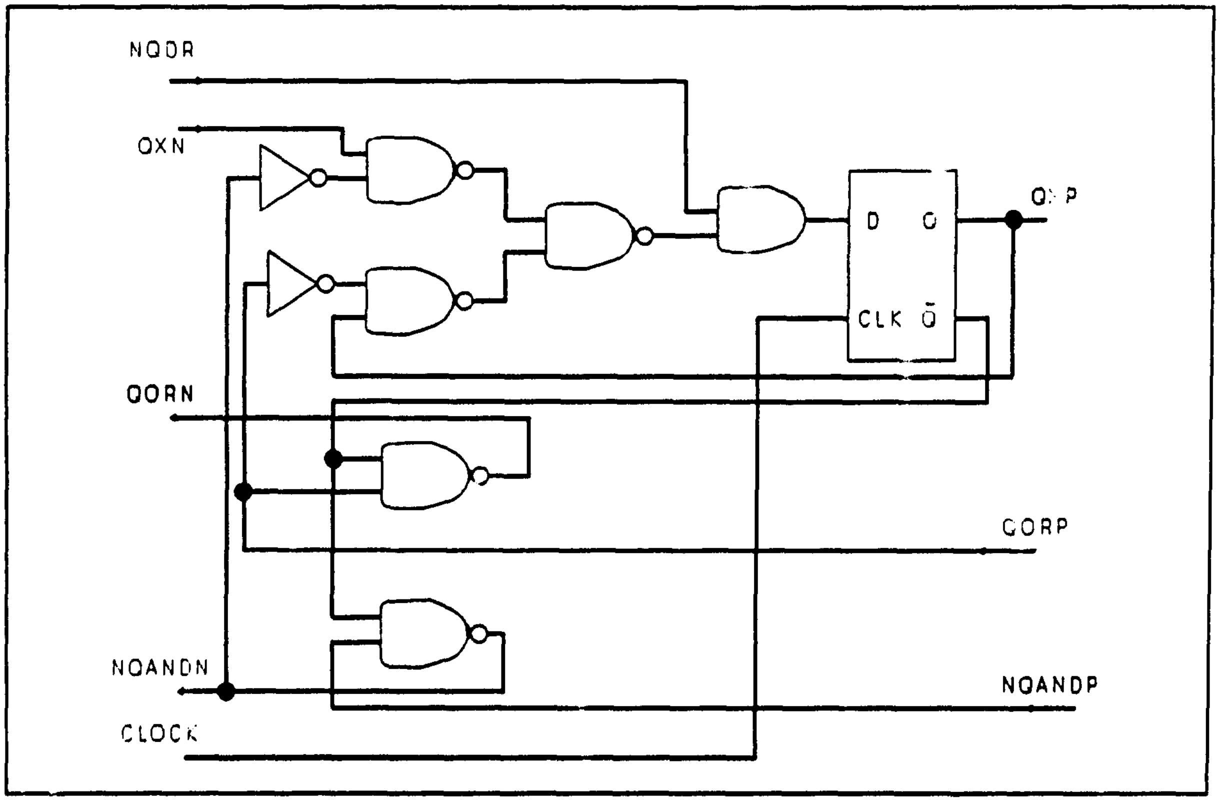


Figure 3.5. EVENBIT bit slice logic diagram.

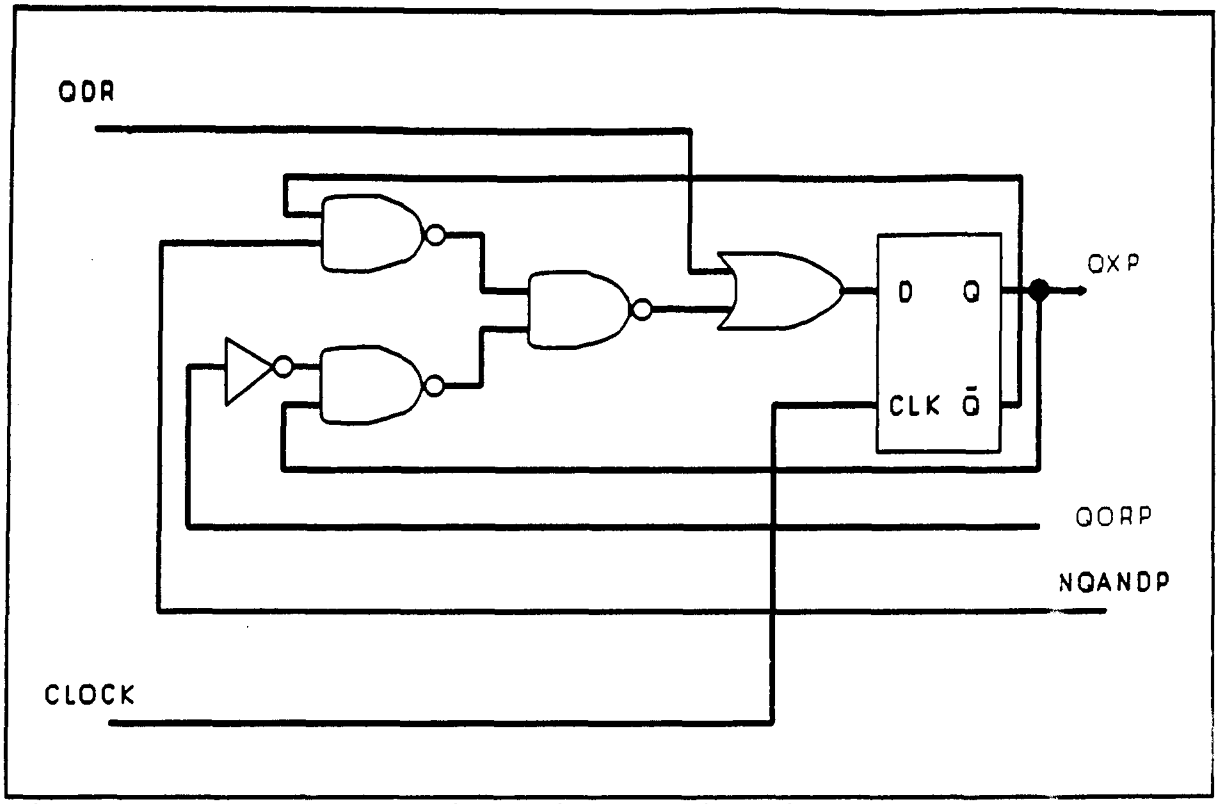


Figure 3.6. MSBBIT bit slice logic diagram.

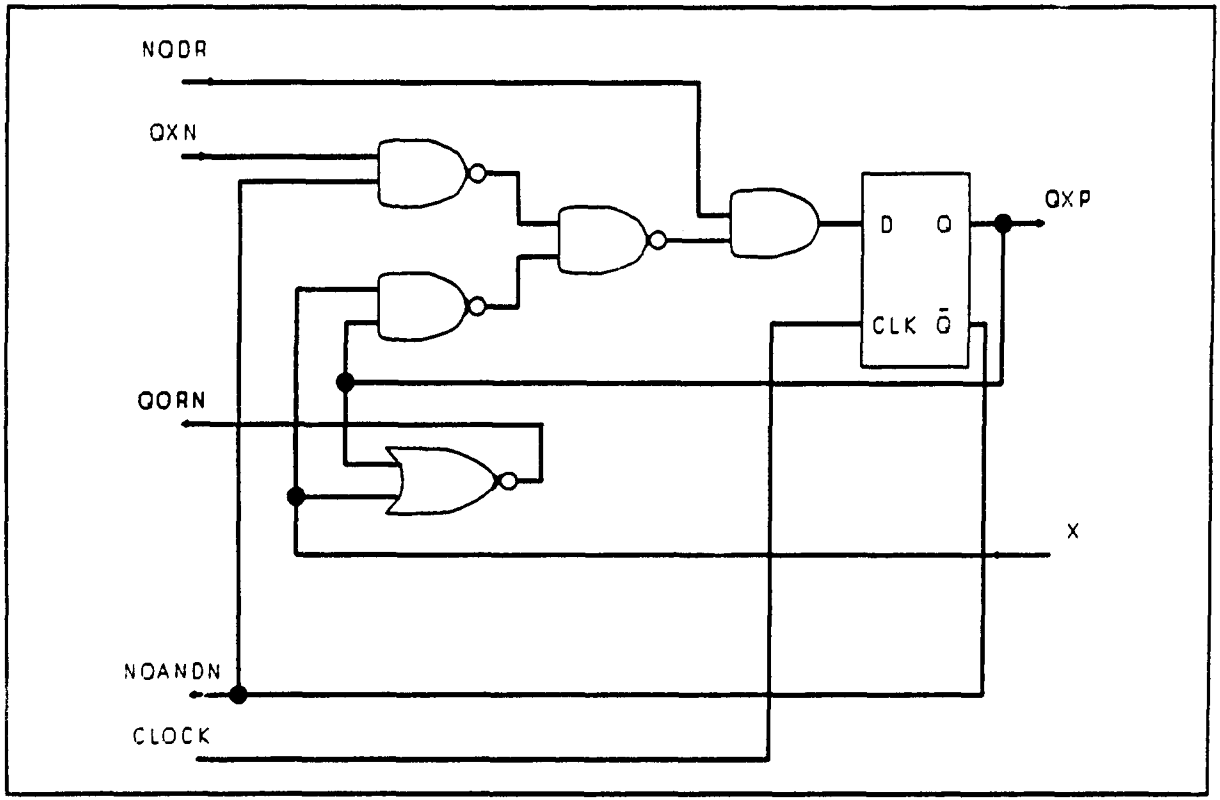


Figure 3.7. LSBBIT bit slice logic diagram.

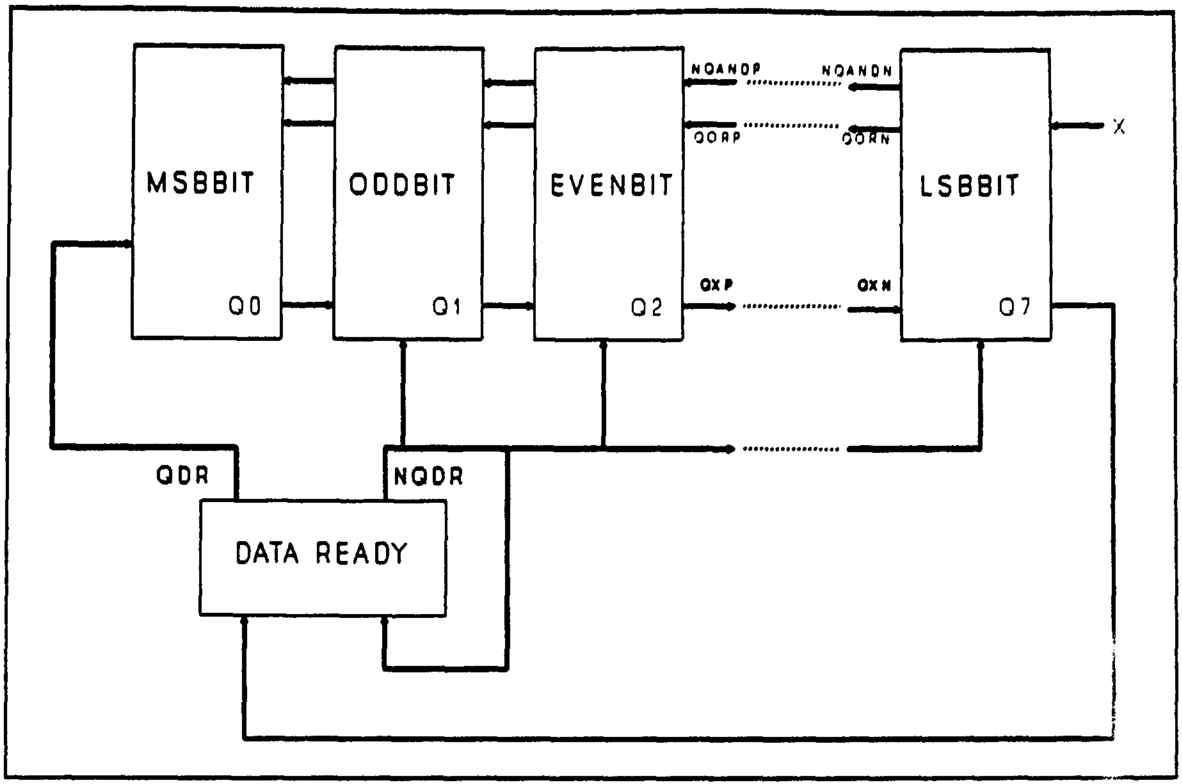
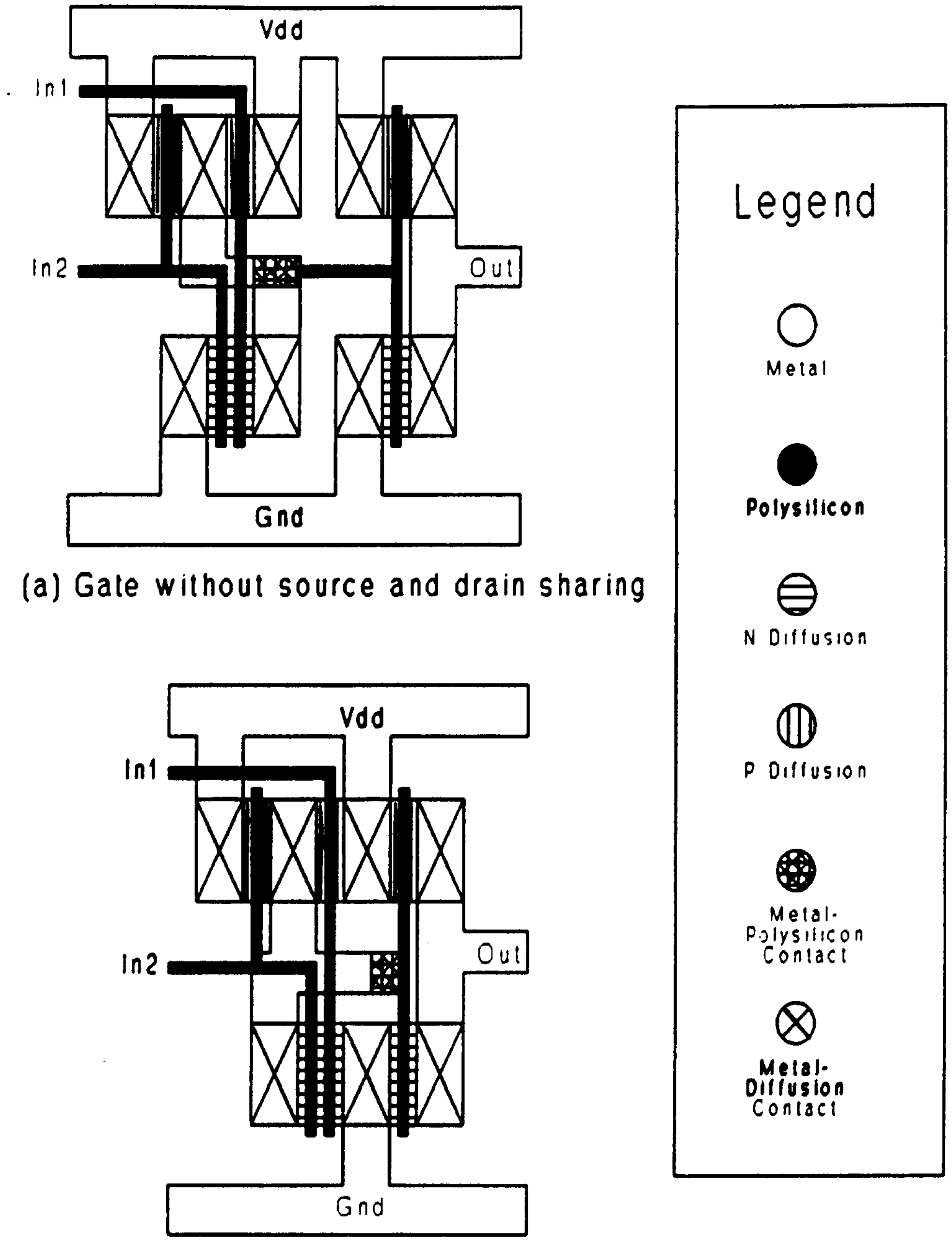


Figure 3.8. Counter component block diagram.

The redesign of the Counter circuit critical paths resulted in an overall reduction in logic elements. Reductions in the size of the Counter circuit layout were also realized by employing MOSFET source and drain sharing techniques. Figure 3.9 illustrates an example of gate layout design using these techniques. In Figure 3.9 (a), a two input AND gate is constructed by connecting independent AND and inverter gates. In Figure 3.9 (b), the same logic gate is realized with fewer connections from the diffusion regions to Vdd and Gnd. The second design requires less area compared to that of the first layout. In the case of the Counter circuit, the layout, in which the logic reduction, and source and drain sharing techniques were employed,



(a) Gate without source and drain sharing

(b) Gate with source and drain sharing

Figure 3.9. Example of source and drain sharing techniques utilized in a MOSFET AND gate design.

required approximately 33 percent of the area required by the original circuit design.

The operation of this circuit was validated with the VHDL, ESIM and SPICE simulation software tools. The VHDL model utilized NAND, NOR, inverter and controlled inverter behavioral descriptions as basic building blocks. The entire VHDL description consisted of structural combinations of these basic gates. Appendix A contains the VHDL models used in the simulations and several sample simulation results. The ESIM model was extracted directly from the circuit layout design. Appendix B contains the results of an ESIM simulation, which analyzed the logical operation of the circuit layout design. Both the VHDL and ESIM results agreed with the anticipated functionality of this component.

SPICE simulations were used to calculate expected propagation delays in the Counter subsystem. The SPICE models are presented in Appendix C. SPICE models were simulated for the basic gates used to construct the Counter. The entire circuit was also successfully implemented and verified with the SPICE simulation software tool. Because of the circuit complexity and memory constraints on the computer workstation, simulations were limited to three clock cycles. Different bits were tested by varying the input signals and the initial conditions. A summary of gate delays computed from the SPICE simulations is presented in Table 3.3. The D flip-flop set-up time is the minimum period for which the input signal must be stable before the clock pulse falling edge occurs. The D flip-flop output delay time indicates the delay measured from the falling edge of the clock pulse to a stable output signal from the flip-flop. Figure 3.10 illustrates the worst case propagation delay path through the Counter subsystem combinational logic. Assuming the X input was available immediately after the eight-bit output was stable, the signal must propagate through twelve basic gates, and be stable for the D flip-flop set-up time. The total worst case delay is the sum of these delays added to the D flip-flop output delay, which equals 18 nanoseconds, as indicated in Table 3.3.

Table 3.3. Delays From the SPICE Simulations.

Delay Description	Delay Time (ns)
Basic Gates (NAND, NOR, Etc)	1
D flip-flop set-up time	4
D flip-flop output delay	2
Worst case combinational logic propagation delay	12
Minimum clock period	18

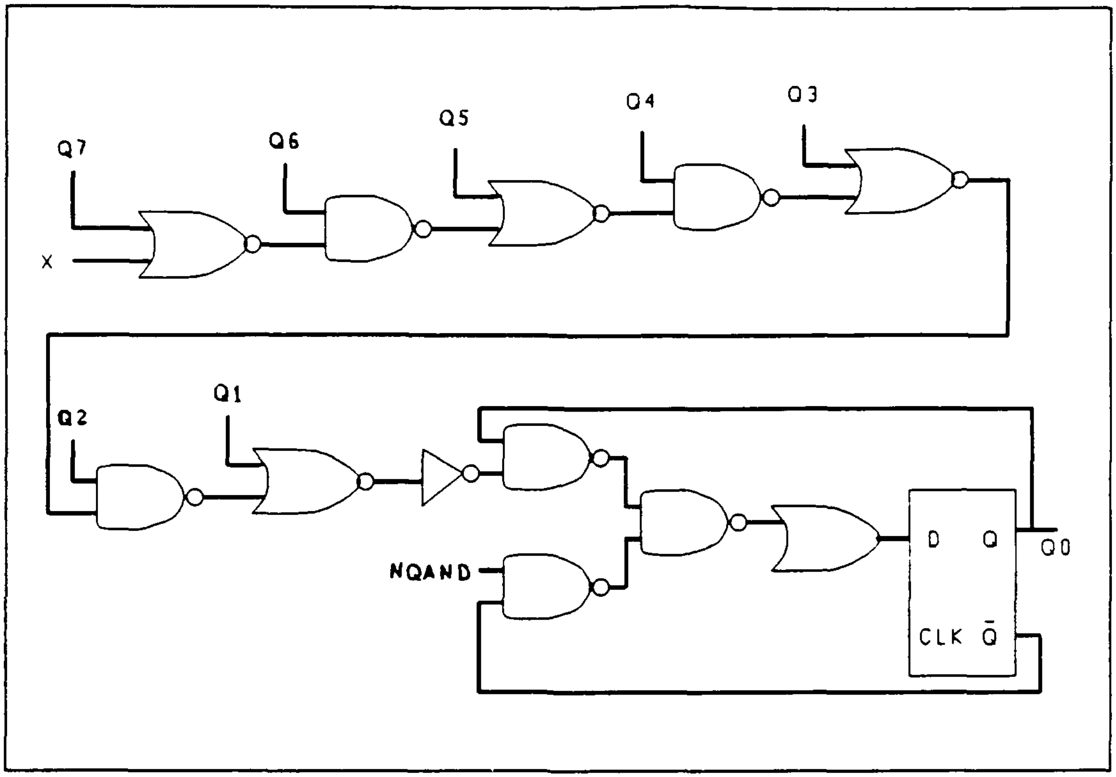


Figure 3.10. Worst case propagation delay path in the counter circuit.

<u>Digital-to-Analog Converter Design</u>. The baseline digital-to-analog (D/A) Converter design is illustrated in Figure 3.11. This approach utilized is known as a ladder network, and it relies upon resistor ratios to establish the bit values. An alternative approach, which only requires half the number of resistors, was also considered. However, this method uses binary weighted resistors, and it requires each resistor to be twice the value of the resistor at the next higher significant bit location. This method would require the same IC layout area, and its performance would be more sensitive to variations in the actual resistor values.

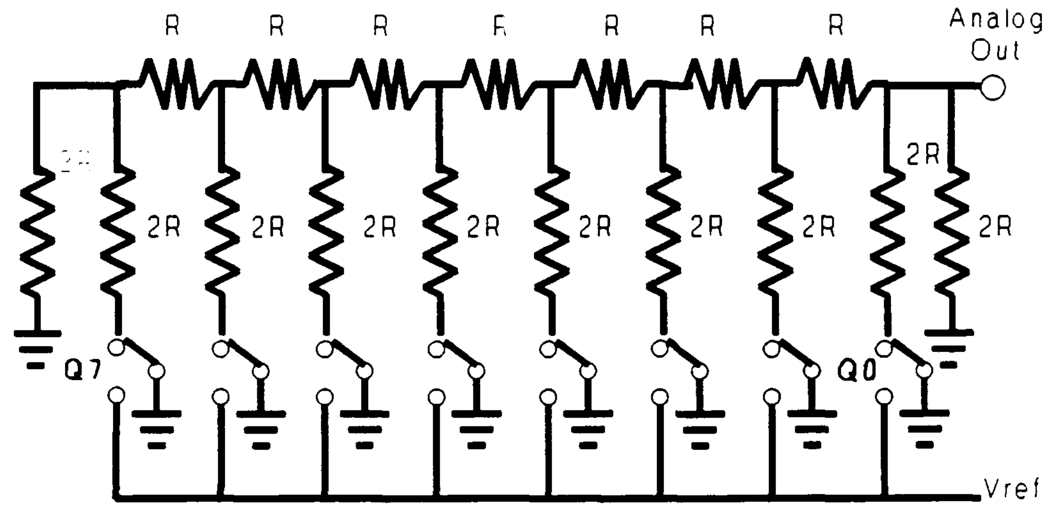


Figure 3.11. D/A converter design.

The D/A Converter circuit consists of a ladder network of ratioed resistors. The minimum value of Analog Out, 0 volts, occurs when the eight bit digital input is '00000000', which is equivalent to decimal '0'. Each incremental change in Analog Out is equal. Therefore, the value of Analog Out corresponding to a specific eight bit digital input can be calculated by multiplying the Analog Out incremental value by the decimal equivalent of the digital input. For example, the decimal equivalent for the maximum value digital input

'11111111' is 255. the maximum output can then be determined by:

$$\text{Analog Out}_{max} = (255)\text{Analog Out}_{inc} \qquad (3.1)$$

where

Analog Out_{inc} is the Analog out voltage increment
Analog Out_{max} is the magnitude of Analog Out when the input signal is '11111111'.

The simplest method of determining the voltage range of the device is to examine the equivalent circuit when Q0 is set to a logic one and all the other bits are set to logic zero. The decimal equivalent to this digital input, '10000000', is 127. The equivalent circuit is illustrated in Figure 3.12. Using network analysis, Analog Out_{127} can be computed as (26:609):

$$\text{Analog Out} = (127)\text{Analog Out}_{inc} = (1/3)\text{Vref} \qquad (3.2)$$

Solving for Analog Out_{inc}:

$$\text{Analog Out}_{inc} = (1/127)(1/3)\text{Vref} \qquad (3.3)$$

Therefore, for a given value of Vref, Analog Out_{inc} and Analog Out_{max} can be calculated using Equations 3.3 and 3.1, respectively.

This circuit could not be tested using the VHDL or ESIM software simulation tools because it is analog variant. However, SPICE simulations were used to verify the circuit's

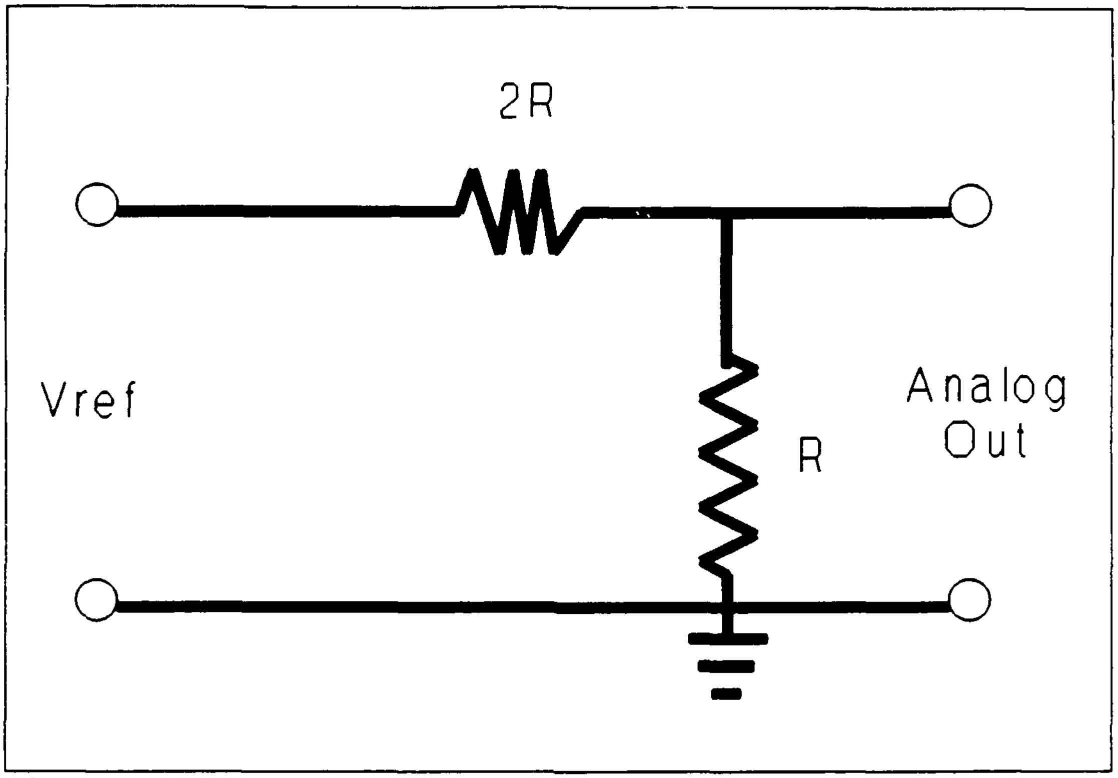


Figure 3.12. Equivalent circuit for D/A Converter with input '10000000'.

operation and to determine appropriate resistor values and transistor geometries. The SPICE models are presented in Appendix C. The switch design was simply two inverters, with the p-channel transistor source of the second switch tied to the reference voltage input, rather than Vdd. This design is illustrated in Figure 3.13. To conserve area, the original design parameters were minimum size inverters, and the resistor values were on the order of 500 ohms. This design resulted in non-linear voltage steps due to the circuit's sensitivity to the resistance of the switches. Therefore, the resistor and transistor parameters were incrementally increased to values of 5000 ohms for the resistor, R, and 30

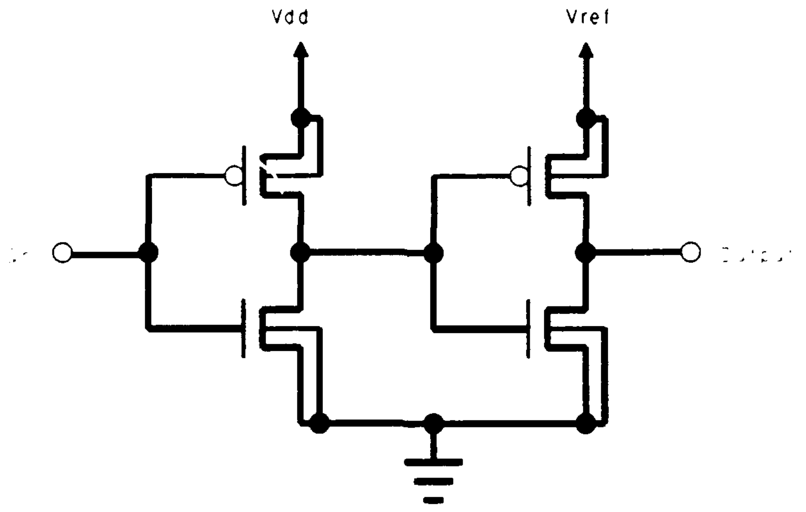


Figure 3.13. Switch design for D/A Converter circuit.

and 90 microns for the n-channel and p-channel gate widths, respectively, in each transistor. These transistor and resistor values produced a D/A Converter with linear voltage outputs over the entire digital input vector range. A summary of the SPICE results for the circuit incorporating the modified transistor and resistor design is presented in Table 3.4.

The final values for the resistors and transistors in Table 3.4 produced the desired linearity in the Analog Out increments. However, the SPICE simulation values for Analog Out_{inc} and Analog Out_{max} were not equivalent to the calculated

Table 3.4. SPICE Simulation Results for the D/A Converter Sizing.

R value (Ω)	N-channel Width (μm)	P-channel Width (μm)	Typical Voltage step (mV)	Worst Case Voltage step (mV)
500	6	15	20	-66
1500	6	15	22	8
1500	24	50	17	7
2500	24	50	16.5	10
2500	30	90	15.5	12
5000	30	90	15	14

values. Using Vref equal to ten volts, the calculated values of Analog Out_{inc} and Analog Out_{max} are 26.25 mV and 6.693 V, respectively. As Table 3.3 illustrates, Analog Out_{inc} equals 15 mV, and Analog Out_{max} equals 3.825 V from the SPICE simulation. These discrepancies are attributed to incomplete switching of the second inverter in the digital switches, and the resistance within the inverter between the output and Vref or ground.

Polysilicon resistors were used in the D/A Converter design because they require less area compared to the equivalent value realized with a thermal diffusion or ion implant process. Using a minimum line width, the required resistor length was computed using a sheet resistance value supplied by the MOSIS vendor, using the relationship:

$$L=R\left(\frac{W}{R_s}\right) \qquad (3.4)$$

where

R is the required resistance value, in ohms
W is the resistor width, in microns
R_s is the sheet resistance of the resistor material, in ohms per square
L is the required resistor length, in microns.

The length of the resistor cell was matched to the Counter bit slice length, and the width was determined by the overall required resistor length. The digital switch layout was also sized to match the dimensions of the Counter bit slice.

Comparator Design. Figure 3.14 depicts a two-stage Comparator circuit. This circuit requires seven MOSFET transistors, labeled M1 through M7 in Figure 3.14. The key aspect in designing this subsystem is that, regardless of the magnitude of the difference between the two analog inputs, the output must be above 4 volts for a digital one, or below 1 volt for a digital zero. The design does not allow the output to be at an intermediate value when the two inputs are nearly equal.

The baseline Comparator was a single stage circuit similar to that used in the CMOS sense amplifiers. This Comparator's performance was simulated with SPICE. When this circuit was tested separately, driven by two ideal voltage sources, the optimum design was manifested for low resistance

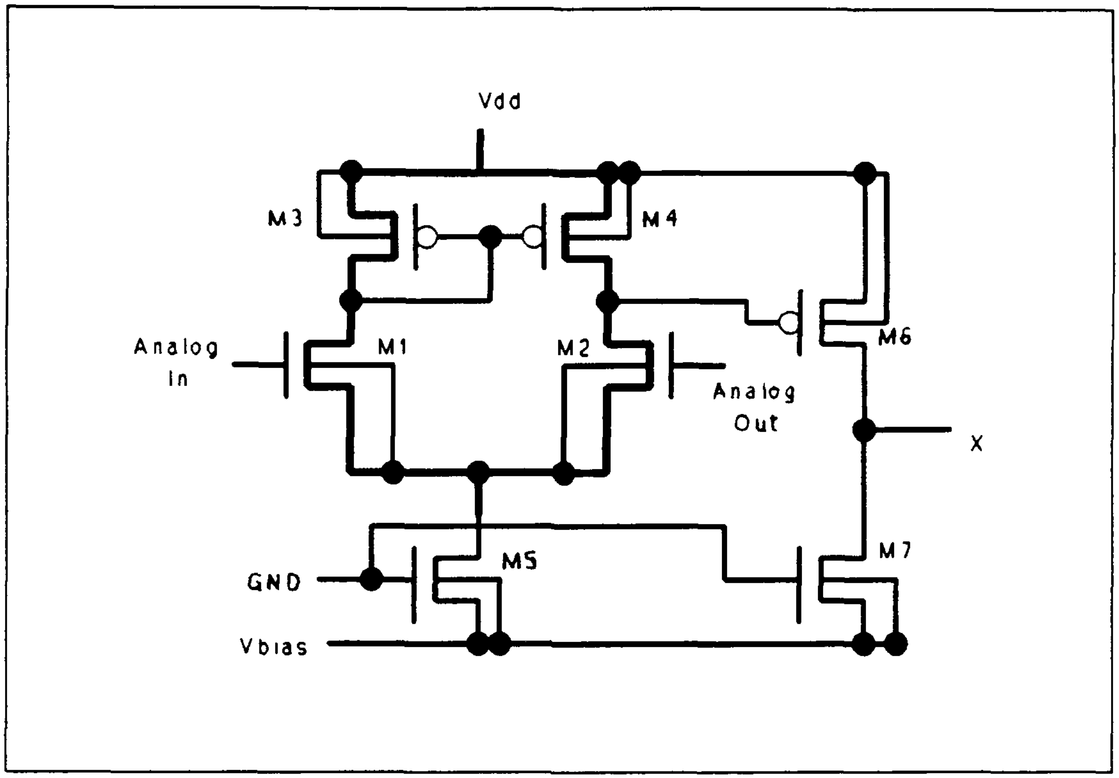


Figure 3.14. Comparator design.

n-channel transistors to improve the switching speed. However, when this simulation was repeated with the D/A Converter driving one input, it was found that a high resistance n-channel was needed to prevent undesirable interaction with the network. Consequently, the initial Comparator design failed to function properly. To function properly, the Comparator should switch between a one and zero output when the difference between the input voltages is less than Analog Out$_{inc}$. Simulations of the Comparator, using the D/A Converter as one input, indicated that, to satisfy these voltage switching requirements, the gate widths of the n-channel transistors had to be on the order of 200 microns.

The corresponding switching times were on the order of 50 nanoseconds, and the output voltage was in the intermediate range when the inputs were nearly equal.

The Comparator design was modified to the two-stage Comparator circuit shown in Figure 3.14, which resulted in improved switching times and more reasonable transistor sizes. Switching times for this circuit design were on the order of 20 nanoseconds. The output signal produced by this design switched from 1 volt to 4 volts in the worst case. SPICE models for the Comparator circuit are presented in Appendix C. This circuit was simulated in SPICE with the D/A Converter output connected as one input, and an ideal voltage source served as the second input. The output was driving an inverter circuit, and it was found that the device could operate for the full analog input range of 0 to 4 volts when Vdd = 5 volts, and Vbias = -4 volts. The transistor sizes developed through the SPICE simulations are summarized in Table 3.5.

Timer Design. The 555 Timer is a standard design, as depicted in Figure 3.15. Ports are included to facilitate external connections of the resistors, R1 and R2, and the capacitor, C0, which establish the clock's pulse width and period. The output of the clock in the original design was driving a large capacitive load (9:Sec 4,17); thus, the layout included a robust level of output buffering. This

Table 3.5. Comparator Transistor Sizes.

MOSFET Transistor	Gate Width (μm)	Gate Length (μm)
M1	10	4
M2	10	4
M3	5	3
M4	5	3
M5	5	4
M6	30	3
M7	15	4

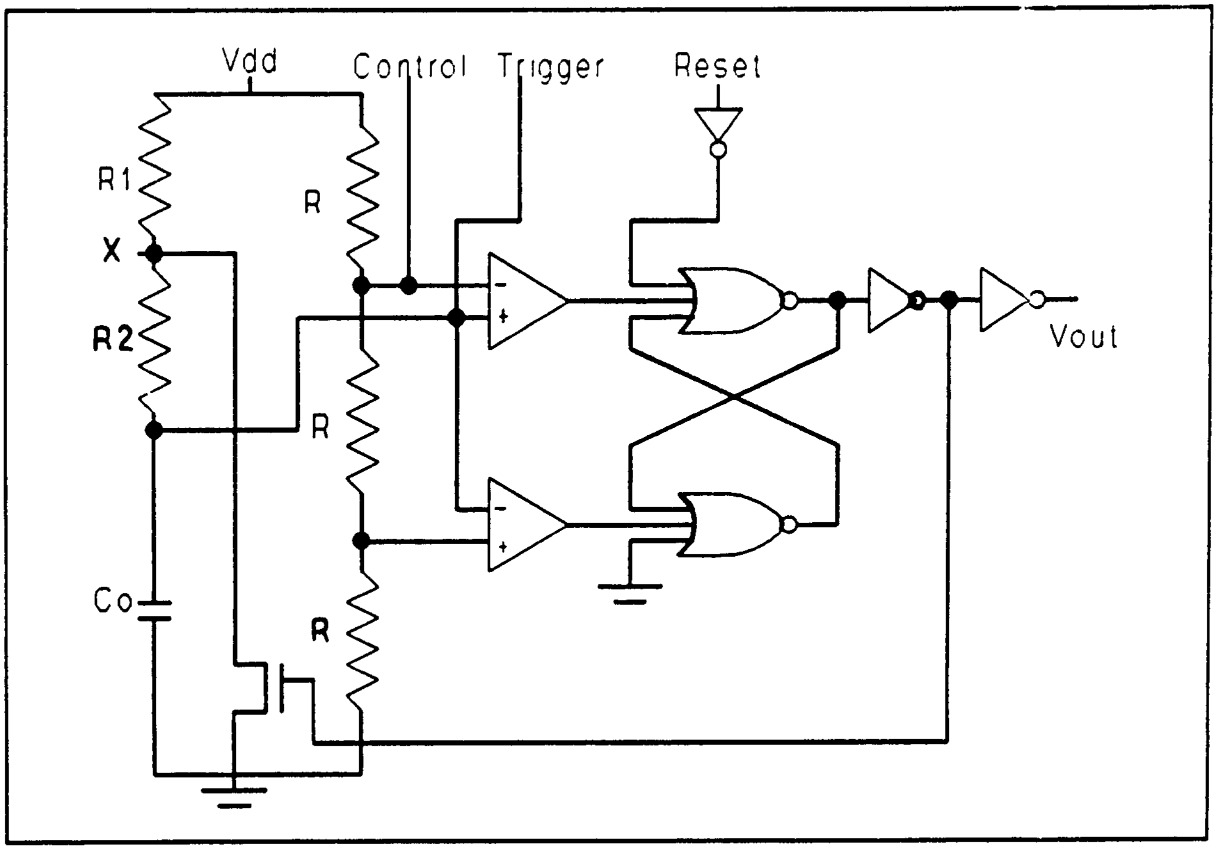


Figure 3.15. Clock design.

capability also satisfies the load requirements of the Counter circuit.

The design of this subsystem was the result of a previous effort. Captain Robert Fitch designed this 555 Timer as part of a piezoelectric robotic tactile sensor IC design (9:Sec 4,13). This circuit was fabricated, tested and operationally verified by Capt Fitch as part of his research. Because this subsystem is an analog circuit, it can not be simulated using either ESIM or VHDL. However, the circuit was modelled and simulated with the SPICE simulation tool. The SPICE models are presented in Appendix C.

The layout of the previous design was modified to be more compatible with the A/D system being designed. The first modification was the replacement of the diffusion resistors with polysilicon resistors, to reduce the design's layout area. Second, the placement of the individual microcells of the subsystem were rearranged to reduce void regions and make the layout more compatible with the other A/D circuit subsystems.

Summary

This chapter discussed the process which was used to develop the A/D converter system IC design. This system consists of four distinct subsystems: the Counter, the D/A Converter, the Comparator, and the 555 Timer. Analog and digital signals are required to connect these subsystems.

Because the majority of the subsystems were not purely digital in nature, simulation and design verification were limited to parametric analyses using SPICE. Design verification of the physical system layout was not possible with the MAGIC software tools or with the standard logic circuit extraction tools.

IV. Experimental Procedures

To evaluate the characteristics of the proposed hybrid WSI configurations, test circuits were fabricated and electrically tested. Before these circuits were fabricated, preliminary studies were conducted to select appropriate procedures and materials. The first section of this chapter describes the procedure used to evaluate candidate techniques to accomplish planar IC die mounting in the host substrate. The procedure for evaluating candidate polyimides as the interlayer dielectric is presented in the second section of this chapter. The third section describes the fabrication procedures used to realize the test circuits, followed by a presentation of the procedures used to electrically characterize the interconnect structures.

Evaluation of IC Die Mounting Procedures

Mounting the IC die in the host substrate is a critical step in hybrid WSI circuit fabrication. The level of success in this step determines the quality of IC die alignment and planarity. As described in Chapter II, different techniques have been employed and proposed in a number of research efforts. This study focused on recommendations aimed at improving the basic procedure used by previous AFIT researchers.

Figure 2.4 shows a cross-sectional diagram of the IC die mounting fixture used in previous AFIT research. As this figure illustrates, gaps between the host substrate walls and the IC die exist which allows the IC die bonding material to contact the reference flat surface. Different techniques have been employed to prevent adhesion of the IC die bonding material to this surface, as reported in Chapter II. The use of an optical flat as the reference surface provided a smooth surface which remained undeformed when heat was applied. However, the epoxy used as the IC die bonding material readily adhered to this surface, requiring repeated cleaning during the cure process. To eliminate adherence between the epoxy and the reference flat surface, a polished Teflon® block was substituted for the optical flat (10:38). However, this block tended to warp when the epoxy's cure temperature was established, resulting in poor planarity in the mounted IC die.

Barrier Coating Evaluation. This evaluation examined the utility of an optical flat coated with a barrier material designed to reduce or eliminate adhesion between the epoxy and the alignment surface. A list of the candidate coating materials is presented in Table 4.1. The first four candidates listed were selected based upon their potential ability to resist adhesion by the epoxy. The last two candidates differ in that adhesion between the epoxy and the coating is anticipated. These coatings were intended to act

Table 4.1. Candidate IC Die Mount Barrier Materials.

Manufacturer	Material	Application Method
Fluorglas	TFE (Teflon®) Spray	Spray
Crown	Epoxy Mold Release	Spray
Miller Stephenson	MS-122 Release Agent	Spray
Miller Stephenson	MS-145 Release Agent	Spin
Shipley	1815 Positive Photoresist	Spin
Ultradel	4501 Polyimide	Spin

as sacrificial layers, preventing direct adhesion to the optical flat. Once the epoxy was cured, these sacrificial layers would be dissolved in an appropriate solution to separate the IC die and host substrate assembly from the optical flat.

The first test involved coating one side of a clean optical flat with a candidate material. As Table 4.1 indicates, the first three candidates were applied using a spray technique. In each case, the optical flat was placed in a vertical orientation approximately six inches from the coating container's spray nozzle. During the spray process, the nozzle was moved across the optical flat's surface to provide an even coating. After the spray process was completed, the surface of the optical flat was gently wiped with a soft cloth to remove the excess material.

The three candidates listed at the bottom of Table 4.1 were applied using a spin coat technique. In each case, the optical flat was placed on the photoresist spinner vacuum chuck. Approximately 4 ml of the sacrificial barrier material was dispensed in the center of the flat, which was then spun for 30 seconds at the following rate: 1000 rpm for the release agent, 4000 rpm for the photoresist, and 2000 rpm for the polyimide. The surface of the flat coated with the release agent was gently wiped with a soft cloth to remove the excess material.

The surface profile for each coating was measured using the Dektak profilometer to determine the influence of the coating on surface smoothness. The optical flat was then placed on a 175°C hot plate (the IC die bonding epoxy cure temperature). To mimic the IC die-to-host substrate epoxy bonding process, two metal washers were placed one inside the other at the center of the optical flat. Epoxy was placed in the gap between the washers and allowed to cure for 30 minutes. Once the epoxy cure was complete, the optical flat was removed from the hot plate and allowed to cool to room temperature. Adhesion of the washers to the optical flat was tested by prying the washers from the optical flat.

<u>Alternate IC Die Mount Procedures.</u> In addition to demonstrating the qualifications of the coatings, the barrier coating evaluation demonstrated important properties of the epoxy during cure. As the epoxy was heated, it became very

fluid in a matter of seconds. As the cure process proceeded, the epoxy became more viscous after approximately five minutes. While the epoxy was in its fluid state, it tended to flow out of the gap region, covering the surfaces of the washers and the glass plate. An epoxy coating with this characteristic would insulate the bond pads on the IC die surface from the metal interconnects. Thus, this evaluation demonstrated the need to minimize the flow of the epoxy over the IC die and the host substrate surfaces, in addition to controlling adhesion to the reference flat. Four alternative IC die mount procedures were devised and evaluated.

Epoxy IC Die Mounting with a Clamped Substrate. A jig was fabricated for use as a clamping fixture for the IC die mounting process. Figure 4.1 depicts the jig. In this procedure, the first step involved the placement of a Teflon®-coated optical flat on the 175°C hot plate. An etched host substrate was then placed on the optical flat, and an IC die was placed in the host's etched cavity. The clamping device was then tightened, mating the host substrate and optical flat. Epoxy, heated to approximately 100°C in a separate container, was applied to the gap regions between the IC die and substrate with a micro-syringe. After five minutes, the clamp was loosened, and the optical flat and host substrate were removed from the hot plate. After the assembly cooled, the host substrate and IC die were examined for excess epoxy on their surfaces. Excess epoxy was removed

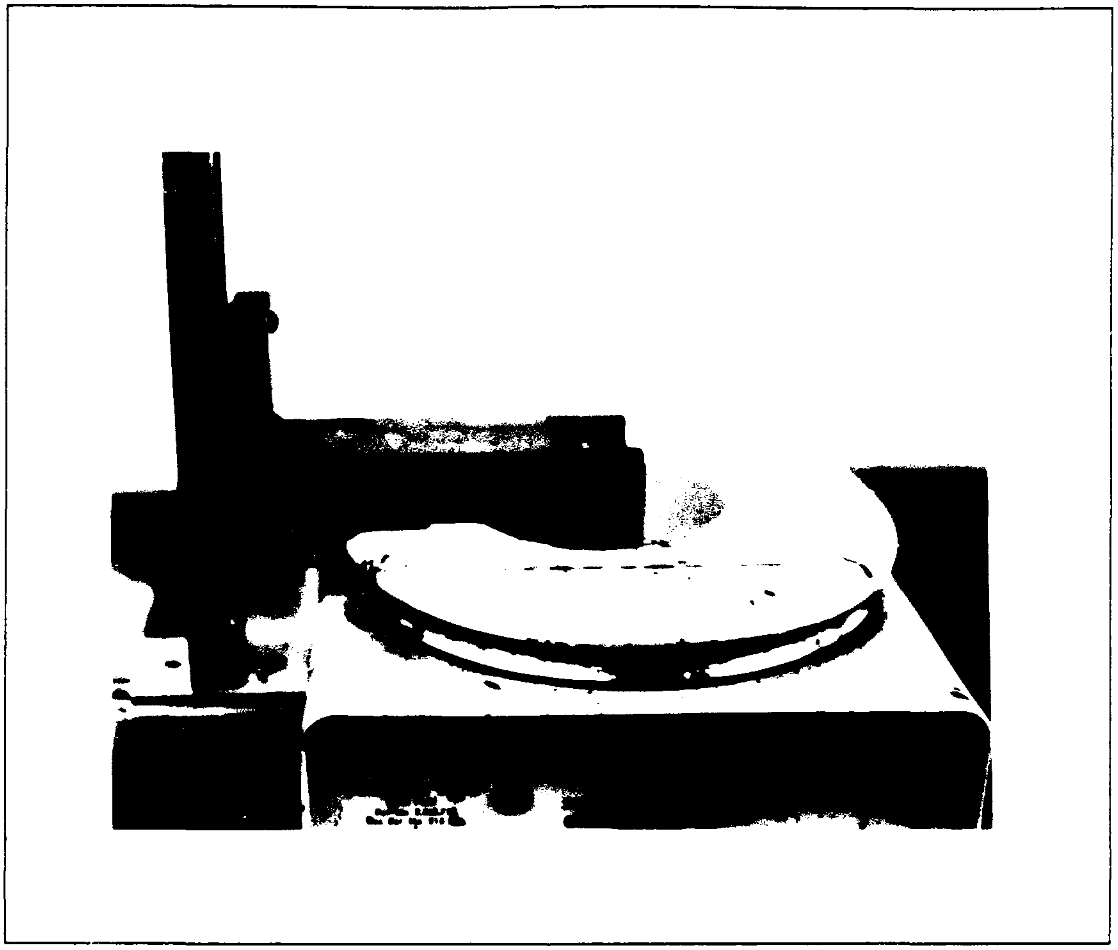


Figure 4.1. Clamping jig used in the IC die mounting experiments.

from these surfaces with an acetone-saturated swab. These steps were repeated until no excess epoxy appeared on the optical flat's surface.

Polyimide IC Die Mounting with a Clamped Substrate. An alternative procedure involved substituting polyimide as the IC die bonding material and photoresist as the barrier coating on the optical flat. The Shipley 1815 positive photoresist's hardbake temperature is 100°C, and the Ultradel 4501 polyimide's softbake temperature is 70°C. The clamping jig was used in this procedure, and the assembly procedure was the same as that described in the previous procedure. In this alternative procedure, the hot plate was heated to 70°C, and heat was applied to the clamped assembly for 15 minutes. Because the polyimide also flowed from the gap region, the host substrate and IC die assembly adhered to the optical flat. After cooling, this assembly was soaked in photoresist developer to dissolve the photoresist sacrificial coating.

Substrate Pre-Assembly Procedure. As stated in Chapter III, one alternative approach to the IC die mounting step in the WSI fabrication process is to mount the IC die in the host substrate's cavities rather than in ports completely etched through the host substrate. Because the thickness of the IC die used in this research effort closely matched the host substrate's thickness, the cavities were micromachined by etching ports completely through the host substrate, and then bonding the host and support substrates together before placing the IC die in the cavities.

The first step in this procedure involved coating the backside of the host substrate with a thin, even layer of the epoxy. The two substrates were then joined and clamped between two optical flats. This assembly was placed on a 175°C hot plate for ten minutes. After the assembly was removed from the hot plate and allowed to cool, the clamps and optical flats were removed. The surfaces of the optical flats and the substrates were cleaned with acetone to remove excess epoxy. In addition, a cotton swab saturated with acetone was used to remove epoxy from the IC die cavity. The substrates were again placed on the hot plate between the two optical flats and cured at 175°C for an additional 60 minutes.

Once this cure process was complete, the substrate assembly was removed from the hot plate and allowed to cool. A thin coating of epoxy was applied to the bottom and side-wall surfaces of the substrate's cavity and the appropriate IC die was inserted. This assembly was clamped together between two optical flats and placed on the 175°C hot plate for ten minutes. After the assembly was removed from the hot plate and allowed to cool, the IC die, substrate and optical flat surfaces were cleaned with acetone to remove excess epoxy. The substrate was again placed between the two optical flats on the hot plate and cured for an additional 60 minutes. During this epoxy cure cycle, a four-inch diameter, 1.0 kg weight was placed on the top optical flat to provide a leveling force on the assembly.

Single-Step IC Die Mount Procedure. The preceding procedure consisted of an epoxy cure step which was performed twice; first, to bond the substrates together, and second, to mount the IC die. This final IC die mount procedure evaluated the effect of combining these two steps.

In this modified procedure, the first step involved placing the host substrate, polished side down, on an optical flat. The IC die was placed in the host substrate's etched cavity. Next, one side of the support substrate was coated with a thin layer of epoxy. The two substrates were then joined and clamped between two optical flats. This assembly was placed on a 175°C hot plate for ten minutes, with the IC circuit facing down to promote planarization. After the assembly was removed from the hot plate and allowed to cool, the optical flat and substrate surfaces were cleansed with acetone to remove the excess epoxy. The WSI assembly was placed, uncovered, on the hot plate for two minutes to promote the final cure of the epoxy in the gap region. The assembly was then removed from the hot plate, and acetone was used to remove the excess epoxy from the IC die and host substrate surfaces. The assembly was again placed between two optical flats on the hot plate for the final 60 minute cure. During this cure, the four-inch diameter, 1.0 kg weight was placed on the top optical flat to provide a leveling force.

Polyimide Evaluation Procedure

The intent of this study was to evaluate three polyimide materials to be used as the interlevel dielectric in the WSI assemblies. Table 4.2 lists the three candidate materials and typical properties reported by the respective manufacturers. Selectilux HTR3-200 was chosen based upon its successful use in previous AFIT research. The two Ultradel

Table 4.2. Properties of Candidate Polyimides (14,42,43).

Characteristic Parameter	Ultradel 4212 (Non-photo-sensitive)	Ultradel 7501 (Photo-sensitive)	Selectilux HTR3-200 (Photo-sensitive)
Relative Dielectric Constant, 1MHz	2.9	2.8	3.8
Dissipation Factor, 1MHz	0.005	0.004	0.006
CTE (ppm/°C)	50	24	20
Hardbake Shrinkage (%wt)	15	8	50
Coating Thickness Range (microns)	5-20	2-10	5-80

polyimides were chosen as representative products designed for thick film and multichip module applications.

In this study, each polyimide was used to fabricate a single-level metal pattern on a bare silicon substrate. The key parameter measured in this evaluation was the percentage of successful metal interconnects that traversed the polyimide surface to the silicon wafer's surface. This parameter was primarily dependent on the ability to produce a uniformly sloped wall on which the metal was evaporated, as illustrated in Figure 4.2. For each polyimide, a method for controlling the via side wall slope was investigated.

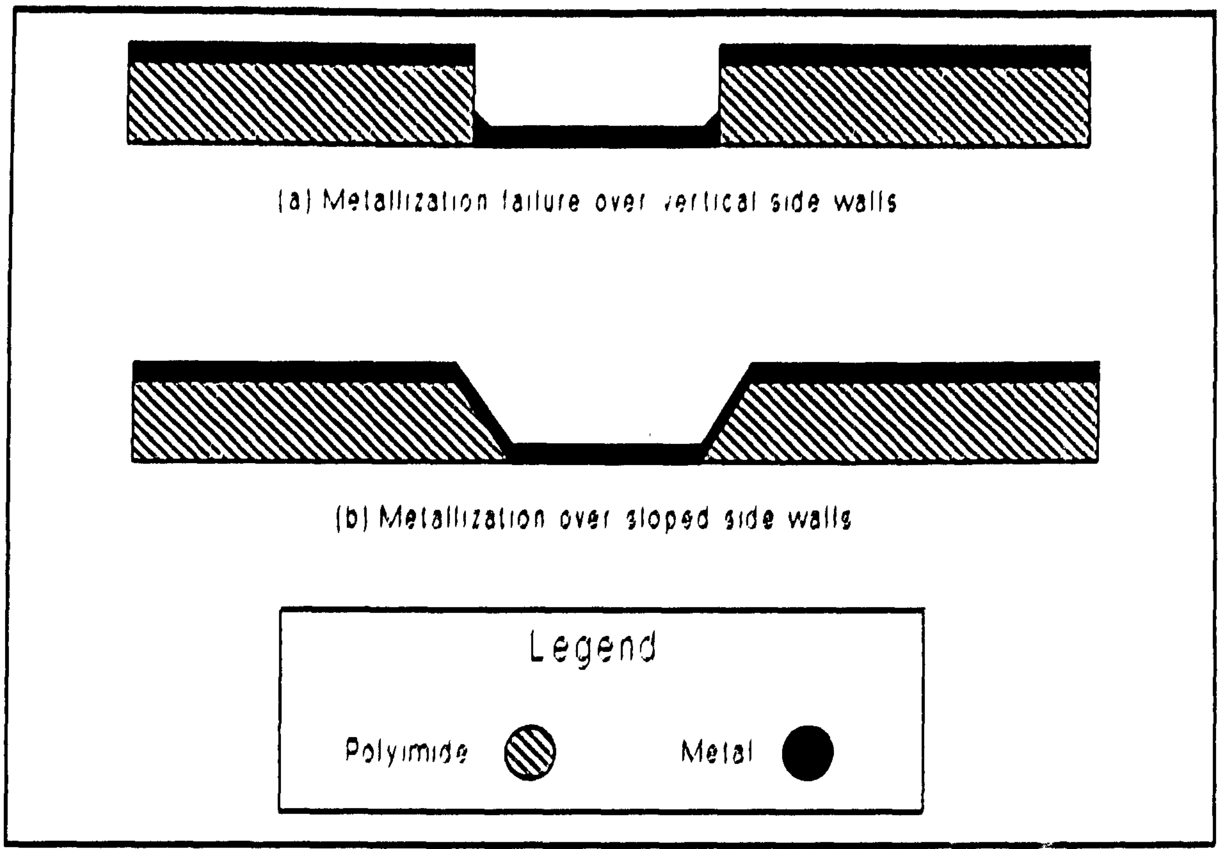


Figure 4.2. Cross-sectional view of metallization in polyimide vias.

Other parameters were also measured in this evaluation. These parameters included: planarization over an even surface, planarization over a varying topology, hard bake thickness loss, and the affects of other chemicals and processes on the polyimide material.

Ultradel 4212 Application and Patterning. Figure 4.3 illustrates the steps involved in the application and patterning of a non-photosensitive polyimide. The detailed procedure used for the Ultradel 4212 polyimide is presented in Appendix D. The manufacturer indicated that the primary parameter which can be used to control the via side wall slope is the polyimide's softbake temperature. Research by

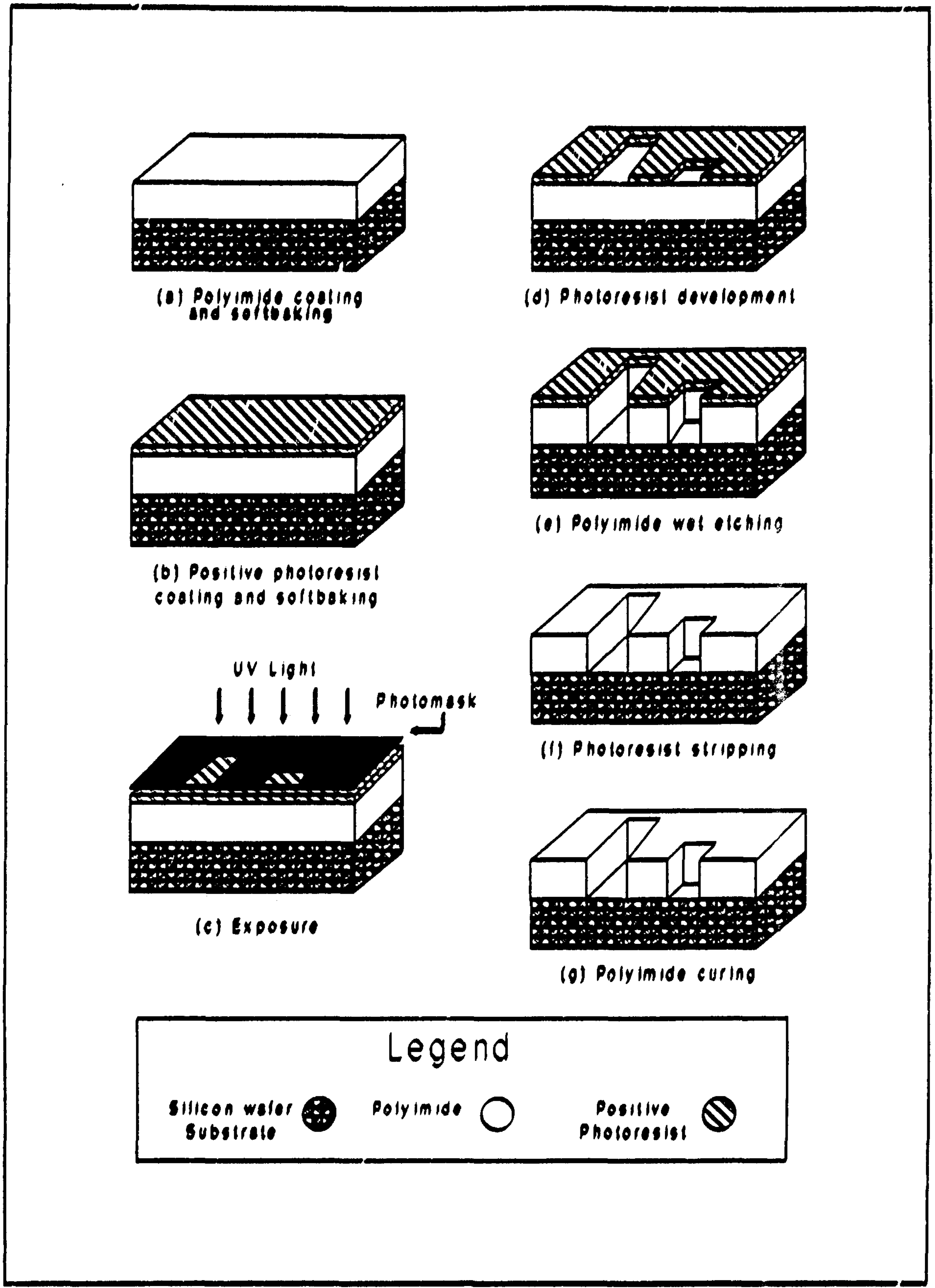


Figure 4.3. Application and patterning procedures for the non-photosensitive polyimides (14).

Amoco has shown that a softbake temperature of 100°C produces vertical side walls, while temperatures above 150°C produce imidization in the coating which prevents proper etching. By varying the softbake temperature between 100°C and 150°C, the slope of the via side walls can be controlled (31).

Samples were prepared using four different softbake temperatures: 100°C, 120°C, 140°C and 150°C. For each temperature, a sample was patterned using the level-one contact-cut mask. This sample was then coated with aluminum. The aluminum was patterned as detailed in Appendix E, using the level-one metal mask. The level-one metal mask was used to pattern the polyimide on one sample for each temperature. This sample was used to produce cross-sections for via side wall slope evaluation. The longer lines on the level-one metal mask facilitated the ability to cross-section the vias.

As indicated in Appendix E, the aluminum was patterned using a solution of 4 parts acetic acid, 4 parts phosphoric acid, 1 part nitric acid and 1 part distilled water. In his research, Takahashi maintained this solution in the 40-45°C temperature range to produce a controlled etch rate of 2000 Å/min (39:161). Etching with this solution at a higher temperature damaged the metal pattern, while etching at a lower temperature reduced the etch rate. Initial tests showed that this procedure caused surface damage to the Ultradel 4212 coating. Discussions with the manufacturer indicated that this was the result of incomplete imidization of the polyimide, due to the lower hardbake temperature. The manufacturer recommended that hardbaking be conducted at 350°C (300°C absolute minimum). The manufacturer also indicated that lowering the temperature of the aluminum etchant may reduce the degree of polyimide surface damage (31).

Because Mainger's work indicated that polyimide baking in excess of 250°C would result in unacceptable IC die shifting (24:Sec 4,42), a test was performed to determine if prolonged baking at 250°C improved imidization. Samples were hardbaked using the cure schedule illustrated in Figure 4.4. At each two-hour interval, after the 250°C temperature was reached, a sample was removed to measure the polyimide coating thickness. In a second test, samples baked at 250°C for four hours and samples baked at 250°C for ten hours were metallized and etched with etchant temperatures of 30, 35 and 40°C. The surfaces were inspected visually and with the stylus profilometer.

A final test was performed on the samples containing the metal patterns after the electrical continuity evaluation. A second layer of polyimide was applied to the samples. Stylus profilometer measurements were taken after the softbake and hardbake processes to determine the degree of planarization over the vias.

Another concern of the polyimide manufacturer regarding the sub-300°C cure temperature was the reduced insolubility

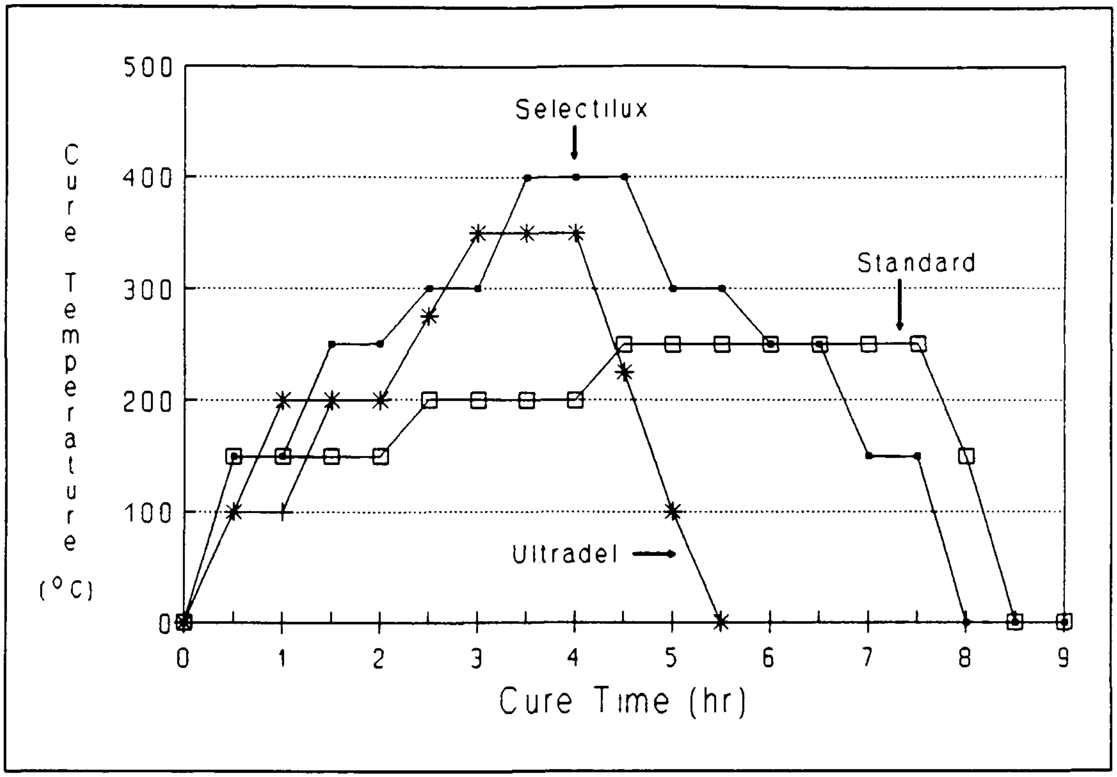


Figure 4.4. Cure schedules for the candidate polyimides (14,24,42,43).

of the cured polyimide upon application of additional polyimide layers. Specifically, incomplete imidization of the polyimide might result in excessive absorption of the solvents from the additional polyimide layers. This solvent absorption might also damage the first polyimide layer. An evaluation was conducted to examine the severity of this effect. First, the polyimide was applied to two bare wafers. One wafer was cured using the cure schedule recommended by Mainger (24:App I,3). The second wafer was cured using the schedule recommended by the polyimide manufacturer, as illustrated in Figure 4.4. A second layer of polyimide was applied to both wafers and softbaked. The wafers were then examined for coating defects by visual inspection, and measurements were made with the stylus profilometer.

Photosensitive Polyimide Application and Patterning. The procedure for applying and patterning the two photosensitive polyimides (Selectilux HTR3-200 and Ultradel 7501) is illustrated in Figure 4.5. The detailed procedures for processing these polyimides are presented in Appendix F. As Figure 4.5 illustrates, the photosensitive polyimide requires fewer processing steps compared to the non-photosensitive polyimide. The use of proximity printing to produce sloped via side walls has been reported in previous research (24,39). In this study, variable mask-to-polyimide separation distances during exposure and its effect on via side wall profiles were examined.

As with the Ultradel 4212, two sets of samples for each polyimide were prepared. One set was patterned with the level-one contact cut mask, and the other set with the level-one metal mask. For each polyimide, several samples were produced with mask-to-polyimide separations of 0, 20, and 50 microns. Aluminum was deposited and patterned on each sample as detailed in Appendix E.

Testing the samples coated with the two photosensitive polyimides was identical to the tests conducted on the Ultradel 4212 polyimide. These tests, as described in the previous section, included: electrical continuity, long duration hardbake shrinkage, and degree of planarization.

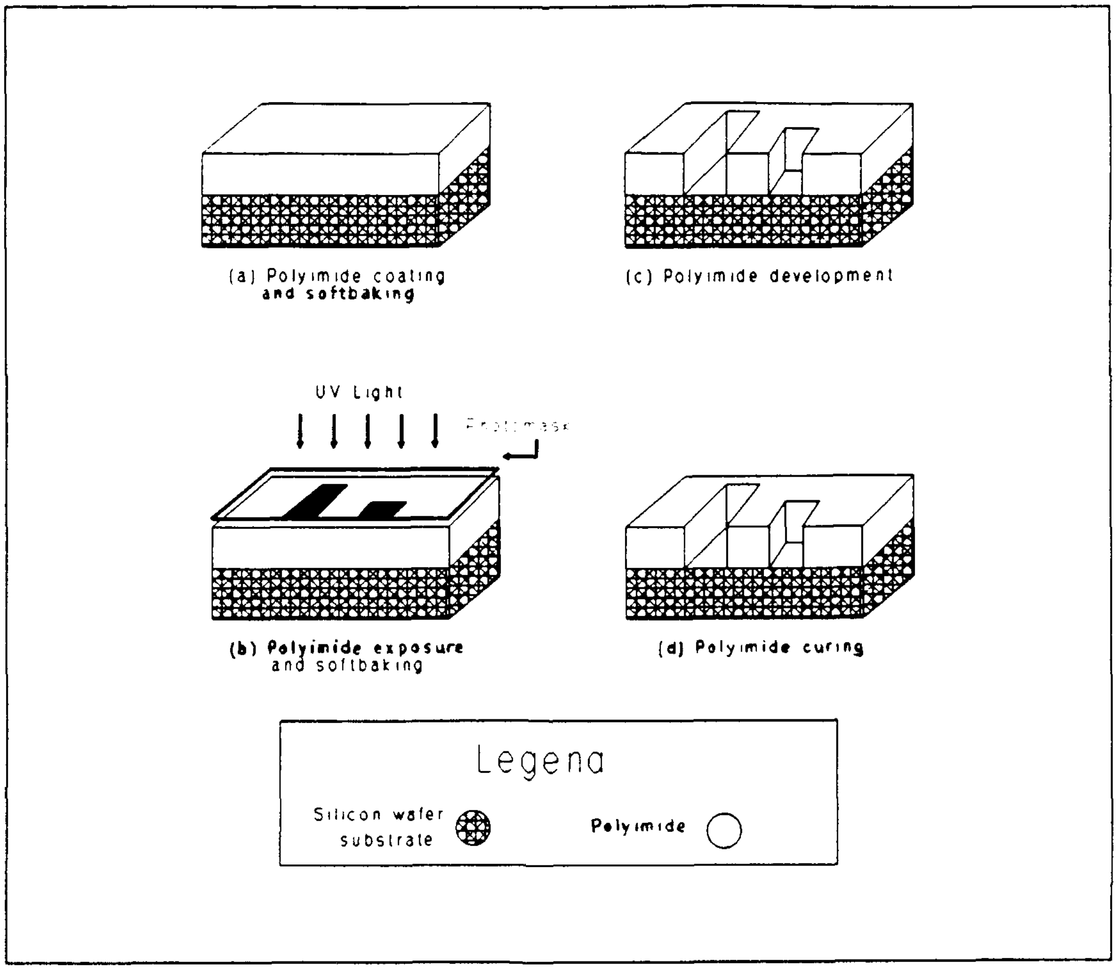


Figure 4.5. Application and patterning procedure for the photosensitive polyimides (14).

<u>Dielectric Constant Evaluation Procedure</u>. The initial test samples were used to evaluate the non-electrical properties of the candidate polyimides. Another set of test samples were produced to evaluate two important electrical properties -- the polyimide's relative dielectric constant and the dissipation factor. These samples were fabricated as parallel plate capacitors using the candidate polyimides as the dielectric material. To accomplish this test, aluminum was evaporated onto a silicon dioxide layer grown on a set of

silicon wafers. Each polyimide was applied and patterned on two of these coated wafers. One of these wafers was cured using the cure schedule developed by Mainger (24: App I,3). The other wafer was cured according to the manufacturer's recommended cure schedule, as illustrated in Figure 4.4. A second layer of aluminum was applied to the set of wafers and patterned to form the parallel plate capacitors.

The relative dielectric constants of the samples were determined by measuring the impedance of the capacitors over a frequency range of 10^3 to 10^7 Hz. The reactive part of this measured impedance was used with the following formula to determine the relative dielectric constant:

$$C=\epsilon_r \epsilon_o \frac{A}{d} \tag{4.1}$$

where

C is the measured capacitance
ϵ_r is the relative dielectric constant
ϵ_o is the permittivity of free space ($8.85 \cdot 10^{-14}$ F/cm)
A is the area of the conducting plates (cm^2)
d is the separation between the plates (cm).

The impedance measurements of the capacitors were also used to calculate the dissipation factors of the dielectric materials. For a parallel plate capacitor, the dissipation factor is calculated as:

$$D = 2\pi fRC \tag{4.2}$$

where

C is the measured capacitance (farads)
R is the measured series resistance of the capacitor (ohms)
f is the frequency of the applied voltage (Hz)
D is the dissipation factor.

The relative dielectric constants and dissipation factors for each polyimide were calculated over the frequency range for the two cure schedules, indicating what effect the incomplete cure had on that electrical property for each candidate.

Fabrication Procedure

The procedures required to fabricate the three WSI configurations consist of specific combinations of the four fundamental steps presented in Figure 2.2. The organization of these processing steps for each configuration is presented in Figure 4.6. This section presents a detailed description of these four basic fabrication steps, as well as an initial measurement step. Table 4.3 presents a summary of the test samples produced for this study.

Host Substrate and IC Die Measurements. The primary requirements of the host substrate are to provide a robust mechanical support structure for the WSI circuit and a smooth, planar surface on which reliable metal interconnects can be fabricated. Silicon (100)-oriented wafers were selected for this project based upon cost, availability, and

Table 4.3 WSI Test Sample Descriptions.

Wafer	Polyimide	WSI Configuration
1	Ultradel 4212	Four die, patterned overlay
2	Selectilux HTR3-200	Four die, patterned overlay
3	Selectilux HTR3-200	Four die, patterned substrate
4	Ultradel 4212	Four die, patterned substrate
A	Selectilux HTR3-200	Single die, patterned overlay
B	Selectilux HTR3-200	Single die, patterned overlay
C	Ultradel 4212	Single die, patterned overlay
D	Ultradel 4212	Single die, patterned overlay

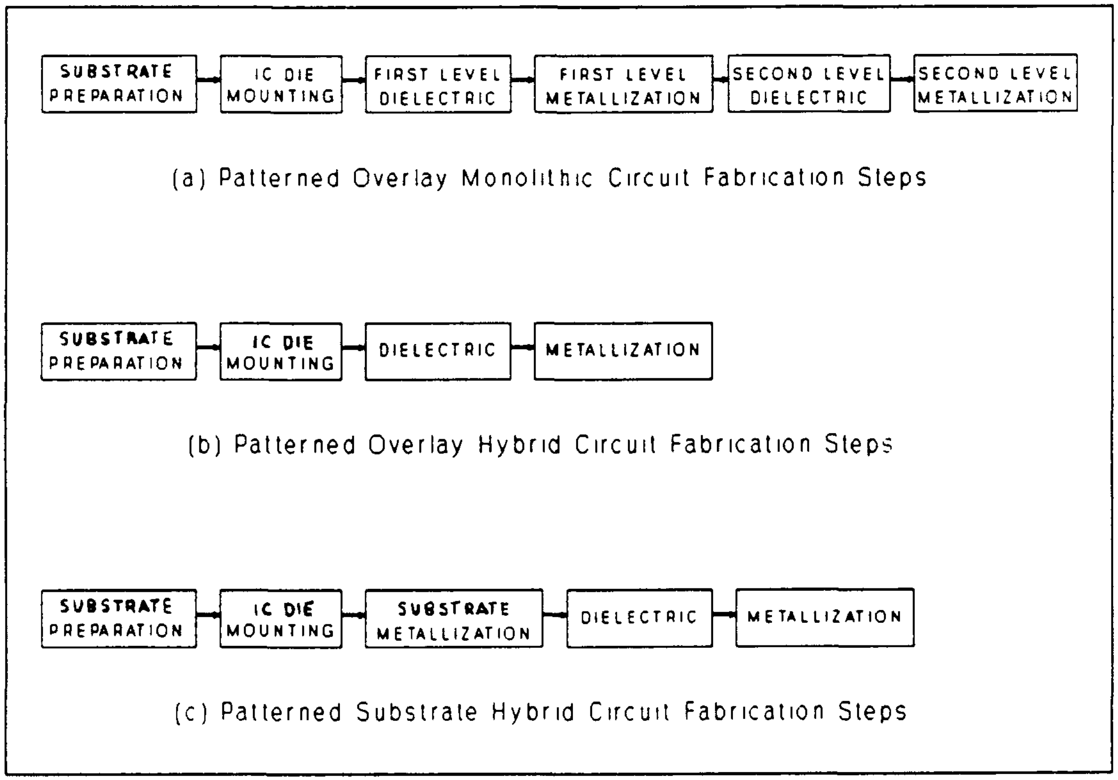


Figure 4.6. Fabrication procedures for WSI circuits.

the results of previous AFIT studies in which fabrication procedures were developed.

The substrate and IC die thickness measurements were made for two purposes. First, it was necessary to determine if the substrates needed to be thinned. Similar thicknesses of the IC die and host substrate are desired to minimize the size of the epoxy-filled transition region. These measurements indicated an average IC die thickness of 500 microns, with all 28 IC die thicknesses spanning 490 to 510 microns. The specified thickness of the host substrates was established to be 500 microns to eliminate the requirement of planar etching. A ±10 micron tolerance was established, based upon the accuracy of the micrometer used to make the measurements.

The second purpose for the host substrate thickness measurements was to calculate the photomask image size required to produce the proper etched cavity in the host substrate. As Figure 4.7 and Equation 4.3 illustrate, the photomask image dimensions depend on the host substrate's thickness. Because the cavity walls slope inward with respect to the host substrate's upper surface, the substrate thickness must be accounted for to produce an opening equal to the IC die dimensions.

The etch mask layout required measurements of the IC die surface area dimensions, as well as the host substrate thickness. Figure 4.7 illustrates the relationship of the required mask image size to these parameters. As illustrated, the image dimensions can be calculated as follows:

$$L_I = L_D - 2R_{111}T_E + 2W\cos\Theta \qquad (4.3)$$

where

L_I is the photomask image length
L_D is the IC die length
R_{111} is the IC die cavity etch rate in the [111] direction
T_E is the total IC cavity etch time
W is the host substrate's thickness
Θ is the slope of the cavity wall with respect to the wafer's planar surface (Θ equals 54.47° for (100)-oriented wafers).

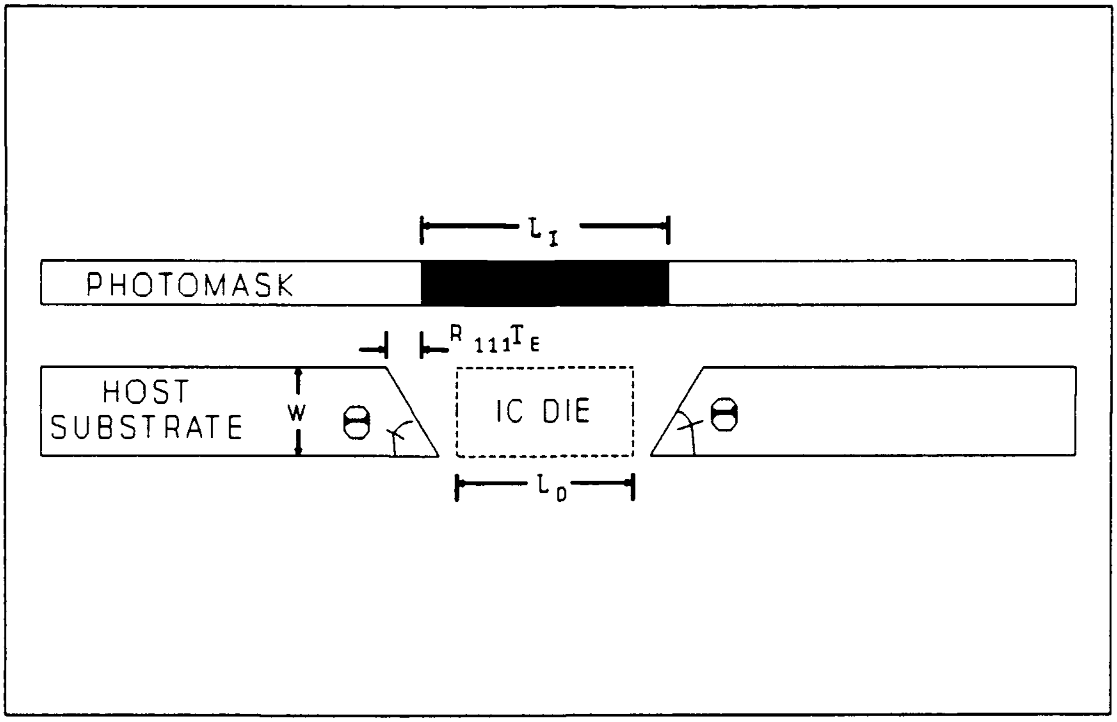
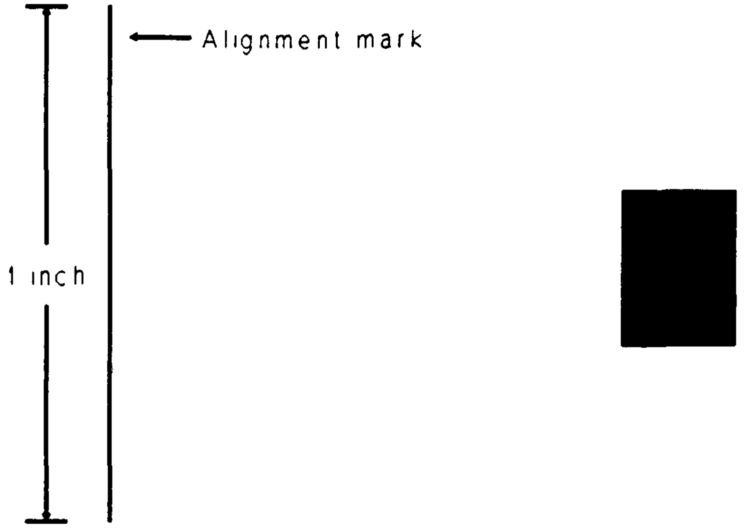


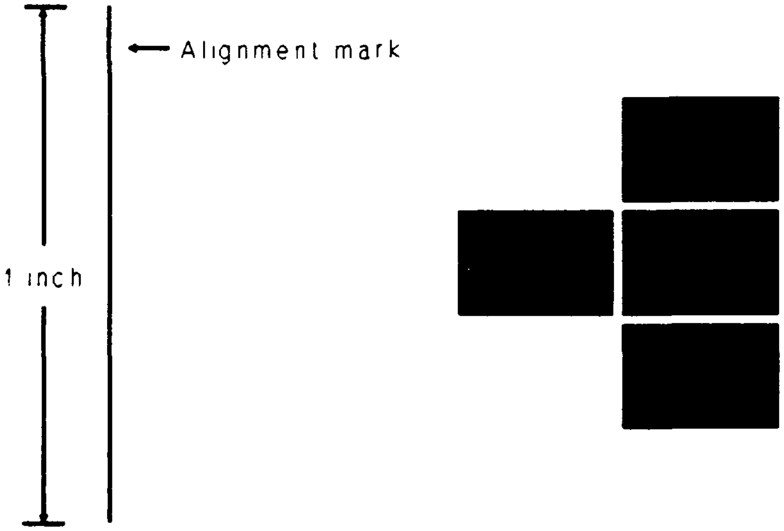
Figure 4.7. Cross-sectional view illustrating the etch window and IC die cavity dimensional relationships.

Photomasks were designed to produce one cavity for the single IC die configuration, and four cavities for the multiple IC die configurations. The two photomask designs are illustrated in Figure 4.8. For the four cavity photomask design, the location of the IC die with respect to each other was chosen to minimize the lengths of WSI interconnects. The procedures implemented to produce the photomasks are presented in Appendix G.

As Figure 4.8 illustrates, alignment marks were placed on both photomask layouts. These marks were used to align the IC die cavity borders with respect to the reference flat on the host wafer. This alignment was critical to ensure consistent cavity dimensions and smooth side walls. Kendall's results indicate that the early research in anisotropic silicon etching produced a wide variation of etch rates in the [111] direction, which he attributed to limitations in alignment between the photomask and the host wafer (on the order of ±1°). He reported that more consistent, and smaller etch rates in the [111] direction occur when alignments on the order of ±0.1° are achieved (19:108). For this reason, the alignment marks were included in the mask designs. Each of the mask image edges was aligned either parallel or perpendicular to the alignment mark. With the mark aligned to the wafer's reference flat, each side in the image was aligned to a (111) plane in the host wafer.



(a) Single IC die etch photmask



(b) Four IC die etch photomask

Figure 4.8. Photomasks for IC die cavity etching.

IC Die Well Etching.

Masking. The etch rate results for the potassium hydroxide (KOH) etchant reported by Kendall indicate that silicon dioxide is a suitable mask material for silicon etching. Figure 4.9 illustrates the experimental results achieved for the etch rates of silicon dioxide layers (R_{CX}) relative to those for the [100] direction (R_{100}). Over a wide range of etchant concentrations and temperatures, these studies revealed that KOH etches silicon in the [100] direction at least 300 times faster compared to the silicon dioxide (19:109). Thus, a 2.0 micron thick silicon dioxide mask will adequately protect the wafer for a sufficient period of time over which the etchant can completely etch through the exposed areas of a 500 micron thick wafer.

Silicon dioxide was grown on the silicon wafers by exposing it to a steam atmosphere at an elevated temperature. The chemical reaction that occurs is (38:343):

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2 \text{ (gas)} \qquad (4.4)$$

Studies have determined that exposing a silicon (100)-oriented wafer to a steam atmosphere at 1050°C for 20 hours results in an oxide thickness of 2.4 microns (38:350). The detailed procedure implemented to accomplish the oxidation used in this research effort is presented in Appendix H.

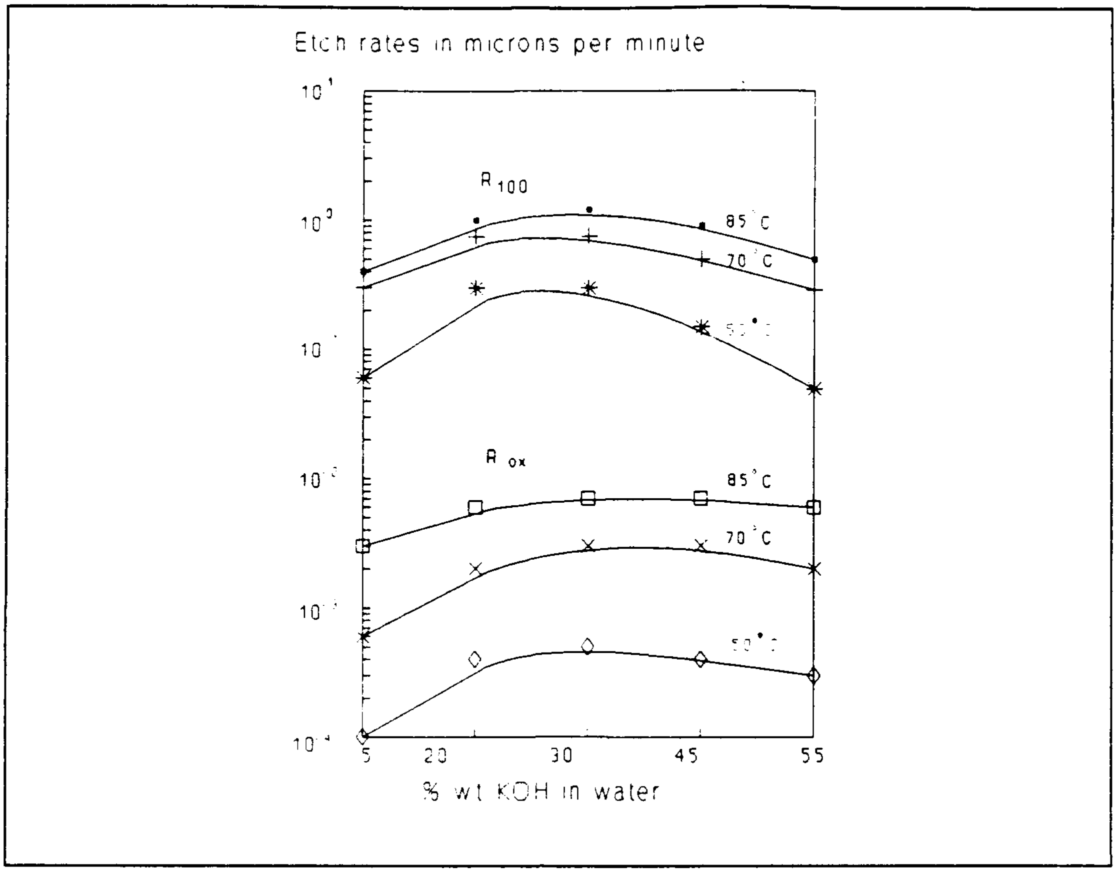


Figure 4.9. KOH etch rates in silicon and silicon dioxide (19:109).

After the oxidation step was completed, the wafer was coated on both sides with negative photoresist. The mask pattern was printed on the unpolished side of the wafer using the procedures outlined in Appendix I. By placing the mask image on the unpolished side of the wafer, the opening on the polished side could be more closely matched to the IC die dimensions. This technique also reduces the size of the transition region between the circuit side of the IC die and the top surface of the host substrate; that is, it manifests itself with a smoother surface upon which to fabricate the interconnects. The negative photoresist was chosen because it provided a sufficiently thick and smooth morphology on the substrate's unpolished back surface, it was compatible with the mask aligner's optical exposure wavelength and energy, and it resulted in a chemically hardened image that was resistant to the etchant.

The next step in the IC die cavity etching procedure was to etch the IC die cavity pattern in the oxide layer. The etchant chosen was a buffered hydrofluoric acid solution (1:4 $HF:NF_4OH$) because it is known to produce stable etch rates at room temperature without damaging the negative photoresist. Appendix J presents the procedure implemented to pattern the oxide layer. Once the etch to the silicon wafer's surface was completed, the negative photoresist was stripped off, and the wafer was cleansed using the procedure outlined in Appendix K.

Silicon Etching. A number of studies have shown that potassium hydroxide (KOH) solutions anisotropically etch single crystal silicon (19,38). The etch rates of the (100) and (110) planes are nearly equal, typically at least two orders of magnitude greater than the etch rate in the (111) plane. The specific etch rates and the relationship between them are both concentration and temperature dependent, as illustrated in Figure 4.10 (19:110).

For this study, four rectangular holes were anisotropically etched into each wafer. As previously discussed, these holes were aligned along the (111) planes,

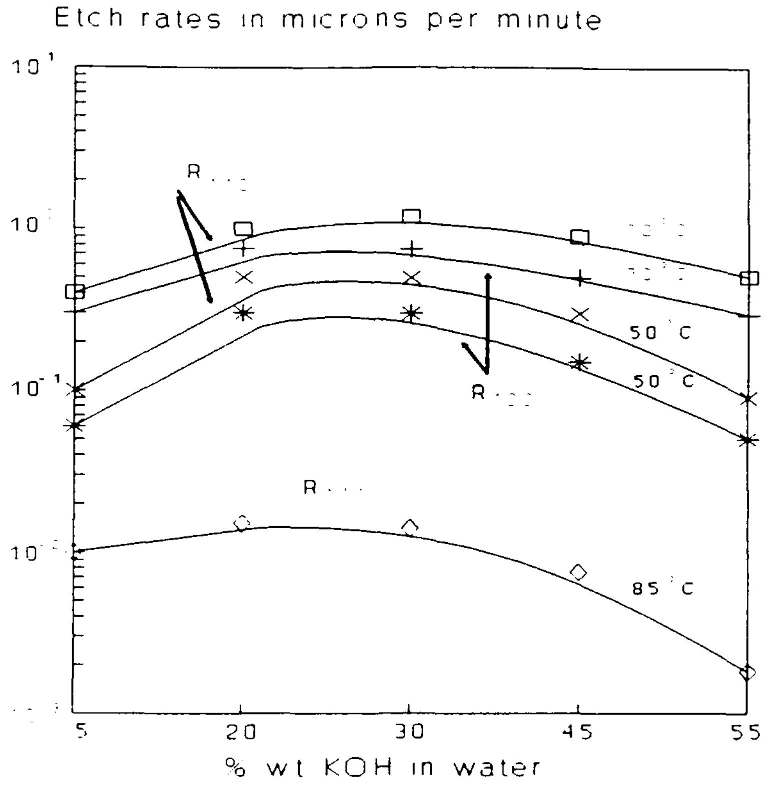


Figure 4.10. KOH etch rates in silicon crystals (19:110).

resulting in sloped walls with a 54.47° angle measured with respect to the top surface of the wafer. A solution of 20% wt KOH and 80% wt distilled water at 60°C was chosen, resulting in a predicted etch rate of 0.4 microns per minute in the [100] direction and 5 Angstroms per minute in the [111] direction.

Temperature control of the etchant was maintained by immersing its beaker in a constant temperature water bath. The water bath was maintained at 60°C during the etch process. Based upon the reported etch rates and the measured host wafer thicknesses, the required etch time was predicted to be 20 hours. Periodic measurements of the wafer thicknesses during the etch process were preformed to determine the experimental etch rate of the solution. The etch procedure is detailed in Appendix L. Once the etch process was completed, the remaining silicon dioxide was stripped off with hydrofluoric acid, and the host wafers were cleaned.

IC Die Mounting. IC die mounting of the test samples was performed using the procedures developed in the IC die mount evaluation experiments. Wafers A and B were prepared using the substrate pre-assembly IC die mounting procedure. The remaining wafers were prepared using the single-step IC die mounting procedure.

In the substrate pre-assembly mounting procedure, the host support substrates were bonded together before the IC die were mounted. First, the host substrate's back surface was coated with a thin epoxy layer and then joined to the support substrate. The substrates were then placed on the hot plate between two optical flats, and the 1.0 kg planarizing weight was added. The epoxy was cured at 175°C for ten minutes, followed by acetone cleansing of all surfaces, including those in the IC die cavity. The substrates were then relocated under the planarizing weight between two optical flats on the hot plate for an additional 50 minutes of epoxy cure time. Next, a small amount of epoxy was placed in the IC die cavities, followed by the IC die.

This epoxy was cured for 60 minutes, with an acetone surface cleaning step after the first ten minutes of cure. Finally, the WSI assembly was subjected to a high temperature cure cycle to ensure the thermal stability of the bond during the polyimide's processing. The details of this IC die mounting process are described in Appendix M.

In the single-step IC die mounting procedure, the host substrate was placed, planar side down, onto a Teflon®-coated optical flat, and IC die were placed in the cavities, circuit side down. One side of the support substrate was coated with epoxy. The two substrates were then joined and clamped between two optical flats. The assembly was placed on a 175°C hot plate for ten minutes. After an early surface cleansing process, the WSI assembly was again placed on the hot plate between the two optical flats for additional epoxy cure time. During this cure cycle, a 1.0 kg, four-inch diameter weight was placed on the top optical flat to provide a planarizing force. This substrate assembly was then subjected to a high temperature cure cycle to ensure the thermal stability of the bond during polyimide processing. The details of this procedure are presented in Appendix N.

Dielectric Application and Patterning. As Table 4.3 illustrates, test samples were fabricated using two of the three polyimide candidates. In all cases, the goal was to create cured polyimide layers ten microns thick. These dielectric layers provided electrical insulation between the interconnect metal layers, as well as vias through which the metal layers could be electrically connected.

Detailed procedures for applying and patterning the Ultradel 4212 polyimide are described in Appendix D. To achieve the maximum slope in the via side walls, a softbake temperature of 140°C was used to process all the samples containing the Ultradel 4212 polyimide. The first polyimide layer on the single IC die patterned overlay configuration was subjected to the high temperature cure schedule recommended by the manufacturer to prevent any damage from the subsequent application of additional polyimide layers. All other Ultradel polyimide applications were subjected to the high temperature cure schedule developed by Mainger (24).

Detailed procedures for applying and patterning the Selectilux HTR3-200 photosensitive polyimide are presented in Appendix F. All of the samples coated with the Selectilux polyimide were exposed using proximity printing with a separation gap of 20 microns to produce sloped via side walls. The high temperature cure schedule developed by Mainger was used to cure each Selectilux polyimide sample (24).

Prior to metallizing the polyimide samples, visual inspections and stylus profilometer measurements of the vias were performed. Visual inspections were used to determine the number of unsuccessful vias caused by defects in the polyimide layer. Visual inspections were also used to determine the level of success in achieving via-to-bond pad alignment. This measurement was important for determining the relative alignment tolerances in multiple IC die configurations. For this project, 200 micron square bond pads were used in the IC die design, with 300 micron center-to-center spacing. These dimensions are approximately twice the size used in standard MOSIS pad frames. The via patterns were designed with 70 micron square via images to allow for a reasonable degree of IC die misalignment. The visual inspection determined whether the pad and via relative scaling were adequate for the degree of alignment found in this study.

The stylus profilometer measurements provided data on the polyimide layer's thickness and the number of completely etched vias. The stylus profilometer was also used to measure the lateral via dimensions, from which the effect of shrinkage during cure was subsequently determined.

The via photomask patterns for each configuration were fabricated using the procedures presented in Appendix G. Figure 4.11 illustrates the mask designs used to pattern the polyimide for the single IC die configuration. The two multiple IC die configurations required only one mask each, as illustrated in Figures 4.12 and 4.13. All of the masks shown were used to pattern the Selectilux polyimide which acted as a negative photoresist. Because the Ultradel 4212 polyimide was patterned using a positive photoresist layer,

(a) Level-1 via pattern photomask

(b) Level-2 via pattern photomask

Figure 4.11. Via patterns for the single IC die patterned overlay.

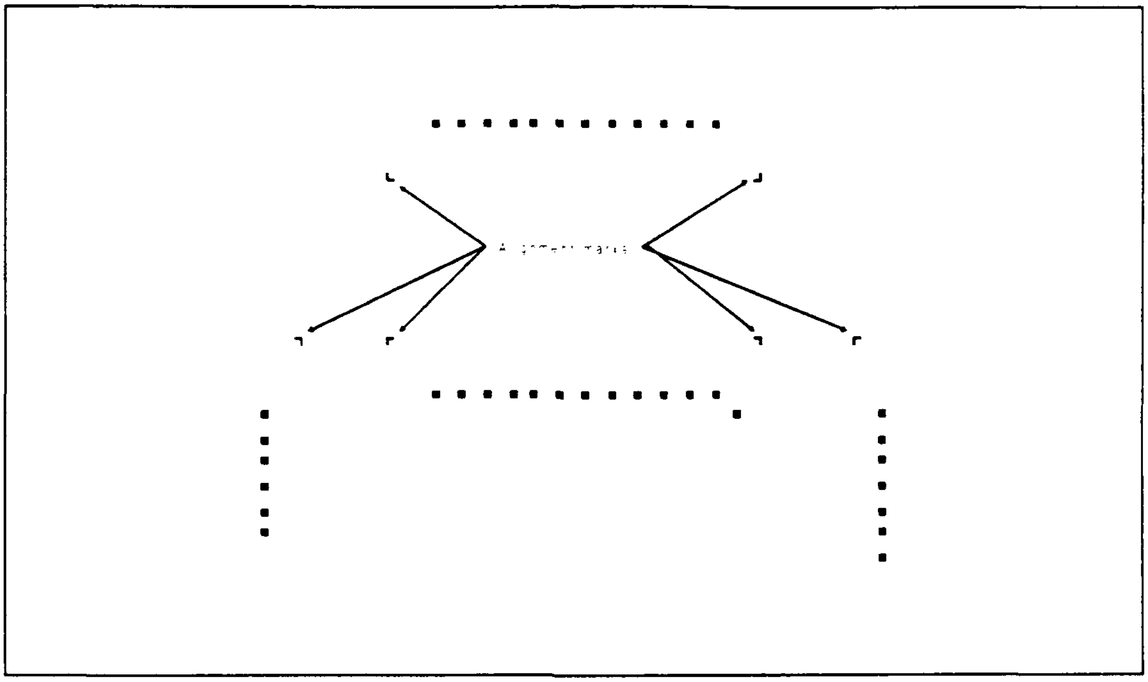


Figure 4.12. Via pattern for the four IC die patterned overlay.

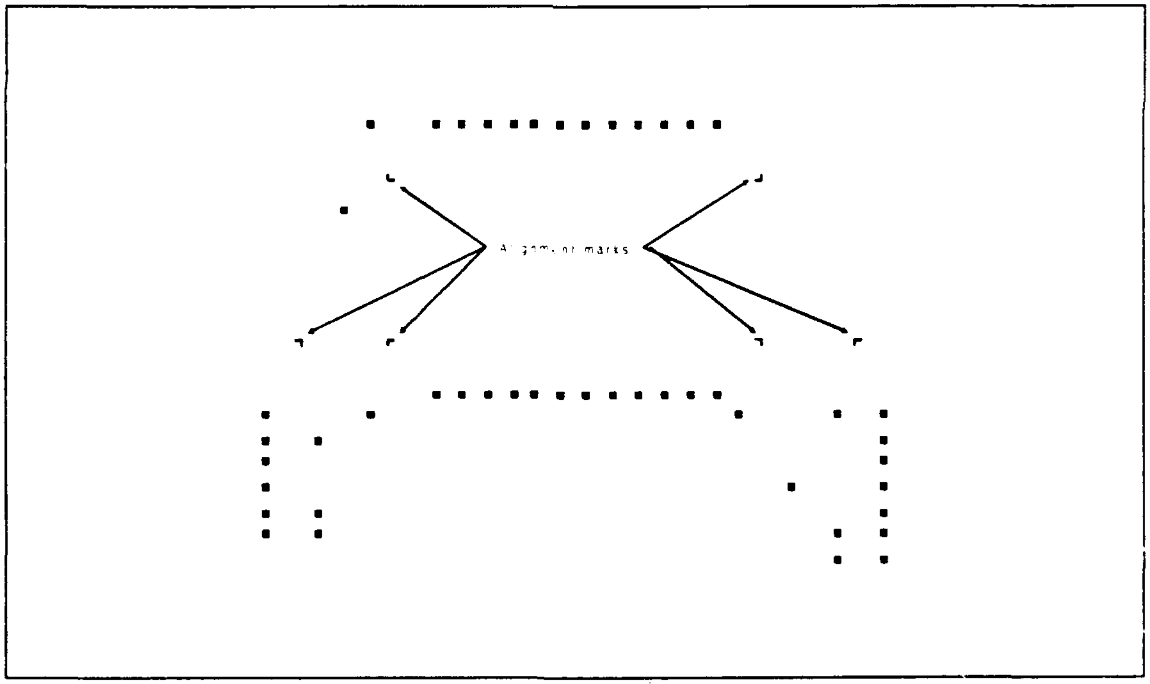
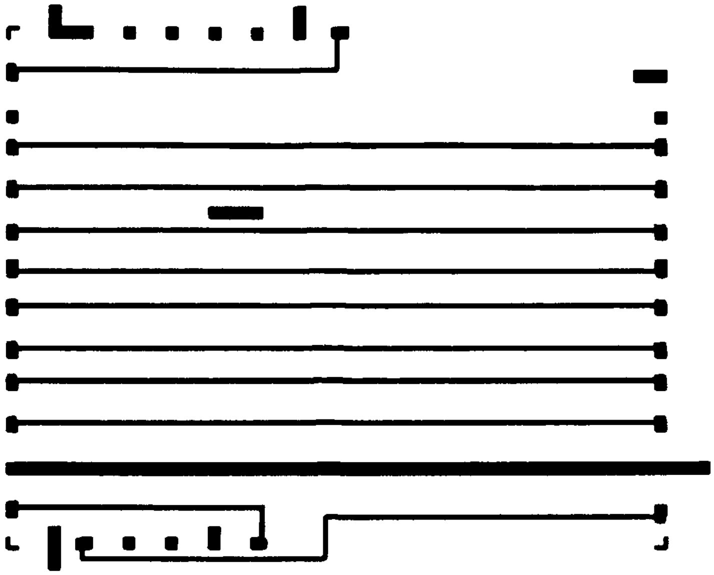


Figure 4.13. Via pattern for the four IC die patterned substrate.

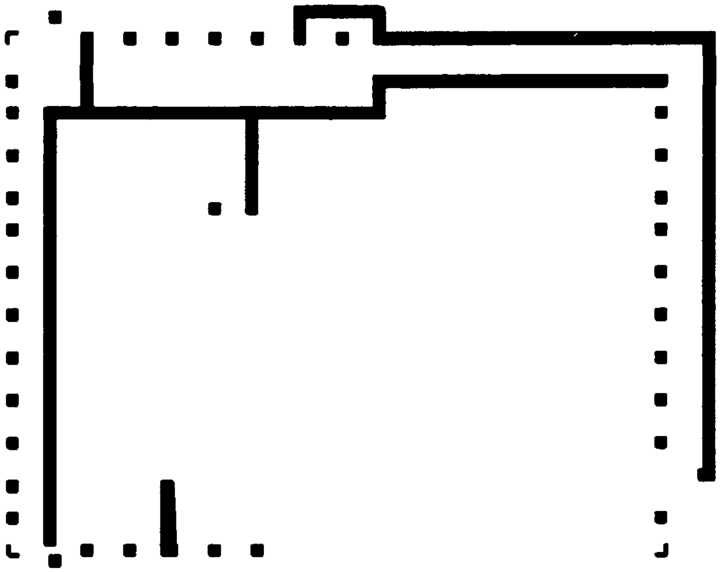
the photomask used to pattern this material required reversed light and dark regions. However, photographic negative duplication of the negative photoresist masks did not produce a correct positive image because the patterns were not symmetrical. Instead, the positive photoresist patterns were produced by reversing the original rubylith pattern.

Metallization Application and Patterning. Aluminum metallization was used to provide the WSI interconnects in this project. First, an aluminum film approximately 1.2 microns thick was evaporated onto the surface of the substrate or patterned polyimide layer. Positive photoresist was then applied and patterned on the aluminum surface. Exposed regions of the aluminum were etched in a solution composed of (by volume) four parts acetic acid, four parts phosphoric acid, one part nitric acid, and one part deionized water. The photoresist pattern was then stripped off, leaving the metal interconnect pattern on the surface. Appendix E details the procedure used to deposit and pattern the aluminum.

A number of metallization photomasks were required for the WSI configurations. Figure 4.14 illustrates the two metallization patterns used to fabricate the single IC die patterned overlay circuit. The four IC die patterned overlay circuit required only one metallization mask, as shown in Figure 4.15. Two metallization patterns, illustrated in Figures 4.16 and 4.17, were required for the patterned



(a) Level-1 metallization photomask



(b) Level-2 metallization photomask

Figure 4.14. Metallization interconnect patterns for the single IC die patterned overlay.

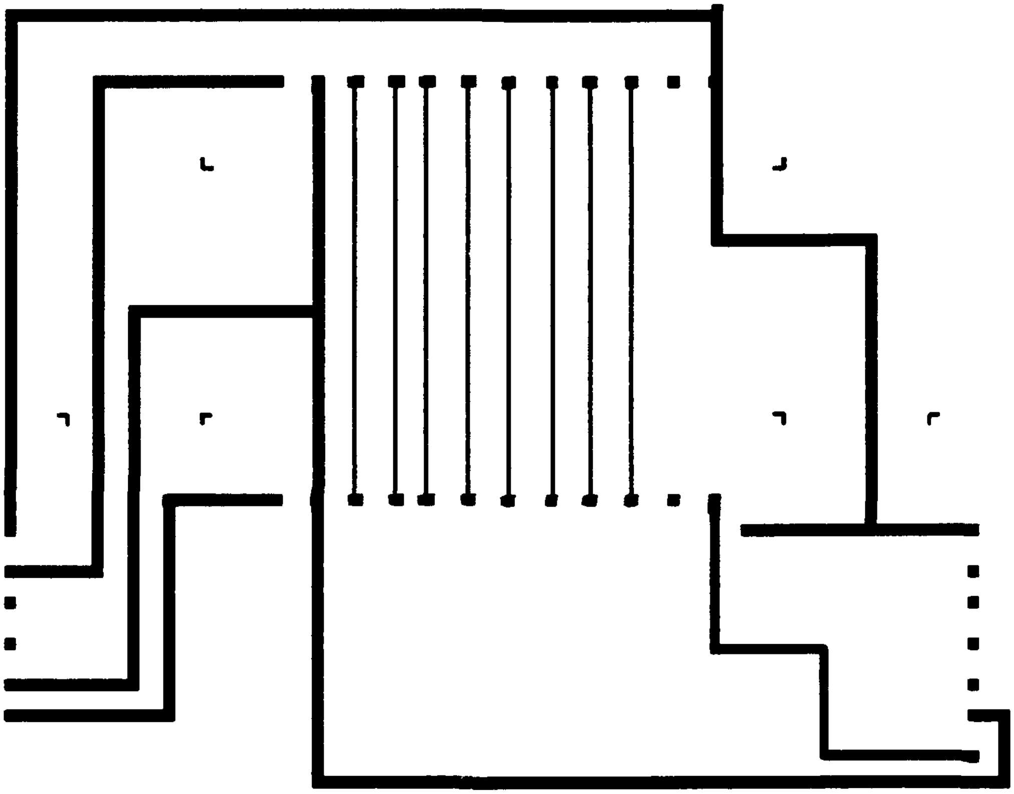


Figure 4.15. Metallization interconnect pattern for the four IC die patterned overlay.

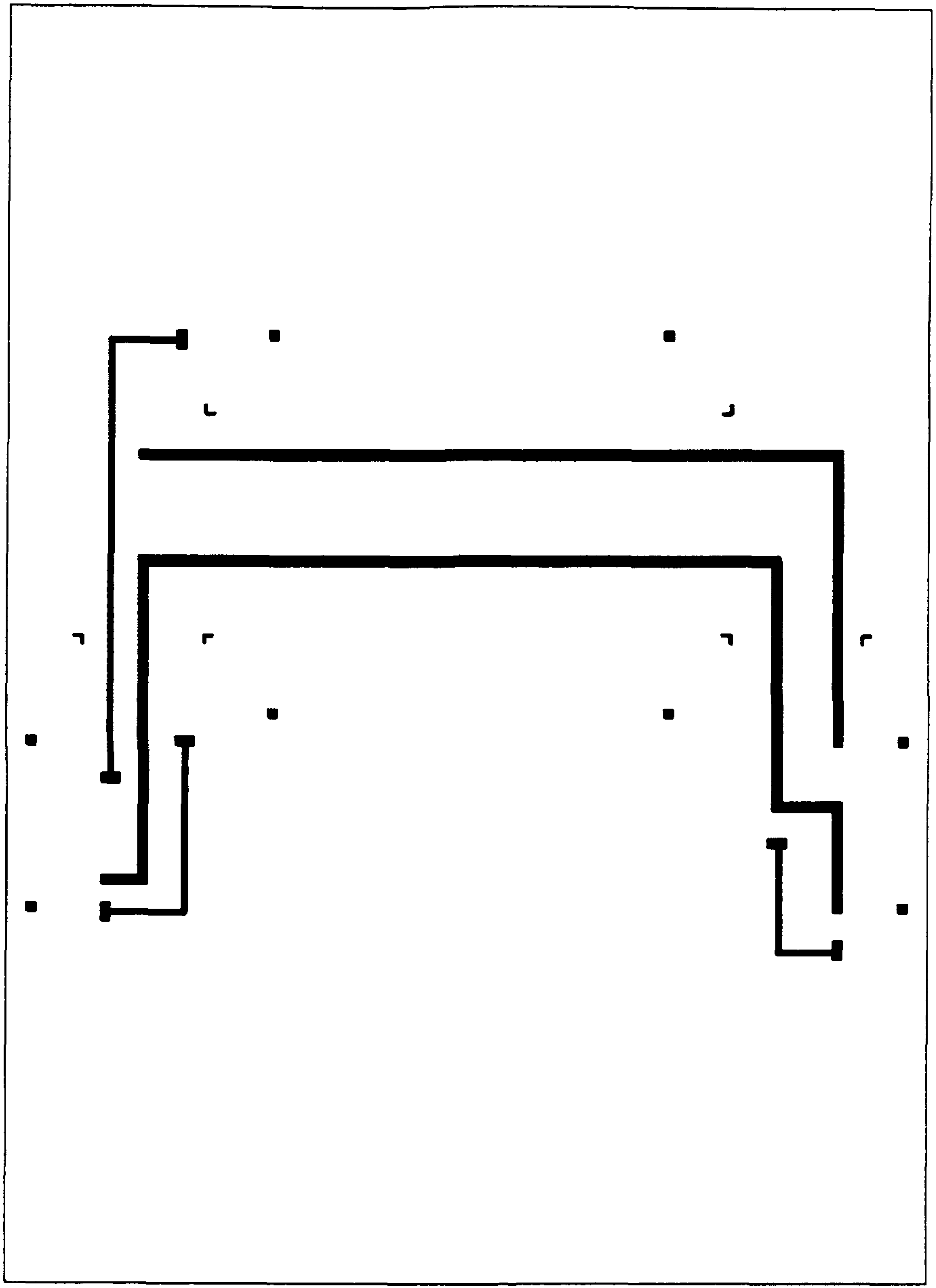


Figure 4.16. Substrate metallization interconnect pattern for the four IC die patterned substrate.

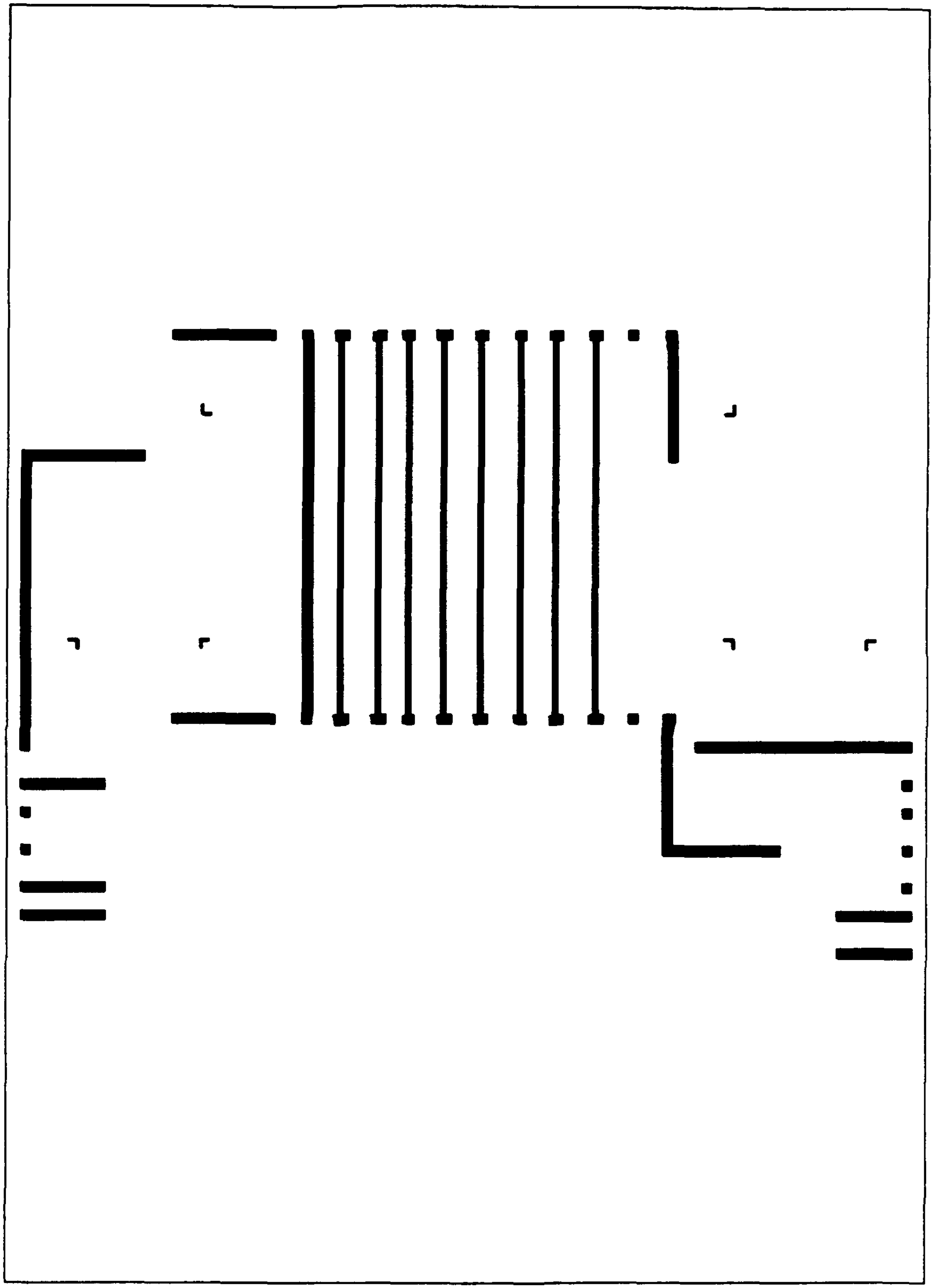


Figure 4.17. Level-1 metallization interconnect pattern for the four IC die patterned substrate.

substrate configuration. It should be noted that the pads on the metallization masks are approximately 50 percent larger compared to the via pattern pads. As stated in the previous section, cured vias that were patterned in the photosensitive polyimide were larger than the via image used to produce them. This enlargement was primarily due to the high degree of shrinkage exhibited by this polyimide. Thus, the pad sizes on the metallization patterns were increased to prevent etching of the exposed regions of the IC die bond pads.

Evaluation Procedures

Evaluation Samples. Based upon the results of the fabrication procedures, two samples were chosen for electrical testing. One sample was the WSI assembly fabricated on a bare substrate during the polyimide evaluation experiments. The second sample was a single IC die WSI assembly. Both samples were fabricated using the Selectilux polyimide as the interlevel dielectric with a common set of via and metal interconnect patterns. The primary difference between the two test articles was the presence of the IC die in the second sample.

Evaluation Measurements. Three primary measurements were performed on the two test articles. These measurements were: continuity and interconnect resistance measurements, signal attenuation and propagation delay, and coupling between interconnects. The electrical continuity testing provided a success-failure metric of the overall fabrication procedure. The latter two measurements provide quantitative information on the electrical characteristics of the WSI interconnects, and how they will likely function in a WSI system.

Continuity and Interconnect Resistance Measurements. The test configuration used to perform these measurements is illustrated in Figure 4.18. Measurements were performed between each connected pad pair, resulting in 12 measurements on the level-one interconnects and 4 measurements on the level-two interconnects. These interconnects are depicted in Figure 4.14. In addition, measurements were accomplished on the level-two metal interconnects along their lengths, excluding any via transitions. Incremental measurements with and without the via transitions were used to calculate the via transition resistances that likely occur as a result of metal thinning.

The primary objective of this performance evaluation was to determine the percentage of successfully fabricated WSI interconnects. The secondary objective was to measure the direct current resistance of the interconnects. This second measurement was used in conjunction with the interconnect geometry measurements to verify the interconnect resistivity. Resistivity can be calculated from:

$$\rho = \frac{wtR}{L} \qquad (4.5)$$

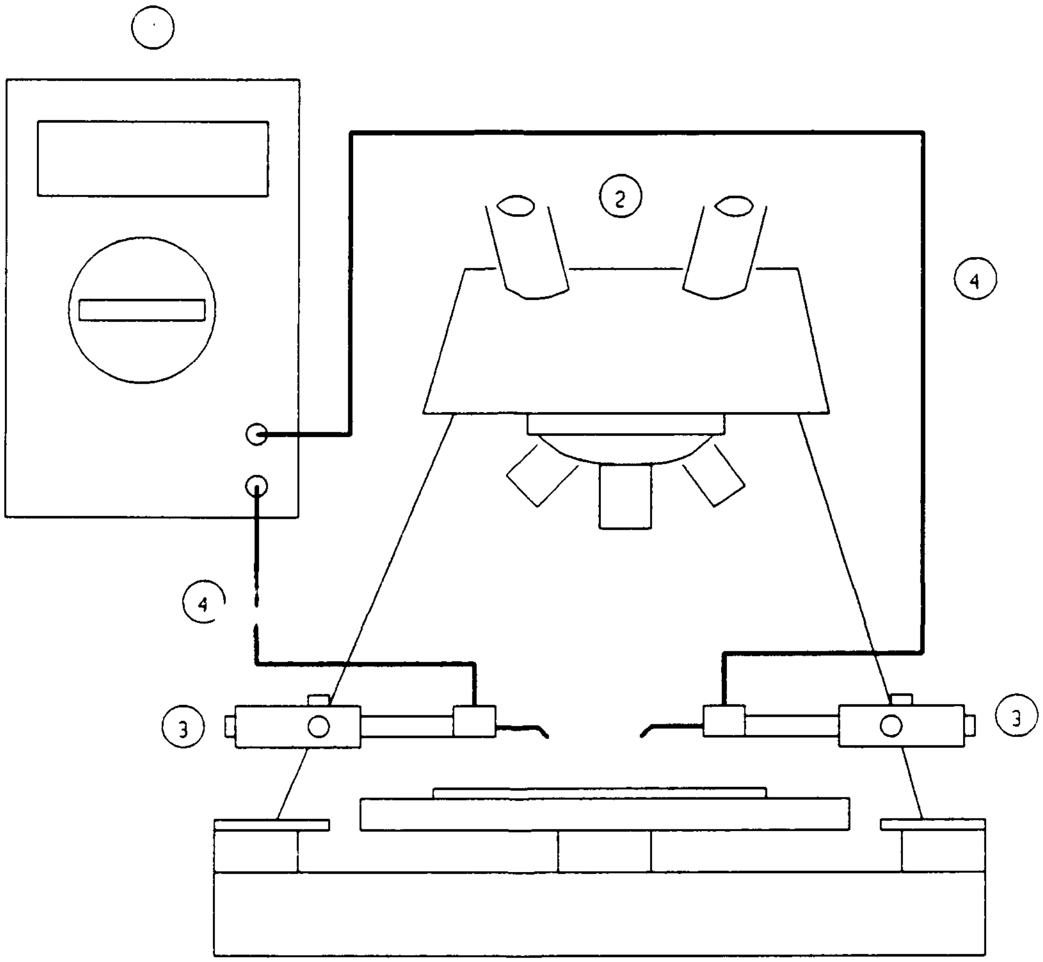


Figure 4.18. Test configuration for accomplishing the continuity and direct current resistance measurements. (1) Fluke 77/AN multimeter, (2) Micromanipulator 6200 probe station, (3) Micromanipulator 550 probes, (4) electrical cabling.

where

ρ is the metal resistivity
w is the interconnect width
t is the interconnect thickness
L is the interconnect length
R is the measured interconnect resistance.

Signal Attenuation and Propagation Delay. The test configuration used to perform this measurement is shown in Figure 4.19. Because no ground plane existed in either test article, an adjacent pair of interconnects was chosen to propagate the input signal. The interconnect pair used on both test articles is shown in Figure 4.20. The output port was measured using a high impedance load, on the order of 1 MΩ, and a low impedance load of 50 Ω.

The input signal was a square wave supplied by a signal generator. The frequency of this signal was varied from 1 kHz to 10 MHz, with measurements taken at each decade and selected intermediate frequencies. A simultaneous sweep of the input and output signals was digitized by the oscilloscope bus, and transferred to a personal computer for storage via an HP-IB interface. Data acquisition was controlled by the personal computer which executed the BASIC program presented in Appendix P.

The time period defined as the propagation delay is illustrated in Figure 4.21. This time period starts when the

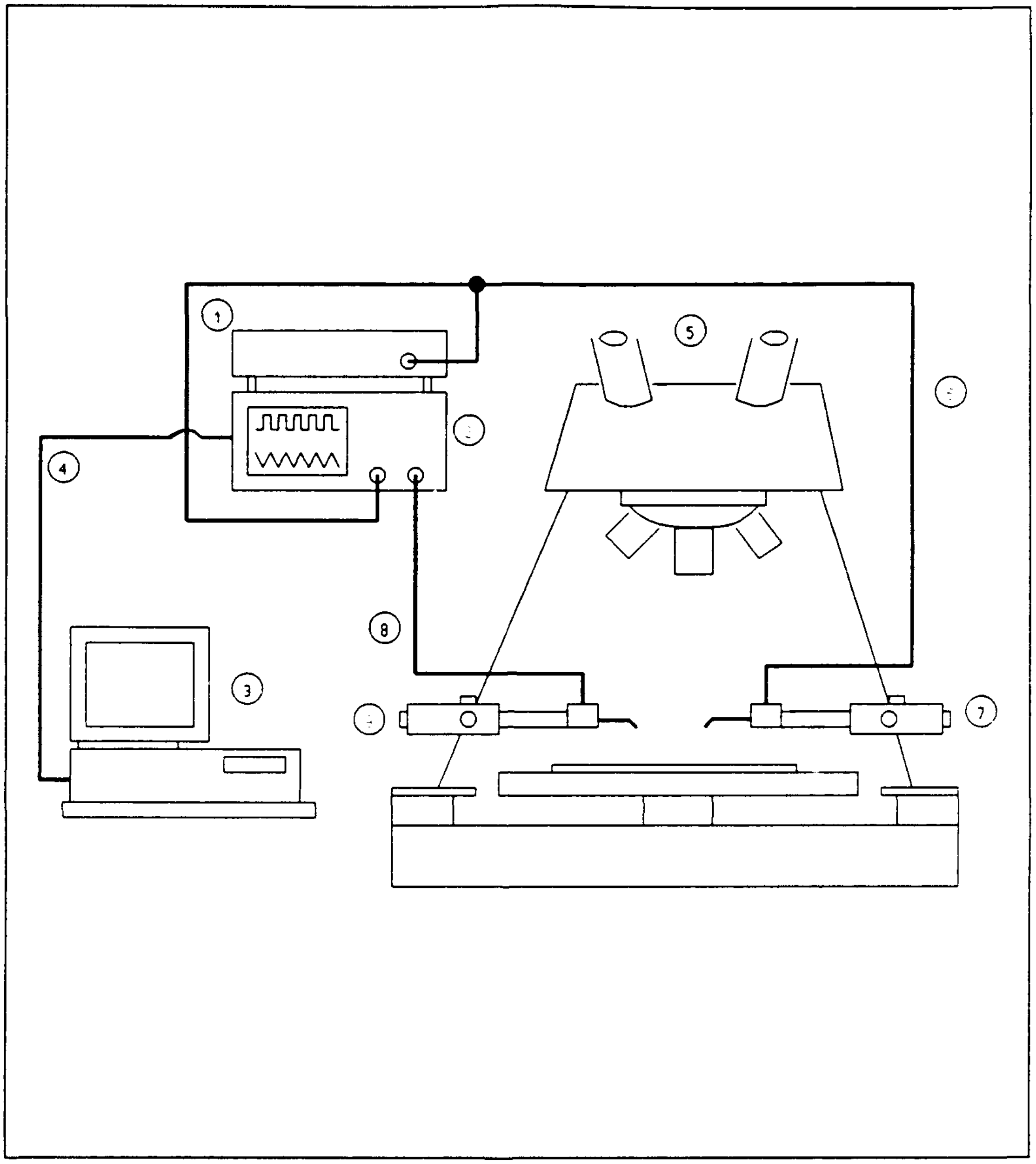


Figure 4.19. Test configuration for accomplishing the signal attenuation, propagation delay and coupling measurements. (1) Hewlett Packard HP 8082A pulse generator, (2) Hewlett Packard HP 54100A digitizing oscilloscope, (3) Zenith Z248 personal computer, (4) HP-IB connection, (5) Micromanipulator 6200 probe station, (6) input signal cable, (7) Micromanipulator 550 input probe, (8) output signal cable, (9) Micromanipulator 550 output probe.

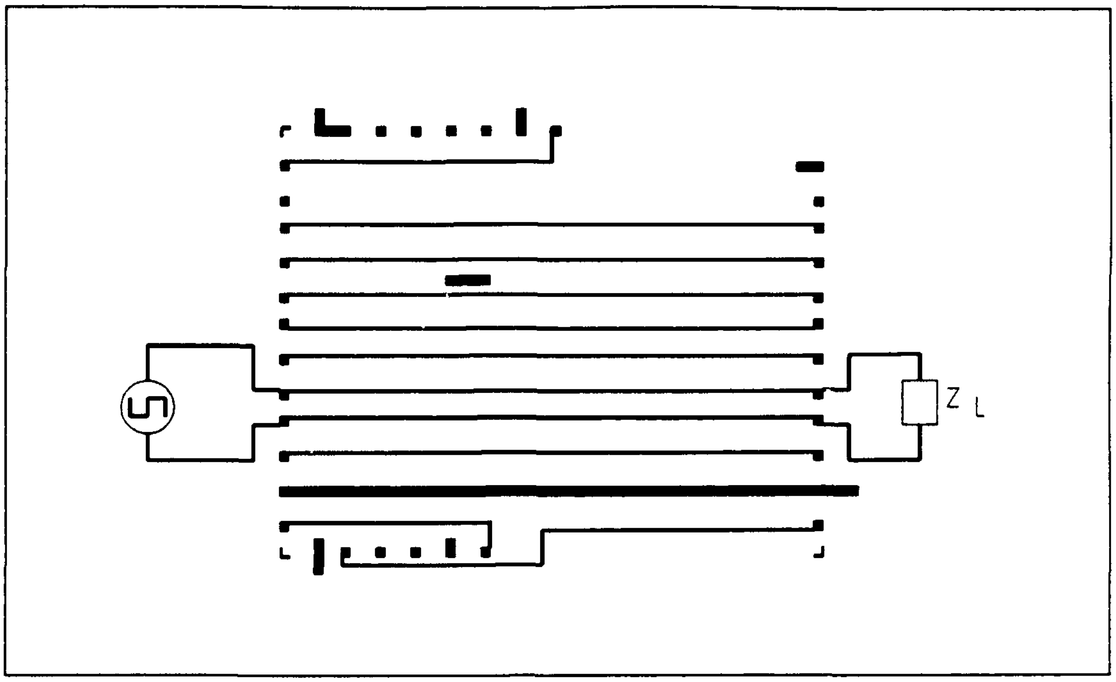


Figure 4.20. Interconnect pair utilized in the signal attenuation and propagation delay measurements.

input signal voltage value equals one half of the maximum applied voltage. The propagation delay time period ends when the output voltage equals one half of its maximum measured value. This propagation delay definition combines the effects of transmission line transit delay with the signal distortion resulting from the RC effect of the interconnect. Single pulse tests at selected frequencies were conducted to verify whether the propagation delay exceeded the period of the input signal. Attenuation was calculated from the magnitude difference between the two signals.

Signal Coupling. The test configuration used to perform the signal coupling measurements is identical to that used in the signal attenuation testing, as illustrated in Figure 4.19. An adjacent pair of interconnects was used to apply

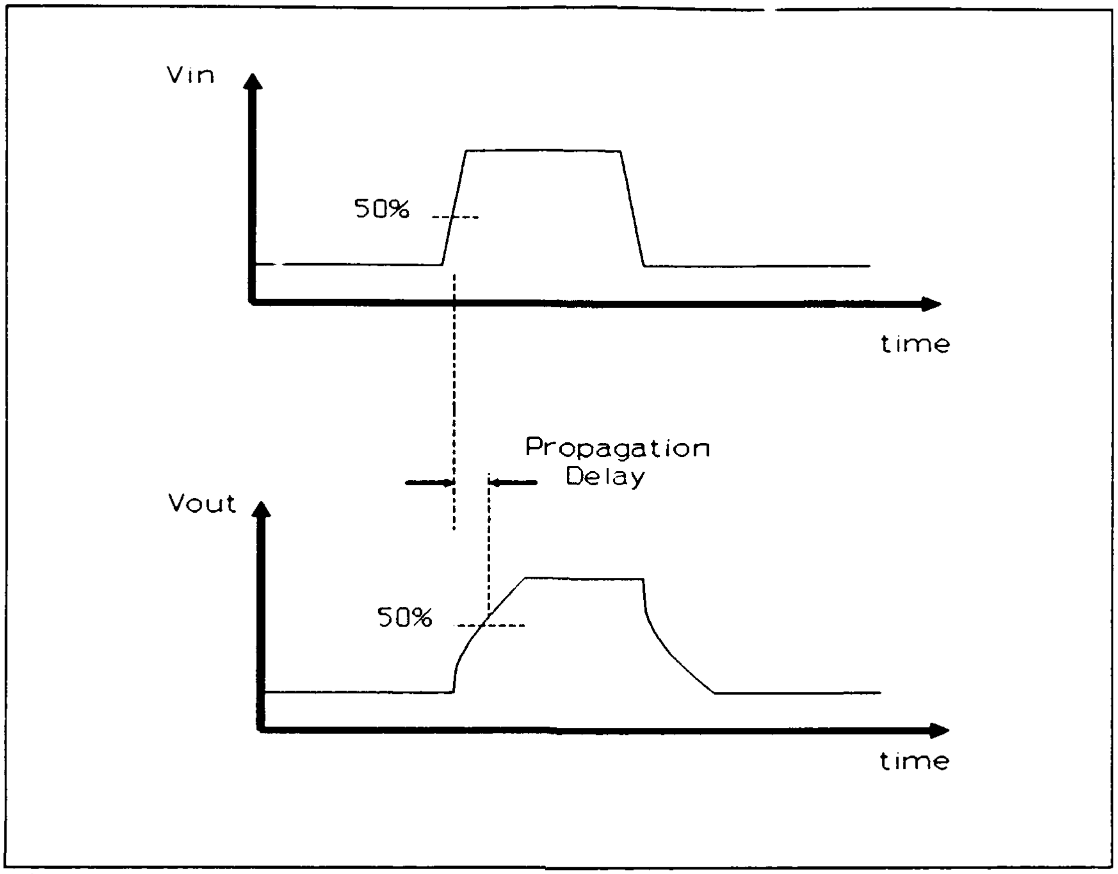
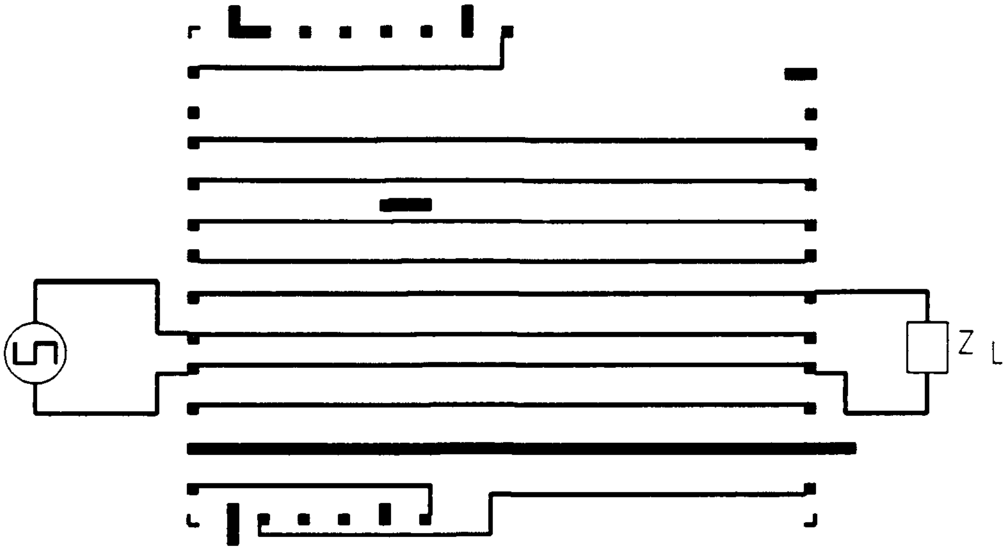


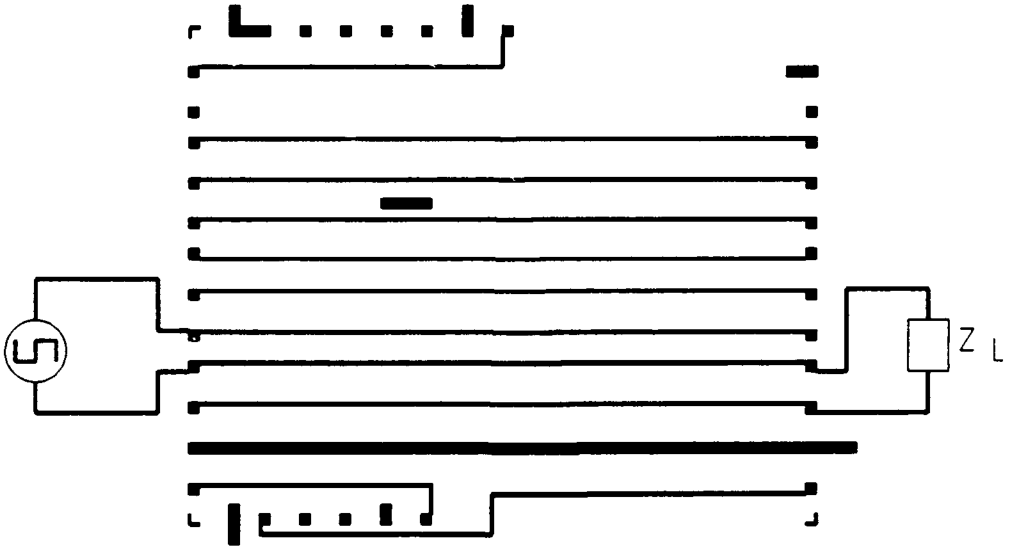
Figure 4.21. Example of the propagation delay measurement.

the input signal. The output signal was measured between the reference ground interconnect and each of the two nearest neighbors, as illustrated in Figure 4.22. A third set of measurements was taken using the interconnects indicated in Figure 4.23. This measurement characterized the crosstalk between the level-one and level-two metal interconnects.

Consistent with the attenuation tests, a square wave input signal was used, and the measurements were accomplished over the frequency range of 1 kHz to 10 MHz. The personal computer, executing the BASIC program presented in Appendix P, was used to control data acquisition and store the



(a) Configuration for first coupling measurement



(b) Configuration for second coupling measurement

Figure 4.22. Metallization interconnects utilized to accomplish the coupling measurements.

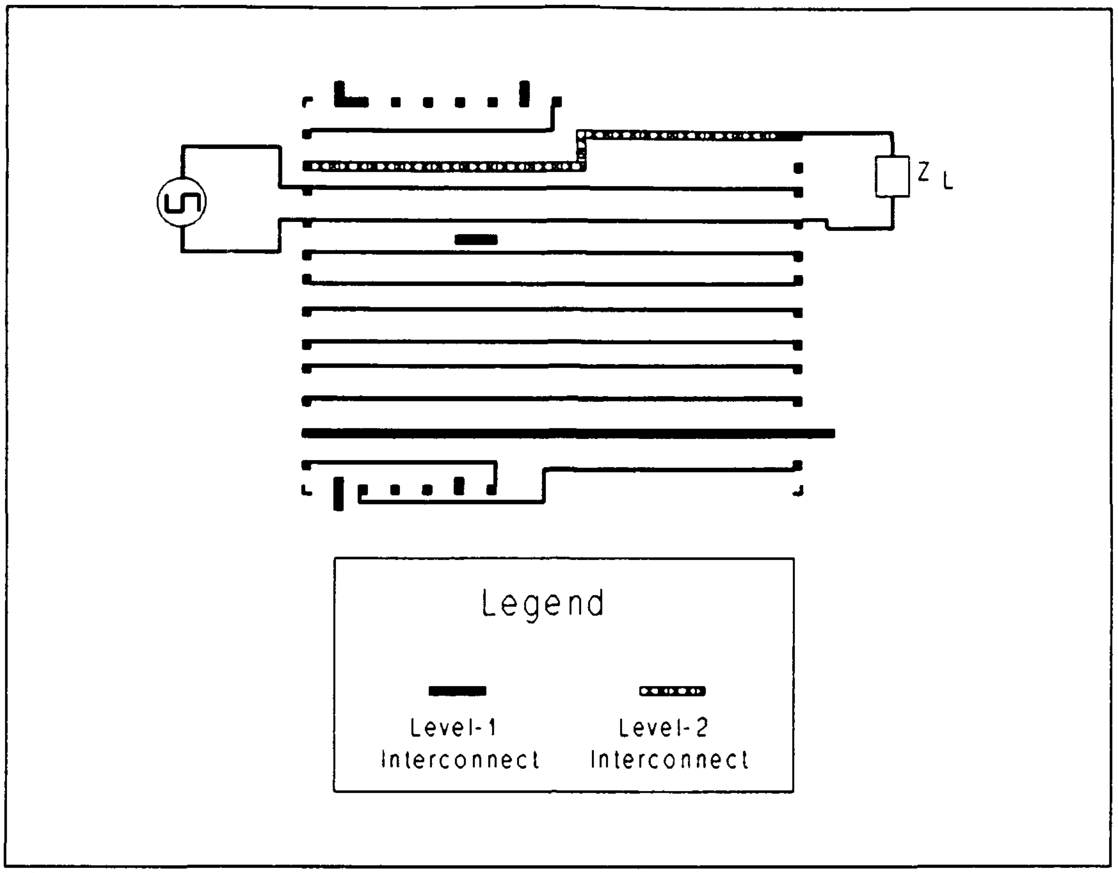


Figure 4.23. Metallization interconnects utilized to accomplish the interlevel coupling measurements.

digitized data processed by the oscilloscope. Measurements were taken with a 1 MΩ and a 50 Ω load.

Summary

This chapter described the procedures used to fabricate the proposed WSI configurations and the performance evaluation techniques that were implemented to determine their electrical characteristics. Prior to the discussion of the fabrication procedures, the methods for evaluating alternative IC die mounting schemes, candidate barrier coatings, and potential dielectric polyimide candidates were presented. The results of these preliminary investigations were incorporated to fabricate the WSI test articles.

The electrical performance evaluation procedures proposed in this chapter included direct current continuity tests to verify the success of the interconnect fabrication process, and a series of voltage pulse excitation measurements for analyzing the performance of the interconnects in terms of propagation delay, attenuation, and coupling.

V. Results and Discussions

This chapter presents the results of the procedures detailed in Chapter IV. This chapter is divided into four major areas that are related to the major WSI fabrication and test procedures discussed in the previous chapter. First, the IC die mounting results are presented, including those for the barrier coating and alternative die mount procedures. Next, the results associated with the candidate polyimide experiments are described and analyzed. The third section of this chapter details the measurements accomplished with the fabricated WSI circuits. Finally, the interconnect electrical characterization results are presented and analyzed.

IC Die Mounting Evaluation Results

The initial measurements in this research effort were focused on evaluating the recommendations of previous researchers that were subsequently implemented to improve the IC die mounting step of WSI circuit fabrication (10,24,39). These recommendations were focused on eliminating the epoxy bond between the optical alignment flat and the WSI assembly. The initial evaluation in this research effort involved screening a number of coatings applied to the optical alignment flat. The purpose of these coatings was to provide a surface that the IC die mount adhesive would not bond to, or to provide a sacrificial layer which could be selectively removed after the adhesive was cured to release the WSI assembly. The results of this evaluation indicated the requirement for modifying the IC die mount procedure. A number of alternative procedures were proposed and evaluated. This section details the results of the barrier coating and alternative die mount procedure evaluations.

Barrier Coating Evaluation. Previous AFIT researchers indicated that a major obstacle in the WSI fabrication process concerned the adhesion of the WSI assembly to the optical alignment flat. One recommendation to overcome this obstacle was to coat the optical flat with a material which would prevent adhesion of the epoxy. A number of candidate materials were evaluated for this purpose. This evaluation focused on identifying a number of key characteristics desired of the coating material.

A list of the candidate materials and their ranking relative to the evaluation areas appears in Table 5.1. The material with the best performance in each evaluation area received a ranking of 1, followed by 2 for the second best material, and so on. The rankings for ease of application were based upon the complexity of the required coating process, and repeatability. Coating thickness uniformity rankings were established by the smoothness of the material layer, as measured by the stylus profilometer. The stylus profilometer measurement for the uncoated optical flat is

Table 5.1. Evaluation of Barrier Coating Materials.

Material	Ease of Application	Coating Thickness Uniformity	Heat Resistance	Barrier Success	Overall Rating
Teflon® Spray	5	4	1	1	Pass
Crown Mold Release	6	3	5	5	Fail
MS-122 Spray	4	5	2	2	Fail
MS-145 Release Agent	3	6	N/A	N/A	Fail
Shipley Photoresist	1	1	2	2	Fail
Ultradel Polyimide	1	1	2	2	Fail

presented in Figure 5.1 as a reference. For the heat resistance category, the rankings were based upon the material's ability to maintain consistent solubility properties without melting when exposed to the required epoxy cure temperature. The rankings for barrier success were based upon the success of the material in preventing epoxy adhesion to the optical alignment flat. If the coating succeeded in preventing epoxy adhesion to the optical alignment flat, it received an overall pass rating.

<u>Teflon® Spray</u>. One advantage in the application of this material was that it was a "dry spray"; that is, the coating was not a fluid when it was applied. The material

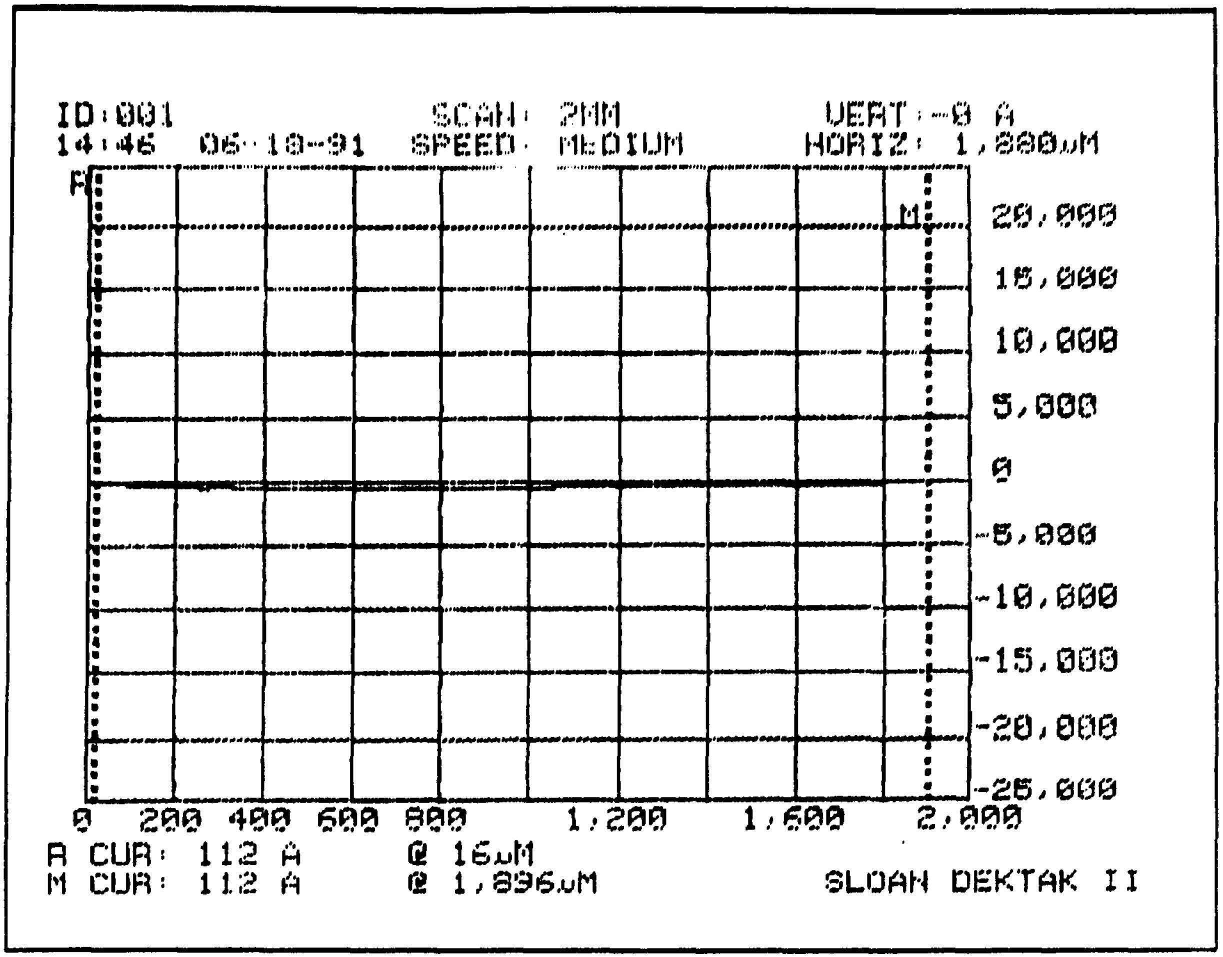


Figure 5.1. Profilometer measurement of an uncoated optical alignment flat surface.

did have a number of disadvantages relative to its ease of application. First, polishing the optical flat with a soft cloth after applying the coating was required to remove excess material. The resulting surface was relatively rough with variations on the order of ±2 microns. Figure 5.2 illustrates the profilometer measurement of a Teflon® coated optical flat surface. Also, multiple applications were required for each surface to eliminate void regions in the coating. Observations of the coatings under an optical microscope indicated that approximately five applications with intermediate polishing produced a usable coating. Also,

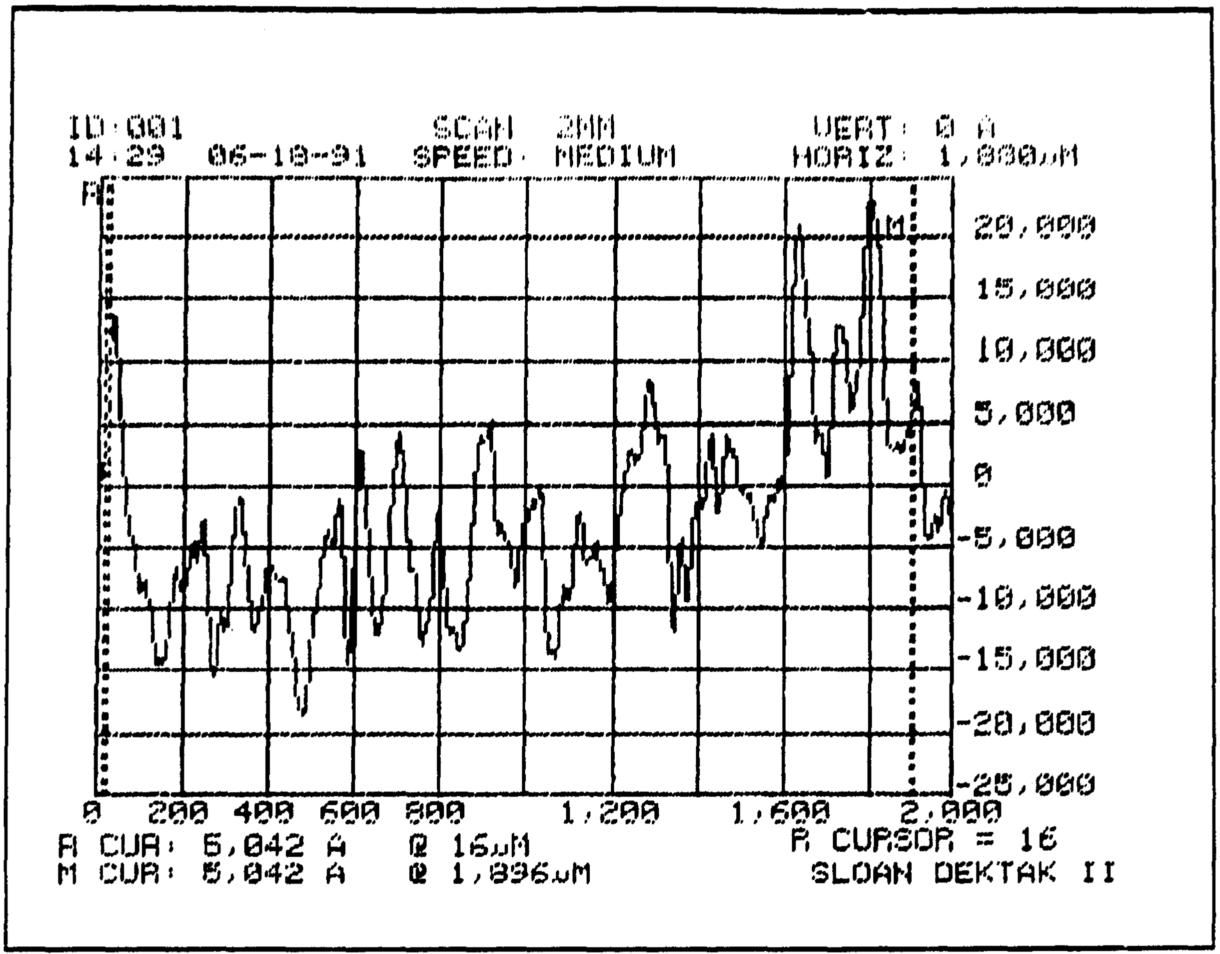


Figure 5.2. Profilometer measurement of a polished Teflon® coating on the optical alignment flat after five spray applications.

the Teflon® coating was prone to scratching during handling, and acetone cleaning of the excess epoxy damaged the coating. As a result, each Teflon® coating could only be used once in the IC die mounting process.

Although the application procedure for Teflon® was cumbersome, this material was superior in the last two categories. Heating the material to the epoxy cure temperature had no apparent effect on the Teflon® spray coating, and the washer assembly was successfully separated from the surface with minimal force after the epoxy's cure.

Crown Mold Release Spray. This material received the poorest rating with respect to ease of application because it required the most processing steps. The mold release spray, unlike the Teflon® spray, was very fluid and uneven when dispensed on the vertically oriented optical flat. To produce an even coating, the optical flat was first sprayed with the mold release spray, and then it was placed on the photoresist spinner. The optical flat was spun at 1000 RPM for 15 seconds, followed by polishing with a light cloth to remove excess coating material. The resulting surface exhibited thickness variations on the order of ±1.5 microns. Figure 5.3 depicts the results from a typical surface profilometer measurement. This material received the poorest rating in the heat resistance category because it was the only coating to catastrophically fail during the epoxy cure test. After approximately five minutes on the hot plate at 175°C, the material began to melt. The coating formed beads on the optical flat's surface. The result was adhesion of the epoxy to the optical flat, and overall failure of the coating.

MS-122 Spray. This material received a better ranking in the ease of application category compared to the Teflon® spray because it did not require multiple applications, although it was also a "dry spray". The final coating was slightly rougher, with thickness variations on the order of ±2.5 microns. The profilometer measurement of

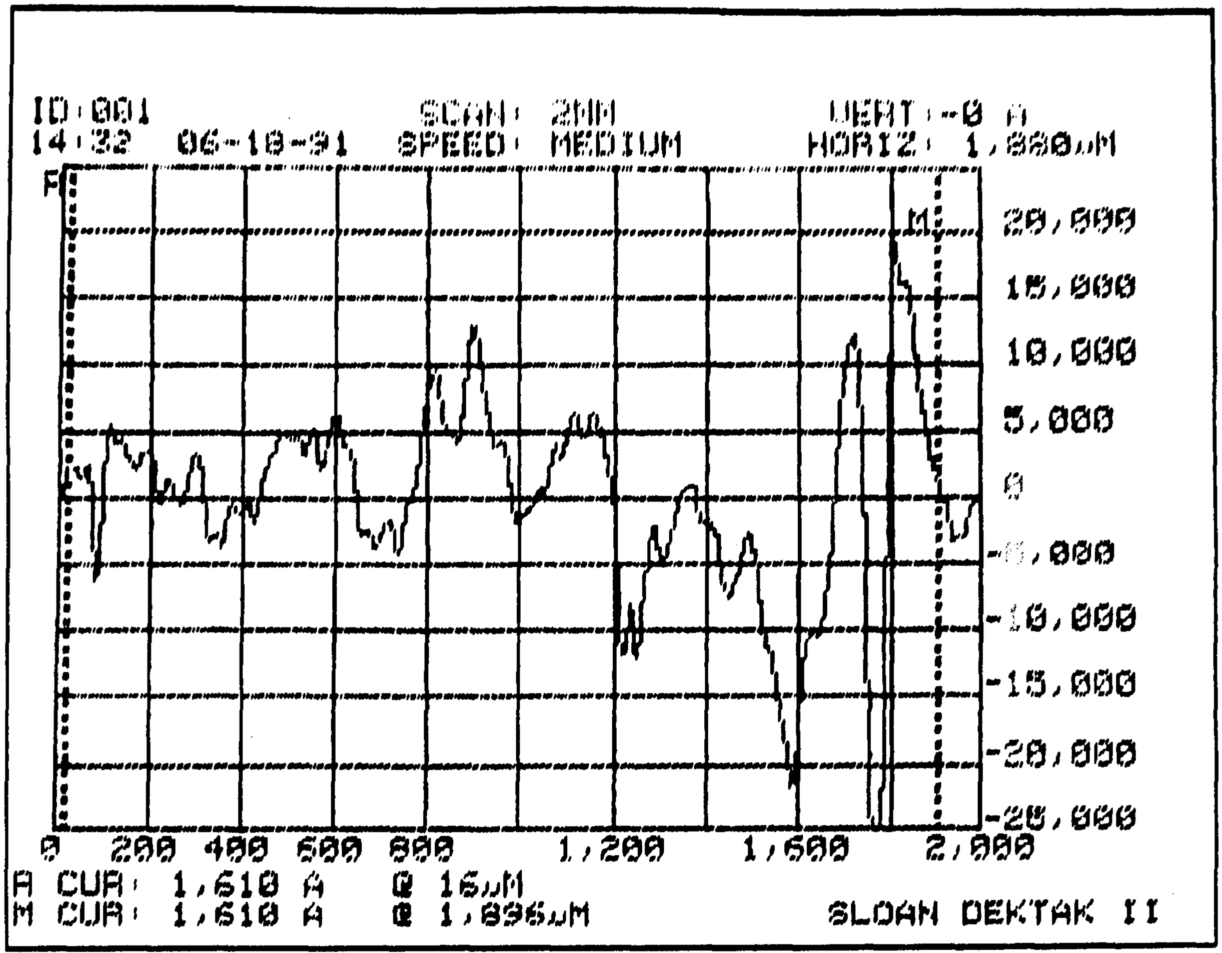


Figure 5.3. Profilometer measurement of the Crown mold release coating applied to the optical alignment flat.

this coating is illustrated in Figure 5.4. The material showed no apparent reaction to the heat applied during the epoxy's cure. However, the material failed to prevent adhesion between the epoxy and the coated reference flat. Thus, this material received a "fail" in the overall rating.

<u>MS-145 Release Agent</u>. This material was applied in liquid form, using a spin coating process. The initial coating appeared uneven, and polishing was required to remove excess material. However, light polishing with a soft cloth tended to remove virtually all of the material. Figure 5.5 illustrates the measured surface profile after the light

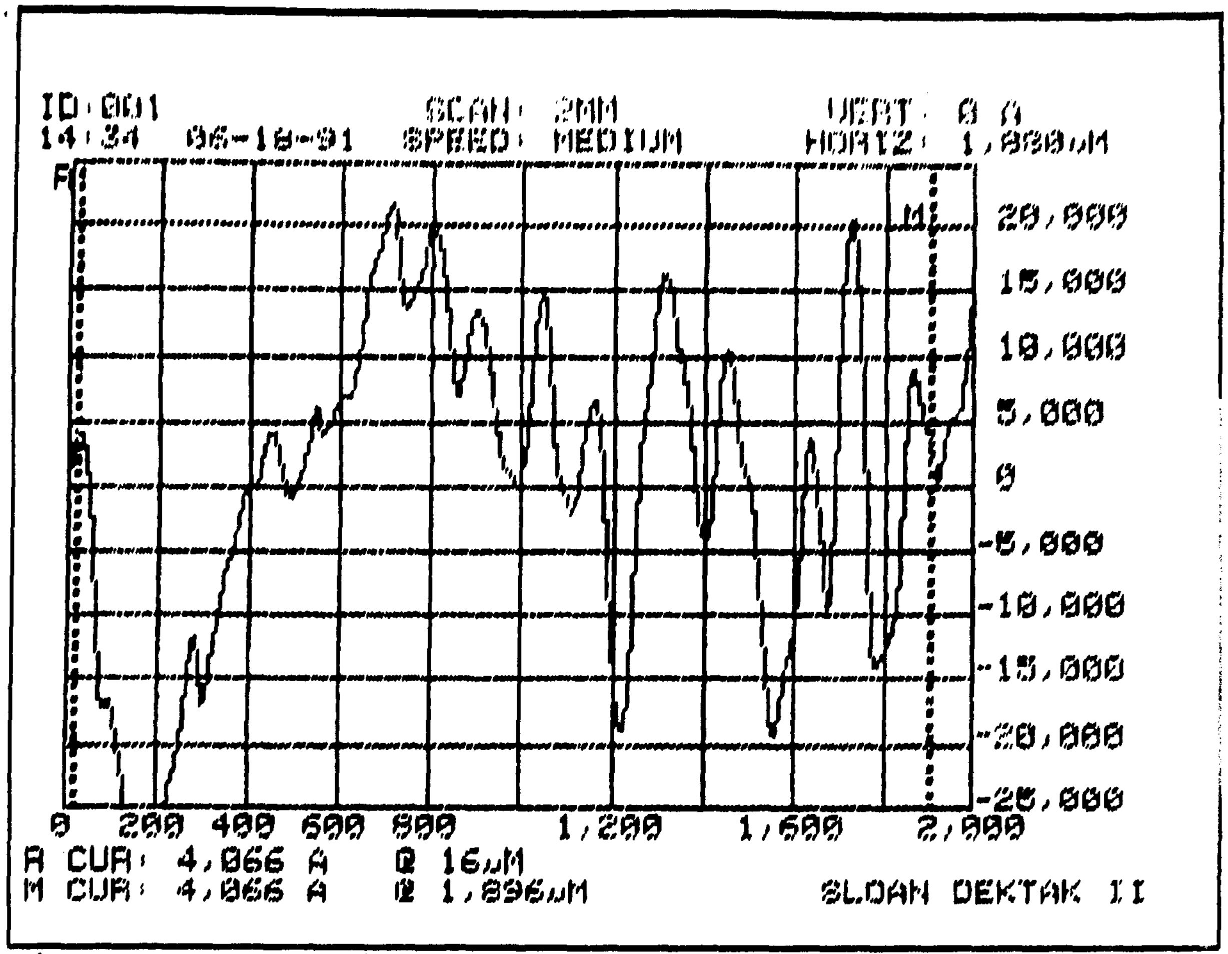


Figure 5.4. Profilometer measurement of the MS-122 coating applied to the optical alignment flat.

polishing process. Because this material failed to adhere to the reference flat, the epoxy cure test was not conducted, and the material received an overall "fail" rating.

<u>Shipley 1815 Photoresist</u>. Unlike the materials discussed previously, the photoresist coating was intended to act as a sacrificial layer rather than as an adhesion barrier. Adhesion between the photoresist and the epoxy was anticipated. Once the epoxy cure was complete, the photoresist layer was to be dissolved in an acetone bath, thus freeing the WSI assembly from the optical alignment flat.

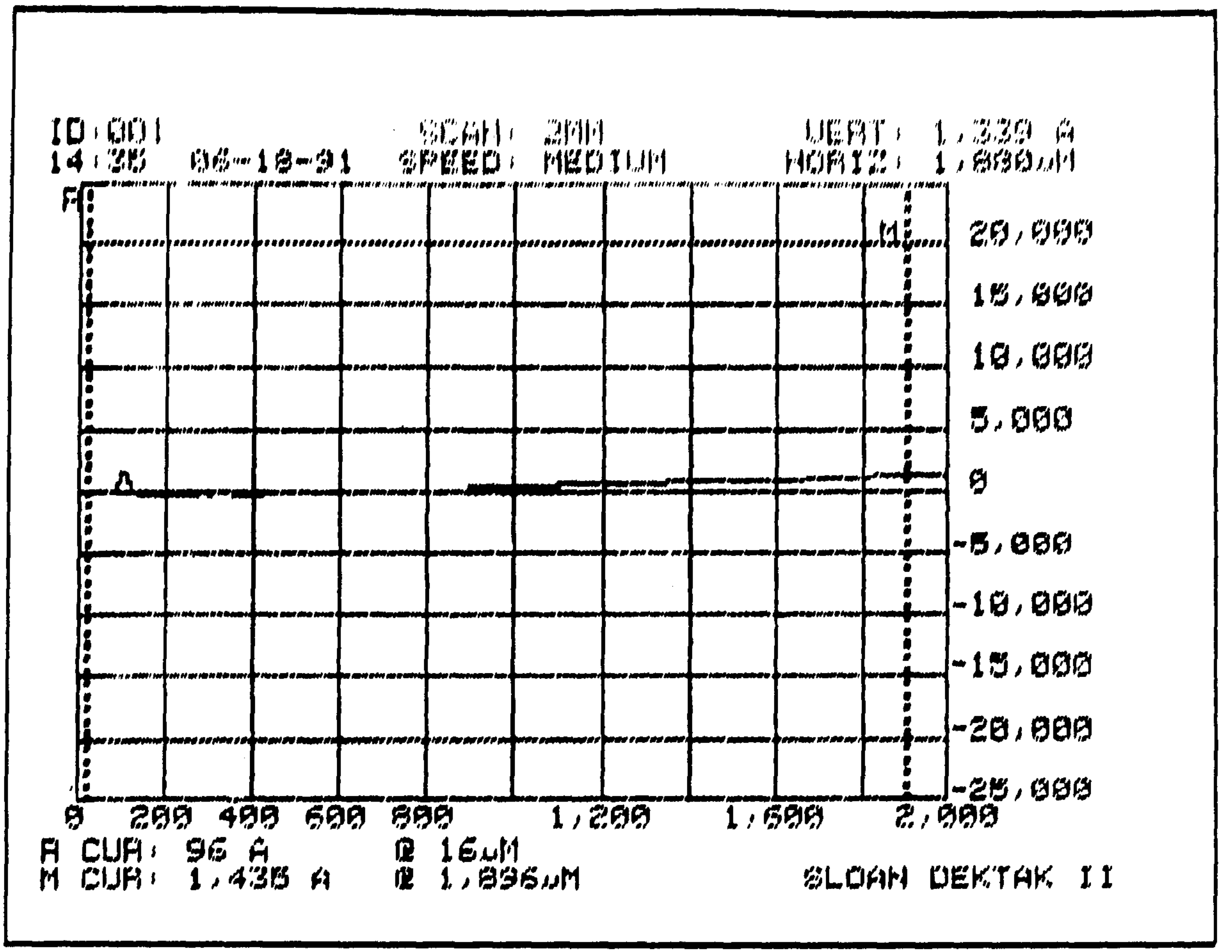


Figure 5.5. Profilometer measurement of the MS-145 coating applied to the optical alignment flat.

This material ranked highest in the ease of application and coating thickness uniformity categories. No additional polishing was required after the spin coating process, and the resulting coating exhibited surface deviations on the order of ±0.1 microns. The corresponding profilometer measurement is presented in Figure 5.6. Although the material did not change in appearance during the cure test, the high temperature did affect the photoresist material properties. Specifically, the photoresist coating subjected to the epoxy cure test would not readily dissolve in acetone, and the washer assembly could not be removed from the optical

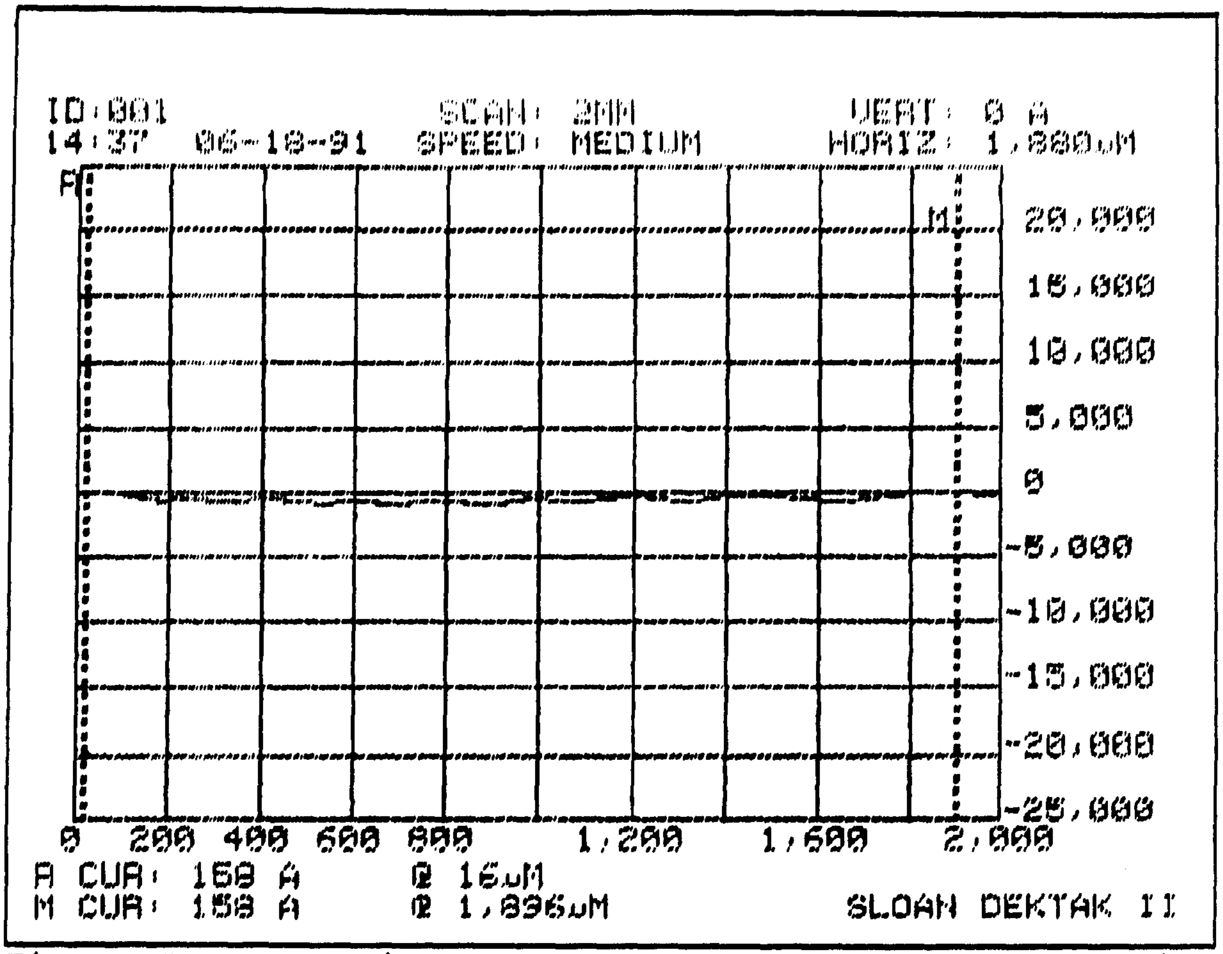


Figure 5.6. Profilometer measurement of the photoresist coating applied to the optical alignment flat.

alignment flat. An additional set of tests revealed that acetone would not dissolve a photoresist layer which was subjected to cure temperatures above 125°C.

<u>Ultradel 4501 Polyimide</u>. In this study, the polyimide coating was intended to be a sacrificial layer, similar to the Shipley 1815 photoresist. This material was applied to the optical alignment flat using a spin coating process, and it required no additional polishing. Surface thickness variations of the coating were on the order of ±0.1 microns. The profilometer measurement for this coating is illustrated in Figure 5.7. However, the material's

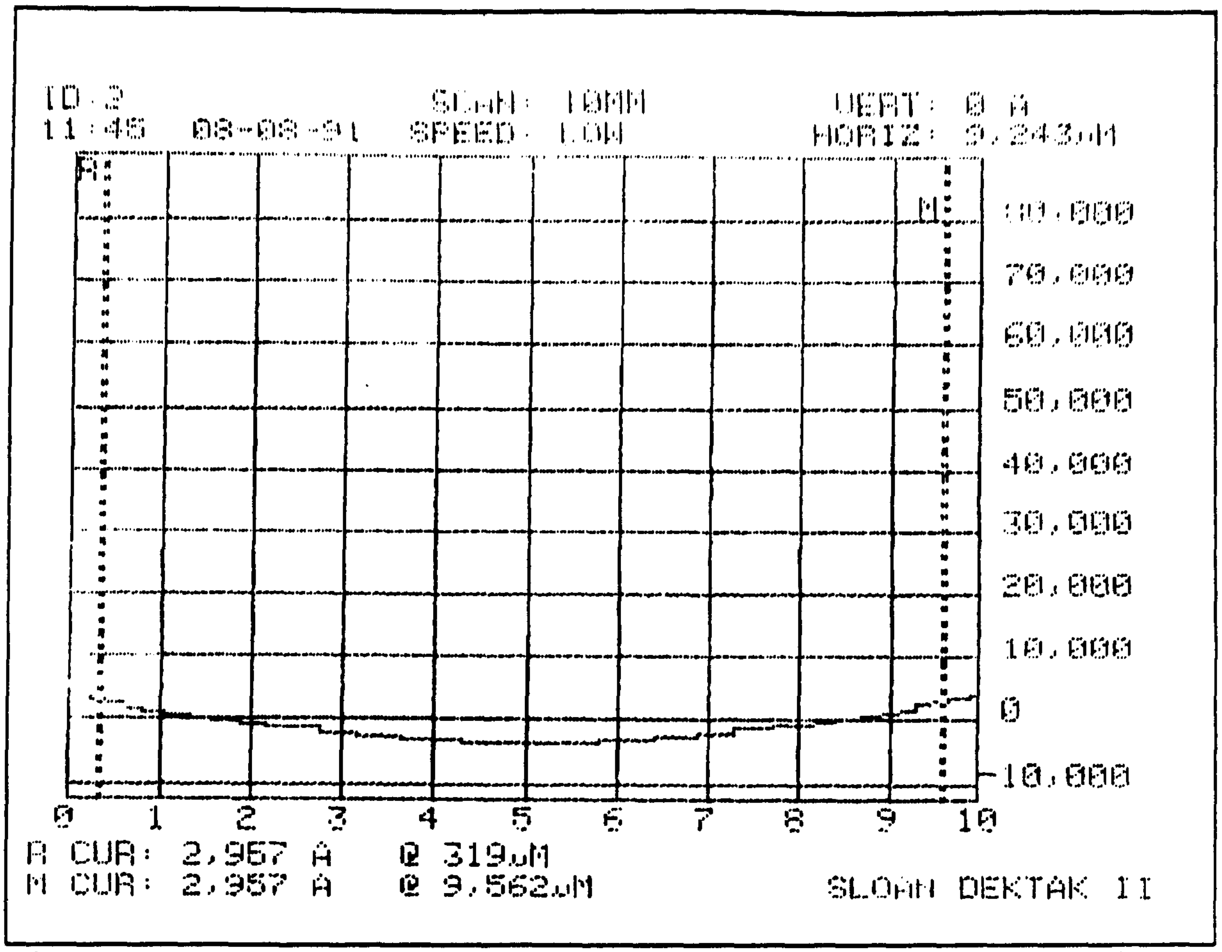


Figure 5.7. Profilometer measurement of the polyimide coating applied to the optical alignment flat.

solubility was affected by the high epoxy cure temperature. The Ultradel material begins to imidize at temperatures above 150°C (31). This imidization process hardens the coating and reduces the material's solubility. Once the epoxy was cured in the wafer assembly, the polyimide was sufficiently hardened that immersion in an etchant solution failed to remove the coating, and the washer assembly could not be removed from the optical alignment flat.

Summary of Barrier Coating Evaluation Results. As illustrated in Table 5.1, only the Teflon® coating provided an adequate barrier for the specific epoxy and cure schedule chosen for this study. This material was selected as the barrier coating for the remainder of this research project.

While conducting the barrier coating evaluation, certain key characteristics of the epoxy adhesive material were observed. The primary concern was focused on the adhesive's viscosity transition during the cure cycle. At room temperature, after mixing, the epoxy was thick and difficult to apply as a uniform thin coating. However, the material became fluid-like at 175°C, and tended to flow onto the surface of the optical alignment flat and washers. Figure 5.8 illustrates an example from the coating evaluations. Epoxy which flows and coats the surface of an IC die in this manner would prevent subsequently applied WSI metal patterns from electrically connecting the circuits. This finding indicated that the standard IC die mount procedure must still include periodic surface cleaning to remove excess epoxy, or it must be modified to reduce epoxy leakage onto the surface of the IC die.

Alternate IC Die Mount Procedure Findings. A number of alternative die mount procedures were proposed. The goal in developing these alternative procedures was to eliminate the epoxy leakage problem or reduce the number of required cleaning steps to realize a more efficient and repeatable procedure.

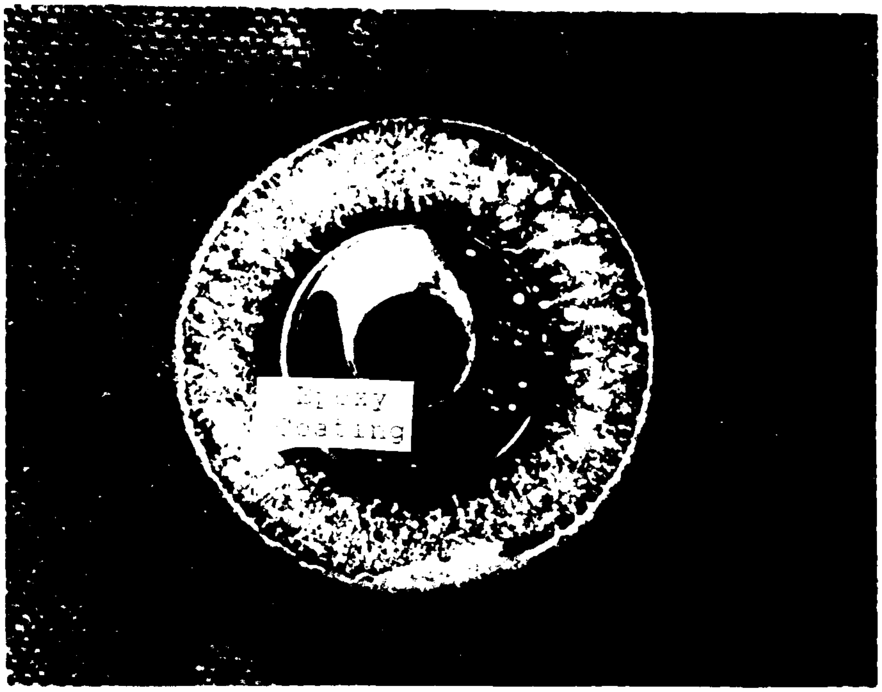


Figure 5.8. Test article from barrier coating evaluation.

Epoxy IC Die Mounting with a Clamped Substrate. The purpose of the clamping jig in this alternative approach was to provide a uniformly distributed force on the planarizing substrate to improve contact between it and the optical alignment flat surface. In its implementation, pressure was applied to the IC die to improve their surface contact as well. This jig was successful in reducing the epoxy's leakage onto the substrate's surface. However, the epoxy still migrated onto the surface of the IC die because of the uneven topology created by the circuit features. This topology is illustrated in Figure 5.9 Thus, this mounting procedure required surface cleaning with acetone at five minute intervals until the gap region was sealed and no excess epoxy was observed on the IC die surface. In a number of cases, the bond between the IC die and the substrate failed during cleaning, requiring that the entire process be repeated.

Polyimide IC Die Mounting with a Clamped Substrate.

Polyimide was evaluated as an alternative adhesive for two reasons. First, the polyimide required a lower cure

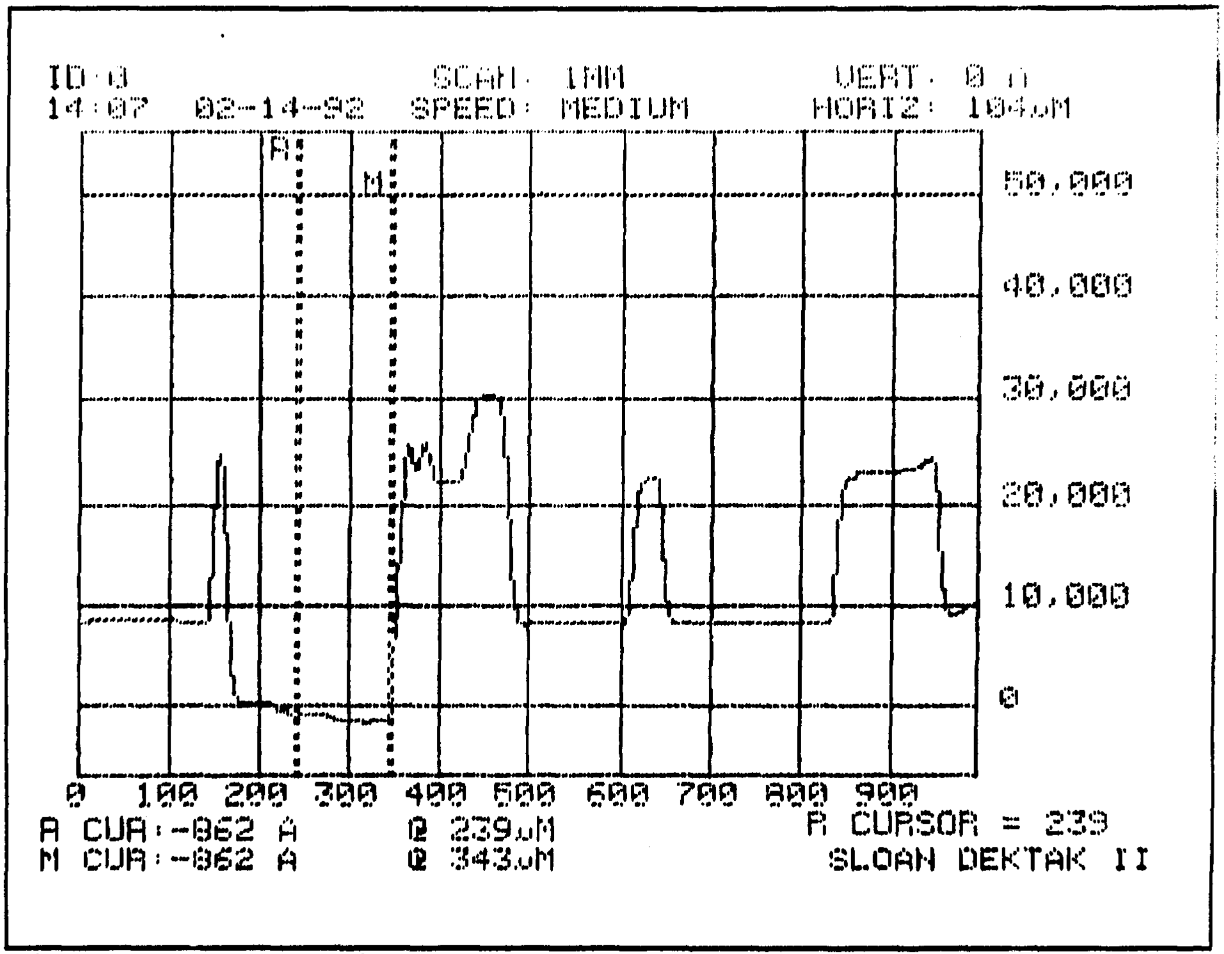


Figure 5.9. Profilometer measurement of the IC die surface topology.

temperature compared to the epoxy, which motivated the consideration and use of sacrificial coatings. Second, a partially cured polyimide coating over the IC die metal contact pads (due to leakage during cure) could be readily patterned to facilitate the successful interconnection of the WSI system. Therefore, the polyimide could be cured without intermediate cleaning steps.

This procedure proved unsuccessful, however. The polyimide material was not designed to be cured as the thick, enclosed column presented by the geometry of the gap region between the IC die and the host substrate. In this application, the polyimide initially cured on its exposed top surface and trapped solvent material in the underlying polyimide. In an attempt to resolve this situation, the cure duration was increased from 15 minutes to four hours, with no apparent affect on the degree of polyimide curing. When the substrate and reference flat were separated, the semi-cured polyimide tended to tear, resulting in a failed bond between the IC die and the substrate.

Substrate Pre-Assembly Procedure. In this alternative procedure, the planarizing and support substrates were bonded prior to the introduction of the IC die. This pre-assembled substrate provided cavities into which the IC die and a small amount of epoxy were placed, with the IC die facing up. In this scheme, the epoxy tended to remain in the cavity rather than flowing over the surface of the IC die.

One key disadvantage was observed in this procedure. The bottom of each cavity did not initially contain any epoxy at the start of the substrate bonding process. However, excess epoxy tended to flow into the cavities when the assembly was raised to the epoxy's cure temperature. A cleaning step with acetone was performed after 10 minutes of heating to remove the excess epoxy in the IC die cavities. Figure 5.10 depicts an IC die cavity after cleaning. As Figure 5.10 illustrates, a small amount of epoxy remained in the corners of the IC die cavity. This cleaning step was

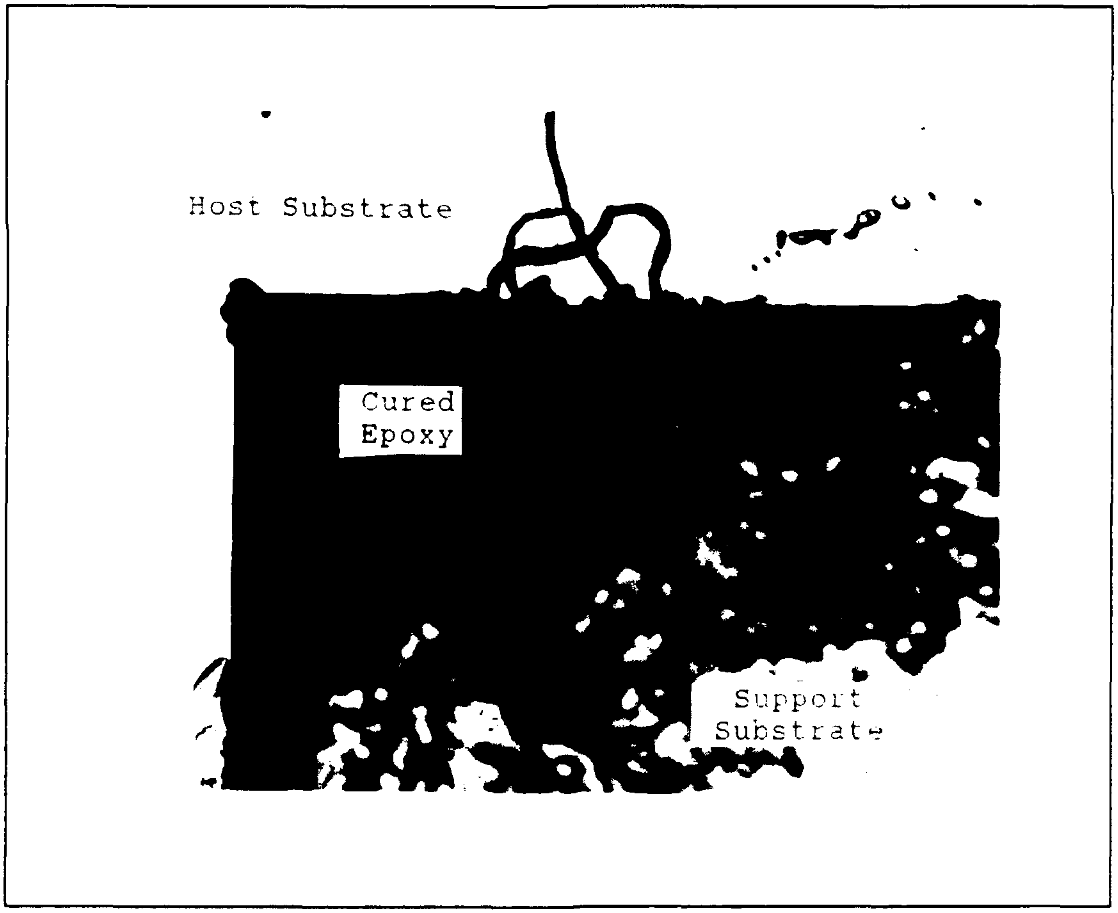


Figure 5.10. Top view of an IC die cavity after the substrate assembly was realized.

incomplete because of the IC die cavity geometry, as shown in Figure 5.11. The overhanging silicon surface, particularly in the corners of the IC die cavity, combined with the small dimensions of the cavity, made the affected areas inaccessible to the mechanical cleaning tool. The excess epoxy resulted in an uneven cavity bottom which subsequently affected the planarity of the IC die.

Another disadvantage of this procedure was the difficulty encountered in placing the IC die into the

Figure 5.11. Cross-sectional view of an IC die cavity after the substrate assembly was realized.

cavities. To reduce the size of the gap region between the IC die and the substrate, the cavity opening was sized to be 50 microns larger (on each side) compared to the IC die. This limitation required perfect alignment of the IC die with respect to the cavity during mounting. The cavity edges were often damaged during this step due to misalignment. This method did exhibit a reasonable level of repeatability during this evaluation, and planar measurements of the IC die mounted using this procedure were generally within tolerance. Two test articles, Wafers A and B, were assembled using this procedure. Planarity measurements from these two test articles are presented in a subsequent sub-section. In addition, this method reduced the number of required surface cleanings and the overall fabrication time for the WSI assembly.

Single-Step IC Die Mount Procedure. This procedure was proposed to overcome the primary disadvantage observed in the Substrate Pre-Assembly procedure, which was the IC die planarity deficiency caused by the residual cured epoxy in the IC die cavity corners. In this method, the IC die were placed in their cavities at the same time that the substrates were bonded together. This alternative procedure also allowed the IC die to be placed in their cavities through the larger etched window opening, eliminating the tight tolerance problem observed in the Substrate Pre-Assembly procedure.

In this alternative procedure, the assembly was initially cured with the IC circuit facing downward (contacting the optical alignment flat). This procedure resulted in the epoxy leaking and coating the IC die in a manner similar to the problem observed in the previous methods. However, this method required only one application of epoxy and two surface cleanings, thereby reducing assembly time and workload. This procedure exhibited the highest degree of repeatability and planarization between the IC die and the substrate surfaces. Six test articles, Wafers C, D, 1, 2, 3 and 4, were assembled using this IC die mount procedure. Planarity measurements are presented in a subsequent sub-section for these test articles.

Summary of Alternative IC Die Mount Procedure Evaluations. Three of the four methods investigated produced acceptable results. In the fourth method -- the Polyimide IC Die Mounting with a Clamped Substrate -- the adhesive always failed to bond the IC die in the host substrate cavity. Also, although the Epoxy IC Die Mount with a Clamped Substrate procedure did produce an acceptable sample, the results were not repeatable, and the procedure was labor-intensive and lengthy.

Based upon these results, the Substrate Pre-Assembly and Single-Step IC Die Mount procedures were selected for further investigation in the fabrication of the WSI circuits. Samples using both methods were produced and evaluated in terms of the degree of the IC die-to-host substrate planarization and success in producing metal interconnects across the transition region.

Polyimide Evaluation Findings

The three candidate polyimides were initially evaluated using bare silicon wafers. This preliminary evaluation was focused on establishing the patternability and planarity capabilities of these materials. In patterning a polyimide, the ability to produce sloped side walls in the vias through the polyimide layer was considered to be a critical requirement. Planarization in this evaluation was measured on a second layer of polyimide that was applied over the vias in the first layer. Although curing temperatures of at least 300°C were recommended for all three candidate polyimides, the choice of the IC die mounting epoxy limited the subsequent processing temperatures to 250°C. This reduced cure temperature poses two potential problems: increased moisture content in the polyimide, and incomplete imidization of the material. The former characteristic can lead to long term reliability problems, but can be controlled by increasing the polyimide's cure duration. The latter quality can also affect the electrical properties of the material. To evaluate this effect, two sets of capacitors were fabricated from each polyimide, one using the standard 250°C cure schedule illustrated in Figure 4.4, the other using the cure schedule recommended by the manufacturer for that polyimide. These capacitors were electrically tested to determine the effect of cure temperature (and duration of cure) on the polyimide's relative dielectric constant and dissipation factor.

For the non-photosensitive Ultradel 4212 polyimide, the slopes of the via side walls were controlled by varying the softbake temperature. The manufacturer recommended a softbake temperature of 100°C to produce vertical via side walls. By increasing this temperature to a level less than 150°C, partial imidization occurred prior to patterning. Etching partially imidized polyimide produced via side walls whose slope was a strong function of the softbake temperature. The resulting slope in the via side walls for samples prepared using softbake temperatures of 120°C and 140°C are shown in Figures 5.12 and 5.13. The via side wall slope measured from these photographs is summarized in Table 5.2. Samples prepared using a softbake temperature of 150°C produced vias which could not be completely etched, because of the degree of imidization. As shown in Table 5.2, the samples produced using a 100°C softbake cure exhibited nearly vertical via side walls.

Proximity printing was used to produce sloped via side walls with the two photosensitive polyimides. This method proved successful with the Selectilux HTR3-200 polyimide as illustrated in Figures 5.14 and 5.15. As these two figures

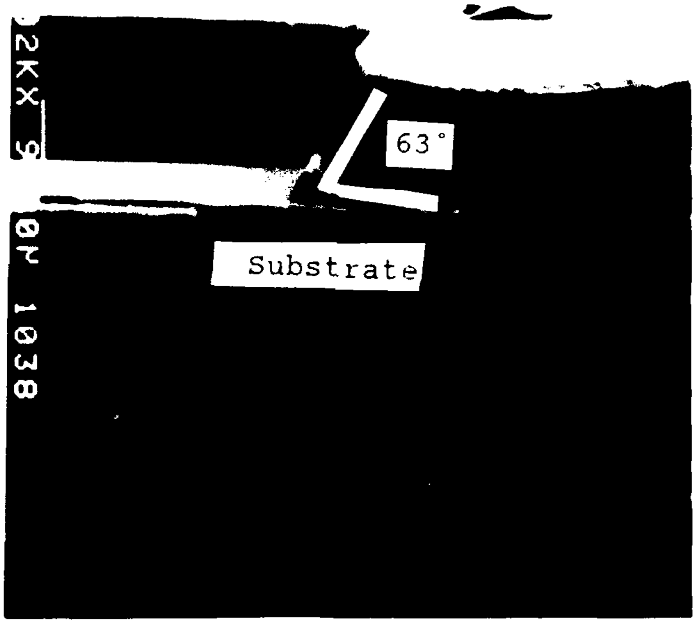


Figure 5.12. Cross-sectional view of a via with a side wall slope equal to 63° formed in the Ultradel 4212 polyimide using a 120°C softbake process.

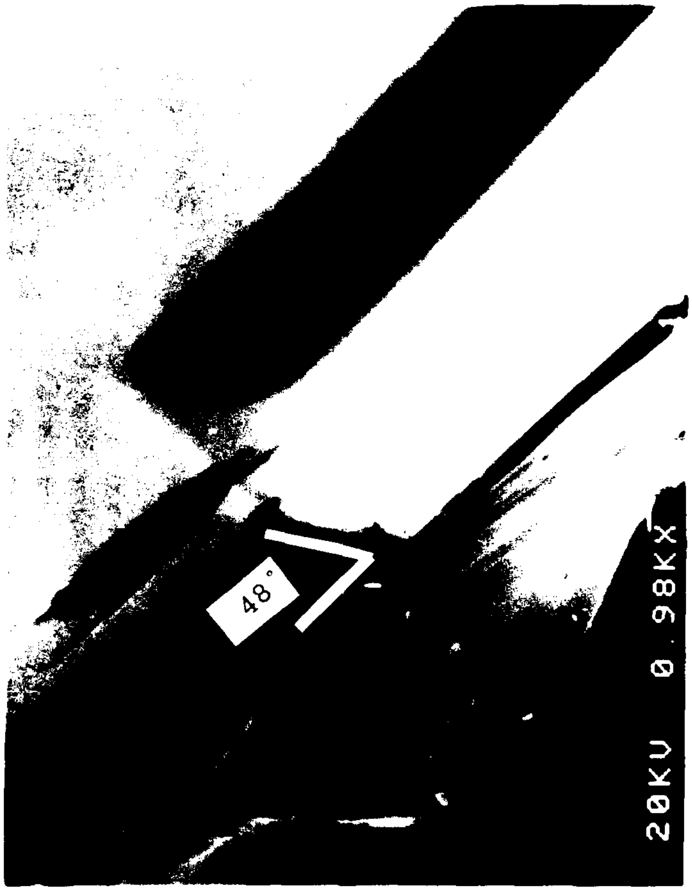


Figure 5.13. Cross-sectional view of a via with a side wall slope equal to 48° formed in the Ultradel 4212 polyimide using a 140°C softbake process.

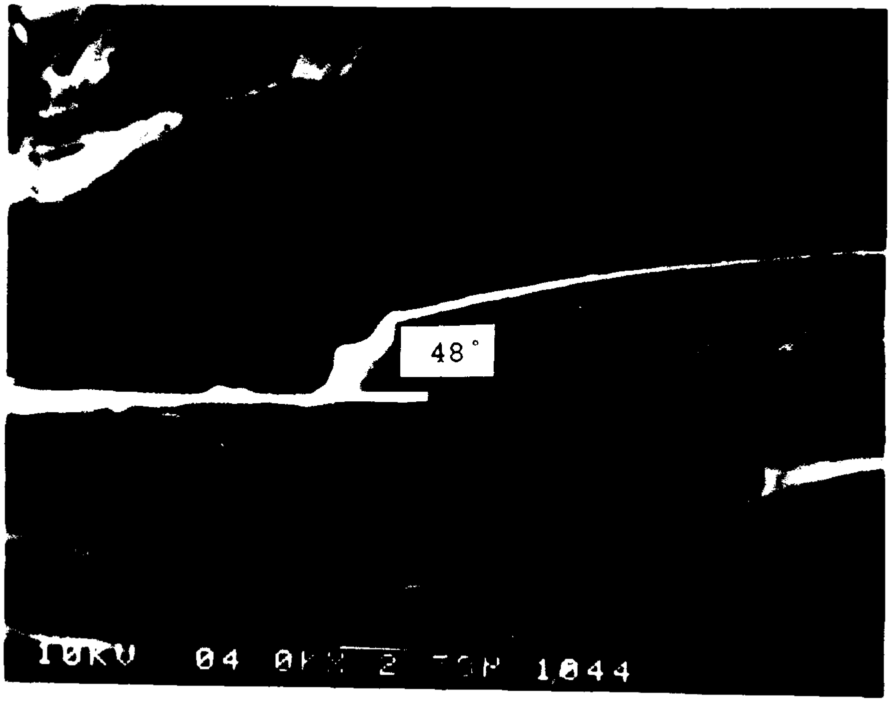


Figure 5.14. Cross-sectional view of a via with a side wall slope equal to 48° formed in the Selectilux HTR3-200 polyimide printed using a 20 μm proximity gap.

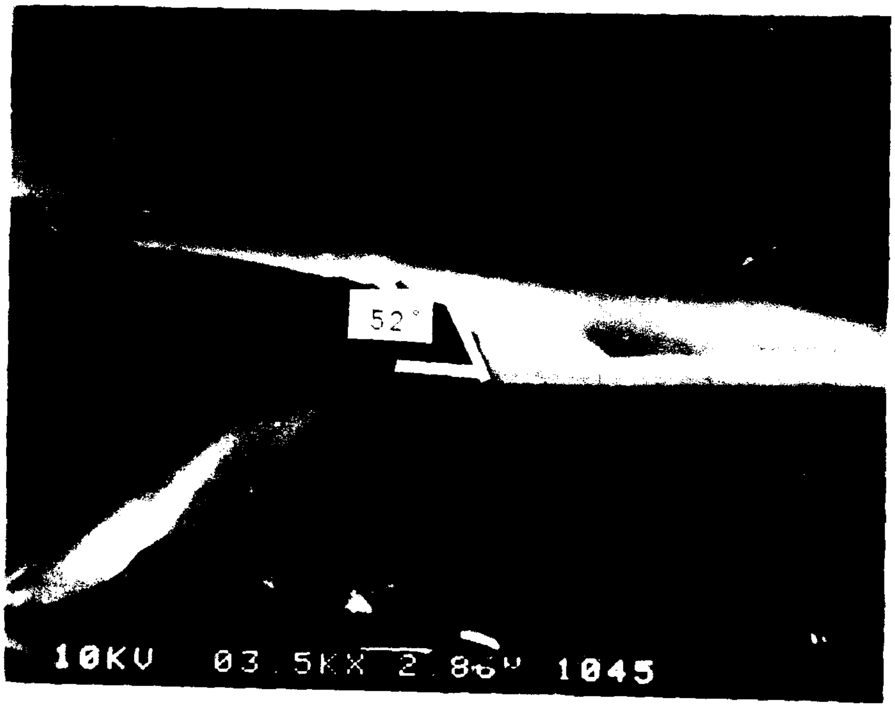


Figure 5.15. Cross-sectional view of a via with a side wall slope equal to 52° formed in the Selectilux HTR3-200 polyimide printed using a 50 μm proximity gap.

Table 5.2. Polyimide Sample Characteristics.

Sample	Polyimide Thickness (μm)	Via Feature Dimensions (μm)	Slope (°)	Good Interconnects
Ultradel 4212 Softbake: 100°C	10.5	Top: 150 Base: 100	85	4 of 25
Ultradel 4212 Softbake: 120°C	13.3	Top: 190 Base: 120	63	3 of 25
Ultradel 4212 Softbake: 140°C	12.9	Top: 200 Base: 120	48	21 of 25
Selectilux Proximity gap: 20 μm	9.4	Top: 250 Base: 90	48	25 of 25
Selectilux Proximity gap: 50 μm	10.1	Top: 275 Base: 90	52	25 of 25
Ultradel 7501 Proximity gap: 0 μm	9.8	Top: 120 Base: 85	90	0 of 11
Ultradel 7501 Proximity gap: 20 μm	9.7	Top: 160 Base: 70	62	1 of 11
Ultradel 7501 Proximity gap: 50 μm	9.5	Top: 175 Base: 80	90	1 of 11

illustrate, the cross-sectional view of these polyimide vias exhibit two regions with different slopes. The slope reported in Table 5.2 is the steeper slope as measured near the host wafer's surface. Contact printing with this polyimide proved unsuccessful in this study. Each sample produced in this study using contact printing exhibited a significantly deformed surface at the conclusion of the high temperature cure cycle. Figure 5.16 illustrates the resulting polyimide coating. This deformed surface was initially attributed to contact pressure being applied to the polyimide during the photolithographic exposure step. However, a subsequent experiment was conducted in which two wafers were coated with the polyimide and softbaked using using identical processes. One wafer was subjected to a photolithographic exposure with no contact pressure for a period of 2.5 minutes (a period of 1.5 minutes was used to prepare the previous test samples). The other wafer was not exposed. The two wafers were then subjected to the high temperature cure cycle. The exposed wafer exhibited a deformed topology similar to the test sample produced using contact printing. The unexposed wafer exhibited a smooth surface. These results indicate that the surface deformations observed on the contact print test sample were the result of overexposure of the polyimide during the photolithographic process.

Proximity printing did not produce the desired results with the Ultradel 7501 photosensitive polyimides. As Figure 5.17 illustrates, contact printing produced smooth, nearly vertical via side walls. The via walls produced using proximity printing with gaps of 20 and 50 microns exhibited severe undercutting, as shown in Figures 5.18 and 5.19. This

Figure 5.16. Selectilux HTR3-200 polyimide coating after a long duration (2.5 minutes) photolithographic exposure and 250°C, 4 hour cure.

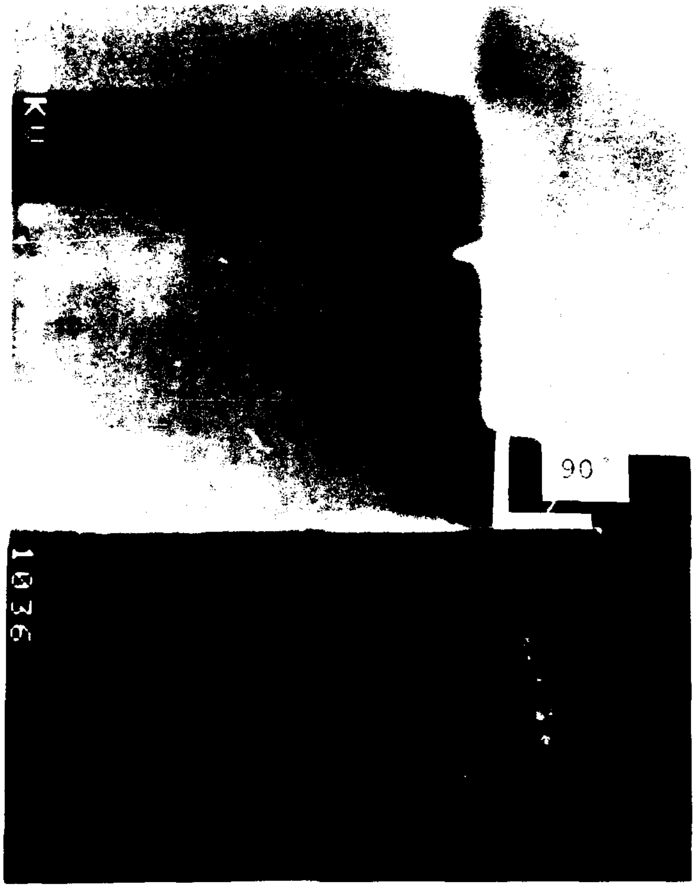


Figure 5.17. Cross-sectional view of a via with a side wall slope equal to 90° formed in the Ultradel 7501 polyimide using contact printing.

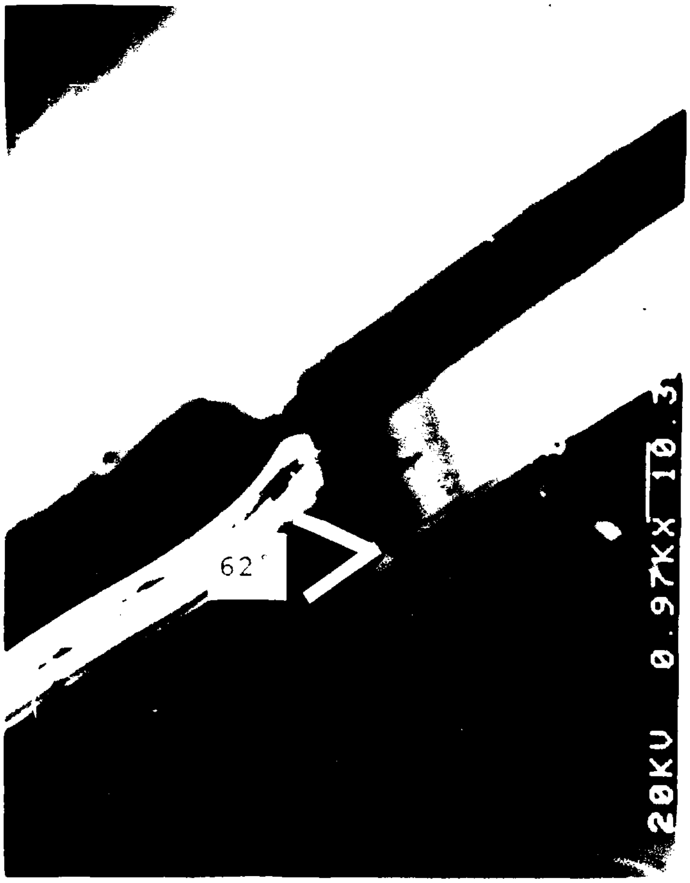


Figure 5.18. Cross-sectional view of a via with a side wall slope equal to 62° formed in the Ultradel 7501 polyimide printed using a 20 μm proximity gap.

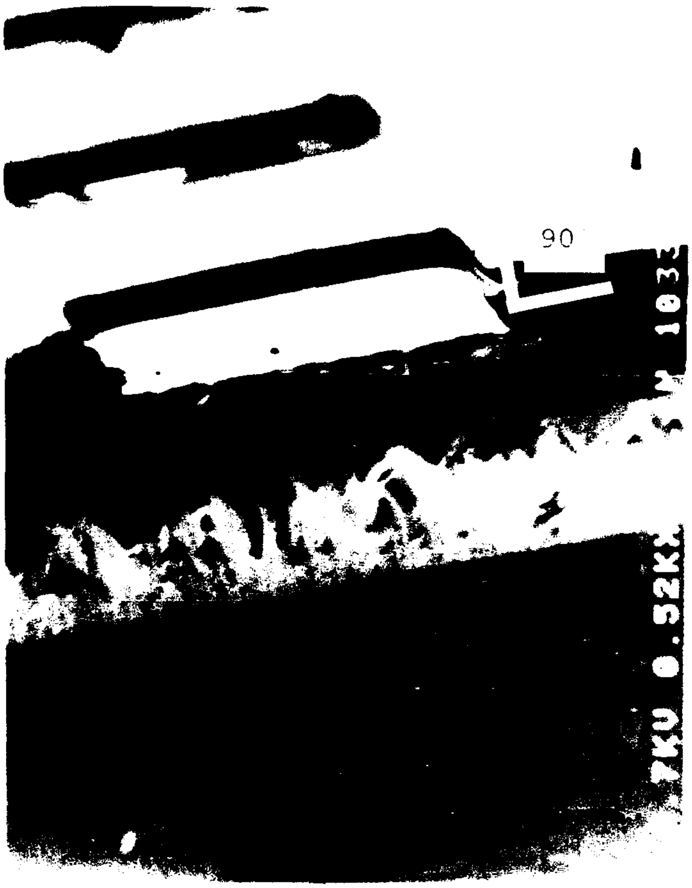


Figure 5.19. Cross-sectional view of a via with a side wall slope equal to 90° formed in the Ultradel 7501 polyimide printed using a 50 μm proximity gap.

undercut region is more difficult to cover using aluminum evaporation compared to a vertical via side wall. The manufacturer recommends a modified projection printing method or dry plasma etching process to produce smooth, sloped via walls in this polyimide (27). Neither of these processes were available for this project.

Top views of vias formed in the three polyimides are illustrated in Figures 5.20, 5.21 and 5.22. As Figure 5.20 illustrates, the area affected by the via formed in the Selectilux HTR3-200 is the largest of the three materials. The vias formed in the two Ultradel polyimides are much more compact, allowing for closer via spacing. The via area dimensions for the three candidates are summarized in Table 5.2.

Aluminum was evaporated and patterned on the polyimide samples. After the aluminum thin film was patterned on the polyimide's surface, stylus profilometer measurements were used to determine the interconnect thickness. The average measured interconnect thickness was 1.0 micron. Minimum and maximum interconnect thicknesses were 0.8 and 1.2 microns, respectively. Figure 5.23 illustrates the two-level metal pattern produced using the Selectilux polyimide. The purpose of these samples was to demonstrate the ability to achieve electrical continuity with the aluminum interconnects as they traversed the length of the via.

Figure 5.20. Top view of vias formed in the Selectilux HTR3-200 polyimide printed using a 20 μm proximity gap.

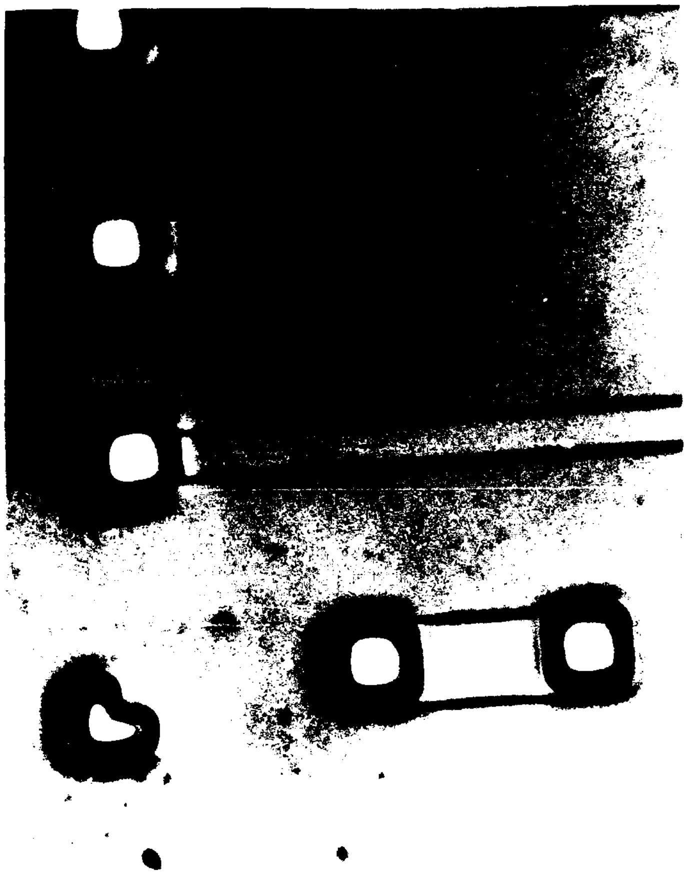


Figure 5.21. Top view of vias formed in the Ultradel 7501 polyimide printed using a 20 μm proximity gap.

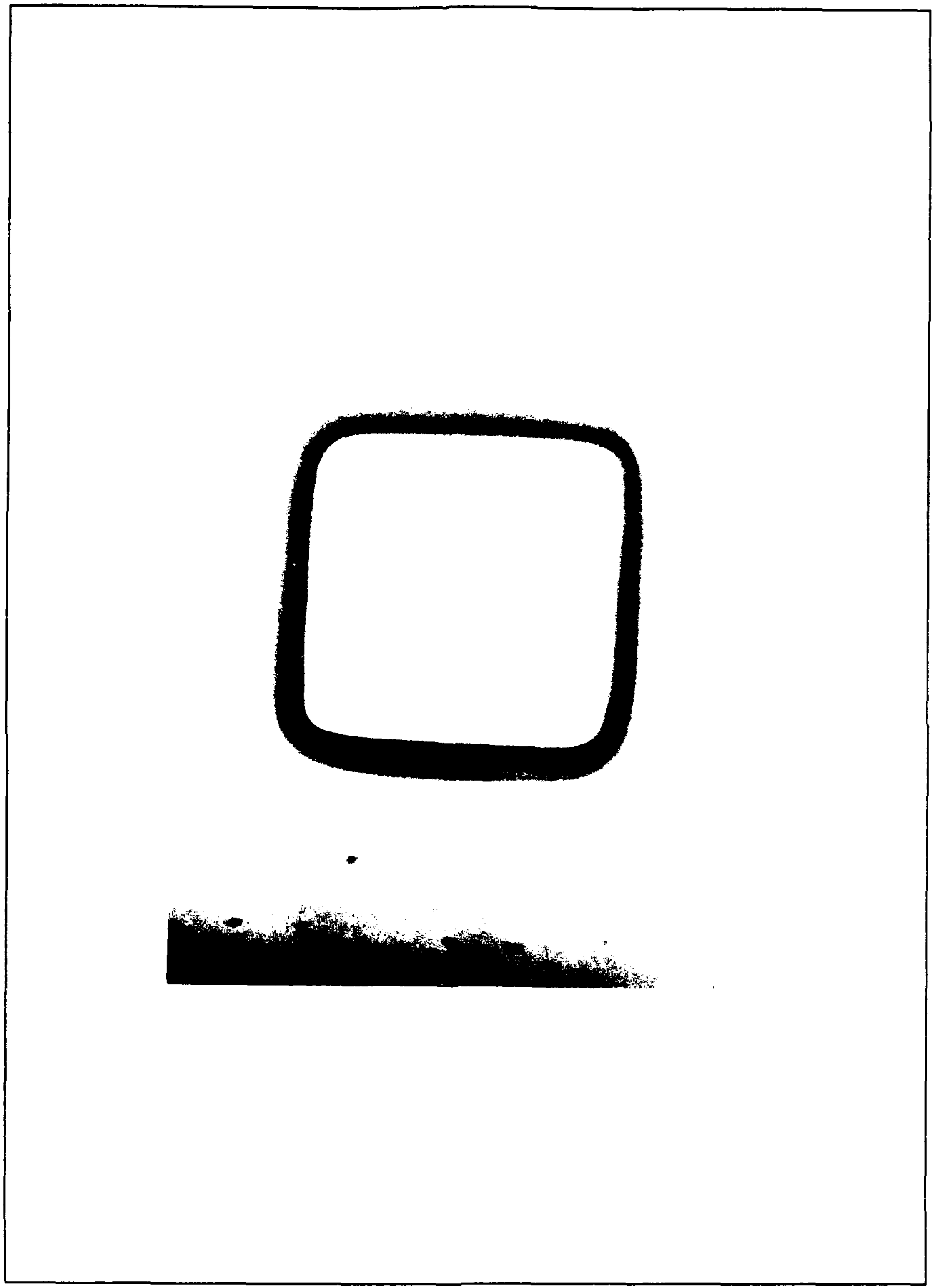


Figure 5.22. Top view of a via formed in the Ultradel 4212 polyimide using a 140°C softbake process.

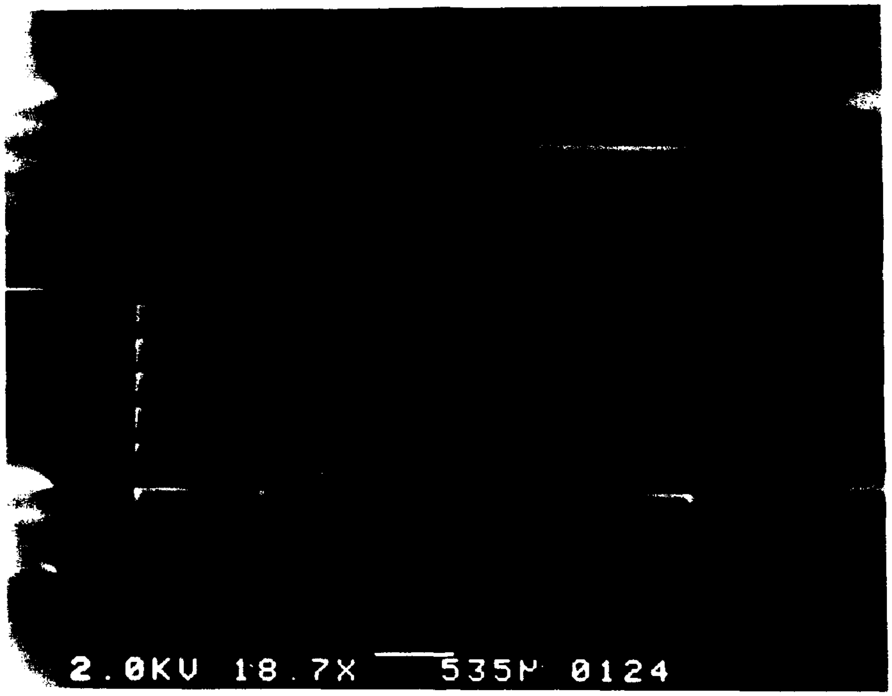
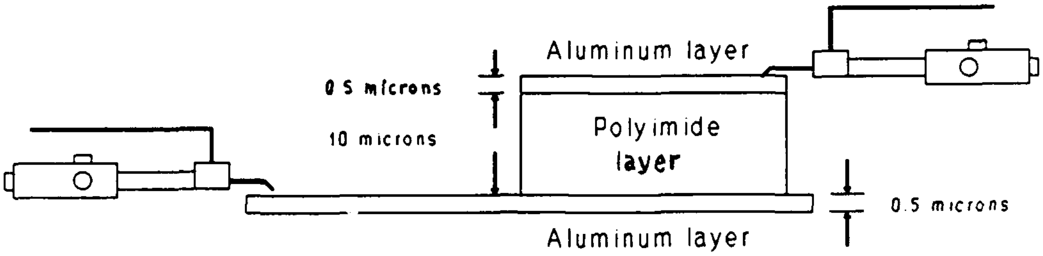


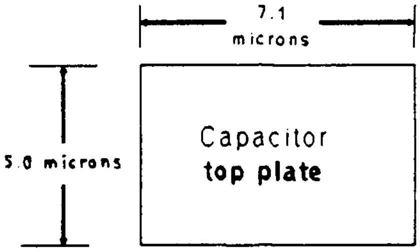
Figure 5.23. SEM micro-photograph (18.7X magnification) of the two-level metallization pattern using the Selectilux polyimide.

Measurement of the electrical continuity in these interconnects was performed using a Micromanipulator probe station (model number 6200). One probe was applied to the metal in the via, the other probe was applied to the interconnect on the polyimide's surface near the via. The probes were electrically connected to a Fluke ohmmeter (model number 72/AN). Table 5.2 presents the results of the electrical continuity testing.

The next samples tested to evaluate the polyimides were the parallel plate capacitors. Figure 5.24 illustrates the design of these capacitors. A fabricated capacitor is shown in Figure 5.25. Three capacitors were fabricated on two silicon wafers for each polyimide. One wafer was processed using the manufacturer's cure schedule, and the other wafer was processed using the standard cure schedule illustrated in Figure 4.4. The relative dielectric constant was calculated using Equation 4.1. The measured capacitor parameters included: dielectric thickness, capacitor plate area, and the capacitance as a function of frequency (1 kHz to 10 MHz). The dielectric thickness and parallel plate area dimensions were measured using the stylus profilometer. The capacitance was measured using a Hewlett Packard impedance analyzer (model number HP 4192). The impedance analyzer was also used to measure the series resistance of the capacitors over the frequency range (1 kHz to 10 MHz). The resistance and



(a) Side view



(b) Top view

Figure 5.24. Parallel plate capacitor design.

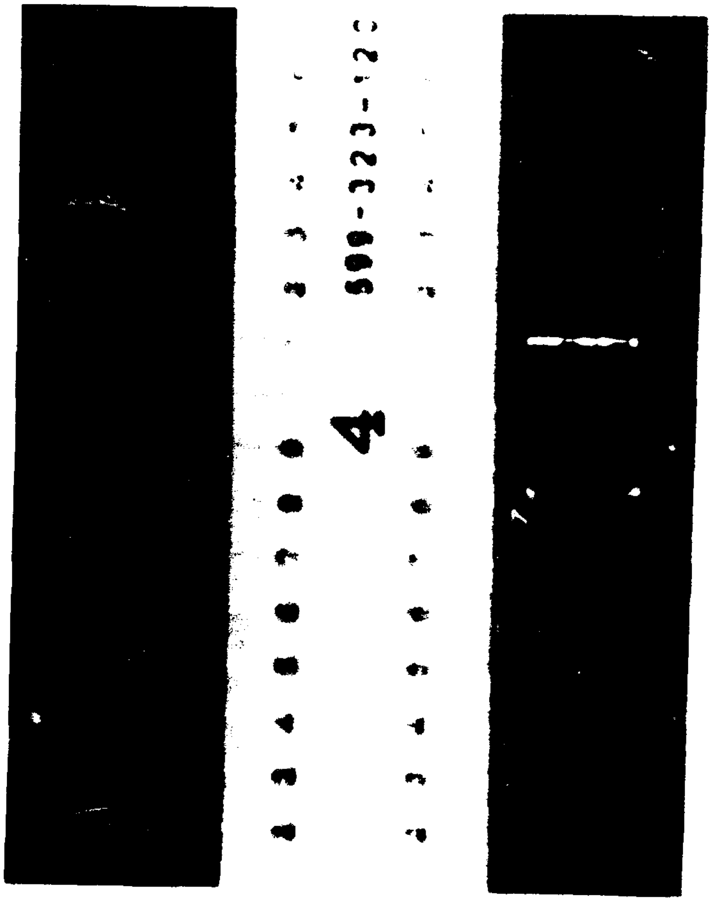


Figure 5.25. Parallel plate capacitor fabricated using the Selectilux HTR3-200 polyimide.

capacitance measurements were used with Equation 4.2 to calculate the dissipation factors of the polyimides.

Table 5.3 summarizes the relative dielectric constant and dissipation factor values calculated for each capacitor structure at 1 MHz. Table 5.3 also presents the manufacturers' published values of these parameters for

Table 5.3. Results of the Polyimide Capacitor Tests Measured at 1 MHz.

Sample	Measured Relative Dielectric Constant	Reported Relative Dielectric Constant	Measured Dissipation Factor	Reported Dissipation Factor
Ultradel 4212 Standard Cure	3.12	2.9	.009	.005
Ultradel 4212 Recommended Cure	3.44	2.9	.006	.005
Selectilux HTR3 Standard Cure	3.18	3.8	.003	.006
Selectilux HTR3 Recommended Cure	3.26	3.8	.019	.006
Ultradel 7501 Standard Cure	2.85	2.8	.010	.004
Ultradel 7501 Recommended Cure	3.57	2.8	.032	.004

Note: The Standard Cure schedule which was developed by Mainger (24), and the manufacturers' Recommended Cure schedules are illustrated in Figure 4.4 (14,42,43).

comparison. The relative dielectric constant variation versus frequency for the two Ultradel 4212 capacitor samples is presented in Figure 5.26. The dissipation factor versus frequency for the Ultradel 4212 samples is illustrated in Figure 5.27. The measured Selectilux HTR-300 relative dielectric constant and dissipation factor curves are illustrated in Figures 5.28 and 5.29, respectively. Figures 5.30 and 5.31 illustrate the relative dielectric and dissipation factor curves for the Ultradel 7501 polyimide samples.

The final polyimide test involved the Ultradel 4212 material. Because of the concern with the use of this material after a high temperature cure of only 250°C, another test was conducted. Two wafers coated with a layer of Ultradel 4212 were subjected to a different high temperature cure, and then coated with a second polyimide layer. The first wafer, cured using the standard cure schedule, exhibited cracks in the first layer after the second layer was applied. This wafer is illustrated in Figure 5.32. The resulting surface was also very rough. These defects have been attributed to reabsorption of the polyimide's solvent by the first layer. The second wafer, cured according to the manufacturer's recommendations, did not exhibit these defects. This result was attributed to the enhanced solvent resistance because of to the more complete imidization of the first-level polyimide material. From these results, it was

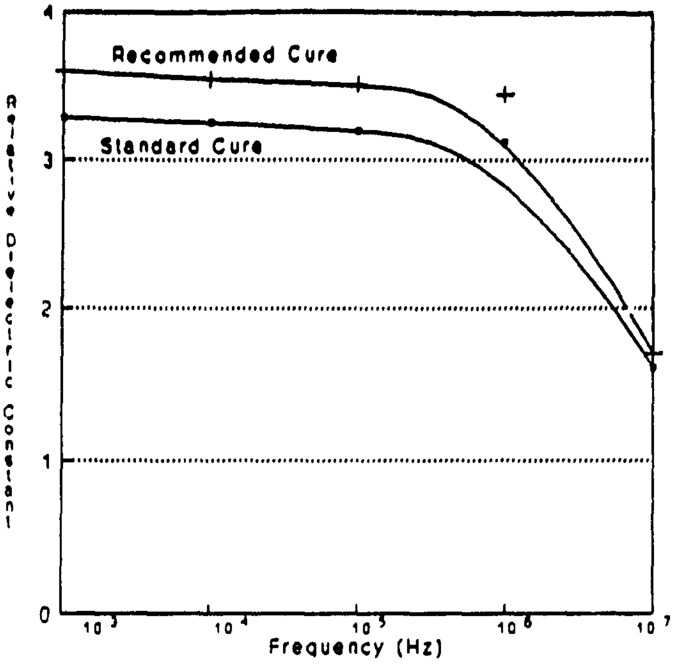


Figure 5.26. Relative dielectric constant as a function of frequency for the Ultradel 4212 polyimide.

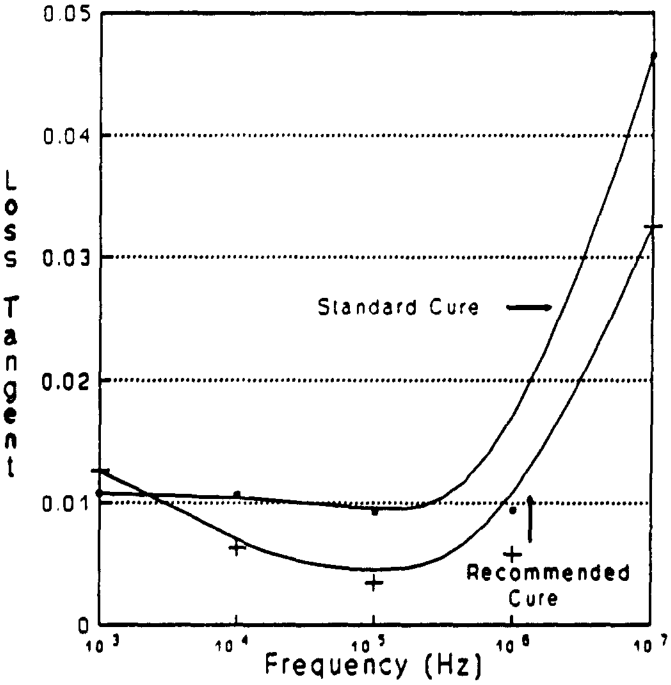


Figure 5.27. Dissipation factor as a function of frequency for the Ultradel 4212 polyimide.

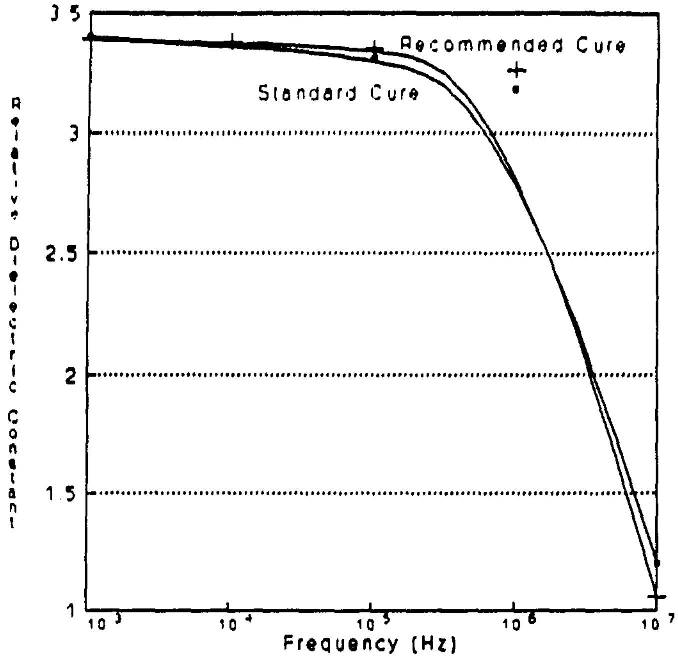


Figure 5.28. Relative dielectric constant as a function of frequency for the Selectilux HTR3-200 polyimide.

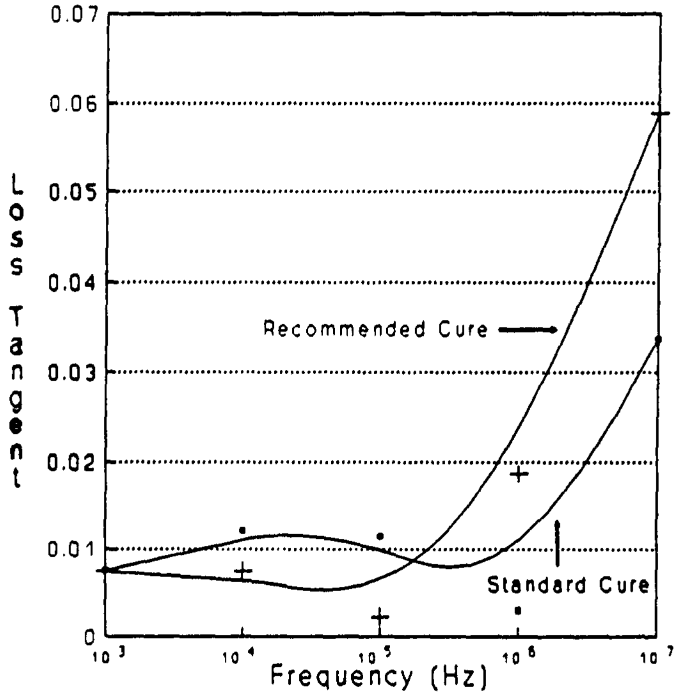


Figure 5.29. Dissipation factor as a function of frequency for the Selectilux HTR3 polyimide.

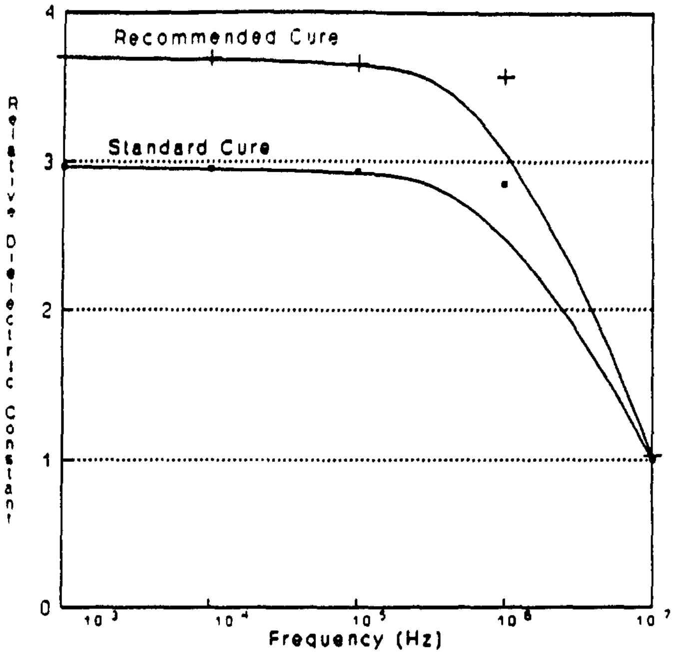


Figure 5.30. Relative dielectric constant as a function of frequency for the Ultradel 7501 polyimide.

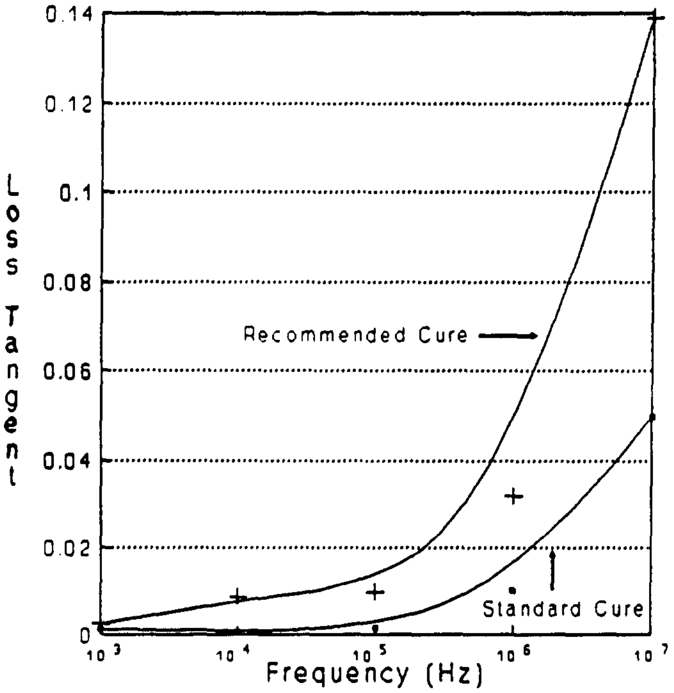


Figure 5.31. Dissipation factor as a function of frequency for the Ultradel 7501 polyimide.

Figure 5.32. Cracks in Ultradel 4212 polyimide layer.

concluded that WSI assemblies requiring multiple layers of the Ultradel 4212 polyimide must be cured according to the manufacturer's recommended schedule.

Summary of the Polyimide Evaluation Results. The primary objective of this evaluation was to determine which of the three candidate polyimides could be patterned to provide vias with geometries suitable for the evaporated metal interconnects. The results demonstrated that the Selectilux polyimide was superior with respect to this aspect. The success rate of interconnects patterned in the Selectilux material was significantly higher (electrical continuity on 100 percent of the interconnects on all samples) compared to the two Ultradel products. An additional advantage of the Selectilux polyimide relative to the Ultradel 4212 material was its photosensitivity, which required fewer patterning steps.

The non-photosensitive Ultradel 4212 polyimide demonstrated a promising degree of success relative to the interconnect electrical continuity tests (electrical continuity on 84 percent of the interconnects on the sample using the 140°C softbake). In addition, vias in the Ultradel 4212 polyimide affected a smaller peripheral surface area compared to those in the Selectilux polyimide. This feature should allow for closer spacing of the interconnects. However, because the Ultradel 4212 polyimide is not photosensitive, it requires several additional processing steps. In addition, the Ultradel 4212 polyimide did not achieve the interconnect electrical continuity success rate of the Selectilux polyimide. Another disadvantage of the Ultradel 4212 polyimide was the requirement to use cure temperatures in excess of the 250°C limit recommended in previous research for the IC die mount epoxy.

The Ultradel 7501 polyimide could not be patterned to produce functional vias, given the available patterning and metallization resources. Continuous metal interconnects could not be fabricated over the nearly vertical or slightly undercut via side walls. However, vias in this material did exhibit a compactness similar to that of the vias in the Ultradel 4212. In addition, the Ultradel 7501 polyimide is photosensitive.

Based upon these results, the Selectilux HTR3-200 and the Ultradel 4212 polyimides were selected for further study in the fabrication of the WSI test articles. For each of these configurations, as illustrated in Figure 1.1 (b), (c) and (d), one WSI circuit was fabricated with each polyimide.

Fabrication Procedure Results

IC Die Cavity Etch. The first step in producing the WSI test articles was the IC die cavity etching. The IC die cavity pattern illustrated in Figure 5.33 was etched into a 2 micron thick silicon dioxide layer which had been grown on

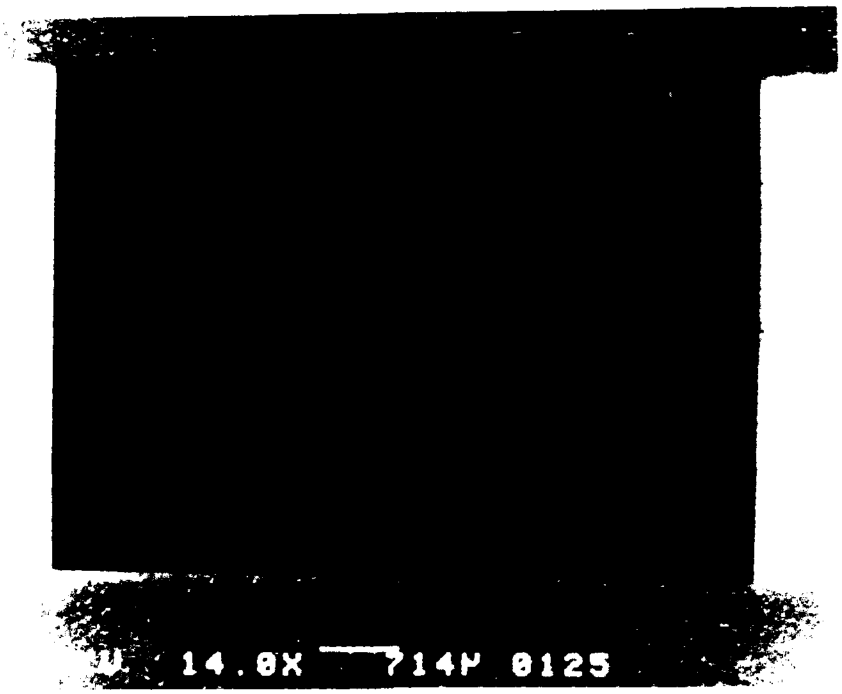


Figure 5.33. IC die cavity pattern etched in the 2 micron thick silicon dioxide layer (14.0X magnification).

the silicon wafer host substrate. The host substrate was then etched in a KOH solution. Periodic measurements of the wafer thickness confirmed an etch rate of 0.43 microns per minute in the [100] direction for the 20% wt KOH solution thermostatted at 70°C. Because the average wafer thickness was 510 microns, the total etch time at this rate was 19.8 hours.

Figure 5.34 shows the resulting IC die cavity. An approximate etch rate in the [111] direction was calculated based upon the difference between the dimensions of the

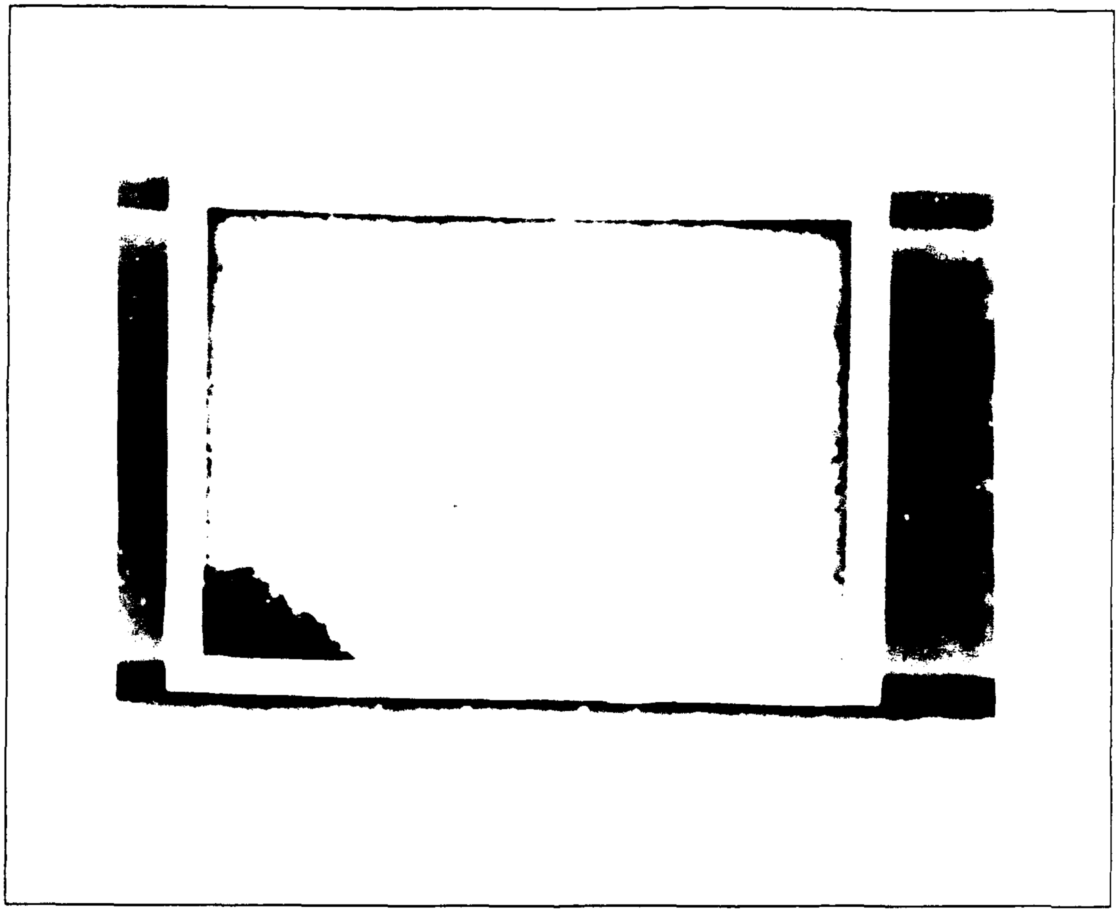


Figure 5.34. IC die cavity opening after the KOH etch (13.3X magnification).

larger opening of the cavity and the initial silicon dioxide window aperture. This etch rate is actually a combination of the silicon dioxide lateral etch rate and the silicon etch rate in the [111] direction. Based upon the measured dimensions, the silicon etch rate in the [111] direction was 0.11 microns per minute. The difference in the dimensions of the two cavity openings (top surface versus bottom surface) was used in conjunction with the wafer's thickness to calculate the slope of the cavity's side walls. The calculated slope was 56°. This slope was also measured directly from an IC die cavity's cross-section, as illustrated in Figure 5.35. This measurement revealed a slope of 57°.

IC Die Mounting. In the next WSI fabrication step, the IC die were mounted into their etched cavities. The IC die in Wafers A and B were mounted using the substrate pre-assembly procedure, and the IC die in the remaining wafers were mounted using the single-step procedure. After each wafer had been processed with the high temperature IC die epoxy cure scheme, measurements were taken with the stylus profilometer to determine the planarity between the IC die and the host substrate. In addition, the relative positions of the IC die with respect to the IC die located in the center of the pattern were measured to determine the alignment tolerances for the via and metal patterns. Figure 5.36 illustrates the locations of the IC die measurements. The planarization measurements are summarized in Table 5.4, and the alignment measurements are presented in Table 5.5.

As Table 5.4 illustrates, the IC die in Wafers A and B exhibited step heights spanning a larger range (-36.1 to 45.7 microns) compared to those measured on the remaining wafers (-2.5 to 33.6 microns). This result implies that the substrate pre-assembly procedure produced less consistent results. The IC die in wafer B protruded from the surface because the hardened epoxy residue in the cavity from the substrate bonding process prevented the complete insertion of

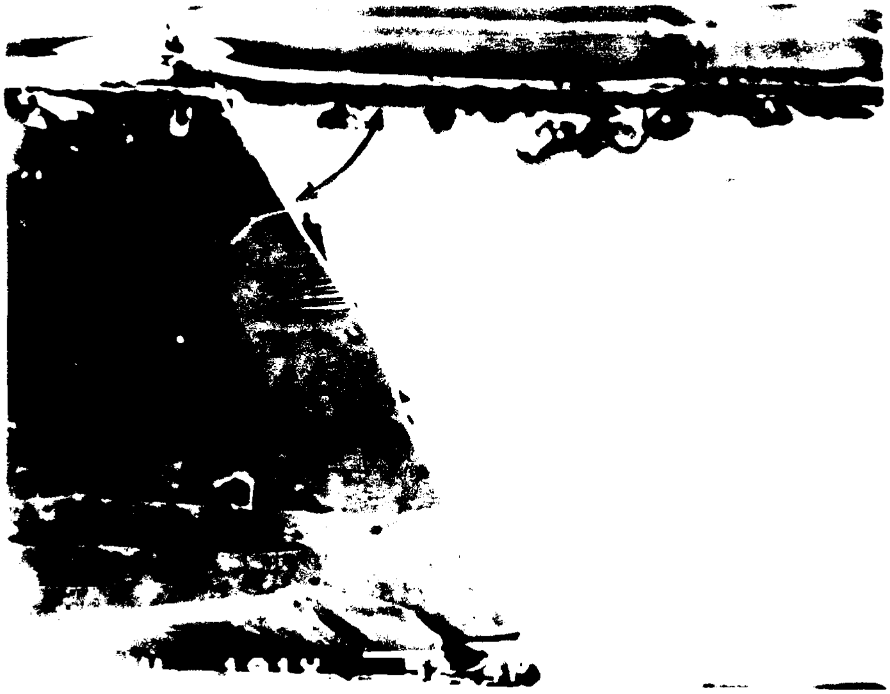


Figure 5.35. Cross-sectional view of the IC die cavity side wall (191X magnification).

the IC die. The single-step procedure produced more repeatable and acceptable results. Given the maximum acceptable step height specification of ±20 microns, 12.5 percent of the measurements from wafers A and B were acceptable, as opposed to 66.7 percent for the remaining wafers (39).

Table 5.5 presents the relative IC die alignment data for those host substrates with multiple IC die. As the results indicate, the relative misalignment of the IC die in these samples was small (10 to 200 microns). Because of this

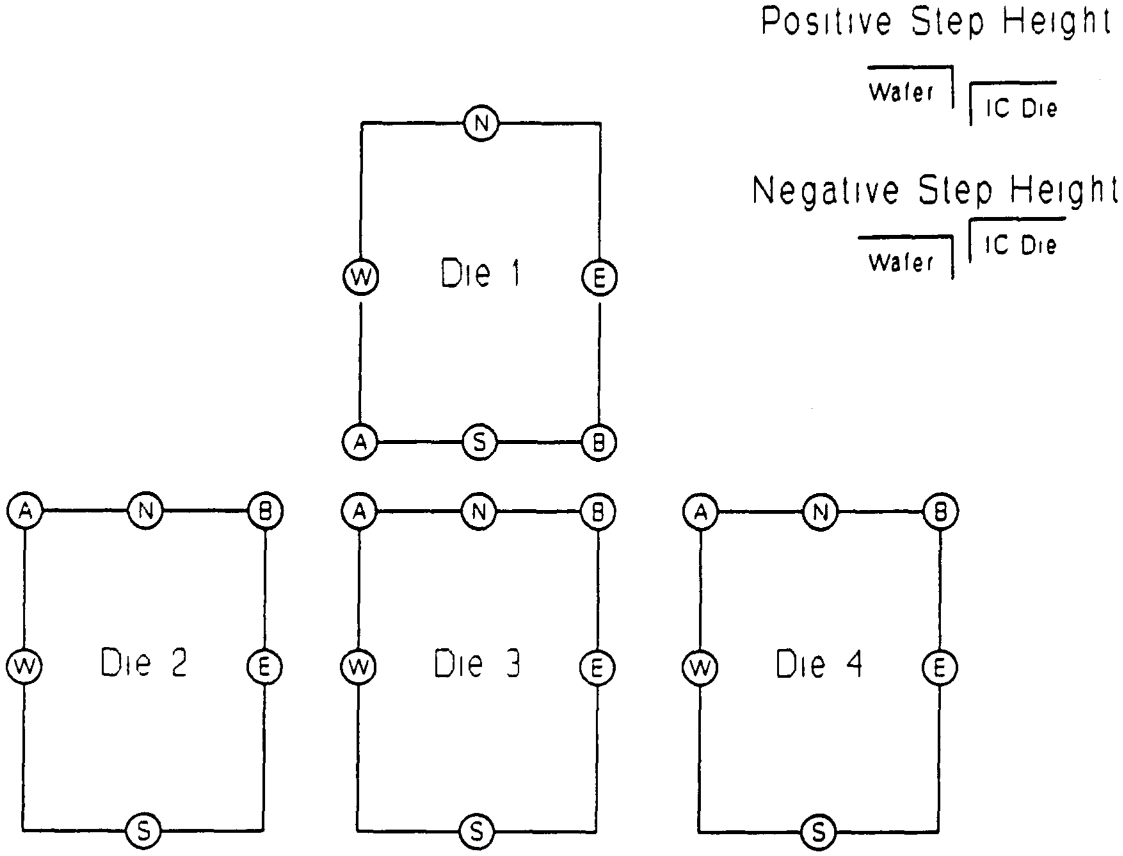


Figure 5.36. IC die planarization and alignment measurement locations.

Table 5.4. IC Die Planarization Results.

Wafer Number	IC Die Number	Step Height (μm)			
		N	S	E	W
1	1	23.8	32.6	32.0	24.7
1	2	33.6	30.6	33.0	32.0
1	3	25.6	30.0	31.8	23.7
1	4	32.8	15.6	24.4	24.8
2	1	14.1	8.3	15.3	7.5
2	2	10.8	7.9	8.4	9.8
2	3	7.0	10.2	12.6	3.5
2	4	-2.5	13.2	7.6	1.3
3	1	29.8	18.4	25.5	18.4
3	2	13.1	19.4	14.6	17.7
3	3	24.2	21.5	28.0	19.2
3	4	28.9	23.6	24.2	21.5
4	1	10.5	17.6	16.3	11.0
4	2	-1.7	19.0	5.6	11.7
4	3	10.4	18.7	17.1	12.8
4	4	18.0	7.5	9.4	17.6
A	1	45.7	-8.1	25.0	24.8
B	1	-21.7	-22.4	-24.9	-36.1
C	1	19.0	4.6	13.6	10.6
D	1	14.5	14.0	11.6	18.6

Table 5.5. IC Die Alignment Results.

Wafer Number	IC Die Number	Point A Error (μm)		Point B Error (μm)	
		x	y	x	y
1	1	25	40	50	70
1	2	80	100	70	80
1	3	0	0	0	0
1	4	110	100	100	115
2	1	40	35	40	125
2	2	150	70	170	40
2	3	0	0	0	0
2	4	70	50	70	50
3	1	10	130	20	80
3	2	90	140	100	30
3	3	0	0	0	0
3	4	125	10	120	25
4	1	40	100	90	50
4	2	130	90	130	30
4	3	0	0	0	0
4	4	150	40	140	200

small variance, it was determined that a standard set of via and metal mask patterns could be used for the given metal bond pad size and pitch. Larger deviations, on the order of ±300 microns would have required sample rejection or fabrication of unique masks for each wafer.

Interconnect Fabrication. Each WSI assembly was completed using a series of dielectric and metallization application and patterning steps. Each configuration required a different series of steps and mask patterns to realize the complete circuit. While performing these steps, measurements were taken to evaluate the success and possible failure mechanisms of the process.

Polyimide Patterning. In each layer of the applied polyimide dielectric, vias were etched to provide connection points for the patterned interconnect metal lines. After each polyimide coating was applied and patterned, measurements were made with the stylus profilometer to determine the completeness of the etch and the thickness of the coating. Visual inspections through an optical microscope were also performed to determine if the via defects were the result of defects in the polyimide coating. The polyimide patterning results are presented in Table 5.6.

As the results in Table 5.6 demonstrate, the percentage of good vias produced in the Selectilux polyimide was greater than those realized in the Ultradel 4212 polyimide. The majority of the defects in the Selectilux polyimide coatings

Table 5.6. Via Patterning Results.

Wafer Identification	Polyimide Thickness (μm)	Number of Vias	Via Defects		Good Vias
			Type I	Type II	
1	Unknown	38	8	30	0
2	10.9	38	1	0	37
3	9.8	51	14	5	32
A (level 1)	11.1	38	0	0	38
A (level 2)	6.0	42	3	2	37
B (level 1)	8.8	38	8	0	30
C (level 1)	12.0	38	5	13	20
C (level 2)	8.0	42	16	3	23
D (level 1)	8.5	38	0	11	27
D (level 2)	5.0	42	24	8	10

NOTE: Type I defects are those caused by defects in the polyimide coating; Type II defects resulted from insufficient via etching. Good vias were completely etched and free of defects.

were caused by defects in the coatings. The primary cause of these defects was trapped gas beneath the polyimide in the IC die-to-host substrate transition regions. When the polyimide coatings were baked, this trapped gas expanded, migrated through the polyimide and fractured the polyimide coating around the perimeter of the IC die. A smaller number of defects resulted from insufficient (non-uniform) polyimide coating; this defect can be attributed to a large step height between the IC die and host substrate. Figure 5.37 shows a successful via on an IC die pad. An example of a polyimide layer defect is illustrated in Figure 5.38.

The poor performance of the Ultradel 4212 polyimide was attributed to the fact that the polyimide material had exceeded its limited shelf life of approximately 6 months when stored at 0°C (31). Because the material was not frozen, a limited degree of imidization occurred in the polyimide during storage. Over the life of this project (9 months) this material had imidized to the point where it could no longer be etched unless the softbake temperature was reduced to 90°C. However, samples produced at this temperature did not exhibit the proper side wall geometry to support the metal patterns. In addition, the partial imidization of the material led to surface cracking during processing, which resulted in a rough polyimide topology.

Metallization Patterning. Aluminum layers approximately 1.2 microns thick were evaporated onto the WSI assemblies and patterned. The resulting metal interconnects were tested for electrical continuity at each via transition and at each point where the IC die-to-host substrate transition region was crossed. Each interconnect was also tested for overall electrical continuity between its end points. The electrical continuity results at the via

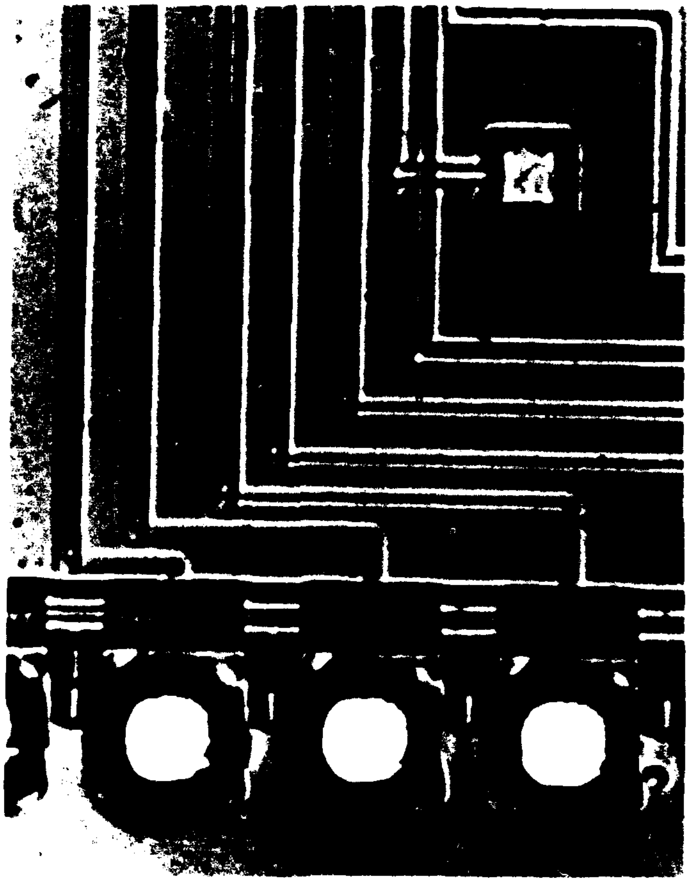


Figure 5.37. Via patterned in the Selectilux polyimide (90X magnification).

Figure 5.38. Typical defect in the Selectilux polyimide layer (90X magnification).

locations are presented in Tables 5.7 and 5.8. End-to-end interconnect electrical continuity is presented in Table 5.9.

Table 5.7. Electrical Continuity Results for Multiple IC Die Samples.

Wafer	Number of Vias	Discontinuities			Number of Transitions	Discontinuities		
		Type I	Type II	None		Type I	Type II	None
1	32	16	5	11	31	25	4	2
2	32	17	3	12	31	25	4	2
3	43	43	0	0	30	30	0	0

NOTE: Type I defects resulted from insufficient metal adhesion and polyimide defects; Type II defects resulted from interconnect discontinuity.

Table 5.8. Electrical Continuity Results for Single IC Die Samples.

Wafer	Number of Vias	Discontinuities		
		Type I	Type II	None
A level 1	33	0	5	28
A level 2	8	2	2	4
B level 1	33	8	11	14
C level 1	33	28	0	5
C level 2	8	7	0	1
D level 1	33	29	0	4
D level 2	8	8	0	0

NOTE: Type I defects resulted from insufficient metal adhesion and polyimide defects; Type II defects resulted from interconnect discontinuity.

Table 5.9. Interconnect Electrical Continuity Results.

Wafer	Number of Inter-connects	Discontinuities		
		Type I	Type II	None
1	17	17	0	0
2	17	16	1	0
3	20	20	0	0
A level 1	12	0	1	11
A level 2	4	2	2	1
B level 1	12	3	3	6
C level 1	12	12	0	0
C level 2	4	4	0	0
D level 1	12	12	0	0
D level 2	4	4	0	0

NOTE: Type I defects resulted from insufficient metal adhesion; Type II defects resulted from interconnect discontinuity.

The test articles fabricated with the Ultradel 4212 polyimide performed poorly with respect to the interconnect electrical continuity performance evaluation. Wafers C, D, and 2, which were coated with the Ultradel polyimide, exhibited a rough surface topology because of cracking. Consequently, the aluminum's adherence was compromised by this rough topology. Also, a large number of the vias were not properly formed during the polyimide's patterning. However, all of the interconnects at properly etched vias where the metal was adequately adhered, did demonstrate electrical continuity, indicating some degree of success with this material and the WSI fabrication technique.

The single IC die test articles fabricated using the Selectilux polyimide were more successful. For the level-one metal on sample A, 92 percent of the interconnects demonstrated end-to-end electrical continuity. The poorer performance of the interconnects on the level-two metal appeared to be the result of poor metal adherence. On sample B, one possible reason for the reduced success rate, 50 percent end-to-end electrical continuity, was thinning of the photoresist used to pattern this metal. This thinning appeared to be the result of the uneven topology over which the photoresist was applied. As the data in Table 5.4 indicates, the IC die surface on sample B was significantly higher (20 to 36 microns) compared to the host substrate surface.

The results associated with the four IC die WSI sample configuration were poor. As Table 5.8 illustrates, the majority of the continuity failures were attributed to a combination of metal adhesion failures and polyimide defects. These defects affected the via formations and the paths over which the interconnects were routed. This rough surface topology limited the metal step height coverage and the coverage of the photoresist used to mask the metal for etching.

Topology also contributed to a majority of the continuity failures observed across the IC die-to-host substrate transitions. Stylus profilometer measurements indicated that void regions existed in the gap region surrounding the IC die. A profile measurement across an IC die-to-host transition region depicting a gap region is presented in Figure 5.39. In most cases, the epoxy and the polyimide coatings failed to fill or bridge these gaps. The resulting step heights were generally too large or steep, creating discontinuities in the interconnects.

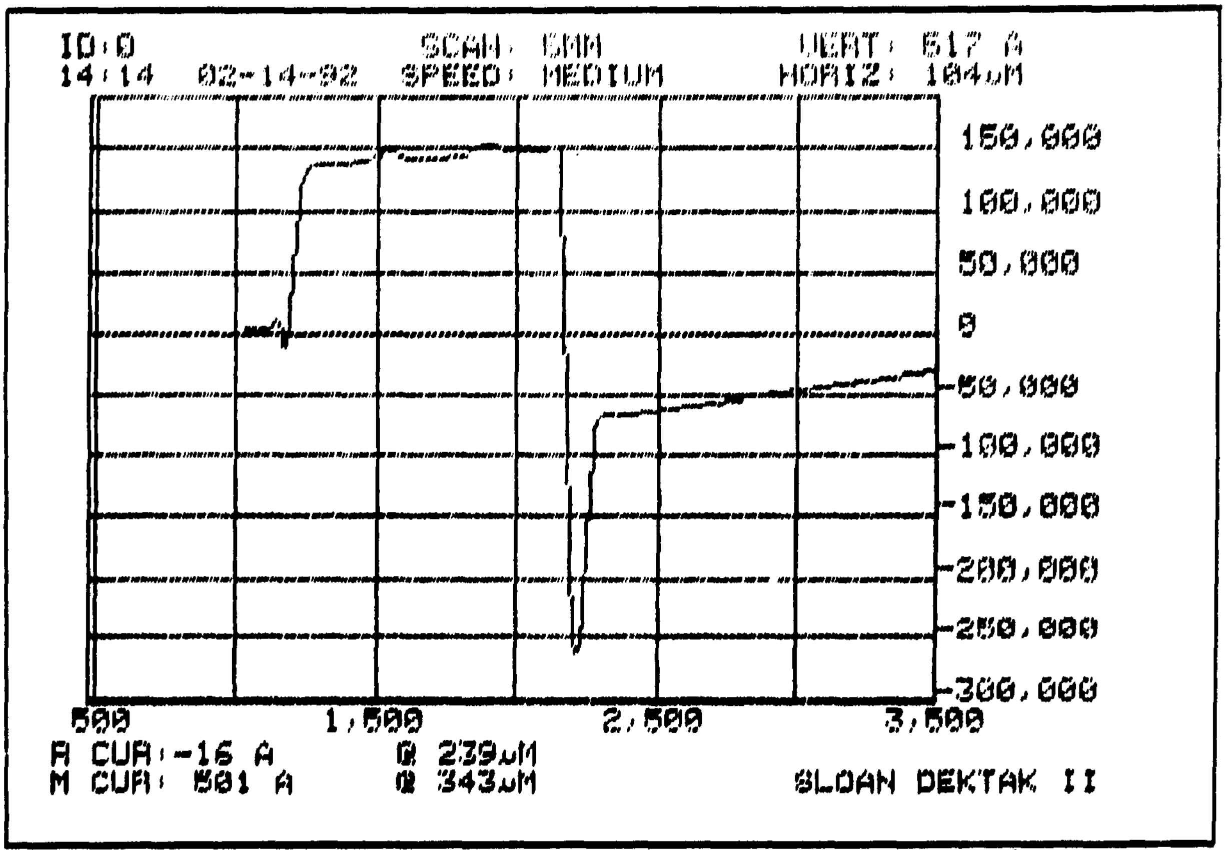


Figure 5.39. Surface profile across the IC die-to-host substrate depicting the existence of a gap region.

Summary of the Fabrication Results. The first step of the process, IC die cavity etching, produced repeatable and acceptable results. The single-step IC die mounting approach also produced repeatable results with acceptable step heights between the surfaces of the IC die and host substrate. However, this method failed to provide a smooth, void-free transition region between the two surfaces. Because these voids were not filled by the epoxy or the polyimide coatings, defects were created in the polyimide coatings, and discontinuities were present in the majority of the interconnects crossing these regions. The Ultradel 4212 polyimide could not be adequately evaluated in this study because the material had exceeded its expected shelf life (6 months), and it began to exhibit inconsistent properties. The Selectilux polyimide samples produced successful interconnects in the single IC die configurations.

Figure 5.40 illustrates the fabricated single IC die WSI configuration. An example of the four IC die patterned overlay WSI configuration is presented in Figure 5.41. Figure 5.42 illustrates the substrate metal patterned on the silicon wafer. A complete patterned substrate test article is shown in Figure 5.43.

Alternative IC Die Mount Adhesive Evaluation. An evaluation of alternative IC die adhesive materials was motivated, based upon the WSI system fabrication results. Alternative IC die adhesives must exhibit qualities similar

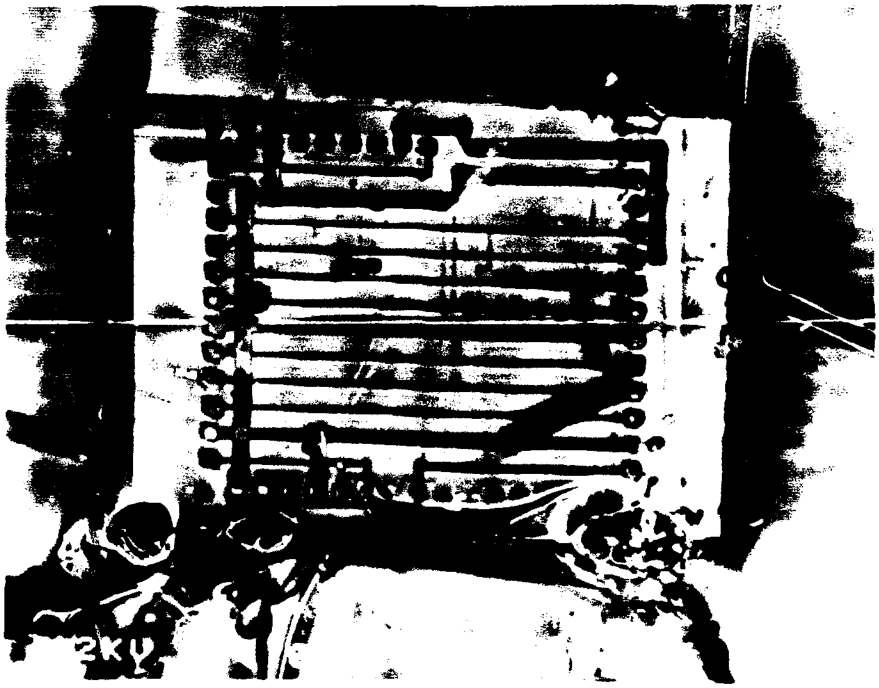


Figure 5.40. Single IC die WSI configuration fabricated with the Selectilux polyimide (14.0X magnification).

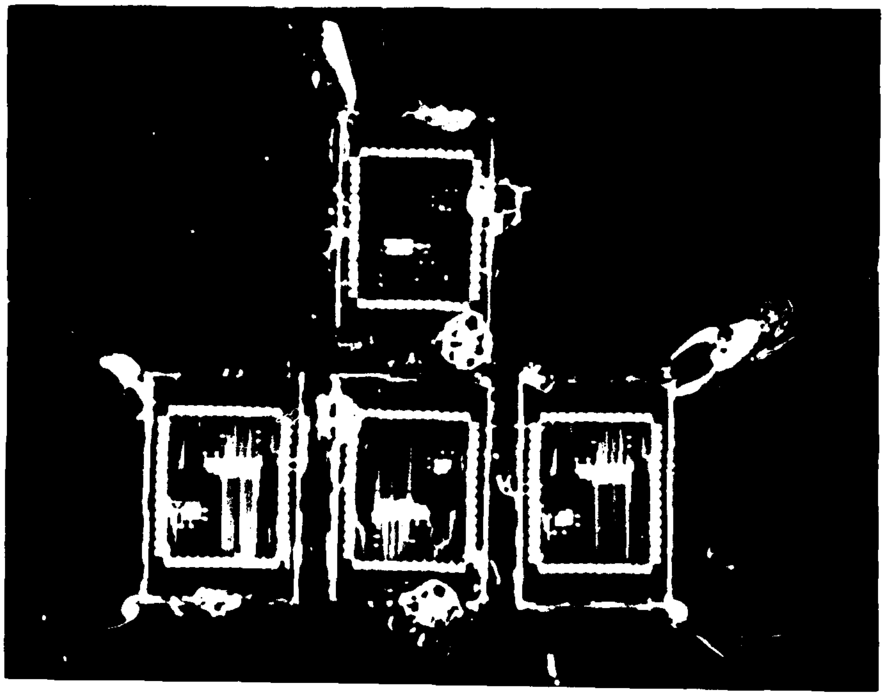


Figure 5.41. Four IC die patterned overlay WSI configuration fabricated with the Selectilux polyimide (4.3X magnification).

Figure 5.42. Substrate interconnect scheme patterned on the silicon host substrate (90X magnification).

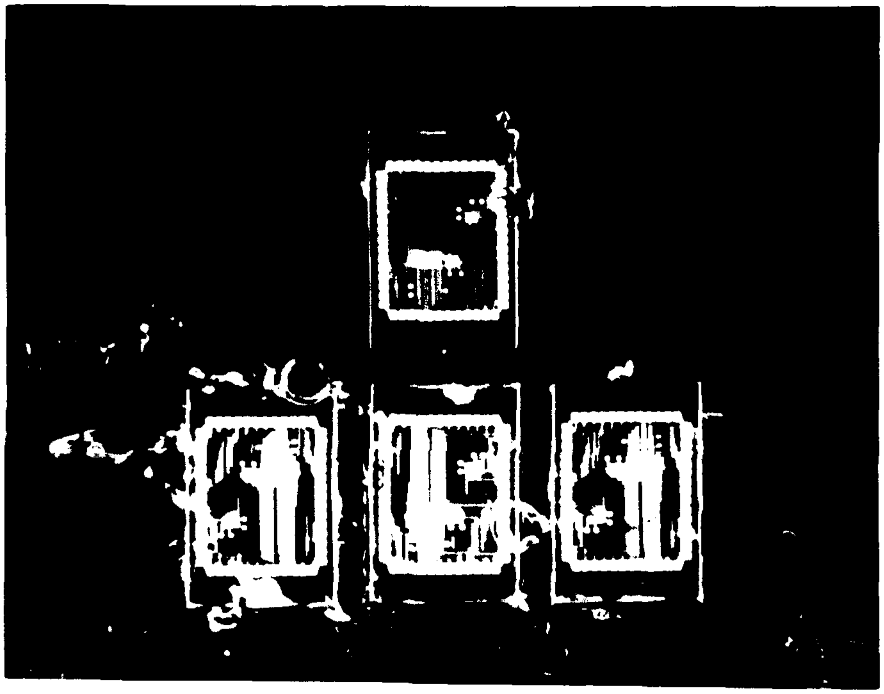


Figure 5.43. Four IC die WSI configuration fabricated with the Selectilux polyimide (4.3X magnification).

to the Master Bond EP34CA epoxy with respect to the coefficient of thermal expansion, cure heat resistance (250°C minimum), and low levels of voiding. In addition, the alternative adhesive must exhibit a higher, more consistent viscosity compared to the Master Bond epoxy throughout its cure cycle to retard flowing onto the IC die's surface. One candidate material which was available for evaluation was A. I. Technology EG7659 flexible paste epoxy. This adhesive is a two component epoxy purported to be highly thermally conductive and electrically insulating.

A test was conducted to provide a preliminary evaluation of this epoxy's applicability as the WSI IC die mount adhesive. For this evaluation, two single IC die WSI structures were assembled using the single-step IC die mounting procedure presented in Appendix N. The alternative epoxy required a temperature of 85°C for the initial cure on the hot plate. Once these two WSI assemblies had completed the epoxy 250°C high temperature cure process, they were coated with the Selectilux polyimide and softbaked. The polyimide was exposed and hardbaked on the substrate surfaces. However, the resulting polyimide coatings were rough due to overexposure. Aluminum was evaporated on the polyimide surface to a thickness of approximately 0.5 microns. Equipment malfunction prevented the deposition of 1.2 microns (the desired aluminum thickness). The aluminum was patterned using the four IC die metallization mask illustrated in

Figure 4.15. However, only three interconnects adhered to both sides of the transition region because of the rough polyimide topology on the first WSI assembly. None of the interconnects adhered to the other WSI assembly. Of the three testable interconnects, two were found to have electrical continuity across the transition region.

This epoxy demonstrated superior viscosity and transition region filling compared to the Master Bond epoxy. As a result of its consistent viscosity, the alternative epoxy flowed out of the transition region no more than 200 microns to either side. The resulting transition region profile is illustrated in Figure 5.44. Acetone cleaning was successful in removing the excess epoxy. However, this cleaning process was often over-aggressive, resulting in the formation of trenches in the transition region.

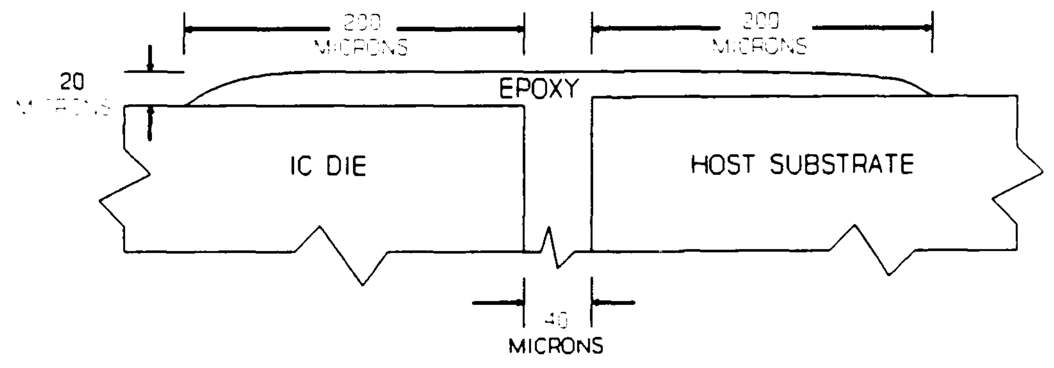


Figure 5.44. Cross-sectional view of the host substrate and the IC die mounted using the alternative epoxy.

Electrical Performance Evaluation Results

Electrical performance evaluation was accomplished on two of the test samples. The first sample was fabricated on a bare silicon wafer using the Selectilux polyimide as the interlevel dielectric, and the single IC die configuration masks were used to pattern the aluminum and polyimide layers. The second sample also used the same polyimide and mask set. However, this sample was fabricated on a substrate with an IC die mounted in it. Electrical testing included: continuity, direct current resistance, signal attenuation, propagation delay, and coupling measurements.

Electrical Continuity and Direct Current Resistance Measurements. The first electrical evaluation tests involved probing the interconnects at both ends to determine their electrical continuity and direct current resistance. The electrical continuity measurements provided a qualitative evaluation of the overall fabrication process. The direct current resistance measurements were used to identify irregularities in the interconnect geometries, such as necking or thinning. The electrical continuity results are presented in Table 5.9; the direct current resistance measurements are summarized in Table 5.10. In addition, Table 5.10 presents the calculated average resistivity of the interconnect metal. This material parameter was calculated using Equation 4.4, assuming no geometrical irregularities.

Table 5.10. Interconnect Electrical Resistivity Results.

Conductor	Thickness (μm)	Width (μm)	Length (μm)	Resistance (Ω)	Resistivity ($\Omega\cdot$cm)
1	1.2	30	4600	65.9	$5.2(10^{-5})$
2	1.2	100	5000	22.1	$5.3(10^{-5})$
3	1.2	150	4750	6.6	$2.5(10^{-5})$
4	1.2	150	3350	4.1	$2.2(10^{-5})$

As Table 5.10 shows, the calculated aluminum interconnect resistivity was larger than $2.7\cdot10^{-6}$ ohms·centimeters, the published resistivity of aluminum (34:19). This increase in electrical resistivity could be the result of material impurities and interconnect cross-section irregularities. Visual inspection of the interconnects did not reveal any interconnect necking, and the profilometer measurements along the interconnects did not indicate any significant thickness deviations. However, one region not evaluated by these measurements was the via side wall region. Given the orientation of the via side walls during metal evaporation, there is the possibility of thinning in this region.

Direct current resistance measurements were also accomplished on three second-level interconnects with the probes contacting the interconnect on the surface of the second-level polyimide rather than in the vias. These measurements and the calculated resistivities are presented in Table 5.11. As these results demonstrate, the calculated resistivities are in closer agreement (within an order of magnitude) with the published electrical resistivity value of aluminum (34:19). Another measurement was accomplished with one probe contacting a via metal pad while another probe was used to make contact with the interconnect at points located every 300 microns along the length of the conductor. Figure 5.45 illustrates the measured resistance as a function of distance from the via.

All of the measurements indicated a significant direct current resistance in the interconnects at the via side walls. These results imply that the one probable cause of this direct current resistance increase was thinning of the metal in that region. Consequently, this region presents a significant impedance for low-impedance circuits, and it is a potential failure point and location for heat concentration.

Table 5.11. Second Level Interconnect Electrical Resistivity Results.

Conductor	Thickness (μm)	Width (μm)	Length (μm)	Resistance (Ω)	Resistivity ($\Omega\cdot$cm)
3	1.2	150	4500	4.3	$1.7(10^{-5})$
4	1.2	150	3100	2.0	$1.2(10^{-5})$

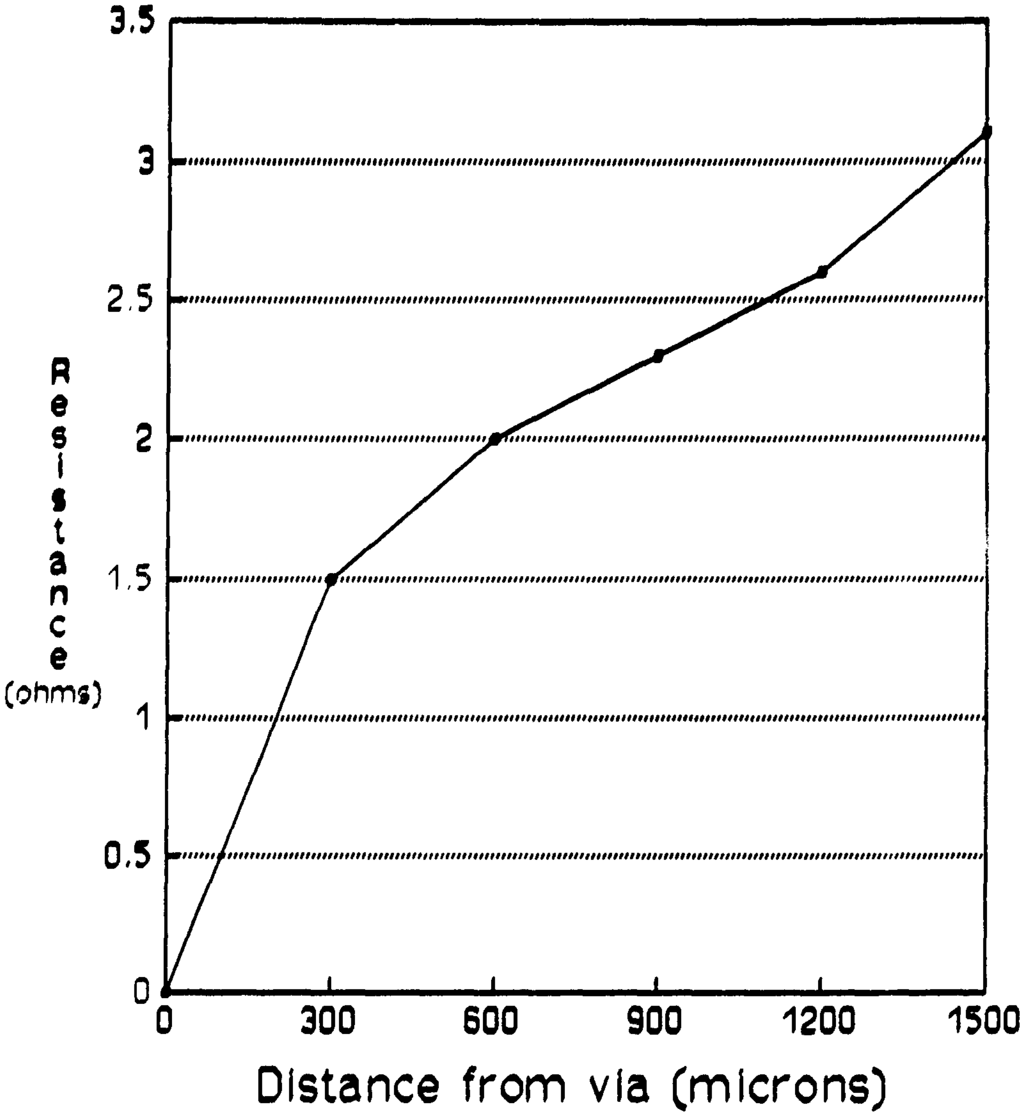


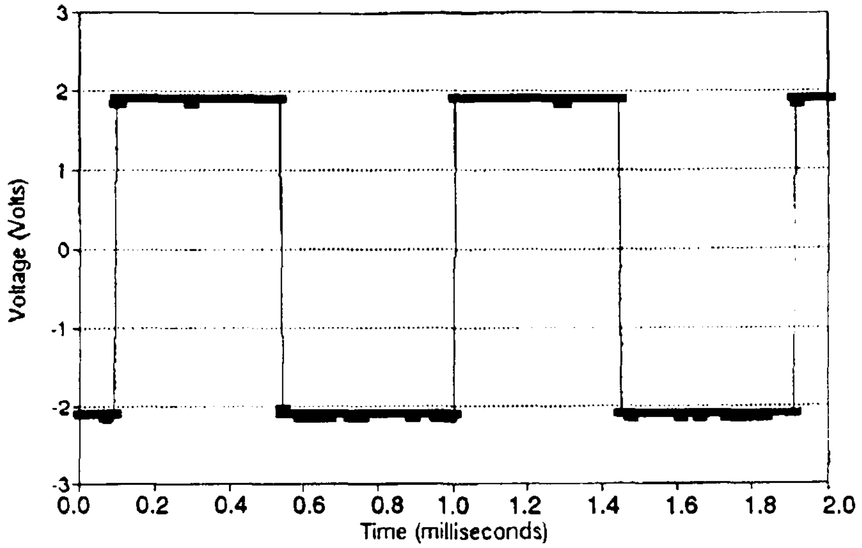
Figure 5.45. Direct current resistance as a function of an interconnect's length on a second-level conductor.

Signal Attenuation and Propagation Delay. The second set of electrical performance evaluation measurements on the two test samples involved measuring signal attenuation and propagation delay across an adjacent pair of interconnects. These measurements were taken on each sample with 1 MΩ and 50 Ω loads. Symmetrical, bipolar square waves were imposed on one end of the interconnect pair, and the load was connected at the other end. Testing was conducted over a frequency range of 1 kHz to 10 MHz.

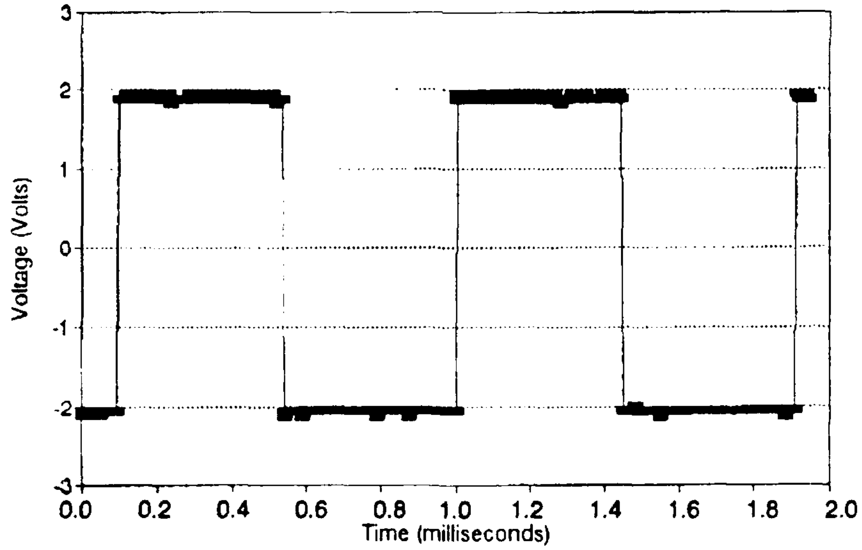
Figure 5.46 illustrates the input and output voltage signals recorded at 1 kHz with a 1 MΩ load. As this figure illustrates, there was no significant perturbation in the waveform that can be attributed to the interconnect's impedance. Figure 5.47 depicts the signals recorded at 5 MHz with a 1 MΩ load. The output waveform at this frequency illustrates the low-pass filter effect of the interconnect. The resistance of the interconnect, combined with the coupling capacitance between the two conductors, created a low pass filter which affected high frequency signals imposed on the interconnects.

For this electrical performance evaluation, attenuation was defined as:

$$A = 20\log\frac{V_o}{V_i} \quad \text{(dB)} \tag{5.1}$$

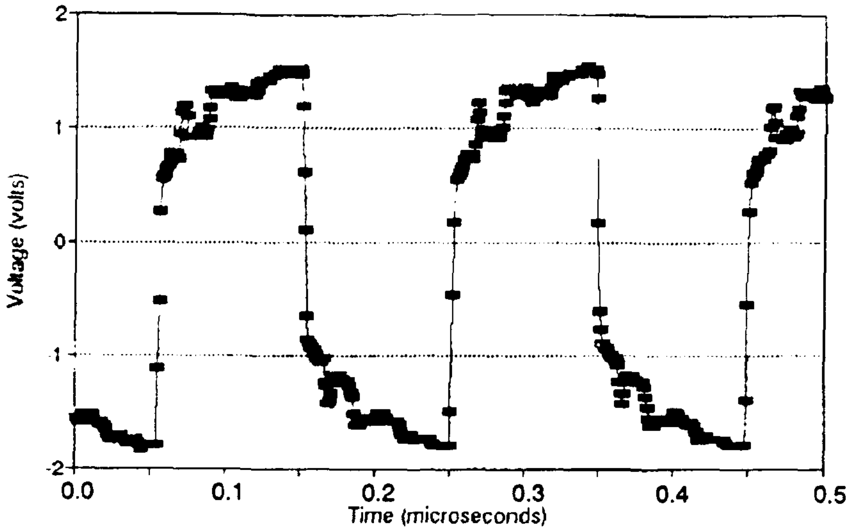


(a) Input signal waveform

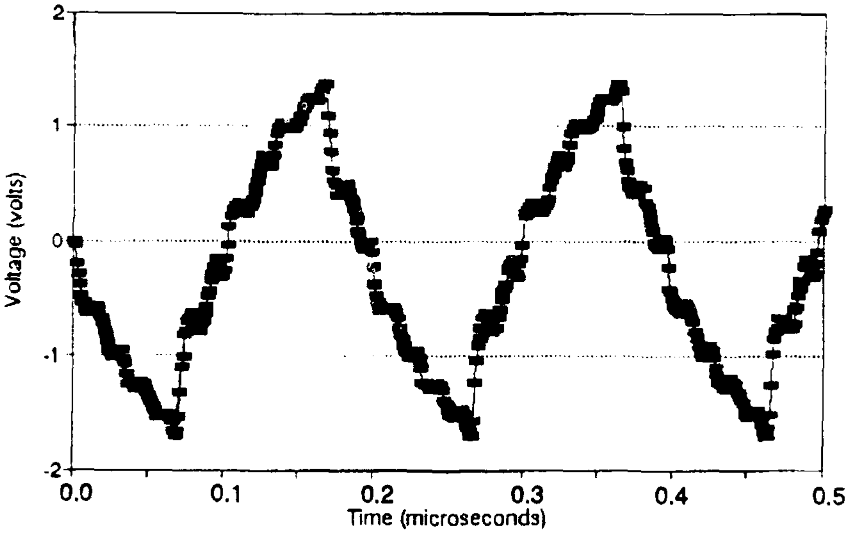


(b) Output signal waveform

Figure 5.46. Signal waveforms measured on WSI interconnect pair for a 1 kHz square wave.



(a) Input signal Waveform



(b) Output signal Waveform

Figure 5.47. Signal waveforms measured on a WSI interconnect pair for a 5 MHz square wave.

where

A is the signal attenuation
V_o is the measured output voltage
V_i is the measured input voltage.

Attenuation values were calculated from the voltage measurements that were accomplished at discrete frequency values over the 1 kHz to 10 MHz range. In Figure 5.48, attenuation is plotted as a function of frequency for the sample without the IC die. Attenuation as a function of frequency for the sample containing the IC die is presented in Figure 5.49.

As the data illustrates, the attenuation for the 1 MΩ load is small over the frequency range investigated. Digital CMOS applications typically use circuits with high impedance loads, which generally can tolerate attenuation levels on the order of the measured results. However, the attenuation measured on both samples with the 50 Ω load was significant. The equivalent circuit in this case can be modelled as three impedances with nearly the same magnitude of resistance in series. The level of attenuation can be attributed to the voltage division of the input signal across these impedances.

Propagation delay was defined as the time difference between the midpoint of the leading edges of the input and output pulses, as illustrated in Figure 4.21. Propagation delay as a function of frequency is presented in Figure 5.50 for the WSI sample without the IC die. Figure 5.51 illustrates the same results for the sample containing the IC die.

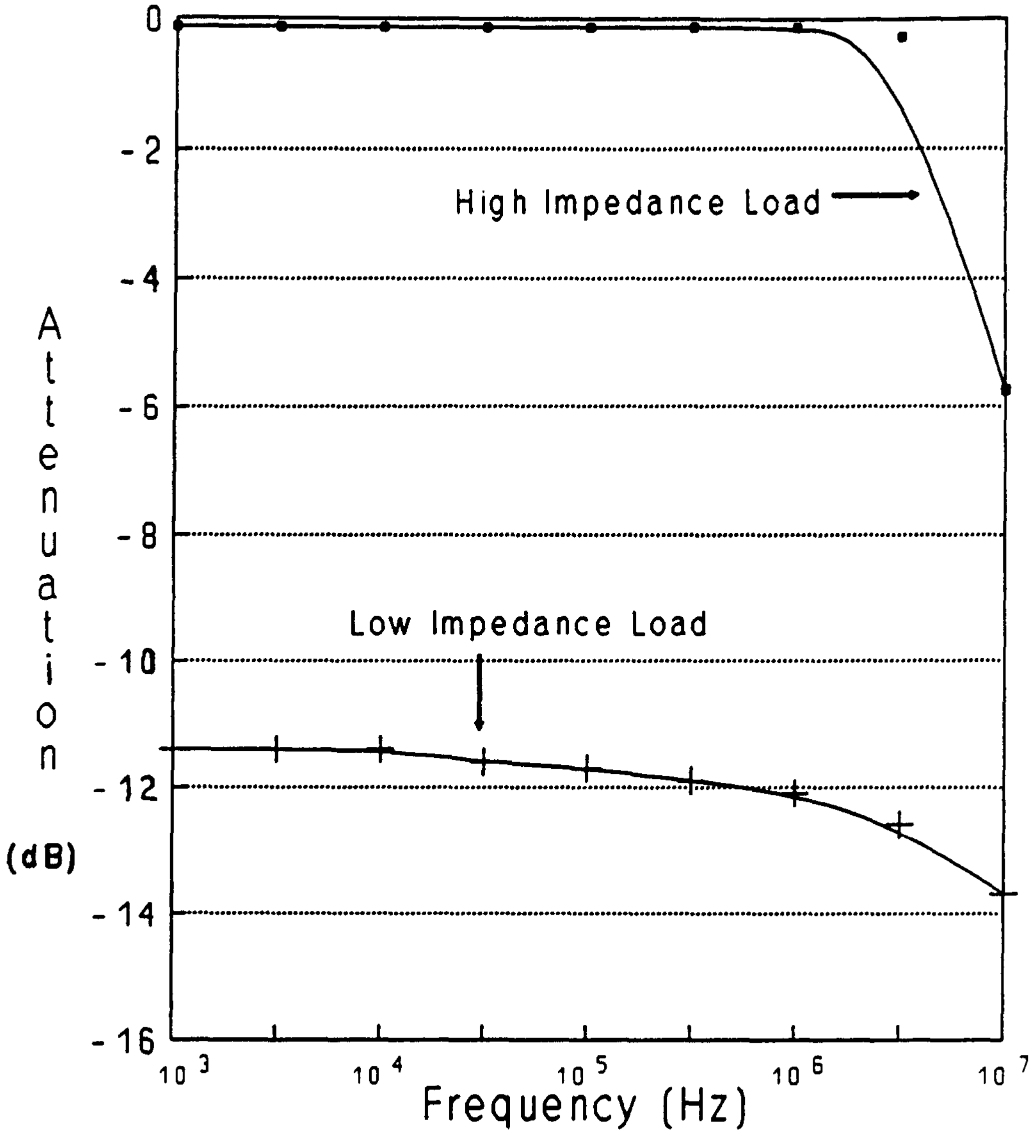


Figure 5.48. Attenuation as a function of frequency measured on the sample with no IC die.

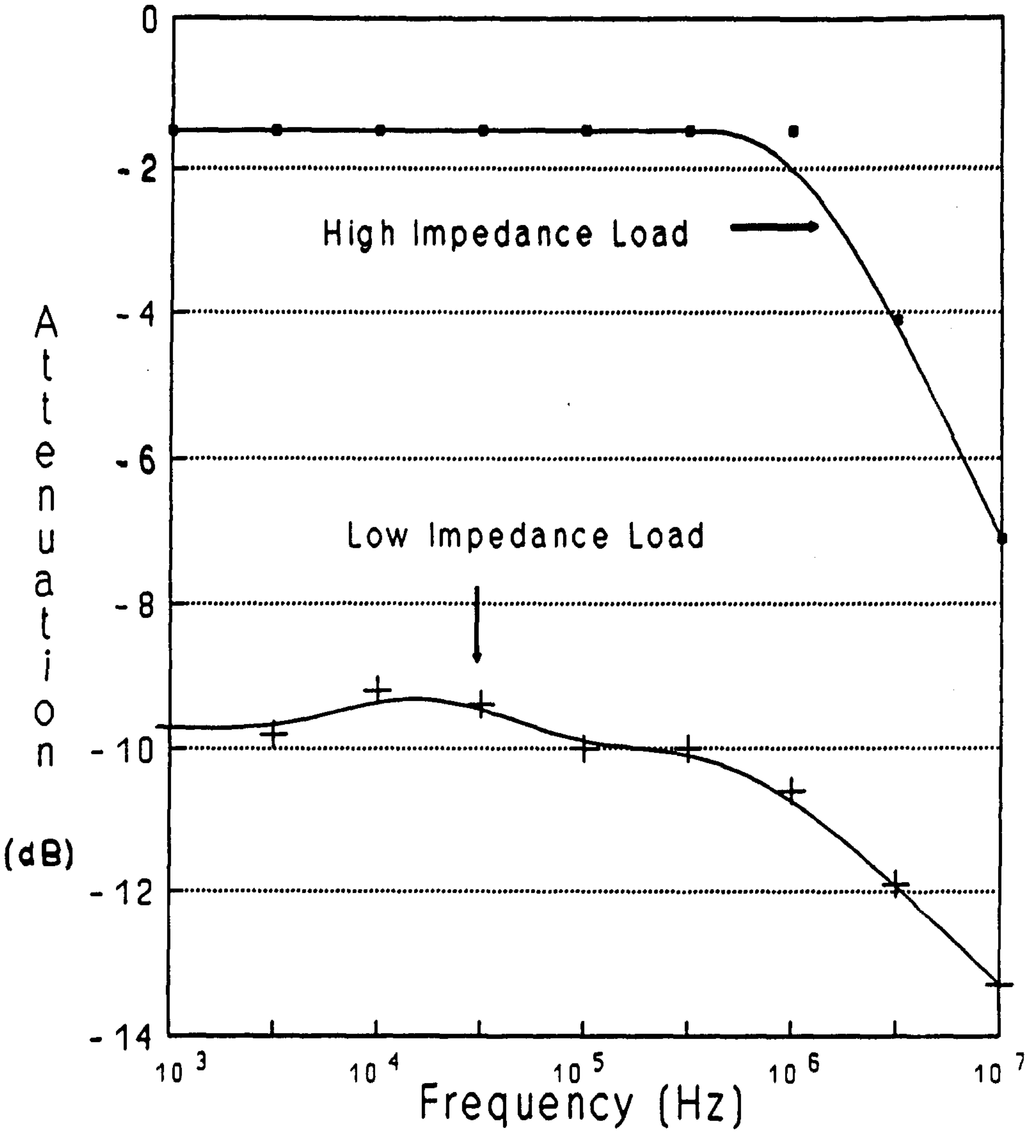


Figure 5.49. Attenuation as a function of frequency measured on the test sample containing an IC die.

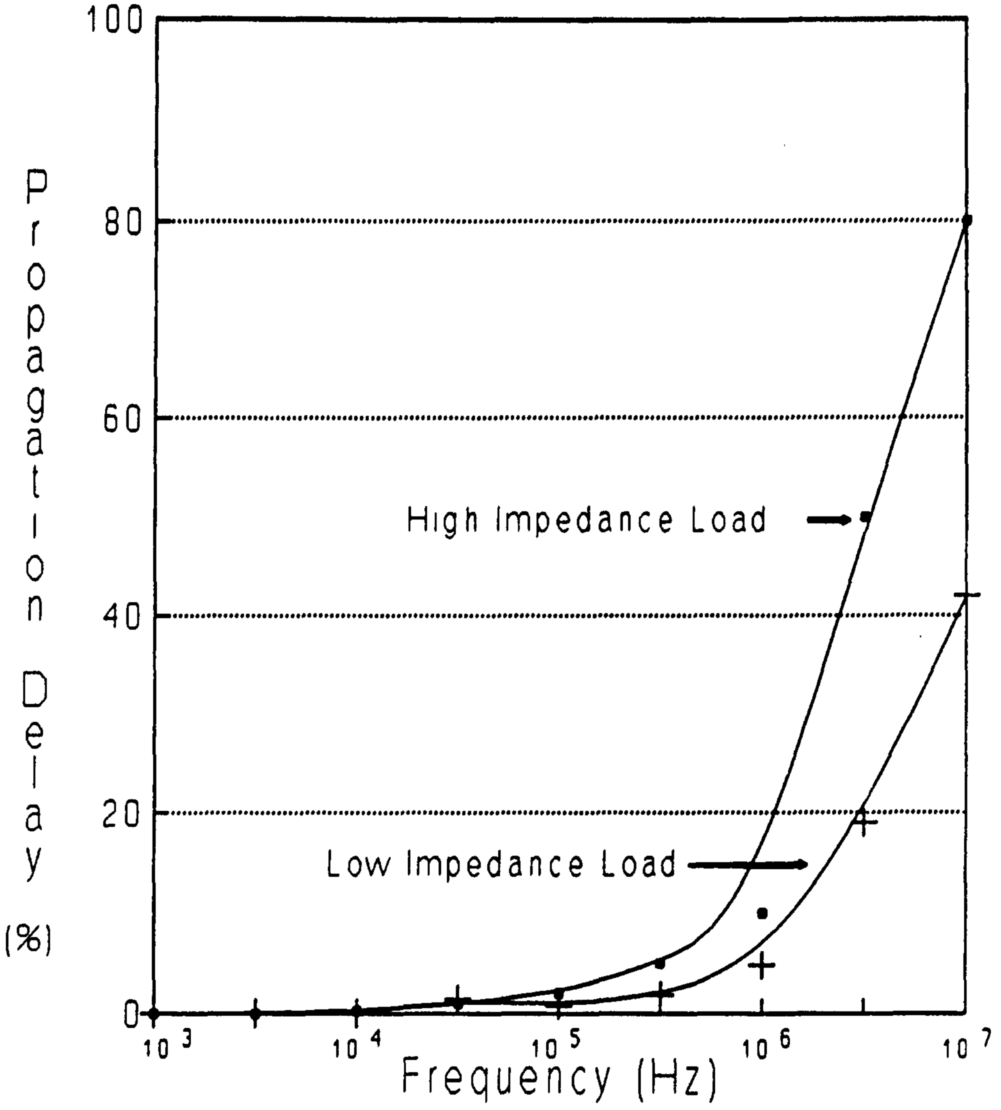


Figure 5.50. Propagation delay as a function of frequency measured on the test sample with no IC die.

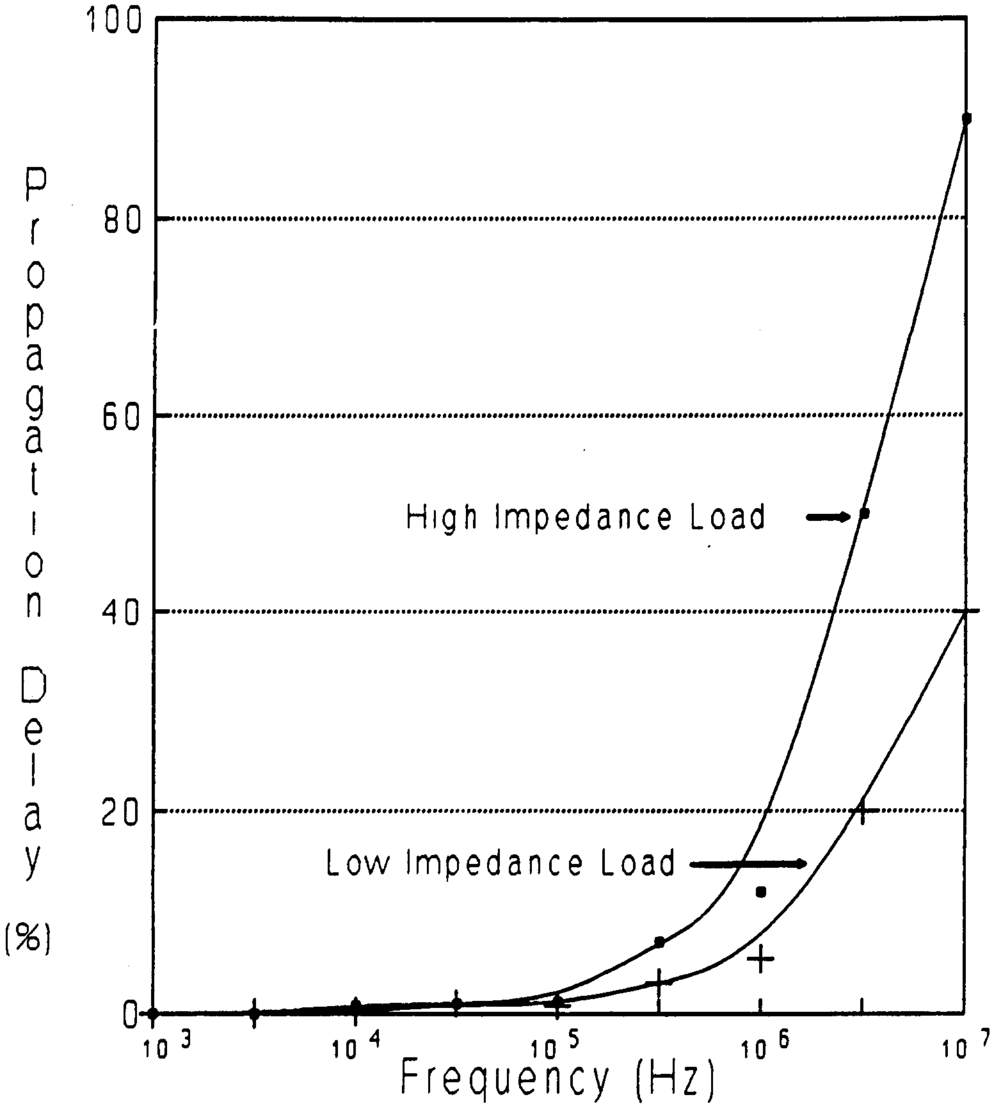


Figure 5.51. Propagation delay as a function of frequency measured on the test sample containing an IC die.

Coupling. Coupling measurements were performed using three different interconnect configurations. The first coupling measurement was accomplished with respect to the interconnect located adjacent to the interconnect contacting the positive terminal of the input signal generator. The signal on the interconnect located adjacent to the common interconnect was measured in the second configuration. The third configuration measured the coupling between the second- and first-level interconnects.

By using the different interconnection combinations described above, coupling was calculated using Equation 5.1. The voltage values were measured at the input and output terminals for the symmetrical, bipolar square waves at discrete frequencies spanning 1 kHz to 10 MHz. For the test sample without an IC die, coupling as a function of frequency is plotted in Figure 5.52. This plot includes measurements from the three test configurations with 50 Ω load and 1 MΩ loads. Figure 5.53 illustrates coupling as a function of frequency for the same test configurations using the WSI test sample containing the IC die.

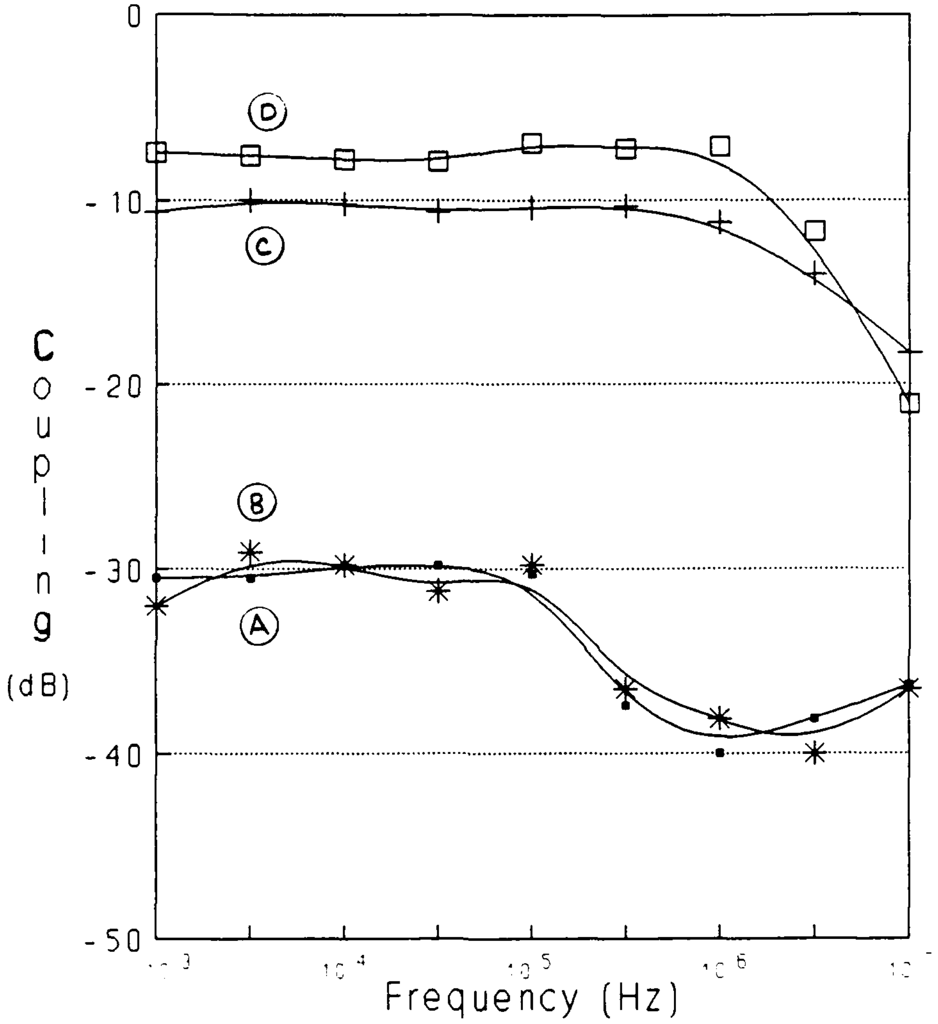


Figure 5.52. Coupling as a function of frequency measured on the WSI test sample with no IC die. (A) Configuration 1, 50 Ω load, (B) Configuration 2, 50 Ω load, (C) Configuration 1, 1 MΩ load, (D) Configuration 2, 1 MΩ load.

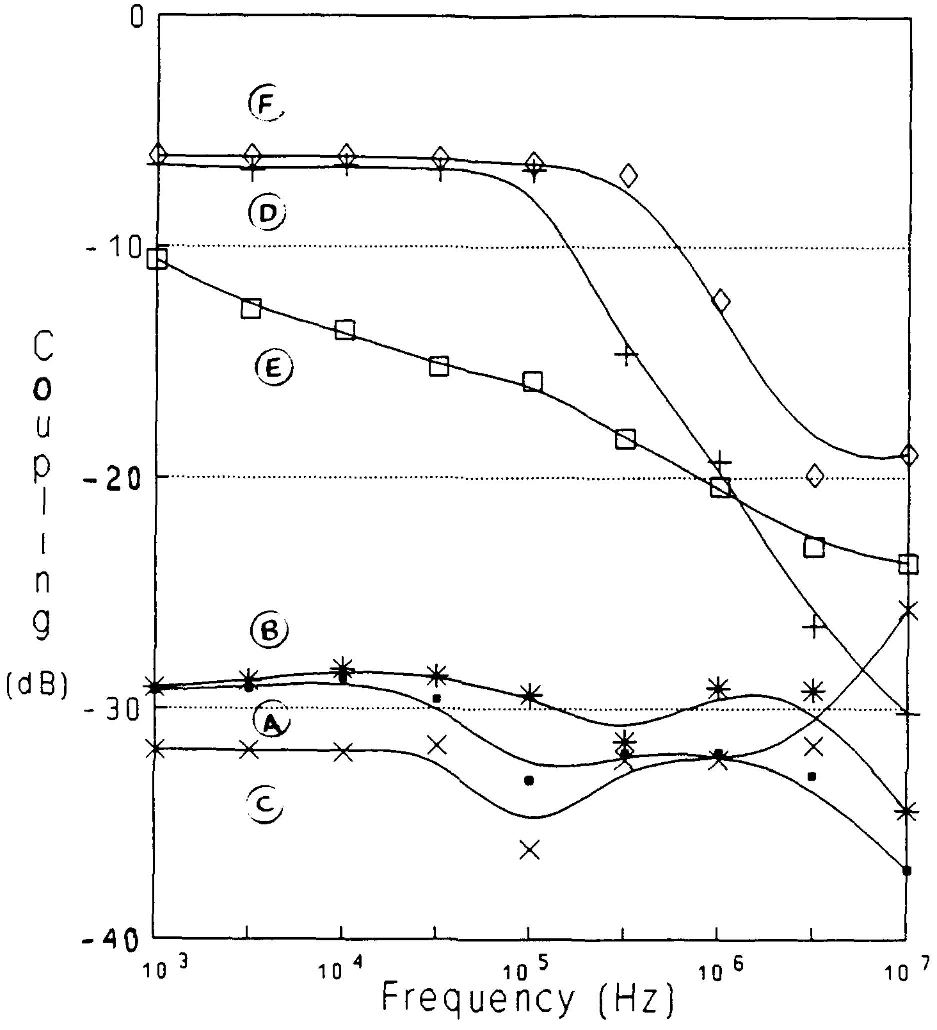


Figure 5.53. Coupling as a function of frequency measured on the WSI test sample containing an IC die. (A) Configuration 1, 50 Ω load, (B) Configuration 2, 50 Ω load, (C) Configuration 3, 50 Ω load, (D) Configuration 1, 1 MΩ load, (E) Configuration 2, 1 MΩ load, (F) Configuration 3, 1 MΩ load.

VI. Conclusions and Recommendations

The objective of this research effort was to investigate the implementation of digital and analog circuits in a WSI system. A test circuit composed of analog and digital subsystems was designed and tested through simulation. IC die containing the test circuit's subsystems were utilized to fabricate the WSI system. Preliminary investigations were conducted to evaluate potential improvements to the IC die mounting procedure, a critical step in fabricating a functional WSI system. An evaluation of candidate polyimides that were to be used as the interlevel dielectric in the WSI system was also performed. Test samples for each of the proposed WSI configurations were fabricated and tested for interconnect electrical continuity. Additional electrical characterization measurements were conducted on two of the test samples. This chapter presents the conclusions drawn from the results of this research effort, and recommendations are formulated for further research in the WSI process.

Conclusions

Evaluation of the IC Die Mounting Procedure. In the investigation of barrier coating materials, the Teflon® spray was the only candidate material which produced acceptable results. The Teflon® spray produced a coating with acceptable smoothness, and it was not adversely affected by the epoxy cure temperature. However, the Teflon® coating was prone to scratching during handling, and acetone cleaning of the excess epoxy damaged the coating. As a result, each Teflon® coating could only be used once in the IC die mounting process.

Of the alternative IC die mounting procedures investigated, the single-step procedure was superior. This procedure produced consistent, repeatable results, with IC die-to-host substrate step heights falling within the maximum tolerance (±20 microns). This procedure was also the least complex of the procedures investigated. Although this procedure generally produced assemblies satisfying the step height tolerance, the regions between the IC die and host substrate exhibited a high degree of voiding. These voids adversely affected the ability of the polyimide material to planarize these regions.

Polyimide Evaluation. The polyimide evaluation demonstrated that two of the three candidates could function as a suitable interlevel dielectric material. Of these two materials, the Selectilux HTR3-200 polyimide was preferred because of the higher success rate in producing interconnects on this material with no discontinuities, particularly in the via regions (100 percent of the interconnects on the test samples demonstrated electrical continuity). The photosensitive nature of the Selectilux polyimide also led to fewer processing steps (four) to realize patterned vias.

The Ultradel 4212 polyimide did not show comparable advantages based upon the high percentage of discontinuous interconnects (16 percent of the interconnects on the test sample produced using a 140° softbake failed to demonstrate electrical continuity). Additionally, because the Ultradel 4212 polyimide is not photosensitive, it requires a greater number of processing steps. However, the Ultradel 4212 polyimide demonstrated vias which were more compact compared to those formed with the Selectilux HTR3-200 material. This characteristic could be important in applications requiring reduced bond pad pitch.

IC Die Alignment. The processing steps involved in etching the cavities in the host substrate and mounting the IC die produced acceptable IC die alignment in this study. The results demonstrated that, given an IC die with a uniform surface area and thickness, along with a uniform host substrate thickness, IC die cavities can be designed and fabricated with small tolerances. With proper alignment to the silicon wafer's crystal orientation, IC die cavities with consistent dimensions and smooth side walls were produced using wet chemical etching. The small tolerances of the IC die cavities (sized 100 microns on each side larger than the IC die dimensions) limited the misalignment of the IC die. A common set of masks was developed which accounted for a small degree of misalignment by maintaining a ratio of the via size to IC die bond pad size of 1 to 3. These common mask patterns were successfully aligned to the bond pads on all of the IC die incorporated in the four test samples.

Fabrication of WSI Test Samples. The primary obstacle in fabricating functional WSI test samples for the multiple IC die configurations was the inadequate filling of the transition regions between the IC die and the host substrate. The epoxy exhibited a large number of voids in this region. The polyimide coatings failed to fill these voids, resulting in large step heights. The evaporated aluminum did not provide continuous interconnects over this inhomogeneous topology. The lack of sufficient continuous interconnects on the multiple IC die WSI test samples prevented electrical testing.

Electrical Performance Evaluation Results. The primary conclusion resulting from the electrical performance evaluation data is that the interconnects behave as lossy transmission lines with resistances of significant magnitude (2 to 60 ohms) that cannot be neglected in an analog circuit application. Potential failure points in the circuit investigated in this research were the interconnects which provide the two analog input signals to the comparator subsystem. The attenuation of these interconnects would most likely result in an erroneous output from the comparator, unless the losses introduced to the signals were matched. Nevertheless, the measured data supports the conclusion that digital circuits with high impedance loads could function properly with the interconnects fabricated during this effort.

Recommendations

Investigation of IC Die Mount Materials. With the increased emphasis on improving microelectronic packaging techniques, new adhesive materials have been developed since the research conducted by Mainger (24). Thermally conductive epoxies, for example, have recently been developed which are compatible with high temperature IC processing environments (46,47). This characteristic may allow bonded substrates to be exposed to temperatures which could completely cure the polyimide coatings and anneal the aluminum interconnects. A preliminary investigation of a thermally conductive epoxy, A. I. Technology EG7659, demonstrated its compatibility with the high temperature IC processing environment, as well as the chemicals and materials required to fabricate a WSI system. Further research is recommended to survey the new developments in adhesive technology and to identify and characterize candidate adhesives. Critical characteristics which should be investigated include: processing temperature limitations, adhesive viscosity, voiding, and bond strength.

Additional investigations into the alternative IC die mount procedures is also warranted. The ability to apply polyimide as an adhesive utilizing a spray coat process may improve upon the results demonstrated in the Clamped substrate mounting procedure. Spray coating could result in a polyimide layer which is sufficiently thin, and could be fully cured to realize an adequate bond for the IC die. Spray coating techniques are possible with polyimide materials (20:40).

Investigation of the Interlevel Dielectric. As indicated in Chapter II, a variety of materials exist which have been utilized as interlevel dielectrics in microelectronic circuits. AFIT research has focused on the polyimide materials because of their ability to provide sufficiently thick layers, their ability to be patterned using wet chemical etching techniques, and their favorable relative dielectric constant. Eliminating the constraint for wet chemical patterning would allow additional materials to be considered, as well as alternative patterning techniques. Specifically, further research is recommended regarding alternative dielectric materials, such as the spin-on glasses and benzocyclobutene polymers. In addition, an investigation focused on dielectric patterning utilizing reactive ion etching is recommended to determine its potential application to future WSI research. Other research efforts have demonstrated the capabilities of reactive ion etching in the formation of smoothly sloped via side walls in dielectric materials (20,28,41).

Characterization of Metallization Techniques. The electrical performance of the interconnects fabricated in this research was limited by high impedance regions located along the via side walls. This high impedance, on the order of 30 ohms for narrow (50 micron width) conductors, and 1 ohm for wide (150 micron width) conductors, resulted from the aluminum metal being thinned, which was caused by one of two factors. First, the slope of the via side wall presented a surface which was nearly perpendicular to the aluminum source during the evaporation process. The nonconformal coating of the aluminum during evaporation may have resulted in a thinner layer of metal on the via side wall. The other possible cause of this thinned region may be attributed to the partial etching of the aluminum during patterning (a result of incomplete coating by the photoresist pattern). The slope of the via side wall and the large step height may have also exceeded the conformal coating capabilities of the photoresist used in this research.

A detailed characterization of the metallization process relative to via topologies is recommended to identify the contributions of these and other potential failure mechanisms. This study could include the investigation of alternative metallization techniques, such as sputtering, as well as alternative metal patterning processes, such as the lift-off technique. An investigation concerned with the effect of photoresist layer thickness on the resulting patterned metal layer thickness is also warranted.

Appendix A. Counter Circuit VHDL Models

This appendix contains the models used to simulate the counter circuit. Each file begins with a description of the file and a list of any required lower level models.

```
---------------------------------------------------------------
---------------------------------------------------------------
--
--  std.vhd
--  Ver 2 (with delays) Date 29 Nov 90
--
--    This file contains VHDL descriptions for the basic
--  components identified by the base_cmos GES system.
--  Descriptions for the transistors are also included.
--  The body of most of the code must be filled in by the
--  user.


entity INV is
    generic(constant tPLH:TIME:=1 ns;
            constant tPHL:TIME:=1 ns);
          port (signal A:in bit;
                signal B:out bit);
end;
architecture inv of inv is
  begin
  --your code goes here.
  B <= not A after 1 NS; -- or use this.
  end inv;


entity INVZ is
    generic(constant tPLH:TIME:=1 ns;
            constant tPHL:TIME:=1 ns);
          port (signal P:in bit;
                signal N:in bit;
                signal A:in bit;
                signal B:out bit);
end;


architecture invZ of invZ is
  begin
  --your code goes here.

  process (a,p,n)
   variable temp_out: bit
```

```
   begin

     if p='0' and n='1' then
         b <= not a after 1 NS;
     end if;
   end process;

  end invZ;


entity NAND_GATE is
    generic(constant tPLH:TIME:=1 ns;
            constant tPHL:TIME:=1 ns);
         port  (signal A:in bit;
                signal B:in bit;
                signal C:out bit);
end;
architecture nand_gate of nand_gate is
  begin
  --your code goes here.
  C <= A nand B after 1 NS; -- or use this.
  end nand_gate;


entity NOR_GATE is
    generic(constant tPLH:TIME:=1 ns;
            constant tPHL:TIME:=1 ns);
         port  (signal A:in bit;
                signal B:in bit;
                signal C:out bit);
end;
architecture nor_gate of nor_gate is
  begin
  --your code goes here.
  C <= A nor B after 1 NS; -- or use this.
  end nor_gate;
```

```
-----------------------------------------------------------------
-- Date:  14 Nov 90
-- Version:  1
--
-- Unix filename:  and2.vhd
--
-- Function: This file is a structural and entity description of an
--   AND gate. The file requires an invertor and a nand gate as
components.
--
-----------------------------------------------------------------

entity and2 is
  port(i1,i2: in bit; o1: out bit);
end and2;

architecture structure of and2 is

signal Z1: Bit;

component inv
  port(a: in bit; b: out bit);
end component;

component nand_gate
  port(a,b: in bit; c: out bit);
end component;

begin
U1: nand_gate port map(i1,i2,z1);
U2: inv port map(z1,o1);
end structure;
```

```
------------------------------------------------------------------
-- Date:  14 Nov 90
-- Version:  1
--
-- Unix filename:  or2.vhd
--
-- Function: This file is a structural and entity description of an
--   OR gate. The file requires an invertor and a nor gate as
components.
--
------------------------------------------------------------------

entity or2 is
  port(i1,i2: in bit; o1: out bit);
end or2;

architecture structure of or2 is

signal Z1: Bit;

component inv
  port(a: in bit; b: out bit);
end component;

component nor_gate
  port(a,b: in bit; c: out bit);
end component;

begin
U1: nor_gate port map(i1,i2,z1);
U2: inv port map(z1,o1);
end structure;
```

```
-----------------------------------------------------------------
-- Date:  14 Nov 90
-- Version:  1
--
-- Unix filename:  dfflop.vhd
--
-- Function: This file is a structural and entity description of an
--   D flip flop. The file requires an invertor and a controlled
--   inverter as gates.
-----------------------------------------------------------------

entity dfflop is
  port(d,clck1: in bit; q,nq: out bit);
end dfflop;

architecture structure of dfflop is

signal c,nc: Bit;
signal z1,z3: Bit;
signal z0,z10,zr0: Bit;
signal z2,z12,zr2: Bit;

component inv
  port(a: in bit; b: out bit);
end component;

component invz
  port(p,n,a: in bit; b: out bit);
end component;

begin
CINV1: invz port map(nc,c,d,z10);
CINV2: invz port map(c,nc,z1,zr0);
CINV3: invz port map(c,nc,z1,z12);
CINV4: invz port map(nc,c,z3,zr2);
INV1: inv port map(clck1,nc);
INV2: inv port map(nc,c);
INV3: inv port map(z0,z1);
INV4: inv port map(z2,z3);
q <= z3;
nq <= z2;
z2 <= z12 when not z12'quiet else
      zr2 when not zr2'quiet else
      z2;
z0 <= z10 when not z10'quiet else
      zr0 when not zr0'quiet else
      z0;

end structure;
```

```
----------------------------------------------------------------
-- Date:  15 Feb 91
-- Version:  1
--
-- Unix filename:  msb3.vhd
--
-- Function:  This file is a structural description of a most
significant bit slice for the counter circuit.
--  The file requires a D Flip Flop, NAND, OR and inverter gates as
components.
--
----------------------------------------------------------------

entity msb3 is
   port(clk1,qdr,qorp,nqandp: in bit; qxp: out bit);
end msb3;

architecture structure of msb3 is

signal Z1,Z2,Z3,Z4,ind,outq,outnq: Bit;

component nand_gate
  port(a,b: in bit; c: out bit);
end component;

component inv
  port(a: in bit; b: out bit);
end component;

component or2
  port(i1,i2: in bit; o1: out bit);
end component;

component dfflop
  port (d,clck1: in bit; q,nq: out bit);
end component;

begin
B1: inv port map(qorp,z4);
N1: nand_gate port map(outnq,nqandp,z2);
N2: nand_gate port map(z2,z3,z1);
N3: nand_gate port map(outq,z4,z3);
Or1: or2 port map(qdr,z1,ind);
DF1: dfflop port map(ind,clk1,outq,outnq);
qxp <= outq;
end structure;
```

```
-----------------------------------------------------------------
-- Date:  15 Feb 91
-- Version:  1
--
-- Unix filename:  oddbit.vhd
--
-- Function:  This file is a structural description of a odd bit
slice for the counter circuit.
--   The file requires a D Flip Flop, NAND, AND and NOR gates as
components.
--
-----------------------------------------------------------------

entity oddbit is
   port(clk1,nqdr,qorp,nqandp,qxn:  in  bit;  qxp,qorn,nqandn:  out
bit);
end oddbit;

architecture structure of oddbit is

signal Z1,Z2,Z3,Z4,ind,outq,outnq: Bit;

component nand_gate
  port(a,b: in bit; c: out bit);
end component;

component nor_gate
  port(a,b: in bit; c: out bit);
end component;

component and2
  port(i1,i2: in bit; o1: out bit);
end component;

component dfflop
  port (d,clck1: in bit; q,nq: out bit);
end component;

begin
N1: nand_gate port map(qxn,z1,z2);
N2: nand_gate port map(z2,z3,z4);
N3: nand_gate port map(outq,qorp,z3);
A1: and2 port map(z4,nqdr,ind);
Or1: nor_gate port map(qorp,outq,qorn);
Or2: nor_gate port map(outq,nqandp,z1);
DF1: dfflop port map(ind,clk1,outq,outnq);
qxp <= outq;
nqandn <= z1;
end structure;
```

```
-----------------------------------------------------------------
-- Date:  15 Feb 91
-- Version:  1
--
-- Unix filename:  evenbit.vhd
--
-- Function:  This file is a structural description of a even bit
slice for the counter circuit.
--  The file requires a D Flip Flop, NAND, AND and inverter gates
as components.
-----------------------------------------------------------------

entity evenbit is
   port(clk1,nqdr,qorp,nqandp,qxn:  in  bit;  qxp,qorn,nqandn:  out
bit);
end evenbit;

architecture structure of evenbit is

signal Z1,Z2,Z3,Z4,Z5,Z6,ind,outq,outnq: Bit;

component nand_gate
  port(a,b: in bit; c: out bit);
end component;

component inv
  port(a: in bit; b: out bit);
end component;

component and2
  port(i1,i2: in bit; o1: out bit);
end component;

component dfflop
  port (d,clck1: in bit; q,nq: out bit);
end component;

begin
B1: inv port map(z1,z5);
B2: inv port map(qorp,z6);
N1: nand_gate port map(qxn,z5,z2);
N2: nand_gate port map(z2,z3,z4);
N3: nand_gate port map(outq,z6,z3);
N4: nand_gate port map(outnq,nqandp,z1);
N5: nand_gate port map(qorp,outnq,qorn);
A2: and2 port map(z4,nqdr,ind);
DF1: dfflop port map(ind,clk1,outq,outnq);
qxp <= outq;
nqandn <= z1;
end structure;
```

```
-----------------------------------------------------------------
-- Date:  15 Feb 91
-- Version:  1
--
-- Unix filename:  lsb3.vhd
--
-- Function:  This file is a structural description of a least
significant bit slice for the counter circuit.
--  The file requires a D Flip Flop, NAND, AND and NOR gates as
components.
--
-----------------------------------------------------------------

entity lsb3 is
   port(clk1,nqdr,qorp,qxn: in bit; qxp,qorn,nqandn: out bit);
end lsb3;

architecture structure of lsb3 is

signal Z1,Z2,Z3,Z4,ind,outq,outnq: Bit;

component nand_gate
  port(a,b: in bit; c: out bit);
end component;

component nor_gate
  port(a,b: in bit; c: out bit);
end component;

component and2
  port(i1,i2: in bit; o1: out bit);
end component;

component dfflop
  port (d,clck1: in bit; q,nq: out bit);
end component;

begin
N1: nand_gate port map(qxn,outnq,z2);
N2: nand_gate port map(z2,z3,z4);
N3: nand_gate port map(outq,qorp,z3);
A1: and2 port map(z4,nqdr,ind);
Or1: nor_gate port map(qorp,outq,qorn);
DF1: dfflop port map(ind,clk1,outq,outnq);
qxp <= outq;
nqandn <= outnq;
end structure;
```

```
------------------------------------------------------------------
-- Date:  15 Feb 91
-- Version:  1
--
-- Unix filename:  ver3.vhd
--
-- Function:   This file is a structural description of a
programmer.
-- The file requires a D Flip Flop, AND gate, LSB3, MSB3, ODDBIT,
and EVENBIT components.
--
------------------------------------------------------------------

entity ver3 is
  port(x,phi1: in bit; qout: out bit_vector(0 to 7); QR: out bit);
end ver3;

architecture structure of ver3 is

signal Z0,Z1,Z2,Z3,Z4,Z5,Z6,Z7,Z8: Bit;
signal dqr,dnqr: Bit;
signal qorp0,qorp1,qorp2,qorp3,qorp4,qorp5,qorp6: Bit;
signal  nqandn0,nqandn1,nqandn2,nqandn3,nqandn4,nqandn5,nqandn6:
Bit;

component LSB3
  port(clk1,nqdr,qorp,qxn: in bit; qxp,qorn,nqandn: out bit);
end component;

component oddbit
  port(clk1,nqdr,qorp,nqandp,qxn:  in  bit;  qxp,qorn,nqandn:  out
bit);
end component;

component evenbit
  port(clk1,nqdr,qorp,nqandp,qxn:  in  bit;  qxp,qorn,nqandn:  out
bit);
end component;

component MSB3
  port(clk1,qdr,qorp,nqandp: in bit; qxp: out bit);
end component;

component dfflop
  port (d,clck1: in bit; q,nq: out bit);
end component;

component and2
  port (i1,i2: in bit; o1: out bit);
end component;
```

```
begin

BIT0: MSB3 port map(phi1,dqr,qorp0,nqandn0,z0);
BIT1: oddbit port map(phi1,dnqr,qorp1,nqandn1,z0,z1,qorp0,nqandn0);
BIT2: evenbit port
map(phi1,dnqr,qorp2,nqandn2,z1,z2,qorp1,nqandn1);
BIT3: oddbit port map(phi1,dnqr,qorp3,nqandn3,z2,z3,qorp2,nqandn2);
BIT4: evenbit port
map(phi1,dnqr,qorp4,nqandn4,z3,z4,qorp3,nqandn3);
BIT5: oddbit port map(phi1,dnqr,qorp5,nqandn5,z4,z5,qorp4,nqandn4);
BIT6: evenbit port
map(phi1,dnqr,qorp6,nqandn6,z5,z6,qorp5,nqandn5);
BIT7: LSB3 port map(phi1,dnqr,x,z6,z7,qorp6,nqandn6);
DF1: dfflop port map(z8,phi1,dqr,dnqr);
A1: and2 port map(z7,dnqr,z8);
qout(0) <= z0;
qout(1) <= z1;
qout(2) <= z2;
qout(3) <= z3;
qout(4) <= z4;
qout(5) <= z5;
qout(6) <= z6;
qout(7) <= z7;
qr <= dqr;

end structure;
```

```
-----------------------------------------------------------------
-----------------------------------------------------------------
-- Date:  15 Feb 91
-- Version:  1
--
-- Unix Filename:  configuration.vhd
--
-- This is the configuration specification file for the project
test
-----------------------------------------------------------------
-----------------------------------------------------------------

use work.all;

configuration system of test_bench is

for test

--             for   PROG1   :   project            use   entity
work.programmer(behavioral);
    for PROG1 : project    use entity work.programmer(structure);
--    for PROG1 : project    use entity work.ver3(structure);
    end for;

end for;

end system;
```

```
---------------------------------------------------------------
---------------------------------------------------------------
-- Date:  24 Nov 90
-- Version:  3
--
-- Unix Filename:  test_bench.vhd
--
-- Function:  This file contains the test bench for testing the
--  counter.  Besides the port map of the component, it
--  generates the input data and clock signals, and has a process
--  that controls the simulation.
---------------------------------------------------------------
---------------------------------------------------------------

entity test_bench is
end test_bench;

architecture test of test_bench is

component project
  port(x,phil: in BIT; qout: out bit_vector(0 to 7); qr: out BIT);
end component;

signal x,phil,qr: bit;
signal qout: bit_vector(0 to 7);
signal stop_sim: boolean := FALSE;

begin
  PROG1: project port map (x,phil,qout,qr);
  phil <= not phil after 15 ns;
  x <= '0',
           '1' after 1 ns,
           '0' after 42 ns,
           '1' after 75 ns,
           '0' after 124 ns,
           '1' after 160 ns,
           '0' after 570 ns;
stop_sim <= TRUE after 900 ns;

STOP_CONTROL: process
  begin
  wait until stop_sim = TRUE;
  assert false report "Simulation Done" severity failure;
end process STOP_CONTROL;

end test;
```

```
'This file was used to implement the model in VHDL

cd test_bench
set base binary
monitor active *'signal
trace *'signal
open run.out
logtime -e run.out
list > run.out
run > run.out
quit
```

Appendix B. Counter Circuit ESIM Simulation Results

```
pan% esim ver3b.sim ver3b.ecmds
454 transistors, 249 nodes (0 pulled up)
initialization took 417 steps
initialization took 0 steps
initialization took 0 steps
initialization took 0 steps
>0101010101010101010101010101010101010101010101010101010101:IZCLK
>1100011100011111111111111111111111111100000000000000000000:IZX
>110000000000000001100000000000000001100000000000000001100:OZ_QDR
>0011000000000000000011111111111111111111000000000000000011:OZ_Q0
>1100111111111111111100111111111111111100110000000000000000:OZ_Q1
>1100001111111111111100001111111111111100001100000000000000:OZ_Q2
>1100000011000000000000000011111111111100000011000000000000:OZ_Q3
>0000000000111111111100000000111111111100000000110000000000:OZ_Q4
>0000000000001111111100000000001111111100000000001100000000:OZ_Q5
>0000000000000011111100000000000011111100000000000011000000:OZ_Q6
>0000000000000000111100000000000000111100000000000000110000:OZ_Q7
454 transistors, 249 nodes (0 pulled up)
sim> quit
pan% exit
pan%
```

APPENDIX C. SPICE Models Utilized in the Circuit Design

```
PROJECT CIRCUIT FOR COUNTER SUBSYSTEM

* POWER SUPPLY AND INPUT VOLTAGES
VDD  1 0 DC 5V
VIN1 2 0 PULSE(0 5 0NS .20NS .20NS 15NS 30NS)
VIN2 3 0 PULSE(0 5 25NS .20NS .20NS 25NS 90NS)

* CIRCUIT BEING ANALYZED

X1 2 3 4 5 6 7 8 1 16 LSB
X2 2 6 13 5 9 10 4 7 1 17 EVENBIT
X3 2 9 14 5 11 12 13 10 1 18 ODDBIT
X4 2 11 20 5 21 22 14 12 1 23 EVENBIT
X5 2 21 24 37 25 26 20 22 1 27 ODDBIT
X6 2 25 28 37 29 30 24 26 1 31 EVENBIT
X7 2 29 32 37 33 34 28 30 1 35 ODDBIT
X8 2 33 32 15 34 1 19 40 MSB

X9 15 37 1 INVERTER

X10 8 5 38 1 AND
X11 38 2 15 5 1 36 DFFLOP

.IC v(8)=5 v(3)=0 v(2)=5 v(4)=0 v(5)=0
.IC v(6)=0 v(7)=0 v(9)=5 v(10)=5 v(11)=0
.IC v(12)=0 v(13)=0 v(14)=0 v(15)=5 v(20)=0
.IC v(21)=5 v(22)=5 v(24)=0 v(25)=0 v(26)=0
.IC v(28)=0 v(29)=5 v(30)=5 v(32)=0 v(33)=0 v(34)=0
.IC v(16)=5 v(17)=0 v(18)=0 v(23)=0 v(27)=0
.IC v(31)=0 v(35)=0 v(19)=0 v(36)=0

.SUBCKT LSB 2 3 4 5 6 7 8 1 13
X1 9 2 8 7 1 13 DFFLOP
X2 8 3 6 1 NOR
X3 8 3 10 1 NAND
X4 7 4 11 1 NAND
X5 10 11 12 1 NAND
X6 5 12 9 1 AND
C1 9 0 50fF
C2 10 0 50fF
C3 11 0 50fF
C4 12 0 50fF
*5 15 0 90fF
*6 3 0 40fF
.ENDS LSB

.SUBCKT EVENBIT 2 3 4 5 6 7 8 9 1 17
X1 10 2 8 11 1 17 DFFLOP
X2 11 9 7 1 NAND
X3 11 3 6 1 NAND
```

```
X4 4 12 13 1 NAND
X5 8 14 15 1 NAND
X6 13 15 16 1 NAND
X7 5 16 10 1 AND
X8 7 12 1 INVERTER
X9 3 14 1 INVERTER
C0 11 0 50fF
C1 11 0 50fF
C2 12 0 50fF
C3 13 0 50fF
C4 14 0 50fF
C5 15 0 50fF
C6 16 0 50fF
.ENDS EVENBIT

.SUBCKT ODDBIT 2 3 4 5 6 7 8 9 1 15
X1 10 2 8 11 1 15 DFFLOP
X2 8 9 7 1 NOR
X3 8 3 6 1 NOR
X4 7 4 12 1 NAND
X5 8 3 13 1 NAND
X6 12 13 14 1 NAND
X7 5 14 10 1 AND
C1 11 0 50fF
C2 12 0 50fF
C3 13 0 50fF
C4 14 0 50fF
C5 10 0 50fF
*6 3 0 40fF
.ENDS ODDBIT

.SUBCKT MSB 2 3 4 5 6 1 13 7
X1 7 2 4 8 1 13 DFFLOP
X2 3 9 1 INVERTER
X3 9 4 10 1 NAND
X4 6 8 11 1 NAND
X5 10 11 12 1 NAND
X6 12 5 7 1 OR
C1 8 0 50fF
C2 9 0 50fF
C3 10 0 50fF
C4 11 0 50fF
C5 12 0 50fF
C6 7 0 50fF
.ENDS MSB


.SUBCKT DFFLOP 2 9 8 7 1 6
X1 9 4 1 INVERTER
X9 4 3 1 INVERTER
X2 2 4 3 5 1 CINV
X3 6 3 4 5 1 CINV2
```

```
X4 5 6 1 INVERTER
X5 6 3 4 7 1 CINV
X6 7 8 1 INVERTER
X7 8 4 3 7 1 CINV2
c0 3 0 .10pF
c1 4 0 .10pF
c2 5 0 .10pF
c3 6 0 .10pF
.ENDS DFFLOP

.SUBCKT INVERTER 2 3 1
M1 1 2 3 1 PCHAN W=15U L=2U AD=75p AS=75p
M2 3 2 0 0 NCHAN W=6U L=2U AD=30p AS=30p
.ENDS INVERTER

.SUBCKT NOR 2 3 4 1
M1 1 2 5 1 PCHAN W=25U L=2U AD=125p AS=125p
M2 5 3 4 1 PCHAN W=25U L=2U AD=125p AS=125p
M3 4 2 0 0 NCHAN W=6U L=2U AD=30p AS=30p
M4 4 3 0 0 NCHAN W=6U L=2U AD=30p AS=30p
C1 5 0 50fF
.ENDS NOR

.SUBCKT CINV 2 3 4 5 1
M1 1 2 6 1 PCHAN W=15U L=2U AD=75p AS=75p
M2 6 3 5 1 PCHAN W=15U L=2U AD=75p AS=75p
M3 5 4 7 0 NCHAN W=6U L=2U AD=30p AS=30p
M4 7 2 0 0 NCHAN W=6U L=2U AD=30p AS=30p
C1 6 0 50FF
C2 7 0 50FF
.ENDS CINV

.SUBCKT CINV2 2 3 4 5 1
M1 1 2 6 1 PCHAN W=6U L=2U AD=30p AS=30p
M2 6 3 5 1 PCHAN W=6U L=2U AD=30p AS=30p
M3 5 4 7 0 NCHAN W=6U L=2U AD=30p AS=30p
M4 7 2 0 0 NCHAN W=6U L=2U AD=30p AS=30p
C1 6 0 50FF
C2 7 0 50FF
.ENDS CINV2

.SUBCKT OR 2 3 4 1
X1 2 3 5 1 NOR
X2 5 4 1 INVERTER
C1 5 0 .10pF
.ENDS OR

.SUBCKT NAND 2 3 4 1
M1 1 2 4 1 PCHAN W=10U L=2U AD=50p AS=50p
M2 1 3 4 1 PCHAN W=10U L=2U AD=50p AS=50p
M3 4 2 5 0 NCHAN W=9U L=2U AD=45p AS=45p
M4 5 3 0 0 NCHAN W=9U L=2U AD=45p AS=45p
```

```
C1 5 0 10FF
.ENDS NAND

.SUBCKT AND 2 3 4 1
X1 2 3 5 1 NAND
X2 5 4 1 INVERTER
C1 5 0 .10pF
.ENDS AND


* Level 4 Model
.model pchan pmos level=4
+ vfb = -.49449 lvfb = .0473111 wvfb = -.078748
+ phi = .711038 lphi = 0 wphi = 0
+ k1 = .549022 lk1 = -.1098 wk1 = .211133
+ k2 = .0225369 lk2 = .0133462 wk2 = .0214418
+ eta = -.011378 leta = .0599553 weta = .0109074
+ muz = 173.524 dl = .502141 dw = -.20323
+ u0 = .129663 lu0 = .0395758 wu0 = -.089559
+ u1 = .0282132 lu1 = .288861 wu1 = -.13103
+ x2mz = 7.49207 lx2mz = -3.3077 wx2mz = 4.43137
+ x2e = -.00081113 lx2e = -.0023066 wx2e = -.0029608
+ x3e = .000855699 lx3e = -.003979 wx3e = -.00061957
+ x2u0 = .00634967 lx2u0 = -.0021908 wx2u0 = .00304801
+ x2u1 = .000525933 lx2u1 = .00057697 wx2u1 = .00896684
+ mus = 187.23 lmus = 89.9055 wmus = -19.539
+ x2ms = 7.00102 lx2ms = -.47434 wx2ms = 8.73424
+ x3ms = -.14304 lx3ms = 11.6728 wx3ms = -7.9883
+ x3u1 = -.016595 lx3u1 = .00351738 wx3u1 = .00384252
+ tox = .028 temp = 27 vdd = 5
+ cgdo = 3.09624e-10 cgso = 3.09624e-10 cgbo = -2.50626e-10
+ xpart = 1
+ n0 = 1 ln0 = 0 wn0 = 0
+ nb = 0 lnb = 0 wnb = 0
+ nd = 0 lnd = 0 wnd = 0
+ rsh = 20.58 cj = .0004015 cjsw = 5.023e-10
+ js = 1.e-08 pb = .8 pbsw = .51
+ mj = .4465 mjsw = .2705 wdf = 0
+ dell = 0
.model nchan nmos level=4
+ vfb = -.78837 lvfb = -.021873 wvfb = -.12029
+ phi = .801437 lphi = 0 wphi = 0
+ k1 = 1.05382 lk1 = .0864105 wk1 = .588742
+ k2 = -.0087349 lk2 = .0845206 wk2 = .0774966
+ eta = -.0025165 leta = .00946697 weta = .00706382
+ muz = 431.198 dl = .7921 dw = -.11735
+ u0 = .051871 lu0 = .0428904 wu0 = -.035902
+ u1 = .0252047 lu1 = .608867 wu1 = -.34032
+ x2mz = 11.1852 lx2mz = -22.808 wx2mz = 38.2982
+ x2e = -.00020831 lx2e = -.0062271 wx2e = -.00071188
+ x3e = .000225369 lx3e = -.000686 wx3e = -.0042937
+ x2u0 = .00301681 lx2u0 = -.014095 wx2u0 = .0297249
```

```
+ x2ul = -.0021476 lx2ul = .00786076 wx2ul = .004818
+ mus = 412.323 lmus = 259.338 wmus = 37.6417
+ x2ms = 4.86473 lx2ms = -19.202 wx2ms = 69.3915
+ x3ms = -2.6586 lx3ms = 47.7003 wx3ms = -13.265
+ x3ul = -.002006 lx3ul = .0668089 wx3ul = -.019504
+ tox = .028 temp = 27 vdd = 5
+ cgdo = 4.88415e-10 cgso = 4.88415e-10 cgbo = -1.44718e-10
+ xpart = 1
+ n0 = 1 ln0 = 0 wn0 = 0
+ nb = 0 lnb = 0 wnb = 0
+ nd = 0 lnd = 0 wnd = 0
+ rsh = 20.58 cj = .0004015 cjsw = 5.023e-10
+ js = 1.e-08 pb = .8 pbsw = .51
+ mj = .4465 mjsw = .2705 wdf = 0
+ dell = 0
*
.OPTIONS DEFL=2U DEFW=6U DEFAS=45P DEFAD=45P
+ITL1=1500 ITL4=300 ABSTOL=100P VNTOL=100U CHGTOL=1E-12
+NOPAGE RELTOL=.004 CPTIME=15000
.END
```

```
PROJECT CIRCUIT FOR D/A CONVERTER SUBSYSTEM

* POWER SUPPLY AND INPUT VOLTAGES
VDD  1 0 DC 5V
VR   2 0 DC 10V
Vb   13 0 DC 0.0V
VG   20 0 DC  -4.0V
VIN1 31 0 PULSE(0 5 0NS .2NS .2NS   15NS 140NS)
VIN2 32 0 PULSE(0 5 15NS .2NS .2NS  15NS 120NS)
VIN3 33 0 PULSE(0 5 30NS .2NS .2NS 15NS 100NS)
VIN4 34 0 PULSE(0 5 45NS .2NS .2NS 15NS 100NS)
VIN5 35 0 PULSE(0 5 60NS .2NS .2NS 65NS 100NS)
VIN6 36 0 PULSE(0 5 75NS .2NS .2NS 45NS 100NS)
VIN7 37 0 PULSE(0 5 90NS .2NS .2NS 45NS 100NS)
VIN8 38 0 PULSE(0 5 105NS .2NS .2NS 15NS 100NS)
VAN 39 0 DC 0.30V

* CIRCUIT BEING ANALYZED

R1 3 0 10k
R2 3 4  5k
R3 4 5  5k
R4 5 6  5k
R5 6 7  5k
R6 7 8  5k
R7 8 9  5k
R8 9 10 5k
R9 10 0 10k
X1 31 10 2 1 SWITCH
X2 32 9 2 1 SWITCH
X3 33 8 2 1 SWITCH
X4 34 7 2 1 SWITCH
X5 35 6 2 1 SWITCH
X6 36 5 2 1 SWITCH
X7 37 4 2 1 SWITCH
X8 38 3 2 1 SWITCH
X9 39 10 12 14  0 20 1 COMPARATOR
*10 14 15 1 INV2
X10 14 15 1 INVERTER
*ic v(12)=3.5v

.SUBCKT SWITCH 2 6 4 1
R1 5 6 9.8k
X1 2 3 1 INVERTER
M1 4 3 5 1 PCHAN W=90U L=2U AD=450p AS=450p
M2 5 3 0 0 NCHAN W=30U L=2U AD=150p AS=150p
.ENDS SWITCH

.SUBCKT INVERTER 2 3 1
M1 1 2 3 1 PCHAN W=15U L=2U AD=75p AS=75p
M2 3 2 0 0 NCHAN W=6U L=2U AD=30p AS=30p
.ENDS INVERTER
```

```
.SUBCKT INV2 2 3 1
M1 1 2 3 1 PCHAN W=10U L=2U AD=75p AS=75p
M2 3 2 0 0 NCHAN W=6U L=2U AD=30p AS=30p
.ENDS INV2

.SUBCKT COMPARATOR 2 3 4 8 7 9 1
M3 1 5 5 1 PCHAN W=10U L=3U AD= 25p AS= 25p
M4 1 5 4 1 PCHAN W=10U L=3U AD= 25p AS= 25p
M6 1 4 8 1 PCHAN W=34U L=3U AD=130p AS=130p
M1 5 2 6 6 NCHAN W=15U L=4U AD=50p AS=50p
M2 4 3 6 6 NCHAN W=15U L=4U AD=50p AS=50p
M5 6 7 9 9 NCHAN W=10U L=4U AD=25p AS=25p
M7 8 7 9 9 NCHAN W=15U L=4U AD=50p AS=50p
.ENDS COMPARATOR


* Level 4 Model
.model pchan pmos level=4
+ vfb = -.49449 lvfb = .0473111 wvfb = -.078748
+ phi = .711038 lphi = 0 wphi = 0
+ k1 = .549022 lk1 = -.1098 wk1 = .211133
+ k2 = .0225369 lk2 = .0133462 wk2 = .0214418
+ eta = -.011378 leta = .0599553 weta = .0109074
+ muz = 173.524 dl = .502141 dw = -.20323
+ u0 = .129663 lu0 = .0395758 wu0 = -.089559
+ u1 = .0282132 lu1 = .288861 wu1 = -.13103
+ x2mz = 7.49207 lx2mz = -3.3077 wx2mz = 4.43137
+ x2e = -.00081113 lx2e = -.0023066 wx2e = -.0029608
+ x3e = .000855699 lx3e = -.003979 wx3e = -.00061957
+ x2u0 = .00634967 lx2u0 = -.0021908 wx2u0 = .00304801
+ x2u1 = .000525933 lx2u1 = .00057697 wx2u1 = .00896684
+ mus = 187.23 lmus = 89.9055 wmus = -19.539
+ x2ms = 7.00102 lx2ms = -.47434 wx2ms = 8.73424
+ x3ms = -.14304 lx3ms = 11.6728 wx3ms = -7.9883
+ x3u1 = -.016595 lx3u1 = .00351738 wx3u1 = .00384252
+ tox = .028 temp = 27 vdd = 5
+ cgdo = 3.09624e-10 cgso = 3.09624e-10 cgbo = -2.50626e-10
+ xpart = 1
+ n0 = 1 ln0 = 0 wn0 = 0
+ nb = 0 lnb = 0 wnb = 0
+ nd = 0 lnd = 0 wnd = 0
+ rsh = 20.58 cj = .0004015 cjsw = 5.023e-10
+ js = 1.e-08 pb = .8 pbsw = .51
+ mj = .4465 mjsw = .2705 wdf = 0
+ dell = 0
.model nchan nmos level=4
+ vfb = -.78837 lvfb = -.021873 wvfb = -.12029
+ phi = .801437 lphi = 0 wphi = 0
+ k1 = 1.05382 lk1 = .0864105 wk1 = .588742
+ k2 = -.0087349 lk2 = .0845206 wk2 = .0774966
+ eta = -.0025165 leta = .00946697 weta = .00706382
+ muz = 431.198 dl = .7921 dw = -.11735
```

```
+ u0 = .051871 lu0 = .0428904 wu0 = -.035902
+ ul = .0252047 lul = .608867 wul = -.34032
+ x2mz = 11.1852 lx2mz = -22.808 wx2mz = 38.2982
+ x2e = -.00020831 lx2e = -.0062271 wx2e = -.00071188
+ x3e = .000225369 lx3e = -.000686 wx3e = -.0042937
+ x2u0 = .00301681 lx2u0 = -.014095 wx2u0 = .0297249
+ x2ul = -.0021476 lx2ul = .00786076 wx2ul = .004818
+ mus = 412.323 lmus = 259.338 wmus = 37.6417
+ x2ms = 4.86473 lx2ms = -19.202 wx2ms = 69.3915
+ x3ms = -2.6586 lx3ms = 47.7003 wx3ms = -13.265
+ x3ul = -.002006 lx3ul = .0668089 wx3ul = -.019504
+ tox = .028 temp = 27 vdd = 5
+ cgdo = 4.88415e-10 cgso = 4.88415e-10 cgbo = -1.44718e-10
+ xpart = 1
+ n0 = 1 ln0 = 0 wn0 = 0
+ nb = 0 lnb = 0 wnb = 0
+ nd = 0 lnd = 0 wnd = 0
+ rsh = 20.58 cj = .0004015 cjsw = 5.023e-10
+ js = 1.e-08 pb = .8 pbsw = .51
+ mj = .4465 mjsw = .2705 wdf = 0
+ dell = 0
*
.OPTIONS DEFL=2U DEFW=6U DEFAS=45P DEFAD=45P
+ITL1=1500 ITL4=300 ABSTOL=100P VNTOL=100U CHGTOL=1E-12
+NOPAGE RELTOL=.004 CPTIME=15000
.END
```

```
PROJECT CIRCUIT FOR COMPARATOR SUBSYSTEM

* POWER SUPPLY AND INPUT VOLTAGES
VDD  1 0 DC 5V
V3   3 0 DC 1.15V
*IN1 3 0 PULSE(0 5 5NS .2NS .2NS 5NS 10NS)
VIN2 2 0 PULSE(1.0 1.3 0NS .2NS .2NS 20NS 60NS)

* CIRCUIT BEING ANALYZED

X9 2 3 4 1 COMPARATOR
*ic v(4)=0

.SUBCKT SWITCH 2 6 4 1
R1 5 6 9.8k
X1 2 3 1 INVERTER
M1 4 3 5 1 PCHAN W=90U L=2U AD=450p AS=450p
M2 5 3 0 0 NCHAN W=30U L=2U AD=150p AS=150p
.ENDS SWITCH

.SUBCKT INVERTER 2 3 1
M1 1 2 3 1 PCHAN W=15U L=2U AD=75p AS=75p
M2 3 2 0 0 NCHAN W=6U L=2U AD=30p AS=30p
.ENDS INVERTER

.SUBCKT COMPARATOR 2 3 4 1
M1 1 5 5 1 PCHAN W= 6U L=2U AD= 30p AS=30p
M2 1 5 4 1 PCHAN W= 6U L=2U AD= 30p AS=30p
M3 5 2 0 0 NCHAN W=50U L=2U AD=250p AS=250p
M4 4 3 0 0 NCHAN W=50U L=2U AD=250p AS=250p
C1 5 0 50ff
.ENDS COMPARATOR


* Level 4 Model
.model pchan pmos level=4
+ vfb = -.49449 lvfb = .0473111 wvfb = -.078748
+ phi = .711038 lphi = 0 wphi = 0
+ k1 = .549022 lk1 = -.1098 wk1 = .211133
+ k2 = .0225369 lk2 = .0133462 wk2 = .0214418
+ eta = -.011378 leta = .0599553 weta = .0109074
+ muz = 173.524 dl = .502141 dw = -.20323
+ u0 = .129663 lu0 = .0395758 wu0 = -.089559
+ u1 = .0282132 lu1 = .288861 wu1 = -.13103
+ x2mz = 7.49207 lx2mz = -3.3077 wx2mz = 4.43137
+ x2e = -.00081113 lx2e = -.0023066 wx2e = -.0029608
+ x3e = .000855699 lx3e = -.003979 wx3e = -.00061957
+ x2u0 = .00634967 lx2u0 = -.0021908 wx2u0 = .00304801
+ x2u1 = .000525933 lx2u1 = .00057697 wx2u1 = .00896684
+ mus = 187.23 lmus = 89.9055 wmus = -19.539
+ x2ms = 7.00102 lx2ms = -.47434 wx2ms = 8.73424
+ x3ms = -.14304 lx3ms = 11.6728 wx3ms = -7.9883
```

```
+ x3ul = -.016595 lx3ul = .00351738 wx3ul = .00384252
+ tox = .028 temp = 27 vdd = 5
+ cgdo = 3.09624e-10 cgso = 3.09624e-10 cgbo = -2.50626e-10
+ xpart = 1
+ n0 = 1 ln0 = 0 wn0 = 0
+ nb = 0 lnb = 0 wnb = 0
+ nd = 0 lnd = 0 wnd = 0
+ rsh = 20.58 cj = .0004015 cjsw = 5.023e-10
+ js = 1.e-08 pb = .8 pbsw = .51
+ mj = .4465 mjsw = .2705 wdf = 0
+ dell = 0
.model nchan nmos level=4
+ vfb = -.78837 lvfb = -.021873 wvfb = -.12029
+ phi = .801437 lphi = 0 wphi = 0
+ k1 = 1.05382 lk1 = .0864105 wk1 = .588742
+ k2 = -.0087349 lk2 = .0845206 wk2 = .0774966
+ eta = -.0025165 leta = .00946697 weta = .00706382
+ muz = 431.198 dl = .7921 dw = -.11735
+ u0 = .051871 lu0 = .0428904 wu0 = -.035902
+ u1 = .0252047 lu1 = .608867 wu1 = -.34032
+ x2mz = 11.1852 lx2mz = -22.808 wx2mz = 38.2982
+ x2e = -.00020831 lx2e = -.0062271 wx2e = -.00071188
+ x3e = .000225369 lx3e = -.000686 wx3e = -.0042937
+ x2u0 = .00301681 lx2u0 = -.014095 wx2u0 = .0297249
+ x2u1 = -.0021476 lx2u1 = .00786076 wx2u1 = .004818
+ mus = 412.323 lmus = 259.338 wmus = 37.6417
+ x2ms = 4.86473 lx2ms = -19.202 wx2ms = 69.3915
+ x3ms = -2.6586 lx3ms = 47.7003 wx3ms = -13.265
+ x3u1 = -.002006 lx3u1 = .0668089 wx3u1 = -.019504
+ tox = .028 temp = 27 vdd = 5
+ cgdo = 4.88415e-10 cgso = 4.88415e-10 cgbo = -1.44718e-10
+ xpart = 1
+ n0 = 1 ln0 = 0 wn0 = 0
+ nb = 0 lnb = 0 wnb = 0
+ nd = 0 lnd = 0 wnd = 0
+ rsh = 20.58 cj = .0004015 cjsw = 5.023e-10
+ js = 1.e-08 pb = .8 pbsw = .51
+ mj = .4465 mjsw = .2705 wdf = 0
+ dell = 0
*
.OPTIONS DEFL=2U DEFW=6U DEFAS=45P DEFAD=45P
+ITL1=1500 ITL4=300 ABSTOL=100P VNTOL=100U CHGTOL=1E-12
+NOPAGE RELTOL=.004 CPTIME=15000
.END
```

```
PROJECT CIRCUIT FOR CLOCK SUBSYSTEM

* POWER SUPPLY AND INPUT VOLTAGES
VDD  1 0 DC 5V
*IN1 2 0 PULSE(0 5 40NS .20NS .20NS 30NS 60NS)

* CIRCUIT BEING ANALYZED
R1 1 2 1k
R2 2 3 2k
Ra 1 4 50K
Rb 4 5 50K
Rc 5 0 50K
X1 3 4 6 1 COMPARATOR
X2 5 3 7 1 COMPARATOR
X3 0 6 9 8 1 NOR
X4 0 7 8 9 1 NOR
X5 8 10 1 INVERTER
X6 10 11 1 INVERTER
C1 3 0 10nF
C2 2 0 1pF
C3 4 0 1pF
C4 5 0 1pF
C5 6 0 1pF
C6 7 0 1pF
C7 8 0 1pF
C8 9 0 1pF
C10 10 0 1pF
C11 11 0 1pF
M1 2 10 0 0 NCHAN W=90U L=2U AD=270p AS=270p

.ic v(2)=5 v(3)=5 v(4)=3.3 v(5)=1.67 v(6)=0 v(7)=0
.ic v(8)=5 v(9)=0 v(10)=0

.SUBCKT COMPARATOR 2 3 4 1
M1 1 5 5 1 PCHAN W=12U L=2U AD= 60p AS= 60p
M2 1 5 4 1 PCHAN W=12U L=2U AD= 60p AS= 60p
M3 5 2 0 0 NCHAN W=4U L=2U AD=20p AS=20p
M4 4 3 0 0 NCHAN W=4U L=2U AD=20p AS=20p
.ENDS COMPARATOR

.SUBCKT INVERTER 2 3 1
M1 1 2 3 1 PCHAN W=15U L=2U AD=75p AS=75p
M2 3 2 0 0 NCHAN W=6U L=2U AD=30p AS=30p
.ENDS INVERTER

.SUBCKT NOR 2 3 4 5 1
M1 1 2 6 1 PCHAN W=12U L=2U AD= 60p AS= 60p
M2 6 3 7 1 PCHAN W=12U L=2U AD= 60p AS= 60p
M3 7 4 5 1 PCHAN W=12U L=2U AD= 60p AS= 60p
M4 5 2 0 0 NCHAN W=6U L=2U AD=30p AS=30p
M5 5 3 0 0 NCHAN W=6U L=2U AD=30p AS=30p
M6 5 4 0 0 NCHAN W=6U L=2U AD=30p AS=30p
```

```
.ENDS NOR


* Level 4 Model
.model pchan pmos level=4
+ vfb = -.49449 lvfb = .0473111 wvfb = -.078748
+ phi = .711038 lphi = 0 wphi = 0
+ k1 = .549022 lk1 = -.1098 wk1 = .211133
+ k2 = .0225369 lk2 = .0133462 wk2 = .0214418
+ eta = -.011378 leta = .0599553 weta = .0109074
+ muz = 173.524 dl = .502141 dw = -.20323
+ u0 = .129663 lu0 = .0395758 wu0 = -.089559
+ u1 = .0282132 lu1 = .288861 wu1 = -.13103
+ x2mz = 7.49207 lx2mz = -3.3077 wx2mz = 4.43137
+ x2e = -.00081113 lx2e = -.0023066 wx2e = -.0029608
+ x3e = .000855699 lx3e = -.003979 wx3e = -.00061957
+ x2u0 = .00634967 lx2u0 = -.0021908 wx2u0 = .00304801
+ x2u1 = .000525933 lx2u1 = .00057697 wx2u1 = .00896684
+ mus = 187.23 lmus = 89.9055 wmus = -19.539
+ x2ms = 7.00102 lx2ms = -.47434 wx2ms = 8.73424
+ x3ms = -.14304 lx3ms = 11.6728 wx3ms = -7.9883
+ x3u1 = -.016595 lx3u1 = .00351738 wx3u1 = .00384252
+ tox = .028 temp = 27 vdd = 5
+ cgdo = 3.09624e-10 cgso = 3.09624e-10 cgbo = -2.50626e-10
+ xpart = 1
+ n0 = 1 ln0 = 0 wn0 = 0
+ nb = 0 lnb = 0 wnb = 0
+ nd = 0 lnd = 0 wnd = 0
+ rsh = 20.58 cj = .0004015 cjsw = 5.023e-10
+ js = 1.e-08 pb = .8 pbsw = .51
+ mj = .4465 mjsw = .2705 wdf = 0
+ dell = 0
.model nchan nmos level=4
+ vfb = -.78837 lvfb = -.021873 wvfb = -.12029
+ phi = .801437 lphi = 0 wphi = 0
+ k1 = 1.05382 lk1 = .0864105 wk1 = .588742
+ k2 = -.0087349 lk2 = .0845206 wk2 = .0774966
+ eta = -.0025165 leta = .00946697 weta = .00706382
+ muz = 431.198 dl = .7921 dw = -.11735
+ u0 = .051871 lu0 = .0428904 wu0 = -.035902
+ u1 = .0252047 lu1 = .608867 wu1 = -.34032
+ x2mz = 11.1852 lx2mz = -22.808 wx2mz = 38.2982
+ x2e = -.00020831 lx2e = -.0062271 wx2e = -.00071188
+ x3e = .000225369 lx3e = -.000686 wx3e = -.0042937
+ x2u0 = .00301681 lx2u0 = -.014095 wx2u0 = .0297249
+ x2u1 = -.0021476 lx2u1 = .00786076 wx2u1 = .004818
+ mus = 412.323 lmus = 259.338 wmus = 37.6417
+ x2ms = 4.86473 lx2ms = -19.202 wx2ms = 69.3915
+ x3ms = -2.6586 lx3ms = 47.7003 wx3ms = -13.265
+ x3u1 = -.002006 lx3u1 = .0668089 wx3u1 = -.019504
+ tox = .028 temp = 27 vdd = 5
+ cgdo = 4.88415e-10 cgso = 4.88415e-10 cgbo = -1.44718e-10
```

```
+ xpart = 1
+ n0 = 1 ln0 = 0 wn0 = 0
+ nb = 0 lnb = 0 wnb = 0
+ nd = 0 lnd = 0 wnd = 0
+ rsh = 20.58 cj = .0004015 cjsw = 5.023e-10
+ js = 1.e-08 pb = .8 pbsw = .51
+ mj = .4465 mjsw = .2705 wdf = 0
+ dell = 0
*
.OPTIONS DEFL=2U DEFW=6U DEFAS=45P DEFAD=45P
+ITL1=1500 ITL4=300 ABSTOL=100P VNTOL=100U CHGTOL=1E-12
+NOPAGE RELTOL=.004 CPTIME=15000
.END
```

APPENDIX D. Non-Photosensitive Polyimide Application and Patterning

Equipment:

Convection bake oven, Watlow Series 700, Winona, MN 55987

Mask aligner, Karl-Suss America MJB-UV300, Waterbury VT 05677

Photoresist spinner, Headway Research 1-EC101D-R485, Garland TX 75042

Optical microscope, Wild Heerbrugg 20, Heerburg, Switzerland

Profilometer, Sloan Technology Dek-Tak II-A, Santa Barbara, CA 93103

Consummables:

Ultradel A/B 200 adhesion promoter solution, Amoco Chemical, Chicago IL 60601

Ultradel 4212 polyimide

Ultradel E113 polyimide etchant

Shipley 1815 positive photoresist, Shipley, Whitehall PA 18052

Shipley 303A photoresist developer

Materials:

3 inch diameter, n-doped, prime (100) silicon wafers, Ziti Inc

Photomask, Eastman Kodak AA1G1 type 1A, Rochester NY 14650

(1) The wafers were baked in the convection oven at 200°C for a minimum of two hours to remove surface moisture.

(2) Each wafer was placed on the photoresist spinner vacuum chuck.

(3) After approximately 2 ml of the adhesion promotor was placed on the wafer's center and allowed to spread for 15 seconds, the wafer was spun for 30 seconds at 4000 rpm.

(4) After approximately 5 ml of polyimide was placed on the wafer's center, the wafer was spun, first for 15 seconds at 500 rpm, then ramped up to 1000 rpm for 15 seconds, and finally ramped up to 2500 rpm for 30 seconds. This process produced a final polyimide thickness of 10 microns.

(5) The wafer was placed in a petri dish, which was then placed in the convection oven for 10 minutes. The temperature of the oven during this step was varied to control the polyimide via side wall slopes.

(6) Shipley 1815 photoresist was applied and patterned on the polyimide surface using the procedures described in Appendix O. Note that the photoresist hardbake step was not required for processing the polyimide.

(7) After developing the photoresist pattern, the polyimide was etched on the photoresist spinner using the following spray schedule:

(a) Ultradel etchant, 45 seconds at 500 rpm,
(b) Ultradel etchant, 5 seconds at 4000 rpm,
(c) Ultradel etchant, 5 seconds at 500 rpm,
(d) Ultradel etchant, 5 seconds at 4000 rpm,
(e) DIW, 15 seconds at 500 rpm, and
(f) dry, 30 seconds at 4000 rpm.

(8) The etched polyimide pattern was inspected under the optical microscope, and a micrometer was used to determine via depth.

(9) The photoresist layer was stripped off the wafer using the procedures described in Appendix O.

APPENDIX E. Metallization Application and Patterning

Equipment:

Aluminum evaporation deposition system, Denton Vacuum DV-602, Cherry Hill, NJ

Hot plate, Thermolyne HP11415B, Dubuque, IA, 52004

Glass beaker

Pyrex thermometer

Polyethylene wafer holder

Consummables:

Aluminum wire

Source boats

Glacial acetic acid (CH_3COOH)

Phosphoric acid (H_3PO_4)

Nitric acid (HNO_3)

Materials:

3 inch diameter, n-doped, prime (100) silicon wafers, Ziti Inc

Photomask, Eastman Kodak AA1G1 type 1A, Rochester NY 14650

(1) The wafers and aluminum sources were mounted in the evaporation chamber, which was then closed and evacuated to a vacuum level of $2 \cdot 10^{-5}$ microns of mercury.

(2) The aluminum was heated and evaporated onto the wafer surfaces at a rate of 2 to 5 angstroms per second as measured by the Maxtek TM-100R thickness monitor crystal located in the evaporation chamber. Deposition was continued until a 12000 angstrom film thickness was measured by the sensor.

(3) The aluminum heat source was removed, the chamber was vented, and the wafers were removed.

(4) The Shipley 1815 positive photoresist was applied and patterned on the metallized surfaces using the procedures outlined in Appendix N.

(5) In a glass beaker, 400 ml of acetic acid, 400 ml of phosphoric acid, 100 ml of nitric acid and 100 ml of deionized water were mixed to produce the etchant.

(6) The beaker was placed on the hot plate to heat the etchant to the appropriate temperature (30-35°C for the wafers coated with the Ultradel 4212 polyimide, 40-45°C for all other wafers).

(7) A wafer with the photoresist pattern was immersed in the etchant and visually monitored until the exposed aluminum was removed.

(8) The photoresist pattern was stripped off using the procedure outlined in Appendix O.

APPENDIX F. Photosensitive Polyimide Application and Patterning

Equipment:

Convection bake oven, Watlow Series 700, Winona, MN 55987

Mask aligner, Karl-Suss America MJB-UV300, Waterbury VT 05677

Photoresist spinner, Headway Research 1-EC101D-R485, Garland TX 75042

Optical microscope, Wild Heerbrugg 20, Heerburg, Switzerland

Profilometer, Sloan Technology Dek-Tak II-A, Santa Barbara, CA 93103

Consummables:

Ultradel A/B 200 adhesion promoter solution

Ultradel 7501 polyimide

Ultradel D750 polyimide developer

Ultradel R750 polyimide rinse, Amoco Chemical, Chicago IL 60601

Selectilux HTR AP-3 adhesion promoter

Selectilux HTR 3-200 polyimide

Selectiplast D-2 polyimide developer, Ciba Geigy, Santa Clara CA, 95054

Isopropyl Alcohol

Materials:

3 inch diameter, n-doped, prime (100) silicon wafers, Ziti Inc

Photomask, Eastman Kodak AA1G1 type 1A, Rochester NY 14650

(1) The wafers were baked in the convection oven at 200°C for a minimum of two hours to remove surface moisture.

(2) The two photosensitive polyimides were applied and patterned using the same procedure. This procedure is outlined in the table below.

(8) The etched polyimide pattern was visually inspected under the optical microscope, and via depth was measured using the stylus profilometer.

Polyimide	Selectilux HTR3-200	Ultradel 7501
Adhesion Promoter:	Selectiplast AP-3 (diluted)	Ultradel A/B 200
Flood Time (sec)	5	5
Speed/Time (RPM/sec)	3000 / 60	4000 / 30
Polyimide Spin Coating:		500 / 30
Speed/Time (RPM/sec)	2000 / 20	1500 / 30
Softbake:		
Temp/Time (°C/min)	65 / 120	105/ 10
Exposure Time (min)	1.5	0.75
Development:		
Developer:	Selectiplast D-2	Ultradel D750
Speed/Time (RPM/sec)	500 / 30	1000 / 120
Overlap:		
Speed/Time (RPM/sec)	500 / 10	1000 / 10
Rinse:	2-Propanol	Ultradel R750
Speed/Time (RPM/sec)	500 / 10	1000 / 15
Dry:		
Speed/Time (RPM/sec)	3000 / 30	3000 / 30

APPENDIX G. Photomask Design and Production

Equipment:

Sun workstation

Coordinatograph machine, Spaulding Instruments 1020-4,
    Pasadena CA

Reduction camera, HLC Engineering 6720P DEKACON III,
    Oreland PA

- 3 inch Wray lens (20X reduction)
- 35 mm Wray lens (50X reduction)

Mask duplicating camera, Ultratech 1500, Sunnyvale CA
    94086

Optical microscope, Wild Heerbrugg 20, Heerburg, Switzerland

Consummables:

Kodak D-8 developer bath

Kodak stop bath

Kodak fix bath

Materials:

Rubylith (40 inch wide)

Kodak 4 by 4 inch High Resolution Photoplates (HRP),
    Eastman Kodak AA1G1 type 1A, Rochester NY 14650

Rubylith Mask Processing

(1) Each mask was designed using the MAGIC circuit layout CAD tool on the Sun workstation.

(2) The mask design was realized as a set of coordinates in microns for the mask openings.

(3) The coordinates were converted to mils for compatibility with the coordinatograph machine, and multiplied by the reduction factor (20 or 50).

(4) The modified coordinates were used to cut the mask image in rubylith on the coordinatograph machine.

HRP Processing

(5) The rubylith pattern was attached to the light screen for the reduction camera.

(6) The appropriate lens was mounted on the camera box, which was located and adjusted to provide the proper image reduction and focus.

'7) The mask pattern was transferred to the HRP using a 7 minute exposure with an F-stop of 8 for the 50X images, and a 2 minute exposure with an F-stop of 2 for the 20X images.

(8) Each HRP image was then developed by immersion into the following baths:

(a) developer solution for 4 minutes,
(b) stop bath solution for 1 minute,
(c) fix bath solution for 1 minute, and
(d) deionized water for 5 minutes.

(9) The HRP was dried using a nitrogen gas purge.

(10) The HRP image was inspected under the optical microscope for image sharpness and contrast.

HRP Copy Processing

(11) The HRP to be copied was placed in the Master HRP holder in the mask duplicating camera.

(12) A blank HRP was placed in the Copy holder of the duplicating machine.

(13) The HRP image was transferred using an 8 second exposure in the duplicating machine.

(14) The HRP with the reverse image was developed by repeating steps 8 through 10 in the HRP processing schedule.

APPENDIX H. Wafer Oxidation

Equipment:

Thermal oxidation furnace, Thermco 4100, Orange CA 92667

Bubbler

Quartz wafer boat

Micrometer, Ash Precision Equipment 7-1800, Detroit MI 48208

Consummables:

Oxygen gas (O_2)

Nitrogen gas (N_2)

Deionized water

Materials:

3 inch diameter, n-doped, prime silicon (100) wafers, Ziti Inc

(1) The furnace's oxidation tube was set to 1050°C and allowed to stabilize at that temperature.

(2) The wafers to be oxidized were arranged in the quartz boat.

(3) O_2 flow was begun in the furnace oxidation tube.

(4) The boat was slowly advanced (one inch per minute) through zone one in the oxidation tube.

(5) The quartz boat was then centered in the furnace tube.

(6) After the boat had been in the furnace's central zone for 15 minutes, the atmosphere in the furnace tube was switched from a dry

O_2 atmosphere to a steam atmosphere.

(7) The steam atmosphere was maintained for 20 hours, requiring that the bubbler supply be refilled at the seven and fourteen hour points.

(8) After 20 hours, the atmosphere in the furnace tube was switched from the steam atmosphere to the dry O_2 atmosphere for approximately 15 minutes.

(9) The quartz boat holding the oxidized wafers was drawn back to the near edge of zone two, and then slowly pulled (one inch per minute) back through zone one.

(10) The boat with the wafers was removed from the oxidation tube and allowed to cool to room temperature.

APPENDIX I. Negative Photoresist Masking

Equipment:

Convection bake oven, Watlow Series 700, Winona, MN 55987

Mask aligner, Karl-Suss America MJB-UV300, Waterbury VT 05677

Photoresist spinner, Headway Research 1-EC101D-R485, Garland TX 75042

Optical microscope, Wild Heerbrugg 20, Heerburg, Switzerland

Consummables:

Waycoat HR200 negative photoresist, Olin Hunt, West Patterson NJ, 07424

Xylene

Butyl acetate

Materials:

3 inch diameter, n-doped, prime (100) silicon wafers, Ziti Inc

Photomask, Eastman Kodak AA1G1 type 1A, Rochester NY 14650

(1) The wafers were cleaned using the process described in Appendix K.

(2) The wafers were baked in the convection oven at 200°C for at least two hours to remove all moisture.

(3) Each wafer was individually placed on the photoresist spinner's vacuum chuck.

(4) After approximately 2 ml of the photoresist was dispensed on the wafer's center, the wafer was spun for 30 seconds at 4000 rpm, which produced a hardbaked image thickness of 0.8 microns.

(5) The wafers were placed in the convection oven for 15 minutes at 75°C to harden the photoresist's surface.

(6) The appropriate photomask was placed in the mask aligner with its emulsion side facing down.

(7) Each wafer was individually placed on the mask aligner's vacuum chuck, and aligned with the mask image. After alignment, the wafer and mask were brought into contact.

(8) The wafer was exposed in the mask aligner for approximately 60 seconds.

(9) The photoresist image was developed after placing the wafer on the photoresist spinner using the following spray schedule:

(a) xylene, 30 seconds at 500 rpm,
(b) butyl acetate, 30 seconds at 500 rpm, and
(c) dry, 30 seconds at 4000 rpm.

(10) The photoresist image was inspected under the optical microscope.

(11) Wafers with acceptable photoresist patterns were placed in the convection oven at 135°C for 20 minutes to harden the image.

(12) The photoresist image was stripped from the wafer's surface using the cleaning process described in Appendix K.

APPENDIX J. Oxide Etching

Equipment:

Convection bake oven, Watlow Series 700, Winona, MN 55987

One liter polypropylene beaker

Polypropylene wafer holder

Recirculating water bath

Consummables:

Ammonium fluoride (NH_4F)

Hydrofluoric Acid (HF)

Materials:

3 inch diameter, n-doped, prime (100) silicon wafers, Ziti Inc

(1) A buffered HF solution composed of 600 ml of NH_4F and 150 ml of HF was mixed in a polypropylene beaker and allow to stabilize for two hours.

(2) The wafers, arranged in a polypropylene wafer holder, were immersed in the buffered HF solution for 5 minutes.

(3) The polypropylene wafer holder and the wafers were rinsed in deionized water for 60 seconds and dried with a nitrogen gas purge.

(4) The color of the oxide in the etched areas was examined and compared with the oxide thickness color chart to estimate remaining oxide thickness.

(5) Steps (2) through (4) were repeated until no oxide remained in the regions being etched.

(6) The wafers were thoroughly rinsed in the water bath for 5 minutes.

(7) The wafers were placed in the convection oven at 200°C for at two hours to remove all moisture.

APPENDIX K. Wafer Cleaning

Equipment:

Glass beaker

Consummables:

Sulfuric acid (H_2SO_4)

Hydrogen peroxide (H_2O_2)

Materials:

3 inch diameter, n-doped, prime (100) silicon wafers, Ziti Inc

(1) The cleaning solution composed of 900 ml of H_2SO_4 and 600 ml of H_2O_2 was mixed in a glass beaker.

(2) The wafers were placed in a propylene holder which was then immersed in the cleaning solution for 20 minutes.

(3) The polypropylene holder and wafers were removed from the cleaning solution and rinsed thoroughly in DIW for ten minutes.

(4) The wafers were dried using a nitrogen purge.

APPENDIX L. IC Die Cavity Etching

Equipment:

Recirculating water bath

Polypropylene beaker and wafer holder

Optical microscope, Wild Heerbrugg 20, Heerburg, Switzerland

Micrometer, Ash Precision Equipment 7-1800, Detroit MI 48208

Consummables:

Potassium Hydroxide (KOH)

Hydrofluoric Acid (HF)

Materials:

3 inch diameter, n-doped, prime (100) silicon wafers with patterned oxide layer, Ziti Inc

(1) An etchant solution composed of 200 grams of KOH and 800 grams of DIW was mixed in a polypropylene beaker.

(2) The recirculating water bath, cooling water, and nitrogen supply were turned on.

(3) The recirculating water bath was allowed to stabilize at the desired etch temperature (typically 60°C to produce an etch rate of 0.43 microns per minute).

(4) The wafers to be etched were placed in the wafer holder, which was, in turn, immersed in the etchant.

(5) The beaker was transferred to the recirculating bath.

(6) To verify the etch rate during processing:

(a) The beaker was removed from the bath.

(b) The wafer holder was removed from the etchant and rinsed in DIW for two minutes.

(c) After drying with nitrogen gas, the thickness of the wafer inside and outside the etched cavity was measured with the micrometer.

(d) The wafers were then immersed in the etchant. The etchant beaker was then transferred to the recirculating water bath.

(7) After the etch process was complete, the etchant beaker was removed from the recirculating water bath, and the wafer holder was rinsed in DIW for two minutes.

(8) The quality and completeness of the wafer etch process was verified using the optical microscope.

(9) Any remaining oxide on the wafer surfaces was stripped by immersing them in a solution of 1:10, HF:DIW until the wafer surfaces became hydrophobic.

(10) The wafers were thoroughly rinsed in DIW and dried with nitrogen gas.

APPENDIX M. Substrate Pre-Assembly IC Die Mounting Procedure

Equipment:

Convection bake oven, Watlow Series 700, Winona, MN 55987
Hot plate, Thermolyne HP11415B, Dubuque IA, 52004
Weight scale, Setra 500L, Acton MA 01720
Wafer clamping jig
Petri dish
1.0 kg weight

Consummables:

Masterbond EP34CA epoxy (components A and B), Masterbond, Hackensack NJ, 07601
Teflon® spray, McMaster Carr 1039K16, Chicago IL, 60680
Acetone

Materials:

3 inch diameter, n-doped, prime (100) silicon wafers, Ziti Inc
IC die
Optical flats

(1) The epoxy components were measured on the weight scale. For a working mixture, 3.5 grams of component A and 7.0 grams of component B were mixed in a plastic cup.

(2) The petri dish was heated to 175°C on the hot plate and then removed.

(3) A small amount of the mixed epoxy was placed in the heated petri dish to increase its viscosity.

(4) A thin coating of the heated epoxy was applied to the nonplanar side of the etched host substrate.

(5) The host substrate was attached to the support substrate.

(6) An optical flat was placed on the hot plate, and the bonded substrates were placed on the optical flat with the IC die cavity face upwards.

(7) A second optical flat was placed on the substrate and a 1.0 kg weight was placed on the optical flat to provide a planarizing force.

(8) After ten minutes, the weight, optical flats and substrate were removed from the hot plate and allowed to cool.

(9) After cooling, excess epoxy was removed from the surfaces of the optical flats and the substrate with a cotton swab soaked with acetone. A cotton swab and acetone were also used to clean excess epoxy from the IC die cavity.

(10) The bonded substrate was placed on the hot plate between the two optical flats.

(11) The 1.0 kg weight was placed on the top optical flat, and the substrate was cured on the hot plate at 175°C for 50 minutes.

(12) The weight, top optical flat and the substrate was removed from the hot plate and allowed to cool.

(13) An array of small beads of epoxy were placed on the bottom of the IC die well using a microsyringe.

(14) The IC die was placed in the cavity, and the bonded substrates were placed on the optical flat on the hot plate, with the IC die facing upwards.

(15) A Teflon®-coated optical flat was placed on the substrate and a 1.0 kg weight was placed on top of the optical flat.

(16) Steps 8 through 12 were repeated to cure the epoxy.

(17) The WSI assembly was removed from the hot plate and placed in the programmable convection oven between two optical flats.

(18) The 1.0 kg weight was placed on the top optical flat to provide a planarizing force.

(19) The WSI assembly was baked in the convection oven using the following cure schedule:

  (a) 150°C for 1.5 hours,

  (b) 200°C for 1.5 hours,

  (c) 250°C for 4.0 hours, and

  (d) cool down to 70°C.

(20) Once the cure cycle was complete, the WSI assembly was removed from the convection oven and inspected.

APPENDIX N. Single-Step IC Die Mounting

Equipment:

Convection bake oven, Watlow Series 700, Winona, MN 55987

Hot plate, Thermolyne HP11415B, Dubuque IA, 52004

Weight scale, Setra 500L, Acton MA 01720

Petri dish

1.0 kg weight

Consummables:

Masterbond EP34CA epoxy (components A and B), Masterbond, Hackensack NJ, 07601

Teflon® spray, McMaster Carr 1039K16, Chicago IL, 60680

Acetone

Materials:

3 inch diameter, n-doped, prime (100) silicon wafers, Ziti Inc

IC die

Optical flats

(1) The epoxy components were measured on the weight scale. For a working mixture, 3.5 grams of component A and 7.0 grams of component B were mixed in a plastic cup.

(2) The petri dish was heated to 175°C on the hot plate and then removed.

(3) A small amount of the mixed epoxy was placed in the heated petri dish to increase its viscosity.

(4) An etched wafer was placed, planar surface down, on a Teflon®-coated optical flat, and IC die were placed, circuit side down, in the etched cavities.

(5) A thin coating of the heated epoxy was applied to one side of the support substrate wafer, which was attached to the etched wafer and IC die.

(6) The bonded wafers on top of the coated optical flat were placed on the hot plate, and a second optical flat was placed on the bonded wafers.

(7) After 10 minutes, the WSI assembly and optical flats were removed from the hot plate and allowed to cool.

(8) The surfaces of the WSI assembly and the optical flats were cleaned with acetone to remove excess epoxy.

(9) The WSI assembly was placed on the hot plate uncovered, circuit side facing upwards for additional curing of 2 minutes.

(10) After the WSI assembly cooled, the surface was re-cleaned with acetone to remove excess epoxy.

(11) The WSI assembly was placed on the hot plate between two optical flats.

(12) The 1.0 kg weight was placed on the optical flat to apply a planarizing force during the 60 minute cure at 175°C.

(13) The WSI assembly was removed from the hot plate and placed in the programmable convection oven between two optical flats.

(14) The 1.0 kg weight was placed on the top optical flat to provide a planarizing force.

(15) The WSI assembly was baked in the convection oven using the following cure schedule:

- (a) 150°C for 1.5 hours,
- (b) 200°C for 1.5 hours,
- (c) 250°C for 4.0 hours, and
- (d) cool down to 70°C.

(16) Once the cure cycle was complete, the WSI assembly was removed from the convection oven and inspected.

APPENDIX O. Positive Photoresist Masking

Equipment:

Convection bake oven, Watlow Series 700, Winona, MN 55987

Mask aligner, Karl-Suss America MJB-UV300, Waterbury VT 05677

Photoresist spinner, Headway Research 1-EC101D-R485, Garland TX 75042

Optical microscope, Wild Heerbrugg 20, Heerburg, Switzerland

Consummables:

Shipley 1815 positive photoresist

Shipley 303A photoresist developer, Shipley, Whitehall Pa 18052

Materials:

3 inch diameter, n-doped, prime (100) silicon wafers, Ziti Inc

Photomask, Eastman Kodak AA1G1 type 1A, Rochester NY 14650

(1) Each wafer was placed on the photoresist spinner's vacuum chuck.

(2) After approximately 2 ml of photoresist was dispensed on the wafer's center, the wafer was spun for 30 seconds at 4000 rpm, which produced a final imaging thickness of 1.5 microns.

(3) The wafers were baked in the convection oven for 30 minutes at 95°C to harden the photoresist's surface.

(4) The appropriate photomask was placed in the mask holder of the mask aligner.

(5) Each wafer was placed on the mask aligner's vacuum chuck, and aligned with mask image. After alignment, the wafer and mask were brought into contact.

(6) The wafer was exposed in the mask aligner for approximately 1.25 minutes.

(7) The photoresist image was developed after placing the wafer on the photoresist spinner using the following spray schedule:

(a) developer (1:10, Shipley 303A:DIW), 30 seconds at 500 rpm,

(b) DIW, 30 seconds at 500 rpm, and

(c) dry, 30 seconds at 4000 rpm.

(8) The photoresist image was inspected under the optical microscope.

(9) Wafers with acceptable photoresist patterns were placed in the convection oven at 105°C for 30 minutes to harden the image.

(10) To strip the photoresist layer, each wafer was placed in mask aligner.

(11) With no photomask inserted, and the aligner in its "Soft Contact" mode, the wafer was exposed for 1.5 minutes.

(7) The photoresist image was stripped after placing the wafer on the photoresist spinner using the following spraying schedule:

(a) developer (1:4, Shipley 303A:DIW), 30 seconds at 500 rpm,

(b) DIW, 30 seconds at 500 rpm, and

(c) dry, 30 seconds at 4000 rpm.

Appendix P. Data Acquisition Software

The following BASIC program was written to perform the data acquisition for the electrical characterization testing. This program was executed using QuickBasic running on a Z-248 computer.

```
' HSCOPE.TXT
'
'
' By Capt Philip C. Reamy and Craig S. Dyson
'
' Sets up and runs the HP 54100 O'scope in remote control,
' Downloads a trace from Channels 1 and 2
'
CLS
LOCATE 1, 1
PRINT "The HP 54100 Acquisition Program Is Running"
'
'
'####### Establish communications with device driver
###########
'
'
OPEN "$DV488" FOR OUTPUT AS #1    'HP Scope
PRINT #1, "BUFFERCLEAR"
OPEN "$DV488" FOR INPUT AS #2    'input from scope
ON ERROR GOTO 1540
'
'####### Initialize MBC-488 board using "SYSCON" command
########
'
PRINT #1, "SYSCON MAD1=3 CIC1=1 BA1=&H300"
DEV1% = 7
'
'####### Set HP Digitizing Oscilloscope into REMOTE
'
PRINT #1, "REMOTE", DEV1%
'
'####### Set TIMEOUT (timeout time=0.056 x A%)
################
'
450  'A% = 100
'PRINT #1, "OUTPUT ", DEV1%, " $ + TIMEOUT "; A$
'
LOCATE 3, 1
PRINT "Configuring the HP O'scope....."
     CMD$ = "STOP"
```

```
     PRINT #1, "OUTPUT ", DEV1%, " $ +", CMD$
     CMD$ = "RUN"
     PRINT #1, "OUTPUT ", DEV1%, " $ +", CMD$
     CMD$ = "DISPLAY BRIGHTNESS HIGH"
     PRINT #1, "OUTPUT ", DEV1%, " $ +", CMD$
     CMD$ = "DISPLAY GRAT GRID"
     PRINT #1, "OUTPUT ", DEV1%, " $ +", CMD$
     CMD$ = "CHANNEL 1"
     PRINT #1, "OUTPUT ", DEV1%, " $ +", CMD$
     CMD$ = "AUTOSCALE"
     PRINT #1, "OUTPUT ", DEV1%, " $ +", CMD$
LOCATE 5, 1
INPUT "Press (s) to store the data into the scope's Memory:
", D$
IF D$ = "s" THEN GOTO 880 ELSE GOTO 450
' 880  CMD$ = "STORE CHANNEL 1, MEMORY 1"
880  CMD$ = "DIGITIZE CHANNEL 1,2"
     PRINT #1, "OUTPUT ", DEV1%, " $ +", CMD$
LOCATE 7, 1
CLS
INPUT "Filename for data from scope's Memory 1: ", DF$
OPEN DF$ FOR OUTPUT AS #3
     CMD$ = "WAVEFORM SOURCE MEMORY 1 FORMAT ASCII"
     PRINT #1, "OUTPUT ", DEV1%, " $ +", CMD$
     R$ = SPACE$(15)
     CMD$ = "POINTS?"
     PRINT #1, "OUTPUT ", DEV1%, " $ +", CMD$
     PRINT #1, "ENTER 07 $ +"
     INPUT #2, R$
     PNTS = VAL(R$)
     LOCATE 9, 1
     PRINT "The number of points is: ", PNTS
     CMD$ = "YREF?"
     PRINT #1, "OUTPUT ", DEV1%, " $ +", CMD$
     PRINT #1, "ENTER 07 $ +"
     INPUT #2, R$
     YREF = VAL(R$)
     CMD$ = "YINC?"
     PRINT #1, "OUTPUT ", DEV1%, " $ +", CMD$
     PRINT #1, "ENTER 07 $ +"
     INPUT #2, R$
     YINC = VAL(R$)
     CMD$ = "YOR?"
     PRINT #1, "OUTPUT ", DEV1%, " $ +", CMD$
     PRINT #1, "ENTER 07 $ +"
     INPUT #2, R$
     YORG = VAL(R$)
     CMD$ = "XINC?"
     PRINT #1, "OUTPUT ", DEV1%, " $ +", CMD$
     PRINT #1, "ENTER 07 $ +"
     INPUT #2, R$
     XINC = VAL(R$)
```

```
     CMD$ = "XOR?"
     PRINT #1, "OUTPUT ", DEV1%, " $ +", CMD$
     PRINT #1, "ENTER 07 $ +"
     INPUT #2, R$
     XORG = VAL(R$)
     CMD$ = "XREF?"
     PRINT #1, "OUTPUT ", DEV1%, " $ +", CMD$
     PRINT #1, "ENTER 07 $ +"
     INPUT #2, R$
     XREF = VAL(R$)
LOCATE 12, 1
PRINT "YINC ="; YINC, "YORG ="; YORG, "YREF ="; YREF
PRINT "XINC ="; XINC, "XORG ="; XORG, "XREF ="; XREF
X$ = SPACE$(15)
Y$ = SPACE$(15)
LOCATE 16, 1
PRINT "Retrieving the data from the scope........"
CMD$ = "DATA?"
PRINT #1, "OUTPUT ", DEV1%, " $ +", CMD$
FOR I = 1 TO PNTS
     PRINT #1, "ENTER 07 $ +"
     INPUT #2, Y$
     X = (I * XINC) + XORG
     Y = ((VAL(Y$) - YREF) * YINC) + YORG
     WRITE #3, X, Y
NEXT I
CLOSE #3
CLS
LOCATE 9, 1
INPUT "Filename for data from scope's Memory 2: ", DF$
OPEN DF$ FOR OUTPUT AS #4
    CMD$ = "WAVEFORM SOURCE MEMORY 2 FORMAT ASCII"
     PRINT #1, "OUTPUT ", DEV1%, " $ +", CMD$
     R$ = SPACE$(15)
     CMD$ = "POINTS?"
     PRINT #1, "OUTPUT ", DEV1%, " $ +", CMD$
     PRINT #1, "ENTER 07 $ +"
     INPUT #2, R$
     PNTS = VAL(R$)
     LOCATE 11, 1
     PRINT "The number of points is: ", PNTS
     CMD$ = "YREF?"
     PRINT #1, "OUTPUT ", DEV1%, " $ +", CMD$
     PRINT #1, "ENTER 07 $ +"
     INPUT #2, R$
     YREF = VAL(R$)
     CMD$ = "YINC?"
     PRINT #1, "OUTPUT ", DEV1%, " $ +", CMD$
     PRINT #1, "ENTER 07 $ +"
     INPUT #2, R$
     YINC = VAL(R$)
     CMD$ = "YOR?"
```

```
     PRINT #1, "OUTPUT ", DEV1%, " $ +", CMD$
     PRINT #1, "ENTER 07 $ +"
     INPUT #2, R$
     YORG = VAL(R$)
     CMD$ = "XINC?"
     PRINT #1, "OUTPUT ", DEV1%, " $ +", CMD$
     PRINT #1, "ENTER 07 $ +"
     INPUT #2, R$
     XINC = VAL(R$)
     CMD$ = "XOR?"
     PRINT #1, "OUTPUT ", DEV1%, " $ +", CMD$
     PRINT #1, "ENTER 07 $ +"
     INPUT #2, R$
     XORG = VAL(R$)
     CMD$ = "XREF?"
     PRINT #1, "OUTPUT ", DEV1%, " $ +", CMD$
     PRINT #1, "ENTER 07 $ +"
     INPUT #2, R$
     XREF = VAL(R$)
LOCATE 12, 1
PRINT "YINC ="; YINC, "YORG ="; YORG, "YREF ="; YREF
PRINT "XINC ="; XINC, "XORG ="; XORG, "XREF ="; XREF
X$ = SPACE$(15)
Y$ = SPACE$(15)
LOCATE 16, 1
PRINT "Retrieving the data from the scope........"
CMD$ = "DATA?"
PRINT #1, "OUTPUT ", DEV1%, " $ +", CMD$
FOR I = 1 TO PNTS
        PRINT #1, "ENTER 07 $ +"
        INPUT #2, Y$
        X = (I * XINC) + XORG
        Y = ((VAL(Y$) - YREF) * YINC) + YORG
        WRITE #4, X, Y
NEXT I
CLOSE #4
CLS
     CMD$ = "LOCAL"
     PRINT #1, "OUTPUT ", DEV1%, " $ +", CMD$
'
'
'
CLOSE
STOP
1540 IF (ERR <> 68) AND (ERR <> 57) THEN PRINT "BASIC ERROR #
"; ERR; " in line "; ERL: STOP
INPUT #2, E$
PRINT E$
INPUT #2, E$
PRINT E$
END
```

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VITA

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The objective of this research effort was to investigate the implementation of analog circuits in a wafer scale integration system. A test circuit composed of analog and digital subsystems was designed and tested through simulation. IC die containing this test circuit were utilized in the WSI system fabrication. Preliminary investigations were conducted to evaluate the potential improvements to the IC die mounting procedure, a key step in fabricating functional WSI systems. These investigations demonstrated a procedure which produced repeatable results in achieving acceptable planarization of IC die and host substrate surfaces. These investigations also demonstrated the successful application of a barrier coating material to prevent adhesion between the IC die adhesive and reference flat during the IC die mounting procedure. An evaluation of candidate polyimides to be used as the interlevel dielectric in the WSI systems was also performed. Test samples for each of the WSI configurations were fabricated and tested for electrical continuity. Additional electrical characterization measurements were conducted on two of the test samples.

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