LOAN DOCUMENT

PHOTOGRAPH THIS SHEET

AD-A244 891

DTIC ACCESSION NUMBER

LEVEL

1

INVENTORY

NRL 9169

DOCUMENT IDENTIFICATION

20 Mar 89

DISTRIBUTION STATEMENT A

Approved for public release;
Distribution Unlimited

DISTRIBUTION STATEMENT

HANDLE WITH CARE

ACCESSION FOR

NTIS	GRA&I	☒
DTIC	TRAC	☐
UNANNOUNCED		☐
JUSTIFICATION		

BY

DISTRIBUTION/

AVAILABILITY CODES

DISTRIBUTION	AVAILABILITY AND/OR SPECIAL	
A-1		

DISTRIBUTION STAMP

DTIC
ELECTE
DEC 3 1991
S D
C

DATE ACCESSIONED

DATE RETURNED

91 1211 061

DATE RECEIVED IN DTIC

91-17645

REGISTERED OR CERTIFIED NUMBER

PHOTOGRAPH THIS SHEET AND RETURN TO DTIC-FDAC

DTIC FORM 70A JUN 90

DOCUMENT PROCESSING SHEET

PREVIOUS EDITIONS MAY BE USED UNTIL STOCK IS EXHAUSTED

LOAN DOCUMENT

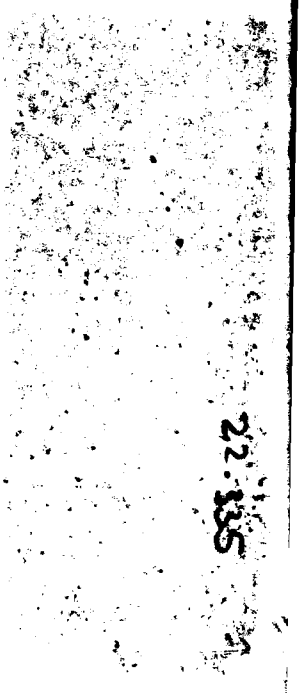
NRL Report 9169

The Variable Speed HF Modem Modulator Design

DAVID L. TATE

Communication Systems Engineering Branch
Information Technology Division

March 20, 1989



SECURITY CLASSIFICATION OF THIS PAGE

REPORT DOCUMENTATION PAGE

Form Approved
OMB No 0704-0188

1a REPORT SECURITY CLASSIFICATION UNCLASSIFIED	1b RESTRICTIVE MARKINGS
2a SECURITY CLASSIFICATION AUTHORITY	3 DISTRIBUTION / AVAILABILITY OF REPORT Approved for public release; distribution unlimited.
2b DECLASSIFICATION / DOWNGRADING SCHEDULE	
4 PERFORMING ORGANIZATION REPORT NUMBER(S) NRL Report 9169	5 MONITORING ORGANIZATION REPORT NUMBER(S)
6a NAME OF PERFORMING ORGANIZATION Naval Research Laboratory 6b OFFICE SYMBOL (*If applicable*)	7a NAME OF MONITORING ORGANIZATION
6c ADDRESS (*City, State, and ZIP Code*) Washington, DC 20375-5000	7b ADDRESS (*City, State, and ZIP Code*)
8a NAME OF FUNDING / SPONSORING ORGANIZATION 8b OFFICE SYMBOL (*If applicable*)	9 PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER
8c ADDRESS (*City, State, and ZIP Code*)	10 SOURCE OF FUNDING NUMBERS PROGRAM ELEMENT NO / PROJECT NO / TASK NO / WORK UNIT ACCESSION NO: DN156-254

11 TITLE (*Include Security Classification*)
The Variable Speed HF Modem Modulator Design

12 PERSONAL AUTHOR(S)
Tate, D. L.

13a TYPE OF REPORT	13b TIME COVERED	14 DATE OF REPORT (*Year, Month, Day*)	15 PAGE COUNT
	FROM Oct. 1986 TO Oct. 1987	1989 March 20	28

16 SUPPLEMENTARY NOTATION

17 COSATI CODES			18 SUBJECT TERMS (*Continue on reverse if necessary and identify by block number*)
FIELD	GROUP	SUB-GROUP	HF modems, AN/USQ-83, ANDVT TACTERM, TMS320

19 ABSTRACT (*Continue on reverse if necessary and identify by block number*)

The battery-operated, Variable Speed High Frequency (HF) Modem transmits data at 2400 bits per second (bps) over HF radio links. Variable data rates of 2400 and 1200 bps are supported. This compact, lightweight unit is a processor-based implementation based on the TMS320C25 digital signal processor. The modem waveform is compatible with the AN/USQ-83(V) and ANDVT TACTERM equipment. This report presents a functional overview of the hardware and software design of the Variable Speed HF Modem modulator.

20 DISTRIBUTION / AVAILABILITY OF ABSTRACT	21 ABSTRACT SECURITY CLASSIFICATION
☒ UNCLASSIFIED/UNLIMITED ☐ SAME AS RPT ☐ DTIC USERS	UNCLASSIFIED
22a NAME OF RESPONSIBLE INDIVIDUAL David L. Tate	22b TELEPHONE (*Include Area Code*) (202) 767-2953 22c OFFICE SYMBOL Code 5531

DD Form 1473, JUN 86 *Previous editions are obsolete* SECURITY CLASSIFICATION OF THIS PAGE

S/N 0102-LF-014-6603

CONTENTS

THE VARIABLE SPEED HF MODEM MODULATOR DESIGN

INTRODUCTION

The Variable Speed High-Frequency (HF) Modem (VSM) is a lightweight, compact HF modem that transmits information at 2400 bits per second (bps) over HF radio links. The VSM is battery operated and requires no operator controls. All control and processing functions are performed through interface signals or processor control. The VSM supports variable data rates of 2400 bps with standard RS-232 signaling and 1200 bps with special purpose signaling. The waveform generated by the VSM is compatible with either the AN/USQ-83(V) or the ANDVT TACTERM (CV-3591). This report gives a functional overview of the hardware and software designs of the VSM modulator. The demodulator in the VSM is under development and will be discussed in a later report.

BACKGROUND

The Information Technology Division (ITD) at the Naval Research Laboratory (NRL) has been a leader in the development of HF radio communication systems for Navy shipboard and land-based communications stations. Historically, these systems use large, heavy equipment to perform the transmission/reception of radio signals and the modulation/demodulation of data. The size, weight, and power required for this equipment do not present a problem in the systems for which they were designed, but they are unsuitable for portable use. The Communication Systems Engineering Branch in ITD has filled the need for a portable HF modem with the design and construction of the VSM. This product is a battery-operated device that is used in a manpack environment. The modem is completely automated and requires no manual operation other than connecting cables to the front panel. All control functions—including application of power, data input, waveform generation, signal output, and power shutdown—are performed through interface control signals and processor commands.

Design Approach

The design of the VSM is based on the following set of requirements:

- The modem must be capable of accepting serial digital data from the operator's message device and transmit the data reliably over HF or shortwave radio.
- The modem must be small and portable enough to be carried on a backpack.
- The modem waveform must be of short duration and compatible with existing receive modems, including the AN/USQ-83 and ANDVT TACTERM.
- Power must be provided by an internal battery pack.

Manuscript approved August 9, 1988.

Equipment Description

The equipment required to use the VSM consists of the modem, a message device, an HF radio, and associated cables. The message device and radio are not supplied with the modem. Figure 1 shows the equipment provided with the modem which is the VSM radio interface cable, message device interface cable, and the VSM operator's manual.

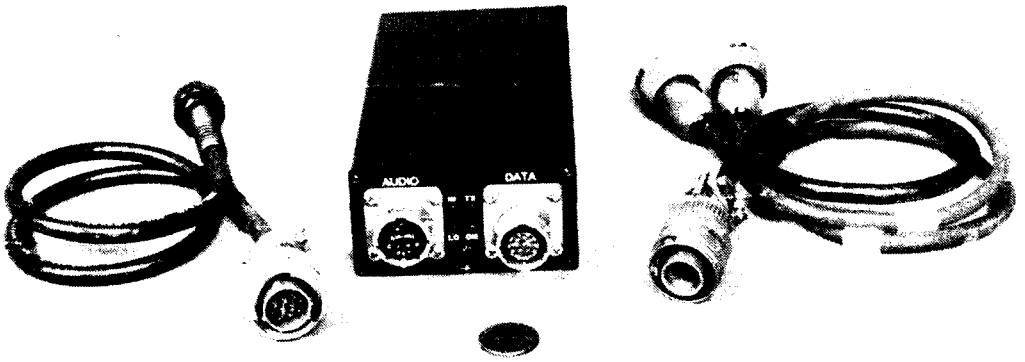


Fig. 1 — The VSM is a small battery-operated HF modem that provides high-speed data transmission in a manpack environment

The VSM is a self-contained battery-operated HF modem designed to provide high-speed, short message transmissions and reception of low data rate, externally demodulated messages. The hardware design includes the necessary components for internal demodulation that will be implemented in later phases of the VSM development. The modem is designed to interface to the message device and generic RS-232 data devices.

The radio interface cable connects the VSM AUDIO connector to standard HF radios through their audio (or handset) connector. The message device interface cable connects the message device to the VSM DATA connector. Figure 2 shows the equipment interconnection diagram.

Reference Documents

The following documents provide additional information about various aspects of the VSM:

- Variable Speed HF Modem Operator's Manual, November 1987,
- Variable Speed HF Modem Technical Reference Manual, September 1987,
- ANDVT TACTERM (CV-3591) Specification, and
- AN/USQ-83(V) Specification.

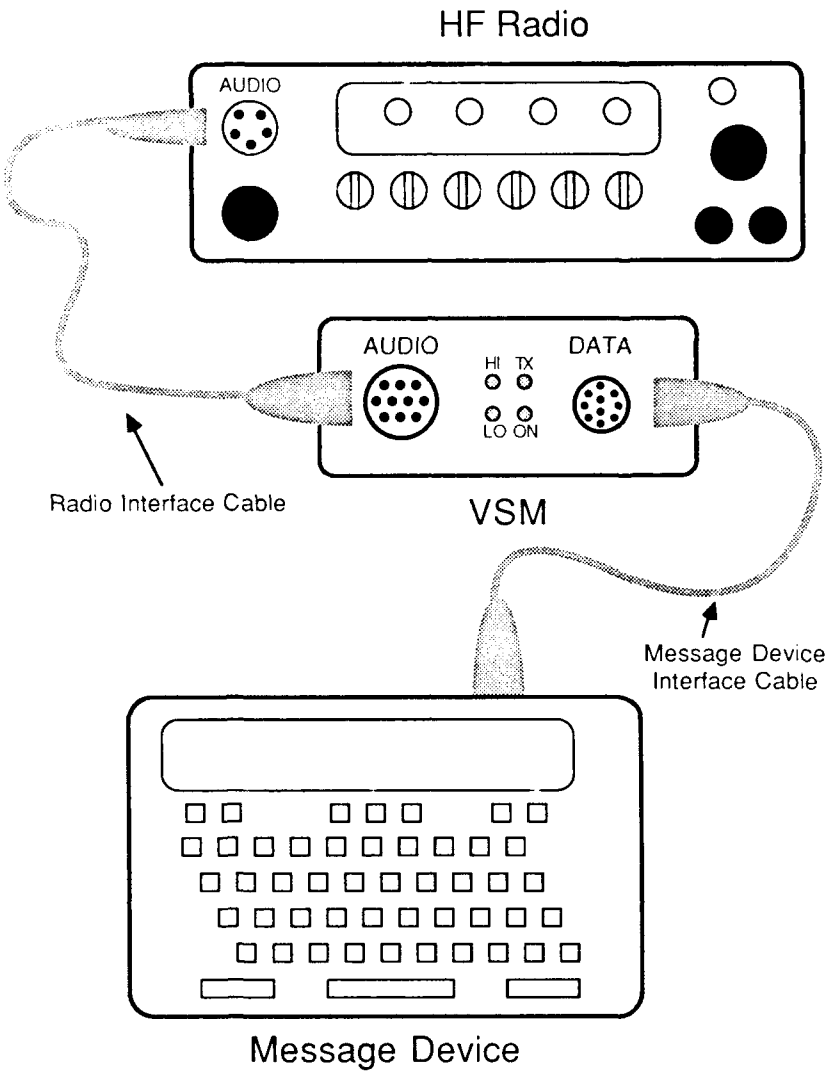


Fig. 2 — Connecting the VSM requires only a cable to the message device and a cable to the HF radio

HARDWARE DESIGN

The VSM is a compact unit that can be carried easily along with other portable communications equipment. The modem is enclosed in an extruded aluminum case that easily withstands the rough treatment given to portable field equipment. The compact enclosure measures 1.5 × 2.5 × 6 in. The digital data device and the HF radio are connected with the two cables supplied with each VSM.

The front panel of the VSM provides connectors for cables to the digital data message device and the HF radio that are labeled DATA and AUDIO respectively. The data output connector from the data device is connected to the DATA connector on the VSM, and the AUDIO connector on the VSM is connected to the audio (or handset) connector on the HF radio. Indicators on the front panel provide status information from the VSM. The ON indicator shows that power has been applied and that the VSM is ready for operation. The TX indicator is used for transmit operations and shows that digital data are being received from the data device and that transmission of the modem signal is in progress. The HI and LO indicators are used for receive operations and indicate that the HF radio audio output level is too high (input signal distortion is occurring due to signal overload) or too low (modem performance is degraded due to weak signals).

Note that no operator controls are provided on the front panel. The VSM design prevents incorrect control settings by an inexperienced operator. Control signals from the data device are monitored by the VSM and are used to start a transmit operation. A minimal amount of battery power is used to sense the status of the power control line from the data device during normal operation. To prevent unnecessary drain on the internal battery when not in use, the VSM disconnects all power when either of the two cables is removed. Audio output levels are fixed to be compatible with standard HF radio equipment to prevent incorrect output level settings. For receive operations, by observing the HI and LO indicators on the VSM, the operator adjusts the audio levels at the radio, thereby eliminating a separate input volume control on the VSM.

The internal construction of the VSM is designed for easy repair and maintenance. Three interconnected printed circuit boards enable board-level replacement of defective components (Fig. 3). The processor, memory, digital-to-analog (D/A) converters, and system-timing components reside on the central processing unit (CPU) board. The CPU board provides switches for selecting various user options that are described in the Software Design Section of this report. The battery pack, power control circuitry, and interface conditioning components reside on the battery board. The integral front panel plate, connectors, and indicators are mounted directly on the front panel board. The front panel board also serves as a mother board with connectors for both the CPU and battery boards, eliminating the need for a separate backplane. The VSM is assembled by inserting the CPU and battery boards into their appropriate connectors on the front panel board, and by sliding the entire assembly into the aluminum enclosure.

CPU and Memory

The CPU must be designed for digital signal processing operations to perform the necessary HF Modem Functions, which are control, signal processing, and arithmetic operations. These processors are specifically designed to perform high-speed, complex calculations. A typical procedure used in HF modem applications is the fast Fourier transform (FFT). The FFT has many iterative processing loops of multiply-and-accumulate operations that must be performed quickly enough to finish the computation on one block of data before the next data block is received (i.e., real-time processing is mandatory). Standard microprocessors do not provide real-time operation.

The CPU selected for the VSM is the Texas Instruments TMS320C25. It is a digital signal-processing chip that is capable of operation at clock rates of up to 40 MHz. Most arithmetic operations, including multiplication, can be performed in a single 100-ns instruction cycle for a maximum computational speed of ten million instructions per second (10 MIPS). The processor is based on a 16-bit data structure and provides double precision (32-bit) operations with the accumulator and multiplier product registers. The processor uses complementary metal-oxide silicon (CMOS) technology to reduce the power supply current requirement.

The internal processing uses integer arithmetic, but floating point operations can be performed, if required, through software. The instruction set includes the arithmetic operations required for digital signal processing such as add, subtract, multiply, multiply-and-accumulate, square, and normalize. Also, double precision operations are supported. Logical operations that are required for interface and control operations include logical And, logical Or, logical exclusive-Or, bit test, shift left, and shift right. Processing control instructions include unconditional and conditional jumps, wait for interrupt, stack operations, subroutine call and return, and software interrupt.

The bus architecture used by the TMS320C25 has separate program and data memory areas. The address space used by both program and data memories can use the entire 16 bits of addressing to provide 64 kilobytes (64K) of program memory and 64K of data memory. The TMS320C25 uses

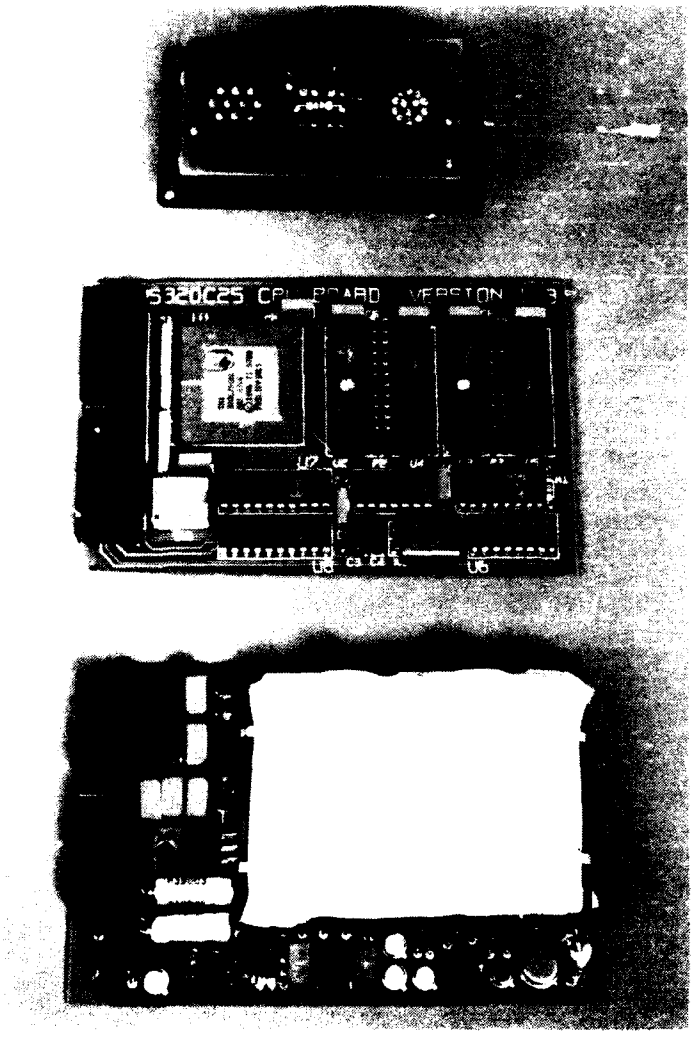


Fig. 3 — The modular design of the VSM comprises three interconnecting circuit boards—the front panel board, the CPU board, and the battery board

the same data and address signals for both memory types and therefore provides separate control signals to efficiently use the multiplexed bus.

The memory selected for the VSM includes programmable read-only memories (PROMs) for nonvolatile program and data storage, and read/write random access memories (RAMs) for transient data storage. The ROMs selected for the VSM are the Cypress Semiconductor CY7C291 parts. These PROMs provide 2K of 8-bit memory (2K × 8 bits) and are used in pairs to provide 2K × 16 bits of program information. The RAMs used are the Cypress Semiconductor CY7C128 components. They are configured as 2K × 8 bits and are also used in pairs to provide 2K × 16 bits of data. Figure 4 diagrams the program memory interface, and Fig. 5 diagrams the data memory interface.

Timing and System Control

Two clock signals compose the timing circuitry in the VSM. The system clock is used by the processor for instruction timing and is the basis for the auxiliary control signals for memory interface controls. The analog interface clock controls the analog-to-digital (A/D) and D/A conversions and the filters used in the analog interface.

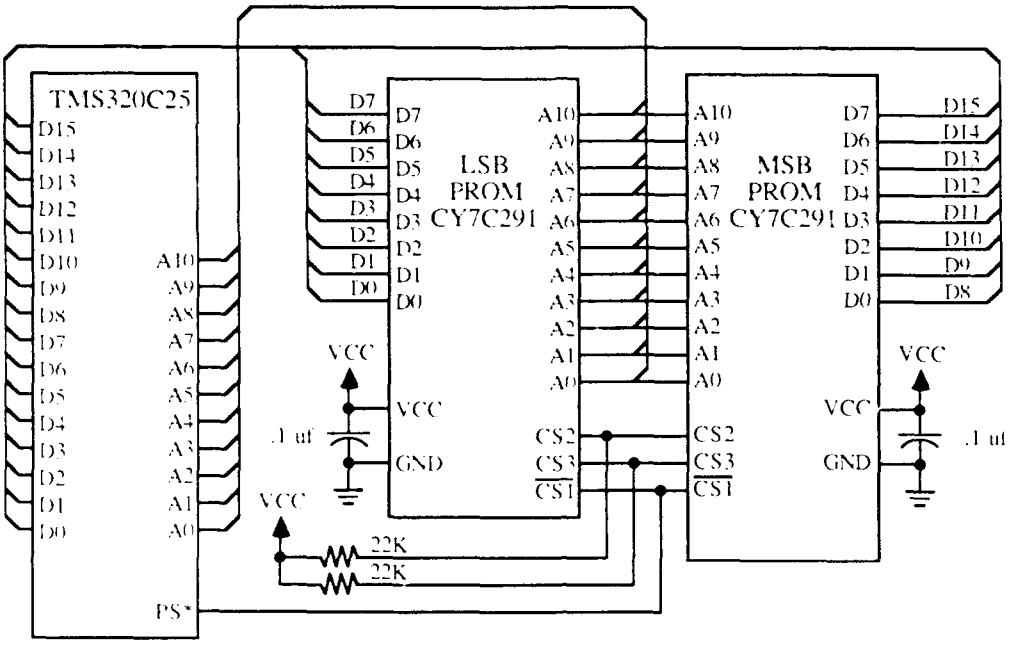


Fig. 4 — The interface to the nonvolatile PROMs requires no additional external components

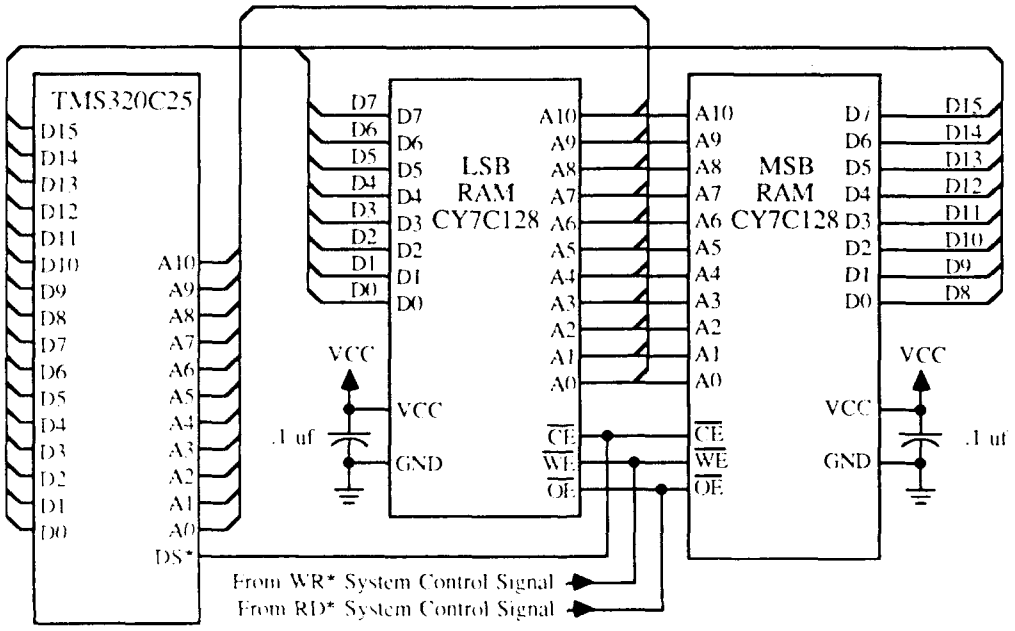


Fig. 5 — The interface to the RAMs requires only minimal external components to generate auxiliary control signals

The system clock is derived from a 16.128 MHz crystal-controlled oscillator. The TMS320C25 processor provides internal circuitry that drives the oscillator and requires only a crystal and two capacitors as the external components (Fig. 6). The crystal frequency of 16.128 MHz chosen for the VSM produces a single-cycle instruction execution time of 248 ns. Although the TMS320C25 processor is capable of running with an instruction cycle time of 100 ns, the increased capability of the processor is not required by the VSM. At the maximum rated speed the processor consumes more power than at lower speeds. The 16.128 MHz crystal provides sufficient execution speed for the VSM program, while operating at reduced power requirements. This frequency also permits the use of the older TMS32020 processor, a slower but compatible alternate CPU. The crystal frequency was specially chosen to use clock signals from the TMS320C25 and a minimum of additional components to provide the total system timing requirements.

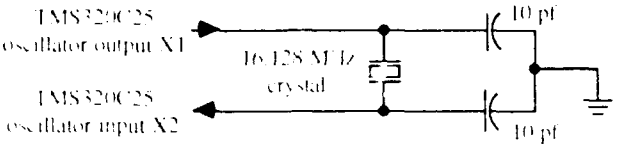


Fig. 6 — The VSM uses the internal oscillator in the TMS320C25 to generate the system clock signal

The analog interface clock drives the analog input/output device. Normally, a separate crystal creates a specific frequency that in turn creates a sample rate of 8000 Hz. The VSM uses a specially chosen system crystal and a divide-by-two circuit to generate a 7200 Hz sample rate. The clock output from the CPU is one fourth the crystal frequency, or 4.032 MHz. A single D-type flip-flop (1/2 of a 74HC74 dual D-type flip-flop) is used in a divide-by-2 configuration to generate the 2.016 MHz analog interface clock from which the 7200 Hz sample rate is derived (Fig. 7).

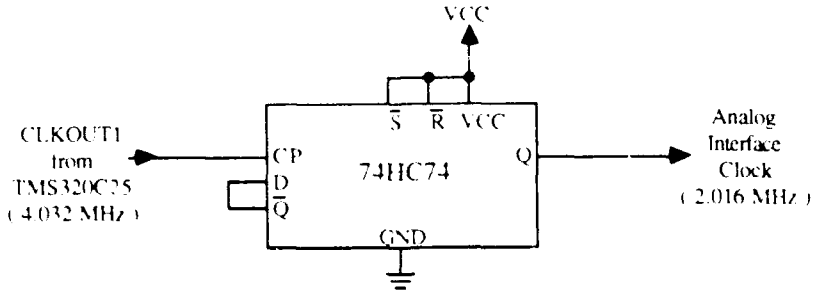


Fig. 7 — A unique method of generating a nonstandard analog interface clock that is derived from the system clock is used in the VSM

Control signals are required to interface correctly to the various memories and input/output (I/O) devices. The TMS320C25 provides signals (designated XX* for signal name XX, active low output) for program memory selection (PS*), data memory selection (DS*), and I/O device selection (IS*). Auxiliary timing signals are generated to perform other control functions (Fig. 8). These signals are derived from the processor read/write signal (R/W*), I/O select signal (IS*), and the strobe signal (STRB*). They comprise the write enable (WR*) and read enable (RD*) signals used by the data memory, and the I/O write (IOWR*) and I/O read (IORD*) signals used by the I/O devices. The auxiliary signals are generated through a 2-to-4 line decoder/demultiplexer (1/2 of a 74HC139 dual 2-to-4 line decoder/demultiplexer).

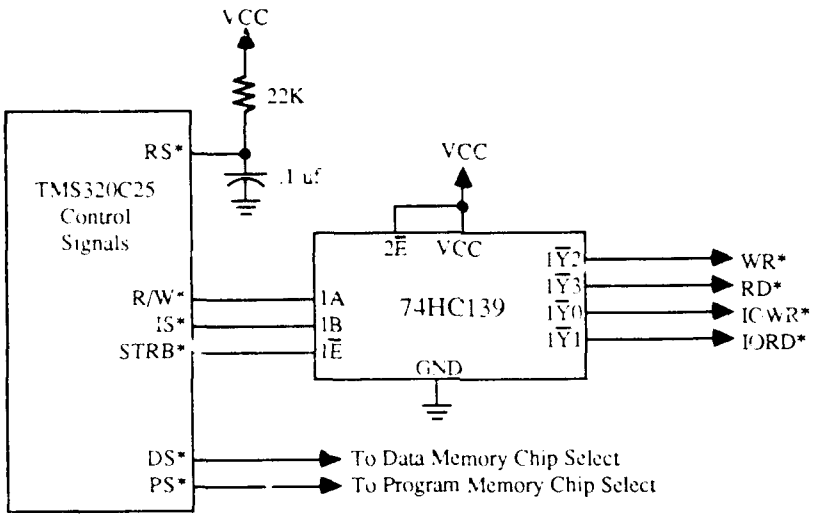


Fig. 8 — All system control signals are available directly from the CPU or are provided through simple decoding logic

The final control signal required by the VSM is the processor reset signal (RS*). This signal is held low long enough for the processor to stabilize after having power applied to it. When RS* is released, the processor begins execution from a known initial state. A resistor/capacitor delay circuit is used to hold RS* low for a predetermined amount of time to assure correct start-up of the processor.

Analog Input/Output

The analog interface in the VSM is based on the Texas Instruments TCM2916 coder/decoder (codec). This device performs the D/A conversion of the modem output, the A/D conversion of received input signals, and the necessary filtering to generate a smooth output waveform and prevent aliasing in the sampled input signal. The TMS320C25 processor has a special serial interface that is used to connect directly to this type of codec. The only external components required by this interface are those that generate the analog interface clock. The serial data and framing signals, required by both the codec and the CPU, are directly connected to each other to provide a simple, direct interface (Fig. 9).

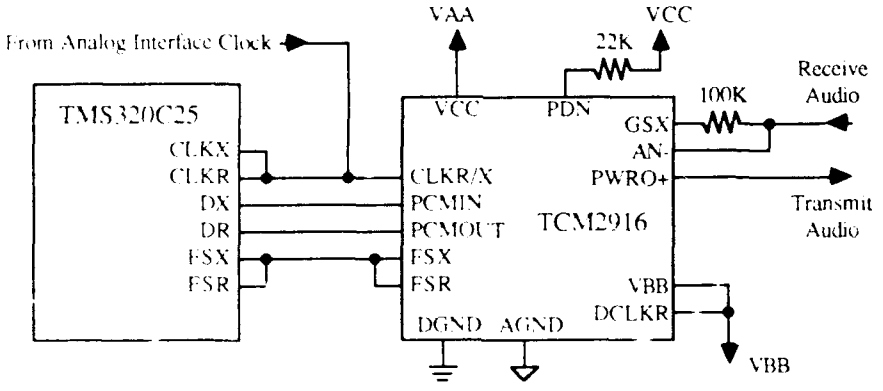


Fig. 9 — Analog input, output, and filtering are performed through a single coder/decoder integrated circuit

The TCM2916 codec is commonly used in telephone circuits with a bandwidth of 4 kHz. The sampling frequency of the analog signals is usually 8.0 kHz. In this configuration, the analog interface clock is required to be 2.048 MHz to provide correct timing for the internal filter circuits. The VSM uses a modification of this configuration. The sampling frequency of the A/D and D/A in the VSM is 7200 Hz, giving a usable bandwidth of 3.6 kHz. The sampling frequency used in the VSM is derived from the crystal frequency by a frequency divider circuit, therefore the crystal frequency must be a multiple of 7200 Hz to perform the correct sampling. The 16.128 MHz crystal frequency was chosen because it is a multiple of 7200 Hz. The other consideration in the selection of the crystal frequency involves the filters in the codec. With a 2.048 MHz analog clock frequency the filter bandwidth is 4 kHz. This bandwidth is too large for the VSM and would degrade performance owing to aliasing. By lowering the analog interface clock to 2.016 MHz by the circuit described previously, the bandwidth is reduced, improving the performance of the VSM. The combination of crystal frequency selection, generation of the analog interface clock, and bandwidth adjustment in the codec is a unique design approach that has been very successful in reducing circuit complexity while fulfilling the operational requirements of the VSM.

Signal conditioning circuitry (Fig. 10) is also provided in the VSM to buffer and amplify analog signals, if required. Component values in the signal conditioning circuit can be changed to increase or decrease the amplification, and the conditioning circuitry provides increased protection for the codec against overload. Amplification is provided by a TL072 operational amplifier and its associated components. Both the input and output signal conditioning circuits are AC coupled to prevent unwanted DC offsets from the HF radio.

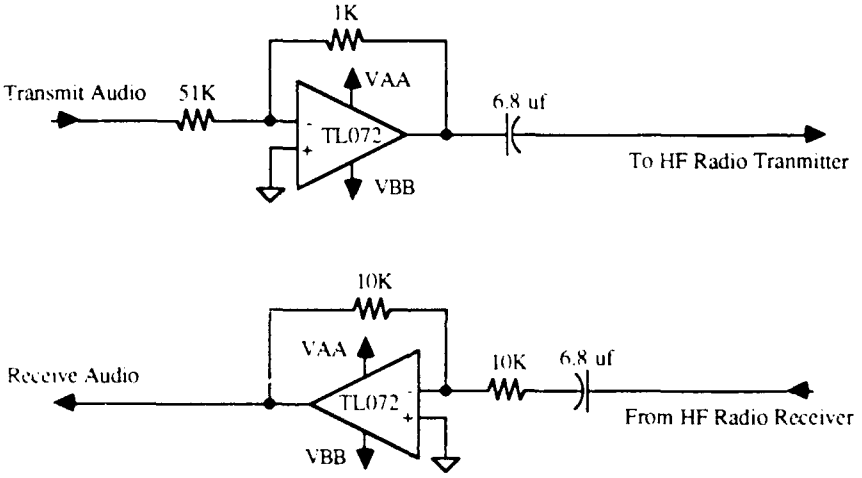


Fig. 10 — Operational amplifers provide amplification and signal conditioning to the analog interface signals

Digital Input/Output

Digital input and output interfaces are provided for data transfer, status, and control. Digital input to the TMS320C25 CPU is accomplished through an octal line driver, the 74HC540. This device allows the CPU to read eight data bits from the various input devices in the VSM (Fig. 11). Power control signals from the message device and user-selectable switch settings are read directly through the 74HC540. Although this is a parallel interface, periodic sampling of the digital data through program control can perform serial data input. The VSM uses this technique for reading serial data from the digital message device. Level conversion and signal buffering is done through a MAX232 RS-232 driver/receiver.

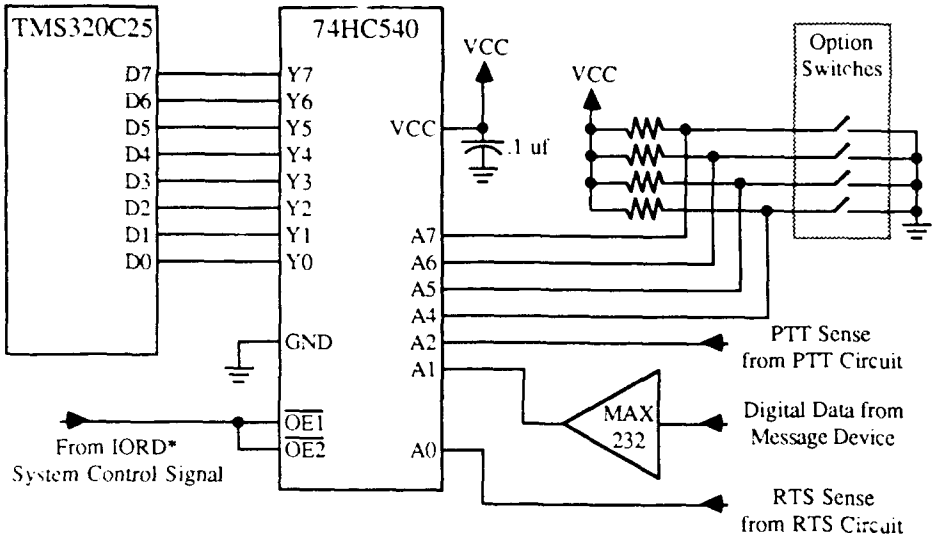


Fig. 11 — The digital input interface reads control signals, message device data, and user-selectable option switches

The digital interface also outputs status information to the front panel, control signals to the HF radio, and serial data to the message device (Fig. 12). The output interface to the CPU uses the 74HC564 octal, D-type, flip-flop. Transistor driver circuits drive the light-emitting diode (LED) displays on the front panel and the keyline circuit that keys the transmitter in the HF radio. Periodic data output through program control generates the serial data and the serial interface clock signals used by the digital message device. Level conversion and signal buffering of these signals is done through the MAX232 RS-232 driver/receiver.

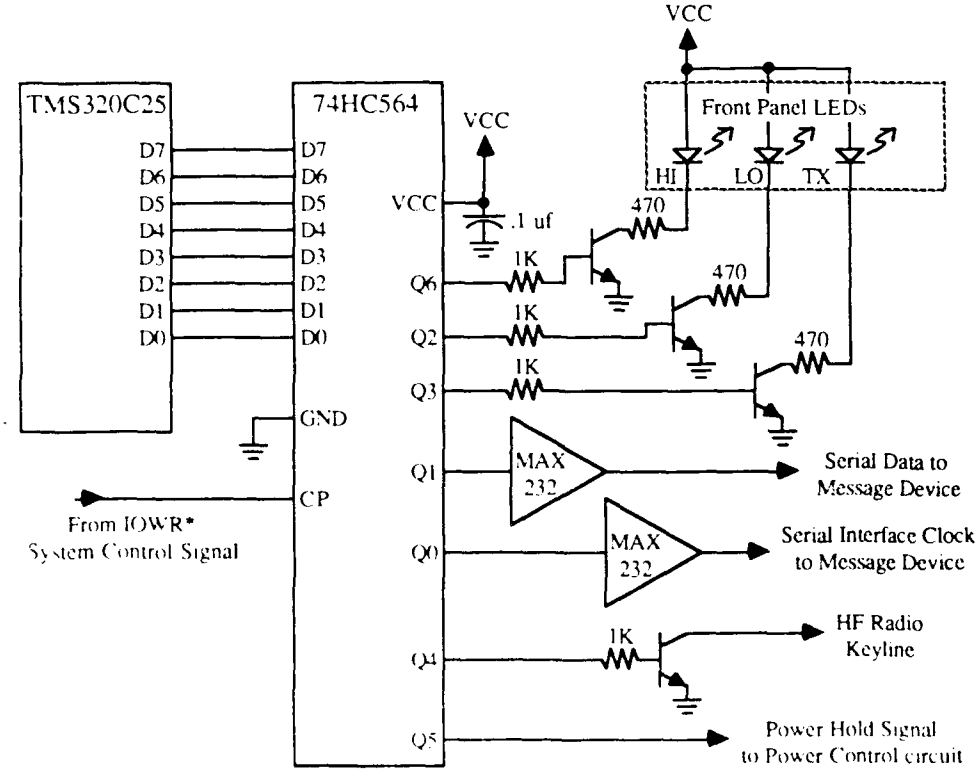


Fig. 12 — The digital output interface outputs control signals, message device clock and data, and front panel display indicator signals

Power Control

The internal battery pack provides the power for the VSM through an electronic power switch (Fig. 13) in the power control circuitry. The switch is activated when the base of a 2N5680 PNP transistor is pulled low. Three mechanisms are used to activate this switch by using three different techniques.

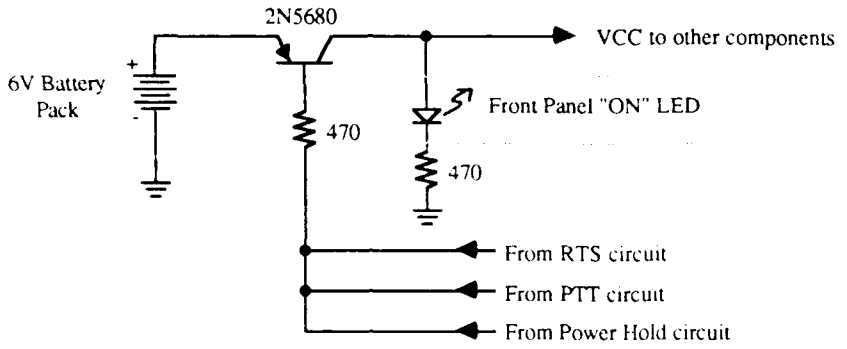


Fig. 13 — Power to the VSM is controlled from three sources to the electronic power switch

The Push-To-Talk (PTT) circuit activates the electronic power switch with a switch closure between the PTT signal and the ground (GND) signal on the DATA connector. This technique is useful with data message devices that usually provide a switch closure to GND to key the HF radio transmitter. This same switch closure can activate the VSM. The connection to GND turns on the 2N2907 NPN transistor (Fig. 14), causing the electronic power switch to turn on and apply power to the VSM. The PTT Sense signal is passed through an isolation diode to the digital input circuitry for use as a status input signal for the processor.

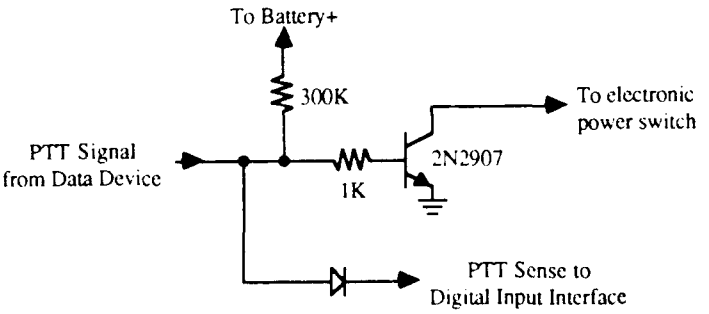


Fig. 14 — Data message devices that provide a switch closure to ground use the PTT interface

The Request-To-Send (RTS) circuit provides the second method for applying power to the VSM. This method is useful with data message devices that comply with RS-232 standards. An active-high logic signal applied to the RTS activates the VSM. In a typical situation, an RS-232 data device would assert the RTS signal in preparation for sending digital data, and would wait for Clear-To-Send (CTS) to be asserted by the VSM before beginning to transmit data. The VSM detects the assertion of RTS and uses it to energize the electronic power switch through the RTS circuit shown in Fig. 15. Protection diodes convert the RS-232 signal levels to the normal transistor-transistor logic (TTL)

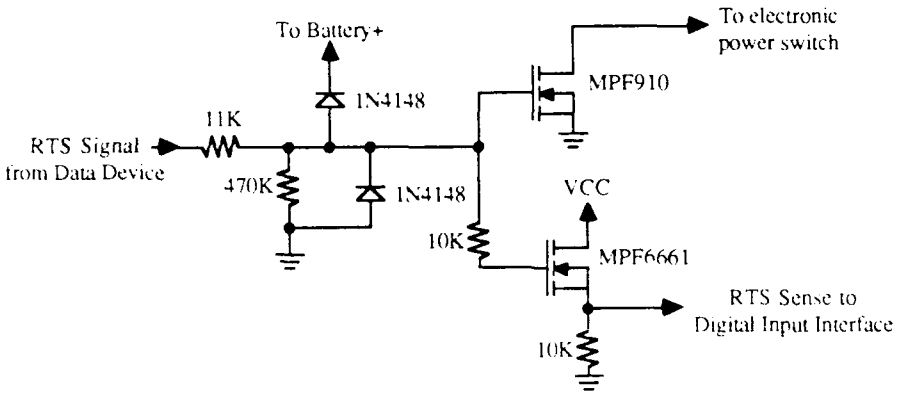


Fig. 15 — Standard RS-232 devices can use the RTS signal to energize the VSM

levels used by the VSM components, and the MPF910 transistor turns on the electronic power switch. The RTS Sense signal is passed to the digital input circuitry through the isolation circuitry comprising an MPF6661 transistor and two resistors.

Power for the VSM is also controlled through the digital output interface. The Power Hold signal is activated under program control from the CPU. This signal is used primarily to prevent the external power control signals (PTT and RTS) from disconnecting power to the CPU before transmission of the modem signal is completed. An MPF910 transistor controls the electronic power switch, and additional components assure reliable shutoff (Fig. 16).

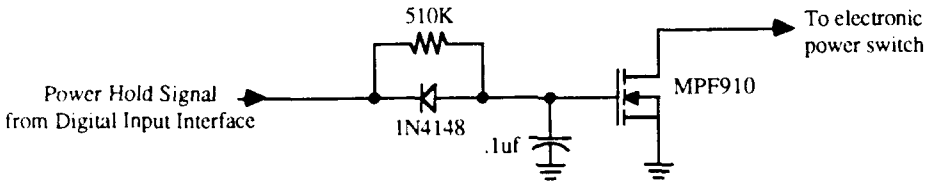


Fig. 16 — Power to the VSM is also under program control through the Power Hold circuit

The power control circuitry also provides separate power supply lines for the analog circuits. The power lines for the analog circuitry are separated from the other digital circuitry in the VSM to prevent switching noise caused by the digital components from creating noise in the analog interface. The TCM2916 codec and the operational amplifiers that generate the analog output require two power supply voltages, a +5 V supply and a −5 V supply. Figure 17 shows the circuitry used to generate these voltages. The analog +5 V supply VAA is derived from the digital +5 V supply VCC through a filtering circuit comprising three capacitors and ferrite bead inductors. This filtering reduces the noise generated by the digital circuits, while closely tracking the battery supply voltage. Generation of the analog −5 V supply VBB is accomplished through an Si7661 voltage converter and two capacitors. This device accepts a nominal +5 V input and creates a nominal −5 V supply voltage from it.

The circuit shown in Fig. 18 recharges the internal Ni-Cd battery pack. The LM317T voltage regulator is configured as a constant current source to provide a current of 100 mA for recharging. The diode is included in the recharging circuitry to prevent damage to the VSM owing to accidental incorrect hook-up of the recharging power supply.

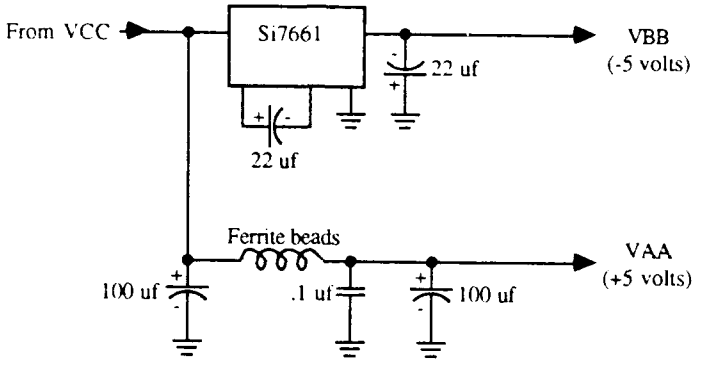


Fig. 17 — Power supplies for the analog circuitry (VAA and VBB) are derived from the digital supply (VCC) and filtered to reduce noise generated by digital components

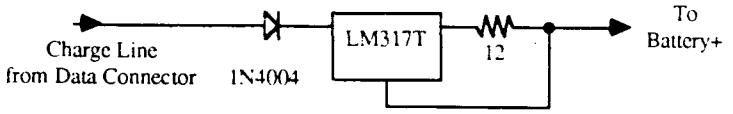


Fig. 18 — A simple recharging circuit allows the internal Ni-Cd battery pack to be recharged through the DATA connector

Although the VSM is designed for short, intermittent periods of use, to prevent battery drain when not in use, the VSM cables are designed so that removal of either the DATA cable or the AUDIO cable disconnects all components from the battery pack. This is accomplished through jumpers located in the cables that allow the completion of the power circuit only when both cables are inserted (Fig. 19). Note that if either cable is removed, the missing shorting plug causes an open circuit with no path from the battery to ground, hence no power is used.

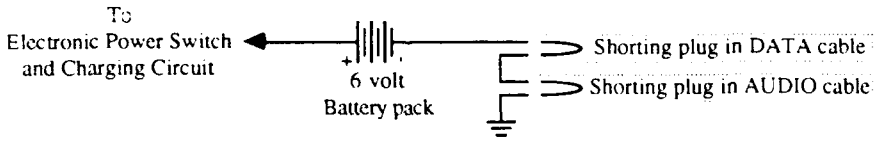


Fig. 19 — Power is completely disconnected when either cable is removed, to prevent unnecessary drain on the internal battery pack

Schematics

The description of the hardware design has been functionally divided into separate parts to provide a clear, concise description of the various sections. The functional descriptions include components that reside on different circuit boards where appropriate. The following schematics show the actual board-level implementation for the various components on the CPU board (Fig. 20), battery board (Fig. 21), and front panel board (Fig. 22).

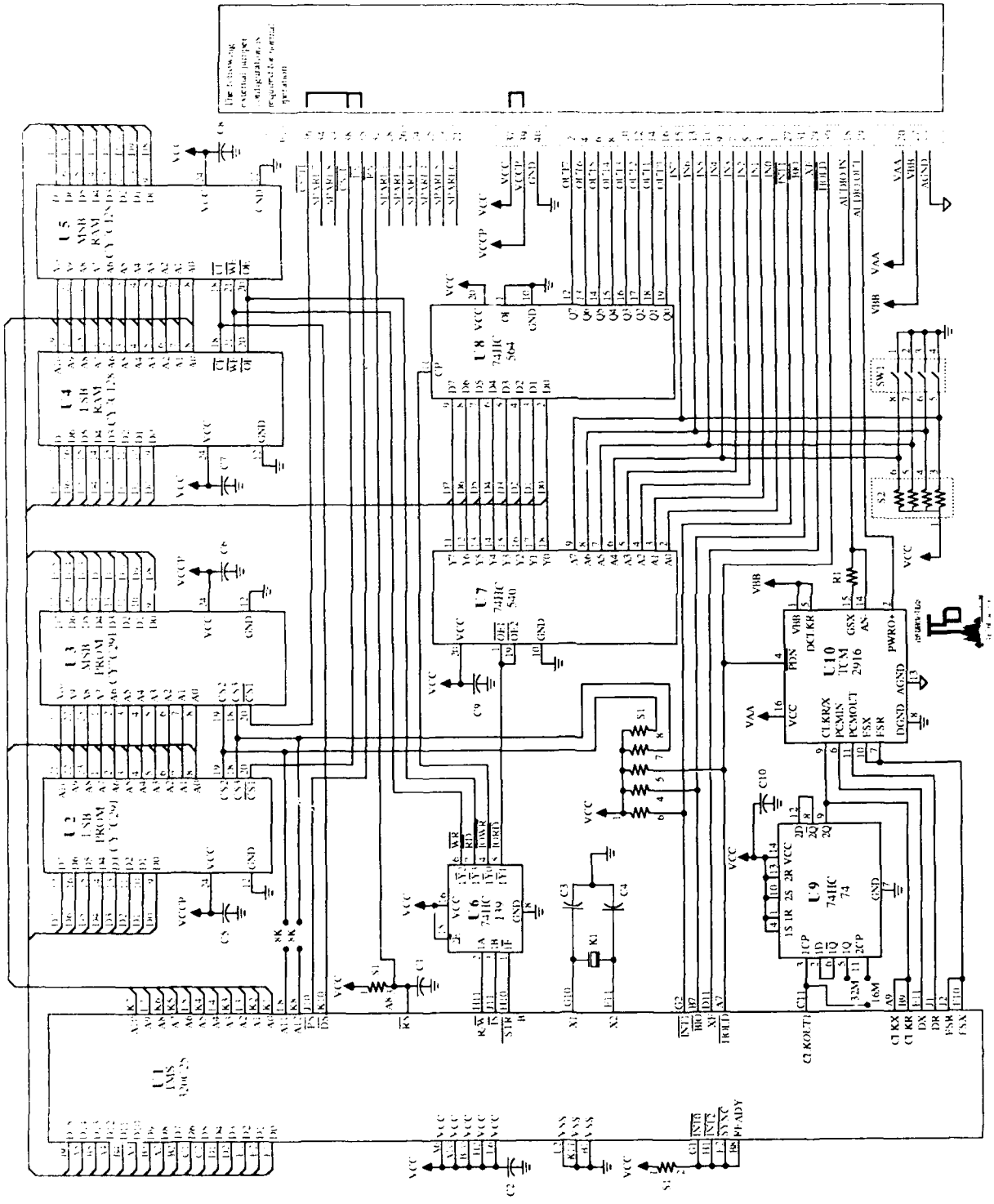


Fig. 20 — TMS320C25 CPU board, version 1.3

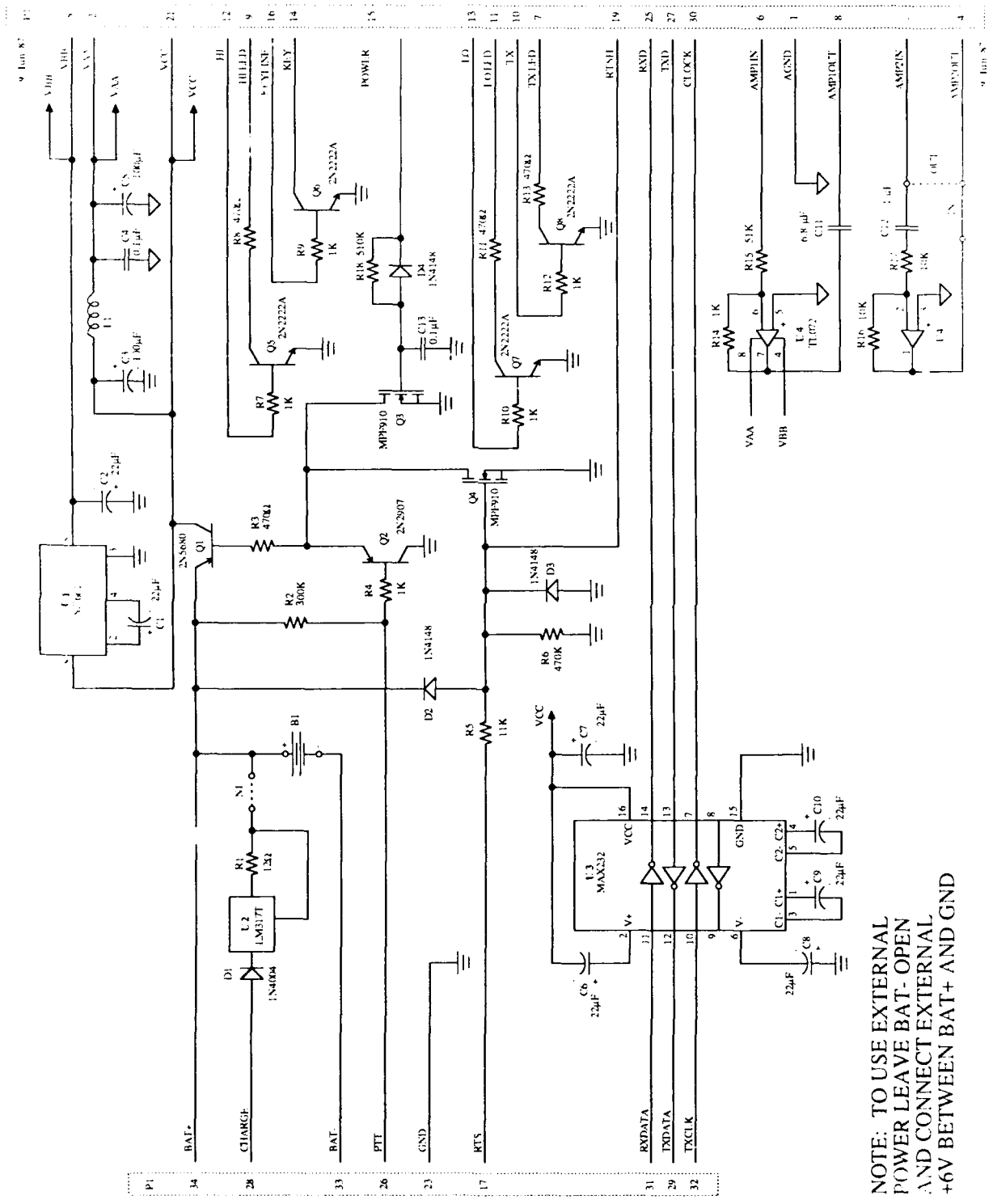


Fig. 21 — Battery board, version 1.3

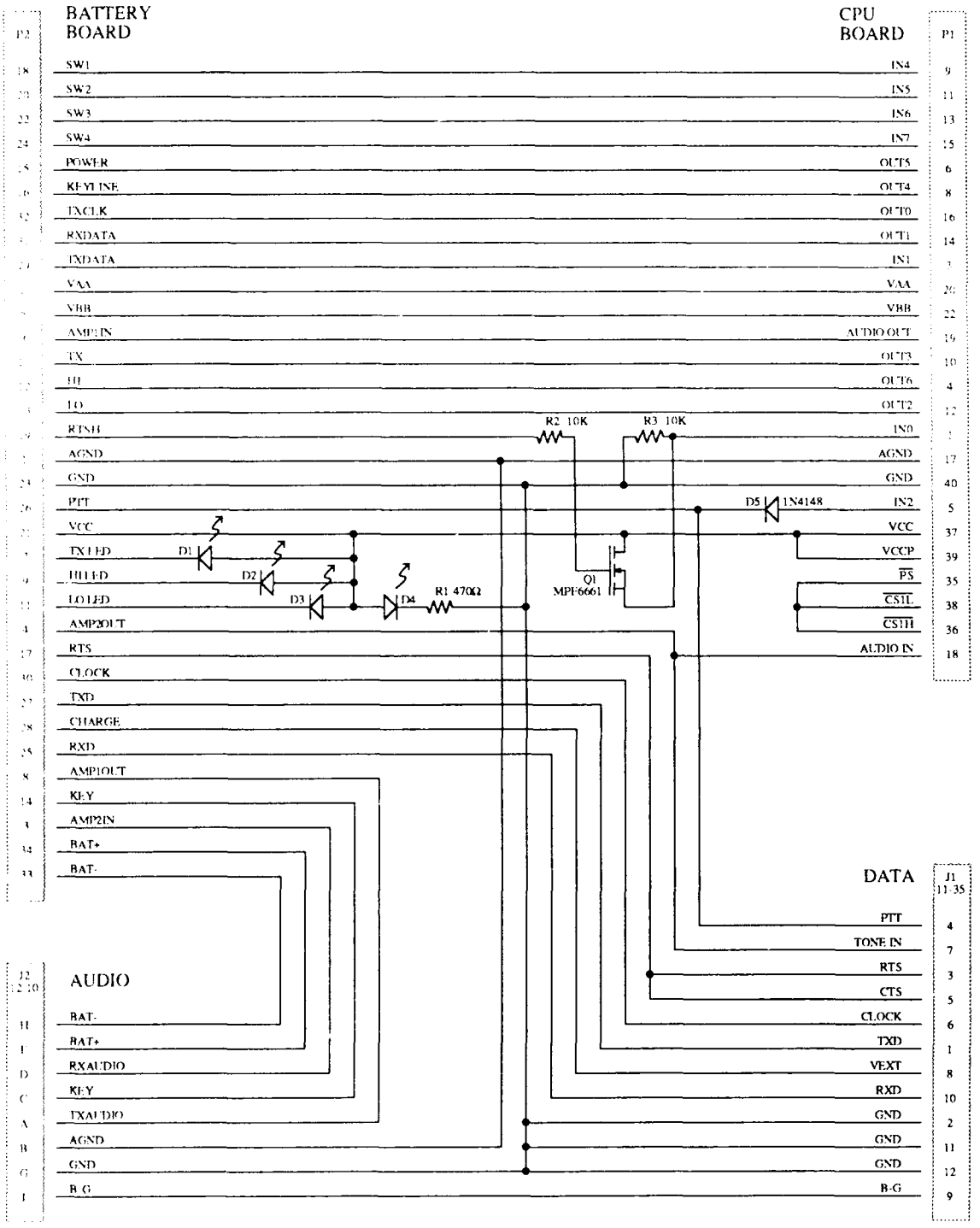


Fig. 22 — Front panel board, version 1.3

SOFTWARE DESIGN

The processor-based VSM uses the TMS320C25 Signal Processor to perform all of the control, interface, and modulation functions. The description given in this report addresses only the transmit functions provided by the initial phase of the VSM development. The receive functions to be implemented in later phases will be described in a separate report. Figure 23 separates the software design into a sequence of functional blocks. A brief description of the software design is given here; the Variable Speed HF Modem Technical Reference Manual gives a more complete description, including subroutine descriptions and program listings.

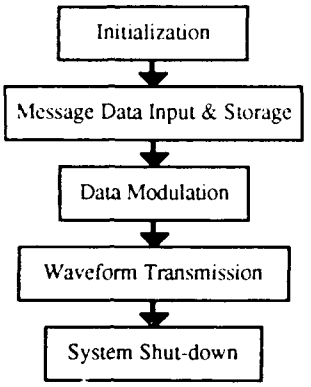


Fig. 23 — The software implementation can be divided into five modules

Initialization

The initialization functions are performed immediately after power is applied by the power control circuitry. These functions include procedures that correctly establish timing and interface controls for the hardware interfaces, as well as initialization of program variables and parameters. A built-in test procedure is also performed to verify the integrity of the program and data memories. After passing the self-test procedures, the VSM asserts the Power Hold signal to allow the processor to control when the power will be turned off.

After initialization of hardware interfaces and software variables, the digital input interface is polled to determine if the data transmission request is from the RTS circuit or the PTT circuit. This information is stored in the RTS/PTT flag for use by the message data input and storage procedures.

Message Data Input and Storage

After initialization, the VSM begins inputting data from the message device interface. The message data input and storage routines perform all of the data input, serial clock synchronization, data manipulation, buffering, and storage required by the modulation procedures.

Two different procedures process the data depending on the type of digital message device being used. The RTS/PTT flag set by the initialization procedures determines the format of the data.

Data devices that assert the PTT signal send synchronous data without use of the VSM serial interface clock. These data are presented to the VSM as an uninterrupted sequence of bits that contain fixed beginning and ending patterns with variable data between the fixed patterns. The beginning

and end patterns serve as timing indicators only, and they are not transmitted by the VSM. In this way, the VSM performs a degree of data compression that reduces the transmission time. Since the message devices that use the PTT signal do not accept clock from the VSM, timing of the digital data is determined by the VSM directly from the received data with compensation made for irregularities.

Data devices that assert the RTS signal send synchronous data that are synchronized to the VSM serial interface clock. These data are read only on the clock transitions and require no compensation for irregularities. No extraneous data are transmitted by these message devices, and the VSM transmits the message data exactly as they are received.

Buffering and storage of data is performed to allow time for the VSM preamble transmission and to ensure proper data transmission.

Data Modulation

Modulation of the data generates a 16-tone quaternary differential phase shift keyed (QDPSK) waveform. The VSM transmits data in frames lasting 13.3 ms giving a baud rate of 75 frames per second. During each frame the 16-tone QDPSK waveform transmits 2 bits of information on each tone for a bit rate of 32 bits per frame, or 2400 bps. The details of the waveform are described in the Waveform Specification section of this report.

Data modulation is performed by the use of an FFT that assigns phases to the 16 tones from the digital data received from the message device. Data modulation procedures involve transfer of data from the data input buffers to appropriate phase vectors in the FFT buffers and execution of the FFT algorithm to generate the corresponding tones for output.

Waveform Transmission

To generate the analog waveform to be transmitted by the HF radio, the tones generated by the data modulation procedures are output to the D/A converter. The waveform transmission modules perform the control of the timing, output sampling, and data transfer to the D/A.

Each data transmission comprises a sequence of three distinct types of waveform transmission: the preamble, data modulation, and the end-of-message (EOM). The waveform transmission modules control the sequence, timing, and waveform generation of the entire transmission. A detailed description of the waveform is given in the Waveform Specification section of this report.

The preamble allows the receive modem to acquire the signal, correct for any frequency offset, and synchronize timing to the transmitted waveform. The length of this preamble is determined by the setting of one of the option switches contained in the VSM. A shortened preamble may be used if transmit and receive radios are kept within tight frequency tolerances. A longer preamble is used for less restrictive radio specifications.

Data modulation transmits user data to the receive site. The VSM uses a fixed data modulation that is compatible with the AN/USQ-83(V) and the ANDVT TACTERM (CV-3591). Since the modulation is identical in both of these equipments, no switch settings are necessary.

The EOM sequence signals the termination of the transmission. This portion of the transmission allows the transmission to terminate quickly to allow the receive site to begin a reply transmission, if required. The AN/USQ-83(V) and the ANDVT TACTERM (CV-3591) use two different EOMs. The VSM supports both EOMs, and the selection is determined by an option switch on the CPU board.

System Shut-down

As the VSM is transmitting the message data, it is also checking for the end of the transmission by use of the RTS or PTT signals. When the end of a transmission is detected, the VSM transmits the data remaining in its buffers followed by the EOM, and then releases the Power Hold control signal to turn off the power.

WAVEFORM SPECIFICATION

The waveform transmitted by the VSM is compatible with the 2400-bps Data-A mode used in the AN/USQ-83(V) and the ANDVT TACTERM (CV-3591). Compatibility with the ANDVT requires the use of the modem processor unit/voice processor unit (MPU/VPU) optional front panel with the switches set to MPU and 24-NOCODEWORD. Other configurations of the ANDVT are not supported. The USQ-83 must be configured for the Data-A mode at 2400-bps data rate.

Waveform Description

This waveform has three separate multitone sections for transmission preamble, data modulation, and EOM indication. The preamble is used for Doppler acquisition and frame- and bit-sync acquisition. The transmission sequence begins with a four-tone, unmodulated Doppler preamble, which is used by the receive modem to measure and correct for the Doppler offset of the received signal. The frame-sync preamble follows and consists of three biphase modulated tones that allow the receive modem to acquire frame synchronization. Sixteen-tone binary (biphase) differential phase shift keying (BDPSK) modulation allows acquisition of synchronization. Data transmission uses 16-tone QDPSK modulation of the user data. Transmission is terminated by sending the EOM indicator by use of 16-tone modulation.

The frame rate of the modem is 75 frames per second resulting in a frame period of 13.3 ms. This frame period is constant throughout the preamble, data modulation, and EOM portions of each transmission. By using the 16 tones and quaternary modulation, the resultant user data rate is 2400 bps.

Doppler Preamble

Each transmission begins with the Doppler preamble. This portion of the transmission allows the receive modem to detect signal presence and to correct frequency offset between the transmit and receive modems. The Doppler preamble consists of four unmodulated tones with equal amplitudes and with initial phases selected to minimize the ration of peak to RMS amplitude of the composite signal. The duration of the Doppler preamble is 24 frames, or 0.32 s. Selecting the short preamble by use of an option switch in the VSM, the duration is reduced to 8 frames, or 0.11 s. Table 1 lists four Doppler tones and their recommended initial phases.

Frame-Sync Preamble

The frame-sync preamble immediately follows the Doppler preamble and is used in the receive modem to determine frame boundaries and establish frame synchronization. The sync preamble consists of three tones phase modulated 180° at the frame rate. The three tones have equal amplitudes, and the initial phases are selected to minimize the ration of peak to RMS amplitude of the composite signal. The duration of the sync preamble is eight frames, or 0.106 s. Table 2 lists the three sync tones and their recommended initial phases.

Table 1 — The Doppler Portion of the Premble Uses Four Unmodulated Tones

Tone Number	Frequency (Hz)	Phase (Radians)
1	787.5	0.0
2	1462.5	1.81
3	2137.5	1.81
4	2812.5	0.0

Table 2 — The Frame-Sync Portion of the Preamble Uses Three Biphase Modulated Tones

Tone Number	Frequency (Hz)	Phase (Radians)
1	1125.0	0.0
2	1800.0	1.57
3	2475.0	0.0

Bit-Sync Preamble (Epoch)

The third part of the modem preamble is called the epoch and is used by the receive modem to determine bit synchronization and to identify the beginning of user data. Table 3 lists the 16 tones in the frequency library used in the epoch. The epoch immediately follows the sync preamble and begins with the transmission of a phase reference frame. The 16 tones have equal amplitudes, and the initial phases are selected to minimize the ration of peak to RMS amplitude of the composite signal. The epoch transmission uses biphase DPSK modulation with a 0 bit encoded as $+90°$ phase shift, and a one bit encoded as $-90°$. The information transmitted in the epoch is a 15-bit pseudo-noise (PN) sequence generated from the polynomial $x^4 + x + 1$ with an initial load of all ones in the sequence generator. The sequence is transmitted 16 times during a period of 15 frames after the phase-reference frame. Table 4 lists the bit assignments for the 240 bits transmitted by using the 16 tones over the 15 frames of the epoch transmission.

Data Modulation

After transmission of the preamble, data modulation begins by sending a 16-tone phase reference frame with initial phases chosen to minimize the peak to RMS of the output waveform. The modulator accepts 2400-bps of user data and transmits 32 bits per frame by using four-phase DPSK modulation of the 16 tones in the frequency library of Table 3. The data consist of 32 consecutive uncoded bits assigned to 16 dibits as specified in Table 5. The assignment of dibits to individual tones corresponds to the tone number (i.e., dibit number one is assigned to tone number one, etc.). The

Table 3 — A 16-Tone Frequency Library Is Used For the Bit-Sync Portion of the Preamble, Data Modulation, and the EOM Transmission

Tone Number	Frequency (Hz)	Tone Number	Frequency (Hz)
1	900.0	9	1800.0
2	1012.5	10	1912.5
3	1125.0	11	2025.0
4	1237.5	12	2137.5
5	1350.0	13	2250.0
6	1462.5	14	2362.5
7	1575.0	15	2475.0
8	1687.5	16	2587.5

Table 4 -- The Bit-Sync Portion of the Preamble (Epoch) Uses a 240-Bit Fixed Sequence with Fixed Frequency Assignments

Tone Number	Frame 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	1	1	1	1	0	0	0	1	0	0	1	1	0	1	0
2	1	1	1	0	0	0	1	0	0	1	1	0	1	0	1
3	1	1	0	0	0	1	0	0	1	1	0	1	0	1	1
4	1	0	0	0	1	0	0	1	1	0	1	0	1	1	1
5	0	0	0	1	0	0	1	1	0	1	0	1	1	1	1
6	0	0	1	0	0	1	1	0	1	0	1	1	1	1	0
7	0	1	0	0	1	1	0	1	0	1	1	1	1	0	0
8	1	0	0	1	1	0	1	0	1	1	1	1	0	0	0
9	0	0	1	1	0	1	0	1	1	1	1	0	0	0	1
10	0	1	1	0	1	0	1	1	1	1	0	0	0	1	0
11	1	1	0	1	0	1	1	1	1	0	0	0	1	0	0
12	1	0	1	0	1	1	1	1	0	0	0	1	0	0	1
13	0	1	0	1	1	1	1	0	0	0	1	0	0	1	1
14	1	0	1	1	1	1	0	0	0	1	0	0	1	1	0
15	0	1	1	1	1	0	0	0	1	0	0	1	1	0	1
16	1	1	1	1	0	0	0	1	0	0	1	1	0	1	0

Table 5 — Data Bits are Paired into Dibits for User Data Modulation

Dibits	Bits		Dibits	Bits	
(Odd, Even)	Odd	Even	(Odd, Even)	Odd	Even
1	1	2	9	17	18
2	3	4	10	19	20
3	5	6	11	21	22
4	7	8	12	23	24
5	9	10	13	25	26
6	11	12	14	27	28
7	13	14	15	29	30
8	15	16	16	31	32

transmitted phase at the beginning of a given frame is defined as the signal phase at the beginning of the previous frame plus the phase shift owing to the user data. The phase shift owing to data is defined as specified in Table 6.

Table 6 — Gray Coding Is Used for DPSK Modulation

Dibit (Odd, Even)		Differential Phase Change
0	0	45°
0	1	135°
1	0	315°
1	1	225°

End Of Message Indicator

The EOM indicator is transmitted as a means of rapidly terminating a transmission and providing a minimum turn-around between transmissions. Two types of EOM transmission are supported, the AN/USQ-83 method and the ANDVT TACTERM method

ANDVT TACTERM End Of Message

The ANDVT TACTERM EOM indicator uses the normal modulation but sends a deterministic data sequence that is permuted based on frame number. The EOM consists of a block of eight frames

of data with 32 bits of the EOM transmitted each frame. A fixed, 256-bit maximal length PN sequence is the basis for the EOM and is listed in Table 7 giving the hexadecimal values for the eight frames.

Table 7 — The ANDVT TACTERM
Uses an EOM PN sequence

Frame	Hexadecimal Values							
1	0	3	A	4	7	1	0	0
2	B	5	0	4	E	C	9	3
3	5	E	D	F	0	D	3	5
4	3	9	E	3	6	1	1	7
5	E	5	4	A	2	5	A	3
6	B	3	2	F	D	E	6	E
7	A	7	D	5	7	0	6	2
8	B	1	E	8	7	F	9	0

The actual information transmitted in each of the eight frames of the EOM is the exclusive Or of the sequence in Table 7 with a dynamic cover sequence. The dynamic cover sequence is generated by successive states of a 32-bit maximal length shift register. This shift register has the following initial hexadecimal fill value:

AE54715A

The initial fill value is the value used in the first frame following the data modulation phase reference frame. On each successive frame the dynamic cover is updated as follows: The shift register contents are shifted left by one bit. If the bit shifted out is a one, then the entire register is exclusive Or'ed with the following hexadecimal sequence:

00400007

The 32 bits of EOM to be transmitted are the result of exclusive Or'ing the corresponding EOM fixed sequence number with the current dynamic cover sequence.

The resulting 32 bits per frame of EOM are mapped into the 16 tones as follows: Eight hexadecimal values represent 16-dibit values. For each hexadecimal value the most significant two bits are the left dibit and the least significant two bits are the right dibit. The left dibit from the left hexadecimal value is phase encoded into tone 16, which is 2587.5 Hz, and the right dibit from the right hexadecimal value is phase encoded into tone number 1, which is 900 Hz. The remaining 14 dibits are phase encoded onto their corresponding tones. The phase encoding is the same format as normal data modulation.

AN/USQ-83 End Of Message

The AN/USQ-83 EOM indicator uses a fixed modulation scheme, which is transmitted for eight frames. During these eight frames, the odd numbered tones are differentially phase shifted 10° and the even numbered tones are differentially phase shifted 170°.

FUTURE PLANS

This report has addressed the initial development of the VSM. This preliminary effort provides a HF modem modulator but requires external demodulation for receive functions. Development of demodulation functions compatible with the current modulator are planned. Implementation of other waveforms (e.g., FSK) are also planned to provide compatibility with other existing equipment. Other digital signal processing applications, such as speech processing, are being planned based on the VSM design.

CONCLUSIONS

The VSM development has given the ITD a basis for the design and construction of state-of-the-art signal processing products. Future efforts in modem and speech processing areas can use this design to implement new applications or develop new hardware based on the VSM design. The VSM provides a powerful tool that will continue to satisfy the signal processing needs of the Navy.