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E. N. Cartagena, B. W. Offord, and H. Walker

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San Diego, CA 92152-5000

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Previous attempts at fabricating vertical bipolar junction transistors (BJTs) on Silicon-on-Sapphire (SOS) have produced transistors with low Early voltages, high leakage currents and low current gain. These problems were attributed high density of microtwin and stacking fault defects at the surface of the silicon which caused enhanced diffusion of the emitter dopant across the base to the collector resulting in emitter-collector diffusion pipes. By utilizing the Double Solid Phase Epitaxy (DSPE) process and limiting the furnace anneals for the base, emitter and collector dopants the effect of emitter-collector shorts on device performance can be reduced. Vertical NPN bipolar junction transistors were fabricated on DSPE improved SOS using conventional furnace anneals. Transistors with an effective emitter area of 40 square microns were measured for current gain (β_{DC}) and Early voltage (V_A). Functional devices with β_{DC} values of up to 70, V_A values of 40 volts and f_T values of 2.4 Gigahertz were recorded.

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E. N. Cartagena	(619) 553-5501	Code 554

VERTICAL NPN BIPOLAR JUNCTION TRANSISTORS FABRICATED IN SILICON-ON-SAPPHIRE

E. N. Cartagena, B. W. Offord and H. Walker
Naval Ocean Systems Center, Solid State Electronics Division,
Code 554 and Code 553, San Diego, CA 92152-5000

Previous attempts at fabricating vertical bipolar junction transistors (BJT's) on Silicon-on-Sapphire (SOS) have produced transistors with low Early voltages, high leakage currents and low current gain[1]. These problems were attributed high density of microtwin and stacking fault defects at the surface of the silicon which caused enhanced diffusion of the emitter dopant across the base to the collector resulting in emitter-collector diffusion pipes. By utilizing the Double Solid Phase Epitaxy (DSPE)[2] process and limiting the furnace anneals for the base, emitter and collector dopants the effect of emitter-collector shorts on device performance can be reduced. Vertical NPN bipolar junction transistors were fabricated on DSPE improved SOS using conventional furnace anneals. Transistors with an effective emitter area of 40 square microns were measured for current gain (β_{DC}) and Early voltage (V_A). Functional devices with β_{DC} values of up to 70, V_A values of 40 volts and f_T values of 2.4 Gigahertz were recorded.

A thin SOS film (0.27 micron) was regrown with the DSPE process to reduce the microtwin defect concentration. This improved film was implanted with phosphorus and annealed. Further epitaxial deposition resulted in a structure with a low resistance buried layer with thickness ranging from 2.5 to 10 microns. Standard bipolar processing was adhered to in subsequent steps with the intrinsic base, extrinsic base, and emitter all formed by ion implantation. Three different base dosages were used in this process with base widths varying from 0.25 micron to 0.40 micron. Table I summarizes the variations of processing performed in this particular lot of wafers along with the associated β_{DC} values that were obtained. All furnace anneals subsequent to epitaxy deposition was limited to 950° C to minimize junction leakage from the formation of emitter-collector pipes prevalent in BJT's formed in unimproved SOS.

WAFER I.D.	EPI THICKNESS (micron)	BASE IMPLANT (@ 100KeV)	β_{DC}
1	2.60	5E12	74
2	2.56	1E13	40
4	3.61	5E12	60
5	3.63	1E13	35
6	3.58	2E13	23
7	4.85	5E12	63
8	4.83	1E13	34
11	10.18	1E13	26
12	10.16	2E13	15

Table I
Process variations for vertical bipolar junction transistors fabricated in DSPE improved SOS material.

A common emitter characteristic curve for a BJT fabricated in DSPE improved SOS is shown in Figure 1. It can be seen from this sample that the effects of enhanced diffusion along dislocations causing emitter-collector shorts is minimized by utilizing the DSPE process prior to epitaxy deposition. A similar wafer that had not received the DSPE improvement process exhibited poor common emitter characteristics and showed no modulation of collector current with variations in the base-emitter voltage. A plot of Early voltage vs. epitaxy thickness is shown in Figure 2 for 4 samples that went through the DSPE process with the same base implant values. In all cases the extracted

Early voltage is significantly higher than that of a corresponding unimproved sample which had an Early voltage less than 1 volt. However, it can be seen that as the film thickness is reduced from 3.6 microns to 2.56 microns the Early voltage decreases from 13 volts to 10 volts implying an increase in defects within the emitter area. Above the 3.6 micron thickness the Early voltage changes very little, i.e. at 10 microns the Early voltage is 14 volts. This is consistent with higher residual twinning defect concentration closer to the silicon-sapphire interface.

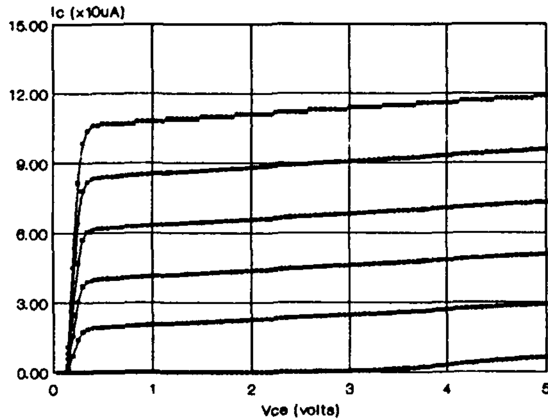

Figure 1 Common emitter curves for a BJT fabricated on SOS with an effective emitter area of 40 square microns. I_b steps of 1 μA.

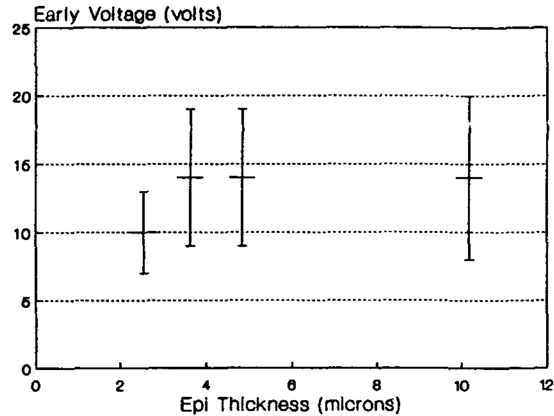

Figure 2 Early Voltage (V_A) vs. epi thickness variations.

[1] F.P. Heiman and P.H. Robinson, "Silicon-on-Sapphire Epitaxial Bipolar Transistors", *Solid State Electronics*, 11, pp. 411-418 (1968).

[2] A. Gupta and P.K. Vasudev, "Recent Advances in Hetero-Epitaxial Silicon-on-Insulator Technology, Part II", *Solid State Technology*, 26, 129 (1983).

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