Northeast Semiconductor, Inc.

767 Warren Road, Ithaca, New York 14850
Office: (607) 257-8827
Fax: (607) 257-7540

November 26, 1991

Dr. Erhard Schimitschek, Scientific Officer
ATTN: Code 808
REF: N00014-91-C-0222
Naval Ocean Systems Center
271 Catalina Boulevard
San Diego, CA 92152-5000

Re:	Contractor	:	Northeast Semiconductor, Inc.
	Address	:	767 Warren Road, Ithaca, NY 14850
	Req. No.	:	s405811srv02/17 APR
	Contract No.	:	N00014-91-C-0222
	Report Date	:	November 26, 1991
	Report Title	:	First Monthly Technical Report
	Period Covered	:	October through November, 1991

Dear Dr. Schimitschek:

Northeast Semiconductor, Inc. encloses its First Monthly Technical (Line Item #0002) pursuant to the provisions of contract Section B entitled, "Supplies or Services and Prices/Costs" for the period of October through November, 1991.

Innovative Techniques for the Production of Low Cost 2D Laser Diode Arrays

1.0 OBJECTIVE

The primary objective of this program is to develop a low cost, high yielding methodology for processing, packaging and characterization of MBE grown two dimensional high power laser diode arrays. Projected increases in overall yield of AlGaAs diode lasers would reduce manufacturing cost from the current $10 to $20 per peak watt to below $3 per peak watt. Emphasis will be placed on innovative packaging techniques that will utilize recent advances in diamond heat sinking technology.

2.0 PROGRAM METHOD AND SCHEDULE

This program consists of four phases which will demonstrate reduced manufacturing cost and improved device performance of NSI's MBE laser diode arrays. The four phases listed below will result in milestones in processing, packaging, and testing along with delivery of the specified number of 5-bar laser arrays.

(i) Concept phase: Conceptual design and organization of this phase II program. NSI will utilize the current side cooled strained relief package to manufacture 5-bar laser diode arrays for base line evaluation. (Deliverables: 3 5-bar arrays.)

(ii) Backplane phase: Development of a copper backplane cooling technology that incorporates CVD diamond submounts. This phase will also include the completion of room temperature photoluminescence development. (Deliverables: 5 5-bar arrays.)

(iii) Diamond Backplane phase: Develop a CVD diamond backplane cooling scheme that will utilize smaller CVD submounts. The reduction in submount size is to decrease the thermal resistance from the laser bar to the backplane. (Deliverables: 5 5-bar arrays.)

(iv) Liquid Cooled Submount phase: An innovative liquid cooled package will be developed. The CVD diamond submounts will be hermetically sealed, electrically isolated and liquid cooled. (Deliverables: 5 5-bar arrays.)

The following global issues not mentioned above will be investigated continuously throughout all four phases of this program:

(1) design and development of a mask set to increase processing and packaging yields,

(2) development and updating of MBE growth software,

(3) design and development of an in-house facet coating station,

(4) evaluation of different facet coating materials,

(5) development of automated tests,

(6) life test and burn-in development.

The master schedule for this program is shown in Table 1. Each phase will require wafer growth, processing, assembly and test. The schedule shows the estimated number of sample fabrications and tests, as well as the time of hardware deliverables and reports.

3.0 PROGRESS THIS PERIOD

3.1 Wafer Growths

As of this date, no wafers have been grown for this contract. NSI MBE machines are currently undergoing a rigorous bakeout and recalibration exercise to improve the quality and performance of the material. It is estimated that wafer growths will begin for this contract in the second week of December.

3.2 Processing

Current efforts are focussed on designing a new mask set. The new mask set will increase processing yield by providing a metalization lift off in the continuous scribe paths. This, in conjunction with the elimination of individual bar numbers, will reduce the risks of current leakage. Also included in this mask set will be a series of test bars to perform pre-packaging evaluations and screening to increase yield.

A facet coating experiment is currently underway. Three facet coating runs were performed by Evaporated Metal Films, Inc. of Ithaca (EMF). Each run had a different front facet coating material applied to determine their effects on device performance and reliability. The three front facet materials being evaluated are: TiO_2, Ta_2O_5, and Al_2O_3 & SiO while the rear facets remain constant with Al2O3. These arrays will be life tested in N_2 and air and compared to NSI's standard Al_2O_3 front facet coating. Results will be included in the next monthly report.

3.3 Testing

Photoluminescence (PL) measurements are done on all of NSI's laser wafers. PL data does give a good indication of device wavelength. However, correlation between device performance and PL has not yet been established. Efforts are being made to automate the PL measurements and correlate PL intensity to laser diode performance.

Progress has been made in designing a new, more reliable life test pulser. The pulser now in use has a history of frequent circuit failures. Prototyping should be completed by the end of December.

3.4 Assembly and Packaging

Major development has taken place this period to increase packaging yield through improvements to the solder joint. Initially, NSI utilized a 50 µm thick InPb solder preform which resulted in excessive solder causing various package failures.

Next, 100% indium plating was investigated. Approximately 15 µm of In solder was plated, but was plagued by voids and unknown contaminations. Arrays were successfully fabricated with In plated solder, but due to excessive voids in the solder joint and the enormous labor involved, this approach was abandoned.

Evaporation of the solder was then investigated. NSI has successfully evaporated 100%In and InPb composition onto the submounts, which has resulted in an enormous increase in packaging yield Although solder evaporation has been reproducible for NSI, more development needs to be performed on the optimal thickness and composition required.

Efforts are also being taken to evaluated CVD diamond vendors for the 2nd, 3rd and 4th phase of this program. Figure 1 shows the proposed CVD diamond submount that will be used for metalization evaluation and development of the copper backplane technology.

4.0 PLANS FOR DECEMBER

For the month of December, NSI plans to grow a minimum of four wafers for this program. Investigation will continue on facet coating materials, PL correlation to device performance, evaporated solder compositions/thicknesses, and CVD diamond. Design will begin for the in-house facet coating station. All global issues mentioned in Section 2.0 will be addressed and continuously investigated during this program.

Very truly yours,

Michael J. Cook,
Principal Investigator
Northeast Semiconductor, Inc.

:nd
Encl: 1 Copy of 1st Monthly Technical Report

cc: (1 copy)
DCMAO Syracuse
ATTN: Mr. Robert Balstra,ACO
615 Erie Boulevard West
Syracuse, NY 13204-2408

(1 copy)
Director, Naval Research Laboratory
ATTN: Code 2627
Washington, DC 20375

(2 copies)
Defense Technical Information Center
Bldg. 5, Cameron Station
Alexandria, VA 22304-6145

(1 copy)
Strategic Defense Initiative Organization
ATTN: T/IS The Pentagon
Washington, DC 20301-7100

TABLE 1. MASTER SCHEDULE FOR SBIR PHASE I
CONTRACT NO. N00014-91-C-0222

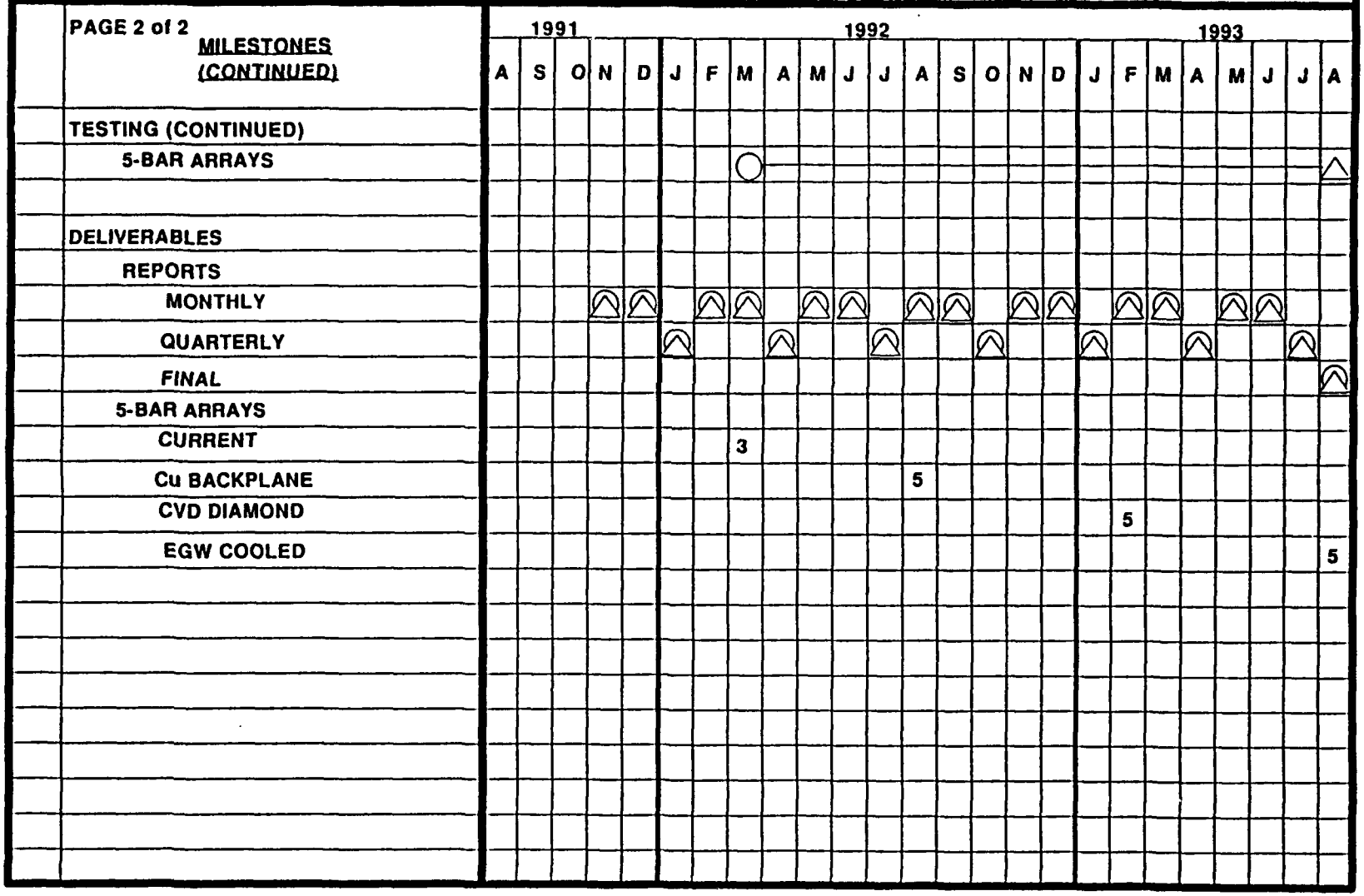
DEPARTMENT : LASER PRODUCT LINE
PROJECT(S) : ONR PHASE II
N00014-91-C-0222

KEY
○ : Start Task
◇ : Milestone
△ : Completion Date 1
▽ : Completion Date 2

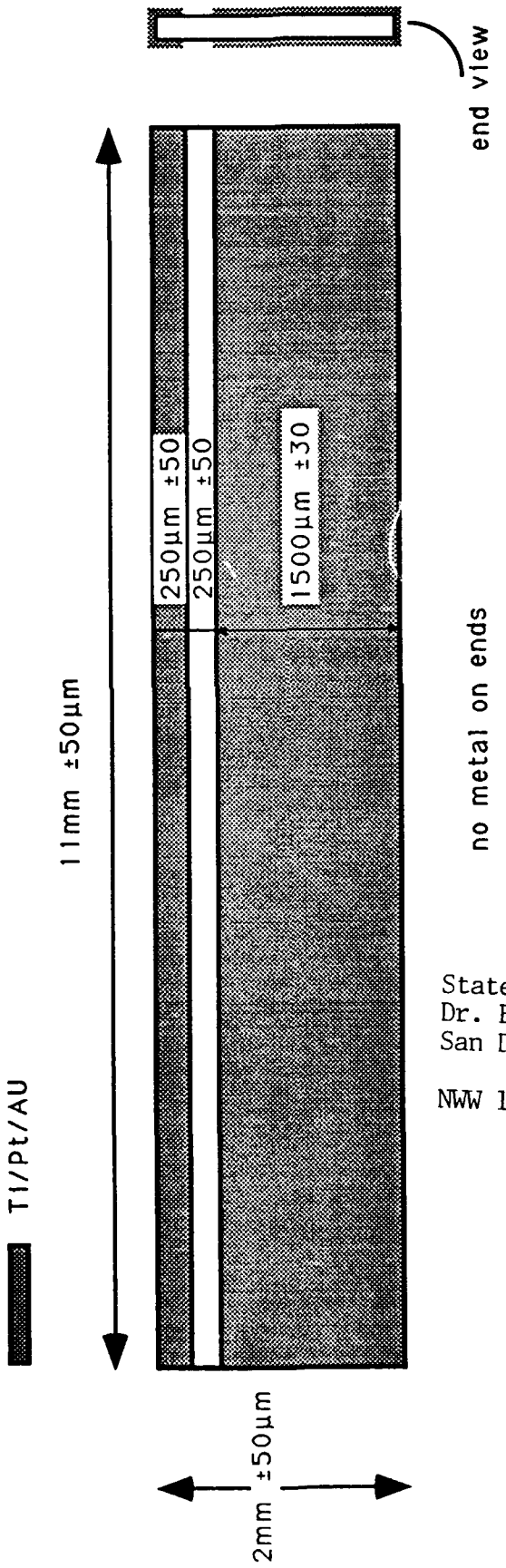
DATE : NOVEMBER 20, 1991
PREPARED BY : GEOFFREY T. BURNHAM
APPROVED BY :

PAGE 2 of 2

MILESTONES (CONTINUED)



Innovative Techniques for the Production of Low Cost 2D Laser Diode Arrays



Statement A per telecon
Dr. Erhard Schimitschek NOSC/Code 804
San Diego, CA 92152-5000

NWW 1/21/92