TO: ANDY FOX

FROM: S. ESPY

SUBJ: TECHNICAL PROGRESS FOR IDDGA - OBP UPGRADE

The following paragraphs describe progress that has been made since 10/15/91.

TOPIC 1 - OBP-80 CHIP SET STATUS

We continue to consume large amounts of test time at Vitesse. At present, 11/5/91, we have functional devices for all seven custom chip types required by the OBP80 board. We have sufficient quantity of devices on hand to build several engineering models. The physical characteristics of the chip set are shown in Table 1. The power shown in the table includes typical I/O loading.

The design target was 50 uW/Fet for internal logic. As you can see, the variability of the power with each design indicates that we are still driven by I/O power. Note that TIC, DMC, MCS, and IPR II have an ECL interface, and the COMM1 has TTL inputs and outputs. All others have GaAs. The I/O count is also a contributing factor.

TABLE 1 OBP80 Chip Set Physical Characteristics

Measured OBP80 Chip Set Characteristics				
Name, Revision, Package	QTY Used	FETs Each	Chip Quiescent Power	Power/Fet
COMM1, 256	2	16 k	3.0 W	225 uW
DMC, 344	1	15 k	3.0 W	200 uW
GALU, 344	1	73 k	6.6 W	90 uW
IPR II, 344	1	26 k	4.4 W	169 uW
MCS, 344	1	37 k	5.5 W	149 uW
MPY II, 256	1	27 k	3.0 W	111 uW
TIC, 256	1	15 k	3.4 W	227 uW
Total Chipset		225 k	33.1 W	147 uW

Although all seven chip types are functional, we continue to experience some test problems. The yield on MCS, MPY II, TIC, COMM1 and DMC is sufficient (>20%) to warrant considering these designs 'production ready'. The GALU and IPR II yields (~5-6%) warrant some concern over the production readiness of the design. For low volume applications like ours, cost is not as much the cause for concern as reliability. Low yield can sometimes belie design problems which will limit the device tolerance to environmental factors.

A question was raised at the CDR in August as to whether our GaAs I/O cells would work across the temperature range. The answer is yes it will. We used the Thermal Stream at Vitesse to collect some preliminary data on the MPY II device. The Thermal Stream has a limited temperature range because it only blows air across the surface of the device. The case temperature was measured on the opposite side of the case from the air stream source.

Consider the data of Figure 1 very carefully. The bold lines represent the the MPY II GaAs output driver swing range. The worst case output high is produced at high temperature and when VTT = -2.2 V. The worst case output low voltage is produced at high temperature and when VTT = -1.8 V. This is seen by the bold lines converging to the right.

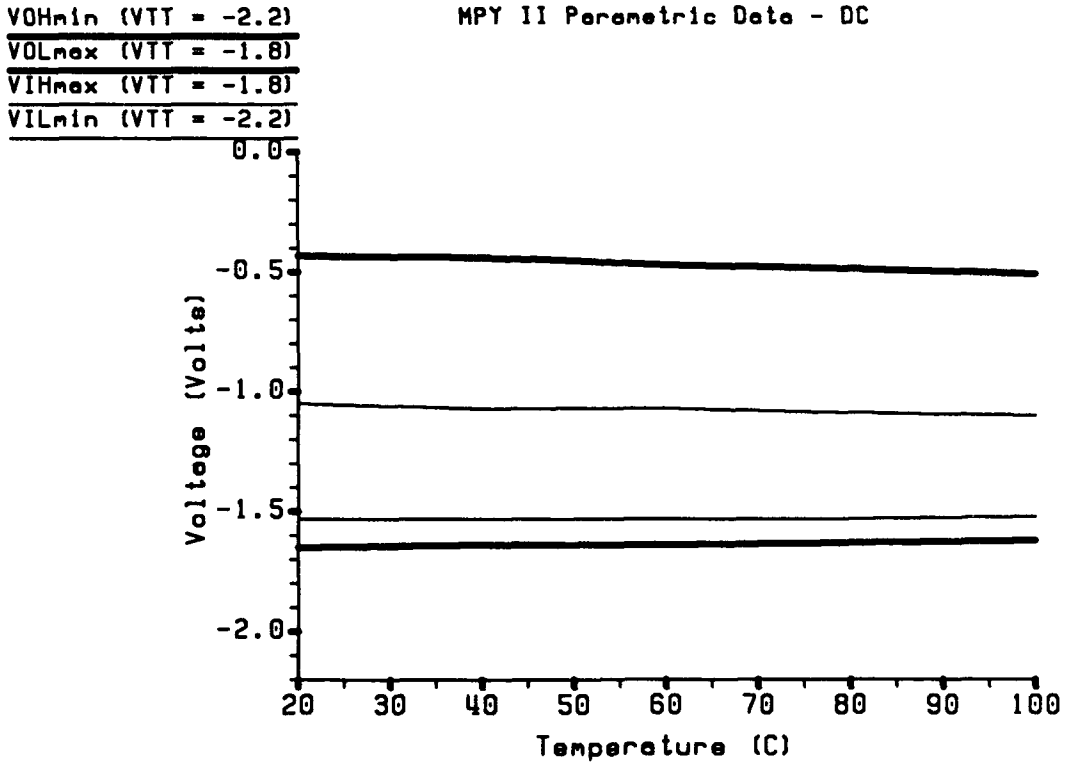

Figure 1 MPY II Voltage Margins vs Temperature

It is important for the VIH and VIL lines (the narrow ones) to be always within the bold lines. This insures that the output driver will always swing a sufficient amount to allow the input receiver to detect the change. GaAs differs from TTL in that the power supply is the reference instead of ground. This manifests itself by way of the worst case VIL occuring at VTT = -2.2 V. Similarly, the worst case VIH occurs when VTT = -1.8 V.

The data of Figure 1 would leave one to believe that the GaAs I/O would function across the range indicated, but that we have a very small margin on the low end. This is true, but is a function of the power supply being used as the reference. For instance, the bold VOL curve would drop by 400 mV if the power supply were changed to the -2.2 V level that was used to collect the worst case VIL data in the narrow line just above it.

Conversely, if the power supply voltage were changed to -1.8 V, the narrow line VILmin would raise by 400 mV. The bottom line conclusion is that even if a chip one one end of the board was operating at -1.8 V, and a chip at the other end was operating at -2.2V, the interface would still function across the temperature range.

The data presented above should indicate why we consider GaAs interface to be useful for local connect only, and should not be passed across connectors, cables, or other media which are prone to develop voltage drops.

A typical delay measurement was made during this test as well. The results are shown in Figure 2.

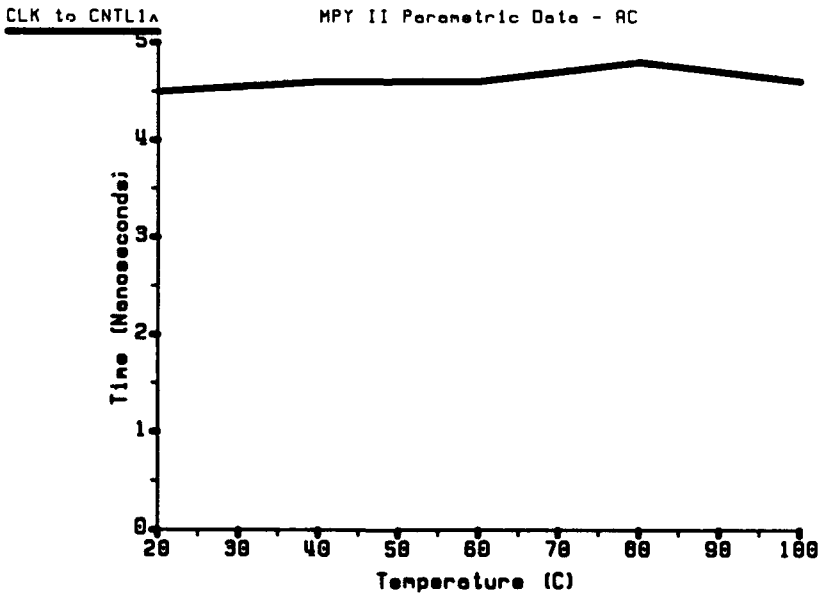

Figure 2 Typical MPY II AC Delay Characteristics

TOPIC 2 - SECS TESTER STATUS

We continue to test the SECS hardware and software since it was received from Analytyx last month. Figure 3 shows the portable SECS tester installed in the laboratory, along with the PC, power supplies, and test equipment. The PC software is responsible for controlling the printed wiring board in the SECS tester.

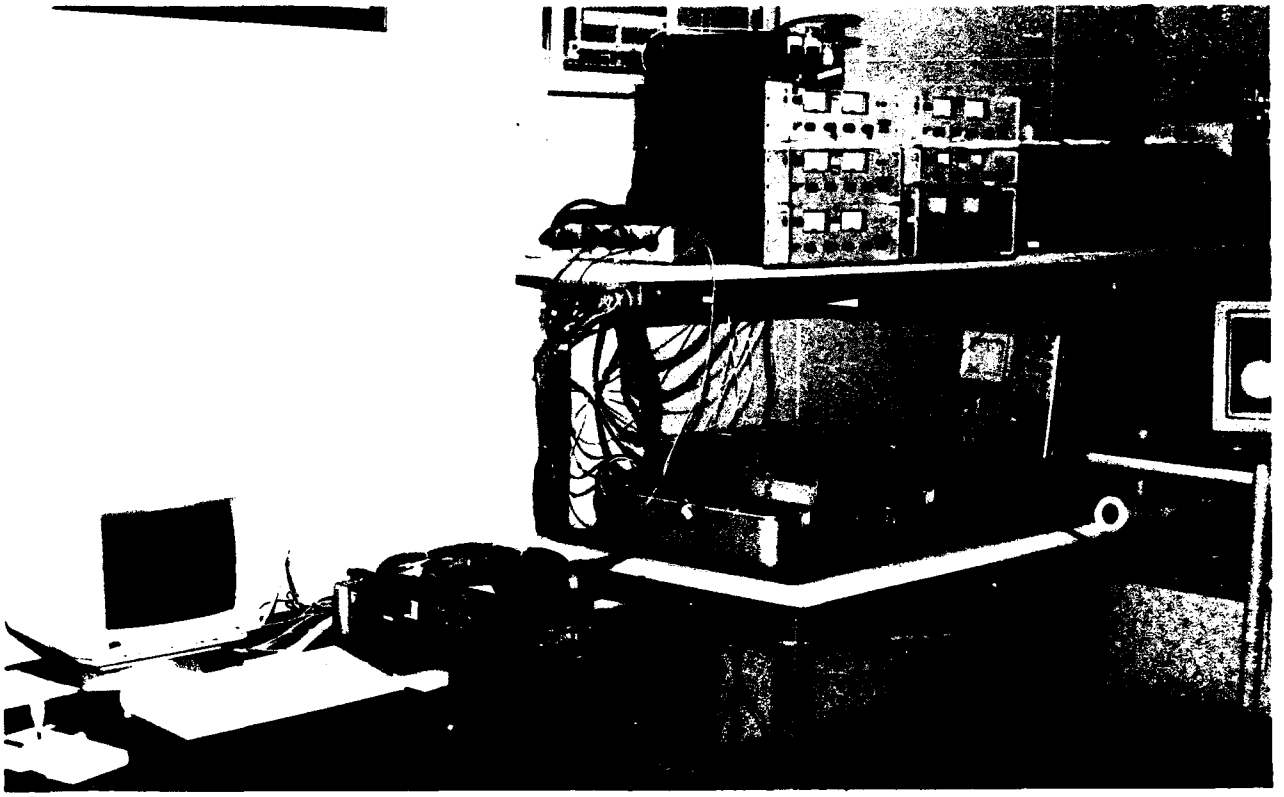

Figure 3 SECS Tester Installation

Figure 4 is a photograph of the inside of the SECS tester. The logic here can capture and assert JTAG (or any other protocol) control pulses onto the backplane connector. The board also converts the thermocouple data from the OBP80 CPU card so that this data can be read from the PC-386/20.

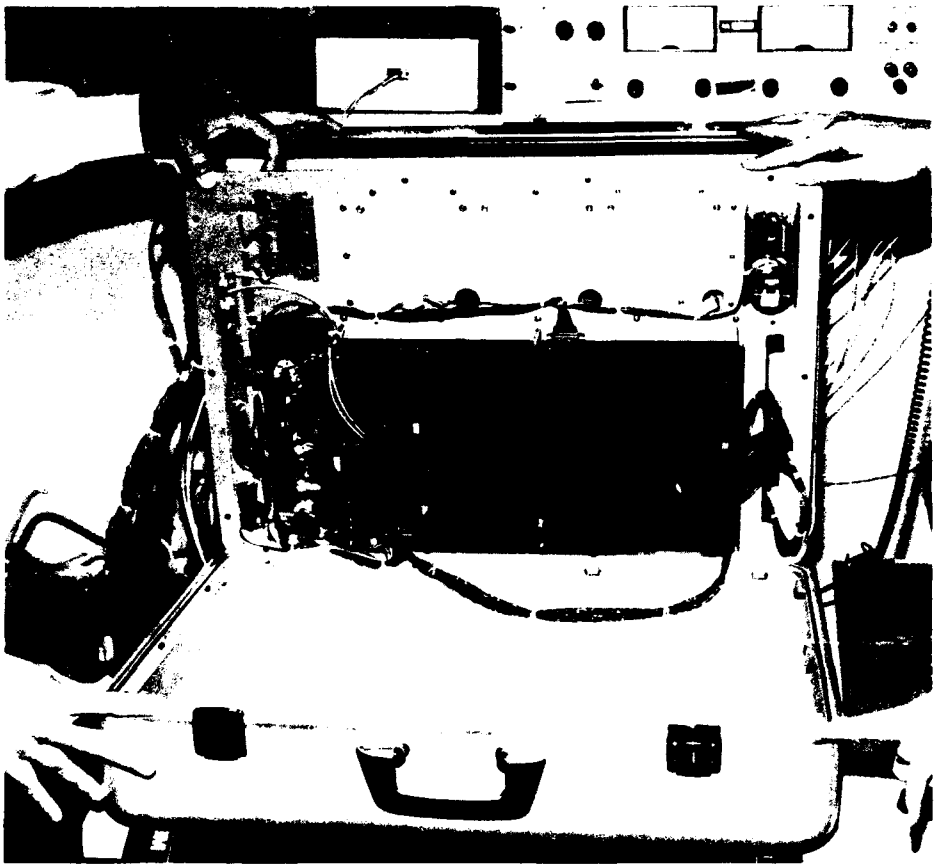

Figure 4 SECS Tester Hardware

We have been through numerous revisions of the software, and tremendous progress has been made in working toward the desired capability. The following capabilities are considered operational:

1. Software control of power supplies and power sequencing,

2. The JTAG macro capability hhas been installed. This feature has some fine options, such as the ability to generate a merged file of manually executed commands whose execution preceeded that of the macro file.

3. The download capability has been tested on short (2 line) programs. The download works fine. Read back capability will not be tested until the board is installed.

The overall impression of the system at present is that it is maturing nicely, and should be ready for initial board test on schedule (12/15/91). A portion of the JTAG protocol (total 600-700 TCLK pulses) has been observed for the two line microprogram mentioned above. Figure 5 is a screen capture on the DAS 9200 of a small portion of the download. The photograph illustrates the interaction between the PC-386/20 and the SECS tester.

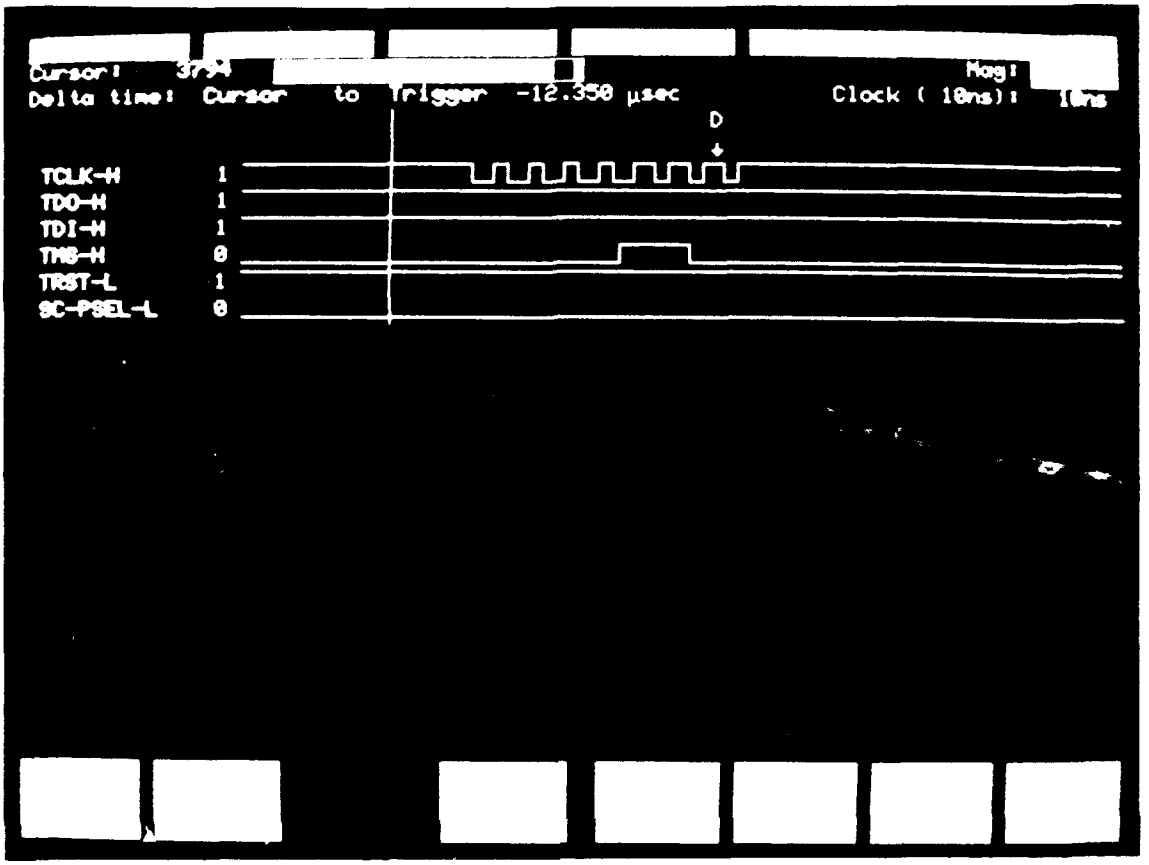

Figure 5 JTAG Protocol Logic Analyzer Screen Capture

The software on the PC pre-loads the serial register for each JTAG signal with a data stream to be sent to the GaAs JTAG controller on-board the TIC. It then issues commands to the SECS tester hardware to generate a variable length (1, 2, 4, 8) string of clocks. This flushes the registers contents out to the appropriate signal pins. Note that there is a significant spacing between pulse trains. This is a function of the PC-386/20 executing numerous machine cycles prior to enabling the next burst.

The protocol is absolutely correct, but not minimal. That is, the JTAG protocol allows redundant clock periods that do not change the machine state to be issued. Specifically, these clocks are used to streamline the SECS tester software control program subroutines. If the minimal JTAG protocol requires 5 clocks, it can be given 8 with the approriate number of 'idle state' commands.

This approach is extremely flexible, and has allowed the software to be modified as frequently as twice a day. Art Jeck and Gary North of Analytyx have come up with an excellent strategy for handling future growth with this tool.

TOPIC 3 - AIT/ MICROWIRE BOARD STATUS

The first prototype OBP80 CPU bare board has been received from AIT/Microwire. This board geometry looks good, but the solder tinning of the pad areas is not as uniform as we would like. It appears good enough to construct the first processor with, and is due to be shipped to SMTEK for component assembly by 11/25/91.

The Single Event Upset test board has also been received from AIT. During the week of 11/11/91 we will debug the software program used by the DAS 9200 logic stimulus module to verify the operation of the IPR. This should provide sufficient time to ship the unit to Brookhaven, NY by the test slot (11/21/91). The test plan agreed to between Todd Weatherford (NRL) and Doug Krening (Martin) should clearly demonstrate the suitablility of GaAs MESFET technology to fly in space environments, given the design situation present on the IPR device.

If you have any comments or questions regarding this memo, please call me at (303) 971-9276.

Steve Espy

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