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CAE TOOLS ASSESSMENT FOR TPS DEVELOPMENT (PRELIMINARY)

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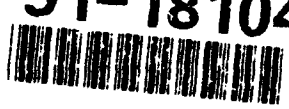

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This report discusses the application of Computer Aided Engineering (CAE) tools to the Test Program Set (TPS) development process, the selection of CAE tools for TPS development, and evaluation recommendations for CAE tools. Electronic design application tools were considered to establish a methodology for TPS development and provide a total computer based TPS development environment. These requirements dictate a highly integrated set of CAE tools which are targeted toward specific TPS development problems. The test strategy generation, testing requirements, reverse engineering, and Interface Device development are the specific TPS development problems investigated. The study will encompass a preliminary report (this report), an interim report and the final report.

The preliminary study selected the Cadence design environment for evaluation on the SUN workstation because of the open CAE software operating environment considerations, circuit representation capabilities and integration with the SABER analog simulation tool. In the PC environment, SONATA, PSPICE, ISPICE, and SILOS CAE

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Assessment For

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Executive Summary

This report discusses the application of Computer Aided Engineering (CAE) tools to the TPS development process, the selection of CAE tools for TPS development, and evaluation recommendations for CAE tools. Electronic design application tools were considered to establish a methodology for TPS development and provide a total computer based TPS development environment. These requirements dictate a highly integrated set of CAE tools which are targeted toward specific TPS development problems. The test strategy generation, testing requirements, reverse engineering, and Interface Device development are the specific TPS development problems investigated. Sun and 386/486 workstation based solutions were addressed. A key decision element is the evaluation of the SPAWAR developed Weapons System Testability Analyzer (WSTA) which only runs on a SUN or MicroVAX. The Cadence design environment was selected for evaluation on the SUN workstation because of the open CAE software operating environment considerations, circuit representation capabilities and integration with the SABER analog simulation tool. In the PC environment, SONATA, PSPICE, ISPICE, and SILOS CAE tools were selected because they are integrated under a common graphical interface, possess advanced features, and share circuit data. Application of SONATA, PSPICE, ISPICE, and SILOS 386/486 based CAE tools were selected to evaluate there effectiveness as a total design environment and as a point solution applied to separate TPS development tasks.

This report recommends moving to the concept verification phase by evaluating Cadence and WSTA on a SUN-3 workstation and SONATA, PSPICE, ISPICE, and SILOS on the 386/486 workstation for application to TPS development.

1.0 INTRODUCTION.

Producing quality and cost effective TPSs in a timely manner is the ultimate goal of the CASS off-load program. Over the past few years, many new technology innovations have evolved in computer aided design (CAD), computer aided engineering (CAE) and automatic TPS development tools. These tools warrant evaluation due to the large number and complexity of the UUTs involved in the CASS off-load. As a consequence to the immensity of the CASS off-load, TPS quality and cost factors require close scrutiny and management. CAE software tools and testability analyzers will help to assure TPS quality by improving the consistency of the TPS development process, generating testability parameters to measure quality of developing test strategies, assisting in ID prototype development, identifying the best diagnostic path (test strategy) and generating technical information for use during design reviews.

2.0 SCOPE.

Applied Research Laboratory is tasked with the evaluation of applying CAE tools to the TPS development process. The report covers the preliminary evaluation process and describes the CAE evaluated tools, their purpose and applicability to TPS development tasks, the CAE software tool selection process and the selection criteria for specific software tools.

3.0 TPS DEVELOPMENT TOOLS EVALUATION RATIONALE

Developing TPSs for many UUTs is a long, tedious, cumbersome and costly task. Any accurate and automated process introduced into the TPS development process will increase efficiency by: minimizing manual calculations and providing graphs and data lists required for analytical comparisons, smoothing performance variations between test engineer skills, increasing TPS quality, and decreasing TPS development costs. Specific areas that electronic design automation tools address in the TPS development process are listed below.

- Improves the consistency and quality of the TPS development process.
- Reduces TPS integration time by performing analysis on new ID designs for correction of electrical ID design errors. The ID simulation analysis increases productivity, thereby reducing the development cost. Simulation of the electrical CASS interface with the UUT discovers interfacing problems prior to TPS integration.
- Acquires hardcopy documentation for UUTs with little, no or poor quality data packages.

- Performs circuit/testability analyses :

  1. for the development of test strategies.

  2. to view the effect of varying component tolerances on circuit outputs using the Monte Carlo analysis technique. The calculation of accurate testing tolerances eliminates tolerance induced problems of retest OK (RTOK) or cannot duplicate (CND). This will cleanse the supply system of bad UUTs that test good.

  3. to verify new ID design through simulation.

  4. on existing UUT circuitry and determine the UUT I/O parameters (for UUTs with no or lacking I/O specifications) employing digital, analog and mixed-mode simulation.

  5. to quickly and accurately identify testability concerns for use in design reviews (organic and contracted lots) employing a testability analyzer, analog fault simulation and digital fault simulation.

CAE software tools and associated methodologies guide quality TPS development by :

1. centralizing the UUT information which allows for concurrent TPS task development because of common access of critical information.

2. entering UUT information into a CAE system serves as the master documentation copy.

3. sharing individual efforts on each TPS task and creating synergy in the TPS development process. Engineering data generated by test engineers is shared with documentation engineers.

4. allowing everyone to work with the latest verified data. Verification of UUT data is accomplished by comparison of the same information from different sources to assure the accuracy of the UUT information.

4.0 CAE TOOLS SUPPORTING TPS DEVELOPMENT TOOLS.

CAE and testability analyzer software tools are key to the TPS development process and require evaluation to test the tools utility and applicability for TPS development. Listed below are the CAE software tools required to develop each TPS deliverable.

* Test Program (TP) - testability analyzer, fault simulation, simulation and schematic capture.

* Circuit simulation is performed for:
  1. performance tests (Monte Carlo simulation)
  2. adjustment/alignment tests.
  3. diagnostic tests.

* Circuit fault simulation and the testability analyzer tools are applied to develop diagnostic fault isolation tests.

* Interface Device (ID) - Schematic capture, simulation, fault simulation.

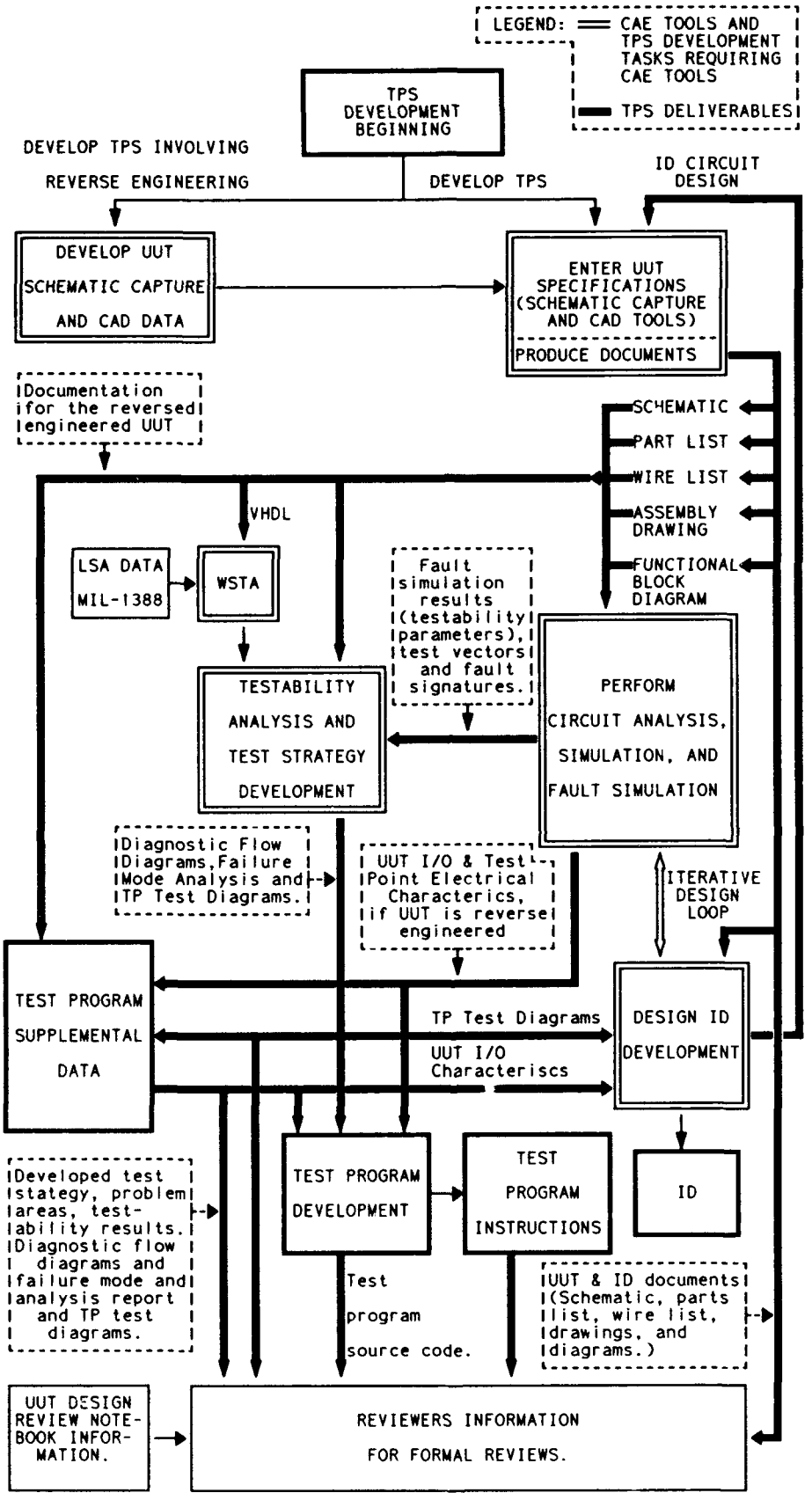
* Test Program Instruction (TPI) - Desktop Publishing.

* Test Program Supplementary Data (TPSD) - CAD, schematic capture, simulation and wordprocessor, if required for supplementary data generation or documentation regeneration.

5.0 TPS DEVELOPMENT INCORPORATING CAE TOOLS.

5.1 Overview. This section describes the incorporation of CAE software into the TPS development process. Figure 1. depicts the inter-relationship between CAE tools and the TPS development process. Doubled block lines show CAE tools and TPS development processes that are accomplished with a CAE system. Blocks with bold lines are the TPS deliverable development tasks. The CAE system is the heart of the design process and serves to alleviate the tedium of performing manual analytical comparisons, generating and reproducing documentation, providing essential design tools for TPS development and producing technical input for design reviews. Circuit analysis, circuit simulation and fault simulation CAE tools serve as cornerstone processes for testability analysis, test strategy, test program, and ID hardware development.

5.2 Schematic Capture Description. The three cases addressed in organic TPS development are the fully documented, incompletely documented, and undocumented UUTs. The incompletely documented and undocumented UUTs requires a partial or total reverse engineering effort. Documented TPS development requires the entry of the schematic circuit for generation of a simulator netlist data and VHDL data. A simulator netlist is required for the circuit simulation tool. VHDL netlist circuit description is a necessary input to the testability analyzer tool. Incompletely documented UUTs requires some reverse engineering for TPS development or application of CAE tools to derive the essential data for documentation.



TPS DEVELOPMENT
INCORPORATING CAE TOOLS
FIGURE 1.

UUT reverse engineering requires the development of connectivity and parts data into a format compatible for entry into the schematic capture software tool. Another output of the schematic capture tools are documents.

The UUT schematic, parts list, and wire list documents are an essential input for testability analysis and test strategy generation during the initial design phase of TPS development.

The TPS documentation consists of a schematic, parts list, wire list, assembly drawings and functional block diagrams. Schematic information is processed into a simulator netlist which is an input for circuit analysis in order to define the UUT's I/O electrical parameters. Reverse engineering and normal TPS development efforts require UUT I/O parameters to establish tolerance values for testing. Monte Carlo simulation techniques yield the variances in UUT output electrical characteristics. The UUT output characteristics establish testing tolerances for all UUTs tested in the field. Regeneration of previously existing documentation by CAE tools is often desirable due to the poor quality of the documentation.

5.3 Testability Analysis and Test Strategy Development. The testability analyzer of choice for CAE evaluation is the Weapon System Testability Analyzer (WSTA). WSTA was chosen because of its availability and suitability as a CAE tool which performs essential analysis during testability analysis and test strategy development. The direct or derived VHDL output from the schematic capture process is input into WSTA for analysis. Another input to WSTA is logistical support data. Logistical support data of replacement costs, replacement time and Mean Time Between Failure (MTBF) are factors considered by WSTA to arrive at a testing strategy. WSTA is the only testability analyzer to factor the logistical data into the decision making process of generating a testing strategy. Factoring in MTBF and historical failing parts increases test efficiency.

Testability analysis and test strategy development requires the results from circuit simulation and fault simulation tools to develop test vectors and interpret fault signatures. Fault coverage and other testability measures are derived through manual calculation of simulation results, fault simulation results or generated by a testability analysis program, WSTA.

The developed test strategy in the form of diagnostic flow diagrams and failure mode analysis and test program testing diagrams serve as crucial inputs to the test program, ID design, and formal design reviews. These documents are crucial because they are the essential input to test program and ID

design development and the document's content ultimately determines TPS quality.

5.4 Circuit Analysis, Simulation and Fault Simulation. Circuit analysis, circuit simulation and fault simulation is the key CAE tool for TPS development. The resulting simulation data is a direct input to every major TPS development task. The inputs for this CAE tool are the simulation netlist from the schematic capture process and manual operation by a CAE operator. The utility of simulation for TPS development is that simulation provides:

1. fault simulation results to calculate testability parameters.

2. UUT output fault signatures for faulted components, mainly for analog circuitry fault analysis.

3. UUT I/O and test point electrical values to establish testing tolerances for the test program and eliminate discovery of a testing tolerance errors during integration. Accurate test tolerances for all boards tested eliminates bad UUTs from the supply system.

4. UUT I/O and test point electrical values for UUTs that lack this information. Generate test program supplemental data.

5. UUT I/O and test point electrical values for ID design which are required during dynamic design development.

5.5 Design ID and Hardware Development. ID design development starts with the test program test diagrams which delineate the functional design of the ID. Matching CASS GPI to UUT I/O characteristics govern the electrical hardware design. The initial ID circuit design is documented by the schematic capture tool. A simulator netlist is generated, and the circuit is simulated. Simulation results are analyzed by the designer and the circuit is modified. An iterative design loop is formed by the designer, schematic capture, and circuit simulator. ID design documentation generated by the schematic capture and supplemental data are input to the formal design reviews.

5.6 Test Program Development. Diagnostic flow diagrams and test program test diagrams from test strategy development are input to the test program development task. Diagnostic flow diagrams or test strategy reports (TSRs) determine the testing sequence during the test program diagnostic testing phase. Test program test diagrams indicate the signal flow connection path between CASS source and sensor assets, the ID and the UUT for each test program testing phase.

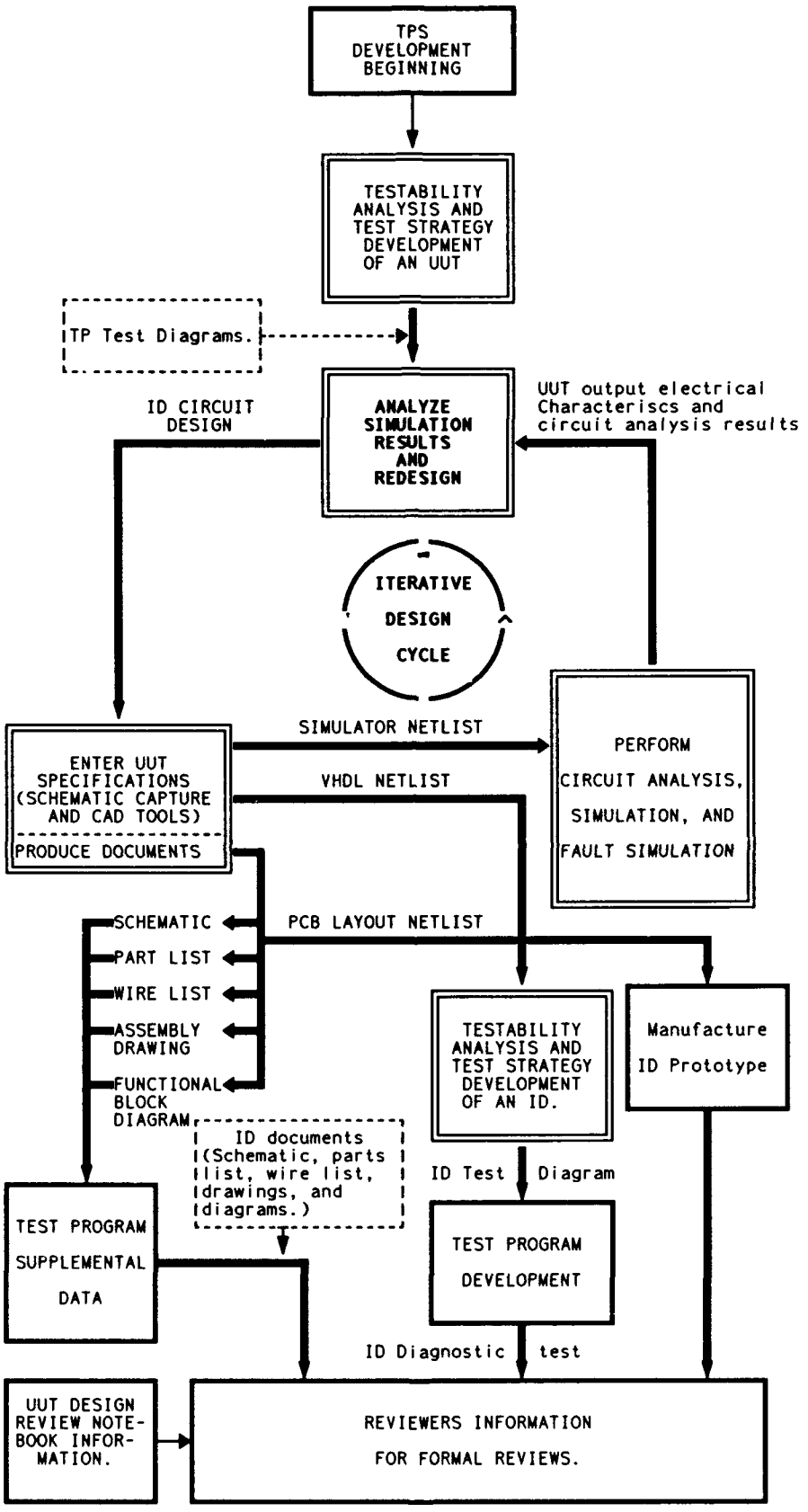
5.7 Organic ID Development. Figure 2 depicts the organic ID development process. Blocks and flow lines that are doubled show the CAE tools and processes aided by CAE tools and their contribution to the development process.

5.7.1 Description. During TPS development, if a CAE system were employed, all documentation for the ID would be developed in the computer. Obtaining hardcopy information easily and quickly is one advantage of using a CAE system. ID design information is available for performing ID circuit analysis and simulation, testability analysis and documentation for formal design reviews. The ID specifications are required as an input for testability analysis and generation of a test strategy. The iterative design cycle is illustrated with the three process blocks of analyze simulation results, entry of schematic information, and circuit simulation. The design/redesign analyze/simulate process ensures ID design quality is a designed-in feature before integration and prototype development begins. Once the ID design is stabilized, the design is analyzed by the testability analysis process to develop an ID test diagram for test program development. Test program development produces an ID diagnostic test. Additionally when the design is stabilized, prototype development is accomplished. The schematic capture interface with prototype development is through a PCB layout netlist.

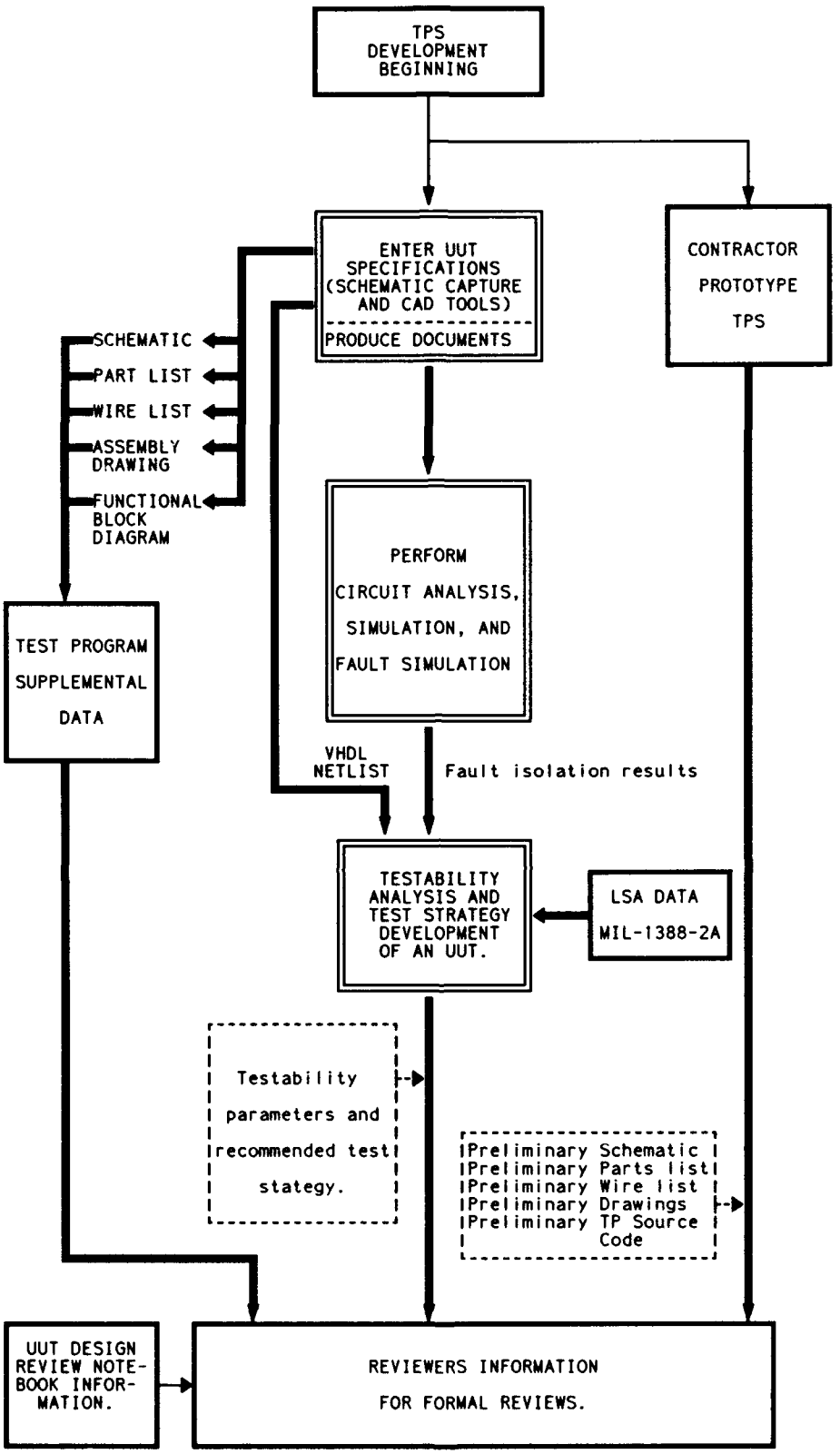
5.8 Verification of Contracted TPS. Figure 3 depicts integration of CAE tools into the contractor TPS verification process. Doubled block lines show where and how the CAE tools fit into the process.

5.8.1 Description. During contractor prototype TPS development, UUT design information is captured for use in circuit or system analysis, circuit or system simulation and testability analysis. The analyses results are reported to the reviewers, along with other pertinent information contained in the UUT Design Review Notebook. The information identifies testability concerns to ensure the problem areas are addressed by the developer.

Without a CAE system, the data collection and analysis task for prototype TPS review is very tedious, time consuming and may not be very thorough. A CAE system allows the government appointed reviewers access to circuit/system analysis results and testability concerns that are identified prior to any review process.



ID DEVELOPMENT
INCORPORATING CAE TOOLS
FIGURE 2.



VERIFICATION OF CONTRACTED TPS

INCORPORATING CAE TOOLS

FIGURE 3

6.0 EVALUATION

6.1 Overview.

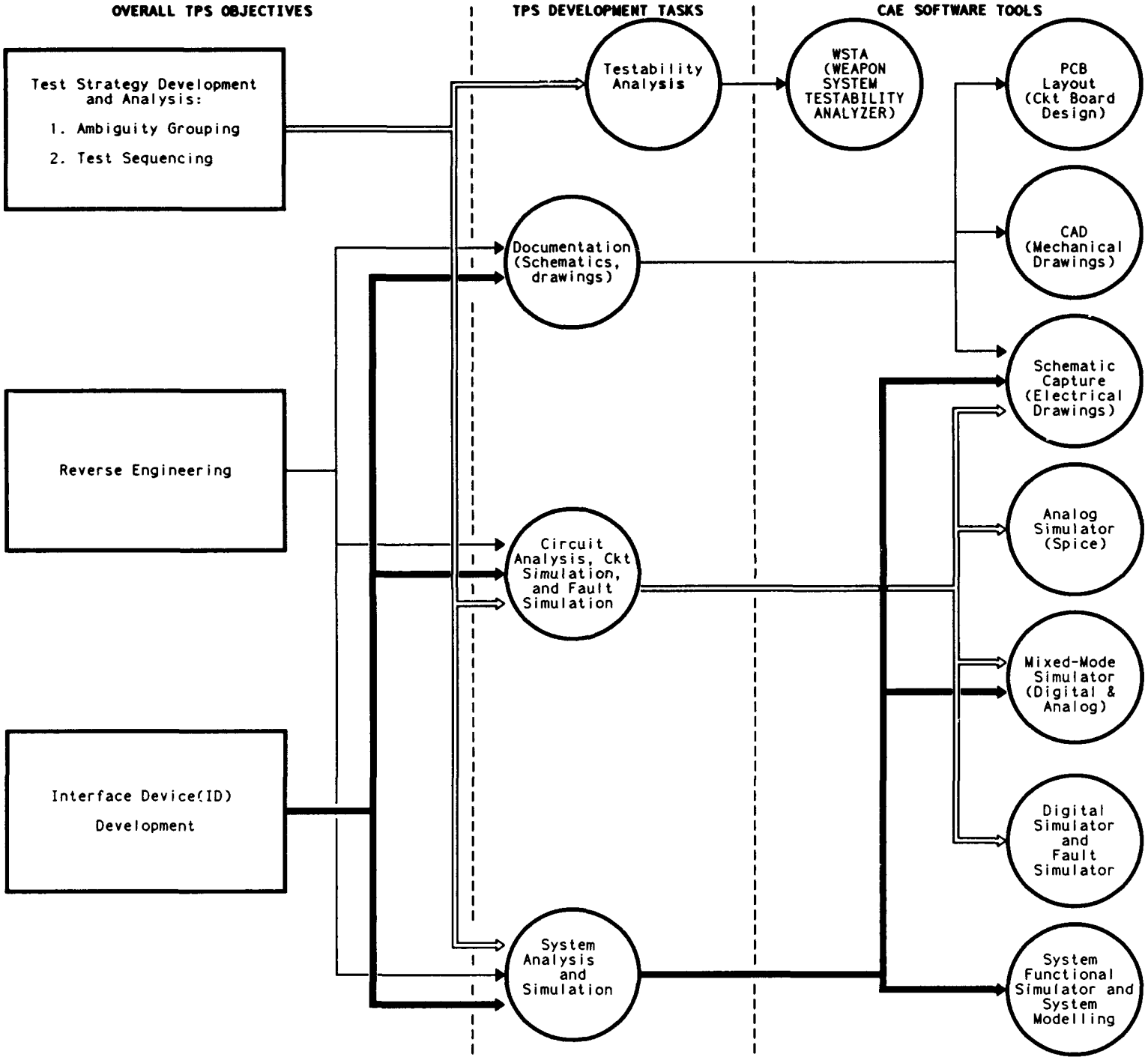
The evaluation is a two phased process covering the selection, application and value of CAE tools for TPS development. Preliminary evaluation, discussed in this report addresses the selection of CAE tools in support of TPS development objectives. The main evaluation covers the application and value of CAE tools for critical TPS development processes.

The preliminary evaluation involves:

1. the definition of overall TPS objectives
2. identifying tasks supporting those objectives
3. defining specific types of software tools in supporting the tasks
4. researching specific software tools for each type of CAE tool
5. selecting the CAE software tools.

The primary evaluation investigates CAE tool application for different development process methodologies concerning testability analysis, test strategy, ID design, and reverse engineering, through the application of CAE tools.

6.2 Preliminary Evaluation Approach. Preliminary evaluation starts with a task analysis approach where different TPS objectives are supported by the tasks required to accomplish those objectives. The tasks are supported by CAE tools required to accomplish the tasks. Figure 4. illustrates the preliminary evaluation approach. Test strategy and testability analysis, ID, and reverse engineering development are the objectives which require support with CAE tools. Tasks employing CAE tools are testability analysis, documentation, circuit analysis, circuit simulation, circuit fault simulation, system analysis and system simulation. CAE tools required to accomplish critical tasks are a testability analyzer, PCB layout, CAD, schematic capture, analog simulator, digital simulator, mixed-mode simulator, digital and analog fault simulators, and a system functional simulator.



CAE Tools Supporting TPS Objectives Figure 4.

TABLE 1 matches CAE software tool capability with TPS development tasks.

TABLE I

TPS DEVELOPMENT TASKS	SOFTWARE TOOLS REQUIRED
* PRODUCE HARDCOPY DRAWINGS AND STORE COMPUTER DATA FOR ANALYSES	* SCHEMATIC CAPTURE/LIBRARIES * CAD PROGRAM * PLOTTER/PRINTER DRIVERS

* CIRCUIT ANALYSIS AND SIMULATION	* COMPONENT VARIATION ANALYZER
	* DIGITAL SIMULATOR
	  * STIMULUS EDITOR
	  * LOGIC ANALYZER
	* ANALOG SIMULATOR (SPICE VARIATION)
	  * FEEDBACK ANALYZER
	  * POLE/ZERO ANALYZER
	  * AC/DC ANALYZER
	  * WAVEFORM EDITOR
	  * FREQUENCY ANALYZER
	* MIXED MODE SIMULATOR

* TESTABILITY ANALYSIS	* WSTA * OTHER SOFTWARE TBD
* SYSTEM ANALYSIS AND SIMULATION (BUBBLE UP)	* SYSTEM BLOCK MODELER (VHDL TOOL) * SYSTEM SIMULATOR

6.3 Primary Evaluation. The primary evaluation objective focuses on the utility and application of CAE tools for specific TPS development processes. PCB layout tools employed during the ID design development and CAD tools for assembly drawing layout will not be covered in order to narrow the focus of the primary evaluation. The primary evaluation focuses on the proof of concept of CAE tool application for TPS development.

During the forthcoming primary evaluation, the feasibility of employing CAE tools to output a VHDL circuit description and then input the VHDL circuit description into a testability analyzer for test strategy development will be explored. The resulting test strategy is essential for good TPS development and for formal design reviews. WSTA is the CAE tool evaluated for test strategy development. Additionally, the evaluation investigates the application and limitations of CAE tools for circuit analysis, fault simulation, testability analyzer results to ID design, TP development and as review data for formal design reviews.

7.0 CAE DESIGN ENVIRONMENT CRITERIA.

7.1 Overview. Eight selection criteria were selected and applied to CAE software packages. The software criteria are outlined in the next paragraphs. The criteria was applied to the total electronic design environment to select an group of CAE tools for the primary evaluation.

7.2 System Design and Analysis. The CAE environment must lend itself to system level (SRA and WRA) design and analysis.

7.3 Circuit Simulation Capability. There are four types of circuit simulation considered. The best CAE packages have the capability of performing all four types of analyses, and they are:

- Analog.
- Digital.
- Mixed Mode (Hybrid)
- Electro-mechanical, thermal, electro-optic.

7.4 VHDL Output. Output an VHDL description or model of the SRA or WRA for entry into the Weapon System Testability Analyzer, WSTA.

7.5 Open Software Environment. Operating environment or CAE framework must allow the integration of other CAE software. Operating environment provides multi-tasking and macro command features to minimize the computational bottleneck of simulator programs.

7.6 Documentation Output. For reverse engineering documentation and documentation enhancement (available documentation or documentation generated from aperture cards may not be of the best quality) purposes, this selection factor is important. Accurate and easily generated documentation is a must for TPS development.
Documentation must be CALS compliant.

7.7 Library Size and Type. Large library sizes to minimize component modelling for simulation. Analog, digital, and hybrid devices library types are considered. Facilities or an editor to create or modify the component model.

7.8 Monte Carlo Simulation Testing . Monte Carlo simulation testing derives the test tolerance for an UUT to account for slight electrical output differences between all UUT of the same type.

7.9 WRA and System Simulation. Bubble-Up capability is important so that WRA electrical and functional behaviors are derived or inferred through simulation of each SRA within the WRA.

8.0 SOFTWARE SELECTION AND PRELIMINARY REVIEW PROCESS.

8.1 Overview. The software selection and preliminary review of CAE software begins with the evaluation fundamentals shown in Figure 4. and discussed in the preliminary evaluation approach paragraph 6.2. The types of CAE software tools organizes the research for these tools. Also, selection of CAE tools is guided by two circuit design approaches. The two ways of applying CAE tools for design are a point design solution and a total electronic design automation design solution. The point design solution employs each type of CAE tool, for example a simulation tool to each design oriented task, point to point. The Electronic Design Automation (EDA) solution provides the same set of tools, but they share information between CAE tools and each use the same user graphical interface. Sharing of information between tools takes place statically through data files or dynamically (real time) through direct data transfer between programs. The same graphical user interface (GUI) presents to the user a common look and feel which minimizes training costs and increases design efficiency. On the 386/486 workstation, Windows is the GUI and on the Sun workstation Looking Glass and Open Windows are GUI's. The primary evaluation studies the value of dynamical sharing of data between CAE tools and the various issues levels of integration between CAE tools and the subsequent impact on CAE tool ease of use. When factoring economic costs into the selection decision of CAE tools, a less than ideal level of integration may be acceptable, thus CAE tools on the 386/486 workstation are considered.

Also, with slight performance tradeoffs, 386/486 workstation are an alternative. Because of the aforementioned consideration, CAE software tools for both the SUN and 386/486 workstation are candidates under consideration for the primary evaluation.

Most CAE tools under consideration implied usage intent is for new circuit design and are required for ID design. However, application of CAE tools toward TPS development is for an already existing design, the UUT. Employment of CAE tools for TPS development is for documentation (schematic capture), circuit analysis (simulation) and fault analysis (fault simulation). Because of the subtle CAE tools intent difference between design and test strategy generation, CAE tools lack certain small capabilities and features. The primary evaluation will look at the application and limitations of CAE tools to TPS development specific problems. The SUN workstation candidate selection process identifies the

companies of Intergraph, Cadence, Viewlogic, and Teradyne. Because Teradyne's Multi-Sim full design environment is not immediately available, Multi-Sim is not under consideration for primary evaluation. Intergraph, Cadence, and Viewlogic product literature were solicited and analyzed.

8.2 Selection criteria was applied to analyze and select specific CAE tools candidates from the CAE marketplace. CAE tool selection criteria for both the SUN and 386/486 workstation are listed below.

Selection Criteria for Individual CAE Tools

Schematic Capture

Large Libraries
Have a compatible output with the Analog & Digital Simulators.

Analog Simulator -

Integrated	Includes a built-in Schematic editor and directly shares netlist data and simulation results. Alternatively, integrated means, the simulator accepts a netlist file from a schematic capture program.
Speed	
Mixed Mode	
Monte Carlo	Determines UUT electrical output tolerances
Fault Simulation	**MOST IMPORTANT CAPABILITY**
Large Libraries	
Behavioral -	System modelling and for black box submodels.
Realtime results	

Digital Simulator

Fault Simulation Capability
Integratable with Schematic Capture
Meets ATPG Requirements

Mixed-Mode Simulation

Must employ the selected analog and digital simulator using the above mentioned selection criteria.

System Simulator

Allow for simulation of WRA's.
Integrates with schematic capture

Preferably all software should use the same GUI.

8.3 On-Site Demonstrations. The next step in the review selection process was to attend on-site demonstrations to get a first-hand view of the software for analysis and review. A pre-screening of the software packages offered by the three CAE companies was performed by ARL. All were thought to be impressive enough to have the NADEP NORVA engineering staff attend another demonstration. The demonstrations that were completed, and their results, based on the eight selection criteria, are detailed in the following paragraphs. The evaluation report for each company is detailed in the CAD/CAE comparison Appendix A.

8.4 The results of the selection and review process employing the CAE tool selection criteria are demonstrated with Preliminary Evaluation Results for Sun Workstation Figure 5. The main determinate forcing the selection of Viewlogic versus Cadence were a hardware constraint (WSTA runs on a SUN-3) and economic considerations (Intergraph hardware costs $60K). Selection of Cadence over Viewlogic was predicated on:

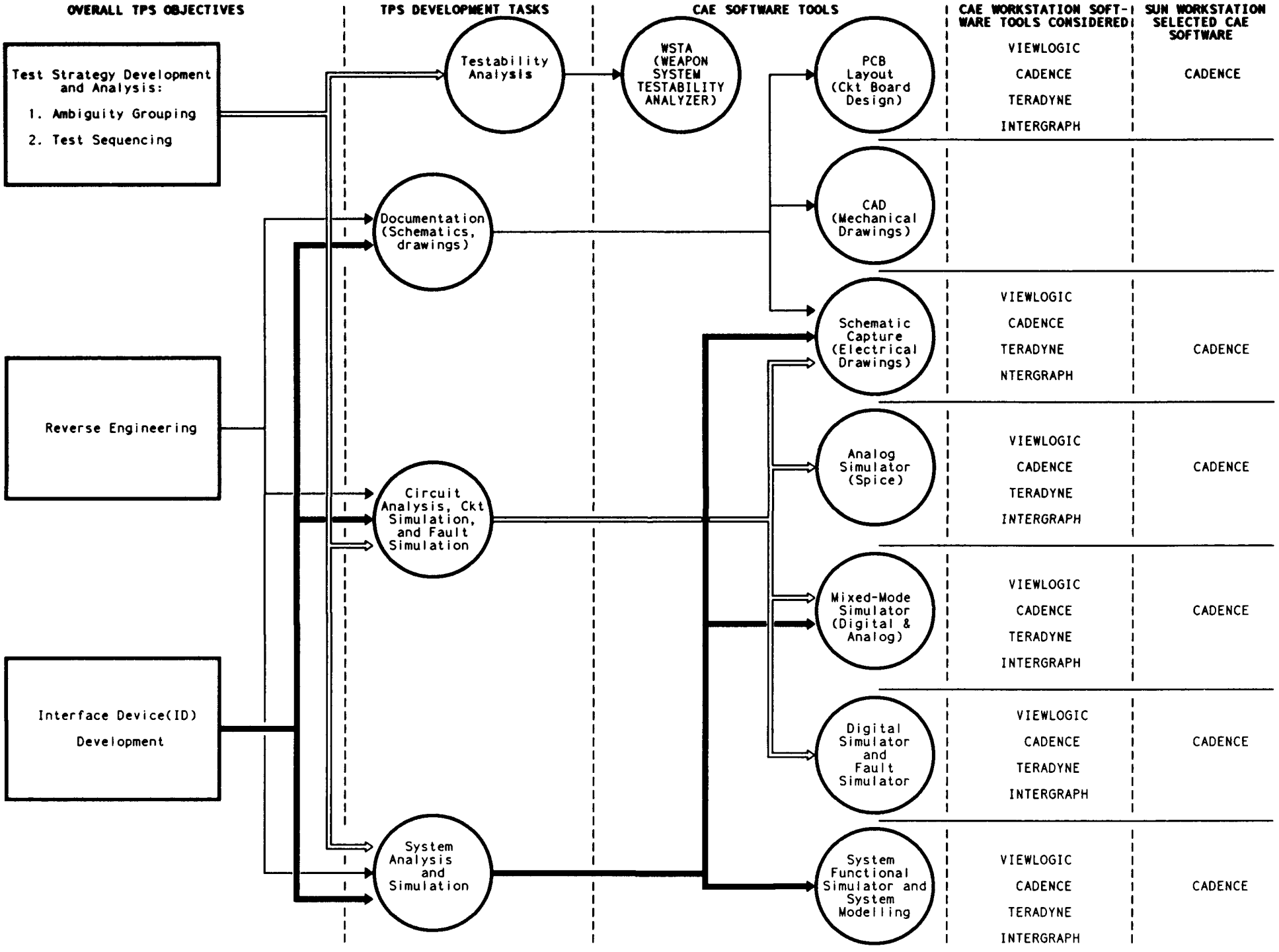
1. Cadence performs mixed mode simulation with Saber for the analog simulator. Saber is the selected analog simulator that displays a fault simulation capability.

2. Cadence performs digital fault simulation on a SUN-3.

3. Cadence SKILL programming language provides for integration of other CAE tools (WSTA) into the CAE environment.

4. Cadence multitasks the individual CAE programs. This may be valuable to run simulations in the background.

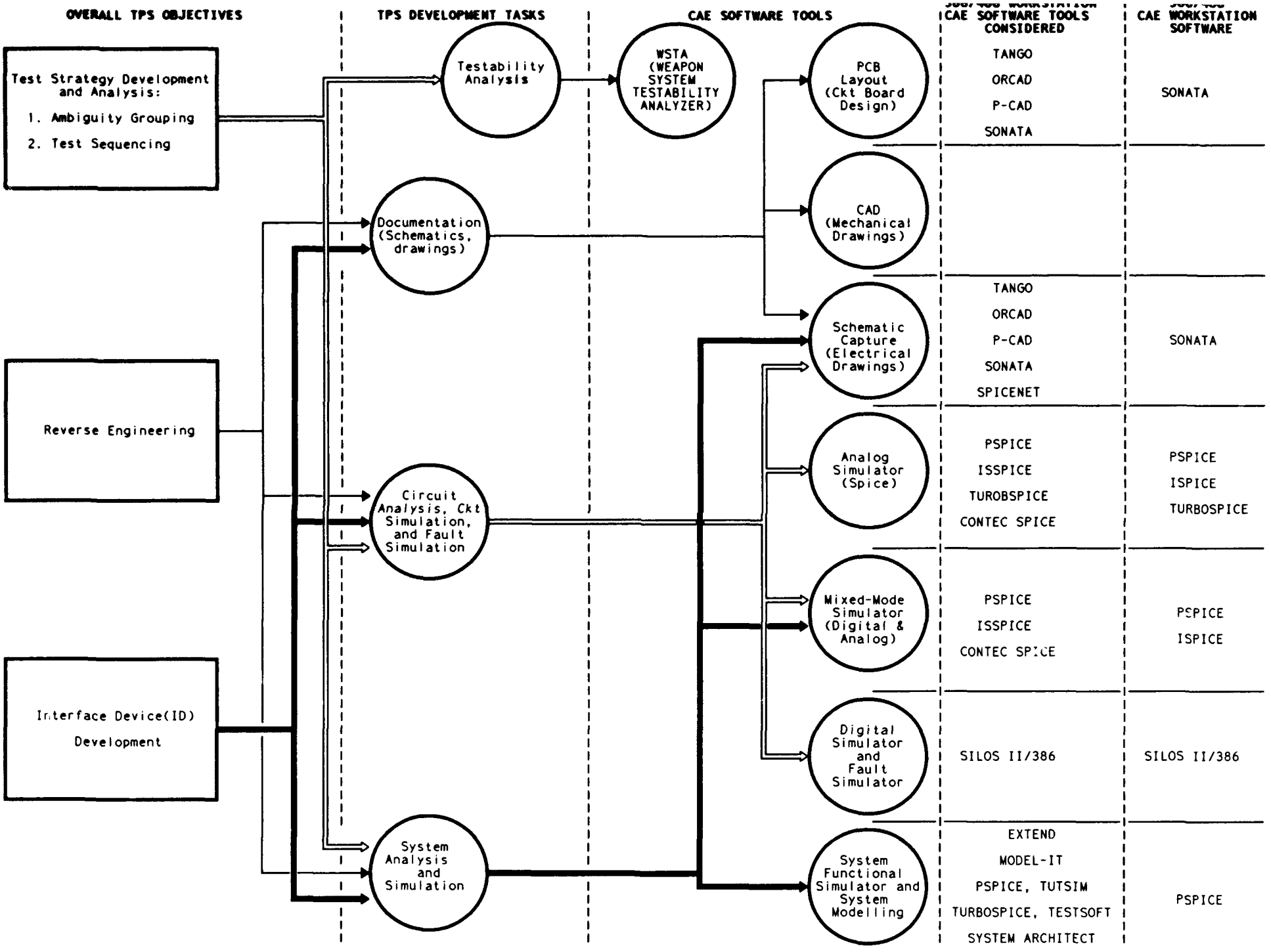
8.5 Testability Analyzer. The WSTA tool will be used as part of the prove-out process to determine if WSTA can play a viable role in the TPS development effort.



Preliminary Evaluation Results for SUN Workstation Figure 5.

8.6 386/486 Workstation CAE Tools

Selection of the 386/486 workstation CAE tools candidates requires the best matching of the vendor CAE tools capabilities with the CAE tool requirements. Information on 386/486 CAE tool capabilities were gleaned from articles and advertisements contained in the magazine Personal Engineering and subsequent solicited company literature. Selection criteria applied to the list of 386/486 workstation vendor CAE tools resulted in a final list of 386/486 workstation CAE tools for the main evaluation. The results of the selection and review process employing the CAE tool selection criteria are demonstrated with Figure 6. Figure 6 shows the 386/486 CAE software tool candidates and selection results. Selection of SONATA was predicated on the multitasking and user friendly advantages of the Windows operating environment, schematic capture additional features, and the dynamic integration of design data results between CAE tools. PSPICE was selected because PSPICE is an establish product and the market standard for SPICE based simulators. Also, PSPICE interfaces with SONATA which is a design environment requirement. PSPICE was selected to perform simple system simulation duties. The search is still on for a good system simulator. ISPICE was selected due to ISPICE tight integration between schematic capture and circuit simulation tools. SILOS was selected because SILOS has a tight interface with SONATA and is the most powerful digital simulator for the 386 workstation.



Preliminary Evaluation Results for 386/486 Workstation Figure 6.

9.0 HARDWARE SELECTION, PRELIMINARY REVIEW PROCESS AND CONCLUSIONS

CAE Hardware and Software Selection Results, Figure 7. illustrates the decision factors concerning hardware platform selection for evaluation. The conclusions drawn from the decision factors are to evaluate CAE software on the SUN-3 and the 386/486 workstations. Hardware selection begins with the investigation and selection CAE software. Selection of CAE software determines the hardware platform the CAE software runs on. From the analysis of the CAE software restrictions, the matching of CAE software capability with desired CAE software capability, and comparison of various CAE software, decision factors arise which govern the selection of a hardware platform. The main decision factor governing the selection of the SUN-3 workstation is the restriction of WSTA only running on the SUN-3 workstation. The main decision factor concerning selection of the 386/486 workstation is economic factors. Parallel evaluation of CAE software on the SUN-3 and 386/486 workstation will access and identify tradeoffs in performance and capability. VAX was not considered due to availability for evaluation and an implied selection restraints of distributed processing (i.e. an workstation environment) and computation power for the money spent.

10.0 RECOMMENDATIONS

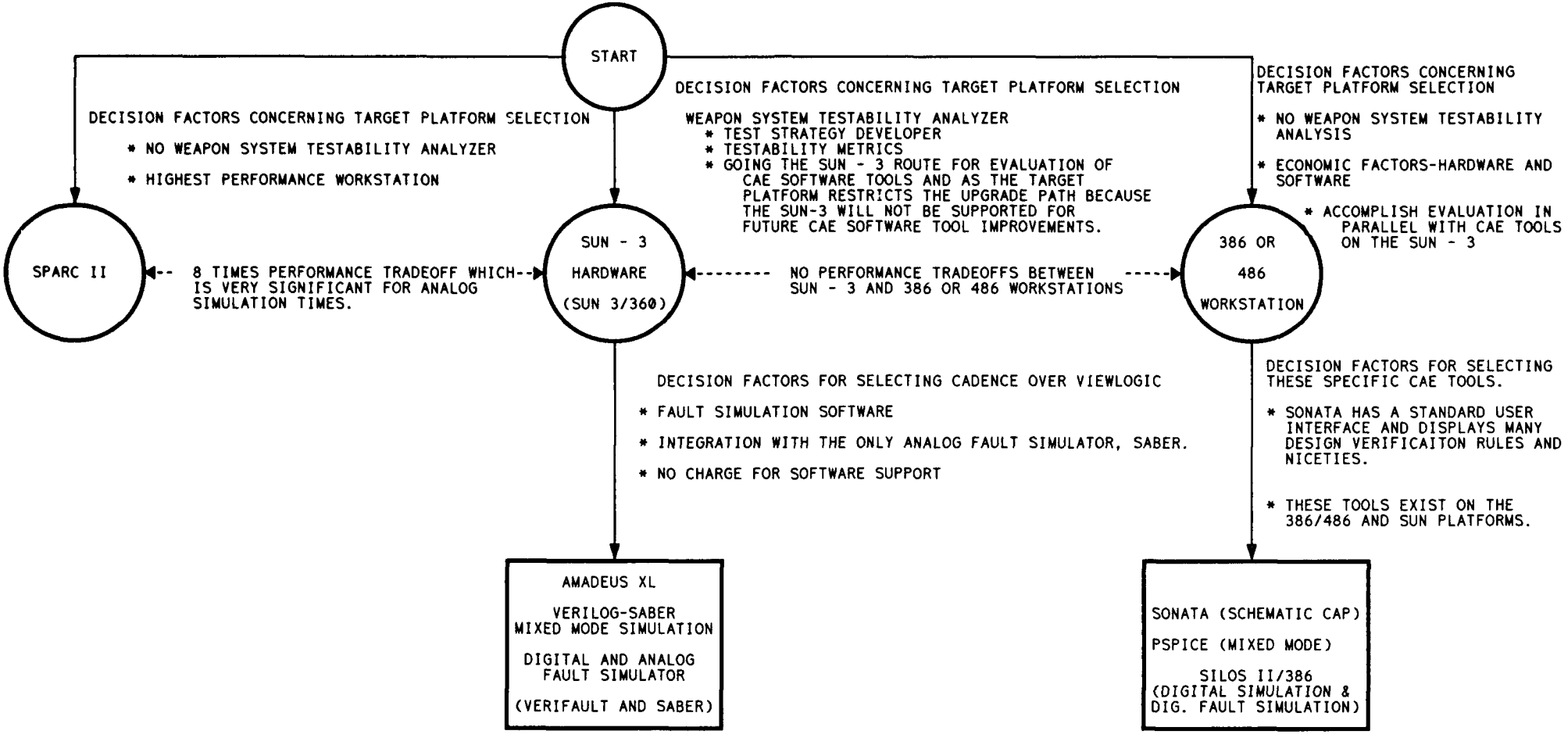
Recommendations are: to obtain necessary equipment and tools to complete the concept verification; to develop and evaluate CAE tool application strategies with regard to TPS development as follows:

- Perform fault simulation, circuit simulation, circuit analysis, and test strategy generation on a SRA and WRA. Investigate circuit modelling techniques. Record simulation waveform and timing results. Time the simulation speed of a full circuit simulation. Calculate SRA and WRA output testing tolerances. Generate TPS documentation. Access various methodologies for fault simulation.

- Evaluate Cadence and WSTA on a SUN-3 workstation based on the above mentioned evaluation tasks.

- Evaluate SONATA, PSPICE, ISPICE, and SILOS on a 386/486 workstation based on the above mentioned evaluation tasks.

- Evaluate SABER on the SUN-3 workstation to access the analog fault simulation capabilities for fault strategy and fault analysis purposes. Record output test vectors for faulted components. Study SABERs behavioral capabilities to do system simulation.



CAE HARDWARE AND SOFTWARE SELECTION RESULTS FIGURE 7.

CAD/CAE COMPARISONS

CADENCE

VIEWLOGIC

INTERGRAPH

COMPANY NAME: VIEWLOGIC

REPRESENTATIVE: MORRIS C. HARMOR

ADDRESS: 6701 DEMOCRACY BLVD., STE. 300, BETHESDA, MD 20817

PHONE NUMBER: (508)480-0881 FAX: (508)480-0882

LIBRARY SIZE/TYPE	OPEN ARCH	BUBBLE UP CAP.	OUTPUT VHDL	OUTPUT W.L.,P.L., ASSY DWG.,SCHEMA.	TYPE OF ANALYSIS	HOST
5400 SERIES	YES	YES	YES	WIRE LISTS	ANALOG	IBM PS/2 386 & 486
7400 SERIES				PARTS LIST	DIGITAL	BASED WORK-
CMOS/CD4000				SCHEMATIC	MIXED MODE	STATIONS
ECL 10K				NO ASSY. DWGs	SABER	SUN
AMD				NO BOARD ROUTING	MONTE CARLO	SPARC
ALTERA EPLD						DEC
EXTENDED ANALOG						

REMARKS: LASAR VI CAN BE USED WITH IT. WILLING TO COOPERATE IN REVERSE ENGINEERING PROBLEM. GRAPHICS LESS IMPRESSIVE THAN OTHER TWO DEMOS.

COMPANY NAME: INTERGRAPH

REPRESENTATIVE: JOSEPH A. CAMPBELL

ADDRESS: 1002 WEST 9th AVENUE, SUITE 310, KING OF PRUSSIA, PA 19406

PHONE NUMBER: (215)265-3562 FAX: (215)265-1404

LIBRARY SIZE/TYPE	OPEN ARCH	BUBBLE UP CAP.	OUTPUT VHDL	OUTPUT W.L.,P.L., ASSY DWG.,SCHEMA.	TYPE OF ANALYSIS	HOST
MILSPEC	NO	YES	YES	WIRE LISTS	ANALOG	INTER-GRAPH
STARTER ANALOG				PARTS LISTS	DIGITAL	WORK-STATIONS
AMD				NO ASSY DWGs	MIXED MODE	
INTEL				SCHEMATIC	SABER IN THE FUTURE	SCHEM CAP ON A PC
DIODE/BJT/AMPLIFIER/JFET/MOSFET				BOARD ROUTING	MONTE CARLO	
MOTOROLA						

REMARKS: VERY IMPRESSIVE DEMO. ALL INFO ABOUT A COMPONENT AT YOUR FINGERTIPS. PREFERRED GRAPHICS. VERY GOOD LOGIC SIMULATION (MIXED MODE). ONLY COMPANY TO SHOW UP WITH A POSSIBLE SOLUTION TO THE REVERSE ENGINEERING PROBLEM. INSTANTANEOUS WIRE PLACEMENT CHECKER.

MAJOR DRAWBACK: HAVE TO USE INTERGRAPH WORKSTATION.

COMPANY NAME: CADENCE

REPRESENTATIVE: WILLIAM F. MANSFIELD, JR.

ADDRESS: 10480 LITTLE PATUXENT PARKWAY, SUITE 400, COLUMBIA, MD 21044

PHONE NUMBER: (301)740-8727 FAX: (301)740-8191

LIBRARY SIZE/TYPE	OPEN ARCH	BUBBLE UP CAP.	OUTPUT VHDL	OUTPUT W.L.,P.L., ASSY DWG.,SCHEMA.	TYPE OF ANALYSIS	HOST
TI (TTL)	YES	YES	YES	WIRE LISTS	ANALOG	SUN
MOTOROLA (HCMOS)				PARTS LISTS	DIGITAL	DEC
NATIONAL/FAIRCHILD (FAST)				SCHEMATICS	MIXED MODE	HP/APOLLO
RCA/GE (CMOS)				BOARD ROUTING	SABER	INTER-GRAPH
HCMOS (HITACHI, SGS-THOMSON, SIGNETICS, TI)				NO ASSY DWGs	MONTE CARLO	NEC
FAST (MOTOROLA, SIGNETICS, TI)					*DID NOT SEE ANY SIM*	SONY
ECL (HITACHI, MOTOROLA, NATIONAL/FAIRCHILD, SIGNETICS)						

REMARKS: BEST VHDL CAPABILITIES OF THE THREE DEMOS. COULD ACCOMPLISH A SYSTEM DESCRIPTION IN VHDL FOR SIMULATION. DID NOT SEE ANY SIMULATION EVEN THOUGH IT WAS REQUESTED PRIOR TO THEIR ARRIVAL. BEST FEATURE WAS THE PACKAGE'S OPEN ARCHITECTURE. MENTIONED CAN USE ACTUAL GEAR FOR SIMULATION (BUILD INTERFACES). SEEMED WILLING TO HELP IN REVERSE ENGINEERING PROBLEM. HITS/LASAR COMPATIBLE. REAL EDIF INPUT/OUTPUT. REAL TIME CONNECTIVITY CHECKS. SYNOPSIS SCHEMATIC GENERATOR. SIMULATION CAN BE FROM SCHEMATIC OR HDL. CAN VIEW CIRCUIT ANALYSIS OUTPUTS AS THEY OCCUR. PCB LAYOUT AND SCEMATIC CAPTURE NOT YET INTEGRATED.

RECOMMEND SEEING ANOTHER DEMO FOR SIMULATION/ANALYSIS PURPOSES.