AFIT/GE/ENG/91D-12

APPLICATION OF SILICON MICROMACHINING TO THERMAL DISSIPATION ISSUES IN WAFER SCALE INTEGRATED CIRCUITS

THESIS

Edward Cosnyka, Captain, USAF
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13. ABSTRACT (Maximum 200 words)

This research effort investigated the application of the silicon micromachining technique to thermal management as applied to integrated circuits. Three silicon micromachined structures and a reference structure were compared as heat-dissipating surfaces using 3-inch diameter, single-crystal silicon wafers: 1) randomly spaced and sized pyramids in (100)-oriented silicon, 2) deep vertical-wall grooves in (110)-oriented silicon, and 3) micro-fluid channels in (100)-oriented silicon. The heat-dissipating silicon wafers were epoxied to silicon wafers hosting heat-producing devices to realize a silicon wafer thermal module. The silicon micromachined structures enhanced heat dissipation from the silicon wafer thermal modules, and they correspondingly lowered the steady-state operating temperature of the devices. In ranked order of performance, the micro-fluid channels, deep vertical-wall grooves, and the randomly spaced and sized pyramids, respectively, dissipated heat from the silicon wafer thermal modules more efficiently than the reference silicon wafer.

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THESIS

Presented to the Faculty of the School of Engineering

of the Air Force Institute of Technology

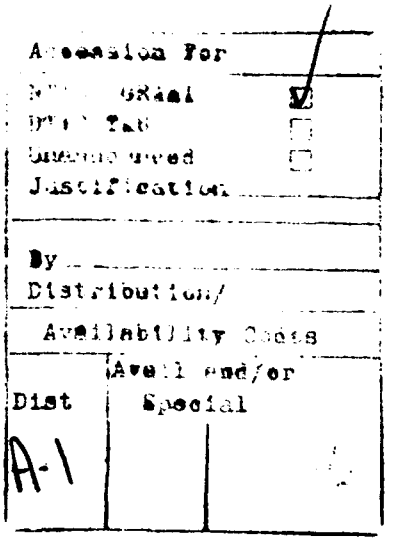
Air University

In Partial Fulfillment of the

Requirements for the Degree of

Master of Science in Electrical Engineering

Edward Cosnyka, Captain, USAF



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I wish to acknowledge and thank my thesis advisor, Lieutenant Colonel Edward S. Kolesar, for his guidance, editing, and the solutions to many of the problems I encountered during my research. I appreciate the support from my committee members, especially Capt Thomas Jenkins.

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I also thank Capt James C. Lyke, Jr. PL/STEE, KAFB, NM 87117 for sponsoring this research.

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Abstract

The purpose of this research effort was to investigate the feasibility of applying the silicon micromachining technique to thermal management as applied to integrated circuits and wafer scale integration techniques.

Three silicon micromachined structures and an untextured reference wafer were compared as heat-dissipating surfaces. These four surfaces were realized using 3-inch diameter, single-crystal silicon wafers. The following structures were micromachined in silicon wafers using wet chemical, anisotropic etching and photolithographic techniques: (1) randomly spaced and sized pyramids in (100)-oriented silicon, (2) deep vertical-wall grooves in (110)-oriented silicon, and (3) micro-fluid channels in (100)-oriented silicon.

The heat-dissipating silicon wafers were epoxied to silicon wafers hosting heat-producing devices to realize a silicon wafer thermal module, simulating the wafer scale integration packaging technique. Two types of heat-producing devices were compared: (1) n-diffused integrated circuit die resistors, and (2) thin-film aluminum resistors. Two configurations of the integrated circuit die were also compared: (1) a single, centered, integrated circuit die and (2) four, centered, integrated circuit die.

Electrical power was applied to the devices to promote heat-dissipation. As the power was applied and allowed to increase, the temperature on the surface of the thermal modules was recorded with an array of thermocouples. Also, infrared images of the module were recorded with an infrared microscope.

The silicon micromachined structures enhanced heat dissipation from the silicon wafer thermal modules, and they correspondingly lowered the steady-state operating temperature of the devices. In ranked order of performance, the micro-fluid channels, deep vertical-wall grooves, and the randomly spaced and sized pyramids, respectively, dissipated heat from the silicon wafer thermal modules more efficiently than the reference silicon wafer. Thus, the silicon micromachining technique may be an effective engineering design tool for thermal management in integrated circuits.

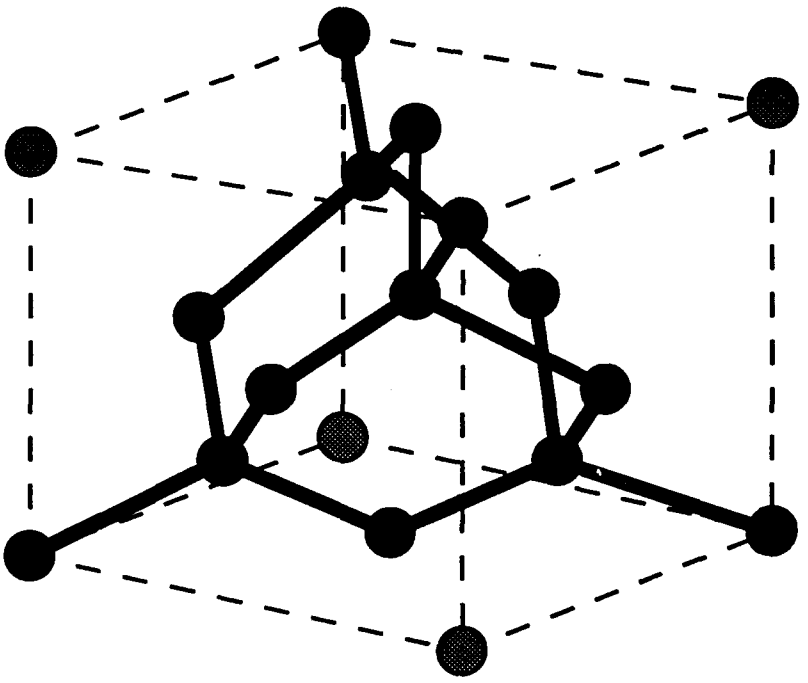
APPLICATION OF SILICON MICROMACHINING TO THERMAL DISSIPATION ISSUES IN WAFER SCALE INTEGRATED CIRCUITS

I. Introduction

Crystalline silicon is the most commonly used material in integrated circuit (IC) fabrication, and it is likely to remain the dominant choice for several decades. Silicon is second most abundant solid material in the earth, and it is readily refined and purified for exploitation in the semiconductor industry to fabricate integrated circuits. More importantly, silicon is easier and safer to work with compared to the other elemental or compound semiconductors used to fabricate a variety of IC devices (e.g., microprocessors, computer memories, etc.) [1].

Recently, research has capitalized on the crystallographic orientation and atomic packing density of silicon and its amenability to anisotropic etching. Appendix A discusses the theory of crystallography and wet chemical anisotropic etching with respect to single-crystal silicon.

Silicon's single-crystal atomic density varies dynamically with respect to its Miller planes (Figure I-1) [2:19-20].



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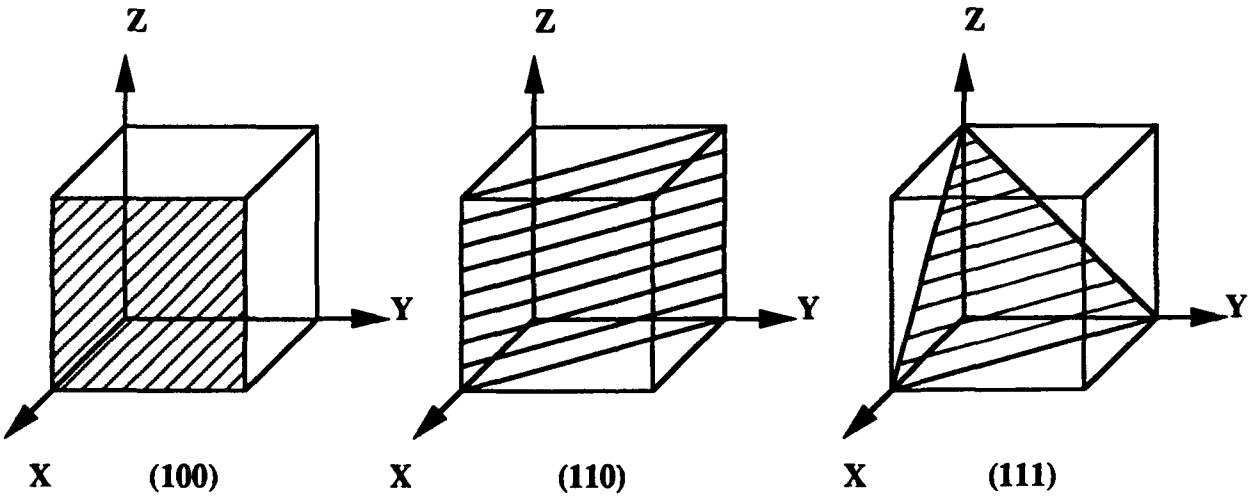


(b)

Figure I-1. Single-Crystal Silicon: (a) Tetrahedral Bonds of Single-Crystal Silicon in the Diamond Structure, (b) Miller Planes [2:19-20].

Certain chemicals which react with silicon are known to remove silicon at different rates in different crystalline directions due to the different atomic planar densities. This behavior results in anisotropic etching or the preference of the chemical reaction to remove silicon faster in the less dense planes. The process that puts anisotropic etching to good use is referred to as surface texturing or micromachining [3]. Micromachining can be used to produce a variety of different surface structures depending upon the chemical etchant selected and the crystallographic orientation of the material (Figure I-2). The resulting (etched) surfaces also have different characteristics (e.g., light reflectivity, heat dissipation, etc.). It is anticipated that improved heat dissipation, due to the ability to control the surface geometries on the backside of a silicon wafer, will enhance the efficiency and reliability of the devices mounted on the wafer's frontside. The fundamental theory of the thermal dissipation analysis utilized in this investigation is developed in Appendix B.

This chapter introduces the principle areas of science that are important to this research--wet chemical anisotropic etching and thermal dissipation analysis.

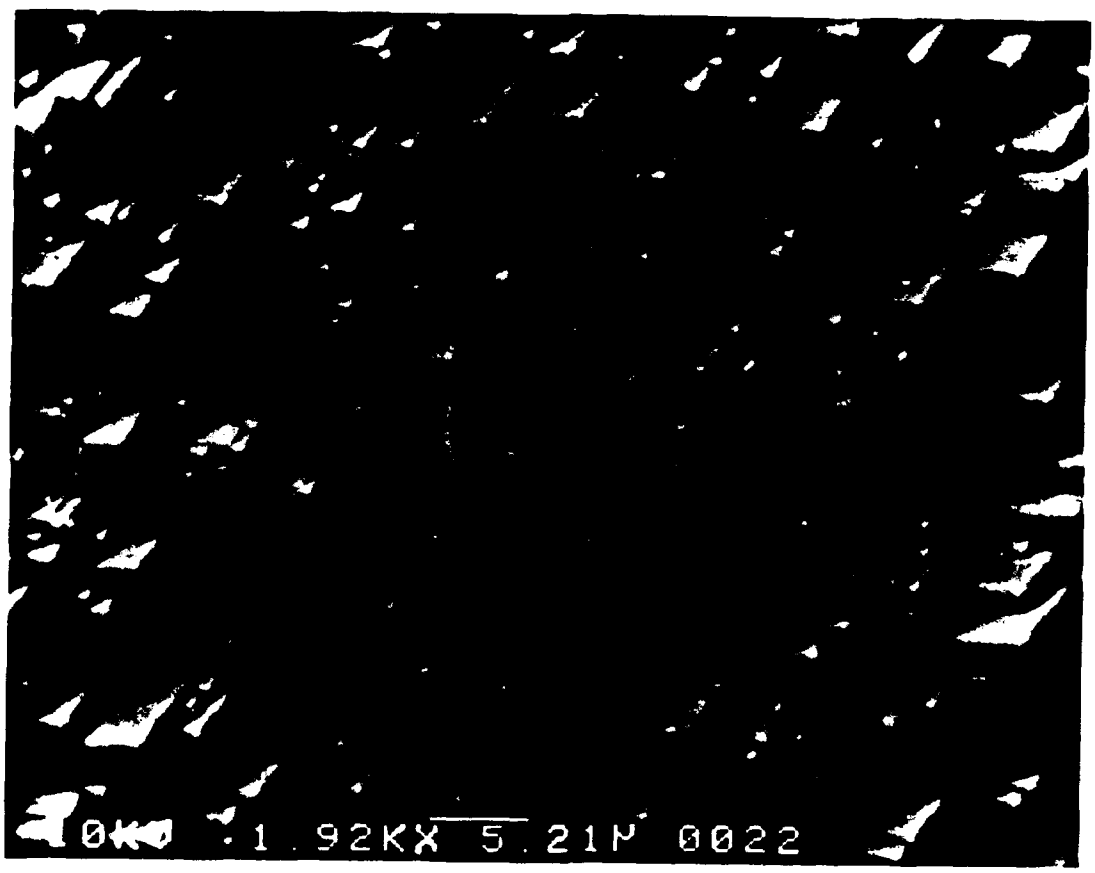


Figure I-2. Micromachined Surfaces. Randomly Spaced and Sized Pyramids (Magnification -1920X) [4].

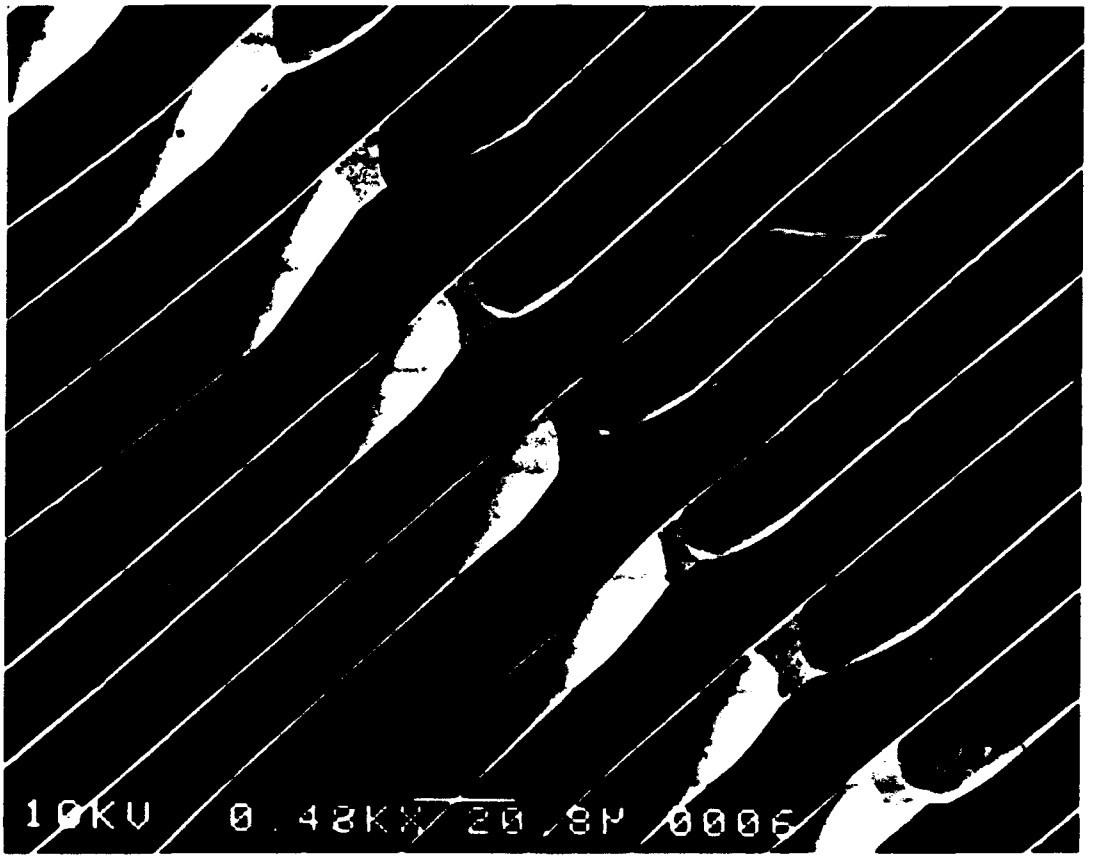


Figure I-2. Micromachined Surfaces (Continued). Deep Vertical-Wall Grooves (Magnification - 480X) [4].

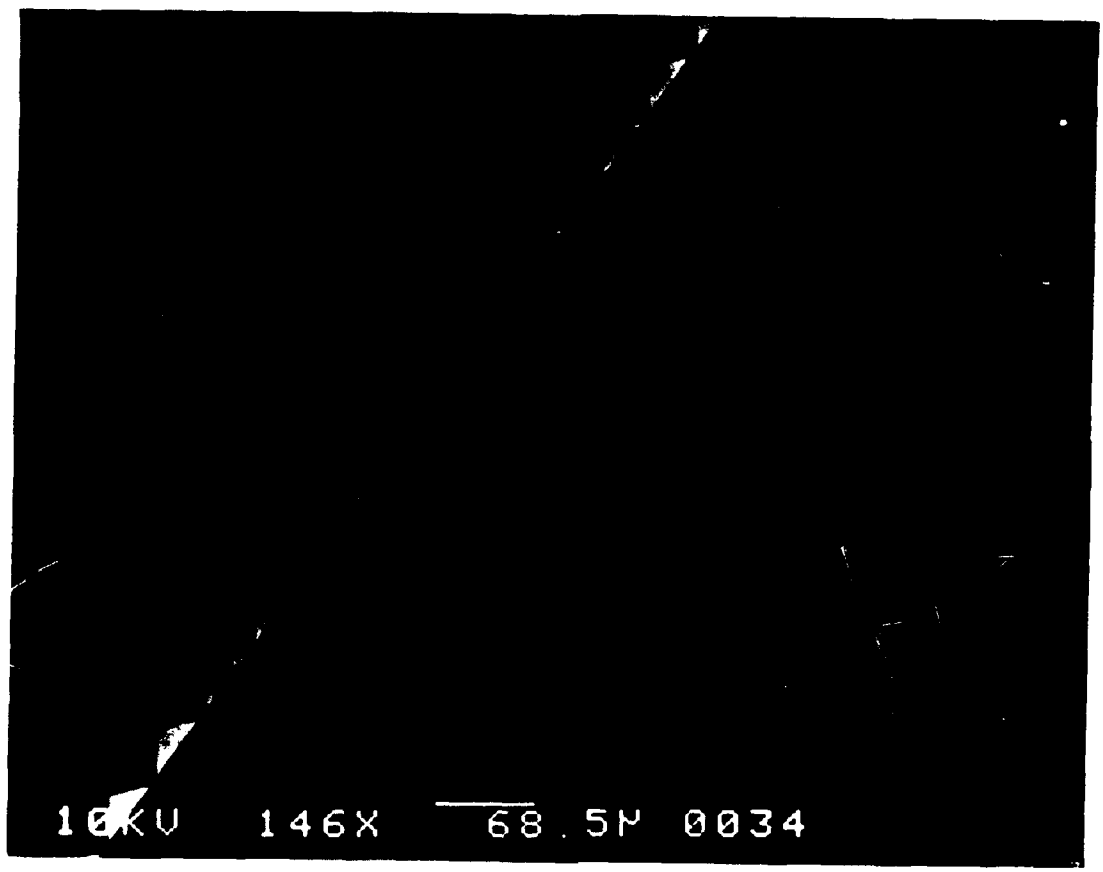


Figure I-2. Micromachined Surfaces (Continued). V-Grooves (Magnification - 146X) [4].

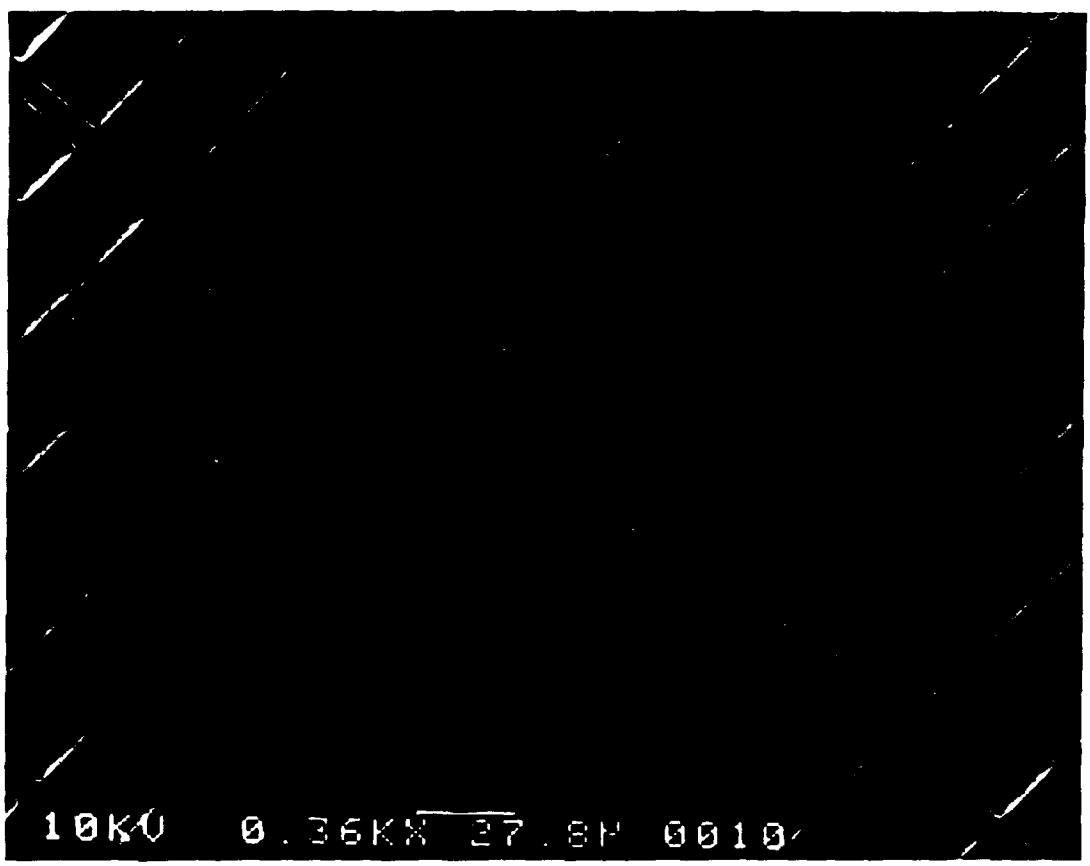


Figure I-2. Micromachined Surfaces (Continued). Inverted Pyramids (Magnification - 360X) [4].

1.1 Background

According to the available technical literature, an immense amount of research concerning thermal management in integrated circuits has been accomplished, especially within the past 5 years, since integrated circuitry is being designed to achieve higher packing densities and operating speeds.

Integrated circuits are usually fabricated on a 400-700 micron thick single-crystal silicon wafer. However, the fabrication process typically only uses the first 20 microns of the wafer's thickness, and the remaining portion of the wafer is primarily used for structural support. The backside of the wafer is increasingly becoming a target for research exploitation, but published research results in this area, with respect to thermal management, are few.

Wet chemical etching was the primary application of science used in this research. The results of this application produced various structures in single-crystal silicon wafers to provide comparative surface textures which were anticipated to alter the heat migration from a sandwich configuration of a heat-dissipating wafer epoxied to a wafer hosting heat-producing resistors.

1.1.1 Wet Chemical Etching. Integrated circuit fabrication incorporates numerous processing steps to remove

unwanted bulk material, dopants, impurities, photoresist from the semiconductor substrate, and deposited thin films. The prevalent process for removing these materials is wet chemical etching. Wet chemical etching employs a chemical reaction to selectively remove unwanted material in a particular processing step. A mask layer of a chemically-hardened material is used to facilitate etching the desired pattern (Figure I-3). Ideally, the chemical etchant selectively and precisely removes the material not protected by the mask, which should be impervious to the etchant [5:520].

Bias, tolerance, etch rate, and anisotropy are terms used to characterize the deviations relative to the ideal etching conditions [5:521]. Bias is a measure of deviation between the mask image and the etched image, or the amount by which the film undercuts the mask (Figure I-4) [5:521]. "Tolerance is a measure of the statistical distribution of bias values" [5:521]. Etch rate is the speed at which the material is removed. It involves the time it takes the etching mechanism to reach the surface, the time for one or more physical or chemical reactions to occur which removes the target material (primarily the silicon substrate in this research), and the impedance of fresh etchant to reach the surface.

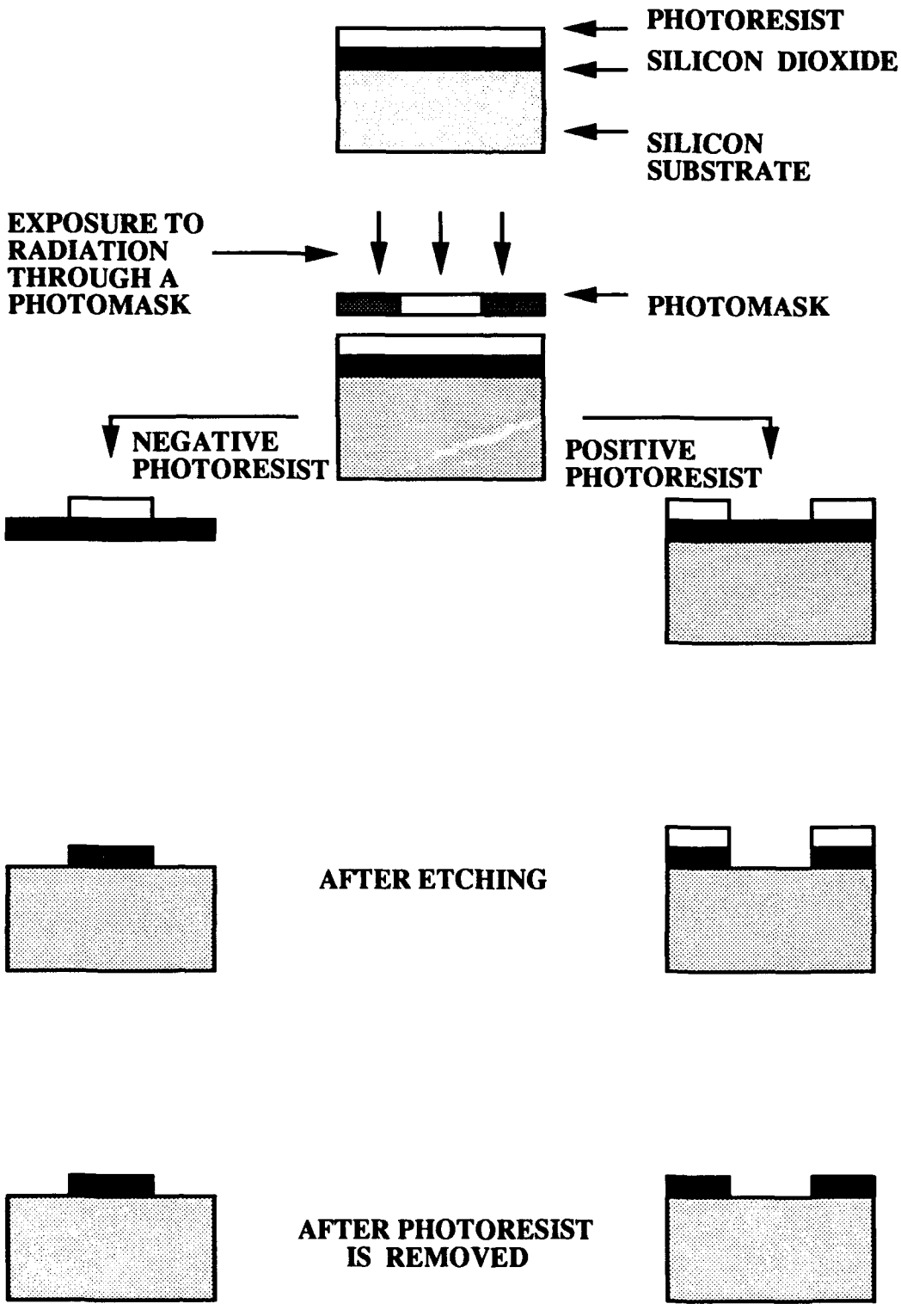


Figure I-3. Using a Photoresist Mask to Etch a Layer of Silicon Dioxide [6:440].

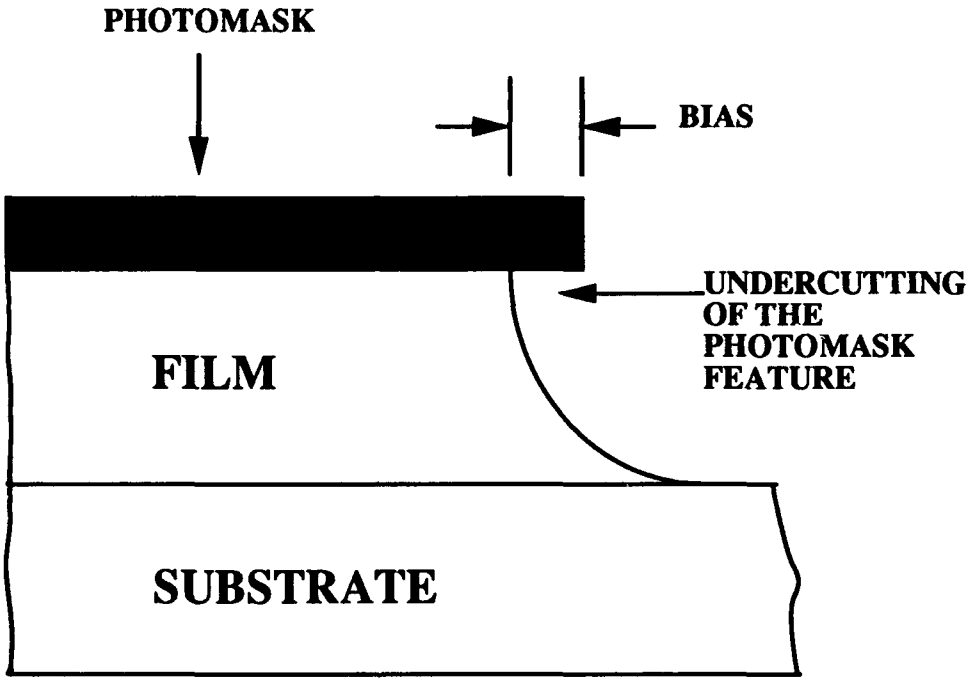
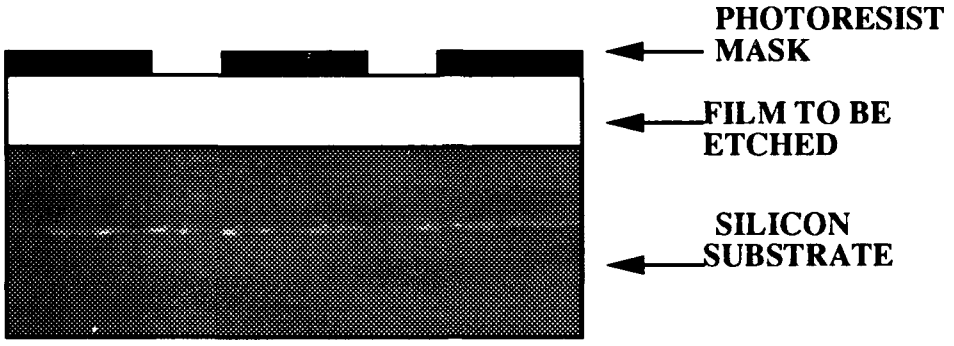


Figure I-4. Etching Bias [5:522].



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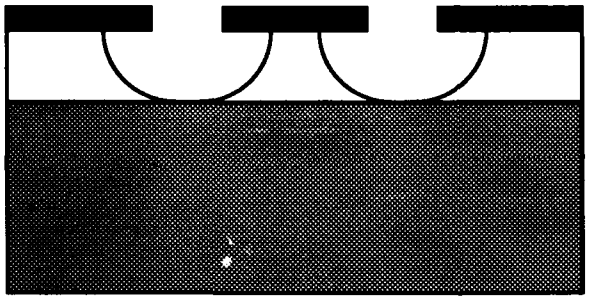

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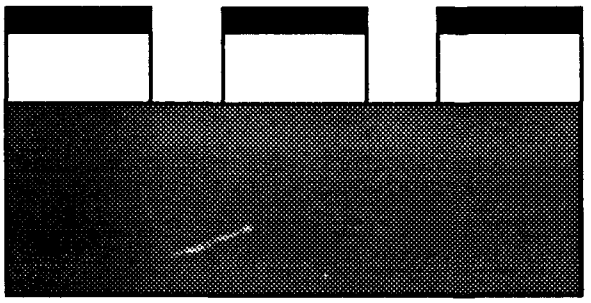


Figure I-5. Isotropic and Anisotropic Etching [5:521].

Anisotropy is the degree to which the etch rate prefers to propagate in certain directions. An isotropic process has the same etch rate in all directions (Figure I-5) [5:522]. Anisotropic etching of a substrate is a function of the crystal lattice arrangement and etching technique.

Atoms in the crystal lattice are more densely packed in some planes (e.g., the (111) plane in silicon); therefore, the crystal is etched slower in these planes, while the material is more readily removed in the other less densely packed planes.

Selectivity is defined as the ratio of the etch rates of different materials [5:523]. Selectivity with respect to the photo resist mask and the substrate are the two most important ratios [5:523]. Selectivity determines the degree of control needed to prevent etching the substrate, and it also determines the propensity for over-etching. Since some degree of lateral etching (over-etching) is likely to occur, the photomask dimensions are usually adjusted to compensate for the amount of photoresist mask undercutting by the film (Figure I-6) [5:523]. Wet etching is generally selective, and selectivity versus isotropy is typically a trade-off when deciding on a specific etch process.

Wet chemical etching refers to those processes using one or more chemical reactions to promote the removal of material from a surface. Wet chemical etching entails three

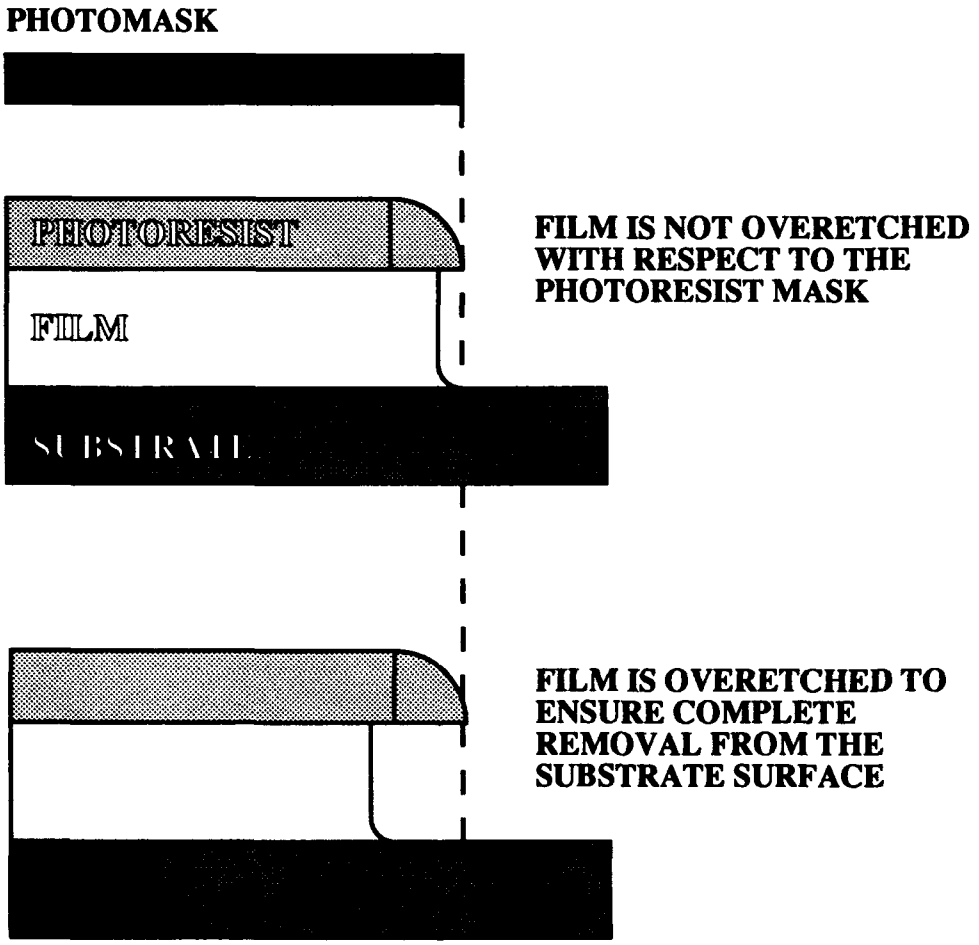


Figure I-6. Overetching [5:522].

fundamental steps: (1) transporting the reactant to the substrate's surface, (2) the chemical reaction(s) which remove the substrate material, and (3) the removal of the by-products [7:451]. Wet chemical etching is widely used because it is reliable and economical. It may also manifest good selectivity with respect to the photoresist mask and substrate [5:529]. The disadvantages of wet chemical etching relative to dry etching are its affinity for isotropy, and the handling and disposing of large amounts of dangerous chemicals [1; 7:202]. Control of the three steps mentioned above is inherently difficult for state-of-the-art feature sizes.

Usually, windows are etched into a mask (a material different from photoresist) layer through which the desired underlying material can then be diffused or implanted, or through which a subsequent etch into the underlying layer can be realized. The etchant should selectively react only with the mask to be etched, and particularly, not with the material which is beneath the mask. Since the chemical reactions also occur laterally, and the substrate must be etched completely through to the next layer, the loss of material in the lateral directions must be accounted for and compensation made in the mask design. Overetching is necessary to ensure complete film removal [7:198].

Reaction rate and reaction time must include the nuances of the geometries of the process and the chemicals. Surface tension on small windows and gas bubbles trapped on surfaces are examples of impedances to the etch process which cause deviations relative to the theoretical rates [7:198]. They will also inflict nonuniform chemical reactions over the surface. Expeditiously removing the by-products (especially tenacious, gas bubbles) of the chemical reactions is necessary to allow fresh etchant to reach the surface and continue a smooth, controlled etching process. Agitation and wetting agents are commonly used to facilitate this process. The goal is immediate etching with the introduction of the etchant, uniform etching, and an abrupt cease to the etching process. Surfactants in etchants accelerate wetting and agitation in the initial phase [7:202]. A quick flush with pure water in the final phase facilitates an abrupt halt to the etching process by removing the lingering etchant from the substrate's surface [7:203].

Several factors may influence the chemical reaction rate: etchant reactions above the substrate's surface, diffusion toward the substrate's surface, chemical reactions with the substrate, and desorption of the by-products from the surface [7:198].

1.1.1.1 Anisotropy. While wet chemical etching is strongly associated with isotropy, certain crystallographic properties and chemical characteristics facilitate varying degrees of anisotropic etching. For example, in single-crystal silicon, the atoms are packed differently in each plane of the diamond lattice structure (silicon atoms are most densely packed in the (111) plane) [6]. Obviously, there will be more chemical reactions which occur on the more densely packed plane, each reaction has a characteristic discrete reaction time which contributes to the total chemical reaction time, and thus, act to slow the material removal process from that plane. Also, more atomic bonds must be broken (and hence formed) in the more densely packed planes.

For example, single-crystal silicon will etch faster in the (100) and (110) planes using a prevalent, relatively safe, and anisotropically-selective potassium hydroxide+water (KOH) system [8]. Specifically, at 85 °C, a 50 % wt mixture of KOH etches single-crystal silicon 200 times faster in the (100) plane, and 86 times faster in the (110) plane, compared to the (111) plane [8]. A variety of surface geometries may be etched or "micromachined" into various semiconductor substrates or films to achieve certain physical or electrical properties by creatively employing isotropic and anisotropic etching. Consistent and

reproducible features on or near the surface of a silicon wafer with dimensions on the order of a few microns can enhance device performance parameters (heat dissipation, radiation reflectivity, radiation absorption, efficiency, reliability, etc.), and these issues have yet to be fully explored and analyzed.

1.1.2 Thermal Dissipation Analysis. Heat in an electronic system accumulates at its source due to the inefficiency of the electronic components to dissipate their thermal energy. Attempts to assist the dissipation of thermal energy from electronic components and systems has always been a critical area of research. Some of the categories of research concerning thermal effects on electronic component reliability include: electromigration, thermally-efficient packaging, failure analysis and thermal cycling, electrostatic discharge, dielectric breakdown, thermal stress analysis, coolant flow, passive air cooling, and forced air cooling [9:1-16; 10:iii-v].

Many failures in integrated circuits can be directly correlated with their operating temperatures [9:19]. High operating temperatures are known to accelerate the failure modes which compromise functional performance outside the conventional operating specifications. Some failures progress gradually; others manifest themselves suddenly, and

are often irreversible. The primary effects of high operating temperatures include: accelerated oxidation, structural changes, chemical reactions, and thermal stress.

Enhanced reliability and efficiency are perpetually sought in every system design, but these characteristics are generally degraded with increasing temperature. As the performance requirements of integrated circuit electronic systems become more restrictive, and circuit density correspondingly increases, thermal dissipation will be a critical factor in the design process.

Standard reliability predictions for military electronic components can be found in the handbook, MIL-HDBK-217 [9:17]. Of the 14 major component categories listed in this handbook, the failure rates for 8 categories are temperature dependent (Figure I-7) [9:17]. Integrated circuits and discrete semiconductors comprise two of these categories.

Equipment cooling and improved thermal management designs usually lower the system's operating temperature. Lowering the operating temperature can improve the reliability of an electronic system (Figure I-8). Higher reliability directly correlates with lower life-cycle costs, higher weapon system sortie rates, and enhanced weapon system survivability [9:20].

1. MICROELECTRONICS *
2. DISCRETE SEMICONDUCTORS *
3. TUBES
4. LASERS
5. RESISTORS *
6. CAPACITORS *
7. INDUCTIVE DEVICES *
8. ROTARY DEVICES *
9. RELAYS *
10. SWITCHES
11. CONNECTORS *
12. WIRE AND PRINTED WIRE BOARDS
13. CONNECTIONS
14. MISCELLANEOUS

* TEMPERATURE DEPENDENCE IN FAILURE-RATE FORMULA

Figure I-7. Major Part Categories in MIL-HDBK-217 [7:17].

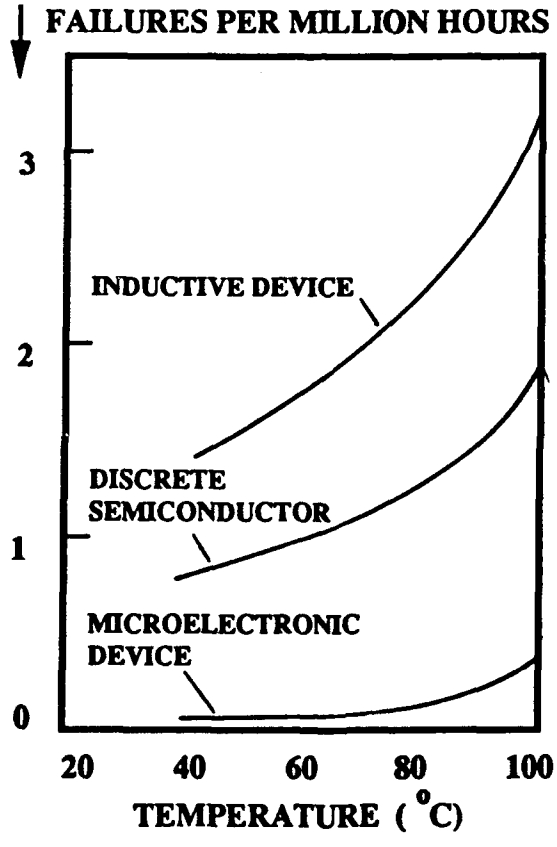


Figure I-8. Failure Rates Versus Temperature [7:17].

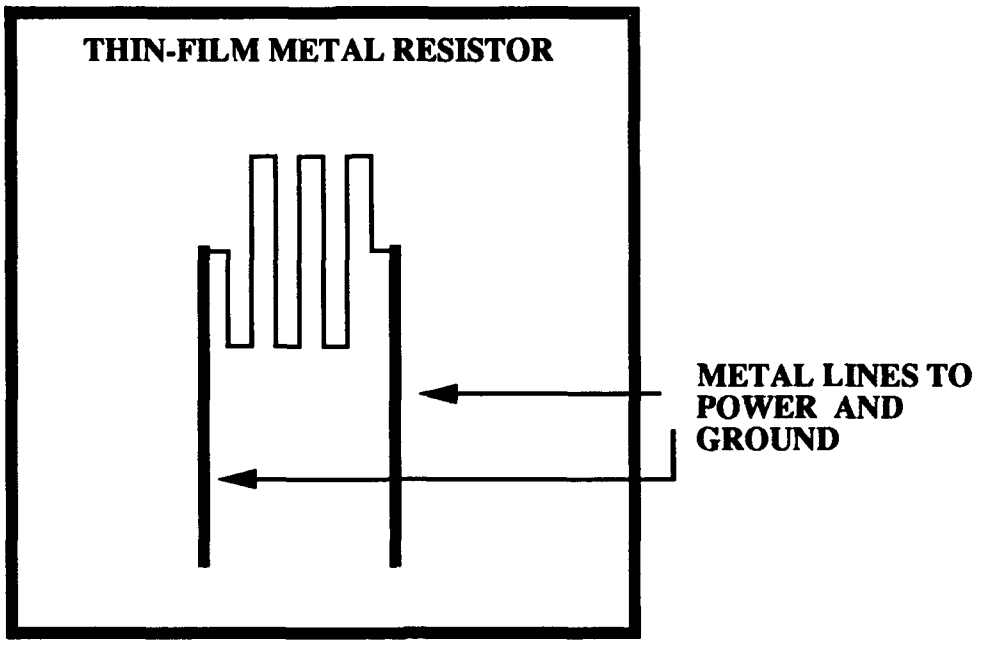
1.2 Problem Statement

As the demands on electronic systems drive electronic component densities in integrated circuits higher and operating speeds faster, the consequential increase in heat accelerates system failures and underscores the importance of thermal management in current and future engineering designs.

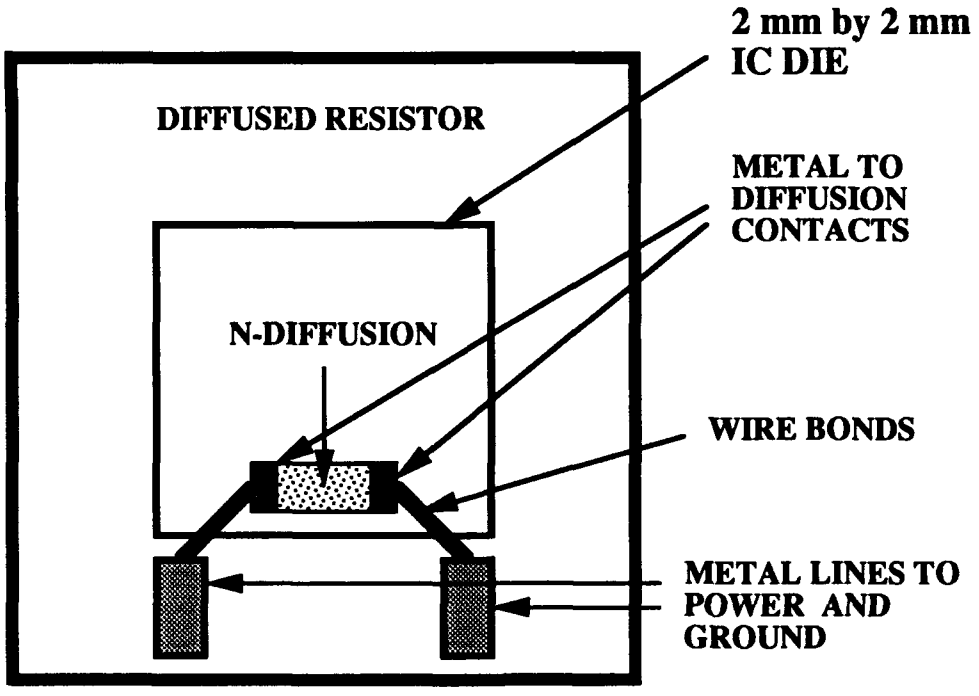
1.3 Scope

Thermal dissipation from two types of heat producing devices was investigated. One type of device was a thin layer of aluminum sputtered onto a single-crystal silicon wafer to realize a heat dissipating resistor (Figure I-9). The other device was an IC die fabricated by the Metal-Oxide-Semi-conductor Implementation System (MOSIS) which was epoxied to a single-crystal silicon wafer (Figure I-9). The latter was also a resistor which was realized with an n-diffusion process. Both of the devices were designed to simulate typical IC die used in wafer scale integration; they could each dissipate approximately 2 watts as the result of an externally applied voltage [11].

Two arrangements of the IC die provided complementary experimental data points from which to derive the conclusions of this investigation. The first arrangement consisted of a single IC die device located at the center on



(a)



(b)

Figure I-9. Two Types of Heat Producing Resistors: (a) Thin-Film Metal Resistor and, (b) Diffused Resistor.

the frontside of the host wafer (Figure I-10). The second arrangement consisted of a configuration of four devices epoxied to and centered on the frontside of the host wafer (Figure I-10).

The wafer hosting each IC die arrangement was epoxied to the backside of four different heat dissipating wafers to create a sandwich configuration (Figure I-11). Three of the four heat dissipating wafers were micromachined on their frontsides; the fourth wafer was an unetched reference (control) wafer.

Three different structures were micromachined using various wet chemical etching methodologies: (1) randomly sized and spaced pyramidal structures, (2) deep vertical-wall grooves, and (3) micro-fluid channels. The pyramidal structures, deep vertical-wall grooves, and the micro-fluid channels were anisotropically etched.

Two experiments were performed on each wafer-sandwich configuration to facilitate data collection when a potential bias was applied to the devices: (1) temperatures were recorded with an array of thermocouples which could be contacted with the wafer sandwiches, and (2) infrared (IR) images of the wafer sandwiches were recorded.

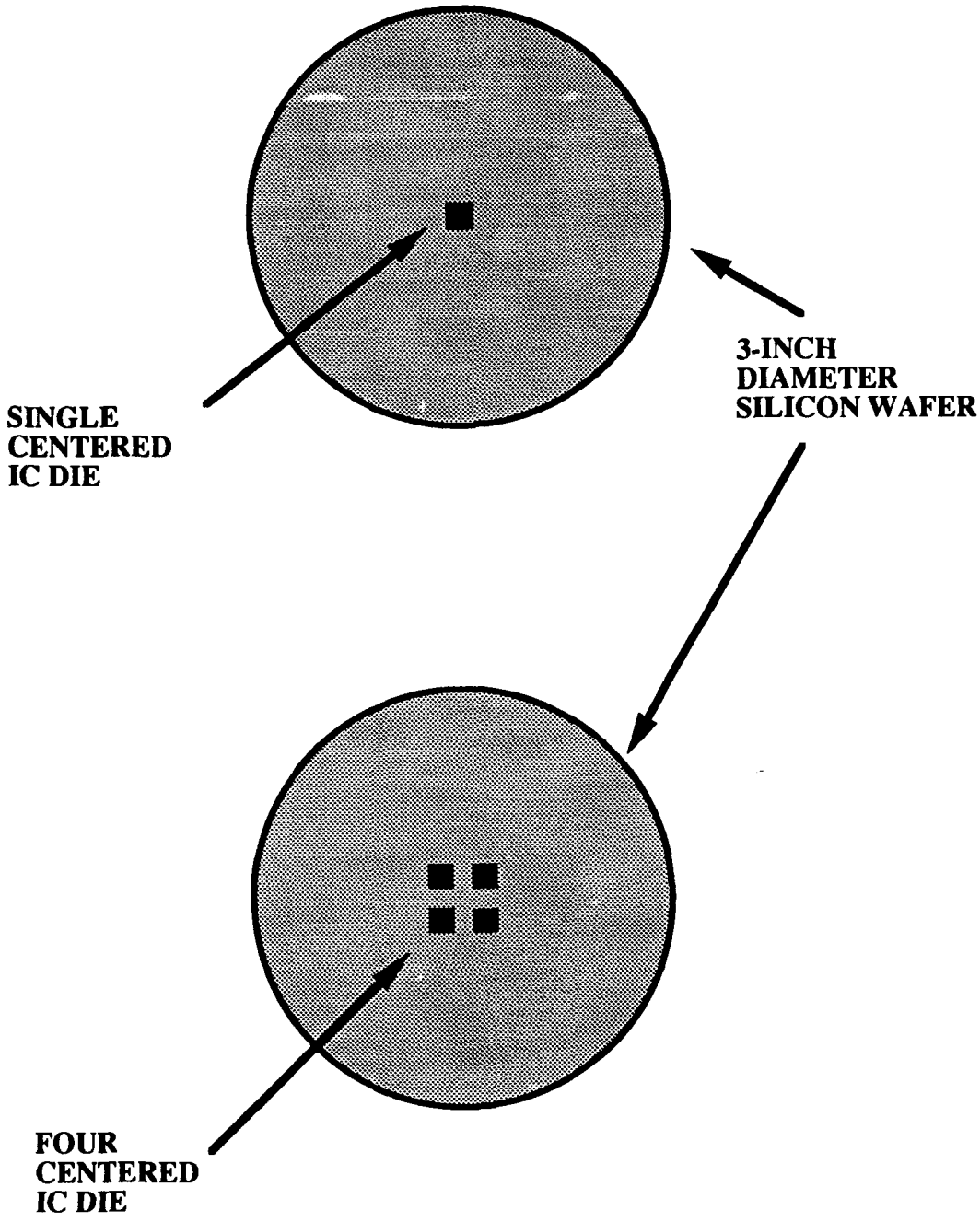
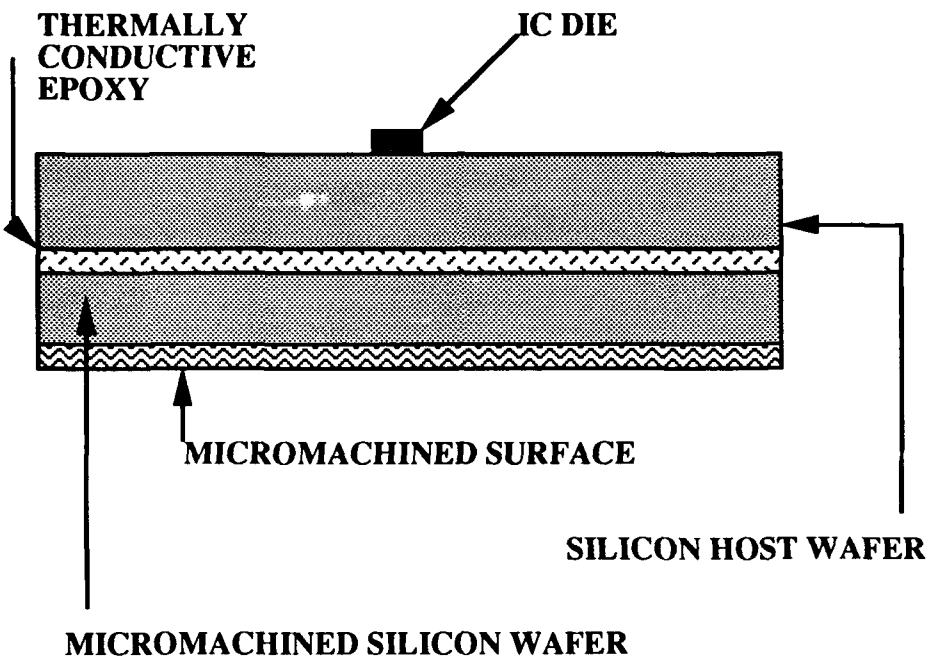


Figure I-10. Arrangement of the IC Die on the Host Silicon Wafers.



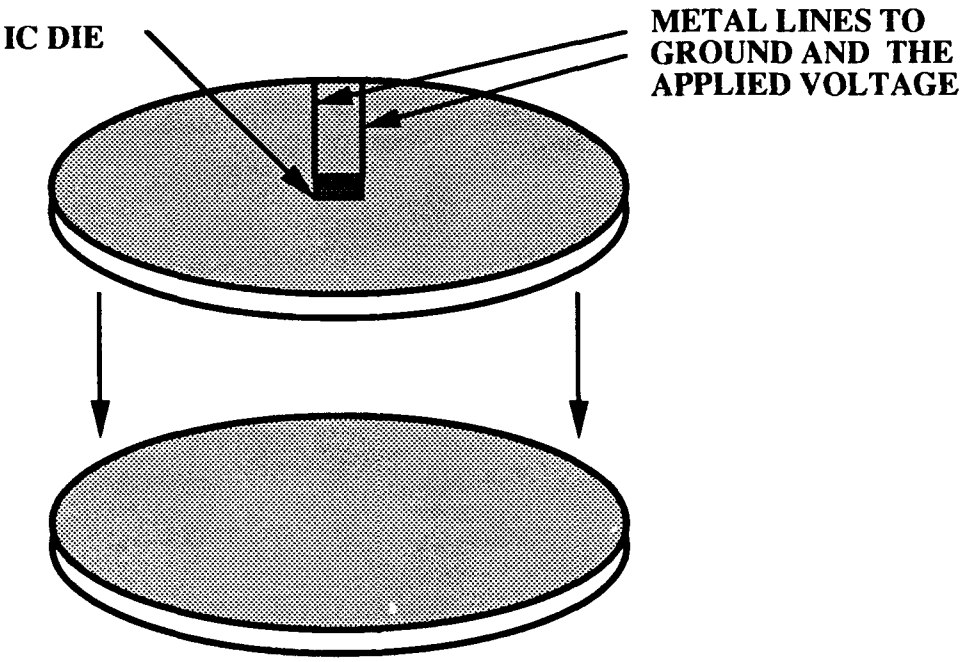


Figure I-11. Silicon Wafer Sandwich Configuration.

The single-crystal silicon wafer with the anisotropically etched micro-fluid channels was electrostatically bonded to Pyrex 7740 plate glass to seal the channel. Deionized water was pumped through the etched micro-fluid channels to facilitate heat flow from the devices and provide an alternate method of cooling [12; 13].

1.4 *Objectives.*

This thesis had several objectives:

1. Experimentally determine the characteristics of heat migration from several integrated circuit (IC) die resistors and thin-film sputtered resistors on a silicon wafer which was epoxied to a host (unetched) silicon wafer arranged in a sandwich configuration (Figure I-11).

2. Determine the passive heat dissipation of an unetched multichip host wafer compared to *in situ* anisotropically-etched heat dissipating structures.

3. Change several aspects of the experiment with respect to a control group of parameters:

a) Backside host silicon wafer surface texturing by micromachining.

b) Arrangement and number of heat-producing resistors on the multichip host wafer (Figure I-10).

c) Monolithic planar integrated circuitry versus epoxied in-place integrated circuits to realize a

multichip thermal module (Figure I-9).

4. Determine the effects of liquid cooling via a closed-loop micro-fluid channel configuration.

1.5 Approach for Analyzing the Micromachining Process Applied to the Thermal Dissipation Problem in Integrated Circuits

The following outline and accompanying flow chart depict the approach and sequence of critical tasks associated with this research (Figure I-12).

1. Wafer Preparation
   - (a) strip and clean 100 wafers (75, (100)-oriented; 25, (110)-oriented)
   - (b) grow a quality silicon dioxide layer and measure its thickness
   - (c) cover one side of the wafer with photoresist to protect it from the subsequent processing steps
2. Device Fabrication
   - (a) determine the required power dissipation from the heat-producing resistors
   - (b) design the resistors and contact pads
   - (c) generate MAGIC files
   - (d) order MOSIS fabricated resistors and measure their values

(e) sputter and pattern thin metal film resistors on silicon wafers and measure their values

3. Micromachining

(a) master the photolithography process for the necessary photomasks

(b) etch randomly spaced and sized pyramidal structures on the front of 25, (100)-oriented silicon wafers

(c) etch deep vertical-wall grooves on the front of 25, (110)-oriented silicon wafers

(d) etch micro-fluid channels in 10, (100)-oriented silicon wafers and seal (electrostatically bond) the micro-fluid channel with a pyrex glass plate

4. Device Mounting

(a) mount the MOSIS fabricated resistors on the front of the host silicon wafers

(b) epoxy the wafers with the sputtered thin-film metal resistors and the wafers with the mounted MOSIS IC die resistors to each type of micromachined substrate wafer (Figure I-11):

i) Normal (unetched, reference wafer)

ii) Randomly spaced and sized pyramidal structures

iii) Deep vertical-wall groove structures

iv) Micro-fluid channel

5. Instrumentation

(a) learn how to operate the infrared microscope and camera system

(b) design and fabricate a jig to hold a 2-D matrix of contact-type thermocouples

(c) configure the necessary instruments to generate heat in the resistors and measure their input voltage and current (calculate the input power)

6. Analysis

(a) obtain thermal images of the silicon wafers as heat is being dissipated

(b) generate the temperature profile on a wafer at various points spanning room temperature to the final operating temperature

1.6 Assumptions

This research is dependent on crystallography theory, heat transfer theory, chemistry and wet chemical etching theory, semiconductor fabrication theory, and the basic assumptions in each of these fields. The primary assumption is that various surface textures affect thermal dissipation, and that they will enhance heat transfer from IC devices.

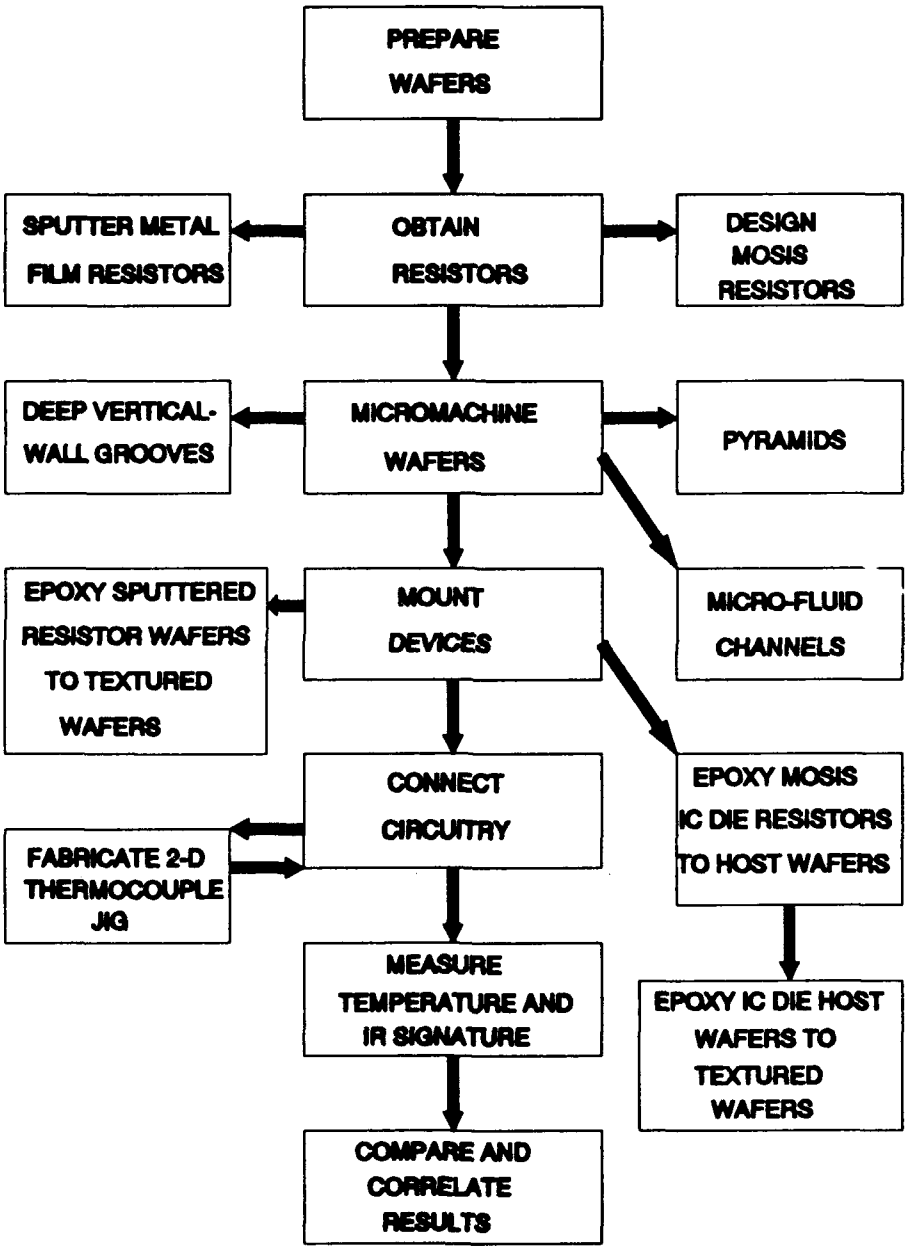


Figure I-12. Flow Chart of Critical Research Milestones.

1.7 Sequence of Presentation

There are five chapters in this thesis. Chapter II is a two-part literature review. The first part summarizes recent research in thermal dissipation from integrated circuits; the second part provides an overview of recent research in single-crystal silicon wafer surface texturing.

Chapter III documents the design considerations necessary for this research. It also documents the preparation and detailed procedures that were accomplished to satisfy the objectives of this thesis.

Chapter IV documents the results of the preparation, procedures, and measurements, including the data obtained from the experiments and simulations.

Chapter V discusses the results of the research accomplished in this thesis investigation, and it also provides conclusions and recommendations.

Appendices are included to emphasize the theory supporting this research. They also provide graphical support to the text and information concerning the equipment utilized in the experiments.

1.8 Summary

This thesis documents the motivation for the research, the approach used to realize the research objectives, and the experimental results obtained which led to the

determination of the thermal characteristics of micromachined single-crystal silicon wafers. The analysis was made with respect to thermal migration from heat-producing resistors through a host silicon wafer sandwich configuration. The resistor devices simulate IC die used in wafer scale integration. Two experimental characterization methods were employed to determine the heat flow from the resistors through the single-crystal silicon substrate, diamond impregnated epoxy, a host wafer, and a micromachined wafer. The methods employed were IR thermal imaging and direct contact thermocouple temperature readings.

II. Literature Review

In response to the reliability problems associated with the high density of modern integrated circuits (IC), significant research has been accomplished to alleviate the thermally-accelerated failure modes found in electronic systems. As the trend to increase the density of electronic components in an integrated circuit continues, interest in thermal management research will correspondingly grow, as indicated by the increasing number of publications addressing thermal management. This chapter provides an overview of recent research in heat transfer technology applied to integrated circuits by summarizing numerous selected articles pertaining to thermal management.

One particular area of research within the broad science of thermal management in integrated circuits, referred to as surface texturing, will also be reviewed. Surface texturing or micromachining is a relatively new approach to the thermal management problem in microelectronics; consequently, micromachining is reviewed in the context of its applications in several other areas of scientific research. Nevertheless, the application of micromachining to thermal management in integrated circuits contributed to the overall objective of this thesis.

2.1 Thermal Dissipation from Integrated Circuits

There are many aspects of thermal management. They are not always clearly distinguishable, but, for convenience, the significant aspects of thermal management may be categorized into specific engineering design approaches: heat sinks, packaging, cooling method or type of coolant, material selection, and component layout, etc. Of these, research in packaging microelectronics has received the most attention, perhaps because packaging may incorporate most or all of the other aspects.

The following subsections describe recent research in thermal management for microelectronics. The subsections are organized to develop some of the engineering design approaches listed above.

2.1.1 Heat Sinks. One of the most obvious ways to enhance thermal conductivity is to provide the IC-generated thermal energy with a plethora of paths along which to flow to a mass with a lower temperature, or to alternatively, provide paths with less thermal resistance (Figure II-1). Heat sinks provide such paths.

For example, in 1989, Charles J. Murray published an article describing a method of cooling microcomputers using liquid-filled pouches [14]. Developed by the 3M Company (3M Industrial Chemical Products Division, St. Paul, MN),

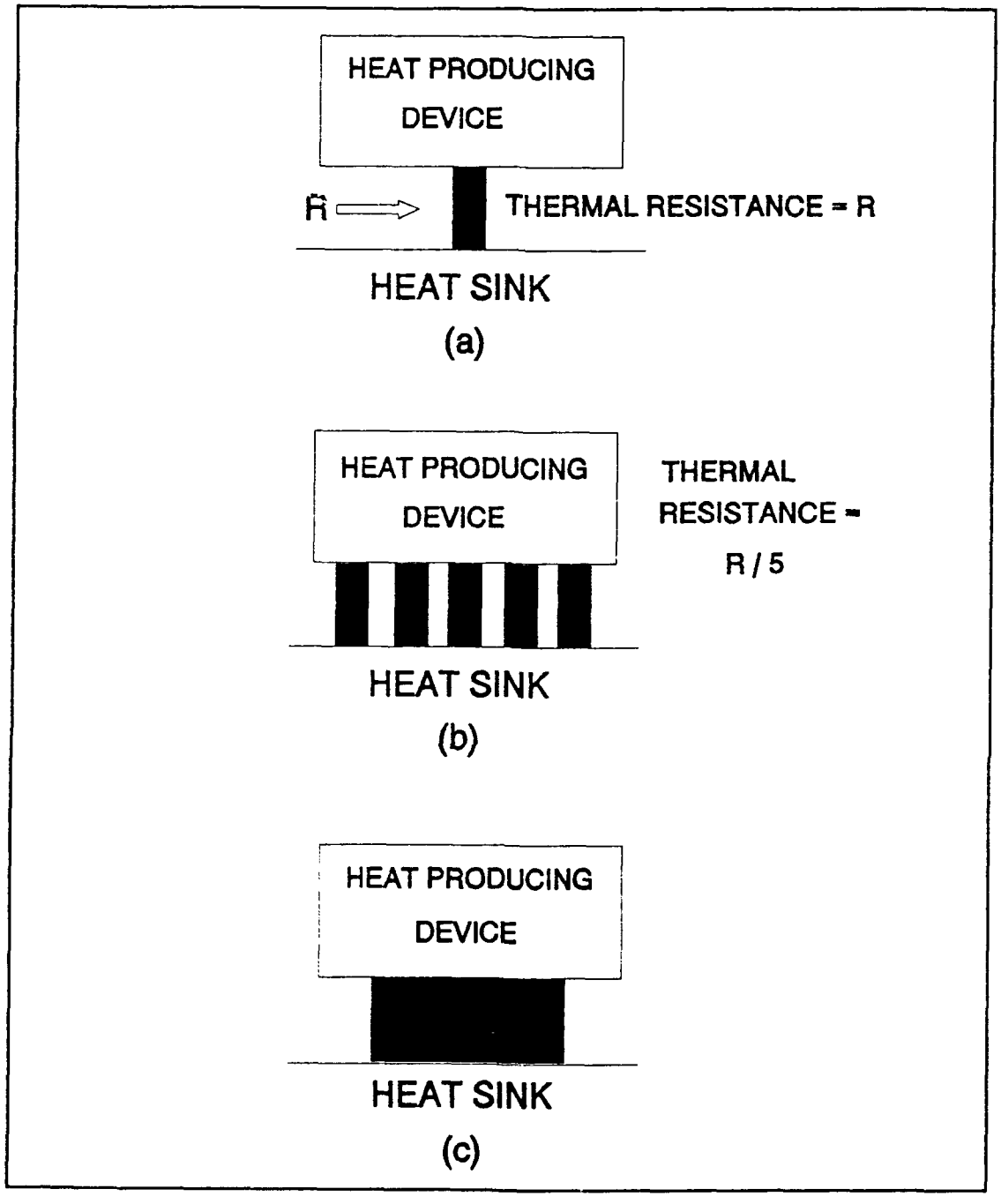


Figure II-1. Thermal Conductivity: Thermal Resistance From a Heat Producing Device to a Heat Sink. (a) Simple Heat Sink Path, (b) Multiple Heat Sink Path, and (c) A Different Material or Size of Path with Inherently More Thermal Conductive Paths.

the pouches filled with Flourinert were used as heat sinks in supermicrocomputers. Heat was conducted into the Flourinert from the electronic devices which were in contact with the pouches, and convection currents within the fluid carried the heat to a cold plate where it was conducted from the fluid to the plate. The Flourinert heat sink was claimed to reduce the computer's operating temperature by 73%, as well as keeping the temperatures more uniform throughout the computer circuitry which contacted the pouches (Figure II-2) [14].

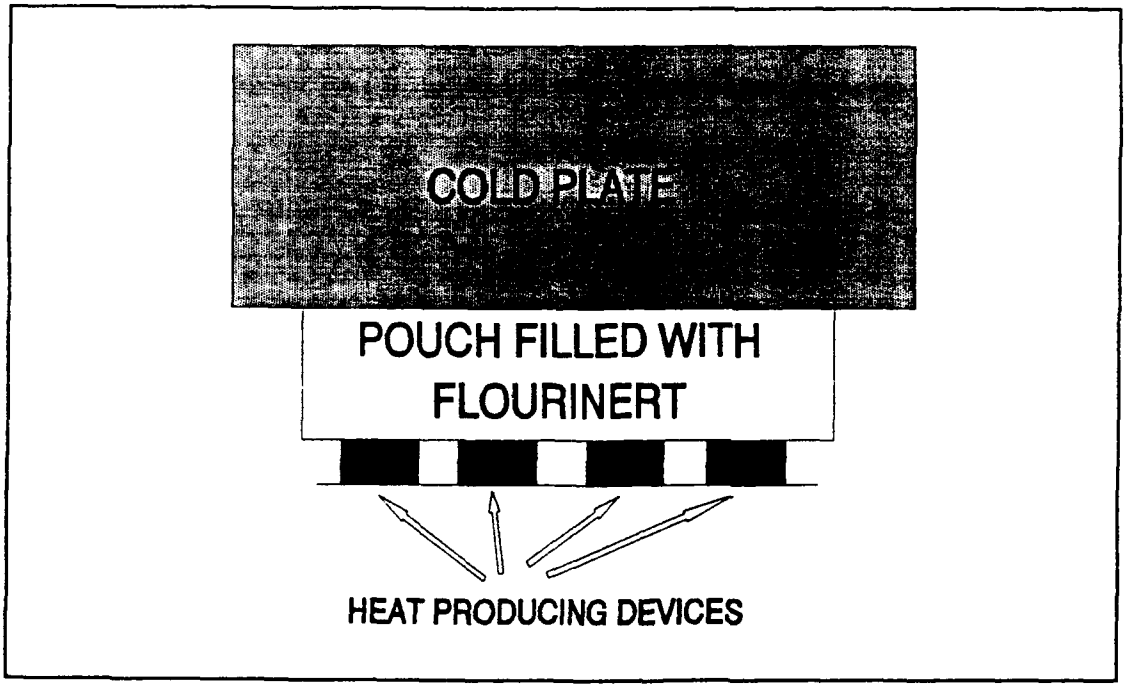


Figure II-2. Flourinert Filled Heat-Sink: The Heat Flows By Conduction From the Devices to the Flourinert Pouch Where It Is Convected Toward the Cold Plate and Finally Conducted Into the Cold Plate (Heat Sink) [14].

In the introduction to, "Chip Environment Key To Digital Performance," printed in the Winter 1990 issue of, Computer Technology Review, by Irwin Maltz, heat and voltage variations were cited as the two most crucial environmental factors limiting the performance of integrated circuitry [15:23-25]. Of the two, heat was regarded as the more serious problem.

In the attempt to increase computer operating speeds, semiconductor devices are being packed more densely to reduce lead lengths between the devices, and consequently, reduce delay times [15:23-24]. Thus, the corresponding heat which is generated also becomes more intense, and cooling becomes a more serious problem.

Irwin Maltz described the Velox Computer Technology, Inc. solution to controlling heat dissipation. Velox's cooling module consists of a thermoelectric-device; cold plates; finned heat sinks; a temperature sensor; and a dual clock speed generator [15:24]. The modules actively pump heat from the devices by using dissimilar metals (the thermoelectric-device) which create an electrical current, allowing heat to migrate from one side of the pn-junction to the other side (Figure II-3) [15:24-25]. The heat was removed via heat sinks, and the modules ultimately reduced the operating temperature of the ICs below the ambient

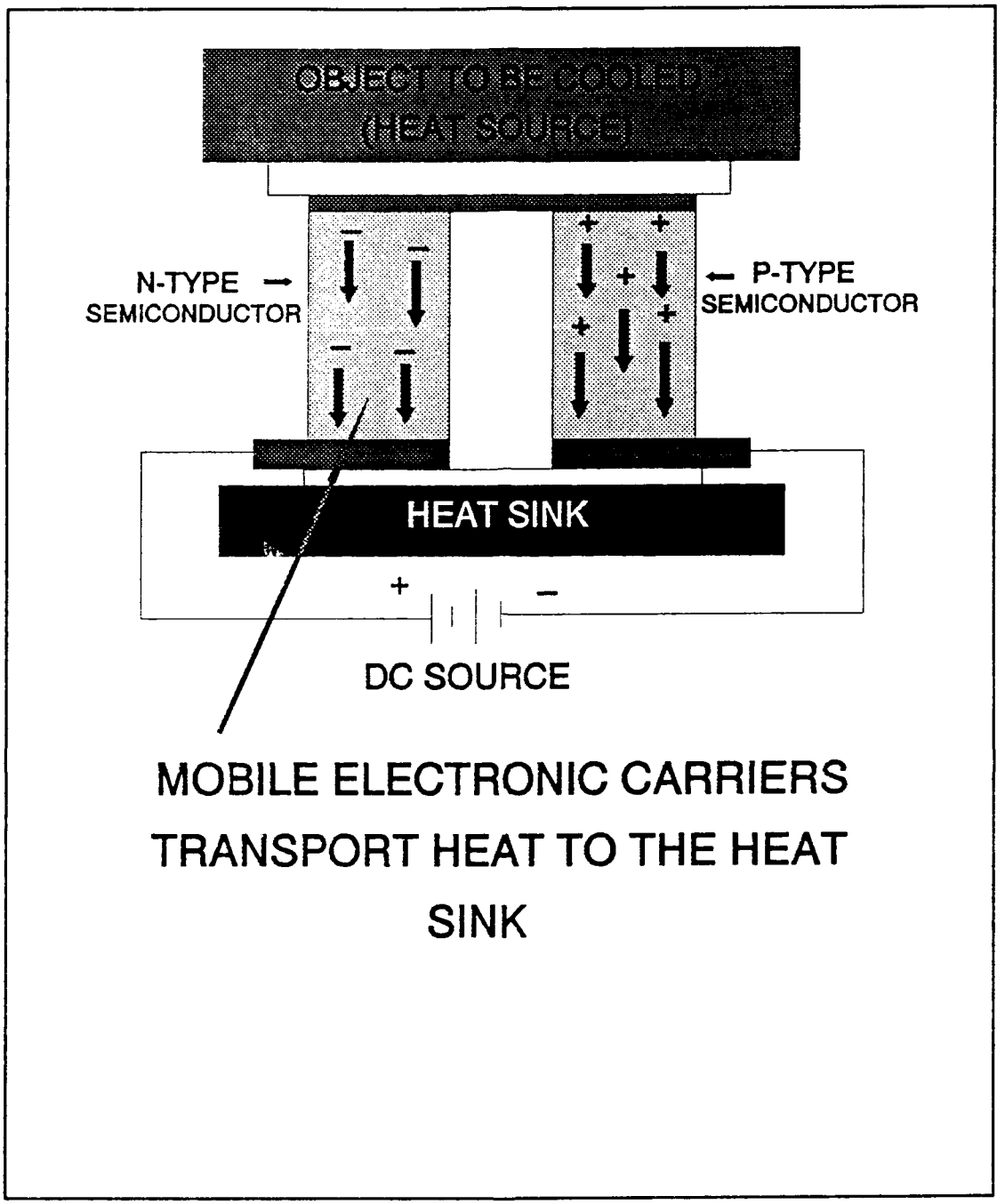


Figure II-3. Thermoelectric Device [15:24].

temperature, which is impossible to accomplish with passive cooling techniques [15:24].

Claude Hilbert, *et al* have developed a high performance, air-cooled heat sink technology for integrated circuits. They claim in their report, "High Performance Air Cooled Heat Sinks for Integrated Circuits," that air-cooling was generally less expensive and more portable (Figure II-4) [16:1022-1031]. The article also reported that high heat transfer was attained with turbulent air flow around finned structures; however, laminar flow through microchannels has been demonstrated to be more efficient [16:1022].

Their research primarily involved the analysis of thin copper fins with varying geometries and configurations attached to the backsides of IC die which acted as heat exchangers [16:1024-1025]. Heat was generated with thin-film resistors. A diode array was used to record temperatures [16:1025]. Type-T thermocouples were used to record the laminar air flow temperatures by placing them among the fins (Figure II-5) [16:1027]. Two different arrays of fins were able to remove more than 600 watts (W) of heat from the IC die hosting the thin-film resistors. This heat exchange was comparable to that attained with liquid cooling methods [16:1030]. Where space is not critical, these types of cooling structures suffice as good thermal management design alternatives.

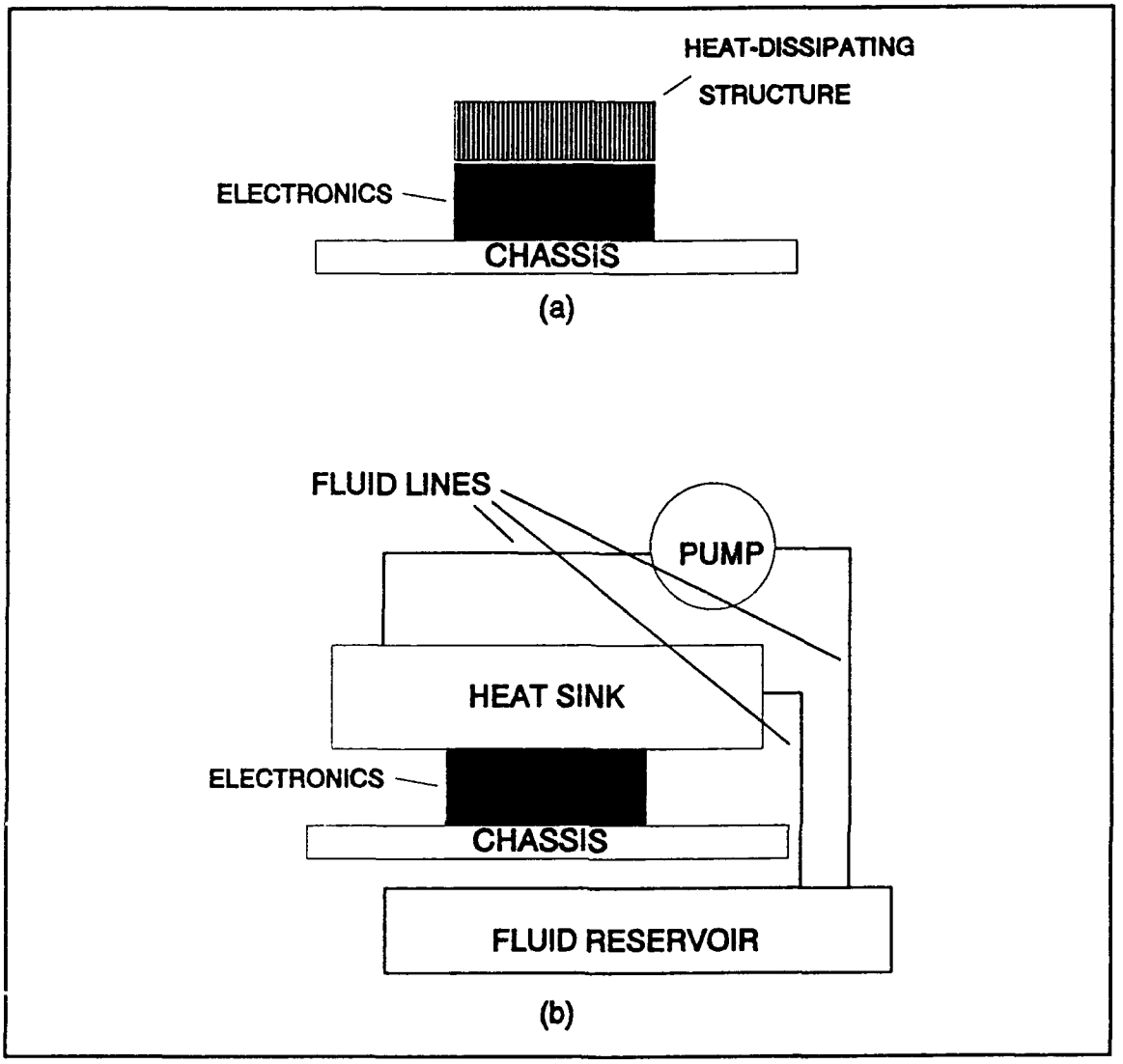


Figure II-4. Logistics of Cooling: (a) Air-Cooling and, (b) Liquid-Cooling.

Crystalline GaAs (0.455 W/(cm-K) substrates have an inherently lower thermal conductivity compared to single-crystal silicon (1.412 W/(cm-K) [17:140]. Gordon C. Taylor, *et al* have claimed a 45% reduction of thermal resistance in high-power GaAs MMIC power amplifiers as a result of their research [17:140-142].

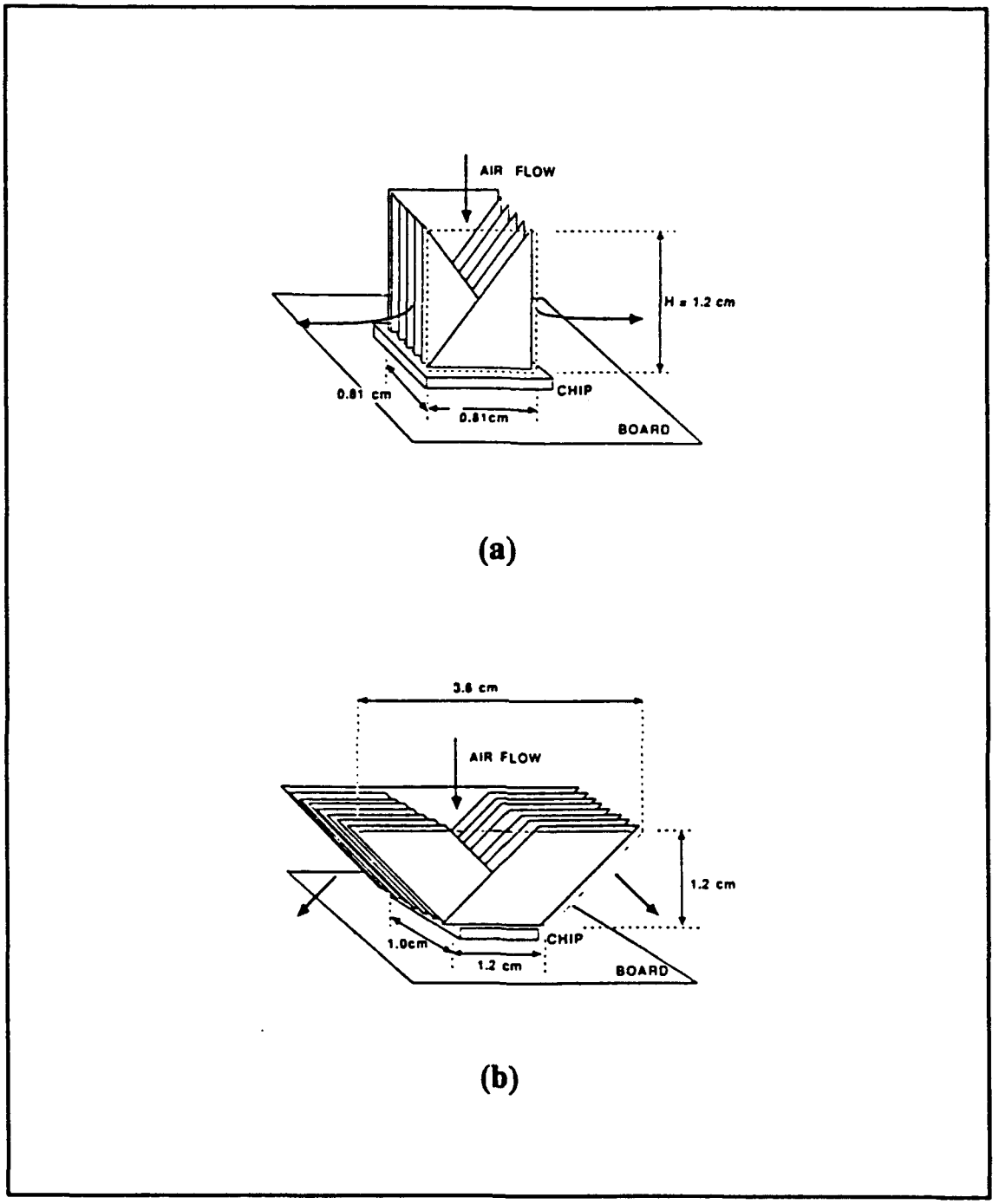


Figure II-5. High Performance Air Cooled Heat-Sinks: (a) Design #1 and, (b) Design #2 [16:1024].

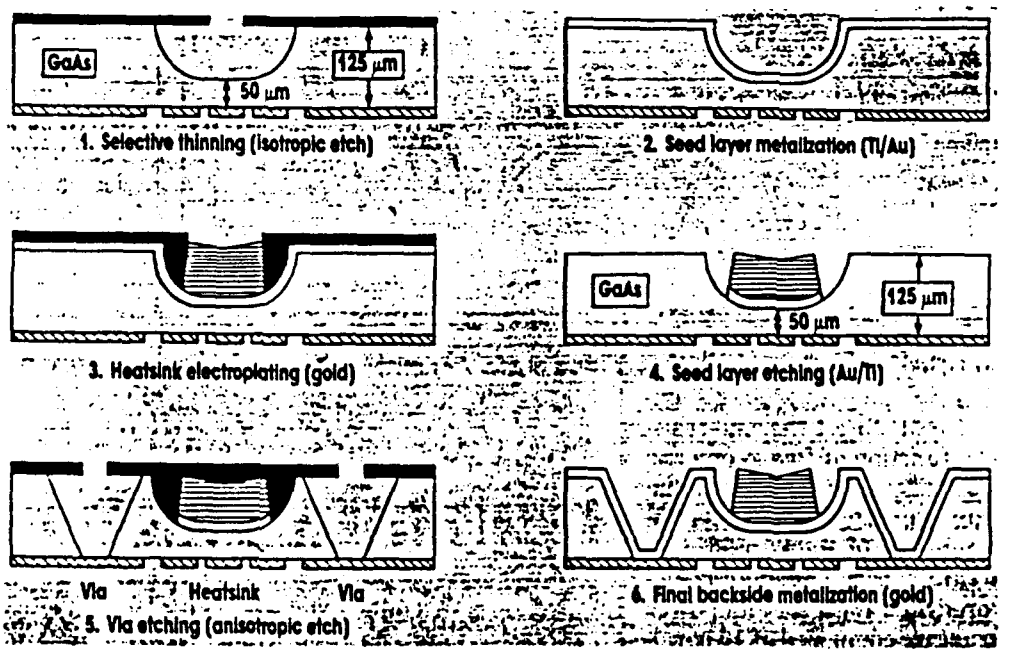
They developed a process to selectively incorporate gold heat sinks directly under the active channel areas of the metal-semiconductor field effect transistors (MESFETs) [17:141]. Only these active regions were isotropically etched on the backsides of the GaAs wafers (Figure II-6). These regions were also metallized with a Ti/Au seed layer and then electroplated with Au heat sinks [17:142]. Table II-1 provides a comparison of the theoretical and experimental results.

Table II-1: Thermal Resistance of Different GaAs MMICs [17:140].

DEVICE SIZE (mm)	POWER (W)	GATE-GATE SPACING (mm)	SUBSTRATE THICKNESS (mm)	WITHOUT HEATSINK (°C/W)		WITH HEATSINK (°C/W)	
				PREDICTED	MEASURED	PREDICTED	MEASURED
1.2	0.5	18.5	100	60.2	58.0	35.9	31.5
2.4	1.0	18.5	100	30.5	28.3	18.0	17.8
2.4	1.0	18	125	47.8	--	33.7	30.6
2.4	1.0	26	125	42.8	--	29.8	33.6
3.0	1.5	18	125	38.6	--	27.1	24.6
3.2	1.5	26	125	32.4	--	22.4	25.4

2.1.2 Packaging. There are many technical articles which discuss the effects of integrated circuit package geometry relative to thermal resistance. For example, Pence and Krusius have reported on the geometrical IC packaging effects on thermal management for six different configurations (Figure II-7) [18:245-251]. Their research supports the conclusion that packages with low thermal

resistance with natural convection cooling have relatively high thermal resistance when cooled with forced fluid techniques [18:245-251]. In their analysis, thermal simulations were used to generate temperature profiles for a pin grid array (PGA), a flatpack, a standard dual-in-line package (DIP), a Si-on-Si flip-chip hybrid, a Si-on-Si embedded hybrid, and an unpackaged silicon IC relative to five cooling techniques: natural convection, forced laminar air, forced turbulent air, forced water, and microchannel cooling [18:248]. From the resulting temperature profiles, Pence and Krusius theoretically determined that the six package configurations performed very differently under the comparative cooling conditions [18:250]. Three important observations were formulated: 1) natural convection is ideally suited to those IC packages with the largest surface area, 2) radiation becomes the dominant heat transfer mode at extremely high temperatures, and 3) the highest heat flux density was achieved with microchannel cooling [18:246-250]. Table II-2 compares the six configurations relative to four of the cooling techniques with respect to their maximum heat dissipation along with their relative ranking (the number in parentheses). The lowest number in parentheses indicates the most heat dissipated in each category.



THE HEAT-SINK PROCESS CONSISTS OF SIX FABRICATION STEPS WHICH ARE FULLY COMPATIBLE WITH STANDARD MMIC PROCESSES

Figure II-6. Integrated Gold Heat-Sinks [17:142].

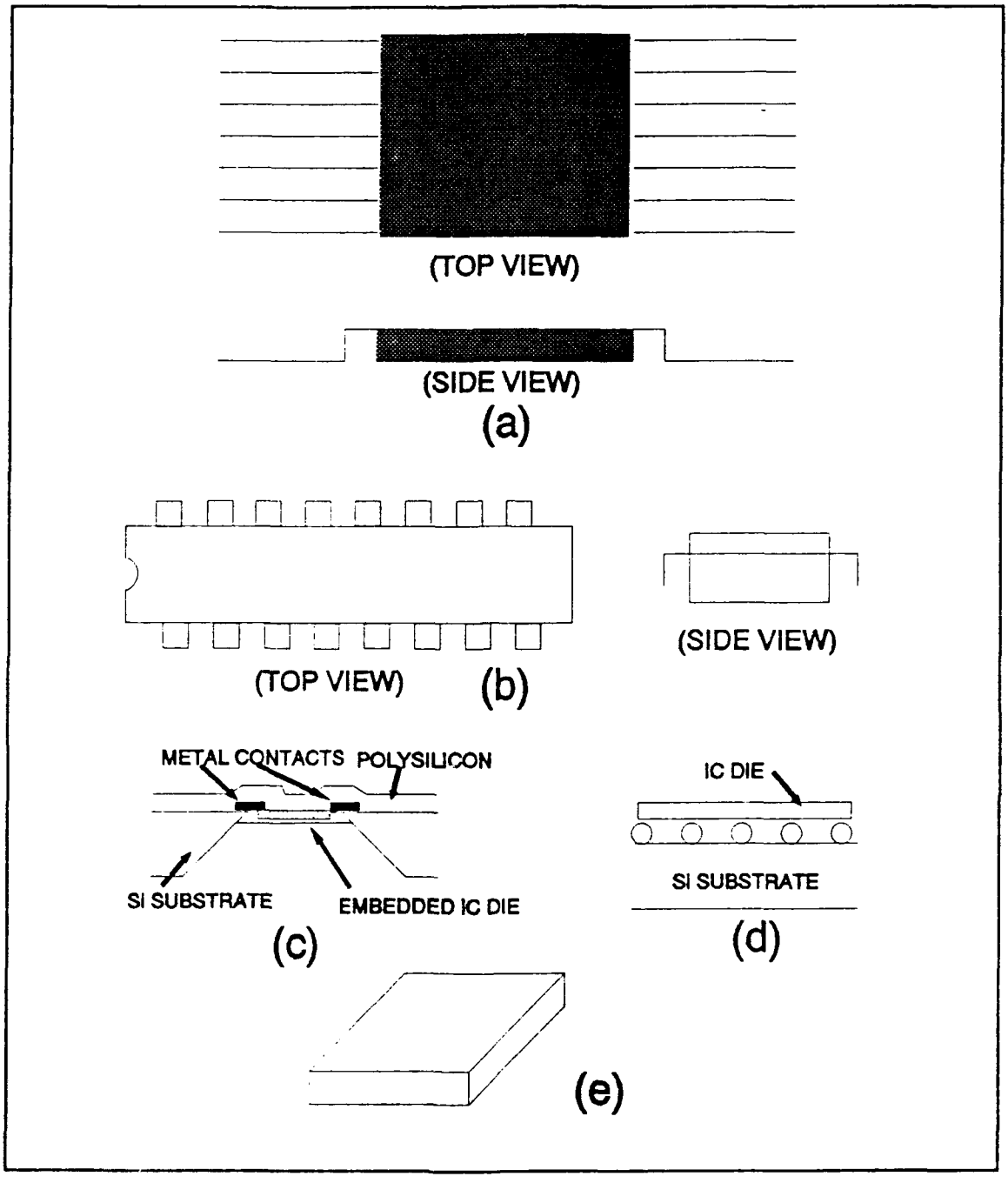


Figure II-7. Six Representative Packages: (a) Top and Side View of a Flatpack, (b) Top and Side View of a Dual-in-Line-Package, (c) Embedded Hybrid, (d) Flip-Chip Hybrid and, (e) Unpackaged IC Die [18:247].

For example, the flatpack has the best heat dissipation under natural convection; the bare chip has the corresponding worst heat dissipation.

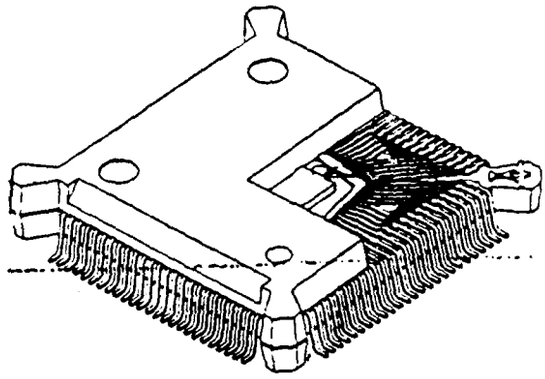
Table II-2: Maximum Heat Dissipation in Watts for Six IC Packages Relative to Four Different Cooling Conditions [18:250].

PACKAGE TYPE	NATURAL CONVECTION	LAMINAR AIR	TURBULENT H_2O	MICROCHANNEL
PGA	2.00 (2)	6.4 (1)	48.3 (3)	781.3 (3)
FLATPACK	2.20 (1)	6.1 (2)	84.7 (1)	280.1 (4)
DIP	2.00 (3)	5.4 (3)	48.7 (2)	102.2 (6)
EMBEDDED	0.80 (5)	2.6 (4)	39.7 (4)	263.9 (5)
FLIP-CHIP	0.85 (4)	2.5 (5)	29.9 (6)	781.3 (2)
BARE CHIP	0.60 (6)	2.5 (6)	34.2 (5)	1694.9 (1)

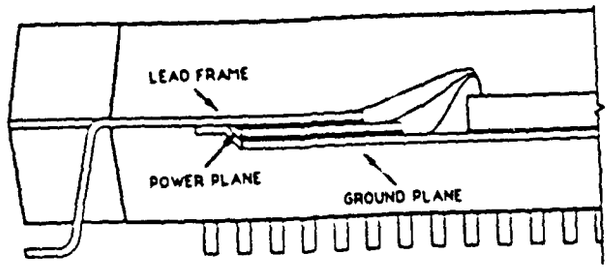
There are numerous unique design applications reported in the literature for packaging integrated circuitry with the goal of improving thermal management. One example is an enhanced plastic-quad-flat-pack (PQFP) designed by Aghazadeh and Mallik (Figure II-8) [19:975-979]. Single layer PQFPs have thermal, electrical, and noise limitations [19:975]. The addition of a power and a ground plane, as is commonly found in a multilayer package, reduces bonding wire lengths. The shorter bonding wires have less inductance, and consequently, less noise [19:975]. The shorter wire bonds are also inherently shorter thermal conductive paths [19:975]. Aghazadeh and Mallik improved the thermal dissipation of a PQFP by employing a multilayer design where the power and ground leads were fabricated in separate metal

layers [19:975]. These metal layers were shown to distribute the heat more uniformly, and they also reduced the thermal resistance from the package's junction to the ambient environment by 38% [19:977]. They further reported that various configurations of the multilayer PQFP designs reduced the thermal resistance from 38% to 43%, as well as reducing the resistance of the wire bonds of the devices packaged in the PQFP [19:975].

In 1987, Hwang, Turlik, and Reisman authored a technical report for the Microelectronics Center of North Carolina (MCNC) entitled, "A Thermal Module Design for Advanced Packaging" [20]. They analyzed a wafer scale multi-chip package which hosted an array of 25, 1 cm x 1 cm ICs with underlying microchannels (Figure II-9) [20:1]. The performance of deep microchannels were compared to shallow microchannels for two different water flow rates (499 cc/sec and 39 cc/sec) relative to their ability to cool the ICs which were operated to dissipate a maximum of 40 W each [20:1]. They further optimized their module design with an analysis that considered the microchannel dimensions, position of the microchannels below the IC array, spacing between the microchannels, number of microchannels, and the resulting statics and dynamics of the material (silicon carbide) [20:8-12]. The heat transfer results were reported



(a)



(b)

Figure II-8. Plastic-Quad-Flat-Pack (PQFP): (a) Cutaway View of a Multilayer PQFP and, (b) Cross-Sectional View of the PQFP [19:975-976].

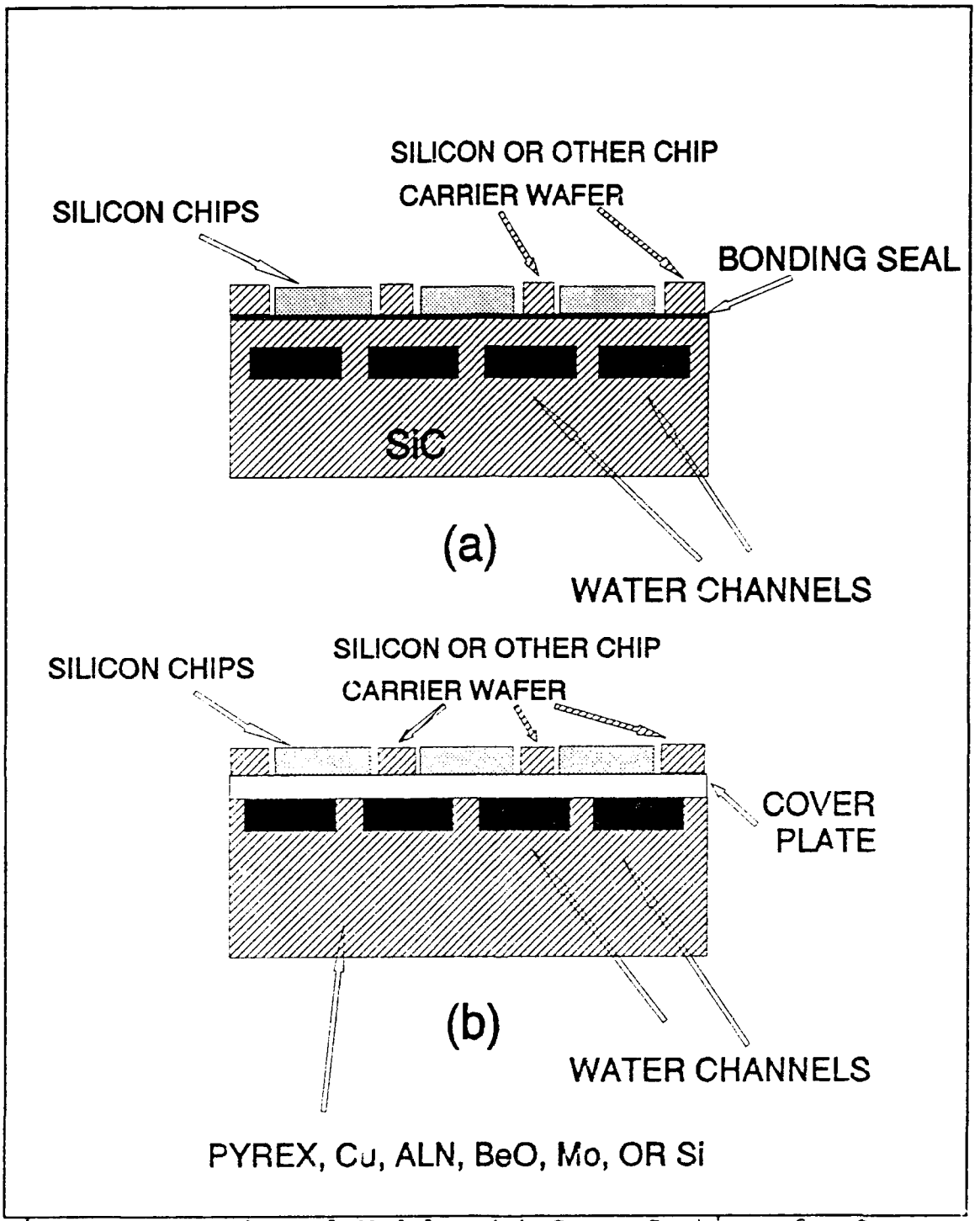


Figure II-9. Thermal Module: (a) Cross-Section of a One Piece Module Design and, (b) Cross-Section of a Two Piece Module Design [20:4].

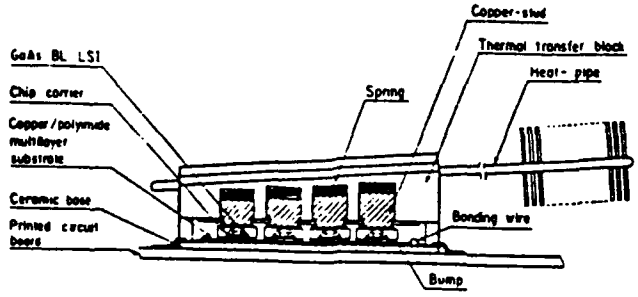
for a variety of variations in the module's design, but their research was only theoretical. In May 1990, Witzman, Smith, and Metelski presented their research results concerning silicon device packaging and the effects on reliability, specifically due to silicon device interconnects [21]. Their research showed that, for silicon, many failures in devices occurred below 150 °C, and failures increased with variations in several environmental parameters (for example, temperature) [21:947]. They detailed silicon device interconnect failure modes in their report, and this limitation was observed to be the key factor for device operation at elevated temperatures [21:948-951].

2.1.3 Cooling Method. A cooling method for semiconductor devices can be either passive or active. A passive method employs thermal conduction from the heat generating device through its material and adjacent mass of material to the peripheries of the device/chip/module/package. The heat is naturally conducted into a large heat sink or the ambient air where it is convected away. Passive cooling also includes thermal radiation (which may be the only means for thermal dissipation in some applications). On the other hand, active cooling refers to the enhancement of thermal

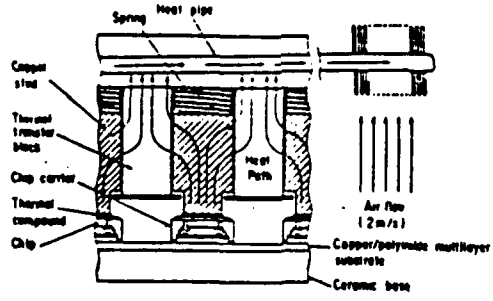
conduction or convection beyond their natural rates which are established by the environment.

Takeshi Miyagi, *et al* wrote an article entitled, "GaAs Multichip Module for a Parallel Processing System," which develops a "high speed data transfer network for a parallel processing system" capable of operating at 100 MHz, and it dissipates 90 W of heat [22:828]. They found it desirable to cool their GaAs multichip module with four, finned, heat-pipes along with forced-air cooling (Figure II-10) [22:828]. The heat-pipe cooling module was invented specifically for their GaAs module; it includes a thermal transfer block, copper studs, four heat-pipes, and a plate with integral thin cooling fins [22:828]. This configuration functionally resembles an automobile engine radiator, and it efficiently dissipates 90 W of heat with a 2 meter/second air flow rate and insignificant acoustical noise [22:832]. They reported that, "the total thermal resistance from the chip to the ambient was approximately 3 °C/W" [22:830].

Liquid cooling is an effective heat transfer technology for cooling semiconductors. Liquid cooling can significantly reduce the operating temperatures of semiconductor devices and help maintain uniform temperatures in ICs. However, liquid cooling systems generally add appreciable weight and costs to a total electronic system. They also manifest potential failure modes.



(a)



(b)

Figure II-10. Heat-Pipe Cooling Module (HCM): (a) Cross-Sectional View of Assembled Module and, (b) Heat Path in HCM [22:831].

Liquid coolant systems also affect a significant design limitation concerning the density of device packaging. That is, devices must be spaced sufficiently far apart to accommodate the coolant system's fluid channel dimension requirements [23:1040].For example, a particular microchannel may effectively extract 50 W of heat from an adjacent square centimeter region hosting several devices for a specific coolant type, flow rate, and microchannel dimensions. If the devices dissipate 2 W each, the circuit density is limited to 25 devices adjacent to the microchannel, and other heat dissipating devices must reside on another square centimeter of the circuit layout.

Wataru Nakayama theoretically analyzed the tradeoff between the density of logic gates and the coolant requirements. He reported that decreasing the lengths of connections between ICs increases the circuit operating speeds and circuit densities, but it also increases the thermal density and does not allow sufficient space for adequate cooling [23:1040-1049]. Nakayama concluded that there are increased wiring distance penalties when liquid cooling techniques are employed [23:1046]. He provided some general wire length formulas in an appendix for model predictions concerning microchannel dimensions, but he excluded the details of his quantitative predictions.

Coolant selection, as well as coolant method, is a thermal management design consideration. Longenecker and Ohlrich discussed the characteristics of water as a semiconductor coolant in, "Cooling Power Semiconductors: Considerations for Water Cooled Systems" [24:16]. They presented an overview of water chemistry, biological contaminants, dissolved solids and gases, additives, and acidity/alkalinity with respect to semiconductor cooling system design and material options [24:16,18,20,22-24,26].

Longenecker and Ohlrich also reported that several compounds are easily dissolved or suspended in water. These compounds, or impurities, may have undesirable effects on the coolant system's components [24:16,18]. For example, suspended particles, such as scale or sand, can be highly abrasive to components in high velocity fluid paths and form particle sediments that clog fluid channels in low fluid velocity paths [24:18]. Similarly, biological growths (bacteria) can form obstructions, and they can also form thermally insulating films, reducing the thermal efficiency of the cooling system [24:18]. The films reduce the conduction of heat from the cooling channel walls to the cooling fluid. However, chemicals used to prevent biological growths can also degrade cooling systems ("chlorine is an effective oxidizing biocide," but it corrodes copper) [24:18]. In addition, CO_2 and O_2 dissolved

in water in sufficient concentrations change the pH and cause the corrosion of several metals [24:18].

2.1.4 Material Selection. Thermal management can be improved with proper material selection. Materials should be appropriately selected for the heat sinks, packaging, and the actual semiconductor devices.

One material with several appealing characteristics for semiconductor fabrication is diamond. Not only does diamond have a very high melting point (approximately 3550 °C), a significant resistance to radiation damage of its crystal lattice structure, superior mechanical strength, and a low affinity for corrosion, it also possesses a superior thermal conductivity [25:49; 26:22].

General Electric's Research and Development Center has synthesized diamond samples from carbon-12 which exhibit a thermal conductivity of 33 W/cm/K, which is 50% larger than natural diamond and 850% larger than copper [26:22-23]. Thin films of this material have a potentially broad range of applications for heat sinks in IC packaging.

In another example of materials applied to thermal management, Arthur O. Capp, Jr. describes a technique for applying thin films of pure copper to substrates as a "new concept in thermal management" in his publication entitled,

"Pure Copper Circuit on Ceramic Substrate Process" [27:37-39]. The pure copper was electrochemically deposited over all of the exposed surfaces and through-holes of an IC die to facilitate thermal conduction to the surfaces [27:37-39]. An enhancement in thermal dissipation was qualitatively depicted but not quantitatively reported.

In September, 1990, Ken Gilleo reported the results of research using flexible printed circuitry as a thermal management scheme in his publication entitled, "Expanding the Capability of Flexible Circuitry" [28:18-21]. In his investigation, a thin, flexible base of polyimide, employed as a printed circuit board, provides numerous, short, heat conducting paths, and the polyimide board can be readily bonded to an even more conductive material [28:21]. Mr. Gilleo also suggested enhancing the circuit's thermal conductivity with copper coated through-holes to provide more parallel paths of conduction. This technology permits thermal transfer in excess of 5 W per square inch [28:18].

In "Maintaining Aluminum Nitride Consistency", Betsy B. Poole discussed research concerning Aluminum Nitride (AlN) in thermal conduction applications [29:19]. Thermal conduction in AlN substrates were measured and correlated with variations in the material's consistency relative to different batches of substrates. She concluded that, "the

thermal performance properties of AlN make it particularly well suited for many hybrid industry applications" [29:21].

Excessive thermal stress is an effect of poor thermal management problems, and the resulting failures can be reduced with thoughtful material selection. My N. Nguyen published an article entitled, "Low Stress Silver-Glass Die Attach Material," to convey the results of research concerning modified sintering techniques [30:478-483]. Silver-filled glass materials are commonly used to attach IC die in ceramic packages, but stresses are created during heat treatment [30:478]. He reported that, "small amounts of appropriate additives provide the process control necessary to relieve the stresses by controlling the sintering rate" [30:478]. The article compared three proprietary additives (reported only as materials A, B, and C) that were dispensed into a silver-glass IC die attach composite during its synthesis, and the author claims a significant decrease in the voids and cracks in large IC die bond areas due to the controllability facilitated by the additives [30:478-483].

In IC device fabrication, IC die are frequently epoxy bonded to substrates. The epoxy is a critical path for heat transfer in wafer scale integration. There is a plethora of epoxies to select from. Grenon and Nagarkar published the

results of their research on silver-filled epoxy die bonding with respect to thermal performance and reliability [31:63-66]. They established the severity of degradation of die bond integrity and degradation of thermal resistance uniformity due to thermal cycling [31:64-65]. However, their research showed minimal effects due to thermal shock [31:64-65]. Several groups of silicon IC die, epoxy bonded to copper substrates, were subjected to thermal shock or thermal cycling, and their resulting shear strengths were compared to the shear strength of a control group. Also, they observed that the thermal resistance of the epoxy was enhanced after exposure to thermal shock and cycling. The thermal resistance of the control group was 1.71 °C/W, and its shear strength was 67.6 kg. In the two groups subjected to thermal shock, their thermal resistances were increased to 1.91 °C/W and 2.16 °C/W, and their shear strengths were reduced to 67.4 kg and 61.5 kg, respectively. For six groups subjected to thermal cycling, thermal resistances ranged from 1.92 °C/W to 2.48 °C/W, and shear strengths ranged from 67.6 kg to 32.0 kg [31:64].

2.2 Silicon Micromachining

Recent thesis work at the Air Force Institute of Technology (AFIT) has involved micromachining single-crystal silicon wafers to achieve various surface textures, and it

has also involved determining the effects of texturing on light absorption and reflection properties.

Captain M. Wayne Carver (GE-88M) used the silicon micromachining process in his thesis to anisotropically etch single-crystal, (110)-oriented silicon wafers. Capt Carver etched large areas of these silicon wafers with sloped-wall grooves that ranged from 5 microns to 100 microns in width, and 870 microns to 1,140 microns in length [3]. He optimized a groove design that was 5 microns wide, 1,000 microns long, 290 microns deep, and they were spaced 25.4 microns apart [3]. Capt Carver proposed that his research would improve the efficiency of solar cells by exploiting the benefits of this particular textured surface for reducing light reflection. Additionally, he predicted that this solar cell design would be more radiation resistant and more efficient for converting solar energy into electrical energy [3].

Captain Stephen Uyehata 90D) also employed the micromachining process to create four different textured surfaces on single-crystal silicon wafers. In his thesis, Capt Uyehata anisotropically-etched deep vertical-wall grooves, and he isotropically-etched randomly spaced and sized pyramid structures to determine their significance and application to low observables technology [4].

In his thesis literature review, Capt Uyehata outlined the genesis of micromachining. He identified research in anisotropic etching as early as 1969 by D. B. Lee at the General Electric Corporation, similar work by J. B. Price at Motorola, Inc., and by Allen and Routledge in 1983 [4:(2-13)]. He also identified subsequent research in surface texturing as it applied to several spin-off technologies: micromachining V-shaped grooves and randomly spaced and sized pyramids by Baroana and Brandhorst with NASA in 1975, micromachining V-grooves by Chappell at the University of California at Berkeley in 1978, micromachining V-grooves by Borden and Walsh with Varian Associates and Nasby with Sandia Laboratories, micromachining randomly spaced and sized pyramids by Baroana and Brandhorst in 1975, micromachining deep vertical-wall grooves by Smeltzer, Kendall, and Varnell with Texas Instruments, Inc., in 1974, micromachining inverted pyramids by Miner and Cristel with the SERA Solar Corporation in 1988, and micromachining inverted pyramids by Blakers with the University of New South Wales in 1989 [4:(2-15)-(2-21)].

Micromachining is also becoming popular in the industrial setting. An article entitled, "Low-Thermal-Conduction Links for Silicon Sensors," in the February 1991 issue of NASA Tech Briefs, describes research involving silicon micromachining by D. Brent Mott of the Goddard Space

Flight Center in Greenbelt, Maryland [32:38]. Mott used a dilute solution of ethylene diamine pyrocatechol (EDP) to anisotropically etch single-crystal silicon [32:38]. Silicon thermal links were immersed in EDP for five minutes at 95 °C to produce a textured surface of randomly spaced and sized pyramids, with bases ranging in size from approximately one micron to five microns [32:38]. The intended application was to reduce the thermal conductivity of monolithic, silicon, thermal-link structures [32:38]. The authors reported that a large density of phonon scattering sites among the pyramids reduced the thermal conductivity of the thermal-links and allowed them to be made shorter, thicker, and consequently, mechanically stronger [32:38].

A large variety of combinations of chemicals, crystallographic orientations, and types of photolithography can be used to vary the parameters of the micromachining process. Since micromachining is a relatively new technology, the area of research for these factors is virtually uncharted. In what may be considered a typical micromachining research effort, U. Schnakenberg, *et al* investigated the effects of additives, pH, and temperature variations of the etchant solution for micromachining single-crystal silicon [33:1]. They found it was possible to control the etch rate by manipulating these three

factors. Specifically, they could "increase the etch rate in the (100)- direction" and suppress the resulting formation of "pyramidal-shaped hillocks" by adding a small amount of hydrogen peroxide (H_2O_2) to the ammonium hydroxide-water (AHW) etchant [33:1-3]. The H_2O_2 acts as a buffer in the AHW solution, stabilizing the pH, which suppresses the formation of hillocks that impede the etch rate in the "(100)-direction" [33:5]. Schnakenberg also investigated selectivities due to the variations in etchant parameters with respect to many materials that were deposited, grown, or sputtered on the single-crystal silicon substrate.

J. Branebjerg, *et al* investigated another parameter of the silicon micromachining process--the etching selectivity of p-doped (p-Si) versus n-doped (n-Si) single-crystal silicon [34:221]. They reported research concerning the exploitation of anodic etching with hydrofluoric acid (HF) solutions to realize microstructures in single-crystal silicon (Figure II-11). The microstructures can be realized by ion implanting p-Si and n-Si regions in the substrate and etching with HF. HF etches the doped silicon when a voltage is applied, and there is a sufficient population of holes generated by illumination or by strong oxidants [34:222].

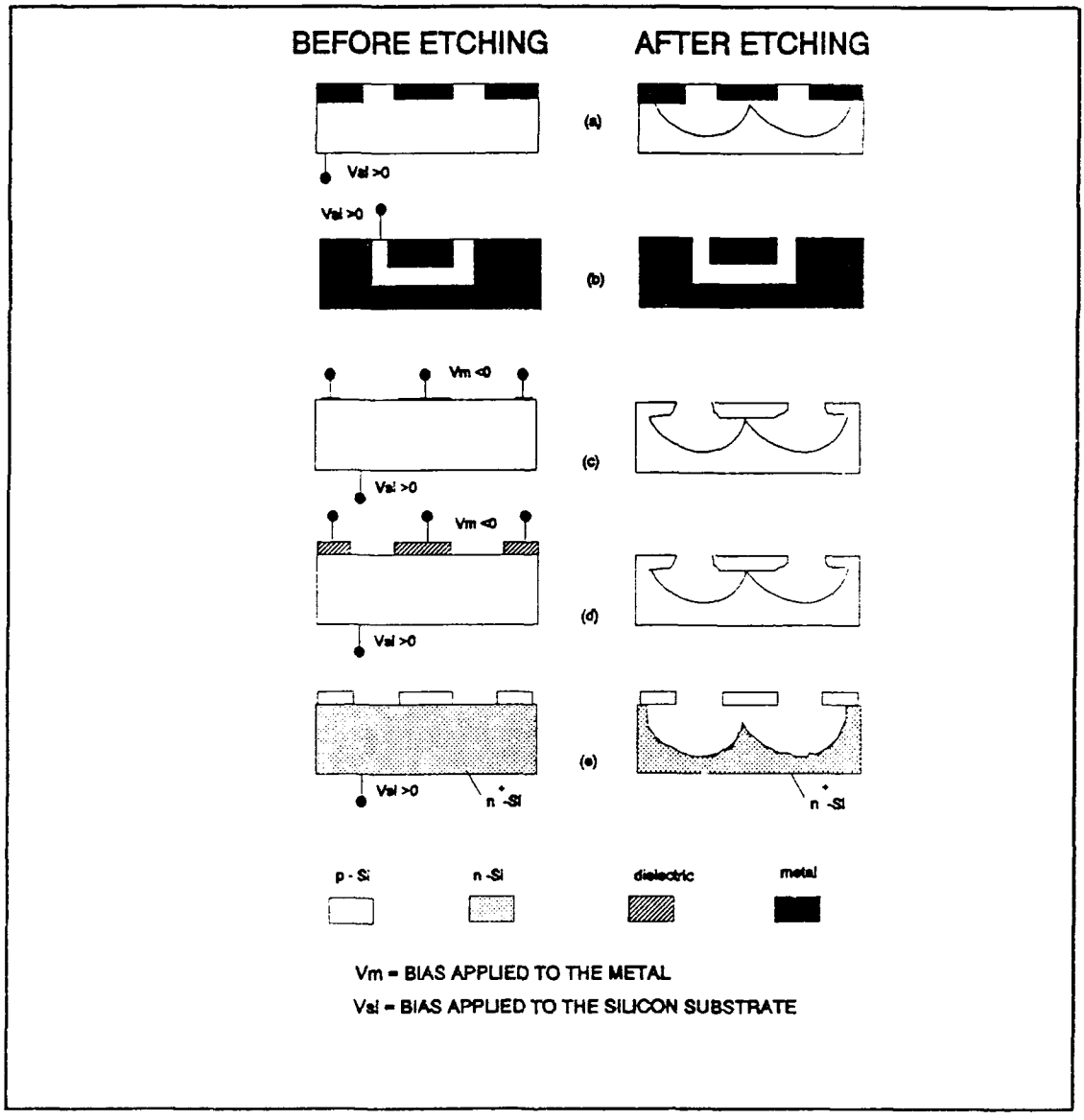


Figure II-11. Anodic Etching of Doped Silicon: (a) p-Si with Implanted n-Type Regions, (b) n-Doped Wafer with a Combination of Diffused and Implanted p-Type Regions, (c) Schottky Barrier Structure, where the Negative Potential Applied at the Metal Induces a Depletion Layer, which is not Etched, (d) MOS Structure, where the Positive Potential Applied to the MOS Electrode Induces an Inversion Layer, which is not Etched, and (e) n^+-Doped Wafer with a p-Doped Epitaxial Layer [34:222].

Micromachining may have unlimited applications in many areas of science. Dr. George A. Hazelrigg, of the National Science Foundation, presented the state-of-the-art research in micromachining on April 23, 1991 to the Air Force Institute of Technology. Dr. Hazelrigg demonstrated how micromachining techniques were used to fabricate gears, electrostatic rotating motors, sensors, pneumatic turbines, and linkages on a scale of 100 microns from the research at AT&T Bell Labs and the University of California at Berkeley [35]. This research was an example of the broad range of applications for micromachining, but it is a new field of science and several technical problems must be solved. Friction between the microelectromechanical device's moving parts remains a significant problem [35]. An adequate lubricant or the ability to micromachine bearings will be necessary to allow these devices to operate sufficiently long for practical applications.

2.2.1 Silicon Micromachining Applied to Thermal Dissipation.

The silicon micromachining effort in this thesis represents follow-on work to the two previous theses accomplished at AFIT by Capt Carver and Capt Uyehata. Whereas they applied silicon micromachining technology to efforts focused on suppressing light reflectivity and

enhancing absorption, this thesis extends the silicon micromachining technology to an application in thermal management in wafer scale integrated circuitry.

Many of the definitions and relationships of silicon micromachining applied to thermal dissipation are derived by Richard J. Phillips in Advances in Thermal Modeling, Chapter 3: Microchannel Heat Sinks [36:109-179]. Definitions and relationships are also provided in Appendix B.

Phillips credits Tuckerman and Pease, researchers at Stanford University, with the genesis of micromachining applied to thermal management [36:109-110]. In the early 1980's, Tuckerman and Pease showed that heat sinks for ICs could be realized with standard microelectronic fabrication techniques [36:110; 37]. In 1981, they fabricated long (several hundred microns), thin (approximately 50 microns by 50 microns) microchannels which dissipated as much as 790 W/cm^2 of heat [36:112]. The microchannels were realized with anisotropic wet chemical etching techniques [36:112]. In their follow-on research concerning microchannels, Tuckerman and Pease attained heat "dissipation in excess of 1300 W/cm^2" [36:112; 37; 38; 39].

Table II-3 compares the relative magnitudes of several heat transfer modes, and it emphasizes the importance of liquid cooling. Phillips provided the contents of

Table II-3 to emphasize the importance of the research concerning microchannels applied to thermal dissipation.

In 1984, Goldberg published the results of his research concerning microchannel heat sinks [36:113; 40]. He analyzed the laminar-flow in 0.635 cm-long microchannels relative to their thermal and fluid performance [36:113; 40]. The microchannels were realized in copper, and widths of 127, 254, and 635 microns were analyzed [36:113; 40]. The copper microchannel heat sinks dissipated heat with a "thermal resistance as low as 3.4 °C/W" from sixteen IC die [36:113].

Table II-3: Typical Range of Values for Convective Heat-Transfer Coefficients (h) Relative to Several Modes [36:111].

MODE	h (W/m^2-°C)
FREE CONVECTION, AIR	5-25
FORCED CONVECTION, AIR	10-500
FORCED CONVECTION, WATER	100-15,000
POOL BOILING, WATER	2,000-35,000
FLOW BOILING, WATER	5,000-100,000

In 1985, Mahalingam obtained experimental results from "air-cooled and water-cooled silicon heat sinks" [36:114; 41]. Thermal resistances as low as 0.02 °C/W and 0.7 °C/W

were realized in 5.0 cm-long microchannels using water cooling and air cooling, respectively [36:114; 41]. The microchannel width studied was 200 microns, the depth was 170 microns, and the separation between the microchannels was 100 microns [36:114; 41].

In 1986, Kishimoto and Ohsaki designed and experimentally analyzed a "water-cooled, multilayered alumina substrate" hosting 25 VLSI chips [36:115; 42]. The VLSI chips were epoxied to the substrate which harbored 8.3 cm-long x 800 micron x 400 micron microchannels and provided a "worst case thermal resistance of 3.3 °C/W under a 2.84 psi pressure drop" [36:116; 42]. Stacking several of the substrates vertically, each with 25 VLSI chips, psovided a 17 kW/liter heat dissipation capacity [36:116; 42].

Phillips also experimentally investigated 0.072 microchannel heat sinks. He obtained heat dissipation values higher than 1,000 W/cm^2 with thermal resistances as low as °C/W using 0.97 cm-long x 220 micron x 165 micron microchannels to cool a four-chiq array of heat producing resistors in 1987 [36:118].

For this thesis effort, the primary application for silicon micromachining is thermal management--to provide a partial solution to the heat dissipation problem in integrated circuitry by inwestigating the effects due to various micromachined surfaces. These effects may then be

optimized in follow-on research, and ultimately developed into IC fabrication steps as a thermal management tool.

III. *Design and Fabrication*

This chapter describes the design and fabrication of the single-crystal silicon wafer thermal modules and the test equipment configurations used to measure their thermal dissipation characteristics. It also details the preparation and silicon wafer processing procedures accomplished to realize the randomly spaced and sized pyramids, deep vertical-wall grooves, and micro-fluid channels that will be evaluated for their ability to enhance heat dissipation from the thermal modules.

The wafer preparation, photolithography, silicon micromachining, and thermal module fabrication were accomplished at the AFIT Microelectronics Laboratory located in Building 125, room 1065, and at the Armstrong Laboratory's Toxic Hazards Division located in Building 79. The diffused resistors were designed using the Magic software tool on the SUN workstations in the AFIT VLSI Laboratory located in Building 640, room 241, and they were fabricated by MOSIS (Metal-Oxide-Semiconductor Implementation System) (Marina del Rey, CA).

The discussion begins with the photomask design and fabrication. Then, the wafer preparation is documented. The silicon micromachining processes used to realize the three heat-dissipating microstructures are detailed in three

separate sections. The diffused resistor design, along with the thin-film aluminum resistor design and fabrication, are also presented. Next, the single-crystal silicon wafer thermal module construction is discussed. Finally, the test equipment configuration design is presented.

3.1 Silicon Wafer Thermal Module Design

As discussed in the first chapter, several configurations of silicon wafer thermal modules were required to provide comparative heat transfer data. Their design was influenced by the resources available within AFIT. Two of these resources were the metallization deposition equipment located in the AFIT Microelectronics Laboratory and access to the services of MOSIS. Since an integrated circuit die-sized heat-generating device was essential for this thermal analysis study, these resources were used to provide two comparative devices for the experiments; the aluminum thin-film resistor and the IC die diffused resistor. It also provided redundancy in case one of the designs failed to perform as intended.

In order to simulate wafer scale integration techniques, the silicon wafer thermal modules were designed to host the heat producing devices. The IC die diffused resistor and the evaporated aluminum thin-film resistor host wafers were designed to be epoxied to the silicon wafers

containing the three comparative heat-dissipating micromachined structures. The heat dissipating structure configurations were adapted from the current research in silicon micromachining. Separate host wafers for the structures and the devices were required to ensure successful module construction throughout the design and fabrication processes. Initially, a single host silicon wafer design was considered where the heat dissipating micromachined structures would be realized on one side of a wafer, and the heat producing devices would reside on the other side. However, it was subsequently decided that the processing sequence for the single wafer design was too risky. The single wafer design would also require silicon wafers that are polished on both sides; the cost of these wafers also motivated the alternative epoxied wafer design.

This research project had several design determining objectives:

1) Compare the heat dissipation from several textured silicon micromachined surfaces.

2) Simulate wafer scale integration heat loads with IC die-sized heat-generating devices.

3) Configure the comparative experiments as consistent as possible.

4) Compare the heat dissipation from two different heat-generating devices--the IC die diffused resistor and

the aluminum thin-film resistor.

5) Maintain simple monolithic silicon fabrication processes.

3.2 *Photomask Design and Fabrication*

Several photomasks were designed and fabricated to realize the silicon micromachined surfaces, IC die recess holes, epoxy-relief holes, aluminum-film resistors, and the aluminum conductors used to wire-bond the IC die to the host wafers.

3.2.1 Photomask Design. Several photomasks were designed for a 50x photoreduction, while others were designed for a 20x photoreduction. The scale of reduction was determined from the dimensions of the required image transfer process, and it was also influenced by the field of exposure limitation (40 x 40 inches) of the photoreduction camera system. The exposure settings for both reductions are listed in Table III-1.

The IC die recess hole and the epoxy-relief hole photomasks were designed first. They were originally designed to accommodate the smallest production IC die available from
MOSIS. The IC die were expected to be 2,000 x 2,000 microns. Correspondingly, the photomask images for the

Table III-1. Photoreduction Camera System Settings.

Component	50x Reduction	20x Reduction
Lens	35 mm Wray	2 inch Wray
Front box setting	32.4541	6.86
Rear box setting	51.7	27.0
F-stop	F4	
Exposure time	10 minutes	10 minutes
Plate	4-inch HRP	4-inch HRP

recess holes were designed as 1,800 x 1,800 squares, and the images for the epoxy-relief holes were designed as 600 x 600 micron squares. The 1,800 x 1,800 micron squares were originally intended to be used with an isotropic etch. Since the host silicon wafers were to be etched to realize the square holes with a depth of 250 microns (approximately halfway into the wafer), the lateral dimensions of the square holes would also increase by 250 microns. The square holes would then be 2,300 x 2,300 microns. They would then accommodate the 2,000 x 2,000 micron IC die and have a 150 micron moat for the excess epoxy.

The IC die recess hole photomasks were redesigned and fabricated to accommodate the actual IC die fabricated by MOSIS. The actual dimensions of the IC die ranged from approximately 2,400 x 2,400 microns square to 2,650 x 2,650 microns square. The IC die dimensions were verified on the coordinatograph table (Mutoh Industries, Model PR12-12LT, Tokyo, Japan) using a magnifying lens with crosshairs in the rubylith cutting jig. Also, the IC die were not cut exactly

square. Consequently, a 2,700 x 2,700 micron square mask was fabricated to realize a sufficiently large recess hole. Fortunately, the original masks intended for this purpose were found to be useful to serve as the pattern for the epoxy relief holes. The resulting 2,700 x 2,700 micron squares were intended to be used with an anisotropic etch. The lateral dimensions were experimentally determined to grow approximately 90 microns as the holes in the host silicon wafer were etched completely through.

A photomask with a single, centered 2,700 x 2,700 micron square hole was designed, and a second photomask with four, centered, 2,700 x 2,700 micron square holes was designed to facilitate the two heat producing IC die configurations (Figure III-1). The dimensions of the configuration for the four, centered, IC die were designed to facilitate contact with the 0.013-inch diameter thermocouple probes (Physitemp, ICT-4, Clifton, NJ 07013). Thus, the four heat producing IC die were designed to be positioned equidistant relative to the center of the host silicon wafer, and the IC die centers were 11,074.4 microns apart. The IC die spacing was determined to provide sufficient area for the excess epoxy, conducting lines, and thermocouple contacts. The epoxy-relief holes were designed to be centered relative to each of the IC die recess holes.

Photomasks were also designed to realize thin-film aluminum conductors (Figure III-2). The purpose of these conductors was to facilitate external electrical power connections to the IC die. To facilitate the aluminum conductor design, a 1,000 micron wide perimeter of aluminum was configured to surround the single, centered, IC die to facilitate wire-bonding from any of the eight diffused resistors on the IC die.

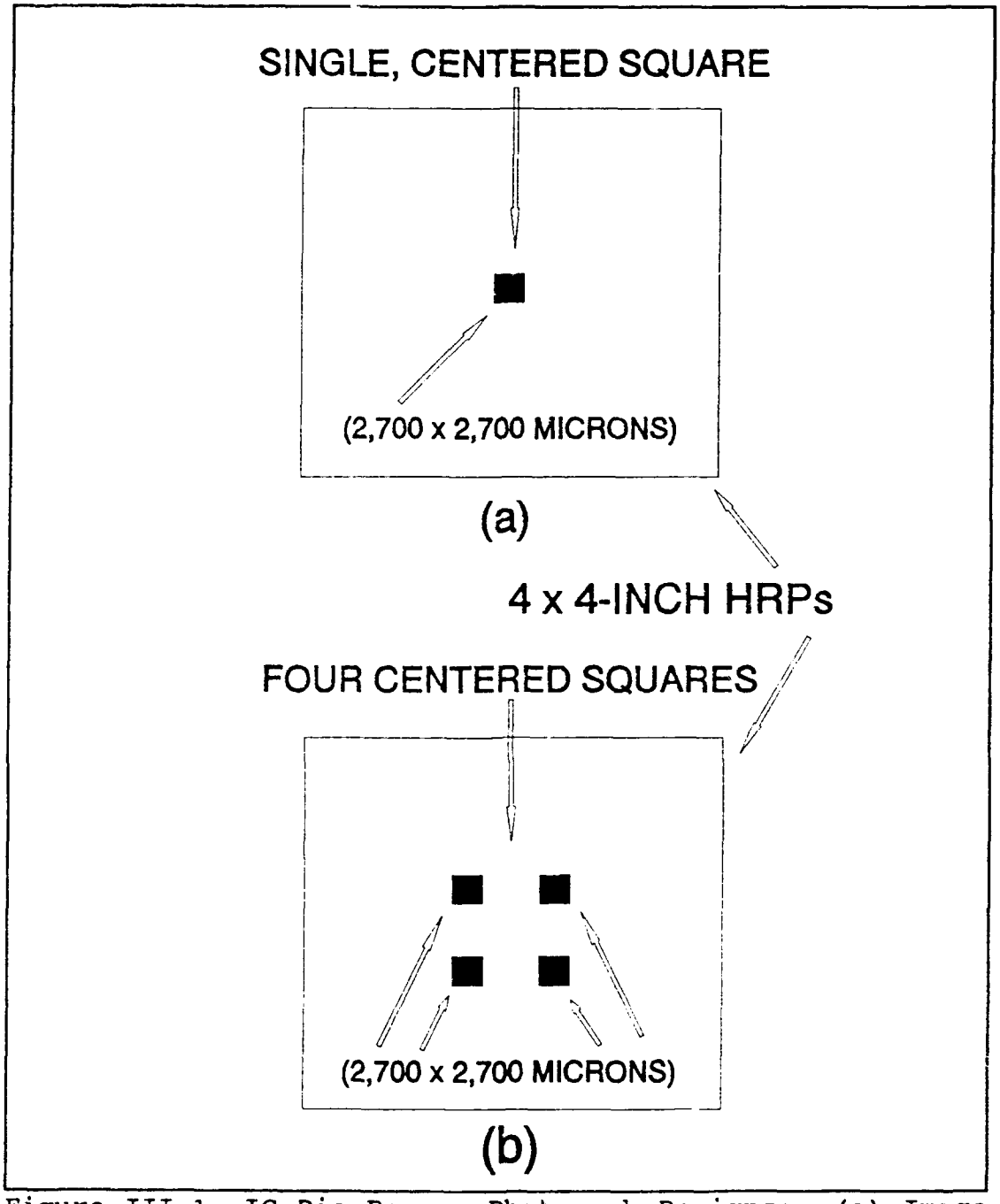


Figure III-1. IC Die Recess Photomask Designs: (a) Image for One IC Die and, (b) Image for Four IC Die.

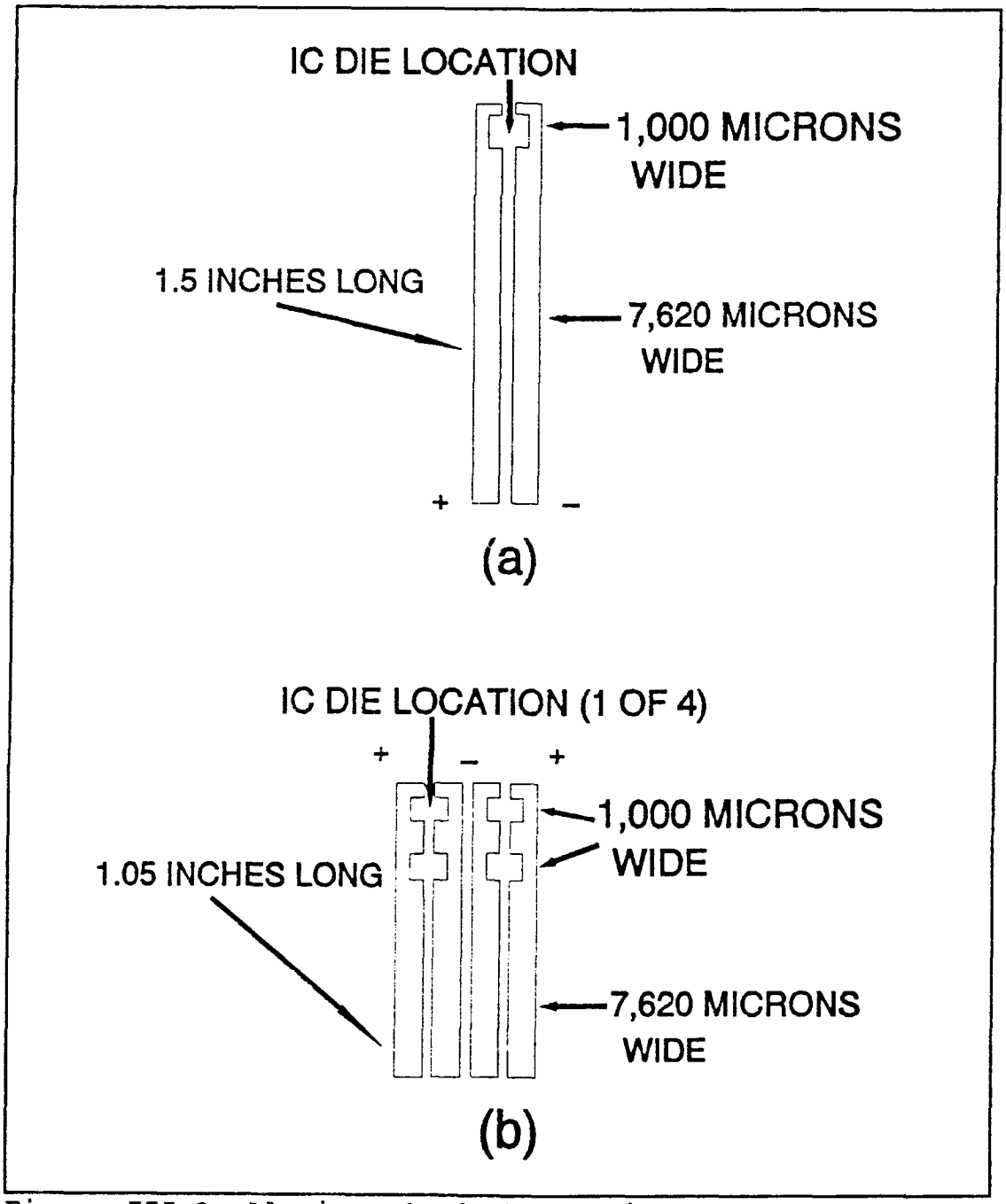


Figure III-2. Aluminum Conductor Designs: (a) For One IC Die and, (b) For Four IC Die.

A 500 micron separation between the aluminum conductors at the top and bottom of the design was incorporated to divide the conductor into two conductors so that an externally applied bias could be applied to the resistors. The image included 1.25-inch long conductor leads to facilitate electrical connections near the edge of the silicon wafer. These leads were designed to be 7,620 microns wide to minimize the voltage drop between the wire-bond and the edge of the wafer. To facilitate wire-bonding, the conductor was designed to be at least 5,000 angstroms thick. Using the resistivity for annealed aluminum ($\rho = 28.28 \times 10^{-9}$ ohm·meter), and $R = (\rho \cdot L)/(W \cdot t)$, a resistance, R, of approximately 0.15 ohms should be realized in each leg of the conductor [25:426]. The length, L, was 0.03175 meters, the width, W, was 7,620 microns, and the estimated thickness, t, was 8,000 angstroms [1]. A photomask was similarly designed for the configuration of the four, centered, IC die. The width of the aluminum conductor surrounding the IC die was similarly designed to be 1,000 microns, but the conductor leads were slightly shorter (1.05 inches). For the thin-film aluminum resistor photomask, a serpentine pattern was designed (Figure III-3). The pattern was designed with a sufficient cross-sectional area to facilitate contacting the silicon wafer with the 0.013-inch diameter thermocouple probe. A 20-micron width was

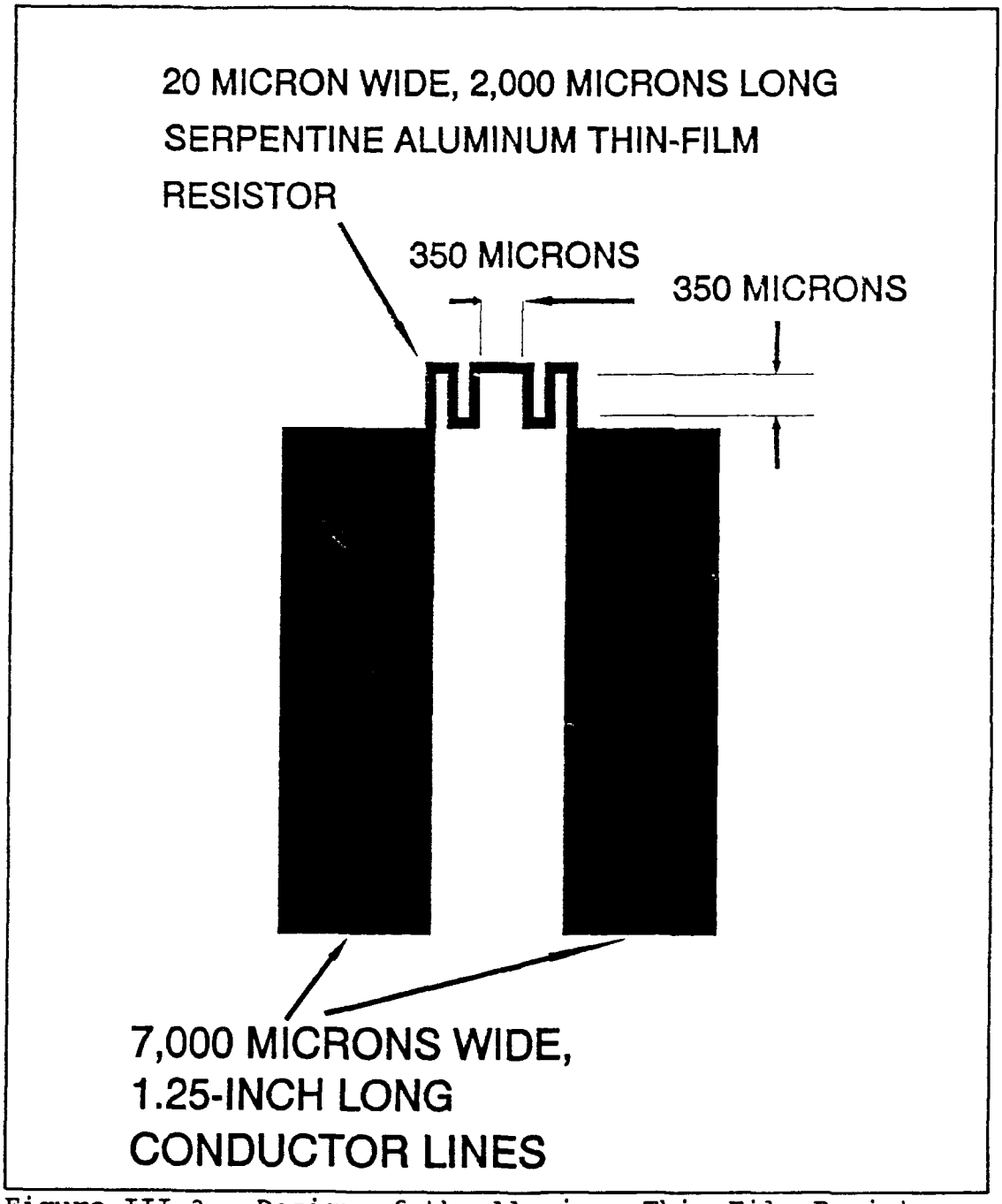


Figure III-3. Design of the Aluminum Thin-Film Resistor.

estimated to realize an adequate IR thermal image, and it also was deemed favorable for realizing a successful yield throughoutthe photolithography and metal lift-off fabrication processes. With a length, L, of 2,000 microns, a width, W, of 20 microns, an expected resistivity, ρ, of 28.28×10^{-9} ohm•meter, and a desired resistance, R, of approximately 33 ohms (to match the MOSIS IC die), a thickness, t, was calculated using the relationship, $R = (\rho \cdot L)/(W \cdot t)$ [25:426]. The thickness, approximately 860 angstroms, was used as an initial design parameter. Several lift-off processes were performed to iteratively determine the actual resistivity of the aluminum. The actual value was then used to estimate the required aluminum thickness.

A photomask was also designed for the micro-fluid channel feed-throughs (Figure III-4). The feed-throughs were designed as 0.0375-inch circles centered 2.25 inches apart, equidistant relative to the center of a host silicon wafer. The 2.25-inch separation facilitated access to the micro-fluid channel host wafers. It was also estimated to be sufficiently far from the edge of the silicon wafer to ensure successful thermal module fabrication. The 0.0375-inch diameter holes were determined to be sufficiently large to facilitate insertion of the 0.8 mm outside diameter (OD) micro-tubing (Valco Instruments Co., Inc., Houston,

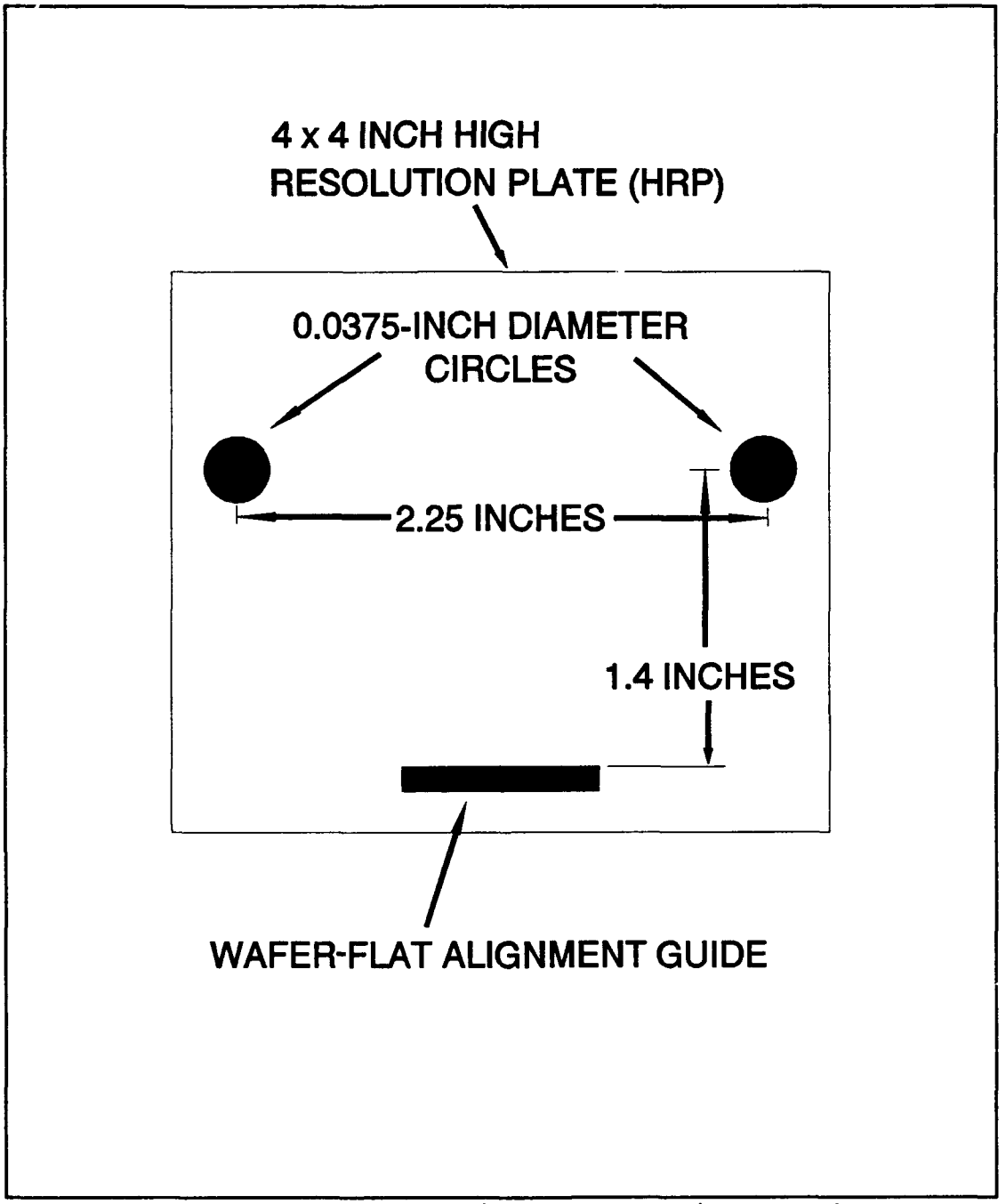


Figure III-4. Photomask Design for the Micro-Fluid Channel Feed-Throughs.

TX 77255). To realize the 0.0375-inch diameter holes, a 0.75-inch circle found on a conventional circle template was utilized (compensating for the 20x photoreduction). In the anisotropic (KOH) etch, squares encompassing the 0.0375 diameter circles would be realized as the etch process proceeded towards the (100) planes [13].

The micro-fluid channel photomask was designed to align with the feed-throughs (Figure III-5). The inlet/outlet accesses, which were aligned with the feed-throughs, were designed as 0.0375 x 0.0375 inch squares. A 0.0250-inch wide canal was designed to connect each access with the micro-fluid channels. The micro-fluid channels were designed to encompass an area slightly larger than the "footprint" of the four, centered, IC die configuration. Thus, the micro-fluid channel network was designed to be 15,240 microns long and 15,875 microns wide. To maintain dimensions in the micron range to within an order of magnitude of the feature sizes discussed in recent research, the micro-fluid channel images were designed to be 100 microns wide [18; 20; 36; 40]. For consistency the channels were also spaced 100 microns apart on the photomask. The photomask contained 76 micro-fluid channels. The depths of the channels were experimentally determined via several iterative etch processes.

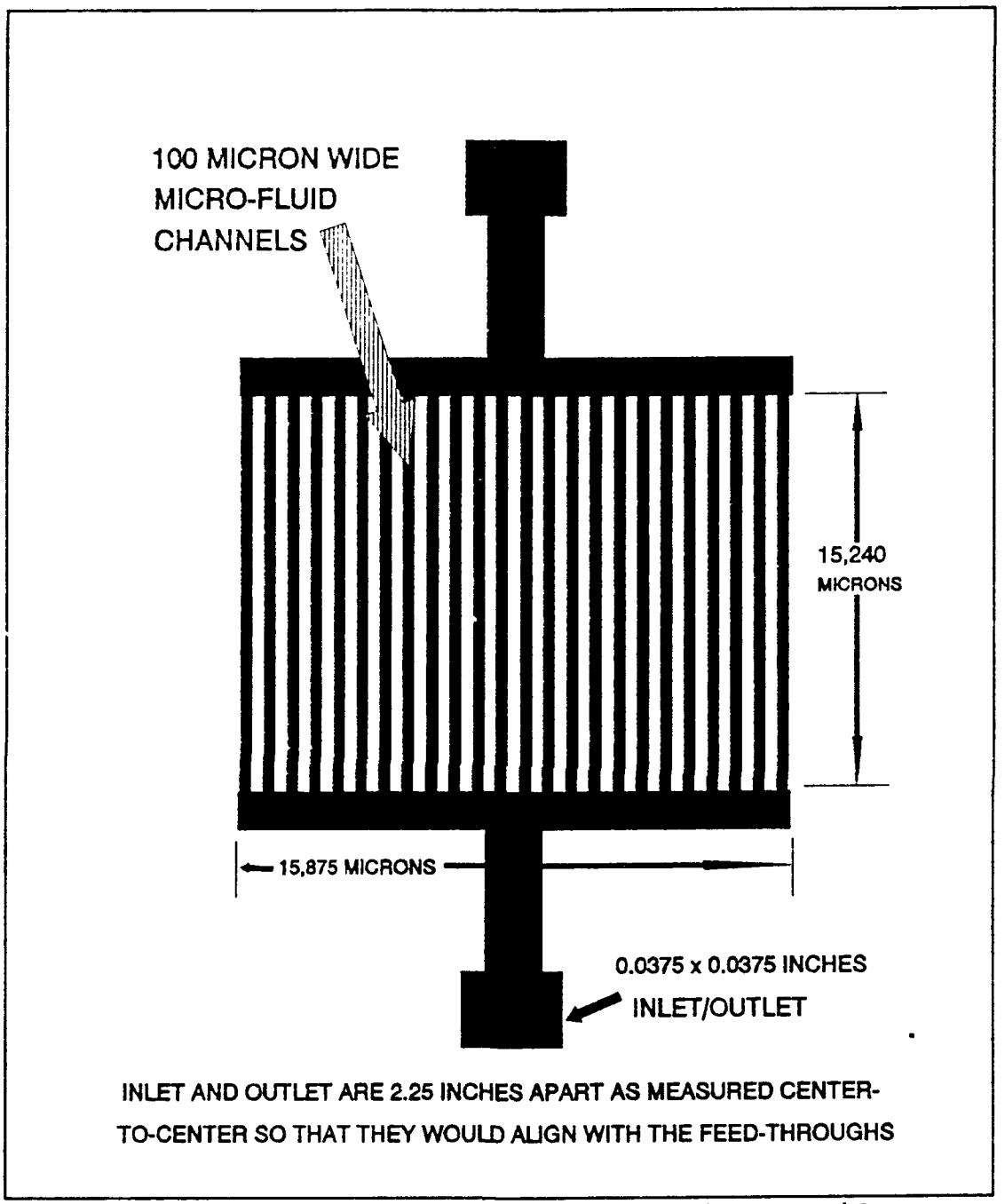


Figure III-5. Photomask Design for the Micro-Fluid Channels.

3.2.2 Photomask Fabrication. The photomasks for the Deep Vertical-Wall Groove (DVWG) structure were designed and fabricated by Capt Uyehata [4]. The remaining photomasks were designed and fabricated using the following procedure:

1) Geometries of the images for the IC die recess holes, epoxy-relief holes, micro-fluid channels, and the evaporated aluminum patterns were determined as discussed in the previous section.

2) 40 x 40 inch squares of Rubylith were secured to the coordinatograph table using masking tape, and the master images were cut into the Rubylith.

3) The Rubylith was then peeled away from the clear backing material to reveal the positive image of the artwork.

4) Each 40 x 40 inch square of Rubylith was secured to the 40 x 40 inch photoreduction screen.

5) The reduced images were captured on 4 x 4 inch high resolution plates (HRPs) (Kodak, Cat 1252303, Rochester, NY 14650) using the photoreduction camera system.

3.2.3 *Photomask Development.* The development of the HRPs was conducted under darkroom illumination conditions (a single, red fluorescent safe-light source) using the following process:

1) The HRPs were placed in a plastic holder and immersed in the Kodak developer solution (1:4, developer:DIW) for 4 minutes.

2) The HRPs were then immersed in a stop bath (16:1,000, stop:DIW) for one minute.

3) The HRPs were then immersed in a fixer bath (4:1, fixer:DIW) for one minute.

4) The HRPs were then rinsed in DIW and dried with N_2 [12].

Reverse images of the metal lines and thin-film resistor photomasks were required. The reverse photomasks were realized using the photomask duplicator (Ultratech, Model Unk, Sunnyvale, CA 94086). The exposure time in the photomask duplicator was experimentally optimized at 8.5 seconds. The duplicates were developed using the identical process implemented to develop the master HRPs. The HRPs were then stored in their original shipping container for subsequent use with the photomask aligner.

The following photomasks were required and fabricated for this thesis:

1) One 1,800 x 1,800 micron square for recessing a single IC die in the host silicon wafer.

2) Four, centered, 1,800 x 1,800 micron squares for recessing four IC die in a host silicon wafer.

3) One 600 x 600 micron square for allowing excess epoxy to flow through it to the backside of the host silicon wafer.

4) Four, centered, 600 x 600 micron squares for allowing excess epoxy to flow through them to the backside of the host silicon wafer.

5) One set of metal lines for wire-bonding a single IC die to the conductors on the silicon host wafer.

6) The reverse image of 5) for exposing the positive photoresist to pattern the aluminum conductors.

7) One set of metal lines for the four IC die for wire-bonding them to the conductors on the host silicon wafer.

8) The reverse image of 7) for exposing the positive photoresist to pattern the aluminum conductors.

9) Metal lines to, and including, a single, thin-film resistor.

10) The reverse image of 9) for exposing the positive photoresist to pattern the aluminum conductors.

11) One 2,700 x 2,700 micron square for recessing a single IC die.

12) Four, centered, 2,700 x 2,700 micron squares for recessing the four IC die.

13) Micro-fluid channel pattern for realizing the liquid cooling technique.

14) Feed-throughs for access through the silicon wafer to the micro-fluid channel.

3.3 *Silicon Wafer Preparation*

Three-inch diameter, (100)-oriented, single-crystal silicon wafers were obtained from Ziti, Inc. (Monterey, CA 93940). The (100)-oriented wafers were n-type (doped with phosphorus) with resistivities spanning 0.005 ohm·cm to 0.020 ohm·cm, and they ranged in thickness from 510 microns to 530 microns. The (100)-oriented wafers were polished on one surface only.

One carousel of 25, (110)-oriented, 3-inch diameter, single-crystal silicon wafers was obtained from Virginia Semiconductor (Fredericksburg, VA 22401). These wafers were polished on both surfaces, and their thicknesses spanned 290 microns to 305 microns, and they were p-type (doped with boron), with resistivities ranging from 1 ohm·cm to 3 ohm·cm.

3.3.1 *Randomly Spaced and Sized Pyramids.* Twenty-four, (100)-oriented silicon wafers were prepared for silicon micromachining to realize randomly spaced and sized pyramids. The silicon wafers were labeled P-1 to P-24 with a hand-held diamond scribe to facilitate their identification. They were then cleaned using the standard

cleaning procedure described in Appendix C. This standard cleaning procedure was used repeatedly, and it is referred to throughout this document.

The silicon wafers were then oxidized using the silicon dioxide (SiO_2) growth schedule described in Appendix D. A specific SiO_2 thickness was required to protect the backside of the wafers from the anisotropic etch process implemented in the hydrazine hydrate (HH) and anhydrous hydrazine (AH) solutions (Pfaltz & Bauer, Waterbury, CT 06708 and Spectrum Chemical Mfg. Corp., Gardenia, CA 90248-9985, respectively). HH was a hydrazine solution that was composed of 85% hydrazine and 15% water. AH was a hydrazine solution greater than 99% hydrazine. A 1 micron SiO_2 thickness was determined to be sufficiently thick to protect the backside of the wafers from the hydrazine etchants [4]. To achieve this SiO_2 thickness, the wafers were oxidized for 100 minutes.

Next, negative photoresist was applied to the silicon wafers according to the process described in Appendix F.

The wafers were then immersed in a 4:1, NH_4F:HF solution to remove the oxide from their frontside surface [12]. They were then rinsed in DIW, placed in the oxygen plasma asher (SPI Supplies, Plasma Prep II, West Chester, PA 19380) to remove the photoresist. Next, they were then immersed in a 100% solution of H_2SO_4 at 100 °C for 30 minutes

to remove the remaining photoresist and organic contaminants. Following this processing step, the wafers were then immersed in an N_2 bubbler in DIW until a 10 megohm resistance standard was achieved which indicated that the residual contaminants were removed. The silicon wafers were then blown dry with N_2. The silicon wafers were then stored in their original shipping container until they were anisotropically etched in the hydrazine solutions (HH and AH) to realize the randomly spaced and sized pyramids on their frontside surface.

3.3.2 *Deep Vertical-Wall Grooves.* Twenty-five, (110)-oriented silicon wafers were prepared for silicon micromachining to realize the deep vertical-wall groove structures. The silicon wafers were labeled V-1 to V-25 with a hand-held diamond scribe to facilitate their identification. They were then cleaned using the standard cleaning procedure described in Appendix C.

The silicon wafers were then oxidized using the silicon dioxide (SiO_2) growth schedule described in Appendix E. The wafers were oxidized for 110 hours.

Next, negative photoresist was applied to the backside of the silicon wafers according to the procedure outlined in Appendix F. The negative photoresist was similarly applied to the frontside of the wafers. The frontside of the wafers

was exposed to an ultraviolet light source through the deep vertical-wall groove (DVWG) photomask in the mask aligner for 15-45 seconds. The DVWG patterns were realized on the wafers by developing the exposed negative photoresist using the procedure described in Appendix G. They were then immersed in a 4:1, NH_4F:HF etchant to remove the SiO_2 from the open windows in the photoresist, rinsed in DIW, and blown dry with N_2. The wafers were then stored in their original shipping container, until needed for the anisotropic potassium hydroxide (KOH) etch process to realize the DVWG structures on the silicon wafer's frontsides.

3.3.3 *Micro-Fluid Channels.* Twenty-five, (100)-oriented silicon wafers were prepared for silicon micromachining to realize the micro-fluid channel structures. The silicon wafers were labeled F-1 to F-25 with a hand-held diamond scribe to facilitate their identification. They were then cleaned using the standard cleaning procedure described in Appendix C. The silicon wafers were then oxidized using the silicon dioxide (SiO_2) growth schedule discussed in Appendix D. The wafers were oxidized for 800 minutes. Approximately 2 microns of SiO_2 was realized.

Next, negative photoresist was applied to the silicon wafer's backsides, and then, to their frontsides, according to the procedure described in Appendix F. The backsides of the wafers was exposed to an ultraviolet light source through the feed-through holes photomask. After the feed-through holes were realized, the wafers were subsequently processed to prepare them for realizing the micro-fluid channel structures on the frontsides of the silicon wafers. This facet was accomplished by cleaning and oxidizing the wafers and applying photoresist to the backside and frontside using the procedures described in Appendices C, D, and F. The frontside of the wafers was exposed through the micro-fluid channel photomask in the mask aligner for 30-45 seconds. The feed-through holes and the micro-fluid channel patterns were realized on the wafers by developing the exposed photoresist according to the procedure described in Appendix G.

Finally, the wafers were immersed in a 4:1, NH_4F:HF etchant to remove the SiO_2 from the open windows in the photoresist. They were then rinsed in DIW and blown dry with N_2. The silicon wafers were then stored in their original shipping container until they were anisotropically etched in KOH to realize the feed-through holes and the micro-fluid channels on their frontside.

3.3.4 *Reference Wafer.* Three, (100)-oriented silicon wafers were prepared as reference (untextured) samples for comparing their performance with the micromachined (textured) wafers. They were not processed for the purpose of photolithography, but they were cleaned using the process described in Appendix C.

The silicon wafers were then transferred to their original shipping container until they were epoxied to the IC die host wafers and the thin-film aluminum resistor host wafers.

3.3.5 IC *Die Host Wafers.* Twenty-five, (100)-oriented silicon wafers were prepared for silicon micromachining to realize IC die recess and epoxy-relief holes. The silicon wafers were labeled D-1 to D-25 with a hand-held diamond scribe to facilitate their identification. They were then cleaned using the standard cleaning procedure described in Appendix C. The silicon wafers were then oxidized using the SiO_2 growth schedule described in Appendix D. The wafers were oxidized for 800 minutes. Approximately 2 microns of SiO_2 was realized.

Next, negative photoresist was applied to the backside of the silicon wafers according to Appendix F. The negative photoresist was similarly applied to the frontside of the silicon wafers. The frontside of the wafers was exposed to

an ultraviolet light source through the IC die recess hole photomask in the mask aligner for 60 seconds. The IC die recess hole patterns were realized on the silicon wafers by developing the exposed photoresist using the procedure described in Appendix G.

The silicon wafers were immersed in a 4:1, NH_4F:HF etchant to remove the SiO_2 from the openings in the photoresist. They were rinsed in DIW and blown dry with N_2.

The wafers were then anisotropically etched in a KOH and DIW solution (20% KOH:80% DIW, by weight) at 50 °C to realize the IC die recess holes [13]. In order to maintain a constant temperature (and an accelerated etch rate), the wafers were immersed in the KOH solution which was prepared in a teflon beaker. The teflon beaker was then immersed in the constant temperature bath (Lufran Superbowl, model SB, Macedonia, OH 44056). The IC die recess holes were anisotropically etched to a depth of 190-210 microns relative to the wafer's frontside. The IC die recess hole depths were measured and recorded after the wafers were immersed in a 100% H_2SO_4 solution, stripped of their native oxide with a 4:1, NH_4F:HF etchant, rinsed in DIW, and dried with N_2.

The wafers were then similarly re-processed to realize the epoxy-relief holes which were anisotropically etched completely through the wafers relative to the center of the

IC die recess holes using the same KOH:DIW (20% KOH by weight) solution at 50 °C. This facet was accomplished by cleaning and oxidizing the wafers and applying the photoresist to their backsides and frontsides using the procedures described in Appendices C, D, F, and G.

The wafers were then re-processed to realize aluminum thin-films which were intended to be used as conductors to the IC die. The aluminum was used to apply an external bias to the diffused resistors on the IC die. The wafers were prepared for metallization using the following procedure:

1) The wafers were baked at 200 °C for 2 hours to desiccate their surface.

2) Hexamethyldisilazane (HMDS) was liberally applied with a dropper to their frontside to promote photoresist adhesion, and the silicon wafers were then spun at 4,000 rpm for 30 seconds.

3) Positive photoresist (Shipley, product S1350J, Newton, MA 02162) was applied with a dropper to their frontside, and they were then spun at 5,000 rpm for 30 seconds.

4) The wafers were pre-baked at 65 - 75 °C for 20 minutes.

5) The wafers were then exposed in the mask aligner for 70 seconds through a reverse image of the metal conductor photomask.

6) The wafers were immersed in chlorobenzene for 2 - 3 minutes to swell the photoresist and correspondingly enhance the metal lift-off process.

7) The wafers were softbaked at 90 °C for 15 minutes.

8) The wafers were developed in a 3:1, DIW:KTI 351 developer solution for 1 minute.

9) The wafers were rinsed in DIW and blown dry with N_2.

10) The wafers were then hardbaked at 90 °C for 15 minutes [1; 12].

The silicon wafers were then transferred to the vacuum deposition system (Denton Vacuum Corporation, model DV602, Cherry Hill, NJ 08003). A thin film of aluminum (approximately 7,000 angstroms thick) was deposited on the wafer's frontside [12]. A maximum of four wafers could be accommodated in the vacuum chamber during each deposition cycle. The wafers were then removed and placed in petri dishes filled with acetone. The acetone dissolved the photoresist which was not exposed to the ultraviolet light, and thus, it also removed the subsequent overlying aluminum layer, leaving the desired metal pattern. Vigorous physical agitation was necessary to remove all of the unwanted photoresist and the aluminum. The film thicknesses were verified with the Dektak stylus profilometer (Sloan Technology Corp., model Dektak IIA, Santa Barbara, CA 93109). Conductive (copper) adhesive tape was placed over

the aluminum metal lines to protect them where repeated physical contacts were to be subsequently made.

Finally, the wafers were placed in their original shipping containers until the IC die were to be epoxied to their frontside and wire-bonded. In practice however, the IC die were ultimately wire-bonded to the copper adhesive tape. Mr. Larry Callahan, Electronics Laboratory, Wright Laboratories, Aeronautical Systems Division, Wright-Patterson AFB, OH performed the wire-bonding task in Building 620 using 0.002-inch diameter aluminum wire. Mr. Callahan opted to wire-bond to the copper adhesive tape instead of wire-bonding to the thin films of aluminum. He realized higher yields when wire-bonding to the copper adhesive tape.

3.3.6 *Aluminum Thin-film Resistor Host Wafers.* Ten, (100)-oriented silicon wafers were prepared to realize aluminum thin-film resistors (by evaporating aluminum). The silicon wafers were labeled M-1 to M-10 with a hand-held diamond scribe to facilitate their identification. They were then cleaned using the standard cleaning procedure described in Appendix C. The silicon wafers were then oxidized using the SiO_2 growth schedule discussed in Appendix D. The wafers were oxidized for 120 minutes to realize a SiO_2 thickness greater than 1 micron.

Next, negative photoresist was applied to the frontside of the silicon wafers according to Appendix F. Then, the SiO_2 on the backside of the wafers was removed by immersing them in a 4:1, NH_4F:HF etchant for 7 minutes to reduce the thermal resistance of the silicon wafer thermal module. The wafers were then placed in the oxygen plasma asher to remove the photoresist from their frontsides. They were further cleansed in acetone and dried with N_2.

Next, the wafers were individually placed on the photoresist spinner, and HMDS was liberally applied to the frontside of the wafers. They were spun at 4,000 rpm for 30 seconds. HMDS was used to promote the adhesion of the positive photoresist [12]. Shipley S1350J positive photoresist was then liberally applied to the frontside of the wafers, and they were spun at 5,000 rpm for 30 seconds. The silicon wafers were baked at 65 °C for 20 minutes to harden the photoresist's surface. When they cooled, the frontside of the wafers were exposed to an ultraviolet light source through the reverse image of the thin-film resistor photomask in the mask aligner for 70 seconds. The resistor patterns were realized on the wafers by developing the exposed photoresist using the following process:

1) The wafers were immersed in a 3:1, DIW:KTI 351 developer solution for 30-60 seconds.

2) The wafers were rinsed in DIW.

3) The wafers were dried with N_2.

The wafers were then hardbaked at 90 °C for 15 minutes. After cooling, they were transferred to their original shipping containers until they were needed in the aluminum evaporation process.

3.4 Silicon Micromachining

The randomly spaced and sized pyramids, DVWGs, and micro-fluid channels were realized using the silicon micromachining technology to provide comparative heat dissipating structures.

3.4.1 *Silicon Micromachining the Randomly Spaced and Sized Pyramids.* The randomly spaced and sized pyramids were realized on the frontside of wafers P-1 through P-24 using two different hydrazine (N_2H_4 or NH_2NH_2) etch solutions. The etch process for these structures was accomplished at the Toxic Hazards Division, Building 79, room 178 in a class III chemical hood.

Immediately prior to transporting the wafers and the necessary laboratory equipment to Building 79, the wafers were cleaned in a 100% H_2SO_4 solution for 20 minutes at 100 °C, rinsed in DIW, and blown dry with N_2.

In the chemical hood at Building 79, 500 ml of HH was added to 333 ml of DIW in a 1,500 ml beaker. The 333 ml of

DIW was sufficient to ensure that the solution would envelope the wafers after they were immersed. The resulting solution was 3:2, HH:DIW (or 425 ml of pure hydrazine and 408 ml of DIW). The solution was heated to 72 °C. This processing temperature was the upper limit advised by Ms Marilyn George, supervisor of biochemistry at the Toxic Hazards Division [80]. When the temperature of the etchant solution stabilized, wafers P-1 to P-13 were placed in a modified container which was fabricated by cutting a wafer shipping container in half and boring access holes into it to facilitate the inclusion of a handle. The modified container was required to facilitate immersing several wafers as a group into a 1,500 ml beaker. The 1,500 ml beaker volume was required to ensure that the wafers would be totally immersed in the etchant solution, since only 500 ml of each hydrazine solution was available.

The silicon wafers (P-1 to P-13) were immersed in a 4:1, DIW:HF solution for 90 seconds to remove the native oxide from the frontside of the silicon wafers. The silicon wafers were then immediately immersed in the hydrazine solution at 72 °C for 30 minutes, and they were agitated at one minute intervals. The wafers were then immersed in a beaker containing bleach, which neutralizes the residual hydrazine via an oxidation process [80]. Finally, wafers P-1 to P-13 were rinsed in DIW and placed in their original

shipping container.

Next, a 3:2, AH:DIW solution was heated to 62 °C in a 1,500 ml beaker to etch the second batch of wafers and provide a comparative result. The 62 °C temperature was the upper limit established by Ms George for the AH solution. Wafers P-14 to P-24 were immersed in the 4:1, DIW:HF solution for 90 seconds, and then they were immediately immersed in the 3:2, AH:DIW solution for 30 minutes and agitated at one minute intervals. The wafers were then immersed in bleach, rinsed in DIW, and placed in their original shipping container, until they were epoxied to the IC die mounted host wafers and thin-film resistor host wafers.

In previous thesis research, a former AFIT graduate student, Capt Uyehata, accomplished the etch process at 70 °C with a 3:2, HH (74%):DIW solution [4:4-31]. In Capt Uyehata's report, he stated that Baroana and Brandhorst used a 3:2 mixture of hydrazine and DIW at 110 °C to realize the pyramids, but they had the benefit of working in a (safer) nitrogen ambient environment [4:4-31]. At that concentration, 110 °C is near the boiling point of hydrazine.

After realizing the results of the hydrazine etch experiment, a second hydrazine etch experiment was performed. An arrangement was made to use the chemical hood

at the Toxic Hazards Division.

Four wafers from each of the two batches in the first experiment were etched a second time. The second hydrazine etch experiment similarly involved two different solution compositions for comparative purposes.

Prior to transporting the wafers and necessary equipment to Building 79, the wafers were cleaned using the procedure described in Appendix C. The wafers were then stored in their shipping container.

Under the chemical hood at Building 79, the two hydrazine solutions used in the first hydrazine etch experiment were mixed as a 1:1 solution in a 1,500 ml beaker. The resulting mixture was a 3:2, DIW:92% hydrazine solution. To slow the reaction of the hydrazine and obtain another comparative result, the solution was only heated to 50 °C.

Once the temperature of the solution stabilized, wafers P-1, P-2, P-16, and P-22 were immersed in the etch solution. P-1 and P-2 were two of the first batch of wafers etched in the previous hydrazine etch experiment; P-16 and P-22 were two of the second batch of wafers etched in the previous experiment.

The silicon wafers were immersed in a 100% solution of HF for 60 seconds, and then they were immediately immersed in the hydrazine solution for 15 minutes at 52 °C (the

temperature of the solution was consistently observed to increase by two degrees centigrade immediately after immersion). The wafers were agitated continuously for 15 minutes. Once removed from the hydrazine solution, they were immersed in bleach to neutralize the hydrazine, and then they were rinsed in DIW. They were then dried and transferred back to their shipping container.

Another solution was realized by diluting the previous solution with DIW. A 3:2, DIW:(3:2, DIW:92% hydrazine) solution was realized. That is, a 3:2, DIW:"previous solution" was mixed in the 1,500 ml beaker. This solution was also heated to 50 °C.

Wafers P-12, P-13, P-14, and P-15 were then immersed in this etchant. The combination of wafers in this batch was identical to the combination of wafers processed in the previous etch; that is, two wafers from each lot in the initial hydrazine etch experiment.

The wafers were then immersed in the 100% HF solution for 60 seconds, and they were immediately immersed in the heated

(52 °C) hydrazine solution for 15 minutes. The wafers were continuously agitated for 15 minutes. They were then immersed in bleach, rinsed in DIW, and dried.

3.4.2 *Silicon Micromachining the Deep Vertical-Wall Grooves (DVWGs).* The DVWGs were realized on the frontside of wafers V-1 to V-25 using a 4:1, DIW:KOH (by weight) solution prepared in a teflon beaker which was immersed in the Lufran constant temperature (40 °C) bath [13]. To prepare the solution, 200 grams of KOH (pellets) was dissolved in 1,000 ml of DIW.

Prior to etching the DVWGs, the wafers were cleaned in 100% H_2SO_4 for 20 minutes at 100 °C to remove contaminants and the remaining photoresist. The wafers were then rinsed in the N_2 bubbler to a 10 megohm resistance standard and blown dry with N_2.

These wafers were then etched in the 4:1, DIW:KOH solution for approximately 720 minutes [81]. After verifying that the DVWG structures were successfully realized, the wafers were then rinsed in DIW, immersed in 100% HF, rinsed again in DIW, and stored in their original shipping container until they were epoxied to the IC die host wafers and thin-film resistor host wafers.

3.4.3 *Silicon Micromachining the Micro-Fluid Channel.* The micro-fluid channel structures and the corresponding feed-through holes were realized on the frontside of wafers F-2 to F-12 with a 4:1, DIW:KOH (by weight) etchant prepared in a teflon beaker which was immersed in the Lufran constant

temperature (50 °C) bath [13]. To prepare this etchant, two-hundred grams of KOH pellets were dissolved in 800 ml of DIW.

Before the micro-fluid channels were realized, feed-through holes were first anisotropically etched completely through the wafers to facilitate access to the micro-fluid channel with the micro-tubing and micro-connectors. Prior to etching the feed-through holes and the subsequent micro-fluid channels, the wafers were cleaned in 100% H_2SO_4 for 20 minutes at 100 °C to remove the contaminants and the remaining photoresist. The wafers were then rinsed in the N_2 bubbler to a 10 megohm resistance standard and dried with N_2.

These wafers were then anisotropically etched for approximately 33 hours to realize the feed-through holes, and 3 hours to realize the micro-fluid channels [13]. The etch rate was periodically monitored and verified with a micrometer and a sacrificial test wafer.

After verifying with an optical microscope that the structures were successfully realized, the wafers were rinsed in DIW, immersed in 100% HF, blown dry with N_2, and stored in their original shipping container until they were electrostatically bonded to the Pyrex 7740 glass plates.

3.5 *Design and Fabrication of the Diffused and Thin-Film Aluminum Resistors*

Two heat-dissipating devices were designed and fabricated to simulate the thermal burden created by an IC die involved in wafer scale integration technology. To provide comparative results, diffused and thin-film aluminum resistors were utilized. They were designed to consume approximately 2 W of electrical power. Complex, contemporary, large-scale IC die typically consume 2 W of electrical power [11].

3.5.1 *Diffused Resistor Design and Fabrication.* For an applied bias of 0 - 10 volts, a 50 ohm resistor will theoretically consume 0 - 2 W of electrical power. The product of the voltage and the current flowing through the resistor yields the electrical power in watts. Thus, a 50 ohm resistor was designed using the MAGIC software tool on the SUN workstations in the AFIT VLSI Laboratory (Figure III-6). After the design was accomplished, 8 of the 50 ohm resistors were submitted for fabrication by MOSIS; the standard 2.0 micron square "tiny-chip" IC die were specified [1]. N-diffusion was specified as the resistor material with a contact pad connected to each terminal of the resistor [1]. Unpackaged IC die were requested so that they could be epoxied directly to the host silicon wafers.

The resistor was designed using a nominal sheet resistance value of 38.3 ohms/sq (published by MOSIS for the standard VLSI technology semiconductor fabrication process). Based upon the power (P) requirement of 2 W, the necessary resistance, R, was calculated from $P = V \cdot I = V \cdot V/R = V^2/R$, where V is the applied voltage and I is the current flowing through the resistor. Then, based upon the resulting 50 ohm resistor requirement and the nominal 38.3 ohms/sq sheet resistance value, a 1.3055 ratio (50/38.3) was determined for the diffused area. Since a 200 x 200 micron contact pad was specified, the width of the diffused area was designed to be 200 microns. For an approximate ratio of 1.31 squares, the length of the diffusion area was calculated to be 262 microns (200 x 1.31). The resulting resistor possessed a 200 x 262 micron area of n-diffusion positioned between the two, 200 x 200 micron sized contact pads. The n-diffusion process was preferred relative to the p-diffusion process to prevent positive space charges from accumulating and inducing internal biasing effects [1].

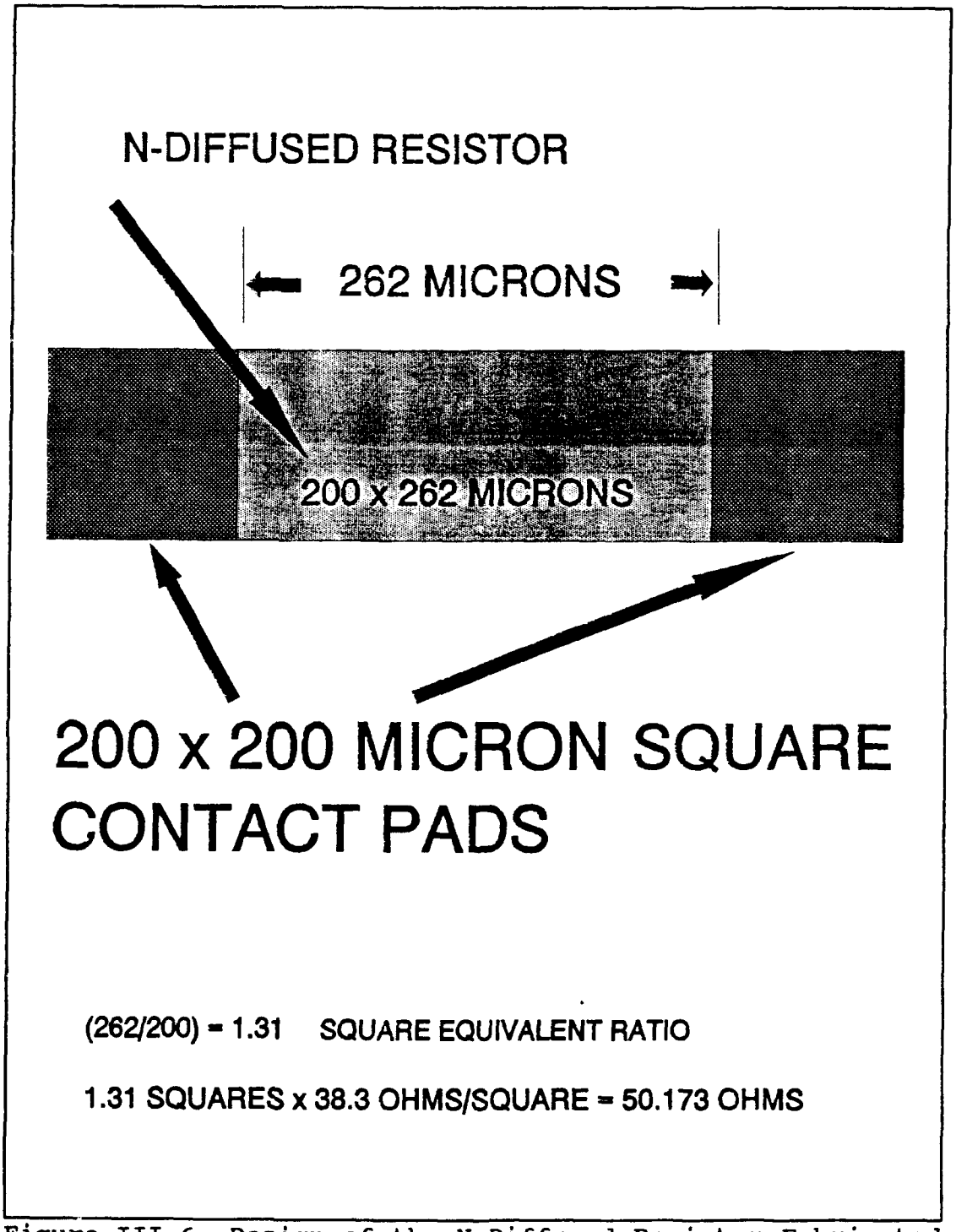


Figure III-6. Design of the N-Diffused Resistor Fabricated by MOSIS.

Once the design on the SUN workstation was complete, a CalTech Intermediate Format (CIF) computer file was created and transferred to MOSIS. The IC die were received approximately 8 weeks later.

3.5.2 *Thin-Film Metal (Aluminum) Resistor Fabrication.* Since the actual value of the MOSIS IC die resistors were measured to be 33 ohms, 33 ohm thin-film resistors were designed to be realized by evaporating aluminum conductors onto silicon wafers. The appropriately modified pattern for the resistor was then fabricated in Rubylith, along with the pattern for the metal-conductor lines used to apply a voltage to the resistor.

The wafers which were exposed to the thin-film resistor photomask were mounted in the deposition system (Denton Vacuum Corporation, model DV602, Cherry Hill, NJ 08003). Thin films of aluminum were iteratively deposited on the wafers until a desired value of resistance was realized, and uniformity was accomplished among the resistors on at least four of the silicon wafers. A maximum of four wafers at a time could be placed in the deposition system. The wafers were then removed and placed in petri dishes filled with acetone. The acetone removed the photoresist which was not exposed to the ultraviolet light, and it also removed the subsequent overlying aluminum layer, leaving behind the

desired metal pattern. Vigorous physical agitation was necessary to remove all of the unwanted photoresist and aluminum. The film thicknesses were verified with the Dektak stylus profilometer (Sloan Technology Corp., model Dektak IIA, Santa Barbara, CA 93109). Conductive (copper) adhesive tape was placed over the aluminum conductor lines to protect them where repeated physical contacts were subsequently made. The resistances were measured with an ohmmeter and recorded. The wafers were then placed into their original shipping containers until they were epoxied to the host micromachined and reference silicon wafers.

3.6 Wafer Sandwich Thermal Module Construction

The silicon wafers hosting each of the three configurations of resistors were epoxied to the heat-dissipating wafers with diamond-filled, ultra-high thermally-conductive (80 Btu·in/sq.ft·hr·°F) and electrically-insulating (10^{14} ohm·cm) epoxy (A.I. Technology, Inc., EG7659, Trenton, NJ 08618) (Figure III-7). This epoxy was selected for its high thermal conductivity and ability to provide heat-flow paths within the silicon wafer thermal modules. Before applying the epoxy to the surfaces of the silicon wafers, they were cleaned with acetone and methyl alcohol.

The following wafer sandwich thermal module configurations were fabricated to realize the objectives outlined in Chapter I and Section 3.1:

1) A thin-film aluminum resistor wafer, hosting one device, was epoxied to the backside of a reference wafer (Module 1).

2) A thin-film aluminum resistor wafer, hosting one device, was epoxied to the backside of a wafer with randomly spaced and sized pyramid structures realized on its frontside (Module 2).

3) A thin-film aluminum resistor wafer, hosting one device, was epoxied to the backside of a wafer with DVWG structures realized on its frontside (Module 3).

4) A thin-film aluminum resistor wafer, hosting one device, was epoxied to the backside of a wafer with a micro-fluid channel structure realized on its frontside (Module 4).

5) A single IC die mounted on a wafer was epoxied to the backside of a reference wafer (Module 5).

6) A single IC die mounted on a wafer was epoxied to the backside of a wafer with the randomly spaced and sized pyramid structures realized on its frontside (Module 6).

7) A single IC die mounted on a wafer was epoxied to the backside of a wafer with the DVWG structures realized on its frontside (Module 7).

8) A single IC die mounted on a wafer was epoxied to the backside of a wafer with the micro-fluid channel structure realized on its frontside (Module 8).

9) Four IC die on a host wafer were epoxied to the backside of a reference wafer (Module 9).

10) Four IC die on a host wafer were epoxied to the backside of a wafer with randomly spaced and sized pyramid structures realized on the frontside of the wafer (Module 10).

11) Four IC die on a host wafer were epoxied to the backside of a wafer with DVWG structures realized on the frontside of the wafer (Module 11).

12) Four IC die on a host wafer were epoxied to the backside of a wafer with a micro-fluid channel structure realized on the frontside of the wafer (Module 12).

These twelve thermal modules were assigned corresponding module numbers one through twelve (Module 1, ...Module 12).

3.6.1 Thin-Film Aluminum Resistor Thermal Module Fabrication. The silicon wafers hosting the thin-film aluminum resistors were epoxied to the heat-dissipating wafers.

First, the heat-dissipating wafers were secured in the wafer clamp part of the jig designed for taking temperature

measurements with the thermocouples. The 2 components of the epoxy (resin and hardener) were mixed (1:1, component A:component B) and spread evenly on the backside of the thin-film aluminum resistor host silicon wafers using a glass microscope slide. These silicon wafers were then placed in contact with the wafers in the wafer clamp. A bare silicon wafer was placed on the top of the silicon wafer thermal module to protect the host resistor wafer. The wafer clamps were then tightened to induce pressure on the module and evenly distribute the epoxy. The module was then removed from the clamp and transferred to an oven. The epoxy was cured at 85 °C for 60 minutes and post cured at 150 °C for 2-8 hours.

3.6.2 *IC Die Mounting.* The MOSIS fabricated IC die were epoxied to the IC die host wafers, designated D-1 to D-25, using the same EG7659 epoxy. The four edges of the IC die were smoothed using an ultra-fine sandpaper (approximately 1000 grit). They were held with tweezers and brushed across the surface of the sandpaper 5 to 10 times to remove the irregularities due to the sawing and lapping process. Epoxy was spread on the backside of the IC die with wafer grippers. The IC die were then placed into their recess holes.

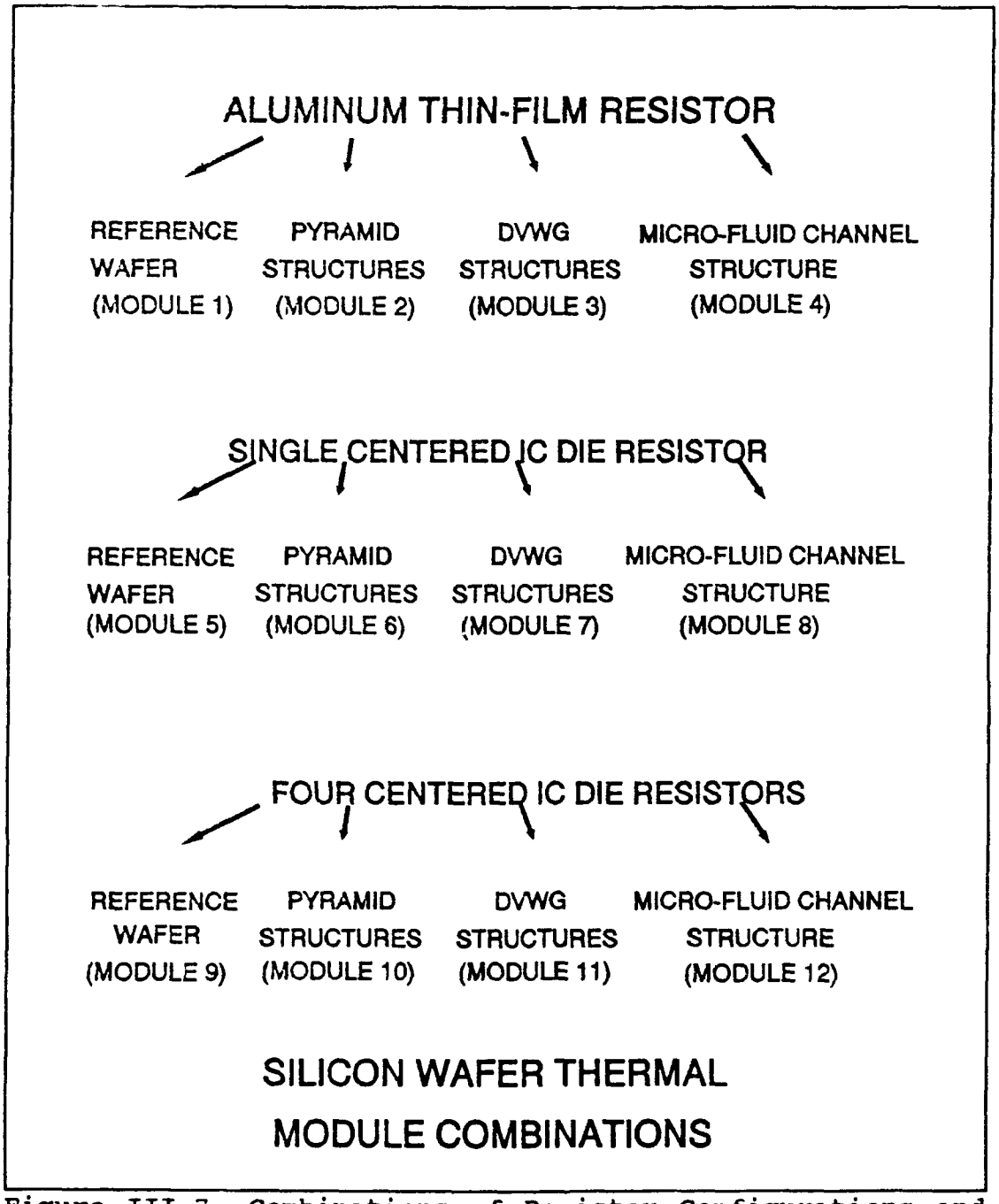


Figure III-7. Combinations of Resistor Configurations and Micromachined Silicon Structures.

Pressure was applied directly to the IC die with a cotton swab to evenly distribute the epoxy. The wafers were immediately transferred to an oven. The epoxy was cured at 85 °C for 60 minutes and post cured at 150 °C for 2-8 hours.

3.6.3 *IC Die Resistor Thermal Module Fabrication.* The silicon wafers hosting the single IC die and the four IC die were similarly epoxied to the four variants of the heat-dissipating silicon wafers.

An epoxy application process was designed for this fabrication step. First, experimentation was performed on a test silicon wafer using a glass slide to apply the epoxy. Numerous application iterations were accomplished until a visibly uniform coating of epoxy was realized between two strips of adhesive tape on a test wafer. The epoxy was cured and measured with the Dektak stylus profilometer and a micrometer; the results are discussed in the next chapter. Ultimately, pairs of test silicon wafers were epoxied together. These results were also measured, and the results are discussed in the next chapter.

The four heat-dissipating silicon wafers (untextured reference wafer and the three textured micromachined silicon wafers containing the randomly spaced and sized pyramids, the DVWGs, and the micro-fluid channel) were secured in the wafer clamp. The two components of the EG7659 epoxy were

mixed (1:1, component A:component B) and spread evenly on the backside of the wafers with the mounted IC die using a glass microscope slide. These wafers were then placed in contact with the wafers in the wafer clamp. The module was then removed from the clamp and immediately transferred to an oven. The epoxy was cured at 85 °C for 60 minutes and post cured at 150 °C for 2-8 hours.

3.6.4 *Micro-Fluid Channel Thermal Module Fabrication.* In order to seal the micro-fluid channel with a water-tight seal, the silicon wafers hosting the micro-fluid channel were electrostatically bonded to Pyrex 7740 glass plates. An electrostatic silicon wafer-pyrex bond was realized by applying 1,600 volts for 20 hours at 150 °C across the wafer and glass thermal module configuration. This voltage/temper-ature combination was suggested by Capt Reston [13].

DIW was pumped through the micro-fluid channel as the thermal analysis was performed on those modules. A peristaltic pump (Omega Engineering, Inc., Model FPU-254, Stamford, CT 06907-0047) was used to pump DIW from a large reservoir (2,000 ml or 4,000 ml beaker) through 1/16-inch inside diameter (ID) tubing. To facilitate access to the micro-fluid channel feed-through holes, the tubing was connected to 0.53 mm ID stainless steel microtubing (Valco

Instruments, Inc., Houston, TX 77255) with 1/8-inch outside diameter (OD) to 0.8 mm OD reducers (Valco Instruments, Inc., Houston, TX 77255). The microtubing was then connected to Valco butt connectors which were aligned with and epoxied to the feed-through holes. The DIW flowed from the reservoir, through the tubing and microtubing, through the micro-fluid channel, through the exit microtubing and tubing, and back into the reservoir (Figure III-8). The specified variable flow rates for the FPU-254 pump span 3 ml/min. to 1,000 ml/min. The flow rate was measured by pumping DIW through the modules into a graduated cylinder and observing the elapsed time. Twenty-five psi was the pump's specified maximum output pressure.

Several samples of the micro-fluid channel cooling configurations were tested for leaks. The speed of the peristaltic pump was increased to realize its maximum output. The system was allowed to operate for several minutes while it was visually inspected for leaks. The test was conducted several times on each sample before epoxying them to the resistor host wafers.

3.7 *Thermal Analysis*

An external bias was applied to the IC die resistors mounted on the silicon wafer thermal modules to realize heat loads on the order of 2 W. A DC power supply was connected

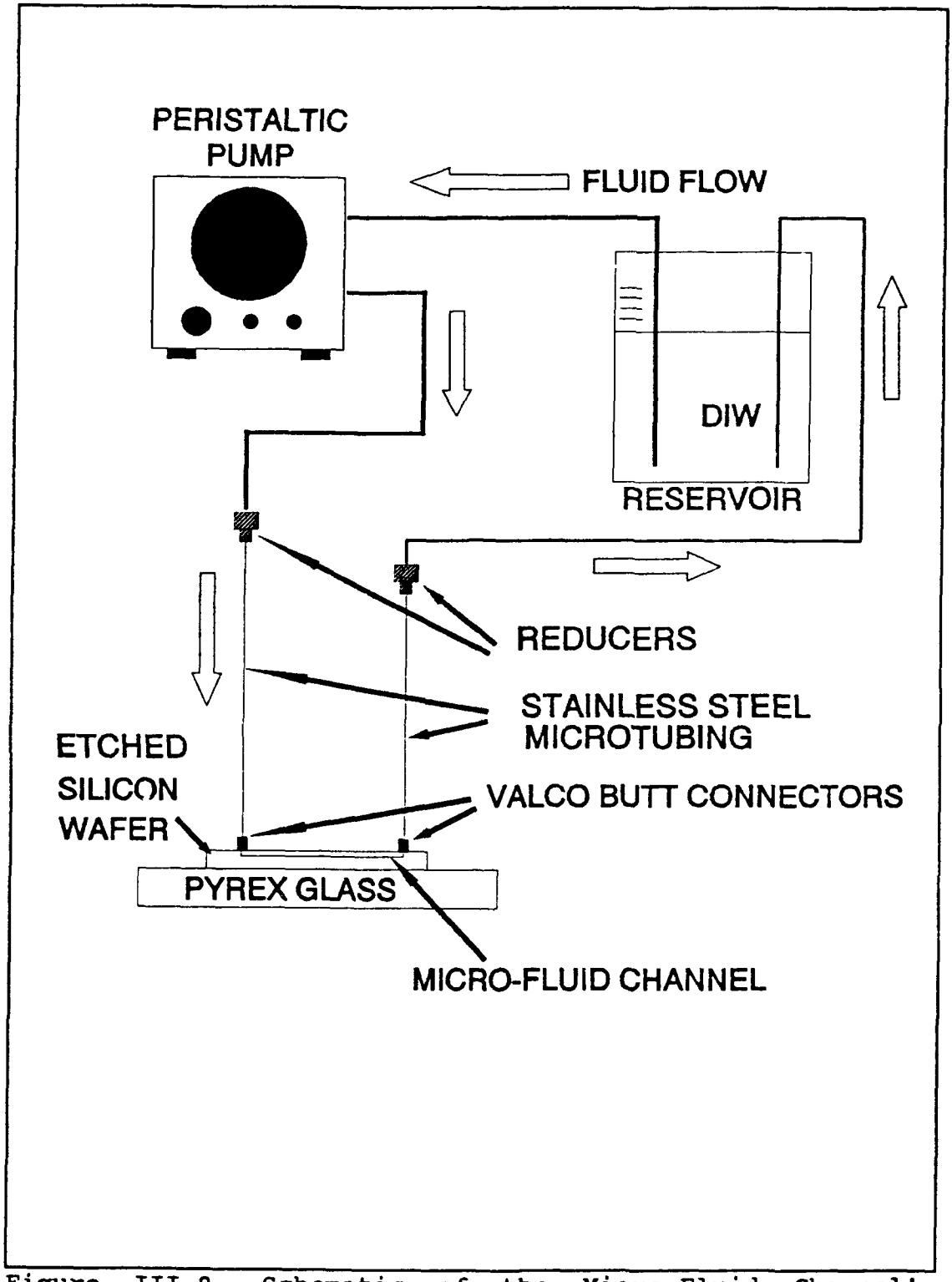


Figure III-8. Schematic of the Micro-Fluid Channel's Operation.

to the resistors with electrical leads and alligator clips which made electrical contact with the thermal module's copper tape contact pad. The current was increased until 2 W was being consumed by the resistor(s) on the thermal module. The applied current was determined for each resistor and resistor configurations as required because of the variation in resistor values. An ammeter was also connected in series with the power supply circuit, and the target power output (P) was determined by $P = I \cdot V = I \cdot I \cdot R = I^2 \cdot R$, where P is the power in watts, I is the current in amperes, R is the value of the resistor in ohms, and V is the voltage impressed upon the resistor. Equal increments of thermal power generation were determined for each resistor, and their temperature and infrared (IR) signatures were recorded in incremental, consistent steps. For example, the temperatures and IR signatures were observed at 0, 0.5, 1.0, 1.5, and 2.0 W.

3.7.1 *Temperature Measurements.* A special jig was designed to secure the wafer thermal modules and record the temperatures at precise locations on the top surface of the IC die thermal modules. The jig was fabricated by the AFIT Model Shop. The jig consists of a teflon block which contained a square 3 x 3 array of thermocouples (Physitemp, ICT-4, Clifton, NJ 07013), and its function was to

facilitate the precise relocation of the thermocouples over the entire surface of the silicon wafer thermal module in two-dimensions with micron-dimensional accuracy (Figure III-9). The ICT-4 thermocouples were specifically fabricated for the IC die temperature measurements. They were connected to a thermocouple scanner card (Keithley Instruments, Inc., Model 7057A, Cleveland, OH 44139). A Keithley Scanner (Model 706) was used with the scanner card to multiplex the signals from the thermocouples and pass them to an electrometer (Keithley model 617) at precise times during a change in the externally applied bias to the thermal module's resistor(s). The signals from the thermocouple array were controlled by a computer program that was written by Capt Wiseman [85]. The program also initialized the scanner and the electrometer for each measurement process. Appendix H posts a copy of the computer program; it was compiled in Turbo Pascal.

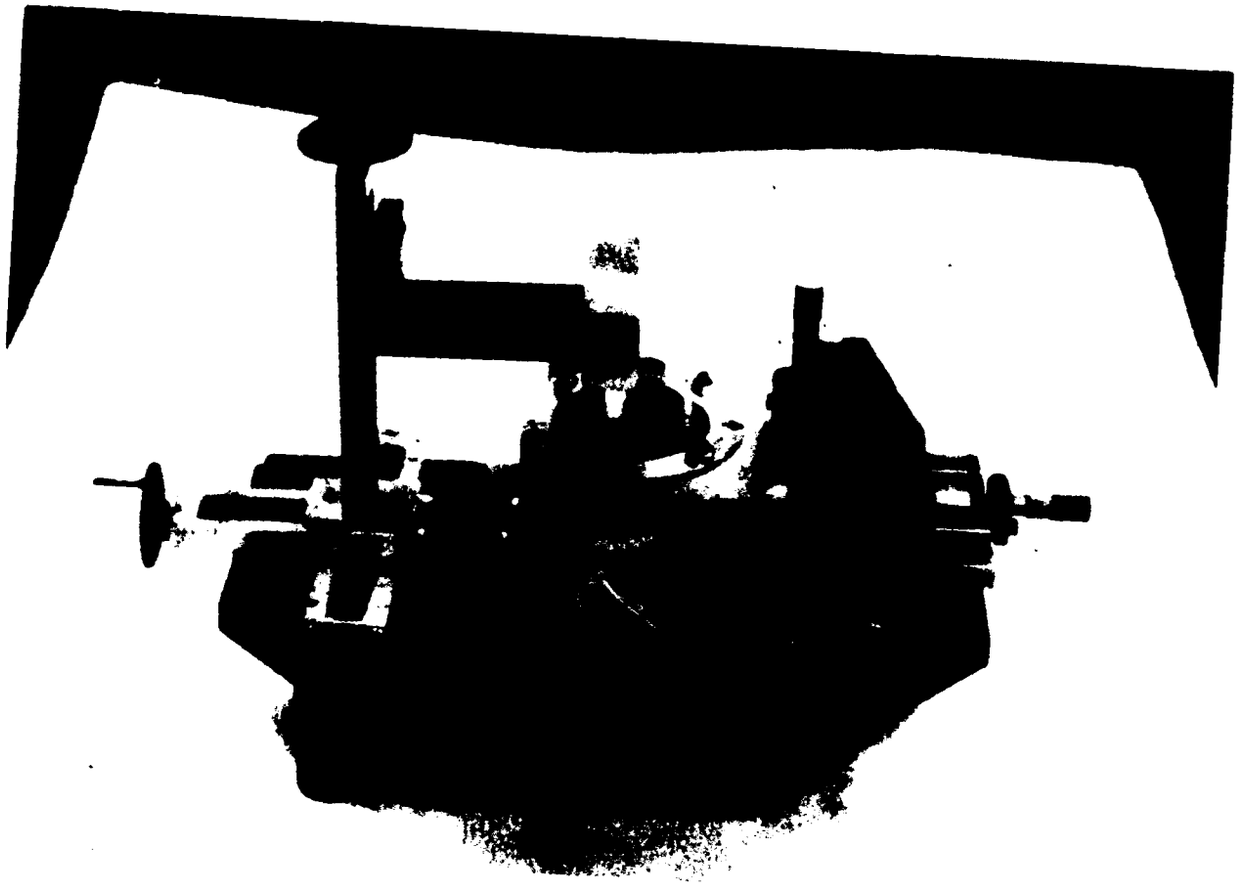


Figure III-9. Thermocouple Jig.

The thermocouple in the center of the thermocouple array was allowed to contact the center of each resistor configuration. The center of each resistor configuration was considered to be the measurement origin. After the temperatures were recorded, the array was moved 2 centimeters from the origin in each of three directions along the surface of the silicon wafer thermal module: 1) up, 2) left, and 3) right. The array was allowed to contact the module at these locations, and the temperatures were recorded. The array was then re-centered. The current was then increased (from 0 amperes the first time) to realize the desired power dissipation in the resistors. After 3-5 minutes, the temperature recording algorithm was reaccomplished. The results are provided in Chapter 4.

3.7.2 *IR Signature Recording.* The silicon wafer thermal modules were placed under the IR Microscope (Research Devices, Inc., Model-F, Berkeley Heights, NJ 08854). The IR signature was recorded on Scotch VHS format videotape (3M Co., Hutchinson, MN 55350-9431) using a Sharp Camcorder as the bias was applied and the heat dissipation increased from 0 W to 2 W. The signatures were also recorded with a Polarcid instant camera at the same predetermined power ratings. The camera was positioned in front of the video display which is part of the IR camera

system. The photographs were taken from the image on the video display screen.

IV. Experiment Results

This chapter discusses the results of the research and experiments described in Chapter III. In this chapter, the final products of the silicon micromachining processes are described. Optical photographs and Scanning Electron Microscope (SEM) photomicrographs of the resulting silicon micromachined structures are provided. The data obtained from the temperature measurements using the thermocouple array is also provided and analyzed.

4.1 Results of the Silicon Wafer Thermal Module Design

Twelve silicon wafer thermal modules were fabricated for the experiments that were described in Chapter III. These modules generated the experimental results as the heat-producing devices when they were connected to a power supply, and the modules' temperatures were spatially recorded with the thermocouple array. Six of the twelve modules provided IR images which were captured with an IR microscope. The four modules hosting the thin-film resistors and the four modules hosting a single IC die were characterized with the IR microscope.

The twelve silicon wafer thermal modules ultimately functioned as designed after minor modifications were implemented in some of the fabrication processes.

The results of each thermal module fabrication process step, as well as the associated deviations and arising complications, are described in the following sections of Chapter IV.

4.2 Results of the Photomask Design and Fabrication

Several photomasks were realized on 4 x 4-inch Kodak HRPs via the processes described in Chapter III. The photoreduction and development processes were accomplished repeatedly until all of the required photomasks hosted dark images with sharp edges separating the dark and light regions on the developed HRPs. The quality of the image sharpness and contrast was optimized by experimenting with the focus, exposure times, and development times. The darkness of the images was compared to those on the photomasks fabricated by Capt Uyehata (they were assumed to be successful) [1; 4]. The desired images were at least as dark, under an optical microscope, as the images on Capt Uyehata's photomasks. The image darkness was realized with exposure times in the 2 - 10 minute range on the photoreduction camera system, and 8.5 seconds in the mask duplicator. It was determined during the silicon wafer processing that the exposure and development times were not very critical. Successful photoresist patterning and metallization products were realized using a reasonably wide

range of exposure and development times. The critical factor in photomask fabrication was determined to be the focus of the photoreduction camera system during the exposure of the HRPs. This crucial factor required extreme care and patience to realize high quality photomasks. Several metallization and photoresist patterning processes were unsuccessful, and their failure is attributed to a poor focus during the HRP exposure. The HRP exposure and development process, and the photoresist exposure and development processes, manifested significant flexibility, as did the steps accomplished in the metallization lift-off process. The requirement to sharply focus the image cut into the rubylith onto the HRP through the photoreduction camera lens exhibited extremely little flexibility, and a successful photomask exhibited clearly distinguishable edges under an optical microscope. On the photomasks containing image regions far from the physical center of the mask, the images were not as sharp, and this problem could not be corrected. For example, the edges were fuzzy and not well defined on the circular images for the feed-through holes used in the micro-fluid channel structure. Fortunately, they were used in the anisotropic KOH etching process which is self-correcting since it seeks to etch the (100) planes. Consequently, focusing was slightly less critical for this application.

Cutting the designed images in the rubylith was tedious, but relatively simple. Because the coordinatograph display was faulty, several extraneous lacerations in the rubylith were covered with red cellophane adhesive tape prior to affixing the rubylith to the photoreduction camera system's screen.

By state-of-the-art microelectronics processing standards, the photolithographic dimensions required for silicon micromachining are large. The smallest feature in this research was the 20-micron wide image for the thin-film aluminum resistor, and thus, problems were nonexistent relative to the feature sizes.

4.3 Results of the Wafer Preparation

Several carousels of single-crystal silicon wafers were cleaned, identified, and oxidized as described in Section 3.3. The thin films of SiO_2 grown on the silicon wafers that were to be etched with the HH and AH were sufficiently thick to protect their backsides from the etchant. The backside of the silicon wafers was not etched in the first hydrazine etching experiment. The average thickness of the SiO_2 on these wafers was 0.83 microns (8,300 angstroms).

The thin film of SiO_2 grown on the (110)-oriented silicon wafers used to realize the DVWGs was sufficiently thick. The average SiO_2 thickness grown on these wafers was

1.6 microns. Figure IV-1 depicts the results measured with the Dektak stylus profilometer of one of the (110)-oriented silicon wafers. Figure IV-1 is a typical example of the results measured with the profilometer for the other wafers.

The initial attempts to pattern the DVWGs on the silicon wafers were unsuccessful. The failures were attributed to the use of less than adequate quality photomasks. After selecting Capt Uyehata's DVWG photomask with the highest quality image, as observed under an optical microscope, success was achieved. With less than extremely sharp and high-contrast images, and with small dimensions (5-micron wide grooves), the ultraviolet light leaked under the dark image of the grooves and polymerized the underlying photoresist. The polymerized photoresist acted as a barrier to the HF etchant, and would not allow the "windows" in the SiO_2 to be realized for the subsequent KOH etch; effectively, the image was lost.

Capt Uyehata demonstrated a successful technique for aligning the DVWG photomask with the (110)-oriented silicon wafer flat in the mask aligner. Since this was a very critical step, extreme care was used to align the wafer flat (it took approximately five minutes to align each wafer) to the photomask. Under the mask aligner microscope, the wafer was iteratively rotated and horizontally repositioned until

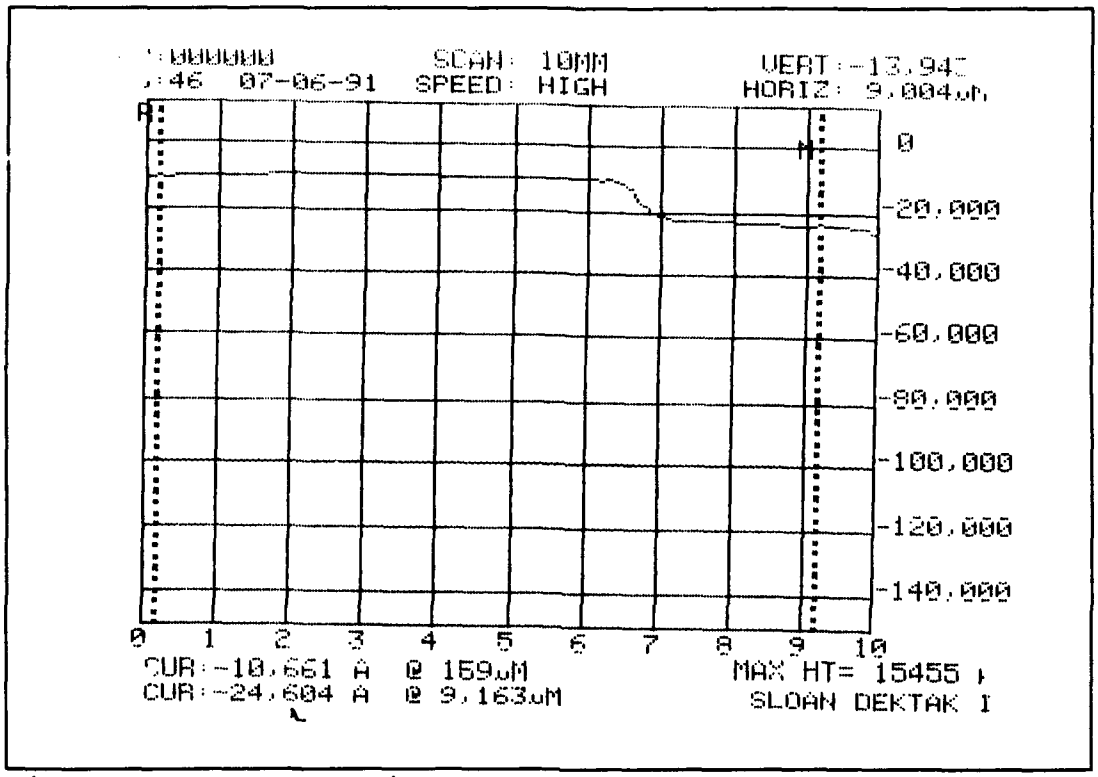


Figure IV-1. Step-Height Measurement of the SiO_2 Thickness on the (110)-Oriented Silicon Wafers Using the Dektak Stylus Profilometer.

the horizontal reference pattern on the photomask was aligned with a thin, bright reflection from the edge of the wafer's flat. The time invested was justified; DVWGs were realized on eleven of the first twelve wafers processed. One of the twelve wafers was aligned to the photomask with the shadow of the wafer flat, instead of the reflection from its edge. The failure to realize DVWGs is probably due to photomask mis-alignment or misorientation of the wafer flat by the manufacturer.

The silicon wafers used to realize the micro-fluid channel (MFC) structures were processed twice; once for realizing the feed-throughs, and a second time for realizing the MFC structures. A thicker SiO_2 growth was required as a mask for the etching process that was intended to micromachine completely through the thickness of the wafer, particularly for the feed-throughs and the epoxy-relief holes. An average SiO_2 thickness of 2.0 microns was required for this etching process to ensure a sufficiently thick protective mask. As a result, opening the windows in the SiO_2 required that the wafers be immersed in the HF etchant for a very long period of time. The etch rate for the HF solution described in Chapter III was experimentally determined to be approximately 0.18 microns per minute. It was discovered during the long immersion times in the HF etchant that the negative photoresist on the wafer's backside would not adhere to the silicon wafer if it was not exposed to ultraviolet light. In contrast, for shorter exposure times to HF, hardbaking the negative photoresist was sufficient to keep it intact without ultraviolet exposure. For longer exposure to the HF etchant, the photoresist needed the added robustness of the polymerized bonds that the ultraviolet light induced.

The silicon wafers used to host the IC die were similarly processed twice to realize the IC die recess holes

and the epoxy-relief holes. Once the IC die recess holes were micromachined on the frontside of the wafer, the pattern for the epoxy-relief holes had to be aligned to the recess holes. Since the surface of the recess holes was approximately 200 microns below the surface of the wafer, the ultraviolet light leaked beneath the image of the epoxy-relief holes causing several unsuccessful pattern transfer attempts. The exposure time was iteratively reduced from 60 seconds, in 5 second increments, to 15 seconds, after which successful pattern transfers were realized. The 15-second duration exposure was sufficient for the transfer of the square image to the photoresist, yet, insufficient to allow an adequate amount ultraviolet light rerquired to polymerize the photoresist beneath the image. Thus, a barrier to the HF etchant was not created.

The depth of the IC die-recess holes had to be measured with a micrometer, because the profilometer is only capable of measuring 63-micron (approximately) step-heights. The IC die-recess hole depths ranged approximately 190 - 210 microns. The etch rate of (100)-oriented single-crystal silicon in the 20% KOH solution at 50 °C was experimentally determined to be approximately 0.243 microns per minute. Figure IV-2 is a pair of SEM photomicrographs of an IC die-recess hole and the epoxy-relief hole micromachined into the frontside of a silicon wafer.

The thin-film aluminum conductors realized on the IC die host silicon wafers were not amenable to the wire-bonding technique used by Mr. Callahan. Several unsuccessful attempts were made to wire-bond to the aluminum and the IC die contact pads with gold wire. The deposited aluminum was determined by Mr. Callahan to be too hard, and the metal on the IC die contact pads was too soft. However, successful wire-bonds were made to the IC contact pads and the conductive, copper adhesive tape with 0.002-inch diameter aluminum wire.

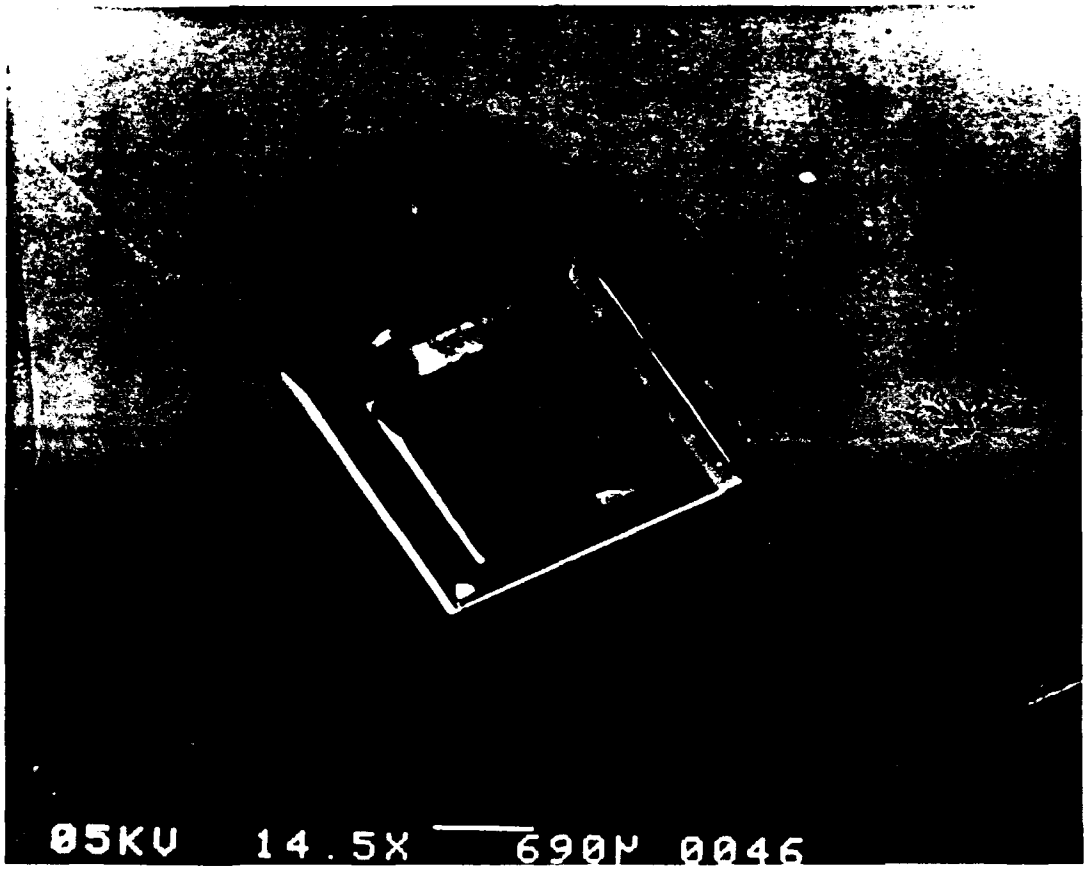


Figure IV-2. IC Die-Recess Hole and Epoxy-Relief Hole in (100)-Oriented Silicon (Magnification - 14.5x).

Figure IV-2 (Continued). IC Die-Recess Hole and Epoxy-Relief Hole in (100)-Oriented Silicon (Magnification - 48.5x).

Ten silicon wafers were cleaned, oxidized, and metallized to realize thin-film aluminum resistors as described in Section 3.3.6. Four, thin-film aluminum resistor host wafers were required for the thermal module combinations. Initially, several attempts with implementing the metallization lift-off technique failed. All of the parameters in the EENG 717 Laboratory Project Handout recipe for metallization lift-off were combinationally varied, but resistors were not successfully realized [12]. It was determined that the quality of the photomask was inadequate. When a high-quality photomask with well-focused, sharp images was used, the resistors were realized successfully each time, even when the other processing parameters were varied systematically.

The aluminum resistor was deposited several times on four silicon wafers. The aluminum deposition rate and thickness were varied iteratively until four resistors, with relatively close values of resistance, were realized on four silicon wafers. Their resistance values were also close (within an order of magnitude) to the values of those realized on the MOSIS IC die. The four thin-film aluminum resistors used in the experiments had measured values of 9, 14, 17, and 22 ohms.

The resistance in the aluminum conductors deposited on all of the silicon wafers was less than 0.2 ohms in each leg, including the resistance of the copper tape.

4.4 Results of the Silicon Micromachining Fabrication Process

As described in Chapter III, the randomly spaced and sized pyramids were realized with anisotropic etching techniques using a hydrazine etchant. The DVWGs and MFCs were realized via an anisotropic, wet-chemical etching process in a constant temperature, KOH etchant.

4.4.1 Results of Micromachining the Randomly Spaced and Sized Pyramids. In the first hydrazine etch experiment, the combination of the HH and AH etchant concentrations and temperatures produced nonuniform regions of randomly spaced and sized pyramids. The AH etchant produced regions of low, medium, and high population densities of pyramids in irregular blotches. The HH etchant produced irregular shaped regions of pyramid population densities. The average size of the pyramids' bases was less than half (2 microns) the size of the pyramids (5 microns) realized in Capt Uyehata's thesis [4]. Because of the smaller sized pyramids and the large regions that were sparsely populated with pyramids, it was determined that the initial hydrazine

solutions were too concentrated and the temperature was too high for achieving uniform results. The concentrated hydrazine solution seemed more characteristic of an isotropic etchant, oxidizing and removing silicon regardless of bond strengths and angles or crystallographic orientation. A second experiment with less concentrated hydrazine solutions at lower temperatures was justified to provide comparative results and help support the conclusions derived from the first experiment. The second experiment provided almost perfectly uniform pyramid population densities over the entire surface of the silicon wafer, as expected. The chemical reactions were evidently sufficiently restricted to respect the crystal orientation and become anisotropic. However, with the most dilute hydrazine solution used at the lowest temperature, the pyramid population became slightly less uniform. The high concentration of DIW seemed to impede the etchant (or possibly the removal of by-products). These results indicate a range of optimum hydrazine etchant concentrations and temperature combinations for realizing uniform pyramid populations.

Figures IV-3 through IV-26 provide visual support of the results. Figures IV-3 and IV-4 are photographs of the polished frontside and unpolished backside, respectively, of an unetched, unprocessed 3-inch diameter, single-crystal,

silicon wafer. They are included for comparison with the etched silicon wafers. Figures IV-5 through IV-9 are photographs of the surfaces of the silicon wafers etched in the two hydrazine experiments. Figure IV-5 is a photograph of a silicon wafer (1st experiment, 2nd batch) etched in AH at 62 °C. The surface is noticeably streaked with varying pyramid population densities. The streaks propagate in the same direction as the bubbles of gas rising from the AH during the violent etch reaction. A dense population of pyramids was found (with the SEM) only in the thin, dark streaks; the light colored regions were very sparsely populated with pyramids. The dark, mirror-like region in the upper left is untextured; it was protected from the etchant by the wafer holder.

Figure IV-6 is a photograph of a silicon wafer (1st experiment, 1st batch) etched in HH at 72 °C. A dense population of pyramids was found only in the dark, gray blotches.

Figure IV-7 and Figure IV-8 are photographs of silicon wafers (2nd experiment, 1st batch) etched in 92% HH at 52 °C. A dense population of pyramids was found over the entire frontside and backside surface. The backside was not protected with SiO_2 for the second experiment.

Figure IV-9 is a photograph of a silicon wafer (2nd experiment, 2nd batch) etched in 37% HH at 52 °C. The

chemical reaction was quite stable and presumed to be a much slower acting etchant. However, the pyramid population density was observed to increase over the entire surface of the silicon wafers. The pyramid population density of these wafers was not as uniform as the pyramid population density of those etched in the 92% HH solution. It was determined that the HH solution was too diluted (especially at 52 °C) to realize a substantial change in the texture of the silicon wafer's surface.

Figures IV-10 through IV-26 are photomicrographs obtained with the SEM. Figure IV-10 and Figure IV-11 are SEM photomicrographs of the polished frontside and unpolished backside, respectively, of an unprocessed, untextured, (100)-oriented, silicon wafer. These images are provided for comparative purposes for all of the silicon micromachined structures. Except for surface debris, there are no visible defects at 189x magnification on the wafer's frontside. On the backside, rectangular protrusions, representative of the (100) planes, are observable.

Figure IV-12 is an SEM photomicrograph of a densely populated region of pyramids. Figure IV-13 depicts a moderately populated region of pyramids. Finally, Figure IV-14 depicts a relatively sparse population. In these three figures, the silicon wafer sample is tilted 40° relative to the vertical. Figure IV-15 is an SEM

photomicrograph of a densely populated region at a higher magnification (1,420x). Here, the pyramidal features are distinguishable. Figure IV-16 and Figure IV-17 are higher magnification (2,600x) photomicrographs of moderately and sparsely populated regions, respectively. The larger pyramids have bases as large as seven microns.

Figures IV-18, IV-19, and IV-20 are SEM photomicrographs of dense, moderate, and sparsely populated pyramid, respectively, where the sample silicon wafer is tilted 10° relative to the vertical.

Figure IV-21 is an SEM photomicrograph of adjacent regions of dense and sparse populations of pyramids. This particular photograph shows the edge of one of the dark streaks on a silicon wafer etched in the first experiment.

Figures IV-22 and IV-23 depict the uniform, extremely dense population of pyramids realized in the second hydrazine etch experiment. These photomicrographs are representative of the entire surface of the silicon wafer. Figures IV-24 through IV-26 are incrementally magnified (1,800x, 3,500x, and 7,000x) SEM photomicrographs of textured surfaces similar to those in Figures IV-22 and IV-23.

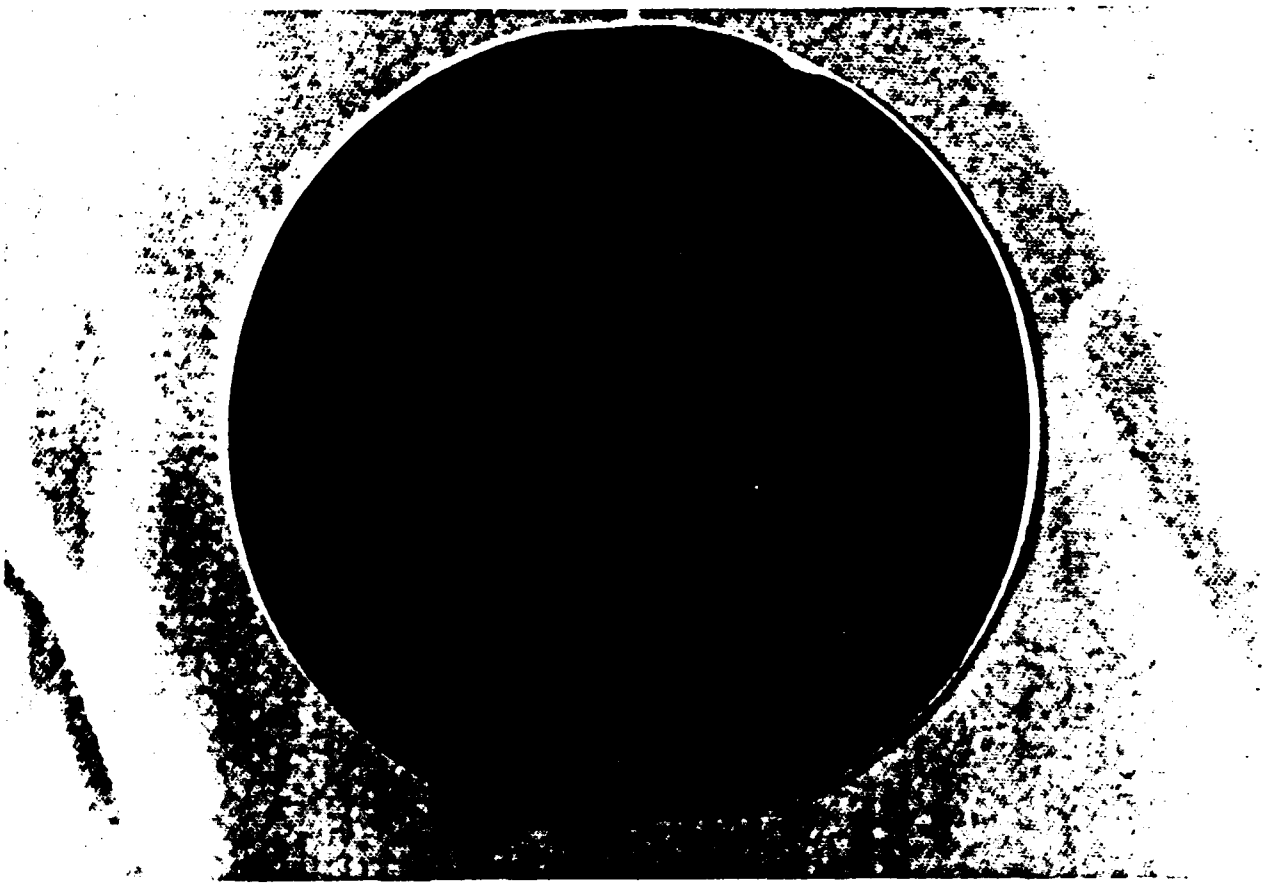


Figure IV-3. Surface of a Polished, Unetched, 3-Inch Diameter, (100)-Oriented Silicon Wafer (Magnification - 1.42x).

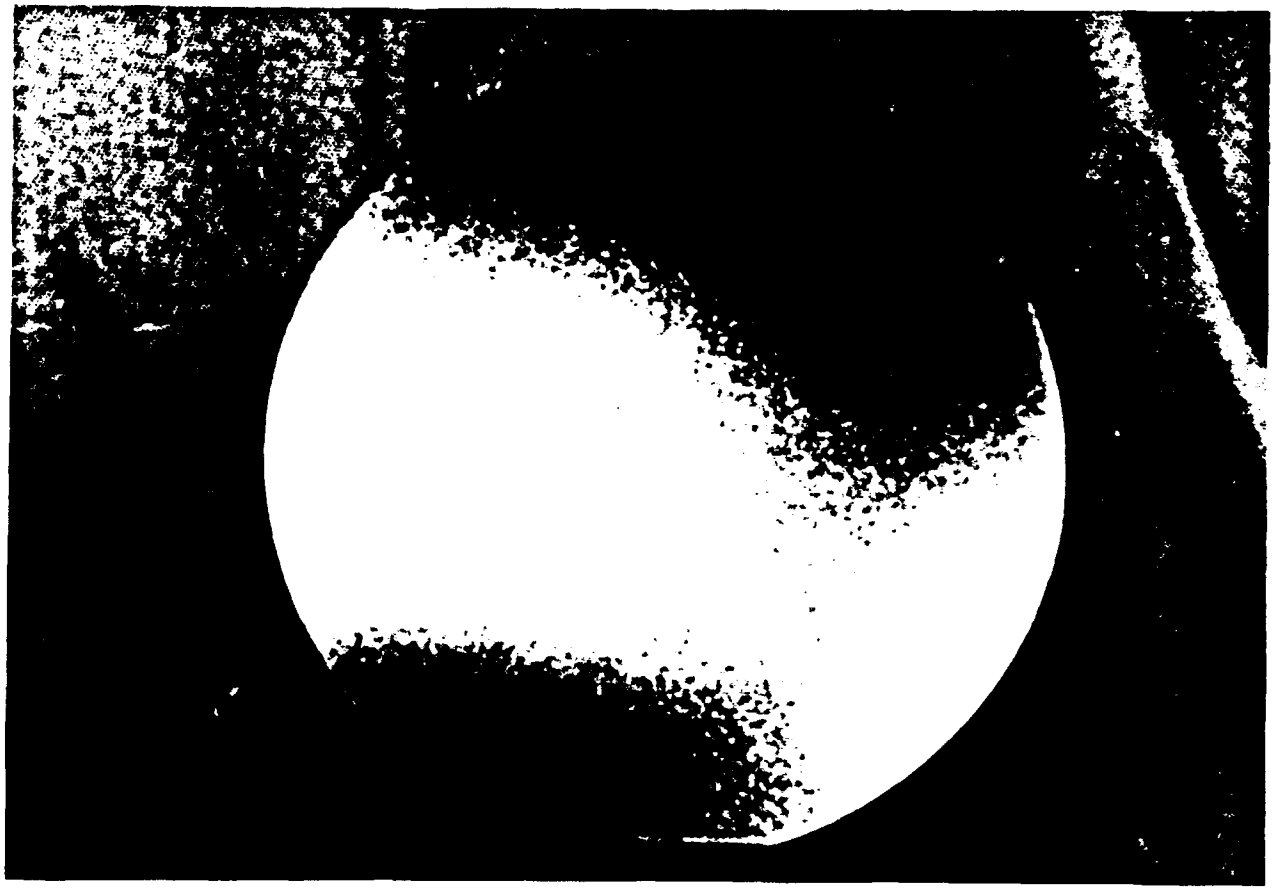


Figure IV-4. Surface of an Unpolished, Unetched, 3-Inch Diameter, (100)-Oriented Silicon Wafer (Magnification - 1.42x).

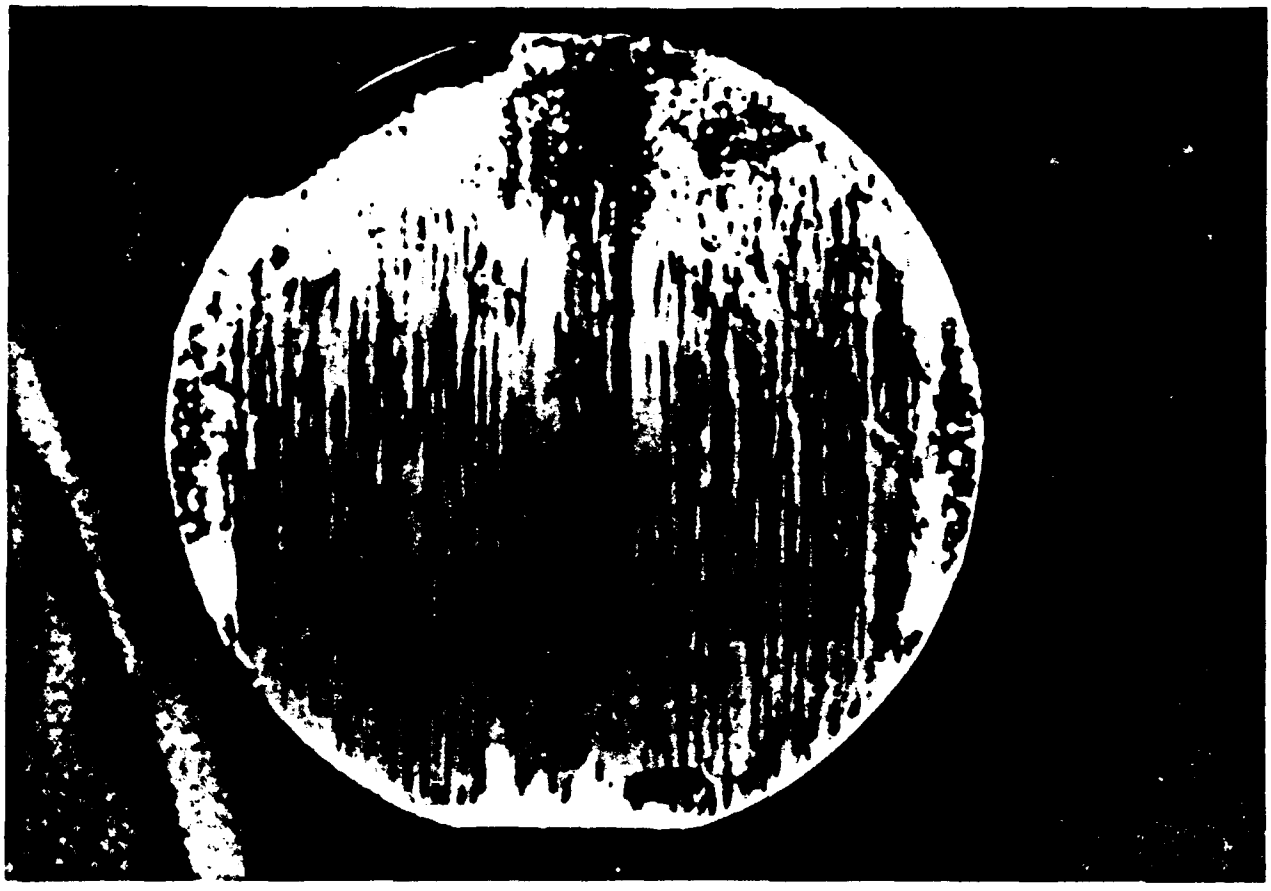


Figure IV-5. Three-Inch Diameter, (100)-Oriented Silicon Wafer Etched in a 3:2, DIW:AH Solution for 30 Minutes at 62 °C (Magnification - 1.4x).

Figure IV-6. Three-Inch Diameter, (100)-Oriented Silicon Wafer Etched in a 3:2, DIW:HH (85%) Solution for 30 Minutes at 72 °C (Magnification - 1.4x).

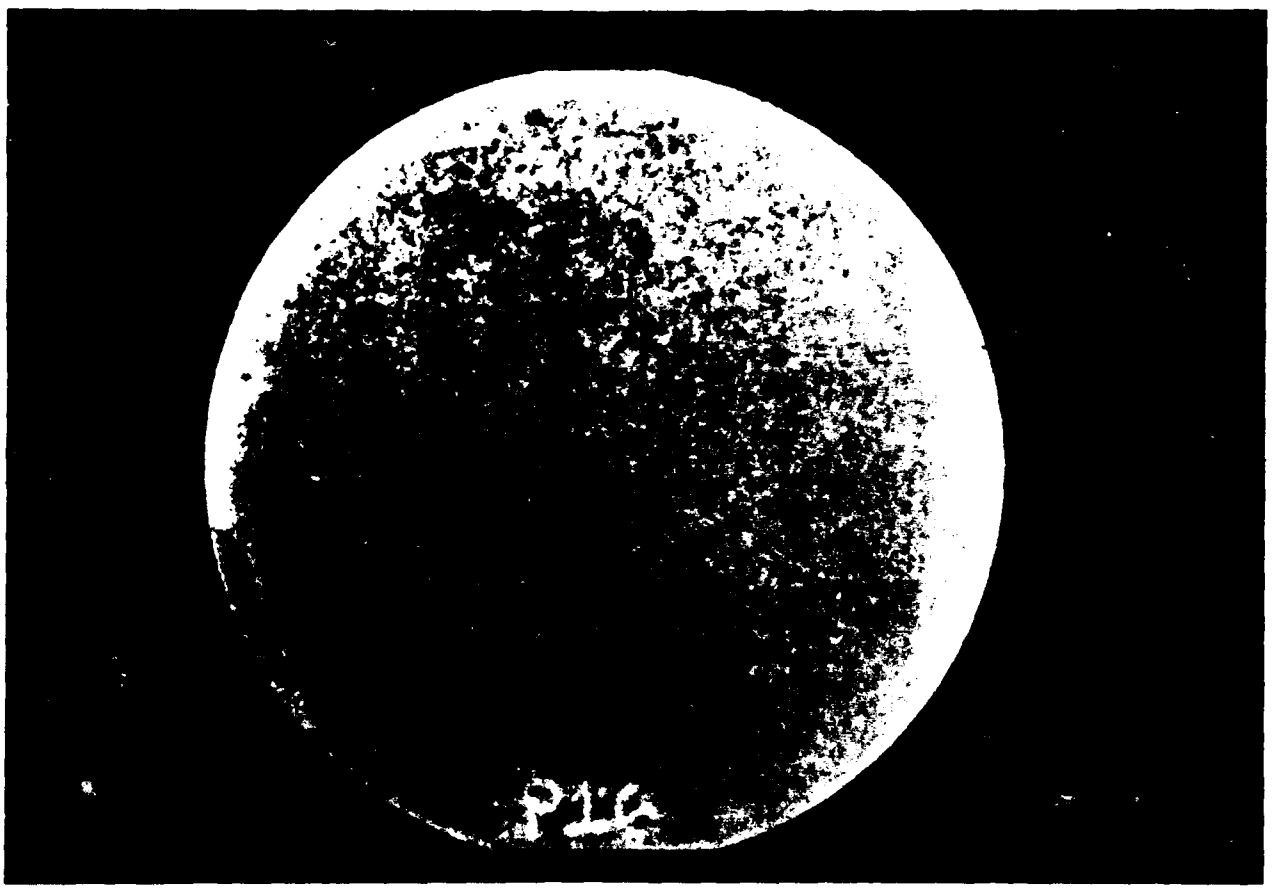


Figure IV-7. Three-Inch Diameter, (100)-Oriented Silicon Wafer Etched in a 3:2, DIW:HH (92%) Solution for 15 Minutes at 52 °C (Magnification - 1.4x).

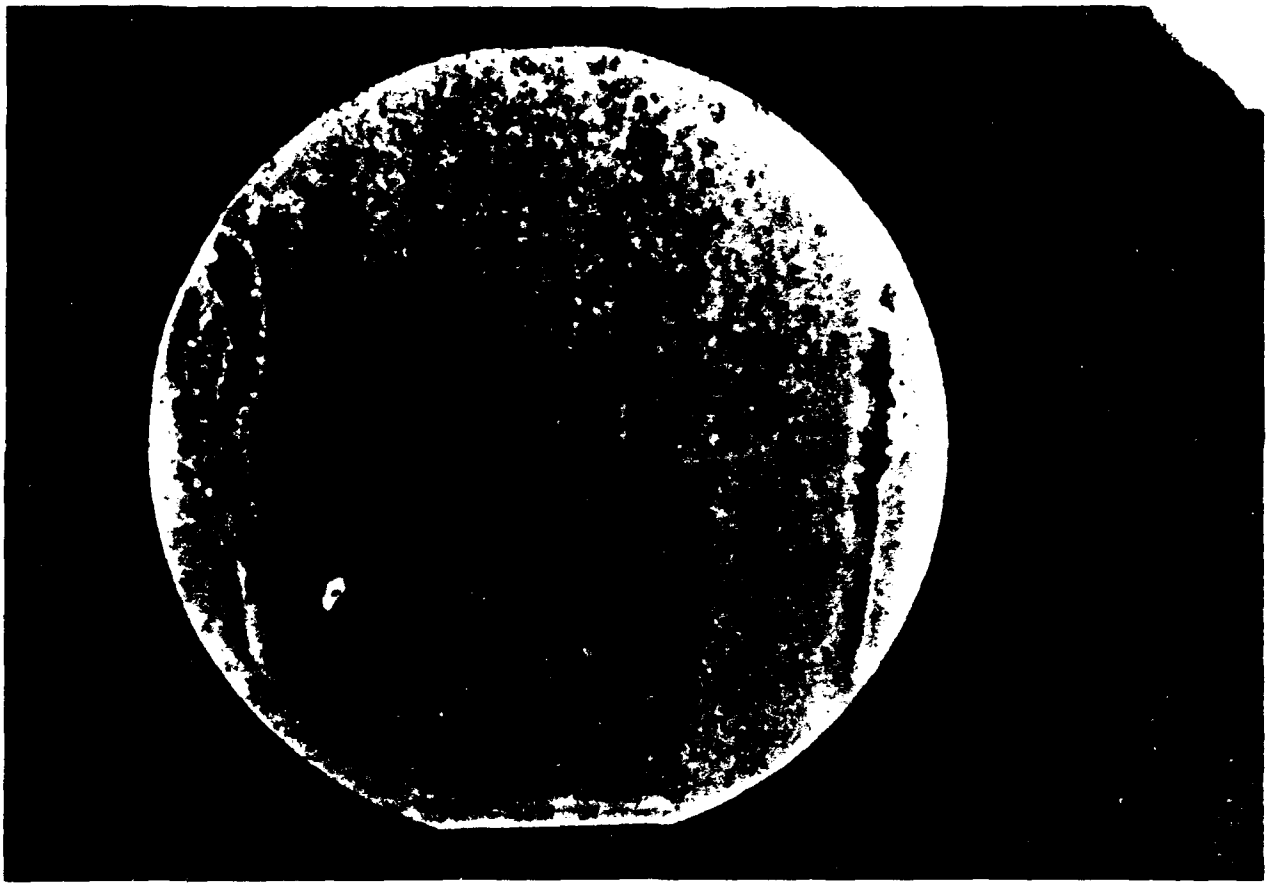


Figure IV-8. Three-Inch Diameter, (100)-Oriented Silicon Wafer Etched in a 3:2, DIW:HH (92%) Solution for 15 Minutes at 52 °C (Magnification - 1.4x).

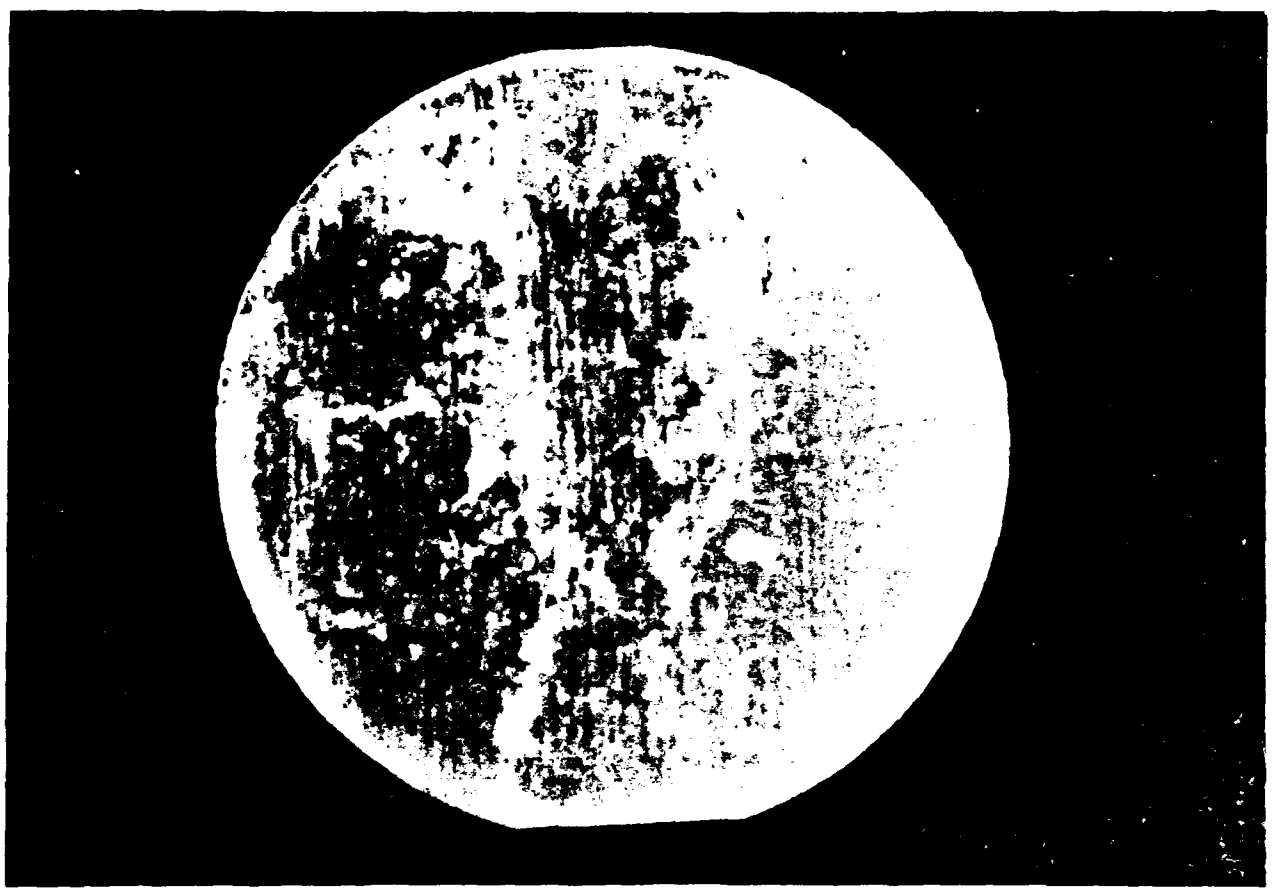


Figure IV-9. Three-Inch Diameter, (100)-Oriented Silicon Wafer Etched in a 3:2, DIW:HH (37%) Solution for 15 Minutes at 52 °C (Magnification - 1.4x).

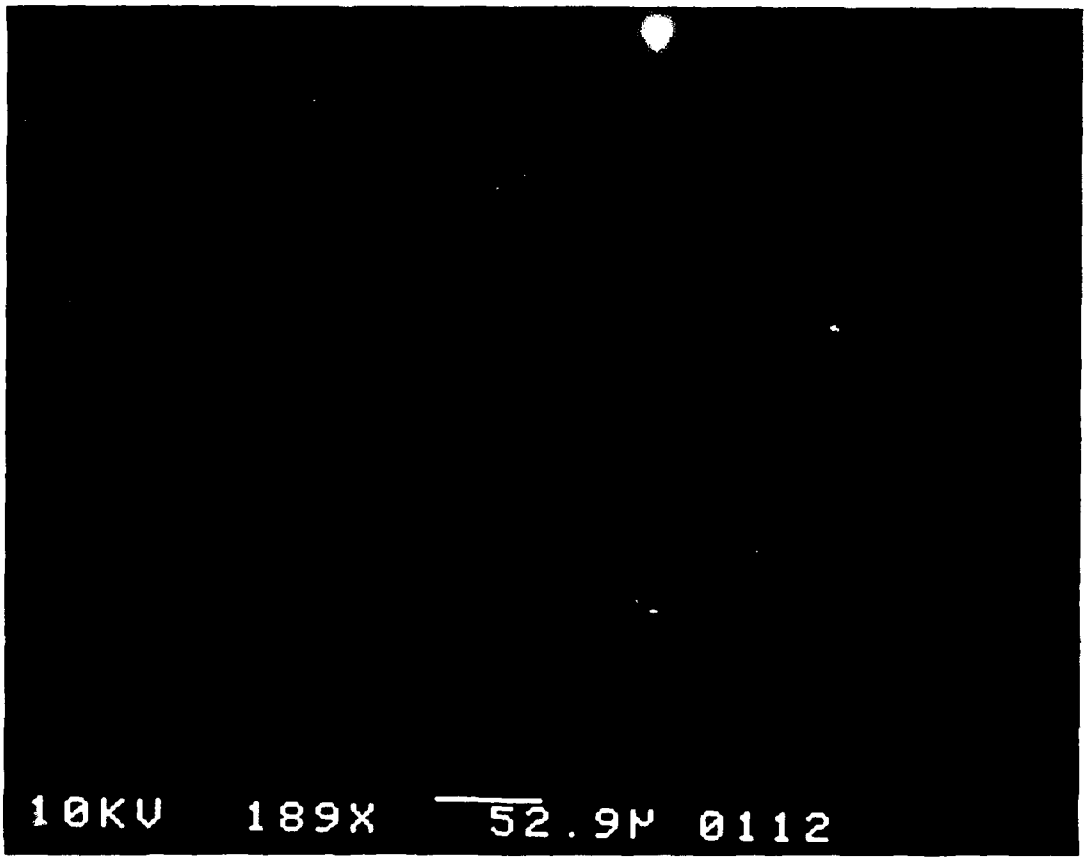


Figure IV-10. Polished, Untextured, (100)-Oriented Silicon (Magnification - 189x).

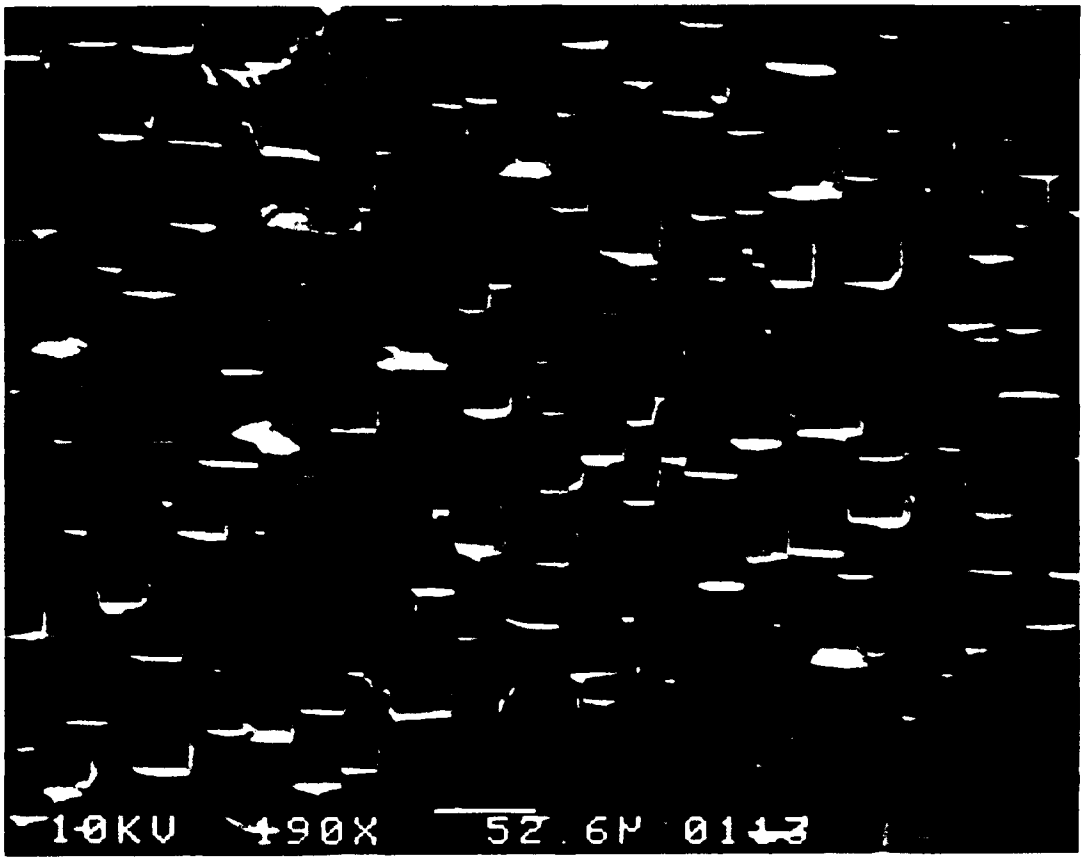


Figure IV-11. Unpolished, Untextured, (100)-Oriented Silicon (Magnification - 190x).

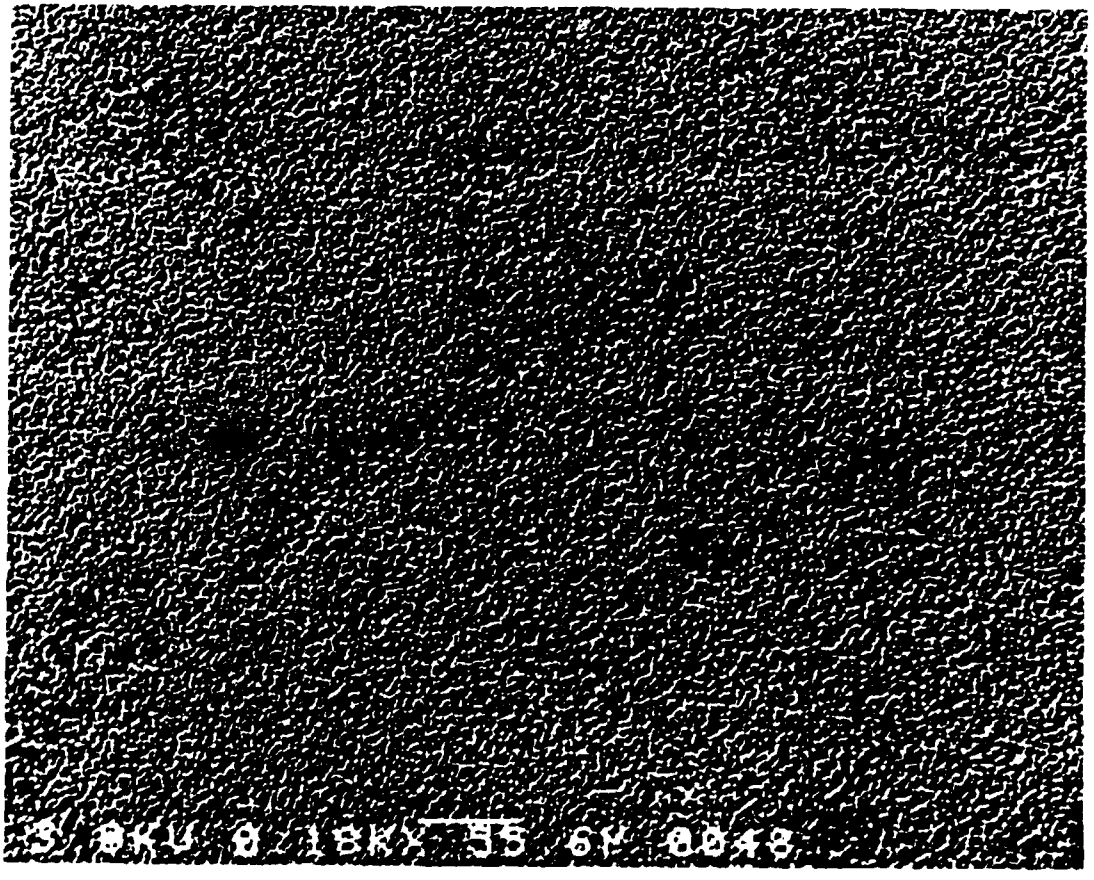


Figure IV-12. Dense Population of Randomly Spaced and Sized Pyramids in (100)-Oriented Silicon (Magnification - 180x).

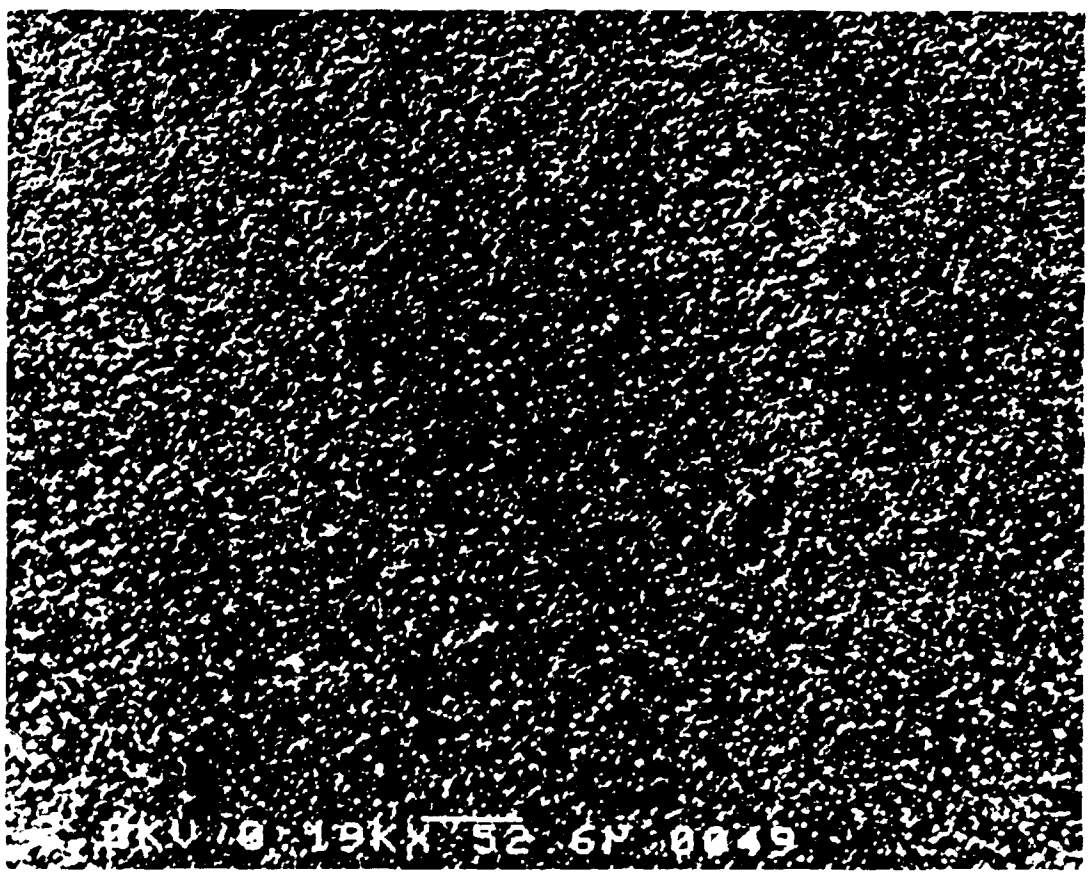


Figure IV-13. Moderate Population of Randomly Spaced and Sized Pyramids in (100)-Oriented Silicon (Magnification - 190x).

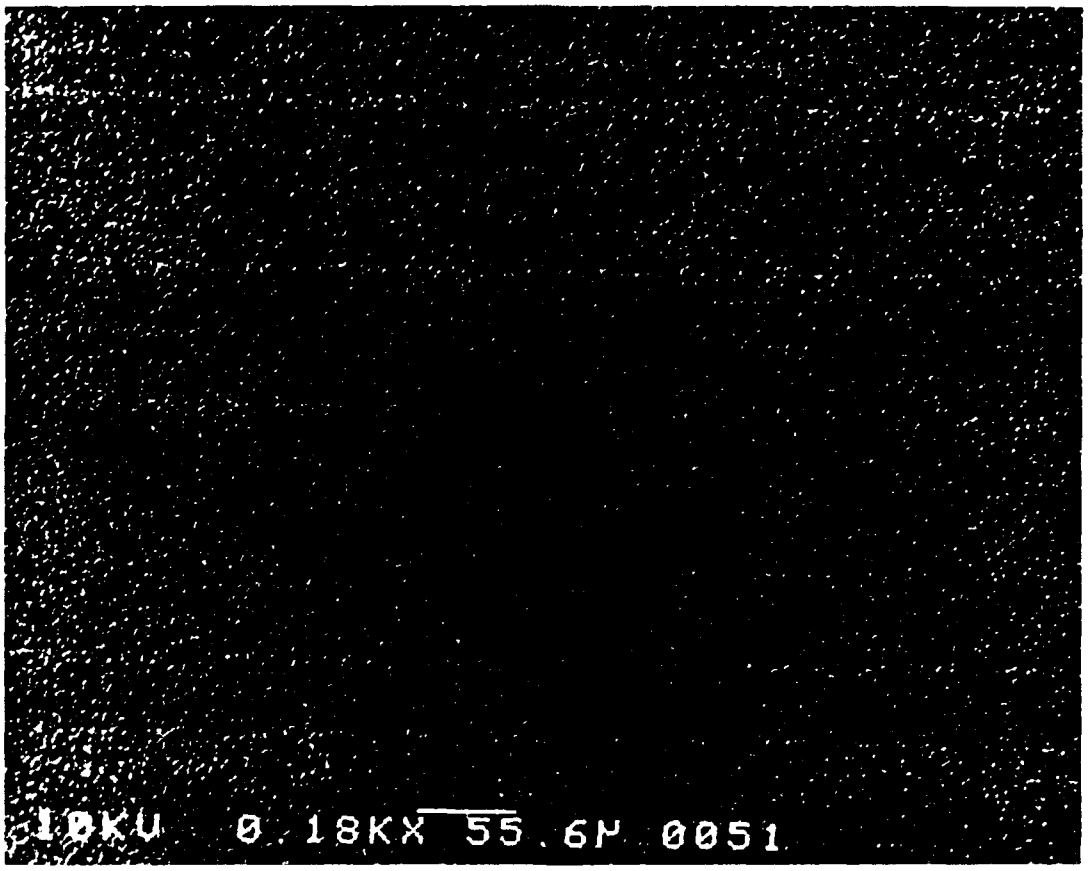


Figure IV-14. Sparse Population of Randomly Spaced and Sized Pyramids in (100)-Oriented Silicon (Magnification - 180x).

Figure IV-15. Dense Population of Randomly Spaced and Sized Pyramids in (100)-Oriented Silicon (Magnification - 1,420x).

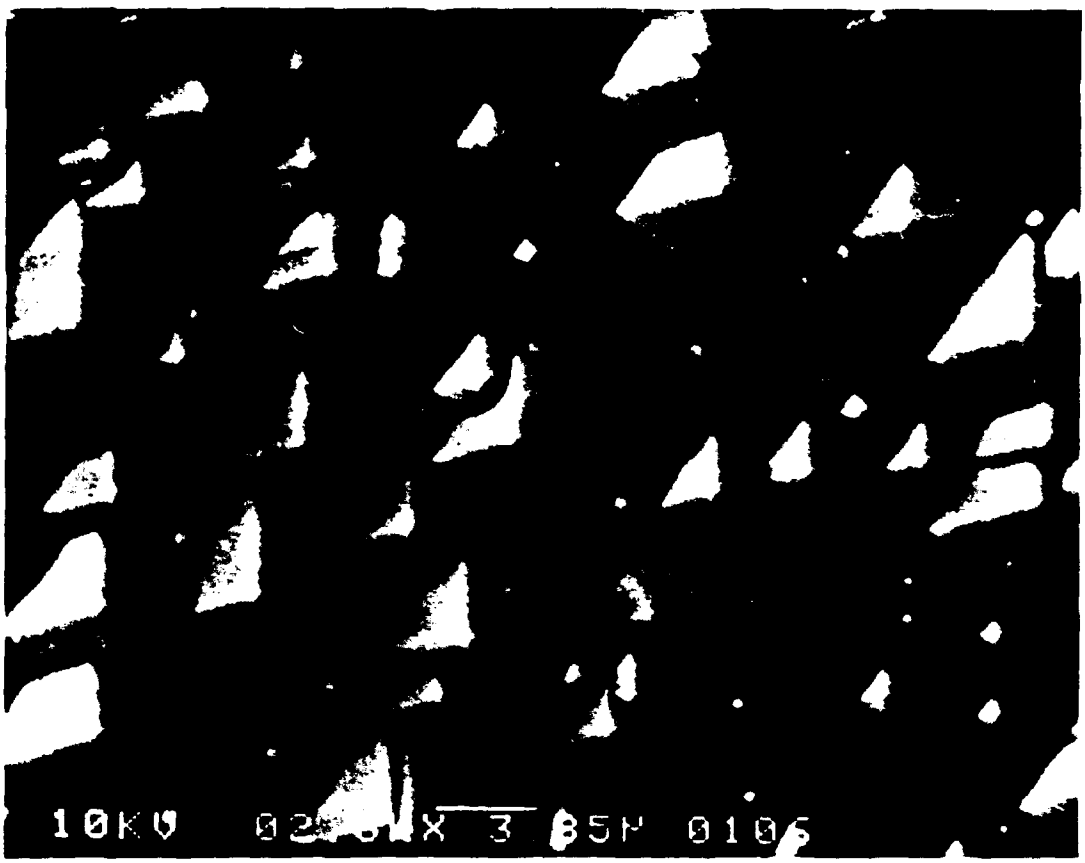


Figure IV-16. Moderate Population of Randomly Spaced and Sized Pyramids in (100)-Oriented Silicon (Magnification - 2,600x).

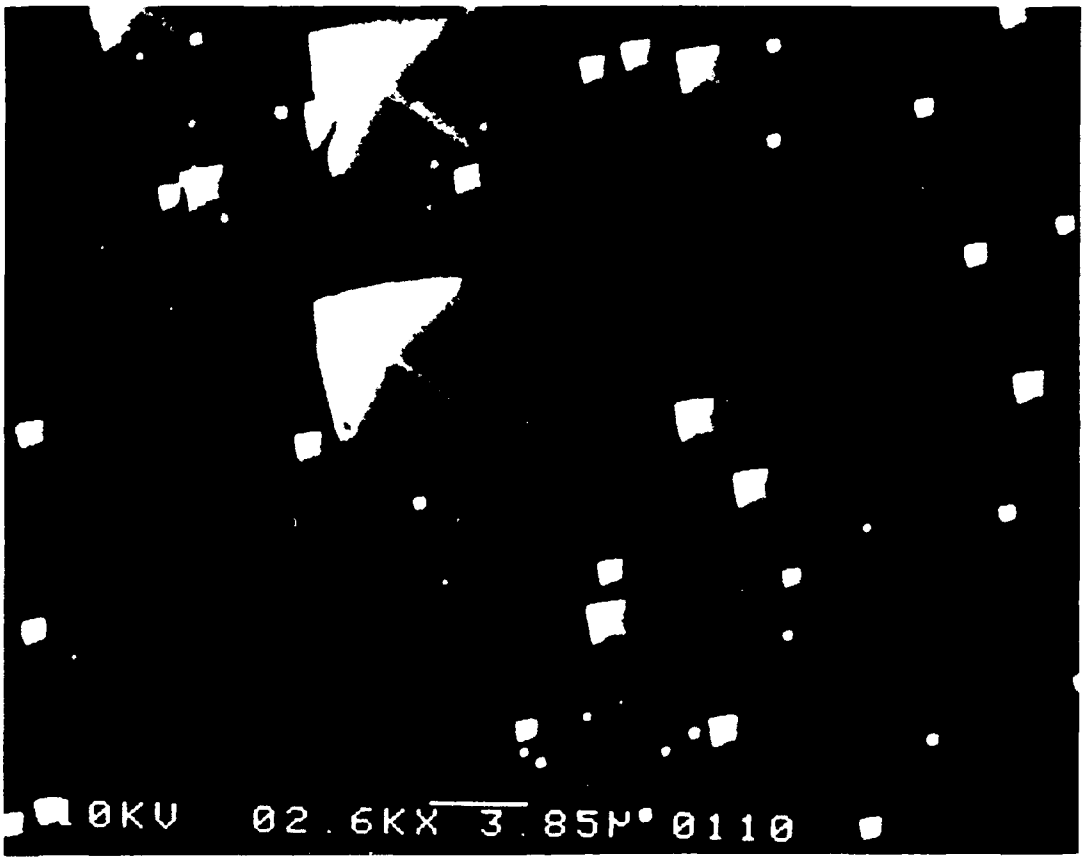


Figure IV-17. Sparse Population of Randomly Spaced and Sized Pyramids in (100)-Oriented Silicon (Magnification - 2,600x).

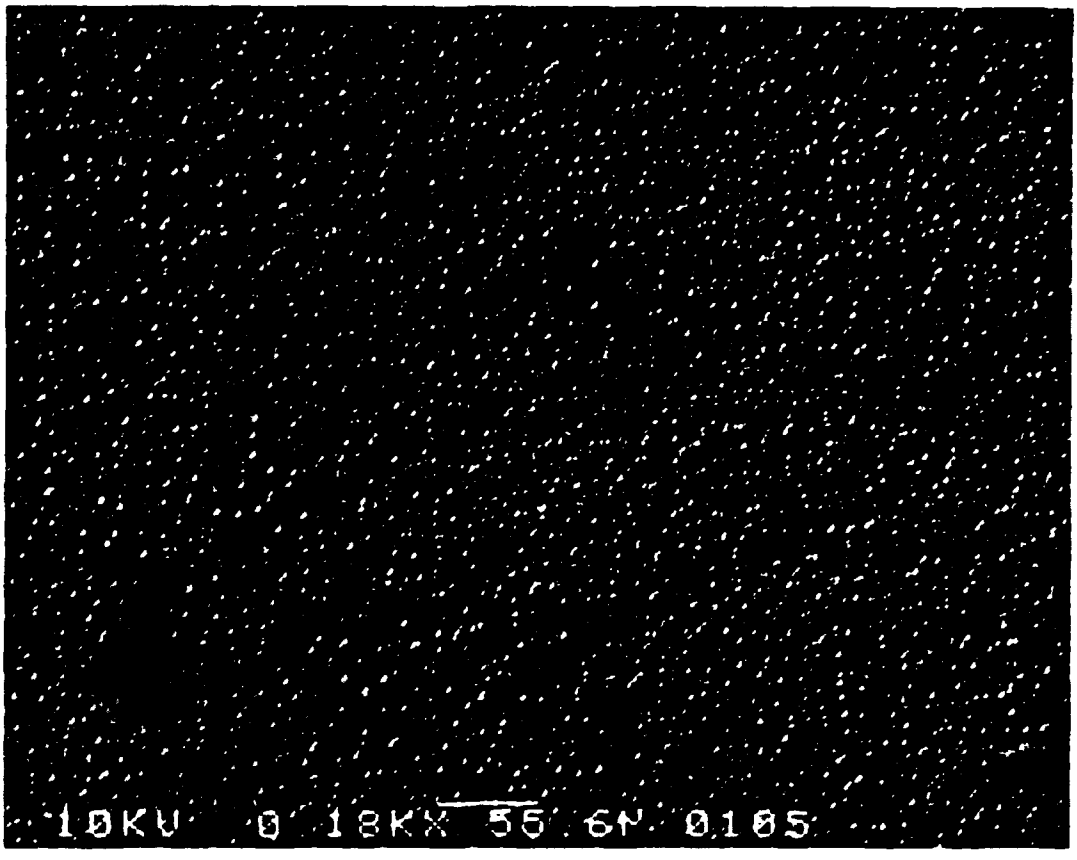


Figure IV-18. Dense Population of Randomly Spaced and Sized Pyramids in (100)-Oriented Silicon (Magnification - 180x).

Figure IV-19. Moderate Population of Randomly Spaced and Sized Pyramids in (100)-Oriented Silicon (Magnification - 180x).

Figure IV-20. Sparse Population of Randomly Spaced and Sized Pyramids in (100)-Oriented Silicon (Magnification - 180x).

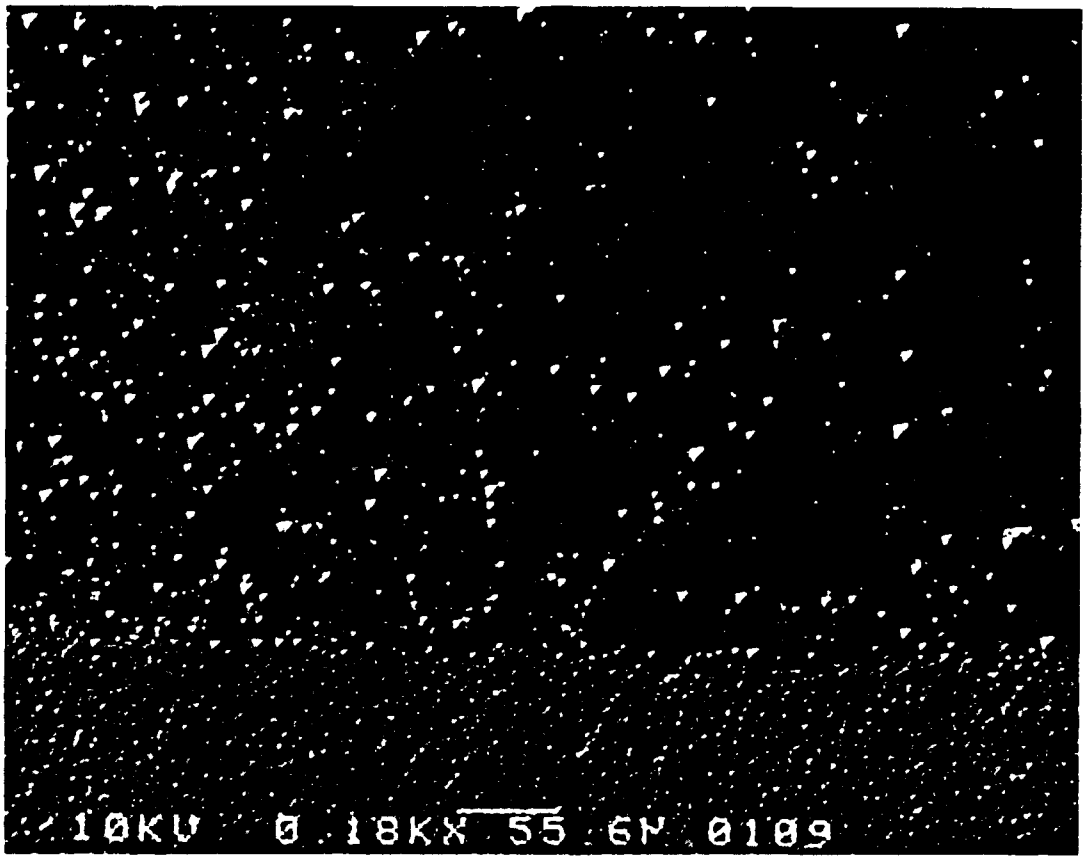


Figure IV-21. Adjacent Regions of Dense and Sparse Populations of Randomly Spaced and Sized Pyramids in (100)-Oriented Silicon (Magnification - 180x).

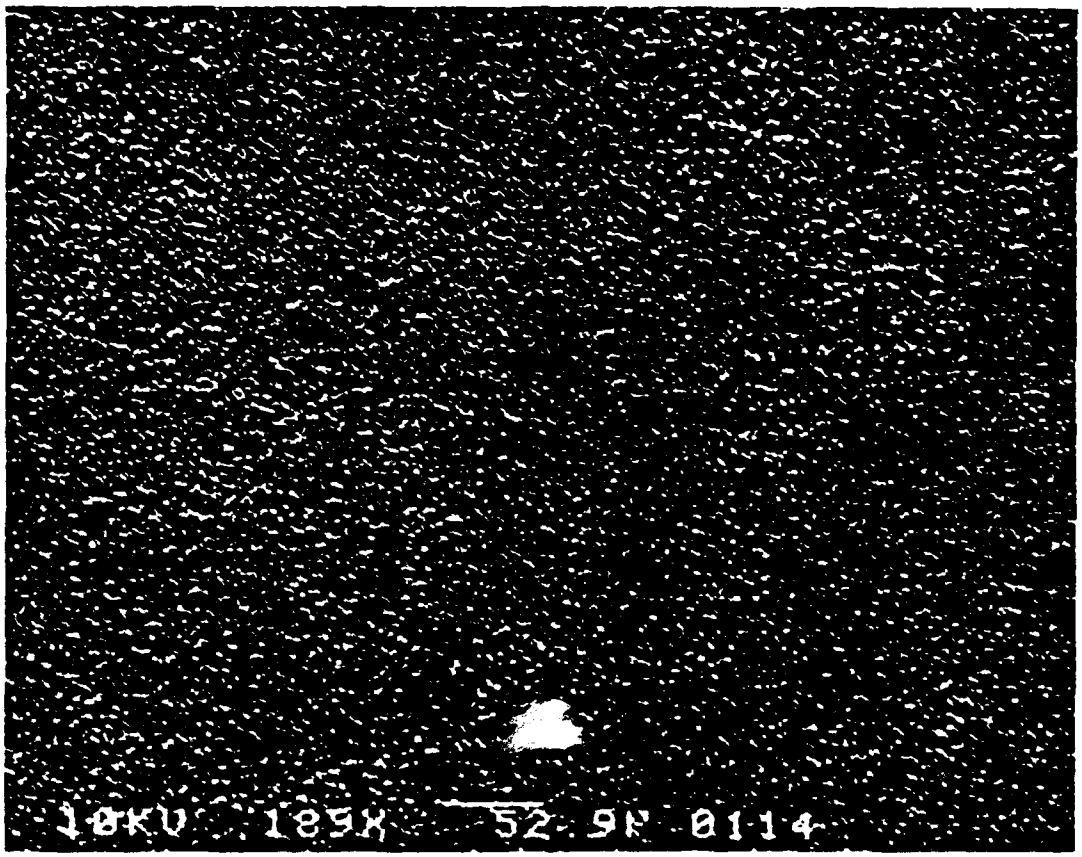


Figure IV-22. Extremely Dense Population of Randomly Spaced and Sized Pyramids in (100)-Oriented Silicon (Magnification - 189x).

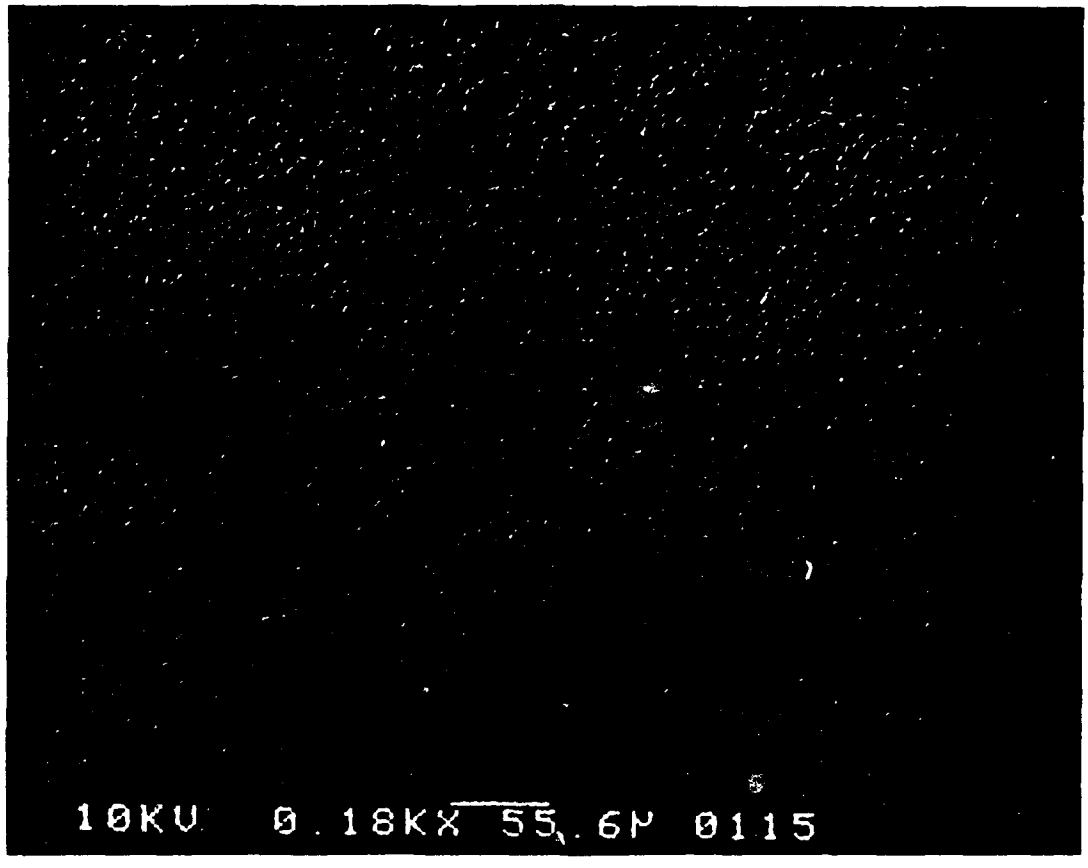


Figure IV-23. Extremely Dense Population of Randomly Spaced and Sized Pyramids in (100)-Oriented Silicon (Magnification - 180x).

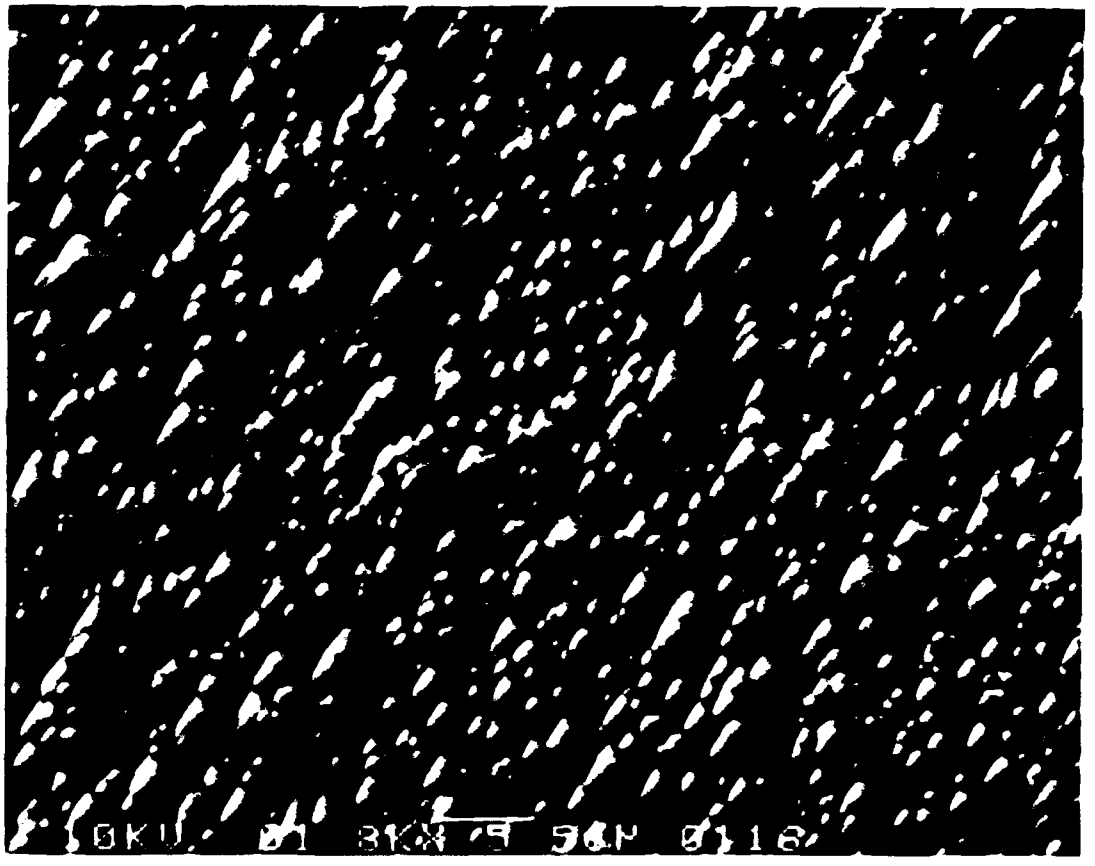


Figure IV-24. Extremely Dense Population of Randomly Spaced and Sized Pyramids in (100)-Oriented Silicon (Magnification - 1,800x).

Figure IV-25. Extremely Dense Population of Randomly Spaced and Sized Pyramids in (100)-Oriented Silicon (Magnification - 3,500x).

Figure IV-26. Extremely Dense Population of Randomly Spaced and Sized Pyramids in (100)-Oriented Silicon (Magnification - 7,000x).

4.4.2 Results of Micromachining the Deep Vertical-Wall Grooves (DVWGs). DVWG structures were successfully realized on several (110)-oriented, single-crystal, silicon wafers. However, there were small, defective regions among the three by three array pattern of squares containing the DVWGs on some of the silicon wafers. Under an optical microscope, defective DVWGs were also observed where the walls between adjoining grooves were missing along varying, microscopic lengths.

Figure IV-27 is a photograph of a (110)-oriented silicon wafer with the DVWGs micromachined on its frontside. Unfortunately, the mirror-like, polished silicon surface which was protected from the KOH etchant reflects the camera lens and surrounding features.

Figures IV-28 through IV-34 are SEM photomicrographs of silicon wafers hosting the DVWGs. Figure IV-28 depicts DVWGs with unsharp edges, showing that SiO_2 is still present on the top surface. Figure IV-29 exhibits one of the previously described microscopic defects in the upper right portion of the photograph--a nonuniform wall thickness along a length that is almost 300 microns. In some sections, varying lengths of the walls were missing entirely, but overall, the microscopic defects were sparsely scattered. Unfortunately, some of the best DVWG structures realized were broken in the N_2 bubbler after the SiO_2 was removed.

Figure IV-27. DVWGs Etched in a 3-Inch Diameter, (110)-Oriented Silicon Wafer (Magnification - 0.885x).

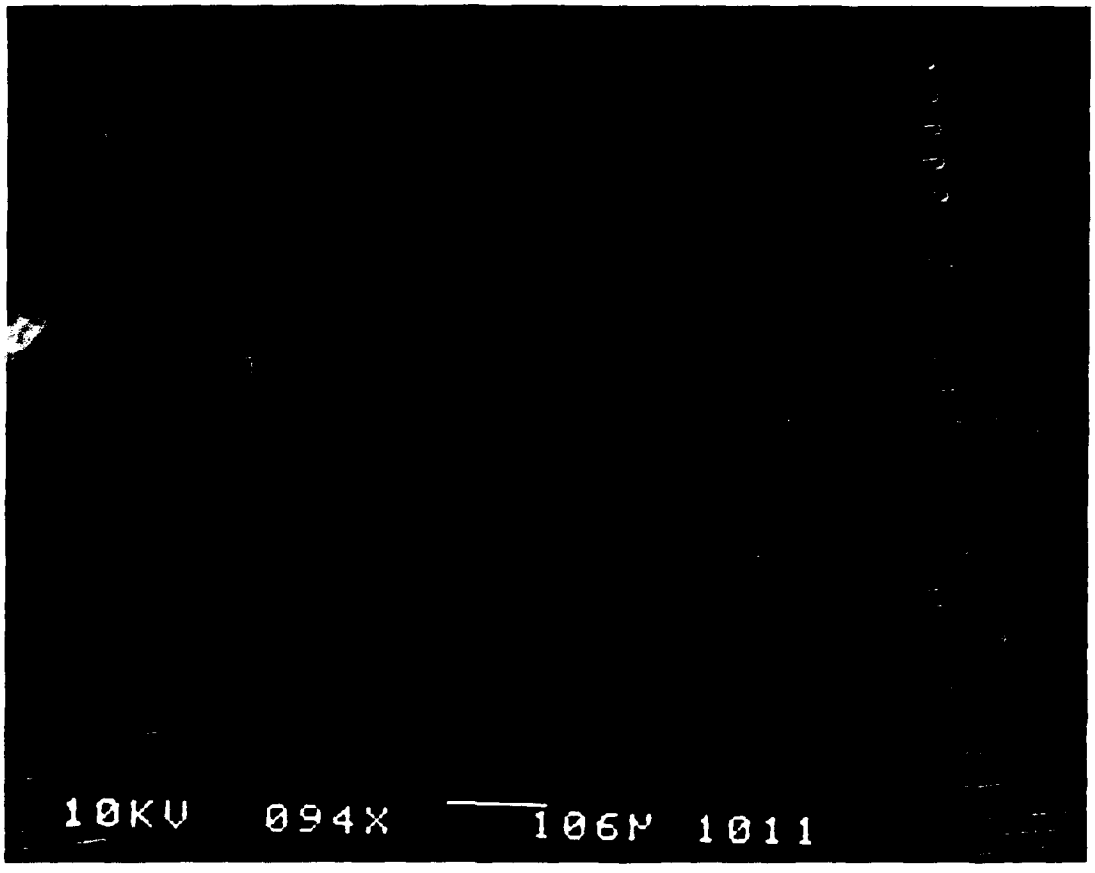


Figure IV-28. DVWGs Etched in (110)-Oriented Silicon (Magnification - 94x).

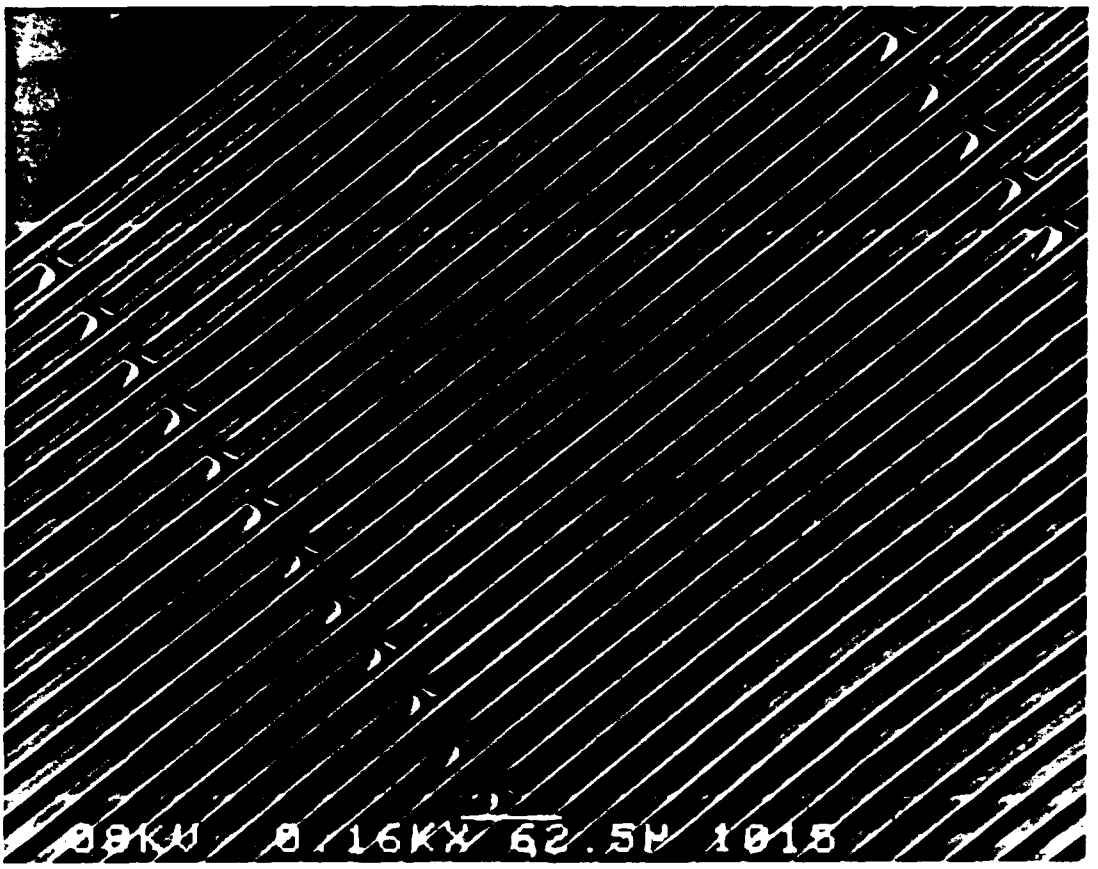


Figure IV-29. DVWGs Etched in (110)-Oriented Silicon (Magnification - 160x).

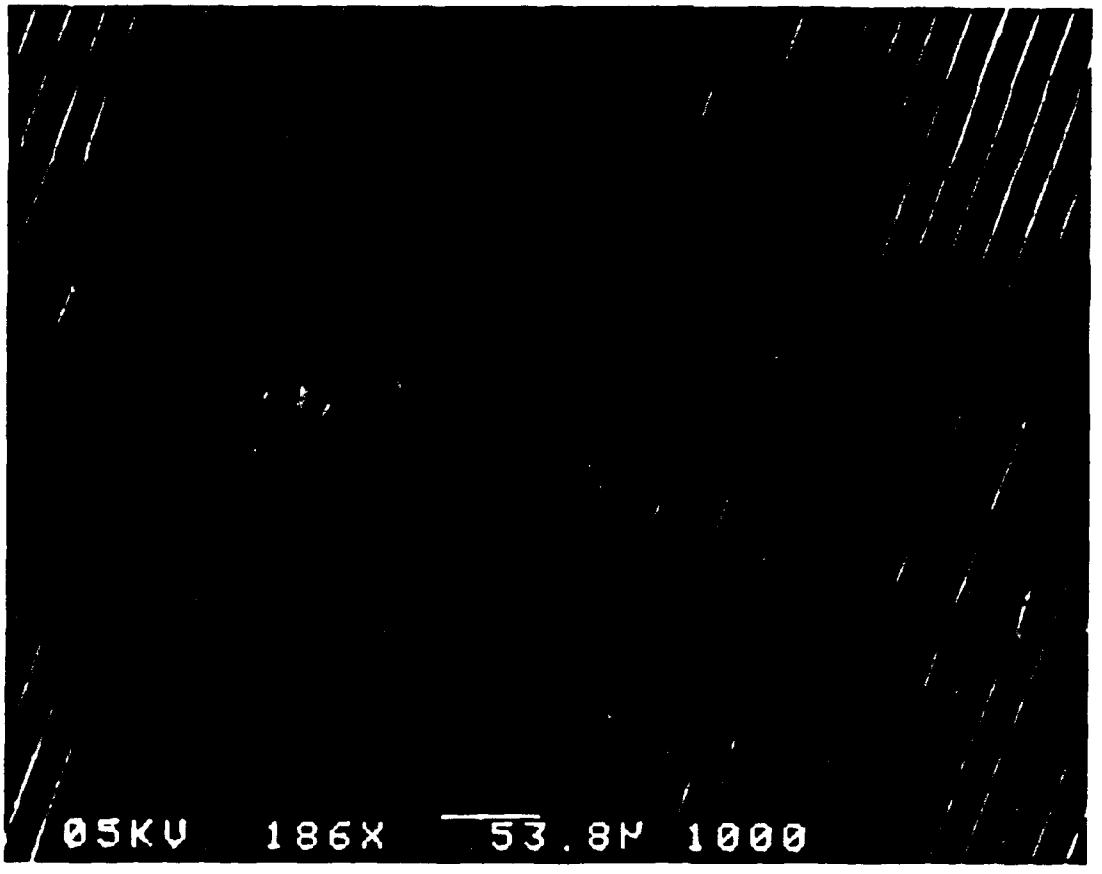


Figure IV-30. DVWGs Etched in (110)-Oriented Silicon (Magnification - 186x).

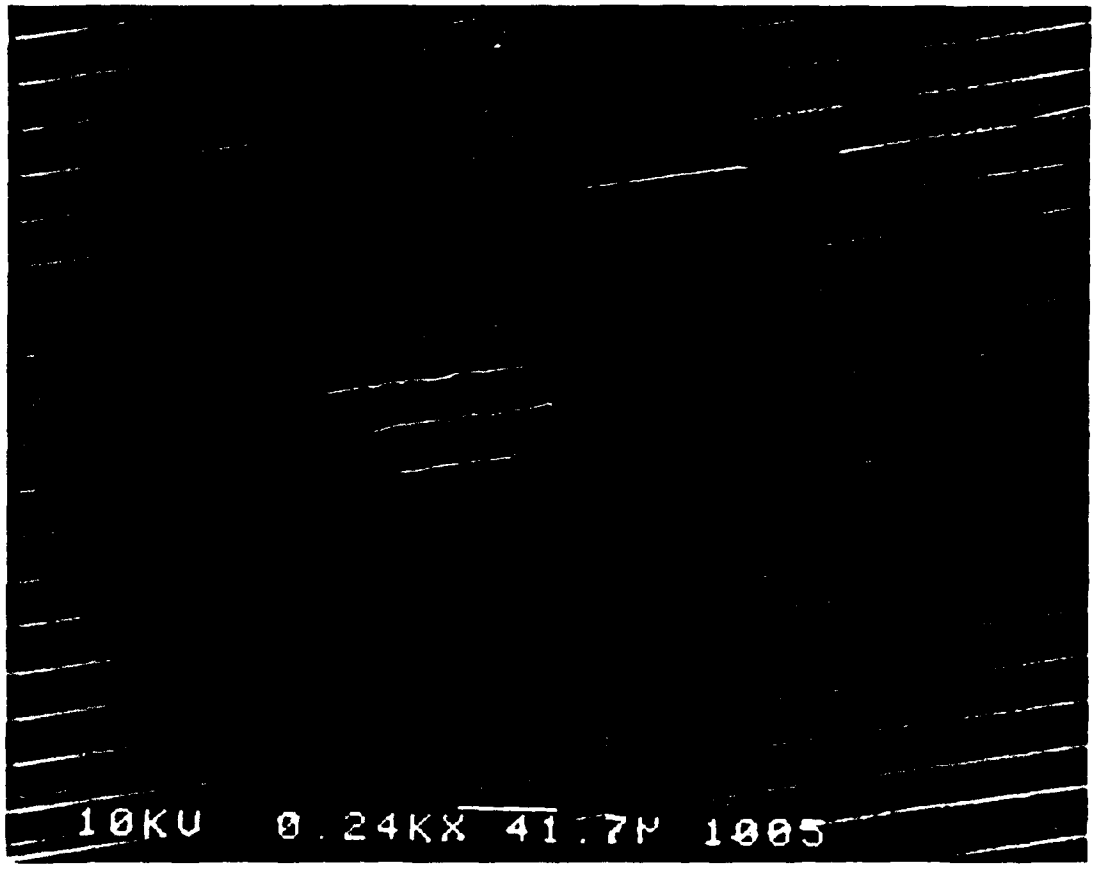


Figure IV-31. DVWGs Etched in (110)-Oriented Silicon (Magnification - 240x).

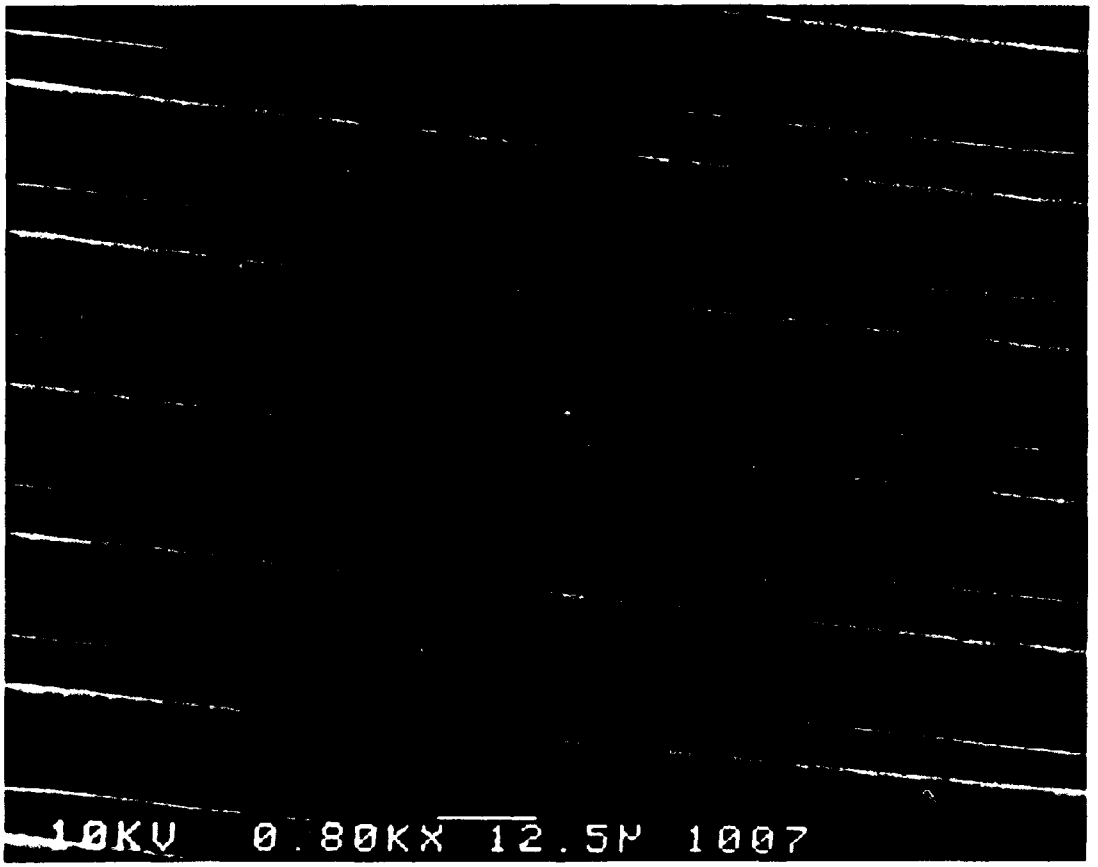


Figure IV-32. DVWGs Etched in (110)-Oriented Silicon (Magnification - 800x).

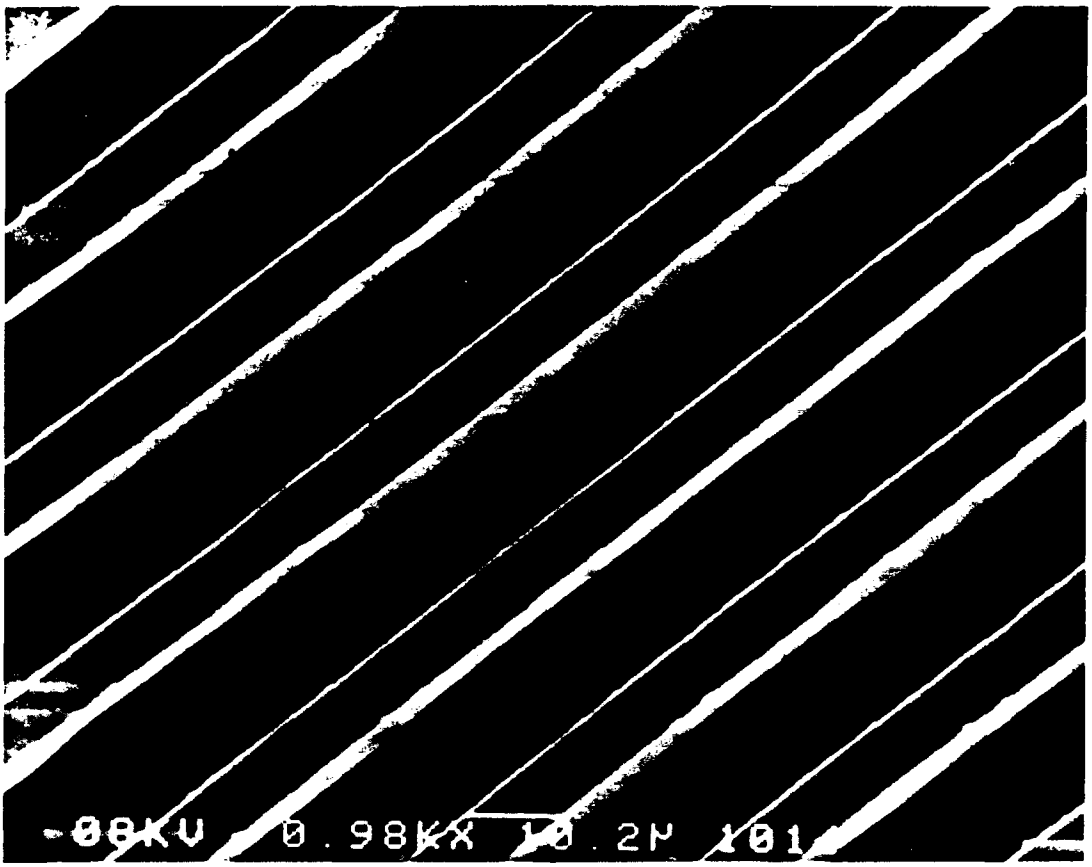


Figure IV-33. DVWGs Etched in (110)-Oriented Silicon (Magnification - 980x).

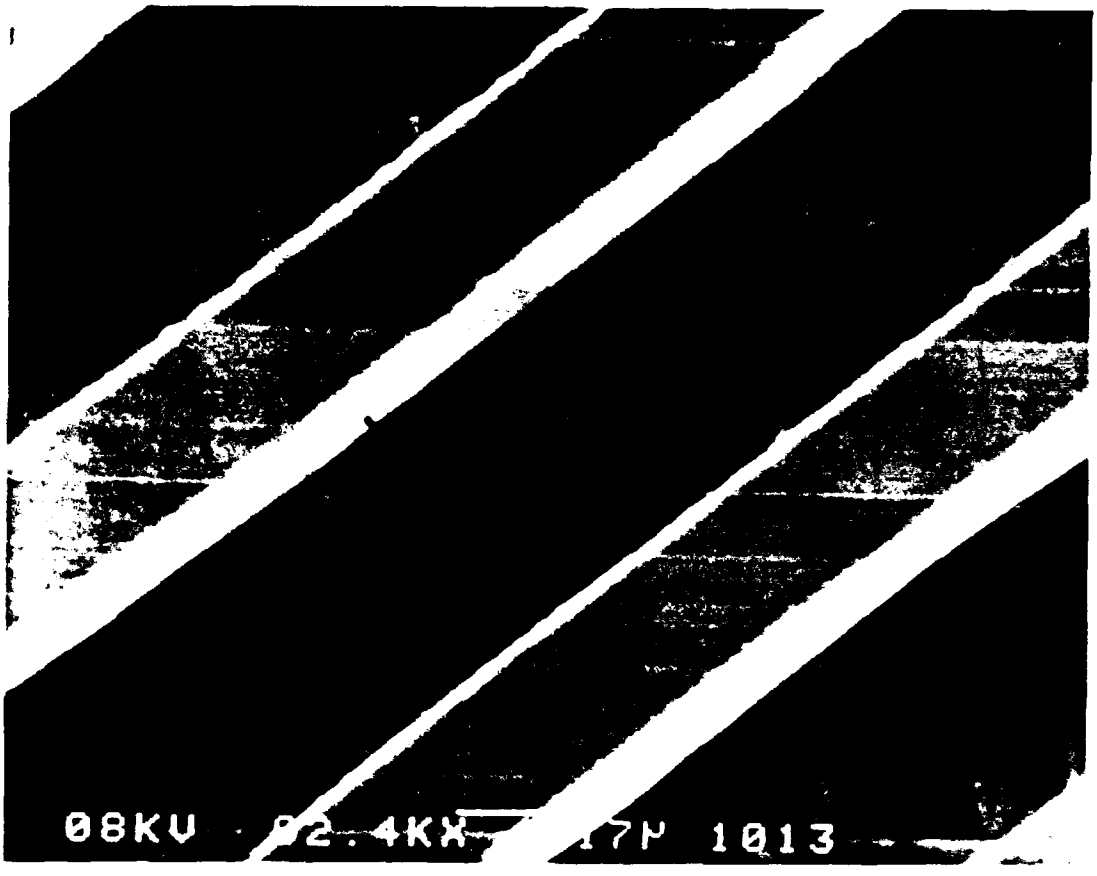


Figure IV-34. DVWGs Etched in (110)-Oriented Silicon (Magnification - 2,400x).

4.4.3 Results of Micromachining the Micro-Fluid Channel (MFC) Structures. The MFC structures were realized on several silicon wafers. Figure IV-35 is an SEM photomicrograph of a portion of the MFC structure, showing the fluid channels at one end of the design. The image was taken using the lowest magnification level of the SEM. Figure IV-36 shows the entire MFC structure.

Each MFC was etched to an average depth of 52 microns. When the 2-micron thick film of SiO_2 (etch mask) was removed in a 100% HF etchant, 50-micron deep MFCs were realized. Each MFC was approximately 100 microns wide, and they were separated from each other by 100 microns. There were sparsely populated defects in the MFC structure on some of the silicon wafers. These defects were primarily caused by the prior feed-through hole etch process.

On some of the MFC structures, the canal region from the MFCs connecting to the feed-through holes was not fully realized. That is, a 1-millimeter gap between the MFCs and the feed-throughs was not consistently etched in the SiO_2. Undeveloped photoresist may have protected the oxide from the HF etchant. During the initial photoresist application, the presence of the feed-throughs created a physical disturbance as the silicon wafers were spun, and the photoresist was not uniformly distributed near these holes. The remaining oxide near the feed-throughs would likely have

also protected the gap from the KOH etchant, and the resulting MFC structures would not have allowed fluid to pass through. The oxide had to be removed between the canal and the feed-throughs. Another oxide growth process was not possible. Since thermally grown silicon dioxide could not be realized uniformly on deviations from a flat surface on the silicon wafer (e.g., scratches in the surface, the edges touching the quartz crucible, the MFC, etc.), HF was directly applied with a small-diameter wire to a the region containing the unwanted SiO_2. As a result, the SiO_2 was successfully removed, although its removal was not precisely confined relative to the ideal pattern. Nevertheless, there were no negative effects which resulted from the manual application of HF to the silicon wafer relative to the operation of the MFC thermal module.

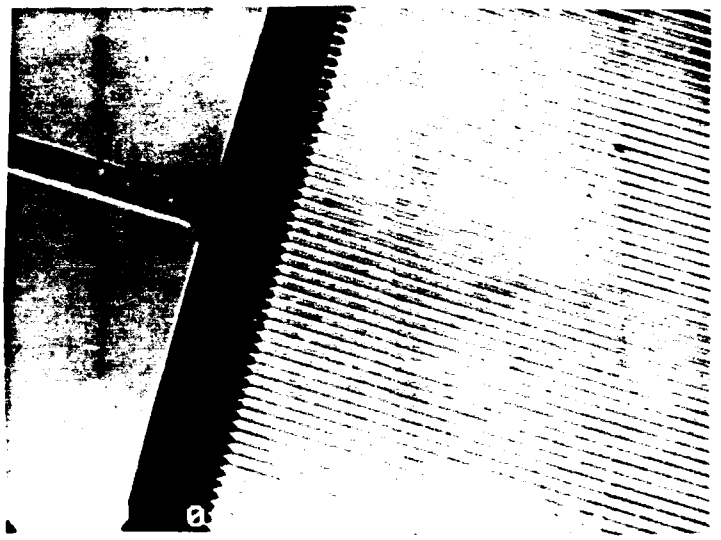


Figure IV-35. Micro-Fluid Channel (Magnification - 8.7x).

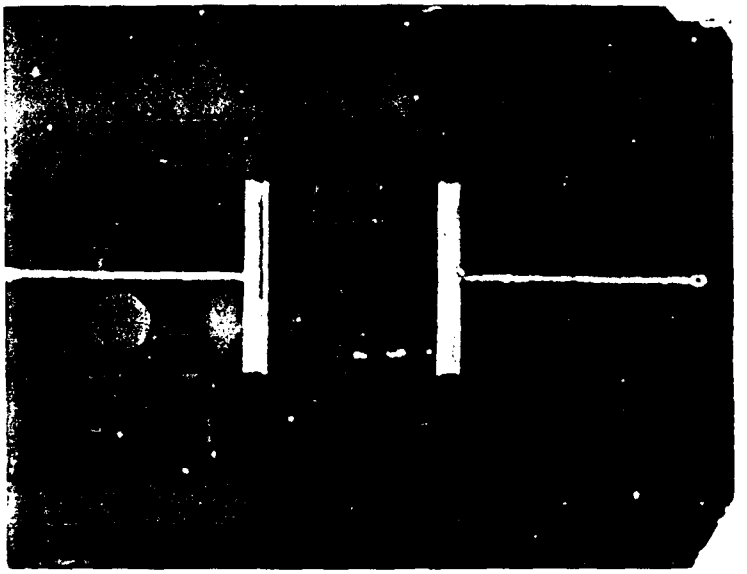


Figure IV-36. Micro-Fluid Channel (Magnification - 1.583x).

4.5 Results of the Design and Fabrication of the Diffused and Thin-Film Aluminum Resistors.

Two heat-dissipating devices were designed, fabricated, and realized. They included the diffused resistor design and the thin-film aluminum resistor variant.

4.5.1 Results of the Diffused Resistor Design and Fabrication. Forty-two IC die were received from MOSIS, Inc. The resistors were measured with microprobes and a multimeter. One of the seven resistors was measured on six of the IC die, and all seven resistors were measured on one of the IC die. The resistors were all 33 +/- 0.2 ohms.

The contact pads were intentionally designed to be sufficiently large, but the metal used by MOSIS, Inc. was apparently too thin to realize successful wire-bonding with gold wire. The specifications for the IC die dimensions were not sufficiently precise; that is, the IC die dimensions were slightly larger than expected, and they varied as discussed in Chapter III. Figure IV-37 is a photograph, provided by MOSIS, of the seven resistors on one of the IC die.

4.5.2 Results of the Thin-Film Metal (Aluminum) Resistor Fabrication. Four, thin-film aluminum resistors were realized on silicon wafers using the metallization lift-off technique. The four resistors described in Section 4.3 functioned as designed. The thickness of the aluminum deposited on the silicon wafers varied with the distance from the evaporation source (Al). Three aluminum step heights, measured within 2-3 millimeters of each other on wafer #M-1, using the stylus profilometer, were 1,829, 1,689, and 1,541 angstroms. On one silicon wafer, the aluminum thickness varied several hundreds of angstroms; within a batch of four wafers, the aluminum thickness varied by more than a thousand angstroms.

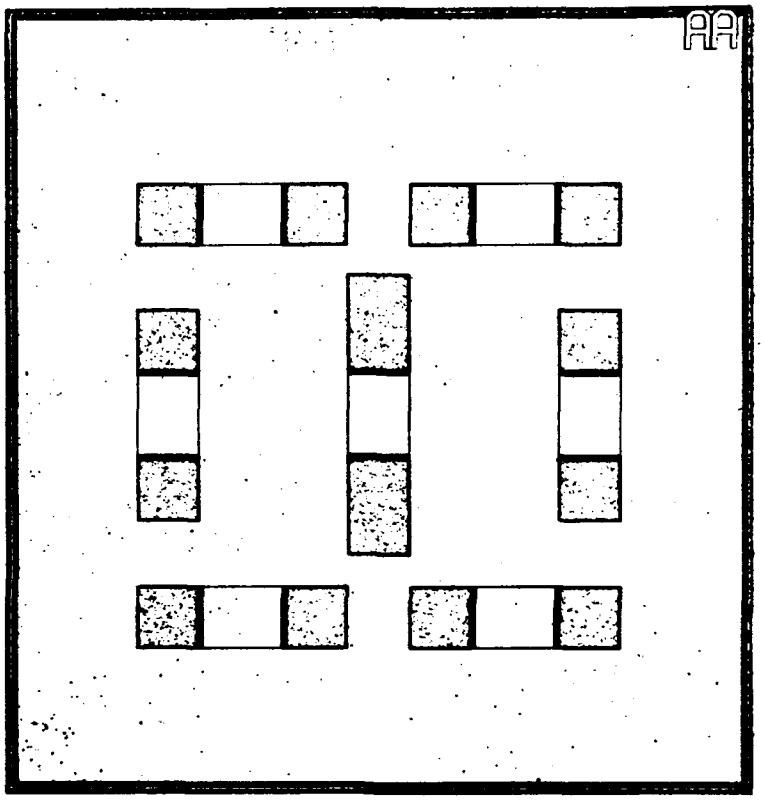


Figure IV-37. Seven Diffused Resistors on the IC Die Fabricated by MOSIS, Inc.

4.6 Results of the Silicon Wafer Sandwich Thermal Module Construction

The silicon wafer thermal modules described in Section 3.6 were constructed to provide a comparative and experimental basis for the subsequent thermal analyses. The epoxy process described in Chapter III was adopted to provide a uniform thickness among the modules. Figure IV-38 depicts a photograph of a silicon wafer with a strip of epoxy spread along its diameter. The epoxy was viscous and cohesive, and excellent results required numerous passes with the glass microscope slide applicator. Many times, re-applications of the epoxy were necessary. The thickness of the epoxy strip in Figure IV-37 varied less than 3 microns along its length as measured with a stylus profilometer. The epoxy cured well, and it provided strong adhesion between the pairs of silicon wafers. On test pairs of silicon wafers, the wafers could not be separated without destroying them. The silicon wafers could only be pried apart in tiny, grain-sized fragments.

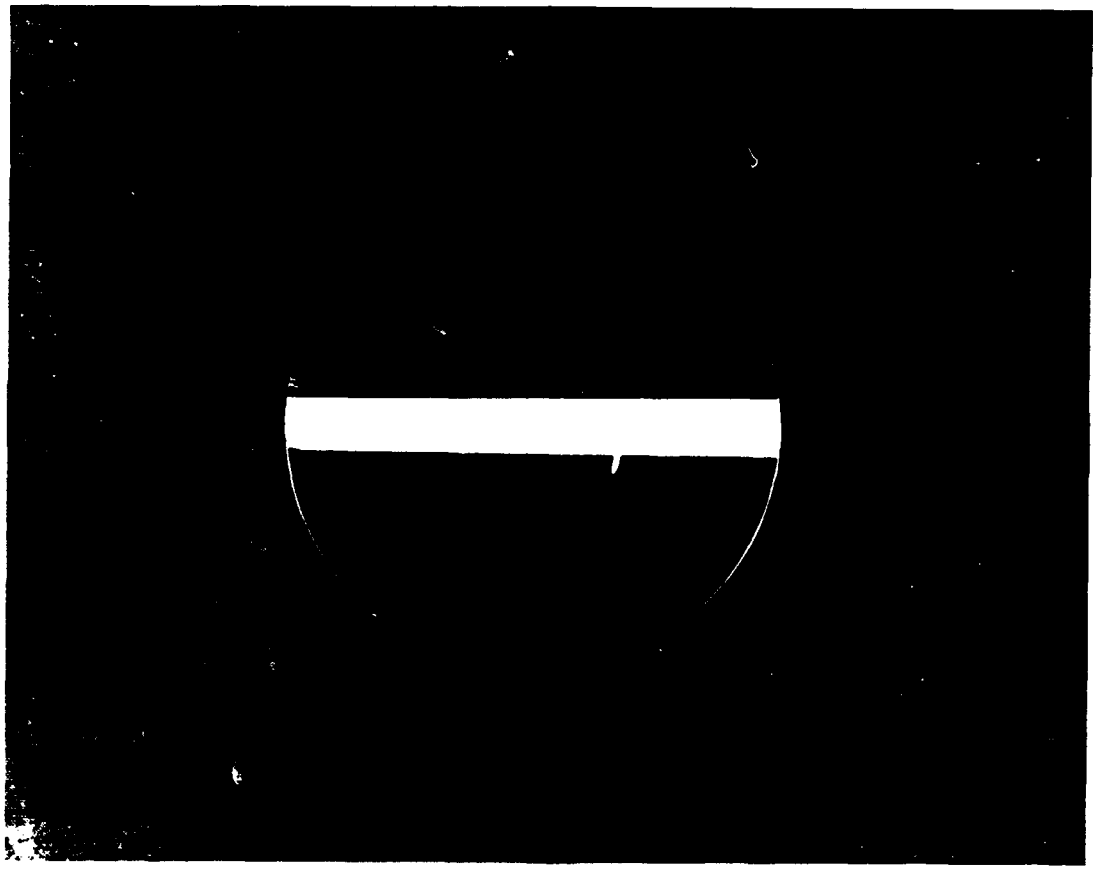


Figure IV-38. Strip of Epoxy Spread on a Silicon Wafer.

Figure IV-39 illustrates the heat flow in the thermal modules, showing the heat emanating from the heat-producing devices, through the silicon wafer thermal modules, to the heat-dissipating silicon micromachined surfaces. Figure IV-39 also illustrates the difference between the heat migration in the thermal modules hosting the IC die and the thermal modules hosting the thin-film aluminum resistors. The IC die host modules likely have a more efficient heat flow path to the micromachined surfaces. The diffused resistors are embedded in the IC die and have an over-glass coating (SiO_2) covering the entire surface of the IC die, which acts to impede the thermal dissipation from its top surface. Also, the IC die are mounted and attached with the thermally conductive epoxy.

In contrast, the thin-film aluminum resistors lie on top of an approximately 1-micron thick film of SiO_2. This thin-film of SiO_2, and the subsequent layer of silicon, provide a more substantial thermal resistance to the heat-dissipating micromachined surface in these thermal modules. Also, the aluminum is not insulated on its top surface from the convective, ambient atmosphere. These factors may have adversely affected the thermal analysis relative to the comparison of the thin-film aluminum resistor thermal modules, specifically; the reference wafer versus the DVWGs.

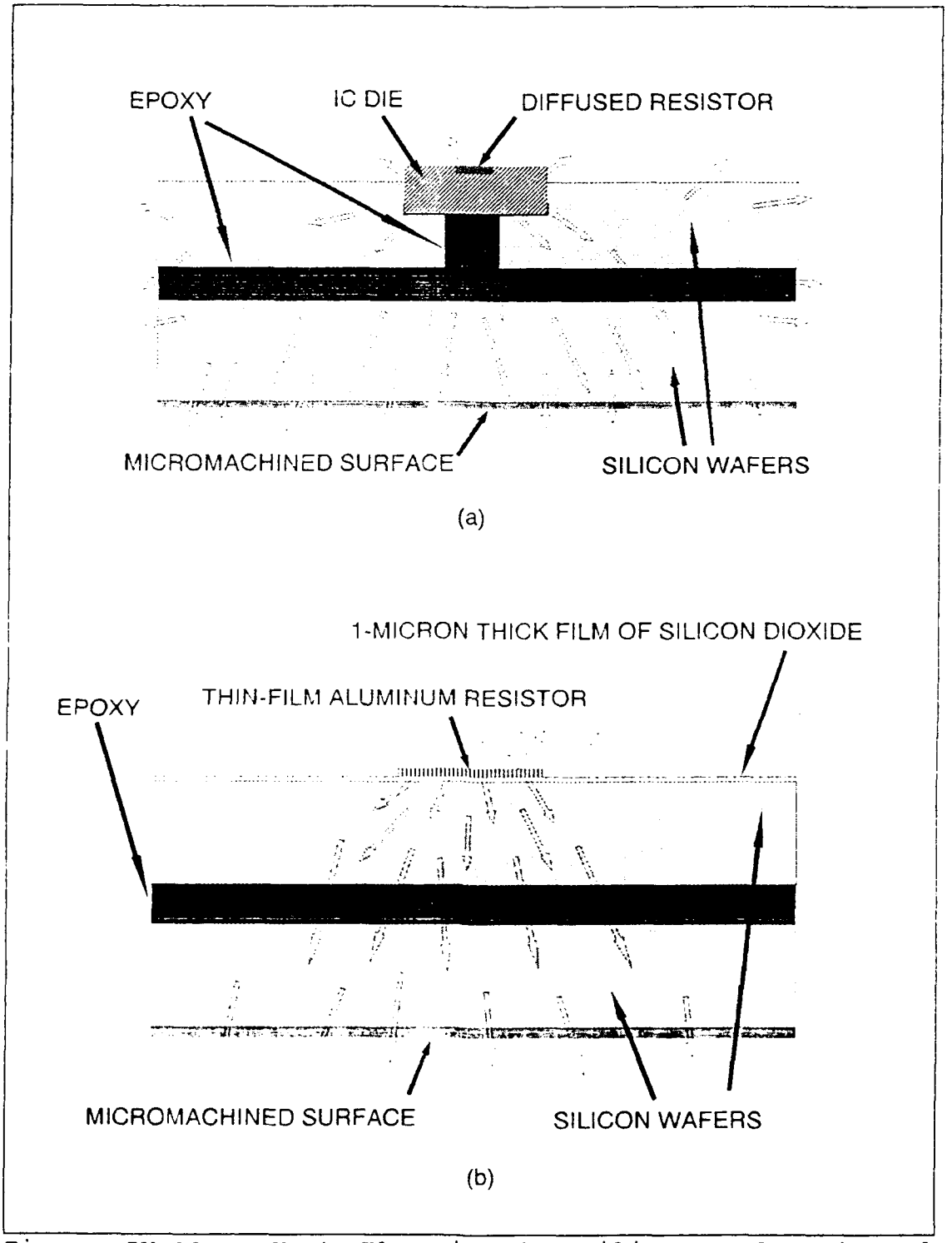


Figure IV-39. Heat Flow in the Silicon Wafer Thermal Modules: (a) IC Die Host Module, and (b) Thin-film Aluminum Host Module.

4.6.1 Results of the Thin-Film Aluminum Resistor Thermal Module Fabrication. The fabrication of these modules was realized as designed. However, there were only four practical positions for recording temperatures with the array. The way the thermal modules were electrically connected limited the surface area of the silicon wafer that was available compared to the size of the thermocouple array, and along with the dimensional constraints of the thermocouple jig, were the critical factors used to determine the four measurement positions. Nevertheless, the four measurement positions were determined to be adequate. Since these thermal modules were the first to be thermally analyzed, the same positions were used in the subsequent thermocouple measurements on the remainder of the modules. However, the temperatures of the thermal modules hosting the four IC die and the MFC thermal modules were only measured in one position--with the thermocouple array centered on the heat-producing device arrangement.

4.6.2 Results of the IC Die Mounting. The IC die were securely epoxied into the die-recess holes in the host silicon wafers. The process used to mount the IC die did not reveal any negative results.

4.6.3 Results of the IC Die Resistor Thermal Module Fabrication. These thermal modules were successfully fabricated. There was a variation in their fabrication from the technique used with the thin-film resistor modules. Pressure was not applied over the entire surface to uniformly distribute the epoxy. Pressure was only applied to the edges of the IC die. This variation was used to preserve the delicate wire-bonds.

4.6.4 Results of the Micro-Fluid Channel Thermal Module Fabrication. These thermal modules were fabricated by electrostatically bonding the silicon wafers hosting the micro-fluid channels to Pyrex glass plates (McMaster-Carr Supply Company, Chicago, IL 60680-4355). The Pyrex glass sealed the micro-fluid channels. Successful bonds between the Pyrex glass and the silicon wafers were realized after 10 to 24 hours at 150 °C with applied dc potentials (Figure IV-40) spanning 1,400 to more than 1,600 volts (Tektronix, Inc., curve tracer and power supply, model 577, Beaverton, OR 97077). The electrostatically bonded wafer-glass sandwich was then epoxy-bonded to the IC die and thin-film resistor host silicon wafers with the thermally conductive epoxy.

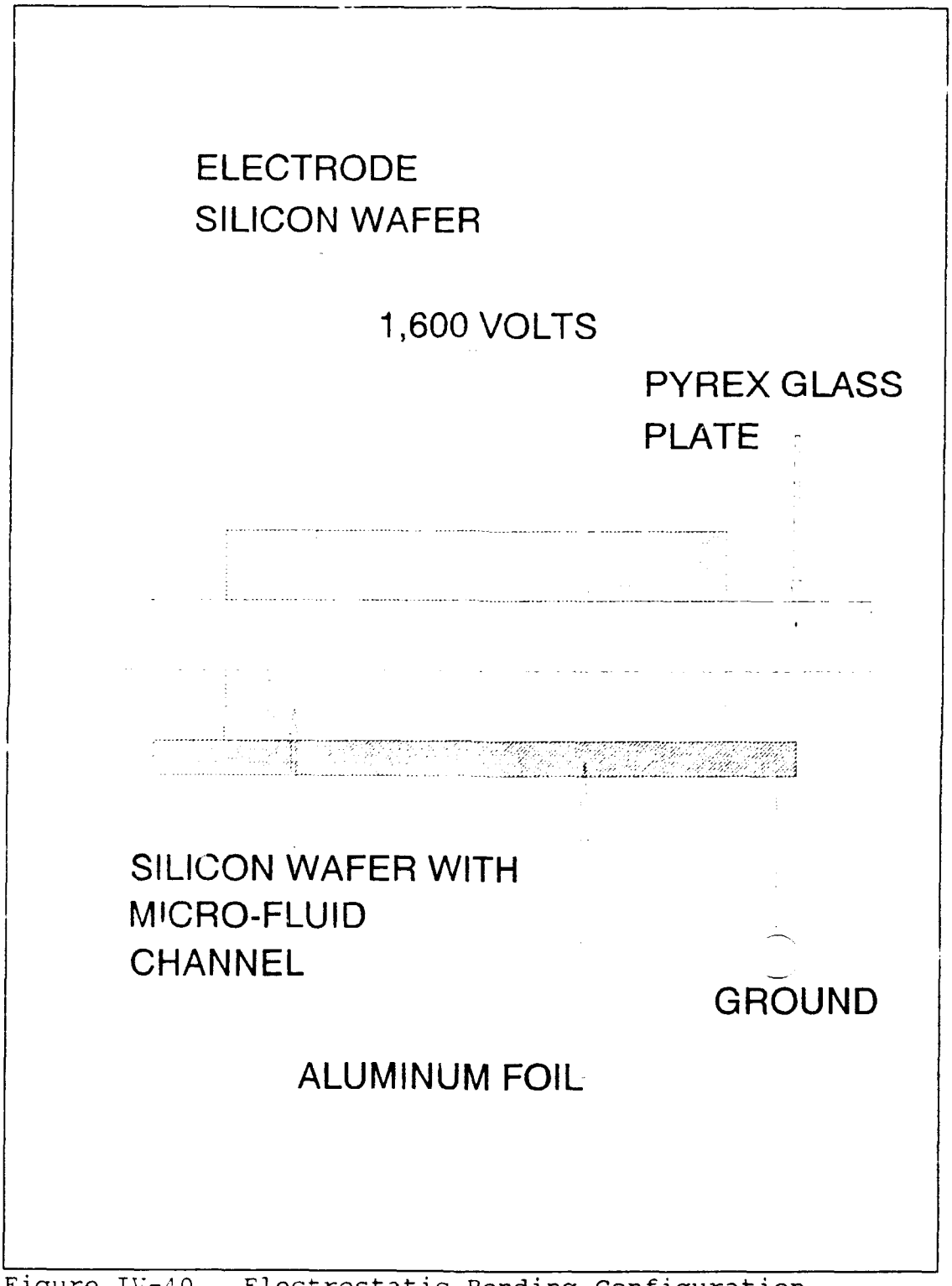


Figure IV-40. Electrostatic-Bonding Configuration.

4.7 Results of the Thermal Analysis

Extra temperature readings were recorded on the thermal modules hosting the thin-film aluminum resistors, because during the preliminary testing, these resistors were determined to be capable of handling significantly larger power dissipation levels.

4.7.1 Results of the Temperature Measurements.

Originally, the thermocouple jig was designed with low pressure springs to independently support the individual thermocouples. A matched set of sufficiently low pressure springs were not readily available, and the springs fabricated by the AFIT Model Shop did not function as intended. Fortunately, the thermocouple array and jig arrangement functioned well without the springs, which were subsequently discarded. The the thermocouple jig's micro-adjustments did not have sufficient range to traverse the entire surface of the thermal modules; however, the coarse adjustments were adequate. The number of revolutions of the thumbwheel on the coarse adjustments was used to reposition the thermocouple array.

The tips of the thermocouples were not optimally oriented because they were welded to the thermocouple handle by the vendor. Their lengths also varied, and their angle of projection with respect to the handle varied. Some of

the thermocouple tips were off-center by nearly 2-3 millimeters. The thermocouples were actually designed for hand-held positioning and operation.

Table IV-1 represents the format used to record the results of the temperature measurement experiments. This computer output file (entitled TEST) represents the measured data for an actual trial involving a thin-film aluminum resistor thermal module at room temperature. Several of these tests were performed to determine the variance in the thermocouple readings and the associated test equipment or the variation in the room temperature. The first column depicts the array position number, the second column is the thermocouple position number within the array, the third column is the voltage measured by the thermocouple, and the fourth column is the converted temperature in °C. The upper left thermocouple is numbered '1', and the numbering proceeds downward and to the right. Figure IV-41 depicts the thermocouple position numbering scheme as viewed looking at the array itself. Thermocouple number five was always centered on the thin-film aluminum resistor and the IC die in array position number one. This position was the reference point relative to the other positions.

The temperature of the silicon wafer thermal module is approximately 23 °C, according to the results in the TEST file (Table IV-1). The temperature range during the first

reading spanned 22.8 to 23.0 °C. Three significant figures were used to analyze the data. The remaining numerical digits were arbitrarily appended by the electrometer, and they are not valid data. Measurements were taken at array position number four twice to verify that the erroneous result in array position four, thermocouple position eight, was an equipment malfunction and not due to a broken thermocouple wire (the thermocouple wires were very delicate). Approximately one hour was required to successfully connect the thermocouple wires to the scanner card. Each time the scanner card was removed and reinserted, one or two wires were subsequently found to be broken.

When the temperatures were measured after the support equipment (primarily, the power supply) had been off for an extended period of time, the ambient temperature (the starting temperature for each module) was approximately 23 °C. The starting temperature was generally 2 to 3 °C higher for measurements taken after the support equipment had been operating for an extended period of time. The surrounding air was warmed by the equipment and the thermocouple jig was warmed as heat was conducted from the thermal modules into the jig.

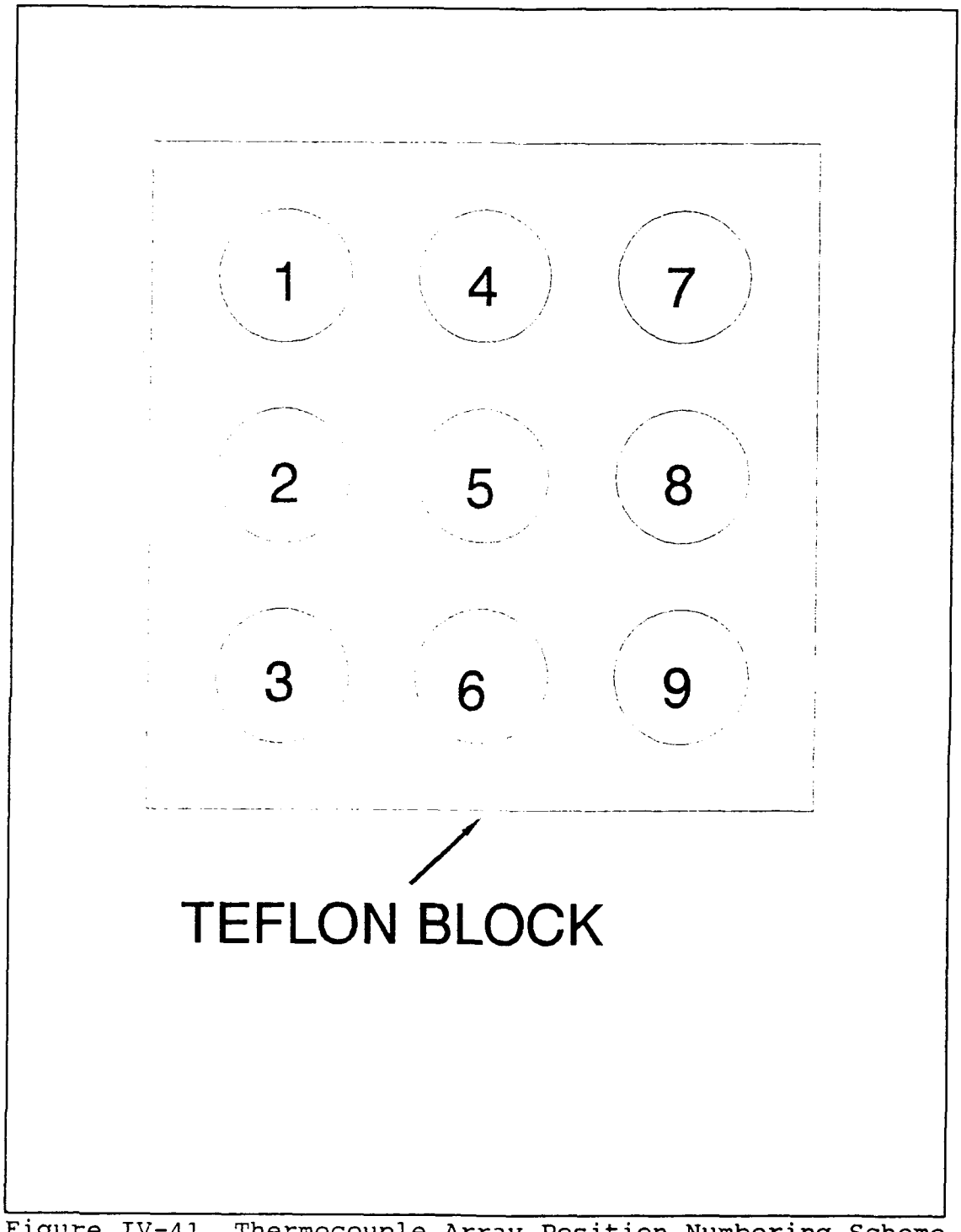


Figure IV-41. Thermocouple Array Position Numbering Scheme as Viewed Looking at the Array Itself.

Table IV-1. Thermocouple Voltage Measurements and Converted Temperatures.

Date = Wed.9-25 Filename = TEST Module Number = MOD1
Input Current = 0.0 A; Input Voltage = 0.0 V; Input Power = 0.0 W

1	1	-4.60000010207295E-0005	2.28813304901123E+0001
1	2	-4.89999983983580E-0005	2.28075637817383E+0001
1	3	-4.40000003436580E-0005	2.29305000305176E+0001
1	4	-4.40000003436580E-0005	2.29305000305176E+0001
1	5	-4.50000006821938E-0005	2.29059143066406E+0001
1	6	-4.09999993280508E-0005	2.30042476654053E+0001
1	7	-3.99999989895150E-0005	2.30288276672363E+0001
1	8	-4.09999993280508E-0005	2.30042476654053E+0001
1	9	-4.40000003436580E-0005	2.29305000305176E+0001
2	1	-4.40000003436580E-0005	2.29305000305176E+0001
2	2	-4.30000000051223E-0005	2.29550838470459E+0001
2	3	-4.40000003436580E-0005	2.29305000305176E+0001
2	4	-4.40000003436580E-0005	2.29305000305176E+0001
2	5	-4.70000013592653E-0005	2.28567409515381E+0001
2	6	-4.30000000051223E-0005	2.29550838470459E+0001
2	7	-4.19999996665865E-0005	2.29796657562256E+0001
2	8	-4.50000006821938E-0005	2.29059143066406E+0001
2	9	-4.50000006821938E-0005	2.29059143066406E+0001
3	1	-4.50000006821938E-0005	2.29059143066406E+0001
3	2	-4.40000003436580E-0005	2.29305000305176E+0001
3	3	-4.60000010207295E-0005	2.28813304901123E+0001
3	4	-4.30000000051223E-0005	2.29550838470459E+0001
3	5	-4.30000000051223E-0005	2.29550838470459E+0001
3	6	-4.40000003436580E-0005	2.29305000305176E+0001
3	7	-4.19999996665865E-0005	2.29796657562256E+0001
3	8	-4.09999993280508E-0005	2.30042476654053E+0001
3	9	-4.40000003436580E-0005	2.29305000305176E+0001
4	1	-5.19999994139653E-0005	2.27337894439697E+0001
4	2	-5.60000007681083E-0005	2.26354064941406E+0001
4	3	-5.50000004295725E-0005	2.26600055694580E+0001
4	4	-5.50000004295725E-0005	2.26600055694580E+0001
4	5	-5.60000007681083E-0005	2.26354064941406E+0001
4	6	-5.50000004295725E-0005	2.26600055694580E+0001
4	7	-5.99999984842725E-0005	2.25370063781738E+0001
4	8	-1.96659993380308E-0002	-8.85705688476563E+0002
4	9	-6.19999991613440E-0005	2.24878025054932E+0001

The experimental data is condensed and tabulated in Tables IV-2, IV-3, and IV-4. The numbers in the first column indicate the power dissipated in the heat-producing device. This power was calculated using the V·I product, where the current (I) was measured with an ammeter positioned in series with the power supply and the thermal module, and the voltage (V) was measured across a specific resistor with a voltmeter. The appropriate current was passed through each resistor to realize the same power dissipation among the heat-producing devices, particularly since the resistance values of the thin-film aluminum resistors varied.

The second column in Tables IV-2, IV-3, and IV-4 lists the temperatures measured by the thermocouple in direct contact with the heat-producing device(s). On the thermal modules with a single device, these temperatures were recorded with thermocouple #5 in array position #1. On the thermal modules with four devices, these temperatures represent the average of the four temperatures recorded by the thermocouples in direct contact with the four devices (thermocouples #1, #3, #7, and #9 in array position #1).

The last four columns depict the averages of the eight or nine thermocouple readings in array positions #1, #2, #3, and #4 for the prescribed power outputs. The values in the column labeled 'Pos1' are averages of the eight thermocouple

readings (excluding thermocouple #5) surrounding the device. In some cases, the average was calculated without including those values considered to be erroneous temperature readings attributable to several causes, for example, the thermocouple was determined not to be in intimate contact with the thermal module's surface. During the latter experiments, the thermocouple in position #8 became disconnected from the scanner card located inside the scanner. Rather then risk breaking the other thermocouple wires, it was not repaired, and the voltage and temperature readings for that thermocouple were disregarded.

Some of the experiments were repeated several times, particularly those relative to the thin-film aluminum resistor host thermal modules. However, the results were consistent (within three tenths of one degree centigrade).

The temperature measurements posted in the tabular format were converted into a graphical representation to condense the information and highlight the important experimental results. Plots of the temperature measurements were created to show the temperature behavior relative to the delivered power. The temperatures recorded by the thermocouples in direct contact with the heat-producing devices are plotted.

Table IV-2. Thermal Module (Thin-film Resistors) Temperatures Recorded With the Thermocouple Array. Module 1, Module 2, Module 3, and Module 4 Contain the Reference Wafer, Pyramids, DVWGs, and MFC, Respectively.

MODULE 1

WATTS	TEMPERATURE (°C)				
	DEVICE	POS1	POS2	POS3	POS4
0	20.9	20.8	20.7	20.7	20.7
0.5	25.1	23.7	23.6	23.6	23.9
1.0	30.3	27.4	26.9	26.8	27.1
1.5	35.5	30.8	30.1	30.1	30.0
2.0	40.5	34.5	32.7	32.2	33.4
5.0	72.7	54.0	50.1	50.1	52.2
7.5	97.8	73.8	64.7	65.6	67.0

MODULE 2

WATTS	TEMPERATURE (°C)				
	DEVICE	POS1	POS2	POS3	POS4
0	24.1	24.1	23.9	24.1	24.0
0.5	27.5	26.7	26.0	26.1	26.1
1.0	30.4	29.2	28.4	28.5	28.6
1.5	33.6	32.0	31.0	31.3	31.3
2.0	37.0	35.2	33.2	33.5	33.8
5.0	54.7	50.9	47.1	48.2	50.5
7.5	70.5	63.8	60.5	63.4	63.6

MODULE 3

WATTS	TEMPERATURE (°C)				
	DEVICE	POS1	POS2	POS3	POS4
0	22.8	22.9	23.2	23.5	23.6
0.5	28.3	26.9	26.6	26.5	26.8
1.0	31.6	28.6	27.7	27.7	28.3
1.5	37.2	34.1	32.1	32.5	32.7
2.0	42.9	38.0	35.5	35.7	36.9
5.0	71.4	57.4	52.5	52.5	54.0
7.5	106.5	78.0	67.1	66.0	70.7

MODULE 4

WATTS	TEMPERATURE (°C)				
	DEVICE	POS1	POS2	POS3	POS4
0	21.8	21.8	----	----	----
0.5	24.4	23.6	----	----	----
1.0	25.9	25.1	----	----	----
1.5	28.8	27.0	----	----	----
2.0	30.2	28.2	----	----	----
5.0	38.3	36.3	----	----	----
7.5	47.5	39.3	----	----	----

Table IV-3. Thermal Module (Single IC Die) Temperatures Recorded With the Thermocouple Array. Module 5, Module 6, Module 7, and Module 8 Contain the Reference Wafer, Pyramids, DVWGs and MFC, Respectively.

MODULE 5

WATTS	TEMPERATURE (°C)				
	DEVICE	POS1	POS2	POS3	POS4
0	24.1	24	24	24	24
0.5	35.0	27	27	27	27
1.0	50.3	32	31	31	31
1.5	78.9	38	36	36	36
2.0	138.9	45	43	41	43

MODULE 6

WATTS	TEMPERATURE (°C)				
	DEVICE	POS1	POS2	POS3	POS4
0	24.8	25	25	25	25
0.5	35.5	27	27	27	27
1.0	50.8	31	30	30	30
1.5	74.7	36	34	34	35
2.0	104.2	42	39	39	39

MODULE 7

WATTS	TEMPERATURE (°C)				
	DEVICE	POS1	POS2	POS3	POS4
0	24.8	25	25	25	25
0.5	36.4	27	27	27	27
1.0	50.0	31	30	30	31
1.5	76.5	36	35	34	35
2.0	93.4	41	39	38	39

MODULE 8

WATTS	TEMPERATURE (°C)				
	DEVICE	POS1	POS2	POS3	POS4
0	24.7	25	----	----	----
0.5	34.2	27	----	----	----
1.0	45.5	28	----	----	----
1.5	57.9	30	----	----	----
2.0	68.3	32	----	----	----

Table IV-4. Thermal Module (Four IC Die) Temperatures Recorded With the Thermocouple Array. Module 9, Module 10, Module 11, and Module 12 Contain the Reference Wafer, Pyramids, DVWGs, and MFC, Respectively.

MODULE 9					
WATTS	TEMPERATURE (°C)				
	DEVICE	POS1	POS2	POS3	POS4
0	24.6	----	----	----	----
0.5	43.0	----	----	----	----
1.0	60.9	----	----	----	----
1.5	79.6	----	----	----	----
2.0	100.4	----	----	----	----

MODULE 10					
WATTS	TEMPERATURE (°C)				
	DEVICE	POS1	POS2	POS3	POS4
0	24.2	----	----	----	----
0.5	40.3	----	----	----	----
1.0	50.9	----	----	----	----
1.5	62.0	----	----	----	----
2.0	74.9	----	----	----	----

MODULE 11					
WATTS	TEMPERATURE (°C)				
	DEVICE	POS1	POS2	POS3	POS4
0	24.9	----	----	----	----
0.5	40.9	----	----	----	----
1.0	58.2	----	----	----	----
1.5	66.9	----	----	----	----
2.0	95.6	----	----	----	----

MODULE 12					
WATTS	TEMPERATURE (°C)				
	DEVICE	POS1	POS2	POS3	POS4
0	20.2	----	----	----	----
0.5	28.5	----	----	----	----
1.0	39.1	----	----	----	----
1.5	46.2	----	----	----	----
2.0	57.2	----	----	----	----

Figure IV-42 compares the temperatures of the thin-film aluminum resistor thermal modules. Figure IV-43 compares the temperatures of the single-IC die host thermal modules. Figure IV-44 compares the temperatures of the four-IC die host thermal modules. Figure IV-45 compares the temperatures of the thermal modules containing the reference wafers. Figure IV-46 compares the temperatures of the thermal modules containing the randomly spaced and sized pyramids. Figure IV-47 compares the temperatures of the thermal modules containing the DVWGs. Figure IV-48 compares the temperatures of the thermal modules containing the MFCs.

The rank order (best (1) to worst (4)) of heat-dissipating performance for the silicon micromachined structures is as follows: (a) for the modules containing the thin-film aluminum resistors: (1) MCF, (2) Pyramids, (3) Reference wafer, and (4) DVWG; (b) for the modules containing the IC die diffused resistors (1 IC die): (1) MFC, (2) DVWG, (3) Pyramids, and (4) Reference wafer; (c) for the modules containing the IC die diffused resistors (4 IC die): (1) MFC, (2) Pyramids, (3) DVWGs, and (4) Reference wafer.

Table IV-5 lists the percentages for the silicon wafer thermal module steady-state operating temperature decrease for each silicon micromachined structure relative to the reference wafer.

Table IV-5. The Percentage of Decrease in the Steady-State Operating Temperature of the Thermal Modules.

Module	Input Power (W)	Decrease in Temperature Relative to the Module Containing the Reference Wafer in Each Group
Module 1	2.0	-----
	7.5	-----
Module 2	2.0	8.6%
	7.5	27.9%
Module 3	2.0	-5.9%
	7.5	-8.9%
Module 4	2.0	25.4%
	7.5	56.5%
Module 5	1.0	-----
	2.0	-----
Module 6	1.0	-1%
	2.0	25%
Module 7	1.0	0.6%
	2.0	32.7%
Module 8	1.0	9.5%
	2.0	50.8%
Module 9	1.0	-----
	2.0	-----
Module 10	1.0	16.4%
	2.0	25.4%
Module 11	1.0	4.4%
	2.0	4.8%
Module 12	1.0	35.8%
	2.0	43%

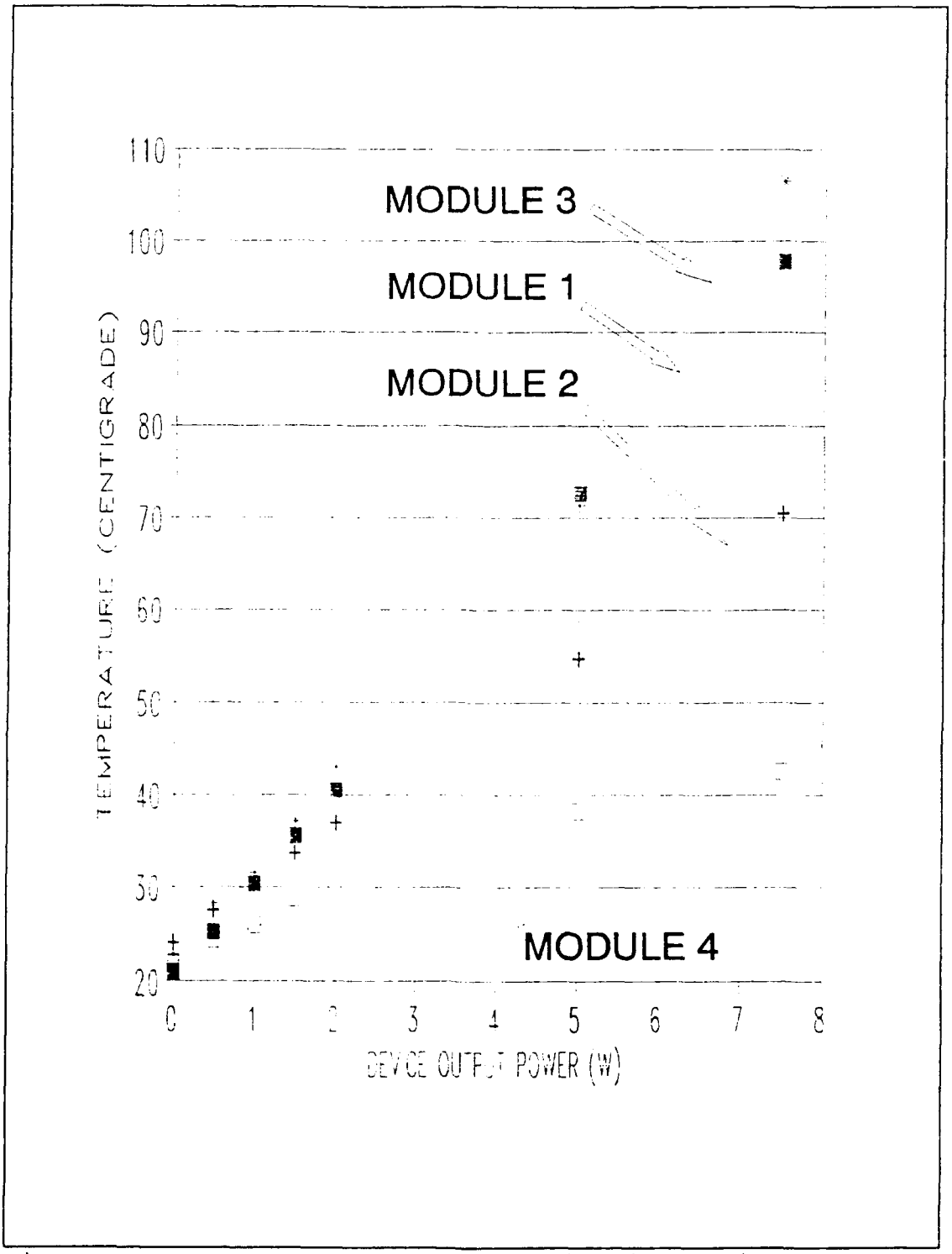


Figure IV-42. Temperatures of the Thin-film Resistor Thermal Modules: Module 1, Reference Wafer; Module 2, Pyramids; Module 3, DVWGs; Module 4, MFC.

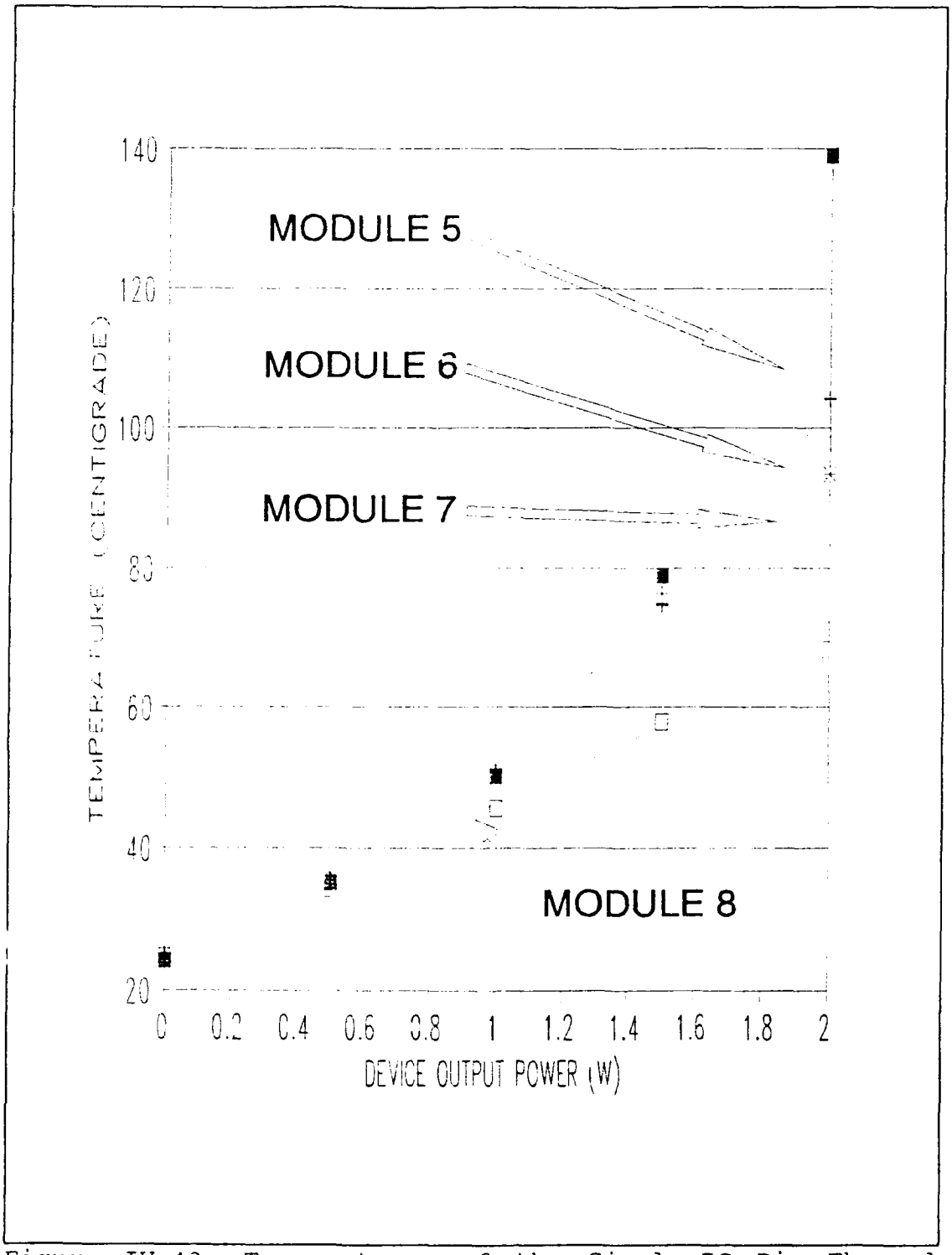


Figure IV-43. Temperatures of the Single-IC Die Thermal Modules: Module 5, Reference Wafer; Module 6, Pyramids; Module 7, DVWGs; Module 8, MFC.

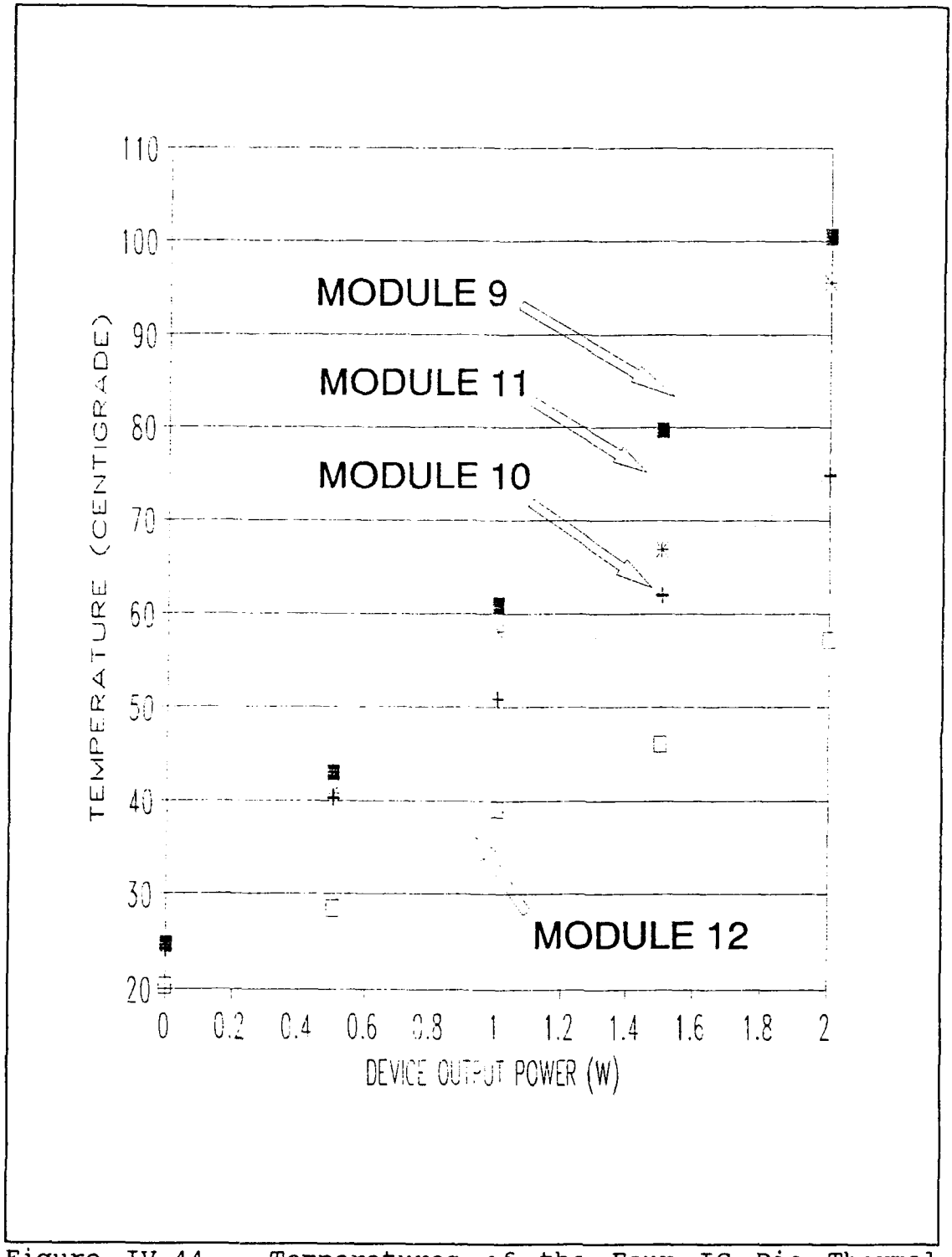


Figure IV-44. Temperatures of the Four IC Die Thermal Modules: Module 9, Reference Wafer; Module 10, Pyramids; Module 11, DVWGs; Module 12, MFC.

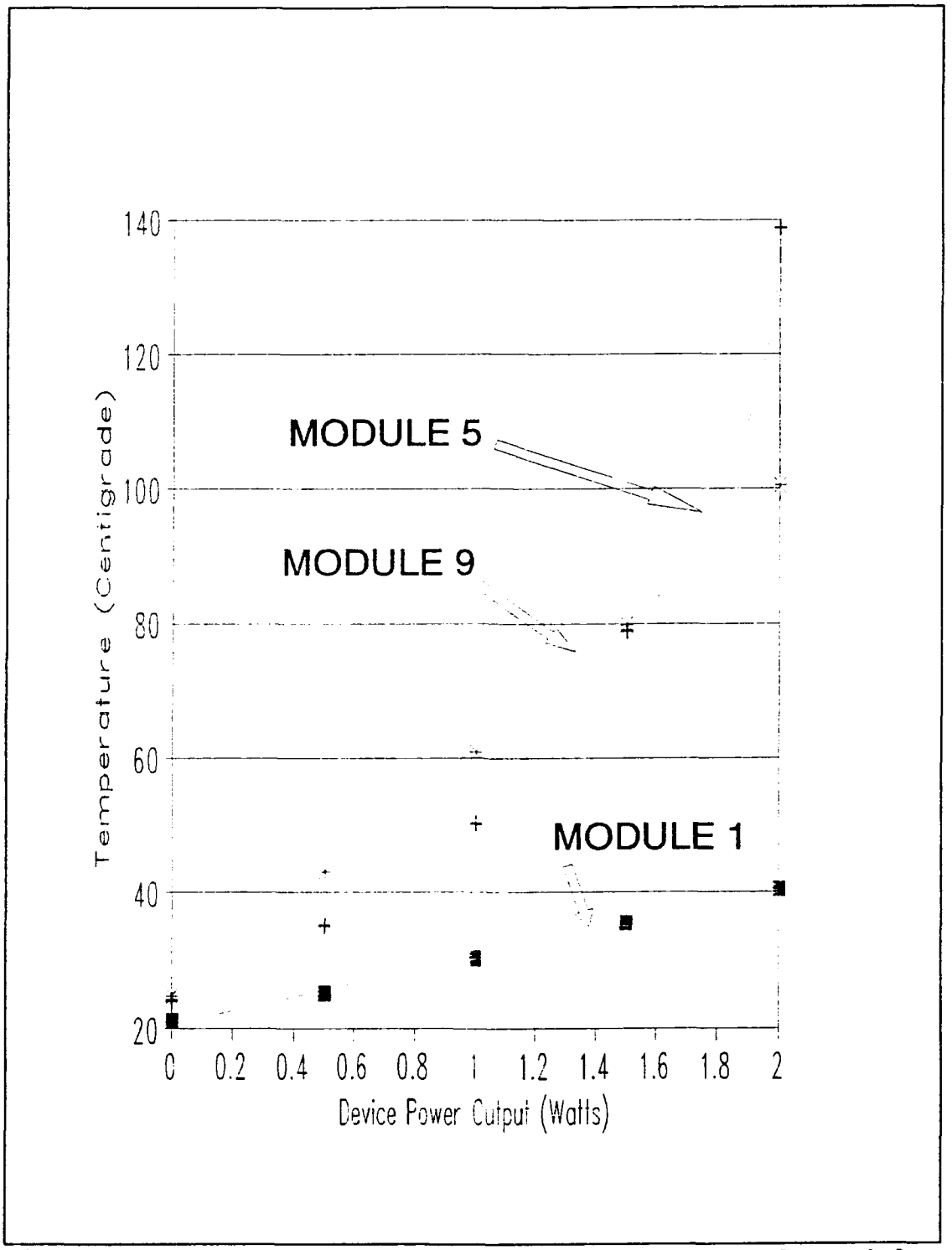


Figure IV-45. Temperatures of the Thermal Modules Containing the Reference Wafer: Module 1, Thin-film Resistor; Module 5, Single IC Die; Module 9, Four IC Die.

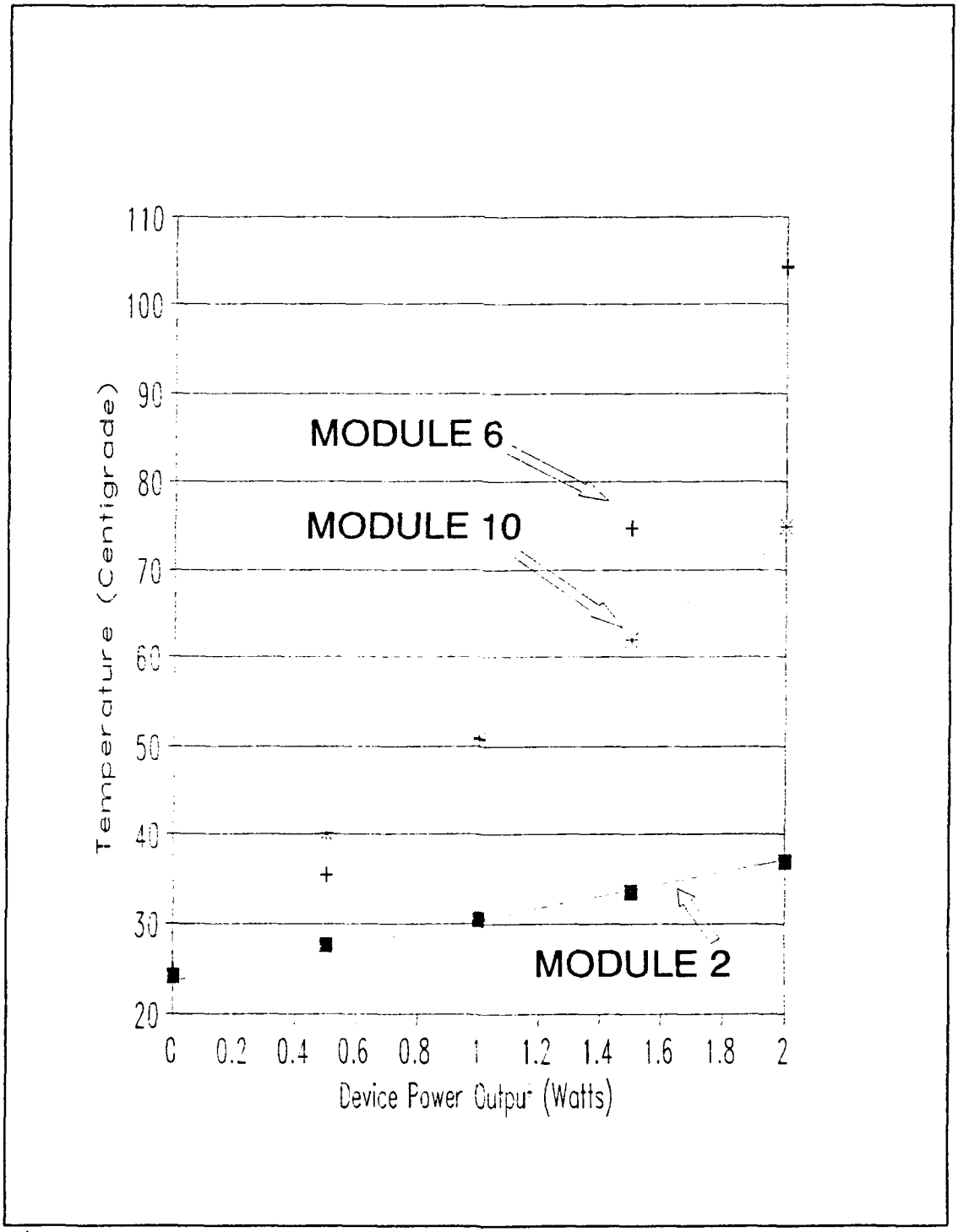


Figure IV-46. Temperatures of the Thermal Modules Containing the Randomly Spaced and Sized Pyramids: Module 2, Thin-film Resistor; Module 6, Single IC Die; Module 10, Four IC Die.

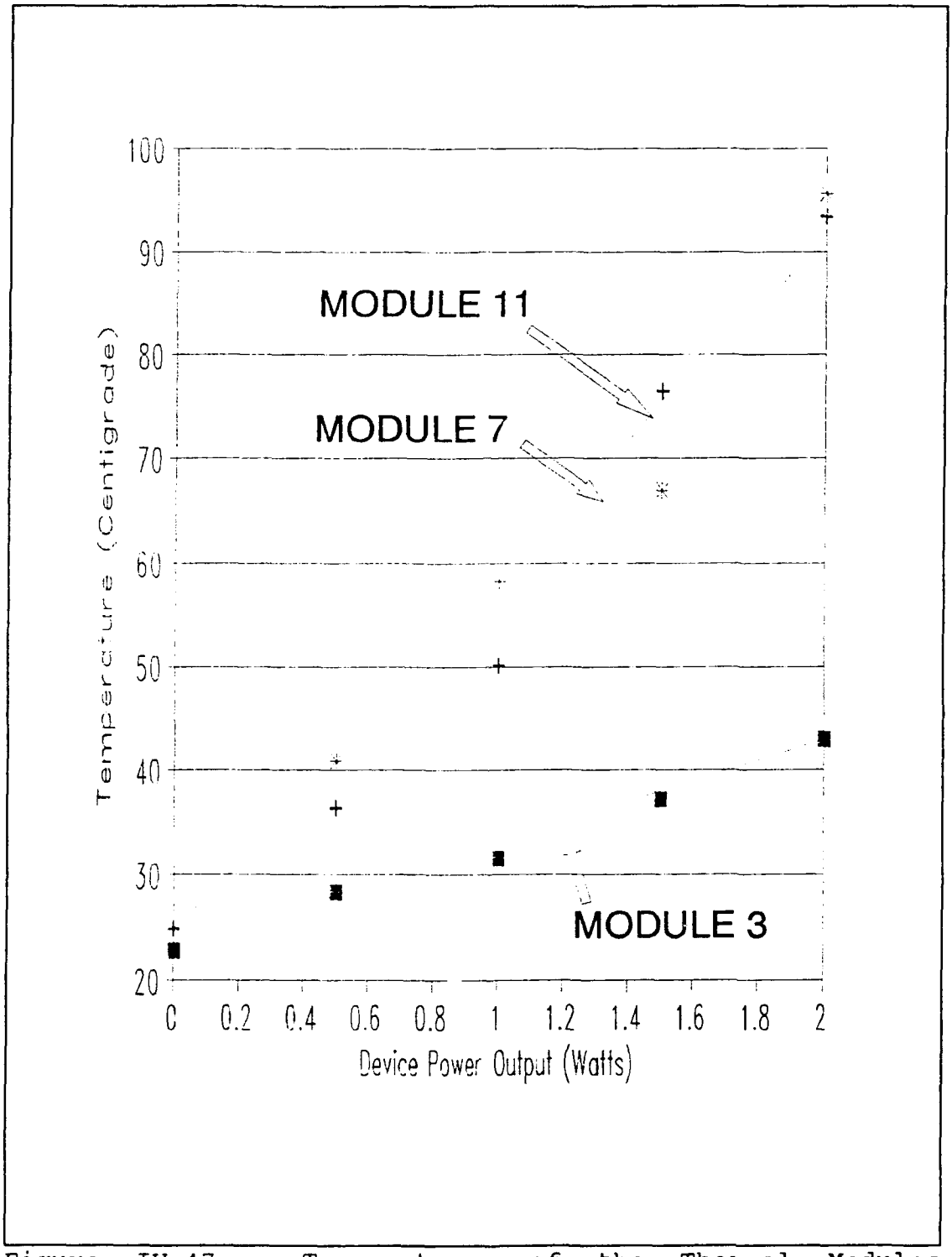


Figure IV-47. Temperatures of the Thermal Modules Containing the DVWGs: Module 3, Thin-film Resistor; Module 7, Single IC Die; Module 11, Four IC Die.

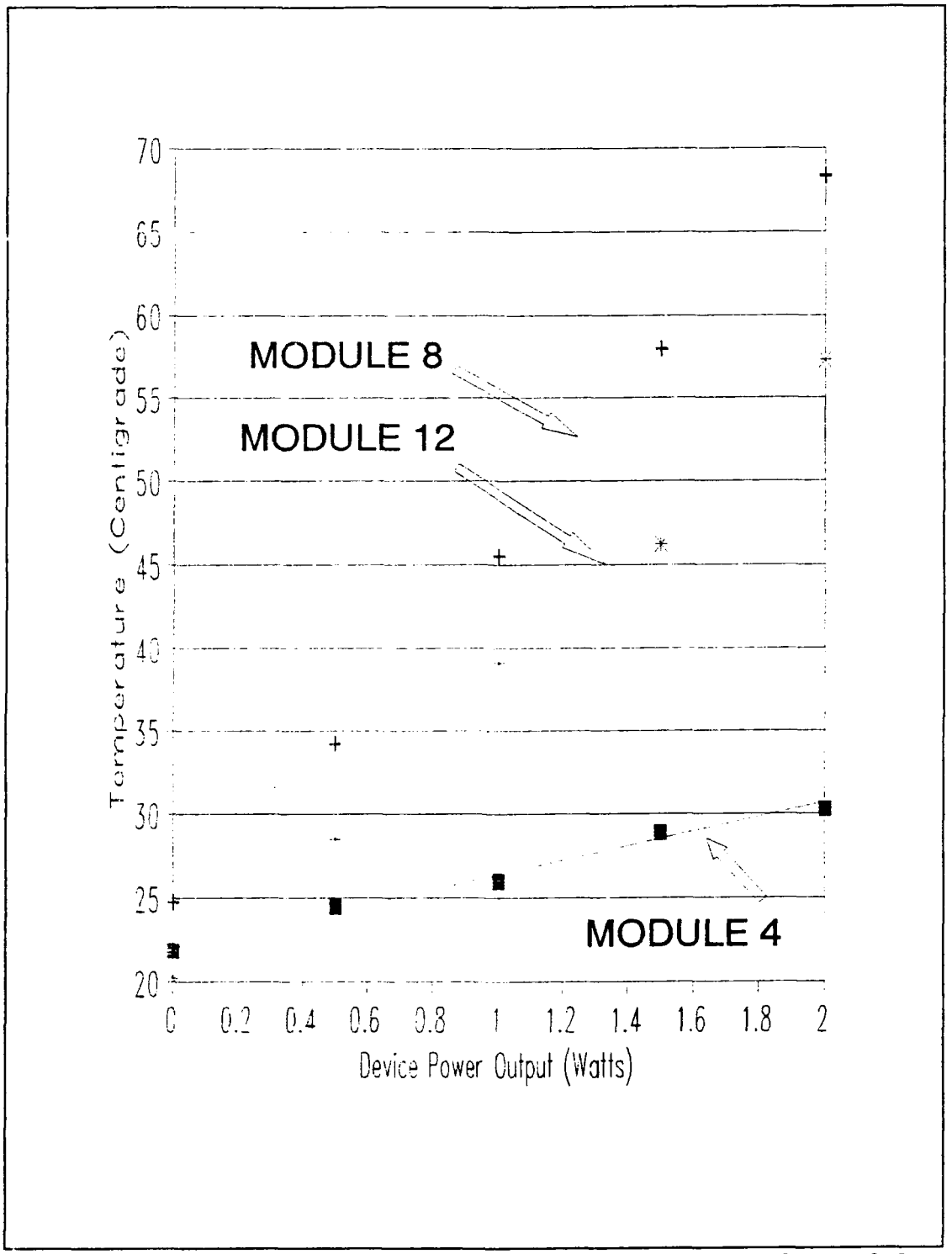


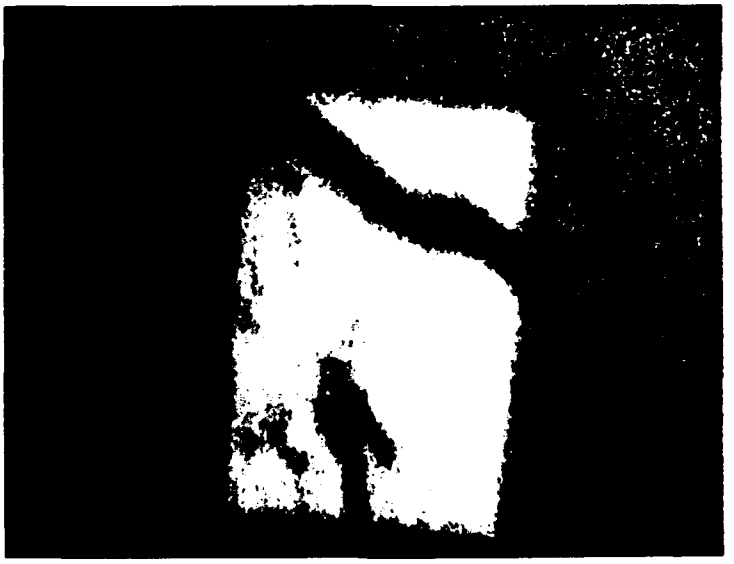
Figure IV-48. Temperatures of the Thermal Modules Containing the MFCs: Module 4, Thin-film Resistor; Module 8, Single IC Die; Module 12, Four IC Die.

4.7.2 Results of the IR Signature Investigation. The thermal images of the heat-producing devices on the silicon wafer thermal modules were recorded with a camcorder and a 2-hour VHS format videotape. The images from Modules 1, 2, 3, 5, 6, and 7 were recorded at the same input power levels used in the temperature measurement experiments. The images were recorded as the applied power was increased and allowed to stabilize. They were videotaped for two minutes at each increment, except for the last increment, which was recorded for three minutes.

The IR microscope has a minimum magnification of 6x. Consequently, approximately one half of the IC die and only a small segment of the thin-film resistor was visible on the IR microscope's video output monitor. An unmagnified image would have been preferred. That is, the thermal image would have been more concentrated, and the results would have been more readily observed. The changes in the images relative to the input power are slight.

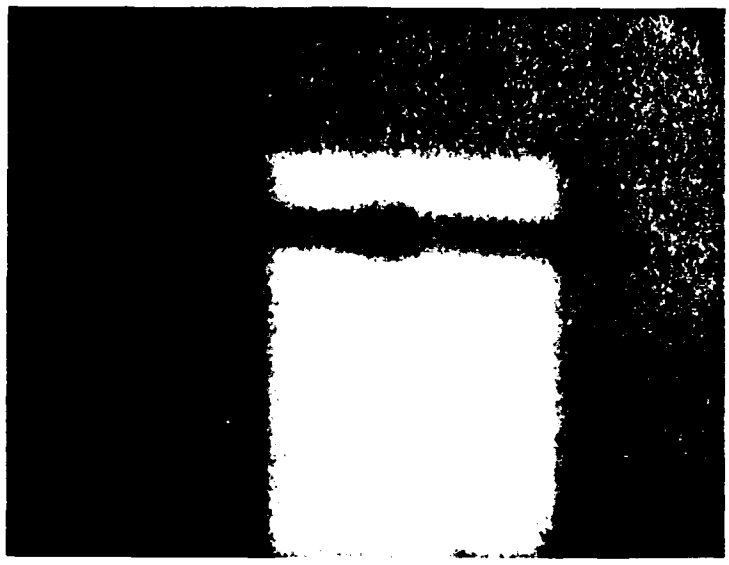
The images were also recorded from the IR microscope video output monitor with a conventional camera. Figures IV-49 through IV-51 are photographs of the monitor depicting comparative images of Modules 5, 6, and 7. They compare the thermal modules with no power applied and the largest applied power (2.0 W for the IC die resistors).

(a)

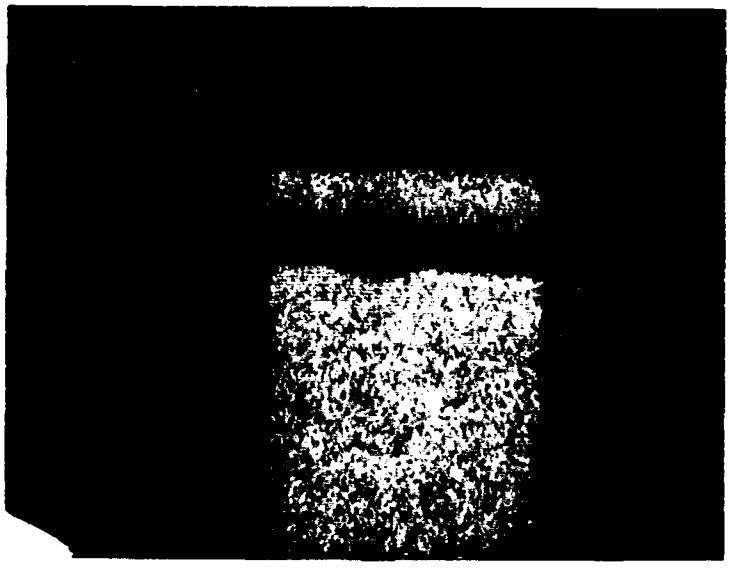


(b)

Figure IV-49. Thermal Image of Module 5--Single IC Die and Reference Wafer at (a) 0 W, and (b) 2 W.

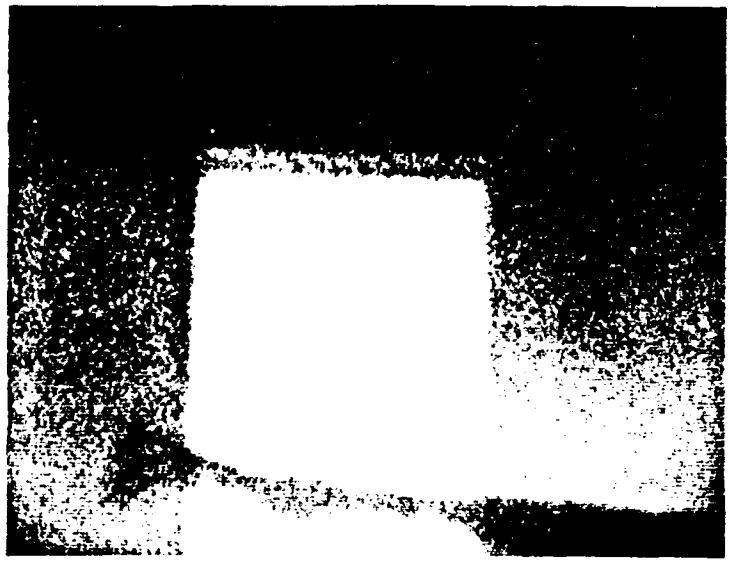


(a)

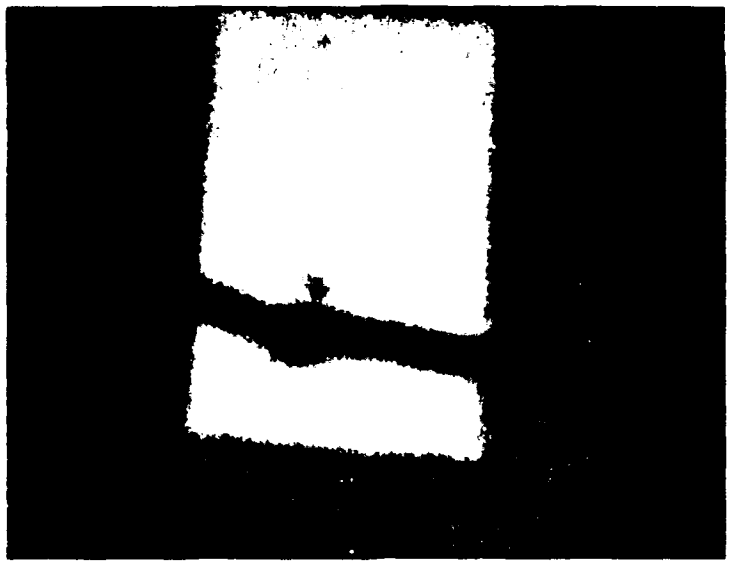


(b)

Figure IV-50. Thermal Image of Module 6--Single IC Die and Pyramids at (a) 0 W, and (b) 2 W.



(a)

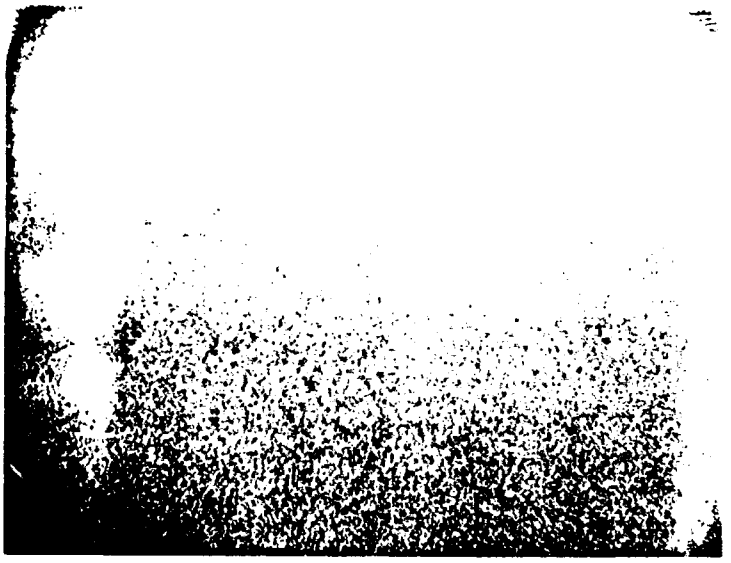


(b)

Figure IV-51. Thermal Image of Module 7--Single IC Die and DVWGs at (a) 0 W, and (b) 2 W.

Figures IV-52 through IV-57 are photographs of the monitor depicting comparative images of Modules 1, 2, and 3. They compare the thermal modules with no power applied, 7.5 W applied, and the maximum power (approximately 28, 30, and 26 W, respectively) applied prior to their catastrophic failure.

As the input power to the heat-generating devices was increased, and the devices became hotter, their images became more clearly focused. Also, the contrast of the images was more pronounced.



(a)

(b)

Figure IV-52. Thermal Image of Module 1--Thin-Film Resistor and Reference Wafer at (a) 0 W, and (b) 7.5 W.

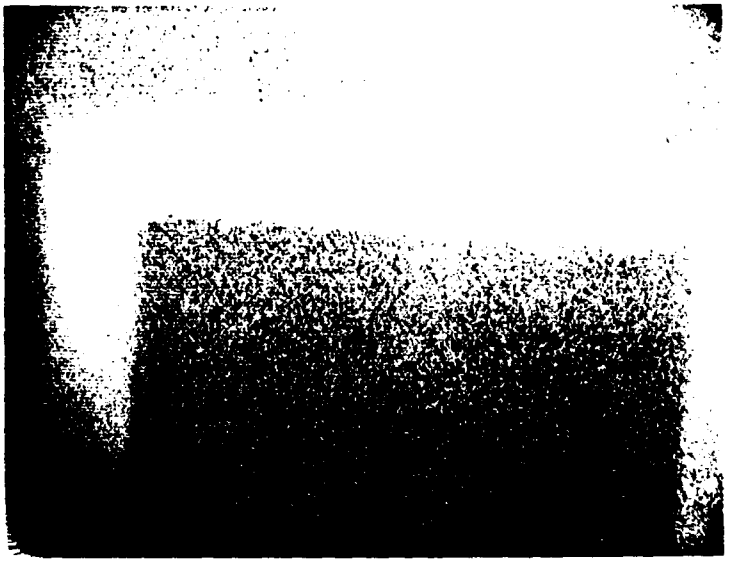
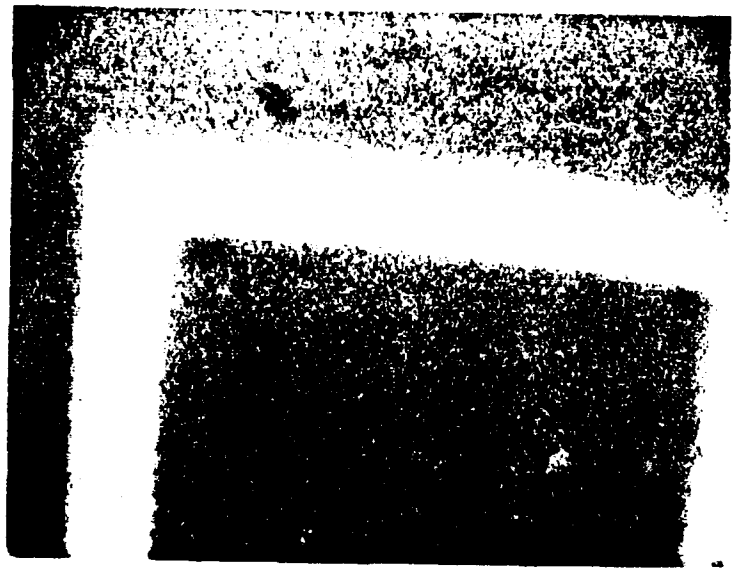


Figure IV-53. Thermal Image of Module 1--Thin-Film Resistor and Reference Wafer at 28 W.

(a)



(b)

Figure IV-54. Thermal Image of Module 2--Thin-Film Resistor and Pyramids at (a) 0 W, and (b) 7.5 W.

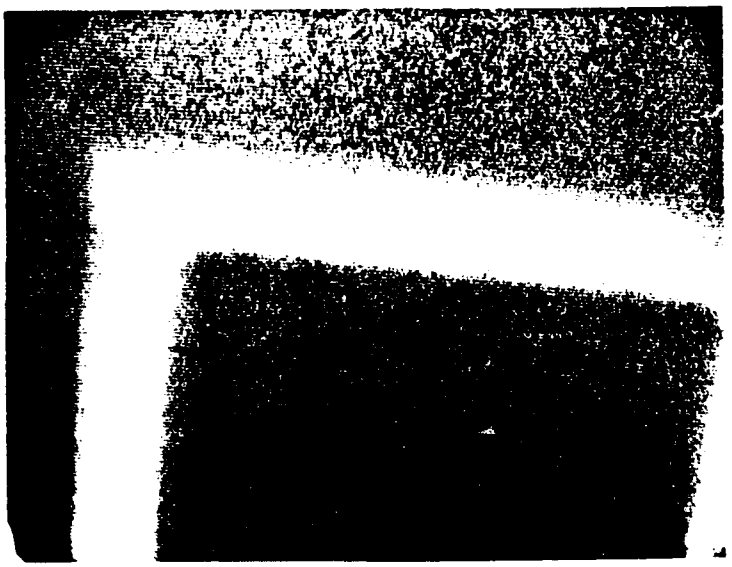
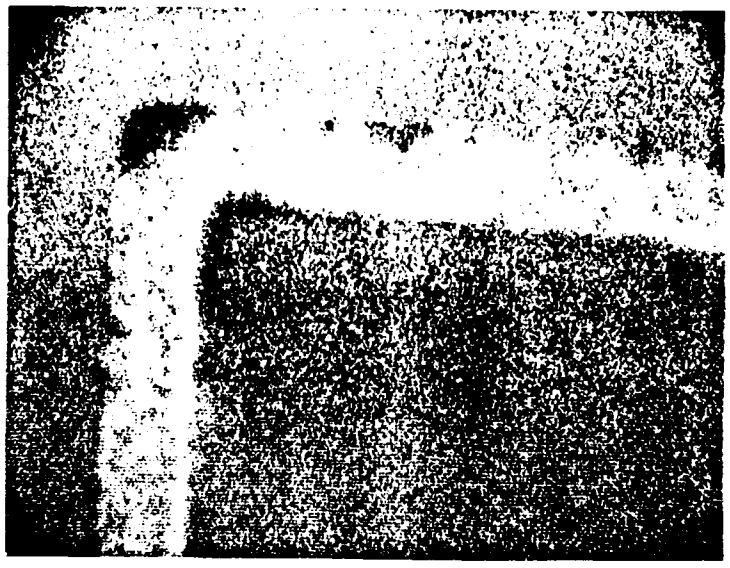
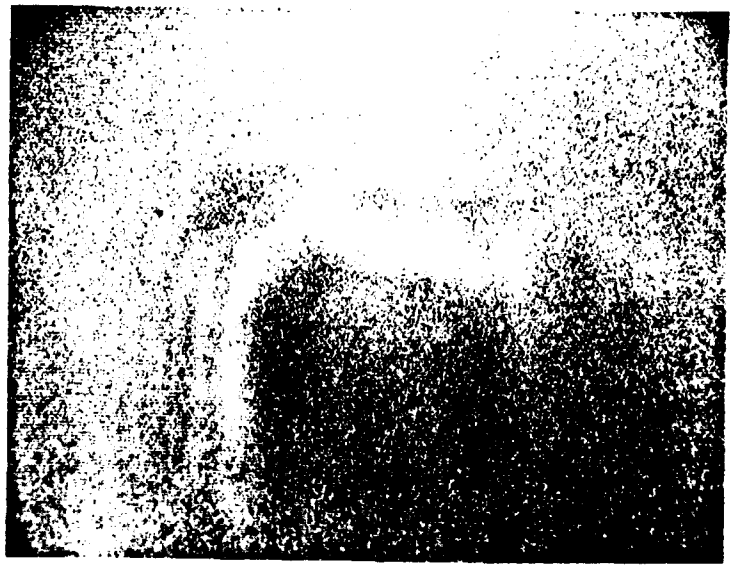


Figure IV-55. Thermal Image of Module 2--Thin-Film Resistor and Pyramids Wafer at 30 W.



(a)



(b)

Figure IV-56. Thermal Image of Module 3--Thin-Film Resistor and DVWGs at (a) 0 W, and (b) 7.5 W.

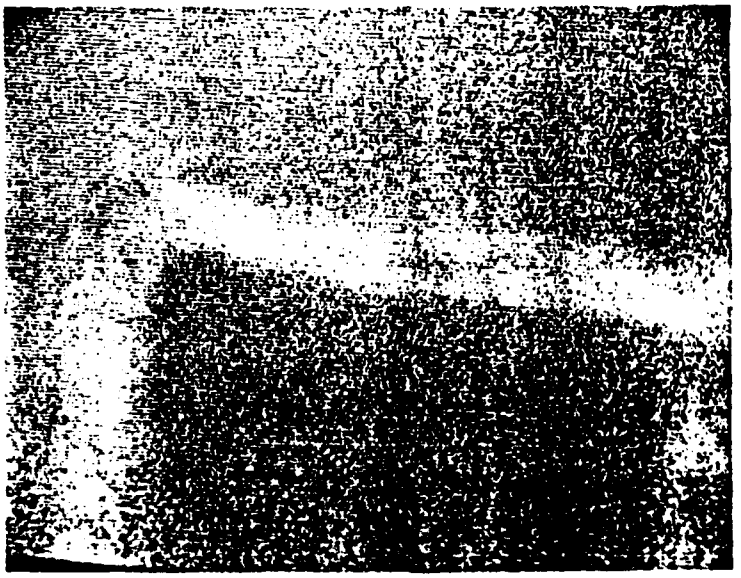


Figure IV-57. Thermal Image of Module 3--Thin-Film Resistor and DWGs Wafer at 26 W.

V. Conclusions and Recommendations

This research effort provided experimental results that support using the silicon micromachining technique as an engineering design tool for thermal management in wafer scale integrated circuits. A comparative thermal analysis of several silicon wafer thermal modules was accomplished. These modules hosted either thin-film aluminum resistors or IC die diffused resistors. The backside of these modules dissipated heat from either an untextured, reference silicon wafer or one of three silicon micromachined structures: 1) randomly spaced and sized pyramids, 2) deep vertical-wall grooves (DVWGs), and 3) micro-fluid channels (MFCs).

5.1 Conclusions

The following significant conclusions were realized during this research effort:

1. The population density and average size of the randomly spaced and sized pyramids realized in (100)-oriented silicon using hydrazine etchant solutions can vary. The variance is attributed to the combination of the solution concentration and the solution temperature. A uniformly textured surface was not realized with highly concentrated hydrazine solutions (3:2, DIW:85% (HH) and 3:2,

DIW:99% (AH)). Uniformly textured surfaces were also not realized with very dilute hydrazine solutions. There seems to be a range of hydrazine solution concentration and temperature combinations that provide optimal surface texture and uniformity. The most uniform results were realized with a 3:2, DIW:(3:2, DIW:92% hydrazine) solution at 50 °C (the solution used in the second experiment as discussed in Section 3.4.1).

2. The most critical parameter of photolithography when applied to silicon wafer photoresist patterning or metallization concerns image focusing. Also, the image dimensions, photoresist thickness, and the distance between the photomask and silicon wafer's surface are critical parameters relative to the ultraviolet light exposure time. Variations of these parameters may propagate unwanted photoresist polymerization which manifests itself as a failure to precisely transfer the image.

3. The silicon micromachined structures effectively reduced the steady-state operating temperature of the heat-producing devices and the silicon material surrounding the device on the silicon wafer thermal modules. The structure's influence on reducing the temperature was more evident as the power to the devices was increased.

4. When the generated heat was more concentrated, as it was with the IC die, the DVWGs reduced the surface

temperature of the device better than the randomly spaced and sized pyramids. The more deeply etched DVWGs conducted the heat via the convection process in the ambient atmosphere more efficiently compared to the pyramids.

5. When the generated heat was more distributed on the surface of the silicon, as it was with the thin-film resistors, the randomly spaced and sized pyramid structure was more effective at lowering the operating temperature of the thermal module. However, the pyramidal textured structure covered the entire surface of the silicon wafer. The DVWGs were limited to a pattern of nine squares, covering approximately 25% of the silicon wafer's surface. If the DVWGs had been realized over the entire surface, they would likely have been more effective than the pyramidal structure in removing the heat to the convective air surrounding the modules.

6. The MFC structures were the best heat-dissipating structures in each experiment, even though the heat was contained relative to the backside of the modules by the one-eighth-inch Pyrex glass plate.

7. The rank order (best (1) to worst (4)) of heat-dissipating performance for the silicon micromachined structures is:

a. for the thin-film aluminum resistors

1. MFC

2. Pyramids

3. Reference wafer

4. DVWG.

b. for the IC die diffused resistors (one IC die)

1. MFC

2. DVWG

3. Pyramids

4. Reference wafer

c. for the IC die diffused resistors (four IC die)

1. MFC

2. Pyramids

3. DVWGs

4. Reference wafer.

Table V-1 compares the heat-dissipating performance of the silicon micromachined structures as discussed in Chapter IV.

5.2 Recommendations

This research effort provided a baseline set of results which motivate the continuance of the pursuit of applying the silicon micromachining technique to thermal management in wafer scale integrated circuit technology. The following recommendations will further advance this application:

1. The (100)-oriented silicon hydrazine etching process should be further characterized relative to the hydrazine solution concentration and temperature. This silicon

Table V-5. The Percentage of Decrease in the Steady-State Operating Temperature of the Thermal Modules.

Module	Input Power (W)	Decrease in Temperature Relative to the Module Containing the Reference Wafer in Each Group
Module 1	2.0	-----
	7.5	-----
Module 2	2.0	8.6%
	7.5	27.9%
Module 3	2.0	-5.9%
	7.5	-8.9%
Module 4	2.0	25.4%
	7.5	56.5%
Module 5	1.0	-----
	2.0	-----
Module 6	1.0	-1%
	2.0	25%
Module 7	1.0	0.6%
	2.0	32.7%
Module 8	1.0	9.5%
	2.0	50.8%
Module 9	1.0	-----
	2.0	-----
Module 10	1.0	16.4%
	2.0	25.4%
Module 11	1.0	4.4%
	2.0	4.8%
Module 12	1.0	35.8%
	2.0	43%

micromachining technique may have a variety of applications (thermal management, light scattering/absorption, etc.).

2. Since it was determined that the silicon micromachining technique affects thermal dissipation, the application of this technique should be further characterized. Follow-on research efforts should include a variety of practical heat-producing devices (e.g.,

microprocessors, computer memories, etc.) used in actual applications of wafer scale integration. The next logical step should incorporate a refined silicon wafer process where the silicon micromachined structures are realized on the same silicon wafer that hosts the wafer scale Ics. Alternatively, the backside surface of an IC die could be textured using the silicon micromachining technique.

3. An in-depth dimensional and mathematical analysis should be made of the experimental data obtained in this research effort. For example, extrapolations could be made to predict the operating temperatures of the devices relative to their power dissipation and the heat-dissipating structure.

4. Other silicon micromachined structures should be thermally analyzed and compared to those realized in this research effort (e.g., v-grooves, thin columns, etc.).

5. Several silicon micromachined structures should be analyzed relative to several thermal convection conditions. For example, forced air directed at different velocities across the structures should be thermally analyzed and experimentally accomplished.

APPENDIX A

CRYSTALLOGRAPHY AND WET CHEMICAL ETCHING

The crystallography of single-crystal silicon (SCS) was introduced in Chapter I. One of the common microelectronic fabrication techniques, wet chemical etching process, and a characteristic of the wet chemical etching applied to SCS, anisotropy, were also introduced in Chapter I. This appendix provides further detail relative to the SCS structure and the wet chemical, anisotropic etching techniques used to realize the silicon micromachined structures investigated in this research effort.

In Figure I-1, the atoms in a representative microscopic portion of SCS are depicted. The tetrahedral bonds are also represented in the figure as dark lines connecting the atoms. The angle realized by adjacent bonds is 109.47° [1]. That is, the four bonds sharing one of the atoms in this tetrahedral arrangement form a 109.47° angle with respect to the central atom. Each silicon atom is covalently bonded to four nearest-neighbor atoms, sharing an electron pair with each nearest neighbor [6]. "Covalent bonds exist between identical atoms having similar outer shells" [1].

For convenience, a portion of SCS can be modelled as a unit cell, as depicted in Figure A-1 [4:2-3]. Then, using the cartesian coordinate system, the {100}, {110}, and {111} planes can be conveniently visualized (Figure I-1). Considering the cartesian coordinate system, {hkl} is the general mathematical representation for a crystal plane. The planar densities of a crystal and the angles between the planes determine the geometry of the structures that can be realized using photolithography and wet chemical, anisotropic etching techniques. The angle (θ) between two planes, $\{h_1k_1l_1\}$ and $\{h_2k_2l_2\}$ can be calculated using the following equation [4:2-3]:

$$\cos\theta = \frac{(h_1h_2 + k_1k_2 + l_1l_2)}{(h_1^2 + k_1^2 + l_1^2)^{1/2} \cdot (h_2^2 + k_2^2 + l_2^2)^{1/2}} .$$

The Miller indices, h, k, and l must be integers (negative, positive, or zero).

As mentioned in Chapter I, the etch rates in the different planar directions in SCS depend upon the densities of atoms in these planar directions, and their corresponding surface free bonds [4:2-4]. Higher surface free bond densities (11.76×10^{14} cm^{-2} for the {111} plane; 9.59×10^{14} cm^{-2} for the {110} plane; and 6.78×10^{14} for the {100} plane) result in correspondingly slower chemical reactions [4:2-4]. That is, etchants remove SCS faster in the {100} planes compared to the {110} planes, and even faster

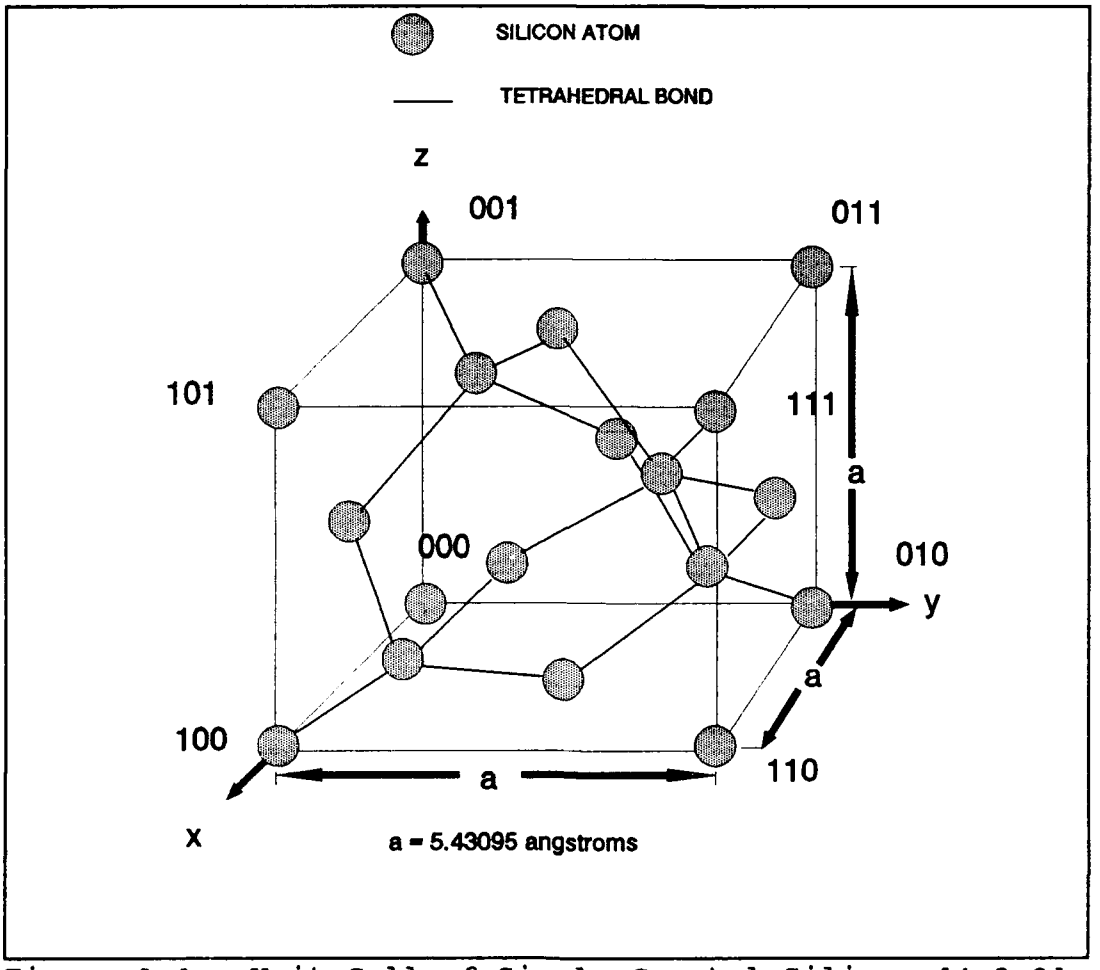


Figure A-1. Unit Cell of Single-Crystal Silicon [4:2-3].

compared to the {111} planes.

SCS has the diamond crystal structure. It has eight atoms per unit cell, its atomic weight is 28.09 g/g·mole, and its density is 2.328 g/cm^3 at 300 K [1]. The center-to-center distance (lattice constant) between the corner atoms in the unit cell is 0.543095 x 10^{-9} meters [1]. The diameter of a silicon atom is 1.22 angstroms [85]. The thermal conductivity of silicon is 1.412 W/(cm·K); the

thermal conductivity of its most common oxide, SiO_2, is 0.014 W/(cm·K) [1].

As explained in Chapter I, the reactions due to wet chemical, anisotropic etching occur along these bonds and planes in the crystal lattice.

Single-crystal, amorphous, and polycrystalline silicon, as well as a variety of other thin film materials, are the most frequent recipients of the wet chemical etch process. One common etchant reaction repetitiously oxidizes the substrate, and then dissolves the oxide; this reaction is termed oxidation-reduction (redox) [5]. Nitric acid (HNO_3) and hydrofluoric acid (HF) are commonly used to perform the oxidation and dissolution of silicon to attain H_2SiF_6 as a solid precipitate. That is,

$$Si + HNO_3 + 6HF \rightarrow H_2SiF_6 + HNO_2 + H_2 + H_2O \quad [5].$$

Acetic acid (CH_3COOH) is commonly used to buffer the reaction and allow the nitric acid to remain concentrated; otherwise, water can be used as the buffer, especially if dissociation is deemed noncritical to a particular etching process. If the acids dissociate, the etch rate decays [5]. A buffer also tends to stabilize the pH of a solution. Normally, the buffer consists of an acid and its conjugate base; buffers act to arrest ions and cations [8].

Most etchants are acids--substances which dissociate in water to liberate a hydrogen ion (H^+) [7]. In general, the

reaction $HA \rightarrow H^+ + A^-$ frees a strong oxidizing agent, (H^+). In a solution of water, if the concentration of hydrogen ions (H^+) is higher than the concentration of hydroxide ions (OH^-), the solution is acidic [85]. For the reverse situation (more hydroxide ions than hydrogen ions), the solution is basic [85]. If the concentrations are relatively equivalent, the solution is neutral [85].

Varying the ratios of the HNO_3 and HF concentrations changes the etch rates. HNO_3 controls the etch rate in an HF-rich solution where ample HF can quickly dissolve the oxide, whereas low HF concentrations act slowly to remove the oxide in an HNO_3-rich solution [5].

At room temperature, HF is likely to be used to etch SiO_2 because it barely etches SCS [5]. A diluted HF solution with an ammonium fluoride (NH_4F) buffer readily etches SiO_2 [5]:

$$SiO_2 + 6HF \rightarrow H_2 + SiF_6 + 2H_2O.$$

During this research effort, the etch rate of SiO_2 was experimentally determined to be approximately 0.18 microns per minute. This rate was realized using a 4:1, NH_4F:HF solution at room temperature.

Potassium hydroxide (KOH) was the wet chemical anisotropic etchant used in this research effort to realize the deep vertical-wall groove (DVWG) and micro-fluid channel (MFC) structures. KOH was also used to etch the IC die-

recess and epoxy-relief holes in the IC die host silicon wafers. KOH is the most selective and non-toxic anisotropic etchant [81:1]. KOH is a strong basic solution [85].

As an alkali (hydroxide of the alkali metal potassium), KOH is hypothesized to etch SCS via the following process [4:2-1]:

1) Injection of holes into the SCS to create a higher oxidation state.

2) Attachment of the hydroxyl pairs (OH^-) to the positively-charged SCS.

3) Reaction of the hydrated silicon with the complexing agent in the solution.

4) Removal of the by-products from the surface of the SCS.

Three proposed chemical equations explain this reaction [81:2]:

1) $Si + 4H_2O + 2(OH)^- \rightarrow Si(OH)_6^{-2} + 2H_2$

2) $Si + 2H_2O + 2(OH)^- \rightarrow Si(OH)_2(O^-)_2 + 2H_2$

3) $Si + 3H_2O + OH^- \rightarrow Si(OH)_4^- + (3/2)H_2$.

In a reaction between stable molecules, an activation energy is required to weaken the bonds between the reactant molecules [85]. Clark and Edell reported a range of activation energies from 0.57 eV to 0.84 eV for several $KOH:H_2O$ etchant concentrations relative to etching (110)-oriented silicon. They also reported etch rates of (110)-

oriented silicon and SiO_2 for several KOH:H_2O concentrations at various temperatures. Their data for 20% KOH in H_2O at 40 °C exhibited excellent selectivity, and this solution concentration and temperature was used in this research effort to realize the DVWGs in (110)-oriented silicon. It was also determined that the lower temperature would result in smoother surfaces and sharper edges of the DVWGs. Others have typically used KOH solutions heated to 60 °C to 80 °C .

Clark and Edell reported activation energies for SiO_2 from 0.79 eV at 22.5% KOH to 1.04 eV at 54% KOH [81]. They offered the following sequence of reactions to explain the SiO_2 etching process ((s)--solid; (l)--liquid) [81]:

$$(1)\ SiO_2(s) + 2(H_2O(l) \rightarrow SiO_2 \cdot 2(H_2O(s))$$

$$(2)\ SiO_2 \cdot 2(H_2O(s)) + 2(OH^-) \rightarrow [Si(OH)_6]^{-2}.$$

Hydrazine was the other etchant used in this research effort. Anhydrous hydrazine and hydrazine hydrate solutions were used to realize the randomly spaced and sized pyramids in (100) silicon. Hydrazine (N_2H_4) is a rocket fuel. It is highly explosive at, or above, its boiling point, and it is a known mild, human carcinogen [80]. Hydrazine is an oxidizer; hydrazine solutions always contain a small amount of H_2O [80]. Its reaction with silicon is not fully understood, but it is thought to either form an unstable silicon nitride complex, or perhaps etch the silicon via the

following reaction with the SiO_2 forming at the surface of the silicon wafer [85]. Hydrazine etches SiO_2 at an insignificant rate.

Figure A-2 depicts the results of etching (100)-oriented and (110)-oriented SCS. The micro-fluid channel structure was etched in (100)-oriented SCS, and the channels are similar to the groove on the right side of Figure A-2 (a). The depth (dg) of the grooves is limited by their width (W_o) at the substrate-oxide interface and the angle (54.74°) that the {111} plane makes with the {100} plane. That is, [4:2-8]:

$$dg = (W_o/2) \cdot \tan (54.74°).$$

The depths of the grooves realized in the micro-fluid channel structure were only 50 microns. The limiting angle was not a factor for this part of the research.

The randomly spaced and sized pyramids were realized by etching the {111} planes in (100)-oriented SCS with the hydrazine etchants [4:2-9]. The angle between the sides of the pyramids, relative to their peak is 70.53° (It is the angle formed among the {111} planes).

The DVWGs resemble the illustration in Figure A-2 (b). The grooves are vertical, and the depths are limited only by the thickness of the silicon wafer.

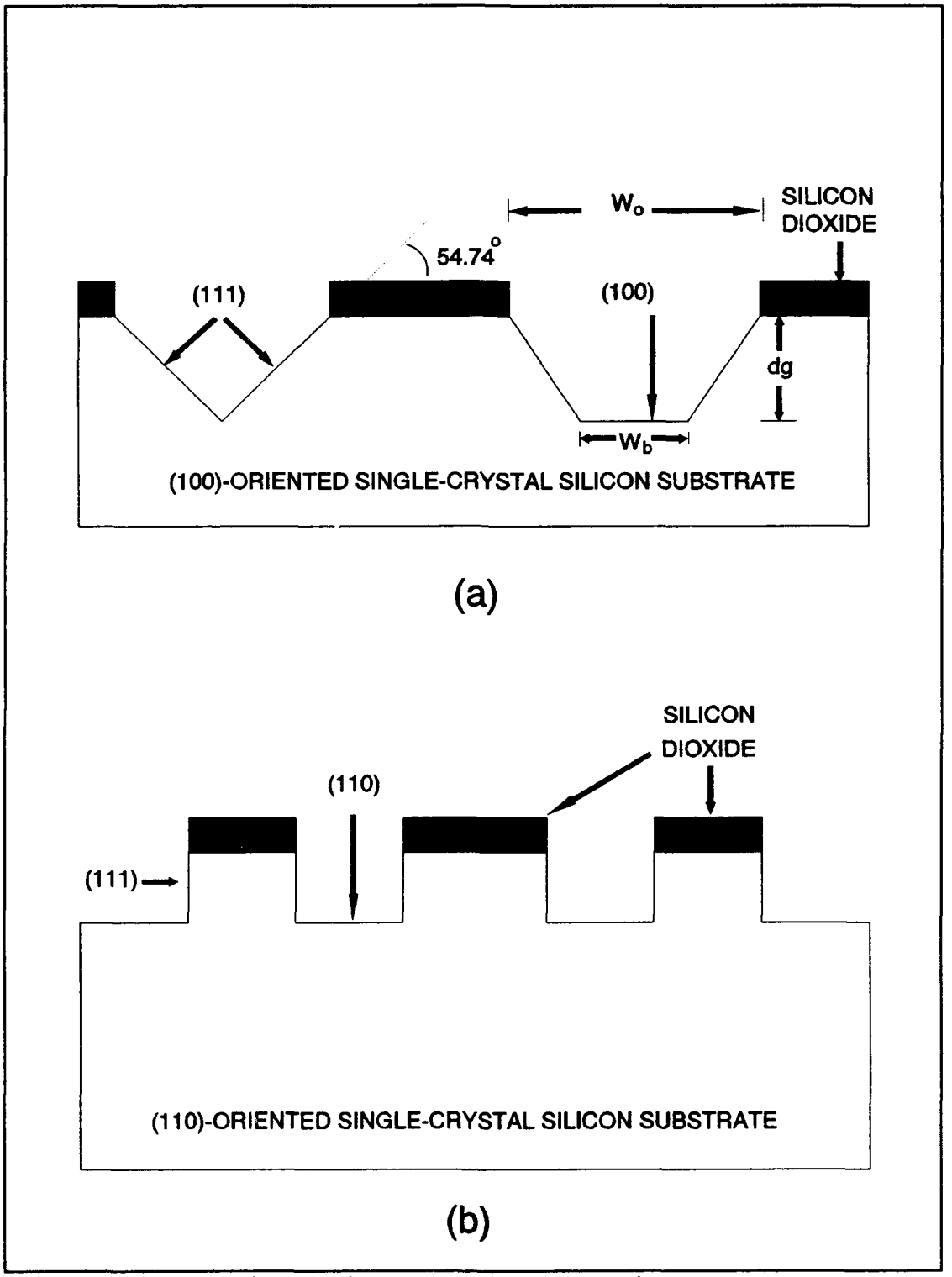


Figure A-2. Orientation Dependent Etching: (a) (100)-Oriented SCS, and (b) (110)-Oriented SCS [4:2-10].

APPENDIX B

THERMAL DISSIPATION THEORY

This appendix discusses the fundamental theory of thermal dissipation or heat transfer. Heat transfer was introduced in Chapter I; this appendix further supports research concerning silicon micromachining applied to thermal dissipation in wafer scale integration.

Temperature is a measure of the energy of an object. Energy, in the form of heat, flows from a hotter region (temperature T1) to a cooler one (temperature T2) at a rate determined by the difference in temperature between the two regions (T2 - T1) and the thermal resistance (R) to the heat flow. A change in temperature is proportional to the thermal resistance times the heat-flow rate; that is, $(T2 - T1) = R \cdot q$, where q is the heat-flow rate [9:21]. This is analogous to energy, in the form of electricity, flowing from a region with a higher electrical potential to a region with a lower electrical potential. The thermal resistance is analogous to the electrical resistance in an electronic device or conductor; the heat-flow rate is analogous to the electric current.

The transfer of energy, in the form of heat, is accomplished by: (1) conduction, (2) convection, or (3) radiation (Figure B-1).

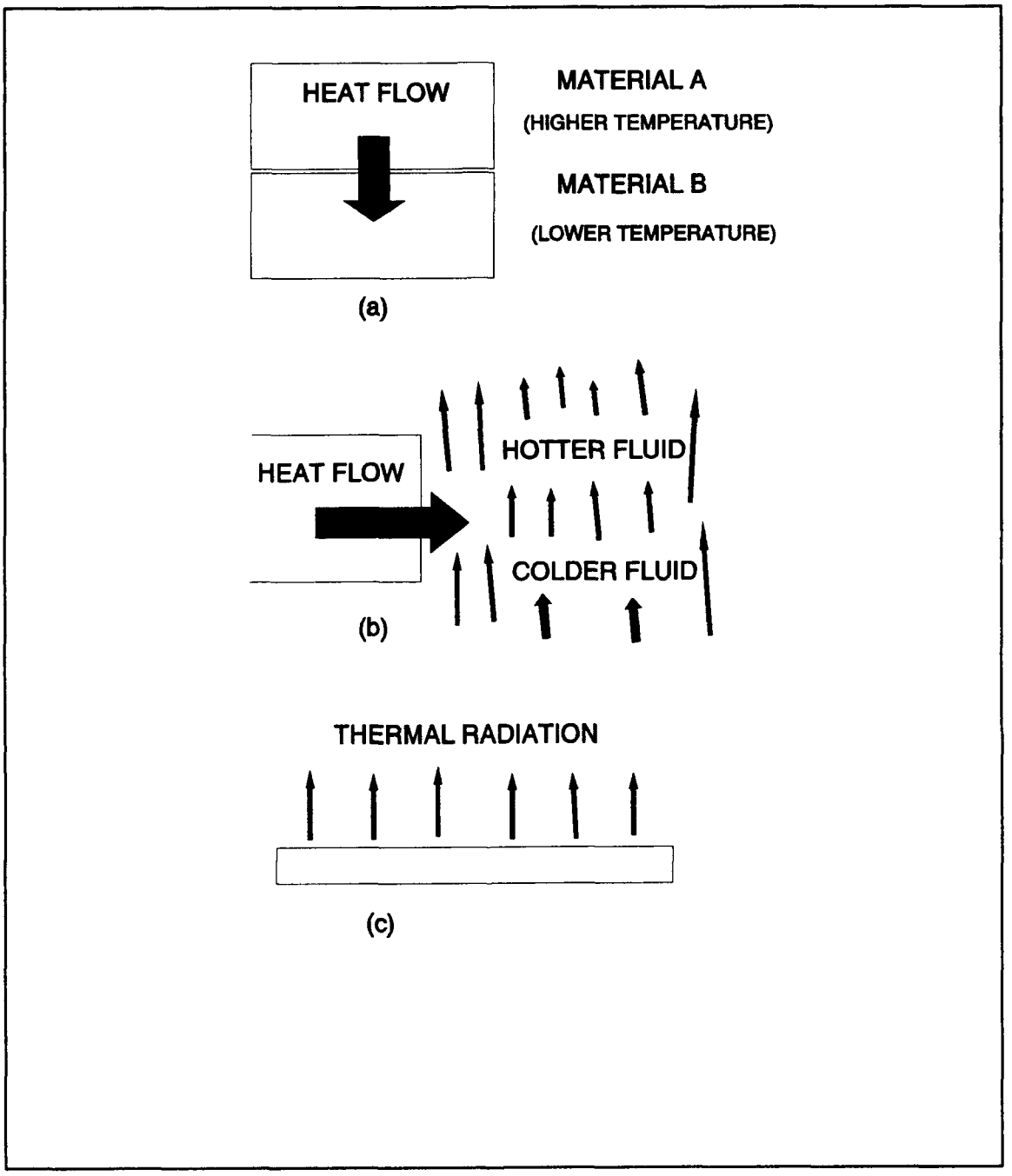


Figure B-1. Heat Flow: (a) Conduction, (b) Convection, and (3) Radiation [9:24].

Heat conduction of heat occurs among molecules in a solid, liquid, or gas [9:22]. As the molecules collide, a kinetic transfer provides the less energetic molecules with energy from the more energetic molecules. Within a homogeneous, isotropic medium, a temperature gradient causes the heat to flow and reduce the gradient. The rate at which the heat flows is $q = - k \cdot A \cdot (\partial T/\partial n)$, where q is the heat-flow rate, A is the cross-sectional area through which the thermal energy flows, and k is the thermal conductivity (Btu/hr·ft·°F or $W/(m^2 \cdot °C)$) of the medium [37:1]. The partial derivative of the temperature is determined with respect to the normal to the area (A) [37:1]. For a homogeneous medium and steady-state heat transfer conditions, the temperature gradient is linear [37:1].

The thermal resistance (R) is calculated by dividing the length of the heat-flow path (L) by the product of the thermal conductivity (k) of the material and the cross-sectional area (A): $R = L/(k \cdot A)$ [9:23]. The thermal conductivity of the diamond-impregnated epoxy used to realize the silicon wafer thermal modules is 80 Btu/hr·ft·°F [38]. Typically, epoxies used in the micro-electronics industry have thermal conductivities in the 1 to 12 Btu/hr·ft·°F range [38]. Table B-1 lists the values of thermal conductivities at 27 °C for several common materials.

Convection refers to the application of pressure to a gaseous or liquid fluid to provide it with a velocity.

Table B-1. Thermal Conductivity of Typical Materials [9:95].

Material	Thermal Conductivity (Btu/hr·ft·°F)
Plastic Foam	0.01-0.08
Air	0.0151
Fiberglass	0.028
Plastic (Polystyrene)	0.09
Epoxy	0.1-0.87
Water	0.349
Glass	1.0-2.0
Steel	28
Nickel	35
Aluminum	122
Gold	170
Copper	220
Silver	240

The purpose is to move the fluid from some object (or other fluid) from which it has obtained energy via conduction. Moving the fluid from discrete points where the fluid contacts the object facilitates a continuous heat transfer via conduction. The fluid flow displaces the heated fluid and replaces it with cooler fluid which continually provides the conduction process with a significant temperature differential.

The heat transfer for convection is given by Newton's Law of Cooling: $q = h \cdot A \cdot (T_o - T_f)$ where A is the area of the object in contact with the fluid, q is the heat transfer rate, T_o is the surface temperature of the object being cooled, and T_f is the temperature of the fluid upstream from the object [37:2].

By thermal radiation, heat transfer is accomplished as electromagnetic wave propagation [37:2]. Photons are emitted

from a hotter object and absorbed by a colder object [9:26]. The heat transfer rate is approximated by the Stefan-Boltzman law: $q = \sigma \cdot A \cdot T^4$ where T is the absolute temperature, A is the area emitting photons, σ is a constant ($\sigma = 0.1714 \times 10^{-8}$ Btu/hr·ft^2·°R^4) for ideal (blackbody) radiation [37:2]. For less than perfect blackbody radiation, the emissivity (ϵ) of the emitter's surface is required to represent the thermal radiation, and it is approximated by $q = \epsilon \cdot \sigma \cdot A \cdot T^4$ [37:2]. Table B-2 gives the values of emissivity for several common material surfaces at 4 °C. Real surfaces have emissivities between 0 and 1 where a value of 1 is the perfect blackbody emissivity [9:96].

Table B-2. Emissivity of Typical Surfaces [9:96].

SURFACE	EMISSIVITY	SURFACE	EMISSIVITY
Silver	0.02	Gold	0.03
Aluminum	0.03	Stainless steel	0.05
Chrome	0.08	Polished aluminum	0.05
Nickel	0.18	Titanium	0.20
White silicone paint (gloss)	0.75	Sandblasted aluminum	0.40
Black silicone paint (flat)	0.81	Grey silicone paint	0.96

When an emitter and absorber are involved in heat transfer, the temperature difference between them determines the heat transfer rate [9:26]. Further, T^4 is replaced by $(T_E^4 - T_A^4)$ in the heat transfer by radiation equation where T_E^4

is the absolute temperature of the emitting body, and T_A^4 is the absolute temperature of the absorbing body [9:27].

For electronic components operating in conventional atmosphere (normal temperature (-54 °C to 125 °C) range), conduction and convection occur simultaneously and are the dominant modes of heat transfer [83:11].

For steady-state conditions, the Laplace equation:

$$\partial^2 T/\partial X^2+\partial^2 T/\partial Y^2+\partial^2 T/\partial Z^2=0$$

is used to solve for the temperature in three dimensions. The temperatures reported in Chapter IV were recorded with the thermocouples after steady-state conditions were attained. Theoretically, the ultimate temperature, T, of the IC die or the silicon wafer containing the thin-film aluminum resistor is determined by $T = T_o + q_G/K$ [83:88]. Here, T_o is the initial temperature, q_G is the heat (in Watts or Btu/hr) imposed on the single-crystal silicon, and K is the loss of heat (W/°C) from the single-crystal silicon to the environment [83:85-88]. The heat loss, K, is considered to be via the conduction mode, but convection influences the process by changing the nearby ambient temperature, establishing a larger temperature differential (T2 - T1).

An important objective of this research was the variation of the K-parameter among the silicon wafer thermal modules. A successful variation would consequently increase the heat loss to the environment and lower the steady-state operating

temperature of the heat-producing device.

The heat generation, q_G, equates to a product of the weight, W (lb or kg), of the device under thermal analysis, the specific heat, c (J/kg·°C or Btu), of the material, and the change in temperature, T, with respect to time, t; that is,

$$q_G = W \cdot c \cdot (dT/dt) \quad [83].$$

Heat transfer via convection is classified as either laminar or turbulent. At lower fluid-flow velocities, energy is transferred among the layers of molecules flowing along the surface. As the fluid-flow velocity increases, it approaches a speed (characteristic of a given fluid) at which the fluid flow becomes turbulent. The transition also depends on the flow distance, and it is defined in terms of the Reynolds number, Re. That is, $Re = V \cdot l/v$, where V is the average fluid velocity, v is the kinematic viscosity of the fluid, and l is the length along the flow where laminar flow ceases [82:109].

These heat transfer modes--conduction and convection--should be exploited to maximize the heat transfer and increase the reliability of integrated circuits. According to several sources, the operating temperature of an electronic component/device strongly influences reliability [9; 10; 14; 16; 18]. Table B-3 provides experimental support illustrating the drastic increase in failures at an increased operating temperature.

Table B-3. Number of Failures After 1,000 Hours of Operation Per Million Units [84:289].

Component	Operating at 25 °C	Operating at 75 °C
Thick film resistor	5	15
Chip capacitor	10	25
Power transistor	50	300
Diode	1	9
Logic ICs		
Small scale integration	125	1125
Medium scale integration	250	2250
Large scale integration	500	4500

APPENDIX C

STANDARD CLEANING PROCEDURE

All of the silicon wafers were cleaned using the following procedure:

1) They were immersed in 100% sulfuric acid (H_2SO_4) for 30 minutes at 100 °C to remove organic contaminants, and then they were rinsed in de-ionized water (DIW).

2) They were immersed in a buffered hydrofluoric acid (HF) solution (4:1, NH_4F:HF) for 5 minutes to remove their native oxide.

3) They were rinsed in a nitrogen (N_2) bubbled, DIW filled tank to a 10 megohm resistance standard.

4) They were blown dry with N_2 gas [12; 43].

5) They were placed back into their original shipping containers, ready to be processed for anisotropic etching, photolithographic imaging, or epoxy bonding.

APPENDIX D

SILICON DIOXIDE GROWTH SCHEDULE USING A WET-OXIDATION SCHEME

In order to grow a thin-film of silicon dioxide (SiO_2) on the silicon wafers, they were placed in a quartz boat and inserted slowly toward the center of the oxidation furnace. The furnace's temperature was pre-equilibrated to the pre-set oxidation temperature of 1075 °C. Oxygen was bubbled through DIW at 95 °C to promote the growth of a wet-oxide thin film. The required SiO_2 thickness was estimated from the wet-oxide growth chart (Figure D-1). The wafers were oxidized for the required period of time specified in their respective preparation sections, and then the oxidation furnace was ramped-down to its lower operating temperature (400 °C). The wafers were then slowly removed from the oxidation furnace and allowed to cool. The SiO_2 thickness was measured and verified with the ellipsometer (Gaertner Scientific Corp., model L117, Chicago, IL 60614) and a stylus profilometer (Sloan Technology Corp., model Dektak IIA, Santa Barbara, CA 93109).

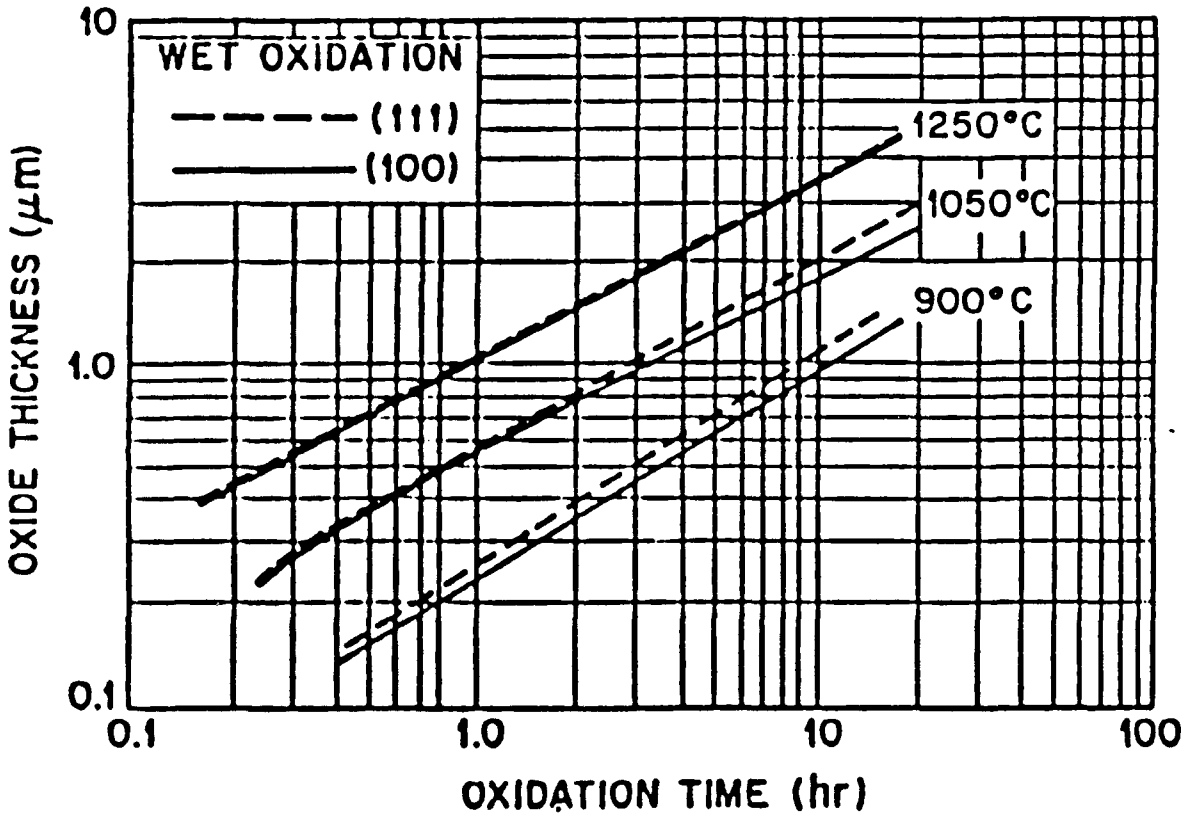


Figure D-1. Oxide Growth in Steam [12].

APPENDIX E

SILICON DIOXIDE GROWTH SCHEDULE USING A DRY-OXIDATION SCHEME

In order to grow a thin-film of silicon dioxide (SiO_2) on the (110)-oriented silicon wafers, they were placed in a quartz boat and inserted slowly toward the center of the oxidation furnace. The furnace's temperature was pre-equilibrated to the pre-set oxidation temperature of 1075 °C. An oxygen flow was initiated at 1 liter per minute to realize a high quality, dry SiO_2 thin-film on the surface of the silicon wafers. The required SiO_2 thickness was estimated from the dry-oxide growth chart (Figure E-1). The wafers were oxidized for the required period of time specified in the (110)-oriented silicon wafer preparation section (Section 3.3.2), and then the oxidation furnace was ramped-down to its lower operating temperature (400 °C). The wafers were then slowly removed from the oxidation furnace and allowed to cool. The SiO_2 thickness was measured and verified with the ellipsometer (Gaertner Scientific Corp., model L117, Chicago, IL 60614) and the stylus profilometer (Sloan Technology Corp., model Dektak IIA, Santa Barbara, CA 93109).

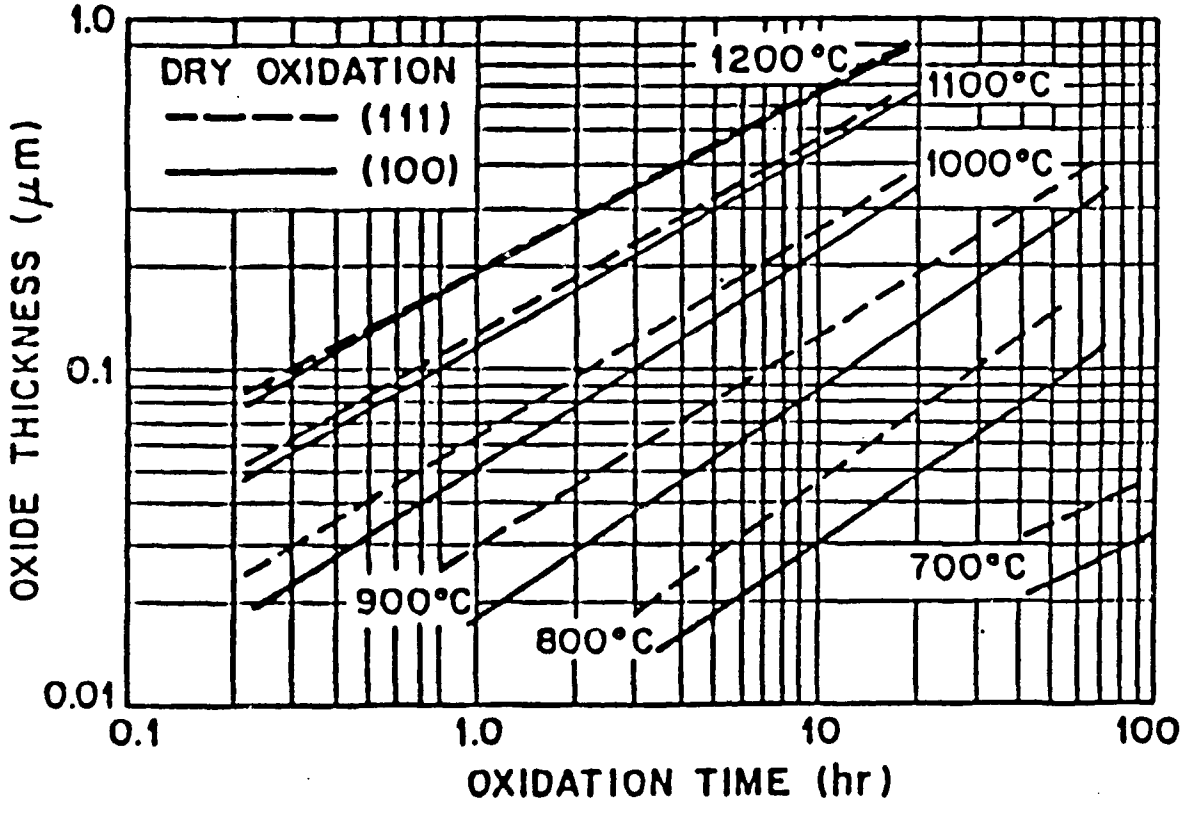


Figure E-1. Dry Oxide Growth [12].

APPENDIX F

PHOTORESIST APPLICATION

The silicon wafers were placed on the photoresist spinner (Headway Research, Inc., model 1-PM101D-R790, Garland, TX 75042). Lens paper was placed between the wafer and the photoresist spinner's chuck to protect the wafer's frontside. After each wafer was placed on the photoresist spinner's chuck, dust was blown from its surface with N_2, and negative photoresist (Waycoat, product HR200, Palisades Park, NJ 07650) was applied to the backside of the wafers with an eyedropper. The wafers were then spun at 4000 rpm for 20 seconds to uniformly distribute the photoresist [12]. The wafers were baked at 75 °C for 15 minutes to remove solvents from the photoresist and harden its surface [12]. When the silicon wafers cooled, they were exposed to an ultraviolet light source for 60 seconds in the mask aligner (Karl Suss, model MJB3 UV300, Waterbury Center, VT 05677) [12]. (Photomasks were not required to maintain a protective SiO_2 thin-film. However, the silicon wafers were exposed to the ultraviolet light through the appropriate photomasks to realize the required images for patterned, anisotropic, wet-chemical etching). The wafers were then hardbaked at 135 °C for 15 minutes to further harden the photoresist [12].

APPENDIX G

NEGATIVE PHOTORESIST DEVELOPMENT

The HR200 negative photoresist was developed using the following procedure:

1) The wafers were placed in the photoresist spinner and spun at 500 rpm.

2) The wafers were purged with N_2 to remove any accumulated dust.

3) Xylene was liberally applied for 45 seconds to the wafer to develop the printed image.

4) N-butyl acetate was liberally applied for 30 seconds to rinse the wafers and stop the development.

5) The wafers were dried with N_2.

The wafers were hardbaked at 135 °C for 15 minutes to further harden the photoresist.

APPENDIX H

THERMOCOUPLE CONTROL AND TEMPERATURE CONVERSION PROGRAM

```
program gpib;
{$N+,E+}
{$M 24000, 0, 655360}
uses Dos, Crt;
{$I TURBO4.INC}
var
  K706,MyAddr,K617:integer;
  RefVCor:single;
  Poll,Stat:      integer;
  Controller:     integer;
  ArrayPos:integer;
  Query: Char;
  Command:       string;
  InputStr:string;
  StrLen:integer;
  CommDesc:sdesc;
  OFileName:string;
  TestV, TestT: single;
  I: integer;
  DataFile: text;
procedure Beep;
begin
  sound(100);
  delay(100);
  sound(300);
  delay(100);
  sound(500);
  delay(100);
  nosound;
end;{Beep}
{$I STRCONV.PAS}
{$I 488UBS.PAS}
procedure Init;
var I:integer;
    Module: string;
    Today:string;
begin
  MyAddr := 21; controller := 0;
  initialize (myaddr,controller);
  ArrayPos:=0;
  K706:=22;
  K617:=27;
  Send488(K706,'RXA0X'); {Scanner Reset-Select Matrix
Mode}
  Send488(K617,'');      {Reset Electrometer}
  ClrScr;
```

```
  write('Enter OutPut File Name');
  readln(OFileName);
  write('What is the Module Number?');
  readln(Module);
  write('What is the date');
  readln(Today);
  write('Disconnect electrometer input, Press <Enter> when
ready');
  readln;
  Send488(K617,'F0XR1XC1XZ1XC0XR0X');   {Setup K617 for
voltage measurement}
  write('Connect electrometer to DUT, Press <Enter> when
ready');
  readln;
  assign(DataFile,OFileName);
  rewrite(DataFile);
  writeln(DataFile,'Date = ',Today);
  writeln(DataFile,'Module Number = ', Module);
  close(DataFile);
end;
procedure RefMeasure;
var
  measurement : string;
  temp: real;
  T2, RefV:single;
begin
  Send488(K706,'B0461C0461X');   {Close Ref Channel}
  Delay(1000);  {Let Settle for 1 Second}
  Enter488(K617,measurement,16);
  valSingle(copy(measurement,5,12),RefV);
  T2:=30-(RefV*1000);
  RefVCor:= (3.8680238E+1*T2) + (4.1277001E-2)*(T2*T2);
  Send488(K706,'B0461N0461');   {Open Ref Channel}
end;
procedure GetPowerSettings;
var
  InputV, InputI, IPower :single;
begin
  write('Enter Input Voltage ');
  readln(InputV);
  write('Enter Input Current ');
  readln(InputI);
  IPower:=InputV*InputI;
  append(DataFile);
  writeln(DataFile, 'Input Voltage = ', InputV);
  writeln(DataFile, 'Input Current = ', InputI);
  writeln(DataFile, 'Input Power = ', IPower);
  writeln(DataFile);
  close (DataFile);
end;
```

```
procedure ReadTemp(I:integer);
const CloseChannel: array [1..9] of string =
         ('B0471C0471X',
          'B0481C0481X',
          'B0491C0491X',
          'B0501C0501X',
          'B0462C0462X',
          'B0472C0472X',
          'B0482C0482X',
          'B0492C0492X',
          'B0502C0502X');
      OpenChannel: array [1..9] of string =
         ('B0471N0471X',
          'B0481N0481X',
          'B0491N0491X',
          'B0501N0501X',
          'B0462N0462X',
          'B0472N0472X',
          'B0482N0482X',
          'B0492N0492X',
          'B0502N0502X');
var
  measurement:string;
  CorV:single;
begin
  Send488(K706, CloseChannel[I]);
  Delay(10000);
  Enter488(K617,measurement,16);
  valSingle(copy(measurement,5,12),TestV);
  CorV:=RefVCor+TestV*1E6;
  TestT:=
2.5661297E-2*CorV-6.1954869E-7*(CorV*CorV)+2.2181644E-11*(
CorV*CorV*CorV);
  TestT:= TestT + -3.5500900E-16*(CorV*CorV*CorV*CorV);
  Send488(K706, OpenChannel[I]);
  Delay(1000);
end;
begin
  Init;
  RefMeasure;
  repeat
    ClrScr;
    GetPowerSettings;
    repeat
      inc(ArrayPos);
      writeln('Place Probe in Array Position #',
ArrayPos);
      write('Press <Enter> when ready');
      readln;
      append(DataFile);
      for i:= 1 to 9 do begin
```

```
        ReadTemp(I);
        writeln(DataFile, ArrayPos, '     ', I, '     ',
TestV, '     ', TestT);
        writeln(ArrayPos, '     ', I, '     ', TestV, '
', TestT);
      end;
      writeln(DataFile);
      close(dataFile);
      write('Another Array Position (Y/N)?');
      readln(Query);
    until (Query in ['N','n']);
    ArrayPos:=0;
    write('Another Power Setting (Y/N)?');
    readln(Query);
  until (Query in ['N','n']);
end.
```

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