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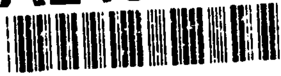

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GATE DRAIN GEOMETRY EFFECT ON THE CURRENT VOLTAGE CHARACTERISTICS OF GaAs MESFETS

Jon S.H. Schoenberg, Capt, USAF and Edward Cohen

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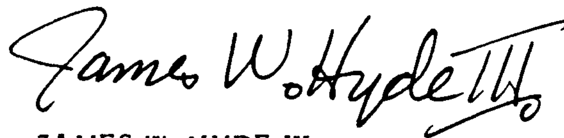

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We investigated the effect of gate-drain distance on GaAs MESFET current-voltage characteristics. DC characteristics of several GaAs MESFETS are determined and compared to results from a computer implementation of a physically based, analytical model by Chang and Day. Their model is modified to account for the effect of longer gate-drain distance, and shows excellent agreement with measured I-V curves across the full range of device geometrics tested.

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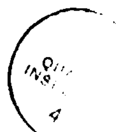

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Gate-Drain Geometry Effect on the Current-Voltage Characteristics of GaAs MESFETS

1. INTRODUCTION

Most of the gallium arsenide (GaAs) MESFET modeling work to date has neglected to quantify the effects of gate to drain geometry on device current-voltage (I-V) characteristics[1]. A physical model by Chang and Day was recently reported[2] which includes the effects of the gate to drain distance L_{DG} and appears to agree well with measured data for short gate-drain spacing encountered in typical GaAs FETs. Recent interest in large signal non-linear modeling for power amplifier design requires accurate knowledge of the I-V characteristics of the MESFETs, but relies on empirical methods to obtain the I-V curves[3,4]. An accurate computer-based model providing accurate DC characteristic simulation based on MESFET physical dimensions and materials properties would reduce the design time of large signal amplifiers. Although the computer model presented here uses measured data as inputs to the simulation to explore the effect of

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[1]Pucel, R. A., Haus, H. A., and Statz, H. (1975) Signal and noise properties of gallium arsenide microwave field effect transistors, in Advances in Electronics and Electron Physics, Vol 38, Academic Press, New York, pp 195-265.

[2]Chang, C-S and Day, D-Y S. (1989) Analytic theory for current-voltage characteristics and field distribution of GaAs MESFET's, IEEE Trans. Electron Devices **ED-36**(No. 2):269-280.

[3]Hwang, V. D., Shih, Y-C., Le, H. M., and Itoh, T. (1989) Nonlinear modeling and verification of MMIC amplifiers using the waveform-balance method, IEEE Trans. Microwave Theory and Techniques **MTT-37**(No. 12):2125-2133.

[4]Curtice, W. R. (1988) GaAs MESFET modeling and nonlinear CAD, IEEE Trans. Microwave Theory and Techniques **MTT 36**(No.2):220-230.

gate-drain distance, the program may be easily modified so that physical and material properties of the GaAs FET are all that are necessary to provide accurate results.

Although the Chang-Day model provides good results for short L_{DG} distances up to 4 micrometers, we report a modified model that is experimentally verified with GaAs FETs with L_{DG} ranging up to 12 micrometers (μm). To determine the range of validity of this model, and to provide a data base of measured data for testing improved models, this paper describes the results of a comprehensive set of GaAs FET measurements. Ten MESFETs with L_{DG} ranging from 3μm to 12μm were fabricated and tested on a common semi-insulating GaAs wafer. Data collected from DC FET parameter measurements were inputs to a computer program based on the Chang-Day model to plot simulated I-V curves to which measured I-V characteristics were compared. The model was modified to incorporate experimentally determined values of pinch-off voltage and to better predict the I-V characteristics of longer L_{DG} devices.

The Chang-Day model was selected for our MESFET modeling because (1) it incorporates a realistic electron drift velocity-electric field relationship[5] and (2) the model simultaneously solves the two-dimensional Poisson equation and diffusion equation in closed form. Therefore, a full set of I-V curves can be obtained within seconds based on experimentally determined MESFET parameters. Another approach to simultaneously solving the two-dimensional Poisson's equation and diffusion equation using numerical simulation was tried using Frensley's model.[6] Using this model requires thousands of mesh points to define the entire active region of our longer devices. These mesh points must be constantly updated throughout the simulation, leading to lengthy computer simulation time. Numerical simulation clearly showed the high field region near the gate edge of the ungated region between the gate and drain. However, calculated I-V results vary widely from experimental data because of the uncertainties in FET physical parameters such as diffusion coefficients and channel thickness.

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[5]Chang, C-S, and Fetterman, H. R. (1986) Electron drift velocity versus electric field in GaAs, Solid State Electronics **29**:1295-1296.

[6]Frensley, W. R. (1981) Power-limiting breakdown effects in GaAs MESFET's, IEEE Trans. Electron Devices **ED-28**(No. 8):962-970.

We developed a FORTRAN program based on the Chang-Day model to derive a full set of I-V characteristics. The program uses Chang and Day's physically based analytical solution assuming a uniformly doped active layer. Results from the computer model are compared to a family of MESFETs designed and tested at RADC and fabricated at a foundry. Distance L_{DG} is the only parameter varied among the MESFETs, making them particularly well suited to modeling the I-V characteristics as a function of L_{DG}, holding all other MESFET physical parameters constant.

2. DESCRIPTION OF EXPERIMENTAL WORK

The family of MESFETs studied were fabricated and tested on a 250μm thick semi-insulating GaAs substrate. The N-type channel is Si^{29} ion-implanted at a dual energy of 120KeV/30KeV. The n^+ contact implants as well as the channel implant are activated by furnace annealing with As-overpressure. Ni:Ge:Au:Ni ohmic metal was evaporated on the n^+ contact regions and alloyed. Mesa isolation provides device isolation. The Ti:Pt:Au 1μm gate is self-aligned in a recessed channel etched for a nominal pinch-off voltage of 2.5 volts. Polyimide passivates exposed channel regions, and Ti:Pt:Au overlay metal is evaporated to a thickness of 1.2 μm for low resistance contacts at the probe pads.

All MESFETs tested have 6-finger interdigitated gate topology, 1μm gate length and 600μm total gate width. Figure 1 shows the gate topology and the three segmented drains that evenly divide the gate periphery. Therefore, the effective gate width for each MESFET segment is 200μm. Each MESFET segment has a unique gate to drain distance L_{DG} defined as the distance between the drain-side edge of the gate and the gate-side edge of the drain as shown in Figure 2. The segmented-drain topology isolates L_{DG} as the only physical parameter that changes when comparing the I-V characteristics among MESFET segments with the same source, gate, Schottky barrier, and channel characteristics. MESFETs were designed with L_{DG} ranging from 3.0μm to 12.0μm in 1 μm increments. In addition, each MESFET contains one reference drain segment to facilitate matching devices with similar pinch-off voltage, parasitic source and gate resistance, and built-in voltage, again isolating the effect of L_{DG} on the I-V curves.

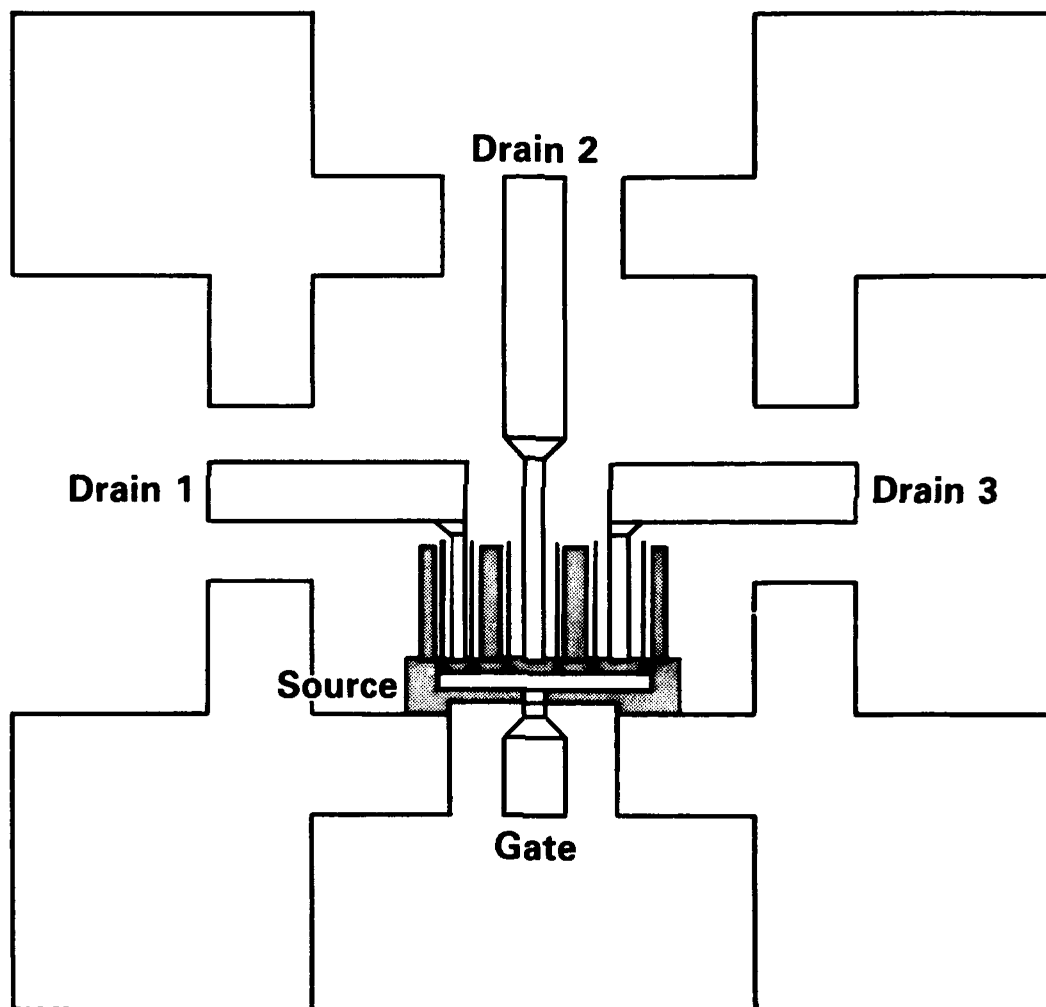

FIGURE 1. Topology of the segmented-drain MESFET with three drains. Each MESFET segment has two gate fingers and 200 μm gate periphery. The shaded region designates source metal. Source metal is bridged over the gate. Drain contacts are compatible with on-wafer coplanar waveguide probe heads with a 4 mil pitch. Note the different gate-drain distances among the three MESFET segments.

Figure 2. (a) Cross-section of MESFET active region defining the critical dimensions used in the computer modeling. (b) Electric field profile along the channel. (c) Electron drift velocity profile along the channel showing field-dependent drift velocity used in the computer model (after Chang and Day, Ref. 2).

DC measurement techniques developed by Fukui[7] were employed to determine the Schottky barrier potential V_{bi}, extrinsic pinch-off voltage V_p, active channel donor density N_D, thickness a, and resistance R_O, as well as parasitic source, gate, and drain resistances R_{SM}, R_G, and R_{DM} respectively. Expressions relating a MESFET's intrinsic channel characteristics with its extrinsically measured parameters are essential to modeling its I-V curves. From Refs. 7 and 1 the gate-to-channel potential W_p required to fully deplete the channel of carriers is given by

$$W_p = \frac{qN_D a^2}{2\epsilon_s} , \quad (1)$$

where q is the electron charge = 1.602×10^{-19} C and $\epsilon_s = \epsilon_r \epsilon_0$ is the dielectric permittivity of the channel. For GaAs, a value of $\epsilon_r = 13.1$ is used throughout our FET modeling. The extrinsically measured pinch-off voltage is related to the channel pinch-off potential by

$$V_p = W_p - V_{bi} . \quad (2)$$

Therefore, the experimentally determined values of V_{bi} and V_p must be added before calculating the channel donor density and thickness. Although not explicitly stated in the Chang-Day model, $V_p = W_p - V_{bi}$ is incorporated into our implementation of the model to properly relate the terminal pinch-off voltage with the channel thickness and donor density.

The second equation required to uniquely determine N_D and a is their relationship to the measured saturation current I_S:

$$I_S = qN_D a Z v_s , \quad (3)$$

where Z if the channel width = 200μm for all MESFETs tested and v_s is the electron saturation drift velocity. The saturation drift velocity in n–GaAs is determined as the temperature dependent value[8]

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[7]Fukui, H. (1979) Determination of the basic device parameters of a GaAs MESFET, AT&T Bell System Technical Journal 58(No 3):771-797.

[8]Sze, S.M. (1981) Physics of Semiconductor Devices, 2nd ed., Wiley, New York.

$$v_s(T) = v_O - \alpha T \ , \tag{4}$$

where $\quad v_O = 12 \times 10^6$ cm/sec ,

and $\quad \alpha = 0.015 \times 10^6$ cm/sec–K .

At room temperature, $v_s = 7.5 \times 10^6$ cm/sec, the value used throughout our MESFET modeling.

Determining N_D and a require experimentally determined values of V_{bi}, V_p and I_S. The Schottky barrier built-in voltage V_{bi} found in Refs. 1 and 6 is

$$V_{bi} = \frac{kT}{q} \ln\left[\frac{A^* T^2}{J_S}\right] \ , \tag{5}$$

where A^* is the effective Richardson constant, T is the junction temperature, k is the Boltzmann constant, and J_S is the gate saturation current. Fukui's method is used to find J_S by a semi-logarithmic plot of gate current as function of gate forward bias and extrapolating to zero gate bias. Using $A^* = 8.7$ Amperes/cm^2–K^2 to account for the effective electron mass in n–GaAs at 300 K, the equation for V_{bi} reduces to:

$$V_{bi} = 0.350 - 0.0258 \ln(J_S) \ . \tag{6}$$

Tabulated values of V_{bi} determined for each MESFET are shown in Table 1.

Pinch-off voltage V_p is determined approximately by monitoring the drain source I-V characteristics as a function of gate-source bias V_G. Drain-source bias V_D is maintained at 0.05 volt to minimize depletion region variation along the channel. Extrapolating the $I_D - V_G$ plot to zero drain current provides an estimate of the pinch-off voltage V_p. This initial value of V_p is refined by a Fukui technique that plots the equivalent drain-source resistance $R_{DS} = V_D/I_D$ as a function of parameter X defined as

$$X = \left[1 - \sqrt{\frac{V_{bi} - V_G}{V_{bi} + V_p}}\right]^{-1} \ . \tag{7}$$

Table 1: Measured and calculated MESFET parameters

TABLE 1									
DEVICE L_{DG} (μm)	V_{bi} Volts	V_p Volts	R_{SM} OHMS	R_{DM} OHMS	R_G OHMS	R_O OHMS	N_D $X10^{16}$ Cm^{-3}	a μm	I_S MA
FI 445 3.0	0.636	2.39	2.30	11.5	35.5	5.08	16.7	0.1620	65.0
FI 445 4.0	0.636	2.39	2.3	13.8	35.5	5.08	16.7	0.1620	65.0
FI 555 5.0	0.653	2.28	1.80	17.3	36.4	5.40	17.4	0.1565	65.2
FI 665 6.0	0.659	2.45	2.0	20.0	36.3	5.50	15.9	0.1682	64.3
FI 775 7.0	0.64	2.46	2.85	24.1	36.1	5.34	16.7	0.1616	64.6
FI 885 8.0	0.658	2.50	2.33	27.7	36.1	5.29	16.3	0.1675	65.6
FI 995 9.0	0.635	2.28	1.44	30.8	37.1	5.71	16.5	0.1602	63.3
FI 10105 10.0	0.64	2.49	2.80	35.6	36.2	5.01	15.7	0.1699	64.1
FI 1115 11.0	0.64	2.49	1.78	37.7	36.5	5.08	15.9	0.1689	64.5
FI 12125 12.0	0.658	2.30	1.35	41.8	36.7	5.35	16.3	0.1623	63.4
$\overline{X}$	0.646	2.40	2.10		36.2	5.28	16.4	0.1639	64.5
σ	0.01	0.09	0.51		0.49	0.22	0.50	0.0044	0.75

The R_{DS}–X relationship is linear for the correct value of V_p. The initial value of V_p is tried and adjusted until a linear relationship is found. The linear R_{DS}–X plot yields the parasitic resistances R_{SM}, R_{DM}, and R_O. Linear extrapolation of the plot to the ordinate yields $R_{SM} + R_{DM}$. Gate I-V characteristics are recorded as suggested by Fukui in Ref. 7 for a gate current density of 10^4 A/cm^2. For a 200μm gate periphery, gate bias readings at 20 mA gate current were recorded to determine the effective resistance in common-source and common-drain configurations. The difference between the common-source and common-drain resistances yields the quantity $R_{SM} - R_{DM}$. Combining it with $R_{SM} + R_{DM}$ obtained from the R_{DS}–X plot (Figure 3) provides the measured values of source and drain resistances used in our model and tabulated in Table 1. The value of R_{DM} is plotted as a function of L_{DG} in Figure 4, showing a linear relationship. The plot extrapolates to the origin indicating a very low ohmic contact resistance. As seen in Table 1, R_{DM} is the distinguishing parameter that varies across the device samples.

The saturated channel current I_S is determined from the drain I-V characteristics to be

$$I_S = I_F - I_{SUB} \; , \tag{8}$$

where I_F is the fully undepleted channel current evaluated at $V_G = + V_{bi}$ and I_{SUB} is the substrate leakage current evaluated at $V_G = -V_p$ with V_D at the knee voltage. The value of I_S is critical to determining N_D and a. Rearranging Eq. (1) to solve for a^2 and substituting into Eq. (3) yields

$$N_D = \frac{1}{2\epsilon_s} \cdot \frac{1}{q\ v_s} \quad \frac{1}{V_p + V_{bi}} \left[\frac{I_S}{Z}\right]^2 \; , \tag{9}$$

with $W_p = V_p + V_{bi}$. For n–GaAs, Eq. (9) may be simplified to

$$N_D = \frac{4.79}{V_p + V_{bi}} \left[\frac{I_S}{Z}\right]^2 \; , \tag{10}$$

where N_D is in units of 10^{16} cm^{-3}, V_p and V_{bi} in volts, I_S in amperes, and Z in cm. In a similar fashion, the channel depth a is found to be

$$a = 2\epsilon_s v_s W_p \frac{Z}{I_S} \quad . \tag{11}$$

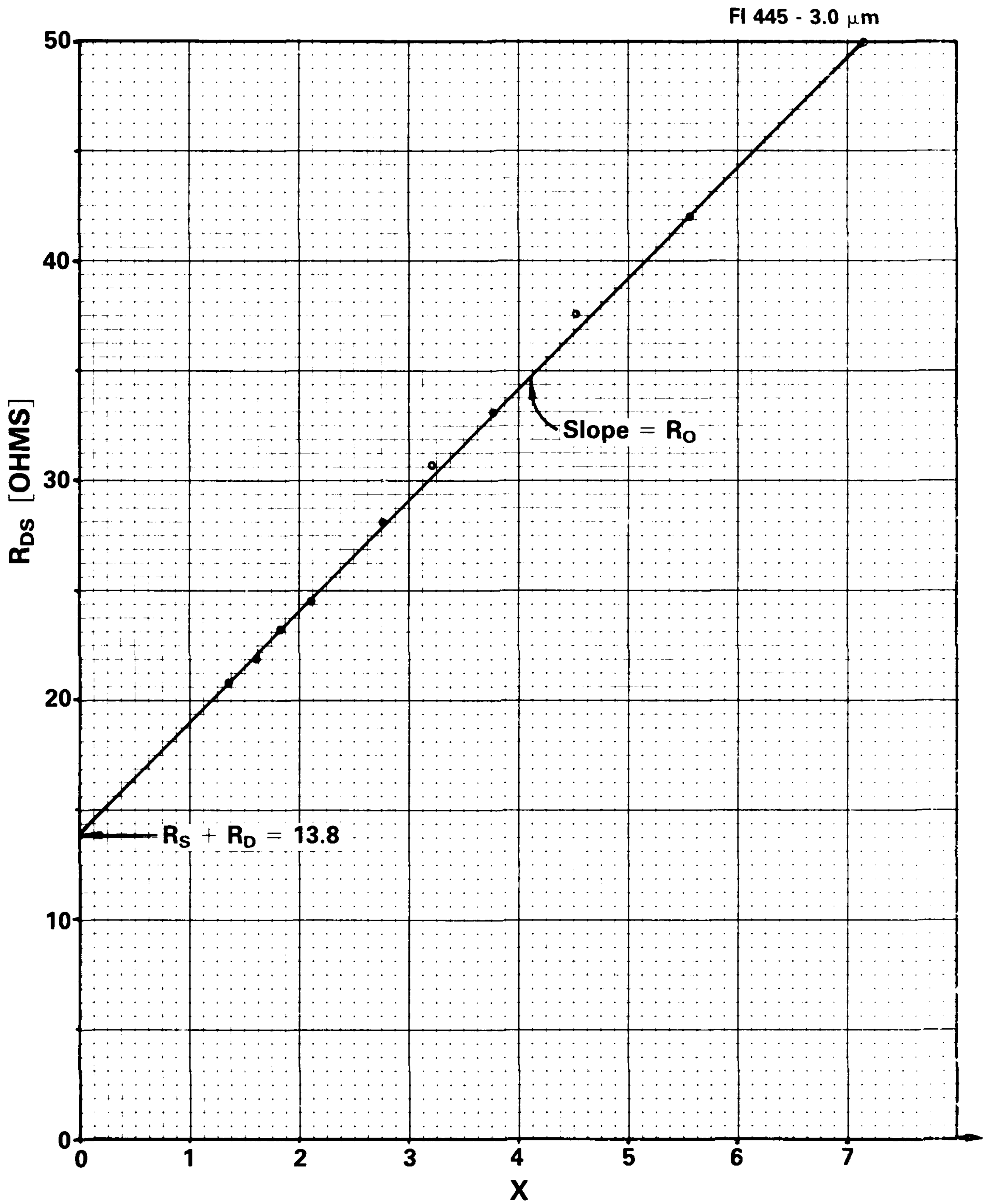

Figure 3. Plot of R_{DS}-X used to determine parasitic resistances R_S, R_D, and R_O.

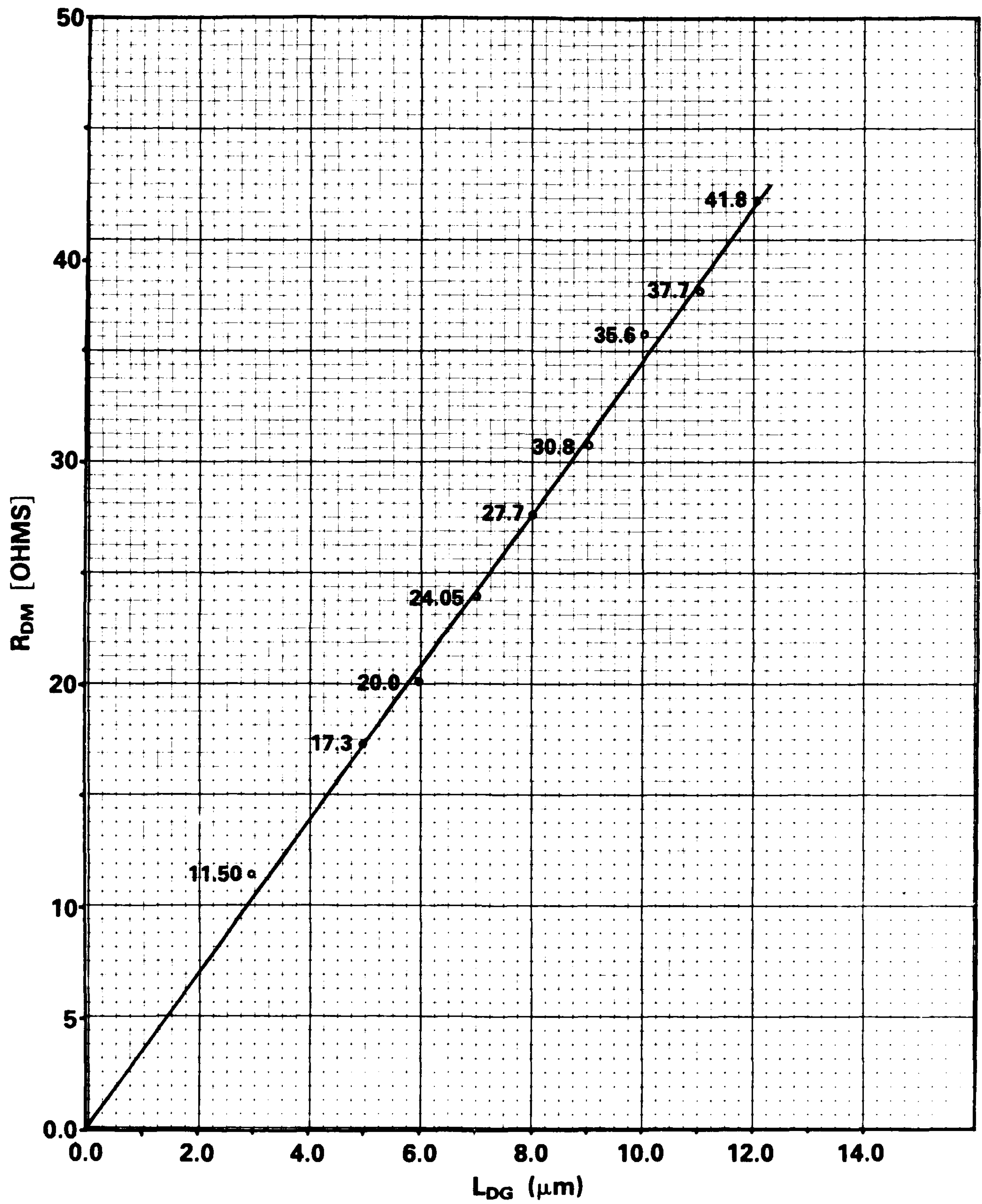

Figure 4. Plot of drain resistance R_{DM} as a function of gate-drain distance L_{DG} showing a linear relationship. The plot is extrapolated to the origin.

For n–GaAs, this expression simplifies to

$$a = 0.174(V_p + V_{bi}) \frac{Z}{I_S} \quad , \tag{12}$$

where a is in microns, I_S in amperes, and Z in cm. Therefore, N_D and a are derived from experimentally determined values of pinch-off voltage, built-in voltage, and channel saturation current.

All experimentally measured and derived parameters used for our MESFET modeling are tabulated in Table 1. Excellent agreement in all parameters is shown, with a standard deviation of less than 4 percent of mean value for all parameters except R_{SM}. The large deviation of R_{SM} may be attributed to the graphical method of its determination. R_{DM} is the distinguishing parameter among the devices due to the change in L_{DG}.

3. COMPUTER MODELING

A FORTRAN computer program was developed following the Chang-Day model which divides the channel into three regions as shown in Figure 2. Electric field and electron transport properties are incorporated into the solution of Poisson's equation and the diffusion equation in the gated low field region (region I), the gated high field region (region II), and the ungated high field region between the gate and drain (region III). A uniform doping profile in the active layer is assumed, which well represents the doping profile data provided by the foundry. The uniform profile assumption simplifies the equations developed by Chang and Day and makes computer solution for the three regions particularly efficient.

3.1 Linear Region

Following Eqs. (42) and (43) in Ref. 2, we calculate the channel current I_C for the linear region by solving the transcendental equation

$$F_{1,L} = I_C - \alpha \left\{ 3 \left[\left(\frac{h_l}{a} \right)^2 - \left(\frac{h_o}{a} \right)^2 \right] - 2 \left[\left(\frac{h_l}{a} \right)^3 - \left(\frac{h_o}{a} \right)^3 \right] \right\} \quad , \tag{13}$$

where

$$\alpha = \frac{q^2 N_D Z \mu a^3}{6 \epsilon_s L} \quad , \tag{13a}$$

with

$$\left(\frac{h_l}{a} \right) = \left[\frac{V_{bi} - V_G + V_D - I_C R_D}{W_p} \right]^{\frac{1}{2}} \quad . \tag{14}$$

$$\left(\frac{h_o}{a} \right) = \left[\frac{V_{bi} - V_G + I_C R_S}{W_p} \right]^{\frac{1}{2}} . \qquad (15)$$

and

The maximum linear range drain voltage $V_{D,LMAX}$ in Eq. (44) of Ref. 2 is used in Eq. (11) above and is itself a function of I_C. We increment I_C until the transcendental equation $F_{1,L} = 0$ with $V_D = V_{D,LMAX}$ in Eq. (14). The maximum channel current-drain voltage point $(I_{C,LMAX}, V_{D,LMAX})$ establishes the upper bound of the linear region.

Next, the interior $I_C - V_D$ points of the linear region are determined, namely those $I_C - V_D$ values that satisfy

$$0 < I_C \le I_{C,LMAX} ,$$
$$0 < V_D \le V_{D,LMAX} . \qquad (16)$$

For a given value of I_C, V_D may be obtained explicitly by rewriting Eq. (13) in the form:

$$\left(\frac{h_l}{a} \right)^3 - \frac{3}{2} \left(\frac{h_l}{a} \right)^2 + \left[\frac{I_C}{2\alpha} + \frac{3}{2} \left(\frac{h_o}{a} \right)^2 - \left(\frac{h_o}{a} \right)^3 \right] = 0 . \qquad (17)$$

Since h_o is a function of I_C and not V_D, we have a cubic equation for $\left(\frac{h_l}{a} \right)$ as a function of I_C. Solving for $\left(\frac{h_l}{a} \right)$ explicitly, we obtain a corresponding value of V_D by Eq. (14). A sufficient number of $I_C - V_D$ points are calculated for the I-V curve plotting using commercial software plotting routines.

3.2 Knee Region

The knee region is defined as the current-voltage values satisfying

$$I_{C,LMAX} < I_C \le I_{C,KMAX}$$
$$V_{D,LMAX} < V_D \le V_{D,KMAX} \qquad (18)$$

with $(I_{C,LMAX}, V_{D,LMAX})$ determined from the linear region solution as the lower bound. The next step is to obtain the upper bound of the knee region $(I_{C,KMAX}, V_{D,KMAX})$. Following Ref. 2, $V_{D,KMAX}$ is derived if we let

$$\left(1 - \frac{h_l}{a} \right) \; [illegible] \; C \; [illegible] = C' , \qquad (19)$$

where $$C = \frac{E_C}{E_L} \quad \text{(a constant)} \quad . \tag{20a}$$

and $$r = \frac{I_C}{I_S} \quad , \tag{20b}$$

where $E_C = v_s/\mu$ is the critical electric field and the maximum field in the linear region E_L is defined as

$$E_L = \frac{1}{2}\left[E_T + \sqrt{E_T{}^2 - 4E_C{}^2}\ \right] \quad , \tag{21}$$

where E_T is the threshold electric field where the electron drift velocity is maximum. Rearranging Eq. (19), we have

$$\left(\frac{h_l}{a}\right)^2 = (1 - rC')^2 \quad . \tag{22}$$

Substituting into Eq. (14) and solving for V_D yields the expression for $V_{D,KMAX}$

$$V_{D,KMAX} = W_p\ (1-rC')^2 - V_{bi} + V_G + I_{C,KMAX}\ R_D \quad . \tag{23}$$

The other consequence of setting $\beta_L = C'$ is that $U_b = 0$ as defined in Eq. (49b) of Ref. 2. The I_C–V_D relationship at $V_{D,KMAX}$ is now given by Eqs. (48) and (46) in Ref 2 as

$$L - \frac{W_p}{E_T}\ (U_a + U_c) - [\text{Eq.(46) of Ref. 2}] = \frac{f_2{}^{MAX}}{r} = 0 \quad . \tag{24}$$

Inserting the expression for Eq. (46) of Ref. 2 and defining X,

$$X = \left(\frac{h_o}{a}\right)^2 = \left[\frac{V_{bi} - V_G + R_S\ I_S\ r}{W_p}\right] \tag{25}$$

into Eq. (24) above will lead to an expression for X that may be solved to get $I_{C,KMAX}$. Observing that

$$r = AX + B\ , \tag{26}$$

where $$A = \frac{V_p}{I_S R_S} \quad , \tag{26a}$$

and $$B = \frac{-\ (V_{bi} - V_G)}{I_S R_S} \quad , \tag{26b}$$

then from Eq. (14) with $V_D = V_{D,KMAX}$, one obtains

$$\left(\frac{h_l}{a} \right) = (-C'A)\ x + (1-C'B)\ . \tag{27}$$

Also, from Eq. (17) of Ref. 2

$$\left(\frac{h_a}{a} \right) = (-CA)\ x + (1-CB)\ . \tag{28}$$

Substituting Eqs. (27), (28), and (25) into Eq. (24) and performing some tedious algebra leads to the "pseudo" cubic equation

$$f_2 = b_0 + b_1 x + b_2 x^2 + b_3 x^3 + b_4 x^{\frac{3}{2}} = 0\ . \tag{29}$$

The coefficients b_m are given by long algebraic expressions calculated in a subroutine of the program. Equation (29) is solved using a Newton-Raphson routine with starting value $X_0 = \left(\frac{h_o}{a} \right)^2$ evaluated at $I_{C,LMAX}$, the known lower bound of the channel current in the knee region:

$$X_{n+1} = X_n - \frac{f_2(X_n)}{f_2'(X_n)} \qquad n = 0, 1, 2, \ldots\ . \tag{30}$$

It follows that the maximum channel current in the knee region is given as

$$I_{C,KMAX} = \frac{[W_p X_{final} - V_{bi} + V_G]}{R_S}\ . \tag{31}$$

Channel length L_A, where the electric field is less than E_L, can be determined by Eq. (48) of Ref. 2 at ($I_{C,KMAX}$, $V_{D,KMAX}$). Channel length L_b, where $E_l < E < E_T$, is calculated using Eq. (52) of Ref. 2. With L_a and L_t determined, the gated channel saturation length L_2 is simply

$$L_2 = L - L_a - L_b\ . \tag{32}$$

With the knee region bounds specified, the interior points are then determined by specifying a value of V_D and calculating the corresponding value of I_C to solve Eq. (48) of Ref. 2 where $U_b \neq 0$.

3.3 Saturation Region

The saturation region is defined as the current and voltage values satisfying

$$\begin{aligned} I_{C,KMAX} &< I_C < I_{C,MAX} \\ V_{D,KMAX} &< V_D \leq V_{D,MAX}\ . \end{aligned} \tag{33}$$

where $V_{D,KMAX}$ is the terminal drain bias and $I_{C,MAX}$ is the maximum attainable channel current for a given (V_G, $V_{D,MAX}$) bias condition. This region's bounds are completely defined except for $I_{C,MAX}$. To determine the I_C–V_D characteristics in the saturation region, we increment the channel current by ΔI_C starting with the lower bound $I_{C,KMAX}$ such that

$$I_C = I_{C,KMAX} + \Delta I_C \quad . \tag{34}$$

Channel lengths L_a, L_b, and L_2 are then calculated. The current I_C is iteratively incremented until L_a becomes negative (indicating a fully saturated channel). $I_{C,MAX}$ is the maximum possible channel current and defines the upper bound of the channel current in the saturation region.

For each incremental value of I_C, the ungated saturation distance L_3 must be calculated to determine the corresponding V_D. L_3 is obtained by solving the transcendental equation Eq. (18) from Ref. 2. We define function f_3 such that

$$f_3 = L_3^2 - [\text{the right hand side of Eq. (18) in Ref. 2}] = 0 \tag{35}$$

Using a Newton-Raphson method, L_3 is iteratively determined using function f_3 and its derivative $f_3' = df_3/dL_3$. A starting value of $L_3 = 10^{-4}$ cm is used since it is expected that the high field region length is approximately this length[9]. With L_3 known, the quantity

$$\Delta V = V(L_3) - V(-L_2) \tag{36}$$

given by Eq. (19) of Ref. 2 can be calculated. It follows that

$$V(L_3) = V_{D,KMAX} + \Delta V \quad . \tag{37}$$

Careful investigation shows that

$$V_D = V(L_3) + I_C R_D \quad . \tag{38}$$

With channel current I_C and corresponding drain voltage V_D determined, I_C is converted to I_D to account for the substrate leakage current. Therefore

$$I_D = I_C + \frac{V_D}{R_P} \quad , \tag{39}$$

[9]Shur, M. S. (1987) GaAs Devices and Circuits, Plenum Press, New York:p.344

where V_D/R_p corresponds to the substrate leakage current I_{SUB}. Measured I_{SUB} at the I-V knee voltage yielded a typical value of R_p = 2500 Ω, which is the value used in this model.

The computer program sequentially finds the I-V relationship in all three regions for discrete values of V_G. A complete set of I-V curves can be calculated and displayed within seconds with the computer model.

4. SIMULATION RESULTS AND MODELING OF GATE-DRAIN REGION

Figure 5 shows the I-V modeling compared with experimental results for two MESFETs with radically different values of L_{DG} (and thus R_D). The MESFET with the lower knee voltage has L_{DG} = 4μm. The second FET has L_{DG} = 12μm. The values in Table 1 specific to the two devices are input parameters in the MESFET model. Excellent agreement between the modeled and measured data is evident, especially with the shorter device.

In order to explain the effect that L_{DG} has on MESFET I-V characteristics, we can begin with the development of Chang of Day in which

$$R_D = R_{DM} + R(V_G) \ , \tag{40}$$

where

$$R_{DM} = R_{dc} + \frac{L_{DG}}{qN_pZ\mu(t-t_o)} \ . \tag{41}$$

is the experimentally determined value of the parasitic drain resistance and

$$R(V_G) = \frac{h}{qN_DZ\mu}\left[\frac{1}{a-h} - \frac{1}{t-t_o}\right] \ . \tag{42}$$

R_{dc} is the drain contact resistance, t_o is the surface depletion width due to surface states on the ungated channel, t is the total active layer thickness, and the depletion width h is

$$h = \sqrt{\frac{2\epsilon_s}{qN_D}\,(V_{bi} - V_G)} \ . \tag{43}$$

Notice that our experimental determination of R_{DM} as a function of L_{DG} is accounted for in Eq. (41). Figure 4 shows that R_{dc} is essentially zero, which is in agreement with drain contact data provided by the foundry.

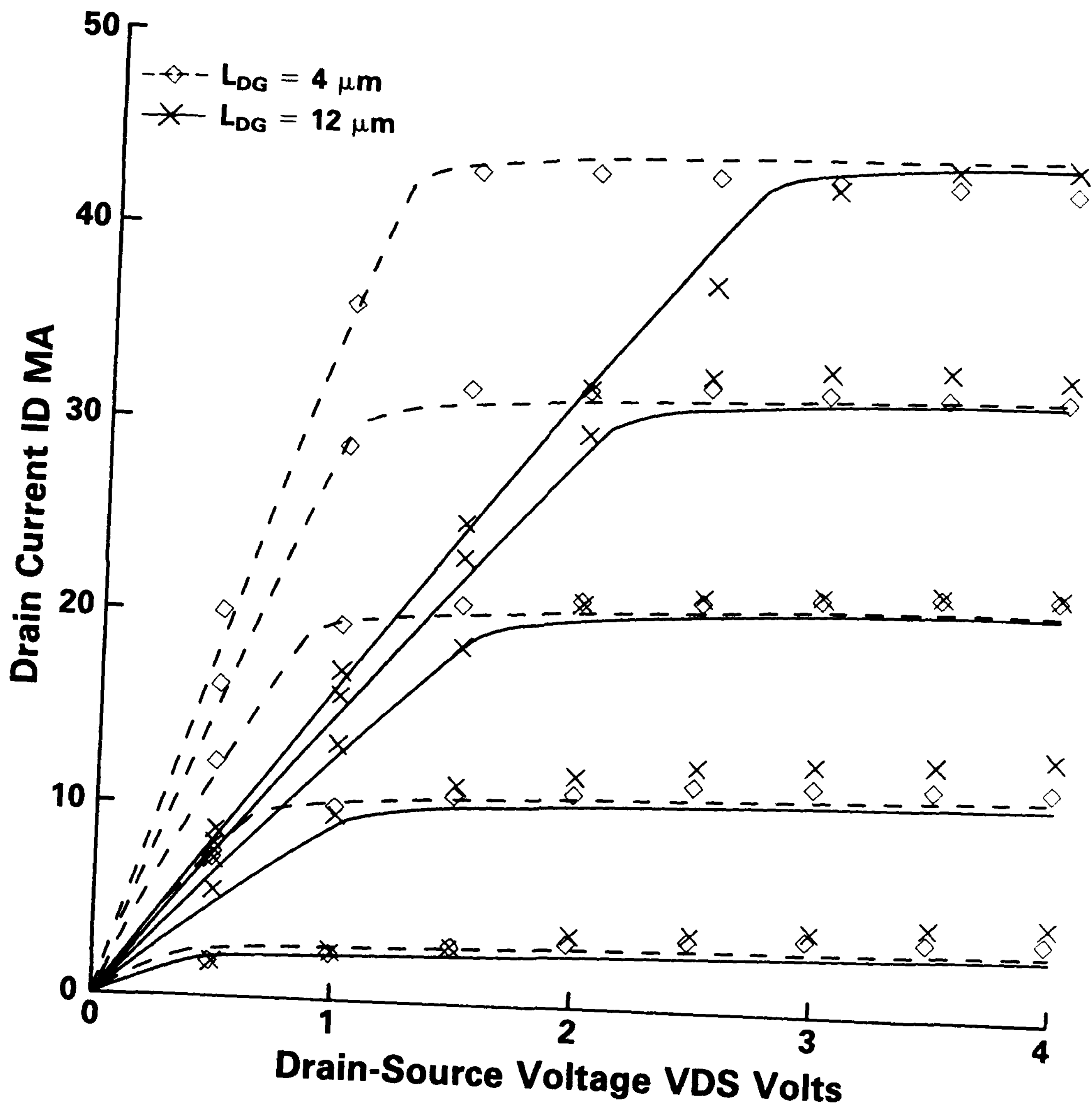

Figure 5. Current-voltage plots generated by the computer model compared with measured data. MESFETs with L_{DG} = 4 μm and L_{DG} = 12 μm are compared, showing the greater drain-source bias required to saturate the longer (12 μm) device.

Furthermore, the slope of the R_{DM}–L_{DG} plot yields the undepleted channel thickness $t - t_o$ in the ungated region between the gate and drain. Rearranging Eq. (41) we obtain

$$(t - t_o) = \frac{1}{qN_DZ\mu} \frac{\Delta L_{DG}}{\Delta R_{DM}} \quad . \tag{44}$$

Using the mean value of $N_D = 1.64 \times 10^{17}$ cm^{-3} and the modeling value of $\mu = 4.0 \times 10^3$ cm^2/v–sec, we obtain a value of $(t - t_o) = 0.1375\mu m$. The depletion width h varies between $0.076\mu m$ at $V_G = 0$ volts and $0.1530\mu m$ at $V_G = -2.0$ volts. For the experimentally determined mean channel thickness $a = 0.1639\mu m$, $R(V_G)$ ranges from 0.15 Ω at $V_G = 0$ volts to 6.15 Ω at $V_G = -2.0$ volts. It should be noted that $R(V_G)$ rapidly approaches very large values as V_G approaches pinch-off.

Chang and Day introduce a scaling parameter s to allow more flexibility in fitting the model to measured data, in which R_D and R_S are taken as

$$R_D = R_{DM} + sR(V_G) \tag{45}$$

$$R_S = R_{SM} + sR(V_G) \quad . \tag{46}$$

A value of $s = 1$ proved to be adequate for our short L_{DG} devices, but as L_{DG} increased, a discrepancy between the model and measured data in the knee region developed, most notably for low V_G. Figure 6 clearly shows this for our $L_{DG} = 12\mu m$ device. The model did not provide adequate channel resistance at low gate bias to fit the data.

To remedy this problem, the channel resistance $R_O(V_G)$ as determined by Fukui in Ref. 7 is added to the source resistance, yielding

$$R_S = R_{SM} + R_{SG}(V_G) \quad , \tag{47}$$

where $$R_{SG}(V_G) = R_O \left[1 - \sqrt{\frac{V_{bi} - V_G}{V_p + V_{bi}}} \right]^{-1} \quad . \tag{48}$$

When this additional term is added to R_S, the model more closely follows the measured results. Figure 5 shows an overlay of the measured and modeled I-V characteristics for a $L_{DG} = 4\mu m$ and a $L_{DG} = 12\mu m$ MESFET. The model shows good agreement with experimental data in the linear and knee region for all

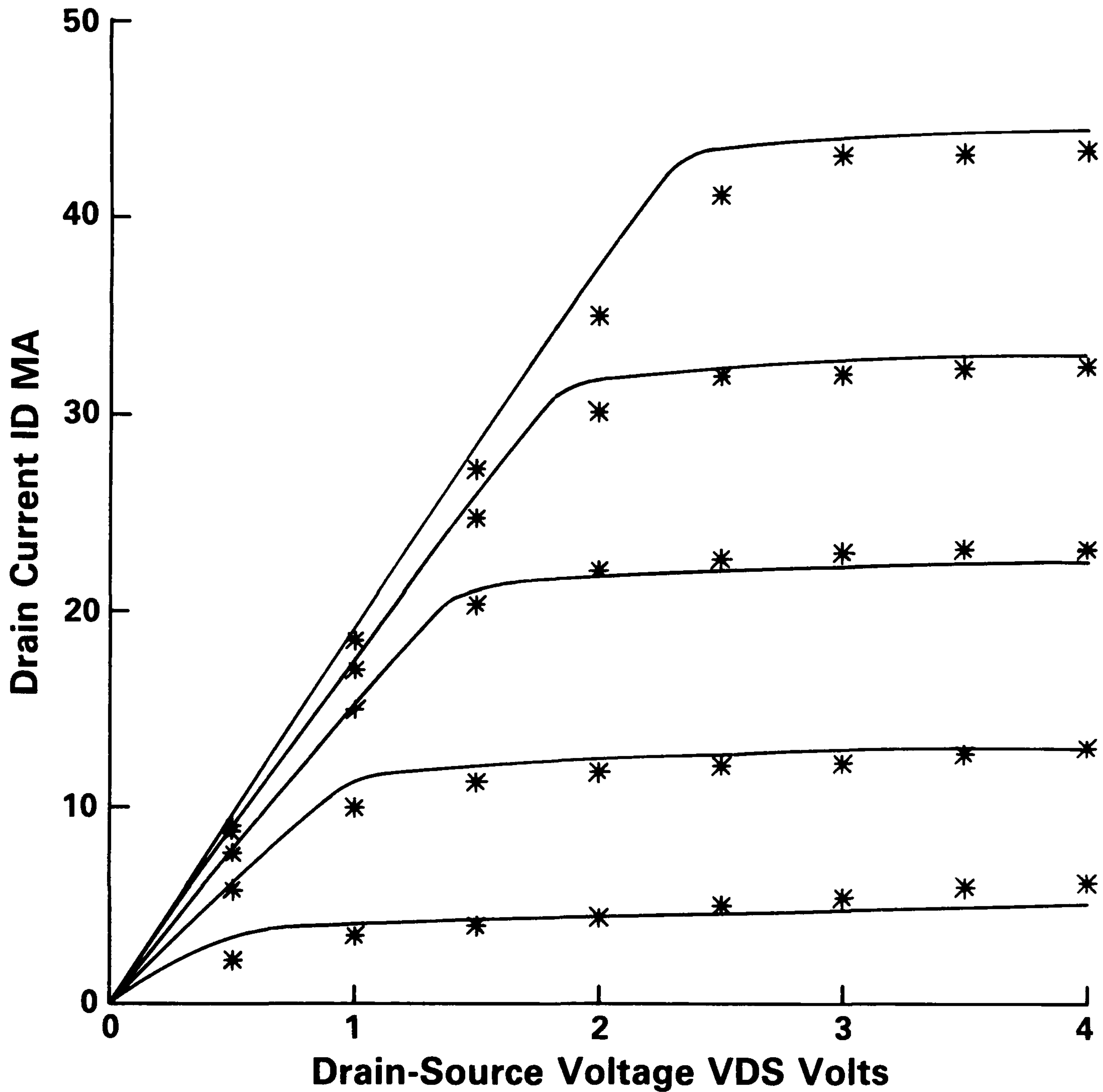

Figure 6. Current-voltage simulation of a MESFET with L_{DG} = 10 μm showing the deviation between the model and measured data for low gate bias in the knee region. The text describes a modification to the model reducing this deviation as shown in Figure 5.

gate biases. In the saturation region, better agreement occurs for lower L_{DG} than for higher V_G, in which the channel current is depressed due to the higher values of $R_{SG}(V_G)$ at these gate biases.

5. CONCLUSION

A computer program based on the physically derived Chang-Day model was developed to describe the drain current-voltage characteristics of GaAs MESFETs. Experimental analysis of a family of MESFETs with various gate-drain distances determined the input parameters to the model. Experimental and modeled results were compared to study the model's effectiveness at predicting the effect of varying gate-drain distance on the drain I-V curves. The model was modified to show better agreement between measured and modeled results in the linear and knee regions across the full range of devices analyzed. The computer model may be easily modified such that all inputs to the model are physical dimensions or quantities, thereby eliminating the need to perform Fukui-type DC tests on devices before simulation. Designers of GaAs MMICs may then find the model useful in predicting the DC operating point of integrated GaAs MESFETs for large-signal design and simulation.

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