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Department Approval: Howard S. Babbitt, III

MITRE Project Approval: Joel Mathews

ABSTRACT

This report describes the design and measured performance of a superconducting Josephson array oscillator. An array of Josephson junctions was fabricated to function as a 12 to 18-GHz frequency agile voltage controlled oscillator for application in analog-to-digital conversion. At a temperature of 4.2 K, measured peak RF power was approximately -84 dBm in a 300 kHz bandwidth. This work was performed in support of MITRE Sponsored Research project 91080, Superconducting Analog-to-Digital Converters.

EXECUTIVE SUMMARY

BACKGROUND

The MITRE sponsored research (MSR) initiative to investigate applications of superconductivity in technically challenging areas of application -- especially, analog-to-digital signal converters -- quickly focused on several subcomponent devices. Because of the generally recognized precise relationship of the Josephson junction oscillating frequency to the voltage across the junction, the group investigating the application elected to focus some of its attention on these devices as a converter component. We sought to understand how to effectively use these junctions with their inherent quantum precision in analog-to-digital converters. Initial analysis showed that individual junctions were impractical; their individual power and impedance levels tended to be too low (fractions of picowatts and ohms, respectively); and their output bandwidth too large.

INVESTIGATION STRATEGY

MITRE chose to investigate arrays of Josephson junctions, teaming with a physics department research group at the State University of New York at Stony Brook (SUNY). MITRE investigators explained our system problem to physicists there, who for several years had worked on stabilizing arrays of junctions. Meanwhile, we developed a cryogenic laboratory capability to be able to make performance measurements on superconductor devices.

ANALYSIS

When our preliminary models suggested promising application possibilities for the superconducting A/D converter (SADC) application, we asked SUNY for design and fabrication support. They created improved designs and fabricated custom lithographic array patterns. They made working oscillator devices, measured performance of them first, and then supplied several working oscillators to MITRE.

EVALUATION RESULTS

The concept of the array as a controlled and coherent oscillator has been demonstrated, with output in the desired frequency range. MITRE's measurement of power output indicated less than ideal power output and the report covers possible reasons for this. Nevertheless, the oscillators work. In addition, SUNY has recently measured the agility of their devices to shift output frequencies (by rapidly modulating the driving bias) while operating at a frequency in the 12 to 18-GHz range and believes the device's frequency agility is better than that of any other known device type in this regard.

ACKNOWLEDGMENTS

Credit is due to R. J. Murray, J. E. Devine, and M. Miana for meticulous engineering assistance. D. E. Loeber and T. L. Taylor, respectively, designed and tested parts of the measurement instrumentation. Technical insight by Dr. J. M. Schoen has kept the effort focused on the research goals of the project and has contributed to the significance of this work.

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SECTION 1

DIGITAL CONVERTERS AND SUPERCONDUCTOR DRIVERS

The MITRE research project to investigate ways of converting analog voltage signals into digital format -- analog-to-digital conversion -- included a program to investigate superconductor components of a converter design. This paper reports on the design and evaluation of a superconductive voltage-controlled oscillator (VCO) as an essential component of a superconducting analog-to-digital converter.

1.1 SUPERCONDUCTING ANALOG-TO-DIGITAL CONVERTERS

The overall architecture of a concept for a superconducting analog-to-digital converter (SADC) as devised by The MITRE Corporation has been described by Schoen [1]. The operational goal of the design is 16-bit precision with a sampling rate of 5 megahertz. The preliminary account of this work includes mathematical models of performance and implementation studies. The MITRE SADC architecture is built upon use of residue number principles: it postulates rapid conversion of analog voltage data into precise frequency data, with multi-channel decomposition of these data through signal phase resolution. As such, frequency and phase precision requirements are equivalent to a system precision of 1 part in 2^{16} and, thus, demand frequency precision $\Delta\omega/\omega \sim 2 \times 10^{-5}$.

1.2 VOLTAGE CONTROLLED OSCILLATORS

Precise conversion of signal information to frequency and the phase information can be accomplished using superconducting Josephson junctions. In following sections, we report design considerations for arrays of Josephson junctions configured as a drive source for a SADC. The design discussion shows some of the options to both increase the output power and reduce the output bandwidth of a VCO array. The report continues with our evaluation measurement results and conclusions. A preliminary account [2] of MITRE design considerations for an SADC VCO has appeared as part of reference 1; and Section 2 is based upon it.

The Josephson-junction array VCO source is the key component of the SADC. There are additional superconducting components in the frequency discriminator unit which electrically follows the VCO, and this frequency discriminator is introduced in the design section. Details of the MITRE frequency discriminator and its subcomponents have been described previously [3] and are outside the scope of this report on the design and evaluation of a superconducting VCO for a specific SADC architecture. The evaluation section describes the test of a typical superconducting VCO. In addition to the present investigation of VCO use, phase-locked arrays of Josephson junctions may offer new superconducting electronics design capabilities outside the present focus on SADC applications. If Josephson junctions

arrays can be controllably engineered and then fabricated, they may offer new possibilities in communication systems design as frequency-agile, precise submillimeter wavelength radiation sources.

SECTION 2

DESIGN CONSIDERATIONS

The main disadvantage of a single Josephson junction as a source in an SADC is low-power output. Adequate power is needed to pass through a delay line(s) and drive one or more phase-detecting mixers. In the absence of firm requirements for the mixers and delay lines, a goal of 10 nW of oscillator output power is desirable. This power level is far in excess of single junction output levels in the picowatt range. In addition, there are impedance mismatch concerns associated with matching the intrinsically low impedance single junction oscillator with transmission lines used for delay. For example, if the mean converter output frequency is 15 GHz, a single shunted junction circuit will tend to have an impedance on the order of only 0.01 to 0.1 ohm. A series array of N junctions can exhibit the phase locked constructive interference of N oscillators with array output power increasing as N^2. Such array characteristics have been verified. Jain, *et al.* [4] show the result of a study of arrays with various numbers of junctions in series and operating at 10 GHz. Their array with 99 junctions achieved an output power of about 5 nW into 50 ohms. For comparison, the single junction output was measured to be about 0.5 pW, which is about two percent of the theoretical matched output of the individual junctions given by $I_c^2 R_n/8 \sim 20$ pW, where I_c is the junction critical current and R_n is the normal-state resistance of a junction.

Another SADC requirement is the need for spectral purity in the VCO. For the MITRE SADC discussed in this report, phase precision requirements equivalent to one part in 2^{16} imply output frequencies must be within the range $\Delta\omega$ given by $\Delta\omega/\omega < 2 \times 10^{-5}$. This is a severe requirement. An analysis by Likharev [5] of thermal noise fluctuations yields a bandwidth that is proportional to both the temperature and the resistance of a single junction. This is a minimum which is increased by other possible noise sources, including $1/f$ noise, for example. According to Likharev, the width at 4 K is 160 MHz per ohm of source resistance. At a frequency of 10^{10} Hz and assuming $R_n \sim 0.01$ ohm, the linewidth associated with a single junction would be $\sim 2 \times 10^8$ Hz. If an array configuration is used, then theoretically this linewidth should be reduced by $1/N$, so that, for $N = 200$, $\Delta\omega/\omega \sim 1 \times 10^{-4}$. Although the linewidth of this particular example is higher than the requirement by nearly one order of magnitude, Jain, *et al.* [4] show that additional shunt resistance will narrow the linewidth.

The critical issue for the desired coherent operation of an array is phase locking. A Josephson junction array will comprise an ensemble of similar but not identical junctions, each hosted in a similar but not identical local environment. A tendency toward incoherent radiation with a distribution of frequencies may be countered by the presence of a judicious locking current. Conditions for phase locking have been investigated theoretically and performance of phase locked arrays has been the subject of significant activity. Empirical information is still used, however, and some investigators [4] report anomalous behavior

with, for example, only 15 percent of the junctions in an array exhibiting mutually locked behavior.

During this investigation, MITRE made progress in analyzing coherent oscillation of Josephson junctions. We have worked on useful designs [3] that generally fit the project requirements. We have selected component layouts that seem realizable and consistent with physical limitations. For example, although we would prefer a large number of junctions ($N \sim 10^3$) to increase output power and improve VCO linewidth, we are restricted by foundry design rules and coherent phase requirements. The need to have all the junctions driven in phase even at the highest frequency (about 20 GHz for the converter) requires all the N junctions to be within approximately one-tenth of a wavelength at this highest frequency after taking into account the somewhat retarded speed of propagation on the junction substrate. Sets of practical values of inductance, capacitance, and resistance have been generated and analyzed by various computer routines. Although earlier accounts of MITRE analysis work on practical designs suited for SADC applications have appeared [1, 2], the MITRE analysis of candidate VCO array designs is reviewed in this section. Because part of the MITRE investigation plan included cooperating with Prof. J. E. Lukens of SUNY to fabricate and evaluate basic VCO designs, the SUNY design practices and parameter expectations were significant. In the remainder of this section, we review some of our basic VCO designs, some improvements suggested by SUNY to improve output stability and some limitations of VCOs with regard to SADC use. After we had made some initial studies based on 20 GHz as an upper frequency and reviewed in section 2.2 below, we made a decision to shift the planned operating range to 9 to 18 GHz. The reduction of the upper frequency allowed use of lower cost evaluation fixtures with no expected loss of generality in evaluation outcomes.

2.1 BASIC DESIGN

To provide a focus of analytical capability, we initiated a design of a suitable test article for the SADC project to test one critical component, the VCO. As an initial design of a VCO test device, we analyzed the design outlined in figures 1 through 3 and the text below. Based on relations given by Jain, *et al.* [4], the estimate of the output power at 10 GHz is 0.16 μW (-38 dBm).

The overview of the basic design is shown in figure 1. It shows a sample array of 200 junctions configured with 50-ohm input and output impedances. The important controlling parameters of the array are listed in table 1. Table 2 shows the predicted performance parameters of the array. The design focus is on measurability first and optimal operation second. The concept of the design is to provide a testable component having projected operating characteristics that appear to support the SADC architecture applications. Thus, the derived array operating characteristics shown in table 2 seem to be generally compatible with SADC use. Integration of the VCO component, however, with a sample-and-hold amplifier input and a superconducting delay line output would require modification of the design [1].

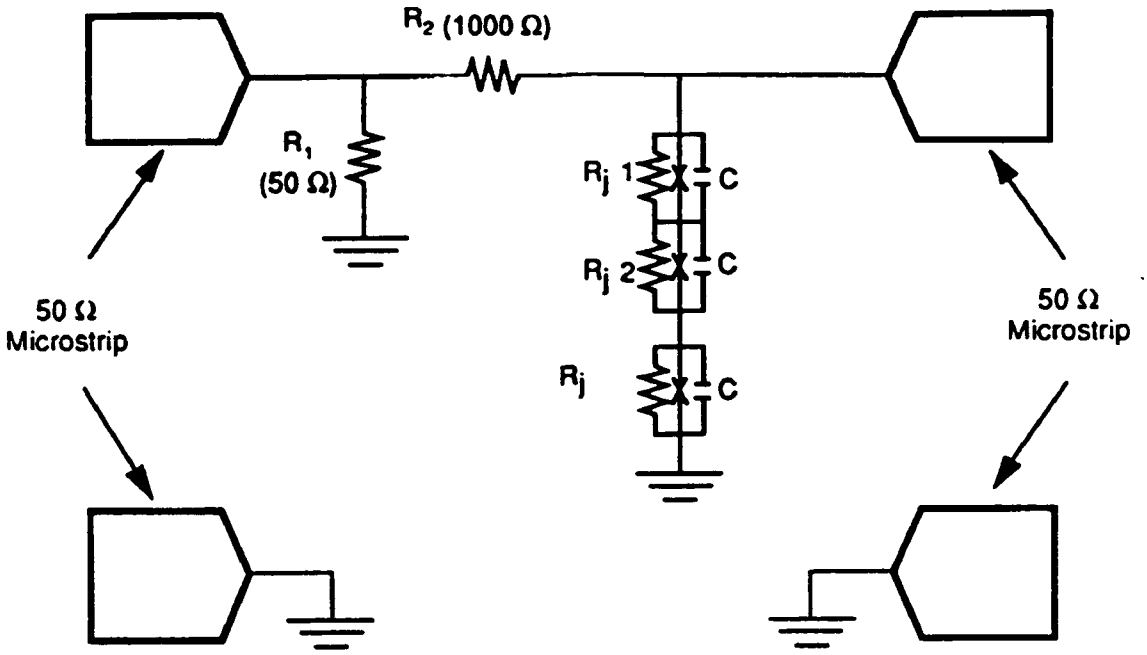

Figure 1. Schematic Diagram of the Josephson VCO Array

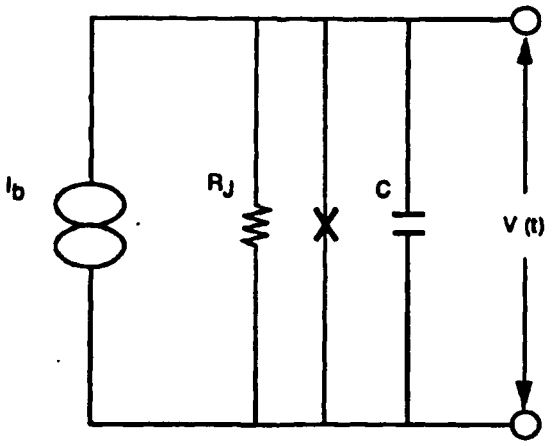

Figure 2. Equivalent Circuit of a Single Junction Unit

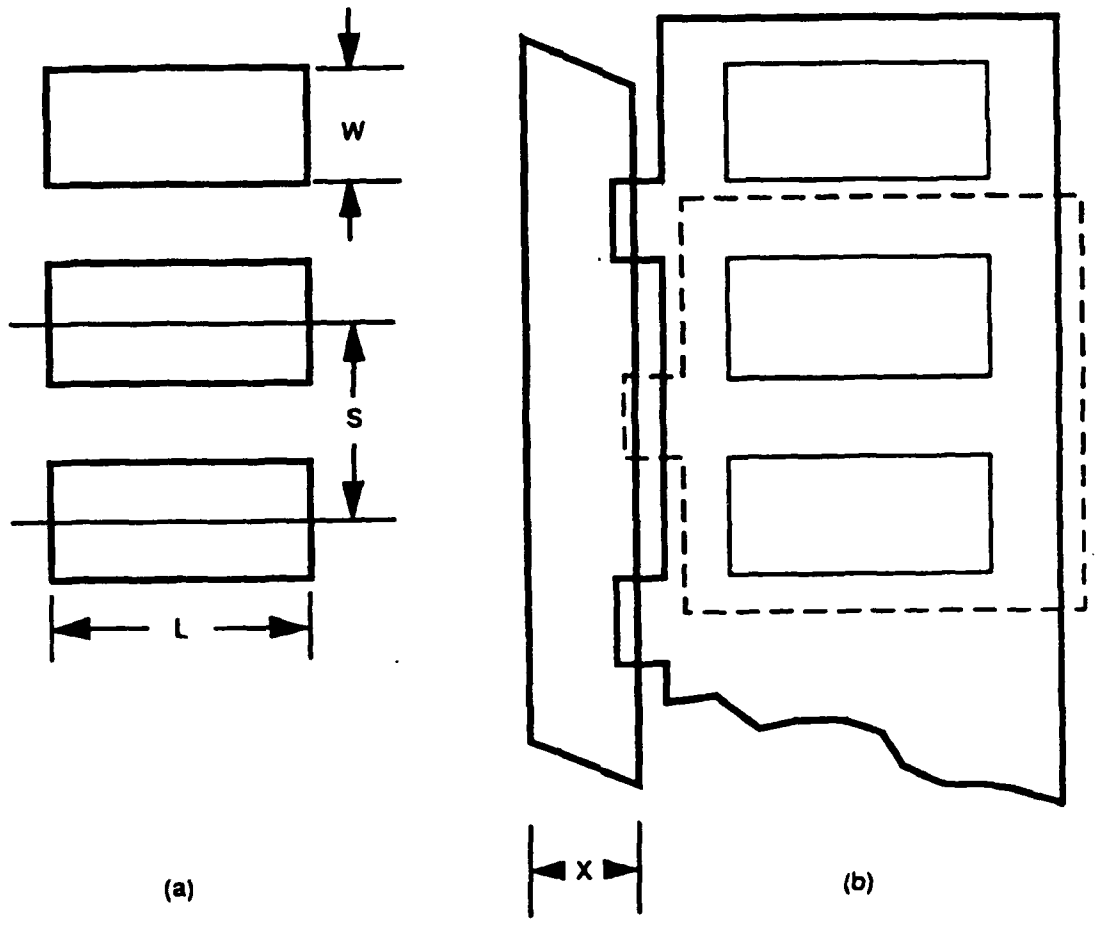

Figure 3. Concept of the Array Pattern. (a) Junction layout with $W = 3$ μm, $L = 6$ μm, $S = 6$ μm, (b) Normal metal shunt of 1 μm thickness with width $x \sim 3$ μm and path length(s) ~ 6 μm based on a resistivity of 0.5 μΩ-cm

Table 1. Array Configuration Specification of a 200-Junction Array

Parameter	Value
Junction width FF [a]	3 μm
Junction length L	6 μm
Junction spacing S [a]	6 μm
Junction critical current I_c [b]	1.8 mA
Junction shunt resistance R_j [c]	0.010 ohm
Number of Junctions N [d]	200
Junction capacitance C [e]	0.81 pF

a minimum width and spacing (pitch) according to Hypres [7].

b $(10^4\ \mathrm{A/cm^2})\ W\ L$.

c Approximate value so that $1.7\ I_c R_j/\Phi_o \sim 15$ GHz.

d $N = \dfrac{10^8\ \mathrm{m/s}}{4S(20\ \mathrm{GHz})}$.

e $C = \left[45\ \mathrm{fF}(\mu\mathrm{m})^{-2}\right] WL$

Table 2. Array Operating Parameters of a 200-Junction Array

Parameter	Value
Reduced current i [a]	[1.52, 2.50]
Operating range of junction current I_b [b] (mA) @ $10 \leq f$ (GHz) ≤ 20	[2.74, 4.5]
Operating range of array input current I_o [c] (mA) @ $10 \leq f$ (GHz) ≤ 20	[55,90]
Bias power to 200 junctions, P_{bias} [d] (μW)	[15,41]
β_c [e]	0.0004
Output frequency f_o [f] (GHz)	[10,20][h]
Linewidth $\Delta\omega/\omega$ [g]	[4.2 x 10^{-7}, 4.9 x 10^{-7}]
Output power P_A [h] (μW)	0.16

[a] i is the reduced current such that $I_c R_j \sqrt{i^2 - 1} / \Phi_o = 10$ or 20 GHz,

[b] $I_b = i\, I_c$,

[c] $I_o = I_b$ (10^3 ohm/50 ohm),

[d] $P_{bias} = N I_b{}^2 R_j$;

[e] $\beta_c = 2eI_c\, R_j{}^2\, C/h$,

[f] f_o to be determined from JSPICE for single junction shunted by R_j, C;

[g] $\Delta\omega/\omega = 2k_B T\omega/P_{bias}$ in accord with eq. 8.17 of Jain, *et al.* Physics Reports, Vol. 106, 1984,

[h] $P_A = [I_c{}^2$ (50 ohm) /2]$\gamma_N{}^N$, where the γ_N-value of 0.002 is obtained from Figure 5-3 of Jain *et al.* (Ibid., pp. 405-6) with N/N_{opt} = (200/5000) = 0.04.

Figure 1 shows the array input and output; as well as, the overall circuit schematic of a 200-junction array. Figure 2 shows the single junction unit cell that is replicated through the array. The bias current I_b flows through this unit and the voltage $V(t)$ develops across it. The time average of this voltage $\overline{V}$ determines the frequency f of junction oscillation: $f = (2e/h)\overline{V}$. The over-bar symbol indicates an average over time that is long with respect to the oscillation period.

The array may be treated as a lumped element providing that the phase difference across its external points is small. This condition limits the array size. The usual criterion [4-6] for spatial limitations related to phase coherence limits the longest linear dimension S such that $S \lesssim \lambda/10$ where $\lambda \sim (c/4)\,(f_{max})^{-1}$ with c being the speed of light in vacuum and f_{max}, the highest frequency of operation. Phase velocities as low as $c/10$ may be possible according to the literature [4].

Minimum spacing of junctions depends on lithographic production limits. The minimum spacing S recommended by the Hypres Corporation for their niobium films is 6 μm [7]. This limit is consistent with SUNY practices [4,6], and this minimum is used in the pattern shown in figure 3. Figure 3(a) shows junctions as rectangles L by W. The dimensions used, 6 μm by 3 μm, yield a junction area of 1.8×10^{-11} m^2. The product of this area and the typically achievable [6] Josephson critical current density J_c of 10^4 A/cm^2 yields an expected tunneling critical current I_c of 1.8 mA. The junction capacitance value of 0.84 pF per junction is consistent with the same junction area and an assumed specific capacitance of 45 fF (μm)$^{-2}$. These values are summarized in table 2.

Figure 3(b) shows a concept for replication of resistively shunted junctions. The pattern shown could be produced by a stepped offset of the upper superconductor film on the lower, both having lateral tabs. The tabs are shown shunted by a normal metal film deposited onto the plane of junctions and over the superconductive tabs to form a line of shunt resistors somewhat displaced from the line of Josephson junction centers.

Although the above pattern (figure 3(b)) concept is achievable, the self-inductance of the shunts is non-optimal. The estimated self inductance of each junction shunt is about 1 pH. The effect is to introduce systematic error into the predictions of array performance (table 2), especially at the higher operating frequencies. Instead of this pattern, investigators at SUNY use an underlying shunt resistance film. Sauvageau [6] shows one example of the SUNY-type of low inductance shunted junction having an effective inductance of 0.1 pH or less.

As referenced in [2] in the section on error analysis, the voltage-to-frequency conversion in the subject superconducting VCOs deviates somewhat from an ideal linear proportion. The overall conversion of signal voltage at the 50-ohm input of the array to a frequency at its output is not a quantum ratio of 16-bit precision, but depends on resistance ratios, voltage fluctuations, etc. This conversion deviation is the result of using a current bias of the array,

not a voltage bias. For example, based on the tabulated performance parameters in table 2, input voltages of 2.75 and 4.50 volts correspond to output frequencies of about 10 and 20 GHz, respectively. Equations[1] of Lukens, *et al.* [8] yield

$$f_1 \approx I_b R_j \Phi_o \left[1-(I_c/I_b)^2\right]^{1/2} \tag{1}$$

where I_b is the bias current and R_j is the (shunted) junction resistance. Using the junction values of table 5-1 and letting $I_b \sim V_{in}/(1000 \text{ ohms})$, this conversion becomes

$$f_1 = KV_{in}\left[1-\left(V^*/V_{in}\right)^2\right]^{1/2} \tag{2}$$

where $K = R_j\Phi_o^{-1}$ $(1000\ \Omega)^{-1} = 4.84$ GHz-V^{-1} and $V^* = (1000 \text{ ohm})\, I_C = 1.8$V. Also, I_b is the bias current, Φ_o is the flux quantum and V_{in} is the input voltage. In what follows in section 2, the current through the array is denoted I, and the bias notation is dropped.

2.2 JSPICE SIMULATIONS

MITRE performed JSPICE simulations to investigate single Josephson junction VCOs. JSPICE is a version of the popular SPICE 2G circuit simulation program which features an embedded Josephson junction model. JSPICE represents an important tool for the design of subsystems of the superconducting analog-to-digital converter. This section describes initial conditions in JSPICE, typical JSPICE simulation results and a discussion of these results.

The Josephson junction model implemented in JSPICE is known in the literature as the resistively shunted junction (RSJ) model [4,5]. The RSJ model includes an ideal Josephson junction in parallel with the junction capacitance and a voltage dependent shunt resistance, as depicted by the equivalent circuit shown in figure 4. (The Josephson RSJ model is between node 1 and ground, and is treated by JSPICE as a single device.) The ideal Josephson

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1 We use both the equation $f = (2e/h)\overline{V}$ and the relations $\overline{v} \equiv \overline{V}/V_c = (i^2 - 1)^{1/2}$, $i \equiv I_b/I_c$, and $V_c \equiv I_c R_j$ associated with equation 2 in reference 7. Since the flux quantum Φ_o is equal to $h/2e$, we can write $f = \Phi_o^{-1}\overline{V}$ and recognize $\overline{V} = I_c R_j\left[(I_b/I_c)^2 - 1\right]^{1/2}$, so that $f = R_j I_b \Phi_o\left[1-(I_c/I_b)^2\right]^{1/2}$.

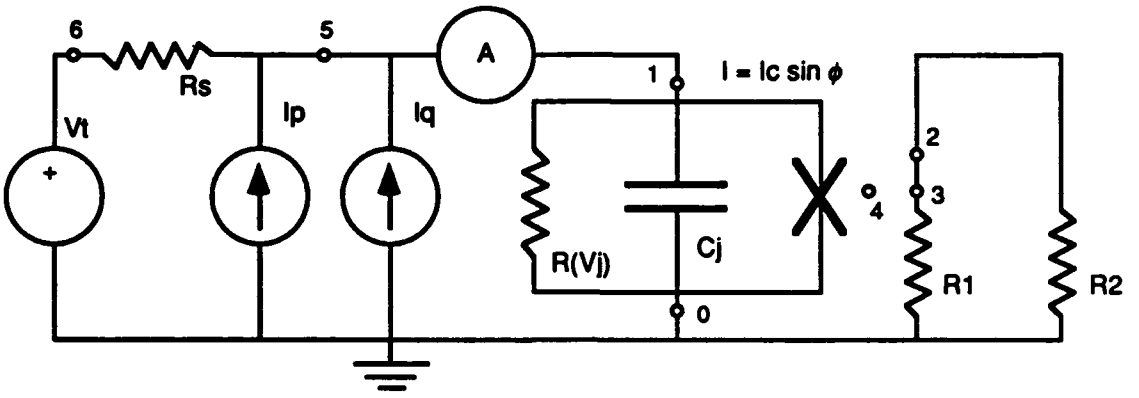

Figure 4. Josephson Junction Voltage Controlled Oscillator

junction obeys the Josephson relations and accounts for Cooper pairs (the superconducting electrons) tunneling through the junction, while the voltage-dependent resistance represents the quasiparticle (single "normal" electron) tunneling current. JSPICE requires that the initial conditions of a Josephson junction be declared, which include the junction phase, ϕ and the junction voltage, V_j. It is appropriate to uniquely specify only one of these parameters, with the other set to zero. Which parameter is specified depends on the initial voltage state (zero or finite) of the Josephson junction.

The zero voltage state of the Josephson junction implies that the current through the junction does not exceed the junction's critical current. In this case the junction phase should be specified, which is given by the Josephson current-phase relation [9] shown here in the alternate form

$$\phi = \arcsin\left(\frac{I_c}{I}\right) \tag{3}$$

where I is the current through the junction.

A finite junction voltage specified as an initial condition implies that the junction phase difference is increasing with time as given by the Josephson voltage-phase relation [10]

$$\frac{\partial \phi}{\partial t} = \left(\frac{2e}{\hbar}\right) V_j \tag{4}$$

In other words, if a constant voltage is applied to the junction, integration of equation (4) shows that

$$\phi = \phi_o + \left(\frac{2e}{\hbar}\right) V_j \, t \tag{5}$$

where ϕ_o is an initial phase. Substitution of this result into equation (5-3) yields

$$I = I_c \sin(\omega j t + \phi_o) \tag{6}$$

where

$$\omega_j = \left(\frac{2e}{\hbar}\right) V_j \tag{7}$$

Thus, an applied voltage on a Josephson junction causes an AC current oscillation through the junction, a phenomenon known as the AC-Josephson effect. The Josephson AC current oscillations will be partially shunted by the junction capacitance and (more importantly) the junction resistance thereby causing the junction voltage to oscillate at a frequency of

$$f = \left(\frac{1}{2\pi}\right)\left(\frac{2e}{\hbar}\right)\overline{V}_j \cong (483\ \text{MHz/mV})\overline{V}_j \tag{8}$$

which is the fundamental voltage-to-frequency relationship which we are exploiting in our analog-to-digital converter architecture. Therefore, an initial condition specification of finite junction voltage causes Josephson AC current/voltage oscillations from time $t = 0$. This condition does not necessarily imply that the junction current exceeds I_c, although if $I < I_c$ the junction voltage oscillations may die out if the junction and its external circuit provide sufficient damping.

If the initial state of a junction is not obvious from the circuit topology, a preliminary simulation with both ϕ and V_j set to zero and all sources set to their quiescent values can provide the initial state of the junction(s). The Josephson junction will rapidly (within 200 ps) converge to its quiescent state, which can be determined by monitoring the node voltages of the circuit. The junction phase is brought out to a dummy node labeled ***NPHI*** within JSPICE.

A Josephson VCO circuit was investigated to establish a correlation between the JSPICE simulation program and ACSL simulation programs separately run at MITRE and described elsewhere [1], additionally, this investigation illustrated an important use of initial conditions in JSPICE. Figure 4 shows the Josephson junction VCO circuit model simulated using the JSPICE program. JSPICE incorporates a quasiparticle resistance model containing a Fermi-like function for the resistance transition between the minimum resistance and the normal state resistance of the junction as the the junction voltage approaches and then exceeds the gap voltage; accordingly, in our modeling, we set the JSPICE variable ***RTYPE***=2 as discussed by Jewett [11]. The current which flows in the short between nodes 2 and 3 can be used to modulate the critical current; thereby, modeling the effect of magnetic field on the

Josephson junction. This modulation option was not used in the simulations presented here, and therefore nodes 2 and 3 were simply connected to ground via 1-kilohm resistors while the JSPICE control current type parameter ***CCT*** was set to zero. Node 4 is the dummy phase node ***NPHI*** referenced above, which cannot be connected to any actual circuit element. The current sources I_q and I_p are the DC bias current and preconditioning current pulse sources, respectively. In the following simulations I_q was set to 99 μA. The test input voltage was represented by the voltage source V_t with source resistance R_s, where R_s had a value of 10 kΩ. All of the following simulations were performed using the JSPICE program running on a VAX 2000 workstation under the VMS operating system. Additionally, identical results were obtained using JSPICE on the MITRE UNIX VAX machines.

Figure 5 depicts the junction voltage as a function of time where the junction was initially biased with the DC current I_q, $\phi = 1.4293$ rad, and $V_j = 0$. At time $t = 10$ ps the junction was pulsed with a 1 ps duration current pulse of 23.5 μA magnitude, and 1 ps rise and fall times. Beyond approximately 60 ps the peak value of the junction voltage was ~1.022 mV. A Fourier analysis performed on the waveform showed the junction voltage to be oscillating at a fundamental frequency of 476.0 GHz with a total harmonic distortion of 0.52 percent. Thus, the frequency spectrum of this Josephson VCO circuit is relatively monochromatic.

The simulations presented in figures 5 and 6 depict the response of the Josephson junction VCO to a step input current waveform. The input current waveform is the sum of the DC bias current and the current from the test voltage source V_t with its associated series resistance R_s. In the simulation, the junction was DC biased at 99 μA with initial conditions of $\phi = 0$ and $V_j = 1.022$ mV. Note in figure 6 at time $t = 0$ that the junction voltage is oscillating in the same manner as it was in figure 5 at time $t = 200$ ps, a manifestation of the junction initial conditions. The use of initial conditions provides the Josephson oscillations at the beginning of the simulation, allowing us to eliminate the preconditioning current pulse and its transient response. This allows the simulations to focus on the desired VCO behavior, where the voltage oscillations are sensitive to perturbation by the external voltage V_t.

2.3 OSCILLATOR PHASE LOCKING

The essence of the VCO multi-junction array is the coherent oscillation of all or almost all of its individual oscillators. The principal fault of the 200-junction array of table 1 is that its output may fail to lock coherently. The conditions for coherent output of multiple-junction arrays depends on several parameters. Hadley *et al.* [12] have examined the intrinsic stability of an array of junctions with respect to both the bias current and the junction beta parameter β_c. The β_c-value (where $\beta_c = 2eI_cR_J^2C/h$) of our test design is only 0.0004 and, thus, barely in the range where [12] predicts some measure of coherence. And thus, the (β_c, I_b)-values are far from their optimal range. Reference 12 recommends a β_c of between 0.5 and 1.0 as well as a reduced current bias, the ratio of applied bias current I_b to critical current I_c, in the range of 2 to 2.5. But values of I_c, R_j and C are, however, not independent of (a) each other, (b) operating frequency constraints, and (c) chip and physical dimensional

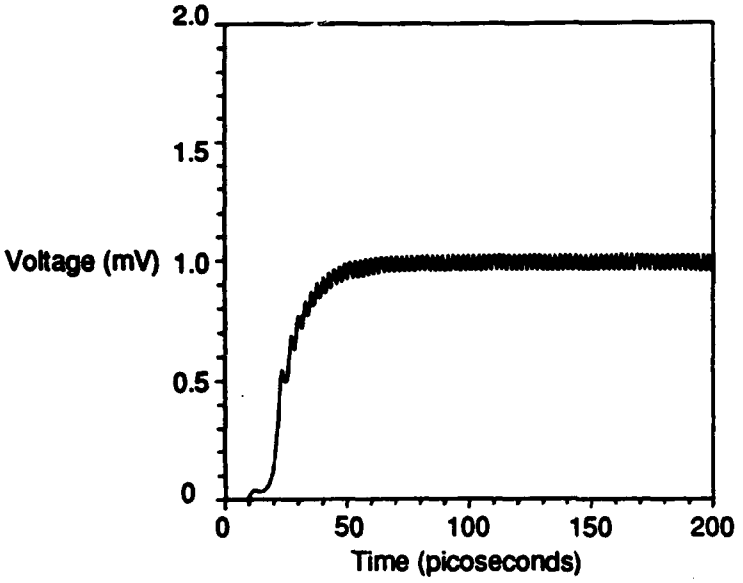

Figure 5. Voltage Response as a Function of Time for a Josephson Junction to a Static Bias and a Conditioning Pulse ($V_t = 0$)

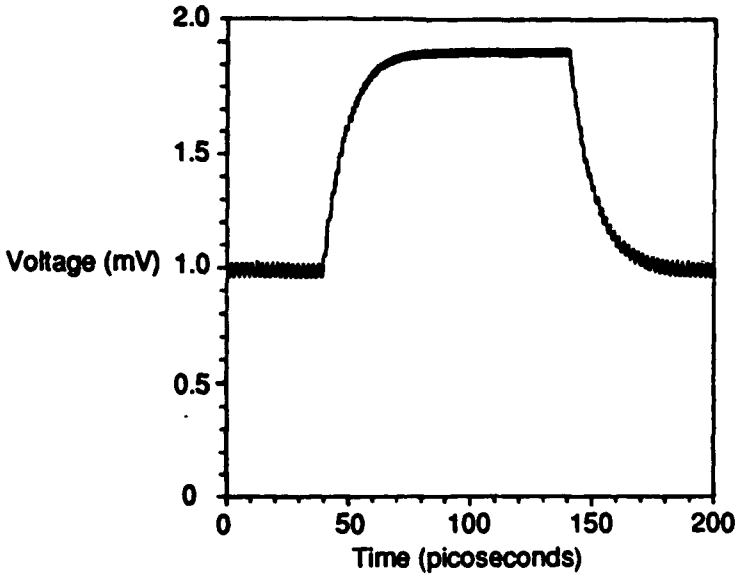

Figure 6. Voltage Response as a Function of Time for a Josephson Junction to a Positive Current Step (Current Bias < I_c)

constraints. The main risk is that production variation in values of I_c (and C) and R_j from junction to junction will not support coherent oscillation of the junctions of the array.

With the greater insight gained by study of the array of table 1, we have considered some modifications to enhance its stability. According to Jain *et al.* [4], the physical effect that is central to phase locking is the constructive interference of the array current components with the high frequency (hf) circuit currents as if the latter were independent perturbing currents. We assume the array to be phase locked and focus on a single junction. We consider the possible small phase variation between that junction current in phase with its source emf but with both (1) current leading voltage in accord with the resistively shunted junction that includes junction capacitance, and (2) perturbed by the locking current flowing through the array and the rest of the hf circuit in its entirety. Inductive feedback shunting the array can complement the effect of junction capacitances within the array which, by the figure of merit of [12], are vanishingly small. While some inductance benefits phase locking by producing a negative phase locking angle p_l, too much hf circuit reactance is undesirable. Notably, increased hf inductance reduces both the magnitude of the locking current in the single junction and the available output power in the load. Reference 4 normalizes the comparison of a single junction reactance to that of the entire hf circuit by introducing a normalized (hf circuit) impedance z_c. It consists of the ratio of the impedance of the hf circuit to the resistance of the array. In a sense, this formulation amounts to a mean apportionment of the finite output impedance. This approach is expanded below to the case of the simple array (table 1) studied in [5] but with the addition of an inductive load. Following reference 4, we observe that variations in local parameters -- for example, currents controlled by shunting resistance and critical current -- can be inversely viewed as the ideal with the rest of the array currents as the amount of variation that can be tolerated while maintaining phase locking of all N quasi-independent sources in the array.

Our preliminary analysis showed the effect of including a finite inductance and then optimized inductance as part of the output impedance, an inclusion which should improve the phase-locking stability of the driving oscillator of the superconducting digital converter proposed by MITRE [1, 2]. Additionally, we analyzed a change of the output stripline/ microstrip from 50 to 2 ohms. This preliminary optimization study concluded that the 200-junction array may require an impedance-matching stripline if the output signal is to provide detectable input levels to room temperature instruments with 50-ohm inputs such as a spectrum analyzer or oscilloscope. Our preliminary study considered three perturbations to the circuit shown in figure 1. All three had to do with changing the output impedance seen by the array. These include (1) adding a feasible and, possibly minimal, series inductance L_s; (2) optimizing L_s for maximum phase locking; and (3) changing the resistive component R_l of the output impedance to better match the intrinsic impedance of the array, that array impedance being 2 ohms in table 2. Lukens *et al.* [8] point out the effects of inductance in the high frequency circuit is to phase delay currents with, possibly, beneficial results. We somewhat arbitrarily choose L_s=100 pH as a realistic minimum inductance in series with the output and calculate the phase locking stability factor $\delta I/I_L$. The inductance value of 100 pH is realizable in small-dimension circuits appropriate to coupling the array to a microstrip

output. For reference, a loop consisting of a 3-μm conductor far from a ground plane and comprising a 1200-μm by 6-μm rectangle has an inductance on the order of 1 nH. This value would be reduced if the inductive loop is near to a conducting ground plane.

Estimates below on the effects of finite inductance in the output circuit are based on the frequency of 15 GHz, the center frequency of the VCO band. Figure 7 shows the high-frequency (output) portion of the array of table 1 and figure 1 as discussed above but modified by an added inductance L_s. Computing the array's normalized impedance z_c [Eq. 16b, ref. 8] by

$$z_c = \left(1/NR_j\right)\left(NR_j + R_l + i\omega L_s\right), \tag{9}$$

yields $z_c = 26\,(1 + 0.181\,i)$, and the locking phase angle p_l from [eq. 17, ref. 8]

$$p_l = \tan^{-1}\left[-\mathrm{Im}(z_c)/\mathrm{Re}(z_c)\right], \tag{10}$$

obtaining $p_l = -0.18$ rad. Now the value of the (presumed) locked current I_L in the array is determined from the complex current $\bar{I}_l$ given by the ratio of the harmonic amplitude to the effective impedance as (eq. 16a of reference 8)

$$\bar{I}_l = \bar{V}/\left(R_j z_c\right). \tag{11}$$

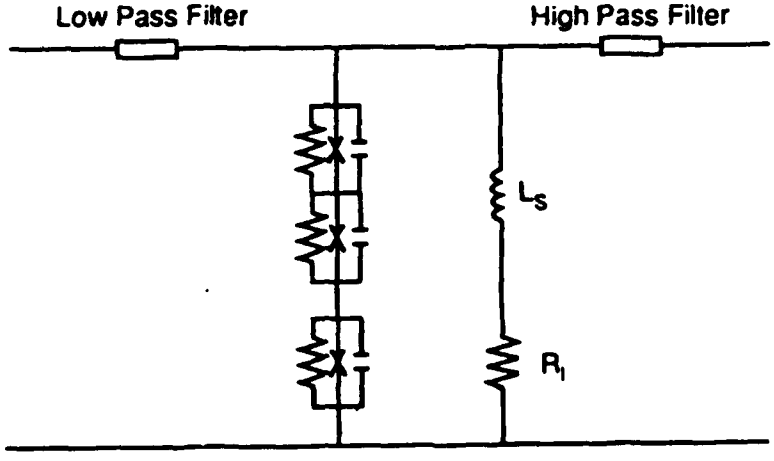

Figure 7. Schematic Diagram of an Inductively Shunted Josephson Array VCO

The bias conditions determine the magnitude of the fundamental frequency amplitude $\overline{V}$. Using values of table 1, it can be shown that $\overline{V}$ = 13 μV at 15 GHz, and with $|z_c|$ = 26 ohms and R_j = 0.01 ohm, $I_L = |I_e|$ = 0.049 mA. The assumed distribution of locking current has a maximum deviation δI_k given by the largest deviation that will not perturb the locked oscillation, namely (eq.19 of reference 8)

$$\delta I_k \approx I_L \min\left\{\left[1+\cos(p_l)\right],\left[1-\cos(p_l)\right]\right\} \tag{12}$$

so that for the (L_s = 100 pH) case studied, δI_k = 0.79 μA.

Other cases were studied for other load conditions. The cases with predicted maximum allowed variation in locking current, and translated to maximum allowed critical current $\delta I_c/I_c$ by assuming the locking or biasing current is a factor of two greater than the critical current. These three cases are tabulated in table 3. The feature we observe is that maximum variations can be small, even thought the third case was optimized under certain conditions (based on the optimal inductance predicted by eq. 20 of reference 8) and is comparable to achievable variability limits in critical currents.

Table 3. Maximum Allowed $\delta I_c/I_c$ of the 200-Junction Array of Figure 1

R_l (ohm)	L_s (pH)	δI_k (μA)	$\delta I_c/I_c$ (%)
50	100	0.79	0.022
50	552	12.5	0.35
2	74	160	4.5

The above sensitivity analysis of phase locking of prototype VCO sources for driving converter circuits shows the sensitivity to critical current variation within an array. SUNY investigators are able to control critical currents across a given array to within about 3-percent of the mean critical current of that array. Individual junctions which fall outside the allowed range will not only fail to contribute to coherent output, but also will contribute to the noise in the output. Preliminary studies of phase locking of our prototype designs based on 50-junction arrays with strong inductive feedback suggested by SUNY [6] show that all junctions would lock at the center of output frequency range but as many as three junctions would become decoupled at the ends of the range. In our design, we had intended to couple the array output directly from (or in place of) the pure resistance element R_l in figure 7.

However, SUNY observed that there is an advantage in extracting only a fraction (about 1/10 *th*) of the oscillator power through the high pass limiting filter (figure 7) and then into a high impedance microstrip transmission line leading to a detector or analyzer. Such a coupling allows the oscillator to be more independent of both frequency of the output and following stage loading effects. This coupling can be conveniently obtained by mismatching a 50-Ω output transmission line to a low characteristic impedance array with load resistor. For example, with respect to table 3, for an R_l of 2 Ω the maximum allowable $\delta I_c/I_c$ of 4.5% provides a manufacturable array (recall that a 3% mean is achievable) for which a 50-Ω coupled line provides the desired loose coupling. The SUNY fabricated and MITRE characterized VCO array described later in section 3 was built using this principle.

2.4 VCO LIMITATIONS

In completing the latest version of a VCO design, we have made some preliminary observations about limitations of the design. We have mentioned the linewidth which, although acceptable in some applications, may be unacceptable in the MITRE converter. Second, we have shown that the VCO design is really a current bias design and the ratio of frequency output to voltage input is not a constant proportion but increases slightly with voltage over the conversion range. Third, the candidate design features a 50-ohm input more suited for experimental evaluation than practical application. Its use in a VCO to quantify a low level signal would necessitate a precision linear wideband preamplifier. Fourth, the candidate design features a high-impedance (50-ohm) output which may not be optimal for driving low-impedance delay line components of a converter, but this drawback is not significant. The above limitations and others related to the sensitivity of the design to parasitic reactances and unavoidable variations in both prescribed reactances and Josephson junction parameters is being investigated. MITRE analysts investigated the internal dynamics of VCOs related to conversion with the goal of mitigating the limitations cited or consequences of them [1]. In particular, Sauvageau [6] and other SUNY investigators have observed that the use of a stabilizing inductive feedback circuit as shown in Figure 7 both enhances oscillator stability and tends to decouple the oscillator from its following load.

2.5 ASSOCIATED COMPONENTS

The purpose of designing an agile VCO of narrow band output is to serve as a source for the frequency discriminator of the A/D converter. The architecture of the analog-to-digital converter proposed by MITRE [1] requires a multiple channel frequency discriminator. Its precision depends on accurate resolution of signals whose frequency vary over an octave. In the MITRE SADC architecture [1], each channel resolves the frequency of the input signal with respect to a given basis consistent with residue number mathematics.

A schematic view of a frequency discriminator is shown as a block outline in figure 8. According to the design concept, the necessary high resolution may be obtained by using different phase delay followed by phase detection. The discriminator incorporates at least one differential superconducting delay line, a superconductor-insulator-superconductor (SIS) phase detector and a low-pass filter of the phase detector output. A more complete review is found in [3].

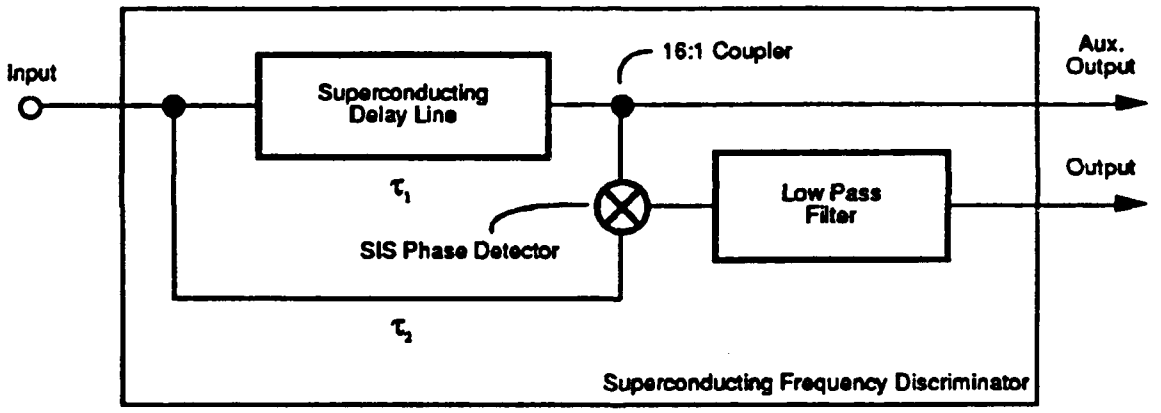

Figure 8. Block Diagram of the Superconducting Delay Line Frequency Discriminator

SECTION 3

VCO EVALUATION

We have concluded a series of measurements on a superconducting voltage controlled oscillator fabricated by investigators at the State University of New York. The sample evaluated was typical of those produced for the investigation of the MITRE SADC architecture. This section describes the sample, measurement conditions and test results. MITRE and SUNY measurement correlation is discussed. The tests included characterizing the VCO output frequency and RF power level as a function of bias current, and a direct measurement of the junction shunt resistance (R_s). The insertion loss of the MITRE cryogenic probe and connecting cable was also measured. This section describes the sample, measurement conditions and test results.

3.1 SAMPLE DESCRIPTION

The VCO design, as fabricated by SUNY investigators, is an iteration of the MITRE design. Our preliminary work in the array design and its principle of operation, are described in sections 1 and 2; and in a prior account [2]. However, the fabricated arrays are different from the arrays MITRE analyzed. In particular, the fabricated arrays use only 65 junctions and an array microstrip terminated with a load and junction detector as described below. MITRE evaluated the typical superconducting VCO sample 20GHz-11G.

The following series of figures show the physical structure of the superconducting VCO array. Figure 9 depicts the overall VCO chip layout. Details of the area labeled "VCO Array" are shown in figure 10. Finally, figure 11 illustrates the "Array of Junctions" of figure 10. Included in figure 11 is a cross-sectional view of the Josephson junction array. Refering now to figure 10, drive current for the VCO array is applied through a parallel bias network as shown. Output oscillations from the VCO array are coupled from the 1-Ω array microstrip into a mismatched 50-Ω microstrip tapped on the incident power side of a terminating 1-Ω resistor. This mismatch is intended to limit the amount of coupled RF power, so as to not disturb the coherent oscillations of the array. The 50-Ω microstrip is transitioned to a 50-Ω coplanar waveguide, which can be connected to an SMA launcher in a cryogenic probe assembly. RF output power may be detected and measured on-chip by an integrated Josephson junction detector through observations of Shapiro steps in the detector junction's DC current-voltage relationship [13,14]. These steps are finite current offsets in the detector current whose magnitudes are proportional to applied RF power -- offsets which SUNY has observed but which we have not observed for reasons given later.

The characteristics which SUNY measured for the VCO sample 20GHz-11G are listed below in table 4. The RF power available from the 50-Ω coplanar waveguide was found to be a maximum of ~4 nW (-54 dBm) at a temperature of 4.2 K. This was measured with a

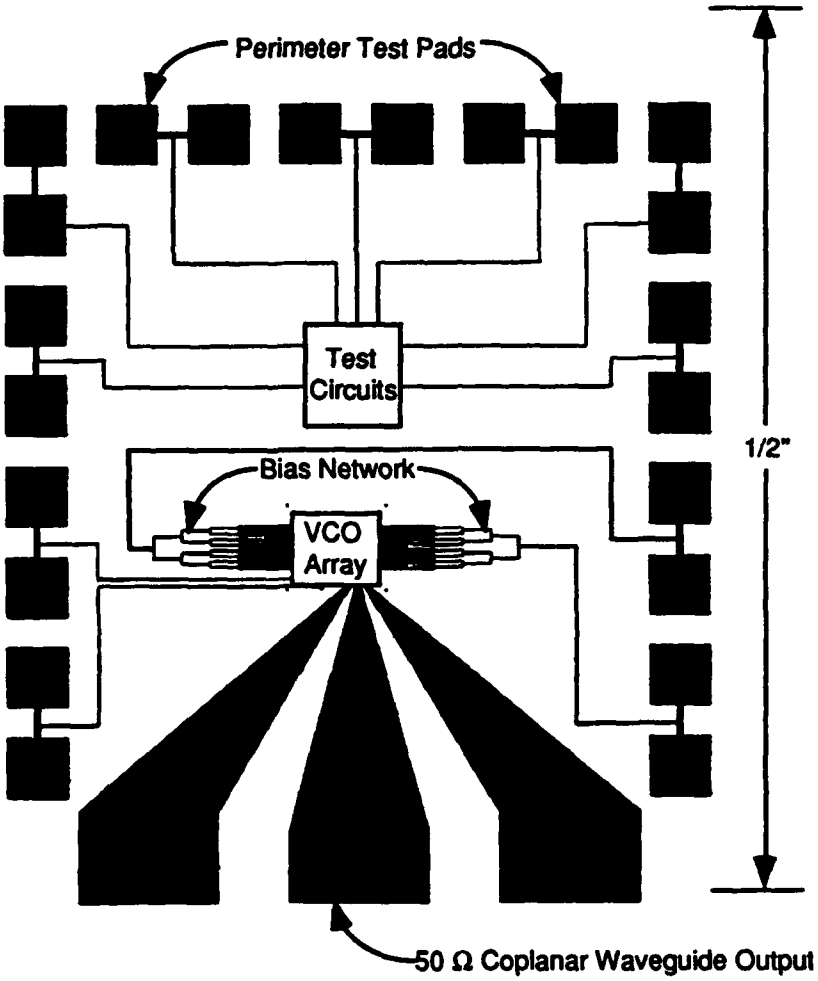

Figure 9. SUNY Superconducting VCO Chip Layout

bolometric power meter, which is broadband and has an advantage over a spectrum analyzer in that the technique is completely passive (i.e., well matched into 50 Ω without any spurious signals emanating from it). There is some concern that spurious power emission from a given spectrum analyzer's first local oscillator (LO) could be present at its input when it is used and thereby affect phase locking in the VCO array. SUNY reported that the output power variation with temperature (from 1.4 K to 4.2 K) was less than ten percent. However, the operation temperature strongly affects the output radiation bandwidth, which was determined by SUNY to be approximately 20 MHz at 4.2 K.

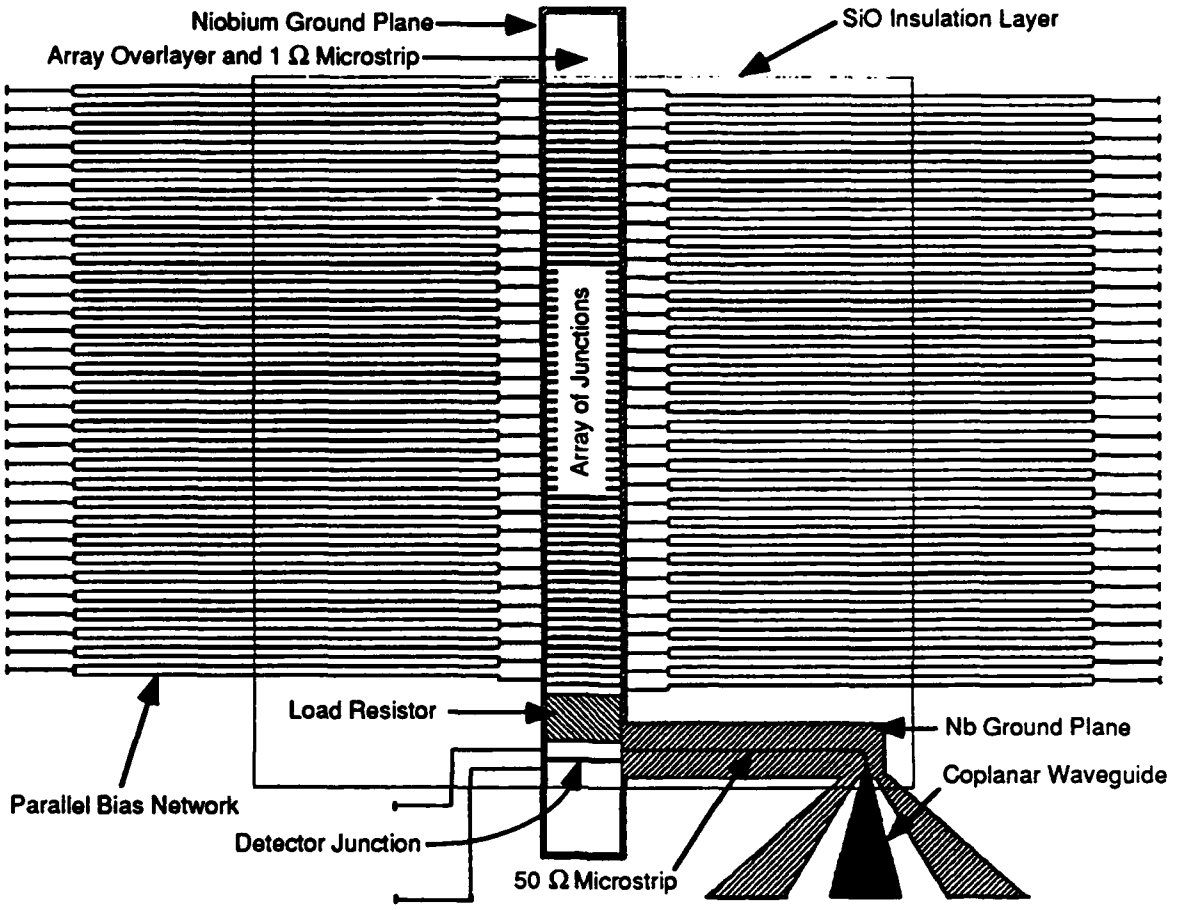

Figure 10. Detail of the VCO Array

Table 4. Performance Characteristics for the Superconducting VCO Sample 20GHz-11G

• Critical current:	$I_c \sim 1\text{mA}$
• Shunt resistance:	$60\ \text{m}\Omega < R_S < 100\ \text{m}\Omega$
• Maximum bias current:	$I_{max} < 150\ \text{mA}$
• Typical operating current:	$I_{operating} \sim 100\ \text{mA}$
• Typical operating voltage:	$V_{operating} \sim 30\ \text{mV}$
• Expected output power:	$P_{50\Omega} \sim 4\ \text{nW}$ (-54 dBm)

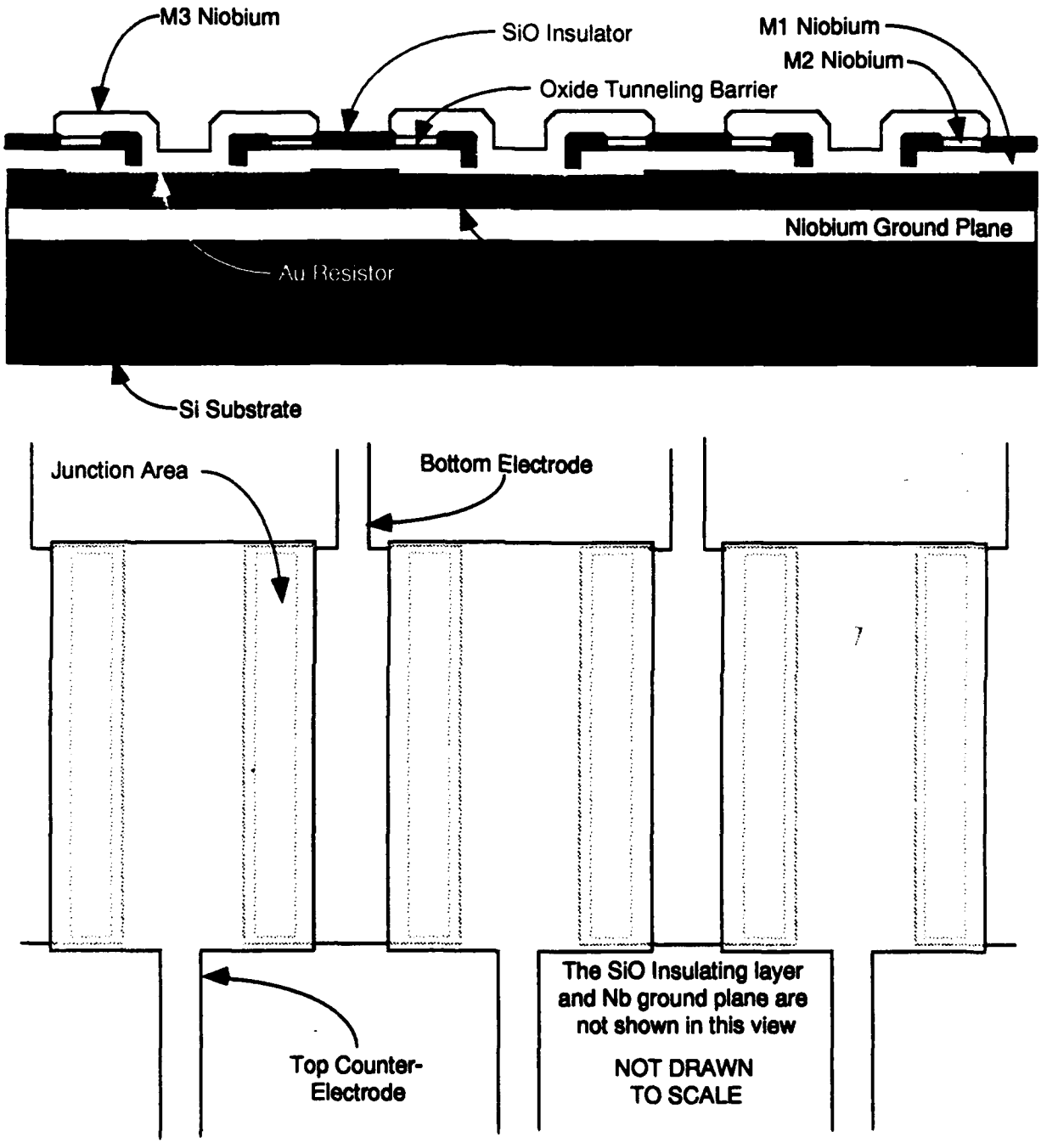

Figure 11. Cross-Sectional and Top-Down Views of the Array Josephson Junctions

3.2 MEASUREMENT RESULTS

In our initial characterization of the superconducting VCO we used a MITRE-built current source to drive the array and an HP71201A spectrum analyzer to measure the output radiation. The MITRE current source is nearly identical to a sweeping, battery-powered supply described in [15], except that we substituted a higher power output transistor (IRF520) for the specified JFET, and laboratory power supplies in place of four 6-V dry cells. These are sufficiently noise free so that battery operation, which we also tested, is indistinguishable. As mentioned above it is important for the spectrum analyzer not to influence the coherent oscillations of the VCO array through leakage of the first LO. SUNY provided us with a conservative specification that any spurious radiation should be less than -120 dBm. We did measure the first LO emission of the HP71201A to be -90 dBm without the spectrum analyzer's HP70620A preamplifier. The integral preamplifier provides an additional 30 dB of reverse isolation, and we were able to verify that the first LO emission was less than -115 dBm with the preamplifier. We also had available broadband isolators which provided an additional 18 dB of reverse isolation each. The VCO sample was attached to the SMA launcher of the MITRE cryogenic probe using silver epoxy. The VCO array is operated in a reservoir of liquid helium at a temperature of 4.2 K or lower. The following paragraphs present various measured data for the superconducting VCO.

3.2.1 Output Power Spectrum

During this initial test we measured the VCO output frequency and power as a function of drive current. Figure 12 shows a typical output spectrum as recorded by the HP71201A, at a bias current of 87.0 mA. It shows a peak response of approximately -84 dBm at a frequency of 18.4 GHz. The peak RF power we observed was 30 dB less than the -54 dBm reported by SUNY [16].

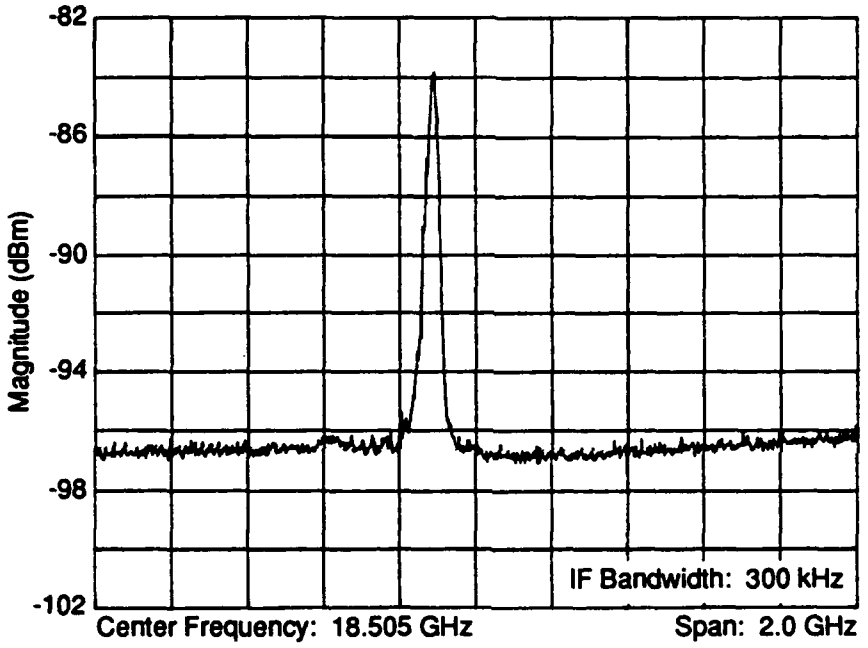

Figure 12. Typical VCO Output Power Spectrum

3.2.2 Frequency Dependence on Bias

In figure 13 our measured data is compared with the theoretical prediction of equation (1), which shows the fundamental frequency observed or predicted as a function of bias current. The three theoretical curves are defined by assignment of various choices of shunt resistance (R_S) and Josephson critical current (I_C) values. Curve 1 is based on values of both R_S and Ic reported in table 1 and curve 3 is based on the previously reported design value of R_S, 20 mΩ. Curve 2 is the result of an empirical fit using R_S and I_C values of 30 mΩ and 0.5 mA, respectively. It is evident from figure 13 that the fit of curve 2 is clearly superior. This

fact, coupled with the 30 dB discrepancy between MITRE and SUNY RF power measurements, led us to pursue additional experiments to reconcile these differences and independently estimate array parameters.

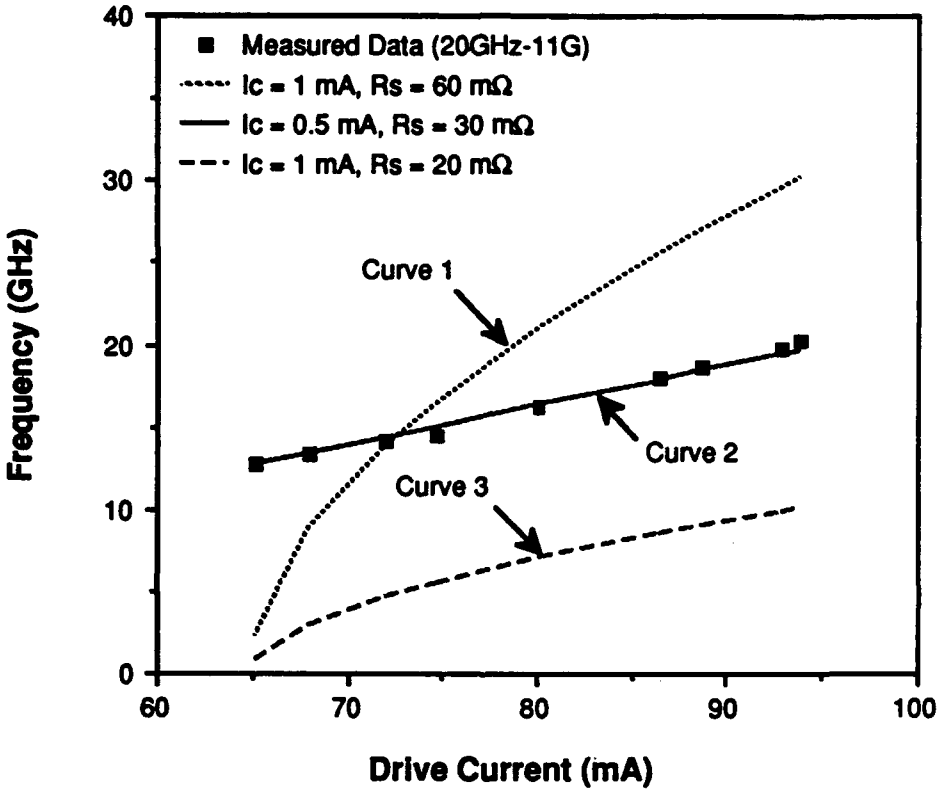

Figure 13. Oscillator Frequency versus Bias Current

According to the design, the integrated detector junction of the VCO array has identical dimensions to, and is fabricated concurrently with the drive junctions of the array. Therefore the detector junction should be representative of each of the 65 array junctions. The detector junction is separately testable, which allowed us to directly measure its shunt resistance R_S. We accomplished this using a four-wire resistance measurement technique, where a Keithley 238 precision current source drove current through the junction and the voltage developed across it was measured with an HP3478A voltmeter. Thus, an accurate measurement of Rs was made by varying the detector junction bias current and recording the resulting junction voltage as shown in figure 14. Below about 0.5 mA the junction voltage drop was

immeasurably small (i.e. superconducting state). This observation indicates that I_c at 0.5 mA for the detector junction, and the slope (37.2 mΩ) of the straight line fit to the data is the measured shunt resistance of the detector junction and hence our best estimate of R_s for the array junctions. SUNY [17] believes, however, that this detector junction is not representative of the array junctions because their measurements show array junction critical currents of approximately 1 mA. We were unable to directly measure array junction critical currents, and hence were unable to confirm their measurements. The slope of the curve indicates the junction shunt resistance R_s. These measurements were made on the detector junction (representative of the individual array junctions) as discussed in the text.

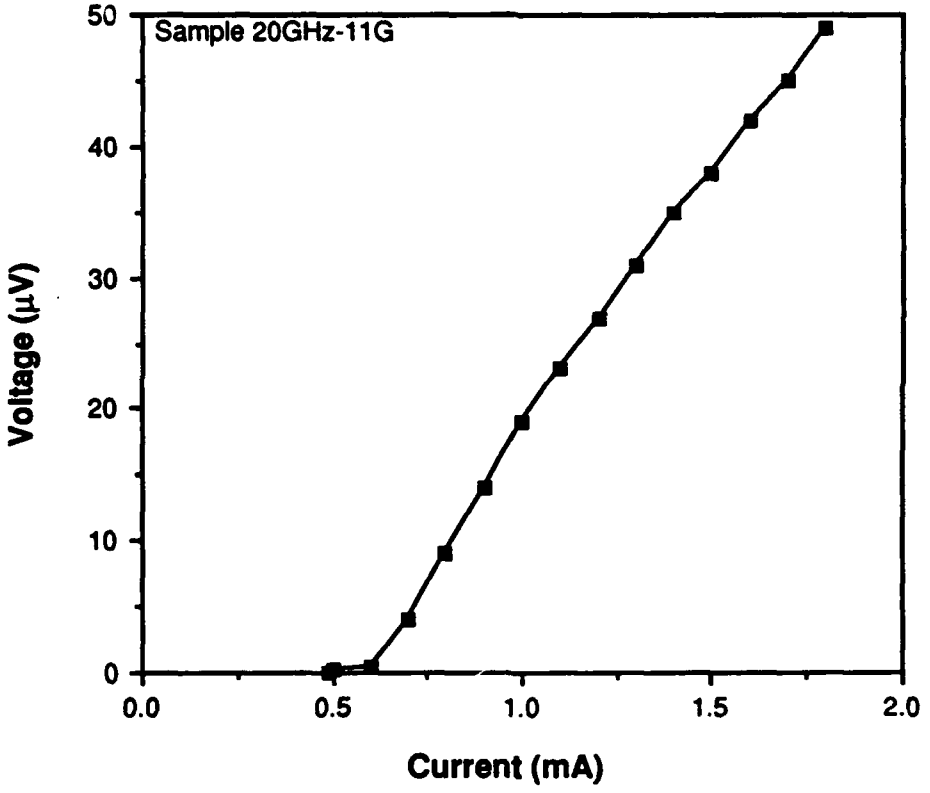

Figure 14. Voltage as a Function of Current for a Single Shunted Josephson Junction.

3.2.3 Comparison to Other Measurements

In an effort to resolve the conflicting output power observations, we measured RF power as a function of VCO drive current using both the HP71201A spectrum analyzer and an HP438A bolometric power meter. Prior to this measurement, we recontacted the VCO chip using indium foil, replacing the silver epoxy which was suspect at cryogenic temperatures. During this experiment, drive current was provided by the Keithley 238 precision current source. Figure 15 contrasts the power measurements taken with the spectrum analyzer and the power meter, while a typical output spectrum for the recontacted VCO chip is depicted in figure 16. Although the peak power measured using the spectrum analyzer was now 6 dB less than the previous measurement (-90 verses -84 dBm), the measurement difference between figures 12 and 16 is likely a result of losses incurred by the chip recontacting.

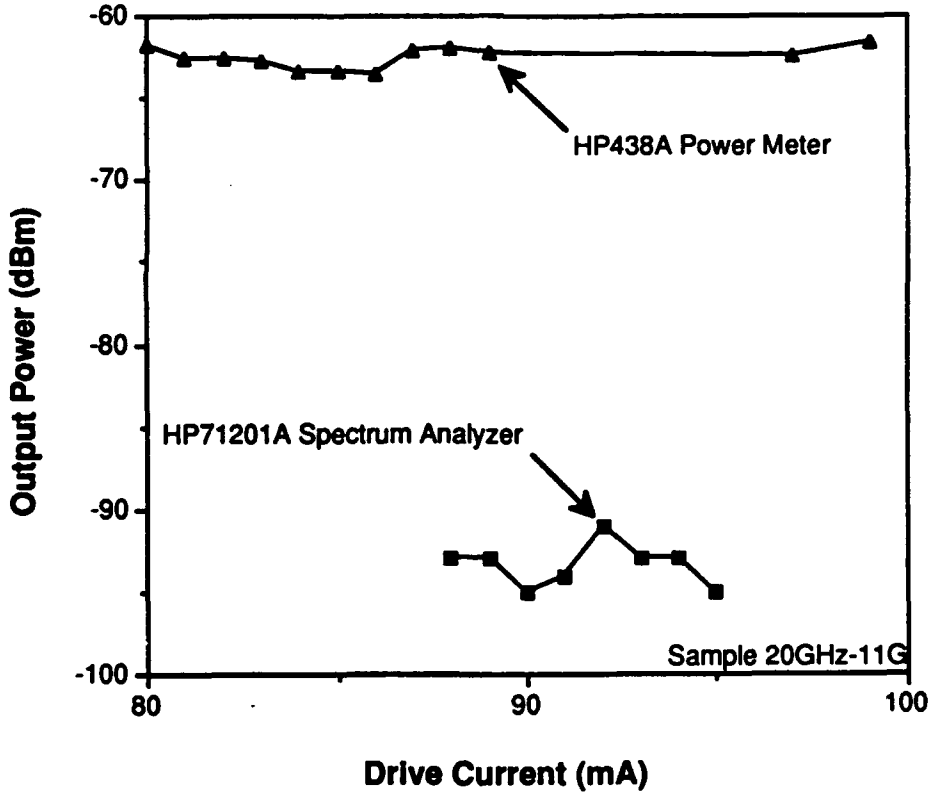

Figure 15. Output Power versus Bias Current

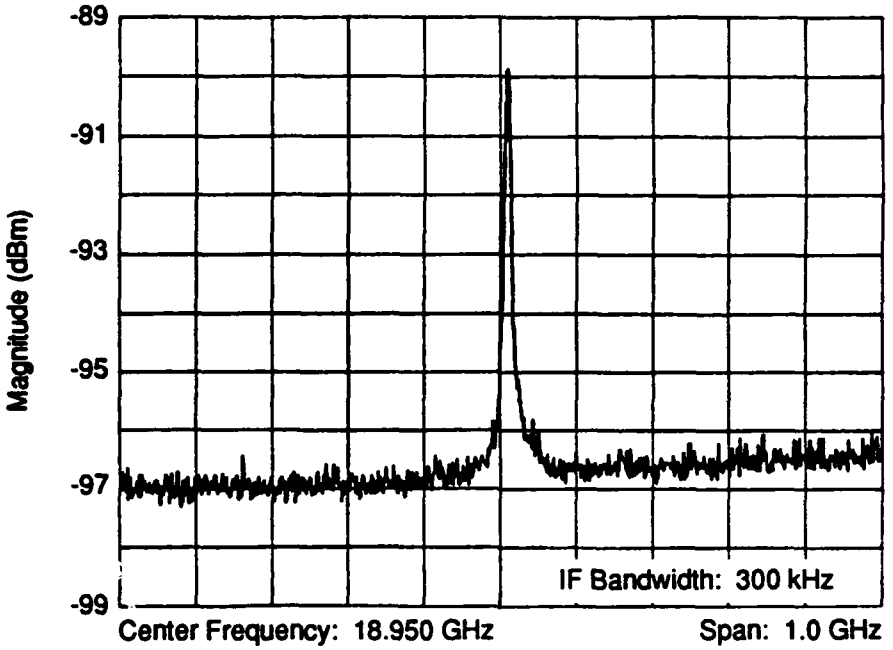

Figure 16. Typical VCO Output Power Spectrum

It is important to recognize that the bandwidth of the spectrum analyzer measurement (figure 16) is quite narrow with respect to the array output bandwidth. SUNY measured an output radiation bandwidth of 20 MHz at 4.2 K, whereas it was necessary for MITRE to use a resolution bandwidth of 300 kHz to sufficiently lower the noise floor to allow the spectrum analyzer power measurements. Since the bolometric power meter integrates all incident RF power, this fact alone accounts for a 20 dB measurement difference between the power meter and the spectrum analyzer. We were not able to correlate this measurement with on-chip power measurements, because MITRE does not have a sufficiently sensitive voltmeter to measure Shapiro steps. SUNY has also suggested [17] that the measured frequency peaks as reported here may be the second harmonic response, and that the fundamental response (at the same frequency) would be obtained at about twice this bias current. We do not believe this to be the case, and through an additional spectrum analyzer investigation we have confirmed that we were indeed measuring the fundamental response.

The insertion loss of the cryogenic probe and connecting cable could be another contributor to the observed output power differences. Insertion loss measurements were taken for the cryogenic probe, and the cable that attached the probe to the test equipment. Figure 17 shows a plot of insertion loss versus frequency for the cryogenic probe, and connecting cable. The maximum insertion loss measured was approximately 6.5 dB at a

frequency of 20 GHz. In comparison, the maximum insertion loss of the SUNY probe and connecting cable has been reported to be about 3 dB [17].

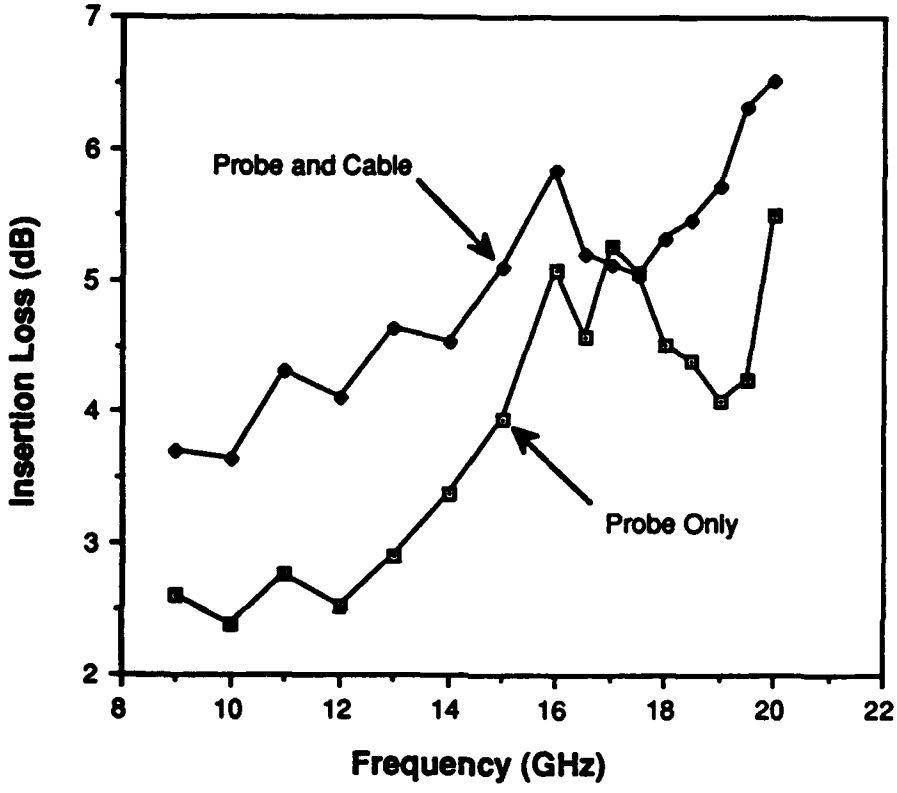

Figure 17. Insertion Loss of the Cryogenic Probe

In concluding our observations on the performance of the sample 20GHz-11G, there are inconsistences between the MITRE data and the baseline data on the array as reported to MITRE by SUNY. The major difference is that the narrowband spectrum analyzer power measurement fails to integrate the available output power. Further measurements should be performed at lower temperature (1.4 K) in order to narrow the bandwidth of the output radiation.

More recently, Wan *et al.* [18] have reported on the ability of these arrays to track a given frequency and then change rapidly to another frequency in response to various modulating bias inputs. They report the ability to tune and track a modulating input at a center frequency

in the 12 to 18-GHz range exceeds a rate of 3.6 GHz. They also report a power level of 0.2 μW as detected on the oscillator chip. When we take into account the impedance mismatch (50:1) in transitioning to the output coax and the 6 dB loss in that coax to room temperature, it appears that our power measurement is about 10 dB down from this level. However, we made a narrow band (300 kHz) measurement by necessity, and the actual power spectrum is more likely to be on the order of 20 MHz.

SECTION 4

CONCLUSION

In summary, theoretical modelling and analysis of superconducting voltage controlled oscillators as driving sources for digital converters is inconclusive. This investigation has not demonstrated their utility for that purpose.. MITRE measurements of VCO chip number 20GHz-11G have been completed to the extent possible with existing MITRE equipment. We have confirmed that coherent oscillations with some degree of phase locking of the 65 junctions of the array are observed. Overall system output power as measured at MITRE at 18 GHz was -84 dBm when measured with a resolution bandwidth of 300 kHz. The fit of the data and such measurements as we can perform on the detector junction appear to be self consistent. VCO output power levels of 0.02 to 0.2 microwatts may be usable for a frequency discriminator drive source in a superconducting analog-to-digital converter design. But if the output spectrum is much broader than 300 kHz, then the precision requirements will be compromised. Measurements by investigators at the State University of New York on these multiple-junction oscillators demonstrate the ability of these arrays to change their output frequency rapidly (a rate in excess of 3.6 GHz) in the range of 12 to 18 GHz.

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GLOSSARY

ADC	analog-to-digital converter
SADC	superconducting analog-to-digital converter
VCO	voltage-controlled oscillator

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