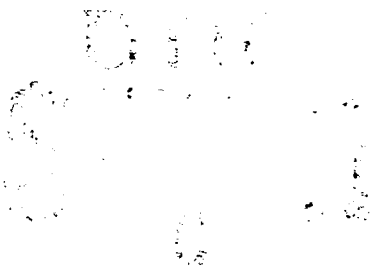

Technical Report 1439
July 1991

ATV Encoder and Decoder Monitor Circuits

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W. S. Morinaga
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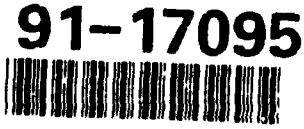

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ADMINISTRATIVE INFORMATION

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Under authority of
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Advanced Systems
Division

RBT

SUMMARY

OBJECTIVES

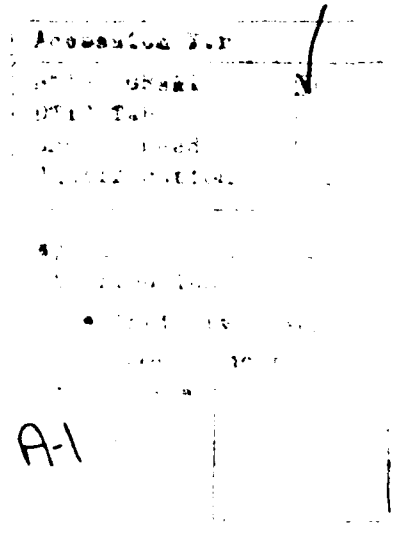
This report was produced to describe the circuits the Advanced Tethered Vehicle (ATV) system employs to monitor the telemetered signals between the surface of the ocean and the submersible vehicle. An additional objective of the report was to explain how these ATV system circuits facilitate in troubleshooting the system.

RESULTS

During initial checkout of the ATV system and throughout the systems tests, the encoder monitor and decoder monitor circuits clearly demonstrated their worth in detecting and troubleshooting problems. In many cases, by using these circuits, malfunctions were rapidly isolated to the surface equipment or to the vehicle equipment. Thus, these monitoring circuits have proven effective in decreasing the ATV system's mean time to repair (MTTR).

RECOMMENDATIONS

In addition to using these monitoring circuits with the Loral encoder and decoder units, with some modification, these circuits can also be used to monitor other similar telemetry systems employing digitally multiplexed data.



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CONTENTS

FIGURES

INTRODUCTION AND GENERAL DESCRIPTION

ATV DESCRIPTION

The Advanced Tethered Vehicle (ATV) system was developed and tested by the Naval Ocean Systems Center, Hawaii Laboratory. The ATV is a remotely operated submersible system designed to perform general work missions down to ocean depths of 20,000 feet. Figure 1 shows the overall ATV system concept. It consists of five main components: (1) the submersible vehicle, (2) the tether cable, (3) the handling system, (4) the control van, and (5) the auxiliary equipment.

The submersible vehicle performs work missions such as installation, maintenance, repair, rescue, or recovery. To perform its mission, the vehicle has two state-of-the-art, position-controlled, force-feedback manipulators, and a variety of tools. Six TV cameras, including a stereo pair, provide visual feedback. To guide the vehicle to the work site, the operator employs five thrusters and various sensors onboard the vehicle, and a deep ocean navigation system.

A tether cable, attached to the vehicle, transmits power to the vehicle and also signals between it and the surface. The tether cable consists of three electrical conductors, three optical fibers, and Kevlar strength members. Signals are multiplexed over one of the three optical fibers, while power is transmitted over the three electrical conductors.

At the surface, the handling system launches and recovers the vehicle, and manages the tether cable. The control van houses the operators and the consoles that control the system. It also contains the electronics that operate the vehicle and communicate with it. Included in the auxiliary equipment are two electrical generators that supply power to the system and also to the maintenance facilities.

SCOPE

This report describes the circuits the ATV system employs to monitor the telemetered signals between the surface and the submersible vehicle. These circuits provide on-line checking of the individual bits in the serial data stream. The ATV telemetry subsystem is also described to show the correlation and importance of the monitor circuits to the system. The telemetry subsystem is presented first, followed by a description of the monitor circuits and their relationships. The report also explains how these circuits facilitate troubleshooting the system.

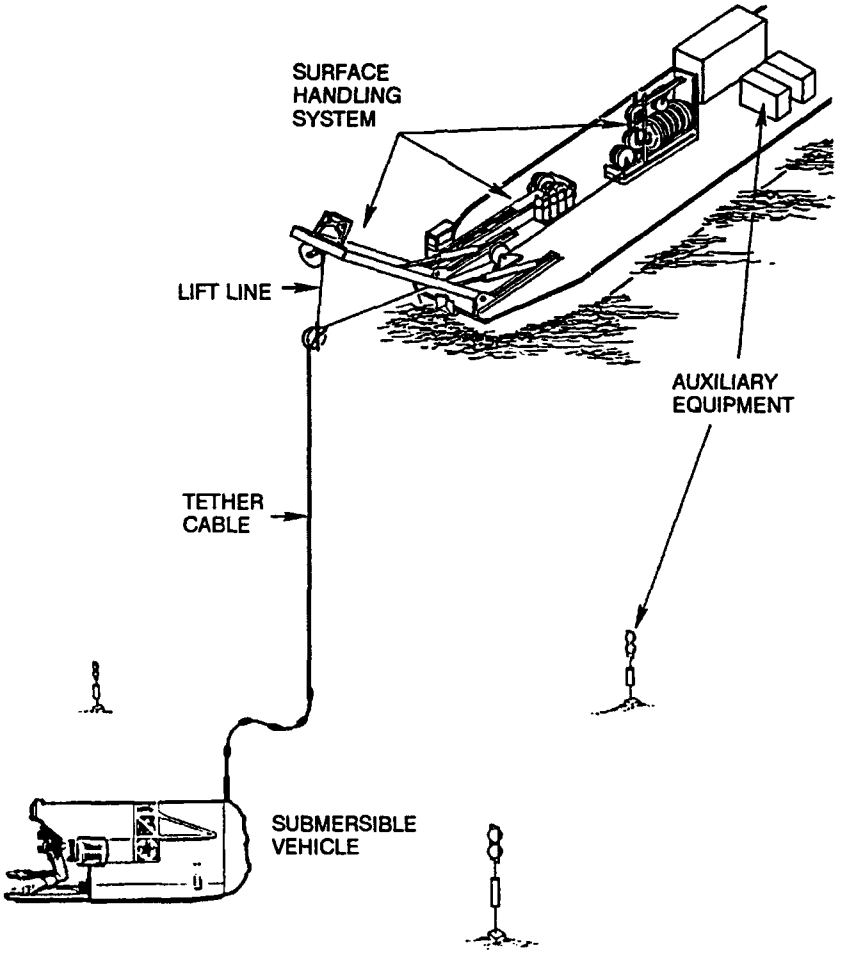


Figure 1. ATV system concept.

ATV FIBER-OPTIC TELEMETRY DESCRIPTION

This telemetry system (figure 2) utilizes wavelength division multiplexing to provide a full-duplex communications system. The downlink optical wavelength is 1.55 microns, while the uplink optical wavelength is 1.3 microns. Commands are transmitted from the surface to the vehicle on the downlink telemetry channel, while vehicle instrumentation data and videos are transmitted from the vehicle to the surface on the uplink channel. All the telemetered signals are digitized, serially multiplexed, converted to an optical signal, and transmitted to the receiver. At the receiver, the optical signal is reconverted to an electrical signal, and the demultiplexer outputs the original input signals.

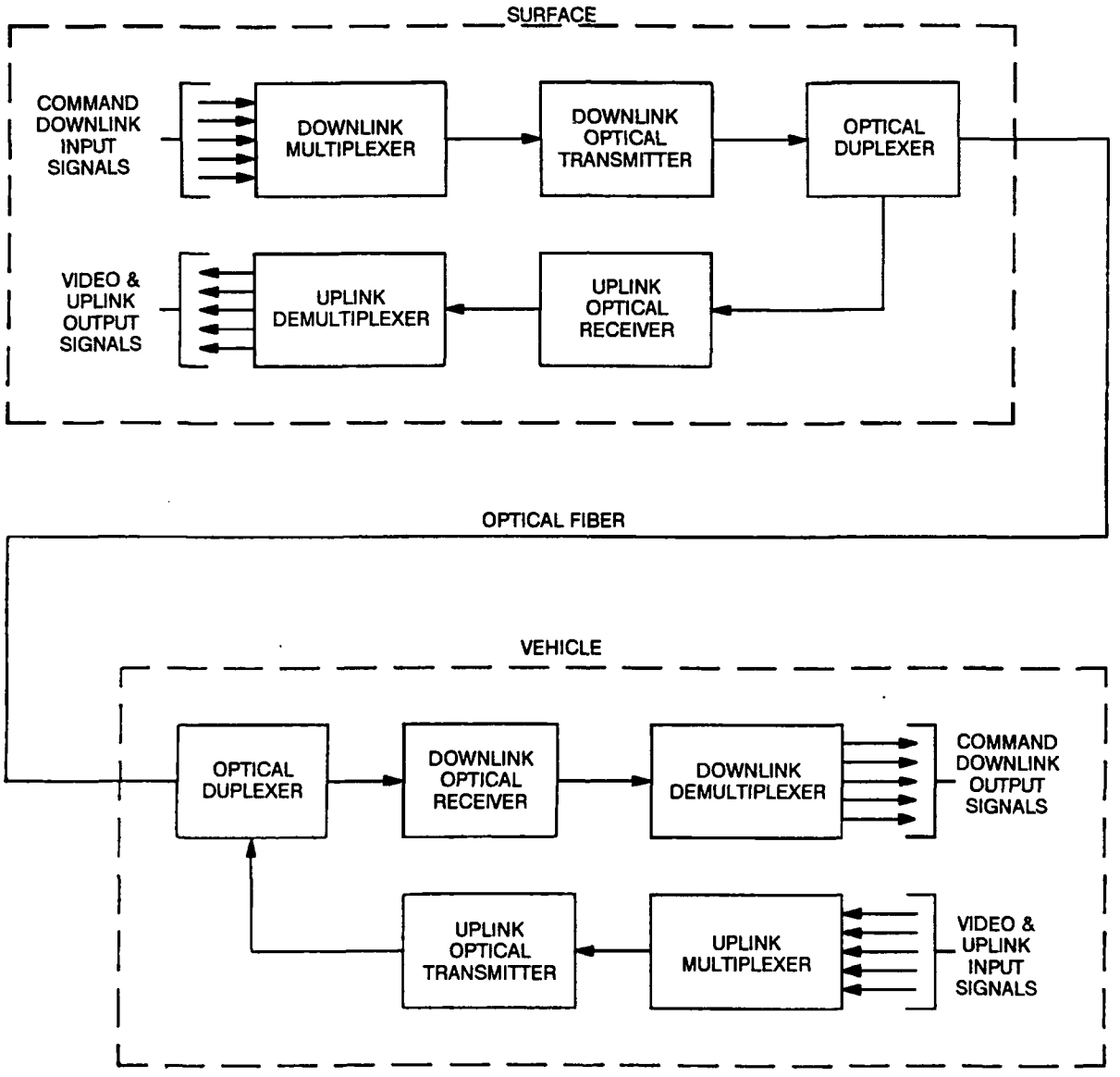


Figure 2. ATV telemetry system, block diagram.

DOWNLINK TELEMETRY CHANNEL

The downlink channel is illustrated in figure 3. Signals transmitted from the surface to the vehicle are the vehicle commands, sonar commands, manipulator commands, and emergency commands. The vehicle command signals are low frequency signals that include digital control signals for switching lights, motors, or solenoid valves; and analog control signals for proportional control of servo valves. These vehicle commands are digitized and multiplexed into a 20-kbps bit stream by the PCM-440A Encoder manufactured by Loral Data Systems. This 20-kbps bit stream and the other commands are multiplexed by a Universal Asynchronous Receiver/Transmitter (UART). The UART's multiplexed output goes to the 1.55-micron optical transmitter.

At the vehicle, the 1.55-micron optical signal is launched into an optical receiver that converts this optical signal back to an electrical one. The signal is then routed to a UART demultiplexer. The vehicle command signal output from the UART is sent to the APD-44A Decoder manufactured by Loral Data Systems. This decoder demultiplexes the 20-kbps bit stream and outputs the individual analog and digital control signals.

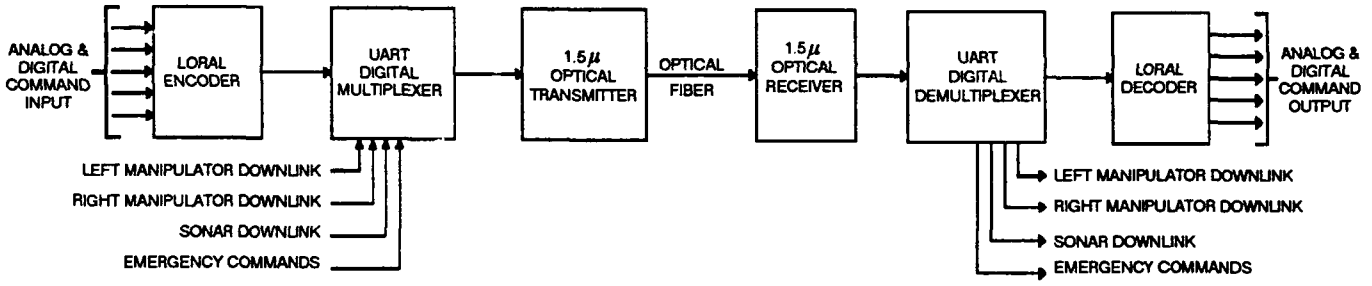


Figure 3. Downlink telemetry channel, block diagram.

UPLINK TELEMETRY CHANNEL

The uplink channel (figure 4) transmits two realtime videos, sonar uplink data, two manipulator uplink data, and vehicle instrumentation data. Similar to the downlink channel, the uplink telemetry channel serially multiplexes the various signals and converts this serial digital signal to an optical signal. The difference is that the the uplink optical wavelength is 1.3 micron. At the surface, the optical receiver reconverts the optical signal back to an electrical signal. This serial digital signal is then demultiplexed, and the original input signals are reproduced.

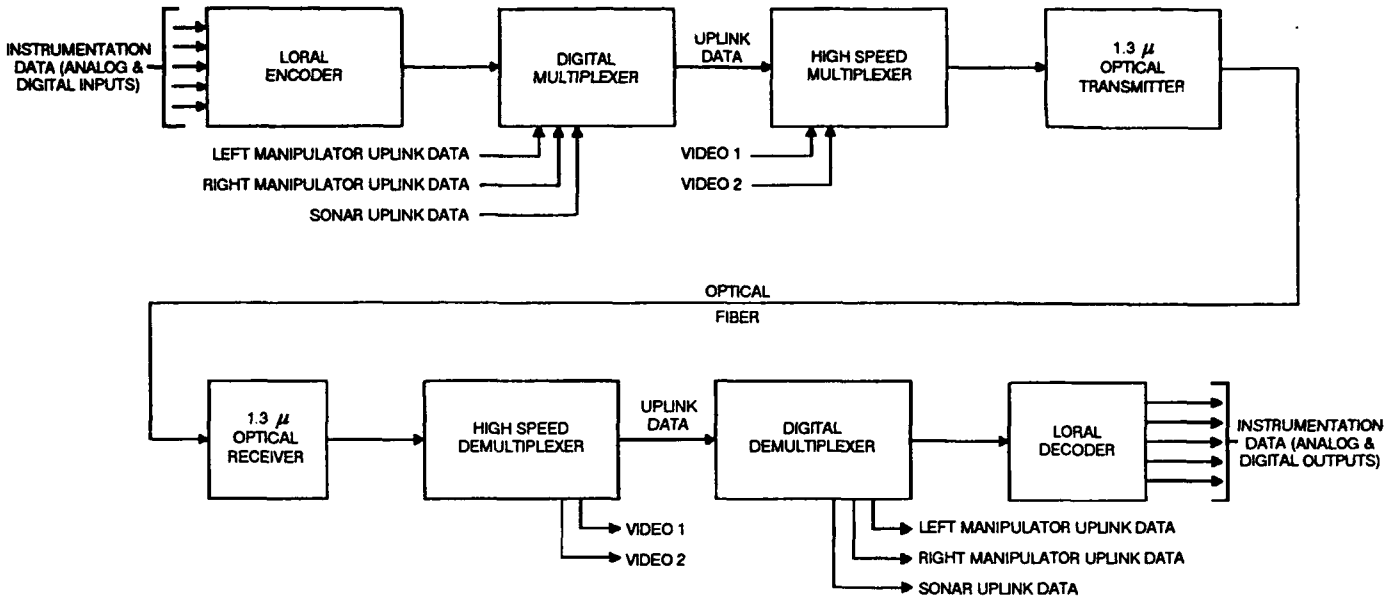


Figure 4. Uplink telemetry channel, block diagram.

Like the vehicle command signals in the downlink channel, the vehicle instrumentation signals are multiplexed by the Loral PCM-440A Encoder, and demultiplexed by the Loral APD-444A Decoder. The vehicle instrumentation data are the low frequency vehicle status and sensor signals, such as heading, altitude, pressure, and temperature data. The instrumentation serial bit stream from the encoder, along with the two manipulator uplink data and the sonar uplink data, are multiplexed by the digital multiplexer. The multiplexed output from the digital multiplexer goes to the high speed multiplexer; this multiplexer digitizes the two videos and also multiplexes the digitized videos with the other combined uplink data. The output from the high speed multiplexer is applied to the 1.3-micron optical transmitter.

At the surface, the optical receiver converts the 1.3-micron optical signal to an electrical signal. This electrical output then goes to the high speed demultiplexer that demultiplexes the input serial bit stream and also converts the digitized video bits to analog signals. The outputs of the high speed demultiplexer are the two videos and the uplink data. Serial uplink data are demultiplexed by the digital demultiplexer. Outputs of the digital demultiplexer are the instrumentation data, the uplink data from the two manipulators, and the sonar uplink data.

LORAL ENCODER AND DECODER

The Loral PCM-440A Encoder is a multiplexer that accepts both analog and digital input signals. It encodes and multiplexes the signals into a synchronous bit stream of digital data. This encoder employs 12-bit analog-to-digital conversion for the analog

inputs. The converse to the encoder is the Loral APD-444 Decoder or Decommutator. It accepts the synchronous bit stream from the PCM-440A Encoder. The decoder bit and frame synchronizes with this received signal, and then demultiplexes these data back into analog and digital signals.

The encoder's output format is as follows. One message frame consists of 65 words, with each word consisting of 16 bits that include 1 parity bit. Thus, a message frame is composed of 65 $\times$ 16 or 1040 bits. The frame rate is 20 times per second (each individual signal is updated 20 times a second); thus, the bit rate is 20,800 bits per second.

The first two words of the frame, Word 0 and Word 1, are sync words that allow the decoder to determine the start of a new message frame. Word 2 to Word 49 are the digitized equivalents of the encoder analog input signals. Thus, 48 analog signals are available for transmission. Since the analog signals are digitized to 12 bits of resolution, only the first 12 bits of the analog words represent data. The last 3 bits of the analog word are not used for data. Word 50 to Word 64 are strictly digital bits of information; that is, all 15 bits of each word are used for digital data. Thus, 225 digital bits of data can be multiplexed.

FUNCTION OF THE MONITOR CIRCUITS

The function of the circuits described in this report is to provide online monitoring or checking of both the data being transmitted by the encoder and the data being received by the decoder. These circuits enable the monitoring of (1) any individual command signal that is transmitted from the surface to the vehicle and (2) any individual instrumentation signal that is received at the surface from the vehicle. This capability to monitor any word or bit in the serial data stream is an excellent troubleshooting aid. In the ATV system, these circuits can quickly determine whether a malfunction is in the surface equipment or on the vehicle.

Besides the capability to monitor individual command and instrumentation signals, the encoder monitor and the decoder monitor circuits can check the status of the ATV telemetry system. The telemetry system's full-duplex operational status can be checked by sending a known command signal on the downlink channel and looping it back onto an instrumentation signal on the uplink channel. By comparing the transmitted downlink signal with its looped-back, received uplink signal, the integrity of the telemetry system can be determined.

Figure 5 shows how the encoder monitor and the decoder monitor circuits were implemented to check the ATV telemetry system. Monitoring was accomplished using the encoder monitor and the decoder monitor circuits. When Word N is selected by the encoder monitor circuit, this 16-bit word (15 bits plus parity bit) is displayed and indicates the status of all 16 bits. The 15 bits of the selected Word N (parity bit excluded) are also wired to the Word 57 inputs of the Loral encoder. Thus, for the downlink command data stream, the 16 bits of Word 57 matches the 16 bits of selected Word N.

At the vehicle end, the 15 bits of Word 57 output from the command decoder are wired to the Word 53 inputs of the instrumentation Loral encoder. So Word 57 of the command data stream (downlink) is transmitted back on Word 53 of the instrumentation data stream (uplink). If Word 53 is the selected Word N for the decoder monitor circuit, then Word 53's 16 bits will match the 16 bits of the command monitor circuit's selected word. If all Word 53's 16 bits of the decoder monitor match the selected Word N's 16 bits of the command encoder, this indicates that the telemetry system is functioning correctly.

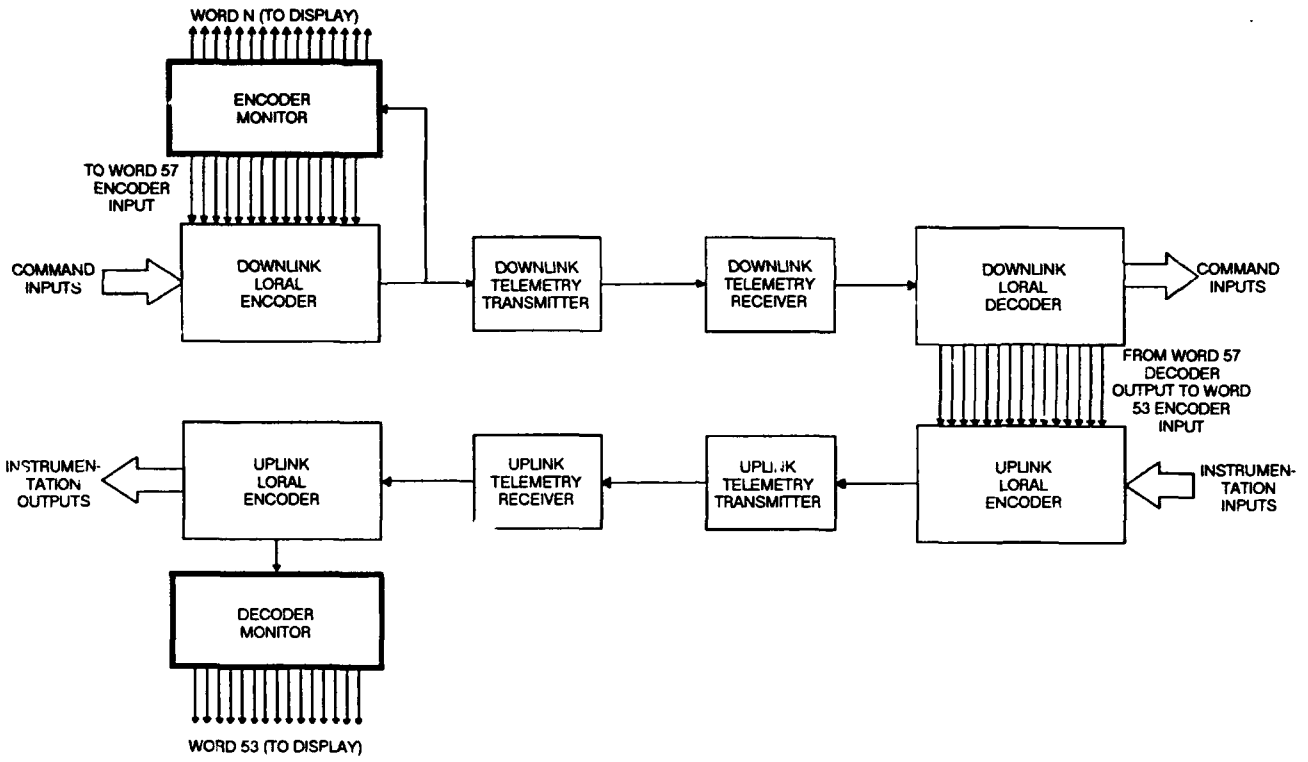


Figure 5. Telemetry status check scheme.

ENCODER MONITOR CIRCUIT

The encoder monitor circuit enables monitoring of the data output signal of the Loral encoder. Figure 6 is a block diagram of the encoder monitor circuit. The major functional blocks are the serial-to-parallel shift register, the word select timing circuit, and the storage register. The "NRZ DATA" signal is the "NRZ-L OUTPUT" serial data stream that is output from the Loral PCM-440A Encoder. The "BIT RATE CLOCK," "WORD PULSE CLOCK," and "FRAME SYNC" signals are also outputs provided by the encoder and are used by this monitor circuit to generate the proper timing signals.

The serial-to-parallel shift register converts the input serial "NRZ DATA" signal to 16 parallel bits (one word length of data). These 16 bits are shifted through the register at the "BIT RATE CLOCK" frequency. The word select timing circuit generates the appropriate signals to select the desired 16-bit word to be monitored. The inputs to this circuit are the "FRAME SYNC," "WORD PULSE CLOCK," "BIT RATE CLOCK," and "BCD WORD SELECT" signals. The circuit's output is the "WORD LOAD" signal that strobes the storage register. The storage register then latches the selected 16-bit word when the appropriate pulse appears on the "WORD LOAD" signal.

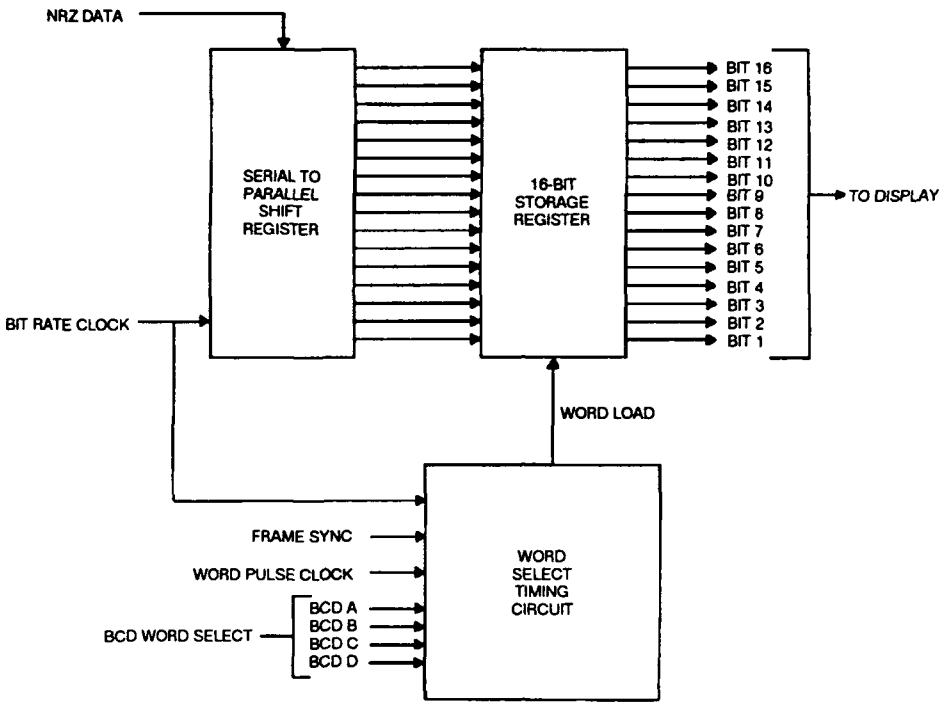


Figure 6. Monitor circuit, block diagram.

CIRCUIT DESCRIPTION

The following paragraphs provide a detailed description of the encoder monitor circuit. Figure 7 is the schematic diagram for this circuit.

U4 and U5 are two 8-bit serial shift registers combined to form a 16-bit serial-to-parallel shift register. The "NRZ-L DATA" is the serial digital data input to pin 1 of shift register U5. The input "BIT RATE CLOCK" signal is inverted by U2A. This inverted signal is called the "SHIFT CLOCK" and is applied to U4-8 and U5-8, which are the clock inputs to the two shift registers. The 16 parallel outputs of U4 and U5 are the individual bits of the "NRZ-L DATA" signal being shifted at the "SHIFT CLOCK" frequency.

The word select timing circuit consists of U2, U3, U6, U7, U8, U13, R3, C17, R5, and C19. The "FRAME SYNC" signal is connected to the RC network, R3 and C17, that filters out noise from the input "FRAME SYNC" signal. This filtered signal then goes to monostable multivibrator, U3A. U3A generates a 600-μs pulse at the trailing or negative-going edge of the "FRAME SYNC" pulse. This U3A output (pin 4) is called the "WORD COUNTER LOAD" signal and is a negative-going pulse. It is connected to the LOAD inputs (pin 11) of both U7 and U8, the synchronous BCD counters. When there is a pulse on the "WORD COUNTER LOAD" signal, the seven "BCD WORD SELECT" inputs are loaded into U7 and U8 on the negative-going edge of the pulse. The "BCD WORD SELECT" inputs are the binary-coded decimal equivalent of the decimal number N, which is the selected word being monitored. N can be any number between 0 and 64.

R5 and C19 filter out noise from the incoming "WORD PULSE CLOCK" signal. This filtered signal is inverted by U2B and is then input to U8-4, the down-count input of the BCD counter. Each time a pulse appears on the "WORD PULSE CLOCK" signal, the combined BCD count of U7 and U8 is decreased by 1 on the positive-going edge of the pulse. When N number of these pulses are counted by U7 and U8, the U7 and U8 outputs will be "0." That is, the outputs Q_A, Q_B, Q_C, and Q_D shall all be "0" or in the low state. On the next pulse of the "WORD PULSE CLOCK" signal, a negative-going pulse is generated at the U7 $\overline{BO}$ output. This $\overline{BO}$ output is connected to the shift register U6 (pin 1).

Shift register U6, in conjunction with the "SHIFT CLOCK" signal, delays the pin 1 input signal by $1\frac{1}{2}$ bit clock times. This delayed signal is at U6-4 and is NANDED by U2C with the "BIT RATE CLOCK" signal. The output of the NAND gate, U2C-8, is inverted by U13E; this inverted output is called the "WORD LOAD" signal. The "WORD LOAD" signal strobes the latches U9 and U10 at the appropriate time. That is, when the 16 data bits of the selected word (Word N in the message) are at the outputs of shift registers U4 and U6, the "WORD LOAD" signal latches U9 and U10. This latching occurs on the positive-going edge of the "WORD LOAD" pulse. Thus, the U9 and U10 outputs are the 16 bits of the selected word (Word N).

TIMING CIRCUIT

Figure 8, the timing diagram for the encoder monitor circuit, shows the waveforms of the signals and also the timing relationships among these signals. Each word of the message frame consists of 16 bits, with a word length of 768 µs. The frequency of the "BIT RATE CLOCK" signal is 20.8 kHz, and the bit period is 48 µs. The rising or positive-going edge of this clock signal coincides with the start of each bit in the message frame. The frequency of the "WORD PULSE CLOCK" signal is 1.3 kHz, with a pulse width of 48 µs. This pulse coincides in time with Bit 15 of each word in the message frame. The "FRAME SYNC" signal has a frequency of 20 Hz and a pulse width of 768 µs. The negative-going edge of the "FRAME SYNC" signal occurs 1-bit time before Word 0 Bit 0 in the message frame. The "WORD COUNTER LOAD" signal has a pulse that occurs at a 20-Hz rate and has a pulse width of about 600 µs.

DECODER MONITOR CIRCUIT

The decoder monitor circuit monitors tne Loral decoder data input signal. Figure 6 is also the block diagram for this circuit. The major functional circuit blocks are the serial-to-parallel shift register, the word select timing circuit, and the storage register. The "NRZ DATA" input to the circuit is the "DELAYED NRZ" output signal from the Loral APD-44A Decoder. The "WORD PULSE CLOCK" signal is the "WORD CLK" signal output from the Loral decoder. The "BIT RATE CLOCK" and the "FRAME SYNC" signals are also outputs from the decoder and are used by the monitor circuit to generate the proper timing signals.

The serial-to-parallel shift register converts the serial "NRZ DATA" signal to 16 parallel data bits. These 16 bits are shifted through the register at the "BIT RATE CLOCK" frequency. The word select timing circuit generates the appropriate signals for selecting the desired 16-bit word to be monitored. The inputs to this circuit are the "FRAME SYNC," "WORD PULSE CLOCK," "BIT RATE CLOCK," and "BCD WORD SELECT" signals. This circuit's output is the "WORD LOAD" signal that goes to the storage register. The storage register latches the selected 16-bit word, when the appropriate pulse appears on the "WORD LOAD" signal.

CIRCUIT DESCRIPTION

The following paragraphs provide a detailed description of the decoder monitor circuit. Figure 9 is the schematic drawing for this circuit.

U2 and U4 are two 8-bit serial shift registers combined to form a 16-bit serial-to-parallel shift register. The "DELAYED NRZ-L DATA" serial input goes to shift register U4 (pin 1). The "BIT RATE CLOCK" signal goes to U2-8 and U4-8, the shift register clock inputs. The combined 16 parallel outputs of U2 and U4 are the individual bits of the "NRZ-L DATA" signal being shifted at the "BIT RATE CLOCK" frequency.

The word select timing circuit consists of U6, U7, U8, U9, R3, C15, R5, and C17. The "FRAME SYNC" signal is connected to the RC network of R3 and C15 that filters out noise on the incoming "FRAME SYNC" signal. This filtered "FRAME SYNC" signal goes to monostable multivibrator U6A. U6A generates a 600-μs pulse at the trailing or negative-going edge of the "FRAME SYNC" pulse. The output of U6A (pin 4) is called the "WORD COUNTER LOAD" signal and is a negative-going pulse. This "WORD COUNTER LOAD" signal is connected to the LOAD inputs of the synchronous BCD counters U7 and U9. When a pulse is on the "WORD COUNTER LOAD" signal, the seven BCD word select inputs are loaded into U7 and U9 on the negative-going edge of the pulse. The "BCD WORD SELECT" inputs are the binary-coded decimal equivalent of the number N, the selected word being monitored. N can be any number between 0 and 64.

R5 and C17 filter out noise from the incoming "WORD PULSE CLOCK" signal. This filtered signal is NANDED with the "WORD COUNTER LOAD" signal. The output of the NAND gate, U8A-3, is applied to the down-count input of BCD counter U9 (pin 4). Each time a pulse appears on the "WORD PULSE CLOCK" signal, the combined BCD count of U7 and U9 is decreased by 1 on the positive-going edge of the pulse. When N number of these pulses are counted by U7 and U9, the outputs of U7 and U9 will be "0." That is, the outputs Q_A, Q_B, Q_C, and Q_D shall all be "0" or in the low state. On the next pulse of the "WORD PULSE CLOCK" signal, a negative-going pulse is generated at the U7 $\overline{BO}$ output (pin 13). This $\overline{BO}$ output is called the "WORD LOAD" signal and is connected to the clock inputs (pin 11) of latches U3 and U5.

The "WORD LOAD" signal strobes the latches U3 and U5 at the appropriate time. That is, when the 16 data bits of the selected word (Word N in the message) are at the shift registers U2 and U4 outputs, the "WORD LOAD" pulse latches U3 and U5. This latching occurs on the positive-going edge of the "WORD LOAD" pulse. Thus, the U3 and U5 outputs are the 16 bits of the selected word (Word N).

TIMING CIRCUIT

Figure 10 is the timing diagram for the decoder monitor circuit. It shows the signal waveforms and the timing relationships among these signals. These signals are very similar to those of the command monitor circuit. Each word of the message frame consists of 16 bits, and the word length is 768 μs. The "BIT RATE CLOCK" signal frequency is 20.8 kHz, and the bit period is 48 μs. The falling or negative-going edge of this clock signal coincides with the start of each bit in the message frame. The "WORD PULSE CLOCK" signal frequency is 1.3 kHz, with a pulse width of 48 μs. This pulse coincides in time with Bit 16 of each word in the message frame. The "FRAME SYNC" signal has a 20-Hz frequency and a pulse width of 24 μs. The positive-going edge of the "FRAME SYNC" signal coincides with the start of Word 0 Bit 0 in the message frame. The "WORD COUNTER LOAD" signal has a pulse that occurs at a 20-Hz rate, with a pulse width of about 600 μs.

EFFECTIVENESS OF CIRCUITS

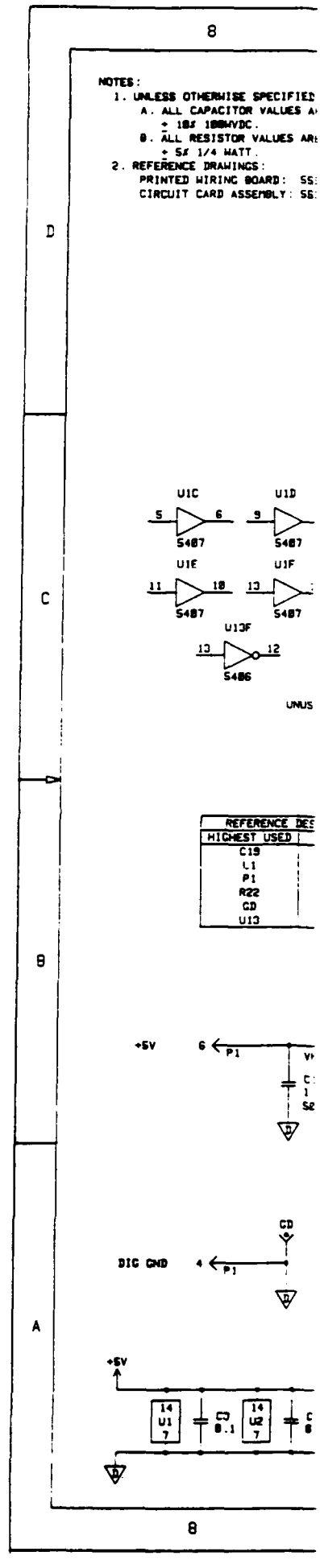
ATV SYSTEM APPLICATION

Many operational hours were logged while developing and testing the ATV system. During its initial checkout and throughout the system tests, the encoder monitor and decoder monitor circuits have demonstrated their worth in detecting and troubleshooting problems. In many cases, malfunctions were quickly isolated to the surface equipment or to the vehicle equipment by using these monitoring circuits. Thus, these circuits have proven effective in decreasing the ATV system's mean time to repair (MTTR).

These monitor circuits were also utilized as a backup for monitoring signals that are displayed to the operators. When a display or the circuit driving that display failed, the monitor circuit was used to select the specific signal that required monitoring. In addition, other signals not normally shown on dedicated displays can also be monitored using these encoder and decoder monitor circuits.

OTHER APPLICATIONS

Besides using these monitor circuits with the Loral encoder and decoder units, these circuits can be used to monitor other similar telemetry systems employing digitally multiplexed data. However, the circuitry would probably have to be modified to match the data or message format and the available timing signals of the particular telemetry system.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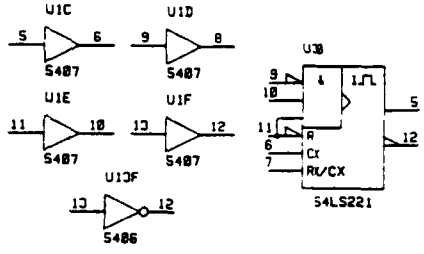
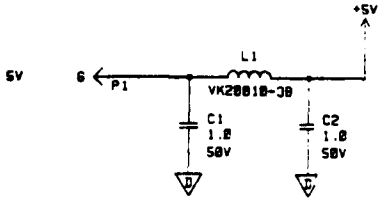
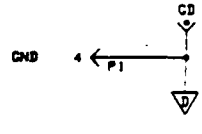
NOTES:
1. UNLESS OTHERWISE SPECIFIED
A. ALL CAPACITOR VALUES A
± 10% 100WVDC.
B. ALL RESISTOR VALUES ARE
± 5% 1/4 WATT.
2. REFERENCE DRAWINGS:
PRINTED WIRING BOARD: 55
CIRCUIT CARD ASSEMBLY: 56
D
C
B
A
U1C
U1D
U1E
U1F
U13F
5
6
9
11
10
13
12
S4B7
S4B6
UNUS
REFERENCE DES
HIGHEST USED
C19
L1
P1
R22
CD
U13
+5V
G
P1
DIG GND
4
14
U1
7
C3
0.1
U2
8

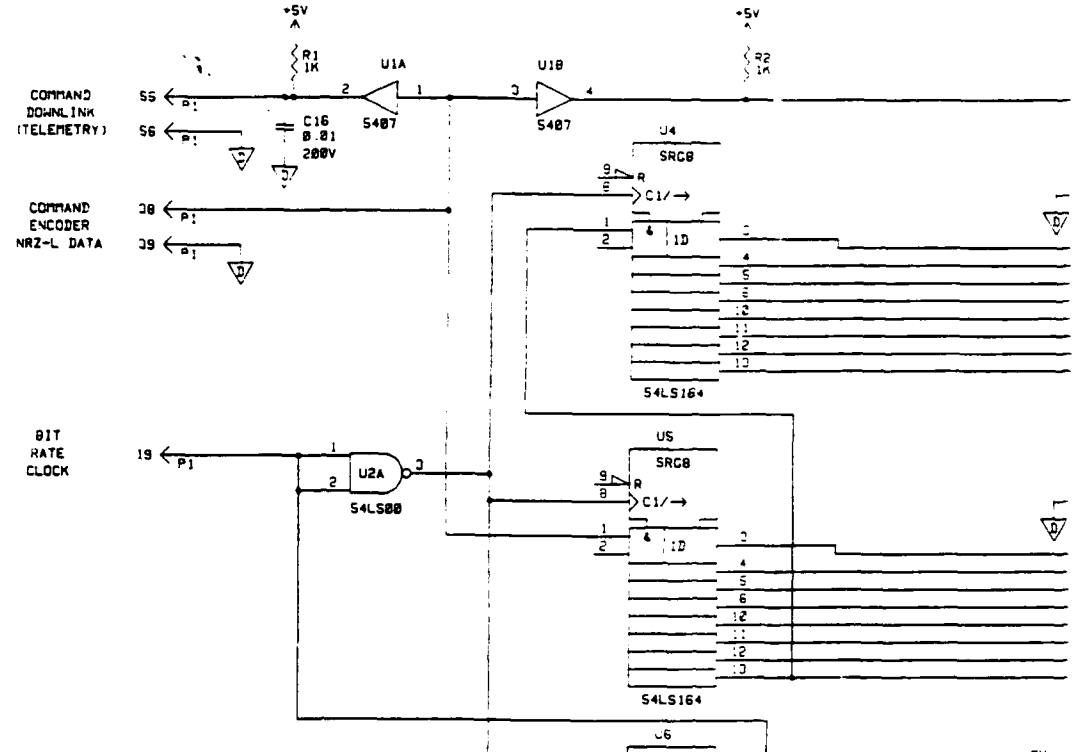
LESS OTHERWISE SPECIFIED:
. ALL CAPACITOR VALUES ARE IN MICROFARADS
± 10% 100WVDC.
. ALL RESISTOR VALUES ARE IN OHMS
± 5% 1/4 WATT.
FERENCE DRAWINGS:
RINTED WIRING BOARD: 55918-8123158
IRCUIT CARD ASSEMBLY: 55918-8123157

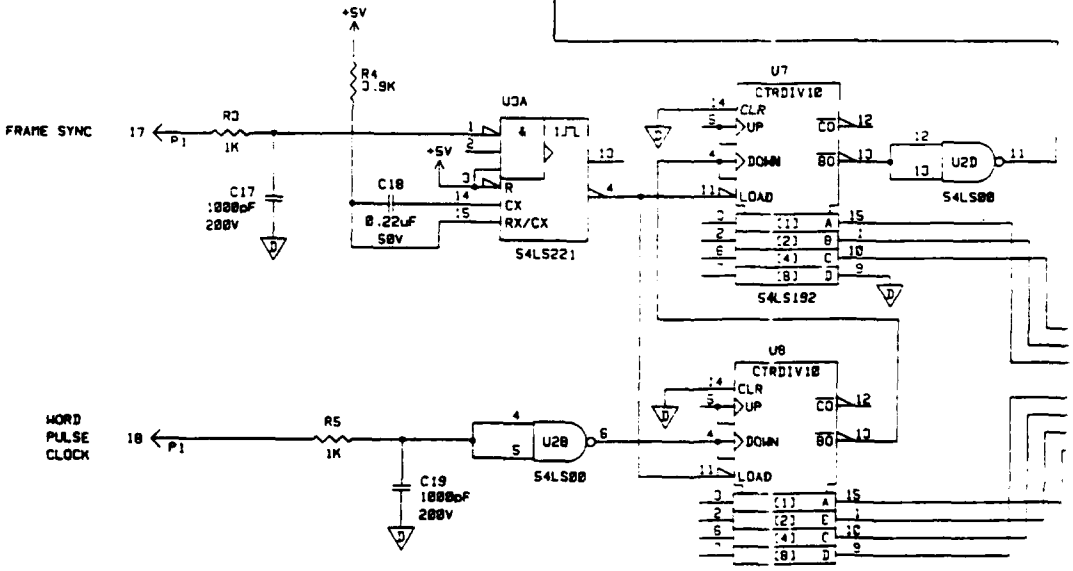


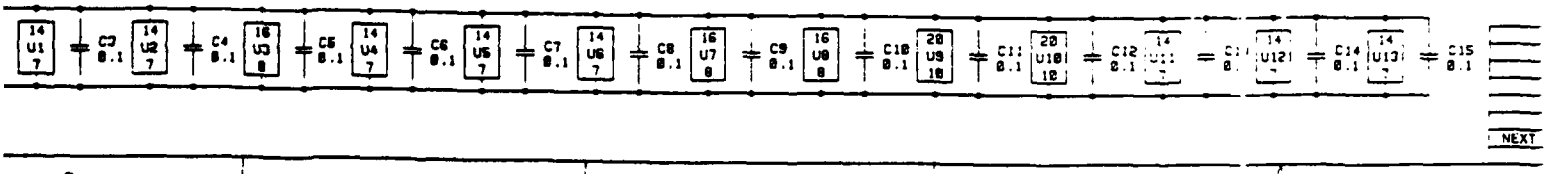
REFERENCE DESIGNATORS	
HIGHEST USED	NOT USED
C19	-
L1	-
P1	-
R22	-
CD	-
U13	-











15-B

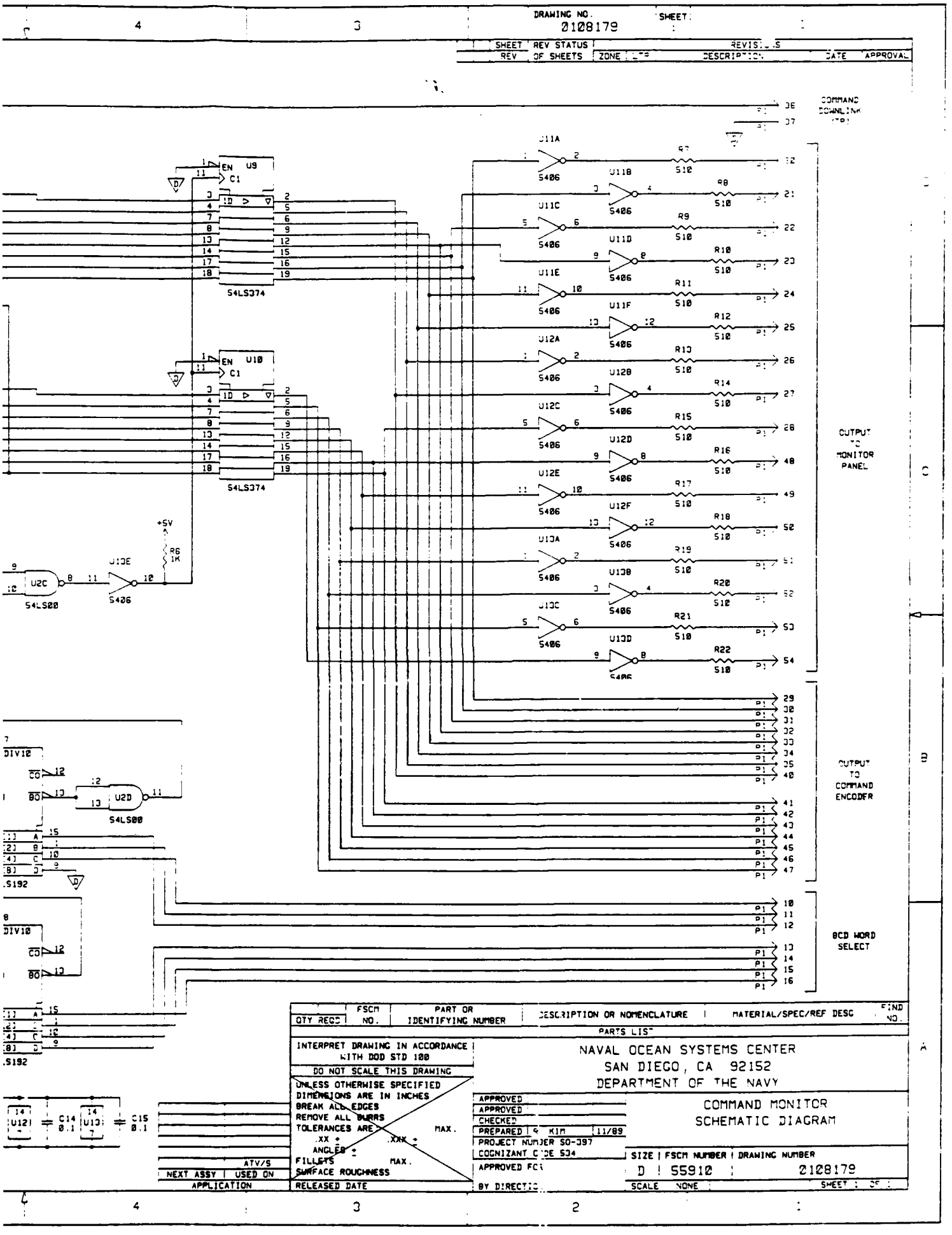
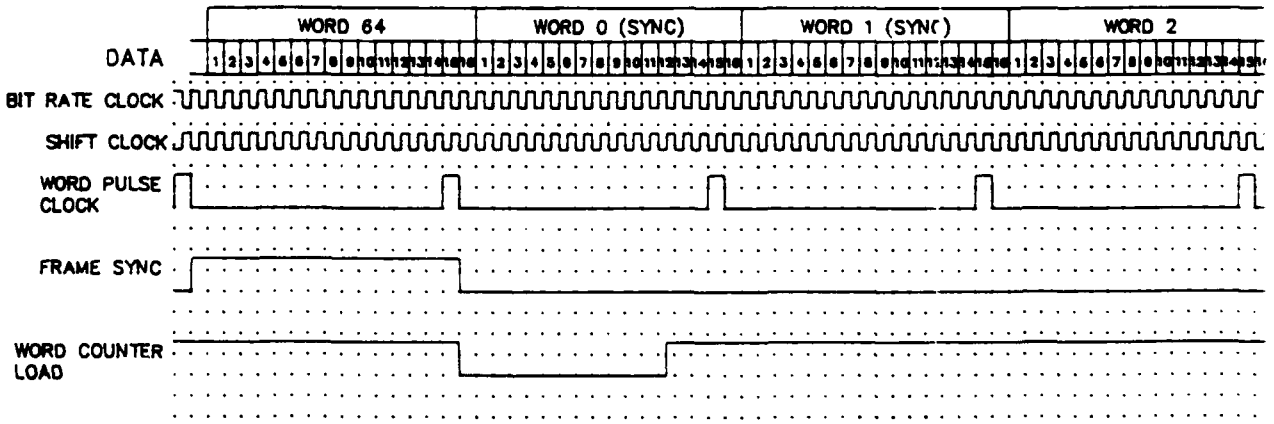


Figure 7. Command monitor, schematic diagram.

11 JUN 1990


WORD 64
WORD 0 (SYNC)
WORD 1 (SYNC)
WORD 2
DATA
BIT RATE CLOCK
SHIFT CLOCK
WORD PULSE CLOCK
FRAME SYNC
WORD COUNTER LOAD

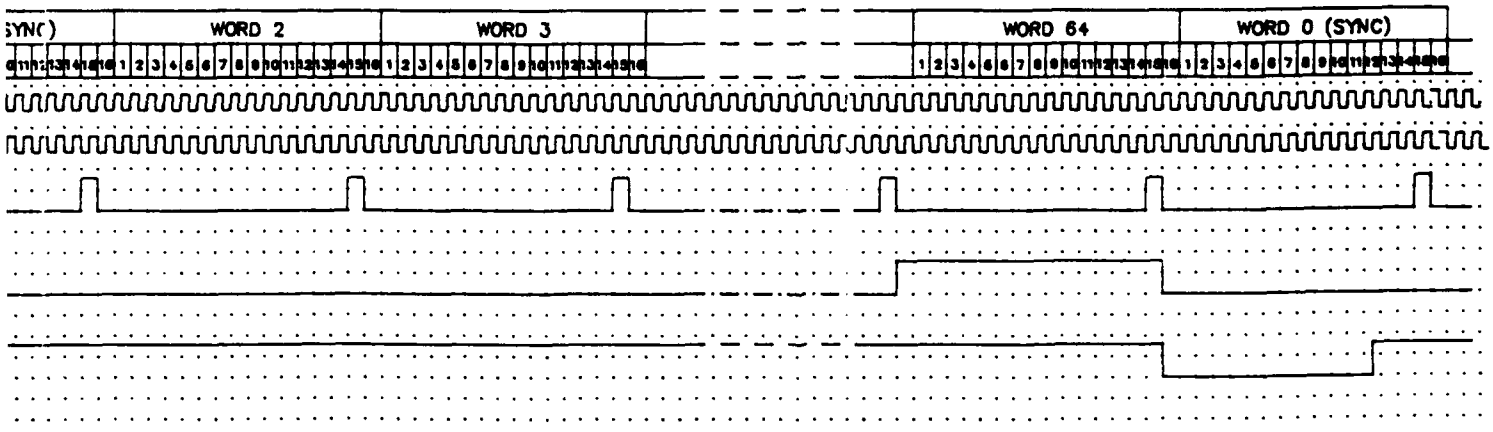
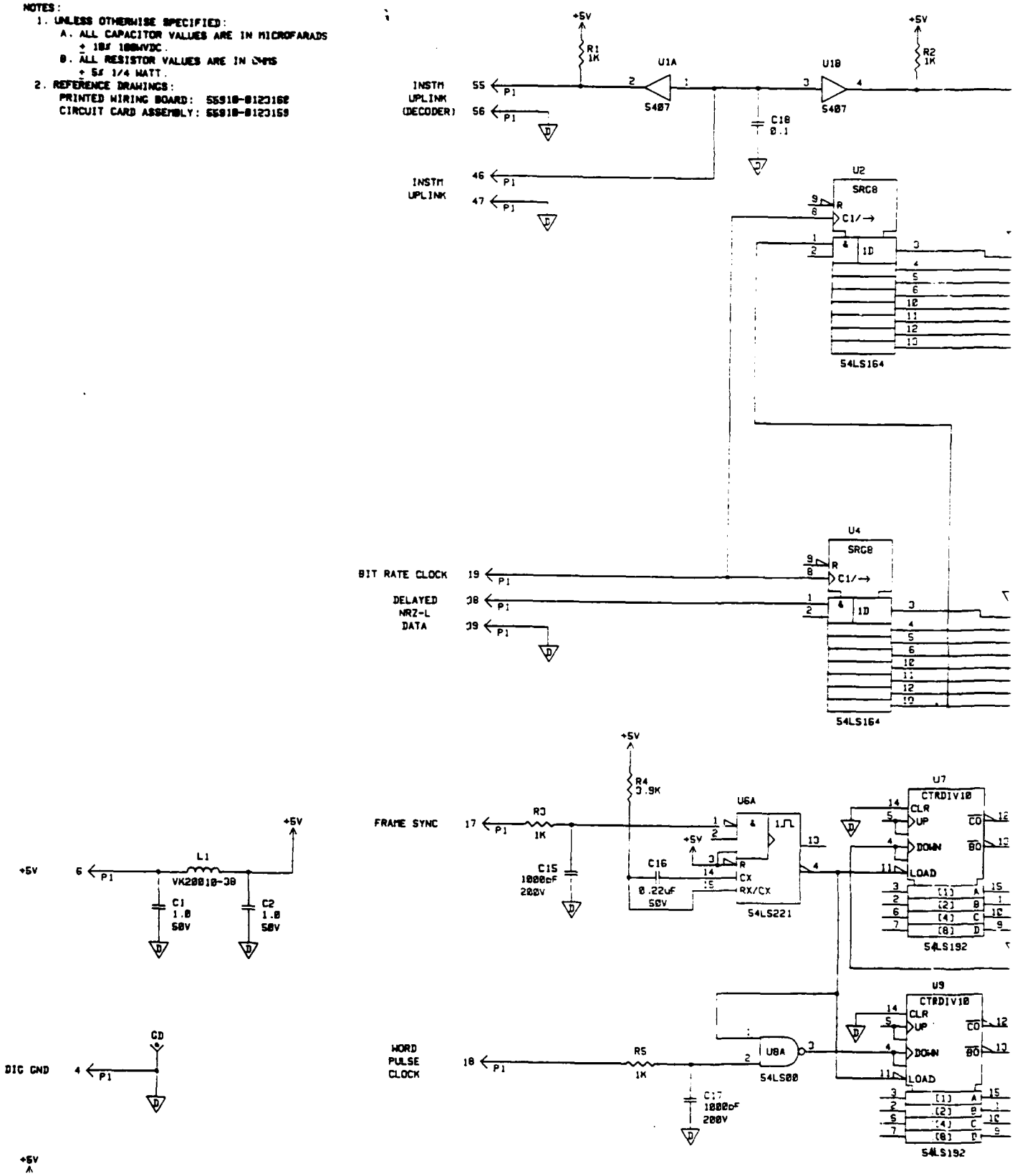


Figure 8. Encoder monitor circuit, timing diagram.

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A. ALL CAPACITOR VALUES ARE IN MICROFARADS ± 10% 100WVDC.
   B. ALL RESISTOR VALUES ARE IN OHMS ± 5% 1/4 WATT.
2. REFERENCE DRAWINGS:
   PRINTED WIRING BOARD: 55910-8123168
   CIRCUIT CARD ASSEMBLY: 55910-8123159



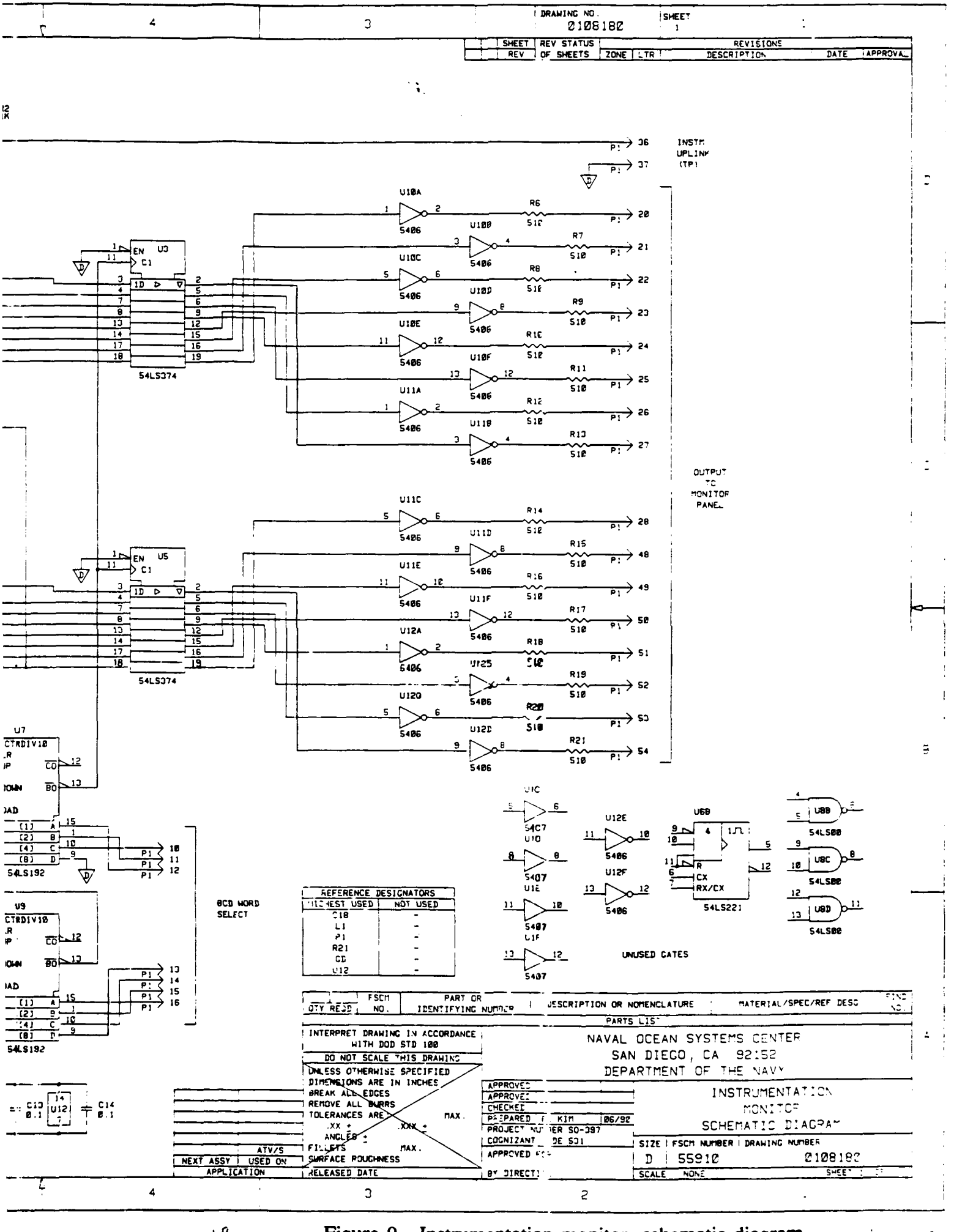
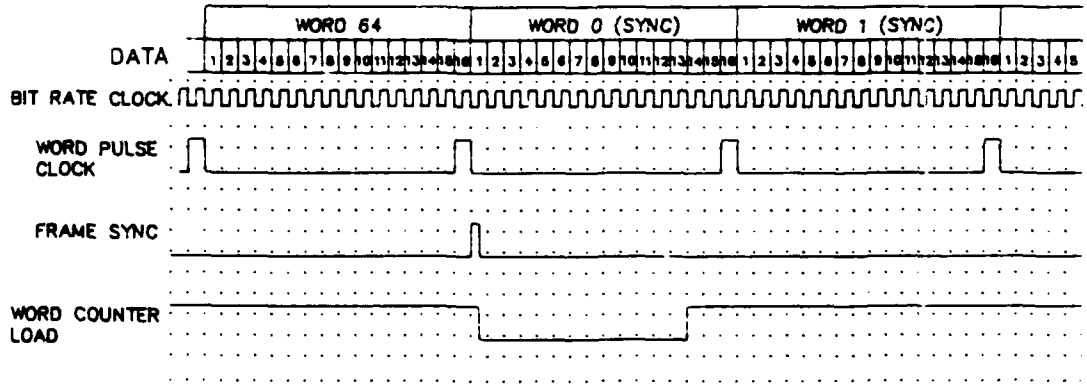


Figure 9. Instrumentation monitor, schematic diagram.


WORD 64
WORD 0 (SYNC)
WORD 1 (SYNC)
DATA
BIT RATE CLOCK
WORD PULSE CLOCK
FRAME SYNC
WORD COUNTER LOAD

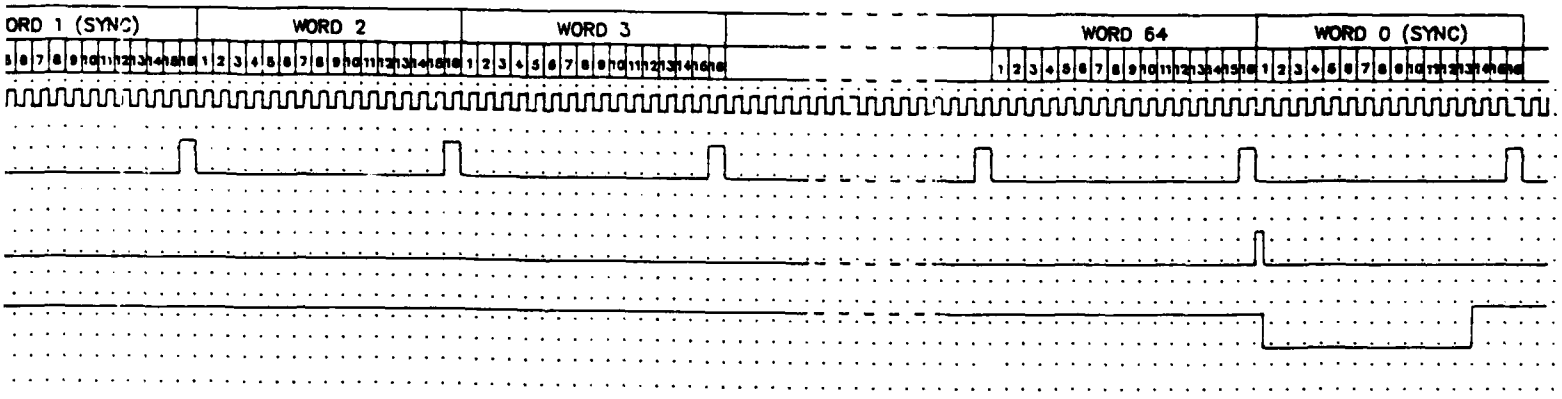


Figure 10. Decoder monitor circuit, timing diagram.

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This report describes the telemetry monitoring circuits employed in the Advanced Tethered Vehicle (ATV) system—a remotely controlled submersible vehicle. These circuits are used to monitor the telemetered commands and data that are transmitted between the surface and the submersible. They provide online monitoring of the individual bits in the serial digital-data stream. The report provides a detailed description of the design and operation of these circuits.

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