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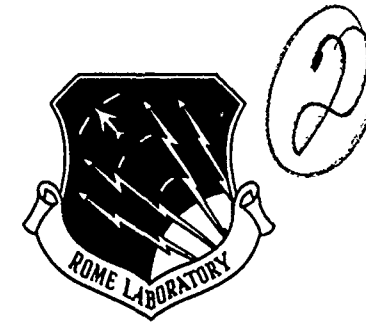

IMPROVED 320x244 - ELEMENT PtSi SCHOTTKY - BARRIER IR-CCD IMAGE SENSOR

David Sarnoff Research Center

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13. ABSTRACT (Maximum 200 words)

This report describes the design, fabrication, and performance of an improved 320x 244-element IR-CCD imager with PtSi Schottky-barrier detectors. The imager has 40mm x 40 mm pixels, and a 44% fill factor.

Design and process modifications used with this imager resulted in a significant improvement in dark-current uniformity and yield. A responsivity of greater than $1x10^4$ electrons/pixel /°C for f/2.0 optics, a saturation signal of $1.4x10^6$ electrons/ pixel, and a charge-transfer inefficiency of $1x10^4$ per transfer were measured for this imager.

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PREFACE

This Final Report was prepared by the David Sarnoff Research Center (Sarnoff), Princeton, NJ, under Contract No. F19628-88-C-0088. It describes work performed from 25 May, 1988 to 5 August, 1989, in the Optoelectronics Research Laboratory, Dr. M. Ettenberg, Director. The Project Supervisor was Dr. G. W. Hughes, Head of Optoelectronic Systems, and the Project Scientist was Dr. F. V. Shallcross. The focal plane array was designed by Dr. W. F. Kosonocky; the chip encoding was done by G. M. Meray. The devices were processed by R. Miller, H. W. James, W. S. Romito and F. J. Tams, III. The array testing was performed by T. S. Villani and J. J. O'Neill, III. The Air Force Technical Monitor was M. Weeks.

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Publication does not constitute Air Force approval of the findings or conclusions of this report. It is intended only for the exchange and stimulation of ideas.

Section I

INTRODUCTION

Metal-silicide photodiode array technology was invented at Rome Air Development Center (RADC), Hanscom AFB, MA, and has been under development there since the early 1970's. In 1973, Shepherd and Yang proposed silicide Schottky-barrier detector (SBD) arrays for infrared thermal imaging [1]. Since then, considerable progress has been made at the David Sarnoff Research Center (Sarnoff), with the support of RADC, Hanscom AFB, on the development of PtSi SBD image-sensor arrays for thermal imaging applications in the MWIR (3 to 5 μm) band and of Pd_2Si SBD image-sensor arrays for applications in the SWIR (1 to 3 μm) band [2-10].

IR-CCD focal plane arrays (FPA's) with 64 x 128 and 160 x 244 elements were designed and fabricated at Sarnoff under contract with RADC, Hanscom AFB, from July 1981 to September 1984 [11-13]. Both of these IR-CCD FPA's had the same basic design in the form of an interline transfer IR-CCD imager with 2:1 vertical interlacing.

Under a contract with RADC, Hanscom AFB, from September 1985 to September 1987, Sarnoff developed a higher (60%) fill-factor version of the the 160 x 244-element IR-CCD FPA (TA13401A), together with a 43%-fill-factor 320 x 244 IR-CCD FPA (TA13401B) [14-16]. These PtSi FPA's were designed to have the same chip size and to be essentially pin-for-pin compatible with the previously developed 160 x 244-element IR-CCD FPA (TA11524) [12,13].

The objectives of the work described in the present report were to design and fabricate an improved version of the 320 x 244-element PtSi array using beneficial design and process changes inferred from test results on the TA13401B device. This report describes the design, fabrication, and performance of this array (TA14804A).

Section II

DESIGN OF THE 320 X 244 IR-CCD FPA

A. FPA ARCHITECTURE

The overall architecture of the present 320 x 244-element IR-CCD FPA is the same as that of the earlier 320 x 244-element imager (TA13401B) [14-16], and the arrays are designed to be pin-for-pin compatible. The size of the array chips for both FPA's are the same, 584 mil x 464 mil, and the photosensitive area of both imagers has a standard TV aspect ratio of 4(H):3(V), with 40-μm x 40-μm pixels. The 320 x 244 FPA is an interline-transfer IR-CCD imager designed for operation with a readout of two vertically interlaced fields per frame. This design allows an area-efficient pixel construction, with two-level polysilicon gates, by using four-phase (double-clocked) operation of the IR-CCD area sensor. Figure 1 shows a schematic layout of the 320 x 244 IR-CCD FPA.

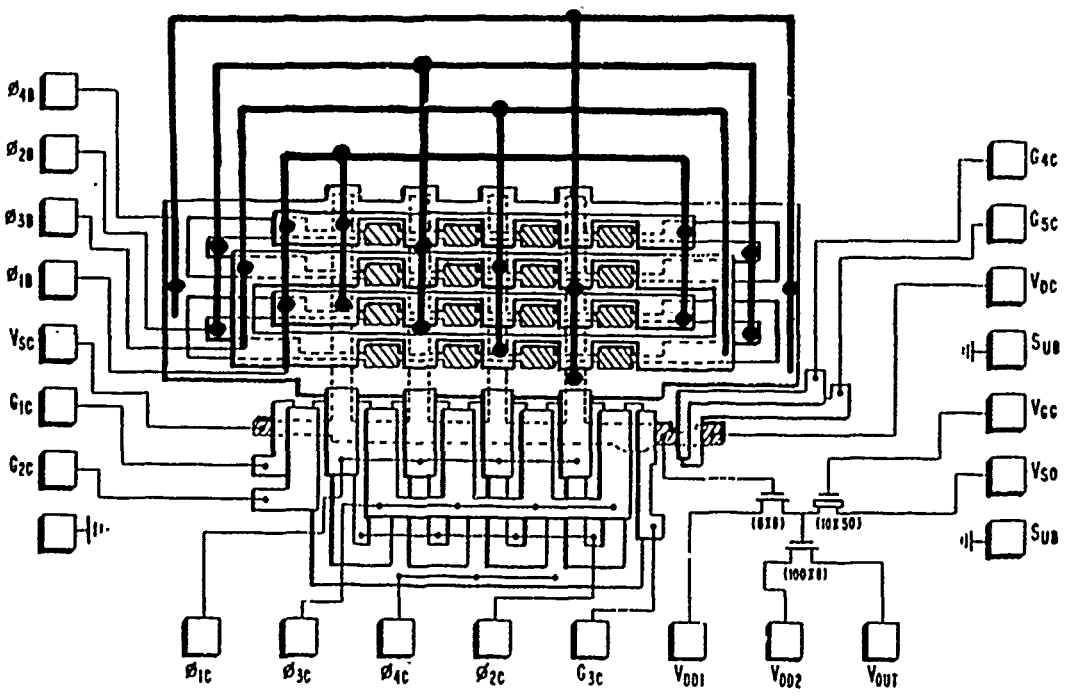

Figure 1. Schematic layout of the 320 x 244 IR-CCD FPA.

B. EVALUATION OF DESIGN AND PROCESS ALTERNATIVES

The earlier 320 x 244-element IR-CCD imager (TA13401B) [14-16] was fabricated using a Perkin-Elmer Model 240 1:1 scanning projection aligner. In order to achieve 40-μm x 40-μm pixels with a fill factor of 43% and a charge-handling capacity of at least 10^6 electrons/pixel using design rules of 2.5 μm and alignment tolerances of ±1.0 μm, the process for this earlier array incorporated several self-alignment features in definition of the buried-channel regions and the Schottky-barrier detector areas. The self-alignment technique required the use of a compensating p-type channel-stop implant at the edges of the buried-channel regions, as well as a heavily arsenic-doped guard ring around the detectors. These devices exhibited dark-current spots that increased with SBD operating voltage above 2 to 3 V. This break-down phenomenon appeared to be associated with the abrupt arsenic diffusion profiles and may also have involved the presence of the relatively heavily doped p-type channel-stop regions.

Subsequent to fabrication of the TA13401B devices, we designed and fabricated the 256 x 256-element TA13866 FPA, partially funded under Air Force Contract No. F29601-86-0247. This device was fabricated using an Optimetrix Model 8605H 5:1 stepper, with alignment tolerances of ±0.5 μm or better, and a theoretical resolution of 1.1 μm. The process sequence generally resembled that for the TA13401B array, although the improved lithographic capabilities eliminated the need for self-alignment of the buried-channel and SBD regions. As a result, the devices were made with a lighter boron channel-stop implantation and a relatively low-concentration phosphorus guard-ring implantation. Test results on these 256 x 256-element devices confirmed that their design and process were satisfactory, and that the problem with dark-current spots occurring with the TA13401B devices had been eliminated.

As a result of tests on the TA13866 and TA13401B devices, it was determined that the fabrication sequence for the new 320 x 244 FPA would follow that used for the 256 x 256 FPA, with the photolithography to be done on the Optimetrix 5:1 stepper. The general chip design would follow that for the TA13401B array, with suitable correction for the use of the TA13866 process.

C. CHIP CONFIGURATION

Figure 2 shows a check plot of the entire FPA die. Note that details of the imaging area and C register are omitted for clarity. There are no test devices on

the actual FPA chip. Test devices required for process control and FPA performance evaluation are placed on a separate strip at the top of the FPA; this strip is sawn off from the array before packaging. The total die size, including the test area, is 584.0 mil by 503.9 mil.

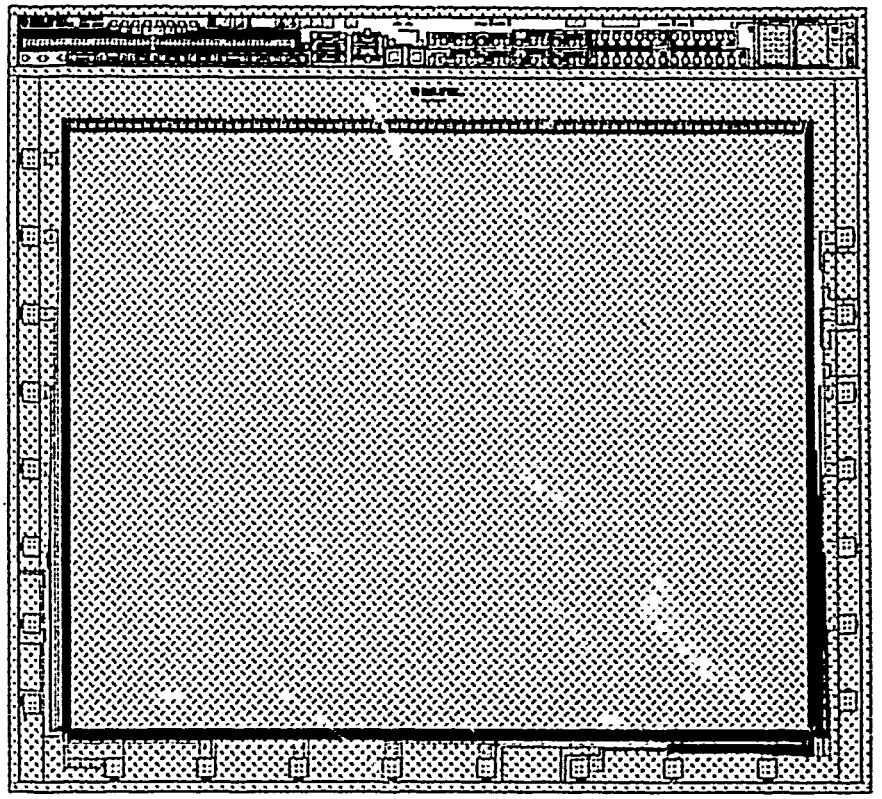

Figure 2. Check plot of TA14804A FPA die.

D. PIXEL DESIGN

Figure 3 illustrates the pixel layout of the IRCCD FPA. The cross-sectional view of the pixel construction is illustrated in Fig. 4. In this construction, the SBD's are contained on all four sides by one or two levels of polysilicon gates. To minimize dark-current spikes, the PtSi SBD's are surrounded by n-type guard rings with a minimum width of 2.0 μm, which are made with the same implantation as that used for the CCD buried channels. The channel stops, between two adjacent SBD's in the vertical direction and the SBD's and buried-channel CCD (BCCD) readout registers in the horizontal direction, are in the form of p-type implanted regions with a minimum width of 2.0 μm and a 5-μm-

long by 6-μm-wide surface channel CCD transfer region between the SBD and the BCCD readout register.

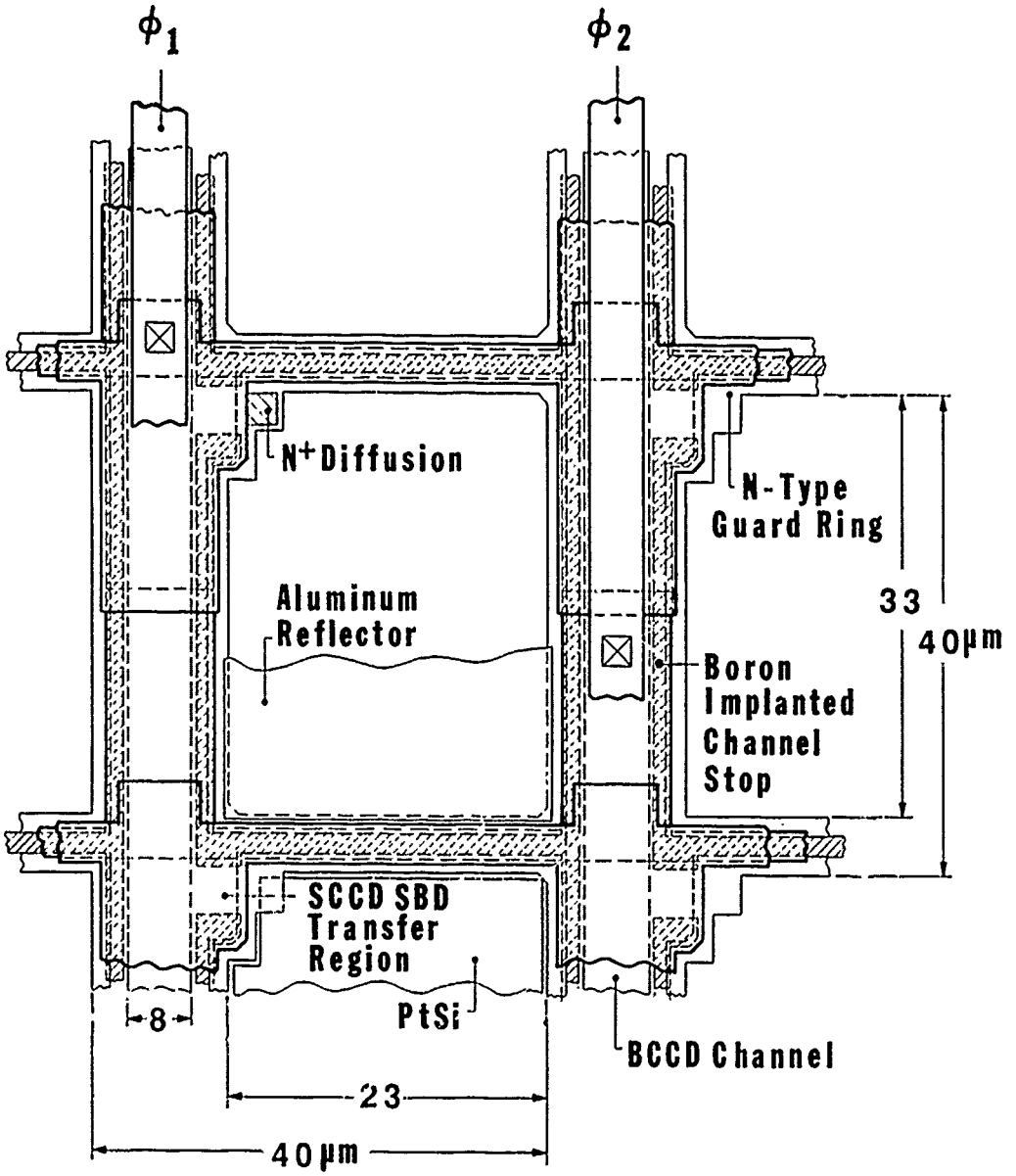

Figure 3. Pixel layout of TA14804A 320 x 244 FPA.

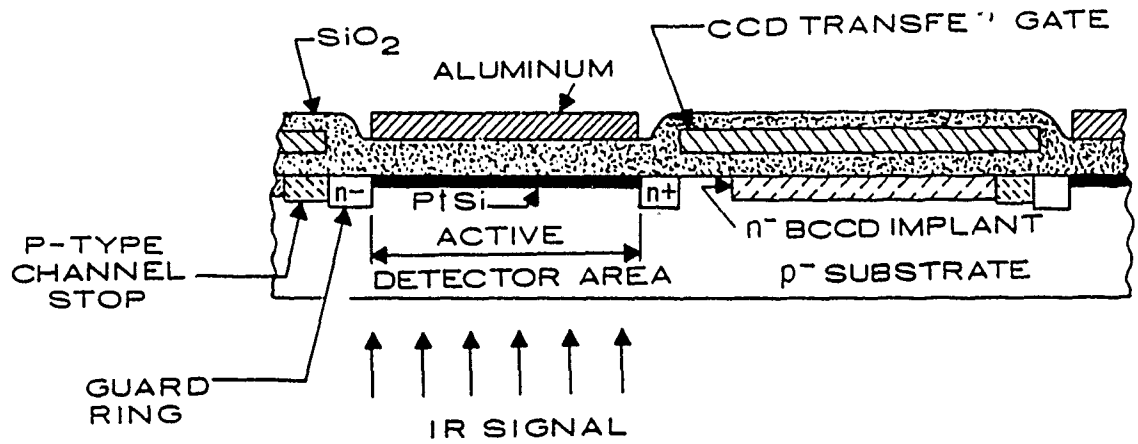

Figure 4. Cross-sectional view of 320 x 244 pixel.

The operation of the SCCD channel-stop regions into accumulation ensures an operational blooming control mode of the SBD's, provided the BCCD readout register has a sufficient charge-handling capacity [13].

A check plot of the pixel is given in Fig. 5, showing additional details of the construction. This design gives a nominal fill factor of 44% based on the area enclosed by the guard ring. Figure 6 shows a photomicrograph of several pixels of the TA14804A FPA. Figure 7 is an SEM micrograph of one pixel.

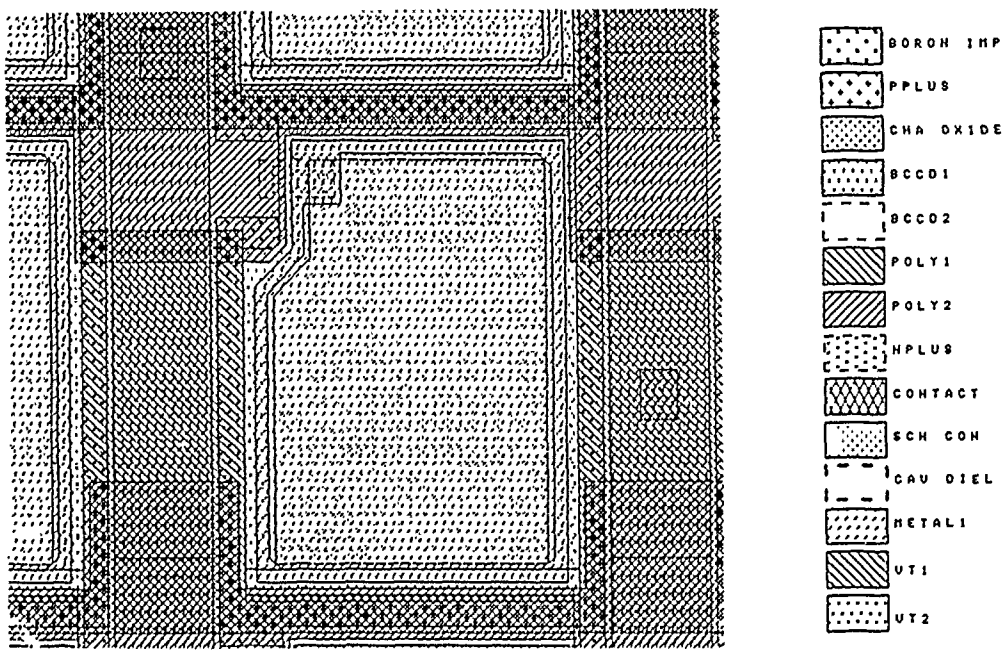

Figure 5. Check plot of TA14804A pixel.

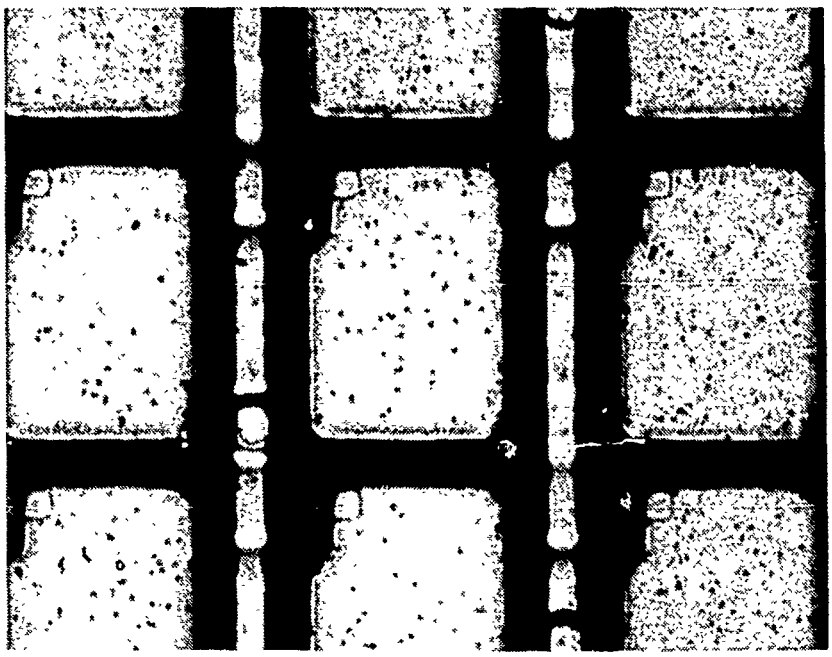

Figure 6. Photomicrograph of TA14804A pixels.

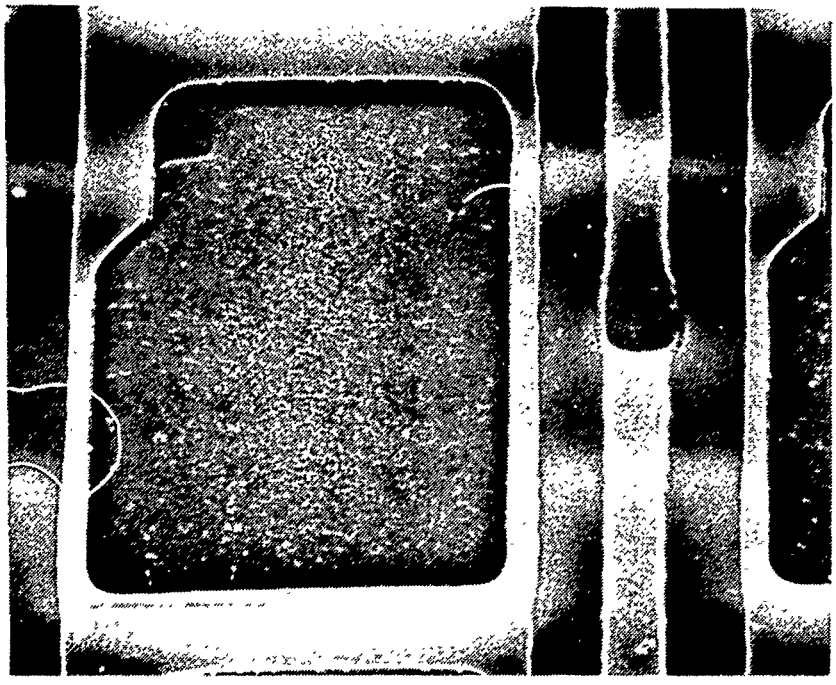

Figure 7. SEM micrograph of TA14804A pixel (at 30°).

E. SATURATION SIGNAL

In an attempt to increase the charge-handling capacity of the new 320 x 244 FPA, the nominal width of the BCCD channel of the B register was increased to 8 μm from the nominal 7 μm used with the earlier TA13401B 320 x 244 FPA, which had a B register saturation signal of 1.4×10^6 electrons per pixel.

Previous measurements of the 160 x 244-element imager (TA13401A) with a 10-μm-wide BCCD channel in the B register showed a saturation signal of 2.6×10^6 electrons/pixel. Therefore, it was concluded that the saturation signal of these BCCD registers corresponded to about 11,000 electrons/μm^2, if the effective width of the BCCD channel of these B registers were reduced by about 1.7 μm on each side. Thus, the effective width of the BCCD channel of the TA13401B array was apparently only about 4 μm. Increasing the nominal channel width from 7 μm to 8 μm was expected to result in increasing the saturation signal of the B register from 1.4×10^6 electrons/pixel to about 1.8×10^6 electrons/pixel.

F. ARCHITECTURE OF B AND C REGISTERS

The serial C register for this FPA was designed for four-phase operation with 10-μm-long gates. This serial output register has a BCCD-1 channel with a width of 16 μm, which also includes a deeper BCCD-2 channel (trench) of 4 μm, as shown in Fig. 8. These channel widths were increased from 12 μm and 3 μm respectively used in the previous 320 x 244 device, with the intent of increasing the charge-handling capacity of the C register, in accordance with the B-register change described above.

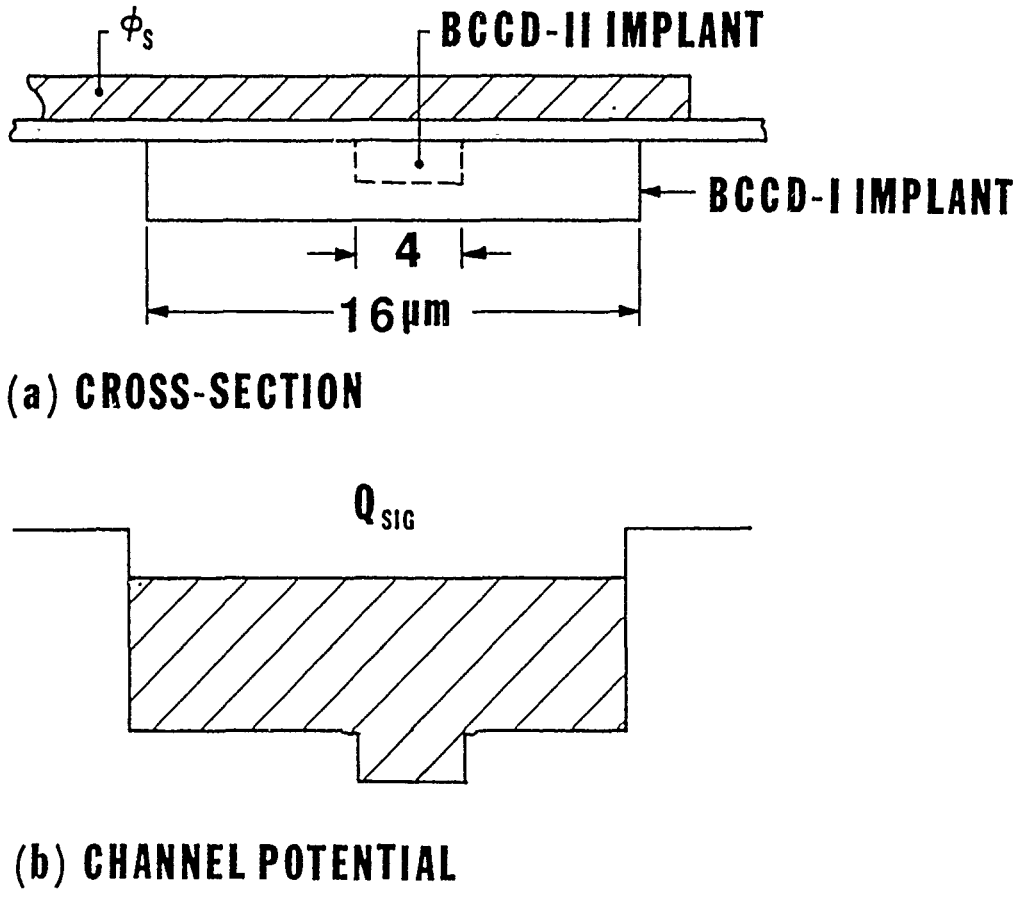

Figure 8. Cross-section of the serial output register.

Figures 9 and 10 are check plots of the upper left and upper right corners of the FPA, showing the bus connections to the B register. This design is essentially the same as that for the earlier 320 x 244-element chip, with minor changes in bus widths. Figures 11 and 12 are check plots for the lower left and lower right corners of the FPA. These plots show details of the input and output sections of the C register, the bus connections for both B and C registers, and details of the output amplifier. The design closely resembles that for the earlier 320 x 244-element FPA, with the exception of the BCCD widths, as described above.

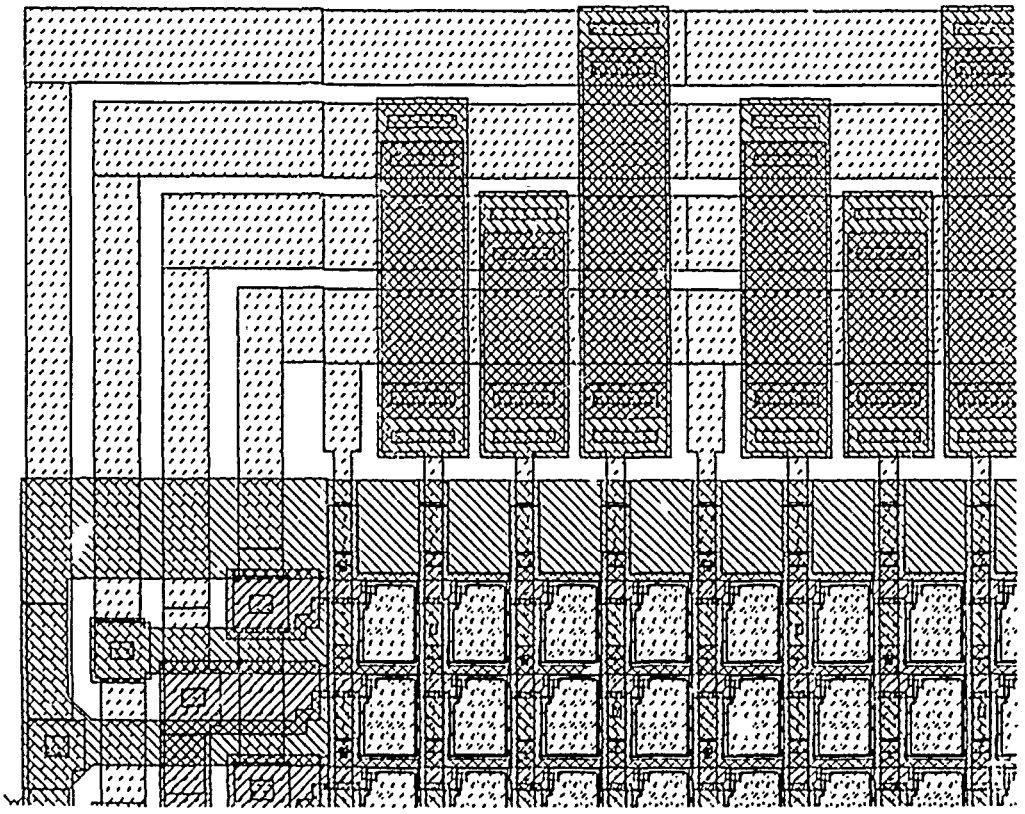

Figure 9. Check plot of upper left corner of TA14804A FPA.

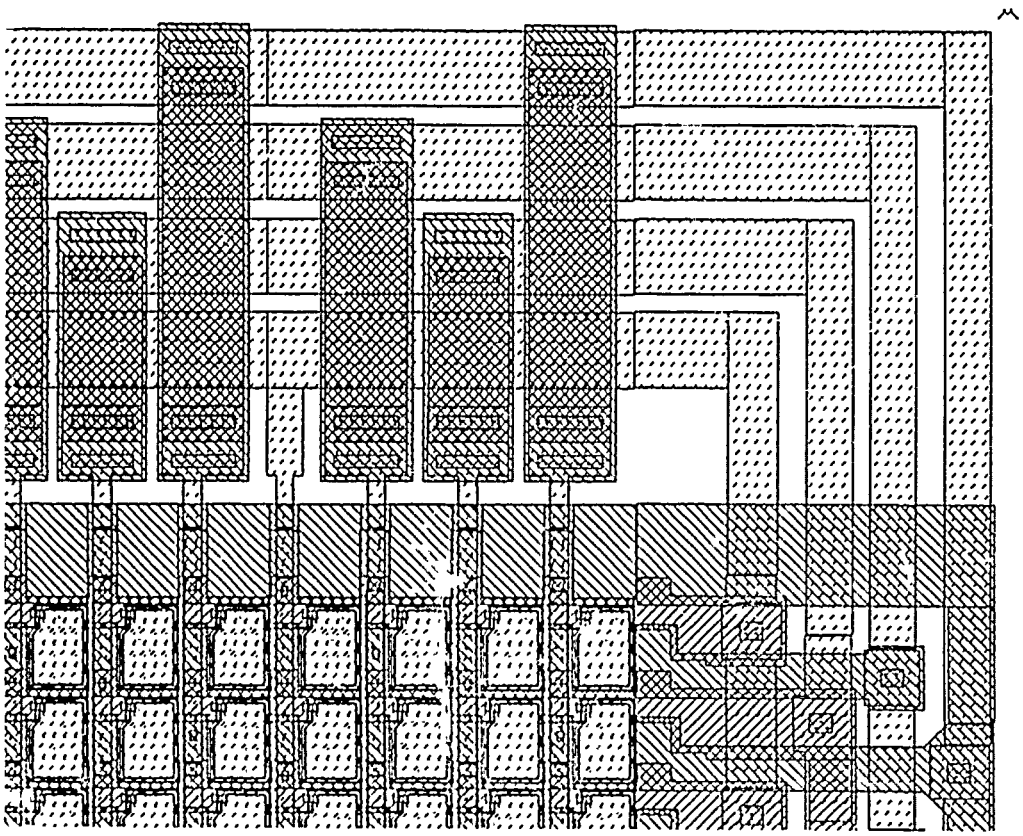

Figure 10. Check plot of upper right corner of TA14804A FPA.

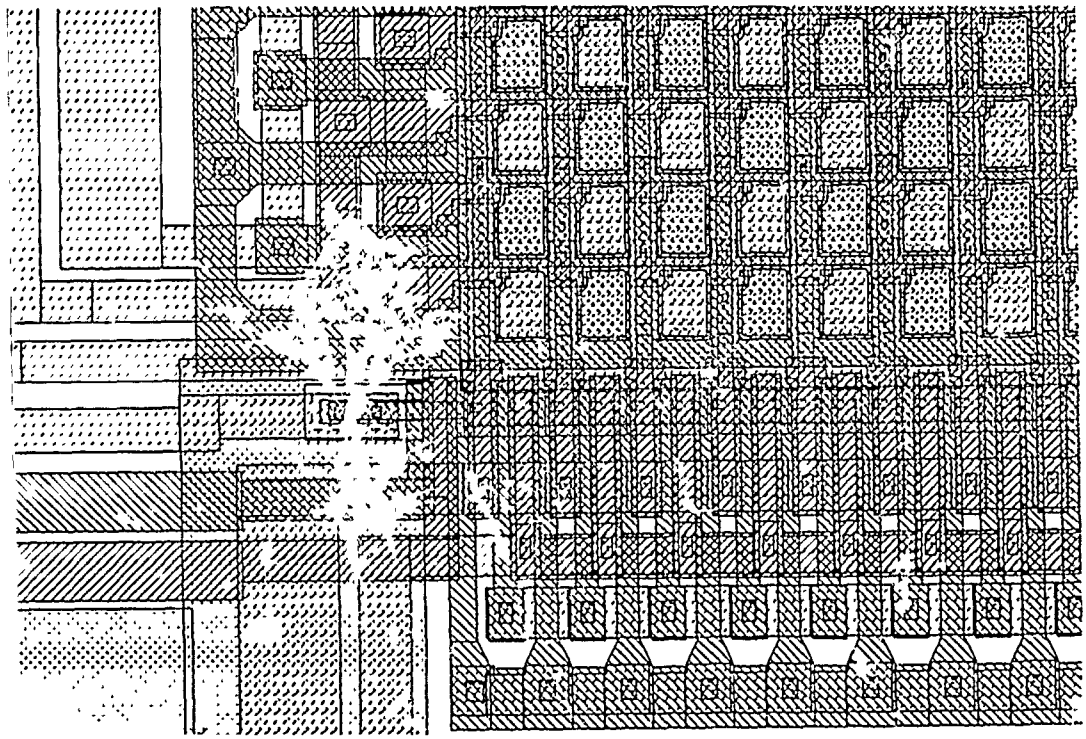

Figure 11. Check plot of lower left corner of TA14804A FPA, showing input to C register.

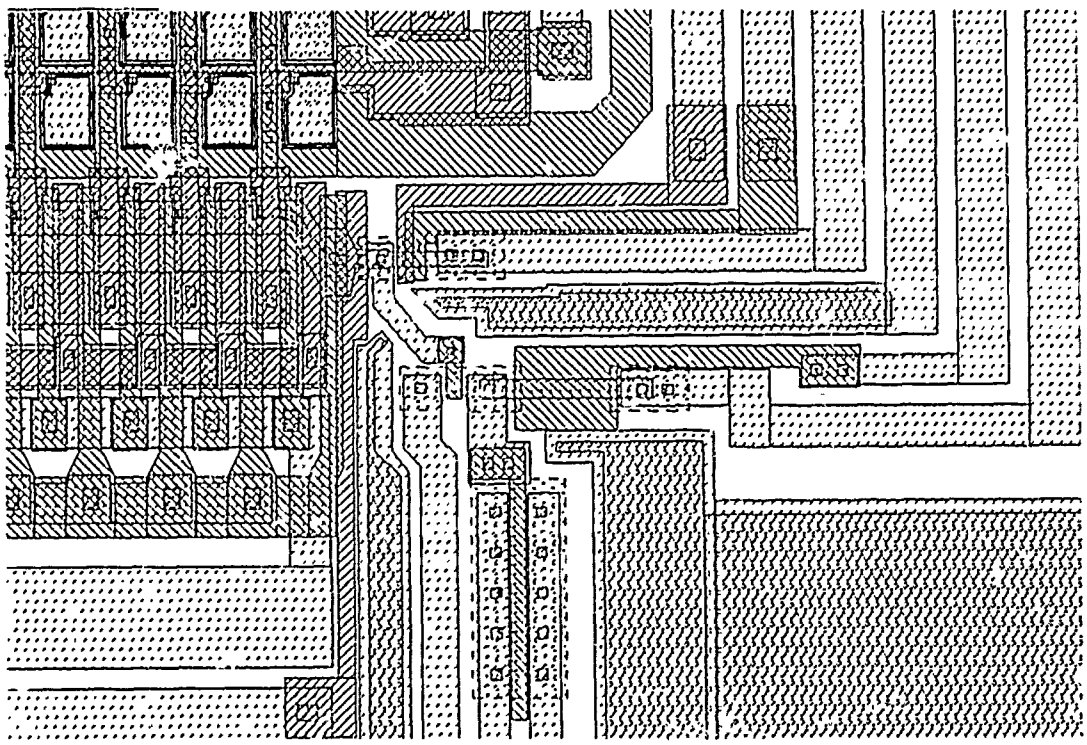

Figure 12. Check plot of lower right corner of TA14804A FPA, showing C-register output and output amplifier.

G. OUTPUT AMPLIFIER

The floating-diffusion capacitance of the two-stage output amplifier of the TA13401B array was measured to be 0.045 pF as compared with the estimated value of 0.04 pF. The transconduction gain of this output stage was measured to be 350 electrons/mV, or 2.8 μV/electron. With the available design rules it would have been possible to decrease the capacitance of the floating diffusion node to about 0.02 pF. However, as result of our experience with a limited linear operating range for the output amplifier of the 256 x 256-element device (TA13866) (with $C_{FD} \approx 0.02$ pF), it was decided to keep the output amplifier of the 320 x 244-element device without change.

Figure 13 shows an SEM micrograph of the TA14804A FPA output amplifier region.

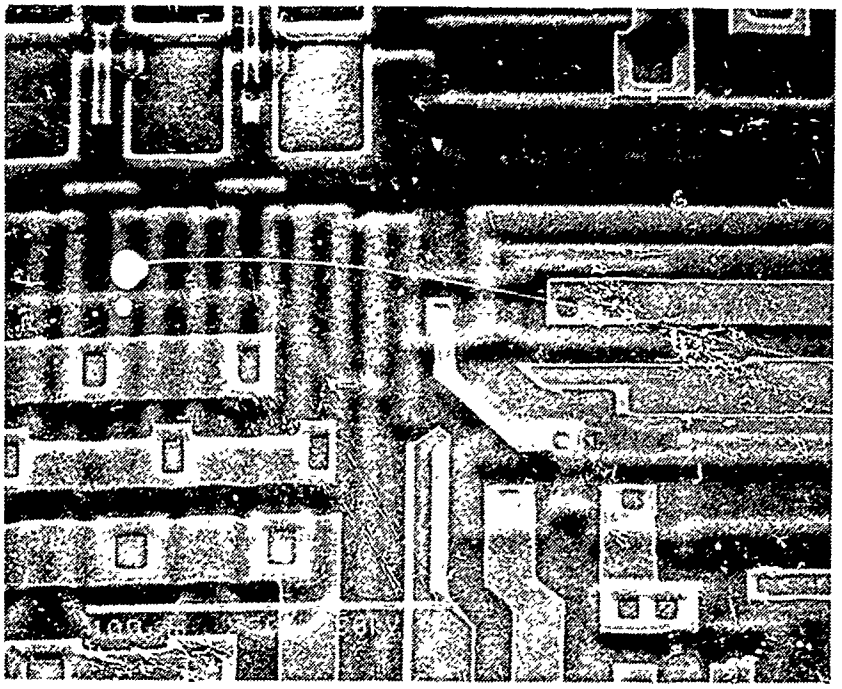

Figure 13. SEM micrograph of TA14804A FPA output amplifier region.

H. TEST DEVICES

Test devices for the TA14804A 320 x 244-element FPA are on a separate strip, which can be sawn off from the array. This test strip is shown at the top of

Fig. 2. These test devices consist of structures for use in photolithography, for standard silicon fabrication control, and for evaluation of FPA performance.

The photolithographic controls include die-by-die alignment keys for use with the 5:1 stepper, alignment verniers and critical dimension cells. Silicon process controls include test resistors for polysilicon and diffusions, and a structure to test for intra-level polysilicon shorts. There are test transistors with first- and second-level polysilicon gates with both buried and surface channels, in addition to a dual-gate buried-channel device. There are test capacitors using both levels of polysilicon.

For evaluating FPA performance, there are standard test Schottky diodes and silicide resistors. The test chip also contains a temperature sensing diode. In addition, there is a series of devices designed to evaluate the effect of variations in structure of the transfer region between the SBD's and the B register. These test structures allow use of the added threshold-adjust implantations with various widths. A further set of structures is designed to test the effects of various widths of channel stop between the vertical channel and the SBD guard ring.

I. OPTIONAL THRESHOLD ADJUSTMENT

In the TA13401B devices, the charge is transferred from the SBD's to the vertical register through a surface-channel CCD transfer region. It was suggested that we increase the threshold (barrier height) of the surface-channel transfer region, to permit operation of the B-register at higher voltages. In response to this suggestion, two optional masks, V_{T-1} and V_{T-2}, were designed to permit tests of added implants in the transfer region on some wafers. The nominal channel length of the added barrier region was varied between the two masks; the length of the implanted region was designed to be 3.0 μm for mask V_{T-1} and 2.0 μm for mask V_{T-2}.

To estimate the required amount of threshold adjustment implantation, process and device simulations were run using SUPREM-3 [17] and MINIMOS [18] programs. Calculated threshold voltages for the poly-2 transfer gate region (from SUPREM-3 [17]) are shown in Table 1, as a function of implantation dosage, for a boron implantation energy of 40 keV. (Note that this calculation ignores any short-channel effects).

Table 1

Calculated Threshold Voltage for Poly-2 Transfer Gate

Implant Dose	Threshold Voltage
0	0.065 V
3 E 11 cm^{-2}	0.789 V
6 E 11 cm^{-2}	1.316 V

To show the expected effect of a change in length of the implanted region, MINIMOS [18] was used to calculate the difference between a 3.0-μm-long implanted strip (as in mask V_{T-1}) and a 2.0-μm-long strip (as in mask V_{T-2}). Figure 14 shows the calculated drain-current vs gate-voltage function for no implant (curve A), and for a 3 E 11 cm^{-2} boron implant with 2.0-μm (curve B) and 3.0-μm (curve C) implant lengths.

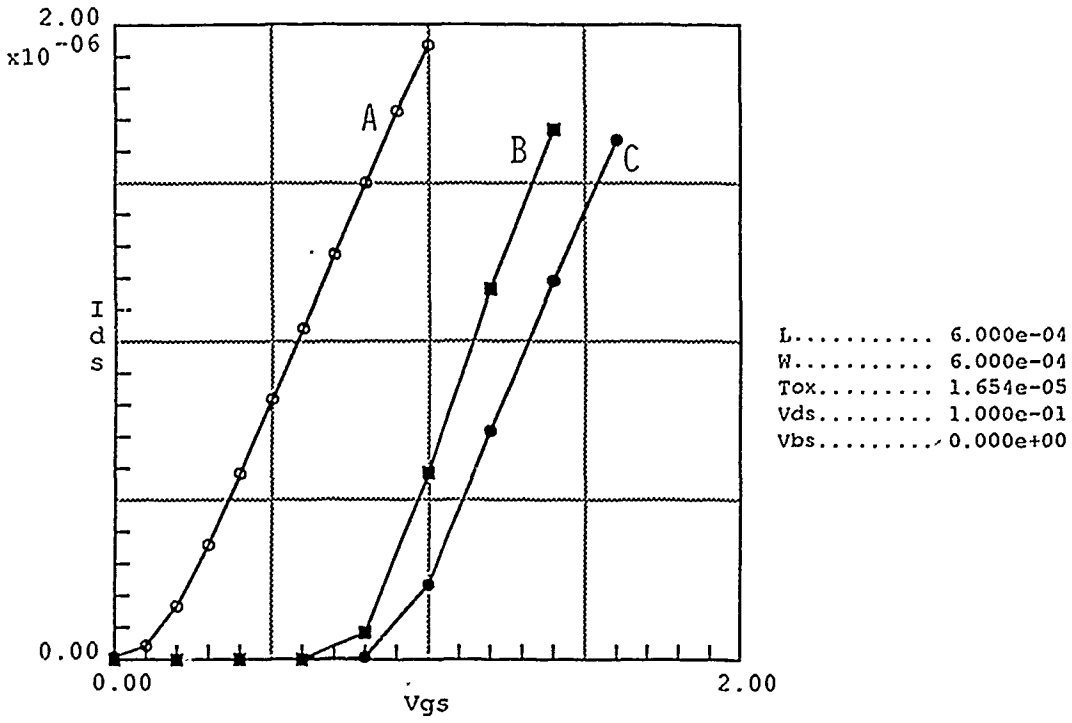

Figure 14. Calculated transfer functiuon for transfer-gate region of TA14804A.
Curve A: no V_T implant.
Curve B: 2-μm implant length.
Curve C: 3-μm implant length.

Section III

FABRICATION OF THE 320 X 244 IR-CCD FPA

A. PHOTOMASKS

To generate photomasks, the chip design was digitized using the ChipGraph™ program on the Mentor Graphics® system. Error checking was performed using the Cadence DRACULA II™ program on Mentor Graphics®. The fabrication process requires the use of 5X reticles as photomasks. Appropriate global and die-by-die alignment keys were added to the masks, which were generated by the mask vender in conformity with specifications.

Table 2 lists the photomasks according to the process sequence, together with the alignment reference for each level.

Table 2

320 x 244 Photomasks by Process Sequence

Level Number	Level Name	Reference Level
02	Boron Implant	---
18*	V_{T-1}	Boron Implant
19*	V_{T-2}	Boron Implant
03	P^+ Diffusion	Boron Implant
04	Field Oxide	Boron Implant
05	Buried Channel-1	Boron Implant
06	Buried Channel-2	Boron Implant
07	Polysilicon-1	Boron Implant
08	Polysilicon-2	Polysilicon-1
09	N^+ Diffusion	Polysilicon-1
10	Contacts	Polysilicon-1
11	Schottky Contact	Polysilicon-1
13*	Schottky Contact -2	Polysilicon-1
12	Dielectric	Polysilicon-1
17*	Dielectric-2	Polysilicon-1
14	Metal	Contacts

* Optional levels

The mask levels 18 and 19 are used for the optional threshold adjustment implantation, as described above.

Based on microscope measurements of devices from Lot 1, it was determined that the original width of the Schottky contact opening on the Schottky contact photomask was larger than optimum, causing some risk that the detectors could contact the channel-stop regions around the detectors or one of the polysilicon busses. It was further determined that the cavity dielectric width was smaller than optimum, causing some risk of reflector shorts. As a result, two additional photomasks were generated (Level 13, Schottky Contact-2, and Level 17, Dielectric-2). The revised Schottky contact is 0.5 μm undersize per side compared with the original mask, while the revised dielectric stripe is 1.0 μm wider on each side.

B. DEVICE WAFERS

To minimize swirl-related nonuniformities in device dark current and responsivity, the devices were fabricated on magnetic Czochralski (MCZ) substrates. To eliminate back-surface optical scattering, the processing was done on wafers polished on both sides. In practice, it was found that the fabrication procedures caused some scratching of the wafer backs, and in many cases it was desirable to give a light polish to the back surface of the completed devices again, either in wafer or chip form, prior to the final anti-reflection-layer deposition.

Figure 15 is a wafer map for the TA14804A 320 x 244-element FPA's, showing the placement of die on a 100 mm wafer. Note that there are 26 chips per wafer with this layout.

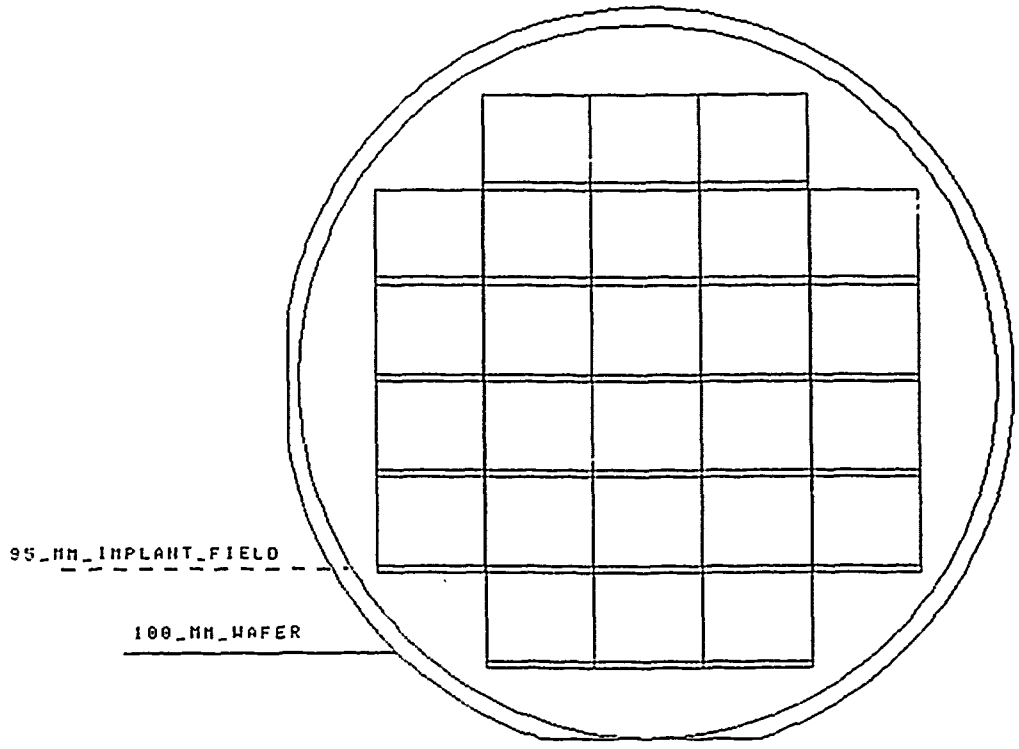

Figure 15. Wafer map for the TA14804A 320 x 244-element FPA's.

C. FABRICATION PROCESS

The device fabrication uses a double-polysilicon NMOS CCD process, carried out in the sequence indicated by Table 2. As shown in Fig. 16a, there is an initial thick field oxide (7000 Å), which is first used in definition of the p-type channel-stop barriers around the detectors. Together with a photoresist mask, the field oxide also serves as a mask against the heavier p+ boron implantation (Fig. 16b). The field oxide is subsequently patterned to provide field oxide in the perimeter of the device, while removing thick oxide from the channel and detector regions (Fig. 16c). The buried channel (and guard ring) implantation is defined by a photoresist mask placed over a thin (250 Å) thermal oxide (Fig 16d). For all wafers in Lots 1 and 2, the BCCD-1 implant dose was 1.3×10^{12} cm^{-2} phosphorus, and the BCCD-2 implant dose was 5×10^{11} cm^{-2} arsenic.

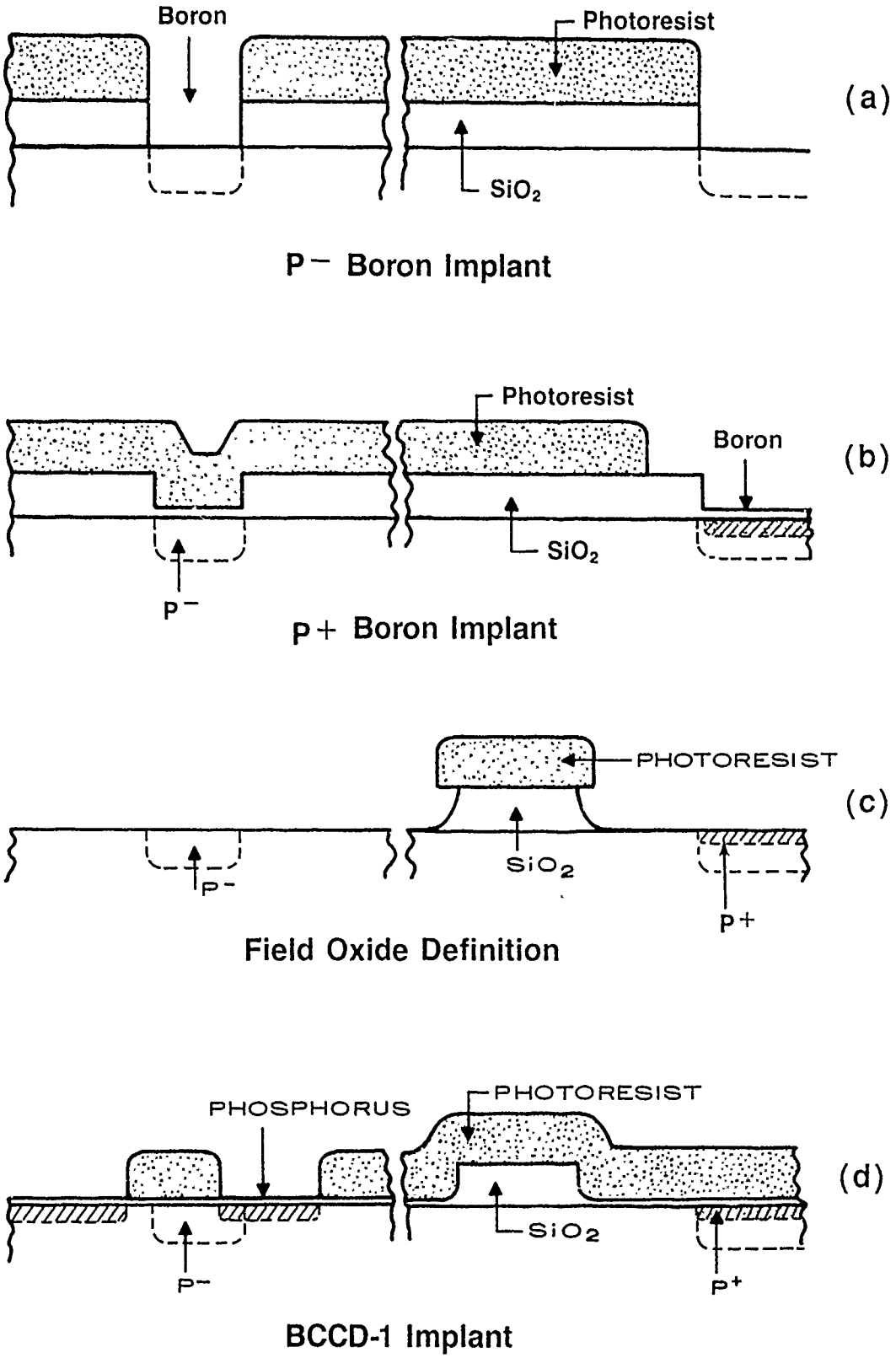

Figure 16. Fabrication process for TA14804A FPA (through BCCD implantation).

The optional threshold adjustment implantation is defined by etching into the thick oxide after the first p-type channel-stop implantation (and removing the photoresist), so that the additional implant appears in both channel-stop and threshold-adjust regions.

Polysilicon patterning is followed by the usual n+ source-drain definition, contact and SBD etching, and cavity-dielectric and metal definition.

The selection of implantation conditions for the p-type boron-doped channel stops surrounding the SBD's was based on test results for the 256 x 256-element TA13866 device (partially fabricated under Air Force Contract No. F29601-86-0247). In order to ensure a sufficient barrier and to avoid sub-threshold leakage in the lightly doped substrate, a relatively deep implant was employed. (Previous simulations have shown the adequacy of this approach). Figure 17 shows the results from an earlier SUPREM-3 [17] simulation of the implant profiles for several possible channel-stop implants, after completion of the process. To ensure an adequate barrier and to minimize possible breakdown problems from over-doping, the implantation conditions were varied among the wafers for both wafer lots, as indicated below.

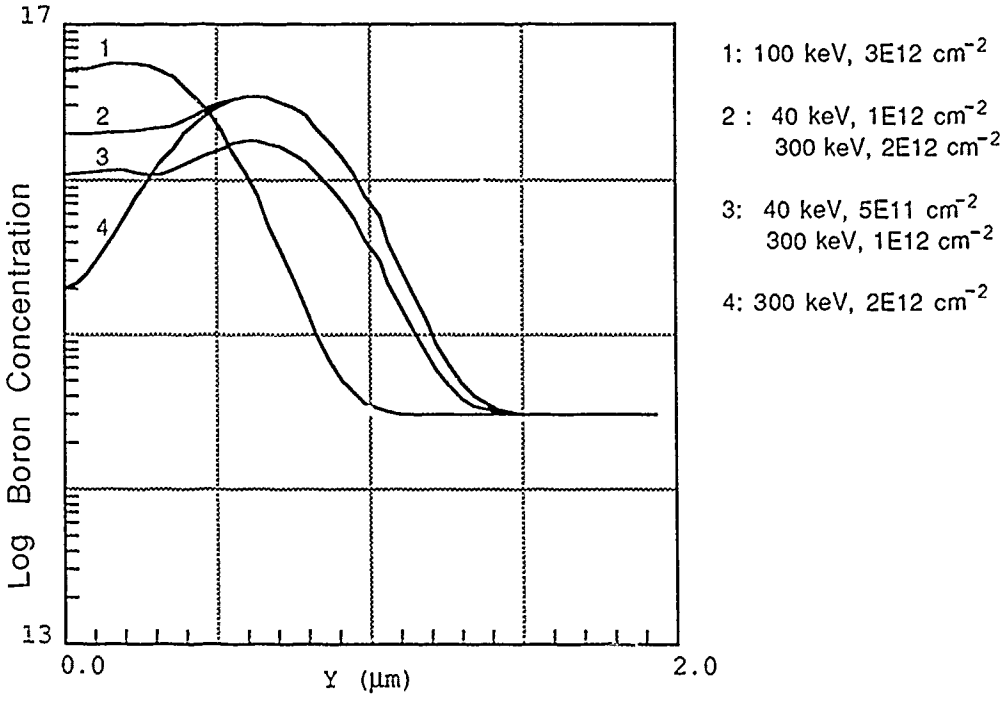

Figure 17. Simulated boron profiles for channel stops.

D. SCHOTTKY-BARRIER-DETECTOR FORMATION

The technique for formation of the SBD's has been described previously [13]. For the TA14804A 320 x 244-element FPA's, a thin (approximately 14-Å) layer of platinum was deposited on the wafers and annealed to form a layer of PtSi in the SBD regions. The unreacted platinum was removed by dip-etching in hot aqua regia. The structure was completed by depositing an approximately 7500-Å layer of SiO_2 and an aluminum reflector. The back of the devices were coated with an antireflection layer of approximately 5300 Å of SiO.

E. WAFER LOTS

Twenty wafers were completed from Lot 1, and 22 wafers were completed from Lot 2. As indicated above, the boron channel-stop implant was varied between the various wafers. Six wafers from Lot 2 were given the optional threshold-adjust implantation. Table 3 lists the channel-stop and threshold-adjust implantations used for each of the wafers. Note that M18 has a nominal barrier length of 3.0 μm, and M19 has a nominal length of 2.0 μm. (The measured length of these regions in the oxide implantation mask on the wafers was 3.6 μm and 2.7 μm respectively, reflecting a dimensional change on oxide etching).

Table 3

TA14804A Implantation Variables

Wafer	Channel Stop Implant (B)	V_T Implant (B)
1A	1 E 12 @ 40 keV + 2 E 12 @ 300 keV	None
1B	1 E 12 @ 40 keV + 2 E 12 @ 300 keV	None
1C	1 E 12 @ 40 keV + 2 E 12 @ 300 keV	None
1D	1 E 12 @ 40 keV + 2 E 12 @ 300 keV	None
1E	1 E 12 @ 40 keV + 2 E 12 @ 300 keV	None
1F	1 E 12 @ 40 keV + 2 E 12 @ 300 keV	None
1G	1 E 12 @ 40 keV + 2 E 12 @ 300 keV	None
1H	1 E 12 @ 40 keV + 2 E 12 @ 300 keV	None
1I	1 E 12 @ 40 keV + 1 E 12 @ 300 keV	None
1J	1 E 12 @ 40 keV + 1 E 12 @ 300 keV	None
1K	1 E 12 @ 40 keV + 1 E 12 @ 300 keV	None
1L	1 E 12 @ 40 keV + 1 E 12 @ 300 keV	None
1M	1 E 12 @ 40 keV + 1 E 12 @ 300 keV	None
1N	1 E 12 @ 40 keV + 1 E 12 @ 300 keV	None
1O	1 E 12 @ 40 keV + 1 E 12 @ 300 keV	None
1Q	5 E 11 @ 40 keV + 1 E 12 @ 300 keV	None
1R	5 E 11 @ 40 keV + 1 E 12 @ 300 keV	None
1T	5 E 11 @ 40 keV + 1 E 12 @ 300 keV	None
1W	5 E 11 @ 40 keV + 1 E 12 @ 300 keV	None
1X	5 E 11 @ 40 keV + 1 E 12 @ 300 keV	None
2A	5 E 11 @ 40 keV + 1 E 12 @ 300 keV	M18: 3 E 11 @ 40 keV
2B	5 E 11 @ 40 keV + 1 E 12 @ 300 keV	M18: 5 E 11 @ 40 keV
2C	5 E 11 @ 40 keV + 1 E 12 @ 300 keV	M18: 8 E 11 @ 40 keV
2D	5 E 11 @ 40 keV + 1 E 12 @ 300 keV	M19: 3 E 11 @ 40 keV
2E	5 E 11 @ 40 keV + 1 E 12 @ 300 keV	M19: 5 E 11 @ 40 keV
2F	5 E 11 @ 40 keV + 1 E 12 @ 300 keV	M19: 8 E 11 @ 40 keV
2G	5 E 11 @ 40 keV + 1 E 12 @ 300 keV	None
2H	5 E 11 @ 40 keV + 1 E 12 @ 300 keV	None
2I	5 E 11 @ 40 keV + 1 E 12 @ 300 keV	None
2J	5 E 11 @ 40 keV + 1 E 12 @ 300 keV	None
2K	5 E 11 @ 40 keV + 1 E 12 @ 300 keV	None
2L	5 E 11 @ 40 keV + 1 E 12 @ 300 keV	None
2M	1 E 12 @ 40 keV + 1 E 12 @ 300 keV	None
2N	1 E 12 @ 40 keV + 1 E 12 @ 300 keV	None
2O	1 E 12 @ 40 keV + 1 E 12 @ 300 keV	None
2P	1 E 12 @ 40 keV + 1 E 12 @ 300 keV	None
2Q	1 E 12 @ 40 keV + 1 E 12 @ 300 keV	None
2R	1 E 12 @ 40 keV + 1 E 12 @ 300 keV	None
2S	1 E 11 @ 40 keV + 2 E 12 @ 300 keV	None
2T	1 E 11 @ 40 keV + 2 E 12 @ 300 keV	None
2V	1 E 11 @ 40 keV + 2 E 12 @ 300 keV	None
2W	1 E 11 @ 40 keV + 2 E 12 @ 300 keV	None

F. CHIP PACKAGING

After the wafers were probe-tested, they were sawn into die. The 320 x 244-element FPA's were bonded in specially designed 32-pin ceramic packages, which were designed for the introduction of the infrared signal through a 544-mil x 424-mil window. (The same packages were used for the earlier TA13401B 320 x 244-element arrays). Figure 18 illustrates the appearance of a 320 x 244-element imager bonded in a 32-pin ceramic package. (Note that the coarse grid pattern in the figure is an aliasing artifact in the photo-reproduction process, not a pattern on the chip itself).

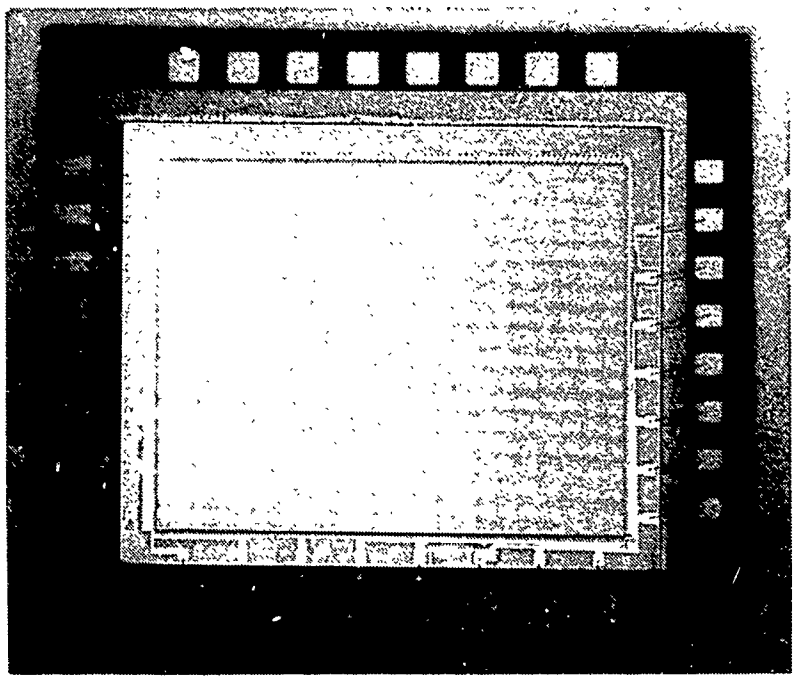

Figure 18. 320 x 244 IR-CCD imager bonded in 32-pin package.

Section IV

OPERATION AND PERFORMANCE

A. WAFER PROBE TESTING

1. Room-Temperature Probing

After fabrication of the wafers was completed, they were initially tested for shorts at room temperature, using the automatic computer-based wafer prober. This probe system uses a Teledyne-TAC-PR-53 prober with a HP9836S computer. The system lists each short location and resistance and draws a wafer map identifying the location of potentially good devices.

The dc probe yield for the 1092 devices tested was 47%. Twenty-three of the 42 wafers tested had dc yields of 50% or higher.

2. Cryogenic-Temperature Probing

Following the initial room-temperature screening, the completed device wafers were probed using the automated cryogenic wafer prober. This unit consists of a Teledyne-TAC-PR-100 wafer prober, which has been modified for operation at cryogenic temperatures. Movement in the X-Y plane is accomplished by a stepping-motor drive table, on which is mounted a hollow copper vacuum chuck, cooled with liquid nitrogen delivered through a set of flexible nickel bellows. To avoid condensation, the cold chuck and prober are enclosed in a sealed box purged with nitrogen.

The cryogenic wafer prober allowed the devices to be characterized for functionality, array defects, and detector uniformity. When connected to appropriate drive electronics and a TV monitor, photos of defect patterns could be obtained of the imagers before dicing.

The first 34 wafers completed were tested on the cold prober. For these wafers, the yield of devices that could be operated was 54%. (Note that some shorts observed on dc probing did not prevent operation). Device wafers with potentially acceptable characteristics were then selected for packaging and further testing.

B. PACKAGED-DEVICE TESTING

The performance of the 320 x 244-element PtSi IR-CCD imagers was evaluated with an IR-TV camera tester, designed to produce an RS-170-equivalent video output. The imagers bonded in the 32-pin ceramic packages were cooled to about 77K by a liquid nitrogen Dewar.

The 320 x 244-element imagers were operated with a standard TV monitor without a frame converter, with the video output corresponding to every second line of standard TV output. To accomplish this, the IR-TV camera was operated with thirty 320 x 244-element frames/s, with two vertically interlaced 320 x 122-element fields/frame and a horizontal clock frequency of 6.2 MHz. This operation produces a video output with a horizontal-line time of 63.5 μs and an imager output signal at every second horizontal line. The RS170 video format can be displayed on a standard TV monitor with a pseudo-interlace producing pairing of two adjacent video lines and two adjacent blank lines.

C. PERFORMANCE CHARACTERISTICS OF THE FPA'S

1. FPA Responsivity and Dark Current

Typically, responsivity was greater than 1 x 10^4 electrons/pixel/°C for f/2.0 optics and a 3.4-μm long-pass filter. For the above operation, the 295K background corresponded to a signal charge of 2.5 x 10^5 electrons/pixel.

Typical dark currents were less than 3 x 10^4 electrons/pixel. The problem of voltage-dependent dark-current spots observed in the previous TA13401B 320 x 244-element devices [14] was not seen for the present arrays, indicating that the fabrication changes incorporated in the new arrays were beneficial.

2. Saturation Signal

A typical saturation signal measured for the TA14804A 320 x 244-element FPA was 1.4 x 10^6 electrons/pixel, determined by direct measurement of C-register drain current. While this amount is comparable to or somewhat greater than that typically observed for the earlier TA13401B 320 x 244-element array, the difference is less than expected, based on the increase in nominal B-register BCCD channel width from 7 μm to 8 μm. Apparently, the effective BCCD channel dimensions were influenced by details of the channel-stop and BCCD implantation profiles, which differed between the two devices, due to the modified

fabrication procedures. In future work, it is planned to evaluate the effect of modifications in the channel-stop and buried channel implantations on the saturation signal.

3. Charge-Transfer Inefficiency of C Register

Charge-transfer inefficiency (loss) measured for operation of the C register of the TA14804A 320 x 244-element FPA was similar to that measured for the earlier TA13401B array. Typically, a charge transfer inefficiency of 1.0×10^{-4} per transfer was measured at 77K, with a background charge of 2.0×10^5 electrons/pixel, a signal charge of 3.5×10^5 electrons/pixel, and a clock frequency of 6.2 MHz.

4. Effect of Optional Threshold-Adjust Implant

As indicated above (Table 3), six wafers from Lot 2 were given an additional boron threshold adjustment implantation in the transfer region between the SBD and B register. Measurements were made of the threshold voltages for transfer on two of these devices, and compared to wafers without additional implantation. Table 4 summarizes the results. As expected, the threshold voltage increased with increasing dosage, although the observed change is somewhat greater than predicted (see Table 1 and Fig. 14).

Table 4

Measured Threshold Voltage for Transfer Region

Wafer	V_T Implant Dose	V_T
2V	None	1.5 V
2H	None	1.9 - 2.0 V
2D	3 E 11 cm^{-2}	3.0 V
2F	8 E 11 cm^{-2}	4.0 - 4.5 V

Determination of detailed effects on device operation (including saturation signal) of the additional implantation in the transfer region will to be done in future work.

Section V

CONCLUSIONS

An improved 320 x 244-element IR-CCD imager (TA14804A) was designed and fabricated, using minimum design rules of 2.0 μm and alignment tolerances of ±0.5 μm. The pixel size is 40 μm x 40 μm, and the nominal fill factor is 44%.

The dark-current spots observed with the earlier 320 x 244-element imager (TA13401B) were eliminated. This improvement is attributed to both design and process modifications incorporated in the new imager.

The change in the process also resulted in improved device yields. A cold-probe yield (identifying operable IR imagers) of 54% was obtained.

FPA responsivity of greater than 1×10^4 electrons/pixel/°C for f/2.0 optics, and C-register transfer inefficiency (loss) of 1.0×10^{-4} per transfer were demonstrated, comparable to those obtained with the earlier TA13401B 320 x 244-element device.

A saturation signal of 1.4×10^6 electrons/pixel was obtained. The expected increase in charge-handling capacity by about 30% was not realized with the new design, in spite of an increase in B-register BCCD width from 7 μm to 8 μm. This effect on charge-handling capacity was apparently the result of differences in the doping profiles at the edges of the BCCD channel as compared to those for the TA13401B process. Future work will examine the effect of modified doping profiles on saturation signal.

An added threshold adjustment implantation in the transfer region between the SBD and the B register on several wafers caused an increase in threshold voltage as expected. Effects of the threshold-adjust implants on FPA operation have yet to be studied.

Section VI

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