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Dose Rate and Total Dose Radiation Testing of the Texas Instruments TMS320C30 32-Bit Floating Point Digital Signal Processor

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The MITRE Corporation has performed in-flux radiation testing of the Texas Instruments TMS320C30 32-bit floating point digital signal processor in both total dose and dose rate radiation environments. This test effort has provided data relating to the applicability of the TMS320C30 in systems with total dose and/or dose rate survivability requirements. In order to accomplish these tests, The MITRE Corporation developed custom hardware and software for in-flux radiation testing. This paper summarizes the effort by providing an overview of the TMS320C30, MITRE's test methodology, test facilities, statistical analysis, and full coverage of the test results.

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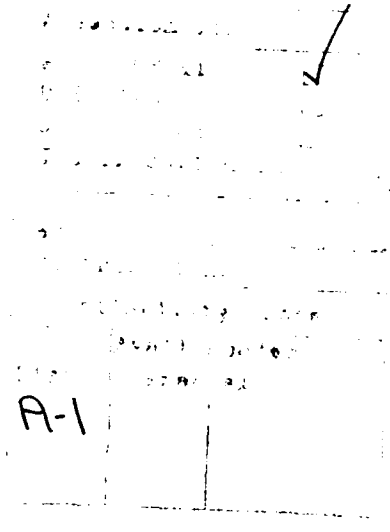

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SECTION 1

INTRODUCTION

This paper describes a test program initiated by The MITRE Corporation to characterize the Texas Instruments (TI) TMS320C30 32-bit floating point digital signal processor (DSP) in both dose rate and total dose radiation environments. This device is applicable to a wide range of signal processing needs including communications, radar, sonar, image processing, navigation, and missile guidance. The processor provides 32-bit floating point signal processing capabilities via a single-chip architecture. In addition, it is the only DSP device to offer a validated Ada compiler for high-level language development as required by many DOD programs. As such, this state-of-the-art device will be a key component in many systems including those with radiation survivability requirements.

The growth of digital signal processing has been fueled by the advent of single-chip DSPs capable of performing fast (single-cycle) multiply and accumulate operations, the staple of all signal processing algorithms. These application-specific microprocessors have evolved from 8- and 16-bit fixed point devices to the current 32-bit floating point capabilities. These capabilities naturally lend themselves to many communications programs as well as other interests including those with radiation hardening requirements. Recognizing the importance of this capability, The MITRE Corporation has characterized this device in the total dose and dose rate radiation environments. Texas Instruments provided 20 devices as well as sophisticated development tools used by MITRE staff to develop a TMS320C30 radiation test bed.

MITRE's test of the TMS320C30 resulted in failures between 4- and 5-K rads (Si) in the total dose environment with a statistical failure level (99-percent probability of survival with 90-percent confidence) of approximately 3-K rads (Si). In the prompt dose rate environment using a 20-30-nanosecond (ns) pulse, the device failed in the area of 1×10^8 rads (Si) per second with a 99/90 failure level of approximately 7×10^7 rads (Si) per second. For the delayed dose rate environment using a 1-microsecond (μs) pulse, the device failed in the area of 5×10^7 rads (Si) per second with a 99/90 failure level of approximately 3.2×10^7 rads (Si) per second. We observed latch-up in both environments at room temperature, at approximately 1×10^9 rads (Si) per second in the prompt environment and at approximately 1×10^8 rads (Si) per second in the delayed environment.

This paper will provide an overview of the TMS320C30 and its fabrication and will describe the test bed developed by MITRE. An overview of the tests and the formulation of applicable statistics will then be provided. Finally, we will provide the results of all tests and relevant discussion.

SECTION 2

OVERVIEW OF THE TMS320C30 DSP

The TMS320C30 is a complementary metal-oxide semiconductor (CMOS) integrated circuit with TTL-compatible inputs and outputs [1]. The DSP has a single-cycle instruction execution time of 60 ns. The processor, fabricated in 1.0-micron (μm) technology, consists of approxi- mately 700,000 transistors. The version supplied is housed in a 180-pin ceramic pin grid array (PGA) package. Relevant to radiation characterization, the TMS320C30 is a *dynamic* device -- it relies on inherent internal capacitance for logic level storage and, therefore, has a minimum operating frequency.

One special feature is its true in-circuit emulation capability. The device is equipped with a modular port scan device, or scan path. This feature allows the connection of an XDS500 emulator, which, unlike previous generation microprocessors, does not require the device to be removed from its target and replaced with an emulator pod to perform software development and test via device emulation. A block diagram of the TMS320C30 DSP is provided in figure 1.

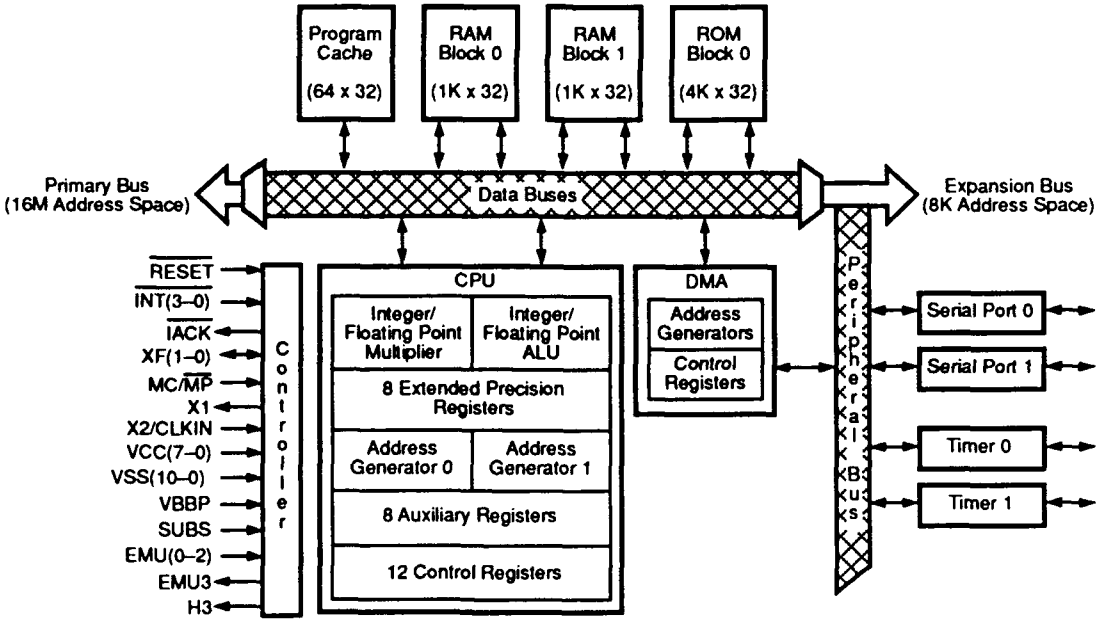

Figure 1. Basic TMS320C30 Block Diagram

The TMS320C30 has a 24-bit address space, which allows it to address 16 million 32-bit words of external memory. In addition, it contains several areas of on-chip memory including a 4-K x 32-bit on-chip ROM block, two 1-K x 32-bit on-chip RAM blocks, and a 64- x 32-bit instruction cache. It contains eight extended precision registers and eight auxiliary registers. Its on-chip peripherals include a direct memory access (DMA) controller, serial ports, and timers.

We tested a total of 15 devices, 10 from the same military-grade preproduction lot (designated lot 1) and 5 from a separate commercial-grade lot (lot 2). Lots 1 and 2, termed EPIC-1A and EPIC-1Z, respectively, by the manufacturer, are the result of two distinct production CMOS processes. Table 1 summarizes the available differences between these two processes.

Table 1. Summary of EPIC-1A and EPIC-1Z Process Differences

Parameter	EPIC-1A (Lot 1)	EPIC-1Z (Lot 2)
Starting Material	13-µm P epilayer (13 ohm-cm)	5-µm P epilayer (13 ohm-cm)
Gate Oxide	25 nm (900 °C)	25 nm (900 °C)
Sidewall Oxide	300 nm	200 nm

Note that the overall sequence of process steps is identical between the two processes and shares the following process techniques:

- Twin-well tank formation
- Identical clad process
- Identical double level metal process
- Identical oxide/nitride overcoat process

The motivation for moving to the EPIC-1Z process stems from the process margin gained at the 1-µm level; therefore, future sub-micron technology may be developed with this newer process. For example, the upcoming TMS320C40 and TMS320C50 will be fabricated using EPIC-1Z material.

SECTION 3

TEST BED DESCRIPTION

While there continues to be a growing need for radiation data for increasingly higher speed microprocessors, testing of such critical devices continues to become increasingly more difficult. Before developing test fixtures to accomplish this testing, a literature search of test methods used for other microprocessors revealed a diversity of methods. We examined tests for such devices as the Intel 8080 [2], 8085 [2,3,4], 8086 [5,6], 80186 [7], 80286 [7], and 80386 [8]; the Inmos Transputer [9]; the Motorola 6800 [2,3], 68000 [10], and 68020 [11]; and the Zilog Z80A [6,12,13,14] and Z8002A [10,12]. After reviewing the cited tests of the various microprocessors listed, we discussed the various methodologies with authorities in the field [15,16,17]. Our investigation led to our test methodology for this device. We performed full in-flux testing while operating the device at full speed. We chose to perform in-flux tests in an effort to provide an accurate characterization of the device's radiation performance. While we are aware that radiation susceptibility may be clock-rate dependent, we operated the device at full speed (16 MHz) since this is a DSP's normal operational regime. Our testing can be classified as that of external control -- we controlled/monitored the device under test via TI's XDS1000 development environment. While we readily employed the XDS1000, it did not provide us the required platform for any radiation environment -- a stand-alone TMS320C30-based card with (external) communications capabilities. For this, we designed and assembled a stand-alone card. Our test fixture consists of a single TMS320C30 with minimal support circuitry, which is shielded during testing, as shown in figure 2.

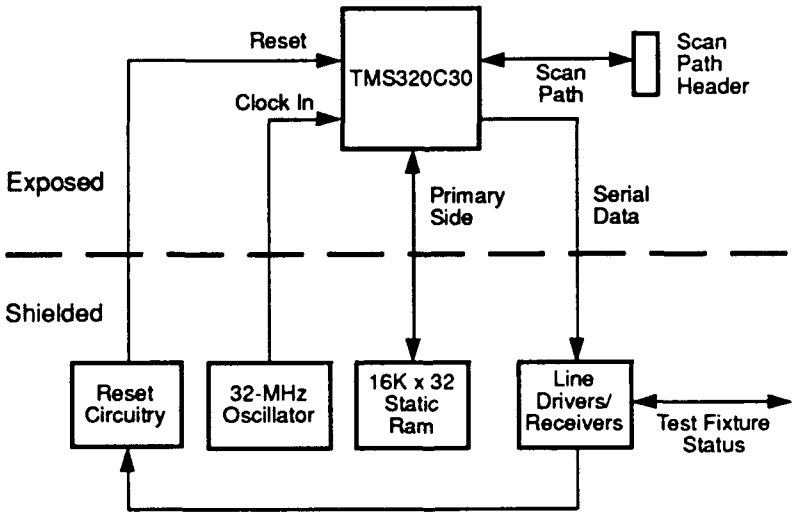

Figure 2. TMS320C30 Radiation Test Fixture

We developed our own custom assembly language programs to test the device. These programs provide comparable completeness to other methods we reviewed -- they test all functional components of the device, use much of the instruction set, and are robust in reporting errors in the wake of radiation effects. These programs execute on the device under test and output test status via one of two on-chip serial ports. Results are passed to a second TMS320C30, part of the XDS1000 development environment, operating in a PC-AT-compatible Zenith Z-248 computer. This second DSP, which operates outside of the radiation environment, provides test results to the host PC's controlling 80286 microprocessor. Results are continuously provided/updated on the PC's display. Tests accomplished include:

- CPU register file
- On-chip memory
- On-chip cache
- On-chip peripherals
- Multiplier, arithmetic logic unit (ALU), auxiliary register arithmetic unit (ARAU)

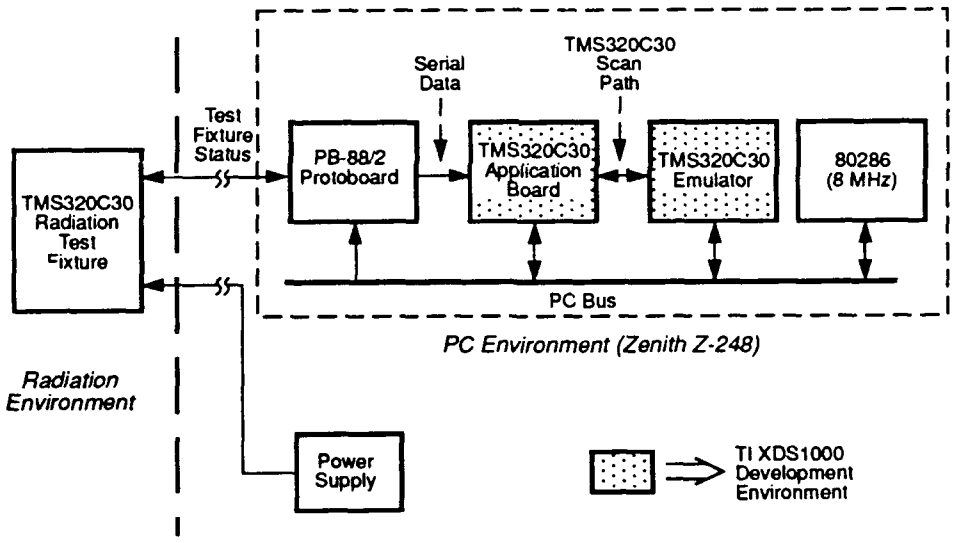

Figure 3. MITRE-Developed Test Bed for TMS320C30 Radiation Testing

SECTION 4

TEST OVERVIEW

Testing of the TMS320C30 determined the total dose failure level, dose rate upset threshold level, and dose rate latch-up threshold level. The testing was performed at the Rome Air Development Center (RADC) radiation facility located at Hanscom Air Force Base in Bedford, MA. The following subsections provide further details of the test procedures and facilities.

4.1 TOTAL DOSE TESTING

The total dose testing of the TMS320C30 was conducted in accordance with the requirements of MIL-STD-883C, method 1019.3 [18]. The exception was that testing was performed at a dose rate of approximately 575 rads (Si) per minute. Testing continued until each device had a functional failure. The testing was performed on a sample size of 10 devices from the EPIC-1A process and 3 devices from the EPIC-1Z process. In addition to the devices being tested, sufficient unirradiated controls were used to ensure proper operation of the test fixture. The testing of the TMS320C30 was conducted in-flux (i.e., functional testing was performed during the radiation exposure). Upon detecting a functional failure, the test fixture recorded the time the failure occurred. In addition, current measurements were taken to characterize device current (I_{CC}) versus total accumulated dose.

The total dose facility uses a Cobalt-60 (Co-60) source. The Co-60 cell is a dry room (10' x 10' x 10') with the source mounted on an elevator assembly positioned near the middle of the room. The strength of the source is approximately 27,000 curies. The radiation exposure rate is determined by the distance of the exposed specimens from the Co-60 source.

4.2 DOSE RATE TESTING

We tested the TMS320C30 to determine the dose rate threshold for upset of the device and to demonstrate the dose-rate-induced latch-up immunity of the device. Testing was performed using both a 20-30-ns full width half maximum (FWHM) pulse and a 1-μs FWHM pulse width. The dose rate testing was performed using both the flash X-ray machine and the LINAC. The flash X-ray facility contains a Pulserad 314 machine manufactured by Physics International Company. The maximum dose rate achievable is 1.6×10^{10} rads (Si) per second with a 20-ns FWHM pulse width. The dose rate that the exposed specimen receives is determined by the distance from the machine's output port. The LINAC facility contains an 18-MeV machine manufactured by Applied Radiation Corporation. The LINAC operates in the electron beam mode for this experiment. The maximum dose rate achievable is 1.3×10^{12} rads (Si) per second with a 20-ns FWHM pulse width and 2.6×10^{10} rads (Si) per second with a 1-μs FWHM pulse width.

4.2.1 Upset

The dose rate upset testing of the TMS320C30 device was in accordance with the requirements of MIL-STD-883C, method 1021.1 [19]. The device was continuously functionally tested throughout the dose rate exposure. The test fixture monitored the internal registers and memory locations of the device while being exposed to subsequently higher dose rates. An upset was defined as any change of state in either the internal registers or the internal memory locations.

4.2.2 Latch-Up

The dose rate latch-up testing of the TMS320C30 device was in accordance with the requirements of MIL-STD-883C, method 1020 [20], with the exception that all testing was performed at room temperature. The test fixture power supply current and functionality of the device were monitored. The device was exposed to subsequently higher dose rates until a latch-up condition occurred. Latch-up was indicated by a current draw significantly greater than nominal, excessive device heating and partial to complete loss of functionality.

4.3 DOSIMETRY

The test facility provided the dosimetry necessary to establish an accurate measurement of the radiation dose received by the TMS320C30 test specimens. These dosimetry procedures are traceable to the National Institute of Standards and Technology (NIST). The dosimetry for the total dose experiment was provided by a Victoreen Model 500 Precision Medical Physics Electrometer. This instrument measures the dose rate of the radiation exposure. Calibration of the dosimetry system is accomplished using thermoluminescent dosimeters (TLDs). The dose rate multiplied by the time of the exposure will yield the total dose accumulated in the test specimens.

The dosimetry for the dose rate experiments was provided by a UM4001 PIN diode. The PIN diode is biased with +100 volts and terminated into a 50-ohm load at an oscilloscope input. The photocurrent of the diode is proportional to the dose rate exposure. The PIN diode response versus the dose rate is 1.1×10^8 rads (Si) per second per volt. This calibration factor is determined using TLDs.

SECTION 5

DATA ANALYSIS TECHNIQUES

We performed a statistical analysis of the test results assuming that the radiation response of the devices followed a lognormal probability distribution. This assumption has been accepted by the nuclear hardening community [21]. (The adoption of this assumption allows the inference of population characteristics from a small sample of data.) Since the calculations must be performed in log space, the real failure levels acquired from the testing are first converted to their equivalent natural logs. The sample mean and standard deviation can then be calculated in log space. These values are then used to determine the adjusted mean failure level, statistical failure level (SFL), and probability of survival (P_S) for the TMS320C30. After these calculations are complete, the results are converted to their equivalent real values for reporting in section 6.

5.1 CALCULATION OF THE SAMPLE MEAN AND STANDARD DEVIATION

We reduced the radiation failure levels to determine the sample mean (X) and standard deviation (s). These and subsequent calculations, shown in [22], were made as follows:

$$X = \frac{1}{n} \sum_{i=1}^{n} \ln (x_i) \tag{1}$$

$$s = \left[\frac{1}{n-1} \sum_{i=1}^{n} (\ln (x_i) - X)^2 \right]^{1/2} \tag{2}$$

where

n = number of devices in the sample

x_i = failure level of the i-th device.

5.2 CALCULATION OF THE ADJUSTED MEAN

The sample mean calculation shown above provides a point estimate of the population mean. A point estimate of the population mean is of limited usefulness, as it does not provide any information about the precision of the estimate. There is no way to determine

the magnitude of the sampling error from a point estimate. Sampling error refers to the range of sample means that would be obtained from independent samples taken from the same population. Information concerning this sampling error is essential to properly interpret the results.

Statistical procedures can be used for estimating the population mean as an interval rather than as a single point. The width of the interval indicates the precision of the estimate. The interval width is proportional to the variability in the individual device radiation failure levels. The standard deviation calculation shown above provides a measure of this variability.

An interval estimate of the population mean (μ) consists of two bounds between which μ is estimated to exist. The lower bound of the interval (termed the adjusted mean, X_a) represents the worst-case estimate of the population mean radiation failure level.

The variation in the radiation failure levels for the devices was accounted for by calculating an adjusted mean failure level. The adjusted mean failure level is defined as including at least 50 percent of the population with a 90-percent confidence level ($P_S / C = 50/90$). This (one-sided) calculation was made as follows:

$$X_a = X - (K_{50/90} * s) \tag{3}$$

where

X = sample mean from equation (1)

s = sample standard deviation from equation (2)

$K_{50/90}$ = tolerance factor for the given sample size with $P_S / C = 50/90$ from table 2.

5.3 CALCULATION OF THE STATISTICAL FAILURE LEVEL

Statistical procedures can be used to estimate an interval that bounds the expected radiation failure levels of the population. The width of the expected value interval is proportional to the variability in the individual device radiation failure levels. A measure of this variability is the sample standard deviation. The lower bound of the expected value interval (the SFL) represents the worst-case estimate of the population minimum radiation failure level.

The SFL is defined as including at least 99 percent of the population with a 90-percent confidence level ($P_S / C = 99/90$). This level represents the radiation level at which devices within the population are expected to begin to fail. Thus, this is the maximum radiation environment in which the device will continue to operate properly. This (one-sided) calculation was made as follows:

$$SFL = X - (K_{99/90} * s) \quad (4)$$

where

X = sample mean from equation (1)

s = sample standard deviation from equation (2)

$K_{99/90}$ = tolerance factor for the given sample size with $P_S / C = 99/90$ from table 2.

Table 2. Tolerance Factors for the X_a and SFL Calculations for Various Sample Sizes

Sample Size (n)	$K_{50/90}$ for X_a	$K_{99/90}$ for SFL
3	1.069	7.640
4	0.819	5.437
5	0.686	4.666
6	0.603	4.242
7	0.544	3.972
8	0.500	3.783
9	0.466	3.641
10	0.437	3.532
11	0.414	3.444
12	0.393	3.371
13	0.376	3.310
14	0.361	3.257
15	0.347	3.212
16	0.335	3.172
17	0.324	3.136
18	0.314	3.106
19	0.305	3.078
20	0.297	3.052
21	0.289	3.028
22	0.282	3.007
23	0.275	2.987
24	0.269	2.969
25	0.264	2.952

5.4 CALCULATION OF THE PROBABILITY OF SURVIVAL

We determined the P_S versus radiation level for each radiation environment. The P_S is a quantitative estimate of probability that the TMS320C30 will continue to properly operate after exposure to a given radiation level. Conversely, the P_S is a measure of the risk of a device failing below the particular radiation level.

To calculate the P_S, it is first necessary to calculate the K_{TL} factor associated with a 90-percent confidence level. The calculation is made as follows:

$$K_{TL} = \frac{X - L}{s} \tag{5}$$

where

X = sample mean from equation (1)

s = sample standard deviation from equation (2)

L = level at which the P_S is to be determined.

We can see from the above that the K_{TL} is the number of standard deviations the sample mean failure level is from the radiation level of interest. Therefore, once the K_{TL} factor is known, normal probability distribution statistics can be applied to determine the P_S. The P_S for the TMS320C30 was calculated by interpolation between the K_{TL} values shown in table 3.

Table 3. K_{TL} Values for P_S Interpolation for Various Sample Sizes (n)

	P_S							
n	0.75000	0.90000	0.95000	0.97500	0.99000	0.99900	0.99990	0.99999
3	2.602	4.258	5.310	6.244	7.340	9.651	11.566	13.932
4	1.972	3.187	3.957	4.637	5.437	7.128	8.533	9.756
5	1.698	2.742	3.400	3.981	4.666	6.112	7.311	8.358
6	1.540	2.494	3.091	3.620	4.242	5.556	6.646	7.596
7	1.435	2.333	2.894	3.389	3.972	5.201	6.223	7.113
8	1.360	2.219	2.755	3.227	3.783	4.955	5.927	6.775
9	1.302	2.133	2.649	3.106	3.641	4.772	5.708	6.525
10	1.257	2.065	2.568	3.011	3.532	4.629	5.538	6.332
11	1.219	2.012	2.508	2.935	3.444	4.515	5.407	6.176
12	1.188	1.966	2.448	2.872	3.371	4.420	5.290	6.049
13	1.162	1.928	2.403	2.820	3.310	4.341	5.196	5.941
14	1.139	1.895	2.363	2.774	3.257	4.274	5.116	5.850
15	1.119	1.866	2.329	2.735	3.212	4.215	5.046	5.771
16	1.101	1.842	2.299	2.701	3.172	4.164	4.986	5.702
17	1.085	1.820	2.272	2.670	3.136	4.118	4.932	5.641
18	1.071	1.800	2.249	2.643	3.106	4.078	4.884	5.586
19	1.058	1.781	2.228	2.618	3.078	4.041	4.841	5.537
20	1.046	1.765	2.208	2.596	3.052	4.009	4.802	5.493
21	1.035	1.750	2.190	2.576	3.028	3.979	4.766	5.452
22	1.025	1.736	2.174	2.557	3.00	3.952	4.734	5.416
23	1.016	1.724	2.159	2.540	2.987	3.927	4.704	5.382
24	1.007	1.712	2.145	2.525	2.969	3.904	4.677	5.351
25	0.999	1.702	2.132	2.510	2.952	3.882	4.652	5.322

SECTION 6

TEST RESULTS

The following subsections provide the total dose and dose rate results for MITRE's test of the TMS320C30.

6.1 TOTAL DOSE TEST RESULTS

The results of our Co-60 testing are shown in table 4 -- here, the SFL varied from approximately 3,000 rads (Si) to 3,500 rads (Si) with a dose rate of approximately 575 rads (Si) per minute. Figure 4 provides the probability of survival versus total accumulated dose.

Table 4. Total Dose Test Results

Lot	*Source*	Dose Rate (rads (Si) per *minute*)	*n*	X (rads (Si))	X_a (rads (Si))	SFL (rads (Si))
1	Co-60	582	10	4,700	4,454	3,163
2	Co-60	566	3	5,560	5,185	3,469

In addition to monitoring the operation of the device under test during total dose irradiation, we monitored the device current. The following curve (figure 5) provides an average device current versus accumulated dose with a dose rate of approximately 575 rads (Si) per minute. Note that the nominal operating current for the TMS320C30 itself is approximately 300 milliamperes.

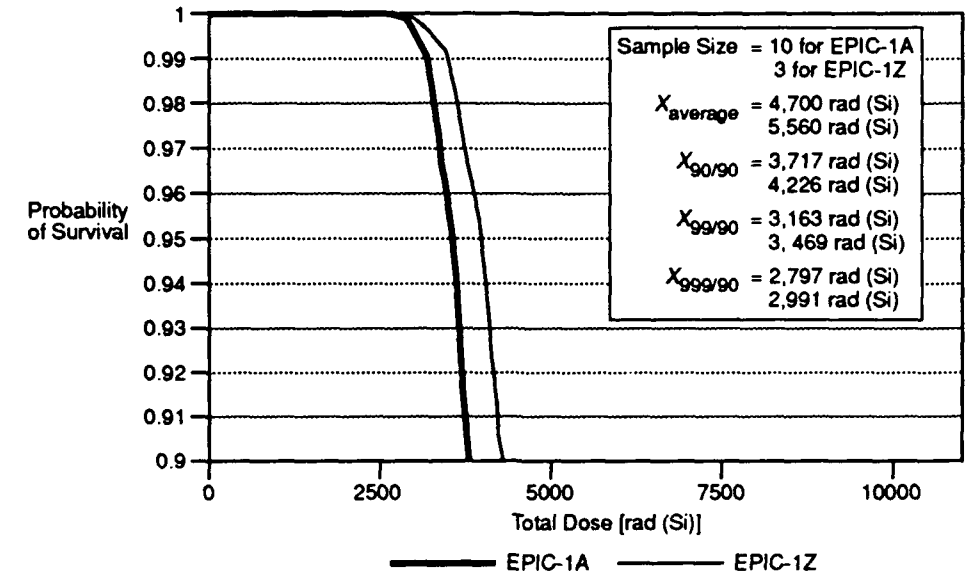

Figure 4. Total Dose Probability of Survival

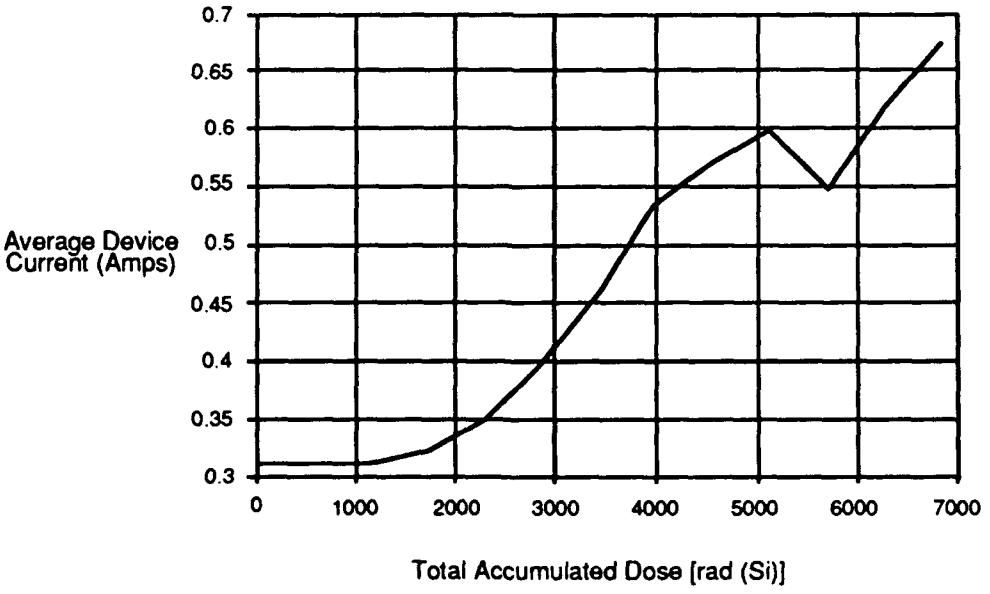

Figure 5. Average Device Current versus Total Accumulated Dose

6.2 DOSE RATE TEST RESULTS

Dose rate testing consisted of both prompt characterization using a narrow pulse (20-30-ns FWHM) and delayed characterization using a wide pulse (1-μs FWHM). Both upset threshold and dose-rate-induced latch-up phenomena were investigated. The use of the flash X-ray facility versus the LINAC facility was based on the order in which the device lots arrived and the availability of the particular facility at the time of their arrival.

6.2.1 Prompt Environment

Table 5 provides the results of upset threshold testing using a narrow pulse of either 20 or 30 ns. Table 6 shows the results of latch-up using the narrow pulse.

Table 5. Prompt Dose Rate Upset Threshold Results (Narrow Pulse)

Lot	Pulse Source	Pulse Width	*n*	X (rads (Si) per second)	X_a (rads (Si) per second)	SFL (rads (Si) per second)
1	Flash X-ray	20 ns	10	1.2×10^8	1.1×10^8	6.8×10^7
2	LINAC	30 ns	5	2.7×10^8	2.1×10^8	7.2×10^7

Table 6. Prompt Dose Rate Latch-Up Results (Narrow Pulse)

Lot	Pulse Source	Pulse Width	*n*	Devices Latched	Minimum Latch-Up (rads (Si) per second)	Maximum No Latch (rads (Si) per second)
1	Flash X-ray	20 ns	10	6	1.6×10^9	3.0×10^9
2	LINAC	30 ns	5	1	1.7×10^9	2.7×10^9

Note the maximum levels we were able to attain using the two different pulse sources. Also note that as we observed latch-up at room temperature, we did *not* test for latch-up

conditions at elevated temperatures. Figure 6 summarizes the prompt dose rate effects by providing the probability of *no* upset versus dose rate.

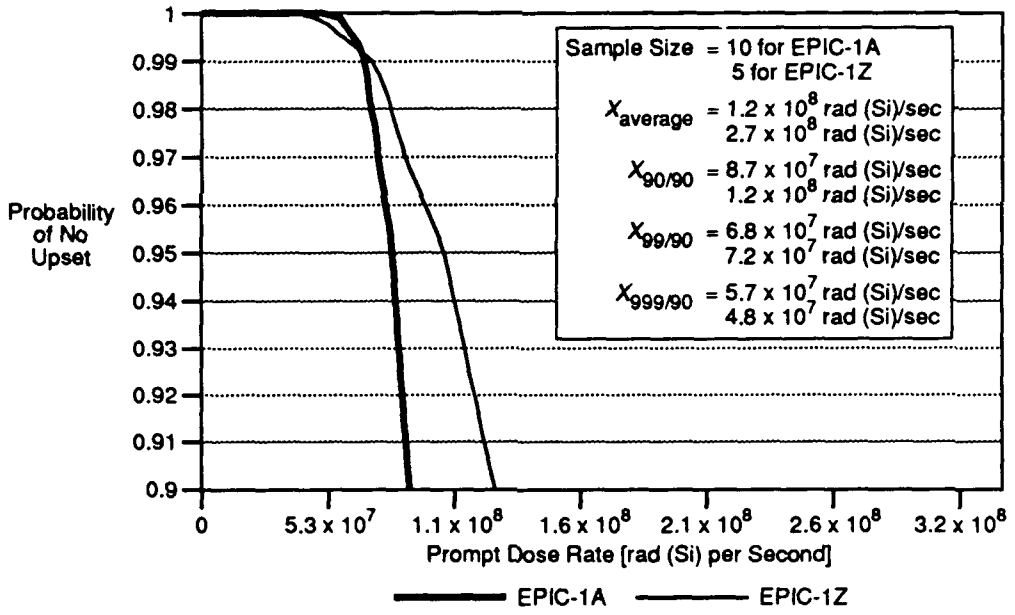

Figure 6. Prompt Dose Rate Probability of No Upset

6.2.2 Delayed Environment

Tables 7 and 8 provide the result of delayed dose rate effects using a 1-μs-wide pulse for upset threshold and latch-up, respectively, with figure 7 providing the probability of *no* upset. As the sample standard deviation was zero for the EPIC-1A devices, we provided a pseudo-P_S curve by using the standard deviation of the EPIC-1Z material -- hence the use of the dashed line to caution the reader.

Table 7. Delayed Dose Rate Upset Threshold Results (Wide Pulse)

Lot	Pulse Source	Pulse Width	*n*	*X* (rads (Si) per second)	X_a (rads (Si) per second)	SFL (rads (Si) per second)
1	LINAC	1 µs	3	3.5×10^7	3.5×10^7	3.5×10^7
2	LINAC	1 µs	5	9.3×10^7	7.8×10^7	3.2×10^7

Table 8. Delayed Dose Rate Latch-Up Results (Wide Pulse)

Lot	Pulse Source	Pulse Width	*n*	Devices Latched	Minimum Latch-Up (rads (Si) per second)	Maximum No Latch (rads (Si) per second)
1	LINAC	1 µs	3	3	5.6×10^7	2.6×10^8
2	LINAC	1 µs	5	0	--	8.4×10^8

6.3 DISCUSSION

During our testing, we observed failures of most all functional units of the TMS320C30. While it was not the goal of this testing to absolutely identify susceptible areas on the device, we did notice a predominance of interrupt-related failures as a result of both dose rate and total dose irradiation. Our use of the serial port for communication worked well enough to detect early failures of the device in all environments; however, that too failed during latch-up testing where current measurements were used to indicate such a condition. When possible, we also used the emulation port of the device to examine failures after testing -- this feature is available on many new microprocessors and should be considered for future testing. Note that as this device does have some dynamic logic on-chip, its inherent hardness will most likely *degrade* with a decrease in clock frequency. As the radiation-induced loss of charge is a direct function of time, the slower clock frequency will provide a longer window for this phenomenon. Therefore, users of the TMS320C30 operating the device at slower clock frequencies should consider this when examining our data.

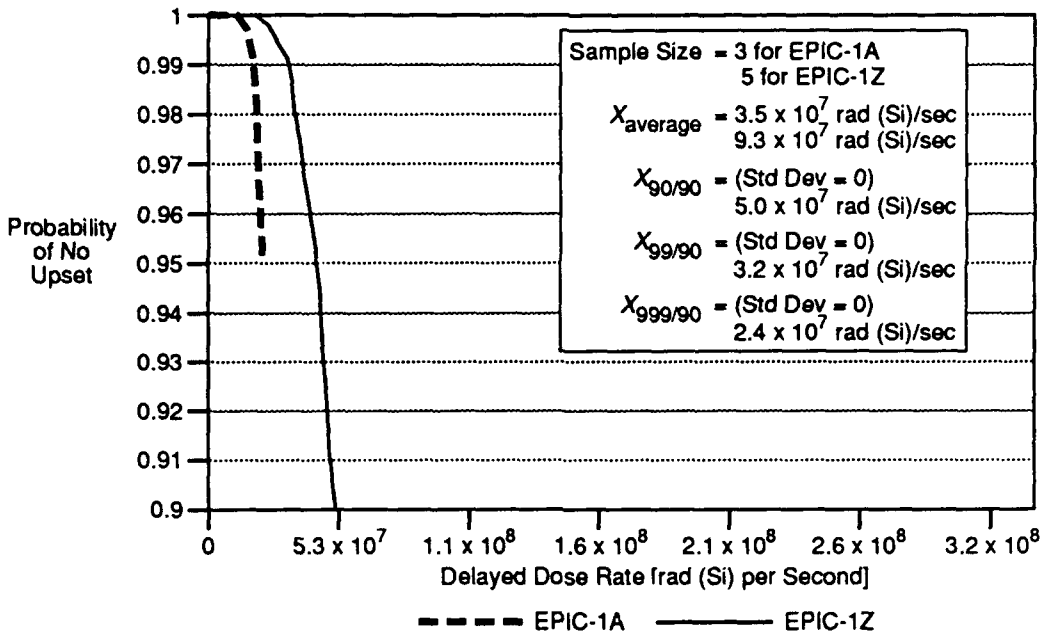

Figure 7. Delayed Dose Rate Probability of No Upset

As the results indicate, the EPIC-1Z material appears to provide more immunity to radiation-induced failure in both environments (presumably due to the thinner epilayer and sidewall oxide). However, the limited number of EPIC-1Z devices tested precludes such a conclusion. In any case, results from both lots indicate the general failure trends of the device. In addition, failures of the EPIC-1Z TMS320C30s provide an indication as to the possible hardness of the next-generation TMS320C40 and TMS320C50.

SECTION 7

CONCLUSION

MITRE's test of the TMS320C30 resulted in failures between 4- and 5-K rads (Si) in the total dose environment with an SFL of approximately 3-K rads (Si). In the prompt dose rate environment using a 20-30-ns pulse, the device failed in the area of 1×10^8 rads (Si) per second with an SFL of approximately 7×10^7 rads (Si) per second. For the delayed dose rate environment using a 1-μs pulse, the device failed in the area of 5×10^7 rads (Si) per second with an SFL of approximately 3.2×10^7 rads (Si) per second. We observed latch-up in both environments at room temperature, at approximately 1×10^9 rads (Si) per second in the prompt environment and at approximately 1×10^8 rads (Si) per second in the delayed environment.

To summarize, this test effort provides the general failure trends of the TMS320C30 but may not reflect the full failure range due to the limited sample size (15 devices total). Testing by other organizations may provide additional data that will expand the user community's knowledge of the full failure range of the TMS320C30.

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*These documents have not been reviewed by the Directorate for Security Review and are therefore not available for public dissemination.

GLOSSARY

ACRONYMS

ALU	arithmetic logic unit
ARAU	auxiliary register arithmetic unit
CMOS	complimentary metal-oxide semiconductor
Co-60	Cobalt-60
DMA	direct memory access
DOD	Department of Defense
DSP	digital signal processor/processing
FWHM	full-width half maximum
NIST	National Institute of Standards and Technology
PGA	pin grid array
RADC	Rome Air Development Center
SFL	statistical failure level
TI	Texas Instruments
TLD	thermoluminescent dosimeter
TTL	transistor-transistor-logic

SYMBOLS

K_{TL}	one-sided tolerance factor
P_s	probability of survival
s	standard deviation
X	sample mean
X_a	adjusted mean