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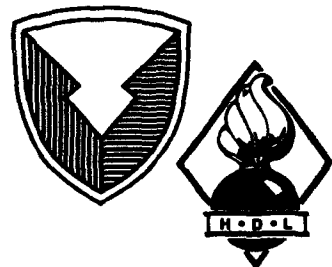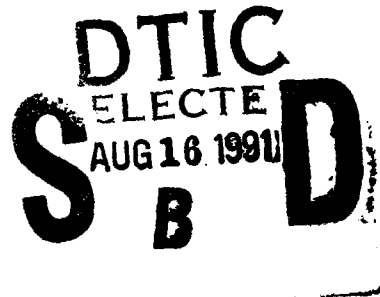**AD-A239 469**

Analog-to-Digital Conversion Techniques

by Clyde C. DeLuca

U.S. Army Laboratory Command
Harry Diamond Laboratories
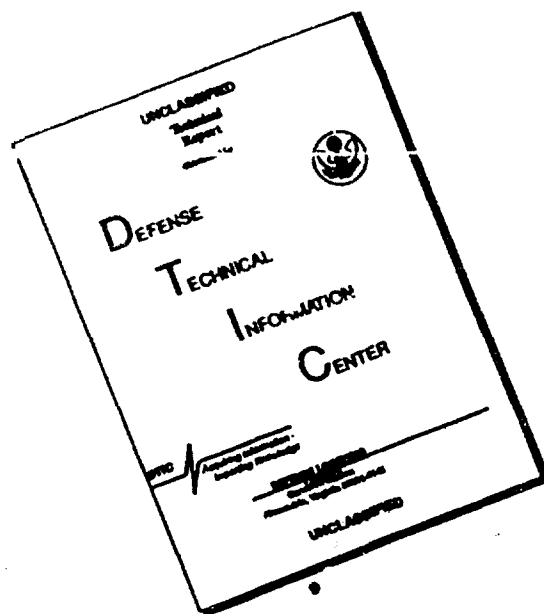Adelphi, MD 20783-1197

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13. ABSTRACT (Maximum 200 words)

Various types of analog-to-digital converters (ADC's) are currently on the market. Intended to familiarize the reader with different ADC's, this report examines three specific types: integrating, successive approximation, and flash or parallel and subranging converters. The methods by which these ADC's process signals are discussed, in addition to their common uses. This report also includes a brief market survey which demonstrates the many ADC's that are available from different manufacturers.

14. SUBJECT TERMS

Analog-to-digital converter (ADC), integrating, successive approximation, parallel, flash, sample/hold

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1. Introduction

Many signal-processing problems can be solved efficiently through the use of digital techniques. However, since the signal often originates in analog form, it must be transformed to a digital form. Many techniques have been employed to make this transformation; one class of device, referred to as analog-to-digital converters (ADC's), is reviewed.

2. Operation of Analog and Digital Circuits and ADC's

In concept and in practice, designers must be concerned that analog circuits perform in the real world, where limits to resolution and accuracy are directly related to physical environment, electrical interference, signal magnitude, component tolerances, and bandwidth. Because digital circuits, on the other hand, deal with binary quantities, they have high noise immunity, no drift, high speed, and low cost. The rules for using digital circuits are few and simple. However, as conversion times increase, accuracy and number of bits decrease. An ADC is often the element that limits the performance of a processing system in such areas as dynamic range and speed.

An ADC operates by taking time samples of an analog signal and outputting a digital word that represents the signal amplitude. The converter quantizes an input signal by approximating a linear transfer function by a staircase (see fig. 1). For a standard ADC, each step occurs every quantum or least significant bit (LSB). The quantum Q, the amplitude resolution, equals the full-scale voltage divided by the number of states ($V_{fs}/2^n$), where n is the number of bits.

Figure 1. Staircase transfer function (ref. 8; reprinted by permission).

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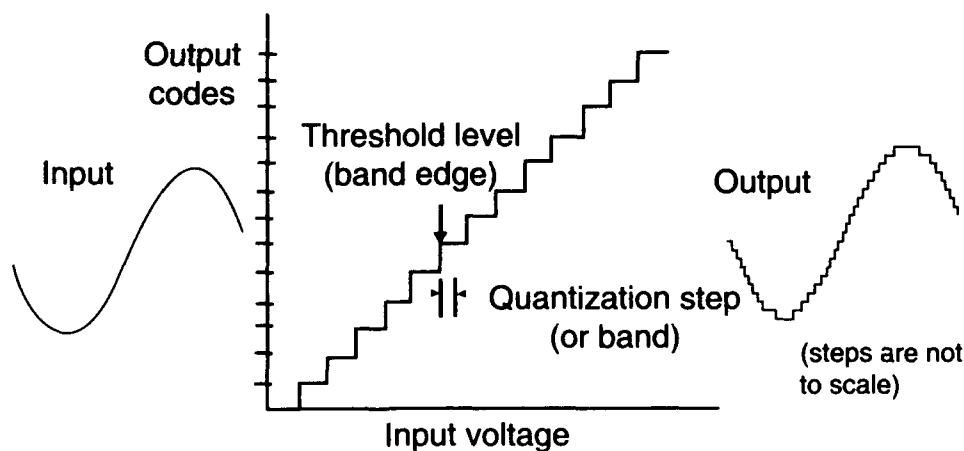
3. Types of ADC's

This report discusses some of the many different types of ADC's, describing the more commonly used ones: integrating (slope or ramp), successive approximation, and flash or parallel and subranging ADC's. These descriptions are intended to give the reader a working understanding of these different types of ADC's.
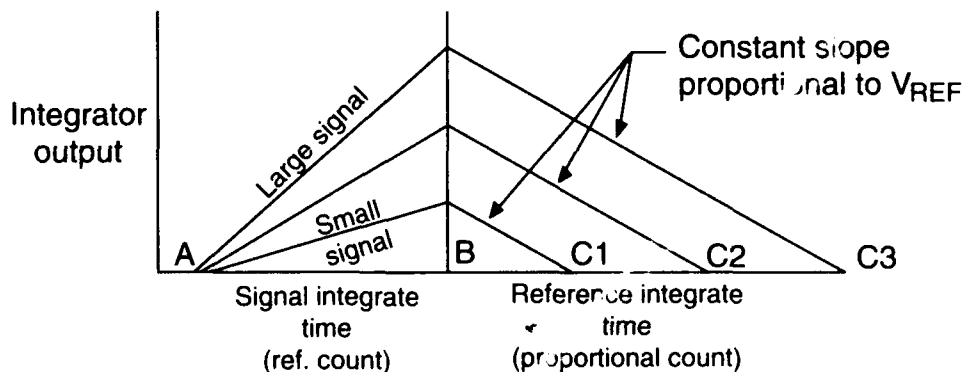
3.1 Integrating ADC's

Integrating ADC's, using ramp or slope techniques, perform an indirect conversion, by first converting the signal to a function of time, and then converting from the time function to a digital number using a counter. These ADC's are suitable for use in digital voltmeters and those applications in which a relatively long time may be taken for conversion. These types obtain the benefits of noise reduction through signal averaging.

In one type of integrating ADC, the single-slope converter, a reference voltage is integrated until the output of the integrator is equal to the input voltage. The time required for the integrator to go from zero to the level of the input is proportional to the magnitude of the input voltage and is measured by an internal clock. Measurement accuracy is sensitive to clock speed and integrating capacitance, as well as the reference accuracy.

The dual-slope ADC is an integrating converter in which the unknown signal is converted to a proportional time interval. The device then measures the interval digitally, by integrating the unknown signal for a predetermined period of time. The integrator input is then switched to the reference and integrates down from the level determined by the unknown, until a zero level is reached. The time for the second integration is proportional to the average of the unknown signal level over the predetermined integrating period (see fig. 2).

Figure 2. Voltage-time relationship in dual-slope conversion (ref. 1; reprinted by permission).

Integrator output

Large signal

Small signal

Constant slope proportional to V_{REF}

A   B   C1   C2   C3

Signal integrate time (ref. count)

Reference integrate time (proportional count)

Though too slow for fast data acquisition, dual-slope converters are generally quite adequate for transducers such as thermocouples, and they are the predominant circuit used in constructing digital voltmeters. A shortcoming of conventional dual-slope converters is that errors (e.g., offsets) at the input of the integrating amplifier or the comparator show up as errors in the digital word.

A scheme for nullifying most input errors in dual-slope converters uses the quad-slope principle. In this scheme, the device goes through two cycles of the dual-slope conversion, once with zero input and once with the analog input being measured. The errors determined during the first cycle are subtracted digitally from the result of the second cycle. The quad-slope scheme results in an extremely accurate converter.

3.2 Successive Approximation ADC's

Successive approximation (SA) converters are widely used, especially for interfacing with computers, because they are capable of high resolution and high speed. Conversion time is fixed and independent of the magnitude of the input voltage. Each conversion is unique and independent of the results of the previous conversion, because the internal logic is cleared at the start of each conversion.

The conversion technique consists of comparing the unknown input against a precise voltage or current generated by a digital-to-analog converter (DAC), shown in figure 3. The input of the DAC is the digital value of the output of the ADC. The conversion process is similar to a weighing process using a chemist's balance, with a set of n binary weights (i.e., 1/2 lb, 1/4 lb, 1/8 lb, 1/16 lb = 1 oz, 1/2 oz, ...) for unknowns up to a pound [4].

Figure 3. 8-bit digital-to-analog converter (ref. 1; reprinted by permission).

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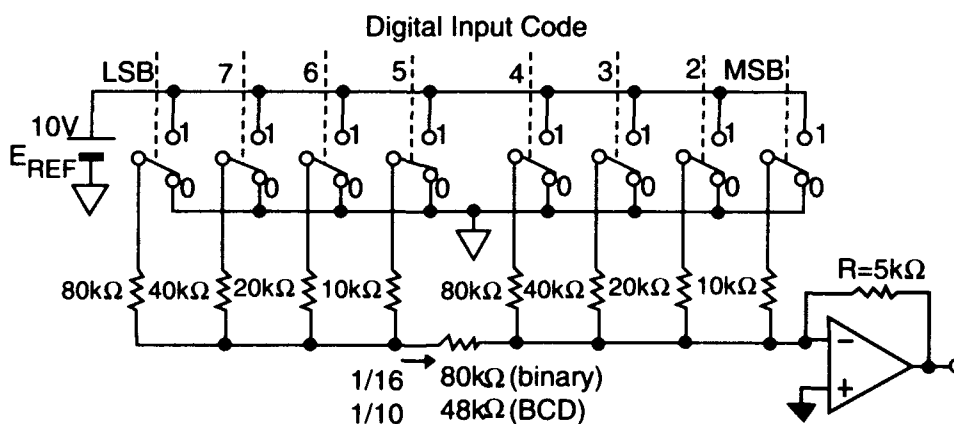
After the conversion command is applied, and the converter has been cleared, the DAC's most significant bit (MSB) output (half scale) is compared with the input. If the input is greater than the MSB, it remains on (i.e., logic 1), and the next bit (quarter scale) is tried. If the input is less than the MSB, it is turned off (i.e., logic 0), and the next bit is tried. If the second bit does not add enough weight to exceed the input, it is left on (1), and the third bit is tried. The process continues in order of descending bit weight until the last bit has been tried. The process completed, the status line changes states to indicate that the contents of the output register now constitute a valid conversion. The contents of the output register form a binary digital code corresponding to the magnitude of the input signal. A block diagram of an SA ADC is shown in figure 4.

If the input were to change during conversion, the output number could no longer represent the analog input. To avoid any problems of this sort, one usually employs a sample and hold (S/H) device ahead of the converter to retain the input value that was present at a given time before the conversion starts. The S/H maintains a constant output throughout the conversion. The status output of the converter could be used to release the S/H from its hold mode at the end of the conversion. An S/H may not be needed if the signal varies slowly enough and is sufficiently noise-free that changes will not be enough to alter the conversion process during the conversion interval.

3.3   Flash or Parallel and Subranging ADC's

Parallel ADC's get their name from an array of comparators connected to a resistor string and an input voltage (see fig. 5). Parallel ADC's are commonly used in radar digitizing, digital signal processing, and spectrum analysis. A parallel or flash converter employs $2^n - 1$ comparators biased 1 LSB apart, starting with +1/2 LSB, where n is the number of bits in the output. For zero input, all comparators are off. As the input increases, it causes an increasing number of comparators to switch state. The outputs of the comparators are applied to gates, which provide a set of outputs that fulfill the appropriate conditions for Gray code output. The advantage of this approach is that conversion occurs rapidly, with speed limited only by the switching time of the comparators and gates. As the input changes, the output changes. This is the fastest approach to conversion. Unfortunately, the number of elements increases geometrically with resolution. The number of bits, and hence the input voltage range of these converters, decreases as the sampling rate increases. Currently, a 10-bit flash ADC has a maximum sampling rate of 50 million samples per second (MSPS). At

Figure 4. Successive approximation ADC (ref. 1; reprinted by permission).
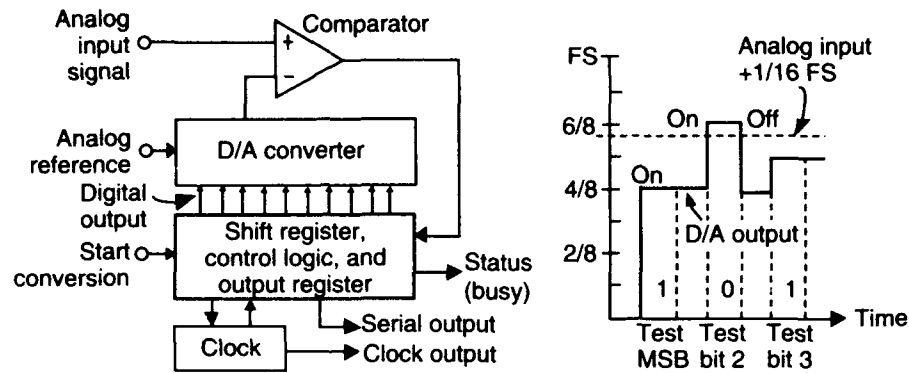
Figure 5. Parallel or flash converter (ref. 1; reprinted by permission).

Quantum-to-gray-code conversion

Level	0	1	2	3	4	5	6	7
MSB	0	0	0	0	1	1	1	1
Bit 2	0	0	1	1	1	1	0	0
Bit 3	0	1	1	0	0	1	1	0
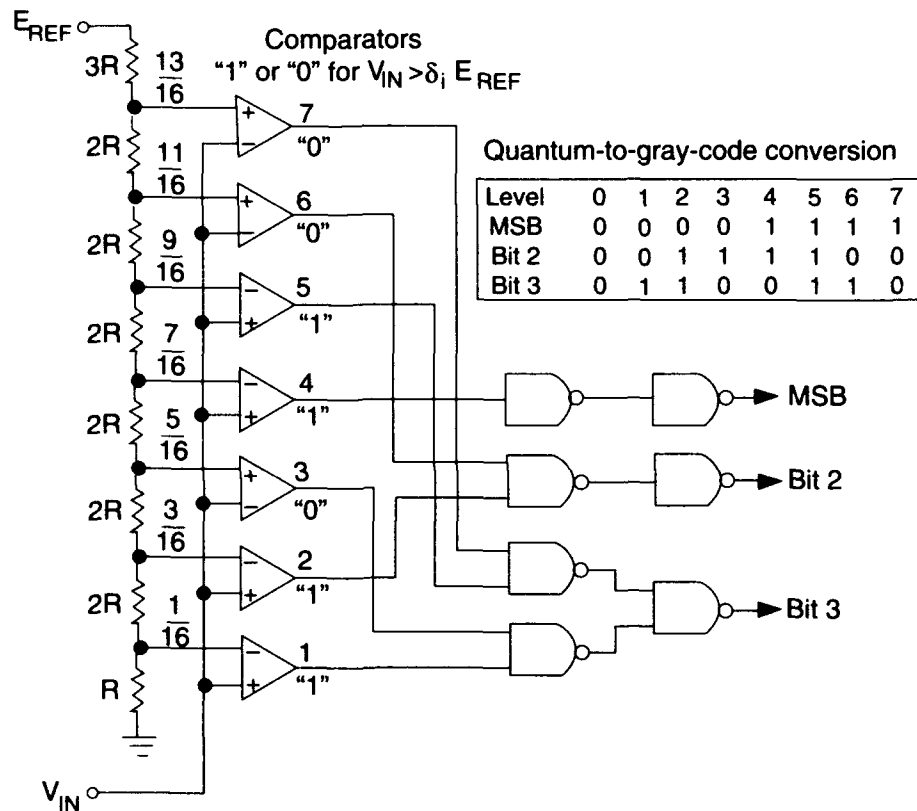
8 bits, the sampling rate increases dramatically to 500 MSPS. See table 1 for the different flash converters currently on the market.

High-speed, high-resolution ADC's employ a subranging architecture with digital error correction. See figure 6 for a block diagram of a 12-bit 10-MSPS ADC. The analog signal is initially sent to an S/H to reduce the aperture jitter of the system. The output of the S/H is sent to two places: a 7-bit flash-encode module and a subtraction circuit. A 7-bit encoder is formed by the parallel connection of two 6-bit flash encoders (see fig. 7). An important feature of the S/H design is that the

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Table 1. A/D market survey

| Device	Type	Resolu-tion (bits)	Clock rate (MHz)	Input voltage (V)	Input bandwidth (MHz)	Linearity (LSB)	Power (W)
Honeywell, Inc.							
HADC77100	F	8	150	0 to +2	60	± 1/2	1.75
HADC77200	F	8	150	0 to –2	100	± 1/2	2.7
HADC78160	SA	16	0.3	± 2.5, 5	0.15	± 1	1.0
HADC77600	F	10	50	2 to –2	25	± 3/4	4.7
ILC Data Device Corporation							
ADC–00300	SUBR	12	2	0 to 5, 10, ± 2.5, 5	10	± 1	4.3
ADC–00110	SUBR	12	10	± 2.5, 5	35	± 1	5.5
TRW LSI Products, Inc.							
TDC1048	F	8	20	0 to –2	7	± 1	*
THC1070	F	10	20	± 1, 2	10	± 1	*
THC1200	SUBR	12	10	± 2.5, 0.16	50	± 1	*
Burr–Brown Corporation							
ADC600	SUBR board	12	10	± 1.25	40	± 1	8.5
ADC603	SUBR	12	10	± 1.25	40	± 1/2	4.5
PCM75	SA	16	0.05	0 to 5, 10	0.025	± 1	1.55
Analog Devices, Inc.							
CAV–1210	SUBR board	12	10	± 1, 2	30	± 1/2	18
CAV–1220	SUBR board	12	20	± 1, 2	35	± 1/2	20.3
AD9005	SUBR	12	10	± 1	38	± 1/2	4.2
AD1175K	INTE	22	20Hz	± 5	2	± 1/2	2.0
AD571J	SA	10	0.04	± 5	0.02	± 1	0.8

Note: F is a flash ADC. INTE is an integrating ADC. SA is a successive approximation ADC. SUBR is a subranging hybrid ADC, unless noted otherwise.
*Information not available.

Figure 6. Block diagram of a 12-bit, 10-MSPS converter (ref. 6; reprinted with permission from ILC Data Device Corporation).
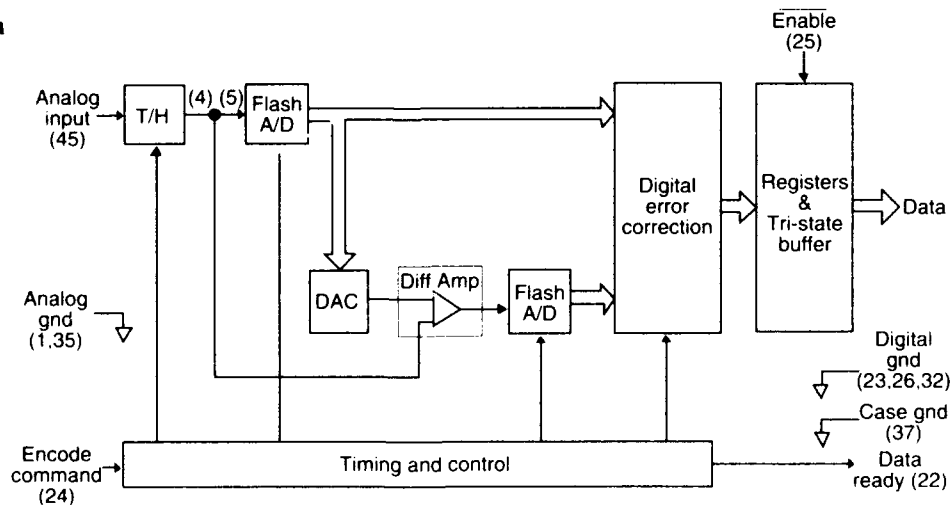
Figure 7. 7-bit flash encoder (ref. 5). ©1987 Burr-Brown Corporation. Reprinted, in whole or in part, with the permission of Burr-Brown Corporation.
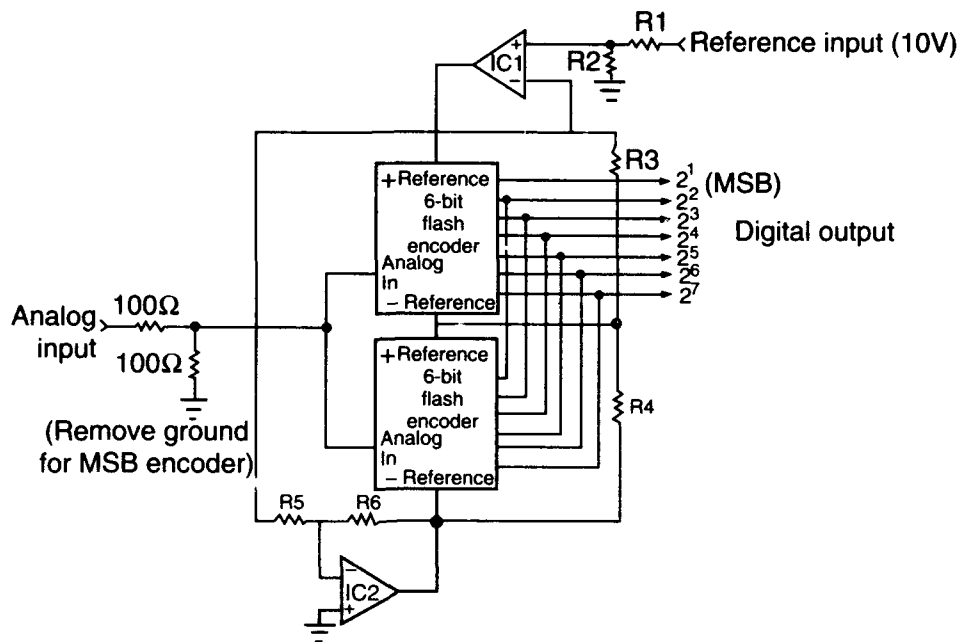
sampling switch is buffered by a fast-settling closed-loop amplifier. This allows the gain of the entire ADC to be predetermined at the modular level, to a typical accuracy of 0.02 percent.

The first encoder determines the initial coarse approximation of the input signal. Two 7-bit flash encoders are used for the MSB and LSB encoders. These provide adequate resolution, accuracy, and range to allow the digital circuitry to assemble the final 12-bit word properly. The digital output from the first flash encoder is sent to the subtraction unit. There, the initial approximation to the analog signal is converted back to analog form and subtracted from the input signal for further processing. The output from the S/H is subtracted from the DAC by means of a resistive network. The output of the resistive network is then amplified by a high-speed amplifier (gain of 32) so that the signal attains the proper range before being applied to the final flash encoder. The output from this amplifier is sent to another 7-bit flash encoder that is similar to the previously mentioned encoder that quantizes the MSB's. Once the data in each of the encoders have been latched, they are then sent to the digital-error correction module to be assembled into the final 12-bit word.

Digital correction is achieved by adding the data from each encoder in the proper manner. Although the first flash encoder determines the signal to only 7-bit accuracy, it is still possible to achieve 12-bit performance, providing that the DAC has the necessary accuracy. The

output of the subtraction circuit contains the difference between the output of the S/H and the analog equivalent of the first 7-bit encoding process. If the 7-bit encoder's accuracy were better than 12-bit, it would only be necessary to have a 5-bit encoder to quantize the residue without digital correction. Since the first encoder is typically only 7-bit accurate, it is necessary that the second encoder have two additional bits to handle the larger difference that could result. The final 12-bit word is then developed at the output of the 12-bit adder.

These subranging ADC's come in different packages. The Analog Devices AD1210 is a 12-bit 10-MSPS converter that comes on a printed circuit board with many individual components. On the other hand, the ILC Data Device Corporation's ADC-00100 comes as a hybrid; all the components are inside a single package. The two are functionally the same, but the hybrid is considerably smaller (1 × 1.5 in. versus 6 × 5 in.) and consumes less power (5.5 versus 18 W).

Researchers are interested primarily in high-speed ADC's for signal-processing applications. Companies that produce high-speed flash and subranging converters include Honeywell, ILC Data Devices Corporation, Analog Devices, TRW, Burr-Brown, and Sipex. Table 1 shows the specifications for several different ADC's. The list is not complete but is a sampling of what is presently on the market.

4. Concluding Remarks

Manufacturers have not yet been able to fulfill the growing demand for more speed and accuracy in ADC's. The maximum capability of current technology ADC's is 12 bits at a sampling rate of 10 MSPS. A few devices can deliver 14 bits at 5 MSPS, but they are large, power hungry, and not much more accurate than the 12-bit subranging ADC's. ILC Data Devices Corporation and Analog Devices are predicting a fully operable 14-bit 10-MSPS ADC by 1991.

Glossary of Commonly Used Terms

Acquisition time: The acquisition time of a sample/track and hold circuit for a step change is the time required by the output to reach its final value, within a specified error band, after the sample/track command has been given. Included in this time are switch-delay time, the slewing interval, and settling time for a specified output-voltage change.

Aperture (delay) time: In a sample/track and hold, the aperture or delay time is the time required after the hold command for the switch to open fully. The sample is, in effect, delayed by this interval, and the hold command would have to be advanced by this amount for precise timing.

Aperture uncertainty (or jitter): Aperture uncertainty is the range of variation in the aperture time. If the aperture is tuned out by advancing the hold command by a suitable amount—or if the signal is being sampled repetitively—this specification establishes the ultimate timing error, hence the maximum sampling frequency for a given resolution.

Automatic zero: To achieve zero stability in many integrating analog-to-digital converters (ADC's), a time interval is provided during each conversion cycle to allow the circuitry to compensate for drift errors. The drift error in such converters is substantially zero.

Code width: Code width is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width (for all but the first and last codes) is the voltage equivalent of 1 least significant bit (LSB) of the full-scale range. Code width should generally not be less than 0.5 LSB or more than 1.5 LSB. Because the full scale is fixed, the presence of excessively wide codes implies the existence of narrow and perhaps even missing codes.

Droop rate: When a sample and hold circuit using a capacitor for storage is in hold, it will not hold the information forever. Droop rate is the rate at which the output voltage changes. The change of output occurs as a result of leakage or bias currents flowing through the storage capacitor. The polarity of change depends on the sources of leakage within a given device. In integrated circuits with external capacitors, it is usually specified as a (droop or drift) current, and in modules or integrated circuits having internal capacitors, as a rate of change.

Linearity, differential: In an ADC, midpoints between code transitions should be 1 LSB apart. Differential nonlinearity is the deviation between the actual difference between midpoints and 1 LSB, for adjacent codes. If this deviation is equal or more than –1 LSB, a code will be missed.

Linearity, integral: While differential linearity deals with errors in step size, integral linearity has to do with deviations of the overall shape of the conversion response. Even converters that are not subject to differential linearity errors (e.g., integrating types) have integral linearity (or just linearity) errors.

Missing codes: An ADC is said to have missing codes when a transition from one quantum of the analog range to the adjacent one does not result in the adjacent digital code, but a code removed by one or more counts. Missing codes can be caused by large negative-differential linearity errors, noise, or changing inputs during conversion. An ADC's proclivity towards missing codes is also a function of temperature.

Monotonicity: An ADC is said to be monotonic if its digital output either increases or remains the same if the input increases. The monotonic condition requires that the derivative of the transfer function never change sign.

Nonlinearity: Nonlinearity in an instrumentation or isolation amplifier is defined as the deviation from a straight line on the plot of output versus input. The magnitude of linearity error is the maximum deviation from a best straight line with the output swinging through its full-scale range. Nonlinearity is usually specified as a percentage of full-scale range.

Pedestal, or sample-to-hold offset step: In sample/track and hold amplifiers, the pedestal is a shift in level between the last value in the sample and the value settled to in the hold; in devices having fixed internal capacitors, it includes charge transfer or offset step. However, for devices that may use external capacitors, the pedestal is often defined as the residual step error after the charge transfer is accounted for and/or cancelled. Since it is unpredictable in magnitude and may be a function of the signal, it is also known as offset nonlinearity.

Sample/track and hold: A sample and hold amplifier is a device that has a signal input, signal output, and control input. In the sample (or track) mode, the output tracks the input until the hold command is applied

at the control input. In the hold mode, the output retains the last value of the input signal that it had at the time the hold command was applied. The term *sample and hold* implies that the device samples the input for a short period of time and stays in the hold mode for the duration of the duty cycle. A track and hold device, on the other hand, spends most of the time tracking the input and is switched into the hold mode for only brief intervals. In data-acquisition systems operating at high update rates (greater than 1 MHz), the terms *track and hold* and *sample and hold* lose their distinction.

Settling time: Settling time is defined as the time elapsed from the application of a perfect step input to the time when the amplifier output has entered and remained within a specified error band symmetrical about the final value. Settling time, therefore, includes the time required for the signal to propagate through the amplifier, and for the amplifier to slew from the initial value, recover from the slew-rate-limited overload, and settle to a given error in the linear range.

Slew rate: Slew rate is a limitation in the rate of change of output voltage, usually imposed by some basic circuit consideration, such as limited current to charge a capacitor. Amplifiers with slew rates greater than 75 V/μs are usually seen only in more sophisticated and expensive devices. The output slewing speed of a voltage-output DAC is usually limited by the slew rate of the amplifier used at its output.

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