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Research and Development on Advanced Silicon Carbide Thin Film Growth Techniques and Fabrication of High Power and Microwave Frequency Silicon Carbide-Based Device Structures

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13. ABSTRACT *(Maximum 200 words)*

A gas source molecular beam epitaxy system has been designed, constructed and commissioned for the growth and doping of SiC thin films at low temperatures. Monocrystalline films of β-SiC on 3° off-axis (100) Si substrates have been obtained at 1075°C, as shown by Auger profiles and reflection high energy electron diffraction. The heteroepitaxial growth of Ti rectifying contacts on n-type α(6H)-SiC has also been achieved at room temperature via ultra high vacuum electron beam evaporation. I-V measurements revealed low leakage currents (≈6nA at −10V) and the lowest ideality factors ever reported for contacts on SiC. Theoretical simulation has shown that SiC IMPATTs are capable of good RF output power in the 30-100 GHz range. However, the dc-RF conversion is fundamentally low and may restrict development. High frequency 6H-SiC MESFETs have been fabricated with the highest values of F_t and F_{max} being 2.9 GHz and 1.9 GHz, respectively. Methods to reduce the source and gate resistances were pursued. Avalanche characteristics in α(6H)-SiC p-n junction IMPATT diode were observed for the first time. This device structure appears promising for high power microwave operation.

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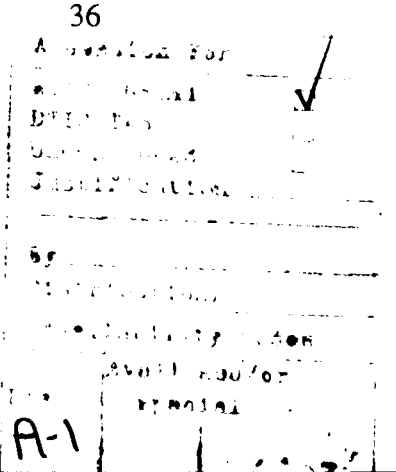

I. Growth of SiC Thin Films at Reduced Temperatures (Rowland/Davis–NCSU)

A. Introduction

Beta SiC, the lone zincblende (cubic) polytype in the Si-C system, has the potential for use in specialized electronic applications utilizing its attractive physical and electronic properties such as wide band gap (2.2 eV at 300K) [1], high breakdown electric field (2.5×10^6 V/cm) [2], high thermal conductivity (3.9 W/cm °C) [3], high melting point (3103K at 30 atm) [4], high saturated drift velocity (2×10^7 m/s) [5], and small dielectric constant (9.7) [6].

Growth of SiC has traditionally been performed on Si substrates due to the lack of availability of high-quality SiC substrates. The recent development of high-purity single-crystal α(6H)-SiC wafers by Cree Research, Inc. has made growth on these substrates more feasible, and future research in this program will employ these materials. Growth on silicon has progressed over the years despite large mismatches in the coefficients of thermal expansion and lattice parameters between the two materials. The technique of chemical vapor deposition (CVD) has been primarily used to date as the method for growth of β-SiC on Si. However, the high growth temperatures normally used and the relative lack of control of growth thickness and doping species found in CVD of SiC have given an impetus to the development and construction of a gas source molecular beam epitaxy (GSMBE) system for growth and doping of SiC. MBE allows for precise control of growth parameters and minimization of sample contamination during deposition. Parameters such as growth thickness and dopant concentration can thus be controlled as closely as possible to the monolayer level and reproducibly obtained using this technique.

Growth using the system has commenced, with experiments performed to date concerned with growth of β-SiC on Si, due to the relative abundance and low cost of Si substrate material. In the following sections we present preliminary results obtained for SiC growth on off-axis Si (100) substrates, including growth of monocrystalline β-SiC. In addition, work to be initiated using α(6H)-SiC substrates provided by Cree Research, Inc. is described.

B. Experimental Procedure

Growth studies were performed on 3° off-axis (100) heavily arsenic-doped Si wafers (ρ=.002.-.004 Ω-cm). All substrates were cleaned prior to growth in the following manner: H_2SO_4 at 70°C for 5 min, DI water rinse for 1 min, 1:1 solution (by volume) of 50% H_2O_2 and NH_4OH at 70°C for 5 min, DI water rinse for 1 min, BOE etch at room temperature for 5 min, and DI water rinse for 2 min. After cleaning, the samples were secured in a SiC-coated graphite sample holder and placed in the load lock. After the load lock reached a

pressure of 2×10^{-6} torr or less, the samples were then transferred to the growth chamber. The base pressure of the system prior to growth is typically 1×10^{-9} torr. The gas-source molecular beam epitaxy system described in detail in previous reports was used for the deposition.

Prior to growth, samples were heated in UHV conditions for about 5 min at the desired growth temperature to remove any surface contaminants. Source gases (Si_2H_6 and C_2H_4) were then introduced to the system to initiate film growth. Flow rates of Si_2H_6 have been varied from 0.2 to 0.4 sccm, while flow of C_2H_4 has been kept at 2.0 sccm in all but one experiment. The pressure during growth has typically been 6×10^{-5} torr. Growth temperatures have been varied to date from 1025°C to 1125°C.

The chemical composition and depth profiles of the samples were obtained using a JEOL JAMP-30 scanning Auger microprobe. Samples which showed a 1:1 Si to C ratio from Auger results were then examined by reflection high-energy electron diffraction (RHEED) with an incident beam energy of 10 keV to determine the crystal structure and an estimate of film quality.

C. Results

Growth at 1075°C with 2.0 sccm C_2H_4 and 0.4 sccm Si_2H_6 for 90 min produced a monocrystalline β-SiC film. Auger spectra from the surface showed the presence of a surface oxide from atmospheric exposure after growth. Once the surface oxide was sputtered away, the sample was found to be stoichometric SiC. Figure 1(a) shows the Auger depth profile from a sample grown at 1075°C with 2.0 sccm C_2H_4 and 0.4 sccm Si_2H_6 for 90 min. The film shows good 1:1 stoichometry to a thickness of around 700Å. The oxygen level shown on the depth profile is a typical background level for the system. Examination of a monocrystalline β-SiC film previously grown on (100) Si using CVD as a standard for comparison gave a resultant Auger depth profile nearly identical to that found in the first 700Å of the film shown in the figure.

Other experimental conditions attempted to date have resulted in a Si-rich stoichometry as shown by Auger analysis. A typical example of this is shown in Figure 1(b), which is a sample grown at 1025°C with 1.0 sccm C_2H_4 and 0.2 sccm Si_2H_6 for 90 min. It is interesting to note that results from growth at 1125°C using 2.0 sccm C_2H_4 and 0.4 sccm Si_2H_6 did not produce a 1:1 SiC ratio as occurred at 1075°C.

RHEED analysis of the SiC sample show the film was cubic in crystal structure and monocrystalline. RHEED patterns (Figure 2) were taken for different orientations of the SiC film. Some signs of streaking of the pattern indicate the film has a fairly smooth morphology and is of relatively good quality. The (110) reflection (Figure 2(b)) shows

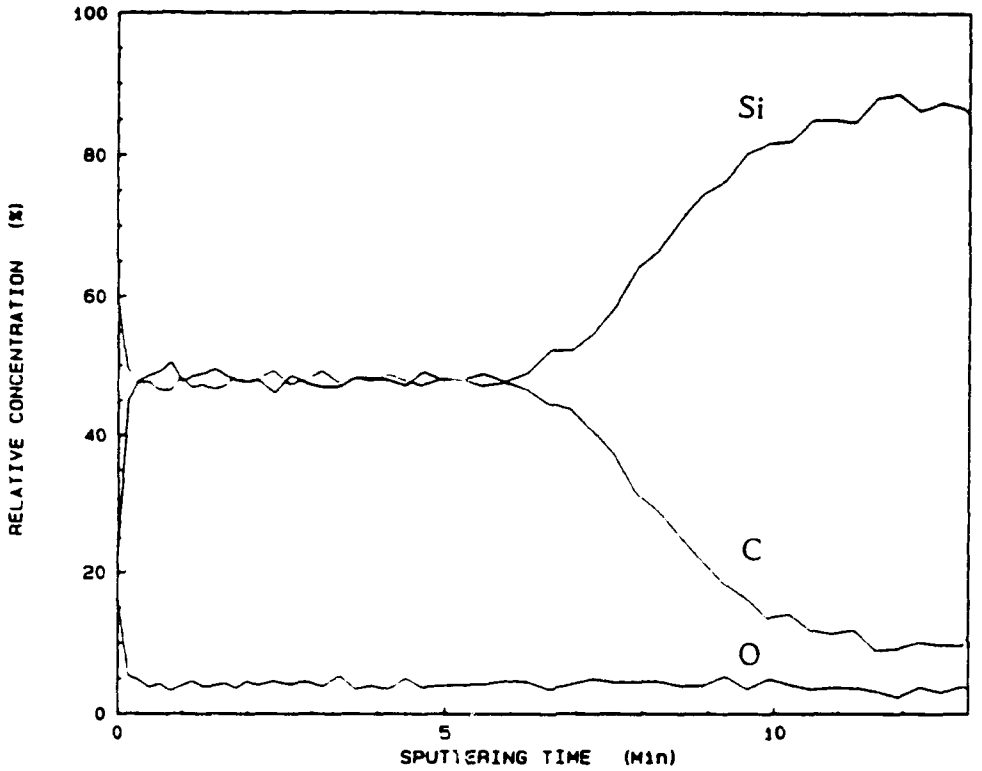

Figure 2a. Auger depth profile of SiC sample grown at 1075°C.

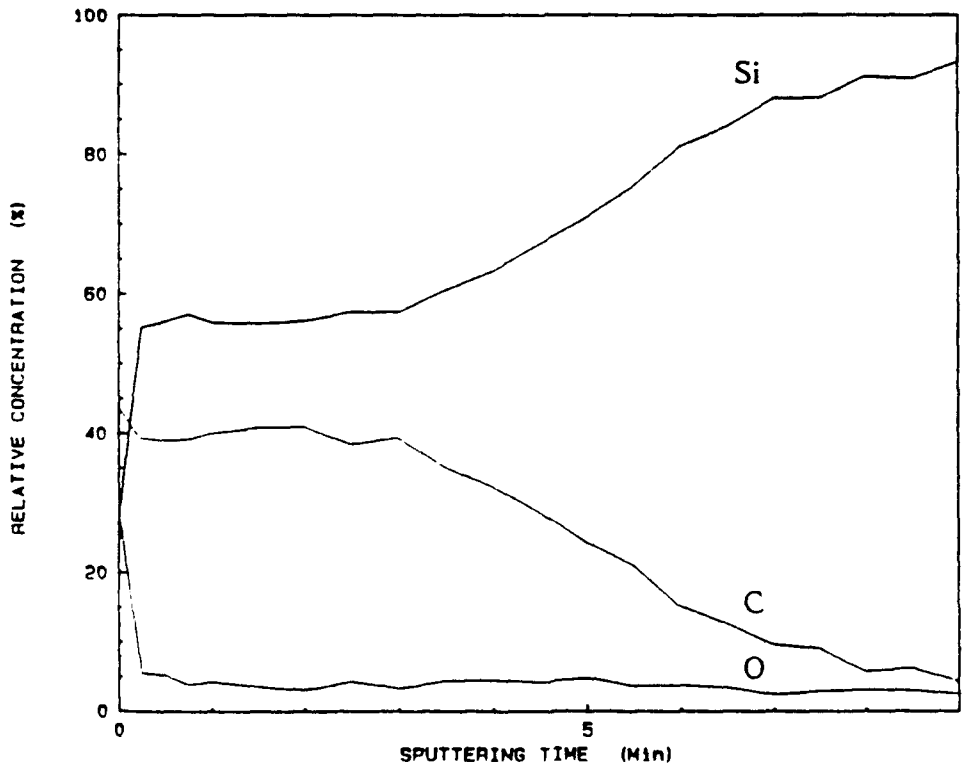

Figure 2b. Auger depth profile of SiC sample grown at 1025°C.

Figure 3a. β-SiC RHEED pattern from (1000) reflection.

Figure 3b. β-SiC RHEED pattern from (110) reflection.

some evidence of twinning in the grown film. Films of β-SiC grown by chemical vapor deposition (CVD) typically show a large density of defects including twins [7]. Optical and scanning electron micrographs of all films to date show a pitted surface region which is likely due to preferential evaporation along {111} planes [8]. Transmission electron microscopy analysis of this film is planned for the near future.

D. Discussion

Auger and RHEED results indicate the presence of epitaxial β-SiC on Si at 1075°C. However, the same conditions at a higher temperature produce a Si-rich film as indicated by Auger. In addition, a film grown at 1125°C with a 10:1 C/Si source ratio (2.0 sccm C_2H_4 and 0.2 sccm Si_2H_6) for 90 min was also Si-rich. The greater C/Si ratio did translate into a greater amount of C in the grown film, but still did not result in a 1:1 Si to C ratio.

The possibility that Si could be diffusing into the growing film, leading to a Si-rich film, comes to mind. However, carburization of the Si substrate was attempted (0.5 sccm C_2H_4 for 10 min) followed by growth at 1125°C at 2.0 sccm C_2H_4 and 0.2 sccm Si_2H_6 for 90 min. This resulted in a film with a similar Si:C ratio and thickness to that grown without the carburization step. Carburized layers grown by CVD, where Si is supplied by diffusion from the substrate, are typically 5-12 nm in thickness when grown in 5 min as the temperature is increased from 25°C to 1360°C [9]. Si-rich layers grown to date in the MBE system are typically much thicker; the thickness of the film shown in Figure 1(b) is approximately 80 nm thick. This is undoubtedly too thick for Si diffusion from the substrate into the growing film to play a major role in the Si-rich character of the films grown at higher temperatures.

Pitting of the sample surface during growth is quite likely related to preferential evaporation of Si [8]. These pits appear rectangular or square in shape, and are believed to actually be pyramids bounded by {111} planes. These pyramids similar to those initially seen for carburization of Si surfaces for SiC growth [10]. Silicon samples heated under MBE conditions at temperatures where significant evaporation occurs (750°C or higher for (100) Si wafers [11]) typically show this pitted morphology. Si films grown as low as 800°C using 1.0 sccm disilane on this MBE system during initial testing of the growth system showed this pitted morphology as seen by optical microscopy. Suppression of formation of these pitted regions may be possible with proper choice of growth conditions and substrate cleaning methods.

E. Conclusions

The MBE growth system designed and built for SiC growth and doping is now operational. Growth of SiC on Si substrates has been achieved. Films grown using MBE

have been characterized using Auger analysis and RHEED. Initial results obtained using this system indicate heteroepitaxial growth of β-SiC on off-axis (100) Si substrates at 1075°C with 2.0 sccm C_2H_4 and 0.2 sccm Si_2H_6 for 90 min. Other conditions, including growth at higher temperatures, have yet to result in SiC films. Further work is necessary to optimize growth parameters and characterize grown films.

F. Future Plans/Goals

Further analysis including transmission electron microscopy and electrical measurements of these films will be employed to examine the defects present in the grown films in greater detail. Further growth experiments are ongoing to determine the optimum source gas flow rates and growth temperatures for β-SiC on Si growth and results from these will be shown in a future report.

In the near future, growth on (0001) α(6H)-SiC substrates provided by Cree Research, Inc. will commence. In addition, doping of SiC films grown on SiC substrates will be performed using Al from an MBE effusion cell as the p-type dopant and N obtained from the electron cyclotron resonance (ECR) plasma decomposition of N_2 as the n-type dopant. In addition, growth will be attempted using an ECR source from ASTeX, Inc. for plasma decomposition of C_2H_4 and CH_4 in order to lower the growth temperature. These SiC films will be characterized using TEM, RHEED, Auger, and secondary ion mass spectrometry (SIMS), and results will be presented in a future report.

II. Heteroepitaxial Growth and Characterization of Titanium Films on α(6H)-Silicon Carbide*

A. Introduction

The thermal and electronic properties of silicon carbide make this wide bandgap semiconductor attractive for use in high power, high temperature, and radiation hard applications. The future development of SiC device technology depends on, and may in fact be limited by, the ability to form good ohmic and Schottky contacts. For an ideal, abrupt junction the barrier height is defined by the Schottky -Mott limit, or the difference between the metal work function and the electron affinity of the semiconductor. However, interface states between the metal and semiconductor cause deviations from ideality. In fact,

*Presented at the Materials Research Society Spring 1991 Conference: L.M. Spellman, R.C. Glass, and R.F. Davis of the Department of Materials Science and Engineering, North Carolina State University, Raleigh, NC 27695-7907; T.P. Humphreys, Hyeongtag Jeon, and R.J. Nemanich of the Department of Physics, North Carolina State University, Raleigh, NC 27695-8202; Sopa Chevacharoenkul of the Microelectronics Center of North Carolina, P.O. Box 12889, Research Triangle Park, NC 27709; and N.R. Parikh of the Department of Physics and Astronomy, University of North Carolina, Chapel Hill, NC 27599-3255.

Pelletier *et al* [12] have reported Fermi level pinning in 6H-SiC due to intrinsic surface states, indicating little dependence of barrier height on the work function of the metal. On the other hand, Waldrop *et al* [13] have reported strong work function dependence for metal/β-SiC barrier heights, giving encouragement for the ability to control barrier heights of metals on 6H-SiC.

The ability to grow epitaxial metal layers on semiconductors presents opportunities to grow novel two- and three-dimensional device structures, extremely high quality heterostructures, and excellent electrical contacts [14]. This report describes the characterization of epitaxial titanium on alpha (6H) silicon carbide and the corresponding electrical characteristics of these contacts.

B. Experimental

Single crystal substrates of 6H-SiC were provided by Cree Research, Inc. All substrates were nitrogen-doped n-type (10^{16} – 10^{18} cm^{-3}). The 6H polytype consists of alternating (0001) planes of Si and C. The Si-terminated (0001) surface tilted 3°-4° off axis towards (11$\bar{2}$0) was used for all depositions and analyses. Some of the substrates were provided with 0.5-0.8 μm thick epitaxial layers of 6H-SiC (n-type, 10^{16} cm^{-3}) grown on the 6H-SiC substrates.

Two experimental procedures were used depending on whether or not the substrates consisted of a SiC epitaxial layer; the procedures differ in terms of cleaning preparation and deposition technique. The first of these was used with SiC substrates on which no epilayers were grown ('bulk substrates'). The substrates were spun with a solution of ethanol, HF, and deionized water (10:1:1) and then introduced into an ultrahigh vacuum (UHV) deposition/ analytical system through a load-lock chamber. Immediately upon entry into UHV (base pressure 10^{-9} Torr), surface structure and chemistry were monitored with a retarding grid LEED/Auger system. The substrate was then transported *in vacuo* into the deposition chamber. Titanium was deposited onto unheated substrates by thermal evaporation from a hot wire filament. The deposition rate was kept at approximately 12 Å/min. until a total thickness of 400-500 Å was achieved.

A second procedure was used with substrates containing SiC epilayers. These substrates were cleaned first by a 10 min. dip in ethanol/HF/deionized water (10:1:1) and then by a thermal desorption in UHV (1 - 5 × 10^{-10} Torr). A resistive graphite heater was used to heat the substrates at 700°C for 15 min. X-ray photoelectron spectroscopy (XPS) and low energy electron diffraction (LEED) were used to monitor surface chemistry and structure, respectively. The XPS system runs with a Riber Mac2 semi-dispersive electron energy analyzer and a Riber pulse counter. Titanium was deposited onto unheated substrates by electron beam evaporation (base pressure 10^{-10} Torr). The first 100Å was

deposited at a rate of 10 Å/min. The deposition was then increased to 20 - 30 Å/min. to give a total thickness of 1000 Å. For samples which were to be characterized electrically, deposition was through a Mo mask in contact with the substrate, leaving a patterned metal film. All subsequent annealing was done in UHV.

Current-voltage (I-V) measurements were taken with a Rucker & Kolls probing station in conjunction with an HP 3135A Semiconductor Parameter Analyzer. The sample structures consist of circular contacts (20 mil diameter) which were deposited on a (0001) SiC epitaxial layer and Ag paint as a large area back contact.

Samples were prepared in cross-section for TEM analysis. Images were taken with both a Hitachi 800 and a Philips 430 microscope. High resolution images were taken with a JEOL 200 CX microscope.

C. Results

The surface chemistry and structure of substrates after surface preparation were monitored with XPS and LEED, respectively. After chemically cleaning the substrates in a solution of ethanol, HF, and deionized water for 10 min., XPS results showed a Si 2p peak at approximately 101 eV (Figure 3), indicative of Si to C bonding in SiC [15-17]. No Si-O bonding, which has been reported at 102.1-102.5 eV [15], was detected in the signal. Other than a shift attributed to sample charging, the Si peak remained essentially the same after a 700°C desorption for 15 min. On the other hand, a C 1s peak at 285 eV present initially was removed after the desorption. This change indicates the desorption of adventitious C (i.e. hydrocarbons), while the major peak remained at 283.5 eV, as expected for C to Si bonding in SiC [15-19].

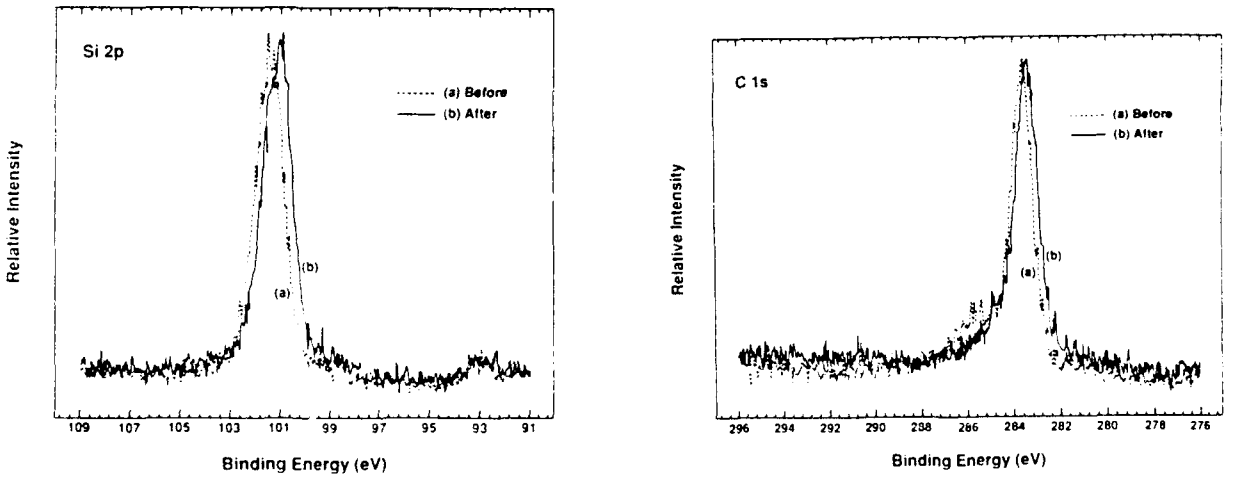

Figure 3. XPS spectra of (0001) 6H-SiC epitaxial layer after 10 min. in ethanol /HF/ deionized water (10:1:1) mixture; a) before thermal desorption, b) after 700°C desorption for 15 min.

Surface structure before and after desorption also has been monitored. LEED patterns show a sharp 1×1 pattern in all cases. Figure 4 shows a representative pattern of a (0001) 6H-SiC epitaxial layer which had been through both the described chemical clean and thermal desorption.

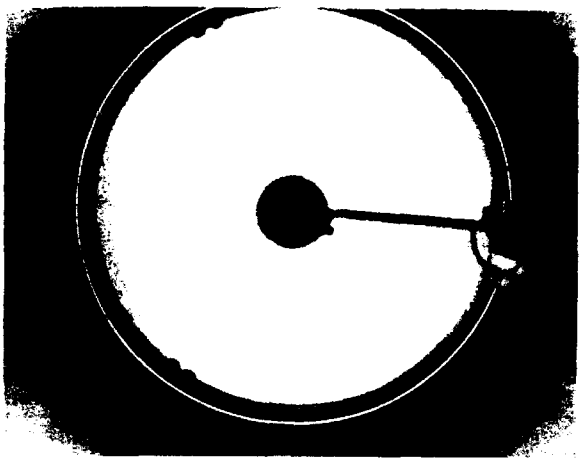

Figure 4. LEED pattern of 6H-SiC after ethanol/HF/DI water (10:1:1) clean plus 700°C desorption for 15 min.

It might be inferred by comparison with a LEED pattern taken of a 500Å Ti layer deposited on an unheated 6H-SiC substrate (Figure 5) that the Ti layer has the same crystal structure as the substrate. In addition, the LEED pattern remained the same through annealing to 900°C in 100°C increments for 10 min. at each temperature. Both Ti (a = 2.95 Å, c = 4.68 Å) and 6H-SiC (a = 3.08 Å, c = 15.11 Å) have hexagonal crystal structures, corresponding to a 4% lattice mismatch in the (0001) basal plane. The consistent 1×1 pattern of these Ti films indicates that growth has occurred epitaxially.

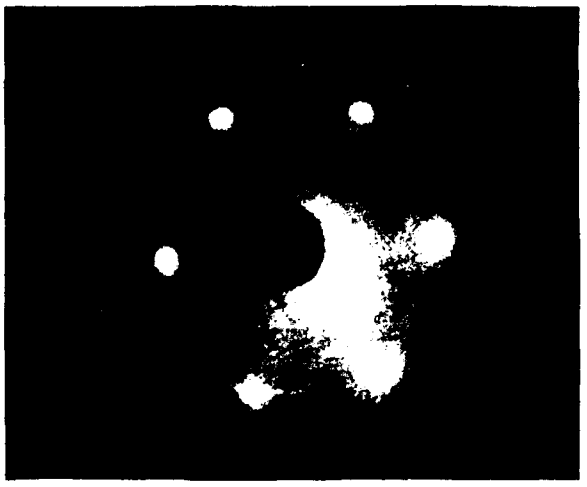

Figure 5. LEED pattern of (500 Å) Ti deposited at room temperature on (0001) 6H-SiC.

Figure 6 shows RBS with channeling spectra of a Ti film on a 6H-SiC substrate. The calculated value of χ, the ratio of the backscattered yield when the substrate is aligned along a channeling direction to that when the substrate is in a non-channeling (random) direction, for the non-annealed sample was 71% while that for the sample annealed at 900°C was 74%. The corresponding value of χ for the SiC near the substrate surface was 6%.

Samples were prepared in cross-section for subsequent TEM analysis. In Figure 7 selected area diffraction patterns of a Ti/SiC interface region is shown. A 900 Å titanium film was deposited on a bulk SiC substrate at 400°C. The diffraction patterns show a superposition of the spot pattern for the film on that for the substrate; for each orientation of the 6H-SiC [19], the Ti spots lie outside the SiC spots due to the smaller lattice parameter of Ti.

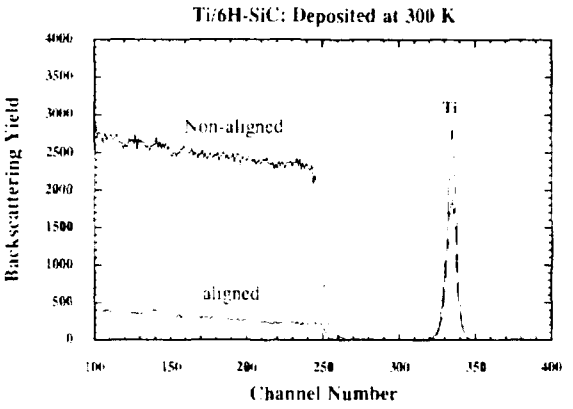

Figure 6. RBS spectrum of Ti/6H-SiC; deposited at 300 K; $\chi = 0.71$.

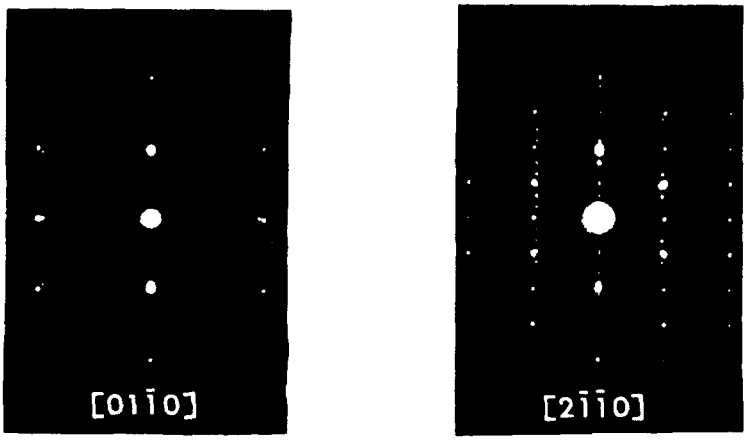

Figure 7. Selected area diffraction patterns of Ti/SiC interface region; deposited at 673 K.

Actual lattice imaging in the interface region can be seen from high resolution images (Figure 8). The 6-layer periodicity in the SiC meets the 2-layer periodicity of the Ti at a non-atomically smooth interface. Close examination of the interface reveals that there appear to be regions of lattice matching. The resulting strain in the lattice might then be relieved by threading dislocations (Figure 9).

Figure 8. HRTEM micrograph of Ti/6H-SiC; Ti deposited at 400°C.

Figure 9. XTEM micrograph of Ti/6H-SiC; Ti deposited at 400°C.

By depositing Ti onto a 6H-SiC epilayer at room temperature and annealing at 700°C for 20 minutes, a reacted layer approximately 250 Å thick has formed. However the reaction zone is too thin to show up in the selected area diffraction pattern. The pattern again shows a Ti layer in the same orientation as the SiC. High resolution microscopy is needed to see the product layer in detail. Figure 10 shows that reaction has resulted in the formation of a phase or phases with different crystal orientations.

Figure 10. HRTEM micrograph of Ti / 6H-SiC; room temperature deposition annealed at 700°C for 20 min.

Electrical characteristics of both un-annealed and annealed Ti contacts to n-type SiC (1×10^{16} cm^{-3}) were measured. Current-voltage characteristics of as-deposited Ti (curve (a) in Fig. 11) were found to be rectifying with a typical 6 nA current at –10 V. A soft breakdown began to occur at –50V, reaching a 30 μA current at –100V. After annealing in UHV for 20 min. at 700°C, the characteristics were degraded (curve (b) in Fig. 11). However, the characteristics improved again with each subsequent 20 min. anneal (curves (c) and (d) in Fig. 11).

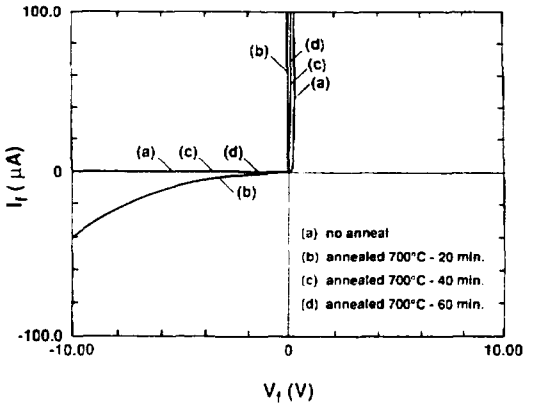

Figure 11. Current-voltage characteristics of Ti deposited on 6H-SiC epitaxial layer (20 mil diameter contact).

Notably low ideality factors for silicon carbide were calculated from plots of log I vs. V for all but the first anneal. For good Schottky diodes and values of voltage V greater than 3kT/q, the diode equation can be written as $J = Jo \exp(qV/nkT)$ [20], where J is the current density and n is defined as the ideality factor. The calculated values of n were below 1.1. No ideality factor could be calculated for the first anneal as the linear regime was too small.

D. Discussion

The combination of LEED, RBS, and TEM results, as well as knowledge of the inherent properties of the two materials, gives good indication of the crystalline nature of the Ti films. A 1×1 LEED pattern similar to that of the substrate was consistently found for the deposited films. The high value of χ (71%) determined from the RBS data may be attributed to the nature of the interface, i.e. misregistry of the film with the substrate, producing strain in the film. As shown in the TEM micrograph of Fig. 9, strain due to the 4% lattice mismatch has been at least partially relieved through the creation of threading dislocations.

However, the fact that epitaxial growth has been achieved (in addition to the deliberate surface preparation) may well be a significant factor producing the excellent electrical characteristics of the contact (Fig. 11). Knowing the workfunction of Ti to be 4.33 eV and the electron affinity of 6H-SiC to be 3.37 eV, the ideal barrier height according to the Schottky-Mott limit is calculated to be 0.95 eV. This result is in qualitative agreement with the rectification behavior observed. Leakage currents on the order of nA were typically found, and correspondingly low ideality factors (1.02 – 1.08) were calculated. Further work will need to be done to determine if reliable barrier heights can be calculated from the I/V characteristics. Richardson's constant will need to be determined from I/V measurements as a function of temperature. Furthermore, log I vs. log V data in the low voltage regime is needed in order to be sure that the current behaves according to thermionic emission theory [20].

Future work is also anticipated in the identification of phases formed in Ti/SiC diffusion couples. A reaction path in which TiC_{1-x} particles form in a matrix of Ti_5Si_3 has been reported [21]. Once phases have been identified, the electrical characteristics on annealing could be attributed to the new product phases formed.

E. Conclusions

A cleaning process for (0001) 6H-SiC has been established which leaves little or no SiO_2 and an unreconstructed surface. Epitaxial growth of Ti on these surfaces at room temperature has been confirmed by LEED, RBS, and TEM. The 4% lattice mismatch is at least partly relieved by the creation of threading dislocations. It seems probable that both the cleaning process and the epitaxial structure of the film have helped produce the excellent rectifying characteristics observed for both un-annealed and annealed contacts. The identification of phases formed on annealing and determination of barrier heights from I/V measurements have been identified as key issues and are currently being investigated.

III. Modeling and Characterization of Electronic Devices Fabricated from SiC (Trew–NCSU)

A. Introduction

Wide bandgap semiconductors such as SiC have the potential to be useful for the fabrication of electronic devices that can operate at high temperature and high power levels in corrosive environments. The high saturation velocity of electrons in SiC indicate that this material should be useful for microwave and millimeter-wave devices. The relatively low electron mobility of this material, however, restricts possible device applications to device structures that minimize parasitic resistances. Much of the device potential for SiC is predicted by figure-of-merit calculations that indicate the potential for superior performance in comparison with traditional semiconductor materials such as Si and GaAs. The figure-of-merit calculations, however, only give a preliminary and approximate indication of the performance potential of devices fabricated from SiC. More detailed information is available from physical device simulators that can predict the dc and RF potential of the devices from material, device design, and operating condition information.

In this report, a physical device simulator for the IMPATT diode is used to examine the microwave and millimeter-wave potential of IMPATT devices fabricated from SiC. The RF performance and design tradeoffs are reported. It is found that SiC IMPATT diodes are capable of RF output power in excess of that available from Si or GaAs devices up to frequencies approaching 100 GHz. The dc to RF conversion efficiency of SiC IMPATTs, however, is quite low, generally less that about 5%. The low conversion efficiency will most likely severely limit the use of SiC for fabrication of these devices. A SiC IMPATT could, however, be useful in high temperature or highly corrosive environment applications.

B. Investigation Procedure

A large-signal, numerical model for the IMPATT diode was used for this investigation. The simulator is based upon solutions to the semiconductor device equations and is, therefore, based upon physical device operation. The simulator has previously been used to predict the microwave performance of Si and GaAs IMPATT diodes and has produced results in excellent agreement with experimental data. For this work the simulator was modified to allow for the investigation of SiC. This involved alterations to the model code to allow for the high electric fields encountered within the SiC device.

For the study the charge carriers are assumed to be in equilibrium with the lattice at all times so that the Boltzmann equation reduces to the continuity equations for electrons

and holes. All transport processes in the semiconductor can then be represented by drift velocities and diffusion coefficients that are functions of the electric field. The impact ionization process is represented by ionization coefficients that are also functions of the electric field. Poisson's equation is used to relate the carrier concentrations and doping levels in the structure to the electric field. The continuity equations and Poisson's equation are solved by finite difference methods.

The model accepts data about the geometry and doping profile of the diode and with the appropriate material data, produces information about the operating characteristics of the diode. Material data files, containing information concerning carrier transport, ionization coefficients, and other basic electrical properties of a specific material, are created for each semiconductor of interest. Since the equations of the diode simulation are independent of the material being investigated, the changing to the appropriate material data file is all that is required to investigate a particular semiconductor.

Both ac and dc solutions are obtained from the model. The dc solution is provided by forcing the program to converge to a steady state with no ac component in the diode voltage. An RF voltage is impressed on the diode to provide ac solutions. The principal output data of the RF simulation are the diode admittance, efficiency, and output power. By selecting the operating frequency by means of the period of the applied RF voltage the frequency performance of the diode can be investigated. In this work the operation of IMPATTs operating from Ka (26-40 GHz) band through W-band (75-110 GHz) was investigated. IMPATT devices are seldom used below Ka band due to the superior performance available from Si bipolar transistors and GaAs MESFETs. Although IMPATTs are useful at frequencies above W-band, this study indicates that RF performance will rapidly degrade with frequency and little benefit from SiC IMPATTs will be obtained.

C. Material Properties

Silicon carbide exists in a large variety of polytypes with different structures and properties. SiC crystal structure is classified into two groups: α-SiC and β-SiC. β-SiC, the only cubic polytype, crystallizes in the zinc-blend structure. The additional hexagonal and rhombohedral polytypes, of which about 170 are known, are referred to as α-SiC. The polytypes of α-SiC differ from each other in the stacking sequence of close-packed planes and are differentiated from each other by a prefix. For example, 393R α-SiC refers to a rhombohedral polytype containing a stacking sequence of 393 layers in its primitive cell. The longest primitive cell in SiC contains 594 layers.

Some of the material properties important for IMPATT simulation have been measured for SiC, but the crystals used were often of different polytypes. It was decided

to choose one polytype for which there is extensive experimental information for evaluation with the IMPATT device model. For properties that have not been measured, a reasonable guess was made.

In this work, the polytype 6H-α-SiC is investigated due to the extensive data on electron transport and avalanche breakdown. Additionally, the epitaxial growth of 6H-SiC by LPE and VPE is well established and should be able to provide material for device applications. 6H-α-SiC is a hexagonal structure with six layers to the unit cell with a stacking sequence of (ABCA'BA') and a bandgap of 3.065 eV.

The ionization rates for avalanche breakdown are required in the simulation. In this work the rates reported by Dmitriev et. al. [22] were used. Dmitriev finds 6H-SiC to be strongly anisotropic with respect to avalanche breakdown. Epitaxial 6H-SiC is typically grown in the c direction and conventional IMPATT diode fabrication would produce devices with the electric field also in the c direction. Dmitriev finds that the process of impact ionization is decisively influenced by superstructure splitting in the conduction band and that holes dominate the carrier generation. The avalanche generation by electrons is considered insignificant. Anikin et al. [23] also find the avalanche breakdown to be anisotropic and dominated by hole generation, but believe that the avalanche mechanism involves deep level states corresponding to residual impurities and not the conduction band superstructure. A comparison of the ionization rates for several semiconductors are shown in Figure 12.

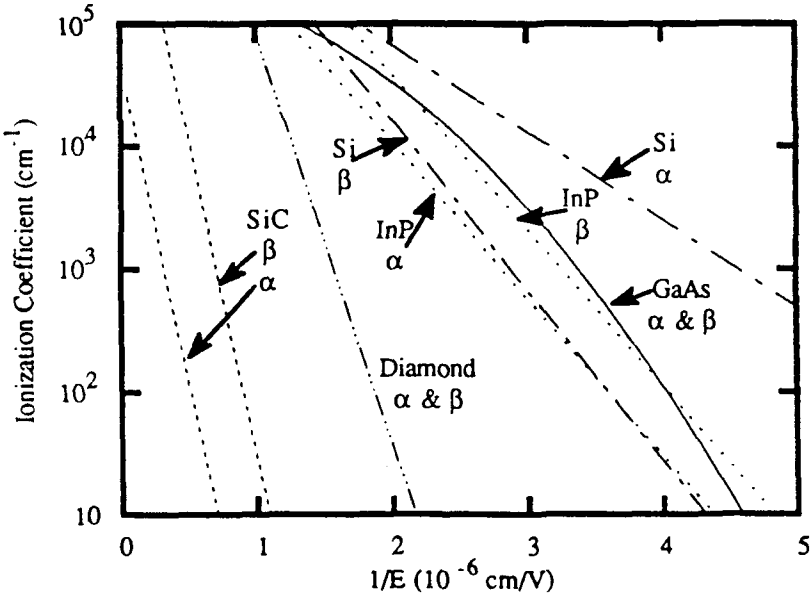

Figure 12. Ionization rates versus electric field for several semiconductors.

Experimental velocity-field characteristics for SiC have been reported [24,25]. The velocity-field characteristics for both electrons and holes for several semiconductors are compared in Figs. 13 and 14, respectively. The saturation velocity for 6H-SiC is 2×10^7 cm/s at room temperature for nitrogen doped SiC with an electron concentration of 10^{17} cm^{-3}. The saturation velocity for electrons in SiC exceeds that of Si, InP and GaAs and suggests that SiC would be superior as a high frequency semiconductor. The electron low field mobility for an impurity concentration of 10^{17} cm^{-3} is 250 cm^2/V-sec. The low field mobility for holes is between 40 and 60 cm^2/V-sec for a carrier concentration of 5×10^{15} cm^{-3}, but hole saturation velocity is still undetermined due to the large electric field required to achieve velocity saturation. The saturation velocity for holes in SiC is estimated to be 5.4×10^6 cm/sec. This approximate value allows the holes and electrons to saturate at the same electric field. While the saturation velocity for holes in SiC could be taken as equal to that of electrons, the electric field necessary for saturation to occur would be 3 to 4 times greater. In an IMPATT diode, where carriers move across the active region at the saturation velocity, the minimum electric field could exceed 1 MV/cm.

Due to the lack of information regarding the diffusion coefficients in SiC, the Einstein relationship is used to calculate the diffusion coefficients from the mobility measurements. A constant value for the diffusion coefficients is assumed. The SiC material parameters used in the simulation are listed in Table I.

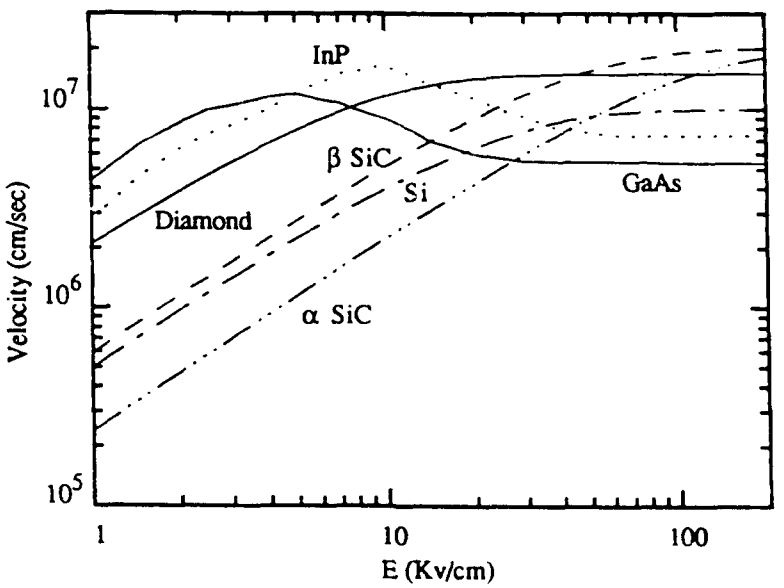

Figure 13. Electron velocity vs. electric field for several semiconductors at Nd=10^{17} cm^{-3}.

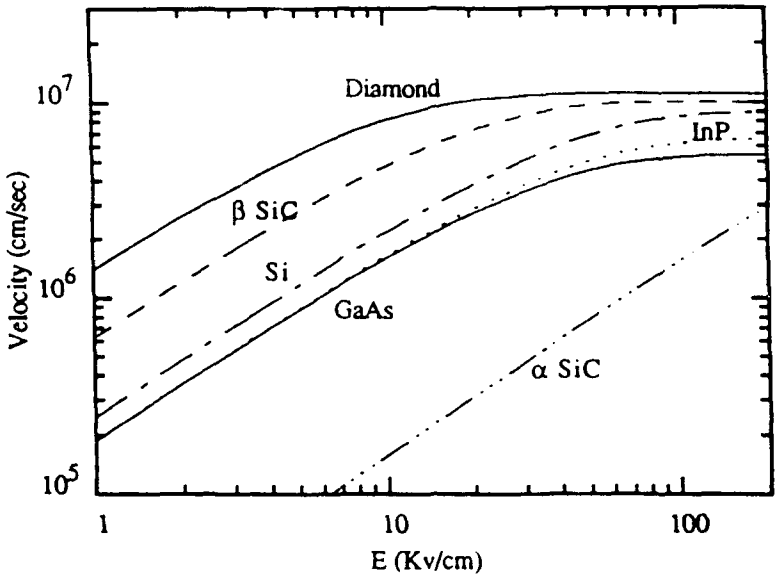

Figure 14. Hole velocity versus electric field for several semiconductors at Nd=10^{17} cm^{-3}.

Table I. Material Parameters for 6H-SiC

Material Parameter	Value
Hole Mobility (μ_p)	50 $cm^2/V\text{-}s$
Hole Saturation Velocity (v_{psat})	5.4 x 10^6 cm/s
Hole Diff. Coeff. (D_p)	0.55 cm^2/s
Electron Mobility (μ_n)	250 $cm^2/V\text{-}s$
Electron Saturation Velocity (v_{nsat})	2.0 x 10^7 cm/s
Electron Diff. Coeff. (D_n)	9.88 cm^2/s
Ionization Constants (α_p) (α_n) ($b_{n,p}$) m (See equation 5.37)	 4.65 x 10^6 cm^{-1} 4.65 x 10^6 cm^{-1} 1.2 x 10^7 V/cm 1

D. Results

IMPATT diodes with a double-drift structure were simulated. The double-drift structure is commonly used for mm-wave devices since electrically it operates as two

diodes in series. The benefits include increased RF impedance and easier matching to the RF circuit. Also, the double-drift structure produces increased RF output power compared to a single drift device. The dimensions and impurity concentrations of the SiC diodes for operation at 35, 44, 60, and 94 GHz are indicated in Table II.

Table II. Optimized Device Designs for SiC Double Drift IMPATT Diodes at Various Frequencies

Freq. (GHz)	p-doping 10^{17} cm^{-3}	p-width μm	n-doping 10^{17} cm^{-3}	n-width μm
35	1.50	1.00	0.63	2.30
44	1.80	0.90	1.00	1.70
60	2.20	0.75	1.15	1.40
94	2.50	0.60	1.50	1.10

The dc solution for a 35 GHz SiC device reveals the internal operation of the device, as indicated in Figure 15. In this figure the solid line represents the electric field inside the diode. The doping densities are indicated by the 'p' and 'n' symbols and the free carriers are indicated with '-' and '+' symbols for electrons and holes, respectively. The region of avalanche is indicated at the top of the figure by the vertical solid lines. The length of the line indicates the strength of the avalanche (i.e., where the avalanche ionization is the strongest). Note that the avalanche region is essentially confined to the p-type material and that little ionization occurs in the n-type material. This indicates that the p-type material is operating as a cathode and is supplying the charge that is injected into the n-type material drift region. For optimum operation the electric field in the n-type drift region should be above the saturation field so that the charge carriers travel at the saturated velocity. If velocity saturation is not maintained the external current will decrease when the velocity of the charge carriers is decreased and the current phase delay will be reduced.

Figure 16 shows the RF voltage and current waveforms for a 44 GHz SiC IMPATT diode with an RF voltage of 80 v. This RF voltage is about 20% of the dc voltage that is applied to the SiC diode (Vdc = 440 v). For materials such as GaAs, the optimum RF voltage that can be supported by the diode are than 50% of the dc voltage. When the RF voltage is increased for the SiC device, the limitations due to the low mobility of the holes

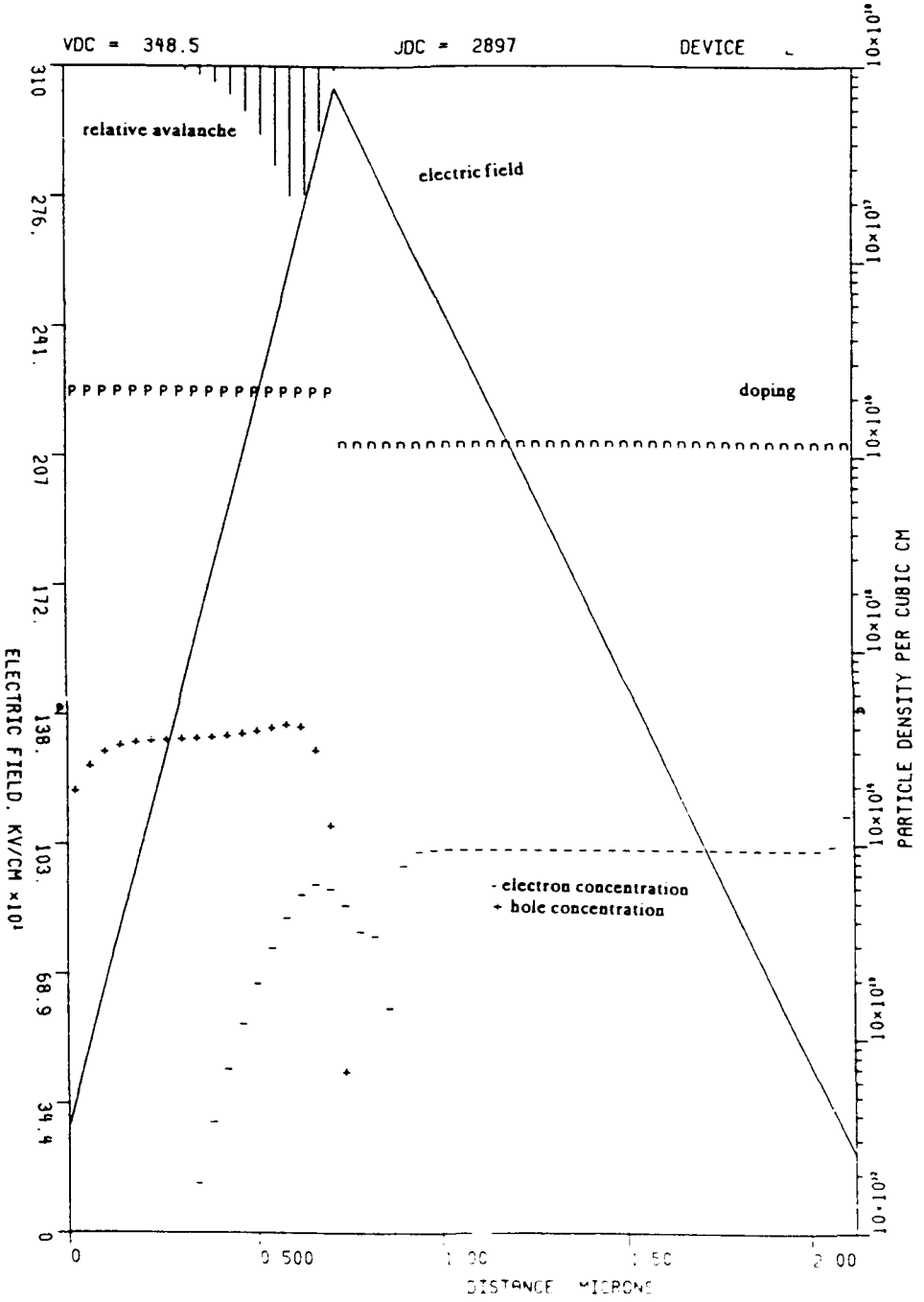

Figure 15. DC solution for a 35 GHz SiC IMPATT diode.

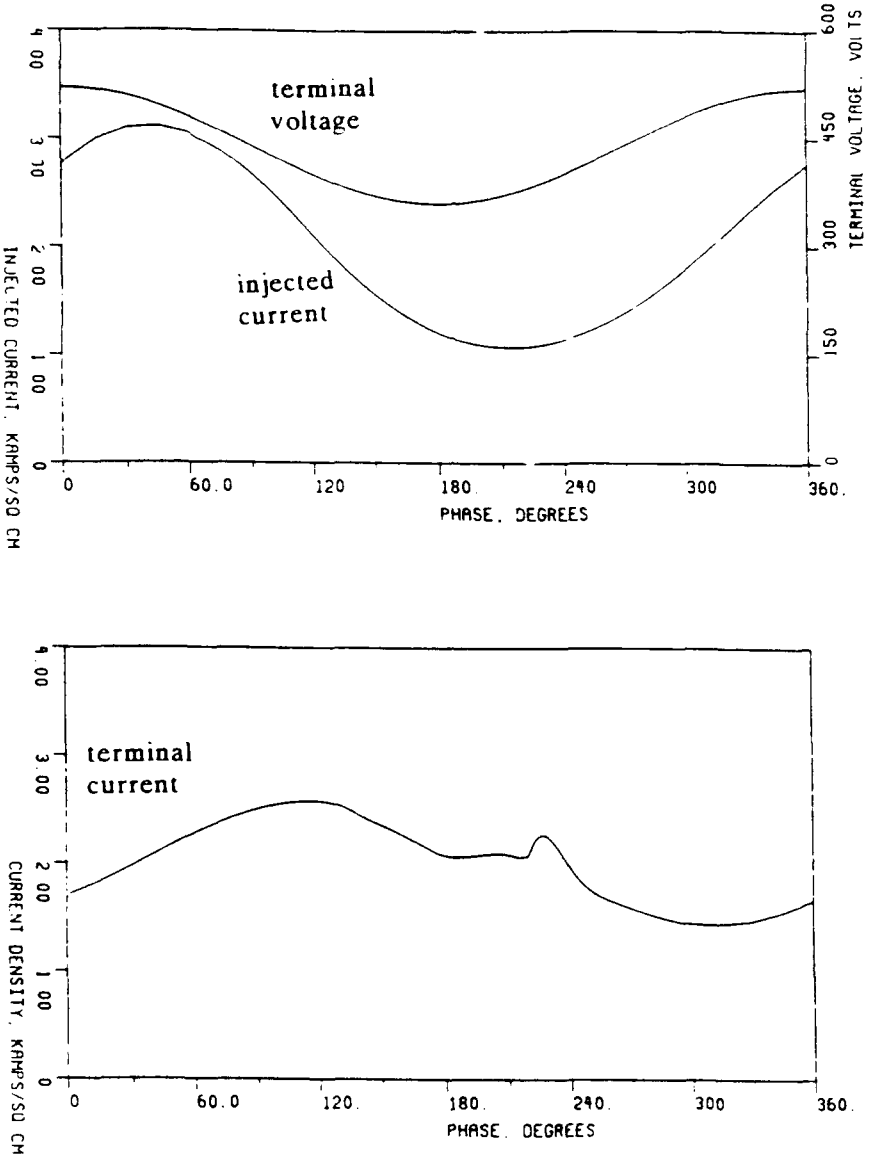

Figure 16. Terminal RF voltage, injected current, and terminal RF current waveforms for a 44 GHz SiC IMPATT diode.

become apparent. Figure 17 shows the terminal current and voltage waveforms for the 44 GHz SiC IMPATT with RF voltages of 80, 110, and 130 v. As the magnitude of the RF voltage is increased, there is a drop in the terminal current near 180 degrees. This occurs because terminal voltage has dropped to its minimum at 180 degrees and the electric field has fallen below the level necessary to maintain the charge carriers at their saturated velocity. As the terminal voltage increases, the electric field rises and the terminal current rises again. It is the low field mobility of holes that limits the magnitude of the RF voltage that can be supported by SiC IMPATTs.

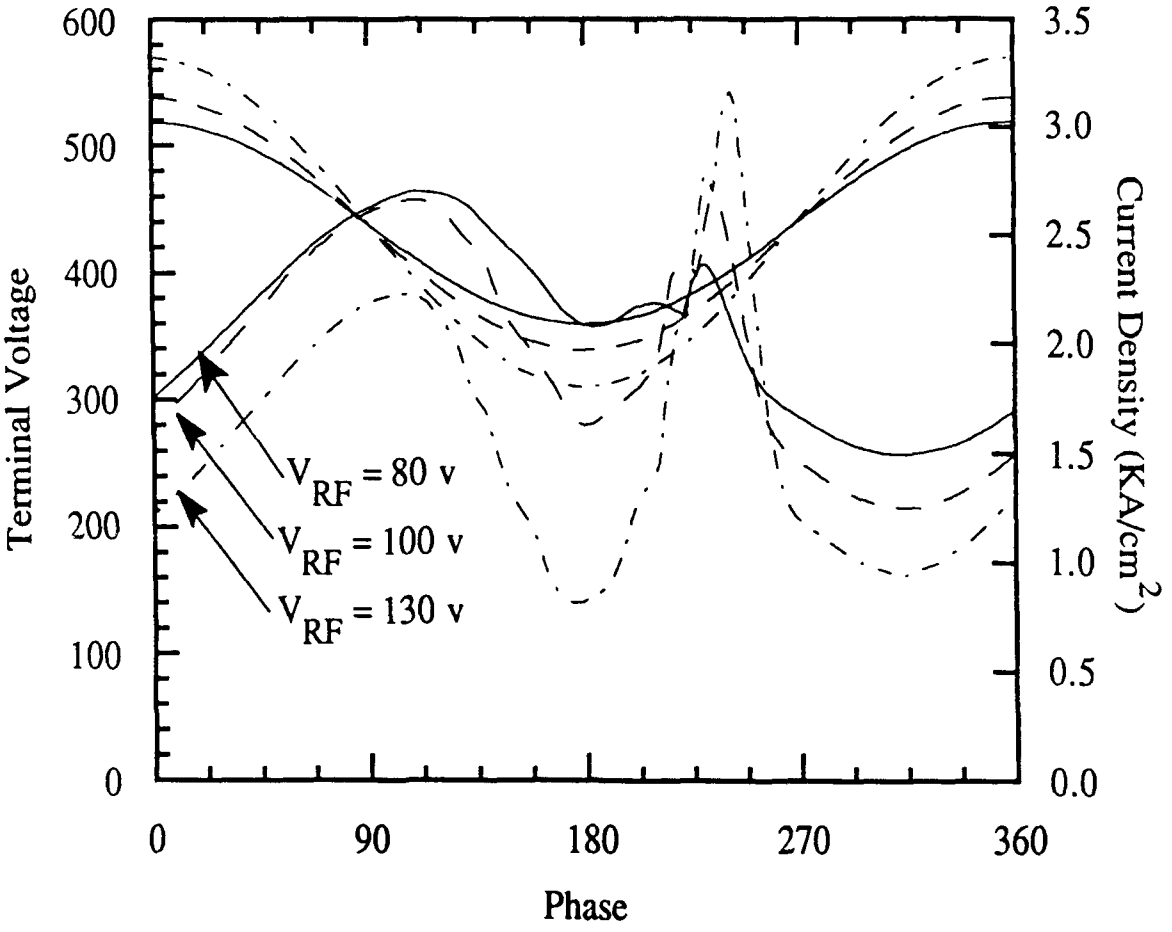

Figure 17. Terminal RF voltage and current vs. phase angle for the 44 GHz SiC IMPATT diode for terminal RF voltages of 80, 110, and 130 v.

The operating conditions and RF performance of the SiC IMPATTs are indicated in Table III. At least two operating bias currents are indicated for each diode. The diode area was designed with consideration of both device impedance matching and thermal resistance limitations. As indicated, good RF output power is available. For example, at 35 GHz 1.5 W RF power can be obtained, although the dc to RF conversion efficiency is only 1.7%. At 94 GHz 0.54 W RF power can be obtained at an efficiency of 1.1%. A comparison of the RF output power versus frequency capabilities of IMPATT diodes fabricated from several materials is compared in Figure 18.

E. Conclusions

The microwave and mm-wave RF operation of SiC IMPATT diodes was investigated by means of a large-signal, numerical IMPATT diode model. The simulator is physics based and allows the operation of the device to be determined as a function of material

Table III. SiC Diode CW Performance

Freq. (GHz)	Area (cm^{-2})	J (kA/cm^2)	I (mA)	V_{dc} (V)	P_{RF} (W)	η (%)
35	$5.0x10^{-5}$	4.0	200	512.4	1.50	1.7
35	$2.0x10^{-5}$	6.0	120	517.2	0.80	1.6
44	$6.0x10^{-5}$	4.0	240	436.9	1.78	1.8
44	$1.5x10^{-5}$	8.0	120	425.6	0.94	2.1
44	$2.0x10^{-6}$	15.0	30	426.2	0.36	3.2
60	$4.5x10^{-5}$	3.0	135	355.9	0.29	0.6
60	$6.0x10^{-5}$	5.0	300	352.1	1.98	1.88
60	$1.5x10^{-5}$	8.5	128	372.7	2.03	4.28
94	$2.0x10^{-5}$	10.5	210	243.1	0.54	1.1
94	$1.5x10^{-6}$	28.6	43	236.3	0.30	3.0

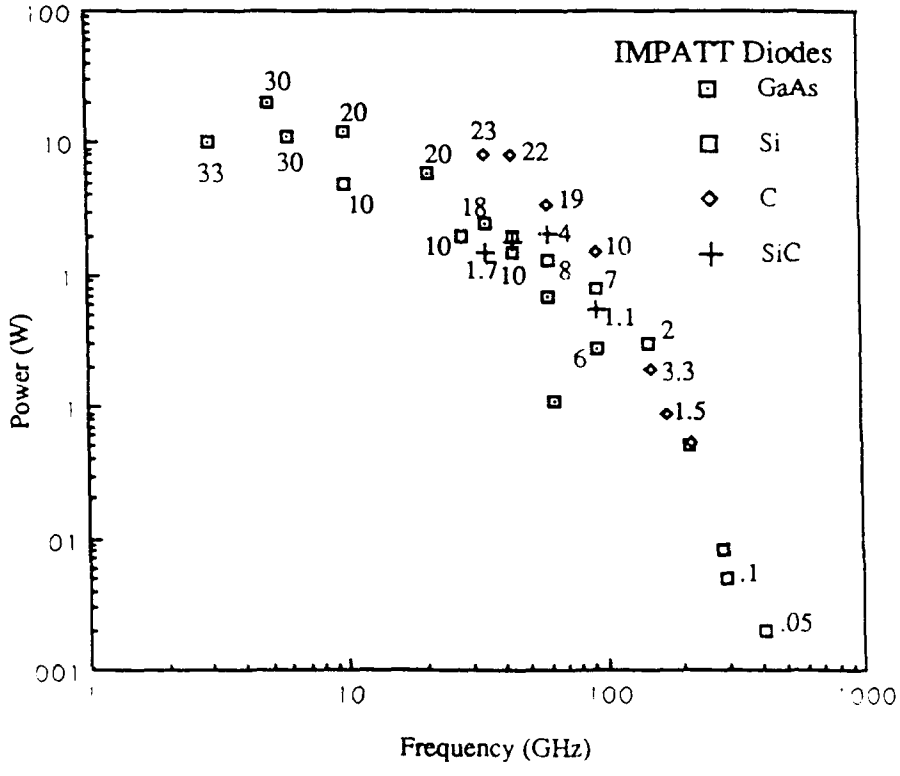

Figure 18. RF output power versus frequency for GaAs, Si, InP, diamond (C), and SiC IMPATT diodes. The numbers represent the DC-to-RF conversion efficiency (%).

characteristics, doping details, and dc and RF operation conditions. The simulator has previously been used to investigate the operation of devices fabricated from Si, GaAs, and InP and yields results in excellent agreement with experimental data. For this investigation the simulator was modified to investigate the performance of SiC devices.

The results of the investigation that SiC IMPATT diodes can operate with good RF output power in the frequency range from 30-100 GHz. The high breakdown voltage of SiC allows large RF voltages to be developed. The high breakdown voltage, however, places a current limitation upon the device operation and thereby restricts the maximum RF power obtainable. Also, the large RF voltage swing allows the internal electric field to drop below the saturation value where charge transport is restricted by the low magnitude of low field mobility. This phenomenon is difficult to avoid and results in low dc to RF conversion efficiency. The investigation indicates that conversion efficiency greater than 10% will be very difficult to achieve. In the simulations performed here, conversion efficiency greater than 5% was not observed.

F. Future Research Plans and Goals

The low efficiency obtainable from SiC IMPATT diodes appears to place a fundamental limitation to the RF operation of these devices. For this reason it is concluded that these devices will not be competitive with other solid state sources. The work completed will be published and no future work on IMPATTs is currently planned. Future work will concentrate on the design optimization and performance investigation of the SiC MESFET devices. In particular, the operation of these devices operating under high efficiency modes such as class B conditions will be investigated. Also, factors affecting gate leakage will be investigated. Experimental characterization work on fabricated devices will be continued.

IV. Fabrication and Characterization of SiC Devices for Microwave Applications (Palmour–Cree Research, Inc.)

A. Introduction

High frequency MESFET devices were reported in the previous period that showed, for the first time, significant power gain in the microwave frequency range. The best values of F_t and F_{max} that were reported for these devices were 2.9 GHz and 1.9 GHz, respectively. At 1.0 GHz, the device had a power gain of 7.0 dB and a current gain of 8.5 dB. In the last report, the effect of gate resistance as a major parasitic for high frequency operation was discussed. Preliminary experiments showed that a large increase in F_{max} resulted from using highly conductive overlayers of gold (750 nm thick) on top of the gate

contact. It was predicted that further improvements in gate resistance would result in even higher frequency operation.

The devices discussed above were the first that were fabricated using a second iteration MESFET mask set that was designed for this project. The gate lengths were much shorter than previous devices, ranging from 0.7 - 1.0 μm, and were achieved using an excimer laser stepper. These are the first submicron gate length devices ever reported in SiC. While this decreased gate length helps overcome the low mobility of 6H-SiC by increasing the electric field under the gate, it also exacerbates the problem of gate resistance. By decreasing the gate length, the cross-sectional area of the gate overlayer is also decreased and the gate resistance is thus increased. Therefore, it was also predicted that a new method for achieving low gate resistances would have to be developed, such as the fabrication of a "mushroom" gate, which has expanding cross-sectional area above the gate.

Another factor that limited the frequency performance of the devices discussed in the previous report was a high channel resistance of 67 Ω. This was primarily due to the channel thickness being too thin, as evidenced by the -4.5 V pinch-off voltage. If the channel had been thicker, allowing a pinch-off voltage in the range of -10 V as was intended, then the source-drain resistance would have been much lower and the F_t and F_{max} would have been correspondingly higher.

Although it was not considered to be a major parasitic, the gate capacitance was also greatly reduced during the last reporting period. This was achieved primarily by changing the isolating pad for the gate contact from Si_3N_4 to SiO_2, which has a much lower dielectric constant, and by making the SiO_2 thicker (500 nm). This reduced the gate capacitance from 5.75 pF to only 1.9 pF.

The main focus of this reporting period has been to further improve the high power / high frequency behavior of 6H-SiC by fabricating high power MESFET structures using some new experimental structures that will reduce both the gate resistance and source resistance. These new structures encompass both fabrication procedures and device design. While these devices have not yet been completed, they should result in significant improvements in the high frequency characteristics of 6H-SiC MESFETs.

The other high frequency device that has been investigated is an IMPATT diode. The last report discussed the advantages of 6H-SiC IMPATT diodes fabricated using a "high-low" doping structure that would allow low voltage avalanche to occur in a heavily doped region and the avalanche current would then go through a lower doped drift region. These "high-low" structures were fabricated using both a pn junction diode and a Schottky diode. Although the doping was not in the proper range to achieve low voltage avalanche

in the p-n junction high-low structures, the leakage currents were very low up to biases >100V, which was encouraging. On the other hand, the Schottky high-low structures showed relatively good avalanche characteristics. One device with a diameter of 102 μm withstood more than 40 mA of avalanche current at 59 V, which corresponds to an avalanche power density of 29 kW/cm^2. While these characteristics were promising, the measured contact resistance of the Schottky contact was unfortunately high. A contact resistivity of 8×10^{-4} Ω-cm^2 was measured on these devices. This resistivity is considered to be too high for efficient operation at 60 GHz, and therefore the focus for IMPATT diodes has been shifted to high-low structures using p-n junctions. Excellent results have been obtained during this period with the p-n junction structures, with low leakage currents, avalanche energies as high as 124 kW/cm^2, and negative conductances in the range -348 mhos/cm^2.

B. Experimental Procedure

High Power / High Frequency MESFETs. The substrates used for this study were sliced from 6H-SiC single crystal boules. The boules were lightly nitrogen doped n-type. The boules were then sliced, lapped and polished into wafers suitable for epitaxial growth. Thin films of monocrystalline 6H-SiC (0001), both p- and n-type, were epitaxially grown on these n-type 6H-SiC (0001) wafers. The MESFETs consisted of a thick p-type epitaxial layer of 6H-SiC having a carrier concentration in the range of 1×10^{15} - 1.5×10^{16} cm^{-3} and a thickness ranging from 2.0 -7.0 μm grown on the n-type 6H-SiC substrate. This p-type layer acted as the buried layer to confine the current to a thin n-type active region which was subsequently grown. This top n-type epitaxial layer had carrier concentrations in the range of 0.9 - 3.0×10^{17} cm^{-3}. For some of the devices the thickness of this layer ranged from 0.25 to 0.34 μm depending on the doping and desired pinch-off voltage of the device. For devices that were grown for recessed gate experiments to be discussed later, the thickness of this layer was made thicker, ranging from 0.49-0.57 μm.

The design for the high power-high frequency SiC MESFET is shown in Figure 19. This design uses a 1 mm gate width consisting of two 500 μm long gate fingers. The gate lengths used on this mask vary from 0.6 μm to 1.0 μm. The gate - drain spacing is 1.5 μm and the source - gate spacing was about 1 μm for all of the devices except the smallest gate length, which had a 0.5 μm spacing.

Two methods for forming the n$^+$ source and drain areas were used. One batch of wafers used ion implantation of N$^+$ into the n-channel layer to form n$^+$ wells. The other method that was used involved the growth of a third epilayer that was subsequently patterned and etched to form n$^+$ mesas. This layer typically had a thickness of 0.2 μm and

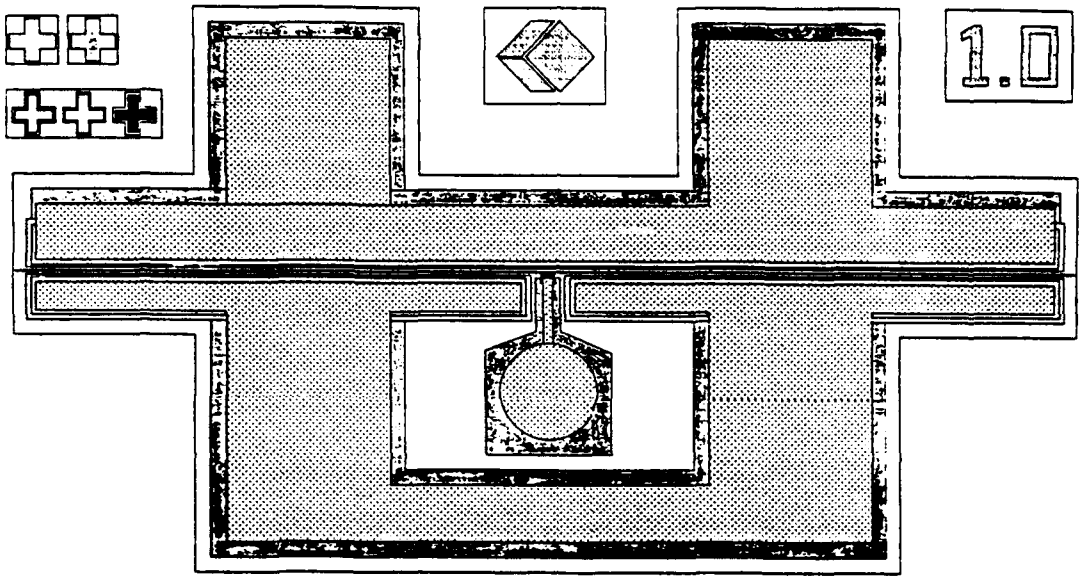

Figure 19. Design for high power, high frequency SiC MESFET. Gate lengths vary from 1.0 μm to 0.6 μm, and source-to-drain distances vary from 3.5 μm to 2.9 μm. The gate width is 1 mm.

a doping of 1×10^{19} cm^{-3}. The fabrication of the different wafer lots has been somewhat similar up to the step that they are currently; the procedures were as follows. The entire device was first isolated on a mesa. Using conventional photolithography techniques, a sputtered aluminum film was patterned onto the SiC surface, which acted as a mask for the reactive ion etching (RIE) of the isolation mesa. The material around the mesa was etched deeply enough to penetrate through the top n-type layer into the buried p-type layer. The Al was then stripped.

For the ion implanted wafers, polysilicon was deposited and patterned, opening windows for the source and drain pattern. The samples were then ion implanted with N^+ to form n^+ source and drain wells, using the polysilicon as the implant mask. The implants were subsequently annealed at high temperature. For the wafers with the n^+ epilayer on them, aluminum was deposited and patterned to mask the n^+ material for the source and drain. The exposed n^+ SiC was then etched away using RIE, to the desired depth in the n-channel layer, leaving n^+ source and drain mesas.

All of the samples were oxidized to grow a thin passivating layer of SiO_2. A thick layer of SiO_2 (≈1 μm) was then deposited, using a low temperature chemical vapor deposition process, over the thin thermal oxide and was patterned to form the center gate contact isolation pad and interconnect bars. Windows for the source and drain contacts were then opened in the SiO_2 and the ohmic contacts were deposited and patterned using the "lift-off" technique.

These ohmic contacts are currently at the annealing stage, after which the fine line gate Schottky contacts will be patterned using an excimer laser stepper (GCA ALS LaserStep 200) at the Microelectronics Center of North Carolina. It is at this stage that a number of different fabrication procedures will be attempted in order to obtain both a recessed gate and/or a mushroom gate. Finally, the gate contact pad metallization will be deposited and patterned on the SiO_2 isolation pad.

IMPATT Diodes. All of the IMPATT diodes that were fabricated during this reporting period used the "high-low" design for low voltage avalanche and were p-n junction based. These devices had the epitaxial structure for the breakdown layers as shown in Figure 20. The starting substrates were n-type that were doped with nitrogen so that n = $1\text{-}3\times10^{18}$ cm^{-3}. The first epilayer, which served as the drift layer, was then grown with a thickness of 1.2 μm and a carrier concentration of $2.3\text{-}3.3\times10^{16}$ cm^{-3}. This layer was followed by a more heavily doped avalanche layer with a thickness of 0.22 μm and carrier concentration of $6\text{-}8\times10^{17}$ cm^{-3}. Finally, the p-n junction IMPATT wafers had a p^+ layer grown on them that was 0.5 μm thick and had a carrier concentration of p = $4\text{-}14\times10^{18}$ cm^{-3}.

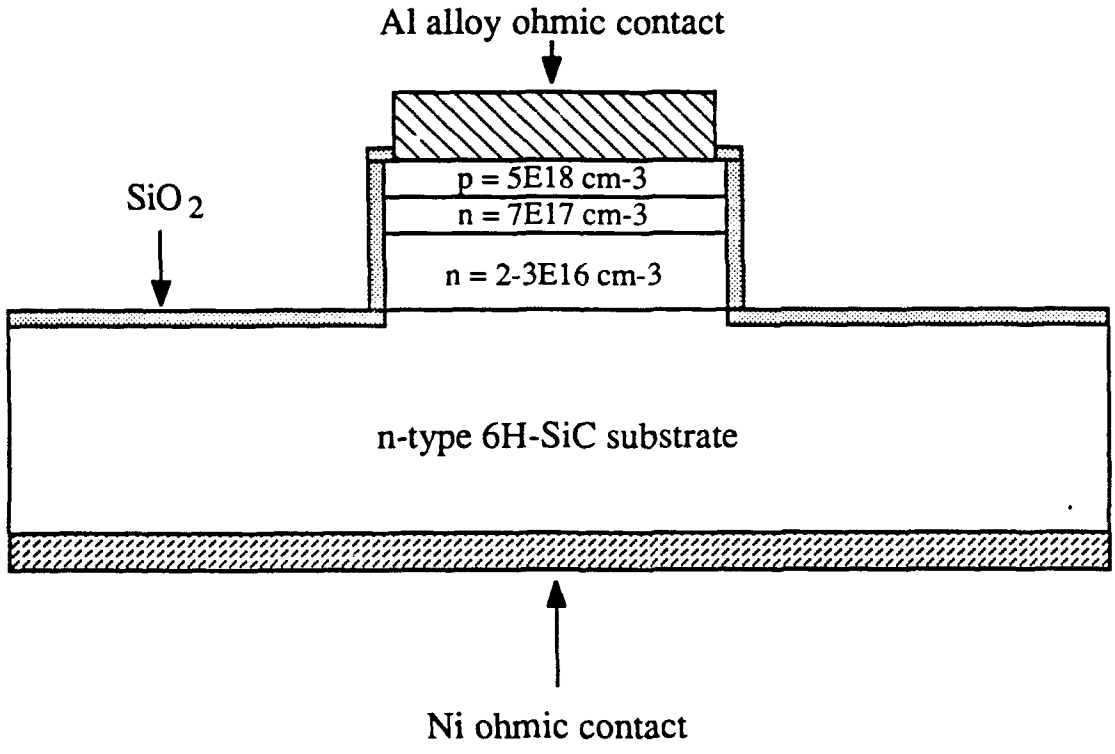

Figure 20. Cross-sectional view of p-n junction "high-low" IMPATT diode structure in 6H-SiC.

The device fabrication for the IMPATT diodes involved first lapping the wafers to a thickness in the range of 150-200 μm thick by diamond grinding the backside of the wafers. The diode mesas were then formed via reactive ion etching using Al as the mask material. The mesas were etched through the epilayers into the n^+ substrate. The samples were then oxidized in wet O_2 to form a passivating layer of oxide on the mesa sidewalls. Using photolithography, windows were etched in the oxide for the topside ohmic contacts. The topside contacts were then formed on the front and backside of the wafer as shown in Figure 20. Seven different diameter dots, varying from 38.1 μm to 381 μm, were used in order to find the device area that yielded the best impedance matching.

C. Results and Discussion

High Power / High Frequency MESFETs. Three batches of high frequency MESFETs were initiated in this reporting period. The efforts on these devices were focused on reducing the two parasitics discussed earlier, source resistance and gate resistance. While all three of these batches are far along in their processing, none of them is finished at this time. As such, the device structures that are being attempted will be discussed in this section. Additionally, some initial experiments on packaging the MESFETs fabricated in the last reporting period for RF power measurements were initiated and will be discussed.

The DC current-voltage plot in Figure 21 shows a 6H-SiC MESFET device with source and drain mesas, fabricated during the last reporting period, that had a gate length and width of 0.7 μm and 1 mm, and a gold overlayer of 750 nm. This device showed good current saturation out to 35 V and a non-destructive breakdown of the SiC at V_D = 37 V. The maximum current for this device was only 50 mA because the channel thickness was not as thick as it should have been, as evidenced by the pinch-off voltage of V_G = -4.5 V and the measured source-drain resistance of 67 Ω. The maximum transconductance of this device was 19 mS/mm at V_G = 0 V. Using a Cascade Microprober, the F_t and F_{max} of this device were measured to be 2.4 GHz and 1.9 GHz, respectively, and the power gain at 1.0 GHz was 7.0 dB.

Had the channel thickness of this device been thicker, or the channel doping heavier, allowing a pinch-off voltage of about -10 V, the power gain and F_{max} would have been much higher because the source resistance would be much lower. Therefore, a new batch of "mesa-style" MESFETs were grown with higher channel doping in the range of $1.5\text{-}3.5\times10^{17}$ cm^{-3}. These devices are being fabricated in a similar fashion to those described in the last report, with the exception of using a thicker gold overlayer (1 μm will be attempted) to reduce gate resistance and a thicker isolating SiO_2 layer (1 μm) to reduce gate capacitance.

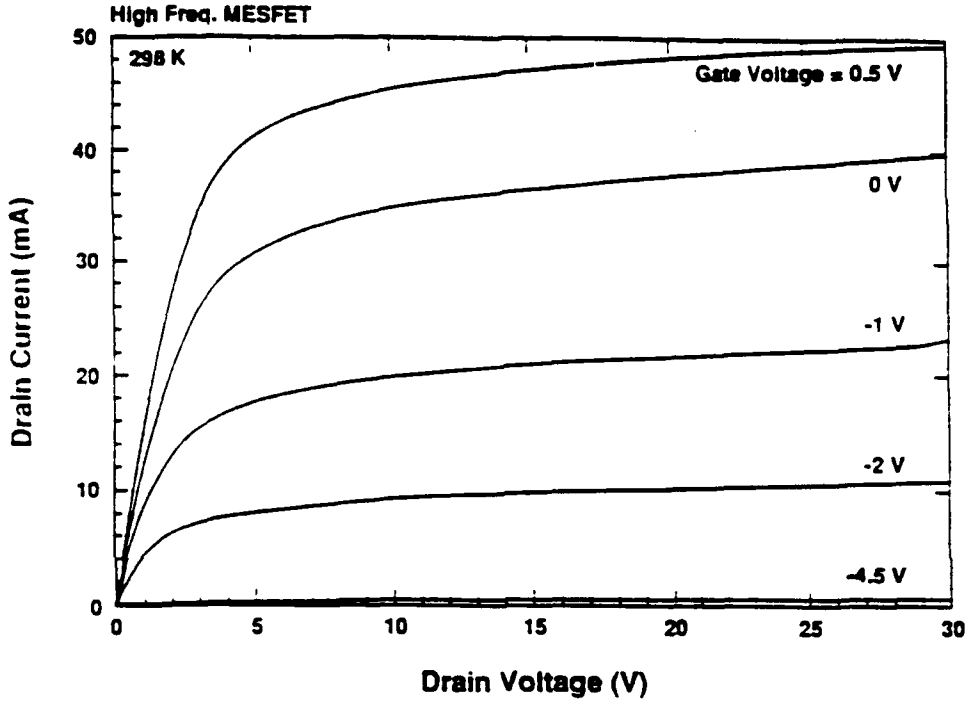

Figure 21. Drain current-voltage characteristics of a 6H-SiC MESFET. The gate length and width were 0.7 μm and 1 mm, respectively. Source-drain distance was 2.1 μm. The maximum transconductance was 19 mS/mm. The gold gate overlayer was 750 nm thick.

Experiments performed in this period with dummy wafers have shown that gold overlayers as thick as 1 μm can be lifted off using the current fabrication methods for photolithography and metal deposition. This should result in a 33% reduction in gate resistance. Combined with the reduced channel resistance, these improvements should allow significant improvement in the high frequency characteristics of the MESFETs.

One of the concerns with the "mesa-style" source and drain structure is that the epilayers introduce extra resistance by virtue of the longer path that is created for the electrons to get from contact to contact. Also, at present, it is easier to get higher source and drain doping using ion implantation rather than epitaxially grown layers. Higher source and drain doping would reduce the contact resistance and a shorter path from contact to contact would reduce the channel resistance. As such, a second batch of MESFETs were grown that were to have the source and drain wells ion implanted instead of epitaxially grown. These devices have been implanted and are now ready for the gate lithography. Again, these devices will also have a thicker gate overlayer that is 1 μm thick.

While these wafer batches will result in significant reductions in source resistance, a new device design is required to make a dramatic reduction in source resistance. A common method for greatly reducing the source resistance of GaAs MESFETs is to

fabricate them with recessed gates. This is a method by which the channel layer is much thicker than normal, but is thinned to the proper thickness directly below the gate, keeping the source-gate cross-sectional area much larger. This structure should be particularly important for 6H-SiC because it allows one to compensate for the relatively low electron mobility.

Therefore, a batch of wafers were grown with which to fabricate some recessed gate 6H-SiC MESFETs. Two different channel thicknesses were used for the channel layer. Three were about 210 nm thicker than required and another three were 280 nm thicker than required. These wafers have already had ion implanted source and drain wells formed and are currently at the photolithography step to form the ohmic contacts. After the contacts are formed, experiments on forming the recessed gate structure will begin. The recesses for the gates will be reactive ion etched to a depth equal to the excess thickness grown into the channel layers (210 nm and 280 nm), prior to the deposition of the gate metal.

Additionally, a method will be attempted during the gate overlayer deposition by which a mushroom style gate will be formed, meaning that the cross-sectional area of the overlayer expands above the gate. If a mushroom gate is achieved in conjunction with a recessed gate, it is expected that these devices will have significant power gain at frequencies of 10 GHz or more.

As stated earlier, an attempt at packaging some high frequency MESFETs for RF power testing was made during this reporting period. The devices were successfully diced with no degradation to the operating characteristics. Because of the high power levels that the devices would operate at, it was decided that the MESFETs should brazed to the headers (standard ceramic microwave packages) as opposed to using silver epoxy. Unfortunately, the high temperature brazing process caused severe electrical degradation of the MESFET's I-V characteristics because of damage to the gate. Therefore, no RF power measurements were performed.

While this degradation phenomenon was discouraging, it was not altogether unexpected. We have also been developing MESFETs for high temperature operation at Cree under a different contract effort, and in the course of this research it was found that the gate metal must be annealed in order to avoid this degradation effect. After annealing, the gates are very stable at high temperature. The difficulty with the microwave MESFETs is related to the fact that these devices also have a gold gate overlayer that is deposited at the same time as the gate metal. Because of the fear of degrading the contacts via gold diffusion, we have not annealed the Schottky contacts on the microwave devices.

In order to determine the effect of annealing Schottky contacts with gold overlayers, a set of wafers have been grown with n-type epilayers for making Schottky diodes. These wafers, which are also still in process, will be fabricated in to large area Schottky diodes, with and without gold overlayers. After annealing the Schottky contacts, the differences between the devices will be characterized. If degradation due to the gold layer does occur, then research will be continued on these devices, with the emphasis focused on finding diffusion barriers to place between the Schottky contact and the gold overlayer.

IMPATT Diodes. The reasons for using a high-low doping profile for the drift layer instead of the more common flat doping profile have been discussed in previous reports. The main reason was difficulty in maintaining low leakage currents at sub-avalanche voltages with the flat doping profile. Therefore, further efforts focused on using a "high-low" structure, which keeps the avalanche voltage low and decreases the sidewall passivation requirements. The potential of the "high-low" structures for IMPATT diodes in SiC have now been demonstrated.

The p-n junction high-low IMPATT structures showed very low reverse bias leakage currents as compared with previous devices. The I-V characteristics of a p-n junction high-low IMPATT diode ($A = 8.11\times10^{-5}$ cm^{-2}) shown in Figure 22 show very low reverse bias leakage current out to about -90 V followed by a sharp avalanche breakdown with a negative resistance slope. The average leakage current at V = -80 V was 80 nA; at V = -50 V, the leakage current was about 2 nA ($J = 2.5\times10^{-5}$ A/cm^2). The avalanche current of this device exceeded 105 mA, corresponding to an avalanche power density of about 120 kW/cm^2. This is a very high power density and it is expected that the junction temperature at this power level is quite high. Indeed, further increases in avalanche current began to degrade the performance of the device.

The reverse bias avalanche characteristics of a different, smaller IMPATT device are shown on an expanded scale in Figure 23. This device, which had an area of 4.56×10^{-5} cm^2, again shows very low leakage current below avalanche at about 97 V. More importantly, the negative resistance of this device can be observed as the avalanche current is increased. The maximum negative resistance of this device is about -63 Ω. This corresponds to a negative conductance of -348 mhos/cm^2. This value of conductance is similar to that normally observed for Si and GaAs IMPATT diodes, which operate within the range of 200-700 mhos/cm^2. It is important to note that this value is for a SiC diode that is not thinned (substrate is ≈200 μm thick), therefore there is a large passive resistance associated with the substrate; in addition, the contact resistance also contributes a large passive resitance component. Thus, the intrinsic negative resistance of the devices is likely to be twice as high as the measured value.

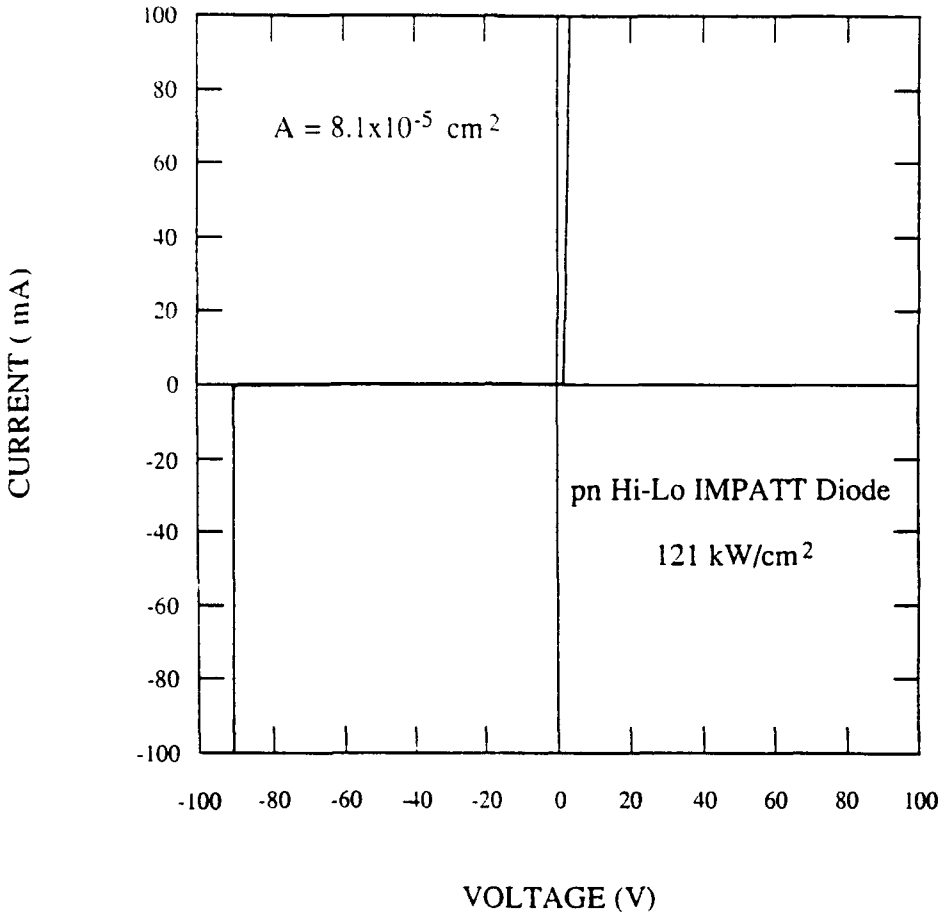

Figure 22. Current-voltage characteristics of a 6H-SiC p-n junction "high-low" IMPATT diode structure. The junction area was 8.1×10^{-5} cm^2.

The avalanche current of 59 mA at 96 V for the device shown in Figure 23 again corresponds to a very high avalanche power density of 124 kW/cm^2. Good avalanche characteristics were observed for other devices with higher breakdown voltages, showing avalanche currents as high as 5 mA at 295 V. However, this corresponds to only 15% of the avalanche power density observed for the lower voltage devices and the yield for the high voltage devices was lower also.

The forward bias I-V characteristics of the IMPATT diode shown in Figure 23 are shown in Figure 24. The diode has a turn-on voltage of about 2.6 V and has a forward current of 50 mA at about 3.5 V. Thus, the diode had a forward resistance of about 18 Ω, or 8.2×10^{-4} Ω-cm^2. Using known bulk resistivities and ohmic contact resistivities for 6H-SiC, the component of the resistance due to the substrate was calculated to be about 5.4 Ω. The p-type ohmic contact resistance was calculated to be about 9.0 Ω (2.2×10^{-4} Ω-cm^2) and the resistance due to the low doped drift region was about 3.0 Ω. Finally, the n-type ohmic contact was calculated to be about 0.6 Ω, resulting in a total

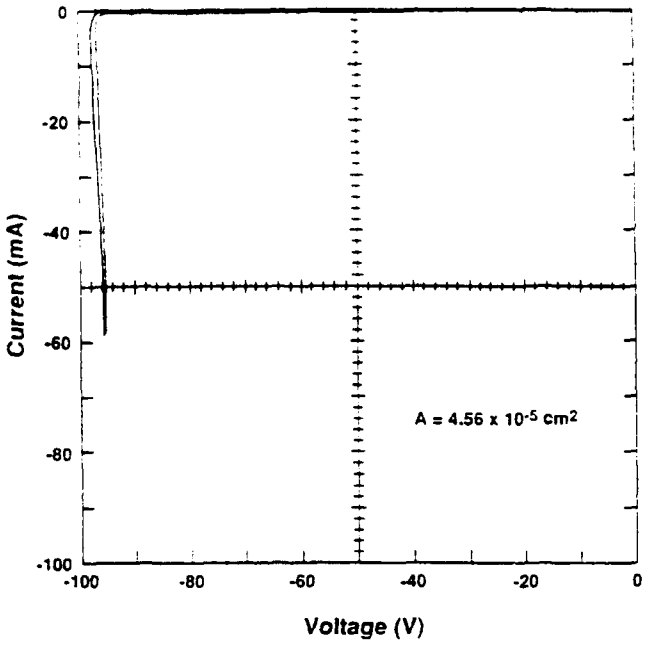

Figure 23. Reverse bias I-V characteristics of a different 6H-SiC p-n junction "high-low" IMPATT diode structure. The junction area was 4.56×10^{-5} cm^2. Note the -63 Ω negative resistance in avalanche and the 124 kW/cm^2 DC avalanche power density.

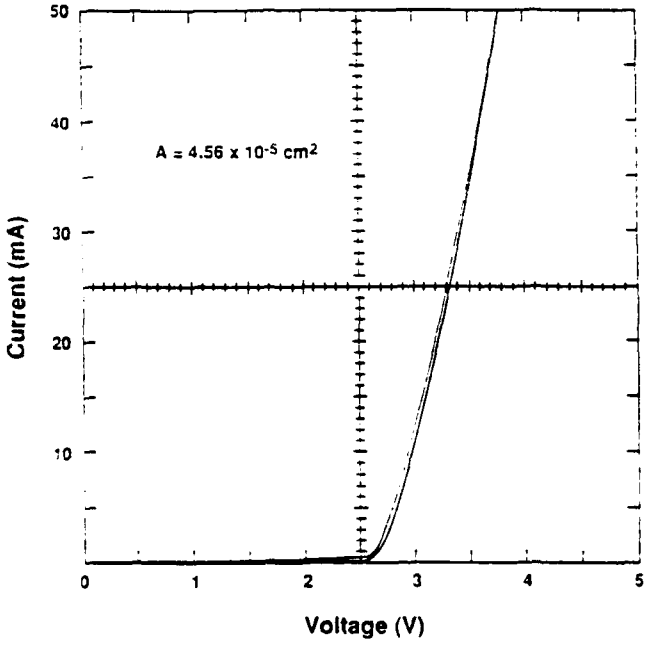

Figure 24. Forward bias I-V characteristics of the same p-n junction "high-low" IMPATT diode shown in Fig. 23. Note the 18 Ω forward bias resistance.

resistance of 18 Ω. If a 6H-SiC IMPATT diode was fabricated with a thinned substrate and backside contact vias, then the substrate resistance could be ignored. Additionally, if the carrier concentration of the p^+ layer could be increased from the 5×10^{18} cm^{-3} obtained with this particular diode to $>2\times10^{19}$ cm^{-3}, the p-type ohmic contact resistance would be reduced by a factor of about three. For similar sized devices from the same wafer lot, resistances as low as 10 Ω were measured, probably due to increased p-type concentration and higher substrate doping. Therefore, with an optimized IMPATT structure, the device resistance could be at least as low as 6.6 Ω (3×10^{-4} Ω-cm^2). Based on these results, a 6H-SiC p-n junction-based high-low IMPATT diode appears to be a promising structure for very high power microwave generation.

D. Conclusions

High frequency 6H-SiC MESFETs have been fabricated that show gain at microwave frequencies, with the highest values for F_t and F_{max} being 2.9 GHz and 1.9 GHz, respectively. The main two parasitics that are currently limiting the high frequency behavior of these devices are source resistance and gate resistance. The source resistance should be reduced by a factor of two, which will allow both higher power and higher frequency devices. The gate resistance is about 40 Ω on these devices. Ideally, this resistance should be reduced by a factor of at least four (<10 Ω).

Three different methods are being pursued to reduce the source resistance. These methods are 1) increasing the channel doping, 2) using ion implanted source and drain wells, and 3) use of recessed gate structures. Two different methods are being pursued to reduce the gate resistance. The first is to simply increase the thickness of the straight-walled gold overlayer by 33%. The second is to try to fabricate a "mushroom" style gate.

Avalanche characteristics for 6H-SiC p-n junction IMPATT diodes have been observed for the first time using a "high-low" doping structure. These devices showed avalanche power densities as high as 124 kW/cm^2. Additionally, they showed negative conductance in avalanche in the range of 348 mhos/cm^2. The forward bias resistances observed were in the range of 4.6-8.2$\times10^{-4}$ Ω-cm^2, without substrate thinning. This value is approaching an acceptable range for high power operation at 60 GHz, the intended frequency for these IMPATT diodes. Based on the observed characteristics and the opportunity for improvement, the p-n junction based IMPATT appears to be a promising structure for high power microwave operation.

E. Future Research Plans/Goals

The plans for the next period are to finish the device fabrication of the three different lots of MESFETs that are in process. These devices will then be evaluated electrically

with both DC and RF measurements. Based on the success of the experimental batches, particularly the recessed gate / mushroom gate devices, more wafer lots will be designed and fabricated.

Additionally, experiments on gate annealing with gold overlayers will be continued, so that high power, high temperature RF power measurements can be performed without device degradation. If degradation does occur during annealing, then research on diffusion barrier metals will be initiated.

Future IMPATT diodes will focus on improving the fabrication of p-n junction "high-low" structures and performing some RF power measurements. However, because of the limited funds available as the end of this contract nears, it is unlikely that any more IMPATT diodes will be fabricated under this effort. The rest of the effort on this contract will focus instead on improving the frequency range of the SiC MESFET devices.

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