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InGaAs-GaAs quantum well vertical-cavity surface-emitting laser using molecular beam epitaxial regrowth

C. Lei, T. J. Rogers, D. G. Deppe, and B. G. Streetman

Microelectronics Research Center, Department of Electrical and Computer Engineering,
The University of Texas at Austin, Austin, Texas 78712-1084

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Data are presented demonstrating a design and fabrication process for the realization of high-efficiency, low-threshold vertical-cavity InGaAs-GaAs quantum well lasers with light emission through the top (epitaxial) surface. Crystal growth is performed using a two-step molecular beam epitaxial growth process to utilize lateral current injection into the device active region. The device structure allows the top surface (emission side) reflector to be optimized (for either high efficiency or low threshold) after crystal growth through the deposition of electron beam evaporated dielectric layers. Maximum continuous-wave output power in excess of 1.2 mW at 300 K, and differential quantum efficiency greater than 25% (3.9 mA threshold) are demonstrated. Low-threshold values of 2.3 mA are measured on devices with increased mirror reflectivity (through the addition of dielectric layers).

There has been considerable recent interest in the vertical-cavity surface-emitting laser (VCSEL) due to significant advantages that this structure possesses in terms of device geometry.¹⁻⁵ The micro-cavity allows for a greatly reduced active volume and thus has the potential for ultralow-threshold currents. Light emission normal to the epitaxial surface, along with the small device area, also make it possible to realize densely packed two-dimensional arrays^{6,7} which may find applications in various future optoelectronic systems, such as optical computers and large-area high-power laser systems. Large-scale wafer testing may also reduce the manufacturing cost of VCSELs relative to lateral-cavity edge-emitting devices. Along with these device advantages from an applications point of view, the device geometry has also been suggested to play an important role in laser performance in a more fundamental way, with the closely spaced, highly reflecting mirrors becoming optically coupled to the VCSEL active region, especially for the quantum well (QW) VCSEL.⁸⁻¹⁰

Despite these advantages, current VCSEL devices still suffer from high-threshold current densities and low-power efficiencies due to limitations in mirror design, and high electrical series resistance due to poor hole carrier injection characteristics across the AlAs-(Al)GaAs heterojunctions used in the *p*-type distributed Bragg reflectors. In this letter we describe a novel VCSEL device structure designed to circumvent these problems. The device structures are realized using a molecular beam epitaxial (MBE) regrowth over a thin *n*-type current blocking layer to allow for lateral current injection into the VCSEL active region, as well as modal confinement of the photon to the lasing cavity. Low-threshold and high-efficiency laser operation is demonstrated. The structure should also be capable of reduced series resistance as compared to other VCSEL designs.

The device structures are epitaxially grown using MBE. A schematic cross section of the upper half of the device is shown in Fig. 1. The initial epitaxial layer structure consists of a $1\ \mu\text{m}$ n^+ -GaAs buffer, followed by a 21.5 pair *n*-type quarter wave stack of GaAs/AlAs, a lower

n-type $\text{Al}_{0.67}\text{Ga}_{0.33}\text{As}$ confining layer, an undoped active region consisting of two $60\ \text{\AA}$ $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ pseudomorphic QWs with three $60\ \text{\AA}$ GaAs barriers, an upper *p*-type $\text{Al}_{0.67}\text{Ga}_{0.33}\text{As}$ confining layer, one *p*-type quarter-wave pair of AlAs/GaAs, a $200\ \text{\AA}$ *p*-type $\text{Al}_{0.67}\text{Ga}_{0.33}\text{As}$ etch stop layer, and finally a $600\ \text{\AA}$ *n*-type GaAs current blocking layer. The *p*- and *n*-type $\text{Al}_{0.67}\text{Ga}_{0.33}\text{As}$ confining layers and QW active region have a total combined thickness of an optical wavelength. The *p*-type AlAs/GaAs pair is grown with an eight-period graded superlattice between the layers in order to minimize series resistance.^{2,4} The substrate temperature is reduced to $535\ ^\circ\text{C}$ for the growth of the QW active region, while the rest of the structure is grown at $600\ ^\circ\text{C}$. After initial growth the wafer is removed from the MBE system and $10\text{-}\mu\text{m}$ -diam openings are formed using standard photolithography techniques in photoresist deposited on the epitaxial side of the wafer. The $600\ \text{\AA}$ *n*-type GaAs current blocking layer is then selectively removed using an $\text{H}_2\text{O}_2\text{-NH}_3(\text{OH})$ etch with the pH adjusted to ~ 7.2 .¹¹ The exposed $200\ \text{\AA}$ $\text{Al}_{0.67}\text{Ga}_{0.33}\text{As}$ is then selectively etched using a dilute $\text{HF-H}_2\text{O}$ solution.¹²

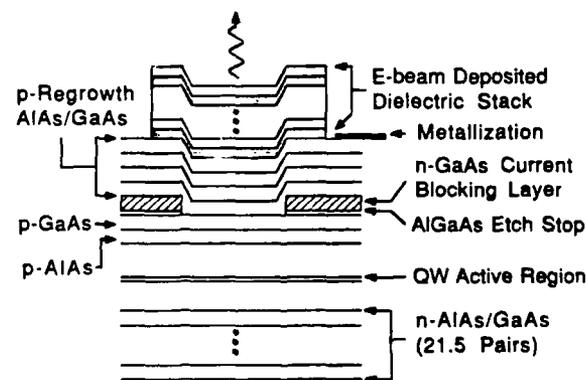


FIG. 1. Schematic cross section (not to scale) showing the VCSEL structure. The device active region consists of two $60\ \text{\AA}$ $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ QWs with three $60\ \text{\AA}$ GaAs barriers. The upper two AlAs/GaAs *n*-type pairs are deposited in a second MBE growth.

This etch leaves a smooth *p*-type GaAs layer on which to perform the next MBE growth. After removing the photoresist mask, the wafer is returned to the MBE system for the growth of two more *p*-AlAs/GaAs quarter-wave pairs, again with superlattice grading layers inserted at each AlAs/GaAs interface.

After the MBE crystal growth, 60- μm -diam photoresist dots are defined covering the previously defined 10- μm -diam regions. A layer of Ag metallization is then deposited on the *p*-type epitaxial surface with a "lift-off" process used to remove the metallization from the 10- μm -diam area. Electrical isolation of the individual VCSEL devices is achieved by etching $\sim 2\text{-}\mu\text{m}$ -deep troughs into the epitaxial layers around each emitter. This leaves rectangular contact pads of $\sim 400\text{ }\mu\text{m}$ on a side of each device. Indium metallization used to mount the wafer for the MBE crystal growth is used for the *n*-side contact. The effectiveness of the current blocking layers is tested by viewing the devices through an optical microscope from the top with an infrared viewer. With the devices under bias, light emission can only be detected in the vicinity of the etched and regrown 10 μm dots, demonstrating the effectiveness of the 600 \AA *n*-type current blocking layer.

The reflectivity of the *p*-side mirror is next enhanced through the deposition of successive pairs of SiO_2/Si dielectric layers using electron beam evaporation. The electroluminescence spectrum is measured before and after the deposition of each pair of SiO_2/Si . The full width at half maximum of the spontaneous spectrum is reduced from $\sim 105\text{ }\text{\AA}$ with just the three-pair AlAs/GaAs Bragg reflector, to $\sim 13\text{ }\text{\AA}$ after the deposition of three pairs of SiO_2/Si . After deposition of the fourth pair of SiO_2/Si , lasing is observed in several of the devices. We note that during the deposition of the first SiO_2/Si pair an error in the SiO_2 layer thickness occurred, which reduced the reflectivity of the top mirror. The design SiO_2 layer thickness is 1620 \AA , while the actual thickness deposited on these devices is $\sim 2400\text{ }\text{\AA}$. The next Si layer has been accordingly thinned to offset the error, but the four-pair SiO_2/Si measures $\sim 0.5\%$ less in reflectivity than for optimized four-pair SiO_2/Si reflectors. Because the reflectivity required for lasing in the QW VCSEL is very high, absolute reflectivity measurements are difficult to perform.

Figure 2 shows the continuous wave (cw) room-temperature lasing characteristics of one of the lower threshold devices. The lasing threshold current is measured to be $\sim 3.9\text{ mA}$, and the linewidth is less than 1 \AA , which is the spectrometer resolution, at the lasing wavelength of $\sim 9830\text{ }\text{\AA}$. The maximum cw output power is greater than 1.2 mW, with a maximum differential slope efficiency of $\sim 25\%$ up to 0.5 mW of power. This cw slope efficiency is close to the highest yet measured for a QW VCSEL,²⁻⁵ in spite of the inevitable absorption loss which occurs in the amorphous Si layers. The relatively high efficiency most likely results from a close to optimum balance between the rear mirror reflectivity, determined by the 21.5 pairs of *n*-type AlAs/GaAs, and the top mirror reflectivity which in this case is only high enough to achieve cw lasing. Above 1 mW of power the slope effi-

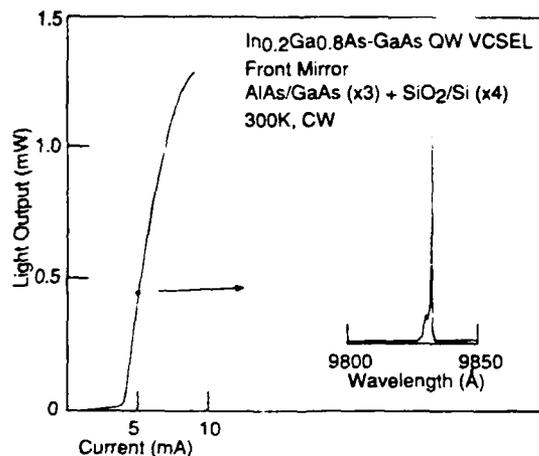


FIG. 2. Light vs current curve and lasing spectrum of the VCSEL of Fig. 1 with four pairs of electron beam deposited SiO_2/Si . The device active region has a 10 μm diameter.

ciency decreases slightly apparently due to device heating.

Figure 3 shows the VCSEL cw characteristics after a fifth SiO_2/Si pair is deposited. For five pairs the threshold current is further reduced, with the device measured for Fig. 3 having a threshold current of $\sim 2.7\text{ mA}$ (a different device than that measured for Fig. 2). A maximum cw output power of 0.9 mW is measured on this VCSEL, which is the highest of several devices measured. The device of Fig. 2 also lased at 2.7 mA with five SiO_2/Si pairs, but with lower output power. Many VCSEL devices which did not lase with four pairs were found to lase upon adding the fifth SiO_2/Si pair. The lowest cw threshold current measured on devices with five SiO_2/Si pairs is 2.3 mA.

The MBE regrowth process provides a particular advantage in that the emission side mirror reflectivity can be optimized to some degree independently of the epitaxially grown structure in order to improve device performance.

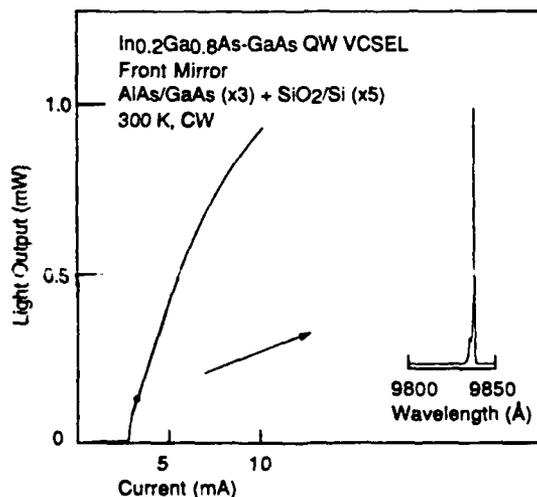


FIG. 3. Light vs current curve and lasing spectrum of the VCSEL of Fig. 1 with five pairs of electron beam deposited SiO_2/Si . As in Fig. 2, the device active region has a diameter of 10 μm .

Low slope efficiency and low power have previously been major drawbacks of the VCSEL,¹⁻⁷ but data from the current devices suggest that these are not intrinsic limitations to the VCSEL, even for QW active regions. Because of absorption loss in the current devices due to the amorphous Si layers used in the top mirrors, considerable improvement in the efficiencies measured for this type of MBE-regrown structure should be realizable with lower loss material choices for the evaporated dielectric stack.

Along with the flexibility in the top mirror design, the regrown device structure presented here offers some degree of optical mode confinement to the laser cavity. Outside the 10 μm active part of the VCSEL, the additional current blocking layers shift the cavity mode away from the ~ 9800 Å lasing wavelength. Reflectivity measurements show in fact that for crystal regions containing the current blocking layers there are no Fabry-Perot transmission peaks in the bandwidth of the high reflectivity region of the semiconductor Bragg reflectors.

Another drawback to previous device structures for the QW VCSEL is very high series resistance, mainly due to the poor hole transport across *p*-type AlAs/(Al)GaAs heterojunctions. In our current devices we also find high series resistance which we have determined to arise from the *p*-type side of the device. Lasing occurs at a forward voltage of ~ 4.5 V, which is comparable to other VCSEL structures utilizing a *p*-type AlAs/GaAs Bragg reflector. Note, however, that previous device structures²⁻⁵ have utilized as many as 20 pairs of AlAs/GaAs on the *p* side, with the series resistance through the mirrors being very sensitive to both *p*-type doping level and interface grading. We believe, therefore, that the series resistance of the current device structure is far from optimized and can be greatly reduced through the choice of number of *p*-type mirror pairs, *p*-type doping level, and interface grading.

In summary, data have been presented on a new

VCSEL device structure which utilizes an MBE regrowth process to allow lateral current injection into the QW active region, optimization of the top surface mirror for high slope efficiency, and optical mode confinement. Because of the planarity of the process, this process may be more readily scalable to reduced device dimensions compared with the VCSEL structures employing deep etching. The device structure also has the potential for less series resistance than other VCSEL designs, which should allow for further improvements in device operating performance.

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