(2)

ONR

SAFENET II FIBER OPTIC IMPLEMENTATION STUDY (FINAL REPORT)

June 28, 1991

Mr. VW.T. Townsend
Mr. T. P. Sevinsky
Mr. F.J. Owens

IBM Corporation 250/058
9500 Godwin Drive
Manassas, VA 22110

N00014-88-C-0745

Contents

Figures

Tables

1.0 INTRODUCTION

The SAFENET II draft Military Handbook, MCCR-0036-DRAFT, establishes requirements and provides guidance for the implementation of a Survivable Adaptable Fiber Optic Network. SAFENET II. The fiber optics communications channel essentially adopts the ANSI Fiber Distributed Data Interface (FDDI) Physical Layer Medium Dependent (PMD) specification, modified by a requirement for increased transmitter optical output power and decreased minimum reciever optical input power (increased sensitivity) to provide a 21 dB overall optical flux budget between (and including) the equipment fiber optic interface connectors (FOIC). A network of cables, optical bypass switches, and spliced fiber joints is described in the Handbook which permit ring operation through up to 5 bypassed nodes while maintaining a minimum 6 dB link optical power margin.

2.0 OBJECTIVES

The overall objective of this study was to validate the Physical Medium dependent fiber optics channel requirements and parameters as described in the SAFENET II Handbook, MCCR-0036-DRAFT, (hereinafter referred to as the Handbook), ie., the fiber, connectors, cable, splices, bypass switches, transmitters and receivers, and the performance parameters associated with them. Specifically, the major issues were:

a. The practicality of constraining the installation of the passive optical network to the maximum optical loss specified in Handbook, and

b. The feasability of providing fiber optic transmitters and receivers which simultaneously meet the requirements of the FDDI Physical Medium Dependent (PMD) specifications as amended by the SAFENET II Handbook and are compatible with anticipated environmental and electronic packaging format constraints.

3.0 ASSUMPTIONS AND GROUNDRULES

In order to focus this investigation on the pragmatic and operational orientation of the objectives, the following assumptions have been made and groundrules adopted:

- o The SAFENET II Handbook and FDDI specifications apply. That is, this is not a system design exercise. The system has been defined as meeting the FDDI PMD secifications except as modified by the Handbook. The issue is whether the system can, in practice, be implemented as described and the availability of active components which can meet the performance specifications in a military environment.

o For breadboarding purposes, where a component is not available exactly as specified in the Handbook, the nearest practical equivalent has been used. A limited length of rad hard "SAFENET" fiber in a single fiber cable construction has been augmented with a long length of commercial equivalent fiber for cost; bypass switches designed to meet MIL-S-24725 but not qualified were used; receivers that meet the SAFENET II requirements are not available and are in part a subject of this study.

o While the implementation study is conducted as a laboratory breadboard exercise, the approach and results will be continually viewed from the viewpoint of a typical platform installation. Whereas a shore-based or commercial network installation can be assembled and tested in any desired order, and segments reassembled, replaced, or "tuned" as necessary, a typical platform installation begins with a set of tested subassemblies (eg., cable assemblies or TCU), follows a prescribed installation proceedure, and culminates in a final test and sell-off.

o A basic famililarity with the fiber optic network as described in the SAFENET Handbook is assumed. This report will adopt the terminology and nomenclature of the Handbook where convenient for simplicity and clarity without formal definitions. The SAFENET II handbook defines the fiber optic network between and including equipment cabinet connectors. We will consider also approaches to intracabinet cabling.

3.1 Typical Installation Sequence

The following is assumed to be a typical platform installation sequence such as a shipboard installation:

a. Install TCUs with tested bypass switches. Bypass switch loss is assumed to have been measured by the switch vendor in accordance with EIA-455-34. Fiber pigtails may or may not be pre-terminated. This is a shipyard process.

b. Pull tested cable. Following installation of the TCUs, multifiber trunk and optical interface cables are pulled through the cableways. The cable is normally unterminated at both ends. Cabled fibers have been 100% tested for optical attenuation and discontinuities. This is a normal shipyard proceedure.

c. Splice trunk and interface cables into TCU. This operation must be performed by someone trained in the particular splicing method employed. Splicing may be accompanied by a joint loss measurement or an active "tuning" of the joint loss, depending on the splice type and installation philosophy.

d. Install the Fiber Optic Interface Connectors (FOIC) on the equipment end of the Interface Cable, if they have not previously been installed and tested.

e. Final optical acceptance testing. At this point, the entire network has been spliced and the only optical accesss into the system is through the FOICs. Any joint loss measurements or active tuning made up to this point are incidental to the splicing and FOIC termination process. This final acceptance test should be done by the agent responsible for the splicing, since the only remedy for a failed test is to rework the installation (resplice).

At this point, the tested and accepted cable plant may lie dormant for an unspecified period of time. When the equipment cabinets are installed, the previously terminated FOICs will be mated and the network is assume to meet specifications.

4.0 APPROACH

The approach to validating the SAFENET II fiber optics implementation was conducted in wo phases. In the first phase, an optical breadboard of the network was assembled using short lengths of cable to simulate Interconnect Cables and Trunk Cables, with optical bypass switches to simulate Trunk Coupling Units (TCU) with up to 5 bypassed nodes. The network fibers (cables and switch pigtails) are joined with splices, in accordance with the SAFENET Handbook. In addition, pairs of optical fiber termini or contacts used in the Mil-C-28876 FOIC and Mil-T-29504 termini used in edge card connectors are included in the launch and receive ports of the network. Using the optical breadboard, the performance of the passive optical components is determined.

For the second phase, the active components (transmitter and receiver) were included. An analysis of the potential performance of a realistic receiver was performed. The simple LED optical source and optical power meter used to measure the passive network is replaced by a fiber optic transmitter and receiver. The performance of the entire physical medium dependent path was then analyzed for the required SAFENET II communication channel performance using a Bit Error Rate Test Set (BERTS) test bed.

4.1 Test bed

The SAFENET II fiber optic breadboard test bed consists of an end-to-end network consisting of a complete transmit and receive port with five intervening bypassed nodes to comply with the SAFENET II Handbook. An optical schematic of the test bed is shown in Figure 1. The color coding is keyed to the actual bypass switches used.

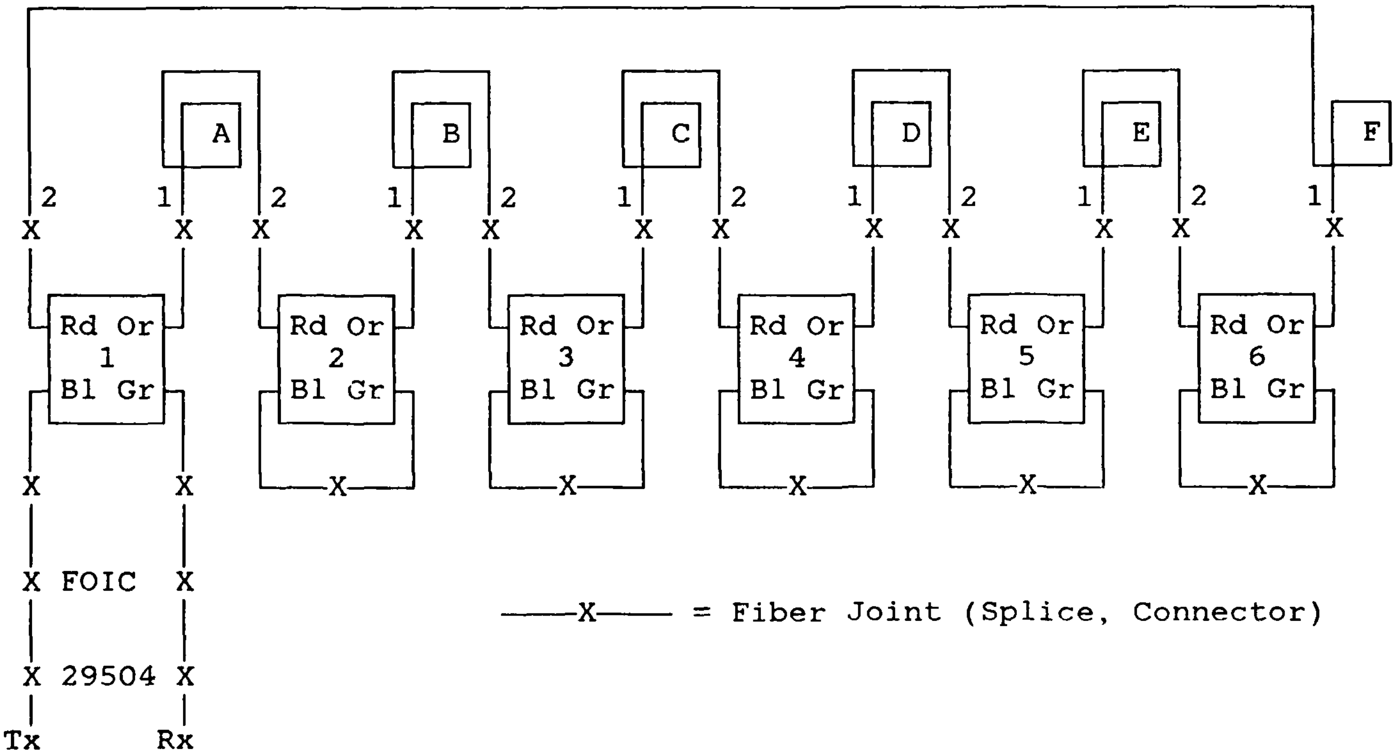


Figure 1. SAFENET II Fiber Optic Network Test Bed Optical Schematic Diagram

Components: The optical components used in the breadboard were as follows:

- Cable: AT&T single fiber FDDI cable containing 62.5/125/.275 rad hard fiber, 400 MHz-km bandwidth.

  Cable was terminated as:

  -- (6) 10-meter trunk cables
  -- (1) 200-meter trunk cable
  -- (4) 5-meter Interface and harness cables

- Optical Bypass Switches: Dicon, model S-FDDI-62 , dual fiber, reversable, non-latching

- Splices: AT&T Rotary Mechanical Splice (RMS)

- Fiber Optic Interface Connector (FOIC): Hughes termini for Mil-C-28876

- Card edge connector: Bendix MIL-T-29504 termini

- Additional 1.2 km spool of non-rad hard fiber.

The normal direction of light propagation in the network is from the optical source, designated as transmitter or Tx, through two 5-meter cables with MIL-T-29504 and MIL-C-28876 termini into the transmit port (Blue)of the first bypass switch. The signal exits the "trunk out" port of switch 1 (Orange), through trunk cable A and into the "trunk in" port of switch 2(Red). The bypass mode for switches 2-6 is Red in and Orange out. The ring completes from switch 6 through trunk cable F to the trunk in port (Red) of switch 1. Switch 1 is always in the normal mode, with receive path from Red to Green and out to the optical detector through the Interconnect cables and connectors. All fiber joints,(-X-), not specifically labeled as connectors are rotary mechanical splices.

In order to maximize the number of different combinations of splice halves (ferrules) in the network breadboard, two modifications were made in the basic configuration. In the first modification, the trunk cables A-F were simply reversed in place, keeping the same network configuration but modifying the bypass switch-trunk splices. In the second modification,the bypass switches were joined directly at the trunk ports and the trunk cables were moved to the receive/transmit ports as shown in Figure 2.

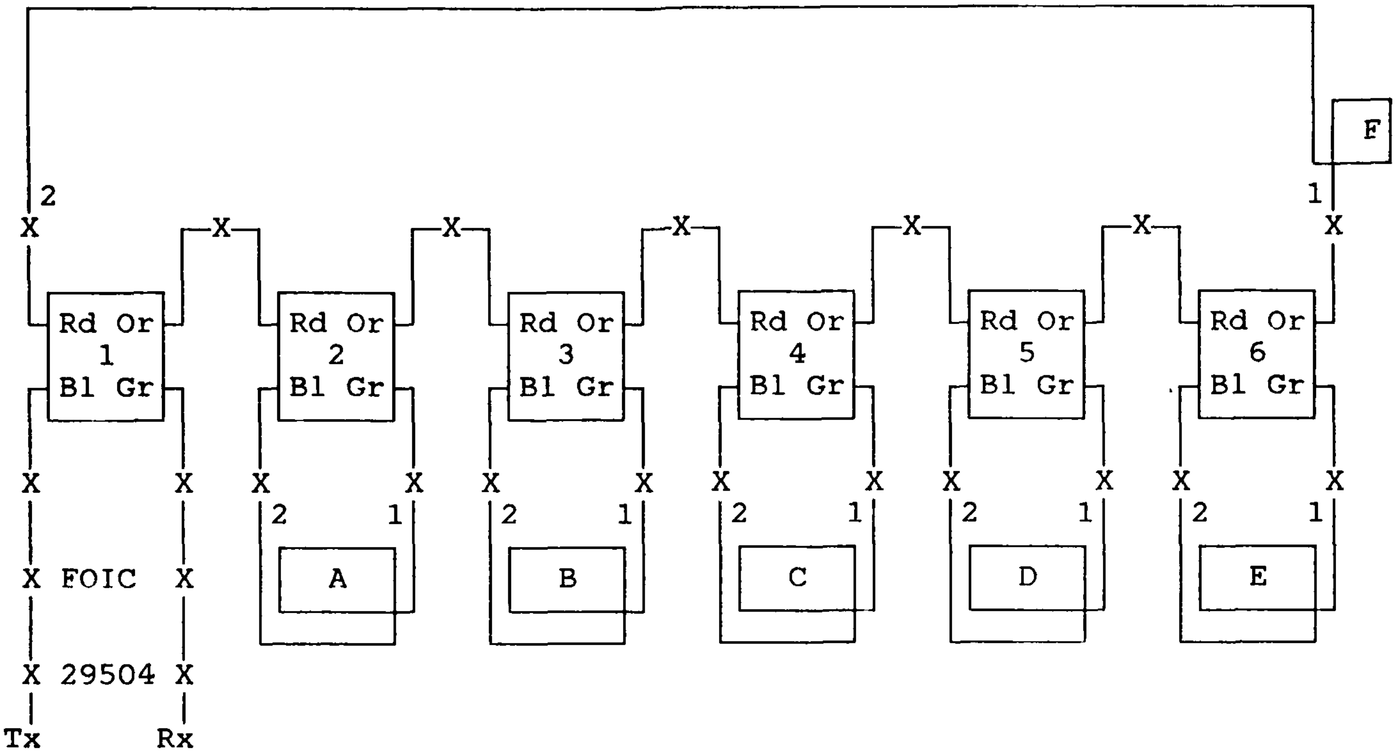


Figure 2. Alternative Test Bed Network Configuration

4.2 Measurement Proceedures

The proceedure for measuring the optical loss at a splice joint is as follows:

1. A 1.3 um surface emitting LED is coupled to the optical fiber test link. The SLED has an integral lens and an additional coupling lens typical of FDDI transmitters.

2. At the joint under test, the launch fiber ferrule is cleaned with methanol, inserted into the detector head of a fiber optic power meter and the launch power in dBm recorded.

3. The launch fiber / ferrule is removed from the meter and a minimum amount of index matching gel applied to the tip.

4. The receive ferrule/fiber is mated with the launch ferrule for a completed splice joint.

5. The distal end (ferrule) of the receive fiber is inserted into the optical power meter and the splice joint is tuned for a minimum by rotating the ferrules with respect to each other.

6. The optical power is recorded and the joint loss is reported as the difference between the power launched and the power received.

A drawing of the rotary mechanical splice is shown in Figure 3.

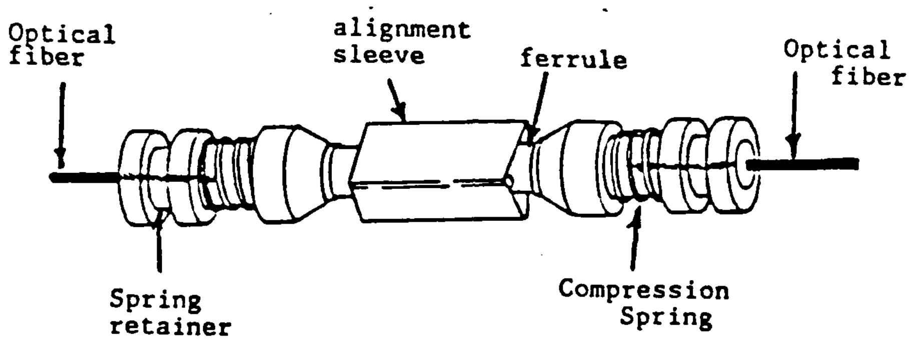


Figure 3. Rotary Mechanical Splice

For a splice measurement, any loss in the short length of receive fiber is ignored. To measure the optical loss in a bypass switch path, the same proceedure is used, except that the loss in the receive path (switch path) is the primary loss being measured. The reported loss is thus the sum of the launch splice into the switch pigtail and the switch path loss itself. This is shown in more detail in Figure 4. To measure the loss in the receive path, for instance, the optical power is measured first at the trunk fiber coming into the TCU. The switch is then spliced to the trunk cable (Red switch pigtail) and the optical power is measured at the Green switch pigtail. The optical path then has both the input splice (Trunk-TCU) and the switch Rx path in series. With the switch set in the bypass mode, the loss through the input splice and bypass path can be measured at the trunk out, or Orange pigtail. The color coding has been used to correspond to the network block diagram and actual switch lead color.

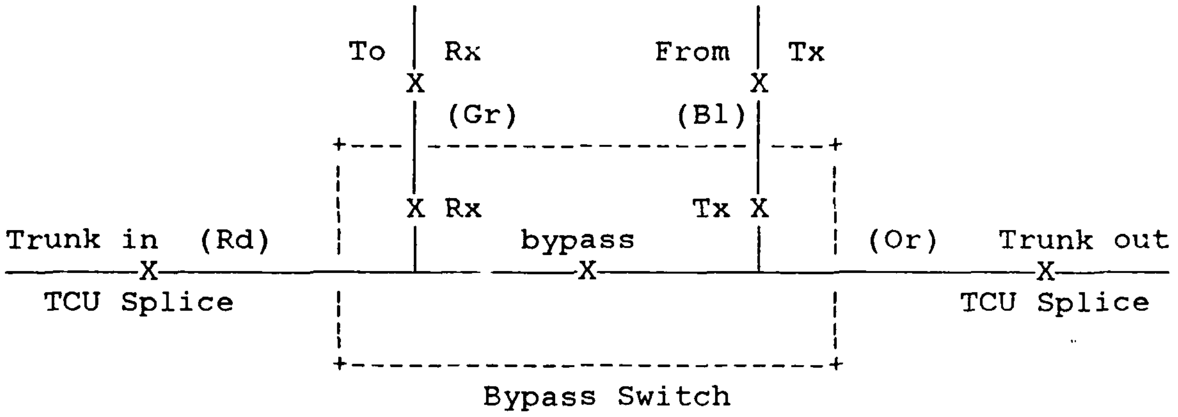
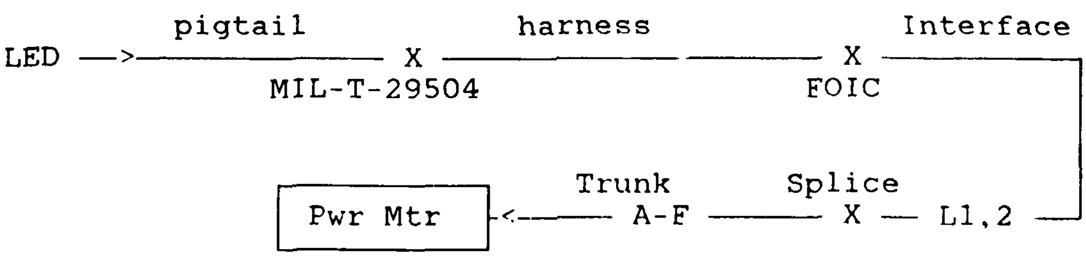


Figure 4. Bypass Switch / TCU Schematic Diagram

5.0 RESULTS

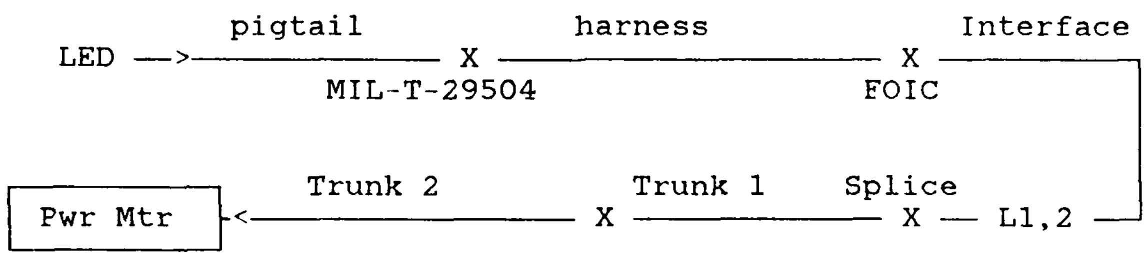
5.1 Passive Components

5.1.1 Rotary Mechanical Splice. Using 5 10-meter cables terminated on both ends with one half of a rotary mechanical splice and two test leads terminated on one end with RMS halves, all possible pairs of pairs were joined and tested singly for attenuation for a total of 84 splices. The 10-meter cables were simulated Trunk Cables for the network breadboard and the test leads were simulated Interface Cables. All cable lengths were cut from a single spool of cable. Since all trunk cables were terminated to form a matched splice with its respective bypass switch pigtail, none of the RMS halves in this test formed a matched pair splice. For identification, the trunk cables are labled A-F with ends A1, A2, B1...F2. All splices involving L1 or L2 were using the following configuration:



The splice under test is between L1 or L2 end of the Interface cable and the Trunk cable. The Trunk cable terminates directly at the optical power meter. The LED optical output is thus mode filtered through the MIL-T-29504 terminus pair to simulate a potential card edge connector within the equipment cabinet and the FOIC of the enclosure with it's 25um gap prior to the launch half of the RMS. This is expected to provide a more realistic estimate of the optical performance than if the splice were illuminated directly by the LED.

For all other splice pairs except those incorporating L1 and L2, the same fiber configuration above is used as the launch configuration and an additional Trunk fiber is added as the receive fiber, as shown in the diagram below:



Thus, the two launch conditions are equivalent except for the additional rotary mechanical splice on the launch side.

For each mated splice pair, three loss measurements were taken:

1. Ferrules rotated for maximum loss (assumed maximum lateral misalignment between fiber cores)

2. Ferrules rotated for minimum loss (assumed minimum lateral misalignment) and

3. Ferrules rotated to align the indexing tabs as an arbitrary measure at random alignment (no tuning).

Histograms for the untuned (random) and tuned minimum loss are shown in Figure 4a and 4b. Actual loss measurements are included as Appendix A for minimum, maximum, and "tabbed" (untuned) values, including the difference between the minimum and maximum losses.

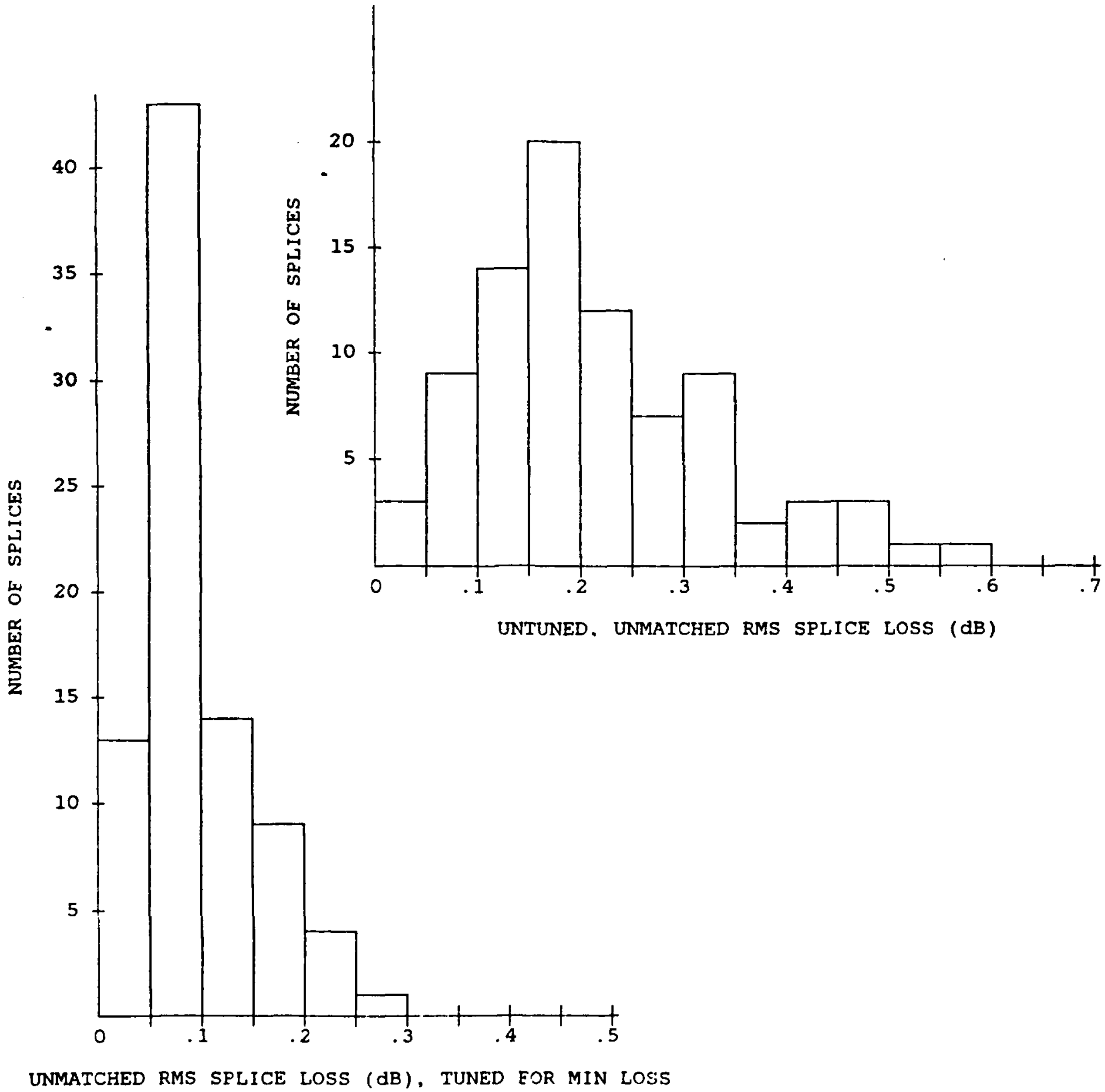


Figure 3. Rotory Mechanical Splice Loss Histograms

5.1.2 Link Breadboard Splices. Interconnection of the fiber optic components into the "5 bypass" breadboard SAFENET II breadboard configuration yields additional splice loss measurements. Network measurements were systematically measured from the launch end as the network joints (splices) were assembled and measured in order. These measurements were made in six trials consisting of a complete ene-to-end assembly and measurement of the network.

Trial 1. - The network of Figure 1 was assembled measured with bypass switches 2-6 in the "bypass" mode.

Trial 2. - Same as trial 1, with bypass switches 2-6 in the "normal" mode, looping the optical signal out through the "receive" switch port and back in through the "transmit" switch port.

Trial 3. - Same as trial 1, with the LED and optical power meter reversed at bypass switch 1, ie., Interface Cable ferrule L1 was moved from Blue to Green, and L2 was moves from Green to Blue.

Trial 4. - Same as trial 2 with LED and optical power meter reversed. (ie., trial 3 with switches in "normal configuration).

Trial 5. - Same as trial 1, except that trunk cables A-E are reversed end for end in place.

Trial 6. - Same as trial 2 with the trunk cables moved as shown in Figure 2.

For the trial 1 -4 configurations (see Figure 1), all trunk cables, interconnect cables, and bypass switch fibers were terminated such that all fiber joints are made with matched RMS ferrules. Since only one end of each trunk cable is accessible to be measured apart from the following switch, matched ferrule RMS joints can be measured at the -1 end of each trunk cable in trials 1 and 2, and at the -2 end in trials 3 and 4. Since the same splice is measured repeatedly in the pairs of trials and are not independent splices, the results are simply averaged as the best estimate of loss. Each splice is then averaged for the mean and standard deviation. The data is shown in Table 1.

Matched Ferrule RMS Joint Loss (dB)			
Splice	Trial 1	Trial 2	Ave.
Or1-A1	.16	.14	.15
Or2-B1	.08	.19	.125
Or3-C1	.22	.15	.185
Or4-D1	.10	.16	.13
Or5-E1	.29	.18	.235
Or6-F1	.17	.19	.18
Gr1-L2	.10	.10	.10
---	Trial 3	Trial 4	---
Rd1-F2	.26	.31	.285
Rd6-E2	.13	.15	.14
Rd5-D2	.21	.20	.205
Rd4-C2	.10	.16	.13
Rd3-B2	.21	.18	.195
Rd2-A2	.10	.20	.15
Average loss:			.17
Std. dev:			.05

Table 1. Matched Ferrule RMS Joint Loss

For trials 5 and 6, where the trunk cables have either been reversed (trial 5) or moved to the Rx-Tx switch ports, the joints at both ends of the trunk cables can again be measured, but this time with unmatched RMS ferrules. The unmatched ferrule joint loss is shown in Table 2.

Unmatched Ferrule RMS Joint Loss (dB)	
Splice	Trial 1
Or1-A1	.16
Or2-B1	.08
Or3-C1	.22
Or4-D1	.10
Or5-E1	.29
Or6-F1	.17
Gr1-L2	.10
---	Trial 3
Rd1-F2	.26
Rd6-E2	.13
Rd5-D2	.21
Rd4-C2	.10
Rd3-B2	.21
Average:	0.19
Std. Dev:	0.05

Table 2. Unmatched Ferrule RMS Joint Loss

5.1.3 Discussion. The 84 single splice loss measurements between trunk and interconnect cable RMS ferrules clearly demonstrates the decrease in average loss gained by tuning for minimum loss (0.10 dB) versus a random, untuned mating (.22 dB). For the tuned splice, only 5 out of 84 were outside the 0.2 dB SAFENET specification, with a maximum loss of 0.27 dB. By contrast, over 40% of the random splices fell outside the specification with a maximum loss of 0.56 dB. Tuning the splice for maximum loss shows how bad the joint could, in principle, be, with a mean loss maximum of 0.36 dB. and only 10 splices within the desired .2 dB. The mean difference between the tuned maximum and tuned minimum was 0.25 dB.

One would expect that the loss for splices formed with matched ferrules would be lower than the mean of the 84 unmatched ferrule spices, both because of the improved alignment of the ferrule match and because the splices as installed in the breadboard network have a variable number of splices and switches in the launch path with increased opportunity for high order mode shedding. The data, however, shows a mean loss of 0.17 dB for the matched ferrule splices versus the 0.10 for the unmatched ferrule splices, although both have similar standard deviations of 0.05 dB. For the network breadboard splices for which the trunk cables have been purposely reversed or moved to create unmatched ferrule splices, the mean loss increases to 0.19 dB, as expected. If the breadboard configurations are examined, it becomes apparent that all splices are measured with the bypass switch fiber as the launch fiber and the AT&T cable as the receive fiber. The 84 single splices were measured with AT&T cable both as the launch and receive fibers. It is a reasonable inference that the systematic difference in splice loss is due to a difference in the cable and switch fibers. If a simple areal mismatch is assumed, the 0.07 dB difference could be caused by as little as a 0.5 micron difference in core diameter! This emphasizes both the sensitivity of the link component losses to fiber parameters and the inability of fiber tolerance specifications (eg., typically +/- 3 um core diameter) to guarantee joint loss limits.

5.1.4 Bypass Switch. As pointed out earlier, a practical measurement of a bypass switch loss includes the splice loss at the launch side of the switch. This is how a loss measurement would be made at installation and thus how the breadboard measurements were made. In our breadboard network configuration, bypass switch #1 was consistently used in the "normal" mode (not bypassed) to provide both the transmit port for the network and the receive port for the return loop of the ring. The remaining 5 switches were were then measured all in the normal mode or all in the bypass mode, depending on the measurement trial.

Switch #1 - The Bl-Or path through switch 1 was normally the transmit port except for trials 3 and 4 when the direction of the signal through the network was reversed. Similarly, the Rd-Gr path through switch 1 was normally the receive port, except for trials 3 and 4. The losses for these ports including their respective launch splices are shown in Tables 3a and 3b. Since both paths in the switch 1 are measured as the transmit port and the receive port, these measurements have been summarized by function (Tx or Rx). Presumably, the apparent switch loss may be affected by whether high order modes are present (transmit end) or shed by intervening fiber joints (receive end).

Matched Ferrule Splice + Switch Switch #1 - Normal Tx			
Trial	Splice + Sw.	Loss (dB)	T/R
1	L1-Bl1+BlOr1	.72	T
2	L1-Bl1+BlOr1	.67	T
3	A1-Or1+OrBl1	.55	R
4	A1-Or1+OrBl1	.56	R
5	L1-Bl1+BlOr1	.61	T
6	L1-Bl1+BlOr1	.61	T
	Mean (Tx):	.653	
	Mean (Rx):	.555	
	Mean (all):	0.62	

Table 3a. Matched Ferrule Splice plus Tx Switch Path Loss - Bypass Switch #1

Matched Ferrule Splice + Switch Switch #1 - Normal Rx			
Trial	Splice + Sw.	Loss (dB)	T/R
1	F2-Rd1+RdGr1	.83	R
2	F2-Rd1+RdGr1	.85	R
3	L1-Gr1+GrRd1	1.42	T
4	L1-Gr1+GrRd1	1.35	T
5	F2-Rd1+RdGr1	.94	R
6	F2-Rd1+RdGr1	.89	R
	Mean (Rx):	1.385	
	Mean (Tx):	.878	
	Mean (all):	1.05	

Table 3a. Matched Ferrule Splice plus Rx Switch Path Loss - Bypass Switch #1

Loss measurements for the remaining 5 switches is shown in table 4. Each switch has a bypass path and a normal receive/transmit path pair, all with their associated launch splices, depending on the direction of the optical propagation.

The mean bypass switch plus launch splice loss data is summarized in Table 5. The manufacturer's loss data as reported on the device data sheets for the switch alone is included for comparison. The two transmit and receive paths were included separately.

Bypass Switch #2		
Trial	Splice + Sw.	Loss (dB)
	Path RdOr2	
1	A2-Rd2+RdOr2	.60
3	B1-Or2+OrRd2	.52
5	A1-Rd2+RdOr2	.66
	Mean:	0.59
	Path RdGr2	
2	A2-Rd2+RdGr2	.68
4	B12-Gr2+GrRd2	.51
6	Or1-Rd2+RdGr2	.84
	Mean:	.68
	Path BlOr2	
2	Gr-Bl2+BlOr2	.85
4	B1-Or2+OrBl2	.40
6	A2-Bl2+BlOr2	1.03
	Mean:	0.76

a. Switch #2

Bypass Switch #3		
Trial	Splice + Sw.	Loss (dB)
	Path RdOr3	
1	B2-Rd3+RdOr3	.78
3	C1-Or3+OrRd3	.78
5	B1-Rd3+RdOr3	.82
	Mean:	0.79
	Path RdGr3	
2	B2-Rd3+RdGr3	.72
4	B13-Gr3+GrRd3	.56
6	Or2-Rd3+RdGr3	.81
	Mean:	.70
	Path BlOr3	
2	Gr3-Bl3+BlOr3	.39
4	C1-Or3+OrBl3	.40
6	B2-Bl3+BlOr3	.40
	Mean:	0.40

b. Switch #3

Table 4a,b. Splice plus Bypass Switch Loss Data

Bypass Switch #4		
Trial	Splice + Sw.	Loss (dB)
	Path RdOr4	
1	C2-Rd4+RdOr4	.41
3	D1-Or4+OrRd4	.39
5	C1-Rd4+RdOr4	.42
	Mean:	0.41
	Path RdGr4	
2	C2-Rd4+RdGr4	.40
4	Bl4-Gr4+GrRd4	.52
6	Or3-Rd4+RdGr4	.47
	Mean:	.46
	Path BlOr4	
2	Gr4-Bl4+BlOr4	.73
4	D1-Or4+OrBl4	.70
6	C2-Bl4+BlOr4	.65
	Mean:	0.69

c. Switch #4

Bypass Switch #5		
Trial	Splice + Sw.	Loss (dB)
	Path RdOr5	
1	D2-Rd5+RdOr5	.88
3	E1-Or5+OrRd5	1.16
5	D1-Rd5+RdOr5	1.01
	Mean:	1.02
	Path RdGr5	
2	D2-Rd5+RdGr5	.57
4	Bl5-Gr5+GrRd5	.88
6	Or4-Rd5+RdGr5	.70
	Mean:	0.72
	Path BlOr5	
2	Gr5-Bl5+BlOr5	.68
4	E1-Or5+OrBl5	.55
6	D2-Bl5+BlOr5	.44
	Mean:	0.56

d. Switch #5

Table 4c,d. Splice plus Bypass Switch Loss Data

Bypass Switch #6		
Trial	Splice + Sw.	Loss (dB)
	Path RdOr6	
1	E2-Rd6+RdOr6	.59
3	F1-Or6+OrRd6	.52
5	E1-Rd6+RdOr6	.55
	Mean:	0.55
	Path RdGr6	
2	E2-Rd6+RdGr6	.50
4	Bl6-Gr6+GrRd6	.53
6	Or5-Rd6+RdGr6	.38
	Mean:	.47
	Path BlOr6	
2	Gr6-Bl6+BlOr6	.58
4	F1-Or6+OrBl6	.71
6	E2-Bl6+BlOr6	.61
	Mean:	0.63

e. Switch #6

Table 4e. Splice plus Bypass Switch Loss Data

Splice plus Switch Loss Summary		
Switch Path	Mean Loss	Data Sheet
Rd-Or 2	.59	.50
Rd-Gr 2	.68	.54
Bl-Or 2	.76	.49
Rd-Or 3	.79	.66
Rd-Gr 3	.70	.61
Bl-Or 3	.40	.53
Rd-Or 4	.41	.65
Rd-Gr 4	.46	.64
Bl-Or 4	.69	.65
Rd-Or 5	1.02	.66
Rd-Gr 5	.72	.52
Bl-Or 5	.56	.57
Rd-Or 6	.55	.67
Rd-Gr 6	.47	.67
Bl-Or 6	.63	.61
Mean:	0.63	.60
Std. Dev:	0.165	
Bl-Or 1	.62	.60
Rd-Gr 1	1.05	.54
Mean:	0.65	.59
Std. Dev:	0.185	

Table 5. Splice plus Bypass Switch Loss Summary

5.1.5 Discussion. In contrast to the breadboard splice data where all receive fibers were cable (AT&T) fibers, all the receive fibers for the splice - switch pairs are switch pigtails. Launch fibers were either cable or switch as can be seen from the data or the breadboard optical schematic diagram. While the transmit and receive paths of switch 1 were appended to the data summary table, the 5 intermediate bypass switches (2-6) are believed to be the most representative. The Bl-Or path for switch 1 shows 0.65 dB loss (with its launch splice) as an input path vs. 0.56 dB when used as the end path. Similarly, the Rd-Gr path shows 1.39 dB on input but only 0.88 at the end. Since any high order mode effects should depend on the joint history on the launch side, The switch losses were compared between trials 2 and 4. These trials have the greatest number of switch paths in series, but with the light direction of travel reversed by swaping the LED source and the detector. The comparison is shown in Figure 5. Although the switch data necessarily includes different launch splices for the two directions of travel, the graph clearly suggests a systematic decrease in apparent joint loss as a function of tne number of previous joints, presumably as high order modes are shed.

The increase in mean splice loss (0.07 dB) when pigtail and cable fibers were mixed suggests that the switch plus splice data may be underestimated by an equivalent amount. If the vendor switch data mean loss of 0.60 dB is increased by .10 dB to include a launch splice, the mean becomes 0.70 dB for a switch- splice pair. If the breadboard data is corrected by the 0.07 dB supposed underestimation, the mean measured loss becomes 0.70 dB also, an interesting but probably fortuitous correspondence.

5.2 Loss Budget

A passive network loss budget for both the maximum loss and the mean, or most probable loss, can now be constructed. The loss values and rationale for the individual elements are:

Splice plus Bypass Switch: Mean: 0.63 dB Max: 1.0 dB

Rationale: The measured mean loss in the breadboard is 0.63 dB, excluding the transmit and receive ports on switch 1 These were evaluated separately since they represent the extremes of maximum and minimum high order modes. A max loss of 1.0 dB is retained from the Handbook, since the bypass switch will be procured to a 0.8 dB max loss spec and a maximum installed loss of 0.2 dB is assumed for the splice.

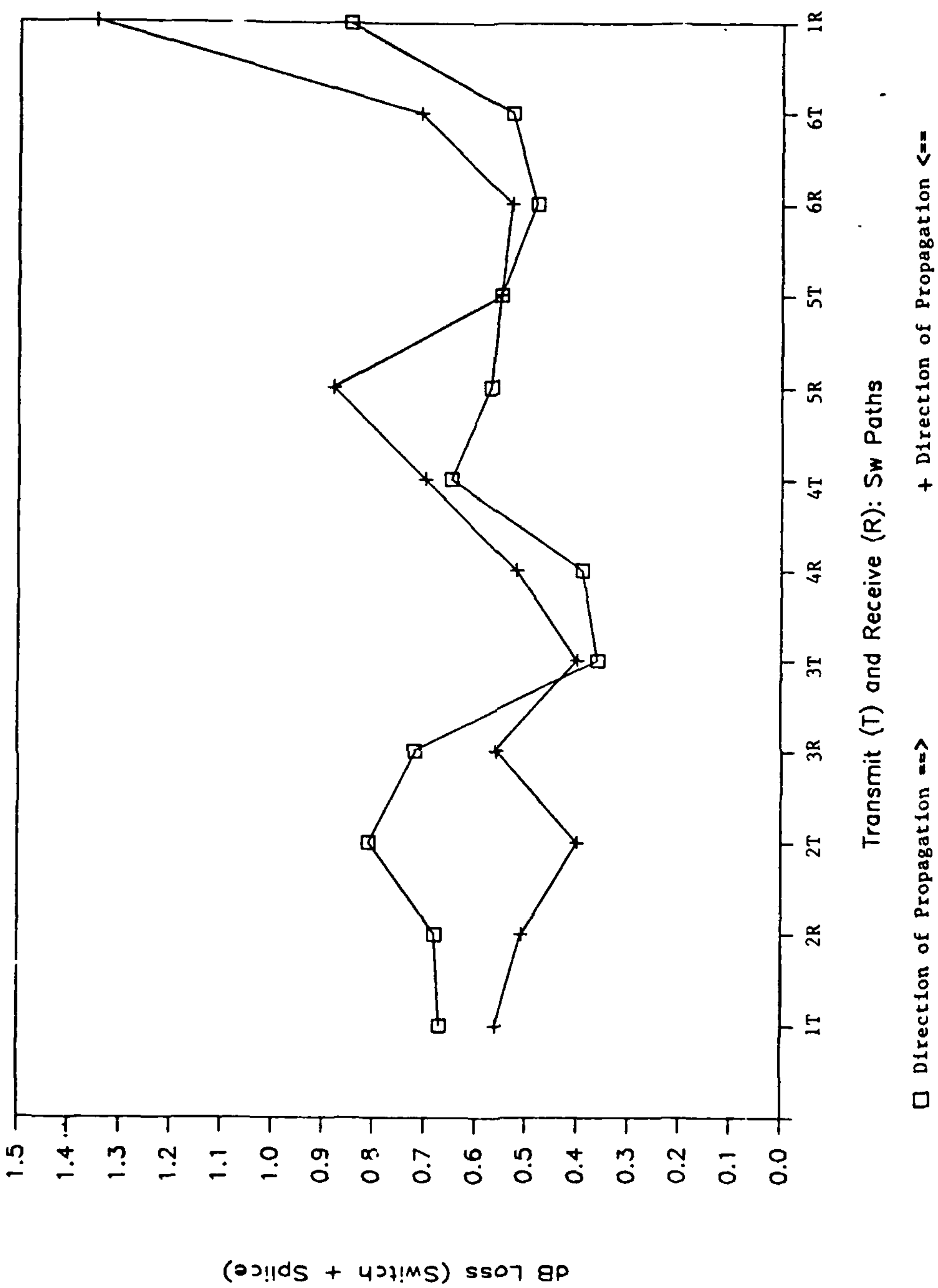


Figure 5. Bypass Switch Losses for Reversed LED and Detector

Splice (only): Mean: 0.19 dB Max: 0.20 dB

Rationale: Although the mean loss for unmatched ferrules with the same launch and receive fiber (trunk cable measurements) was 0.10 dB, the actual data from the breadboard was 0.19 dB, presumably due to fiber mismatch. If the splice plus switch measurements underestimate the loss by a similar amount, it is important to use splice and switch data either as measured or corrected consistently. Since switches and extra splices appear in pairs in the network, the resulting loss budget is unchanged.

Cable, Interconnect: Mean: 0.1 dB (0.05 km) Max: 0.2 dB (0.1 km)

Cable, Trunk: Mean: 0.2 dB (0.10 km) Max: 0.4 dB (0.2 km)

Rationale: The specified max cable loss of 2.0 dB/km is used without modification. The reduced mean losses assume that the mean length of the trunk and interconnect cables is only half the allowable maximum.

FOIC: Mean: 1.0 dB Max: 1.0 dB

Rationale: The maximum loss of 1.0 dB is retained from the specification since the comnnector loss is controlled by the fiber termination process and tested as built. The mean loss was not reduced because the 28876 connector has a 25 um septum between contacts which introduces additional mode selective loss. Any reduction in mean loss is incorporated in the high order mode loss below.

High Order Mode Loss: Mean: 0.5 dB Max: 1.0 dB

Rationale: While HOM loss is an essential element of the loss budget if the optical source is not mode filtered or otherwise controlled, a valid measurement of the effect is difficult since the effect is distributed among all the fiber joints and depends strongly on loss history. Based on the breadboard loss data comparing optical propagation in both directions, and our experience with multimode LED systems, The range of 0.5 dB to 1.0 dB would seem to be appropriate.

Using the above values for the mean and maximum component loss, the following loss budget has been constructed. The transmit and trunk paths have been listed as a cumulative path loss through bypassed nodes. The receive path loss is shown separately to derive the complete path loss for the transmitter to any port. The component values have been shown in detail for the first two ports for illustration. The fixed loss differentials per node have been continued for a total of 9 ports. The maximum link loss values are identical to the example in Appendix F of the SAFENET II Handbook. The bypass switch loss and its input splice loss have not been separated to correspond to the way the components would be monitored at installation.

SAFENET II LOSS BUDGET		Cumulative (Tx + trunk)		Receive Path	
Node	Link Component	Mean	Max	Mean	Max
0	FOIC (Tx)	1.0	1.0		
	Cable, Interconnect	0.1	0.2		
	Splice (I/C-TCU) + BPS	0.63	1.0		
	Splice (TCU-Trunk)	0.19	0.2		
	Cable, Trunk	0.2	0.4		
	Cum. Subtotal (node 1)	2.12	2.8		
1	Splice (Trunk-TCU) + BPS1			0.63	1.0
	Splice (TCU-I/C)			0.19	2.0
	Cable, Interconnect			0.1	0.2
	FOIC			1.0	1.0
	H.O. Mode Loss			0.5	1.0
	Node 1:			4.54	6.2
2	Splice (Trunk-TCU)+ BPS1	0.63	1.0		
	Splice (TCU-Trunk)	0.19	0.2		
	Cable, Trunk	0.2	0.4		
	Cum. Subtotal (node 2)	3.14	4.40		
	Splice (Trunk-TCU) + BPS2			0.63	1.0
	Splice (TCU-I/C)			0.19	0.2
	Cable, Interconnect			.1	.2
	FOIC			1.0	1.0
	H.O. Mode Loss			0.5	1.0
	Node 2:			5.56	7.80

Table 6. SAFENET II Passive Component Loss Budget

SAFENET II LOSS BUDGET (Cont'd)		Cumulative (Tx + trunk)		Receive Path	
Node	Link Component	Mean	Max	Mean	Max
3	Trunk Path Losses	1.02	1.6		
	Cum. Subtotal (node3)	4.16	6.0		
	Interconnect Path Losses			2.42	3.4
	Node 3:			6.58	9.4
4	Trunk Path Losses	1.02	1.6		
	Cum. Subtotal (node 4)	5.08	7.6		
	Interconnect Path Losses			2.42	3.4
	Node 4:			7.50	11.0
5	Trunk Path Losses	1.02	1.6		
	Cum. Subtotal (node 5)	6.10	9.2		
	Interconnect Path Losses			2.42	3.4
	Node 5:			8.52	12.6
6	Trunk Path Losses	1.02	1.6		
	Cum. Subtotal (node 6)	7.12	10.8		
	Interconnect Path Losses			2.42	3.4
	Node 6:			9.54	14.2

Table 6. SAFENET II Passive Component Loss Budget (Cont'd)

SAFENET II LOSS BUDGET (Cont´d)		Cumulative (Tx + trunk)		Receive Path	
Node	Link Component	Mean	Max	Mean	Max
7	Trunk Path Losses	1.02	1.6		
	Cum. Subtotal (node 7)	8.14	12.4		
	Interconnect Path Losses			2.42	3.4
	Node 7:			10.56	15.8
8	Trunk Path Losses	1.02	1.6		
	Cum. Subtotal (node 8)	9.16	14.0		
	Interconnect Path Losses			2.42	3.4
	Node 8:			11.66	17.4
9	Trunk Path Losses	1.02	1.6		
	Cum. Subtotal (node 4)	10.18	15.6		
	Interconnect Path Losses			2.42	3.4
	Node 9:			12.60	19.0

Table 6. SAFENET II Passive Component Loss Budget (Cont´d)

The total Tx to Rx mean and maximum path losses for 9 nodes is summarized in the table below. The mean margin and minimum margin indicate the excess optical signal over that required for 2.5E-10 BER, assuming that the fiber optic receiver and transmitter pair can support the minimum 21 dB optical flux budget specified by SAFENET. The additional component loss margins suggested for adverse environments in Appendix F of the Handbook have been included in the last two columns.

		Normal Environment				Adverse Envr.	
Node (Tx=0)	# Nodes Bypass	Max Loss	Mean Loss	Min Margin	Mean Margin	Min Margin	Mean Margin
1	0	6.2	4.94	14.8	16.06	11.98	13.49
2	1	7.8	6.16	13.2	14.84	9.22	11.24
3	2	9.4	7.38	11.6	13.62	6.46	8.99
4	3	11.0	8.60	10.0	12.40	3.70	6.74
5	4	12.6	9.82	8.4	11.18	0.94	4.49
6	5	14.2	11.04	6.8	9.96	(-1.82)	2.24
7	6	15.8	12.26	5.2	8.74		(-0.01)
8	7	17.4	13.48	3.6	7.52		
9	8	19.0	14.70	2.0	6.30		

Table 7. SAFENET II Loss Budget and Margin Summary

5.2.1 Discussion. The maximum loss column of Table 7 is identical to the maximum loss values derived in Appendix F of the SAFENET II Handbook, and is a good "worst case" design point. As summarized in the Handbook, up to 5 bypassed nodes can be accomodated without falling below the required 6 dB system margin. In practice, of course, the actual excess margin is invisible and expresses itself as a latent increase in link capability. The mean, or expected, loss has been estimated from these empirical data and gives both an indication of the likelihood that the network can be installed as specified without excessive tuning and rework, and also an indication of the actual excess margin likely to exist. This excess margin can be expressed either as a potential for traversing additional bypassed nodes in an emergency, or the ability to absorb the increased losses of operation under "adverse" environments. A network path, of course, does not exceed its specified error rate with any excess margin >0.

5.3 Active Components

Having established a mean or expected link loss with a maximum loss limit, the remaining question is the availability of a transmitter and receiver pair that can concurrently meet the FDDI specifications, the optical output power and sensitivity of the SAFENET II requirements, and the physical and environmental constraints of typical military electronic packaging.

The approach will be to perform a brief analysis of expected receiver performance, including noise-limited front end sensitivity and projected implementation and application dependent penalties. Since receivers meeting all the requirements are not presently available, the analysis will be supplemented with some spot checks of a representative of good commercial bipolar receiver design and a PIN-FET front end breadboard intended for applications similar to SAFENET.

5.3.1 Optical Receiver. Optical receiver performance is usually characterized by the minimum optical input power necessary to reproduce the input data electrically with a given minimum Bit Error Rate (BER), usually 1E-9 or, for FDDI, 2.5E-10. Generally the temperature, or temperature range is specified, along with the test data pattern, often a pseudorandom bit stream (PRBS) such as 2E7-1. By convention, unless otherwise specified, the data pattern is assumed to be sampled in the center of the bit time or "eye opening", the optical input extinction ratio is zero (100% light modulation), and the optical input rise and fall time is small compared to a bit time. While this allows the sensitivity of different receivers to be easily compared, if other conditions are specified or can be derived for the application, these must be taken into account in evaluating a specific receiver for an application.

A complete receiver generally includes the detector and preamplifier, post amplification, and a decision circuit to regenerate a logical electrical output. For these receivers, sensitivity data is normally based on direct measurement with a bit error rate test set (BERTS). Often, however, a sensitive detector and preamp combination will be packaged and reported to have a given sensitivity, much the same as an optical receiver. In these cases, the sensitivity has been calculated from a measurement of noise spectral density, and an assumed noise bandwidth and detector responsivity. The calculated sensitivity further assumes no penalties for back end receiver implementation, which must be considered in a comparison of "receivers".

5.3.2 FET Front End Receiver Analysis. Most commercial FDDI compatible receivers use a bipolar transimpedance front end. A comparison of available commercial receivers with the SAFENET II requirements indicates that an approach for improved sensitivity should be considered. Both FET based preamplifiers and avalanche photodiodes (APD) can provide increased sensitivity. Since the APD requires a high voltage supply with temperature tracking, its implementation is more suited for packaging formats where footprint is not at a premium and with reduced temperature extremes. Consequently, the FET preamp is considered here asthe approach of choice. Its potential performance is analyzed in the following section.

The following is an estimate of the performance of a practical fiber optic receiver channel utilizing a FET preamplifier when used in an FDDI environment. A block diagram of the receive channel is shown in Figure 7. The general approach to the analysis is as follows:

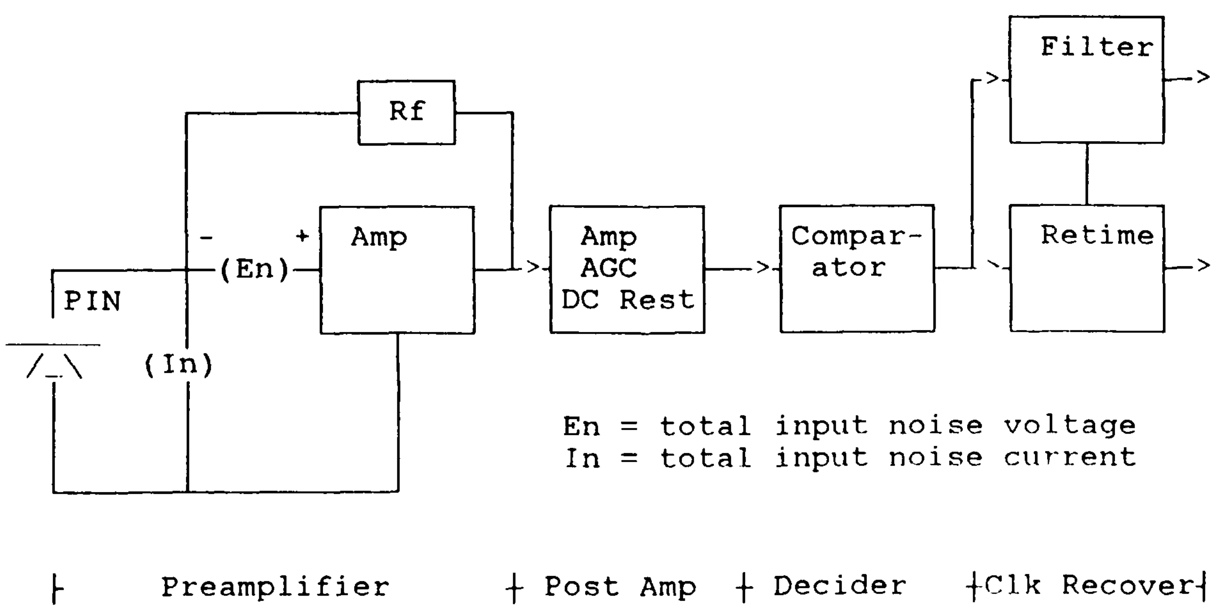


Figure 7. Receive Channel Block Diagram

a. Estimate the sensitivity of the preamplifier based on signal to noise ratio (SNR), preamplifier transfer characteristic (volts/milliwatt, optical), a bit error rate (BER) of 1E-9, and temperature.

b. Derate the preamplifier sensitivity for BER < 1E-9, Rx input jitter, input non-zero optical rise and fall times and input optical extinction ratio. The limits for these parameters have been taken from the FDDI PMD Specification, draft Rev 7.2, (3-30-88).

The methods and assumptions used to calculate the base sensitivity and each of the derating factors are covered in the following sections. The results are summarized in the figures and in Table 8.

PRE-AMPLIFIER SENSITIVITY

The transimpedance preamplifier sensitivity was calculated using the following assumptions and approach:

a. Use of a GaAs, N-channel FET as the amplifier input device.

b. A sequence of APL programs were written and executed to calculate each of four noise components as current or voltage inputs to the preamplifier and as noise voltage outputs from the preamplifier. A total noise output was obtained by assuming the density to be flat over the noise bandwidth of the receiver and the receiver to have an equivalent noise bandwidth of 122 MHz.

The equations and parameters used to compute the value of each of the noise sources are given in the following sections. The general constants are:

Electron Charge (Q) = 1.602E-7 ms ns
Boltzmann´s Constant (Kb) = 1.38E-11 v ma ns /deg K
Temperature (Ta °K) = 273 + Tc(°C)

The resulting noise density is "per root gigaHertz"; multiply by 3.16E-05 to convert to the more familiar "per root Hertz".

c. Feedback resistor (Rf) thermal noise current density:

Inr = ((4 x Kb x Ta/Rf)**.5) ma/root GHz

Inr has been calculated as a function of temperature for three values of Rf: 25K, 20K, and 15K-Ohms.

d. Shot Noise Due to Gate Leakage

It has been assumed that the gate leakage current is 50 na maximum at 25°C and doubles for each 10°C increase in temperature.

Inl = ((2xQxIglx(2**(Tc-25)/10))**0.5

e. FET Channel Conductance Noise (referred to input)

It has been assumed that the "excess noise factor" (Nf) = 1.8, that the transconductance (Gm) is 25 milliMho at 25°C and has a temperature coefficient of -0.5%/°C. Further, it has been assumed that the transconductance is constant over the receiver noise bandwidth.

Ena = ((4xKbxTaxNf)/Gm)**0.5

f. Shot Noise Due to PIN Diode Dark Current

It has been assumed that the PIN diode dark current is 5 na maximum at 25°C and 85 na maximum at 85°C. The dark current at any other temperature was calculated from:

Id = (5E-6)x2**((Tc-25)/14.69)) ma

The noise current density was calculated from:

Ind = (2xQxId)**0.5

g. Preamplifer Total Noise Output:

It has been assumed that all noise sources are flat over the frequency range of interest, that the receiver frequency response is equivalent to a two pole filter with 3 dB bandwidth of 100 MHz. The resulting equivalent noise bandwidth (NBW) is 122 MHz. The effective preamplifier output noise voltage is:

En = {[(RfxInr)**2 + (RfxInl)**2 + (RfxInd)**2 +
+ (Ena)**2] **0.5} x (NBW**0.5)

The significant noise contributors (evaluated for Rf = 20K and referred to the preamplifier output) are shown individually in Figure 8 as a function of temperature. The total output noise is also shown. For the conditions assumed, the preamplifier feedback resistor thermal noise dominates at low temperature and the noise from the FET gate leakage current is dominant at high temperature. The noise due to PIN dark current and due to the FET channel conductance are not significant.

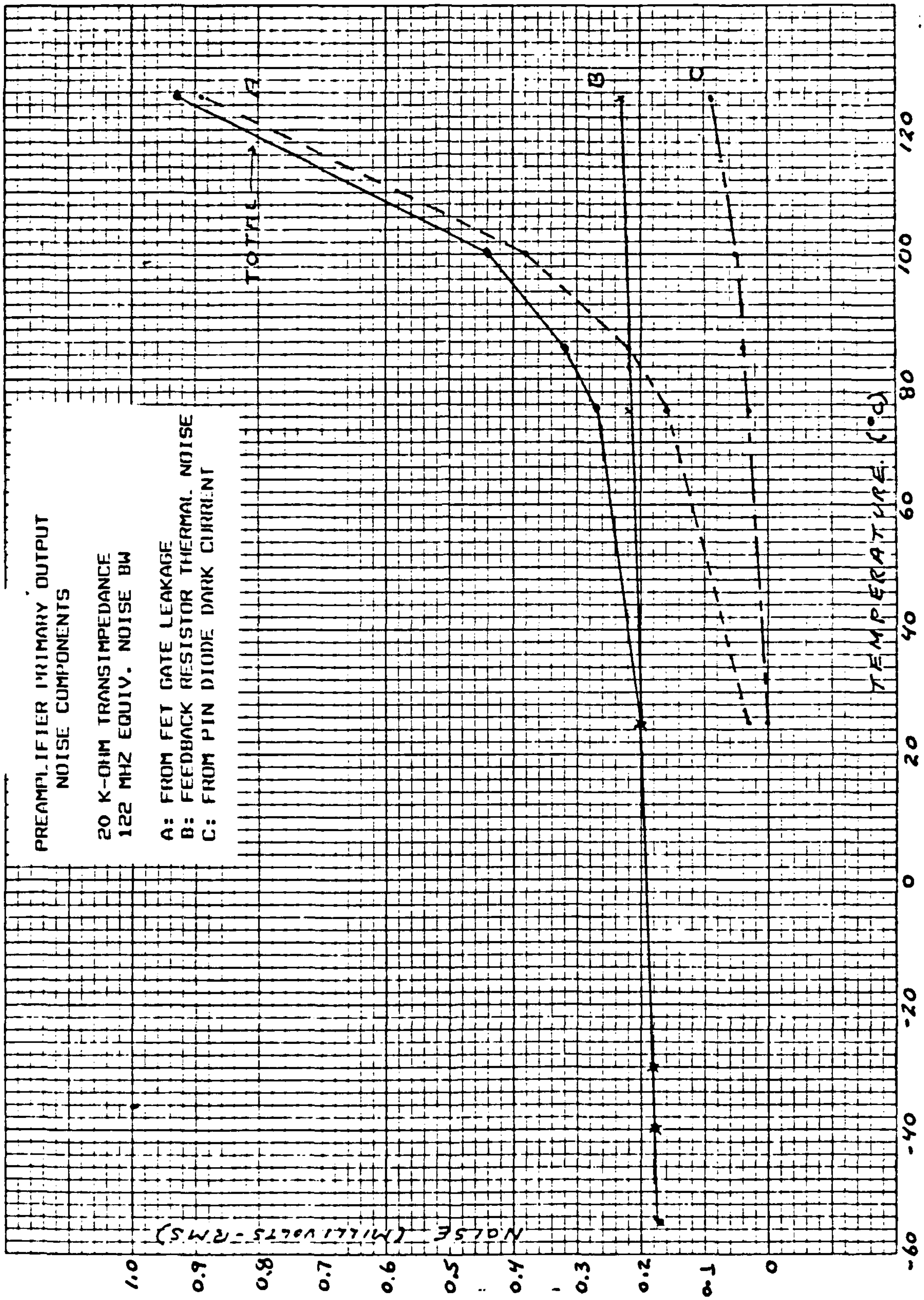


Figure 8. Preamplifier Primary Output Noise Components

PREAMPLIFIER SENSITIVITY

The preamplifier sensitivity is then calculated from:

$$S = 10 \times \log (6 \times En/K) \quad \text{where}$$

S = sensitivity in mw, average at BER = 1E-9
En= total noise in volts
K = preamplifer transfer characteristic = R x Rf
R = PIN diode responsivity = 0.8 ma/mw, minimum
Rf= transimpedance, K-Ohms

It should be noted that this "sensitivity" figure is based strictly on the signal to noise ratio at the preamplifier output and must be derated for a complete receiver operating with less than ideal inputs.

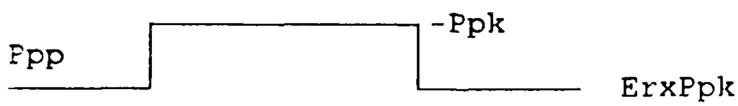
The preamplifier sensitivity for three values of transimpedance is plotted vs temperature in Figure 9. At low temperature, sensitivity is improved by increasing the value of Rf. It can be shown that the change in sensitivity is proportional to the square root of the old and new values of Rf. At high temperatures, no such improvement is seen because gate leakage noise dominates.

TEMPERATURE PENALTY

As can be seen from Figure 9, the variation in sensitivity with temperature (-40°C to 85°C) is -0.6 to +1.9 dB.

NON-ZERO INPUT EXTINCTION RATIO

The FDDI specification defines the transmitter output extinction ratio as 0 to 5%. The effect of a non-zero extinction ratio on the receiver performance has been calculated as follows:



Where: Ppk = peak power input
Ppp = peak-to-peak power input
Er = extinction ratio (0 - 0.05)
Pav = (Ppk + ErxPpk)/2 for 50% duty cycle
Ppp = Ppk - ErxPpk

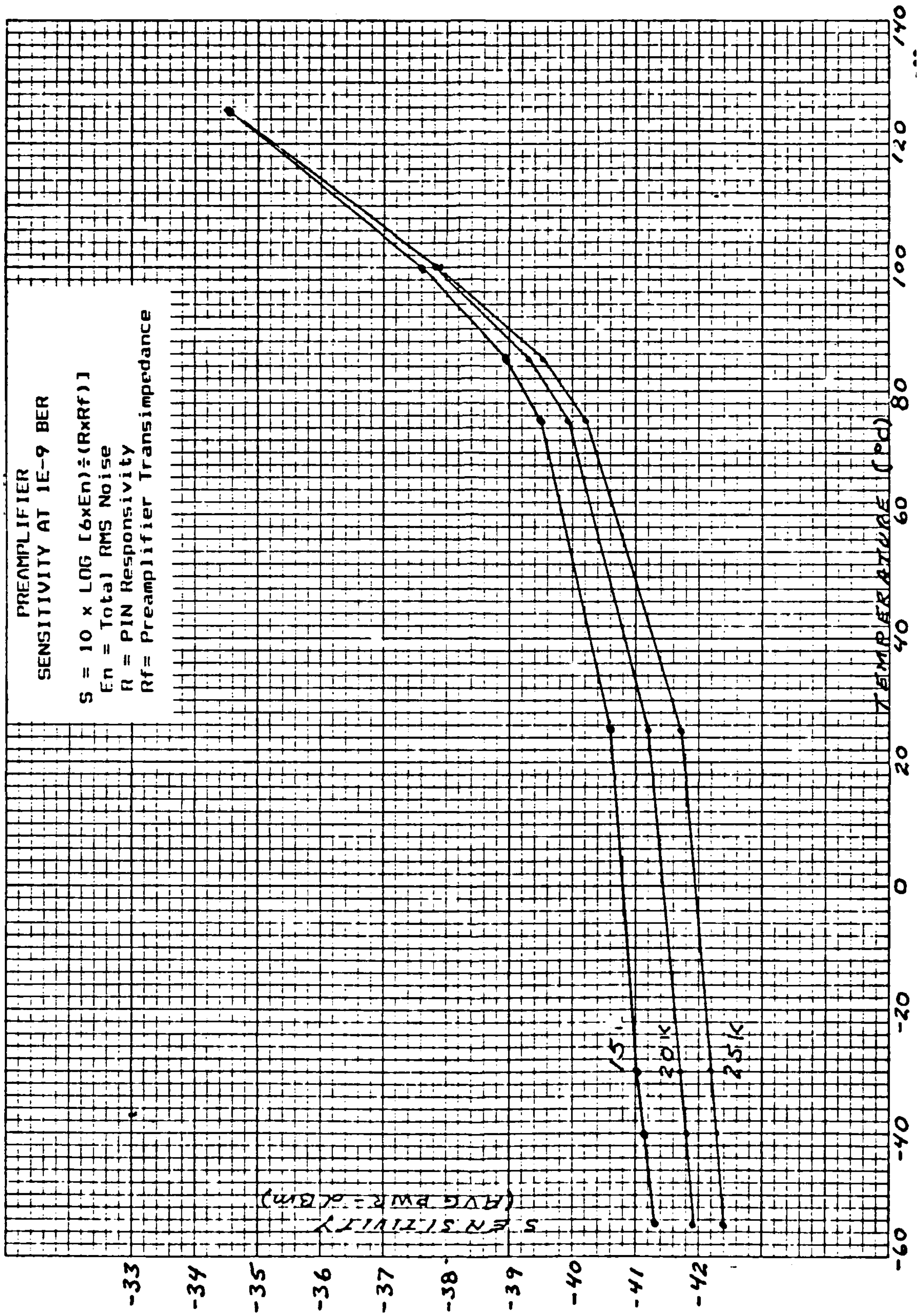


Figure 9. Preamplifier Sensitivity at 1E-9 BER

The question to be answered is how much the average power must be increased, if Er is non-zero, to maintain the same peak-to-peak signal:

$$\begin{aligned} Ppp1 &= Ppp2 \\ Ppk1 - Er \times PPk1 &= Ppk2 - Er2 \times Ppk2 \\ Er1 &= 0 \\ Er2 &= Er > 0 \\ Ppp1 = Pk1 &= Ppk2(1-Er) \qquad (1) \end{aligned}$$

$$Pav1 = Ppk1/2 \quad \text{and} \quad Pav2 = Ppk2 + Er \times Ppk2$$

$$Pav1/Pav2 = 2/Ppk1 \times Ppk2 \times (1+Er)/2 = Ppk2 \times (1+Er)/Ppk1$$

Substituting from (1) above for Pk1:

$$Pav2/Pav1 = (1 + Er)/(1 - Er)$$

If Er = 0.05, then the power penalty is:

$$Sp = 10 \log (1.05/0.95) = 0.43 \text{ dB.}$$

NON-ZERO RISE AND FALL TIMES and NON-ZERO DUTY CYCLE DISTORTION

The FDDI specification defines the rise and fall times of the receiver input as 0.6 to 5 ns. The input duty cycle distortion is specified to be 0 to 1 ns peak to peak.

Two approaches were taken. Both base the penalty on the change of amplitude of the fundamental of an alternating 1/0 data pattern (that is, a 62.5 MHz square wave) as the rise/fall times are increased from 0 to 5 ns. The assumption is that the frequency response of the receiver is such that only the fundamental will be effective at the decider input.

a. First Approach: The receiver input was modelled as a trapezoidal waveform with equal rise and fall times. An APL program was written and executed to compute the amplitude of the fundamental and harmonics as a function of rise/fall time and duty cycle distortion. The resulting penalty was calculated from:

Sp = 10 x log (F1/F2), where F1 = fundamental amplitude with zero rise/fall times and zero DCD, and F2 is the amplitude with non-zero rise/fall times and non-zero DCD. The results are shown in Figure 10.

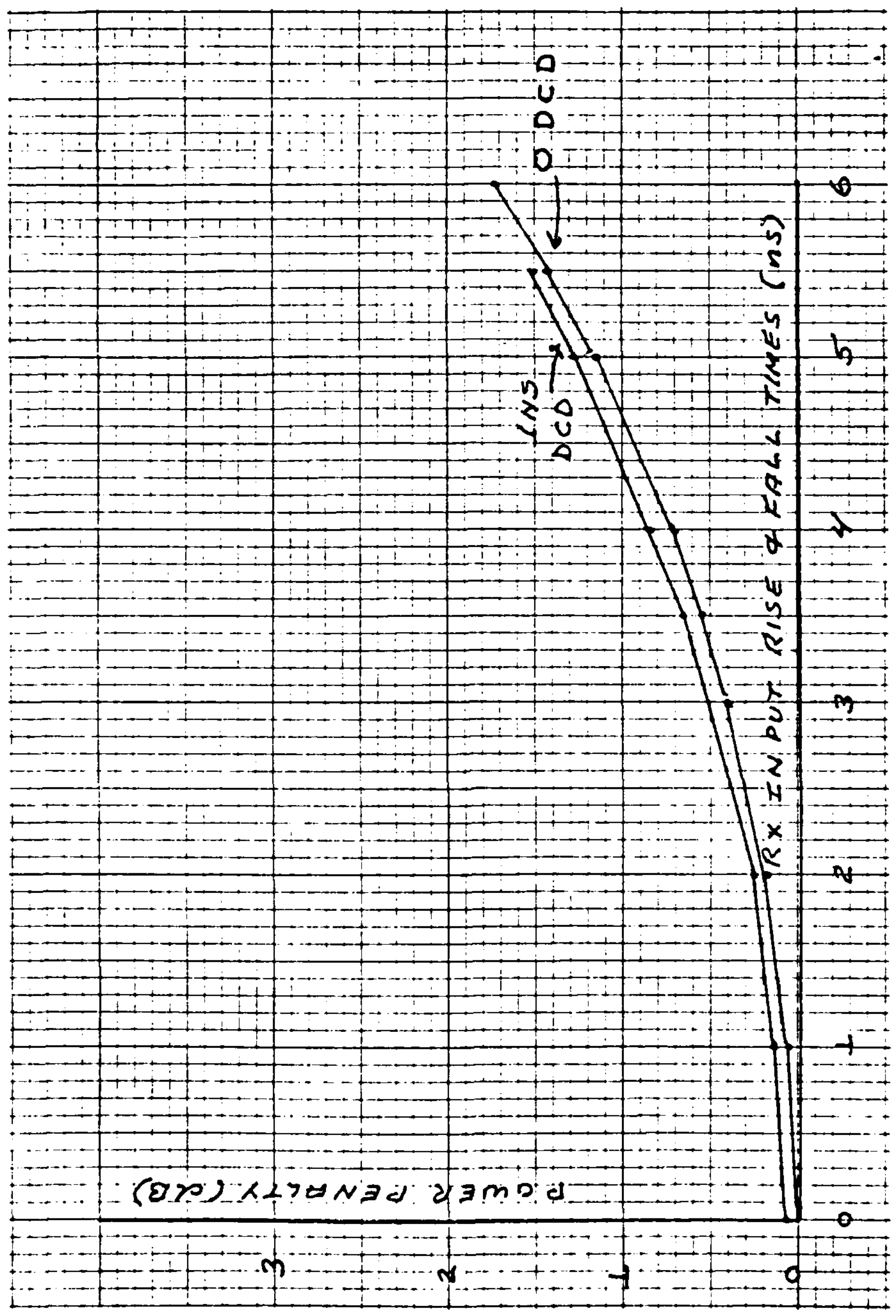


Figure 10. Effect of Rise/Fall Time and DCD

b. Second Approach: As a check on the approach described above, the transmitter output was modelled as a trapezoidal waveform with 3.5 ns rise/fall times (per FDDI specification) and the fiber was modelled as a low pass filter with a bandwidth such as to give, overall, a receiver input rise/fall time of 5 ns:

Trx = transmitter output rise time
Trf = fiber rise time
Trxf = receiver input rise time

Trf = ((Trxf**2))**0.5 = (25 - 12.25)**2 = 3.57 ns

(Circuit simulations have shown that the exact value is 3.5 ns.)

For a single order low pass filter, the filter time constant and pole frequency are related to the 10 to 90% rise time by:

TC = Trf/2.19
Fp = 2.19/(2 x π x Trf)

The magnitude of the attenuation of a single pole filter as a function of frequency is given by:

|G(f)| = 1 / [1 + 2 x π x Trf x F/2.19)**2] **0.5

|G(f)| = 0.847

The amplitude of the fundamental of a 3.5 ns rise time trapezoidal waveform is reduced by 0.881 relative to that from a zero rise time waveform.

Thus, the overall penalty is:

Sp = 10 log ().881 x 0.847) = 1.27 dB

This agreed well with the corresponding penalty using approach a. which is 1.16 dB.

INPUT DATA DEPENDENT JITTER (DDJ), INPUT RANDOM JITTER (RJ), AND CLOCK RECOVERY ACCURACY

The FDDI specification defines the DDJ to be 0 to 1.2 ns peak to peak, and the RJ to be 0.76 ns peak to peak. It has been assumed that the clock recovery circuit will sample the center (point of maximum SNR) of the receiver output pulses within ± 1 ns. The jitter specification has been interpreted as to mean that the input signal can be advanced or delayed by an amount equal to one-half the peak to peak jitter specification.

The power penalty caused by jitter and timing inaccuracy has been evaluated by referring the sampling time and jitter to the input of the deceider circuit and by considering the effect on the signal to noise ratio at the input to the deceider circuit. This approach avoids the complication of translating amplitude and time variations into the phase modulation of the receiver input.

Jitter phase modulates the input to the receiver. It has been assumed that the modulation will be of such a frequency that it is passed through to the decider circuit but that the clock rcovery circuit is undisturbed. An alternating 1/0 input has been assumed. Because of the receiver bandwidth limiting, the input to the decided circuit will be sinusoidal with the ideal instant of sampling occuring at the peak (mid-Baud time). Jitter which does not affect the clock recovery circuit will cause the signal peak to be advanced or delayed and thus the instant of sampling will not correspond to the peak (point of maxomum SNR). Similarly, inaccuracy in the clock recovery circuit will result in sampling at a time which is not optimum. The power penalty can be calculated from:

$$Sp = -10 \times \log [\cos ((Tj + Tcr)/Tb) \times 180^\circ)]$$

Where Tj = total peak jitter
Tcr = peak clock recovery inaccuracy
Tb = Baud time = 8 ns.

For the specified values: Sp = 1.47 dB

NON-IDEAL POST AMPLIFIER AND IMPLEMENTATION LOSS

The preceeding sections have dealt with the sensitivity penalties which are dependent upon receiver input conditions and which effectively reduce input power. Some allowance must be made for a non-ideal implementation, but this penalty is much harder to quantify for the general case since it depends upon specific circuit design and element selection as well as trade-offs between performance and circuit complexity. For example:

a. The input offset voltage and current of the decider circuit can introduce a significant penalty. this penalty can be made insignifican if the gain of the receiver is kept sufficiently high. This may require the use of some form of AGC and, hence, increased circuitry.

b. All of the optical power available at the input fiber may not reach the PIN diode or be effective. The coupling efficiency will depend upon the size of the fiber, PIN active area, coupling mechanism (fixed pigtail vs connector), and the precision with which the receiver has been assembled.

c. The receiver amplifiers will not be exactly linear in phase and thus a data dependent jitter over and above that which has been considered here will be introduced.

d. To handle the continuous 40% to 60% duty cycle allowed by the FDDI data encoding implies the need for a dc coupled receiver or, more likely, some form of dc restore. In either case, the circuitry will not be perfect and some additional penalty will be introduced.

e. There needs to be some margin between the expected performance and whatever acceptance test limits are imposed.

f. To account for the imperfection in implementation, an additional 0 to 1.5 dB penalty has been added to the performance losses.

The receive channel performance is summarized in Table 8. Note that the largest penalty in Table 8 is highly dependent on the required operating temperature range specified for the receiver, and also on the value assumed for the FET gate leakage. Other penalties may be takes as variable, as the range given implies, and will depend on actual receiver implementation. Manufacturable performance (and cost!) can also depend on the ability and willingness to select premium performance devices, such as detectors and FETs, and the acceptable yield of the overall manufacturing process.

5.3.3 Experimental. In order to verify and illustrate some of the sensitivity penalities that can be imposed on a receiver by the FDDI requirements, samples of a commercial FDDI compatible bipolar transimpedance preamp receiver and an IBM FET transimpedance preamp receiver breadboard were checked in the test setup of Figure 11.

ITEM	SENSITIVITY (avg power)	PENALTY (dB)
FET Preamplifier @ 20K Transimpedance 25°C, 1E-9 BER	-41.2 dBm	
Decrease BER to 2.5E-10		0.2
Operating Temperature (-40°C to 85°C)		-0.6 to 1.9
Non-zero Input Rise/Fall Times (5 ns max)		0.0 to 1.2
Non-zero Extinction Ratio (5% max)		0.0 to 0.4
Input Duty Cycle Distortion (0 to 1 ns peak)		0.0 to 0.1
Input Data Dependent Jitter Random Jitter, Clock Recovery Accuracy		0.0 to 1.5
Implementation Loss		0.0 to 1.5
RECEIVE CHANNEL SENSITIVITY RANGE	-41.6 dBm to -34.4 dBm	

Table 8. Receive Channel Sensitivity Performance Summary

Selected data patterns are clocked out of the BERTS into the FDDI fiber optic Tx. The Tx optical output passes through the interconnecting fiber optic network into the receiver under test. An AMD AM7985A FDDI ENDEC Data Separator (EDS) chip is used to recover clock from the data stream and retime the data. Data and clock are fed back to the BERTS where the data is compared to the transmitted data and bit errors are collected. In a normal BER test, the recovered data is resampled directly in the BERTS; the AM7985A clock recovery stage has been added to simulate the complete SAFENET receive channel.

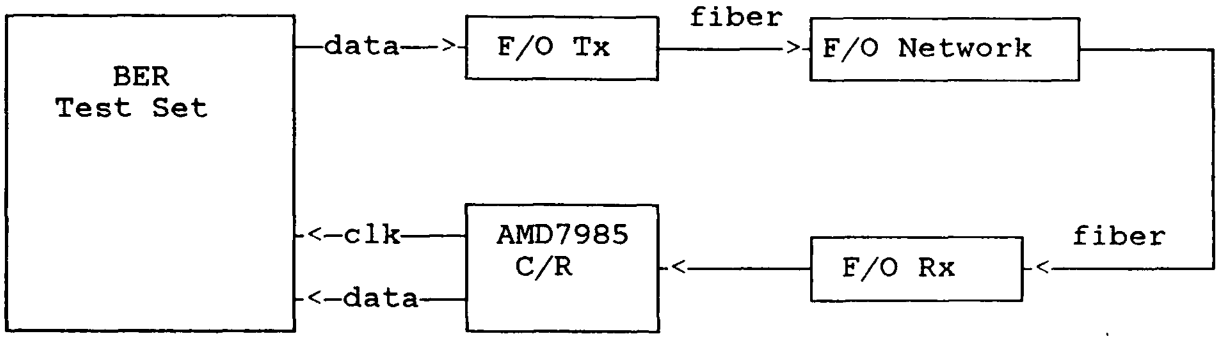


Figure 11. F/O Receiver Sensitivity Test Set Up

4.3.4 Test Proceedure. Three commercial FDDI bipolar receivers and the FET preamp breadboard were each tested as follows:

Test 1. - Fast rise and fall, PRBS - A 2E7-1 PSBS from the BERTS drives the Tx. The optical signal is passed through the SAFENET breadboard in the 5-node-bypass mode, without additional cable lengths, and used as the input to the receiver under test. Measured optical rise and fall times at the receiver input were 1.1 ns and 2.0 ns respectively. This approximates the usual "spec sheet" conditions for sensitivity measurement except that the clock recovery stage is included and the optical extinction ratio is undetermined. The average input optical power at the receiver is decreased by introducing additional attenuation in the fiber network until bit errors can be accumulated by the BERTS. The BER for several power levels is plotted.

Test 2. - Maximum rise, fall times and PRBS - With the same input data stream to the transmitter, a several hundred foot length of 100/140/.29 step index fiber was interposed between the transmitter output and the fiber optic network, and tuned for a measured 4.9 ns rise time and a 5.1 ns fall time. This approximates the maximum 5.0 ns input rise and fall time allowed at the receiver by the FDDI PMD specification. The step index fiber was introduced after a measurement of the network rise/fall times with the additional 1.2 km of graded index fiber showed little additional bandwidth penalty with the transmitter at room temperature. By comparing the BER curve with the results from test 1, the sensitivity penalty for receiver input rise and fall time can be determined.

Test 3. - Unbalanced data pattern - While the PRBS in tests 1 and 2 is, in the long term, DC balanced, or 50% duty cycle, the FDDI 4B/5B NRZI code allows a long term unbalance between 40% and 60% duty cycle. These extremes are likely to be more difficult for the receiver to handle than the test pattern in the FDDI PMD Appendix, and we use them here to simulate a worst case data pattern. A pattern generator is added to the test setup to introduce a 10-bit 1011010110 60% duty cycle word, or its inverse and the transmitted optical data stream is maintained in the fast rise time mode. Average optical input power is measured using a 50% duty cycle pattern. The penalty for unbalanced data pattern is determined from the BER curve.

Test 4. - Unbalanced data pattern and maximum rise and fall - The conditions of tests 2 and 3 are combined to determine to what extent the effects of unbalanced data and maximum rise and fall are additive.

5.3.5 Results. The BER curves for the three bipolar and one FET receivers are shown as Appendix C. The sensitivity extrapolated to 2.5E-10 BER for the 4 tests is summarized in the following table 9.

4.3.6 Discussion. In drawing conclusions from the receiver data, it is important to keep in mind that the tests are not intended to be comprehensive enough to be considered a valid receiver evaluation exercize. The tests are intended to show a potential for improved sensitivity using a FET front end, consistent with the previous analysis, and that derating penalties need to be applied to nominal receiver sensitivity data, whether bipolar or FET. Two sources of such penalties have been demonstrated.

TEST	BIPOLAR			FET
Vendor Test Data (1.)	-36.7	-36.2	-36.3	---
1. Fast Tr,Tf; PRBS	-36.5	-35.4	-35.8	-39.0
2. Slow Tr, Tf; PRBS	-35.2	-34.8	-35.5	-38.7
3a. Fast Tr, Tf; 40% D.C.	-35.7	-36.0	-35.7	-38.3
3b. Fast Tr, Tf; 60% D.C.	-34.8	-35.4	-35.1	-37.4
4a. Slow Tr, Tf; 40% D.C.	-34.2	-33.6	-34.3	-38.3
4b. Slow Tr, Tf; 60% D.C.	-32.5	-32.7	-32.7	-37.9

Note 1. Vendor data at 1E-9 BER extrapolated by 0.2 dB

Table 9. Receiver Sensitivity (dBm, ave., 2.5E-10 BER) vs. Tr, Tf and Data Pattern

The lack of correspondence between the vendor test data and our measurements (test 1) may be due to the fact that our test setup includes a separate clock recovery stage (the AMD FDDI chip), or it may be due to other differences in the test setup not immediately apparent. The significance is between the nominal test 1 data and the tests with maximum allowed optical rise and fall times, and unbalanced data sequences.

In comparing the sensitivities of the bipolar and FET approaches, note that the FET front end has been designed against a stringent (24.4 dB) dynamic range requirement and is not optimized for sensitivity. Also, performance may improve when implemented in a hybrid format. It should be assumed that both the bipolar and FET receivers represent nominal or average parts. No information can be inferred about performance spread due to device characteristics or manufacturing tolerances. From the analysis of sect.5.3.2 the sensitivity of the FET front end noise is apparent. The projected performance of the FET will depend critically on the high temperature limits imposed by the electronic packaging format.

5.3.7 Transmitter. Since it is not clear that an optical receiver meeting the SAFENET II -39.0 dBm requirement is a realistic goal, the possibility of launching additional power from the transmitter to maintain the design link budget becomes an important issue. Specifically, the issue is: how much power can be launched into the 62.5/125/.275 fiber while staying within the rise time, wavelength and spectral width envelope of the FDDI PMD specification over the full temperature range of operation. The envelope assures that the system bandwidth does not fall below 90 Mhz at the 2 km fiber length, due principally to chromatic dispersion in the fiber. In general, output power is the limiting factor at high temperature, and wavelength shift towards higher fiber dispersion at low temperature limits the allowable risetime and spectral width.

Our best available guidance in this respect is that we are currently designing a 125 MBaud transmitter to launch into 100/140/.29 GI fiber with a minimum launched power of -12.0 dBm average at 75°C. Typically, the difference in launched power for these SLEDs between 62.5 um and 100 um fiber is about 4 dB and depends strongly on the coupling optics. As a check, the maximum coupled power to SAFENET fiber for two LEDs was measured. One LED was a standard lensed commercial package oiptimized for 62.5 um fiber. The second LED, uncased, was coupled using an SLH 1.8 0.32 pitch Graded Index (GRIN) lens. At the same time, the fiber cable into which the power was launched was given a variable wrap around a smooth mandrel as a mode filter to estimate the amount of additional attenuation that might be introduced by intracabinet fiber bends, and its effect on the system loss. The results are shown in Table 10.

Note that the coupled power in Table 10 is CW and is equivalent to -14.9 dBm average and -13.6 dBm average for the vendor and GRIN lens coupled LEDs respectively. These may be considered typical values and do not reflect production tolerances or high temperature operation.

The mandrel wrap data was taken not to suggest the use of a mode filter, but to estimate the effects of fiber bends in the transmit fiber inside an equipment cabinet. The pigtail loss values are a measure of the loss in the mandrel wrap as measured at the FOIC and being launched into the network. The network loss values are the excess loss produced by the mandrel wrap but measured at the receive end of the network. The relatively decreased effect of the mandrel wrap at the receive end vs the launch end indicates that much of the high order mode loss has shifted from the network back to the mandrel wrap mode filter. These kinds of effects should be taken into account when designing a network which includes intracabinet fiber.

LED Coupling	Mandrel Diameter	Number of Turns	Loss (dB) Pigtail	Loss (dB) Network
VENDOR PACKAGE P= -11.9 dBm, CW	0.5 inch	0.25	0.75	0.15
		0.50	0.96	0.19
		1.0	1.20	0.26
		2.0	1.45	0.32
	1.0 inch	0.25	0.35	0.10
		0.50	0.51	0.15
		1.0	0.60	0.17
		2.0	0.72	0.20
UNCASED LED SLH LENS P= -10.6 dBm, CW	0.5 inch	0.25	0.77	0.19
		0.50	1.02	0.22
		1.0	1.31	0.31
		2.0	1.58	0.39
	1.0 inch	0.25	0.40	0.06
		0.50	0.53	0.08
		1.0	0.74	0.12
		2.0	0.83	0.17

Table 10. LED - Fiber Coupling and Mandrel Wrap Effects

6.0 PACKAGING CONSIDERATIONS

The SAFENET II network description and loss budget is defined as FOIC to FOIC and includes the FOIC loss. This is consistent with a commercial FDDI installation in which the fiber optic transmitter and receiver are an integral part of the mating component to the equivalent of an FOIC. This is unlikely to meet the packaging requirements of most platform installations of SAFENET, especially if the MIL-C-28876 box connector is used as specified.

Assuming that the fiber optic transmitter and receiver will be included on an electronic page assembly, there are two options for connecting the fiber optic components to the FOIC: (1) The Tx/Rx may be connected directly with the mating FOIC connector, or (2) the page assembly may include fiber optic contacts as part of the card edge (backpanel) connector.

If the Tx/Rx connected directly to the FOIC is pigtailed, the pigtail must be terminated with the contact for the box mounted MIL-C-28876 connector. When the page is installed or removed, the contact must be removed from the box connector insert with a special tool and the pigtail is removed with the page. If the Rx/Tx is connectorized, the fiber/cable can be disconnected at the page. In either case, the fiber must be disconnected when the page is removed and represents some potential for accidential damage. Since in either case, the Tx/Rx optical performance is specified in the attatched fiber, the required Rx/Tx performance is identical to that specified in the SAFENET Handbook.

Many electronic systems have a Standard Electronic Module (SEM) packaging format specified (Eg., SEM-D, SEM-E). In order to stay within the usual 0.3 Or 0.6 in page pitch, component height is restricted (to about .2 in) such that a standard connectorized fiber optic component cannot be accomodated without severe restrictions on placement within the cabinet. It is customary for these formats to provide optical contacts in the backplane connector. Connectors with cavities for MIL-T-29504 termini are available and allow the page to be installed and removed without concern for the fiber optics. However, the introduction of the contacts produces an additional joint loss which must modify the optical performance as seen at the FOIC. Approximately 1 dB of additional loss (maximum) should be allowed for both the transmitter and receiver, although the usual difference between the average transmit and receive losses will be apparent due to HOM losses.

7.0 CONCLUSIONS AND RECOMMENDATIONS

1. Based on the specific breadboard components tested,the passive component loss budget from Apendix F, Safenet II Handbook (MCCR-0036-Draft) appears to be valid as a worst case (maximum loss) budget. Considering the system design margin and the expected (mean) component loss, the most probable link performance is considerably better than the worst case analysis would indicate.

2. The actual fiber optic cable plant installation should be specified as a maximum FOIC-to-FOIC loss (probably FOIC[n] to FOIC[n+2]), not on an individual component basis. This loss specification should be modified from the Handbook loss budget to reflect the difference between precision test connectors and the allowed loss for a mated box-cable pair of half connectors. Two possible ways to ensure a good quality installation are (1) Require rework of abnormally high component losses as probed with an OTDR, or (2) specify an additional mean path loss for the system that is consistent with the expected loss values, not worst case.

3. While the minimum splice loss for the rotary mechanical splice should be obtained using matching ferrules (splice halves), splices made with unmatched ferrules do not appear to be enough more lossy to significantly impact the network operation. The difference in splice loss is likely to be overshadowed by small differences in cable and switch pigtail fibers.

4. Specifications for the active components, ie., transmitter and receiver, need to be adjusted. More launched power than -18 dBm avg. is achievable; -39.0 dBm avg. receiver sensitivity does not appear to be realistic. Receiver performance needs to be specified and tested under worst case data pattern and environmental conditions. The receiver channel must include the symbol synchronization or clock recovery process. A FET preamplifier design appears to be the best approach, although there are serious high temperature performance issues for both the receiver and transmitter. Realistic performance figures for active components which are manufacturable at reasonable yield, meet worst case application requirements including environmental factors, and are packaged to be compatible with the electronic packaging format, cannot be determined prior to development and hybrid prototype evaluation. It is not clear at what cost the present 21.0 dB link budget can be supported.

5. Survivability of the physical network, ie., the ability to sustain communications integrity through the loss of node electronics or loss of optical continuity, is as much a function of system design as optical margin. The capability to bypass groups of nodes in a hierarchical fashion, and to interpose fiber optic regenerators as required can provide a higher level of network survivability than the ability to bypass a couple of contiguous nodes more or less. This generally implies the grouping of bypass switch functions of various configurations and regenerators into ring "concentrators". The optimum network configuration is platform specific.

6. Environmental and packaging requirements for the transmitter and receiver are determined by the packaging format requirements for the electronics. The case temperature range over which the active components must meet the specified optical performance is derived from a thermal analysis of the interface card and depends on the card thermal environment, the thermal impedances between the component and the card thermal sink, and the power dissipation of all the card components.

APPENDICES

APPENDIX A

ROTARY MECHANICAL SPLICE TEST DATA

Mated pair	Max	Min	Delta	"Tabbed"
L1-A1	0.46	0.07	0.39	0.09
L2-A1	0.18	0.01	0.17	0.01
A2-B1	0.27	0.06	0.21	0.26
-B2	0.16	0.1	0.06	0.14
-C1	0.22	0.07	0.15	0.15
-C2	0.44	0.24	0.2	0.29
-D1	0.39	0.13	0.26	0.24
-D2	0.24	0.03	0.21	0.19
-E1	0.36	0.07	0.29	0.16
-E2	0.26	0.08	0.18	0.22
-F1	0.24	0.06	0.18	0.07
-F2	0.29	0.08	0.21	0.19
L1-A2	0.36	0.07	0.29	0.15
L2-A2	0.2	0.06	0.14	0.11
A1-B1	0.36	0.06	0.3	0.19
-B2	0.32	0.25	0.07	0.29
-C1	0.39	0.1	0.29	0.15
-C2	0.57	0.23	0.34	0.5
-D1	0.86	0.09	0.77	0.56
-D2	0.35	0.07	0.28	0.17
-E1	0.53	0.04	0.49	0.49
-E2	0.53	0.07	0.46	0.14
-F1	0.36	0.11	0.25	0.28
-F2	0.36	0.12	0.24	0.33
L1-B1	0.36	0.06	0.3	0.2
L2-B1	0.26	0.08	0.18	0.25
B2-C1	0.25	0.13	0.12	0.16
-C2		0.27		0.34
-D1	0.33	0.23	0.1	0.33
-D2	0.24	0.04	0.2	0.12
-E1	0.34	0.14	0.2	0.23
-E2	0.18	0.13	0.05	0.17
-F1	0.23	0.07	0.16	0.1
-F2	0.27	0.1	0.17	0.21
L1-B2	0.16	0.02	0.14	0.06
L2-B2	0.14	0.09	0.05	0.1
B1-C1	0.38	0.1	0.28	0.29
-C2	0.55	0.19	0.36	0.53
-D1	0.49	0.16	0.33	0.42
-D2	0.26	0.1	0.16	0.1
-E1	0.43	0.12	0.31	0.34
-E2	0.3	0.08	0.22	0.11
-F1	0.26	0.17	0.09	0.24
-F2	0.34	0.1	0.24	0.18
L1-C1	0.44	0.1	0.34	0.34
L2-C1	0.29	0.08	0.21	0.28

ROTARY MECHANICAL SPLICE TEST DATA (Cont'd)

C2-D1	0.63	0.11	0.52	0.35
-D2	0.43	0.15	0.28	0.4
-E1	0.66	0.04	0.62	0.31
-E2	0.46	0.2	0.26	0.32
-F1	0.54	0.19	0.35	0.2
-F2	0.55	0.2	0.35	0.45
L1-C2	0.64	0.1	0.54	0.3
L2-C2	0.57	0.19	0.38	0.32
C1-D1	0.43	0.1	0.33	0.16
-D2	0.38	0.07	0.31	0.13
-E1	0.43	0.09	0.34	0.25
-E2	0.38	0.07	0.31	0.15
-F1	0.29	0.1	0.19	0.19
-F2	0.26	0.05	0.21	0.11
L1-D1	0.52	0.09	0.43	0.2
L2-D1	0.45	0.17	0.28	0.2
D2-E1	0.38	0.12	0.26	0.25
-E2	0.25	0.05	0.2	0.08
-F1	0.21	0.09	0.12	0.19
-F2	0.22	0.06	0.16	0.08
L1-D2	0.3	0.14	0.16	0.24
L2-D2	0.26	0.09	0.17	0.15
D1-E1	0.59	0.06	0.53	0.43
-E2	0.42	0.1	0.32	0.24
-F1	0.39	0.13	0.26	0.17
-F2	0.42	0.12	0.3	0.4
L1-E1	0.42	0.02	0.4	0.07
L2-E1	0.34	0.1	0.24	0.2
E2-F1	0.2	0.07	0.13	0.18
-F2	0.21	0.1	0.11	0.13
L1-E2	0.32	0.04	0.28	0.2
L2-E2	0.14	0.03	0.11	0.11
E1-F1	0.39	0.19	0.2	0.21
-F2	0.48	0.12	0.36	0.46
L1-F2	0.26	0.02	0.24	0.02
L2-F2	0.16	0.01	0.15	0.03
L1-F1	0.28	0.09	0.19	0.21
L2-F1	0.19	0.08	0.11	0.13
Ave.:	0.357	0.102	0.251	0.223
Sigma:	0.138	0.057	0.141	0.120

APPENDIX B - NETWORK BREADBOARD TEST DATA

Trial #1 RMS Ferrules matched Switch 2-6: bypass	
Splice (+Switch)	Loss (dB)
29504	0.33
FOIC	1.22
L1-Bl1 + BlOr1	0.72
Or1-A1	0.16
A2-Rd2 + RdOr2	0.60
Or2-B1	0.08
B2-Rd3 + RdOr3	0.78
Or3-C1	0.22
C2-Rd4 + RdOr4	0.41
Or4-D1	0.10
D2-Rd5 + RdOr5	0.88
Or5-E1	0.29
E2-Rd6 + RdOr6	0.59
Or6-F1	0.17
F2-Rd1 + RdOr1	0.83
Gr1-L2	0.10
FOIC	0.69
29504	0.78

Trial #2 RMS Ferrules matched Switch 2-6: normal	
Splice (+Switch)	Loss (dB)
29504	0.33
FOIC	1.22
L1-Bl1 + BlOr1	0.67
Or1-A1	0.14
A2-Rd2 + RdGr2	0.68
Gr1-Bl1 + BlOr2	0.85
Or2-B1	0.19
B2-Rd3 + RdGr3	0.72
Gr3-Bl3 + BlOr3	0.39
Or3-C1	0.15
C2-Rd4 + RdGr4	0.40
Gr4-Bl4 + BlOr4	0.73
Or4-D1	0.16
D2-Rd5 + RdGr5	0.57
Gr5-Bl5 + BlOr5	0.68
Or5-E1	0.18
E2-Rd6 + RdGr6	0.50
Gr6-Bl6 + BlOr6	0.58
Or6-F1	0.19
F2-Rd1 + RdGr1	0.85
Gr1-L2	0.10
FOIC	0.65
29504	0.93

TTrial #3 RMS Ferrules matched Switch 2-6: bypass LED/Detector reversed	
Splice (+Switch)	Loss (dB)
29504	---
FOIC	---
L1-Gr1 + RdGr1	1.42
Rd1-F2	0.26
F1-Or6 + OrRd6	0.52
Rd6-E2	0.13
E1-Or5 + OrRd5	1.16
Rd5-D2	0.21
D1-Or4 + OrRd4	0.39
Rd4-C2	0.10
C1-Or3 + OrRd3	0.78
Rd3-B2	0.21
B1-Or2 + OrRd2	0.52
Rd2-A2	0.10
A1-Or1 + OrBl1	0.55
Gr1-L2	---
FOIC	---
29504	---

Trial #4 RMS Ferrules matched Switch 2-6: normal LED/Detector reversed	
Splice (+Switch)	Loss (dB)
29504	---
FOIC	---
L1-Gr1 + RdGr1	1.35
Rd1-F2	0.31
F1-Or6 + OrBl6	0.71
Bl6-Gr6 + GrRd6	0.53
Rd6-E2	0.15
E1-Or5 + OrBl5	0.55
Bl5-Gr5 + GrRd5	0.88
Rd5-D2	0.20
D1-Or4 + OrBl4	0.70
Bl4-Gr4 + GrRd4	0.52
Rd4-C2	0.16
C1-Or3 + OrBl3	0.40
Bl3-Gr3 + GrRd3	0.56
Rd3-B2	0.18
B1-Or2 + OrBl2	0.40
Bl2-Gr2 + GrRd2	0.51
Rd2-A2	0.20
A1-Or1 + OrBl1	0.56
Gr1-L2	---
FOIC	---
29504	---

Trial #5 RMS Ferrules Unmatched Switch 2-6: bypass Cables A-F Reversed	
Splice (+Switch)	Loss (dB)
29504	---
FOIC	---
L1-B11 + BlOr1	0.61
Or1-A2	0.15
A1-Rd2 + RdOr2	0.66
Or2-B2	0.25
B1-Rd3 + RdOr3	0.82
Or3-C2	0.25
C1-Rd4 + RdOr4	0.42
Or4-D2	0.19
D1-Rd5 + RdOr5	1.01
Or5-E2	0.32
E1-Rd6 + RdOr6	0.55
Or6-F2	0.17
F1-Rd1 + RdOr1	0.94
Gr1-L2	---
FOIC	---
29504	---

Trial #6 RMS Ferrules Unmatched Switch 2-6: normal Cables A-E moved	
Splice (+Switch)	Loss (dB)
29504	---
FOIC	---
L1-B11 + BlOr1	0.61
Or1-Rd2 + RdGr2	0.84
Gr2-A1	0.25
A2-B12 + BlOr2	1.03
Or2-Rd3 + RdGr3	0.81
Gr3-B1	0.24
B2-B13 + BlOr3	0.40
Or3-Rd4 + RdGr4	0.47
Gr4-C1	0.12
C2-B14 + BlOr4	0.65
Or4-Rd5 + RdGr5	0.70
Gr5-D1	0.19
D2-B15 + BlOr5	0.44
Or5-Rd6 + RdGr6	0.38
Gr6-E1	0.15
E2-B16 + BlOr6	0.61
Or6-Rd1 + RdGr1	0.89
Gr1-L2	---
FOIC	---
29504	---

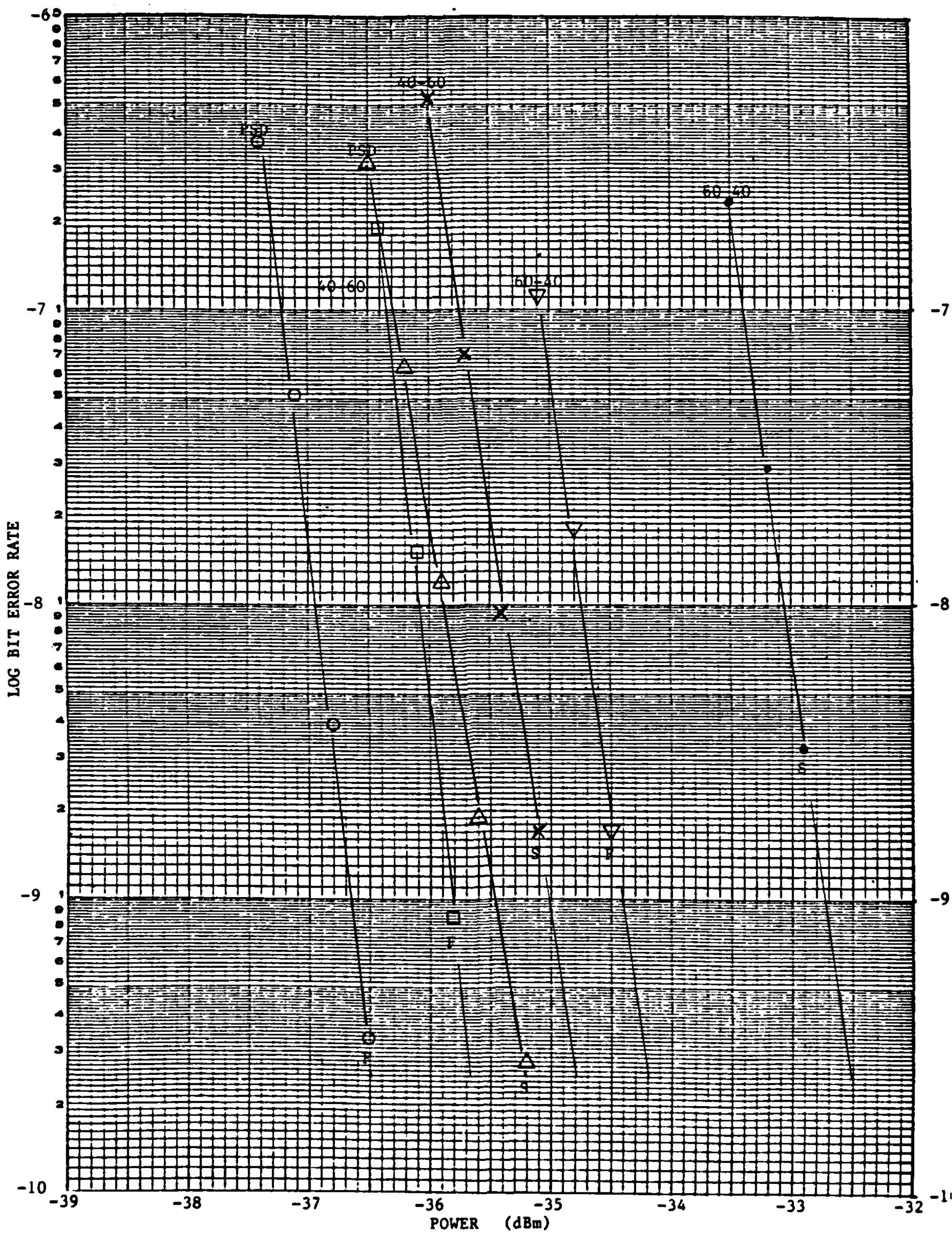


Figure C-1. BER Curves, Bipolar Receiver #1

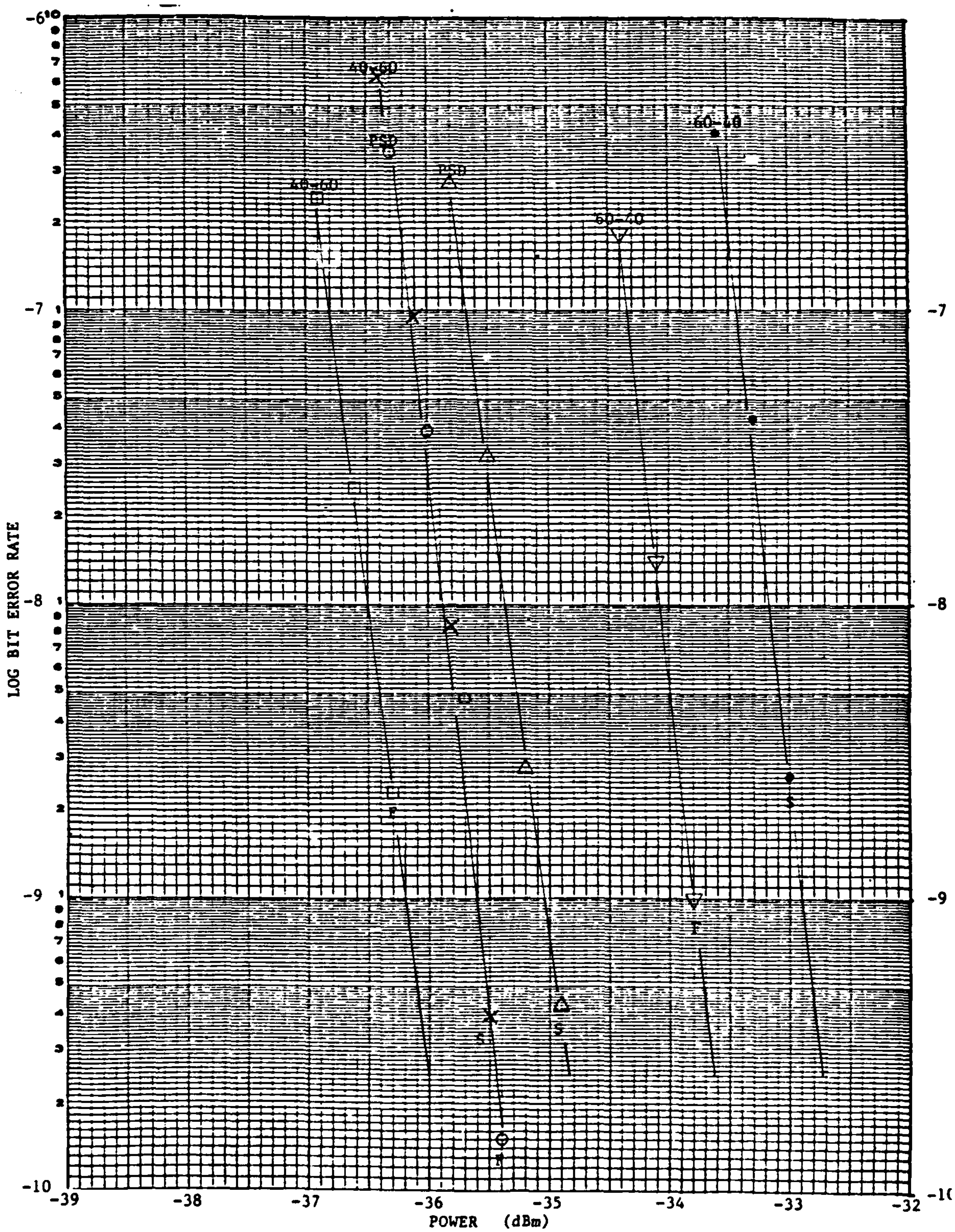


Figure C-2. BER Curves, Bipolar Receiver #2

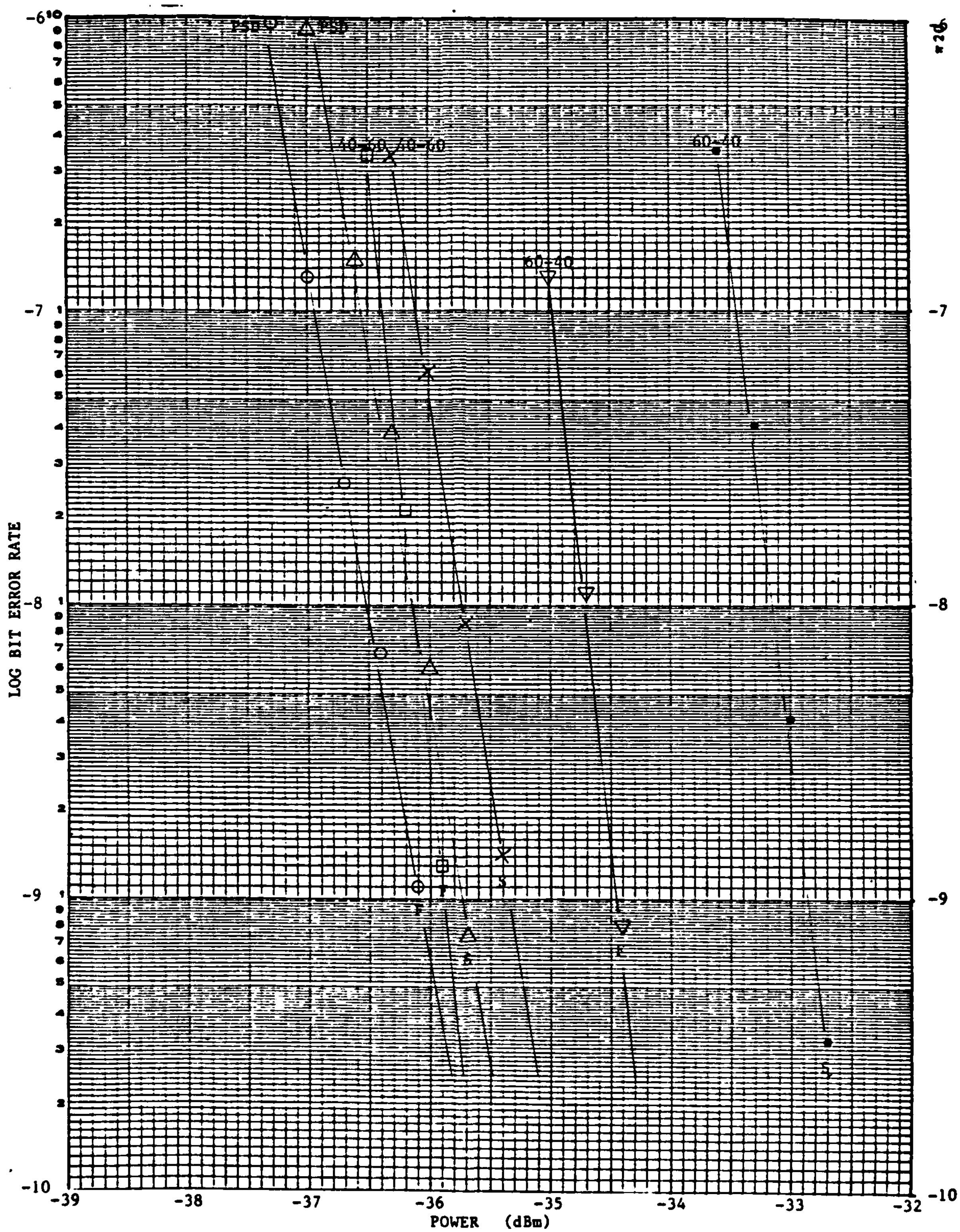


Figure C-3. BER Curves, Bipolar Receiver #3

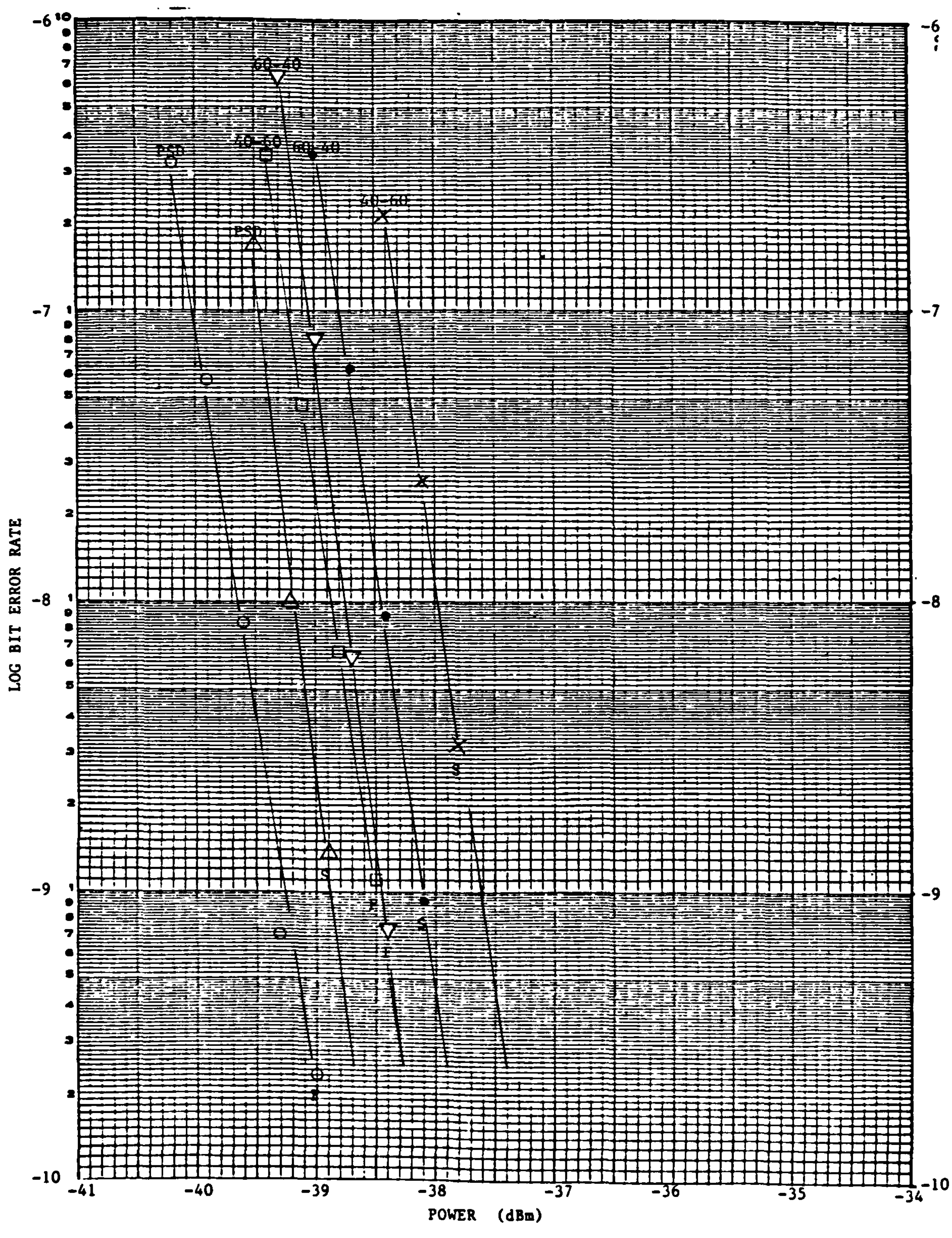


Figure C-4. BER Curves, FET Receiver Breadboard