

AD-A237 946



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MONOLITHIC INTEGRATION  
OF  
SEMICONDUCTOR AND SUPERCONDUCTOR COMPONENTS

DARPA/ONR Contract No. N00014-90-C-0226

Honeywell Sensor and System Development Center  
10701 Lyndale Avenue South  
Bloomington, MN 55420

1 April 1991 - 30 June 1991

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Department: Norman A. Foss *N.A. Foss* Phone #: 612/887-6424

91-04250

## 2.0 PROGRAM SUMMARY

The goal of the program is to develop transistor technology compatible with high transition temperature superconductor technology so that transistor pixel switches can be integrated with  $\text{YBa}_2\text{Cu}_3\text{O}_7$  superconducting microbolometers in the same silicon substrate. A 4x4 matrix-addressable superconducting microbolometer array will be delivered at the completion of the program.

## 3.0 PROGRAM STATUS

### Task 1.0: Vendor Selection

Mary Weybright, a graduate student in electrical engineering at Stanford University working under the direction of Prof. James D. Plummer, has been engaged as a consultant to model the performance of bipolar transistors at low temperature, in order to determine doping profiles needed for the transistor switches at each pixel.

Monolithic bipolar transistors from a potential vendor, ECI of Santa Clara, CA, have been tested after being subjected to  $700^\circ\text{C}$  for one hour. This heat treatment, which corresponds to that to be used in depositing  $\text{YBa}_2\text{Cu}_3\text{O}_7$  on silicon substrates containing the transistors, did not change the device performance at room temperature.

A preferred vendor for the monolithic bipolar transistors has been identified. Honeywell's Micro Switch Division of Richardson, Texas is capable of performing this work, and will charge a lower price than any other vendor. Government approval has not yet been obtained for Honeywell Micro Switch to perform this work.

### Task 2.0: First Fabrication Run

#### Task 2.1: Film Development

Superconducting films of  $\text{YBa}_2\text{Cu}_3\text{O}_7$  have been grown in-situ on 3 - inch silicon wafers coated with amorphous silicon nitride and polycrystalline yttria stabilized zirconia. These films show onset of superconductivity at  $\sim 88\text{ K}$  and zero resistance at  $\sim 65\text{ K}$ . The temperature coefficient of resistance (TCR) is about  $0.15\text{ K}^{-1}$  at the midpoint of the transition ( $\sim 73\text{ K}$ ) (see attached figures). Although the TCR of these films is not quite as high as desired, it is high enough to make a very good bolometer. These films were grown using a combination of pure ozone from Honeywell's ozone distillation system, and ordinary oxygen. The growth temperature for optimum superconducting properties was between  $700^\circ\text{C}$  and  $735^\circ\text{C}$ . These growth

temperatures are believed to be low enough to allow survival of the transistors which will be embedded in the substrate. The substrates used are ideal for fabrication of microstructures by silicon micromachining techniques.

The University of Minnesota has begun work as a subcontractor to assist in the film development, including measurements of noise in the superconductor films.

**Task 2.2: Mask Design**

The first fabrication run will use existing masks from DARPA/ONR Contract #N00014-88-C-0394.

**Task 2.3: Vendor Electronics**

For the first fabrication run, transistors will not be embedded in the substrate.

**Task 2.4: Integrated Device**

The steps have been defined for a process of bolometer fabrication in which the  $\text{YBa}_2\text{Cu}_3\text{O}_7$  film is deposited before etching of the silicon microstructure. This should result in bolometers with good mechanical integrity and good superconducting properties. Several steps of the proposed process have been tested in the laboratory. In particular, the patterned  $\text{YBa}_2\text{Cu}_3\text{O}_7$  films have been successfully passivated against the KOH etchant used to fabricate the silicon microstructures. A complete fabrication run using this process on 8 wafers began in June 1991. It will be completed by the first week of August 1991.

**Task 2.5: Device Evaluation**

Work on this task has not begun.

**Task 3.0: Second Fabrication Run**

**Task 3.1: Film Development**

Work on this task has not begun.

**Task 3.2: Mask Design**

The mask design is nearly complete. The distance from the center of one pixel to the center of a neighboring pixel in the 4 x 4 array is 125  $\mu\text{m}$ . Minor modifications to the mask design may be required to be compatible with the fabrication process used by the transistor fabrication vendor.

**Task 3.3: Vendor Electronics**

Mary Weybright, our consultant at Stanford University, has modelled theoretically the performance of the bipolar transistors at low temperature, in order to determine doping profiles needed for the transistor switches at each pixel. Further progress in the design of the transistors requires data from actual devices.

**Task 3.4: Integrated Device**

Work on this task has not begun.

**Task 3.5: Device Evaluation**

Work on this task has not begun.

**Task 4.0: Third Fabrication Run**

Work on this task has not begun.

**4.0 ACCOMPLISHMENTS (for 1 April 1991 to 30 June 1991)**

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zero resistance at ~65 K. The temperature coefficient of resistance (TCR) is about  $0.15 \text{ K}^{-1}$  at the midpoint of the transition (~73 K) (see attached figures). Although the TCR of these films is not quite as high as desired, it is high enough to make a very good bolometer. These films were grown using a combination of pure ozone from Honeywell's ozone distillation system, and ordinary oxygen. The growth temperature for optimum superconducting properties was between  $700^\circ \text{ C}$  and  $735^\circ \text{ C}$ . These growth temperatures are believed to be low enough to allow survival of the transistors which will be embedded in the substrate. The substrates used are ideal for fabrication of microstructures by silicon micromachining techniques.

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**Task 3.5: Device Evaluation**

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**Task 4.0: Third Fabrication Run**

Work on this task has not begun.

**5.0 PROBLEM AREAS/ISSUES**

- Performance of transistors at low temperature must be adequate for good switching performance.
- Transistors must survive the high growth temperature of the  $\text{YBa}_2\text{Cu}_3\text{O}_7$  films.
- Growth of high quality  $\text{YBa}_2\text{Cu}_3\text{O}_7$  films must be achieved at temperatures sufficiently low to allow survival of the transistors.  $\text{YBa}_2\text{Cu}_3\text{O}_7$  films must exhibit sharp superconducting transitions and smooth morphology.

- The  $\text{YBa}_2\text{Cu}_3\text{O}_7$  films must retain their sharp superconducting transitions after the bolometers are fabricated.

## **6.0 CORRECTIVE ACTION**

- Utilize calculations of transistor performance to optimize low temperature performance.
- Use PtSi ohmic contacts.
- Passivate the  $\text{YBa}_2\text{Cu}_3\text{O}_7$  films with yttria stabilized zirconia, silicon dioxide, and silicon nitride to prevent damage during the bolometer fabrication.

## **7.0 GOALS FOR THE NEXT PERIOD (1 July 1991 to 30 September 1991).**

- Complete the first fabrication run (without transistors embedded in the substrate).
- Complete the characterization of bolometers fabricated in the first fabrication run.
- Begin work at Honeywell Micro Switch Division on design and fabrication of transistors embedded in the silicon substrate.
- Complete the transistor design calculations for the second fabrication run.
- Complete the mask design for the second fabrication run and obtain the completed masks.

## **8.0 PUBLICATIONS**

### **8.1 Papers Published in Refereed Journals**

None

### **8.2 Papers Published in Conference Proceedings**

None

### **8.3 Presentations**

#### **a. Invited**

B.R. Johnson, "Superconducting Microbolometer Infrared Detector Arrays on Silicon Microstructures," presented at the International Superconductor Applications Convention, San Diego, CA, January 14-16, 1991.

b. Contributed

B.R. Johnson, P.W. Kruse, S.B. Dunham, "YBa<sub>2</sub>Cu<sub>3</sub>O<sub>7</sub> Films For Infrared Bolometers on Silicon Microstructures," to be presented at the Materials Research Society Fall Meeting, December 2-6, 1991, Boston, MA.

The following paper was presented at the DARPA Second Annual High Temperature Superconductors Workshop, Sheraton Tara Hotel and Resort, Danvers, MA, October 3-5, 1990.

B.R. Johnson, C-J Han, T. Ohnstein, B.E. Cole and P.W. Kruse, "Monolithic Integration of Semiconductor and Superconductor Components."

**9.0 FINANCIAL**

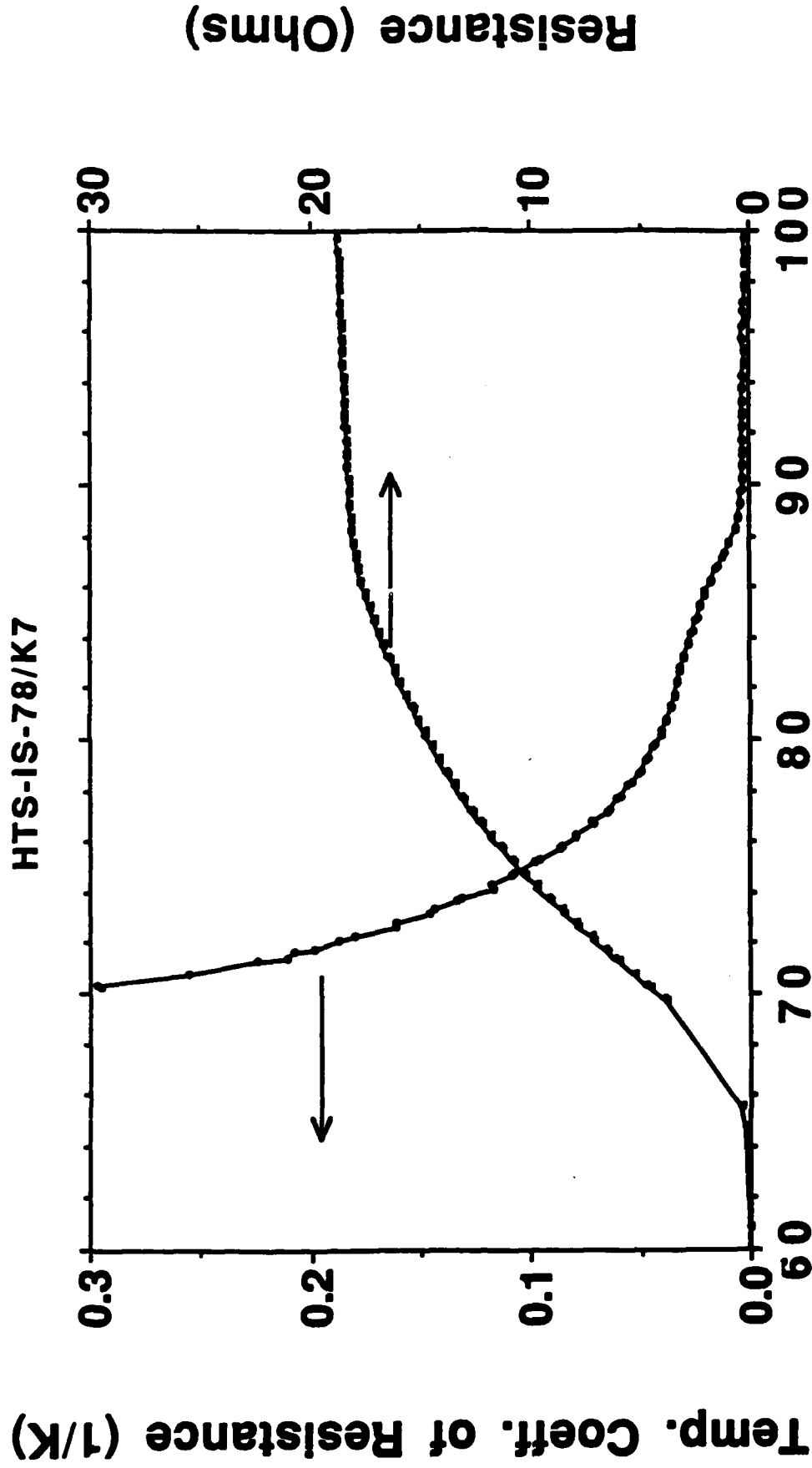
A.	Funding Authorized	\$300,000
B.	Funds Expended or Committed (Week ending 23 June 1991)	\$272,852
C.	Additional Funds Required to Complete Contract (by 30 June 1992)	\$262,022

PK:Semi/SuperJun91rev1(7/1/91)



# R vs. T and TCR vs. T

HTS-IS-78/K7

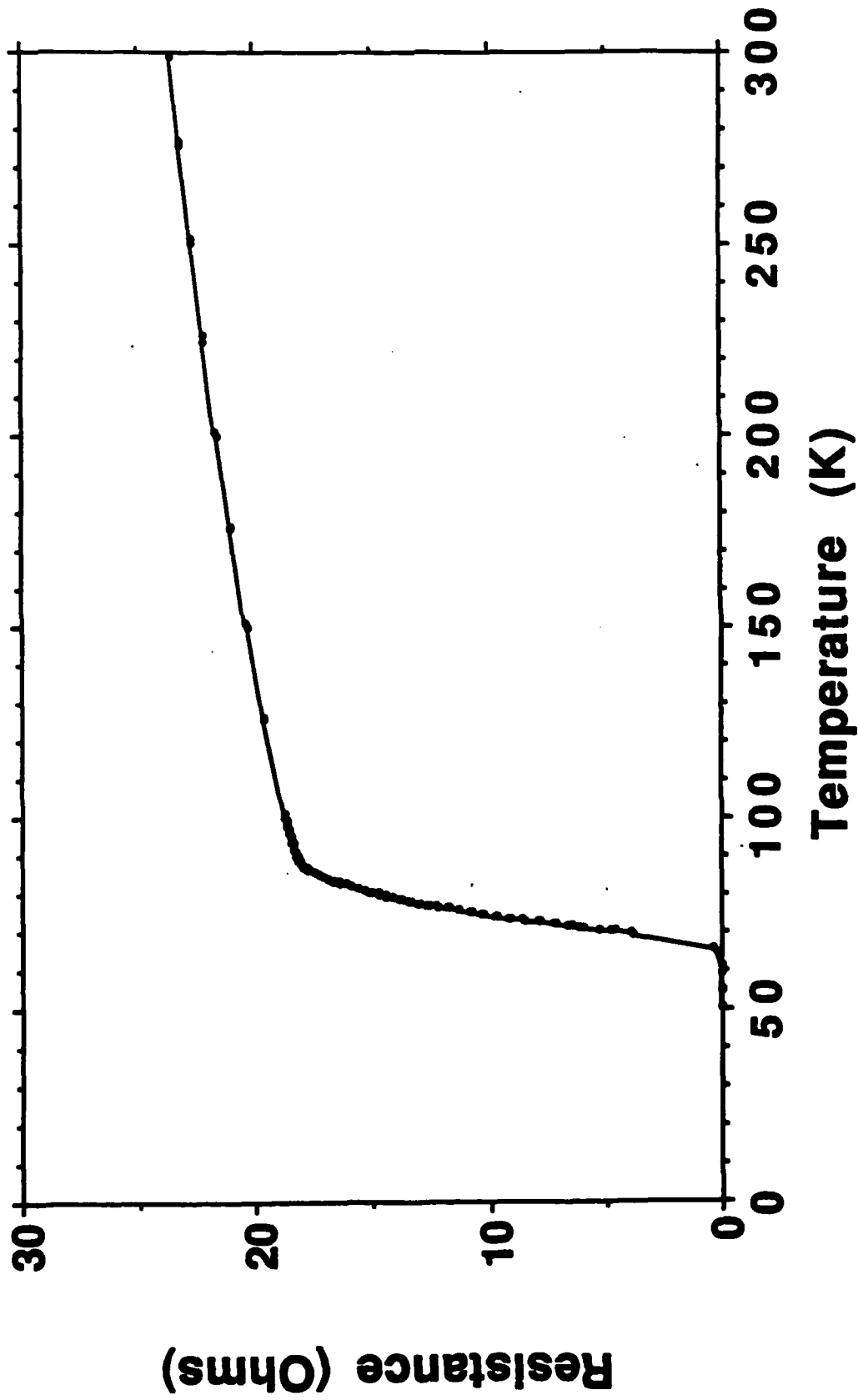


Honeywell

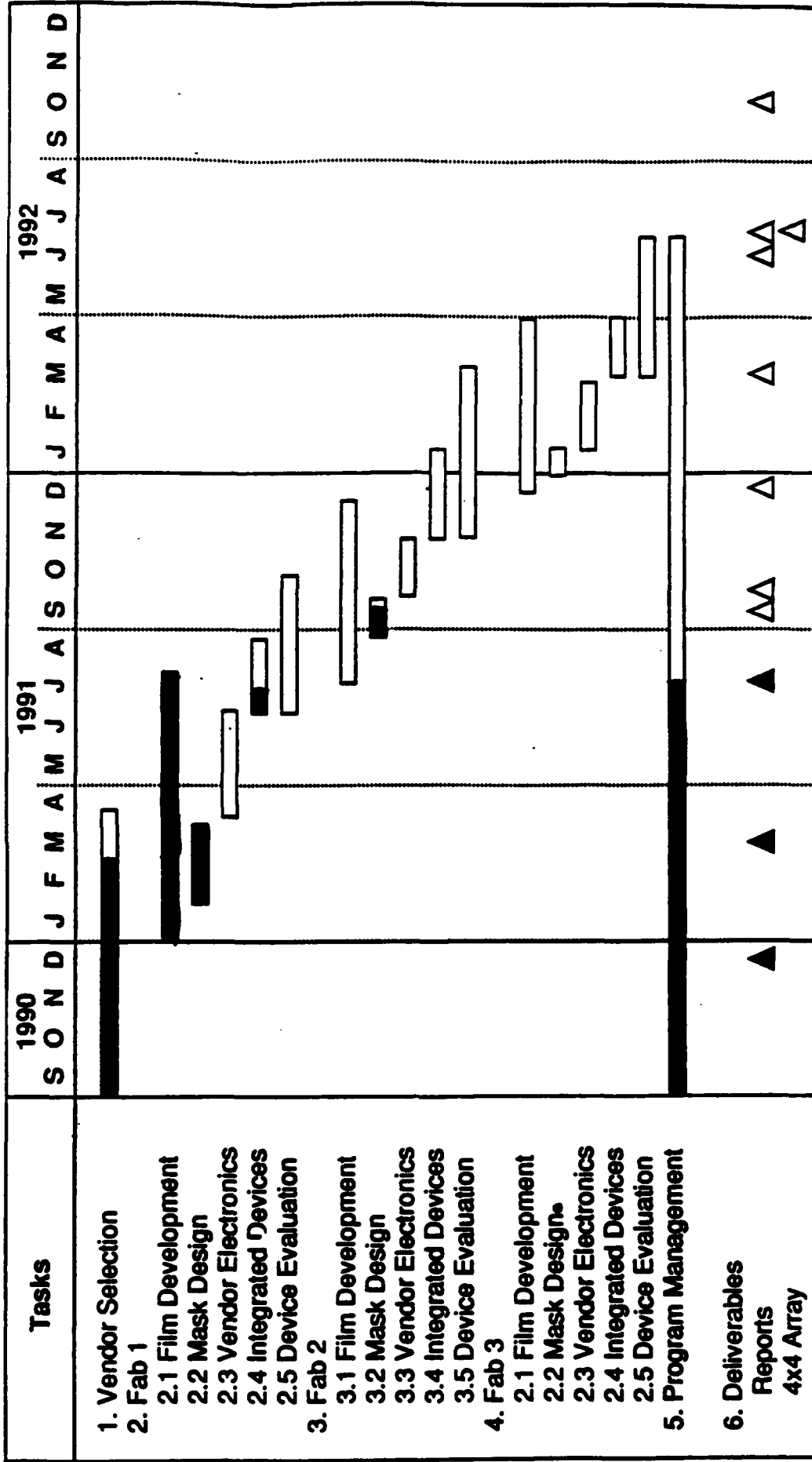
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# Resistance vs. Temperature

HTS-IS-78/K7



# Program Schedule



Honeywell