Final Report

# DEFECT REDUCTIONS IN EPITAXIAL GROWTH USING SUPERLATTICE BUFFER LAYERS

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By

S.M. Bedair, Professor and N. El-Masry
Electrical and Computer Engineering Department
North Carolina State University
Raleigh, North Carolina 27695-7911

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Electrical & Computer Engineering Department
North Carolina State University
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# ABSTRACT

The final report is based on the thesis of two Ph.D. students working in the area of defect reduction using strained layer superlattices. The students are: C.L. Tarn and N. Hamguchi.

A variety of attempts to reduce the defects density in GaAs epitaxial films grown on Si substrates using annealing, InGaAs-GaAsP strained-layer superlattices, strained-layer superlattices combined with annealing, and the selective etching are presented. The following results were obtained:

(1) Both conventional furnace annealing/slow cooling and rapid thermal annealing were effective to eliminate microtwins and stacking faults. However, the conventional furnace annealing/slow cooling showed more promising results in terms of dislocations reduction. This conventional furnace annealing reduces dislocation density to about high $10^7$ $cm^{-2}$.

(2) The maximum critical thickness of strained-layer superlattices from our calculation is function of the density of bent-over threading dislocation. By considering the high density of grown-in threading dislocations in GaAs epitaxial layer on Si substrate our calculation expects a much higher maximum critical thickness than that of Van der Merwe's, Matthews, and People and Bean's predictions.

(3) The thermally activated nature of the effectiveness of strained-layer superlattices in blocking threading dislocations has been predicated by our energy equilibrium model. From our energy equilibrium calculation the minimum critical thickness of strained-layer superlattices was predicted as a function of processing temperature.

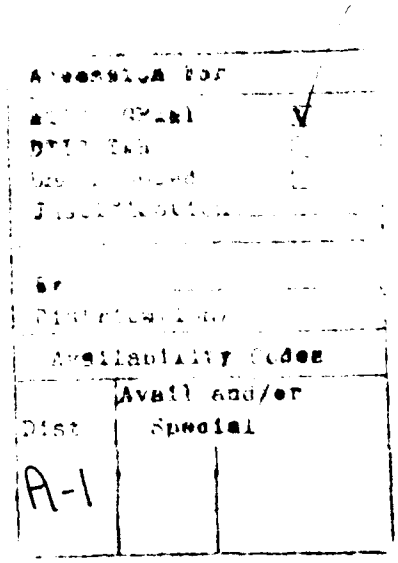
(4) It has been shown that $In_xGa_{1-x}As$-$GaAs_{1-y}P_y$ ($y=2x$) is an appropriate and highly effective

buffer layer for reducing dislocations originating at GaAs-Si interface. The SLS structure also permits high values of strain to be employed without the SLS generating dislocations of its own. However, the effectiveness of the SLS depends on the density of dislocations.

(5) Several interactions between the strain field of the SLS [$In_xGa_{1-x}As$-$GaAs_{1-y}P_y$ (y=2x)] and the threading dislocations in GaAs grown on Si substrate were observed. Favorable conditions for dislocation reduction were realized when (i) the dislocation is bent at the SLS interface and propagate to the sample edge, (2) two dislocations interact to cancel each other by forming a loop, and (iii) two dislocations react to form a third one at a node.

(6) The effectiveness of SLS [$In_xGa_{1-x}As$-$GaAs_{1-y}P_y$ (y=2x)] in blocking threading dislocations was significantly improved by employing intermittent annealing during and/or post the SLS growth. The thermal energy from annealing provided the energy to overcome the energy barrier for threading dislocations to have a stable misfit dislocation segment glide along the SLS interface.

(7) A technique combing selective etching and conventional furnace annealing/slow cooling successfully improved heteroepitaxial GaAs crystalline quality on Si substrate. After conventional furnace annealing/slow cooling the patterned GaAs on Si sample, a well defined dislocation network was formed to confined within 1 $\mu$m beneath the GaAs top surface.



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# 1. INTRODUCTION

Heteroepitaxial GaAs on silicon is a very promising material for the fabrication of monolithic electronic integrated circuits. To date, several device structures have been fabricated in this heteroepitaxial material. These include: light emitting diodes (LED's)[1], metal semiconductor field-effect transistors (MESFET's)[2], solar cells[3,4,5], modulation-doped field-effect transistors (MODFET's)[6] and laser diodes[7,8] and recently medium-scale integrated circuits[9]. The monolithic integration of GaAs/AlGaAs double heterostructure LED's and Si metal-oxide-semiconductor field-effect transistors (MOSFET's)[10] have been demonstrated.

Silicon is a favored semiconductor material for integrated circuits because of its low cost, large wafer size, and superior mechanical properties. However, gallium arsenide is the preferred choice for ultrafast digital circuits, microwave integrated circuits, and electro-optical applications due to its high electron mobility and tremedous optical properties. The main problems which hold up the extensive use of this compound semiconductor are its mechanical fragility, poor thermal conductivity, and lower radiation resistance. In addition, gallium arsenide substrates are relatively expensive and more defective when compared to silicon. The obvious advantages of placing GaAs epitaxial layers on Si substrate are (i) a low cost, light weight, large area passive substrate with superior strength and thermal conductivity, (ii) allow optical and high-frequency III-V devices to be integrated with very large-scale integrated (VLSI) silicon circuitry on a monolithic chip, and (iii) the possibility of superior thermal dissipation in power devices.

It is well recognized that the crystal quality of epitaxial gallium arsenide deposited on silicon will be substantially inferior to that deposited on gallium arsenide substrates. However, experience accumulated over the past 2-3 years shows that the quality exceeds

previous expectations considering the mismatch in lattice constants and thermal expansion properties. The quality of the material has steadily improved through the use of buffer layers to trap and suppress crystal defects originating at the interface between the silicon substrate and the III-V epitaxial layers.

A very stable native oxide on silicon substrates represents the first barrier to epitaxial growth of GaAs on silicon. This thin oxide layer isolates the underlying ordered silicon lattice and exposes an amorphous surface to incoming III-V species. The native oxide proved to be an effective barrier to earlier attempts to grow epitaxial GaAs on Si. Molecular beam epitaxy with its sophisticated instrumentation and ultrahigh vacuum, determing when a "clean" silicon surface is present.

Some GaAs crystal orientations, including the most desirable {100}, consist of alternating monoatomic layers of gallium and arsenic atoms. Unless the silicon substrate surface is atomically flat (or all steps are an even number of atomic layers in height) and growth proceeds without two dimensional nucleation, multiple nucleation will occur on the surface; and when these regions grow together to form a continuous film, the layers of a given species may or may not be in alignment with the same species from one separately nucleated region to the other. If two regions are misaligned, then the resultant boundary is called an antiphase boundary. These defects were commonly encountered in the early films and were once considered to be a major limitation to the technology. However, by 1985, convincing evidence had emerged that the antiphase boundaries could be suppressed[11]. This major development was achieved by initiating the growth with a prelayer of either As or Ga and by use of an intentionally misoriented or "tilted" substrate with a surface orientation of about 4 degrees from the (001) toward the (011)[12]. Silicon surfaces with this orientation, when subjected to high temperatures (such as during oxide removal), rearrange to form steps with double-atomic-layer heights[13].

This same tilted surface orientation serves to significantly reduce another type of crystal imperfection -- threading dislocations associated with the lattice mismatch. In the very early stages of growth, lattice mismatch is accommodated at least partially by compressive strain, and the GaAs lattice spacing contracts in an attempt to match the underlying Si spacing. After a few nanometers the strain energy exceeds that required to form dislocations and misfit dislocations are formed. Two types of misfit dislocations are observed to occur[14]. One of these lies in the interface plane and does not generate threading dislocations that propagate into the epitaxial layer By use of tilted substrates most of the misfit dislocations are of the favorable type that are located in the interface region.

Additional dislocation reduction can be obtained by use of superlattice intermediate layers. The strain fields built into the superlattices can bend over dislocations that would otherwise propagate into the subsequently deposited epitaxial layers. These superlattices may be thin, alternating layers of different composition or alternating layers of the same composition but deposited at different temperatures[15]. Finally, some dislocation reduction can occur by annealing during growth of the thicker portions of the epitaxial layer or by a separate anneal after growth[16].

By use of the above approaches to minimize defects and their propagation, the GaAs on Si structures have a region of poor crystal perfection localized to within approximately 100-300 nm of the interface. This is followed by the remainder of the epitaxial layer which has a relatively good quality. For devices, such as field effect transistors, whose critical current paths are located near the upper surface of the epitaxial layer, the imperfect interface is innocuous. However, some potential applications of GaAs on Si require carrier transport through the interface region.

Another serious problem for device application is wafer bowing that results from the different thermoelastic properties of GaAs and Si. On cooling from the epitaxial growth temperature the free contraction of GaAs is 260% greater than that of Si. The resulting

wafer is bowed with a concave GaAs surface and high tensile stresses within the GaAs layer. Depending on the growth technique, the wafer bow may range from an acceptable 5 μm to greater than 50 μm over a 2-in. wafer. In severe cases the tensile stresses exceed the elastic limits of GaAs and cracking occurs. For the fine-line lithography required for LSI circuits the wafer bow should be less than 10 μm over a 2-in. wafer.

The extent of wafer bow is dependent on the deposition temperature, which should be minimized whenever possible. Calculations of stress and wafer bow made using the approach of Vilms and Kerps[17] for typical GaAs-on-Si parameters show that increasing the deposition temperature by 100°C results in a 10 μm increase in wafer bow. Some residual misfit strain (4.1%) at the deposition temperature was included in the calculation to adjust the results to experimentally observed values. Besides restricting the epitaxial deposition to the lowest possible temperatures, wafer bowing can be alleviated by use of selective epitaxial deposition or by etching the epitaxial films into a pattern of localized areas.

Some difficulties are also encountered in processing GaAs-on-Si structures during device fabrication. Gallium arsenide preferentially cleaves along {110} planes, but silicon cleaves along {111} planes. Adjustments in wafer dicing and mask alignment may be necessary to conform to these different cleavage properties. The two materials also have different sensivities to the etchants employing in processing and, depending on the process conditions and temperatures, cross-doping or cross-contamination can impose restrictions, particularly when functional devices are to be present in both materials.

Although GaAs on Si has led to sucessful fabrication of a number of discrete GaAs devices on Si, the residual defect problem still impedes the progress of this technology. In this thesis, a variety of attempts to reduce the defect density using annealing, InGaAs-GaAsP strained-layer superlattices, and selective etching are presented.

Chapter 2 presents a detailed review of the progress to date and the remaining challenges. Results of the annealing effects on defects reduction are described in Chapter

3. Chapter 4 discusses the theoretical modeling of strained-layer superlattices. Chapter 5 presents the effectiveness of using InGaAs-GaAsP in reducing dislocations in GaAs epitaxial layer grow on Si substrates. The important interactions between threading dislocations and strained-layer superlattice are presented in Chapter 6. Results from intermittant annealing and/or after the strained-layer superlattices growth are discussed in Chapter 7. Chapter 8 describes the effect of using selected etching (epi-layer shrinkage) in reducing defects. Finally, Chapter 9 summarizes these results and suggests further research activities.

# 2. BACKGROUND

There has been considerable sucess recently in the growth of GaAs on Si and the fabrication of devices using this material. It is clear that while substantial progress has been made, improvements in the understanding of the generation and control of defects in heteroepitaxy are required to reach the promising optical interconnects, optoelectronic integrated circuits and monolithic integration of ultra-high speed GaAs with high density Si VLSI. In the following sections, we review the progress to date and the remaining challenges with respect to; the role of Si surface, suppression of antiphase disorder, initial nucleation, GaAs thick layer growth, the growth procedures, residual stress in GaAs epitaxial layer, and defect control.

## 2.1 Si Surface

One of the key elements of the success of GaAs on Si growth is the advent of improved Si wafer cleaning techniques. Native Si oxides desorb at high temperatures and leave substantial amounts of carbon on the surface. RCA and other earlier common chemical cleans form an oxide that can be desorbed in UHV between 800-900°C, but require a brief flash cleaning at approximately 1150°C to remove the residual carbon[18,19]. This high temperature is impossible to achieve in conventional III-V MBE or MOCVD epitaxial systems. Also high temperature exposure is incompatible with any Si devices that are already on the substrate. Thus, a lower temperature cleaning procedure was essential. Ishizaka et al.[20], developed a cleaning procedure which consisted of sequential forming and etching of a thin oxide layer on Si. This process forms a non-stoichiometric oxides which desorbs below 800°C and most importantly, leaves the surface carbon free. DLTS

and SIMS measurements by Xie et al. indicate there is still a small amount of residual carbon left on the surface[21,22]. However, this technique is a substantial improvement over earlier techniques. AES measurements by Biegelsen et al.[23] show that ozone oxidation leaves carbon on the surface and require an even higher oxide desorption temperature than the Ishizaka clean.

## 2.2 Suppresion of antiphase disorder

A second key element for GaAs on Si growth is the preparation of a surface which prevents antiphase disorder (APD). Antiphase disorder is commonly observed in the growth of compound semiconductors on elemental semiconductors. This was particularly severe for the initial investigations of GaP/Si[24] and GaAs/Ge[25]. The problem lies in the fact that both the diamond cubic (Si) and zincblende (GaAs) structures are composed of two interpenetrating FCC sublattices. The (100) plane contains only one of the two FCC sublattices. A real (100) surface contains steps, and if these steps are an odd number of atomic layers high, the surface is then composed of atoms from both sublattices. This presents a problem when GaAs is grown on such a Si surface. Bringans et al.[26] showed that As has a strong affinity for Si(100) surface. Coupled with the fact that the Si preheat and cool-down occurs in a high As activity (high As flux), this leads to the conclusion that GaAs growth on Si starts with As-Si bonds. Therefore, GaAs nucleated at opposite sides of a step that is an odd number of atomic layers high will grow together forming an antiphase boundary, as shown in Fig. 2-1. For the (100) orientation, this problem can be avoided if all the atomic steps are an even number of atomic layers high and the nucleating species is of a single type (i.e. As). While this model is overly simplistic because a real surface almost certainly has some remaining single steps, it is useful to understand and the processes to approach this desired configuration.

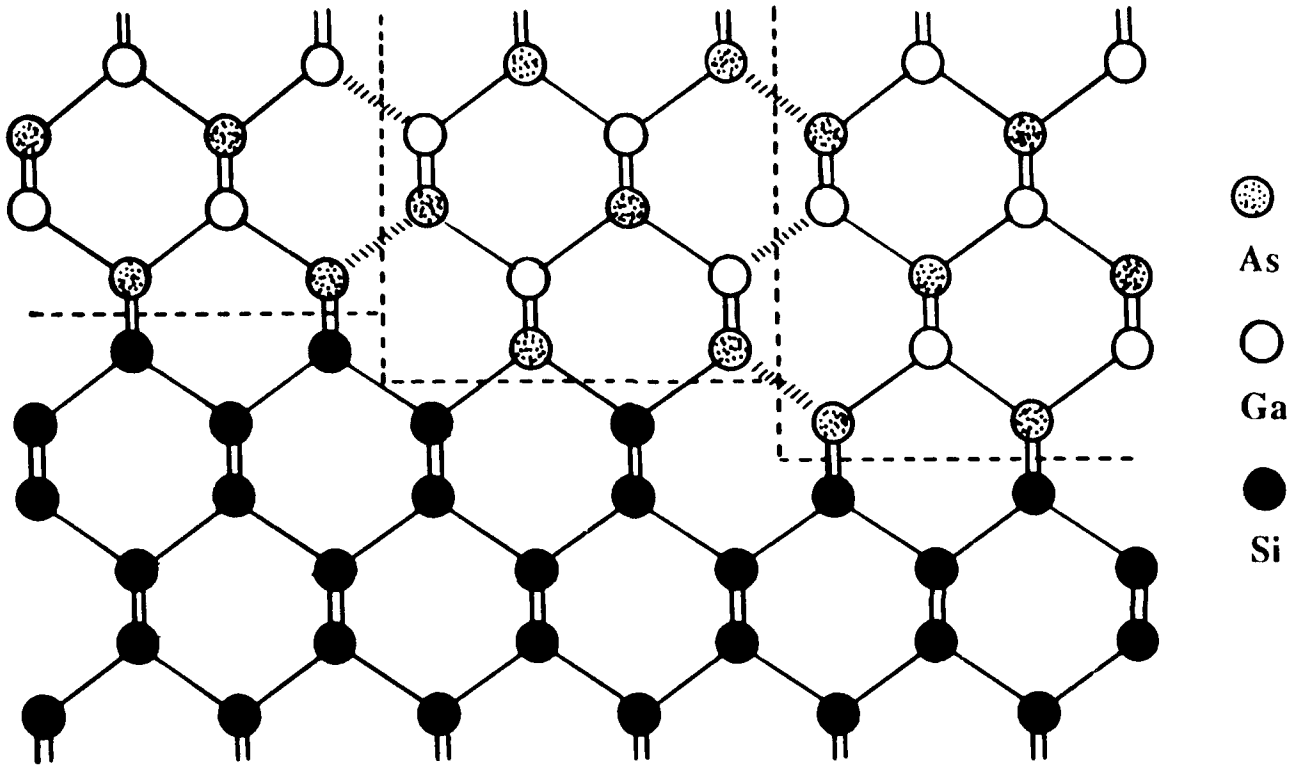



Fig. 2-1 Mechanism of APB formation during polar-on-nopolar growth due to the presence of single-height steps on the substrate surface.

There are at least two potential approaches to avoid antiphase domain boundary (APBs) : one is to somehow enforce a perfect doubling of the height of all surface steps while the other involves a switch to a different crystallographic orientation on which APBs do not form.

2.2.1 Step doubling on (100) surfaces

Most investigators working on GaAs-on-Si growth have preferred to continue to work with the conventional (100) orientation, or with wafers deliberately misoriented from the (100) orientation by a few degrees, relying on step doubling for the suppression of APBs.

When a step on Si (100) surface is an even number of atomic layers high, the two sublattices on the GaAs side are in registry again, and an APB will not occur at this step. Unfortunately, it is well established experimentally that for "as polished" exactly (100)-oriented Si surfaces, the most common step height is one atomic layer[27,28] and there is in fact ample evidence[29] that the growth of GaAs , and other III/V compounds such as GaP, on exactly (100)-oriented Si or Ge substrates usually exhibits copious APBs.

It was first indicated by Henzler and Clabes[27] that misoriented Si(100) surfaces tend toward step doubling with increasing annealing temperature. This was subsequently followed up in careful detail by Kaplan[28], who reported that on Si surfaces tilted by a few degrees from the (100) plane towards the (011) plane, most steps are two atoms high. In as much as the step density on deliberately misoriented surfaces is much higher than for accurately oriented (100) surfaces, a certain amount of step doubling is to be expected, and that step doubling might be extensive if there is a simple energetic preference for double steps over single steps. However, unless the number of remaining single-height steps is drastically reduced, such tilting would not aid in the drastic suppression of APBs. In any event, it is hard to see how APBs could be avoided completely over the entire area of an entire wafer. In order to achieve APB-free growth, it is necessary that all steps be two

atoms high, not just the majority of steps. At first glance, such a proposition appears hopeless. Yet it has become clear since early 1985 that such a perfect step doubling can indeed be achieved, leading to perfectly APB-free epitaxial growth of GaAs onSi (100):

(a) Recently, Fischer et al.[2,30] have reported growth on deliberately misoriented substrates, which does indeed appear tc be free of APBs, judging from the anistropic etching patterns of device structures on the epitaxial layers. Anisotropic etching is one of the simplest and most powerful techniques to test for APDs.

(b) Similarly convincing evidence of APD-free growth, based on an anisotropy of the RHEED patterns that was uniform over the entire wafer area was presented by Nishi et al.[31] The Si wafers in that work were not deliberately misoriented, but probably had a small amount of accidental misorientation. Similar results had been reported earlier by same group for MOCVD growth GaAs on Si. Reflection high-energy electron diffraction (RHEED) evidence similar to that of Nishi et al., but less direct, had been earlier presented by Wang[32], and by hindsight it appears likely that Wang also had achieved APB free growth.

(c) Perhaps the most convincing direct evidence for perfect step doubling already on the pre-growth Si (100) surface is contained in the stunning recent work by Sakamoto and Hashiguchi[33], who showed that a nominally (100)-oriented Si surface would go from a singly-stepped surface to a doubly-stepped surface during a prolonged high-temperature anneal (20 min. at 1000°C), with all step terraces belonging to the same sublattice. Calculations by Aspnes show that there is an energetic preference for one type of double step, type a in Fig. 2-2, instead of type B double steps and single steps. It is likely that the temperature of this surface reording is lowed by using Si misoriented from the (100), since the steps are closer together and therefore the Si atoms do not have to diffuse as far to find a step.

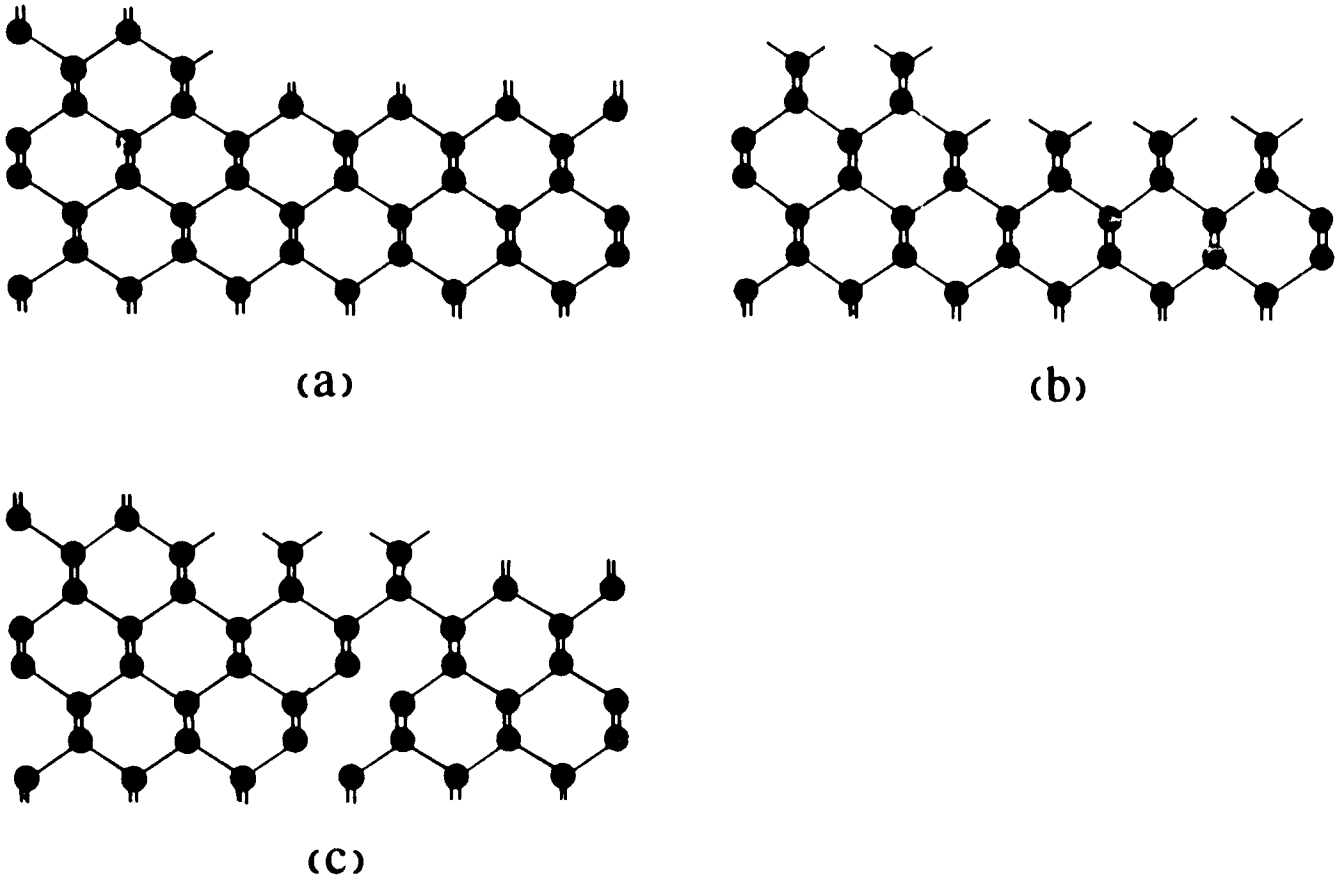



Fig. 2-2 Steps on the Si(100) surface : (a) Type A bouble step. (B) Type double step. (c) Type A and B single steps.

2.2.2 Using (211) orientation Si substrate

The higher temperature-time cycles required for surface reconstruction might be avoided by using the (211) orientation Si sustrates as suggested by Kromer[34,35,36,37]. The (211) surface has the advantage of providing a natural site selection for As and Ga atoms. Atoms from both sublattices are on the (211) surface, having one and two dangling bonds, respectively (Fig. 2-3). Because As has a stronger tendency to bond to Si than Ga does, As preferentially bonds to the Si sites with double dangling bonds, leaving the sites with single dangling bonds for Ga. Therefore, the As and Ga are each positioned on only one sublattice, and no APB is formed. This was confirmed experimentlly using crystallographic etching techniques by Wright et al.

The (211) surface also has the advantage of being non-polar, unlike the (100) surface. Therefore, no net electric field exists at the GaAs/Si (211) interface as must exist at the GaAs/Si (100) interface. One might expect less intermixing at the (211) GaAs/Si interface; however, this depends upon the magnitude of the chemical potential driving force compared to the electric field driving force. Because many device processing steps are anisotropic, switching to the (211) orientation would involve developing an entirely new Si processing technology, and it is unlikely that the Si industry would consider such a switch. It thus appears important to solve the potential problem on the (100) surface.

## 2.3 Initial nucleation

The events occuring during the initial stages of nucleation are not clear. There has been a great deal of debate about whether the very first layer bonding to Si is always As. Fisher et al.[12] have done etching experiments that suggest that a Ga pre-layer is formed when the deposition is done at high temperature with low V/III flux ratios. The etch pits formed in these wafers had a different shape than those on wafers grown at low

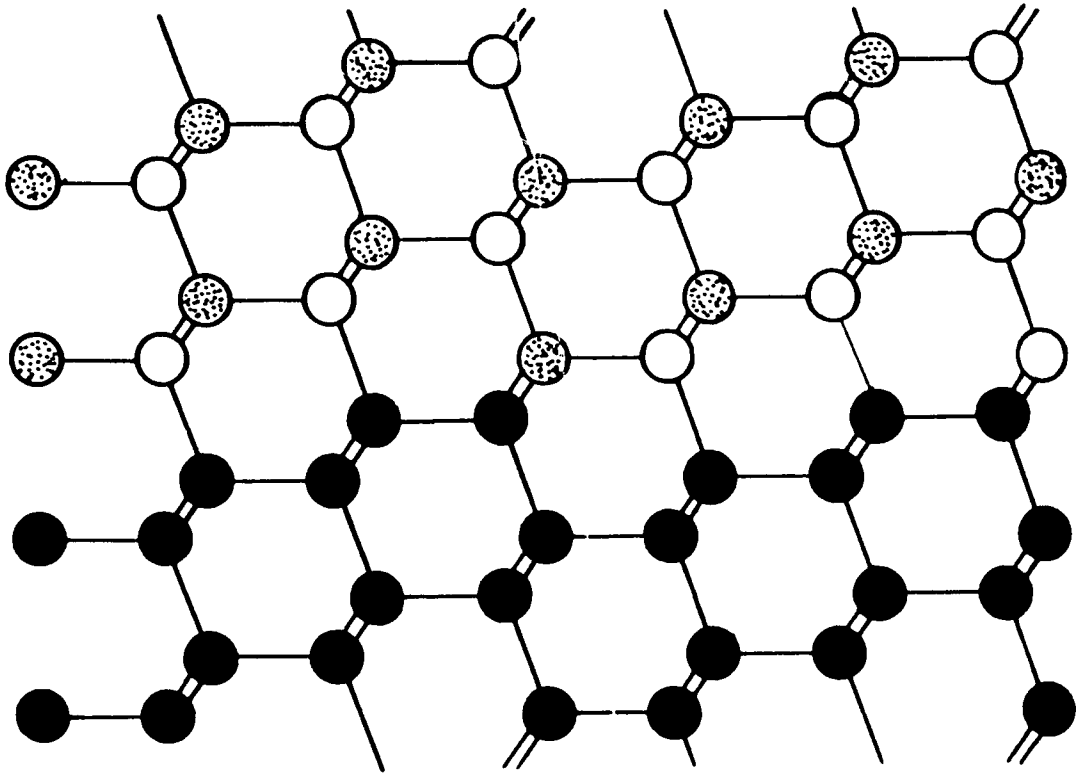


Fig. 2-3 A (211)-oriented polar-on-nopolar interface. On such a surface, APBs do not form even in the presence of steps, because the two sublattices differ in the way they are back-bonded to the substrate, leading to sublattice control by chemical bonding preference.

temperatures. Both types of etch pits are seen in material containing APBs, indicating that As occupies different sublattices in the two materials. Because of the much stronger preference for As to bond to Si compared to Ga (in fact, there are several thermodynamically stable SiAs compounds but no SiGa compounds), it is unlikely that large regions of a wafer would contain a Ga prelayer.

Several analysis from Bringans et al.[38] are also worth noting:

(i) In the absence of Ga, a single monolayer of arsenic is very strongly bound to both Si(100) and Si(111).

(ii) When a monolayer of As is deposited on Ga pre-monolayer, most of the As moves througn the Ga layer to bond to the Si.

(iii) For GaAs-on-Si(111), the bonding appears to take place predominatly between Si and As atoms. This also consistent with interface models such as that due to Northrup in which Ga-Si bonds are present several atomic layers below the outermost Si-As bonding layer.

(iv) For GaAs-on-Si(100), the area between islands is not As-terminated Si, but consists of a thin layer which probably contains both Ga and As atoms.

(v) The use of Ga prelayers rather than As prelayer does not alter the bonding observed at the interface but, in the case of GaAs-on-Si(111), reduces the area between islands.

(vi) For Si(100) surfaces tilted about [011] and annealed, it was shown that double height atomic steps predominate and that a monolayer of As could form without disrupting the step structure.

(vii) The Ga prelayer can cause

(a) a reduction of the Ga mobility leading to an increase in the density of GaAs nucleation sites.

(b) lower contact angles of the GaAs islands at the initial stages of the epitaxy since the Ga prelayer causes a different substrate-overlayer bonding character under the islands.

(c) alters the surface morphology at thicknesses just greater than that at which the films becomes continuous.

Kromer[39] has proposed a model consistent with both the Fisher results[12] and the facts known about As-Si bonding. He postulates that an exchange occurs between the As and Si such that As atoms occupy sites in the Si surface layer, in such a way that the GaAs/Si interface charge is neutral. The Ga atoms then bond to As in this layer, so the net effect is that the first layer on the top of the Si surface consists of atoms in the Ga sublattice. This would reduce the energy associated with the high electric field. The reason this does not happen at lower temperatures and higher V/III ratios is that interface reordering may be induced by either high Ga coverage or high tempeatures.

In addition, Biegelsen et al.[40], utilizing graded-thickness samples for studying the initiation nucleation mechanisms, showed

(i) surface diffusion even at 400°C is high.

(ii) the mobile species is most likely Ga.

(iii) nucleation is determined by Ga stable cluster formation followed by $As_4$ capture and Ga immobilization.

The initial growth of GaAs on Si is further complicated by an additional observation: GaAs islands tend to nucleate at steps on the Si surface. Rosner et al.[41] have investigated the effect steps have on the morphology of initial nucleation. Plan-view TEM results showed that growth is significantly enhanced in the direction parallel to the step edges. The ordering of the islands along the step edges is more pronounced the greater the degree of misorientation from the (100) axis, where there are more steps. Because of this, the arrangement, type of steps and the manner in which islands coalesce are key in determing the structure of the GaAs film. This result is inconsistent with all of the layer-by-layer theories for heteroepitaxy.

## 2.4 Thick layer growth

The most common growth procedure used for GaAs on Si involve two stages: growth of a buffer layer at a slow rate and low substrate temperature, followed by a device layer using conventional GaAs homoepitaxial conditions. This has empirically been shown to improve the surface morphology of the resulting GaAs film[42]. Several workers have suggested that growth begun at low temperatures ensures that a monolayer of As bonds to the Si in order to prevent APD formation. However, Uhrberg et al.[43] have found that As strongly bonds to Si and does not desorb unless the wafer is heated to 650°C or higher.

The improvement in surface morphology observed when a low initial growth temperature or a misoriented substrate is used is also a consequence of the nucleation mode. As the substrate temperature is lowed, nucleation becomes increasingly dominant over surface transport to grow islands, so many more islands form. The aspect ratio (height/length) of the islands also decreases. When such islands coalesce, the resulting surface topography is much smoother than that obtained from films nucleated at higher temperatures. The improvement in surface morphology with substrate misorientation was explained by Lee[44] in a similar manner. Since nucleation occurs predominantly at steps, perhaps more nuclei are formed when there are more steps.

Fisher et al.[12] have also correlated surface morphology with dislocation structure. They found depressions where clusters of threading dislocations reached the surface. The appearence of these depressions is different depending on whether the substrate misorientation is towards [011] or [001].

## 2.5 The growth of GaAs epitaxial layer on Si

Historically, the first GaAs epitaxy on Si was demonstrated by vapor phase epitaxy (VPE) in 1981 with a Ge-coated Si substrate[5]. However, this VPE work was discontinued because it was not suitable for a direct GaAs growth on Si or for growth of AlGaAs heterostructures. VPE was followed by molecular beam epitaxy (MBE)[32,45] and metalorganic chemical vapor deposition (MOCVD)[46].

At present, both MBE and MOCVD grow reasonably good quality GaAs on Si devices structure. The overall materials properties appear to be similar to each other. However, MBE has achieved better surface morphology and lower background doping level than MOCVD. These factors may partially explain why MBE-grown GaAs is more sucessful in GaAs IC fabrication. However, MOCVD is considered to be a more viable technique to bring GaAs on Si technology into pratical application.

Stolz et al.[47] have found the MBE initial growth conditions are not optimal. They can be significantly improved by applying the migration enhanced epitaxy (MEE) growth technique, by starting growth under extremely low $As_4$-flux conditions without predepositing As at high substrate temperatures. MEE is a modified MBE growth technique, which has proven to produce high-quality homoepitaxial GaAs layers even at low growth temperatures. Thus, MEE should be particularly suitable for the required low-temperature initial growth of GaAs on Si.

The following sections will briefly review both the substrate cleaning and growth procedures of MOCVD, MBE, and MEE growth techniques.

### 2.5.1 MOCVD

2.5.1.1 Si substrate cleaning (Henderson procedure[48])

(i) Degrease 5 minutes each with 1,1,1 trichloroethane, acetone, and methanol.

(ii) Distilled water rinse, 5 minutes in ultrasonic bath.

(iii) Etch : $H_2O$ : $H_2O_2$ : $H_2SO_4$ = 1 : 1 : 1, for 10 minutes.

(iv) Distilled water rinse, 5 minutes in ultrasonic bath.

(v) Etch : $H_2O$ : $H_2O_2$ : $NH_4OH$ = 1 : 1 : 1, for 10 minutes.

(vi) Distilled water rinse, 5 minutes in ultrasonic bath.

(vii) Etch : $H_2O$ : HF = 50 : 1, 10 minutes.

2.5.1.2 Two step growth of MOCVD

(i) The Si substrate is first annealed at 950°C in $AsH_3$ + $H_2$ atmosphere for 10-20 minutes.

(ii) The substrates were cooled down to 350-450°C and a 100-500 Å thick GaAs layer was grown as the first buffer layer. The growth rate of this buffer layer is 0.2-0.5 μm/hr.

(iii) The substrates were heated to the conventional GaAs growth temperature of 650-700°C then 1.5-4 μm thick GaAs layers were grown at growth rate 2-4 μm/hr and an optimum V-III ratio of ~15.

### 2.5.2 MBE

2.5.2.1 Si substrate cleaning (Ishizaha and Shiraki procedure[20])

(i) Degrease 5 minutes each with 1,1,1 trichloroethane, acetone, and methanol.

(ii) Distilled water rinse, 5 minutes in ultrasonic bath.

(iii) Etch : $H_2O$ : $H_2O_2$ : $H_2SO_4$ = 1 : 1 : 1, for 10 minutes.

(iv) Distilled water rinse, 5 minutes in ultrasonic bath.

(v) Etch : $H_2O$ : $H_2O_2$ : $NH_4OH$ = 1 : 1 : 1, for 10 minutes.

(vi) Distilled water rinse, 5 minutes in ultrasonic bath.

(vii) Etch : $H_2O$ : HF = 50 : 1, for 10 minutes.

(viii) Etch : boiled $HNO_3$, for 10 minutes.

(ix) Distilled water rinse, 5 minutes in ultrasonic bath.

(x) Etch : $H_2O$ : HF = 50 : 1, for 10 minutes.

(xi) Distilled water rinse, 5 minutes in ultrasonic bath.

(xii) repeat step (viii) to (xi) for several cycles.

2.5.2.2 Two step growth for MBE

(i) After the introduction to the growth chamber, the Si substrate was heated to 800-950°C with or without $As_4$ beam for 10-20 minutes or until obtaining a RHEED pattern indicative of a clean surface.

(ii) A thin GaAs layer (100-450 Å) is first deposited at low substrate temperature (<350°C) with the growth rate of 0.1-0.4 μm/hr.

(iii) Substrate was heated up to 600-650°C, and the growth rate was increased to ~0.8 μm/hr.

### 2.5.3 MEE

The one-side polished (100) Si substrate (2° off in [011]) were prepared according to the procedure described by Ishizaki and Shiraki[20] without the $HNO_3$ boiling step. Before growth, the substrate was heated to 1000°C for 15 minutes to remove the oxide layer and to form the required double-step surface structure. The growth conditions of the first GaAs monolayer on the Si substrate was varied as follows:

(i) $As_4$ predeposition at high substrate temperature (T>600°C).

(ii) Simultaneous or alternating supply of Ga and $As_4$ with varying flux ratios.

(iii) Ga deposition on substrate surfaces at 300°C.

The remaining growth was performed at a substrate temperature of 300°C. First, 50 nm of GaAs was deposited. The samples were annealed for 15 minutes at 580°C. Growth was then continued at 300°C.

## 2.6 Residual stress in GaAs layer grown on Si

Residual stress in GaAs films on 4° off (100) Si has been investigated with X-ray diffraction technique by Yao et al.[49] It was experimently confirmed that the GaAs lattice suffers tetragonal deformation, with the c-axis being [100]. The GaAs lattice tilts by approximately 0.2° toward the tilted direction of the substrate. They found that two-dimensional compressive stress dominates in GaAs films thinner than 0.3 μm in thickness, while two-dimensional tensile stress dominates in thicker films. The variation of stress is understood in terms of a combination of misfit stress and thermal stress. The two dimensional compressive stress in the layers thinner than 0.3 μm is due to the misfit stress. The estimated critical thickness for the formation of misfit dislocations is ~1 nm by using Matthews' model. Above this critical thickness misfit dislocation is induced in the layer and relax the misfit strain. The abrupt decrease in the lattice strain in the layer thinner than 0.3 μm can be interpreted as a result of the release of the misfit stress. However, layers thickness than 0.3 μm suffer two dimensional tensile stress. This is due to the thermal stress. Since the thermal expansion coefficient of GaAs is larger than that of Si by twice, the thermal stress acts as two dimensional stress in the epilayer while it acts as compressive one near the interface in the Si substrate. It is likely that the thermal stress dominates after the release of the misfit stress.

Morkoç et al.[50] have also measured the strain in different thickness GaAs films on Si. They noticed that at room tempertature the lattice parameter parallel to the film plane (along [001]), $a^{//}$, expands by about 0.13% as compared to the bulk GaAs lattice parameter. This expansion occurs although the lattice parameter of GaAs is 4.1% larger than the substrate Si lattice parameter. The out-of-plane GaAs lattice parameter (along [100]), $a^{\perp}$, correspondingly exhibits a contraction of 0.09%, which can be explained assuming that $a^{//}$ and $a^{\perp}$ are related by Poisson's ratio. $a^{//}$ in thinner films (300, 500 Å) is found to be contracted, in contrast to the thick film case . $a^{\perp}$ follows again Poisson's ratio and is now expanded. GaAs films of about 1000 Å thickness show hardly any strain at all at room temperature. Variation of strain with film thickness also been observed in $Ge_xSi_{1-x}$ films on Si substrates[51]. The differential thermal expansion between the GaAs film and Si substrate, which is not present in the GeSi/Si system, adds complications to the picture. In the case of GeSi/Si, very thin films grow elastically strained. Since the lattice mismatch is large, the strain energy exceeds the energy for the formation of dislocations after the growth of a few monolayer. Hence, the system becomes progressively incommensurate with increasing film thickness. The remaining small amount of strain is due to a residual-coherency at the interface, which has not been completely removed by discommensurations. In the GaAs on Si system the same effects presumably occur at the growth temperature. The strain observed at room temperature, however, results from a superposition of coherency and thermal strain. In thick layers with essentially no coherent strain the observed in-plane tensile strain at room temperature then follows from the fact that the thermal expansion of $a^{//}$ is forced to follow the thermal expansion of Si substrate. The thermal expansion coefficient of the two lattices are $\alpha_T(Si)=2.3*10^{-6}/K$ and $\alpha_T(GaAs) = 4.68*10^{-6}+3.82*10^{-9}*T\ /K$. Therefore, $a^{//}$ of thick GaAs layers ends up to be expanded at room temperature. This is shown schematically in Fig. 2-4. In thinner films the thermal strain can not completely cancel the in-plane contraction due to coherency

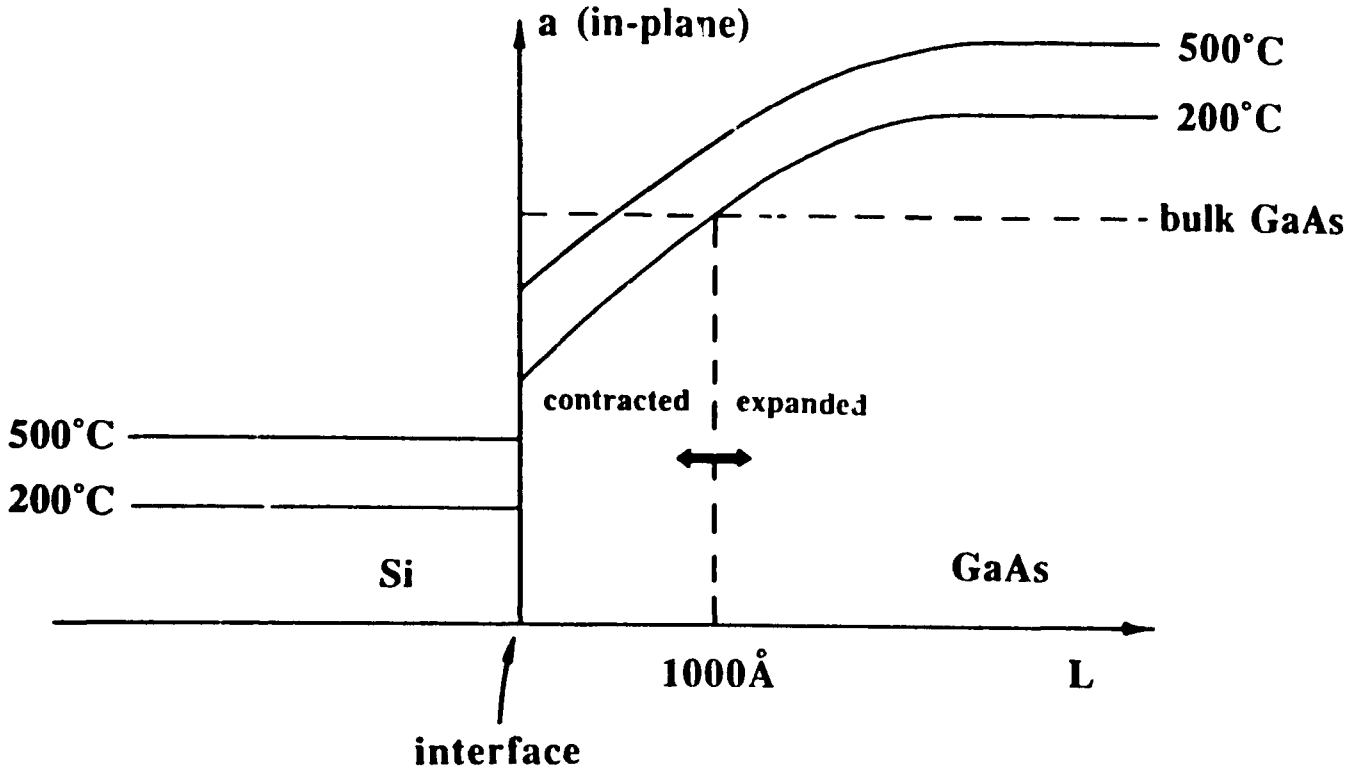



Fig. 2-4 Schematics of in-plane lattice parameters of the Si substrate and GaAs film at the growth temperature and at room temperature. The difference of the lattice parameters at both temperatures corresponds to the change due to the thermalexpansion of the Si substrate. The dash line indicates the intrinsic lattice parameter of GaAs at room temperature if there were no constraints from the substrate.

effects and those layers remain in-plane contracted at room temperature. At 500 Å to 1000Å a cross-over between in plane contraction and expansion occurs, which indicates that for those film thicknesses the elastic strain from coherency effects and thermal strain balance.

Assuming a simple elastic model, Yao et al.[49] have calculated two-dimensional stress by using $\{(\upsilon-1)C_{12}-C_{11}\}e_{zz}/\upsilon$, where $e_{zz}$ is the strain component normal to the interface and the $\upsilon$ the Poission's ratio. As shown in Fig. 2-5, even the 2 μm thick film suffers large tensile stress of ~$10^9$ dyne/cm$^2$. Based on the above consideration, Yao et al. have calculated the residual stress in the epilayer in terms of a combination of misfit stress and the thermal stress. The misfit stress is calculated by using Matthews' model[52],

$$\sigma_M=(\frac{E_f}{1-\upsilon})\varepsilon=(\frac{E_f}{1-\upsilon})(f-\delta)=(\frac{E_f}{1-\upsilon})[\frac{b(1-\upsilon\cos^2\theta)}{8\pi h(1+\upsilon)\cos\lambda}]\ln(\frac{h}{b}) \qquad (2.1)$$

where $E_f$ is the Young's modulus of GaAs film, $\varepsilon$ is the strain in GaAs film, $\upsilon$ is the Possion's ratio, $\delta$ is the strain relaxed by misfit dislocation generations, h is GaAs film thickness, b is the Burgers vector, $\theta$ is angle between the dislocation line and its Burgers vector, and $\lambda$ is the angle between the slip direction and that direction in the film plane which is perpendicular to the line of intersection of slip plane and interface. While the thermal stress is calculated by using the bi-metal strip model[53],

$$\sigma_T=E_f(\alpha_s-\alpha_f)(T-T_o)[1+3(\frac{a_f}{a_s})(\frac{E_f}{E_s})] \qquad (2.2)$$

where $\alpha_s$ and $\alpha_f$ are the thermal expansion coefficients of substrate and GaAs film respectively, $a_f$ and $a_s$ are the lattice parameters of substrate and GaAs film respectively, T is the growth or processing temperature, and $T_o$ is room temperature. The calculated result (solid lines in Fig. 2-5) shows a cross-over of compressive and tensile stresses at ~0.08 μm. However, it is noted that the value of the thermal stress shows fair agreement with the

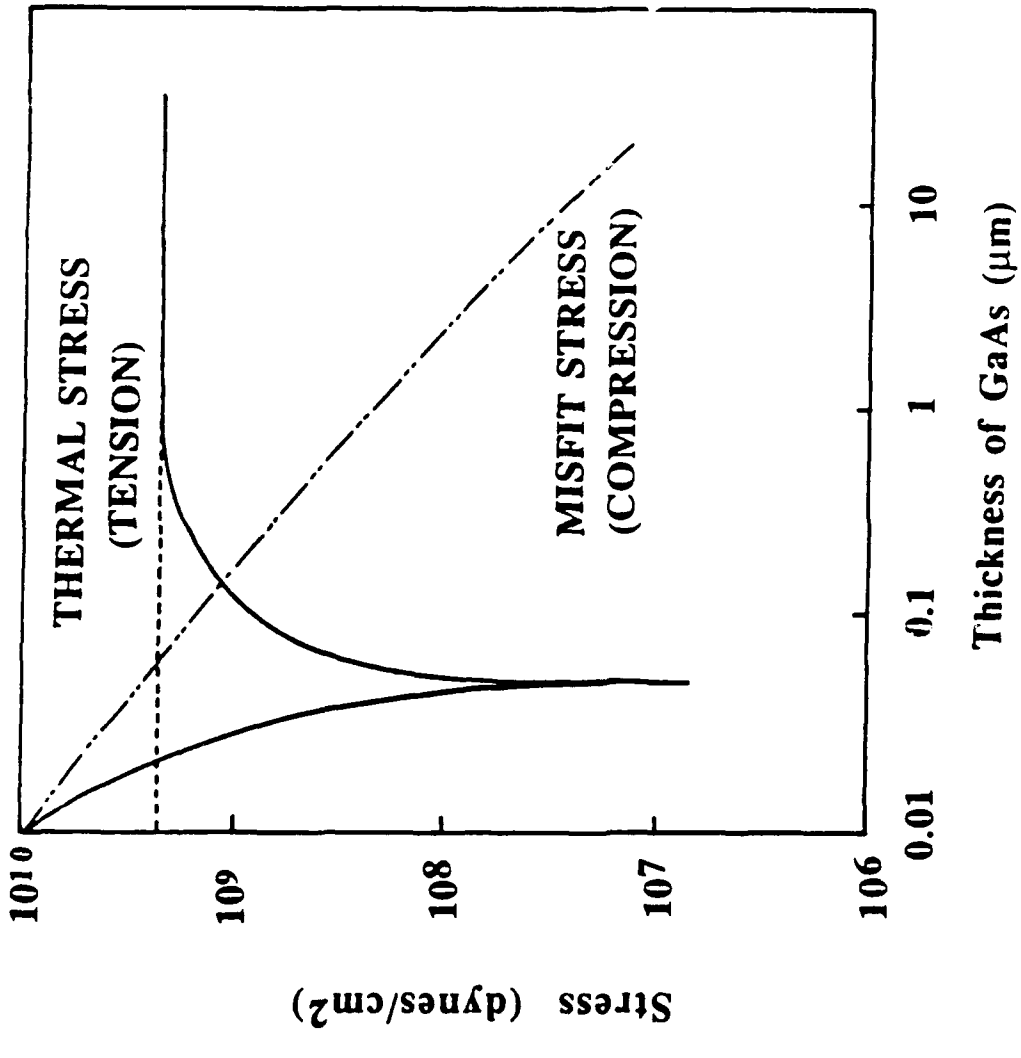



Fig. 2-5 The variation of stress in GaAs/Si system as function of GaAs thickness.

experimental values. The calculation qualitively explains the variation of residual stress in the epilayers with the film thickness.

## 2.7 Defect control

Although a number of GaAs devices and even ICs have been fabricated in GaAs on Si, the residual defects still impede the progress of GaAs on Si technology. It is clear that the combination of lattice and thermal expansion coefficient mismatches create structural and electrically active defects in the GaAs layers. Dislocations and other electrically active defects are the most important remaining obstacles for GaAs on Si to overcome in order to successfully meet most of the applications goals for the technology. There have been a variety of attempts to reduce the defect density by using: thermal annealing, strained-layer superlattices, thermally strained-layer and various nucleation schemes. This section will present a brief overview of these defect reduction techniques.

### 2.7.1 Annealing

High temperature thermal annealing is a particularly important process to reduce the defects in GaAs on Si layers for both MBE and MOCVD materials. Two different annealing methods, rapid thermal annealing (RTA)[54] and conventional furnace annealing[16], have been investigated. It was proven that both of them were effective in eliminating microtwins or stacking faults. Also well defined dislocation networks formed at GaAs/Si interface following the annealing. Perfectly aligned edge type dislocations were observed in high resolution TEM after proper annealing. However, in most cases many crack or slips are formed in the annealed surface. This may be ascribed to the film stress release during high temperature annealing. Therefore, it is necessary to minimize residual film stress.

For devices where sharp interfaces between different layers are required, high-temperature post-growth annealing is quite undesirable since usually it favors cross diffusions of dopant impurities. Moreover, recent work on GaAs/Si shows that in the case of the MOVPE, RTA enhances drastically the Si diffusion across the heterointerface[55], and also increases the residual strain level in the epilayer[56]. Therefore, a more appropriate thermal annealing step is still under investigation.

2.7.2. Cyclic annealing

Okamoto et al.[57] have reported on the use of thermal cycles (in situ TC) on dislocation reduction. The thermal cycles were carried out as follows: First, the growth was interrupted after 1.75 μm GaAs were grown, and the samples were cooled to 300°C from the growth temperature of 700°C. Immediately after that, the samples were heated to 900°C in the flow of $AsH_3$ and $H_2$. The samples were kept at 900°C for 5 minutes to effectively reduce dislocation density. After the cycles were executed either 1 or 4 times, the samples were cooled to 700°C, and the top GaAs layers were grown. The dependence of the etch-pits-density (EPD) on cycles times is shown in Fig. 2-6. As the number of cycle time is increased, the EPD is reduced. Only a slight reduction in EPD is expected by increasing the number of cycle times to more than 4.

2.7.3. Thermally strained-layer

J.W. Lee et al.[58] have proposed thermally strained-layers for the purpose of reducing defects without increasing film stress. In the usual strained-layer superlattices the lattice strain is produced by the enforced lattice mismatch of two crystals with different lattice constants. Another way to introduce strain into a heteroepitaxial layer structure is by varying the growth temperature without changing the material choice. In MBE or MOCVD for instance, if the substrate temperature can be alternated within a short time period, the epitaxial film may be either contracted or extracted periodically due to the dissimilarity of thermal expansion coefficients between the substrate material and the epitaxial material.

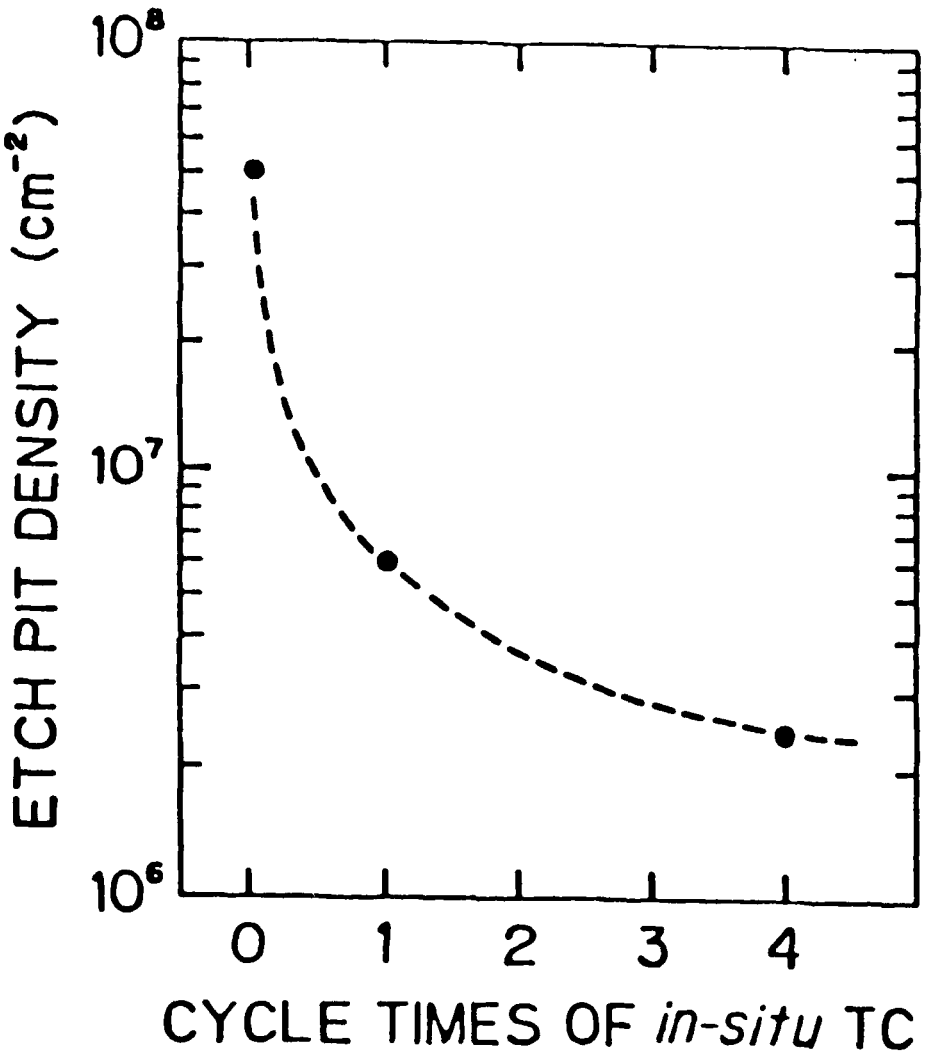



Fig. 2-6 The effect of in-situ TC cycle times on EPD. Every sample include a ten-period- $In_{0.1}Ga_{0.9}As$-GaAs SLS.

This bimetallic crystal deformation brings a dynamic strain variation into the epitaxial layer with the same period as the substrate temperature cycle. Since the strain is induced by thermal variation, we may call it a " thermally strained-layer (TSL)". The strain in the TSL will be constant whenever the growth temperature is kept constant. The strain variation during TSL growth depends on the difference between the thermal expansion coefficient of the substrate crystal and that of the epilayer crystal, as well as the amplitude of the temperature cycle. Since the GaAs thermal expansion coefficient is ~2.6 times larger than Si, GaAs TSL may introduce a relatively large strain variation into GaAs on Si layer during epitaxy. With this idea TSL may be used as a defect filtering buffer layer in GaAs-on-Si layers.

To grow such a buffer layer the substrate temperature was cycled with a short period as illustrated in Fig. 2-7. The as-grown GaAs layers were extremely smooth and flat, and compatible with ion implantion and thermal annealing processes.

2.7.4 Strained-layer superlattice

Matthews and Blakslee[59] first proposed the use of GaAsP-GaAs strained-layer superlattice (SLS) for GaAs/GaAs. Fisher et al.[12] and Bedair et al.[60] have used InGaAs-GaAs superlattices to reduce the dislocation density. Fisher is working in the high density regime with GaAs on Si, while Bedair is working in the low density regime of GaAs homoepitaxy, and both report reduction of 100-1000X. As a significant reduction in the dislocation density has been obtained. However, both GaAsP-GaAs and InGaAs-GaAs superlattice structure have all been mismatched from the GaAs in one direction. GaAsP-GaAs superlattice has a smaller average lattice constants than GaAs. On the other hand, InGaAs-GaAs superlattice has an average lattice constants larger than that of GaAs. This latice constant mismatch has several inherent shortcomings. In particular, the total thickness of the SLS should be less than the critical thickness, ($h_{c,\ max.}$), in order to prevent the generation of misfit dislocations at GaAs/SLS interface. Consequently, this

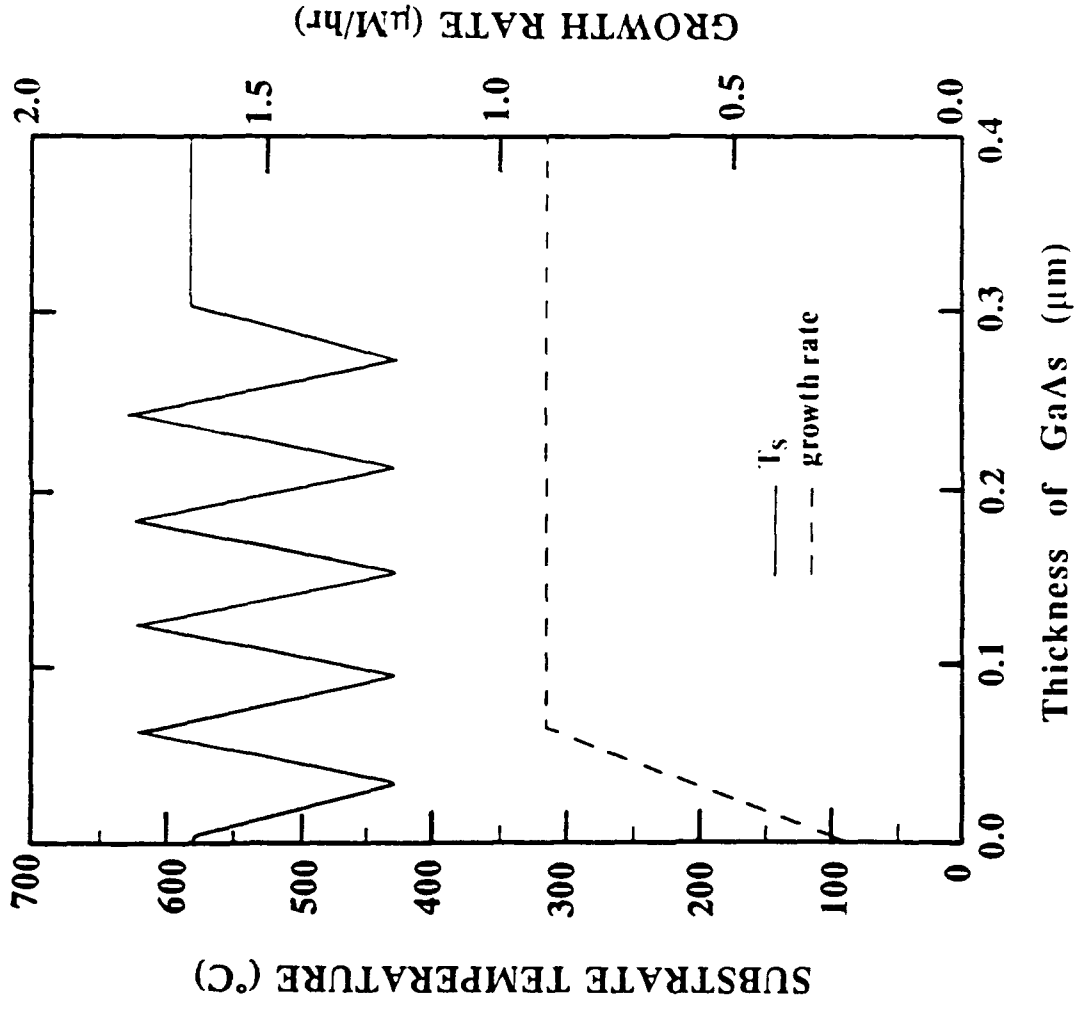



Fig. 2-7 TSL growth control.

will limit the number of interfaces capable of suppressing the propagation of threading dislocations. Furthermore, the ternary-binary SLS will also limit the amount of strain that can be present between sucessive layers in the SLS. It would seem that perhaps the most desiable final (various intermediate superlattices might also be used) strained layer superlattice would consist of materials with both larger and smaller lattice constants than GaAs, with their average being that of GaAs.

2.7.5 Impurity diffusion

Holonyak et al.[61] have shown that low temperature Zn diffusion (680°C) is effective in reducing the dislocation density in epitaxial GaAs grown on Si. The reduction in the dislocation density is suggested to be due to the increased concentration of point defects generated during the Zn diffusion, resulting in enhanced dislocation climb.

The precise mechanisms by which Zn diffusion reduces the dislocation density is not well understood; the effect is likely related to the diffusing Zn's ability to enhance the self-diffusion rate in GaAs and also $Al_xGa_{1-x}As$. This behavior leads to the much studied impurity-induced layer disordering (IILD) due to Zn diffusion in $Al_xGa_{1-x}As$-GaAs superlattices. Zinc diffuses in GaAs by an interstitial-substitial mechanism., and has been proposed to occupy a column III lattice site with the creation of a column III interstitial, e.g.,

$$Zn_I^{++} \rightarrow Zn_{Ga}^{-} + Ga_I^{+} + 2h^{+},$$

where $Zn_I^{++}$ refers to a doubly charge interstitial Zn atom, $Ga_I^{+}$ is a charged interstitial Ga atom, $Zn_{Ga}^{-}$ is the substitial Zn acceptor, and $h^{+}$ is a free hole. Note that the heavy p-type doping resulting from Zn diffusion will favor a high crystal solubility for the donor-like interstitial defects. The movement of dislocations in a crystal due to climb depends on the point defect concentrations in the crystal, since dislocation climb results in either the creation or annihilation of point defects. The effect of the Zn diffusion, therefore, is to create an excess concentration of gallium interstitial, which then may be trapped by

dislocations. This results either directly in annihilation of the dislocations, or increased dislocation motion and more intensive mutual annihilation of dislocations. It is also possible that, if the dislocations are electrically charged, the increased hole concentration due to the heavy p-type Zn diffusion could affect mobilities.

If the dislocation reduction due to Zn diffusion is related to IILD operation of Zn, then other acceptors (on column III sites) such as Be or Mg could also be effective in reducing dislocations. The greater flexibility possible in varying the p-type doping ($n_d \geq 10^{19}$) during epitaxial growth of the GaAs-on-Si may lead to greater reduction of dislocations.

2.7.6 AlGaAs-GaAs superlattice

Hayafuji et al.[62] reported on the effectiveness of using AlGaAs-GaAs superlattices in reducing dislocation density. The reduction of dislocation density is not due to the misfit strain but the crystal hardening of AlGaAs and the bending of dislocations at the superlattice. The mechanism of dislocation density reduction was proposed as following: The epitaxial layers on Si are totally subjected to tensile stress caused by the difference of thermal expansion coefficient between GaAs (or AlGaAs) and Si. Furthermore, the AlGaAs layers within the superlattice are locally subjected to the compressive stress caused by the difference of thermal expansion coefficients between AlGaAs and GaAs. On the other hand, it has been found that dislocations hardly thread in the GaAs layer by adding only a little Al, that is to say, the critical stress of AlGaAs for dislocation threading is extremely higher than that of GaAs. Since the tensile stress in GaAs layer is considered beyond the critical stress, the dislocation can thread in the GaAs layer. The dislocation threading becomes larger, with thinner the GaAs layers, because the subjected tensile stress is larger. However, since the locally subjected compressive stress in the AlGaAs layer within the superlattice is considered not to be beyond the critical stress, the dislocation might be blocked at the superlattice and bent along the interface plane.

## 2.7. Summary

Progress in sucessful growth of GaAs/Si has been substantial over the past 4 years. Perhaps most importantly, it has provided insight into the key issues for not only GaAs on Si, but other lattice mismatched heteroepitaxial systems. The important role of the Si surface ordering and misorientation are well known, although not yet fully understood. The two step growth process currently yields the best results but appears to result in island formation rather than layer-by-layer growth. Finally, the remaining dislocations and electrically active defects limit the performance of lasers and many well cause long term reliability problems for other high current or high temperature devices. The dislocations density still appears to be in the $10^7$ $cm^{-2}$ range for 2-3 μm thick films of GaAs on Si and this is too high by a factor of $10^4$. Now approaches to dislocation control may allow the realization of many new device and IC possibilities with GaAs on Si.

# 3.0 Defects and Annealing Effects

## 3.1 Introduction

Recently, considerable progress has been made in the heteroepitaxial growth of GaAs on Si. Several possible means for getting better crystalline quality by improving growth technique have already been implemented. These include the use of selected tilt substrates[11], two step growth[42, 45, 46], and Ga prelayer[28]. Despite these significant progress in GaAs on Si growth techniques, the defect density in as grown GaAs epilayer is still not satisfactory for device application. Therefore post growth defect reduction treatment is highly required to achieve this goal. This chapter is concerned with the defect reduction in GaAs epilayer grown on Si using ex-situ annealing. Detailed defects structure in as grown GaAs epilayers on Si substrates will be reviewed and the effectiveness of rapid thermal annealing and conventional furnace annealing will be discussed

## 3.2 Experiment

The GaAs/Si samples used in this study were grown by the MBE and MEE growth techniques at different laboratories. Rapid thermal annealing is made with a quartz chamber heated by twelve 2.5 kw halogon lamps. The sample is placed between two silicon wafers on which the temperature is measured through a thermocouple. The temperature flash is started at 300 °C and a temperature of 900 °C is reached within 10 seconds. The lamps are then stopped. Conventional furnace annealing was employed under an overpressure of Arsine in the metalorganic chemical vapor deposition (MOCVD) reactor at 830 °C for 50 minutes followed by slow coooling (10 °C/min). Transmission Electron Microscopy

(TEM) was used for the structure characterization. Foils for TEM were thinned by mechanical polishing followed by standard ion-thinning techniques. Cross-sectional TEM observations were performed on a Hitachi-800 (200 KV), using the conventional two-beam diffraction technique.

### 3.3 Defects structure

As mentioned in chapter 2, a high density of threading dislocations can form under non-ideal heteroepitaxial GaAs on Si growth conditions. However the sources of these threading dislocations are still not generally agreed upon. Pashly et al.[63] have discussed the possibility for dislocation introduction during epitaxial growth. These are :

(i) the extension of substrate dislocation.

(ii) the accommodation of translational and rotational displacement between agglomerating islands that are close to the epitaxial orientation.

(iii) the formation of dislocation loops by the aggregation of point defects.

(iv) plastic deformation of the film, both during growth and subsequent cooling and removal from the substrate.

The first mechanism undoubtedly operate to some extent, but, because Si substrates contain very little dislocations than are observed in overgrowth, it can not be the dominant mechanism.

The second possibility, that of dislocation generation due to the accommodation of (small) translational and rotational displacement between agglomerating islands, has been shown experimently to be a major factor. The density of nucleation sites for the islands and the manner of their subsequent coalescence will influence the dislocation density of the final film.

The next possibility for dislocation introduction is the aggregation of point defects to form dislocation loops. Because thin-film growth often occurs under highly non-equilibrium conditions point defects would be trapped in a growing film. These point defects could aggregate to form dislocations threading the foil.

The role of plastic deformation in the generation of dislocations during thin film growth is expected to be highly significant, since there are 4.1% lattice parameter and 260% thermal expansion coefficient mismatch between GaAs and Si. A density of $8*10^6$ /$cm^2$ misfit dislocation was needed to accommodate the lattice mismatch. For the thermal expansion coefficient mismatch the dislocation that will be generated will depend on the cooling rate. However, it is expected to be much higher than the needs for lattice mismatch.

Fig.3-1 shows the cross-sectional TEM micrograph of as-grown (MBE) GaAs epitaxial layer on Si substrate. The area near the GaAs/Si interface has too many dislocations to define the density. Over the first 0.5 μm the dislocation density is reduced quickly and near the 2 μm top layer it appears to be close to $2x10^8/cm^2$. The Peierls-Nabarro friction force[64] within the GaAs crystal were considered to be responsible for the decreasing dislocation density with increasing the thickness. Also, the annihiliation effect between threading dislocations at high growth temperature help the reduction of dislocations density. The in-depth profiles of dislocation density is shown in Fig.3-2. The dislocation density in GaAs diminishes as thicker epilayers are grown. This effective decrease in dislocation density corresponds to enhanced electrical and optical properties. Therefore, in order to take advantage of GaAs/Si integrated devices, it is necessary to grow GaAs epilayers greater than 2 μm in thickness to optimize material quality.

Fig.3-3 illustrates the cross-sectional TEM bright field image of MEE grown GaAs epitaxial layer on Si. The complementary dark field image is shown in Fig. 3-4. This image revealed the presence of planar defects (microtwins) on {111}-type plane in the

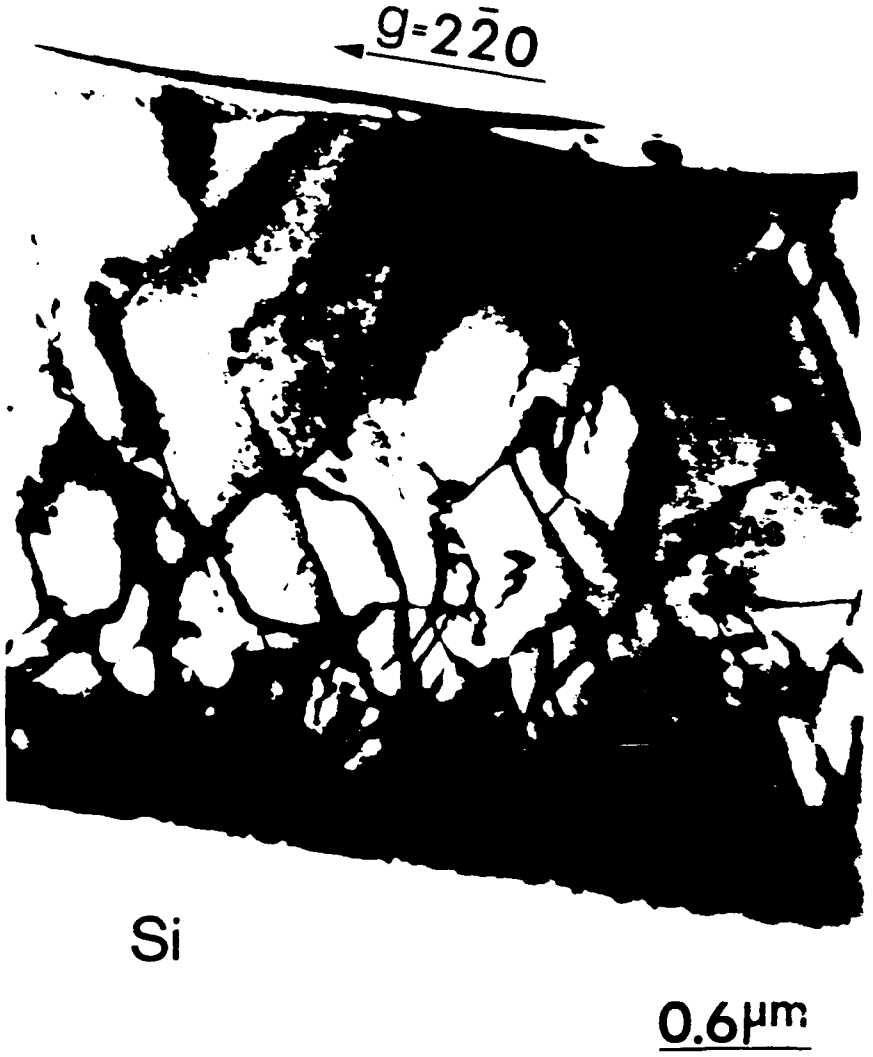



Fig. 3-1 Cross-sectional transmission electron micrograph of as grown GaAs on Si sample.

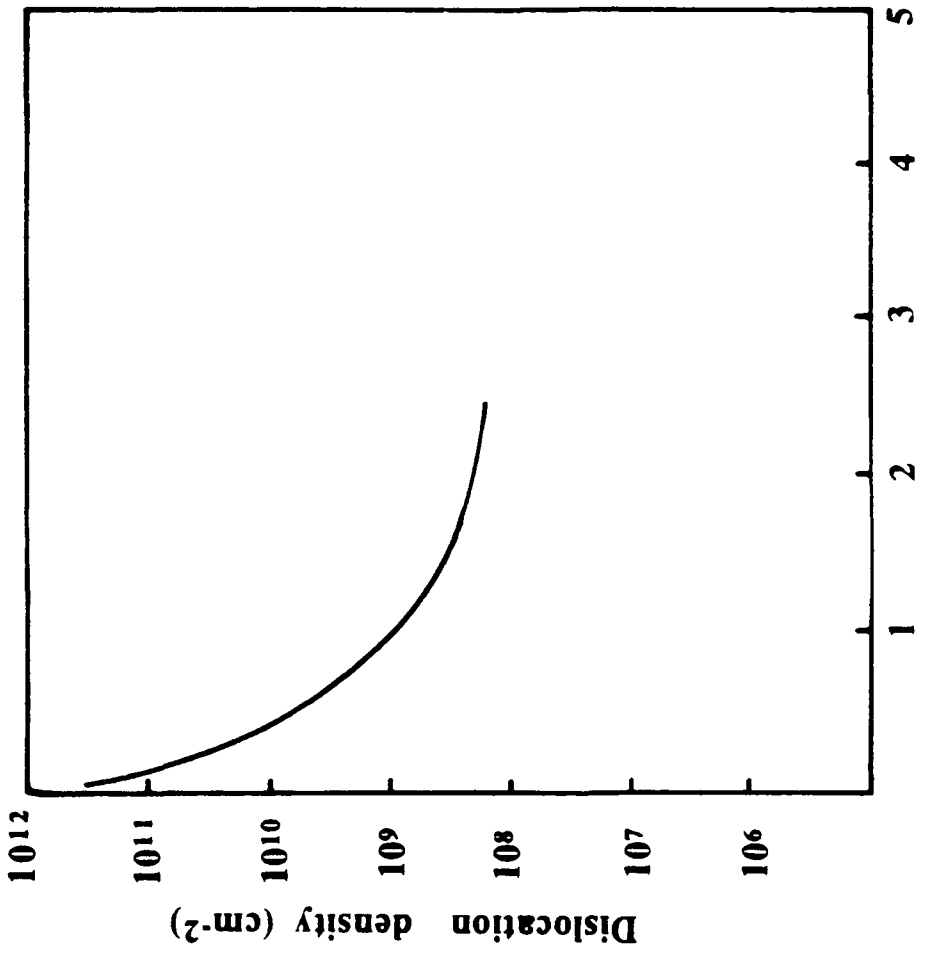



Fig. 3-2 Dislocations density profile of the GaAs layer grown on Si substrate.

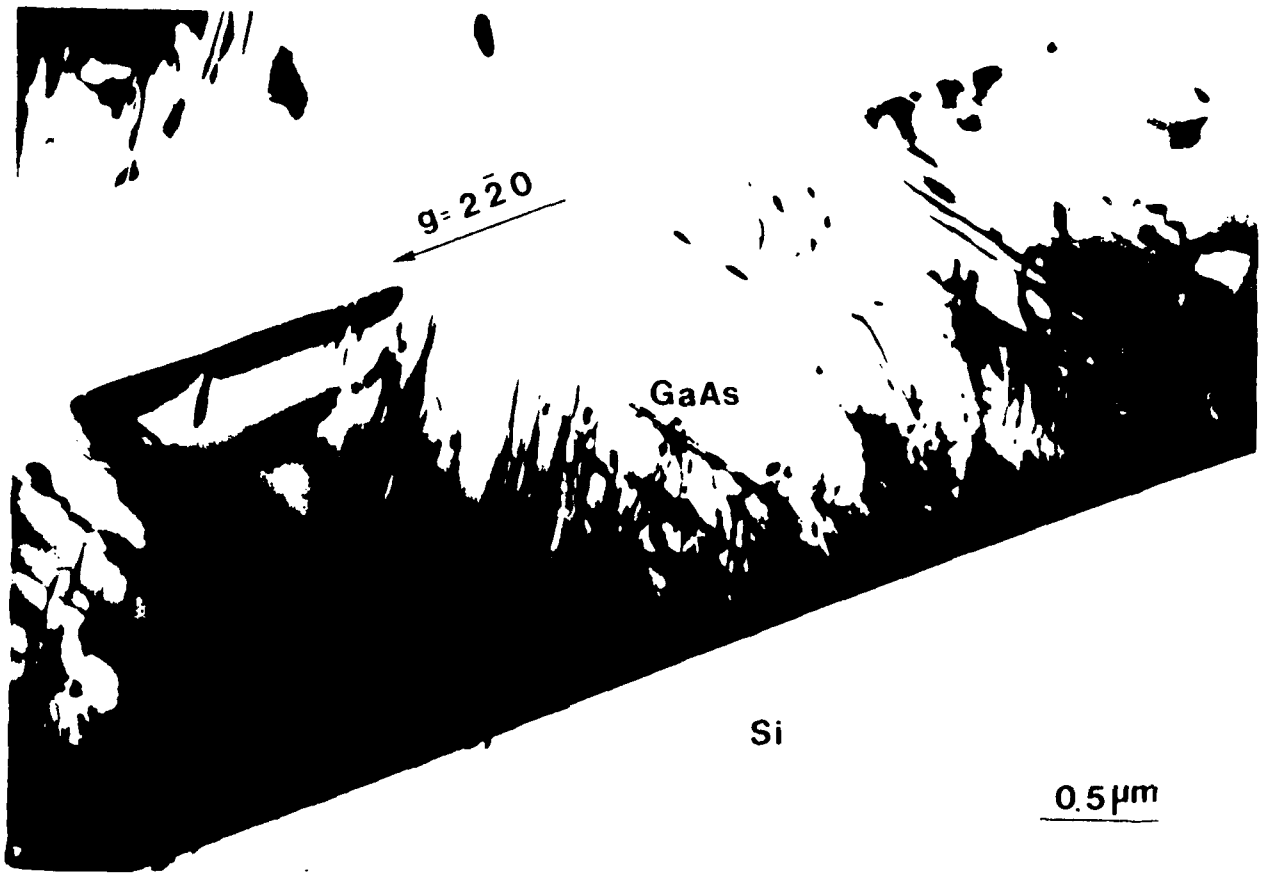



Fig. 3-3 Cross-sectional TEM bright-field image showing microtwins on {111} type plane and threading dislocations.

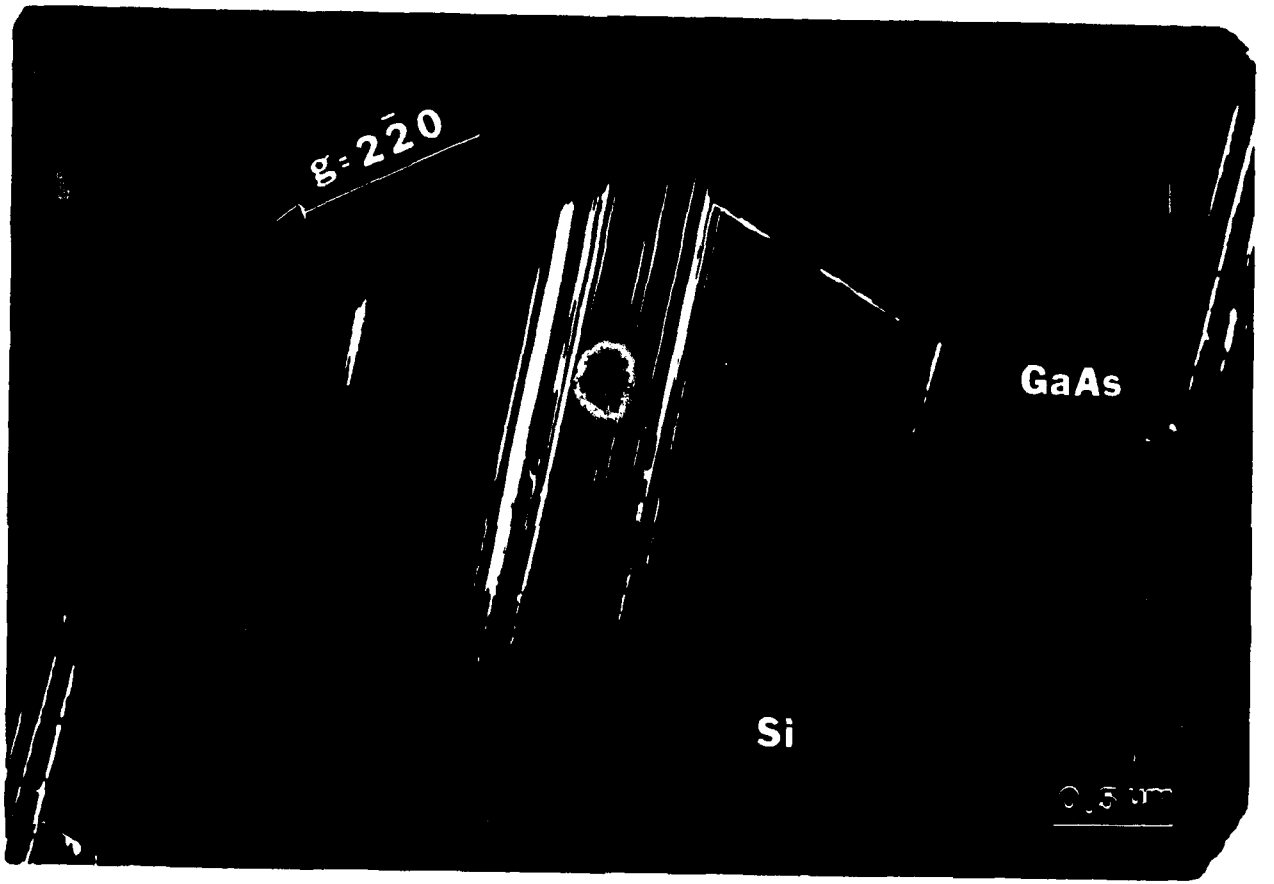



Fig. 3-4 Cross-sectional TEM dark-field image showing microtwins on {111} type plane and threading dislocations.

GaAs epilayers. These planar defects could be caused by the morphological irregularities or Si surface imperfection. It might also be from the reordering of the high strain within different islands when they merged during the initial growth[66]. The density of this planar defects across the GaAs epilayers is almost kept in the same level. However, for some planar defects when a pair of microtwins intersect, only one continues to propagate through the GaAs. This annihilation process that accompanies the increase in GaAs thickness could slightly decrease the microtwins density close to the GaAs top surface.

Fig.3-5 is a bright-field TEM image of the GaAs-on-Si grown by a different run. The image shows massive dislocations networks which have threaded from the interface to the film surface. In addition to these threading dislocations, a large number of stacking faults and microtwins are present. The weak beam dark field image, Fig.3-6, clearly illustrates the fringe contrast of stacking faults. These stacking faults might form to accommodate misfit between coalescing islands during the initial growth[66].

## 3.4 Annealing

The free energy of a highly defected thin film is greater than of that a perfect crystal by an amount approximately equal to the stored strain energy[65]. While a highly defected thin film certainly increases the entropy of the film, the effect is small compared to the increase internal energy (retained strain energy). The term -TS in the free energy equation may, therefore, be neglected and the free-energy increase equated directly to the stored energy. Therefore

$$F=E-TS \qquad (3.1)$$

becomes

$$F=E$$

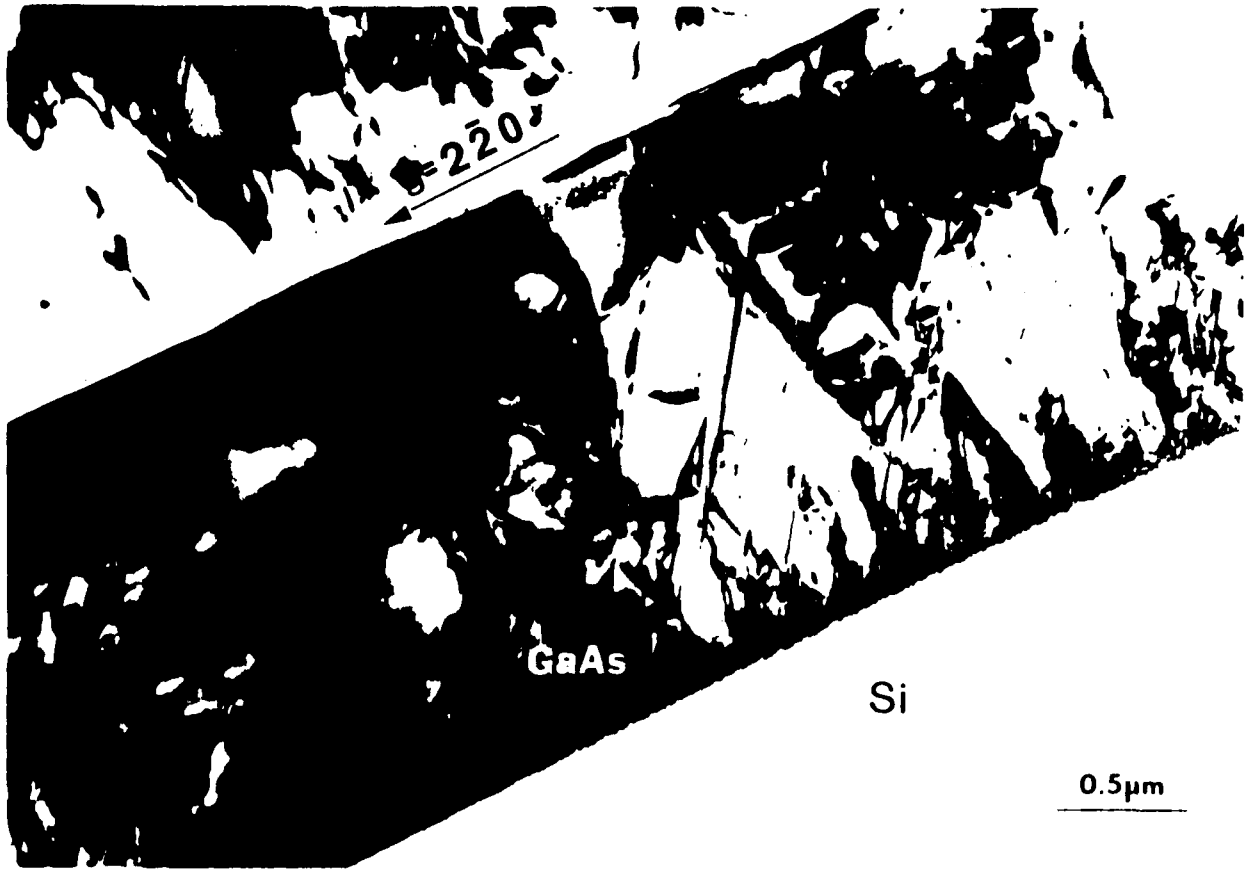



Fig. 3-5 Cross-sectional TEM bright-field image showing staching faults and threading dislocations.

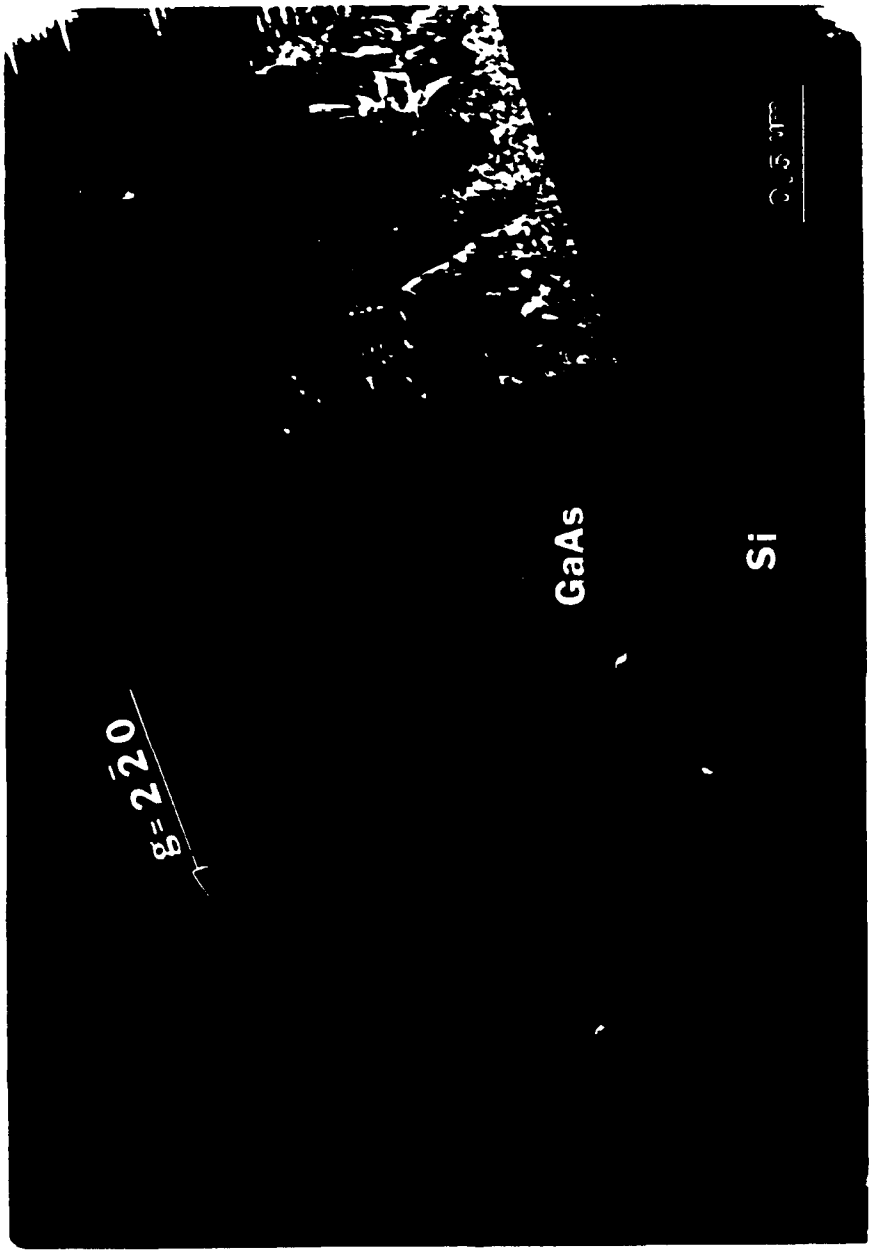



Fig. 3-6 Cross-sectional TEM bright-field image showing staching faults and threading dislocations.

where F is the free energy associated with the defects, E is the internal, or stored energy, S is the entropy increase due to the defects, and T is the absolute temperature.

Since the free energy of highly defected thin films is greater than that of a perfect crystal, the defects density may decrease spontaneously. However, a highly defected thin film does not return to the ideal condition by a simple reaction because of the complexity of its state. Heating a highly defected thin film, therefore, greatly speeds up the defects reduction processes.

The technique of annealing is widely used for recovery and recrystallization of plastically deformed crystals. The driving force for these processes to occur is the reduction of strain energies accompanying the defects which were created by deformation, and hence, their rates depend directly on the degree of deformation. This technique is, therefore, expected to be very effective for improving microstructure of epilayers having a high density of defects due to nonideal growth conditions. Despite the progress made to date, the reproducible optimization of the growth condition of GaAs on Si has not yet been achieved. The poor quality epilayers has often resulted from unoptimized growth conditions. It is believed that annealing can be used as an effective technique to supplement the method developed earlier for defect density reduction. A recent study[16, 54] has also indicated that the most efficient way to eliminate defects is by post-annealing. Post annealing has resulted in a great reduction of defects in the upper part of the film[16, 54]. However, due to the difference in the thermal expansion coefficients of GaAs and Si the internal stress in GaAs can be affected by the annealing procedure. Since additional stresses will produce more defects, then the annealing process must be chosen appropriately to eliminate the production of additional stress in the materials. Both conventional furnace annealing combined with slow cooling and rapid thermal annealing were employed for comparative study.

The cross-sectional TEM bright field micrograph, Fig.3-7, illustrates the defect morphology in GaAs film on Si after rapid thermal annealing (RTA). Compared with as grown GaAs epilayer, microtwins and stacking faults were all eliminated after RTA. However, a much higher threading dislocation density can be found in GaAs epilayer after RTA. A recent study[56] has indicated that RTA drastically increases the residual stress/strain level in GaAs films. It has also been demonstrated that the residual stress/strain in the GaAs is attributed mainly to the difference in thermal expansion (between GaAs and Si) during cooling from the processing temperature to room temperature. Cooling rate is considered as an important factor for the level of residual thermal stress/strain in the GaAs films. The fast cooling rate during RTA enhances the thermal stresses in GaAs epilayer on Si. Although rapid thermal annealing is proved to be useful for improving a number of properties of a variety of epitaxial heterostructures. A number of threading dislocations can be induced in GaAs epilayers from the highly enhanced thermal stress after RTA.

Fig.3-8 illustrates the cross-sectional TEM bright field image of GaAs epilayer on Si substrates after conventional furnace annealing/slow cooling. Apparently, both stacking faults and microtwins which originally appeared in as grown GaAs epilayer on Si were completely eliminated. Also well defined dislocation networks formed at GaAs/Si interface following the annealing and only a few threading dislocations are present near the GaAs film top surface. By the conventional furnace annealing/slow cooling process, the dislocation density in GaAs top surface is reduced from $2x10^8/cm^2$ to $8x10^7/cm^2$ which is more effective than RTA. Theorectically, a density of $\sim 8x10^6/cm^2$ misfit dislocations are needed to accommodate the lattice mismatch between GaAs and Si. Many threading dislocations, which are not directly contributing to the accommodation of the lattice mismatch beteween GaAs and Si and simply raise the free energy of the system, are eliminated after the conventional furnace annealing. However prolonged annealing did not

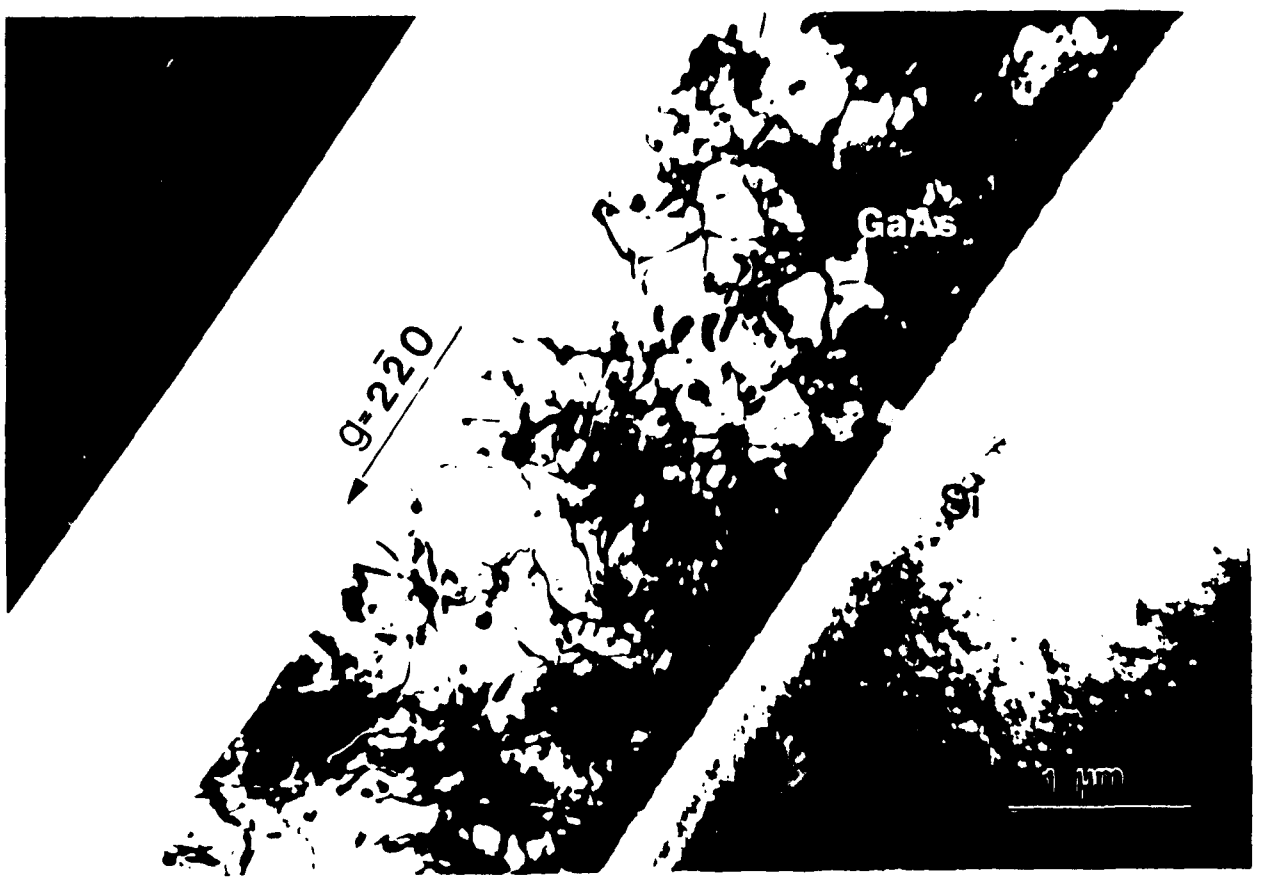



Fig. 3-7 Cross-sectional transmission electron micrograph of GaAs on Si sample after rapid thermal annealing (900°C, 10 sec).

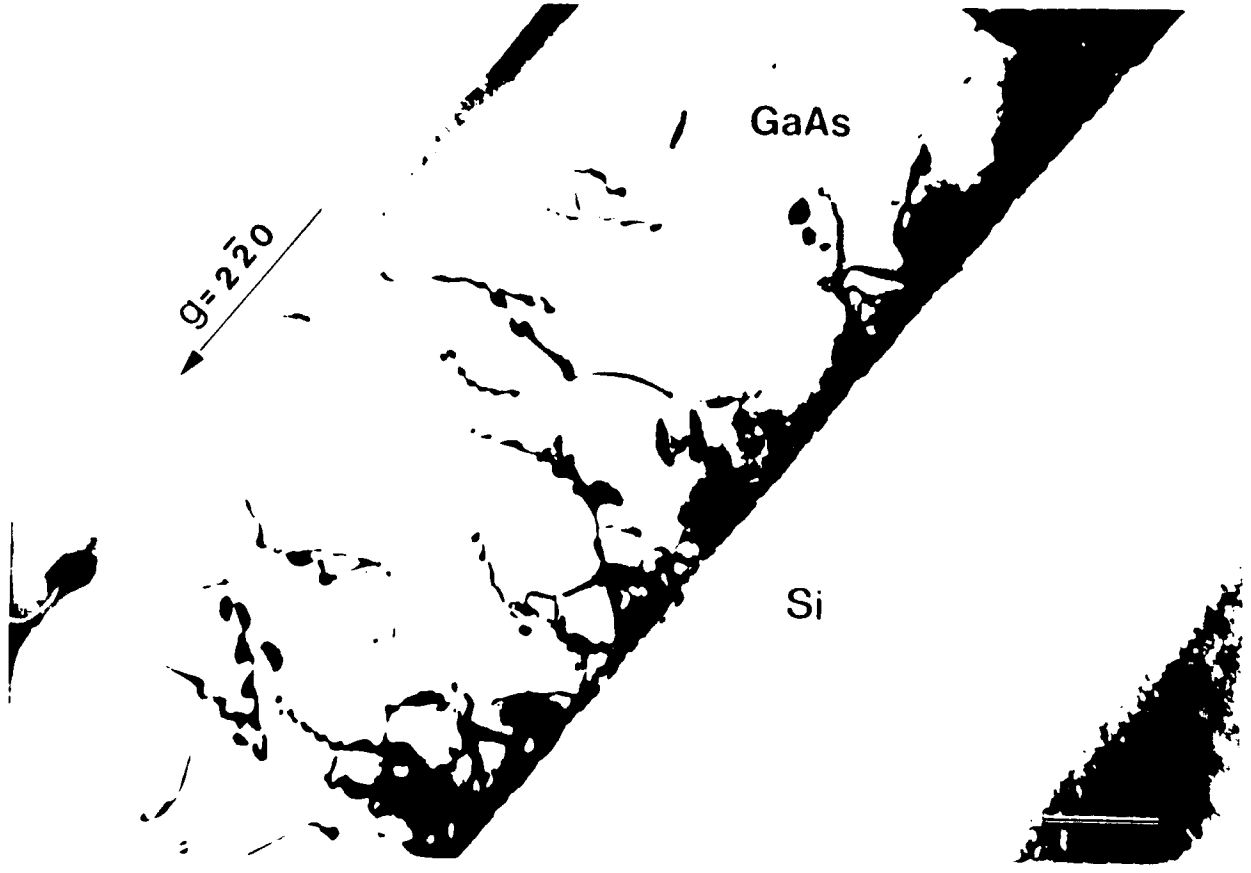



Fig. 3-8 Cross sectional transmission electron micrograph of GaAs on Si sample after conventional thermal annealing (830°C, 1 hr.)

achieve any further dislocation reduction. At this dislocation density the chance of dislocation interaction is low. The limitation is attributed to the thermal expansion coefficient mismatch between GaAs and Si. The in-depth dislocation density profile, Fig.3-9, show the dislocation density in conventional furnace annealed GaAs-on-Si drastically decreasing with increasing layer thickness and seem to saturate at thickness of about 2 μm.

## 3.5 Summary

Detailed defects structure in GaAs epilayer grown on Si substrates were observed using Transmission Electron Microscopy. The presence of threading dislocations, microtwins, and stacking faults have also been observed in different as grown GaAs epitaxial layer on Si. Two different annealing methods, conventional furnace annealing/slow cooling and rapid thermal annealing, have also been investigated. It is proven that both of them were effective to eliminate microtwins and stacking fault. However, the conventional furnace annealing/slow cooling showed more promising results in terms of dislocations reduction. This study also provided insight into the important role of residual stress/strain in achieving successive defect reduction technique. This conventional furnace annealing reduces dislocation density to about high $10^7/cm^2$. However, these defect densities are still several orders of magnitude higher than the required for most device applications, therefore, other means of reducing the defect density are needed.

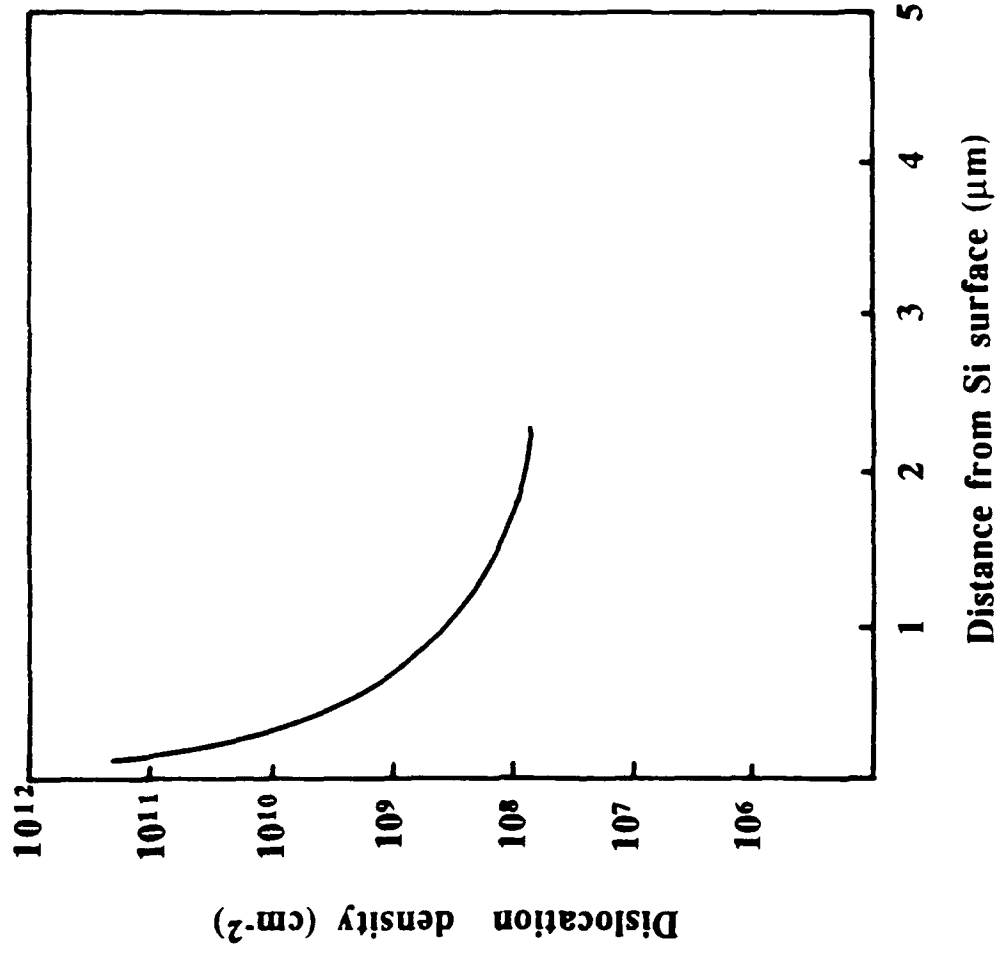



FIG. 3-9 Dislocation density profile of conventional furnace annealed GaAs epitaxial layer grown on Si substrates.

# 4.0 STRAINED LAYER SUPERLATTICE

## 4.1 Introduction

Esaki and Tsu[67] suggested that interesting electronic properties could be achieved in a "superlattice" comprising a succession of thin layers of alternating composition. In many applications, the multilayer structure, called strained layer superlattice, can be used to create semiconductors with tailored bandgaps by varying the thickness and periodicity of the layers[68]. The superlattice can also be used as dislocation barriers between Si and other compound semiconductors[69,70,71]. In this chapter, the application of the "strained-layer superlattice" concept in reducing defects in GaAs epitaxial films grown on Si substrate is discussed. The misfit strain in the strained layer superlattice can be used to drive threading dislocations to the edge of the epitaxial thin film and thus improve its quality. This process is influenced by the film thickness, the orientation of the interface, the dimensions of the interface paralled to its plane, and the misfit between the film and the substrate.

The following parameters has been considered during this study :

(1) The maximum film thickness (maximum critical thickness, $h_{c,\,max.}$) at which new misfit dislocations become energetically favorable to be created by the strained-layer superlattice.

(2) The film thickness (minimum critical thickness, $h_{c,\,min.}$) at which threading dislocations glide to the edge of the sample and escape.

(3) The density of threading dislocation that can be removed by glide.

## 4.2 Maximum critical thickness

In many applications, the multilayer structure must be free of dislocations to achieve optimum properties, yet the lattice mismatch associated with the strained-layer superlattices produces coherency strains in the as-grown layer structures that enhance the likelihood of misfit dislocation formation. The existence of this maximum critical thickness was first detailed by Van der Merwe[72, 73], and later by several authors including Matthews et al.[74] and People and Bean[75].

### 4.2.1 Van der Merwe's Model

Van der Merwe[72, 73] initially calculated the maximum critical layer thickness of a lattice mismatched overlayer on the basis of energy consideration. To determine for each film thickness the most stable configuration of the system, the sum of the elastic strain areal energy density ($E\varepsilon$) and the areal energy density corresponding to a grid of misfit dislocations ($E\delta$) was minimized :

$$\frac{\partial ( E_\varepsilon + E_\delta )}{\partial \varepsilon} = 0 \qquad (4.1)$$

The energy per unit area associated with elastic strain in the film is given by

$$E_\varepsilon = [ \frac{2 \mu (1+\upsilon)}{1-\upsilon} ] \varepsilon^2 h \qquad (4.2)$$

with $\mu$ is the shear modulus, $\upsilon$ is Possion's ratio, $\varepsilon$ is the elastic strain parallel to the film plane, and h is the film thickness. Equation 4.2 is exact for isotropic solids and for cubic crystals in case the film orientation is {001}, {011}, or {111}. [For anisotropic solids $\mu$ and $\upsilon$ should be expressed in the general elastic constants as $\mu=1/2(C_{11}-C_{12})$ and $\upsilon=C_{12}/(C_{11}+C_{12})$.] In other cases Equation 4.2 is a good approximation.

In the derivation of the energy density of the dislocation network, Van der Merwe started with an integration over the interface potential, eventually leading to

$$E_\delta = \frac{\mu b}{\pi^2\sqrt{2}}(1+\beta-\sqrt{(1+\beta^2)}-\beta\ln\{2\beta[\sqrt{(1+\beta^2)}-\beta]\} \tag{4.3}$$

with

$$\beta=\pi(f-\varepsilon)2\sqrt{2}(1-\upsilon)$$

Here b is the magnitude of the Burgers vector of an edge-type dislocation in the interface plane and f is the lattice mismatch.

Based on energy minimization, the equilibrium theory predicts the maximum critical thickness as

$$h_{c,\,max.} = \frac{b}{16\pi f(1+\upsilon)}(-\ln\{2\beta[\sqrt{(1+\beta^2)}-\beta]\}) \tag{4.4}$$

The dependence of maximum critical thickness on relative misfit in the case of Van der Merwe's calculation is illustrated in Fig. 4-1.

4.2.2 Matthews and Blakeslee's Model

Matthews and Blakeslee's[74] approach was slightly different. They composed an expression for the dislocation grid energy density from the energies of individual (edge) dislocations. The energy of an edge dislocation in the interface between a pair of crystals is approximately

$$E_e = \frac{\mu b}{4\pi(1-\upsilon)}[\ln(R/b)+1] \tag{4.5}$$

where b is the magnitude of the Burgers vector of the dislocation, and R the distance to the outermost boundary of dislocation's strain field. The separation of misfit dislocations depends on the fraction of total misfit that is accommodated by dislocation lines. If the stress-free lattice parameters of the overgrowth and the substrate are $a_f$ and $a_s$ respectively,

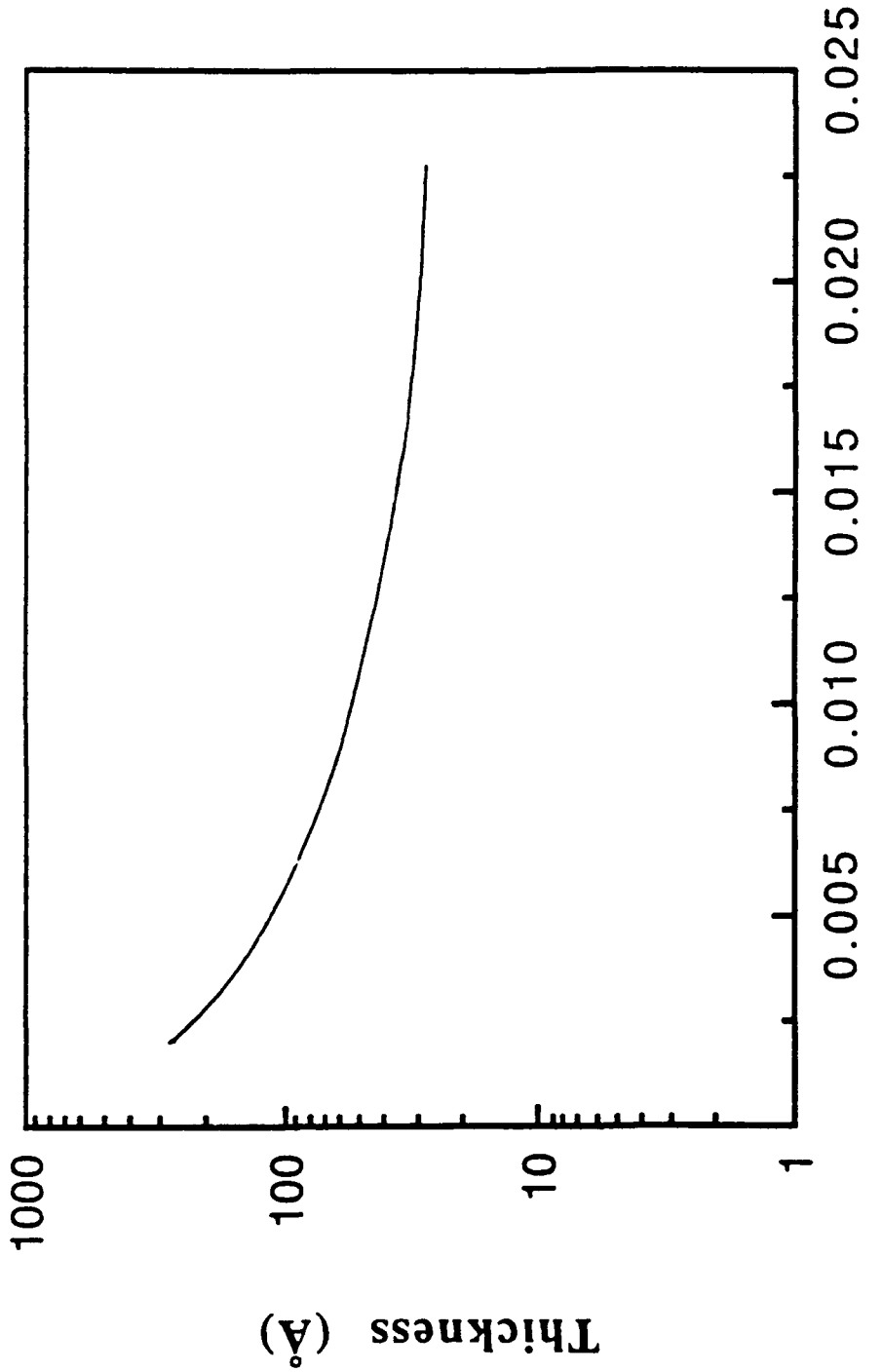



Fig. 4-1 Plot of the calculated maximum critical thickness vs.mismatch (f) from Van der Merwe's model.

and the thickness of the film is much less than the thickness of its substrate, then a convenient definition of the total misfit is

$$f= (a_s - a_f) / a_s \tag{4.6}$$

If a film is strained so that the lattices of the film and substrate are in register at the interface, then $\varepsilon=f$. If the misfit is shared between dislocations and strain, then

$$f= \varepsilon + \delta \tag{4.7}$$

where $\delta$ is the misfit accommodated by dislocations. A positive value for f implies that strain is tensile and that misfit dislocations are positive Taylor dislocation (i.e. the extra atomic planes lie in the overgrowth). The separation of parallel misfit dislocation is

$$S=b/\delta \tag{4.8}$$

The energy of two perpendicular and noninteracting arrays of edge dislocations with separation S is approximately

$$E_\delta = \frac{\mu\, b\, (f-\varepsilon)}{2\,\pi\,(1-\upsilon)}\,[\,\ln(R/b)+1] \tag{4.9}$$

The appropriate value for R is difficult to determine. However, if 2S is less than the film thickness h, then R≈S. If 2S>h, then R=h and the value of $\varepsilon$ that minimizes $E_\delta+E_\varepsilon$ is

$$\varepsilon^*= [\,\frac{b}{8\pi(1+\upsilon)h}\,][\,\ln(h/b)+1] \tag{4.10}$$

The largest possible value for $\varepsilon^*$ is the misfit f. If the value of $\varepsilon^*$ predicted by Eq.(4-7) is equal to or larger than f, the film will be strained to match the substrate precisely. If $\varepsilon^*$ is smaller than f, then a portion of f, equal to $\delta=f-\varepsilon^*$, will be accomodated by dislocations. The thickness at which it becomes energetically favorable for the first misfit dislocations to be made is obtained by setting $\varepsilon^*=f$ in Eq.(4-7):

$$h_c= [\,\frac{b}{8\pi(1+\upsilon)f}\,][\,\ln(h/b)+1] \tag{4.11}$$

If the film thickness is such that $\delta \geq 2b/h$, then $R \approx S = b/(f-\varepsilon)$ and

$$h_c = \left[\frac{-b}{8\pi(1+\upsilon)\varepsilon^*}\right] \ln 2(f-\varepsilon^*) \tag{4.12}$$

The misfit strains predicted by this equation are slightly larger than those predicted by more sophisticated calculation of Van der Merwe et al.[72] Fig. 4-2 illustrates the maximum critical thickness -misfit relations of Eq. (4.11) and (4.12).

4.2.3 People and Bean's Model

Analogously to Van der Merwe's[72, 73] original approach, People and Bean[75] equated the strain areal energy density to an interfacial energy density. They assumed that the growing film is initially free of threading dislocations, and that interfacial misfit dislocations will be generated when the areal strain energy density [of Eq. (4.2)] exceeds the self energy of an isolated dislocation of a given type. Due to the fact that the screw dislocation have the minimum energy density, being less than the edge dislocation energy density by a factor of $1/(1-\upsilon) \approx 1.4$. The areal energy density associated with an isolated screw dislocation at a distance h from a free surface is approximately

$$E_\delta = \left[\frac{\mu b^2}{8\pi\sqrt{2}\,a(x)}\right]\left(\ln\frac{h}{b}\right) \tag{4.13}$$

where a(x) is the bulk lattice constant of the film and h denotes the film thickness. Equating (4.2) and (4.13) and set $h = h_{c,\,max.}$, one obtains.

$$h_{c,\,max.} \approx \left(\frac{1-\upsilon}{1+\upsilon}\right)\left(\frac{b}{40\pi}\right)\left[\left(\frac{1}{f^2}\right)\ln(h_c/b)\right] \tag{4.14}$$

The maximum critical thickness vs. misfit of Eqn (4.14) is as shown in Fig. 4-3.

4.2.4. A Revised Model

In the diamond- and Zinc-blende-type lattice, perfect dislocations have Burgers vector b=a/2<110>[78, 79, 80,81]. Of the three main types, namely, edge-, screw-, or 60°-

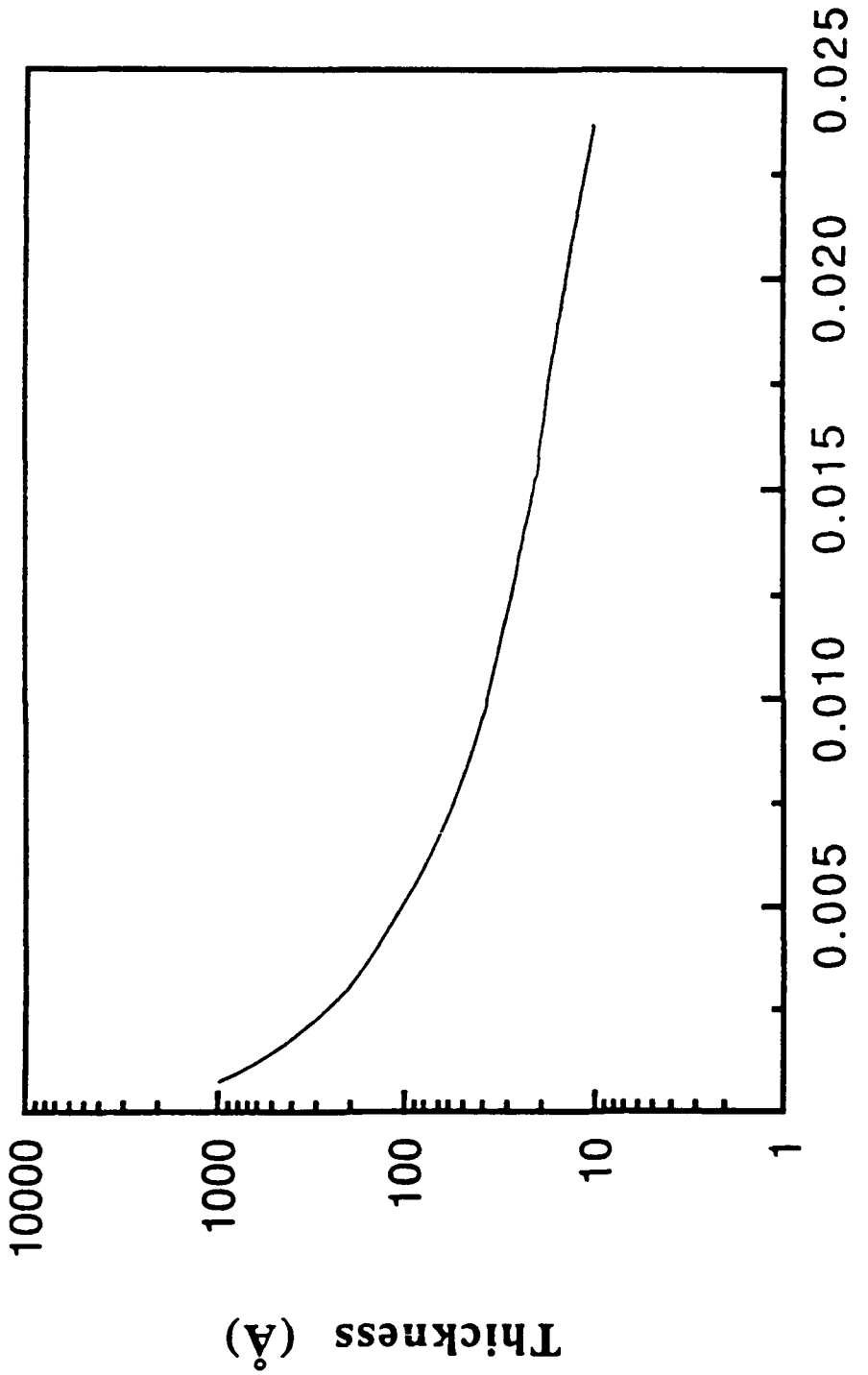



Fig. 4-2 Plot of the calculated maximum critical thickness vs.mismatch (f) from Matthews and Blakeslee's model.

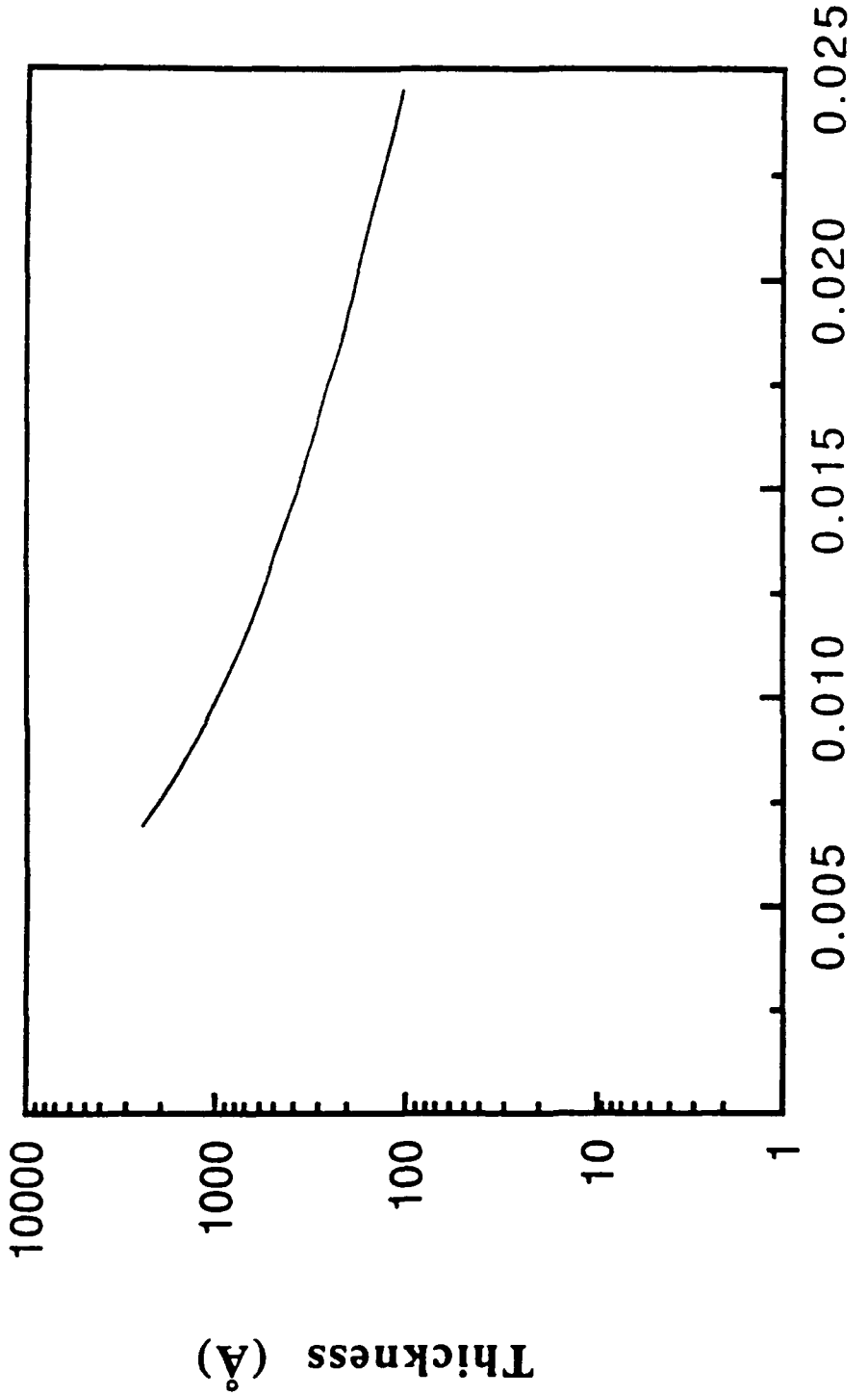



Fig. 4-3 Plot of the calculated maximum critical thickness vs.mismatch (f) from People and Bean's model.

mixed dislocations, the edge type has the highest core energy[78, 79] and the screw type cannot relax tetragonal mismatch, leaving the 60°-mixed type as the most likely one to relax the lattice mismatch in a bicrystal. We recalculated the maximum critical thickness considering that in GaAs films the dislocations are predominantly of 60°-mixed type instead of pure edge dislocations.

Then Van der Merwe's[72, 73] expression becomes

$$h_c = \frac{b\,(1-\upsilon/4)}{8\,\pi\,f\,(1+\upsilon)}\,(-\ln\{\,2\,\beta\,[\sqrt{(1+\beta^2)}-\beta\,]\,\}), \tag{4.15}$$

and Matthews and Blakeslee[74] expression leads to

$$h_c = [\,\frac{b\,(1-\upsilon/4)}{2\,\pi\,(1+\upsilon)\,f\cos\lambda}\,]\ln(h/b)+1] \qquad \text{for } 2S > h \tag{4.16}$$

$$h_c = [\,\frac{-b\,(1-\upsilon/4)}{2\,\pi\,(1+\upsilon)\varepsilon^{*}\cos\lambda}\,]\ln 2\,(f-\varepsilon^{*}) \qquad \text{for } \delta \geq 2b/h \tag{4.17}$$

However, for GaAs-on-Si system the threading dislocation density ( $\geq 10^7/cm^2$) at the GaAs buffer upper surface is high enough to relax some of the strain in the multilayer structure by bend-over process. The maximum critical thickness will be much higher than the values pedicted by Van der Merwe and Mathews. If the density of threading dislocation removed by glide is $\rho$, then the strain been relaxed is $\rho b/8$. Van der Mer's expression becomes

$$h_c = \frac{b\,(1-\upsilon/4)}{8\,\pi\,(\,f-\rho b/8\,)\,(1+\upsilon)}\,(-\ln\{\,2\,\beta\,[\sqrt{(1+\beta^2)}-\beta\,]\,\}), \tag{4.18}$$

Matthews and Blakeslee's expression converts to

$$h_c = [\frac{b\,(1-\upsilon/4)}{4\,\pi\,(1+\upsilon)\,(f-\rho b/8)\cos\lambda}][\,\ln(h/b)+1] \qquad \text{for } 2S > h \tag{4.19}$$

$$h_c = \left[\frac{-b(1-\upsilon/4)}{4\pi(1+\upsilon)\varepsilon^{*}\cos\lambda}\right] \ln 2\,(f-\rho b/8-\varepsilon^{*}) \qquad \text{for } \delta \geq 2b/h \tag{4.20}$$

Fig.4-4 shows the relation between the maximmum critical thickness and the misfit for two different densities ( $\rho=10^6$ cm$^{-2}$ and $5*10^6$ cm$^{-2}$ ). It is apparent that the higher the bend-over dislocation density, the more difficult for new dislocations to be generated if strained film growth is continued. This is because part of the misfit strain parallel to the film plane has been relaxed by the formation of bent-over misfit dislocation segment. The residual misfit strain is less energetically favorable for new dislocation nucleated by strained layer when the film growth is continued.

## 4.3 Conditions for the removal of threading dislocations

The removal of a threading dislocation as a result of the force exerted on it by the misfit strain is illustrated in Fig. 4-5. In this figure a threading dislocation (labeled "A") extends from the substrate to the free surface of an epitaxial film. This dislocation bows under the influence of the misfit strain, and when the film thickness exceeds a critical value, it glides to the edge of the sample and escapes. Bowing and motion to the specimen edge are shown by dislocation B and C respectively.

Matthews et al[69,70,71] have initially given an in-depth review of this minimum critical thickness, as obtained via mechanical equilibrium theory. Hirth[79] re-examined this dislocation bending process in multilayer structures for the anisotropic case with the purpose of defining the possible variation in $h_{c,\,min.}$ values. In our derivation we assumed that the minimum critical thickness is determined solely by energy balance. This approach differs from the previous theory.

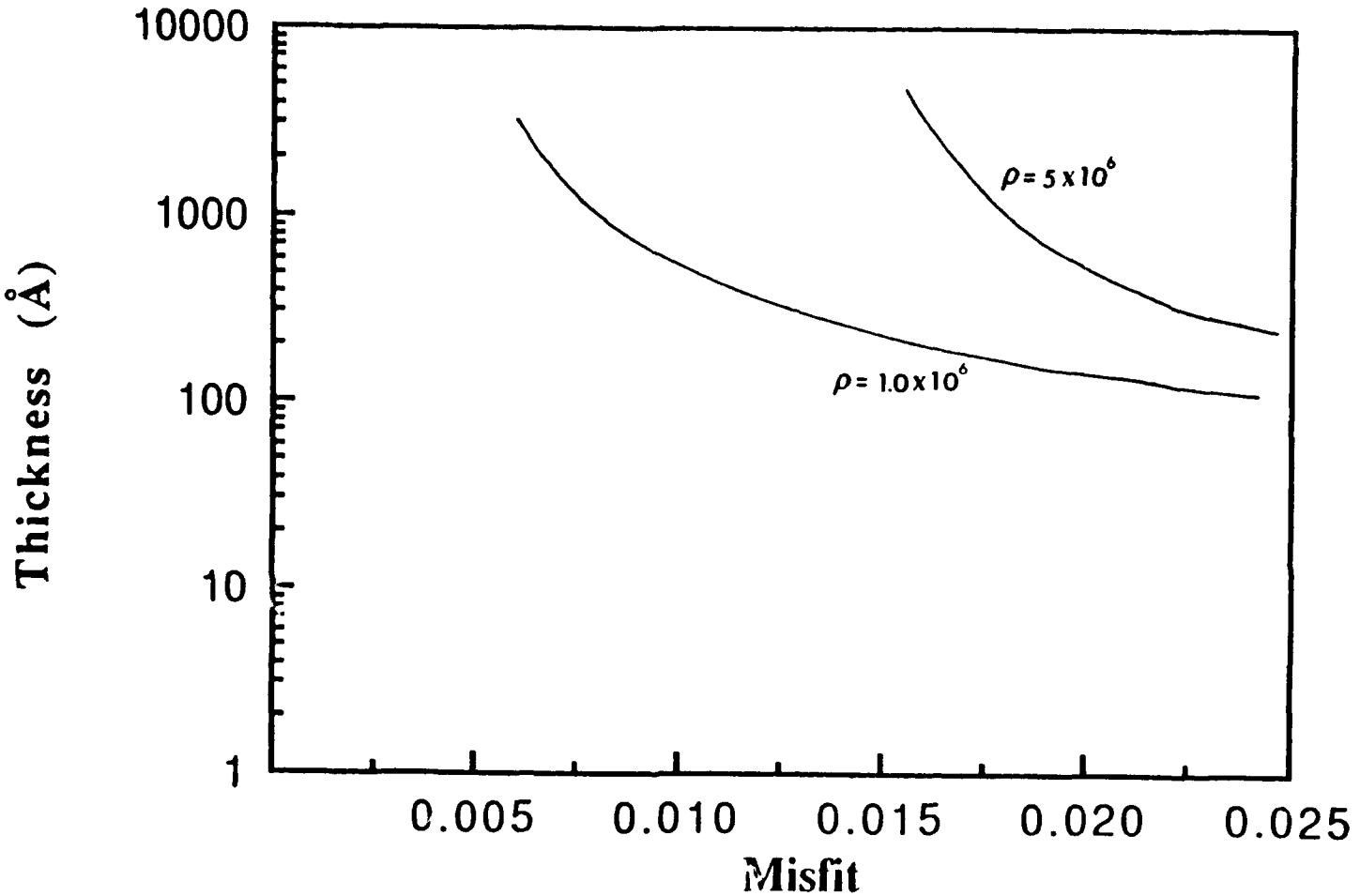



Fig. 4-4 Plot of the calculated maximum critical thickness vs.mismatch (f) from our revise model for two different densities of bent-over dislocation ($\rho = 10^6$ cm$^{-2}$, $\rho = 5\times10^6$ cm$^{-2}$ ).

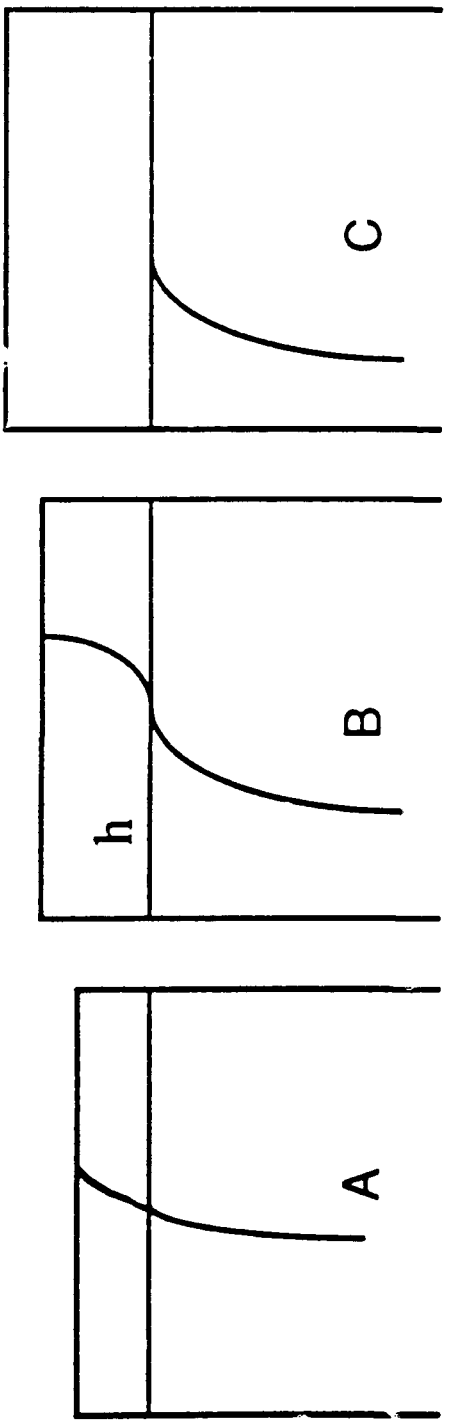



Fig. 4-5 Stages in the removal of a threading dislocation from an epitaxial thin film.

### 4.3.1 Critical thickness ($h_{c,\ min.}$)for the removal of threading dislocations

4.3.1. Matthews and Blakeslee's Mechanical Equilibrium Model[69, 70, 71]

Fig. 4-6 shows a grown-in threading dislocation in a (a) coherent interface, (b) critical interface, and (c) incoherent interface; the nature of the interface is determined by the epilayer thickness h. The tension in the dislocation line is denoted by $F_D$ and the force exerted on the dislocation line by misfit stress is denoted by $F_H$. Initially, the interface is assumed to be coherent for film thickness $h_a$ ; and critical for film thickness $h_b$ (i.e. $F_H = F_D$), whereas, for film thickness $h_c$ , $F_H > F_D$, allowing the dislocation to elongate in the plane of interface, thereby producing a length LL' of misfit dislocation line.

Assuming the elastic constants of the two media A and B are equal, the force exerted on the dislocation line by misfit stress is

$$F_H = 2\mu \frac{(1+\upsilon)}{(1-\upsilon)} b\, h\, \varepsilon \cos\lambda \qquad (4.\ 21)$$

$\mu$ is the shear modulus of B and C, $\upsilon$ is the Possion ration and $\lambda$ is the angle between the slip direction and that direction in the film plane which is perpendicular to the line of intersection of the slip plane and the interface. The tension in the dislocation line is approximately

$$F_D = \frac{\mu b^2 (1-\upsilon\cos^2\beta)}{4\pi(1-\upsilon)}\left[\ln\left(\frac{h}{b}\right)+1\right] \qquad (4.22)$$

where ß is the angle between the dislocation line and its Burger vector.

The maximum value of the strain $\varepsilon_{max.} = f$. If $F_H > F_D$, the dislocations move and hence $h_{c,\ min.}$ is determined by the equality of $F_H$ and $F_D$. Equating (4.21) and (4.22), and making the replacement $h=h_{c,\ min.}$ and $\varepsilon=f$ one obtains

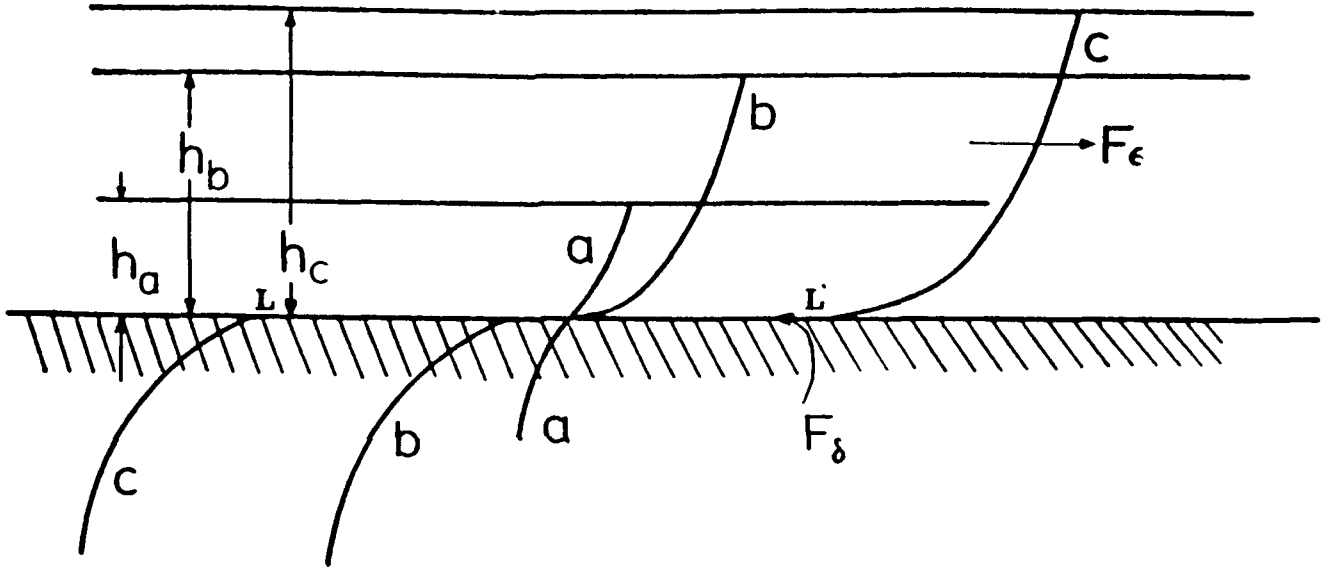



**Fig. 4-6 Elongation of a grown-in threading dislocation to form a length LL' of misfit dislocation line. Initially the interface is assumed coherent (a); for film thickness $h_b$ the interface is critical (i.e. $F_\epsilon = F_\delta$); whereas for film thickness hc, $F_\epsilon > F_\delta$ allowing the dislocation to elongate in the interface plane, thereby producing a length LL' of misfit dislocation line.**

$$h_{c,min} = \left[\frac{b(1-\upsilon\cos^2\beta)}{8\pi f(1-\upsilon)\cos\lambda}\right]\left[\ln\left(\frac{h_{c,min}}{b}\right) + 1\right] \qquad (4.23)$$

A plot of the minimum critical thickness-misfit relation given by Eq(4.23) is shown in Fig.4-7.

4.3.2. Elastic Anisotropic Model[79]

Hirth[79] re-examined the dislocation bending process in multilayer structures for the anisotropc elastic case with the purpose of defining the possible variation in $h_c$, min. values.

Loss of coherency occurs by the generation of a dislocation dipole as depicted in Figure 4-8. The dipole could nucleate at a free surface or simply spread from a threading dislocation. The (111) glide plane and the Burgers vector a/2[011] are inclined to the (001) interfaces. The force arising from the coherency stress is conveniently determined by coordinates fixed on the glide system, i'=[001]/$\sqrt{2}$, j'=[111]/$\sqrt{3}$, k'=[211]/$\sqrt{6}$. In these coordinates b=[b,0,0], $\sigma_{12} = (\sqrt{6}/6)\sigma_{11}$, and the dislocation sense vector $\xi$ is parallel to k'.

The force on the dislocation is then the product of the Peach-Koehler force per unit length, $\sigma_{12}b$, and the segment length h'=($\sqrt{6}$/2)h,

$$F_{PK} = c\varepsilon bh/4. \qquad (4.24)$$

where $c = 2\mu(1+\upsilon)/(1-\upsilon)$ for the isotropic case and $c = c_{11} + c_{12} - 2(c_{12}^2/c_{11})$.

For the configuration of Figure 4-8, the line tension force on the movable segment D is given by

$$F_T = 2(K/4)\ln(h'\alpha/b) \qquad (4.25)$$

where (K/4 ) is the energy prefactor and $\alpha$ is a core cut-off parameter. The factor 2 appears because there are two fixed segments E giving a force acting on the movable segment D. This expression differs from the Matthews' work[69,70,71] in the use of h' as the outer cut-

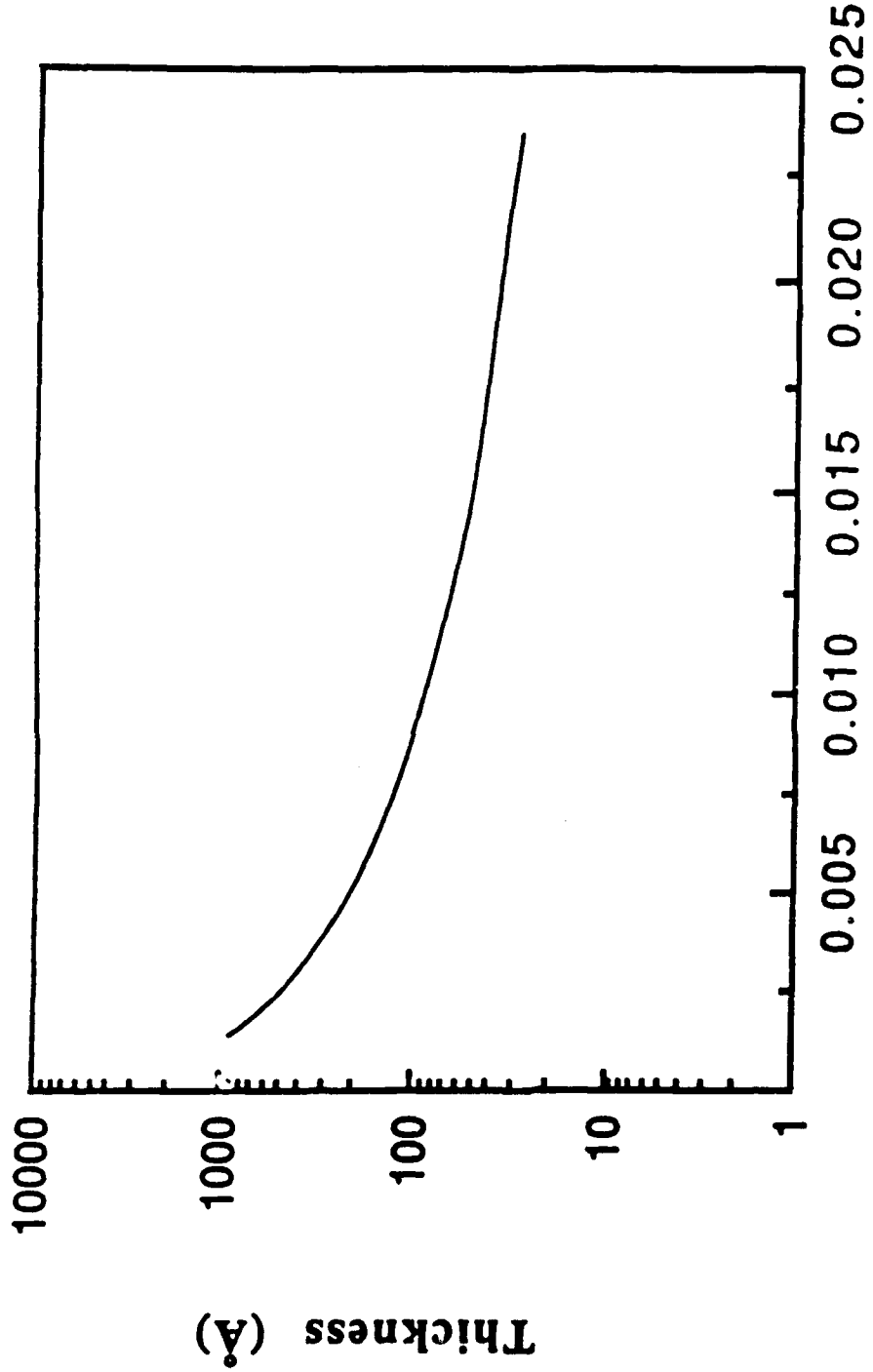



Fig. 4-7 Plot of the calculated minimum critical thickness vs.mismatch (f) from Matthews and Blakeslee's model.

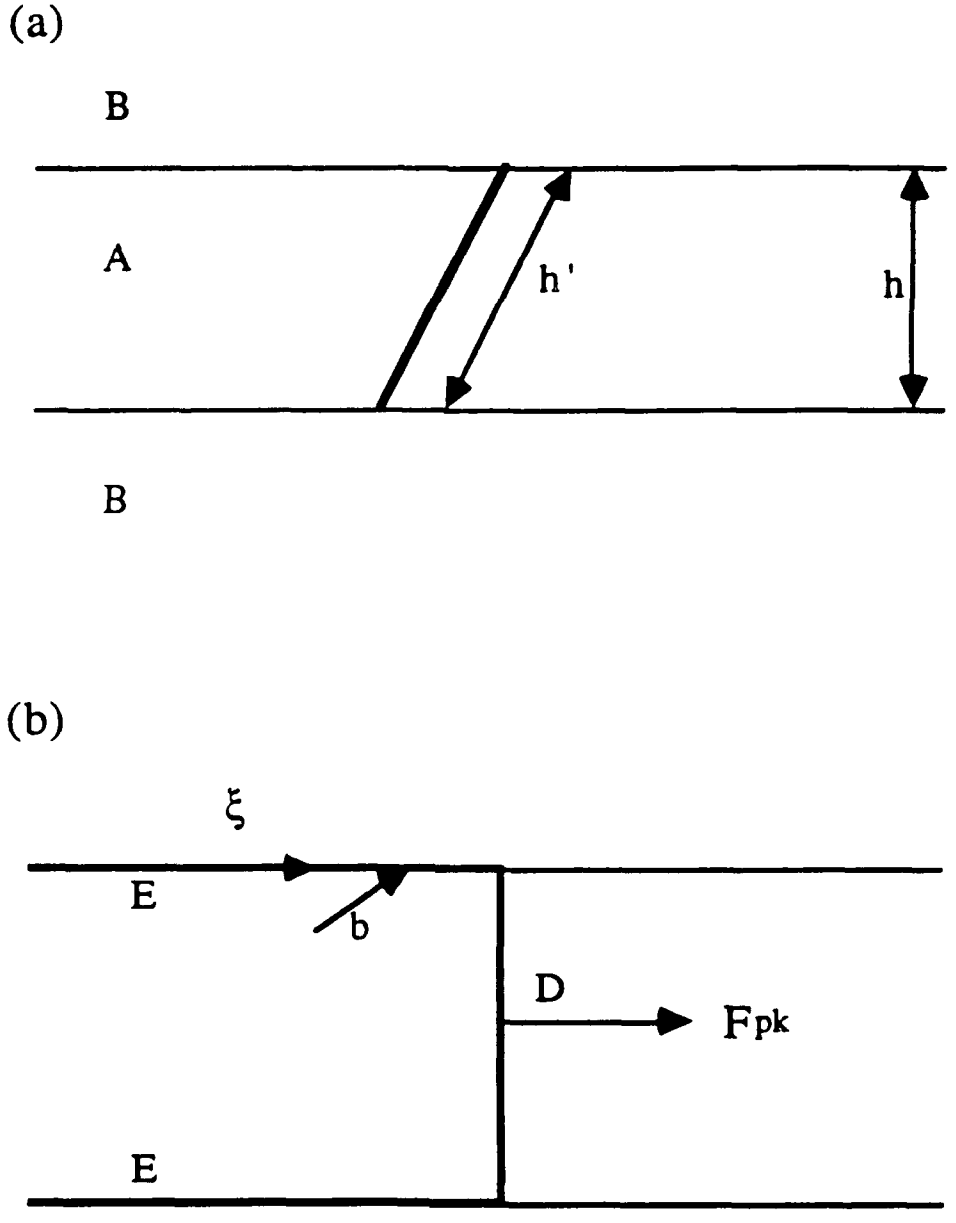



Fig. 4-8. View of dislocation configuration, (a) parallel to glide plane and interfaces of an A layer, (b) perpendicular to b and ξ.

off for the dislocation. With the value $h'=(\sqrt{6}/2)h$ and using $\alpha=3$, typical for convalent bound solids, Equation (4-25) becomes

$$F_T=(K/2\ )[\ln(h/b)+1.30] \tag{4.26}$$

In the isotropic case,

$$K=[\mu b^2/(1-\upsilon)](1-\cos^2 ß) \tag{4.27}$$

where ß is the angle between the Burgers vector and the sense vector. For {100} layers, ß=60°.

In the anisotropic case, explicit solutions for K are available but different coordinate transformations are needed in order to use them. For the screw portion of segments E with Burgers vector $b_S=a/4[110]$ the coordinate set is $i'=[112]/\sqrt{6}$, $j'=[111]/\sqrt{3}$, $k'=[110]/\sqrt{2}$. In this set, the screw energy factor is

$$K_s=(c_{44}' +c_{55}' - c_{16}'^2)^{1/2} \tag{4.28}$$

with $c_{44}'=c_{44}-H/3$, $c_{55}'=c_{44}-H/6$, $c_{16}'=\sqrt{2}H/6$, and $H=2c_{44} + c_{12} - c_{11}$. For edge component, the appropriate coordinate set is $i'=[001]$, $j'=[110]/\sqrt{2}$, and $k'=[110]/\sqrt{2}$. The edge component of the Burgers vector has two corresponding energy factors given by

$$K_{e1}= (c_{11}' + c_{12}' )\{[c_{55}'(c_{11}'-c_{12}')]/[c22'(c_{11}'+c_{12}'+c_{55}')]\}^{1/2} \tag{4.29}$$

and

$$K_{e2}= (c_{22}'/c_{11}')^{1/2}K_{e1} \tag{4.30}$$

with $c_{11}'=c_{11}$, $c_{22}'=c_{11} + H/2$, $c_{11}'= (c_{11}'c_{22}')^{1/2}$, $c_{12}'= c_{12}$, $c_{55}'= c_{44}$.

The total energy factor is

$$K=(K_s b_s^2 + K_{e1}b_{e1}^2 + K_{e2}B_{e2}^2\ )/b^2 \tag{4.31}$$

The critical value $h_c$, that above which dislocation spreading is favored, is determined by equating (4.24) and (4.25). The minimum critical thickness-misfit relation arising from Hirth's anisotropy calculation is shown in Fig 4-9.

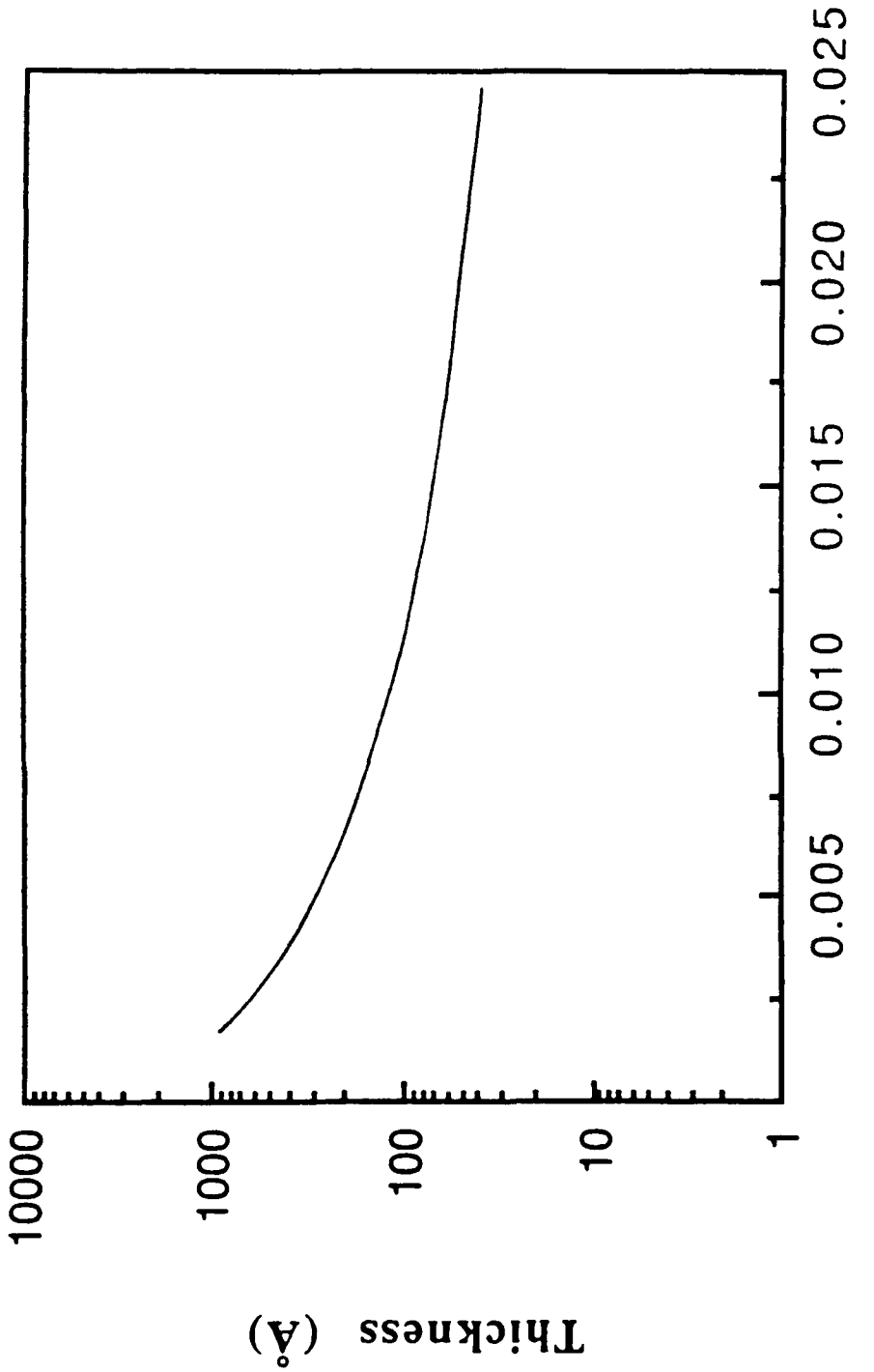



Fig 4-9 Plot of the calculated minimum critical thickness vs.mismatch (f) from Hirth's model.

4.3.3. Energy Equilibrium Model

Our derivation of minimum critical thickness is based on the energy balance consideration. Therefore, this approach differs from the previous models, in which mechanical equilibrium of a grown-in threading dislocations determines the onset of interfacial misfit dislocations. Instead, we compare the system energy for threading dislocations with or without a length of misfit dislocation segment in growing film of the same thickness. The threading dislocation configurations are shown in Fig.4-10 (a) and (b). The energy terms considered in this calculation are : (1) the film strain energy, (2) the dislocation self energy, and (3) the interaction energy between the dislocation segments.

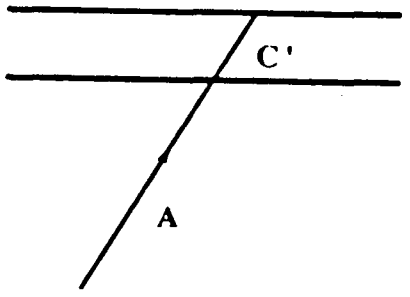
The difference in the strain energy ($\Delta E_\varepsilon$) between the two configuration in Fig. 4-10(a) and Fig. 4-10(b) is the negative of the proportion of strain energy that is relaxed due to the formation of a length "L" of misfit dislocation. The areal strain energy density[72, 73, 74, 76, 77] associated with a film of thickness "h" is given by

$$E_\varepsilon = [\frac{2\mu(1+\upsilon)}{1-\upsilon}]\varepsilon^2 h \qquad (4.32)$$

where, $\mu$ is the shear modulus of the thin film, $\upsilon$ is the Poission's ratio, h is the thickness of the film, and $\varepsilon$ is the elastic strain parallel to the film plane.

The area which the misfit strain has been accommodated by the formation of a length "L" of misfit dislocation is approximately equal to the product of the range affected by dislocation and the length of misfit dislocation. The convenient calculation for the range affected by misfit dislocation are as follows. If the misfit (f) between the strained layer and substrate is fully relaxed by the formation of a grid of misfit dislocations, then the spacing between misfit dislocations is

$$D = \frac{b_e}{f} \qquad (4.33)$$

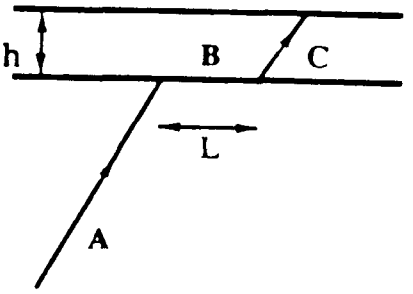



$\xi_A = \frac{1}{2}[011]$

$\xi_C = \frac{1}{2}[011]$

$b = \frac{a}{2}[10\bar{1}]$

(a)




$\xi_A = \frac{1}{2}[011]$

$\xi_B = \frac{1}{2}[-110]$ $\quad b = \frac{a}{2}[101]$

$\xi_C = \frac{1}{2}[011]$

(b)

Fig. 4-10 View of dislocation configuration parallel to glide plane interfaces of a strained layer of thichness "h", (a) without a misfit dislocation segment (b) with a misfit dislocation segment.

where $b_e$ is the edge component of Burgers vector on the film plane for the misfit dislocation. The total misfit dislocation length per unit area is equal to

$$\Sigma L_i = 2\frac{f}{b_e} \tag{4.34}$$

Then the range affected by misfit dislocation is equal to the affected area per unit length of misfit dislocation, resulting in

$$\frac{1}{\Sigma L_i} = \frac{b_e}{2f} \tag{4.35}$$

Thus, the area which the misfit strain has been accommodated by the formation of a length "L" of misfit dislocation is therefore

$$A = \left(\frac{b_e}{2f}\right) L \tag{4.36}$$

The difference in the strain energy ($\Delta E_\varepsilon$) that accompanies the movement from the configuration shown in Fig. 4-10(a) to that in Fig.4-10(b) is composed from the negative of the product of Eq. (4.32) and Eq. (4.33), resulting in

$$\Delta E_\varepsilon = -\frac{\mu(1+\upsilon)b_e L}{(1-\upsilon)f}\varepsilon^2 h \tag{4.37}$$

The change in the self-energy of the dislocation associated with the configurations as shown in Fig.4-10(a) and Fig.4-10(b), ($\Delta E_D$), is equal to the self energy of a length "L" of misfit dislocation which is given approximately by[64]

$$\Delta E_D \cong \frac{\mu b^2 L}{4\pi(1-\upsilon)}(1-\upsilon\cos^2\beta)\ln\left(\frac{\alpha R}{b}\right) \tag{4.38}$$

where $\beta$ is the angle between the dislocation line and its Burgers vector. The most appropriate value for R is difficult to determine. As long as the misfit dislocation density is

low, the screening distance R is equal to film thickness as h. If the dislocation density increases, R is limited by the strain field of neighboring dislocations. However, for the single dislocation case that we consider at here, the value of R is approximately equal to the film thickness "h". The core parameter $\alpha$ is taken equal to $\alpha$=4 for most semiconductors.

The interaction energy difference ($\Delta E_I$) between two configurations (Fig. 4-10(a) and (b) is given as

$$\Delta E_I = E_I(A,B) + E_I(B,C) + E_I(A,C) - E_I(A,C') \tag{4.39}$$

This interaction energy between dislocations has been derived by Hirth[78]. The interaction energy between the two intersecting dislocations in the coplanar case, such as $E_I(A,B)$ and $E_I(B,C)$, is written in the form

$$W_{12} = \frac{\mu}{4\pi}\{(b_1\cdot\xi_1)(b_2\cdot\xi_2) - 2[(b_1\times b_2)\cdot(\xi_1\times\xi_2)] + \frac{1}{1-\upsilon}[b_1\cdot(\xi_1\times e_3)][b_2\cdot(\xi_2\times e_3)]\} I(x_\alpha, y_\beta) \tag{4.40}$$

Here

$$I(x,y) = x\ln\left(\frac{R - y - x\cos\theta}{x}\right) + y\ln\left(\frac{R - x - y\cos\theta}{y}\right),$$

$$I(x_\alpha, y_\beta) = I(x_2,y_2) - I(x_1,y_2) - I(x_2,y_1) + I(x_1,y_1),$$

$$R = (x^2 + y^2 - 2xy\cos\theta)^{1/2},$$

$$e_3 = \frac{\xi_1\times\xi_2}{|\xi_1\times\xi_2|},$$

and $\theta$ is the angle between the two intersecting dislocations.

For two parallel dislocations segment, such as A an C in Fig. 4-10(b), the interaction is

$$W_{12} = \left(\frac{\mu}{4\pi}(b_1\cdot\xi_1)(b_2\cdot\xi_2) - \frac{\mu}{4\pi(1-\upsilon)}\{(b_1\cdot e_3)(b_2\cdot e_3) + [(b_1\times\xi_1)\cdot e_3)][e_3\cdot(b_2\times\xi_2)]\}\right) I(x_\alpha, y_\beta) \tag{4.41}$$

where now

$$I(x, y) = R - \frac{1}{2}(y - x)\ln(R + y - x) + \frac{1}{2}(x - y)\ln(R + x - y)$$

$$R = [(x - y)^2 + \eta^2]^{1/2}$$

$\eta$ = the separation between the two parallel dislocations.

However, when the separation between two parallel dislocations is close to zero, such as dislocation A and C' in Fig. 4-10(b), equation (4.41) is not appropriate for calculating interaction energy. Instead, the interaction energy between the dislocations is determined from

$$W_{12} = \frac{\mu b^2 (1 - \upsilon \cos^2\beta)}{4\pi(1 - \upsilon)} \int_0^{L_1} dl_1 \int_0^{L_2} \frac{dl_2}{dl_1 + dl_2}$$

$$= \frac{\mu b^2 (1 - \upsilon \cos^2\beta)}{4\pi(1 - \upsilon)} \left[ L_1 \ln\left(\frac{L_1 + L_2}{L_1}\right) + L_2 \ln\left(\frac{L_1 + L_2}{L_2}\right) \right] \qquad (4.42)$$

where $L_1$ and $L_2$ are the length of dislocatin segment, $\beta$ is the angle between the dislocation line and its Burger vector.

By using equation (4.40), we find

$$E_I(A,B) = \frac{\mu a_1^2}{32\pi}\left[\frac{2 + \upsilon}{1 - \upsilon}\right] I(x_\alpha, y_\beta)$$

$$I(x_\alpha, y_\beta) = M \ln\left\{\left(\frac{3}{2}\right)\left(\frac{[M^2 + L^2 + ML]^{1/2} + L + M/2}{M}\right)\right\}$$

$$+ L \ln\left\{\left(\frac{3}{2}\right)\left(\frac{[M^2 + L^2 + ML]^{1/2} + M + L/2}{L}\right)\right\} \qquad (4.43)$$

$$E_I(B,C) = \frac{\mu a_1 a_2}{32\pi}\left[\frac{2 + \upsilon}{1 - \upsilon}\right] I(x_\alpha, y_\beta)$$

$$I'(x_\alpha,y_\beta)=\frac{h}{\sqrt{2}}\ln\{(\frac{3}{2})(\frac{[\frac{h}{2}^2+L^2+\frac{hL}{\sqrt{2}}]^{1/2}+L+\frac{h}{\sqrt{2}}}{\frac{h}{\sqrt{2}}})\}$$

$$+L\ln\{(\frac{3}{2})(\frac{[\frac{h}{2}^2+L^2+\frac{hL}{\sqrt{2}}]^{1/2}+\sqrt{2}\,h+\frac{L}{2}}{L})\} \qquad (4.44)$$

where M and h are the thicknesses of substrate and strained-layer, $a_1$ and $a_2$ are the lattice parameters of substrate and strained-layer.

By using Equation (4.41), $E_I(A,C)$ is given as

$$E_I(A,C)=\frac{\mu a_1 a_2}{8\pi}[\frac{1-\upsilon/4}{1-\upsilon}]I''(x_\alpha,y_\beta)$$

$$I''(x_\alpha,y_\beta)=I''(x_2,y_2)-I''(x_1,y_2)-I''(x_2,y_1)+I''(x_1,y_1)$$

$$I''(x_1,y_1)=[M^2+L^2+ML]^{1/2}-\frac{1}{2}(M+\frac{L}{2})\ln\{[M^2+L^2+ML]^{1/2}+M+L/2\}$$

$$+\frac{1}{2}(M+\frac{L}{2})\ln\{[M^2+L^2+ML]^{1/2}-M-L/2\}$$

$$I''(x_1,y_2)=[(M+\frac{h}{\sqrt{2}}+\frac{L}{2})+\frac{3L^2}{4}]^{1/2}-\frac{1}{2}(M+\frac{L}{2}+\frac{h}{\sqrt{2}})\ln\{[(M+\frac{h}{\sqrt{2}}+\frac{L}{2})+\frac{3L^2}{4}]^{1/2}$$

$$+M+\frac{h}{\sqrt{2}}+\frac{L}{2}\}+\frac{1}{2}(M+\frac{h}{\sqrt{2}}+\frac{L}{2})\ln\{[(M+\frac{h}{\sqrt{2}}+\frac{L}{2})+\frac{3L^2}{4}]^{1/2}-M-\frac{L}{2}-\frac{h}{\sqrt{2}}\}$$

$$I''(x_2,y_2)=[\frac{h}{2}^2+L^2+\frac{hL}{\sqrt{2}}]^{1/2}-\frac{1}{2}(\frac{h}{\sqrt{2}}+\frac{L}{2})\ln\{[\frac{h}{2}^2+L^2+\frac{hL}{\sqrt{2}}]^{1/2}+\frac{h}{\sqrt{2}}+\frac{L}{2}\}$$

$$+\frac{1}{2}(\frac{h}{\sqrt{2}}+\frac{L}{2})\ln\{[\frac{h}{2}^2+L^2+\frac{hL}{\sqrt{2}}]^{1/2}-\frac{h}{\sqrt{2}}-\frac{L}{2}\}$$

$$I''(x_1,y_1)=L-\frac{L}{2}\ln(3) \qquad (4.45)$$

By using equation (4.42), $E_I(A,C')$ is given as

$$E_I(A,C')=\frac{\mu a_1 a_2}{8\pi}[\frac{1-\upsilon/4}{1-\upsilon}]I'''(x_\alpha,y_\beta)$$

$$i'''(x_\alpha, y_\beta) = M \ln\left(\frac{M + \frac{h}{\sqrt{2}}}{\frac{h}{\sqrt{2}}}\right) + L \ln\left(\frac{M + \frac{h}{\sqrt{2}}}{\frac{h}{\sqrt{2}}}\right) \tag{4.46}$$

The difference in system energy $\Delta E$ that accompanies the movement from configuration shown in Fig. 4-10(a) to that in Fig. 4-10(b) is the sum of the change of strain energy $\Delta E_\varepsilon$, self energy of dislocation $\Delta E_D$, and the interaction energy $\Delta E_I$

$$\Delta E = \Delta E_\varepsilon + \Delta E_D + \Delta E_I \tag{4.47}$$

For a given degree of misfit (f=0.0135) between the strained layer and the substrate, the change of total energy ($\Delta E$) with the length of misfit dislocation (L) is as shown in Fig. 4-11. For a thinner strained layer (h=50Å, curve a), the strain energy relaxed ($\Delta E_\varepsilon$) is not enough to compensate the increment of the sum of self energy and dislocation interaction energies, the change of total energy ($\Delta E$) continuously increase with the increase of the length of misfit dislocation, so that the misfit dislocation segment can never be stablized at this thickness. However for thicker layer (curce b, c, and d), beyond a finite length (L*) of misfit dislocation segment the change of total energy term ($\Delta E$) pass the maximum point ($\Delta E^*$) and decreases with increasing of the length of misfit dislocation. Moreover, the values of $\Delta E^*$ and L* are decreased as the thickness of thin film is increased. We note that when L is less than a critical value L*, the sum of the change of self energy and interaction energy term dominates and $\Delta E$ increase with L, while for L>L*, the change of strain energy term dominates and $\Delta E$ decreases with increasing L. This means that there is an energy barrier for the threading dislocation to glide along the strained layer interface. The length of misfit dislocation must be longer than a critical length (L>L*) before it can continue to glide along the interface with a decrease in system energy. Any threading dislocation with misfit dislocation segment L>L* become energetically favorable to glide along the strained layer interface and move to the sample edge. Moreover, when

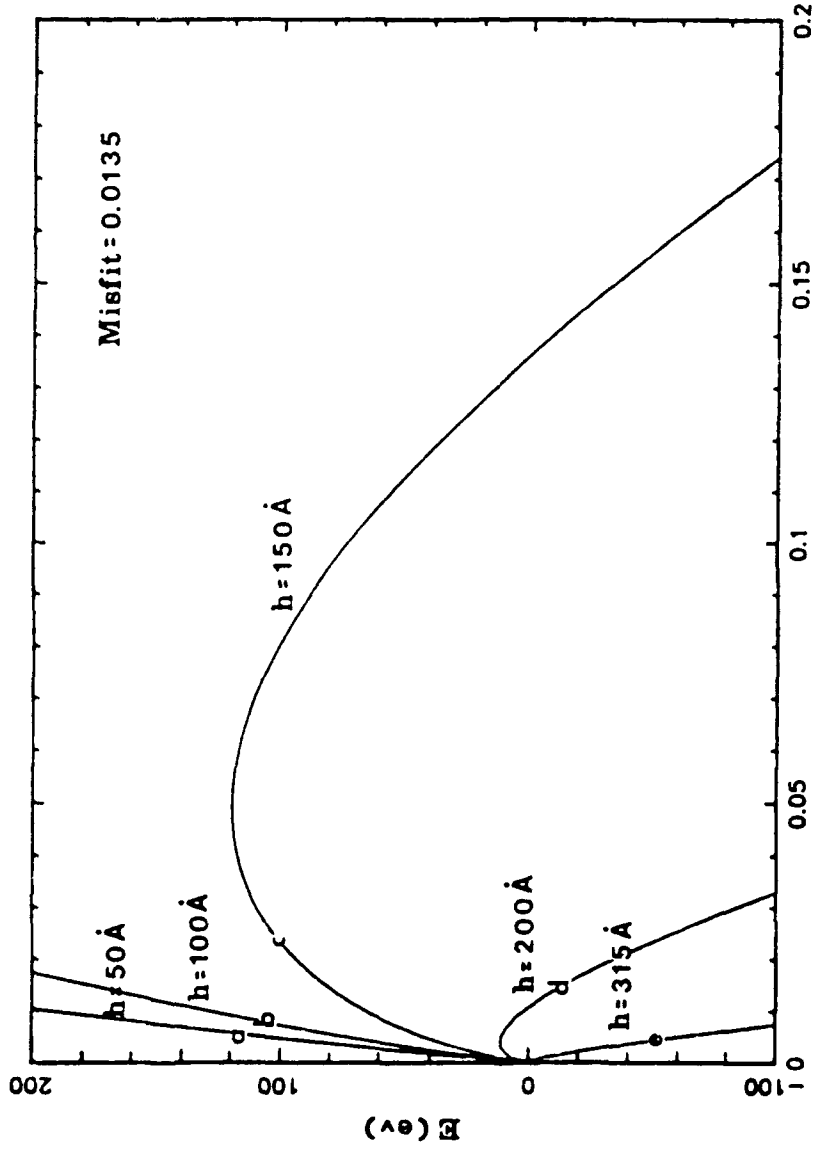



Fig. 4-11 The change of total energy (ΔE) with the length of misfit dislocation (L) for a given misfit (f=0.0135) with different layer thickness.

the thickness of strained-layer reaches 315 Å, there is no energy barrier, it is energetically favorable for a threading dislocation to spontaneously bend along the strained-layer interfaces.

Fig. 4-12 illustrates that increasing the misfit (f) between the strained layer and the substrate also increases the importance of the change in the strain energy term and leads to the decrease of the critical misfit dislocation length (L*) and the energy barrier ($\Delta E^*$). For a given degree of misfit (f), we defined the minimum critical thickness as the thickness at which the critical misfit dislocation length (L*) and the energy barrier ($\Delta E^*$) are equal to zero. Fig. 4-13 illustrates the minimum critical thickness -misfit relation.

For a given degree misfit strained-layer with layer thickness less than the minimum critical thickness that we predicted in Fig. 4-13. There is an energy barrier for the formation of a critical length of misfit dislocation and the energy barrier can be decreased by raising either the film thickness (h) or the misfit (f). However, we must somehow provide energy to the system in order to form a stable misfit dislocation segment. This energy can be provided in the form of thermal energy. The number of threading dislocations with a misfit dislocation segment longer than L* which exists in equilibrium at a given temperature will be given by the exponential relation

$$n = A \exp(-\Delta E^*/kT) \tag{4.48}$$

This equation reflects the thermally activated nature of the threading dislocations bent-over process. Moreover, the effectiveness of strained-layer in blocking threading dislocations can be improved by temperature increasing.

It is clear from previous discussion that the number of bent-over threading dislocation in a given seystem depends sensitivily on the total energy change ($\Delta E$) associated with the introduction of misfit dislocation. Generally speaking, $\Delta E$ is determined in part by the thickness of strained layer (h) and the misfit between the strained

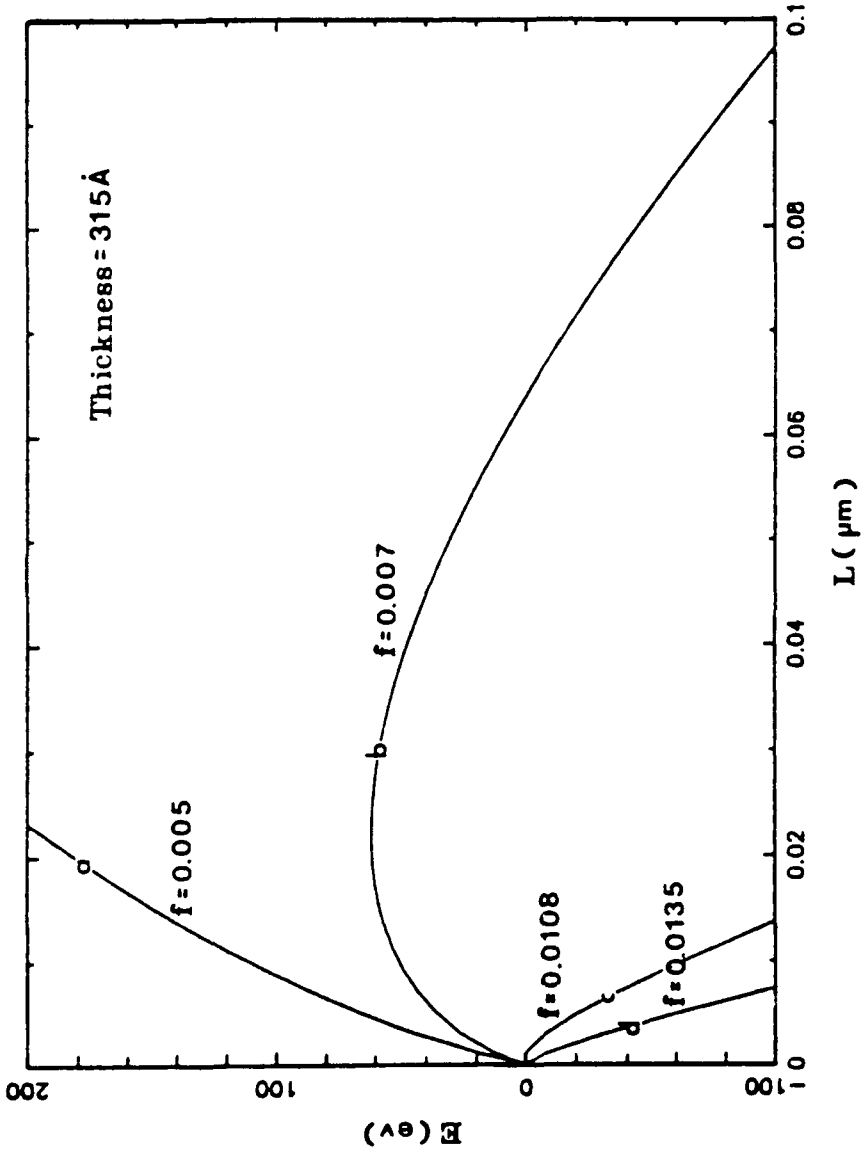



Fig. 4-12 The change of total energy (ΔE) with the length of misfit dislocation (L) for a given thickness (h=315 Å) with different misfit (f).

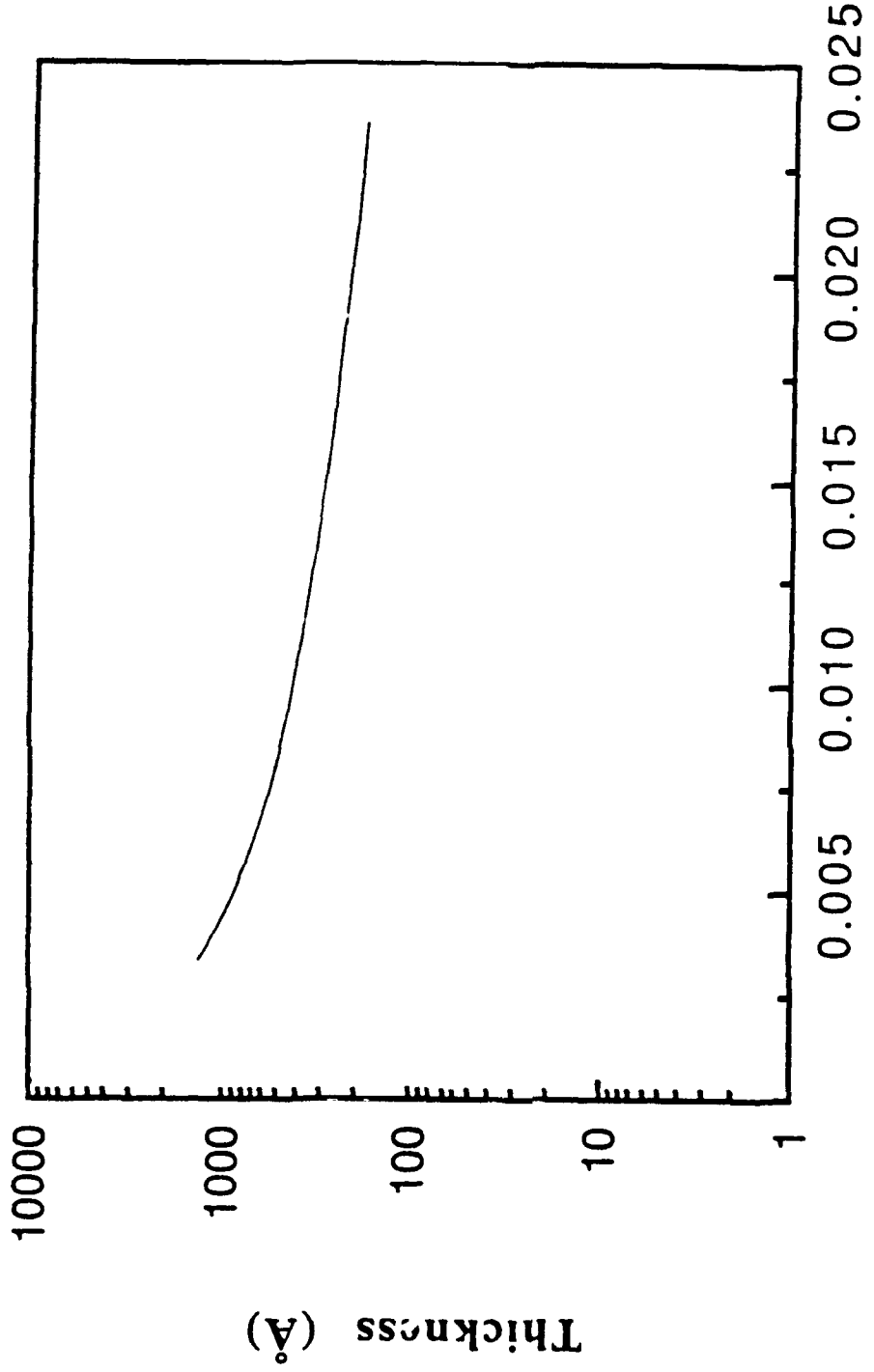



Fig. 4-13 Plot of the calculated minimum critical thickness vs.mismatch (f) from our energy equilibrium model.

layer and substrate. On the other hand, if there is a large misfit and/or thicker strained layer the $\Delta E$ can be expected to be small.

Fig. 4-14 displays the comparison of the minimum critical thickness-misfit relation from our energy model, Matthews an Blakeslee's mechanical equilibrium model and Hirth's anisotropy approach. However, our model gives a higher minimum critical thickness than Matthew's and Hirth's model does. It may be worthwhile to emphasize the simplifications that could attribute to the deviation of our prediction from realistic minimum critical thickness. These simplifications are :

(1) The area which the misfit strain has been accommodated by the formation of the misfit dislocation segment is only an approximate value. This area could be affected by the interface inperfection and the neighboring defects.

(2) Equation (4.32) is a good approximation for calculating areal strain energy density in general case. However, the elastic anisotropic should be involved in the calculation for more accurate prediction.

(3) The image force which is in the vicinity of the free surface will affect the interaction energies between dislocations. However, the image problem is a formidable one which has not yet been solved.

(4) When the dislocation length or spacing between two dislocations is close to the value of Burgers vector, the end effect will introduce error in interaction energy calculation. However, there is not proper correction to make up this error.

(5) The simplification of dislocation self energy (equation 4.38) where R is equal to the film thickness and R=4 are not appropriate when the grown-in dislocations density are high or different strained-layer system are involved.

(6) Since the thermally activated nature of the threading dislocation bent-over proces, the environmental temperature should be an important factor in determining the minimum critical thickness.

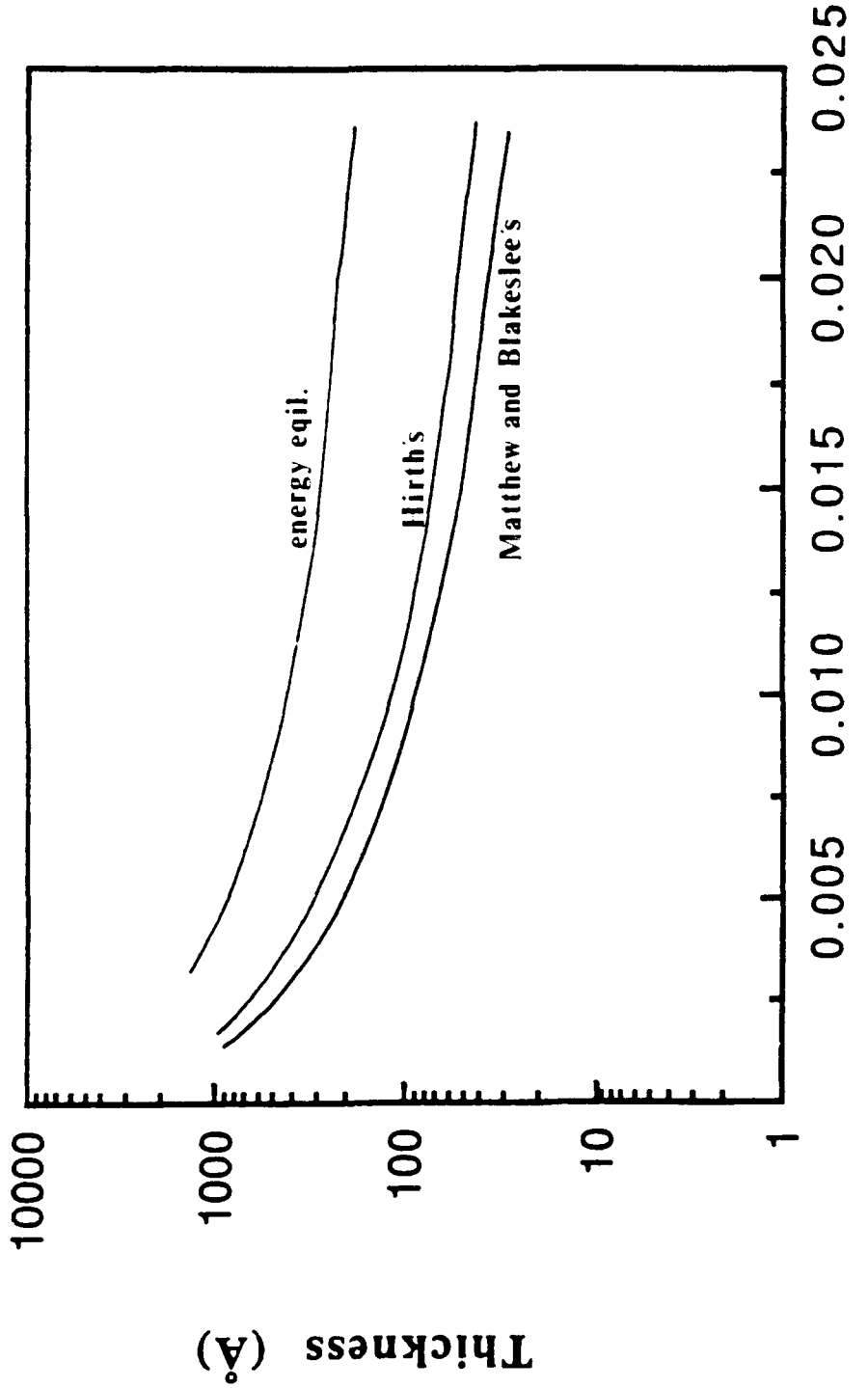



Fig. 4-14 Plots of the calculated minimum critical thickness vs. mismatch (f) from Matthews and Blakeslee's model, Hirth's elastic anisotropic model, and our energy equilibrium model.

## 4.4 The number of dislocations that can be removed by glide

The number of threading dislocations that can be removed by misfit strain depends on a small extent on the orientation of the interface and on interface shape. In the simple and approximate calculation made below these dependences are neglected. By assuming that the interface is (001) and that it is a square of side L. The edges of the square are assumed to be parallel to the <110> directions in (001). The Burgers vector of the threading dislocation are assumed to be of type a/2<110> and to be inclined at 45° to (001). These threading dislocations move by glide on {111} planes and, when they do so, they generate misfit dislocations with lines parallel to the <110> directions in (001).

If all threading dislocations glide to the specimen edge then the average length of misfit dislocation lines is L/2. If the number of threading dislocations per unit area is $\rho$ then the length of misfit dislocation line per unit area is

$$\rho L/2 \tag{4.49}$$

As half of the misfit dislocations lie along one <110> direction in the interface and half lie along the other, the average separation of parallel misfit dislocations is

$$4/\rho L \tag{4.50}$$

If the misfit accommodated by dislocation is $\delta$ then the average separation of parallel misfit dislocations is also equal to

$$(b_e \cos\lambda)/\delta \tag{4.51}$$

$\cos\lambda=1/2$ for specimens with the geometry considered above. Thus the density of threading dislocations removed by glide is

$$\rho=8\delta/b_e L \tag{4.52}$$

The upper limit to the density of threading dislocations that can be removed is obtained by setting $\delta$ equal to the misfit f. This upper limit is therefore

$$\rho_{max.}=8\delta/b_eL \tag{4.53}$$

## 4.5. SUMMARY

In clusion, the maximum critical thickness of strained-layer superlattice was considered as function of the number the bent-over threading dislocations. The thermally activated nature of the minimum critical thickness of strained-layer in blockin threading dislocations was predicted by our energy equilibrium model. However, solution of better theoretical prediction of minimum and maximum critical thickness are necessary for fully exploring the effectiveness of strained-layer superlattices in reducing dislocation.

# 5. THE EFFECTIVENESS OF STRAINED-LAYER SUPERLATTICES

## 5.1. Introduction

The use of strained-layer superlattice for semicondutor materials has been utilized extensively in recent years. Matthews and Blakeslee[69, 70, 71] first proposed the use of $GaAs_{1-y}P_y$-GaAs strained-layer superlattice as a dislocations reduction buffer for the GaAs/GaAs. Fisher et al[12] repoted that by a transmission electron microscope (TEM), the dislocation density of GaAs/Si is reduced by $In_xGa_{1-x}As$-GaAs SLSs'. However, it is evident that these ternary-binary SLS system cannot be grown lattice matched to the GaAs substrate. Moreover, these SLS structures, which as a whole have a lattice constant that corresponds to the ternary material with composition of x/2 (or y/2), have several inherent shortcomings. In particular, the total thickness of the SLS must be less than the critical thickness hc, max., in order to circumvent the generation of misfit dislocations at the GaAs epilayer interface. Consequently, this will limit the number of periods and, therefore, the number of strained interfaces that are available to suppress the propagation of the threading dislocations. It follows, therefore, that in order to alleviate these problems in the ternary-binary SLS system, we require a superlattice composed of two materials having equal, but opposite, matches, such that the average lattice constant matches that of the GaAs substrate. An exceptional material candidate is an $In_xGa_{1-x}As$-$GaAs_{1-y}P_y$ (y=2x) SLS which can be grown lattice matched to GaAs. A further advantage of utilizing this particular SLS structure is that high values of strain ( $\varepsilon$=f instead of 1/2f for ternary-binary structure) can be accommodated without the SLS generating dislocations of its own. Other potential material system are GaAsP-GaAsSb, GaAsP-InGaAsSb[82], and $GaAs_{0.52+x}In_{0.48-x}P$-

$Ga_{0.52-x}In_{0.48-x}P$. Moreover we have previously reported that the ternary-ternary SLS buffer was very effective in blocking dislocations originating at the GaAs substrate. Indeed, it was apparent that a very low density of threading dislocations in GaAs epilayer was achieved. The schematic diagrams of the binary-ternary and ternary-ternary strained superlattice are shown in Fig.5-1. In addition, table 5-1 summarized the character different between binary-ternary and ternary-ternary strained-layer superlattice system.

## 5.2. Where to insert the SLS buffer

The observed dislocation density at the GaAs interface is the order of $10^{12}$ $cm^{-2}$. Further increase in the thickness of the GaAs film has resulted in some reduction in dislocation density. When the GaAs film is increased to 2-3 μm, dislocation density in the range of $10^8$ $cm^{-2}$ have been identified in previous chapter. Further increases in thickness of GaAs film has not resulted in any further reduction in the dislocation density. GaAs film thicker than 4 μm can cause substrate bending and GaAs epilayer cracking due to the built up of stresses. We believe that inserting the SLS should be several stages at a GaAs film thickness of 2-3 μm away from the GaAs/Si interface. At this GaAs film thickness the efficiency of the SLS in filtering dislocation density of $10^8$ $cm^{-2}$ will be higher than density of $10^{12}$ $cm^{-2}$ at the GaAs interface. It is apparent as shown in Fig. 5-2, that inserting the SLS at a GaAs thickness of only 1 μm away from GaAs/Si interface, the efficiency of SLS is drastically limited due to the existence of high density of threading dislocations. However, for GaAs buffer layer thickness greater than 2 μm the efficiency is improved, this is clearly shown in Fig. 5-3.

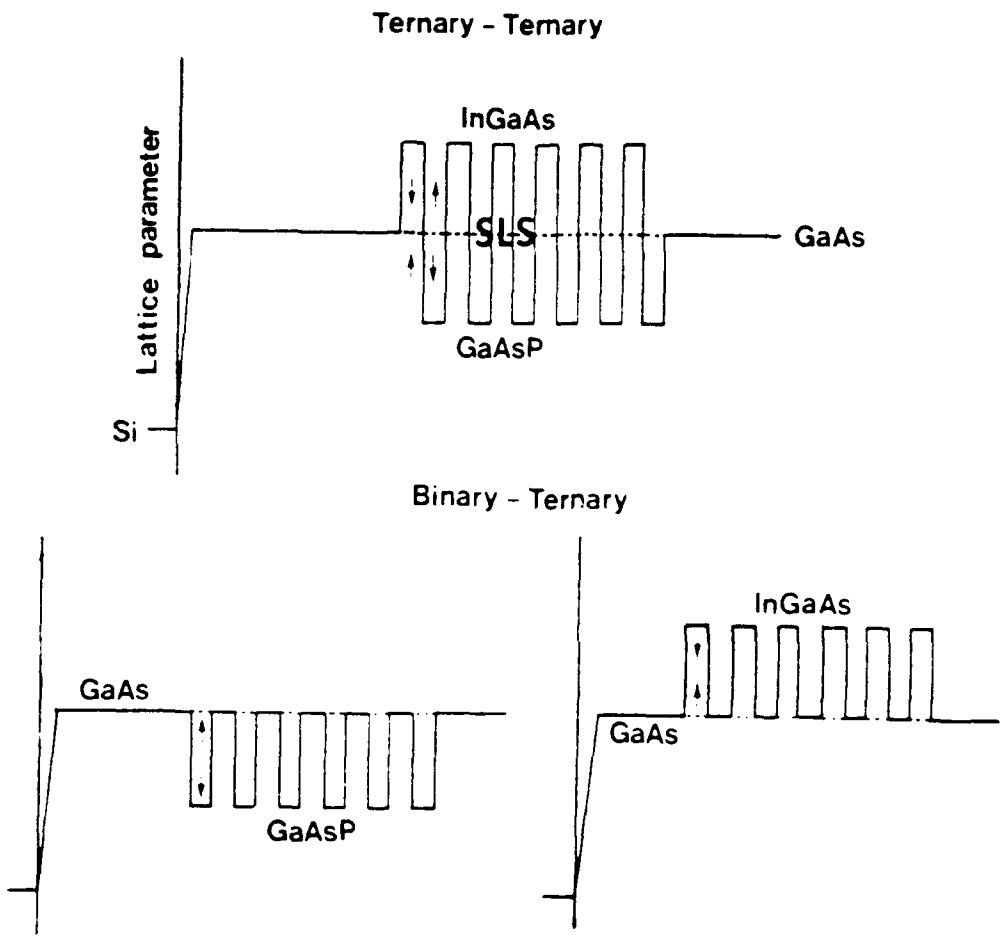



Fig. 5-1 Schematic diagram of strained-layer superlattices structure.

## STRAINED LAYER SUPERLATTICES

| SLS | Candidate | Strain | Character |
|---|---|---|---|
| Binary-Ternary | GaAs-GaAsP<br>InGaAs-GaAs | $\epsilon = \frac{1}{2} f$ | limit total & individual thickness |
| Ternary-Ternary | $In_xGa_{1-x}AS$-<br>$GaAs_{1-y}P_y$<br>$(y=2x)$ | $\epsilon = f$ | unlimited total thickness<br>limited individual thickness |

Table 5-1 The character different between binary-ternary and ternary-ternary strained-layer superlattices system.


Fig. 5-2 Cross-sectional TEM bright-field image illustrating the effectiveness of the InGaAs-GaAsP in bending threading dislocations of thinner (1μm) GaAs epi-layer on Si.


Fig. 5-3 Cross-sectional TEM bright-field image illustrating the effectiveness of the InGaAs-GaAsP in bending threading dislocations of thicker (2μm) GaAs epi-layer on Si.

## 5.3. Observation on the effectiveness of SLS

### 5.3.1 Experimental details

Here we investigate the effectiveness of utilizing a highly strained $In_xGa_{1-x}As$-$GaAs_{1-y}P_y$ in reducing the density of threading dislocations that propagate from the GaAs/Si interface. The GaAs on silicon samples used in this study were provided by the University of Illimois, Spire Corporation, and Kopin Corporation. Samples have also been grown in our Laboratory. The strained-layer superlattices and GaAs epitaxial layers were grown by metalorganic chemical vapor deposition (MOCVD). Several $In_xGa_{1-x}As$-$GaAs_{1-y}P_y$ SLS structure with y=2x have been investigated. The corresponding values of x and y were varied in the ranges of 8-25% and 16-40%, respectively. Individual layer thicknesses were varied from 80 to 300 Å, depending on the the ternary alloycomposition. The intrinsic strain was maintained in the 0-2% range. Transmission electron microscopy (TEM) samples for both cross-sectional and plan-view were prepared by mechanical thinning followed by ion milling.

### 5.3.2. Results and Discussion

The effectiveness of utilizing the InxGa1-xAs-GaAs1-yPy structure as buffer layer is shown in the bright-field micrograph of Fig.5-4. In this image, regions denoted by X and Y are areas of low and high dislocation densities, respectively. It is clear that the impinging dislocations on the SLS in region X are confined by the strained field and bent along the SLS interface planes. Consequently, almost all the dislocations impinging on the SLS are blocked and do not thread to the GaAs top layer. Indeed, it is evident that the SLS is most effective in confining and bending the dislocations in the absence of a perturbing strain field generated by another dislocation. However, the interaction and a merger of a high density of dislocations in region Y results in an upward threading of

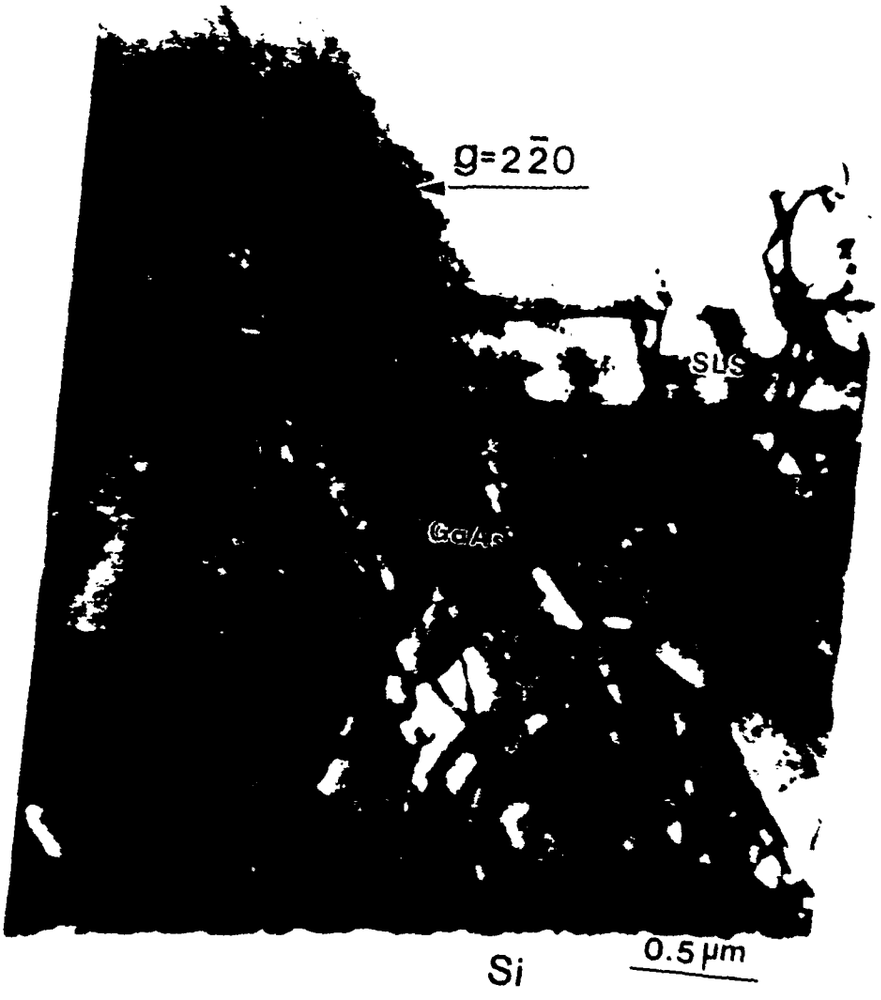



Fig. 5-4 Cross-sectional TEM bright-field image illustrating the effectiveness of the InGaAs-GaAsP strain-layer superlattices in bending threading dislocations.

dislocation into the GaAs epilayer. Moreover, the higher the dislocation density, the greater the likelihood of dislocation-dislocation interactions and, consequently, the greater the probability that some of the dislocations will thread into the GaAs epilayer. Clearly, the SLS has only a finite capacity for bending the dislocations in the intefacial planes of the SLS.

Plan-view bright-field TEM has also been performed in order to asses the effectiveness of the SLS. Figure 5-5 shows a plan-view micrograph of the as-grown GaAs/Si interface prior to the growth of the SLS. The bending and propagation of dislocations along the <110> directions within this SLS are illustrated in Fig. 5-6. Also shown is the interaction between neighboring dislocations. In a plan-view TEM of the GaAs epilayer grown on top of the SLS, two distinct dislocation density regions are discernible. In an area of approximately 100 $\mu m^2$, no threading dislocations were observed. We believed that this area corresponds to region X in Fig. 5-4, where the SLS is highly effective in bending the dislocations. In contrast, we have also identified a region where the dislocation density is fairly high as shown in Fig. 5-7. this area may be compared to region Y in Fig. 5-4 where we have observed a small fraction of dislocations threading through the SLS. An average dislocation density of ~$2x10^7$ $cm^{-2}$ has been achieved by plan-view TEM observation.

The dislocation reduction effect of InGaAs-GaAsP strained-layer superlattice grown on GaAs/Si can be clearly seen by in-depth profile of dislocation density. The position of SLS's is shown in Fig. 5-8 by "SL". A Step-like reduction of dislocation density is observed at the superlattice. This is due to the termination of dislocation by formation of loops at SLS's. After passing through the superlattice position, the dislocation density density reduces continuously with the thickness without saturation[84].

In Fig. 5-9 the experimental data for the layer thicknesses of InxGa1-xAs-GaAs1-yPy strained-layer superlattices grown on GaAs epitaxial layer on Si has shown


Fig. 5-5 Plan-view transmission electron micrograph of as-grown GaAs on Si sample.

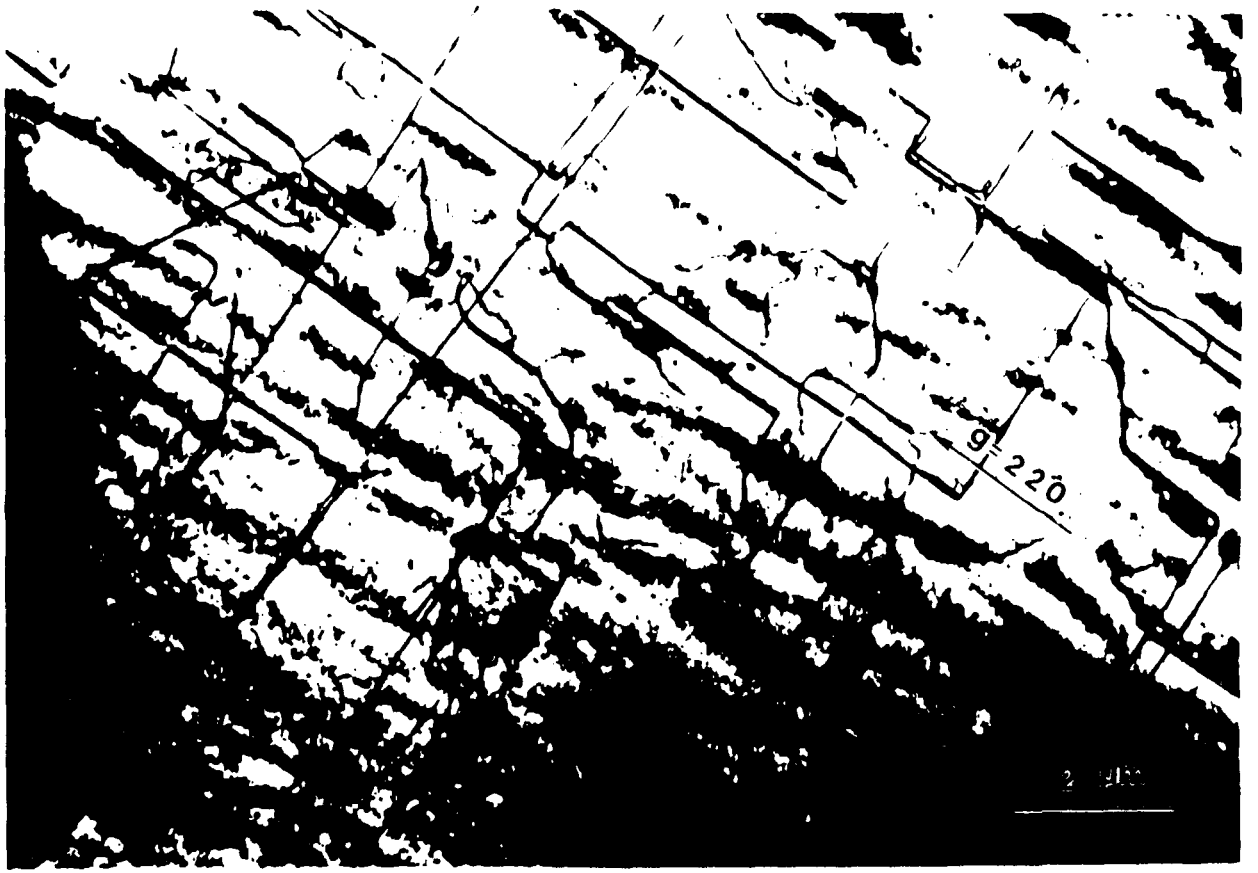



Fig. 5-6 Plan-view transmission electron micrograph illustrating the bending and propagation of dislocations along the <110> directions within the InGaAs-GaAsP SLS.


Fig. 5-7 Plan-view transmission electron micrograph of epitaxial GaAs grown on top of the SLS.

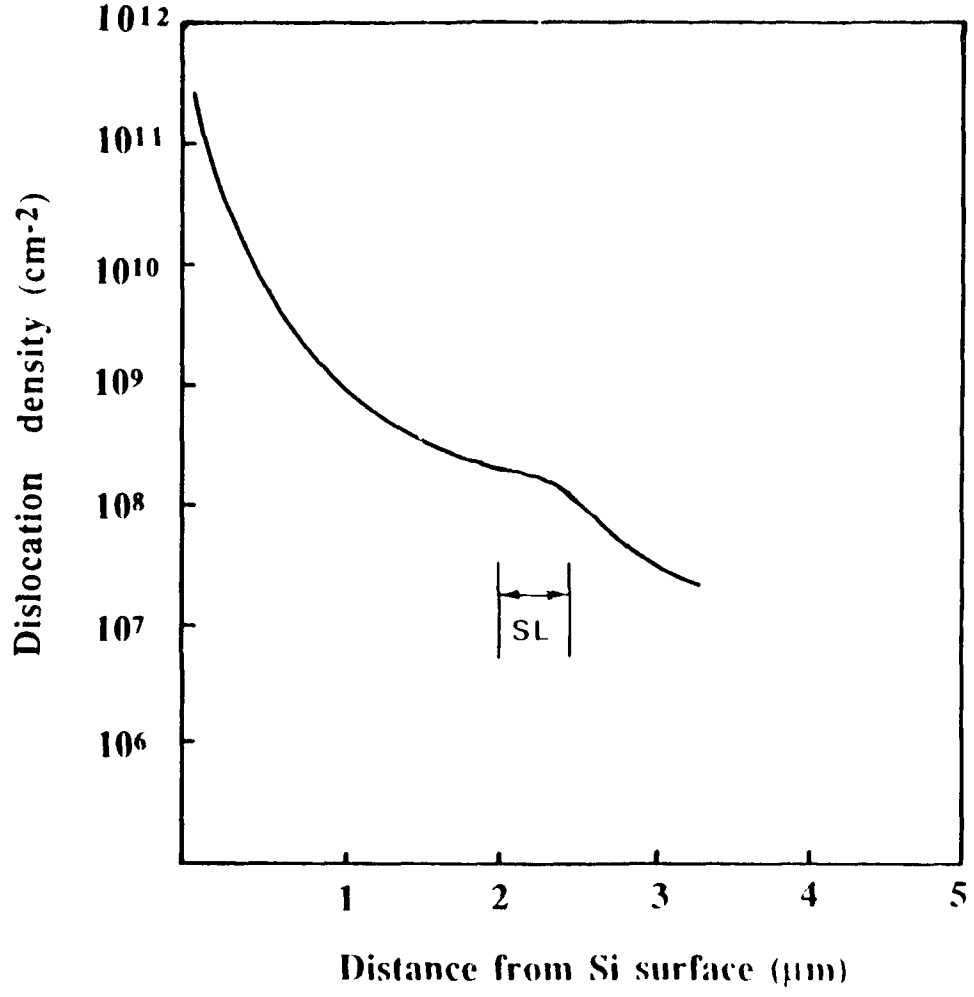



Fig. 5-8 Dislocation density profile of GaAs layer grown on Si substrate. The position of InGaAs-GaAsP strained-layer superlattice is shown by "SL" in the figure.

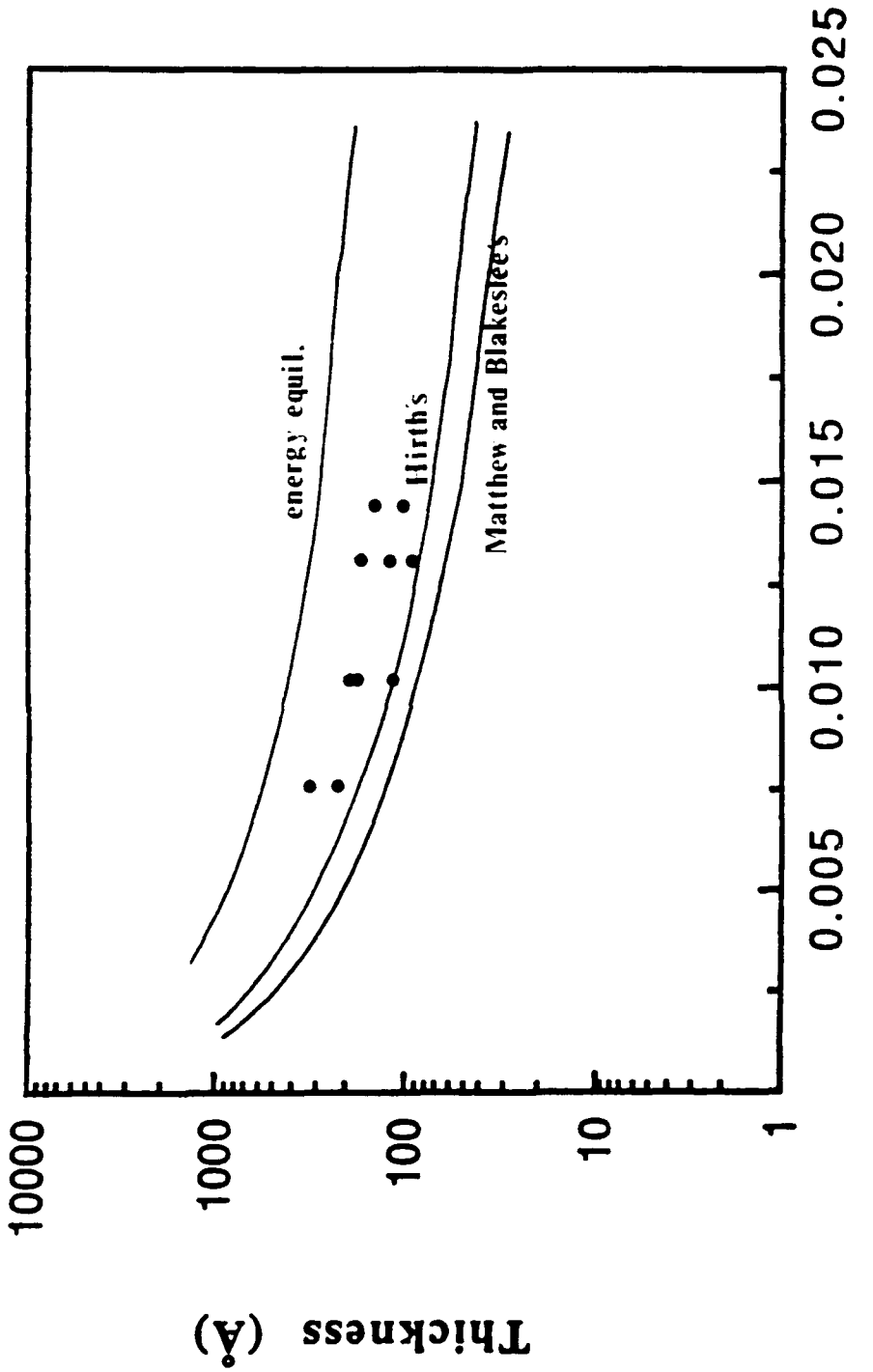



Fig. 5-9 Plots of the minimum critical thickness vs. mismatch (f). Experimental data from InGaAs-GaAsP grow on top of GaAs epilayer on Si substrate are compared with theoretical predictions.

bending effect are plotted as a function of the misfit (f). The measurements are based on the TEM observation. Theoretical predictions from our energy equilibrium model (Fig. 4-13), Matthews and Blakeslee's mechanical equilibrium model (Fig. 4-7), and Hirth's elastic anisotropic approach (Fig. 4-9) are compared in Fig. 5-8 with the experimental data. However, the quantative agreement between our energy equilibrium and the experimental data is not exact. Possible causes of discrepancy between our theoretical calculation and the observed results are :

(1) The area which the misfit strain has been accommodated by the formation of the misfit dislocation segment is only an approximate value. This area could be affected by the interface inperfection and the neighboring defects.

(2) Equation (4.32) is a good approximation for calculating areal strain energy density in general case. However, the elastic anisotropic should be involved in the calculation for more accurate prediction.

(3) The image force which is in the vicinity of the free surface will affect the interaction energies between dislocations[78]. However, the image problem is a formidable one which has not yet been solved.

(4) When the dislocation length or the spacing between two dislocations is close to the value of Burgers vector, the end effect will introduce error in the interaction energy calculation[78]. However, there is not proper correction to make up this error.

(5) The simplification of dislocation self energy (equation 4.38) where R is equal to the film thickness and R=4 are not appropriate when the grown-in dislocations density are high or different strained-layer system are involved.

(6) Since the thermally activated nature of the threading dislocation bent-over proces, the environmental temperature should be an important factor in determining the minimum critical thickness.

(7) The residual thermal strain introduced from the thermal expansion coefficient different between GaAs and Si results in a higher strain level than the strain which is simply equal to the misfit between strained-layer and GaAs substrate. And this higher strain level increase the importantceof the change of strain energy (equation 4.37) in our calculation, and make the experimental data lower than our therorectical prediction.

## 5.4. Summary

In conclusion, it has been shown that the $In_xGa_{1-x}As$-$GaAs_{1-y}P_y$ ($y=2x$) is an appropriate and highly effective buffer layer for reducing dislocations originating at GaAs-Si interface. The SLS structure also permits high values of strain to be employed without the SLS generating dislocations of its own. However, the present results also indicate that the effectiveness of the SLS depends on the density of dislocations. For instance, when the dislocation density is low, the threading dislocations are confined to the SLS intefaces and do not propagate into the GaAs epilayer. In contrast, when the dislocation density is very high, it is apparent that the SLS is not as effective. Further work is required to optimize the SLS structure by varying the strain and the number of the SLS layers in order to achieve high-quality GaAs on silicon with a very low dislocation density. Solution of better theoretical prediction of minimum and maximum critical thickness are necessary for fully exploring the effectiveness of strained-layer superlattices in reducing dislocation in GaAs epilayer grow on Si substrates. It is also evident that much more work is needed to understand the interaction and movement of dislocations at the SLS interfaces.

# 6. THE INTERACTION BETWEEN DISLOCATIONS AND SLS

## 6.1 Introduction

Chapter 5 reported on the effectiveness of InGaAs-GaAsP strained-layer superlattices in blocking threading dislocations in GaAs/Si epilayers. The nature and interactions of these dislocations with the SLS have not yet been fully studied. Detailed study of such interactions can lead the way to the proper understanding of the SLS parameters which are effective in blocking dislocations. This study is aimed at understanding the interactions which take place between the threading dislocations and the SLS strain field.

## 6.2. Experiment

This study utilized GaAs/Si samples grown in different laboratories. Highly strained SLS ($In_{1-x}Ga_xAs$-$GaAs_{1-y}P_y$) were grown on the GaAs/Si samples. A GaAs cap layer was grown on the SLS structure that made the total thickness of the epitaxial films on the Si substrate to be about 3 μm. The corresponding values of x and y were varied in the range of 8%-25% and 16%-40%, respectively. Individual layer thickness varied from 80-300Å depending on the ternary alloy composition. The compositions of the two ternary alloys (x and y) are adjusted such that the SLS was lattice matched to GaAs. The SLS was grown by metalorganic chemical vapor deposition (MOCVD). The SLS structures have been grown as a series of five-period strained layers separated by 0.2 μm GaAs. The growth conditions of SLS were disscussed earlier in chapter 4. Rapid thermal annealing (RTA) of the GaAs/Si samples was done at 900°C for 10 seconds prior to the growth in an

argon ambient. In situ furnace annealing was carried out in the MOCVD reactor at 830°C for 20 minutes in an overpressure of arsine. Annealing of the GaAs on Si was applied to achieve some dislocation reduction in GaAs epilayer. Transmission electron microscopy (TEM) was used for the structure characterization. Foils for TEM were thinned by mechanical polishing, followed by standard ion-milling techniques. Defect analyses were studied using a Hitachi-800 (200 KV), using conventional two-beam diffraction technique and g·b analyses (where g and b are the diffraction and Burgers vector, respectively).

### 6.3 Results and discussion

The g·b analysis show that GaAs on Si heteroepitaxy generally suffers from two types of threading dislocations propagating into the GaAs epilayer. Pure edge dislocations with b= $\pm$a/2[110] or $\pm$a/2[-110] are on the (001) plane parallel to the GaAs /Si interface. The second type are mixed dislocations with b=$\pm$a/2[011], $\pm$a/2[01-1], $\pm$a/2[101], and $\pm$a/2[10-1] that make 60° with their respective dislocation lines. The SLS has a number of effects on these dislocations as a result of their interactions with the SLS stress field. Table 6-1 illustrates the possible interactions that have been experimentally verified. Figures 6-1(a)-(d) show cross-section TEM micrographs where the interactions are taking place between threading dislocations and the SLS-strain field. In this figure, the SLS has x=0.2 and the individual strained layer thickness was 80 Å. The micrographs are taken up using four different operating reflections. Using Figs 6-1(a)-(d), g·b analysis allows us to detertmine the dislocation types. The possible Burgers vector in each of the reflections corresponding to Fig. 6-1 are tabulated in Table 6-2. The invisibility criterion in the table confirms that dislocation A is of a pure edge nature. This dislocation propagates through the strained-layer superlattice unaffected by the strain field. Dislocations B, C, D, and E were identified as 60° "mixed" dislocations. The 60° dislocations were bent inside the SLS and changed their direction to one of the <110> directions along the SLS interfaces. Bending requires that every threading dislocation experience a gliding force. This force is

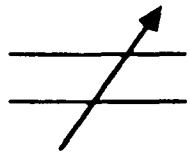
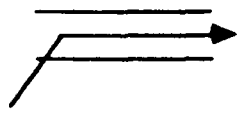
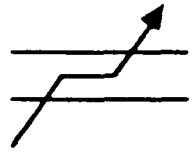
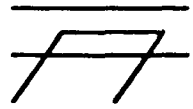
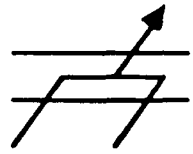
| Behavior | Conditions |
|---|---|
|  | i. edge dislocation (zero shear force)<br>ii. no P-K forces applied on dislocation. |
|  | finite P-K forces fully bend over the dislocation. |
|  | not enough P-K forces applied on dislocation |
|  | two similar but opposite sign Burgers vector dislocations → dislocation loop |
|  | b1 + b2 → b3 |

Table 6-1 The observed dislocations interactions with the SLS.

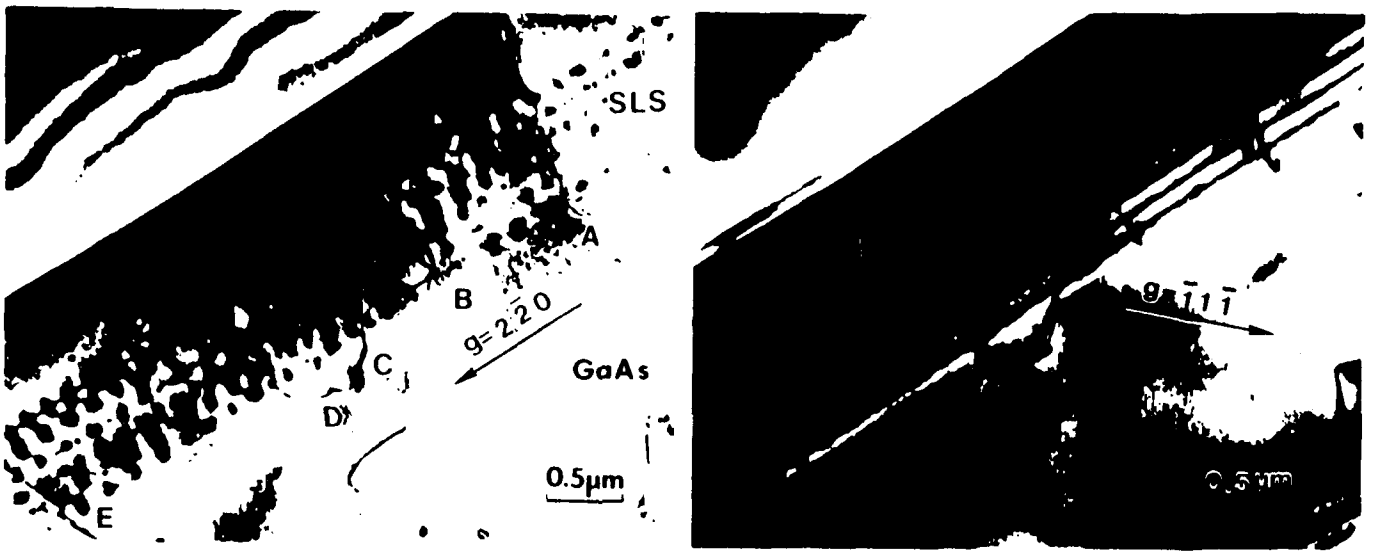
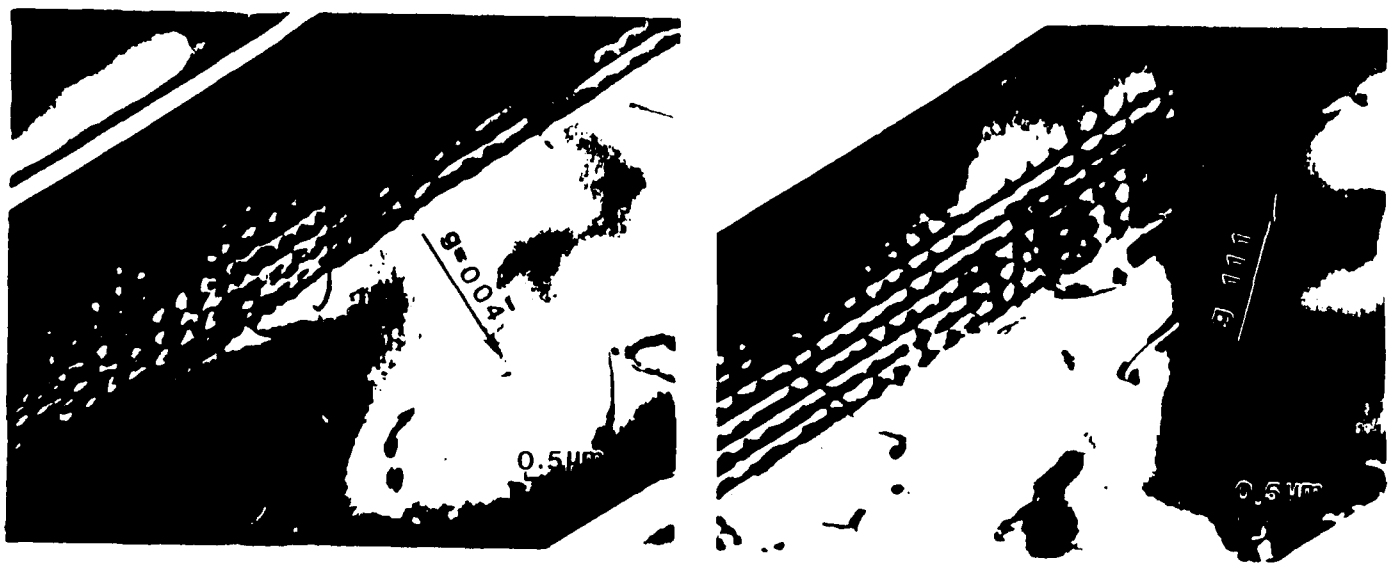



Fig. 6-1 Cross-sectional TEM micrograph showing the interaction between threading dislocations and the SLS. The micrographs are two beam bright field images with reflecting conditions : (a) g=[220], (b) g=[-11-1], (c) g=[004], (d) g=[-111].




c d

Fig. 6-1 Cross-sectional TEM micrograph showing the interaction between threading dislocations and the SLS. The micrographs are two beam bright field images with reflecting conditions : (a) g=[220], (b) g=[-11-1], (c) g=[004], (d) g=[-111].

Transmission Electron Microscope g·b Analyses

| Dislocation | Invisiblity Criterion | Burgers Vector (±) |
|---|---|---|
| A | g=(004) | a/2[1$\bar{1}$0] (edge type) |
| B | g=($\bar{1}$1$\bar{1}$) | a/2[10$\bar{1}$] or a/2[011] (Mixed) |
| C | g=($\bar{1}$11) | a/2[101] or a/2[01$\bar{1}$] (Mixed) |
| D | g=($\bar{1}$1$\bar{1}$) | a/2[10$\bar{1}$] or a/2[011] (Mixed) |
| E | g=($\bar{1}$1$\bar{1}$) | a/2[10$\bar{1}$] or a/2[011] (Mixed) |

Table 6-2 Transmission electron microscope g·b analyses of Fig. 6-1 (a) - (d).

the Peach-Koehler force (PF) that depends on the strain ($\varepsilon$) and the layer thickness (h). Matthews and Blakeslee have proposed a $h_{c,\,min.}$ as a critical layer thickness of the SLS for bending the threading dislocations. SLS layer thickness (h) was chosen such that $h_{c,\,min.} < h < h_{c,\,max.}$, where $h_{c,\,min.}$ and $h_{c,\,max.}$ are the calculated layer thicknesses following Matthews and Blakeslee's model (using $\varepsilon_{max.}$=f the lattice mismatch). Therefore, there will be finite stresses from SLS, acting to bend over and confine the threading dislocations.

The lattice mismatch (f=$\varepsilon$) in the SLS offers a biaxial state of stress $\sigma_{11}= \sigma_{22}=\sigma$, where $\sigma=K\varepsilon$ [K is a constant which is dependent on the shear modulous $\mu$ and Poission's ratio $\upsilon$[86]. Assuming isotropic behavior, then from the crystal symmetry of the diamond cubic $\sigma_{33}$, the shear stresses and strains are equal to zero. The resolved shear stresses and strains are equal to zero. The resolved shear stresses in the slip planes and slip directions are shown in Table 6-3. From Fig. 6-1 and Table 6-3 one comes to the following observations: (a) For GaAs grown on the exact (001) Si substrates the shear stress acting on the edge dislocations is zero in the slip direction. (b) The 60° mixed dislocations is subjected to a resolved shear stress in the slip plane and slip direction of $\sigma/\sqrt{6}$. It is apparent from the above results that the slip direction of edge dislocation A in Fig. 6-1 is parallel to the film plane (001), and the stress field of the SLS under these conditions has no effect on the dislocation. Conversely, there are finite stresses from the SLS to bend over and confine the mixed dislocations B, C, D, and E. Clearly such a technique is the most desirable for a significant reduction in the dislocation density when the majority of the dislocations are of the mixed type.

If the force acting on the dislocation is insufficient to keep it bent at SLS interface, threading dislocations are either unperturbed or wavily propagate within the SLS as shown in Fig. 6-2. The SLS in this sample consisted of $In_{0.8}Ga_{0.92}As$ and $GaAs_{0.84}P_{0.16}$ and the misfit strained at the interfaces in the SLS are considered to be smaller than that in the

Resolved Shear Stress In the Different Possible Slip Planes and Slip Directions for GaAs Film on (001) Si Substrate.

| Slip Plane | Slip Direction | Shear Stress |
|---|---|---|
| (111) | $[10\bar{1}]$ | $\sigma\sqrt{6}$ |
| | $[01\bar{1}]$ | $\sigma\sqrt{6}$ |
| | $[1\bar{1}0]$ | 0 |
| $(\bar{1}11)$ | [101] | $-\sigma\sqrt{6}$ |
| | $[01\bar{1}]$ | $\sigma\sqrt{6}$ |
| | [110] | 0 |
| $(1\bar{1}1)$ | $[10\bar{1}]$ | $\sigma\sqrt{6}$ |
| | [011] | $-\sigma\sqrt{6}$ |
| | [110] | 0 |
| $(11\bar{1})$ | [101] | $\sigma\sqrt{6}$ |
| | [011] | $\sigma\sqrt{6}$ |
| | $[1\bar{1}0]$ | 0 |
| (001) | [110] | 0 |
| | $[1\bar{1}0]$ | 0 |

Table 6-3 Resolved shear stress in the different possible slip planes and slip directions for GaAs film grown on (001) Si substrate.

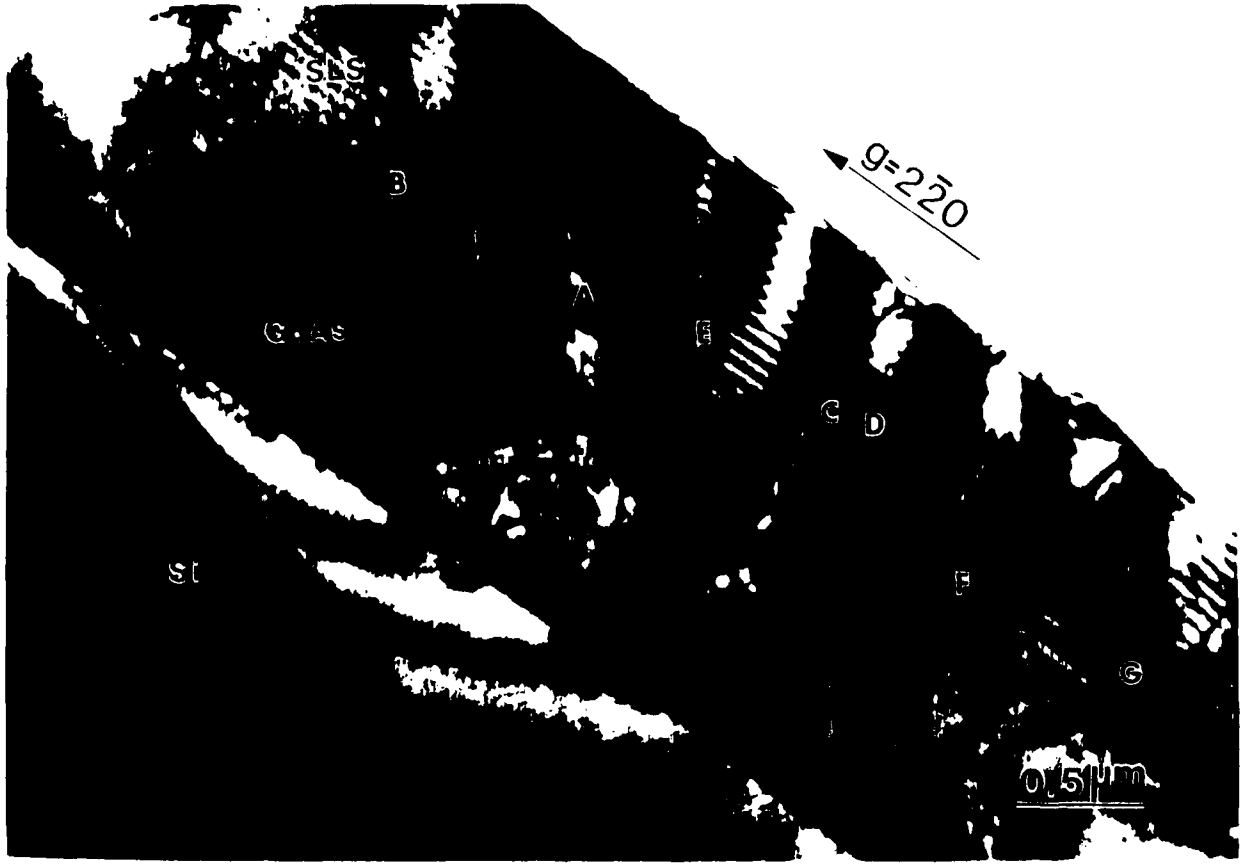
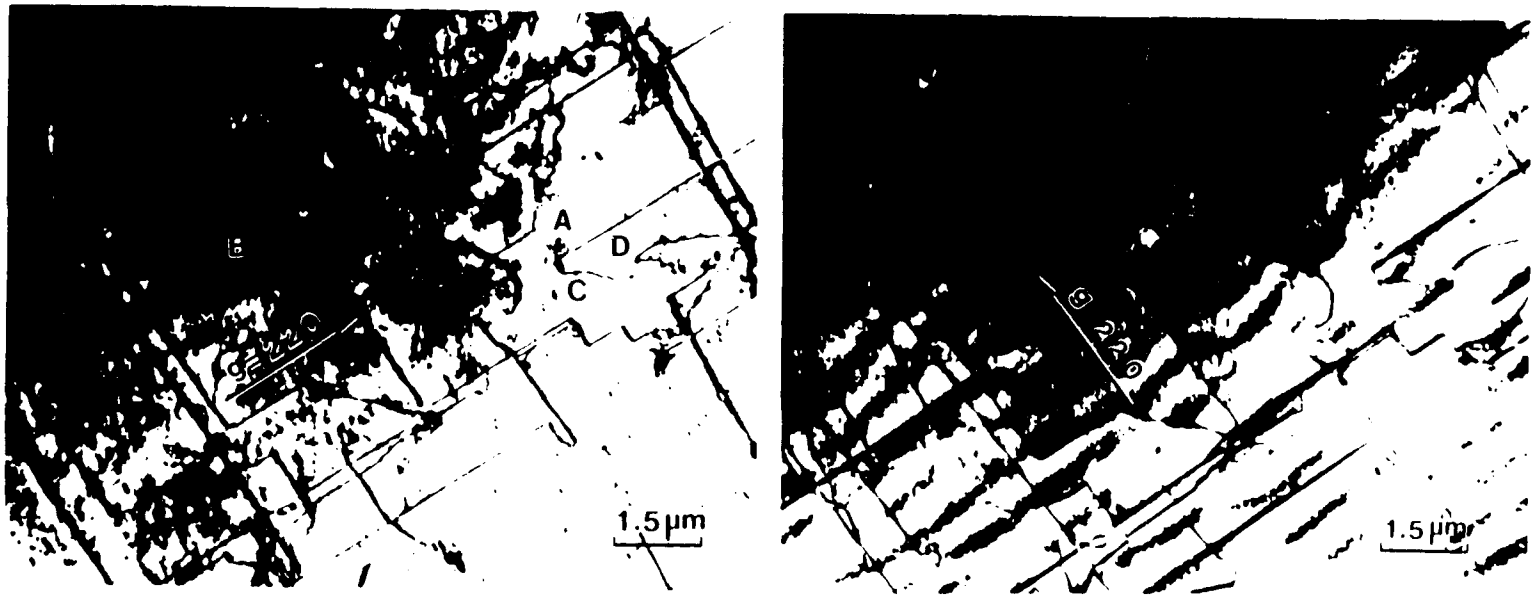



Fig. 6-2 Cross-sectional TEM micrograph illustrating the effect of insufficient bending forces on a mixed threading dislocations.

sample above. A dislocation marked by arrow D penetrated through the SLS without being bent as shown in Fig. 6-2. The g·b analysis revealed that this dislocation is of mixed type. Another dislocation marked by arrow E in Fig. 6-2 changed the direction of propagation a few times.

Figures 6-3(a)-(d) show plan-view micrographs of the bent dislocations within the SLS interface. Using g·b analysis almost all the bent (stairlike) dislocations were identified as 60° mixed dislocations. A few segments were found to be edge dislocations identified as A and B in the figure. It is evident that mixed dislocations are strongly affected and bent by the strain field of the SLS. The bent dislocations tend to propagate for several micrometers at the SLS interfaces in <110> directions unless they are forced to interact with a strain field of a neighboring defect.

Interactions between adjacent threading dislocations depend on their stress field and their separation distance. Since a high dislocation density ($10^8$-$10^9$ $cm^{-2}$) is penetrating the SLS, the distance between the dislocations is sufficiently close for interactions. The repulsive and attractive stress fields between the dislocations are clearly shown in both Fig. 6-3 and 6-4. Dislocations that react to form a third one at a node are observed in Fig. 6-3. As seen, dislocations A, C, and D are interacting at a node. Using g·b analysis the corresponding Burgers vectors are as follows: $\pm$a/2[110] for dislocation A, $\pm$a/2([101] or [-101]) for dislocation C, and $\pm$a/2([011] or [01-1]) for dislocation D. The possible reactions at that node are as follows: $b_A+b_C=b_D$, $b_C+b_D=b_A$, or $b_A+b_D=b_C$. Any of these reactions will result in 50% decrease in the number of interacting dislocations. Meanwhile Figure 6-4 shows a condition where two dislocations react to form a loop. From the figure, using two beam conditions and different diffraction vectors, the Burgers vector for dislocations X, Y, and Z have the form $\pm$a/2([101] or[01-1]), $\pm$a/2([011] or [10-1]) and $\pm$a/2 ([101] or [01-1]), respectively. Dislocation X is threading from GaAs epilayer and

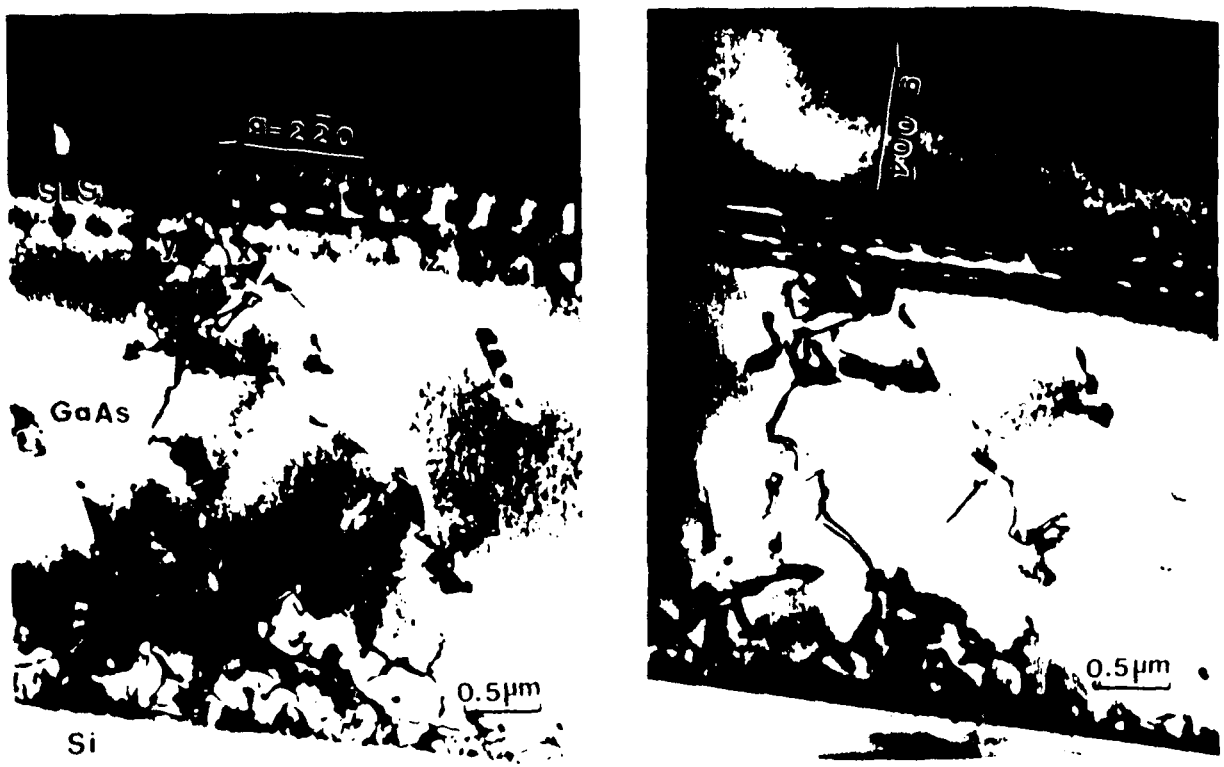



a b

Fig. 6-3 Plan-view TEM micrograph illustrating the interactions between bent dislocations at the SLS interfaces : (a) g=[220], (b) g=[2-20], (c) g=[400], (d) g=[040].

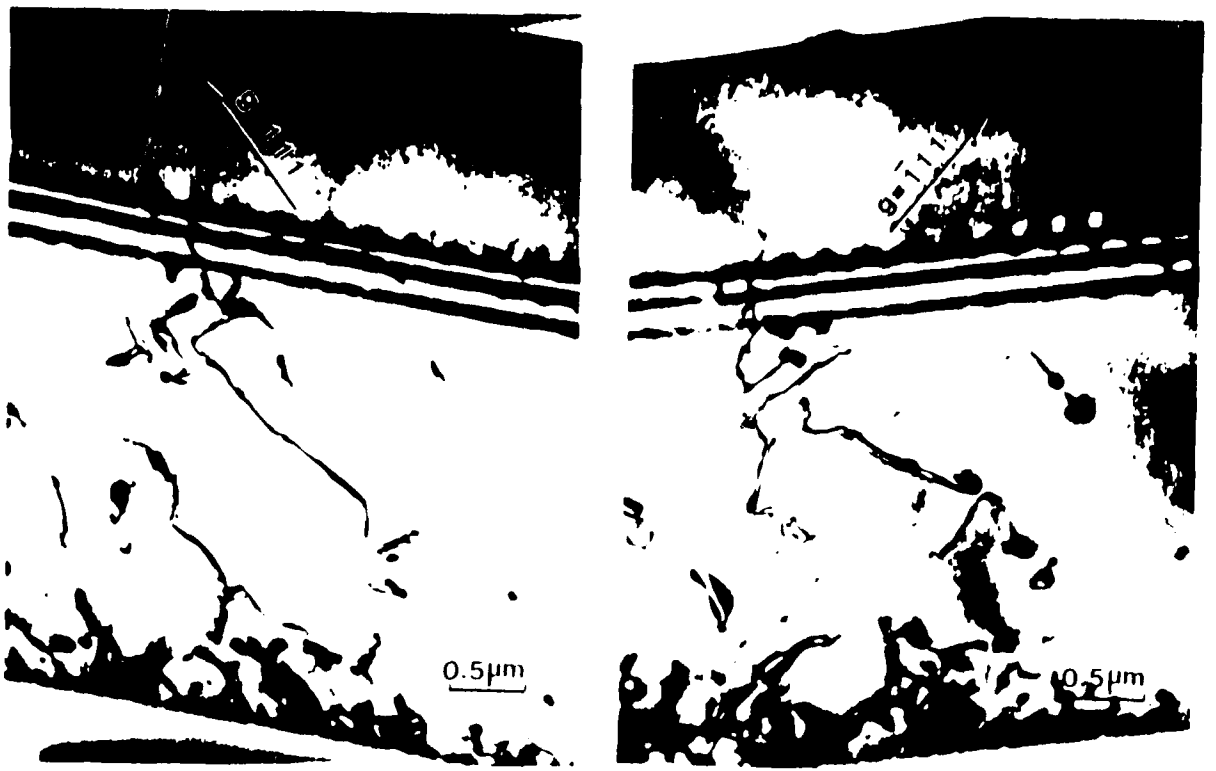

c d

Fig. 6-3 Plan-view TEM micrograph illustrating the interactions between bent dislocations at the SLS interfaces : (a) g=[220], (b) g=[2-20], (c) g=[400], (d) g=[040].




a b

Fig. 6-4 Cross-sectional TEM micrograph illustrating the interaction between threading dislocations and the SLS. The micrograph are two-beam bright-field images with four reflecting conditions (a) g=[2-20], (b) g=[00-4], (c) g=[1-11], (d) g=[-111].




c d

Fig. 6-4 Cross-sectional TEM micrograph illustrating the interaction between threading dislocations and the SLS. The micrograph are two-beam bright-field images with four reflecting conditions (a) g=[2-20], (b) g=[00-4], (c) g=[1-11], (d) g=[-111].

interacting with Y. However, the reaction ( $b_x + b_y = b_z$ ) would result in an increase in their total self-energy. Mutual repulsive forces from the total self-energy increase tend to keep the dislocations X and Y separated. repelled by dislocation Y and also affected by the strain field of the SLS, dislocation X bends and propagates along the SLS interface. When two adjacent dislocations X and Z close, due to their similar but opposite Burgers vectors, they join one another and form a loop. This type of reaction is an important mechanism in the current dislocation reduction technique. Table 6-1 summarizes the above discussed interactions between the SLS and the threading dislocations.

## 6.4. Summary

Several interaction between the strain field of the SLS [$In_xGa_{1-x}As$-$GaAs_{1-y}P_y$ ($y=2x$)] and the threading dislocations in GaAs grown on the Si substrate are observed. The stress field associated with the SLS has a shear component that forced the 60° mixed dislocations to bend at the SLS interface. The individual layer thicknesses should be close to $h_{c,max}$, in a given superlattice to maximize the gliding forces acting on the dislocations. The bent dislocations propagate at the interface for a distance of several micrometers. The number of dislocations which propagate and interact within the SLS is high such that the distance between them is sufficiently close to cause interactions. Favorable conditions for dislocation reduction are realized when (1) the dislocation is bent at the SLS interface and propagates to the sample edge, (2) two dislocations interact to cancel each other by forming a loop, and (3) two dislocations react to form a third one at a node.

# 7. THE EFFECTIVENESS OF STRAINED-LAYER SUPERLATTICE COMBINED WITH ANNEALING

## 7.1 Introduction

The initial results of utilizing the GaAsP-InGaAs strained-layer superlattice buffer in reducing the dislocation density in GaAs/Si films indicates the following:

i) In areas of low dislocation density, almost all threading dislocation are blocked and bent along the SLS interfacial planes.

ii) The SLS is most effective in confining the bent dislocation at the interface in the absence of strain field generated by another dislocation.

iii) The bent dislocation in the low density regions can propagate along the SLS interface several microns without disturbance. This indicates that under certain strain levels the bending of threading dislocations is energetically favorable.

iv) The SLS layers do not have an infinite capacity in bending the threading dislocations. The strain level, the layer thickness and the number of periods of the SLS affect the force acting on the dislocations and effectively bend them.

v) The effect of strain in SLS's on dislocation reduction may be reduced by high dislocation densities in SLS's.

A significant improvement of the crystalline quality of GaAs on Si has also been achieved by using conventional furnace annealing. However, further reduction in dislocation density is required from the viewpoint of developing the aforementioned defect-sensitive devices.

Encouraged by the quality of the annealed herterointerface and the effectiveness of using strained layer superlattice; this chapter will investigate the effect of preannealing

combined with intermitent annealing during or after the SLS growth on the further reduction of dislocation density. The optimization of both the intermediate strained layer superlattice structure and annealing would have the advantage to improve the SLS efficiency significantly.

## 7.2 Experiment

The GaAs/Si samples used in this study were grown by molecular beam epitaxy (MBE) growth technique. Thermal annealing was employed under over pressure of Aresine in the metalorganic chemical vapor deposition (MOCVD) reactor at 830 °C for 30 minnutes prior to the strained layer superlattice growth. The SLS used in this study was grown at 650 °C by MOCVD as previously described. Three types of SLS-annealing combination structures were studied: structure (A): three groups of 5 periods SLS [$In_{0.2}Ga_{0.8}As$-$GaAs_{0.65}P_{0.35}$ (80Å/layer)] separated by 800 Å GaAs. Structure (B): annealing during the growth for two groups of 4-periods highly strained SLS with the same structutre as in structure (A). The growth was interrupted and annealed in-situ at 830 °C for 10 minutes then slowly cooled down to SLS growth temperature at 650 °C. This was followed by four groups of 5-periods SLS having the same strain level and a 1 μm GaAs cap layer. Structure (C) was annealed after the SLS growth, where three groups with the same SLS as in structure (A) were grown with a 1 μm GaAs cap layer followed by post annealing at 830 °C for 30 minutes. Fig.7-1, 2, and 3 show the layer structures and their parameters, respectively. Transmission Electron Microscopy (TEM) was used for the structure characterization. Cross-sectional TEM observations were performed on a Hitachi-800 (200KV), using the conventional two-beam diffraction technique.

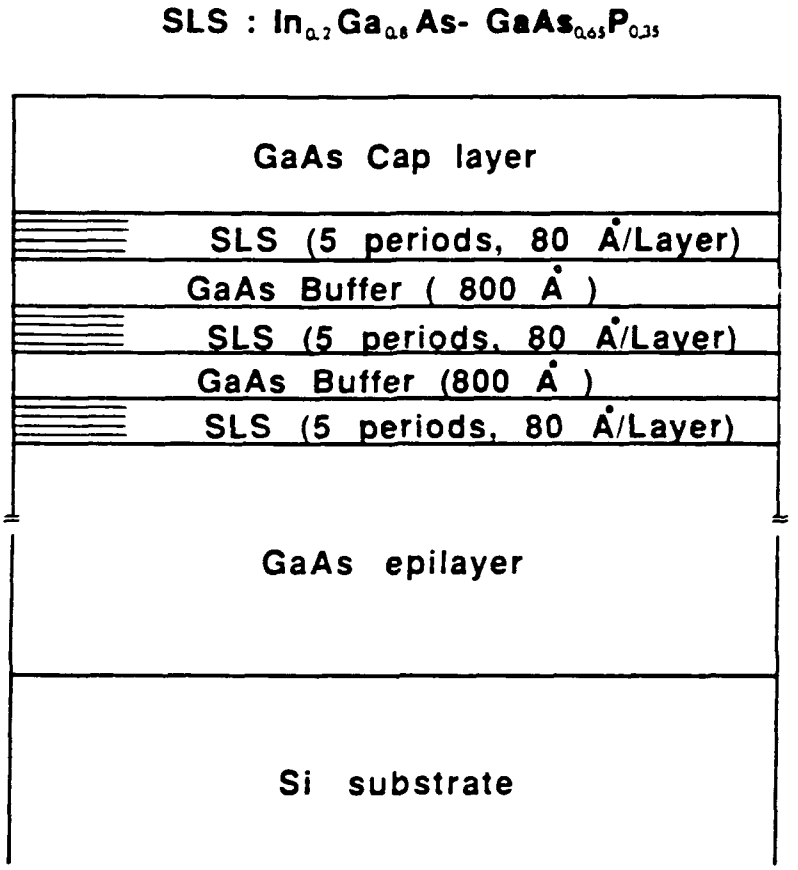



Fig. 7-1 Schmatics of InGaAs-GaAsP strained-layer superlattices structure.

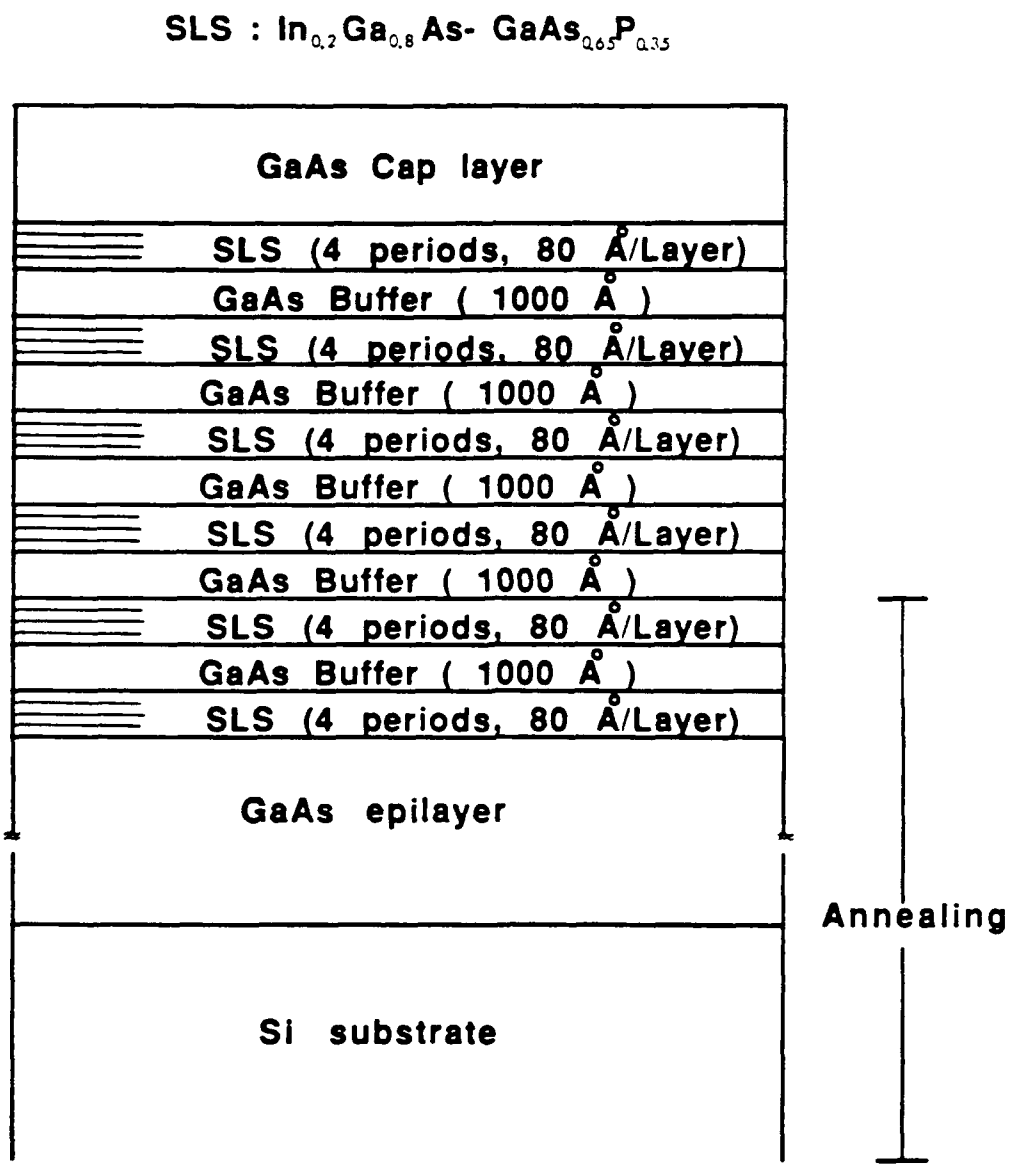



Fig. 7-2 Schmatics of InGaAs-GaAsP strained-layer superlattices structure.

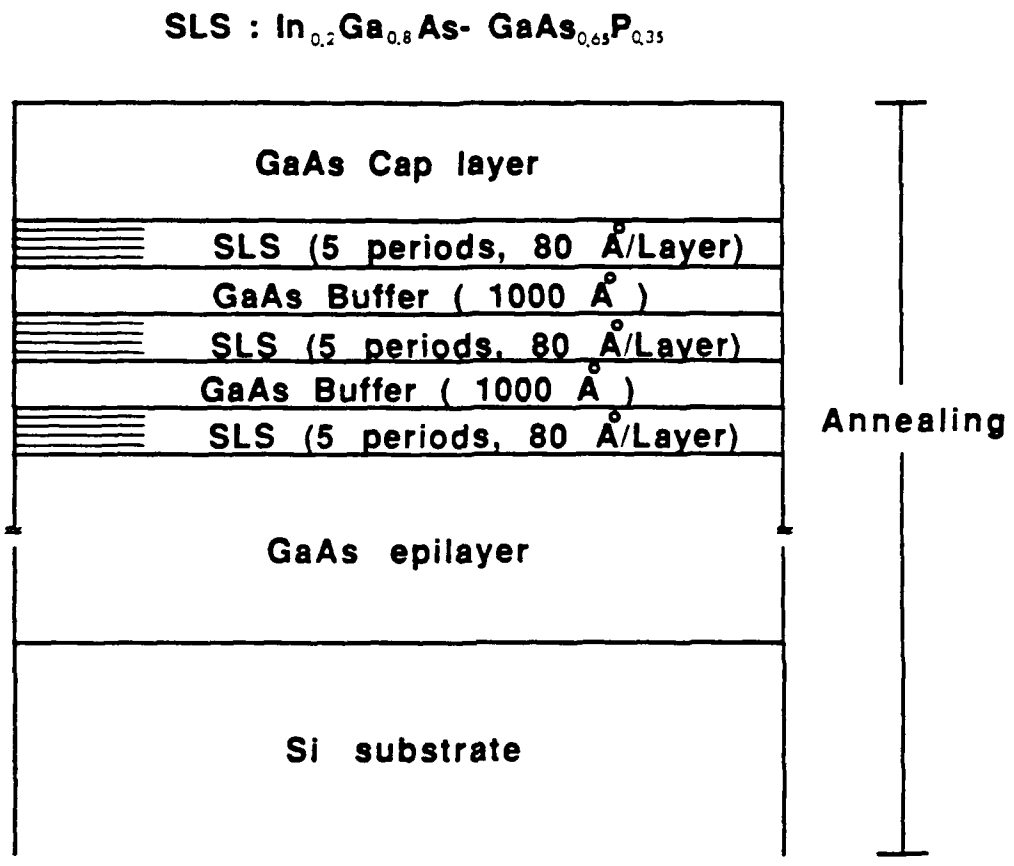



**Fig. 7-3** Schmatics of InGaAs-GaAsP strained-layer superlattices structure.

## 7.3 Results and discussion

It is apparent from the experimental results in Chapter 5 that for the strained-layer superlattice to be made more effective, the density of impinging dislocations on the SLS must be reduced. This reduction in dislocation density can be achieved by conventional furnace annealing which a much low dislocation has been sucessfully obtained in Chapter 3.

Shown in Fig. 7-4 is a cross-sectional TEM micrographs of GaAs-on-Si sample which was conventionally furnace annealed before the growth of SLS. Numerous dislocations are seen to initiate at the GaAs/Si interface and only some of them reach the strained layer superlattice. The number of grown-in threading dislocations reaching the SLS is much lower than the sample which was not annealed (Fig. 7-5) prior to the SLS growth.

The bent dislocations in the low density regions can propagate along the SLS interface a distance of several microns without disturbance, this occurs in the absence of a strain field generated by a neighboring dislocation. There is a critical separation distance between the threading dislocations below which the local relaxation offered by the dislocations will relax the SLS. The residual strain ($\varepsilon$) will be reduced to $\varepsilon=( f - \delta )$, where $\delta$ is the strain relaxed locally by the dislocation and f is the misfit strain. The critical separation distance can be estimated as:

$S_{crit.}= b\perp/f$, where $b\perp$ is Burger's vector edge component of the threading dislocation in the strained film plane. The calculated values of $S_{crit.}$ and f are as follows:


Fig. 7-4 Cross-sectional TEM bright-field image of GaAs on Si sample which was conventionally furnace annealed prior the growth of InGaAs-GaAsP strained-layer superlattices.


Fig. 7-5 Cross-sectional TEM bright-field image of InGaAs-GaAsP strained-layer superlattices directly grown on as grown GaAs on Si sample.

| f | 0.0075 | 0.0108 | 0.0144 |
|---|---|---|---|
| S(Å) | 267 | 185 | 13 |

From the table it is obvious that the higher the misfit strain on the SLS the shorter is the distance allowed between the dislocations threading the superlattice, i.e. the higher the dislocation density that the SLS can handle. Thus, the higher the strain level, the layer thickness and the number of periods in the SLS are, the better the effectiveness of the superlattice in bending dislocations.

As demonstrated in Chapter 4, the probability that a threading dislocation can bend and glide along the strained layer superlattice interfaces is proportional to

$$\exp(-\Delta E^*/KT) \tag{7.1}$$

where $\Delta E^*$ is the critical total energy change. The value of $\Delta E^*$ depends primarily on two factors : (i) strained layer thickness (h) and (ii) the misfit (f) between strained layer and substrate. As the thickness and/or misfit increase the value of $\Delta E^*$ decrease. Equation 7.1 reflects the thermally activated nature of the threading dislocation bending process; that is, as temperature is raised, the increased thermal energy enhances the probability that a threading dislocation would have a stable misfit segment increased. At a more elevated temperature, the effectiveness of the SLS in blocking threading dislocations natually becomes stronger. Therefore, employing an annealing process with a temperature higher than the strained layer superlattice growth temperature during or after the SLS growth, is expected to have a tremendous improvement in the effectiveness of SLS's.

The TEM micrographs of cross-sectional samples which have been intermittently annealed during and after the SLS growth are illustrated in Fig 7-6 and 7-7 respectively. Before the intermittent annealing, the bent dislocations at the SLS interfaces form segments of misfit dislocations only along the <110> directions. This creates a high density of two dimensional dislocation network at the SLS interfaces which may enhance the annihilation interactions. It is obvious that the interaction between SLS and threading dislocations is enhanced by internittent annealing. Also, it is clearly indicated that the threading dislocations are strongly confined within the annealed two series of SLS and that gliding along the SLS interfaces occured. By this intermittent annealing process, the grown-in threading dislocation density can be dramatically reduced. This will allow the gradual reduction of the dislocation density and the subsequent SLS to powerfully and effectively bend the threading dislocations without the local relaxation of the SLS strain by the high threading dislocation density.

Interdiffusion between SLS layer may occur at the annealing temperatures. However Fig. 7-8 indicates that the SLS stay coherent after annealing at 830°C for 30 minutes and that the interface abruptness for such application of SLS is not critical. Most of the strain at the SLS interface have already been relaxed by the existing misfit dislocations of bend-over threading dislocations and no additional misfit dislocations can be generated by the SLS itself during the annealing procedure.

Slow and fast cooling after annealing were also employed for the previously mentioned structures after SLS growth. Fig 7-7 is the cross-sectional TEM images of the specimen which was annealed and slowly cooled after the SLS growth, while Fig. 7-9 shows the effect of fast cooling of the same structure after annealing. Plan-view bright-field TEM has been performed on structure (C) with slow cooling to assess the effectiveness of the post annealing. Fig. 7-10 shows a plan-view micrograph which a dislocation density of $6 \times 10^6$ $cm^{-2}$ has been observed by post-annealing and slow cooling

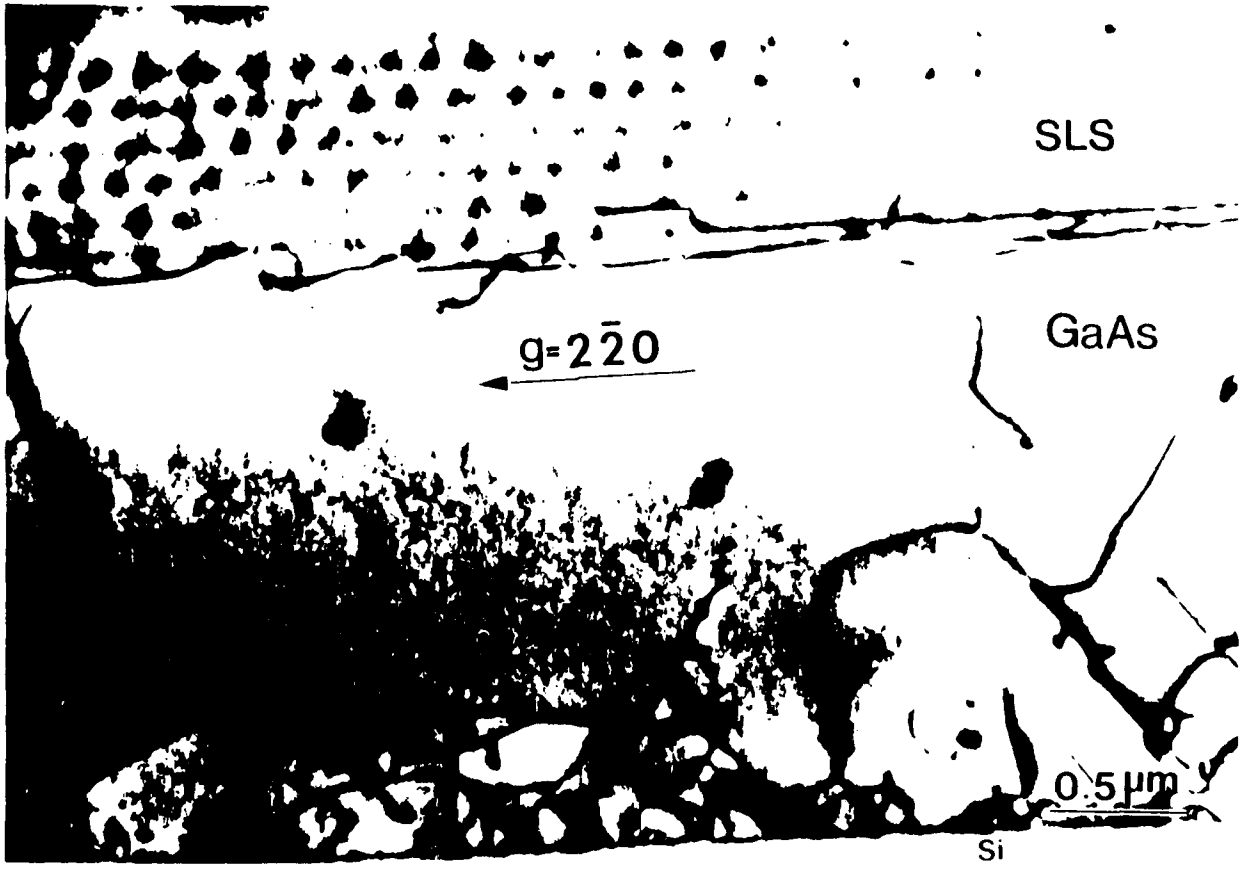



Fig. 7-6 Cross-sectional TEM bright-field image illustrating the effectiveness of the combination of SLS and intermittant annealing in dislocations reduction.

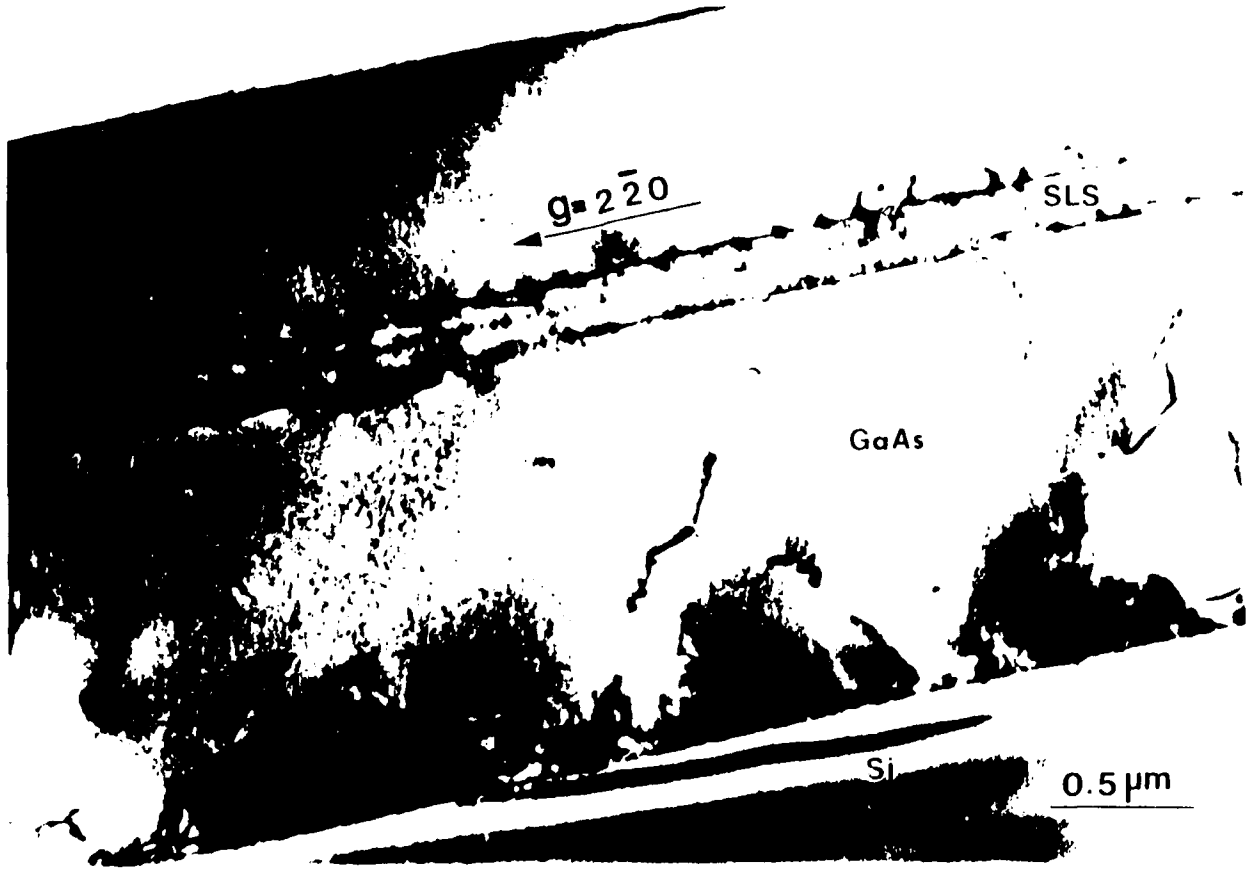



Fig. 7-7 Cross-sectional TEM bright-field image illustrating the effectiveness of the combination of SLS and post annealing (slow cooling) in dislocations reduction.

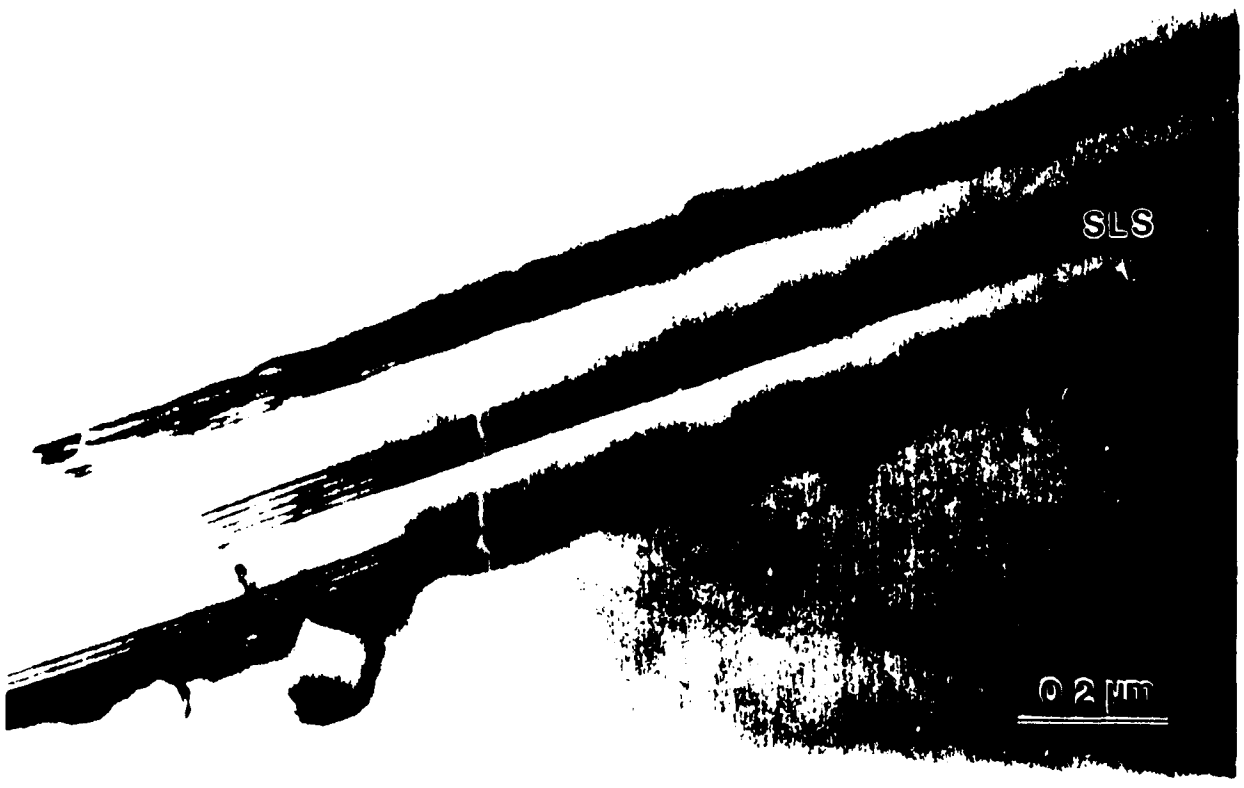



Fig.7-8 Cross-sectional TEM bright-field image illustrating the effectiveness of the combination of SLS and post annealing (slow cooling) in dislocations reduction.

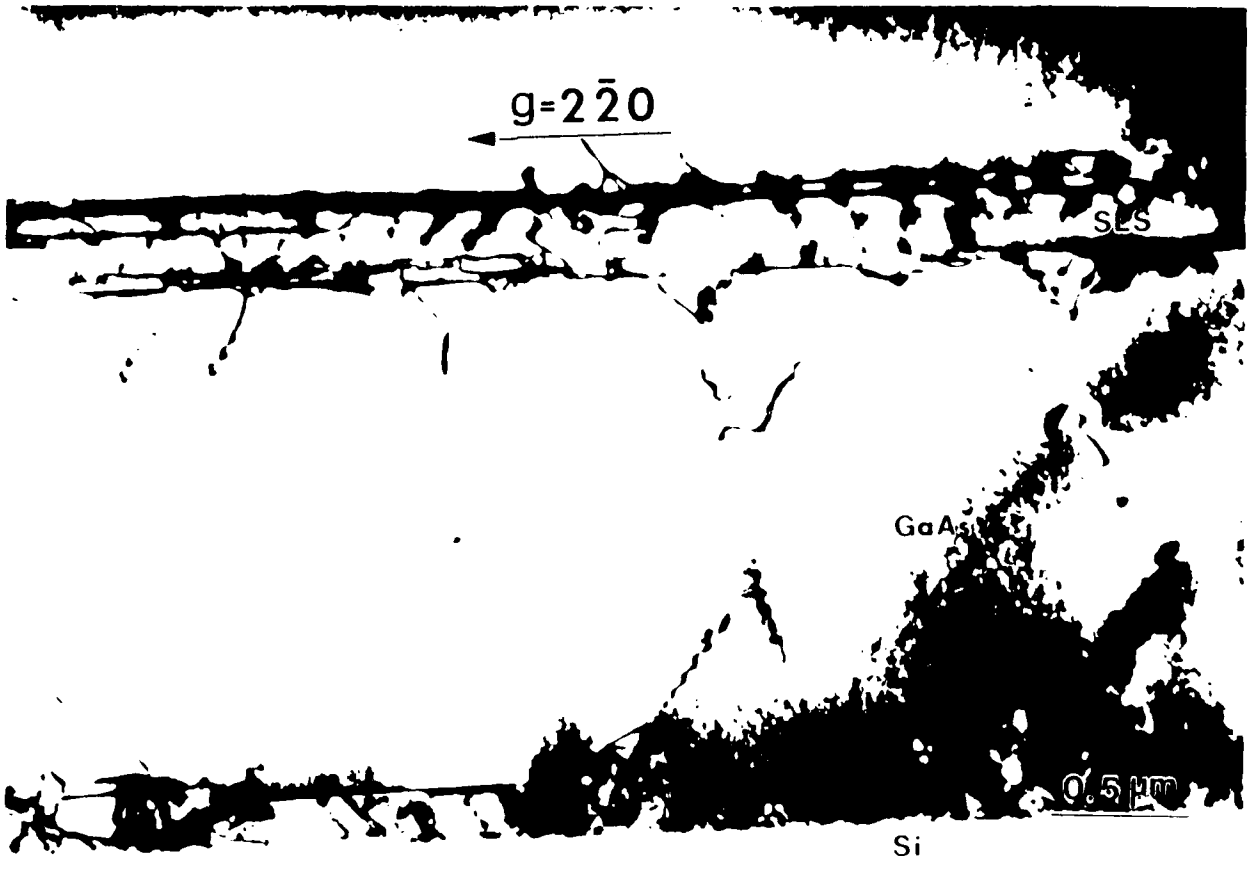



Fig. 7-9 Cross-sectional TEM bright-field image illustrating the effectiveness of the combination of SLS and post annealing (fast cooling) in dislocations reduction.

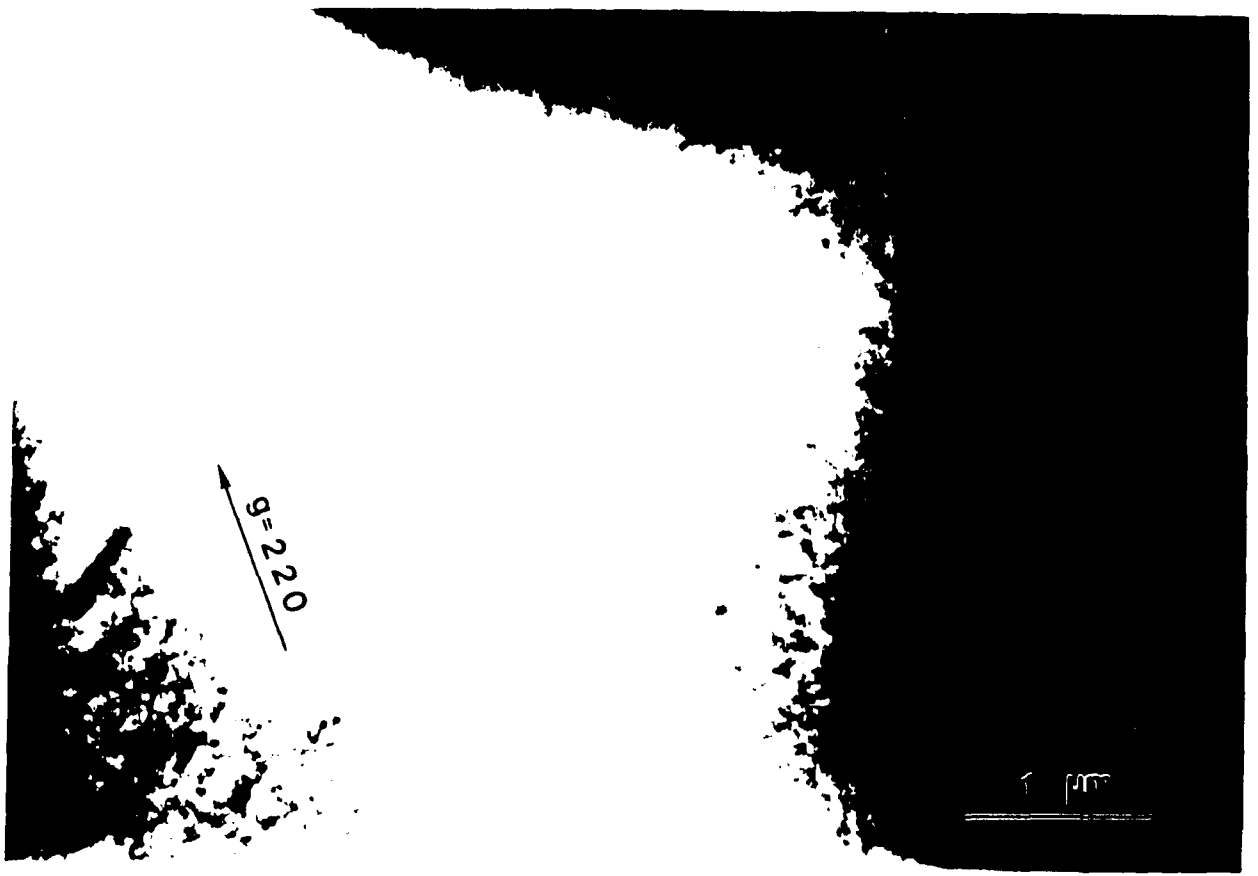



Fig. 7-10 Plan-view TEM micrograph illustrating the effectiveness of the combination of SLS and post annealing (slowcooling) in dislocations reduction.

the samples with SLS's. A FWHM (full width at half-maximum) of 170" of double crystal X-ray rockin curve result indicating a dislocation density of less than $1*10^7$ $cm^{-2}$ has also been achieved from X-ray rocking curve results. It is apparent from the above results that post-annealing of the SLS shows significant defect confinement within the SLS, where the whole SLS structure during annealing can be considered as a dislocation sink. However, considering the higher thermal expansion coefficient mismatch between GaAs and Si, fast cooling after annealing induces a high thermal strain that create more misfit dislocations within the SLS compared to slow cooling. Therefore, annealing coupled with slow cooling, is required to reduce the residual thermal stresses in the grown structure.

## 7.4 Summary

In conclusion, we have found that the effectiveness of SLS in blocking threading dislocations is improved by increasing the ($\varepsilon$), the layer thickness (close to $h_{c,\,max.}$) and the number of the strained layers. The SLS coupled with intermittent annealing during or after the SLS growth permits a remarkable reduction of threading dislocation density. The intermittent annealing provides the energy for the interaction between threading dislocations and the strain of SLS, therefore the efficiency of these SLS's can be significantly improved. It has been shown that the conventional annealing followed by slow cooling is an effective technique to minimize the thermal stresses which enhance the further generation of defects during fast cooling of the GaAs structure. Further work is in progress to optimize the SLS/annealing parameters in order to achieve device quality GaAs epilayers grown on Si substrates.

# 8. SELECTIVE ETCHING OF GaAs ON Si

## 8.1 Introduction

One of the important issues in defect reduction in GaAs epitaxial layer grown on Si is the presence of residual stresses in the GaAs epitaxial layer. It has been shown that GaAs epitaxial layers grown on Si substrates experience a uniform biaxial tension stress in the plane of the layer of about 1.5 kbar at room temperature (300 K)[86, 87]. This was consistent with the GaAs layer being unstressed at growth temperature (about 600°C). The difference in the thermal expansion coefficient between GaAs and Si results in the observed uniform biaxial tensile stress at lower temperatures. The misfit stress from the 4.1% lattice mismatch has been relaxed by the existence of misfit dislocations for layer thickness over the critical thickness (≈ 6 Å) of GaAs on Si. The presence of stress is also important for device application, since it leads to the modification of the band structure of GaAs, and thus affect the optical and electrical properties.

Recently, Cathodoluminescence (CL) scanning electron microscopy studies in the vicinity of microcracks in GaAs/Si revealed considerable variations in the optical properties near the microcracks[88]. In particular stress relief was found at the intersection of two microcracks[88]. Thus, it is of great interest to explore the effect of other types of boundaries such as those formed by patterning or selected-area epitaxy. If stress reduction can be achieved in a controlled manner, it would have important implications for defects reduction in GaAs epilayer grown on Si.

A simple model[89] has been presented which was used to calculate the wafer bow (or warpage, stress) in the film based on thickness, area of coverage, and film type. The stres equation relates the bow to film thickness, geometry, and material properties as :

$$\delta=3\left(\frac{R}{t_s}\right)^2 E_f\left(\frac{1-\upsilon}{E_s}\right) t_f \qquad (8.1)$$

where: $\delta$ =wafer bow ( $\delta>0$) for convexity, R=wafer radius, $t_S$=substrate thickness, $E_f$=Young's modulus of the film, $E_S$=Young's modulus of thesubstrate, $\upsilon$=Poisson's ratio for the substrate, and $t_f$ = the film thickness, all substrates are [100] orientation. If a portion of the film is etched open, the stress is reduced proportionally as shown in Fig. 8-1. The stress model then becomes

$$\delta= K\, t_f\, A \qquad (8.2)$$

where K= the product of material and geometric terms $(R/ts)^2 E_f(1-v/E_S)$, and A=fractional area of wafer covered by films. The assumption in equation (8.2) is supported by the data in Fig. 8.2, showing the bow vs. coverage area at a constant thermal $SiO_2$ thickness on Si substrate[88].

Therefore, for an appropriate size of patterning epitaxy the stress field in the epilayer can be almost relaxed. When the stress field in GaAs epilayer on Si is almost relaxed , a large number of defects, which are not contributing to accommodate the residual stress field and the lattice mismatch between GaAs and Si and which are simply raising the free energy of the system, can be eliminated after an appropriate annealing. In charpter 3, conventional furnace annealing/slow cooling procedure has been considered as a favorable annealing procedure without inducing any extra stress after processing. According to Matthew's model[69, 70, 71] only $8x10^6/cm^2$ misfit dislocations should be generated to accommodate the lattice mismatch between GaAs and Si. Therefore, a technique combining selective etching and conventional furnace annealing/slow cooling is considered as the most promising way to achieve device quality GaAs film on Si substrates. In this

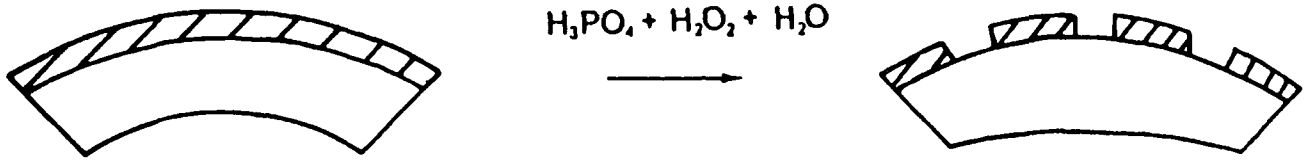



Fig. 8-1 Reduction in bow with film opening.

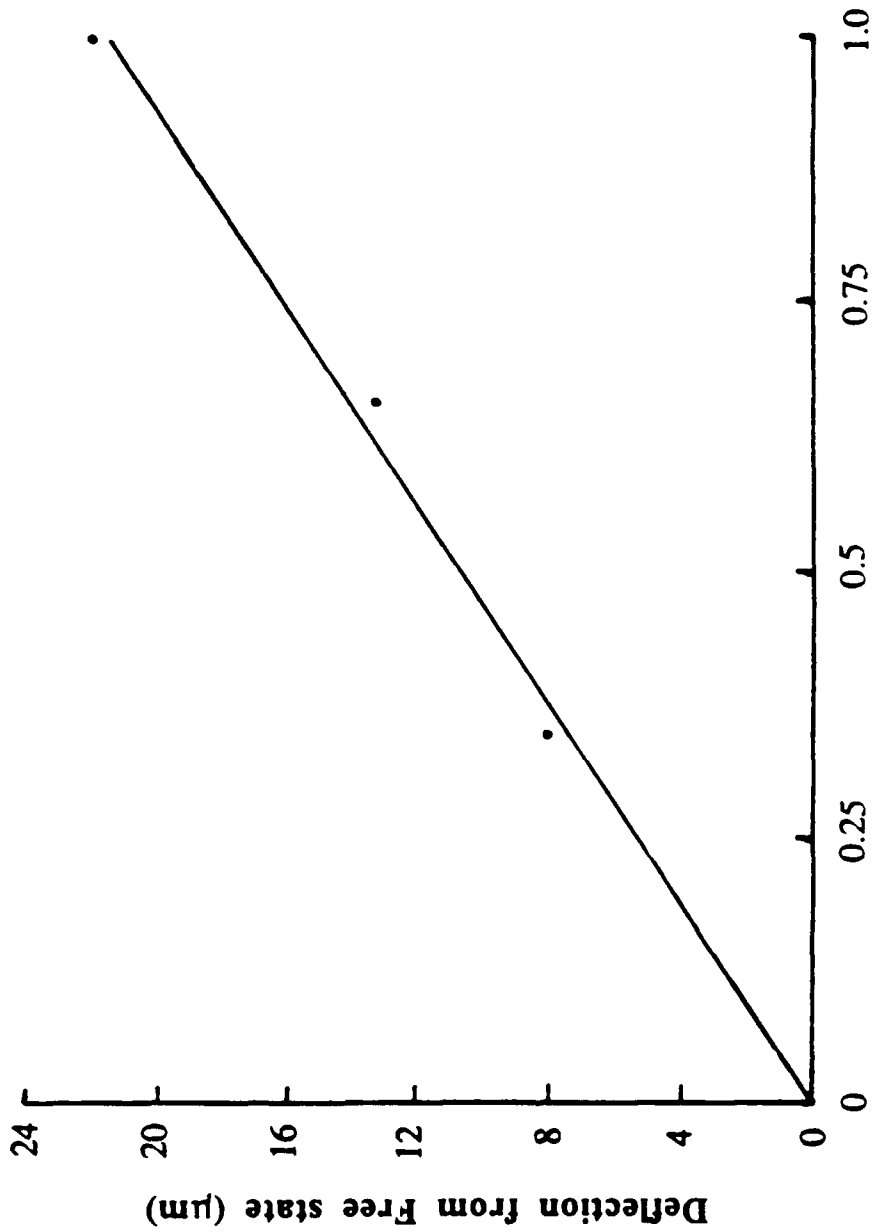



Fig. 8-2 Bow dependence on film coverage area.

chapter we will describe characteristic results of (1) the selective etching of GaAs on Si samples (2) the selective growth of GaAs on a partly $SiO_2$ masked Si substrate.

## 8.2 Experimental

The GaAs/Si samples were grown by MBE using a two-step process previously reported. The thickness of the epitaxial layers were 2.5 μm. Epitaxial layers were patterned with edges paralled to <110> directions by using standard photolithography techniques followed by a 1: 1: 5 $NH_4OH$: $H_2O_2$: $H_2O$ etch (GaAs removal rate ~ 2 μm/min.) The mask is 30 μm x 30 μm square separated by the 20 μm wide stripe of unmasked area. Both etched and as-grown GaAs-on-Si samples were annealed under an overpressure of Arsine in the metalorganic chemical vapor deposition (MOCVD) reactor at 830 °C for 50 min. followed by slow cooling (10 °C/min.).

Transmission Electron Miscopy (TEM) was used for the structure characterization. Cross-sectional TEM observations were performed on a Hitachi-800 (200 KV), using the conventional two beam diffraction technique.

The epitaxial GaAs was also investigated by double crystal X-ray diffraction using a Rigaku model diffractometer with a (400) rocking curves. From the full width at half-maximum of the GaAs (400) peak, we can make an approximate assessment of defect density in the GaAs. If the mosaic GaAs is assumed to consist of many subcrystals with a Gaussian distribution of orientations, the upper bond on the dislocation density is given by[90]

$$D \leq FWHM^2/9b^2 = 4.1 \times 10^2 \text{ cm}^{-2} (\text{FWHM/arsecond})^2 \qquad (8.3)$$

where b is the dislocation of Burger's vector, $a_o/\sqrt{2}$, for GaAs.

X-ray topography, where a Lang camera was used with Cu Kα1 radiation, was also utilized to study the defects density.

## 8.3 Results and discussion

The cross-sectional TEM micrograph of conventionally furnace annealed patterened GaAs on Si samples for g=2-20 and g=111 are shown in Fig. 8-3 and 8-4. High crystal quality of GaAs epilayer on Si has been achieved after this promising defect reduction procedure. Threading dislocation is the only defect revealed in the GaAs epilayer. A well defined dislocation network are confined within a 1 μm region above the GaAs/Si interface. Moreover, it is also shown that a dislocation free zone within 1 μm beneath the GaAs top surface exist. This is the best result that has been reported so far without using any intermediate defects confined layer.

A comparative study was performed by using double crystal X-ray diffraction. Table 8-1 demonstrate the X-ray rocking curve results for the annealing effect on both patterned and unpatterened GaAs on Si. The full width at half-maximum (FWHM) of GaAs (400) peak data can demonstrates the effectiveness of the selective etching-annealing combined technique. For samples with patterning after annealing the FWHM values decrease to 20%. There is only a 6.55% decrease for unpatterned GaAs on Si samples. The patterned-annealed sample had a FWHM of 170" indicating a dislocation density of less than $1x10^7/cm^2$. By considering the edge effect , the patterned GaAs epilayer should be much less than $1x10^7/cm^2$ .

The selective area epitaxy of GaAs on a partly $SiO_2$ masked Si substrates from Spire corporation was also used for comparisive study. Fig. 8-5 shows the cross-sectional TEM micrograph of a selective area (100 $\mu m^2$) grown sample. There exists higher defects density compared to selectively etched sample (Fig. 8-3 and 8-4). This is due that the epitaxial GaAs coverage area is larger than that of selective etching GaAs on Si samples. It

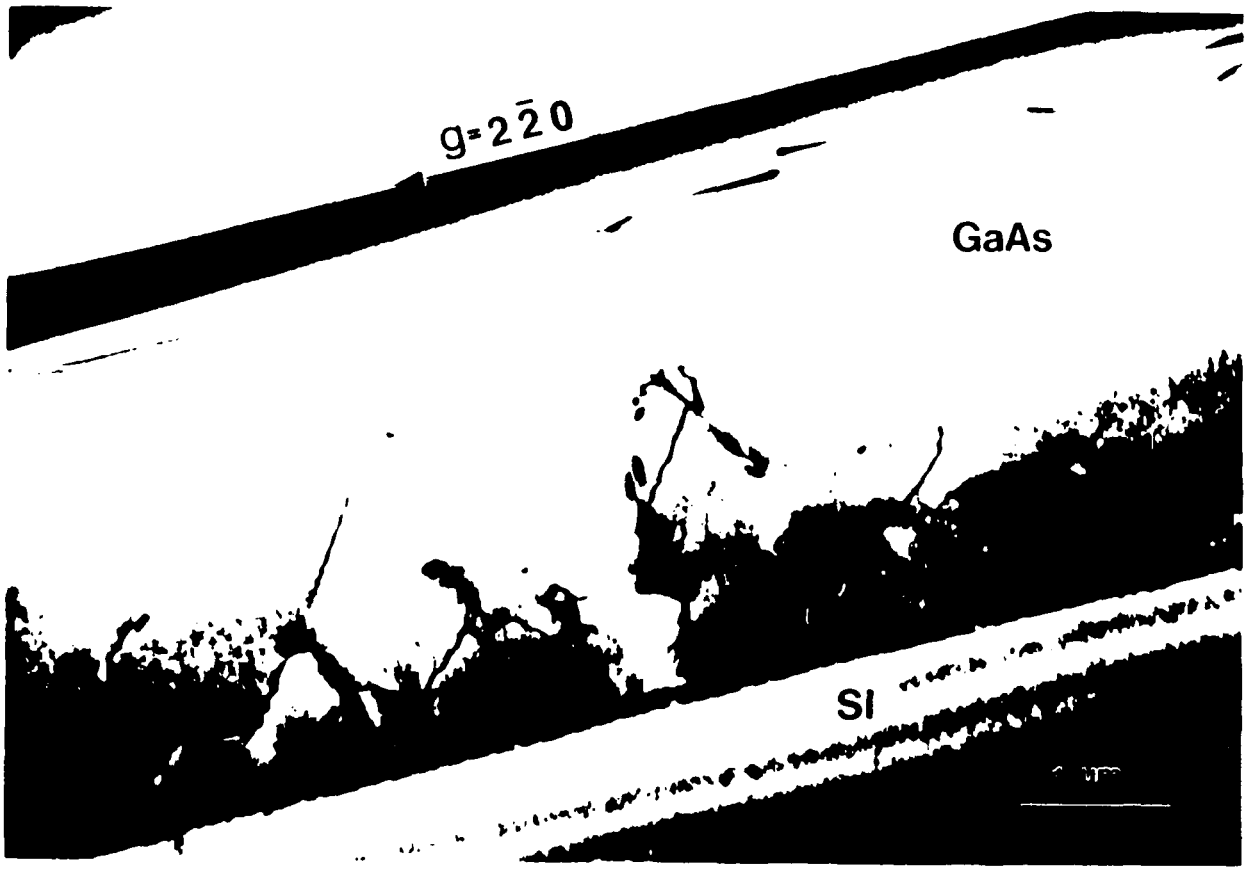



Fig. 8-3 Cross-sectional transmission electron micrograph of GaAs on Si sample after selective etching and annealing.

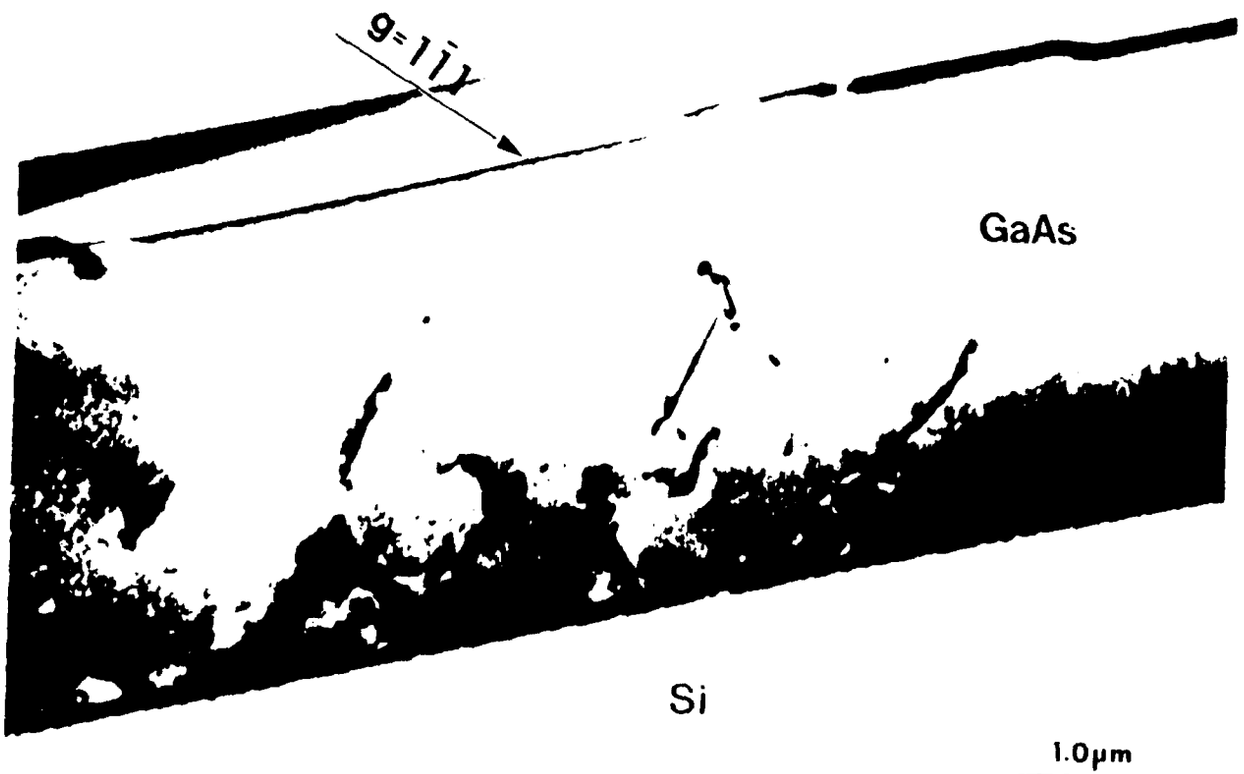



Fig. 8-4 Cross-sectional transmission electron micrograph of GaAs on Si sample after selective etching and annealing.

| | before annealing | after annealing |
|---|---|---|
| | FWHM (sec.) | FWHM (sec.) |
| with etching | 212.5" | 170" |
| without etching | 209.4" | 195.8" |

Table 8-1 A comparative double crystal X-ray rocking curve results for the annealing effect on both patterned and unpatterned GaAs on Si substrate.

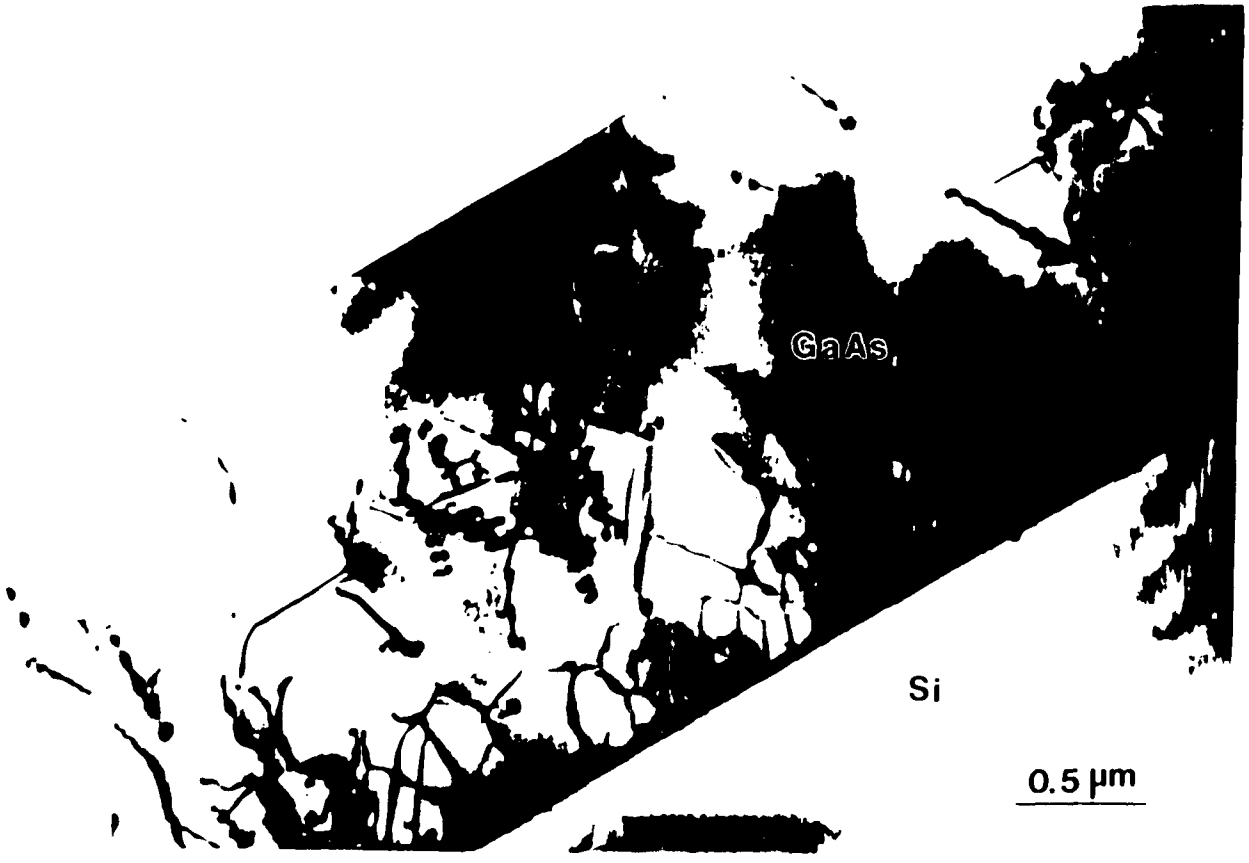



Fig. 8-5 Cross-sectional TEM micrograph of the selective area grown GaAs on Si sample.

has been reported that there is a technique limitation for selectively epitaxial gowth of GaAs on the smaller window size[90]. However, Fig. 8-5 shows better crystal quality than that of as grown GaAs on Si which has been reported in Chapter 3. This result is not unexpected due to the decrease of residual thermal stress by area shrinkage.

## 8.4 Summary

In conclusion, we have demonstrated the stress in patterned GaAs grown on Si substrate is decreased as the film coverage area decreases. Thus, for small geometries, stress in GaAs epilayer can be relieved, and this will open the possibility for having more sucessfully improved heteroepitaxial crystalline quality. After conventional furnace annealing/slow cooling the patterned GaAs on Si sample, a well defined dislocation network was found to confined within the 1 μm region above the GaAs/Si interface. There also exists a dislocation free zone within 1 μm beneath the GaAs top surface. Moreover, we have found a significant decrease in the FWHM for patterned GaAs epilayer grown on Si substrate after annealing. The decrease in FWHM can be attributed to the reduction of dislocation density.

# 9. CONCLUSIONS

(1) Both conventional furnace annealing/slow cooling and rapid thermal annealing were effective to eliminate microtwins and stacking faults. However, the conventional furnace annealing/slow cooling showed more promising results in terms of dislocations reduction. This conventional furnace annealing reduces dislocation density to about high $10^7$ $cm^{-2}$.

(2) The maximum critical thickness of strained-layer superlattices from our calculation is function of the density of bent-over threading dislocation. By considering the high density of grown-in threading dislocations in GaAs epitaxial layer on Si substrate our calculation expects a much higher maximum critical thickness than that of Van der Merwe's, Matthews, and People and Bean's predictions.

(3) The thermally activated nature of the effectiveness of strained-layer superlattices in blocking threading dislocations has been predicated by our energy equilibrium model. From our energy equilibrium calculation the minimum critical thickness of strained-layer superlattices was predicted as a function of processing temperature.

(4) It has been shown that $In_xGa_{1-x}As$-$GaAs_{1-y}P_y$ (y=2x) is an appropriate and highly effective buffer layer for reducing dislocations originating at GaAs-Si interface. The SLS structure also permits high values of strain to be employed without the SLS generating dislocations of its own. However, the effectiveness of the SLS depends on the density of dislocations.

(5) Several interaction between the strain field of the SLS [ $In_xGa_{1-x}As$-$GaAs_{1-y}P_y$ (y=2x)] and the threading dislocations in GaAs grown on Si substrate were observed. Favorable conditions for dislocation reduction were realized when (i) the dislocation is bent at the SLS interface and propagate to the sample edge, (2) two dislocations interact to cancel each other by forming a loop, and (iii) two dislocations react to form a third one at a node.

(6) The effectiveness of SLS [ $In_xGa_{1-x}As$-$GaAs_{1-y}P_y$ (y=2x)] in blocking threading dislocations was significantly improved by employing intermittant annealing during and/or post the SLS growth. The thermal energy from annealing provided the energy to overcome the energy barrier for threading dislocations to have a stable misfit dislocation segment glide along the SLS interface.

(7) A technique combing selective atching and conventional furnace annealing/slow cooling sucessfully improved heteroepitaxial GaAs crystalline quality on Si substrate. After conventional furnace annealing/slow cooling the patterned GaAs on Si sample, a well defined dislocation network was formed to confined within 1 μm region above the GaAs/Si interface. There also exists a dislocation free zone within 1 μm beneath the GaAs top surface.

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# Appendix I

## Interactions of Dislocations with SLS

This part of Dr. Yamaguchi's Ph.D. deals with the critical layer thickness for a single strained layer, followed by that of multiple layers. The interaction of dislocations with strained layer superlattices will then be discussed.

## A-1. CLT for a single layer

The value of the critical layer thickness for a single strained layer of GaAsP (GaP = 0.15) was experimentally determined. XRT was employed to examine the coherency of the interface between the substrate and the epitaxial films. XRT was first taken on the substrate prior to the growth. The growth of the GaAsP layer was performed in a stepwise fashion with each step resulting in the deposition of a controlled thickness added to the previously existing film. The interface between the ternary layer and the GaAs bulk was characterized at each step by transmission XRT. Figures A-1(a) to A-1(d) show the XRT micrographs taken from the substrate alone and from the corresponding area of a GaAsP film whose thickness was increased in steps. The presence of threading dislocations in the GaAs substrate is shown in Fig. A-1(a). For a thin GaAsP approximately 600 Å thick, only the threading dislocations in the substrate were observed. When the GaAs film thickness was increased to 900 Å, a few generation sites for misfit dislocations appeared near the sample edge as indicated by arrows in Fig. A-1(b). The number of these generation sites increased as the thickness of the GaAsP film was further increased to 1200 A as indicated by arrows in Fig. A-1(c). When the thickness reached 1600 Å, misfit dislocations were formed from these generation sites indicating the process of glide at

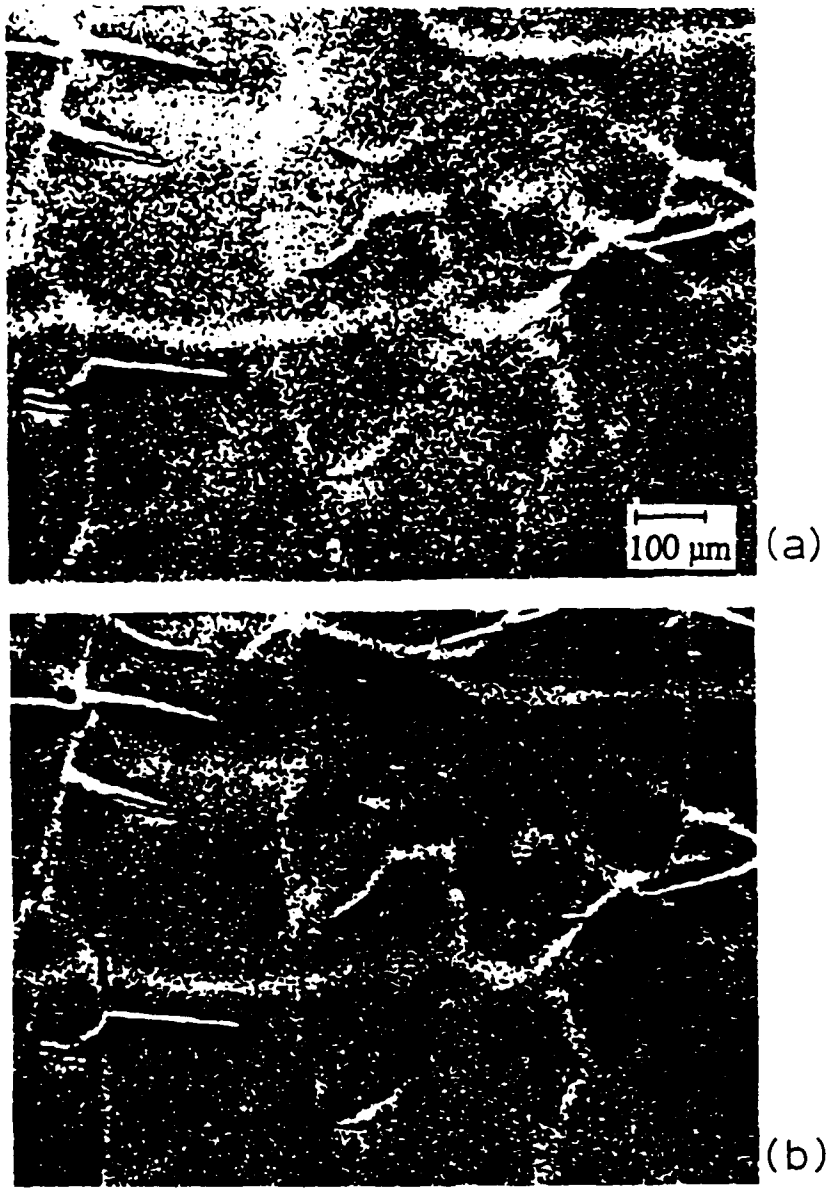



Figure A-1 X-ray topographs showing generation of misfit dislocations in epitaxial GaAsP (GaP≅0.15) layer. The layer thickness, h, was increased in a stepwise manner: (a) GaAs substrate; (b) h≅900 Å; (c) h≅1200 Å; (d) h≅1600 Å. Generation of dislocations was first observed in (b) as indicated by arrows.

(c)

(d)

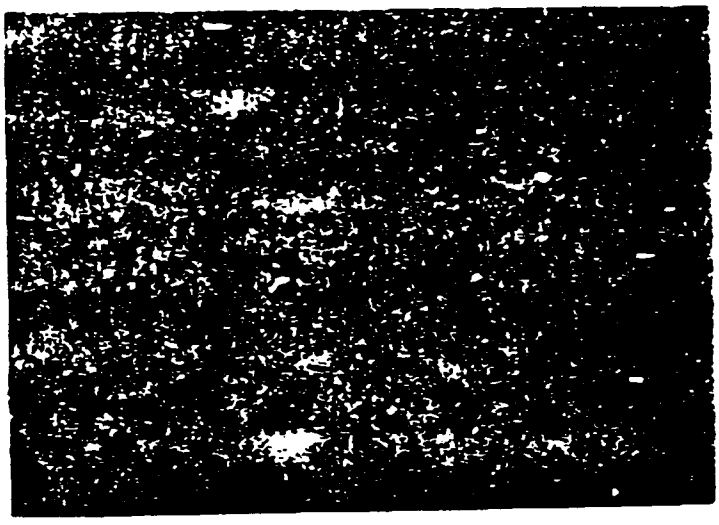
Figure A-1 (contined.)

the GaAsP/GaAs interface as shown in Fig. A-1(d). In order to ascertain that the nucleation spots were not introduced by any defect such as adsorbed impurity species caused by the exposure to air during XRT, a series of GaAsP (GaP=0.15) was repeated without interrupting the growth. The XRT taken on these samples confirmed that misfit dislocations were observed on the layers with the thickness greater than $\approx$ 900 Å. From these observations, it is concluded that the value of the CLT for the onset of misfit dislocations in a GaAsP (GaP - 0.15) single layer is approximately 900 Å. This value is a few times higher than the value predicted for a SLS by Matthews and Blakeslee and approximated one fifth of that determined by People and Bean.

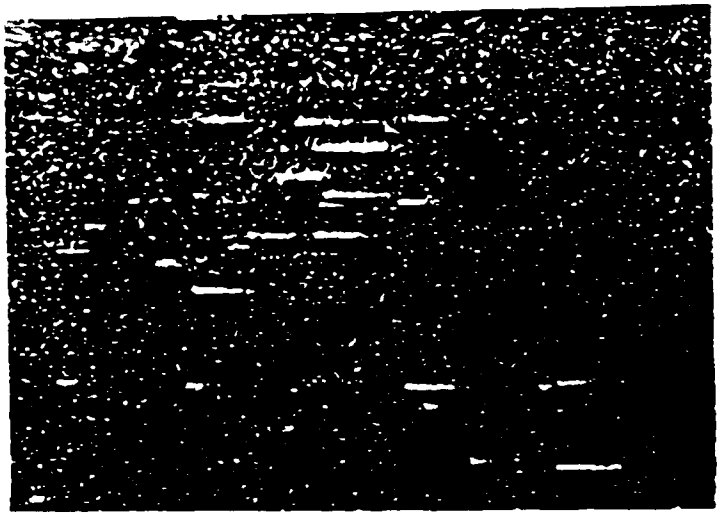
A series of single strained layers of InGaAs (InAs = 0.08) is grown to confirm the above results. This composition give the same strain level as GaAsP on GaAs but with compressive strain. Figures 1-2(a) through (d) show X-ray topographies taken at four samples with different layer thicknesses. Similar spots as seen in Fig. A-1 are shown in Fig. A-2(a) where the layer thickness is approximately 1000 Å. Higher density of such nucleation sites where line defects are starting to form are observed in a 1500 Å thicken layer A-2(b). In layers with the thickness 2000 Å and 2500 Å each, dislocations are no longer discernible as shown in Figs. A-2(c) and (d).

## A-2. CLT for a SLS

The onset of misfit dislocations in SLS's constructed of InGaAs and GaAsP epitaxial layers with equal thicknesses was investigated. Alternate GaAsP and InGaAs layers are under compression and tension such that the SLS as a whole is lattice-matched to the GaAs substrate. This choice of a SLS material system allows one to study critical thickness phenomena for the

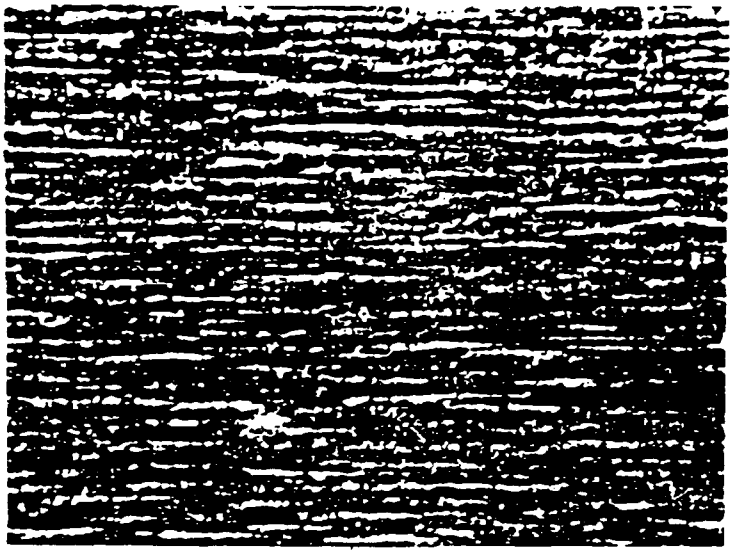


(a)



(b)

Figure A-2 X-ray topographs showing the generation of misfit dislocations in eptiaxial InGaAs (InAs=0.08) layers. The layer thicknesses are : (a) ≅1000 Å; (b) ≅1500 Å; (c) ≅2000 Å; (d) ≅2500 Å. The nucleation sites of misfit dislocations similar to those observed in Fig. 3-5 are seen in (a).



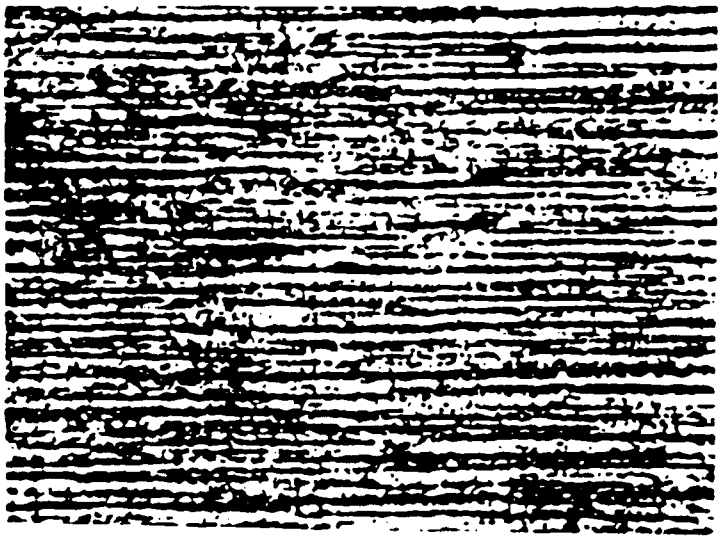




Figure A-2 (continued.)

individual layers of the SLS. Since the strain level with this SLS is a constant, misfit dislocations are not expected to form as the number of the SLS periods is increased. EBIC was used to determine the value of the CLT for the constituent layers of this SLS structure. By utilizing XRT one can reveal misfit dislocations located at the GaAs/SLS interface easily. This is due to the fact that the intensity of the beam diffracted by the GaAs buffer and substrate is strong enough to give clear images of defects by Bormann effects. The satellite peaks, on the other hand, are too weak to project clear defect images. Therefore, XRT is not suitable for identifying misfit dislocations within a SLS.

Figure A-3 shows EBIC images of InGaAs/GaASP SLS's whose period thickness was varied from 500 to 800 with the compositions fixed at InAs - 0.08 and GaP = 0.16. The structures of the SLS's are listed in Table A-1. In Fig. 3-7 (a) where the SLS period is 500 Å, even with the acceleration voltage of 25 kV which is sufficient to probe the SLS, no misfit dislocations were observed, indicating that the ternary layer thickness did not exceed the CLT. As shown in Fig. A-3(b), when the period thickness was increased to $\cong$550 Å misfit dislocations increased for the SLS with the period thickness of 800 Å as shown in the Fig. A-3(c). From these observations the critical value of the period thickness for a misfit of 0.6% is estimated to be approximately 550 Å. Therefore, the value of the CLT for each layer of the SLS is determined to be approximately 280 Å, which is in reasonable agreement with the Matthews' and Blakeslee's model.

Photoluminscence measurements made on SLS's with different thicknesses support the EBIC results, Curve (a), (b), (c) and (d) in Fig. A-4 show PL spectra obtained at 77 K from SLS's with the period thickness of 500 Å, 600 Å, 700 Å, and 850 Å, respectively, The

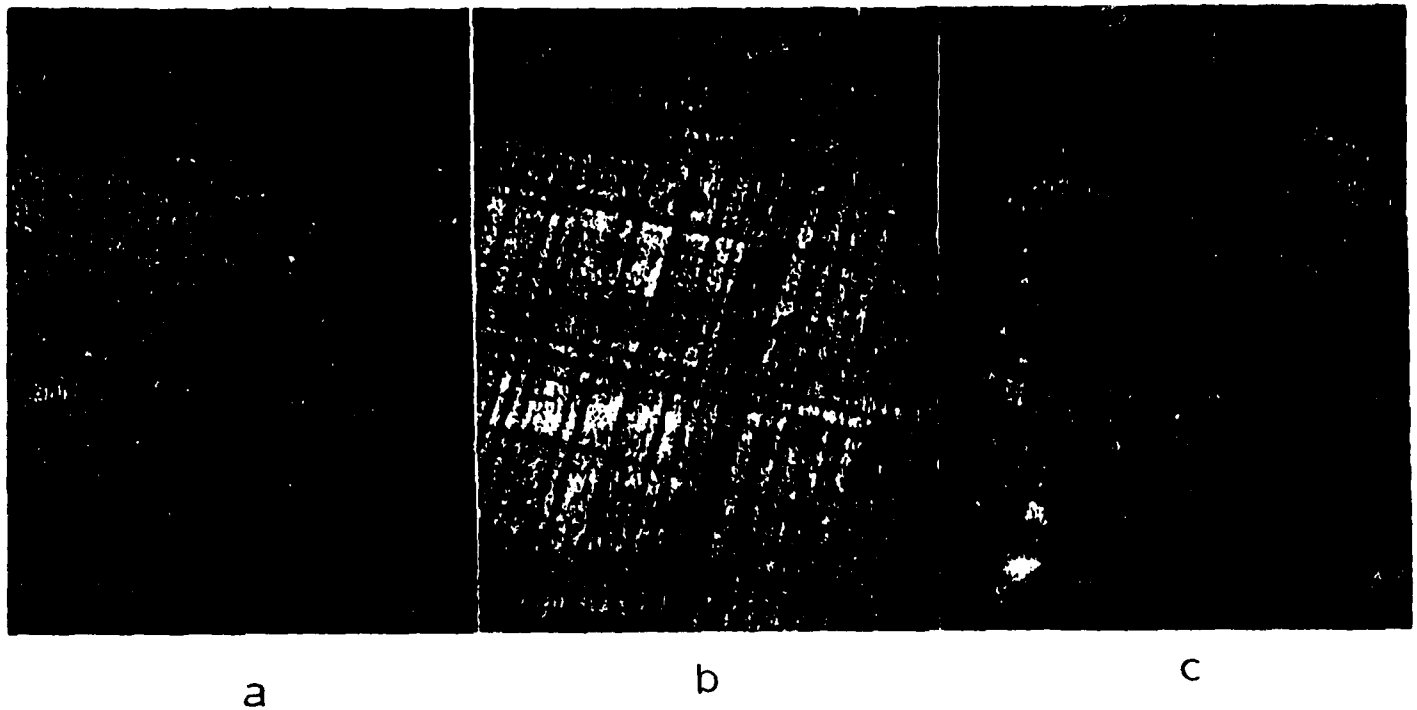



Figure A-3 EBIC micrographs showing at the interface of three SLS's. The period thicknesses, $d_p$, are : (a) 513 Å; (b) ≅550 Å; (c) ≅800 Å.

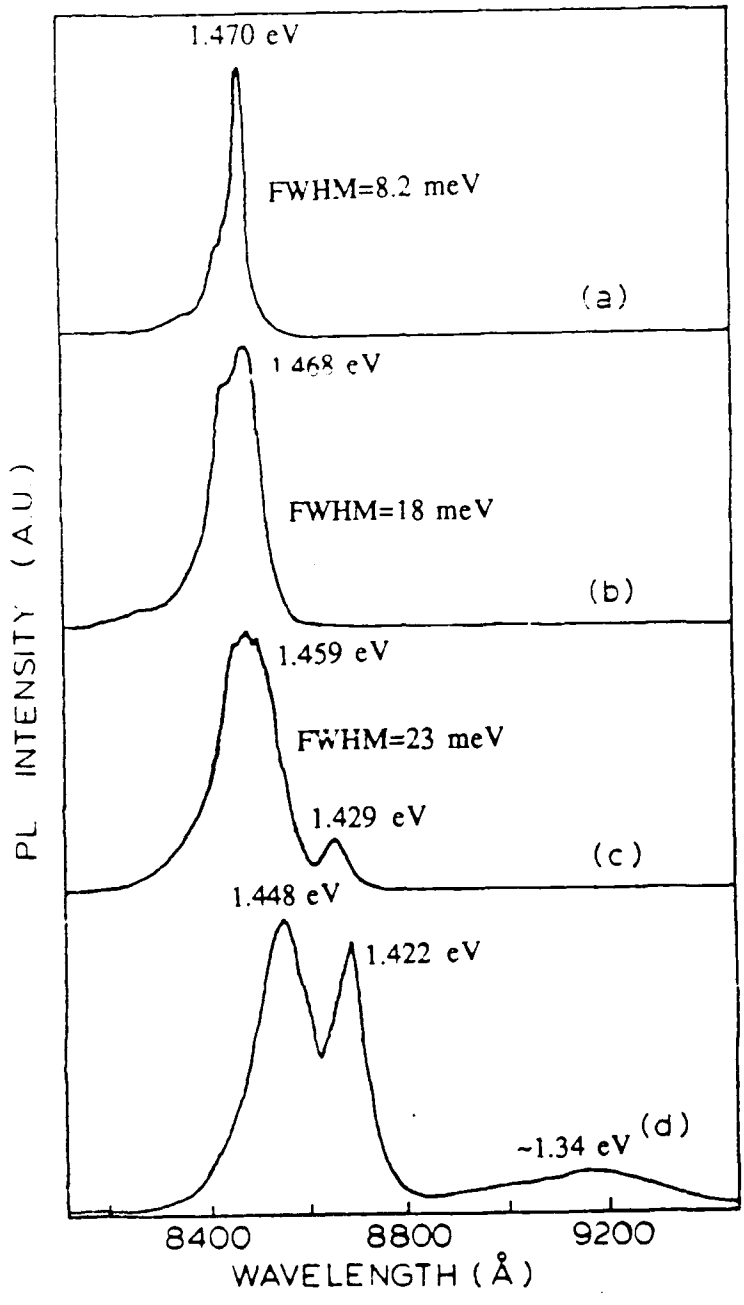



Figure A-4 77K PL spectra of SLS's with period thickness : (a) 470 Å; (b) 600 Å; (c) 700 Å; (d) 850 Å.

structures of the SLS's are tabulated in Table A-1. SLS's with the layer thicknesses greater than the CLT predicted by Matthews and Blakeslee show considerably broader peaks than those with the layer thicknesses smaller than CLT. The peak about 26-30 meV lower than the highest energy peak which only seen in the two SLS's with larger layer thicknesses may be due to the compositional fluctuation in the InGaAs layers. These SLS's were grown before the gas handling system was modified and such fluctuation corresponds to about 19-25% higher InAs composition. The very broad peak at about 1.35 eV, which is only present in the SLS with the largest layer thicknesses, may be related to the defect levels created by the misfit dislocations as reported by Joyce et al. They have studied InGaAs/GaAs (InAs-0.17) single quantum wells with varying thicknesses and identified broad emission bands related to interface defects, most likely due to misfit dislocations.

### A-3 Dislocation Configuration in SLS

In the proceeding two section the onset of misfit dislocations was discussed in two kinds of structures. A SLS with its period thickness above the CLT is studied in detail by two techniques, XRT and EBIC. The SLS consists of 10 periods of GaAsP (GaP=0.16) and InGaAs (InAs=0.08) and the period thickness is 1000 Å which exceeds the value of the CLT for the mismatch. As a result of the layer thickness exceeding the CLT, misfit dislocations were generated in the SLS. Several types of dislocations have been observed and are schematically illustrated in Fig. A-5. In this figure, curves 1 through 4 depict threading dislocations originating from the substrate and bending due to the misfit strain whereas curve 5 depicts a dislocation unperturbed by the SLS. Curve 6 in the figure shows a dislocation half loop generated in the SLS because of the layer thickness is in excess of the CLT.

Table A-1. InGaAs/GaAsP SLS structures.

| Sample | InAs (%) | GaP (%) | No. Periods | Period Thickness (Å) |
|---|---|---|---|---|
| A | 8 | 16 | 20 | 513 |
| B | 8 | 16 | 6 | 550 |
| C | 8 | 16 | 6 | 800 |

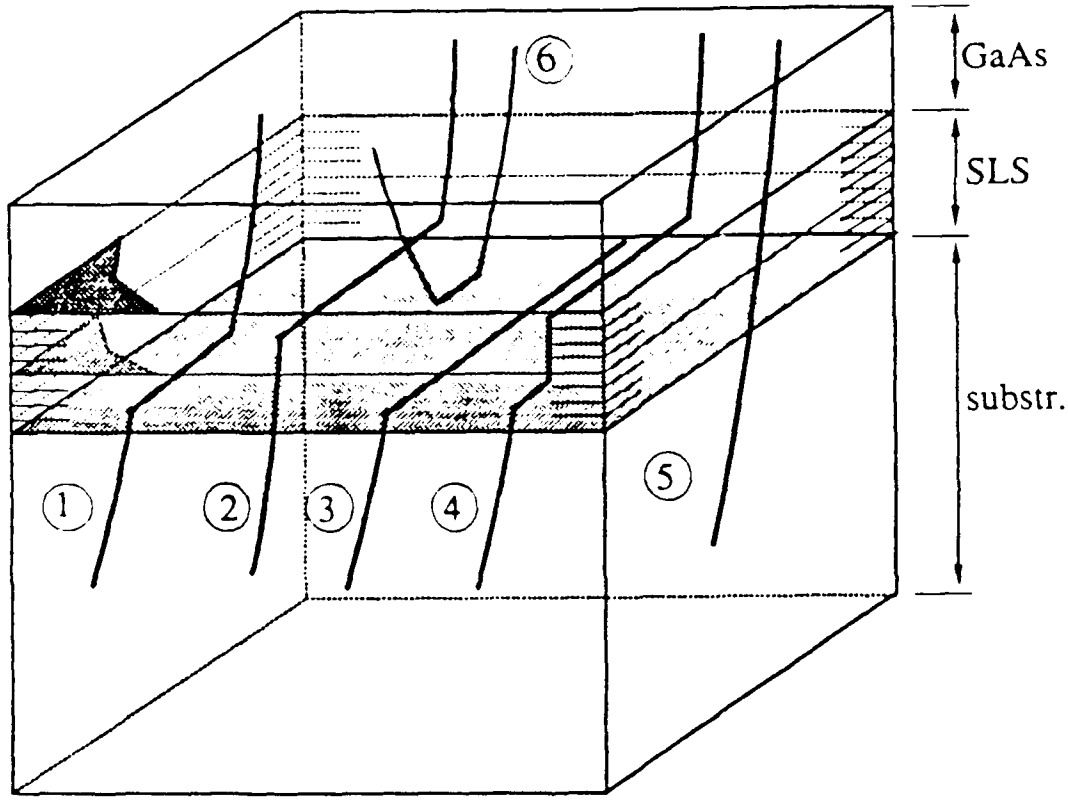



Figure A-5 Schematic representation of dislocation configurations in a SLS. Curve 1 through 5 shows dislocations originated from the substrate whereas curve 6 shows a dislocation generated at the SLS/GaAs interface.

The strain field due to lattice mismatch at the interfaces forces the threading dislocations to bend. When the dislocations are bent at the interface between the SLS and the GaAs buffer layer, XRT will identify both threading dislocation sand corresponding misfit segments as indicated by arrows in Fig. A-6(a). In contrast, EBIC shows only the dark line representing the bent segment of the dislocation as shown in Fig. A-6(b). The dark spot at the end of the misfit segment shows the point where the dislocation has escaped to the surface. The three dimensional contour of this dislocation is given by curve 1 in Fig. A-5. The dislocation depicted by curve 2 in Fig. A-5 schematically illustrate a dislocation that is bent within the SLS. In order to remove the dislocation, the interfacial strain must be large enough to drive the dislocation to the edge of the wafer as schematically illustrated by curve 3 in Fig. A-5.

Figures A-7(a) and (b) illustrate the situation where a dislocation has been prevented from propagating along the GaAs/SLS interface. The dislocations thread upwards and band at the interfacial plan of the SLS due to the strain field and finally emerge from the free surface. In XRT, Fig. A-7(a), only the misfit segment at the GaAs/SLS interface denoted by $M_1$ is observed. The result from EBIC in Fig. A-7(b) shows that the dislocation was bent again at a SLS interface after threading upwards from the GaAs/SLS interface to exit at the surface. The misfit segment lying at the interface within the SLS is indicated by arrow $M_2$ in the micrograph. The distance that this dislocation propagated along the SLS interface is only about 35 $\mu$m. Some dislocations, however, were found to travel more than a few hundred microns in the same sample. The schematic configuration of this dislocation is given by curve 4 in Fig. A-5. There are some dislocations found to penetrate through the SLS without being bent. This type of dislocation is denoted by an arrow in Fig. A-8. The threading dislocation in the substrate is

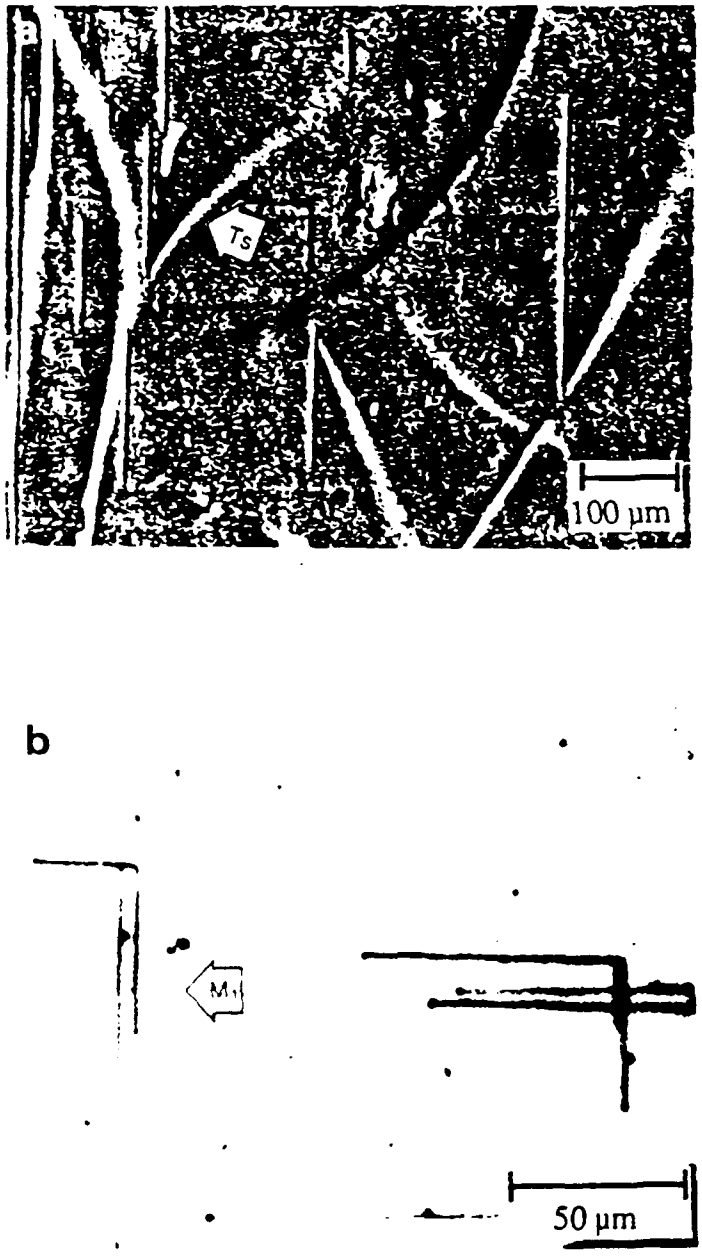



Figure A-6 XRT (a) and EBIC (b) micrographs showing dislocations bent at the GaAs/SLS interface as indicated by arrows. These types of dislocations are schematically illustrated by curve 1 in Fig. 3-9.

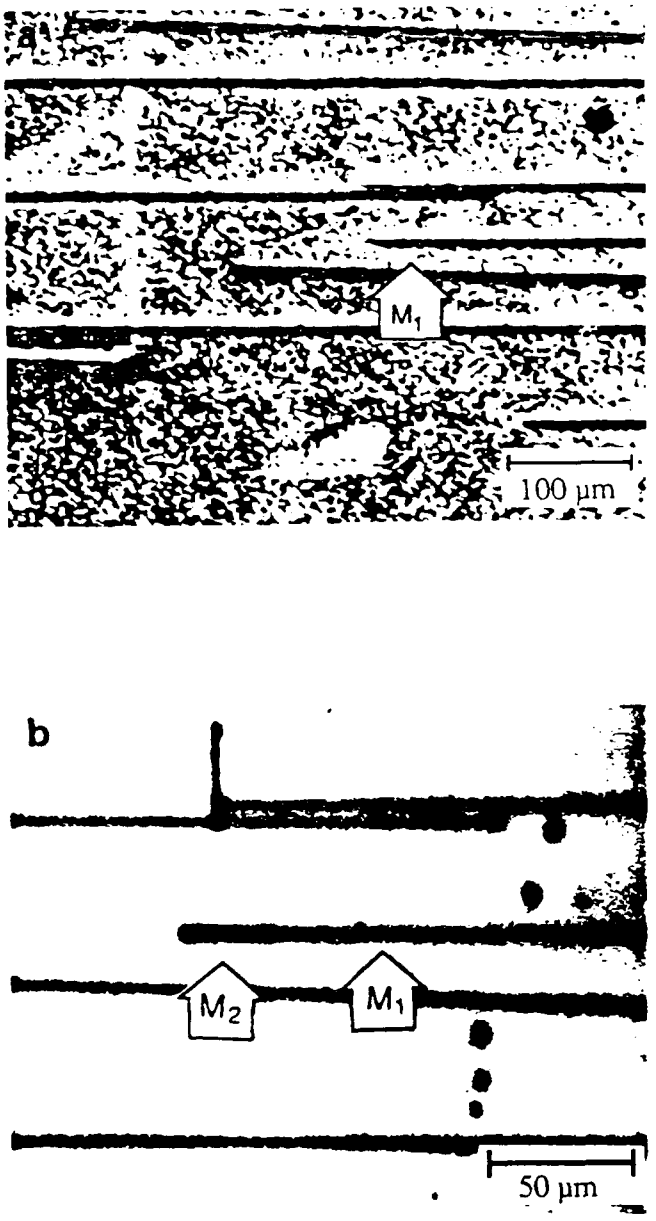



Figure A-7 XRT (a) and EBIC (b) micrographs showing a dislocation which is repeatedly bent and threades upwards in the SLS. Note that the misfit segment within the SLS, indicated by arrow M2, is invisible in XRT. This type of dislocations is depicted by curve 4 in Fig. 3-9.

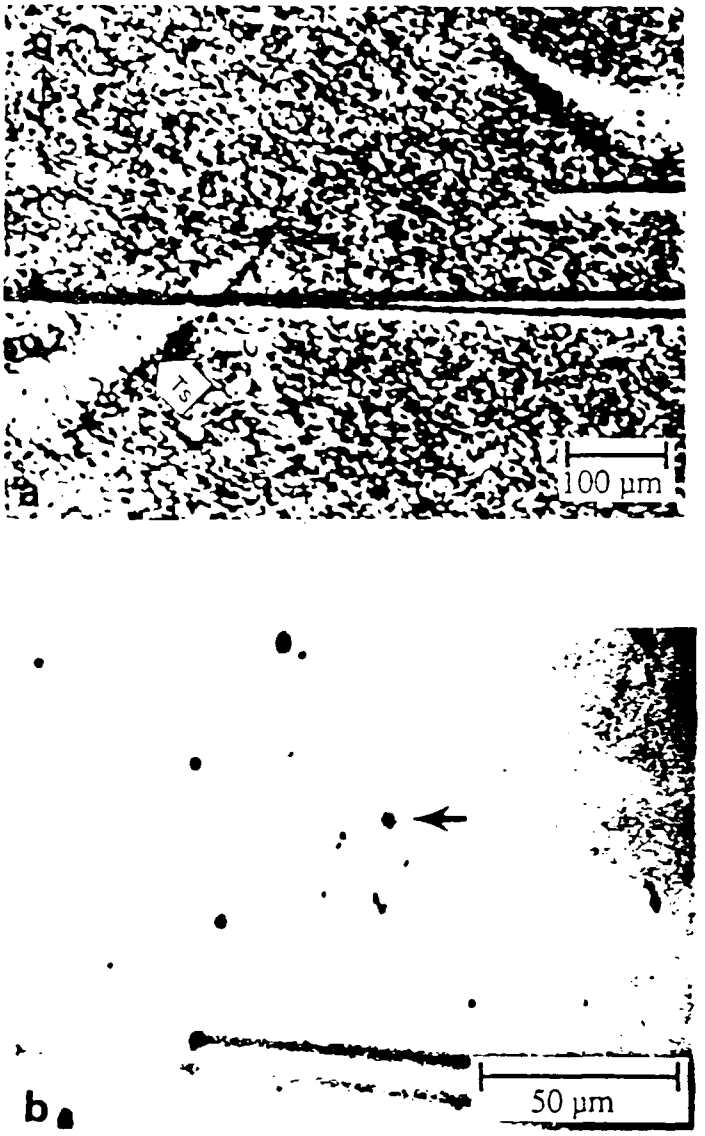



Figure A-8 XRT (a) and EBIC (b) micrographs showing a threading dislocation which penetrated through the SLS without being bent. This type of dislocation configuration is schematically illustrated by curve 5 in Fig. 3-9.

shown in XRT, Fig. A-8(a), whereas the dark spot indicating that the dislocation threaded through the SLS without being bend is seen in EBIC, Fig. 3-12(b). Curve 5 in Fig. A-5 illustrates this kind of dislocation. A misfit dislocation generated as a result of lattice mismatch was observed in the SLS. XRT shown in Fig. A-9(a) indicates the misfit dislocation lies at the GaAs/SLS interface and did not originate from a substrate dislocation. EBIC image shown in Fig. A-9(b) reveals two emerging spots of this dislocation at the surface as indicated by an arrow. Curve 6 in Fig. A-5 corresponds to this type of misfit dislocations. These type of dislocations were observed to cross-slip in the SLS. XRT micrograph shown in Fig. A-16(a) indicates a misfit dislocation marked by an arrow. Curve 6 in Fig. A-5 corresponds to this type of misfit dislocations. These type of dislocations were observed to cross-slip in the SLS. XRT micrograph shown in Fig. A-16(a) indicates a misfit dislocation marked by arrow $M_i$ generated at the GaAs/SLS interface. It is seen in the EBIC micrograph, Fig. A-10(b), that this dislocation bent along a direction perpendicular to the segment $M_i$ after threading up in the SLS. The dark spot at the other end of this misfit dislocation indicates that this dislocation finally escaped to the surface. As of yet there is no clear understanding why both types of dislocations are present, in particular, those that penetrate the SLS and those that are bent by the interfacial strain.

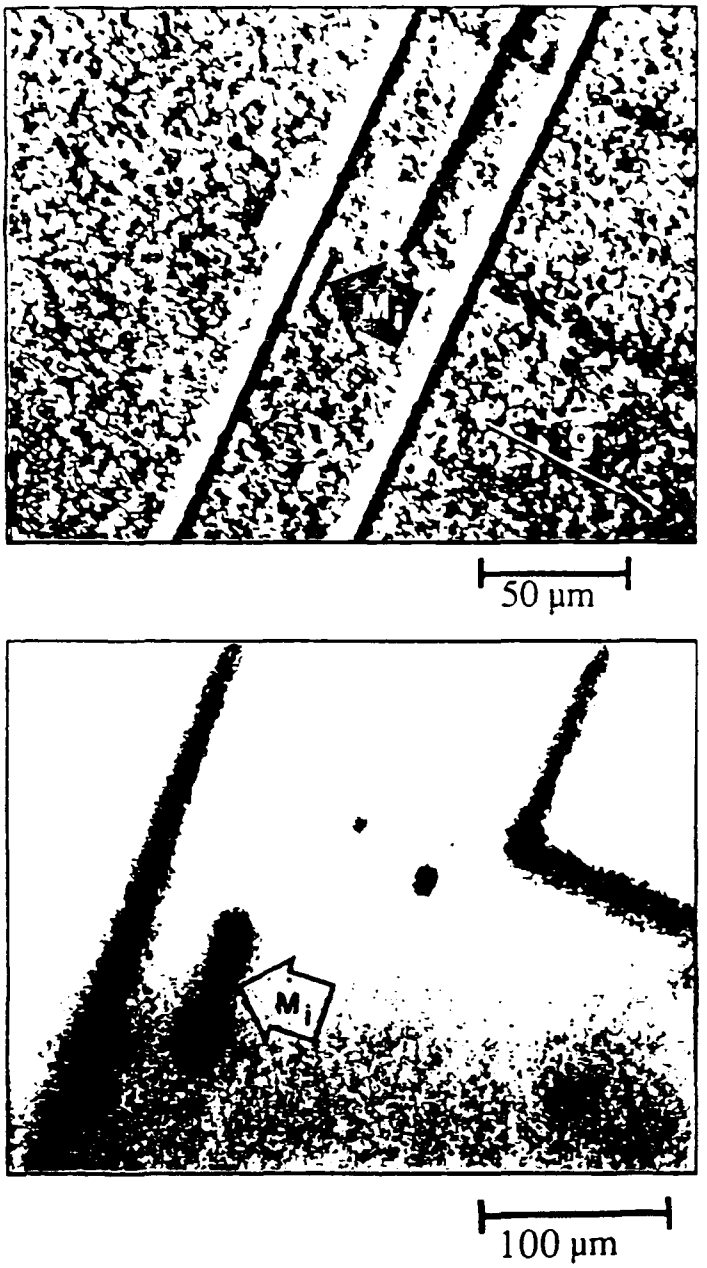



Figure A-9 XRT (a) and EBIC (b) micrographs showing a misfit dislocation generated at the GaAs/SLS interface.

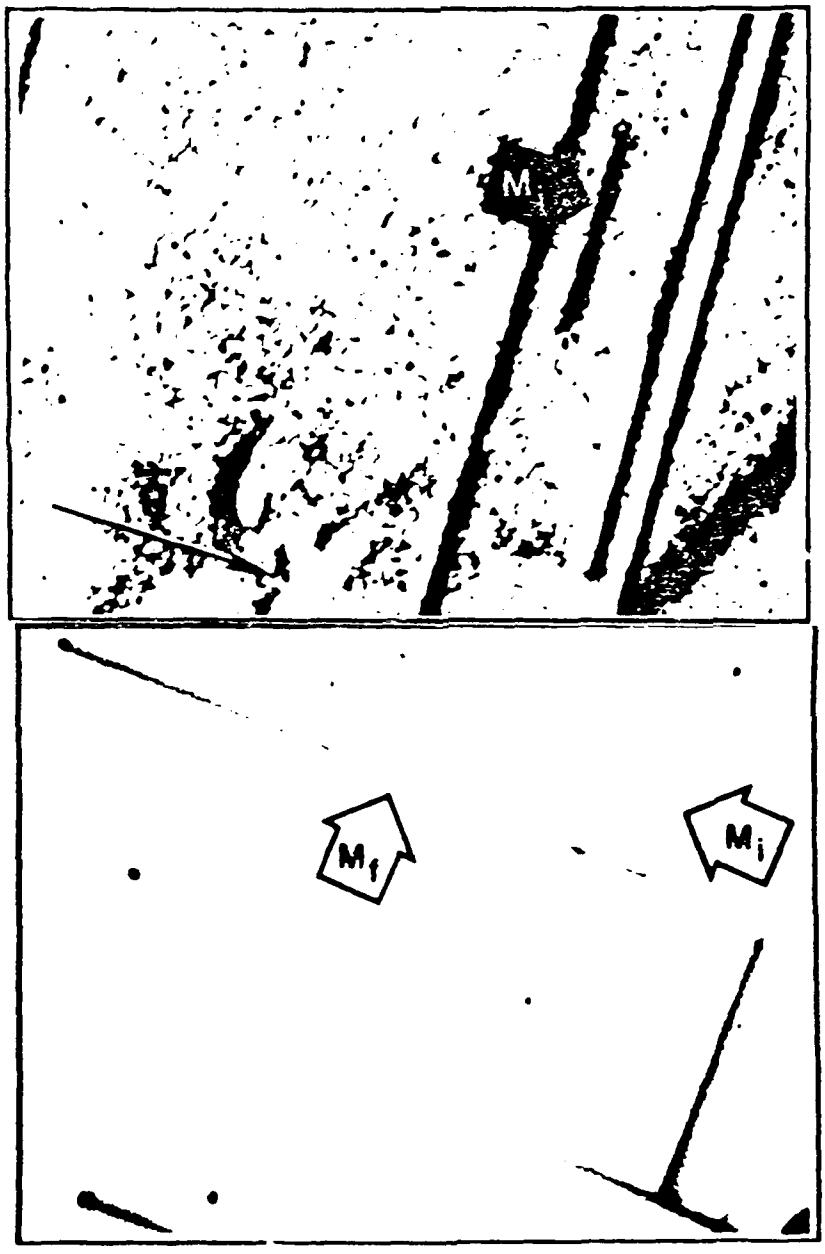



Figure A-10 XRT (a) and EBIC (b) micrographs showing a misfit dislocation generated at the GaAs/SLS interface and cross-slipped in the SLS.