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Asynchronous Design for Parallel Processing Architectures

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The objective of this research is to provide an interconnect synthesis methodology which facilitates a modular design approach without compromising the global performance. The main tasks of this effort will be the development of the theory for optimal interconnect circuit synthesis from a high-level specification, with emphasis on testability and fault-tolerance asynchronous interface among concurrently computing hardware, and the application of this design methodology to physical implementations of parallel processing systems.

Progress:

In the past six months, we have continued our research of the testability of asynchronous control circuits, and studied the gate-level implementation of such circuits.

As described in the progress report of December 1990, we have addressed the problem of the testability for two areas of asynchronous design: speed-independent circuits and self "timed" circuits. Speed-independent circuits are designed to work independently of the gate delays in the circuits. "timed" circuits are designed to work assuming that each gate follows a minimum and maximum delay assumption. Our results show that if there are any single or multiple stuck-at-faults (SAFs) on any gate output, an hazard-free speed-independent asynchronous circuit will automatically halt [1,2]. This results yields a simple test of asynchronous control circuits for output SAFs: cycle through any sequence of input transitions, and if the circuit responds as expected, the circuit is output SAFs free; otherwise, the circuit is faulty.

There are other SAFs which will not automatically halt a circuit. Examples of non-halting SAFs are faults on a gate input node in a speed-independent circuit or faults on any non-primary input/output node in a "timed" circuit. We have developed theories which determine the testability of such faults and a procedure which detects those non-halting faults (not just SAFs in this case) which are established as testable by the theories, for both speed-independent and "timed" circuits [3].

Our testability study has provided much insight into the causes of hazards in asynchronous circuits and the means of synthesizing such circuits from a high-level specification. In addition to testability of asynchronous circuits, we are interested in providing a synthesis tool which will generate a gate-level implementation of a circuit suitable for a standard-cell or gate-array implementation. It has been shown that the arbitrary delay elements can be added to a hazardous "timed" design to create a hazard-free "timed" design from high-level descriptions. We investigated the synthesis of gate-level hazard-free circuits *without* added delay elements, because such elements are bound to degrade circuit performance.

We have developed a prototype synthesis system which uses heuristics to synthesize a non-optimal gate-level speed-independent circuit from a signal transition graph (STG) specification. We can handle only deterministic circuits at the moment, which are asynchronous circuits with no input conditionals. This is a promising beginning because other existing synthesis systems either provide circuits which use building blocks normally unavailable in gate-arrays or only provide Boolean equations which the designer has to map to a set of available gates. In the later case, the resulting circuit has to be tested for hazards, and if a hazard exists, has to be tweaked until a hazard-free implementation is found.

Future research for the next two quarters:

We will focus future research on the synthesis system, including optimization algorithms for speed-independent implementations, robustly testing them, and comparing synthesized circuits with published hand-optimized designs. In addition, we will incorporate timing information into the synthesis system to further optimize the circuit for performance.

On the synthesis side, we need first to prove that a gate-level speed-independent implementation exists for all legal STG specifications, and then to construct a generic algorithm that will generate the corresponding gate-level circuit. We are currently investigating a theoretical basis of the heuristics used in our synthesis system, to determine if the heuristics are sufficient to synthesize a gate-level speed-independent circuit for all legal STG specifications, and if not, to formalize algorithms such that such a circuit can be guaranteed. In addition we are developing algorithms which will optimize the circuit for area and speed, while maintaining the hazard-freedom of the circuit.

On the testability side, we will generalize our theories to cover non-SAFS, for example the stuck-open-faults and the bridging faults, and establish the testability properties and testing procedures for such faults. We also plan to study the testing strategies for large-scale asynchronous circuits, in which scan-path designs may prove more efficient.

References:

[1]. Peter A. Beerel and Teresa H.-Y. Meng, "Semi-Modularity and Self-Diagnostic Asynchronous Control Circuits", published in *Advanced Research in VLSI*, MIT Press, March 1991, and presented in the *Workshop of High-Level Synthesis*, March 1991.

[2]. Peter A. Beerel and Teresa H.-Y. Meng, "Semi-Modularity and Self-Diagnostic Asynchronous Control Circuits", submitted to *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, June 1991.

[3]. Peter A. Beerel and Teresa H.-Y. Meng. "Testability of Asynchronous "Timed" Control Circuits with Delay Assumptions", *28th ACM/IEEE Design Automation Conference*, June, 1991.

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1. Peter A. Beerel and Teresa H.-Y. Meng, "Semi-Modularity and Self-Diagnostic Asynchronous Control Circuits", presented at *The Fifth International Workshop on High-Level Synthesis*, and published in *Advanced Research in VLSI*, pp. 103-117, MIT Press, March, 1990.

2. Teresa H.-Y. Meng, Robert W. Brodersen, and David G. Messerschmitt, "Asynchronous Design for Programmable Digital Signal Processors", *IEEE Trans. on ASSP*, pp. 939-952, Vol. 39, No. 4, April 1991.

3. Teresa H.-Y. Meng, "Design OF Asynchronous Parallel Architectures", *Parallel Algorithms and Architectures for DSP Applications*, ed. M. Bayoumi, Kluwer Academic Publishers, April 1991.

4. Peter A. Beerel and Teresa H.-Y. Meng. "Testability of Asynchronous Self-Timed Control Circuits with Delay Assumptions", *Proc. 28th ACM/IEEE Design Automation Conference*, June, 1991.

5. Peter A. Beerel and Teresa H.-Y. Meng, "Semi-Modularity and Self-Diagnostic Asynchronous Control Circuits", submitted to *IEEE Trans. on CAD/ICAS*, June 1991.