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FAILURE MECHANISMS ON GaAs INTEGRATED CIRCUITS: ELECTROMIGRATION ON GaAs

General Electric Company

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13. ABSTRACT (Maximum 200 words)

The objective of this program was to investigate two aspects of electromigration on GaAs devices: 1) the rate of electromigration of typical metallizations on GaAs, and 2) the occurrence of electromigration assisted interdiffusion of the gate metal and the GaAs in GaAs FETs.

A life test was conducted, and the rate of electromigration was found to be influenced by the type of barrier metallization used. It was found that electromigration is no worse on GaAs than on silicon. It was found that interdiffusion of the gate metal into the GaAs was not significant at the test conditions used during the life test.

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"ELECTROMIGRATION ON GALLIUM ARSENIDE"

This contract resulted from a Program Research and Development Announcement in the area of Failure Mechanisms in GaAs. GE has investigated electromigration on GaAs. They compared substrate material (oxidized silicon vs GaAs), and barrier metal, and examined resistance and Schottky junction voltage changes. It had been hoped that use of existing equipment and set up from a previous electromigration experiment would improve the likelihood of success. This was not to be, because of problems with the equipment, particularly the boards in the life test oven which plagued this effort. In spite of these difficulties, some results have been obtained. No enhancement of electromigration rates was observed for the GaAs substrates, and a bamboo effect was apparent in the 1 micrometer wide gate metal lines. The barrier breakdown experiment produced less than desired results, and GE has recommended a follow on to the barrier breakdown experiment at temperatures in excess of 200C.

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Table of Contents

List of Figures

List of Tables

1 Background

The objective of this program was to investigate two aspects of electromigration on GaAs devices: 1) the rate of electromigration of typical metallizations on GaAs, and 2) the occurrence of electromigration assisted interdiffusion of the gate metal and the GaAs in GaAs FETs.

1.1 ELECTROMIGRATION ON GaAs

There have been few measurements of electromigration on GaAs reported and even fewer for refractory metal-gold metallization systems typical of GaAs FETs. However, accelerated life tests of power GaAs FETs have shown that electromigration can be an important failure mechanism in these devices.

Irvin and Loya[1] reported that low noise FETs under DC stress at 250° failed because of voiding in the gate fingers. The gate was of aluminum, but the gate bonding pad had a PtTiAu layer over the aluminum to prevent Au-Al intermetallic formation. The voids were believed due to Kirkendahl voiding resulting from Au-Al formation caused by the disruption of the PtTi barrier during ball bonding. However, since the voids occurred at the point of maximum current density and also where the current density gradient was maximum and was in the direction of the electron flow, it was suggested that electromigration played a role in the failure process. This was confirmed when it was observed that the median life was 3 to 10 times longer when the devices were aged at the same temperature without bias.

The void formation was apparently due to two mechanisms, electromigration and Kirkendahl voiding, with electromigration playing a major role. It is estimated that the

current density in the device tested was ~10^3-10^4 A/cm², a level well below that at which electromigration effects are expected to be important.

White et al[2] observed similar voiding in GaAs power FETs with aluminum gates and gold bonding wires. Later, White[3] showed that void formation occurred whether gold or aluminum wires were used, indicating that intermetallic formation is not necessary for the void formation and that electromigration is the dominant failure mode. Figure 1 compares the Arrhenius plots obtained by White for the samples with gold and aluminum wires. The activation energies for the two cases were different.

Drukier and Silcox[4] also reported that electromigration in the gate fingers was the dominant failure mode resulting from DC life testing of MSC power FETs with TiW-Au gate metallization. Likewise, Hughes Aircraft has reported that electromigration in the gates is a major failure mechanism in both Fujitsu and NEC power FETs. In contrast, Fukui et al[5] have reported no catastrophic failures in power FETs with aluminum gates

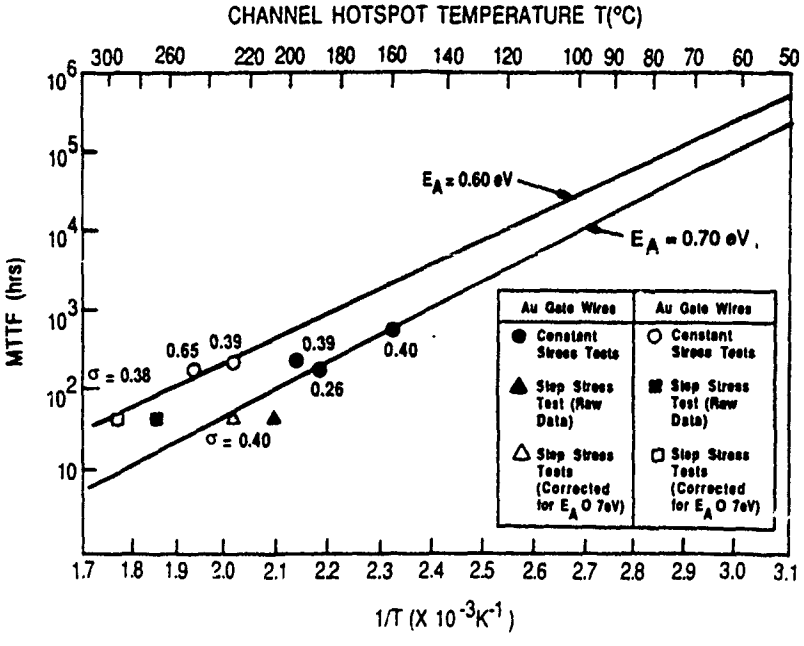

Figure 1. Arrhenius Plots for Both Al and Au Bond Wires to Al Gate Power FETs

with a silicon nitride coating when tested for as long as 3000 hours at 250°C. A current density of 2.5 x 10^5 A/cm^2 was used, and no voiding was observed.

Thus electromigration has been observed to be a potential failure mechanism in GaAs devices, and, because of the unexpected observation that gate finger voiding in GaAs devices appears to occur at very low current densities, there is reason to believe that the rate of electromigration may be larger for GaAs substrates than for silicon substrates. Davey and Christou[6] have emphasized the need for further research on this phenomenon. Three effects may contribute to this acceleration: 1) the gallium doping of the metal from the substrate may affect the rate of electromigration; 2) it may be related to the much higher thermal expansion coefficient; or 3) it may be related to the much lower thermal conductivity of the GaAs relative to Si. Since the relative thermal expansion of the metal and substrate can affect the residual stress in the film, it can also impact the electromigration process. The lower thermal conductivity can result in higher local temperatures and temperature gradients.

Few, if any, controlled electromigration experiments have been done using GaAs substrates. Because of its potential importance as a failure mechanism in GaAs microcircuits, as well as in discrete GaAs MESFETs, such experiments are needed.

1.2 ELECTROMIGRATION ENHANCED INTERDIFFUSION

Most digital GaAs microcircuits are fabricated using MESFET logic with a refractory metal-gold metallization system. Both TiW-Au and TiPt-Au are commonly used. The TiW and TiPt serve both to form Schottky barriers with the GaAs and as a metallurgical barrier between the gold and the GaAs. This metallurgical barrier is needed to prevent interaction between the Au and the GaAs. Similar barriers are also commonly used in silicon VLSI circuits to prevent silicon dissolution in the aluminum at ohmic contacts.

The integrity of the barrier layer is critical to the reliability of the microcircuit. In the Electronics Laboratory, a TiPt-Au system is used as the gate metal system for GaAs

integrated circuits. The stability of the barrier has been evaluated using the FATFET structure contained in the test element group shown in Figure 2. The barrier height and shape factor were derived from the I-V characteristics of the gate junction. The sample was annealed at 300°C in nitrogen for 101 hours, and the samples were removed periodically for recharacterization. The results are summarized in Table 1. The barrier height (ϕ) is very stable with no consistent variation over the 101 hours of anneal. The random variation in ϕ and n are believed to be within the accuracy of the measurement. Certainly, there is no consistent increase or decrease in these parameters with time.

Subsequently, an electromigration experiment was carried out using the electromigration test line shown in Figure 2. This test line was 1.25 micron wide, 0.5 micron thick,

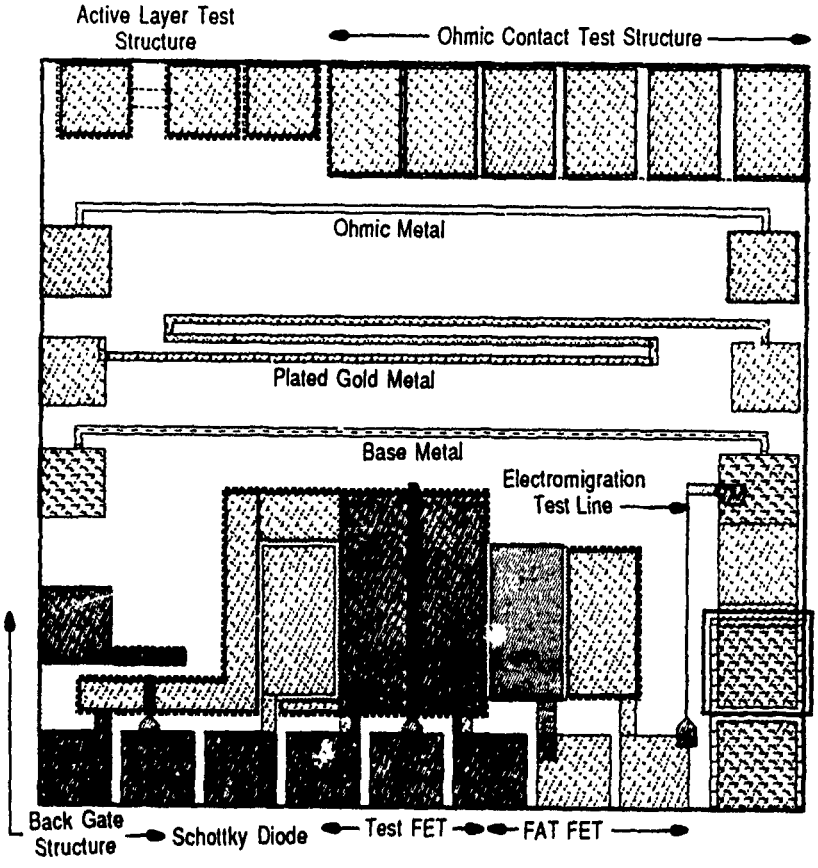

Figure 2. Test Element Group Used for Metallization Evaluation

and 300 micron long. The experiment was carried out on a probe station using a heated platform. A constant current source was used to supply a current of 2 x 10^6 A/cm^2.

Two probes were used on each pad, one serving as a Kelvin probe so that the voltage drop across the line could be monitored continuously during the experiment. This setup made it possible to estimate temperature rise due to self-heating and to calculate the average metal resistivity with time as an indicator of electromigration damage.

The sample was held at 250°C for 94 hours before failing catastrophically. The line resistivity was stable until about 4 hours before failure. Failure occurred when the line melted open at one end. Examination of the failed line using the SEM/Microprobe and Auger indicated that electromigration not only caused voiding and accumulation of gold, it also apparently caused vertical mixing of the metals and the GaAs. The Pt layer diffused down to mix with the GaAs, Ga diffused up into the gold, as did the Ti. Apparently, the TiPt metallurgical barrier had broken down allowing alloying of the metals and the GaAs.

Table 1. Barrier Height and Shape Factor vs. Time at 300°C

	Δ (eV)	n
Initial	.71	1.41
1h	.73	1.33
2h	.73	1.36
10h	.73	1.36
18h	.71	1.50
34h	.71	1.43
56h	.73	1.33
101h	.71	1.44

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A second experiment was conducted to explore these phenomena further. A GaAs FET with a double-fed gate (Π gate) was used instead of a test stripe. This FET has a 0.4 micron gate length. A DC current of 1 x 10^6 A/cm^2 was established in the gate metal while the device was held at 225°C. The test was stopped periodically, and the Schottky barrier characteristics and operating characteristic of the device were measured. Changes in these properties were used as indicators of degradation in the metal/GaAs Schottky barrier system, and therefore as indicators of the integrity of the metallurgical barrier.

During 13 hours of stress, the I_{dss} of the FET, the Schottky barrier height, and the ideality factor all changed. The device failed after 19 hours of stress, with the gate fusing open.

These results indicate that the metallurgical barrier is much less stable at 225°C in the presence of a high current density than the same system is at 300°C without the presence of the current. Apparently, electromigration in some way disrupts the metallurgical barrier, allowing interdiffusion of the metals. Significant disruption occurs well before voiding causes failure.

These results are based on the two experiments described above, and further work is necessary to fully understand and quantify the phenomenon. It can have a major impact on the reliability of GaAs integrated circuits using metal systems with a metallurgical barrier. To the author's knowledge, no investigations of this mechanism have been reported in the literature.

2
Program Plan

This program was designed to take advantage of the facilities and experience gained on an earlier program, "Metallization Qualification for VLSI" from which an electromigration life test facility and test sample design were already available. The facility was capable of stressing up to 300 lines simultaneously at ambient temperatures as high as 150°C. It was a computer controlled facility in which the resistance of each line was continually monitored and updated in a data file. A test sample consisting of four stripes of different lengths and widths with Kelvin contacts for accurate resistance measurement had also been designed. It was anticipated that this sample could be used for the electromigration on GaAs experiment and that another sample would be designed to study the electromigration assisted interdiffusion experiment. If the new samples were designed properly, the same life test facility and test board could be used for both facilities, with minor modifications to the test software.

Table 2 lists the test sample variations to be evaluated on this program.

Table 2. Test Sample Variations

Substrate	**GaAs, Oxidized Si**
Metallization	500A Ti, 1000A Pt, 6500 Au 500A Ti, 1000A W/10%Ti, 6500A Au 500A Ti, 500A Pt, 6500A Au 500A Ti, 500A W/10%Ti, 6500A Au
Width	1μm, 4μm

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Both GaAs and silicon substrates were used for the electromigration voiding experiment so that a direct comparison could be made between the rate of electromigration on the two materials. Both TiPt and TiW barrier layers were evaluated since both materials are frequently used in the gates of GaAs FETs. Two different barrier layer thicknesses were used to evaluate the effect of barrier layer thickness on susceptibility to electromigration assisted interdiffusion. A 1µm line width was chosen because it is typical of GaAs FET line widths, while a 4µm wide line was included to make failure analysis of degraded samples easier: the resolution of most analytical equipment is marginal at 1µm.

The approach to the experiments is outlined in Table 3.

The details of the test sample design are described in Section 3. A single test sample design was used for both experiments. This sample consisted of an FFT, the gate of which was designed to be an NIST standard electromigration test line. If just the gate structure is used, standard electromigration testing can be done. In the interdiffusion experiment, the gate-source junction is forward biased and the voltage drop between the gate and the drain is monitored. In this way, the drain contact is used as a Kelvin contact to the channel immediately beneath the gate. The measured voltage drop will consist of the voltage drop across the junction plus the resistance of the gate itself.

Table 3. Approach

1. Design Test Sample
2. Fabricate Test Samples
3. Characterize Test Samples
4. Step Stress Tests - Choose Current Density
5. Life Tests - 1000 Hours
6. Failure Analysis

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The life test boards were designed for the voiding experiments in which a controlled current is applied between two specific pins and the voltage drop across two other pins is monitored. By properly bonding out each of the chips, it was possible to use the same boards for both experiments and it was possible to run both experiments simultaneously in the same oven.

In order to determine the proper stress conditions for the life test, a step stress test was necessary since the rate of electromigration for these materials is uncertain. Since the life test oven was limited to an ambient temperature of 150°C, the step stress was run at fixed ambient of 150°C and the current density was stepped up from 5×10^5 A/cm² until failures were observed. The life test was then run at 150°C ambient and at a current density somewhat below that at which the step stress test terminated.

A single life test was run in which a total of 200 test lines were stressed at the same current density, 10 samples for each combination of test sample parameters. The 20 variations are listed in Table 4.

The life test was monitored continually, and the voltage drops measured across the lines or FETs were recorded and updated whenever they changed by more than a set value. After the life test, the samples were removed from the test and evaluated on the bench for both line resistance change and changes in FET characteristics. Degraded samples were analyzed for cause using the SEM and AUGER.

The test samples are described in more detail in Section 3. The results of the step stress test are presented in Section 4. The life test and its implementation are described in Section 5, and the results of the life test are presented in Section 6. The failure analysis results and the conclusions of the program are presented in Sections 7 and 8.

Table 4. Test Sample Variations

FETs	Resistors
• GaAs, Thin TiPt, 1μm	• GaAs, Thin TiPt, 1μm
• GaAs, Thick TiPt, 1μm	• GaAs, Thick TiPt, 1μm
• GaAs, Thin TiPt, 4μm	• GaAs, Thin TiPt, 4μm
• GaAs, Thick TiPt, 4μm	• GaAs, Thick TiPt, 4μm
• GaAs, Thin TiW, 1μm	• GaAs, Thin TiW, 1μm
• GaAs, Thick TiW, 1μm	• GaAs, Thick TiW, 1μm
• GaAs, Thin TiW, 4μm	• GaAs, Thin TiW, 4μm
• GaAs, Thick TiW, 4μm	• GaAs, Thick TiW, 4μm
	• Silicon, Thin TiPt, 1μm
	• Silicon, Thick TiPt, 1μm
	• Silicon, Thin TiPt, 4μm
	• Silicon, Thick TiPt, 4μm

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3
Test Sample Description

A test circuit suitable for the needs of this test program was designed. The circuit serves the dual purpose of allowing diode barrier characteristics and line stripe resistance to be monitored during electromigration testing. The test line length, width of connecting lines, and Kelvin contact placement all conform to the recommended test structure presented by H. A. Schafft[7].

The test circuit consists of four FET structures each with a gate width of 800μ. Two of the structures were designed with a 1μ gate length and two with a 4μ gate length. Kelvin contacts were included as part of each gate structure, and contacts for source and drain were provided.

The bonding pad layout for the test circuit was designed to conform to assembly into a 24-pin DIP package. Further, the pin-out arrangement in the 24-pin package was designed to conform to test equipment in place at the Electronics Laboratory. The equipment had been used previously for an electromigration experiment[8].

A step-and-repeat cluster was generated on a CALMA system that consists of five electromigration test circuits and one Test Element Group (TEG) containing resistivity, line width, and various process monitoring structures.

Each electromigration circuit has nominal dimensions of 2280μ by 1600μ. A 2-inch diameter wafer yielded approximately 200 test units after processing. A CALMA plot of the test cluster is shown in Figure 3.

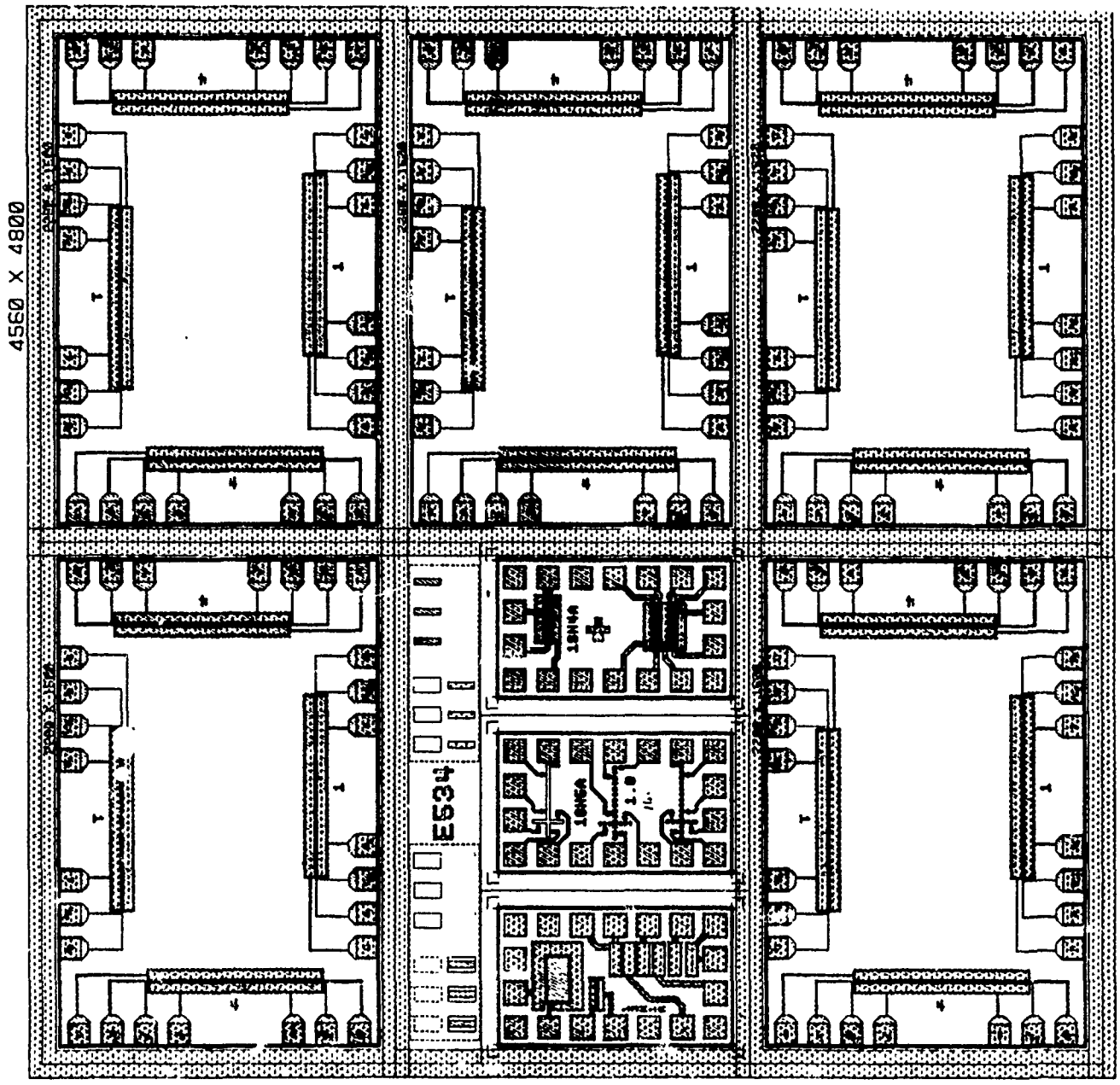

Figure 3. CALMA Plot of Electromigration Test Circuit Cluster

The test samples were prepared using GaAs and silicon wafers with two thicknesses of platinum and titanium-tungsten barrier layer metals. An SiO_2 layer of 20,000Å was formed on the silicon wafers. The silicon wafers were subjected to oxide etch steps to simulate the surface topography of processed GaAs structures.

The wafers used for sample preparation were processed at the fabrication facility of General Electric's Electronics Laboratory. Figure 4 shows the process flow and barrier metal variations used to prepare test samples. All metallization patterns were formed using a lift-off process technique.

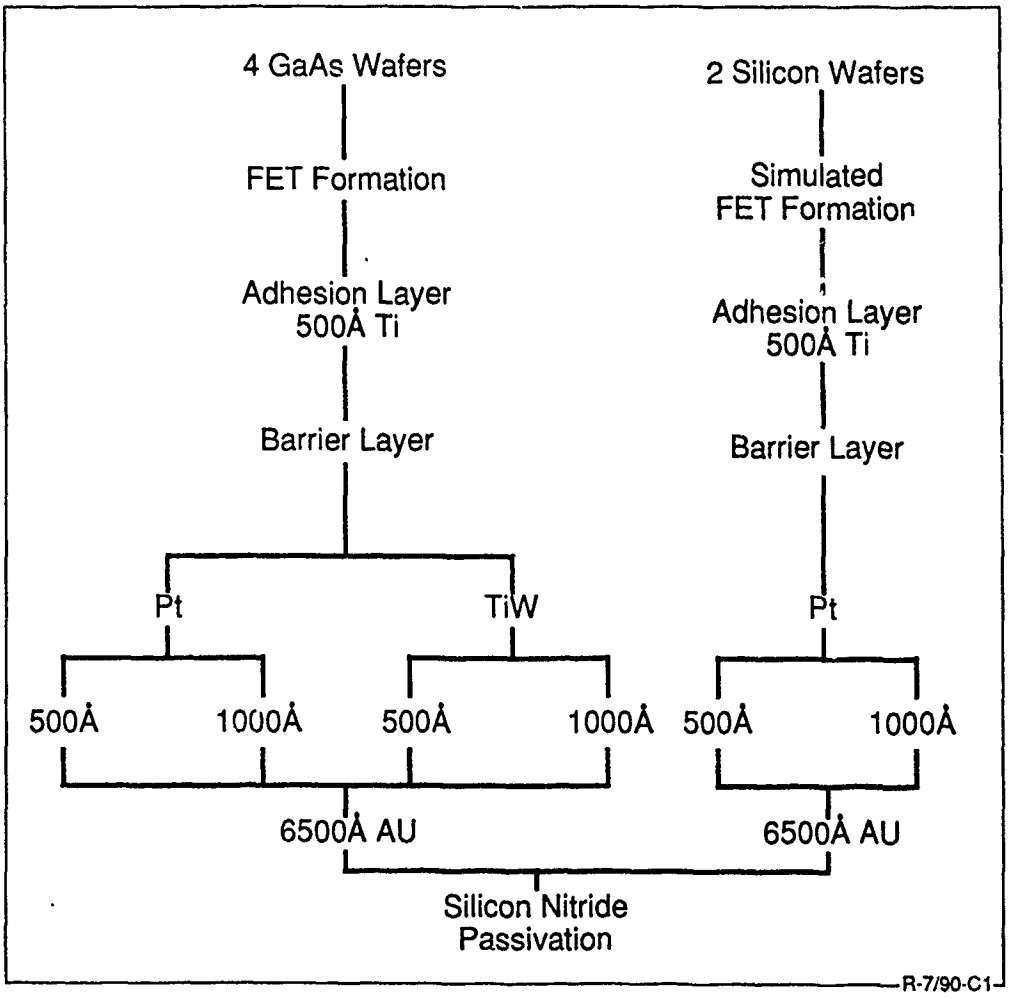

Figure 4. Wafer Process Flow With Barrier Metal Variations

One unforeseen problem encountered during the wafer processing concerned the difference in GaAs and silicon wafer thicknesses. Commercially available 2-inch diameter silicon wafers are 0.014 inches thick while 2-inch diameter GaAs wafers are 0.024 inches thick. This presented a severe problem in trying to use photomask stepper equipment. The equipment was set up to focus the photomask image on GaAs wafers only and would have required a costly readjustment to re-focus for silicon wafer thickness. The problem was solved by cementing two silicon wafers together using a high temperature curing epoxy.

For the purpose of sample identification during the life test, the wafers were designated as shown in Table 5.

Following normal 1μ wafer processing at the Electronics Laboratory, FET structures were evaluated at 35 test sites on each of the GaAs wafers. I_{dss}, G_m, V_{po} (pinch-off), V_{dbl} (drain-source breakdown), and R_{on} (channel on-resistance) were measured during the evaluation. Table 6 shows these values for wafer number 1. A negative or zero gain measurement indicates locations where no gate diode was formed. This situation typically results when the gate metallization is lost during lift-off. For these devices, test limit values are recorded for V_{po}, V_{dbl}, and R_{on}. The wafer probe measurements for all processed GaAs wafers fell well within the normal parameter limits.

Table 5. Wafer Identification

Wafer Type	Wafer No.	Barrier Layer
GaAs	1	1000Å Pt
GaAs	2	1000Å TiW
GaAs	3	500Å Pt
GaAs	5	500Å TiW
Silicon	1	500Å Pt
Silicon	2	1000Å Pt

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Table 6. Electrical Test Results on GaAs Wafer 1

LOT 884101 ELECTROMIGRATION CIRCUIT WAFER 1

SITE #	Idss	Gm(0)	Voo (V	Vd51 (V)	Ron	
1	286.1	87.55	-4.2	-10.148	5.25	
2	280.8	90.16	-4.1	-10.794	5.18	
3	467.5	-.02336	-8.1	0	.119	
4	283.3	90.89	-4.1	-10.304	5.08	
5	286.6	89.67	-4.2	-9.84	5.19	
6	319.4	86.12	-4.8	-8.49	4.91	
7	333	85.35	-5.1	-8.496	4.83	
8	467.5	0	-8.1	0	65.8	
9	301	88.61	-4.4	-11.598	5.03	
10	467.5	0	-8.1	0	.119	
11	297.9	89.8	-4.3	-9.32	5.11	
12	307.5	85.58	-4.6	-12.908	5.17	
13	331.2	87.06	-5	-11.468	4.71	
14	333	86.54	-5	-12.614	4.71	
15	335.5	84.84	-5.1	-11.11	4.85	
16	329.1	86.5	-5	-10.784	4.86	
17	339.6	84.51	-5.2	-13.078	4.82	
18	345.7	87.97	-5.2	-11.514	4.51	
19	304.5	89.18	-4.4	-13.912	4.94	
20	345.2	21.94	-8.1	-13.344	4.89	
21	296.3	89.27	-4.3	-13.41	5.23	
22	326.6	85.96	-4.9	-13.378	4.99	
23	331	88.53	-4.9	-12.71	4.7	
24	323.1	86.52	-4.8	-13.648	4.96	
25	311.7	85.63	-4.7	-12.294	5.2	
26	290.1	88.28	-4.2	-14.468	5.39	
27	467.5	0	-8.1	0	.119	
28	316.1	89.35	-4.6	-13.856	4.91	
29	467.5	0	-8.1	0	.119	
30	299.1	92.25	-4.2	-15.21	5.06	
31	327	90.47	-4.6	-11.198	4.84	
32	323.4	86.71	-4.9	-13.79	4.91	
33	296.7	88.45	-4.3	-15.364	5.31	
34	313.4	89.63	-4.4	-12.898	5.07	
35	407.9	57.55	-8.1	-6.718	4.39	
SUMS	11869.3	2940.846c4		-186.2	-358.6c4	219.276
MEANS	339.1	72.6	-5.32	-10.2	6.15	

Figure 5 shows a finished test unit on GaAs wafer 1 prior to die separation. The die were separated at the Electronics Laboratory using a diamond saw.

Test samples were assembled, wire bonded, and lidded by an outside vendor. The die were bonded to the package using a non-electrically conductive epoxy and were wire bonded with gold ball bonding equipment. Figures 6 and 7 show, respectively, units assembled in the resistor test stripe (configuration 1) and FET (configuration 2) fashion.

Package pin number 1 is to the top in both Figures 6 and 7. Referring to Figures 6 and 7, the individual lines on each test circuit were identified according to Table 7.

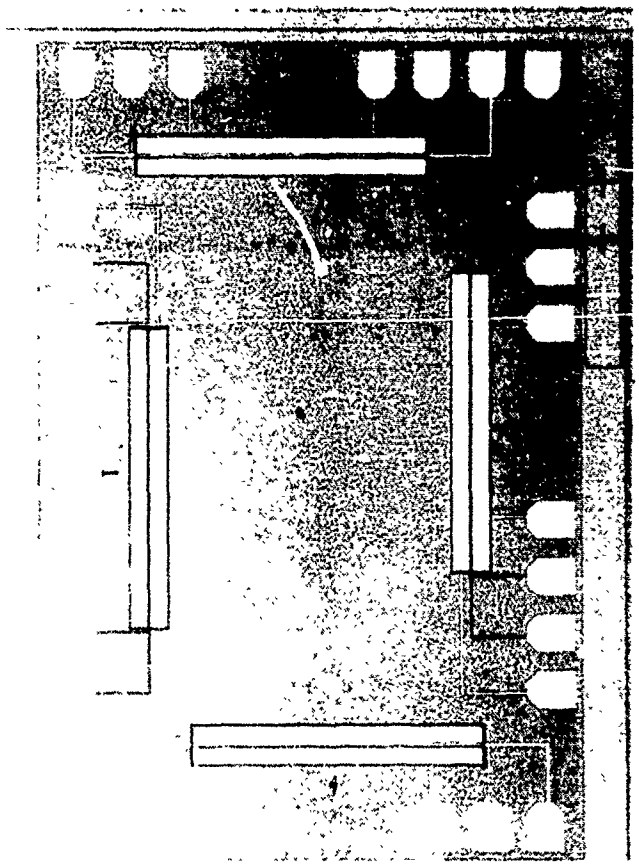

Figure 5. Electromigration Test Circuit of Wafer 1 Prior to Die Separation

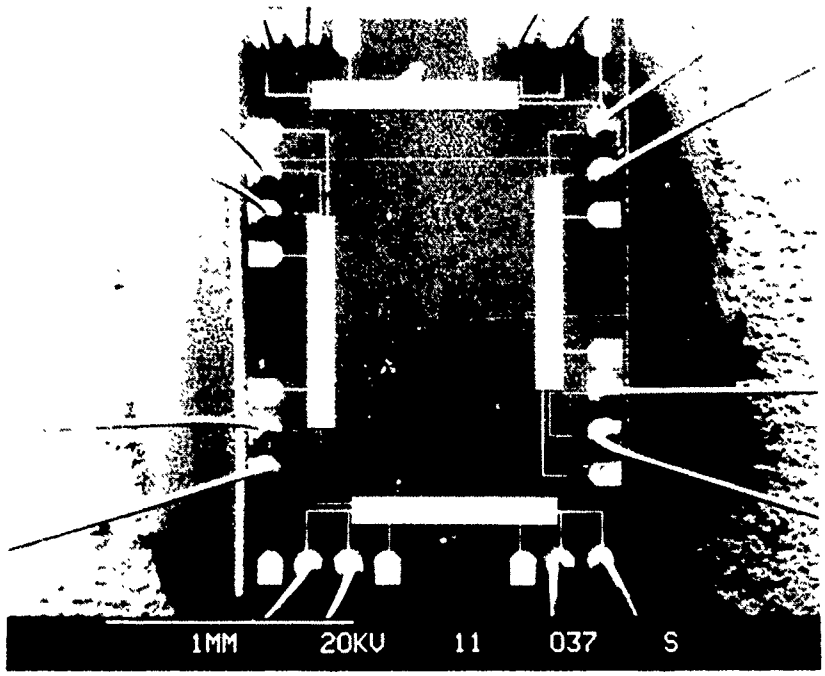

Figure 6. Test Unit From GaAs Wafer 1 Assembled in Resistor Stripe Configuration (Configuration 1)

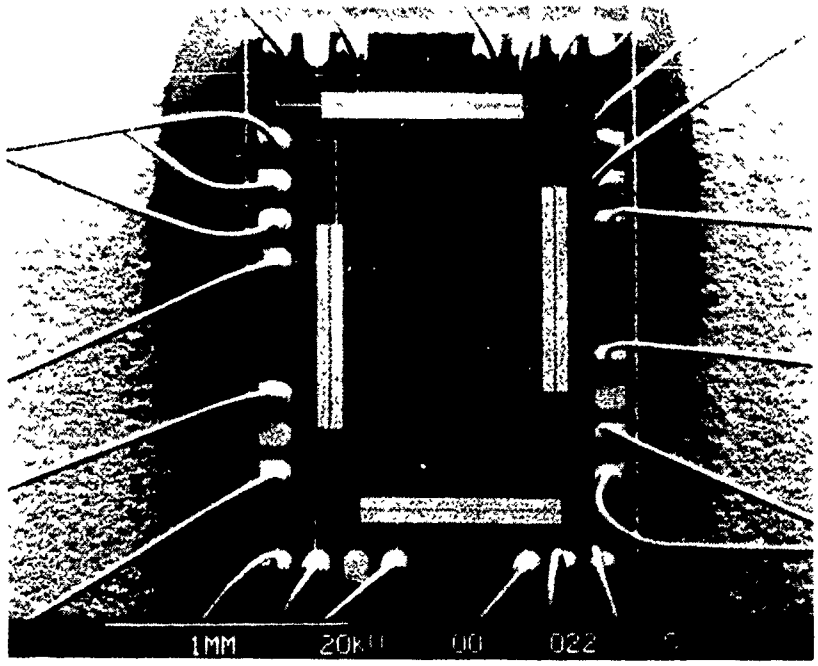

Figure 7. Test Unit From GaAs Wafer 2 Assembled in FET Configuration (Configuration 2)

For the purposes of identification in the life test, each sample was identified according to the following scheme:

Wafer Type Wafer Number Configuration Sample Number Line Number

For example, G1-1-3-1 corresponds to GaAs wafer 1, resistor configuration, sample 3, test line 1. G1-2-3-1 corresponds to GaAs wafer 1, FET configuration, sample 3, test line 1. Since there were only resistor test stripes fabricated on silicon, all silicon samples were configuration 1.

Table 7. Test Line Identification by Position on Test Circuit. Package Pin Number 1 is at the top.

Line Number	Position
1	Bottom
2	Left
3	Top
4	Right

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4
Step Stress Test

A step stress test was planned for the purpose of determining conditions for a longer life test. It was proposed that increasingly higher current density be applied in steps at an elevated temperature for a relatively short period of time (72 hours). A small number of samples from each wafer would be tested and monitored electrically. In this way, conditions for a longer life test (1000 hours) could be determined quickly.

Two samples from each GaAs and silicon wafer were selected for the step stress test. All units were mounted onto circuit boards in the test oven. For the test, all number 1 lines were connected in series, all number 2 lines were connected in series, etc.

During the test a constant current was passed through each string of test lines with the oven held at 150°C. For the resistor lines the current was passed through the gate metallization stripe and the voltage was monitored at the Kelvin contacts at each end of the stripe. For this test, the current was uniform along the stripe and the voltage drop across the line is proportional to the resistance of the line, which increases as voiding due to electromigration increases. For the FET configuration samples, the current is fed into one end of the gate, through the gate junction, and out the source contact. This simulates the gate current in an RF power FET with the current along the gate stripe being maximum at the feed end and decreasing with distance along the stripe. Under these conditions, voiding will be maximum near the feed end of the gate. During the test, the voltage drop between the Kelvin contact at the feed end of the gate stripe and the drain contact of the FET is measured. In effect, the drain contact is used as a Kelvin contact to measure the voltage in the channel beneath the gate. The measured voltage for the FET configuration consists of the sum of the gate metal resistance and the forward voltage drop across the gate Schottky junction. Therefore, if the junction degrades or becomes shorted, or if

gate metal voiding occurs, this voltage drop will vary. Therefore, in either configuration, the monitored voltage drop will provide an indication of progress of electromigration, either voiding or junction shorting.

A high current density in a thin resistive film causes a condition of "self heating" in which the temperature of the film will rise above the ambient temperature. It is important to know the amount of self heating so that the test conditions are known accurately. Prior to beginning the test, an attempt was made to measure the self heating on each test stripe in the test oven. Test line self heating is measured in the following way:

a. A low constant current, I_1, is picked so that current density is $<<1 \times 10^6$ A/cm^2.
b. At room temperature, T_1, I_1 is passed through the test line and Kelvin contact voltage, V_1, is measured.
c. Heat the sample to a high test temperature, T_2, pass current I_1 through the test line, and measure Kelvin contact voltage V_2.
d. Establish a high constant current density ($>1 \times 10^6$ A/cm^2) in the test line by passing current I_3, and measure the Kelvin contact voltage, V_3.
e. Calculate the temperature rise, $\Delta T=(T_3-T_2)$, using the following equation:

$$\Delta T=(T_2-T_1)*((I_1/I_3)*V_3-V_2)/(V_2-V_1))$$

When this measurement was made, values of 40°C to 70°C were calculated. Bench top measurements showed that the oven measurements were almost an order of magnitude too high.

A lengthy investigation followed during which test equipment, circuit boards, oven, and current sources were all eliminated as the source of the measurement error. It was found that a current leakage path(s) existed which was a function of temperature. At 120°C and above, the voltage measured at Kelvin contacts could be seen to drop as temperature increased.

During the course of this investigation, the leakage became increasingly worse. With all circuit boards removed from the test rack inside the oven, a leakage of several milliamps would flow in what should have been open circuit conditions.

The leakage path(s) was traced to the circuit board backplane. The leakage was finally eliminated by thoroughly cleaning the backplane with various solvents.

The step stress test was run at the conditions shown in Table 8.

Because of software problems, it was possible to monitor only test lines 2 and 3 (4μ lines) during the step stress test.

After each step in the test, an FET sample was randomly selected and removed for curve tracer measurements. After the first step, the samples showed a general rise in resistance. After the second step, the samples showed a general decrease in resistance back toward the original values and in some cases slightly lower than original. This behavior has been observed during other electromigration tests[8].

There were still no significant changes in either resistor stripes or FETs following the step at $J=3x10^6$ A/cm^2. Changes were observed following the final step. Three FET units, one each from wafers 1, 2, and 3, were severely degraded. Figure 8 shows a normal gate-source diode characteristic from wafer 3 and Figures 9 and 10 show the gate-source diodes of degraded FETs from wafers 1 and 3 respectively.

Several of the resistor stripes showed resistance increases of 2-3% following the final step. Previous electromigration work has shown that resistance changes of this magnitude are significant. It was judged that the step stress test results were sufficient to choose a set of test conditions.

Table 8. Test Conditions for Step Stress Test

Temperature °C	J Amp/cm^2	Time Hr
150	$1.5X10^5$	72
150	$1X10^6$	72
150	$1.5X10^6$	72
150	$2X10^6$	72
150	$3X10^6$	72
150	$4X10^6$	72

R-7/90-C7T

Figure 8. Normal Gate-Source Diode Characteristic

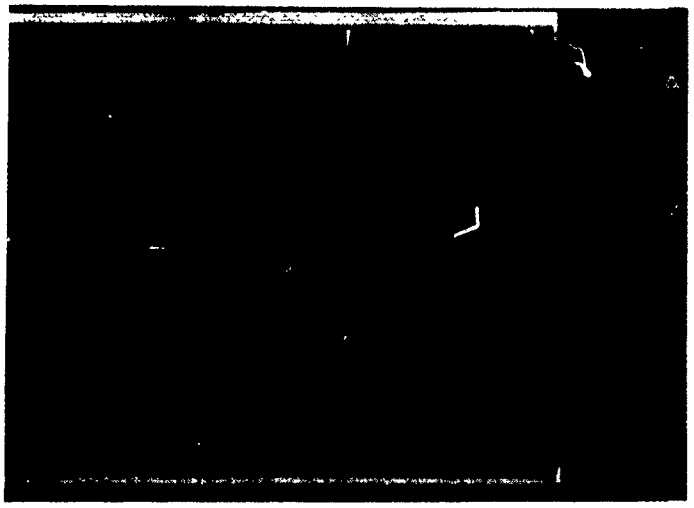


Figure 9. Degraded Gate-Source Diode on Sample from Wafer 1

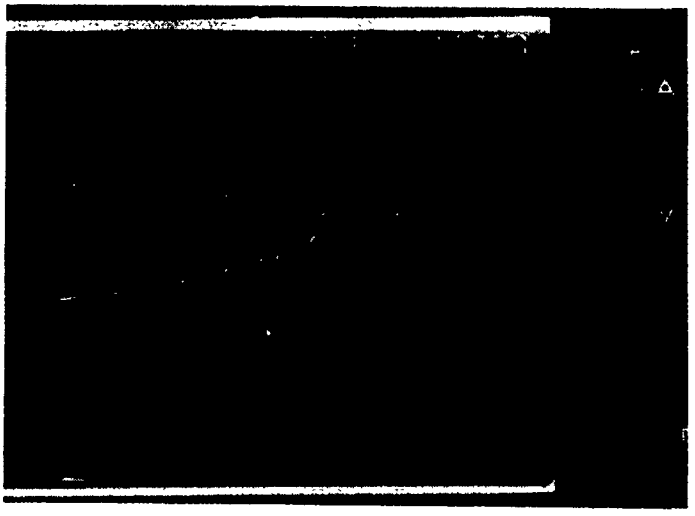
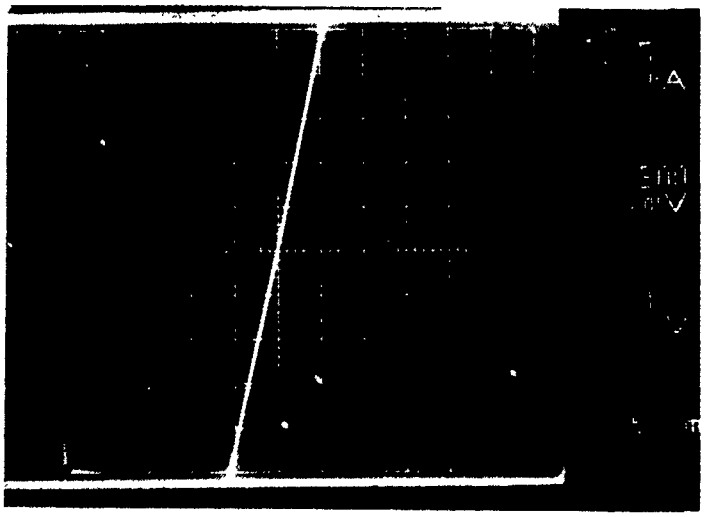


Figure 10. Degraded Gate-Source Diode on Sample from Wafer 3



5
Life Test

It seemed clear from the step stress test results that significant degradation could be caused in a short period of time with very high current densities of 3-4x10^6 A/cm^2. Furthermore, the test seemed to indicate that the FET structures would suffer considerably more damage faster than the resistor samples. Since the program would allow for only one life test in the 1000 hour range, it was decided that a lower current density would be used for the life test. Life test conditions were set at:

Temperature: 150°C

Current Density: ~2.5x10^6 A/cm^2

Table 9 describes the life test samples selected.

Table 9. Life Test Samples

Wafer Type	Wafer No.	No. Samples	Configuration
GaAs	1	5	1
GaAs	2	5	1
GaAs	3	5	1
GaAs	5	5	1
Silicon	1	5	1
Silicon	2	5	1
GaAs	1	6	2
GaAs	2	5	2
GaAs	3	5	2
GaAs	5	5	2

R-7/90-C8T

Test equipment used in a previous electromigration life test was in place at the Electronics Laboratory. This equipment is capable of simultaneously stressing up to 300 test lines at elevated conditions of current density and temperature. A computer program written for the HP-85 computer controls the operation of a Datalogger. The Datalogger continuously scans each of the test positions serially, measuring the voltage at the test stripe Kelvin contacts. At the beginning of the test, a scan file is created containing the following information on each test stripe:

a. Serial number
b. Time of day
c. Date
d. Total time under test
e. Voltage at Kelvin contacts

A 3-volt Zener diode has been placed across each test stripe in a reverse biased position. The purpose of the diode is to provide electrical continuity when individual test stripes fail catastrophically. The reverse leakage of this diode at the operational conditions is at least three orders of magnitude less than the test current. Therefore, the Zener diode will cause no significant error in test data.

The initial voltage across each sample is stored in an array in computer memory. During each scan the new value for each line is compared to the value stored for that line in the array. The computer program has been written such that a change in voltage of 1% will cause the information described above to be stored in a buffer for later storage on disk. Each time a change in voltage of 1% is recorded for a particular line, the new voltage is inserted into the array and becomes the base value against which succeeding measurements are compared. Catastrophic failure is detected when the Zener voltage is measured.

Figure 11 diagrammatically describes the life test setup.

In the course of getting the life test started, it was noticed that a current leakage path(s) was once again affecting the test voltage measurements. This leakage behaved in an equivalent fashion to the leakage found prior to the step stress test. That is, a leakage of several milliamps started as soon as the oven reached 120-125°C and became worse with increasing temperature.

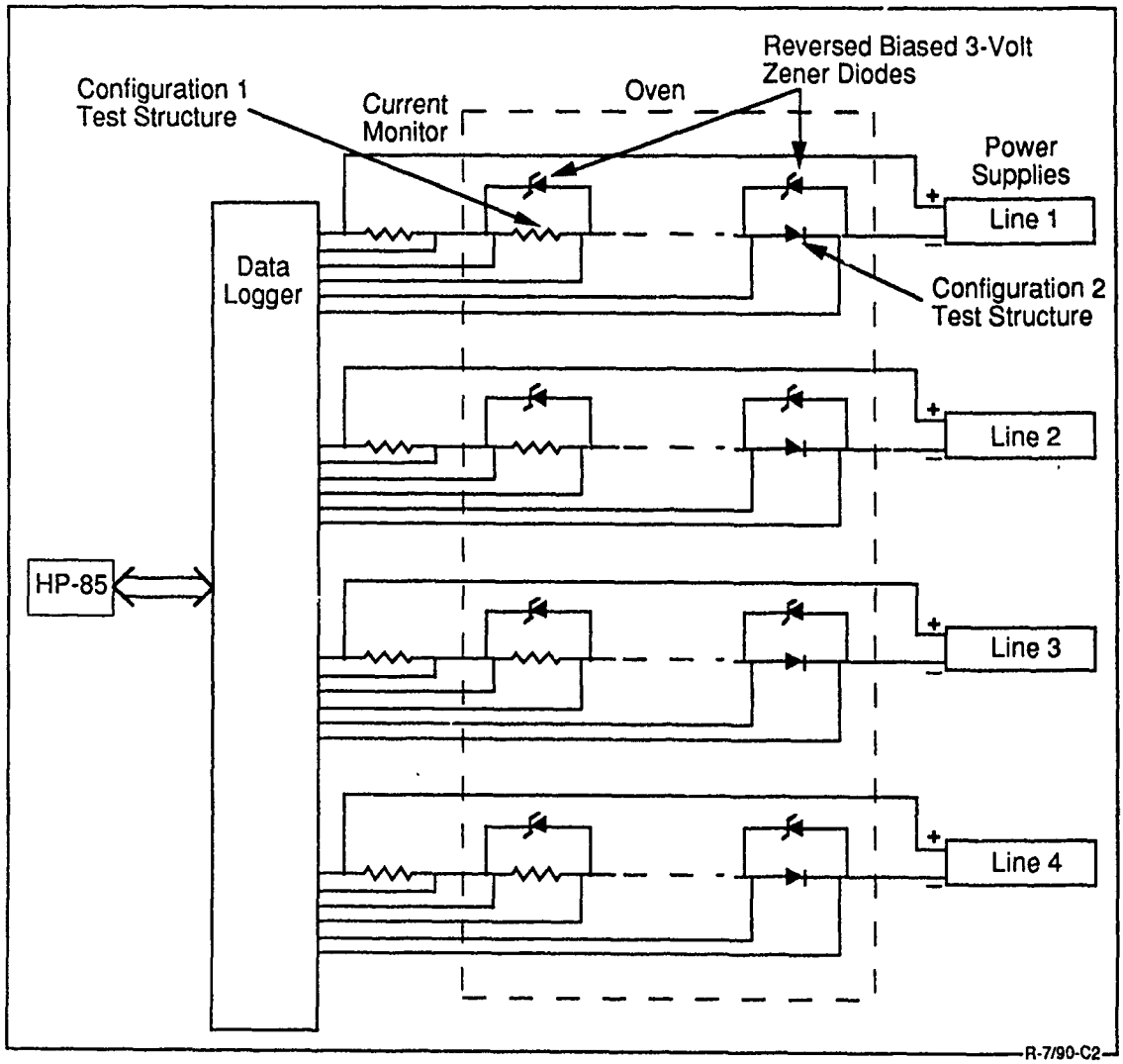


Figure 11. Diagram of Life Test Setup

The leakage was once again traced to the backplane in the test rack. Thorough solvent cleaning and physical abrading of the backplane were no use in reducing the leakage. To make matters worse, the circuit boards used in the test began to deteriorate by emitting bromine gas and organic filler.

Because of the restrictions imposed by limited remaining funds, the circuit boards could not be replaced and the only option remaining was to repair the backplane and attempt to retard the board deterioration.

The backplane was replaced (a matter of reconnecting over 600 wires) and the circuit boards were heavily coated with Hysol Epon 828 epoxy. The boards were test-baked at 150°C for 500 hours. The boards showed no further signs of deterioration. However, because of warping, it was not possible to remove and replace boards at intervals during the test. This meant that only a sampling of FET units could be removed for curve tracer evaluation at regular intervals.

The life test was begun and the following FET readout schedule used:

TEST TIME AT READOUT, HR
24
84
226
390
726
1121

After the last readout, an open circuited failure occurred in test line 1. It was not possible to locate and repair the failure without removing and replacing test boards. Test line number 1 was not stressed further during the remaining test.

The current density was increased to approximately 3.5×10^6 A/cm^2 and the test was continued using test lines 2, 3, and 4 for an additional 164 hours.

6
Data Analysis

6.1 VOIDING EXPERIMENT

Ten lines of the 12 different combinations of line width and barrier metal, and substrate were stressed and the resistance of the line was measured before and after the stress. The change in resistance, averaged over the 10 lines for each combination, is shown in Table 10. This data is taken following 1121 hours of life test plus the additional 164 hours at the higher current density.

The accuracy of the measurements is no better than 1% and, therefore, the only significant increases occurred for the 4μm TiW lines on GaAs and for the 1μm and 4μm lines on silicon. The largest change was sustained by the silicon substrate samples with the thin TiPt barrier. The TiW barrier samples experienced a much larger change than those with the TiPt barriers.

Table 10. Resistor Variations During Life Test

GaAs/Thick TiPt/4μm	0.4%	GaAs/Thick TiPt/1μm	0.4%
GaAs/Thin TiPt/4μm	-0.2%	GaAs/Thin TiPt/1μm	-0.6%
GaAs/Thick TiW/4μm	5.2%	GaAs/Thick TiW/1μm	-0.1%
GaAs/Thin TiW/4μm	6.8%	GaAs/Thin TiW/1μm	0.3%
Si/Thick TiPt/4μm	-0.6%	Si/Thick TiPt/1μm	-1.3%
Si/Thin TiPt/4μm	5.6%	Si/Thin TiPt/1μm	13%

R-7/90-C9T

The 4μm lines varied significantly more than the 1μm lines. This may be explained in terms of the effect of the grain size on the rate of electromigration. Subsequent SEM analysis shows that many of the grains have diameters in excess of 1μm but not more than 4μm and therefore some of the 1μm lines can have grains blocking grain boundary diffusion (bamboo effect).

Comparing electromigration on GaAs with that on oxidized Si, we can say that, if anything, the rate of electromigration on Si is larger. This might have been partially caused by the fact that the self-heating of the lines was slightly higher for the Si substrate. There is no evidence to support the contention that electromigration on GaAs is more severe than on oxidized silicon.

6.2 ELECTROMIGRATION ASSISTED INTERDIFFUSION EXPERIMENT

The measured change in voltage drop across the gate junction during the life test is shown in Table 11. These values are the average of 10 lines for each category.

There was obviously very little change in the Schottky junction during the life test. This was confirmed by a comparison of the transistor characteristics and leakage currents measured using a curve tracer for each sample before and after the life test.

Table 11. Changes in Junction Voltage Drop

GaAs/Thick TiPt/4μm	2%	GaAs/Thick TiPt/1μm	2%
GaAs/Thin TiPt/4μm	3%	GaAs/Thin TiPt/1μm	5%
GaAs/Thick TiW/4μm	2.5%	GaAs/Thick TiW/1μm	1%
GaAs/Thin TiW/4μm	2.5%	GaAs/Thin TiW/1μm	2%

R-7/90-C10T

6.3 CURRENT DENSITY

During the life test, all of the number 1 lines were arranged in series with a single constant current supply feeding the series chain. This included both resistor samples and transistor samples and samples from all six wafers. Three other series chains were formed by the number 2, 3, and 4 lines. The current supplies were set to apply a nominal current density of 2.5×10^6 A/cm^2 to each line. However, because the line width and thickness varied from wafer to wafer and line to line, the actual current density varied from sample to sample. The actual current density can be estimated from the measured voltage drop across each resistor line:

$$j = v/\rho l$$

where j = the current density,

ρ = the resistivity of gold (2.4×10^{-6} ohm cm), and

l = the line length (.08 cm)

The estimated current densities for each of the lines on each of the wafers are listed in Table 12.

The 4μm lines were stressed at or near the planned 2.5×10^6 A/cm^2, but the actual current density for the 1μm lines was significantly higher. This was due to the variability in the width of the 1μm lines from wafer to wafer. The TiW lines had somewhat lower current density than the TiPt lines, primarily because the thickness of the gold on those wafers was about 50% higher. These current density variations must be taken into account in interpreting the degradation data of Tables 10 and 11.

Table 12. Estimated Current Densities

Wafer	Current Density (A/cm^2)
GaAs/Thick TiPt/4μm	$2.8x10^6$
GaAs/Thick TiPt/1μm	$3.8x10^6$
GaAs/Thin TiPt/4μm	$3.0x10^6$
GaAs/Thin TiPt/1μm	$4.5x10^6$
GaAs/Thick TiW/4μm	$2.1x10^6$
GaAs/Thick TiW/1μm	$4.3x10^6$
GaAs/Thin TiW/4μm	$2.0x10^6$
GaAs/Thin TiW/1μm	$3.3x10^6$
Si/Thick TiPt/4μm	$3.2x10^6$
Si/Thick TiPt/1μm	$5.1x10^6$
Si/Thin TiPt/4μm	$3.0x10^6$
Si/Thin TiPt/1μm	$4.7x10^6$

R-7/90-C11T

6.4 GRAIN SIZE EVALUATION

The rate of electromigration is known to be a function of the grain size of the metal films. At the life test temperature, grain boundary electromigration is dominant and, therefore, films with smaller grains may be expected to have a higher rate of electromigration. This is particularly true for very narrow lines with line widths of the same order of magnitude as the grain size. Electromigration will be reduced substantially if a large grain completely crosses a line so that there are no grain boundary paths around the grain. This bamboo effect has been found to result in a substantial increase in lifetime of aluminum lines as their width of the line approaches 1μm.

Figure 12 is a backscatter electron image of a line from wafer 1, taken in the SEM. Backscatter emission is known to be much more sensitive to composition and grain orientation than secondary emission and, therefore, backscatter photographs can be used, at least qualitatively, to evaluate the grain structure of metal films. In the picture, the preponderance of large grains is clearly visible. The varying grain orientations, as indicated by the contrast between grains, is also evident. Analysis of the grain size distribution from this picture indicates that the grains are log-normally distributed with a median grain size of about 1μm and a sigma of 0.5.

Figures 13 through 17 are backscatter photographs for the other five wafers. The grain size distributions for the other wafers appear to be similar to that of wafer 1. These photographs were taken after the life test using samples which had been stressed.

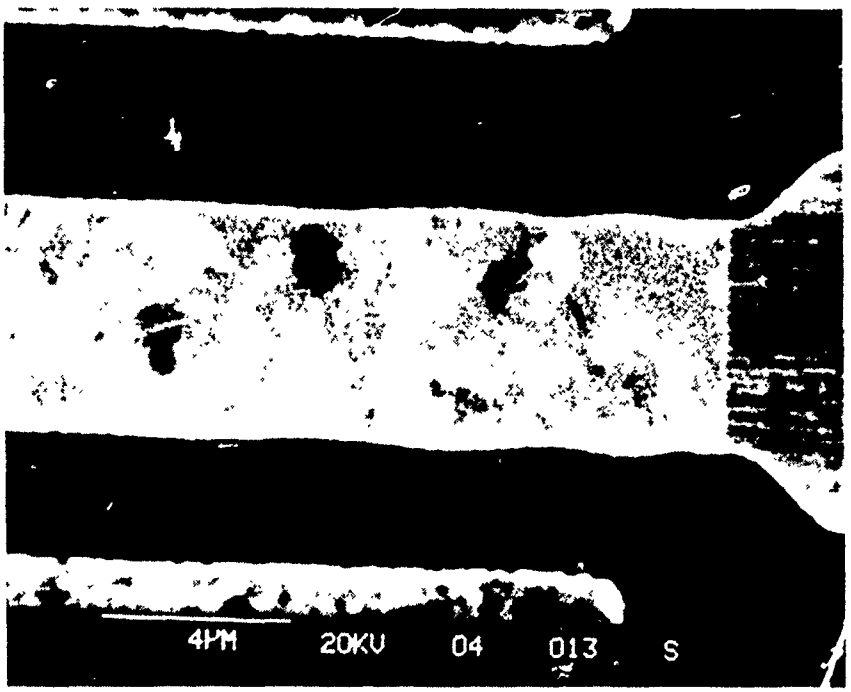


Figure 12. Backscatter Photograph of Line G1-2-4-3 Showing Large Grain Structure

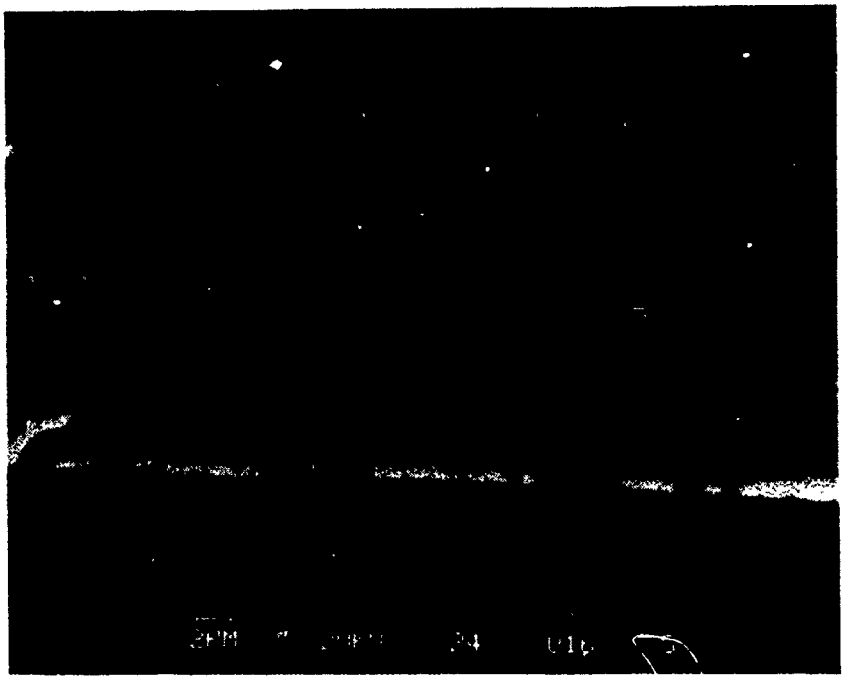


Figure 13. Backscatter Photograph of Line G1-2-4-1

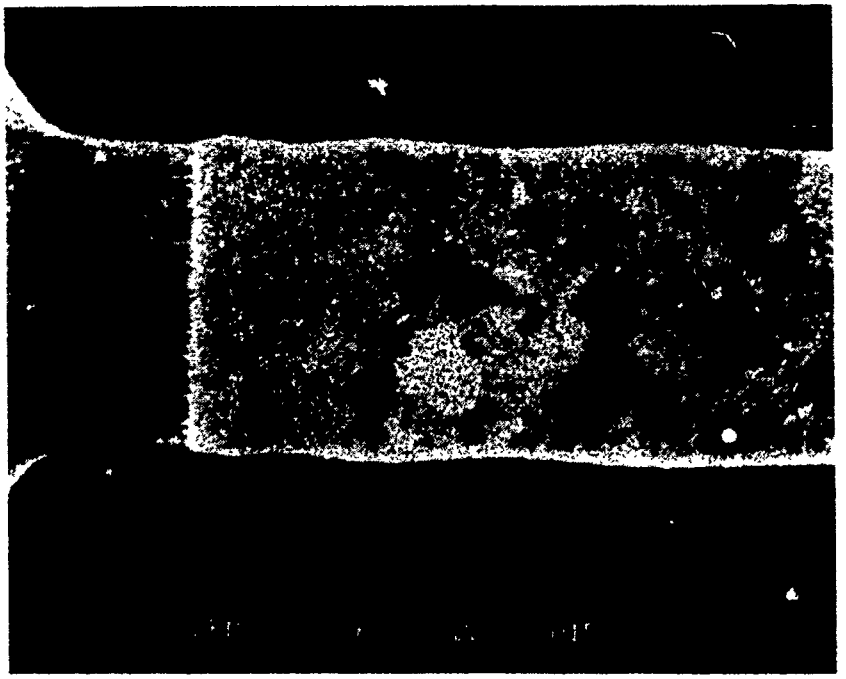


Figure 14. Backscatter Image of Line G3-2-2-3

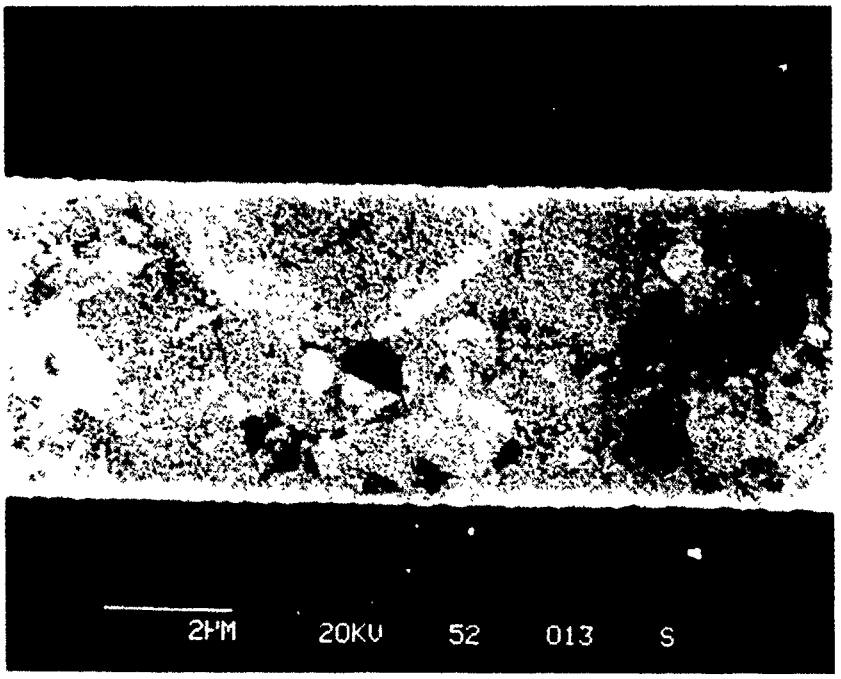


Figure 15. Backscatter Image of Line G5-2-1-3

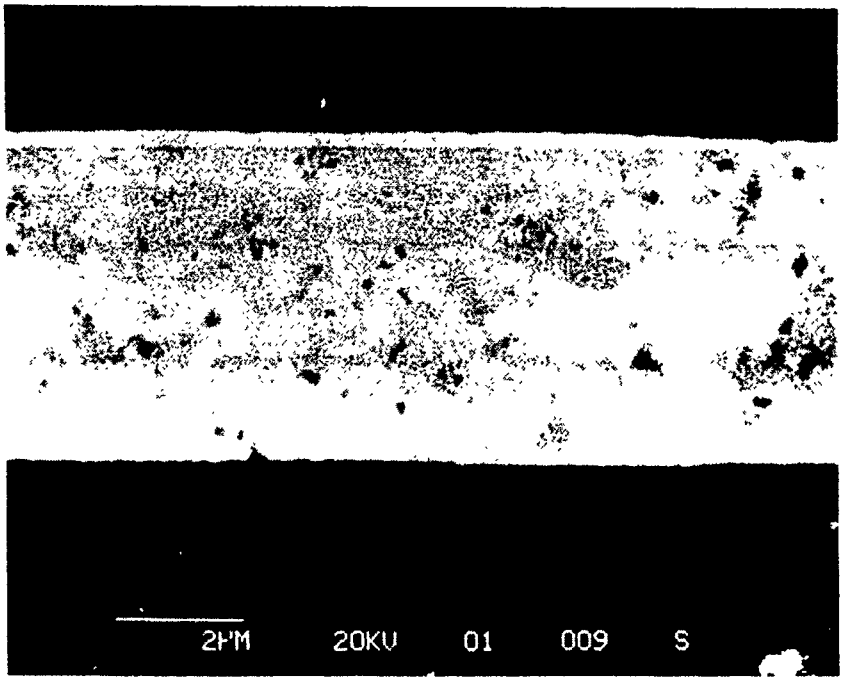


Figure 16. Backscatter Image of Line S1-1-4-3

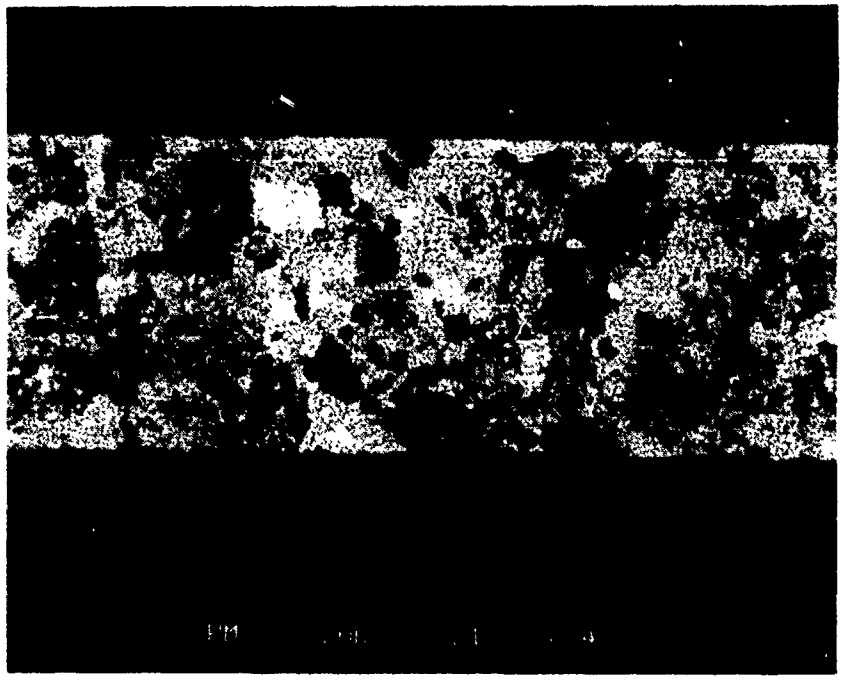


Figure 17. Backscatter Image of Line S2-1-1-1

7
Failure Analysis

7.1 SEM ANALYSIS

Samples from each of the four GaAs and two silicon wafers were examined for electromigration damage. The lids were removed from the samples and the silicon nitride passivation was removed. Figures 18 and 19 demonstrate typical electromigration damage to 1μ and 4μ lines from GaAs wafer 1. Hillock formations can be seen on the 4μ line in Figure 19. Electromigration on GaAs wafer 1 was not extensive but did occur on both width lines.

Units from GaAs wafer 2 consistently showed more electromigration damage than any other GaAs or silicon wafer. The single failure during this test came from GaAs

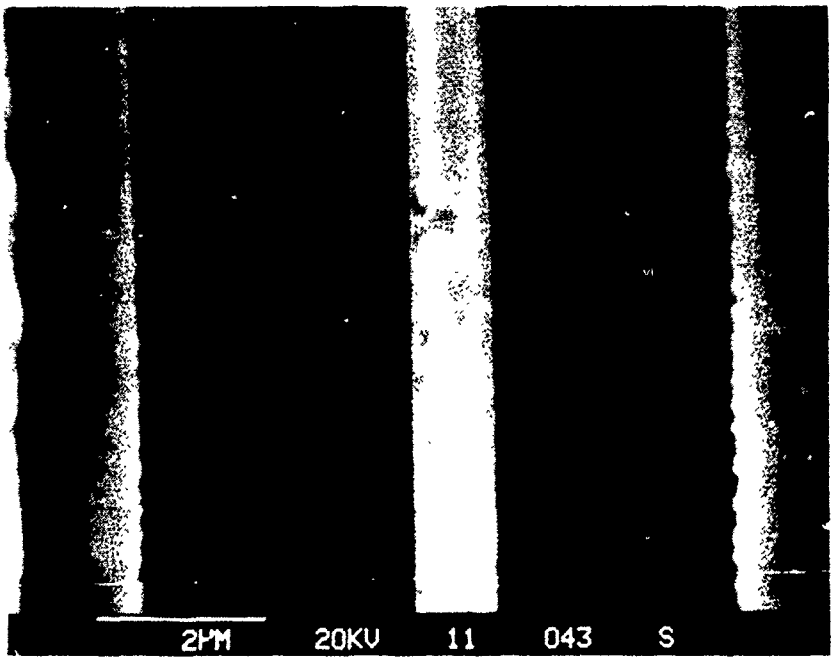


Figure 18. Typical Electromigration on 1μ Line, GaAs Wafer 1, Sample G-1-1-1-2

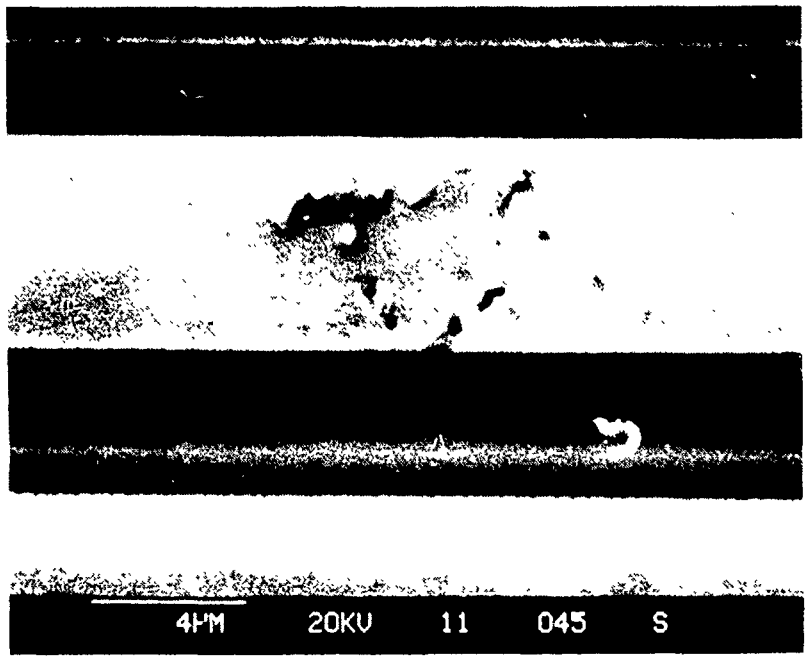


Figure 19. Typical Electromigration on 4µ Line, GaAs Wafer 1, Sample G-1-1-1-1

wafer number 2. The failure was a 1µ resistor stripe and is shown in Figure 20. As in all the samples evaluated, the electromigration on this failure appears to have originated from the bottom of the test line.

This failure occurred after 750 hours into the life test, and subsequently "healed." The failure was intermittent when examined at room temperature. It was not possible to locate an exact failure site and the failure may not have been due to voiding in the line.

Figures 21 and 22 show examples of the typical electromigration damage found on units from GaAs wafer 2. The titanium-tungsten barrier layers on GaAs wafers 2 and 5 were sputter-deposited in a different system than that used to sputter-deposit platinum on GaAs wafers 1 and 3. In both cases, a thin (~500Å) layer of gold was sputter-deposited last because the final thick (6500Å) layer of gold was evaporated in a third, separate system. It is standard practice not to expose metallization layers that are subject to oxidation in air as would have happened in the transfer from one system to another.

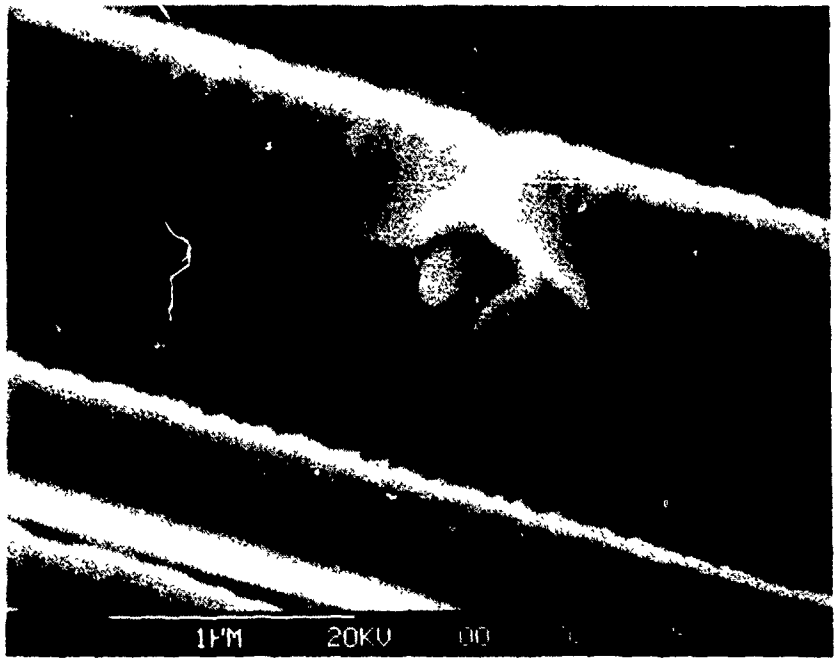


Figure 20. Failure Site on 1μ Line From GaAs Wafer 2, Sample G-2-1-1-2

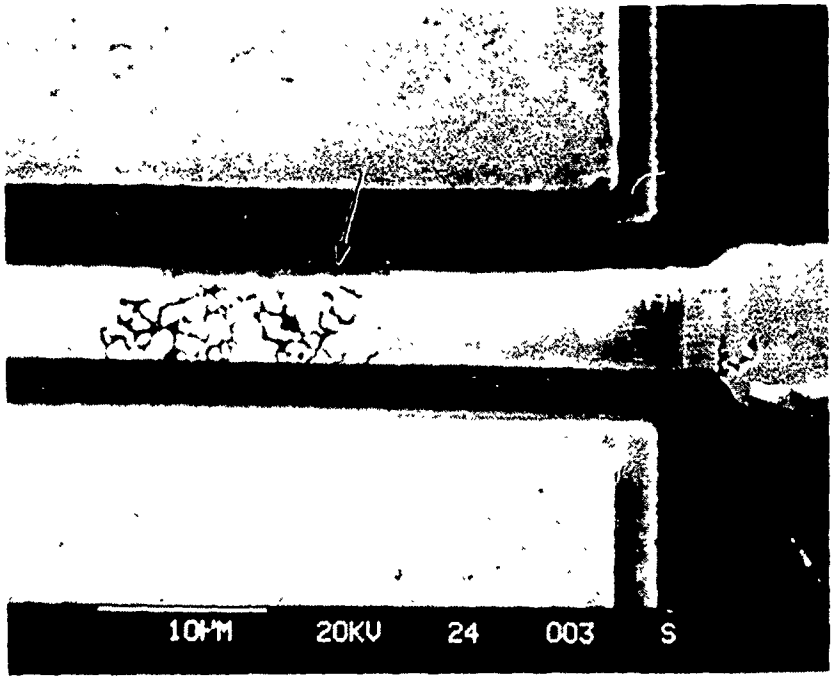


Figure 21. Electromigration Site on 4μ Line, GaAs Wafer 2, Sample G-2-2-4-1

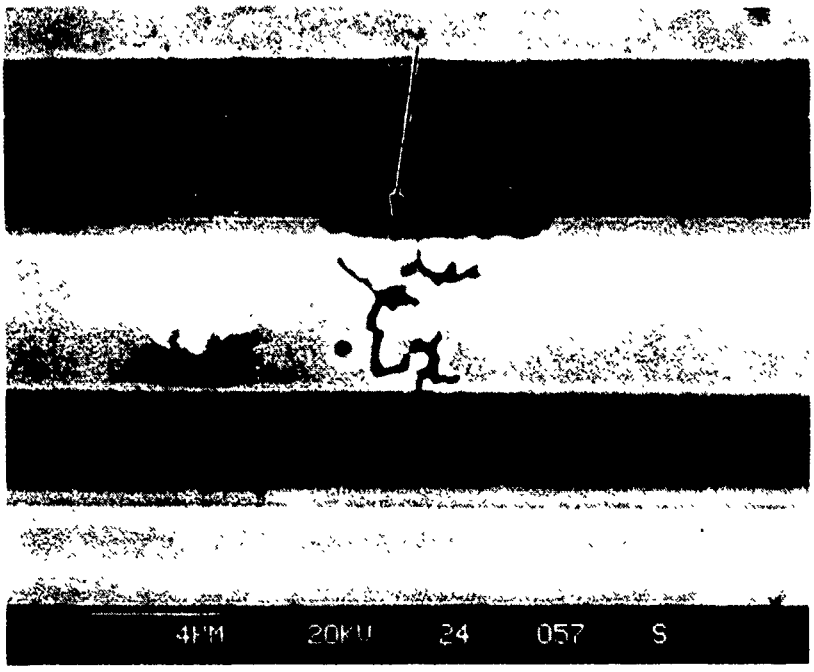


Figure 22. Electromigration Site on 4μ Line, GaAs Wafer 2, Sample G-2-2-4-3

It was reported by wafer process personnel that wafers in the Ti-W system became considerably hotter than wafers during the Pt deposition. Since the process used was a photoresist lift-off technique, all metal layers are deposited through an opening in a photoresist layer. During the Ti-W deposition, the higher than normal temperature caused the photoresist to flow, slightly narrowing the gate dimension. This resulted in what appeared to be a narrow ledge of gold which protruded beyond the edge of the thick gold. At electromigration sites, this thin layer disappeared. The arrows on Figures 21 and 22 point out areas where the thin gold ledge is missing.

Figures 23 and 24 show, respectively, electromigration on 1μ and 4μ lines on a sample from GaAs wafer 3. Hillock formation can be seen to the left of the site.

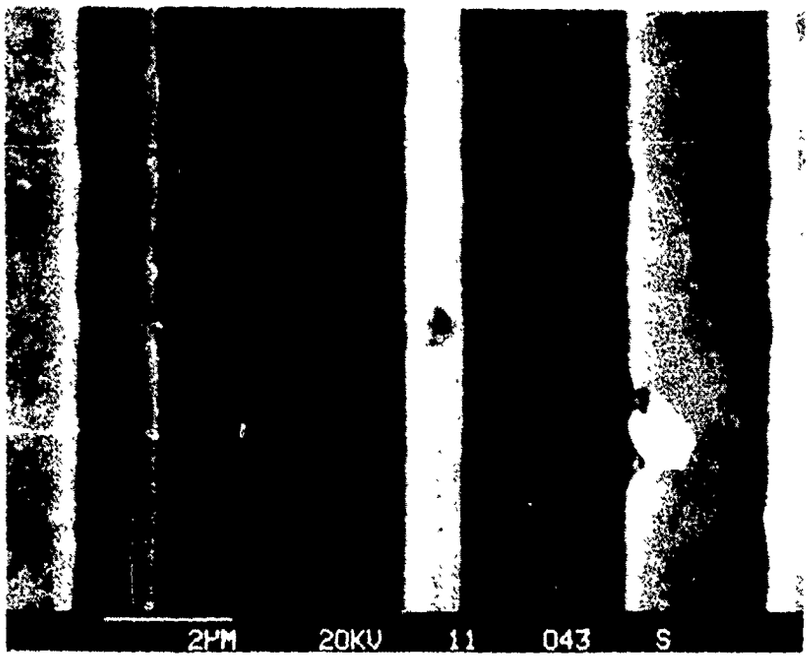


Figure 23. Electromigration Site on 1μ Line, GaAs Wafer 3, Sample G-3-1-1-4

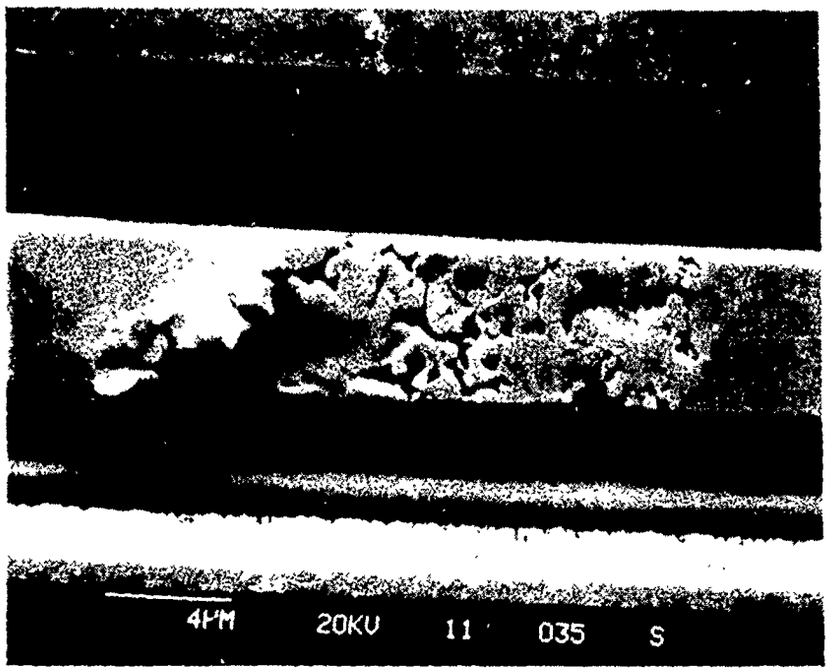


Figure 24. Electromigration Site on 4μ Line, GaAs Wafer 3, Sample G-3-1-1-3

Figure 25 shows a typical damage site from a GaAs wafer 5 sample. The disappearance of the thin gold layer is evident on samples from both GaAs wafers 2 and 5. Like GaAs wafer 2, samples from GaAs wafer 5 showed extensive electromigration damage.

Figures 26 and 27 show typical damage to a sample from silicon wafer 1 and Figure 28 shows typical damage to samples from silicon wafer 2. Electromigration on both silicon wafers was markedly different from electromigration on the GaAs wafers. Figure 27 represents the worst case damage found on either silicon wafer.

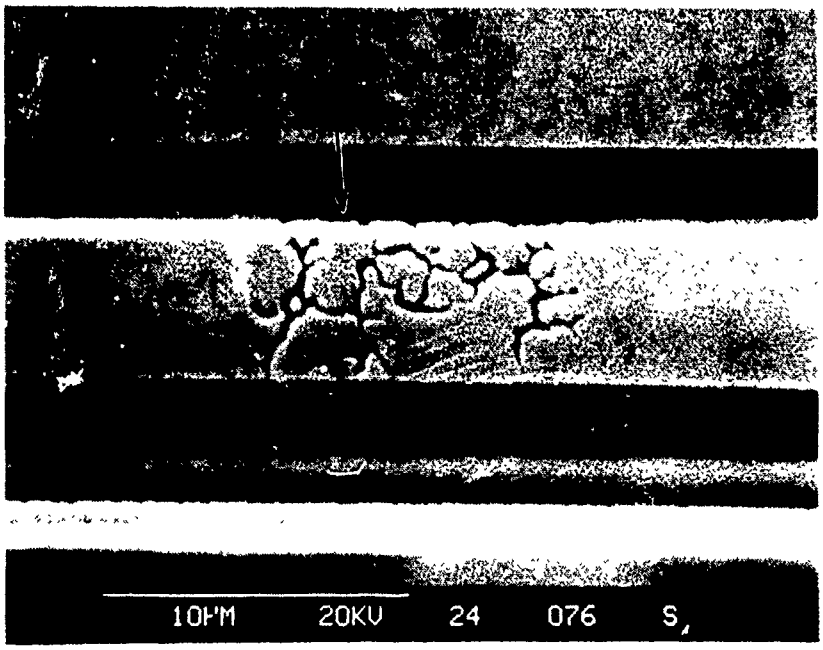


Figure 25. Typical Electromigration Site on a 4μ Line, GaAs Wafer 5, Sample G-5-1-1-1

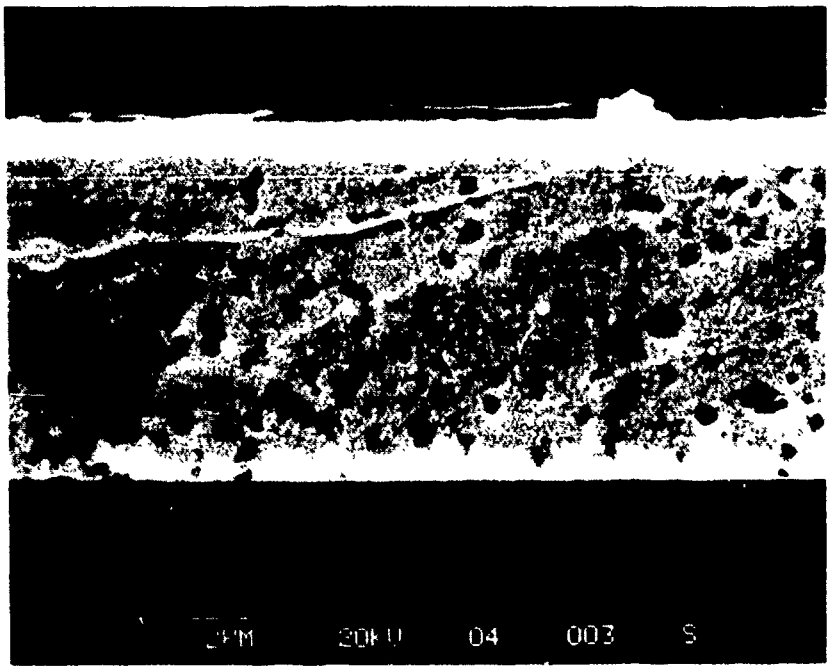


Figure 26. Typical Electromigration Site on 3μ Line, Silicon Wafer 1, Sample S-1-1-4-3

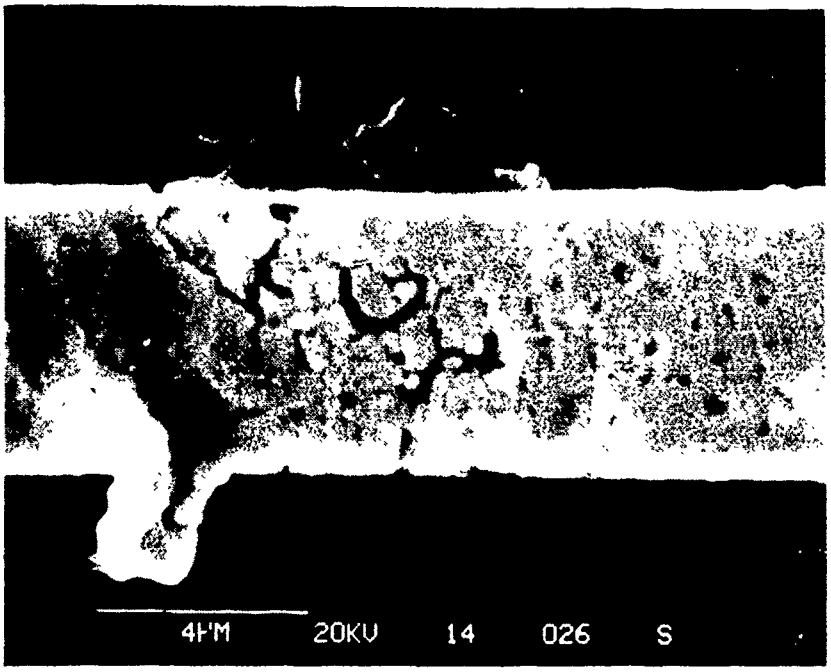


Figure 27. Worst Case Electromigration Site on 4μ Line, Silicon Wafer 1, Sample S-1-1-4-1

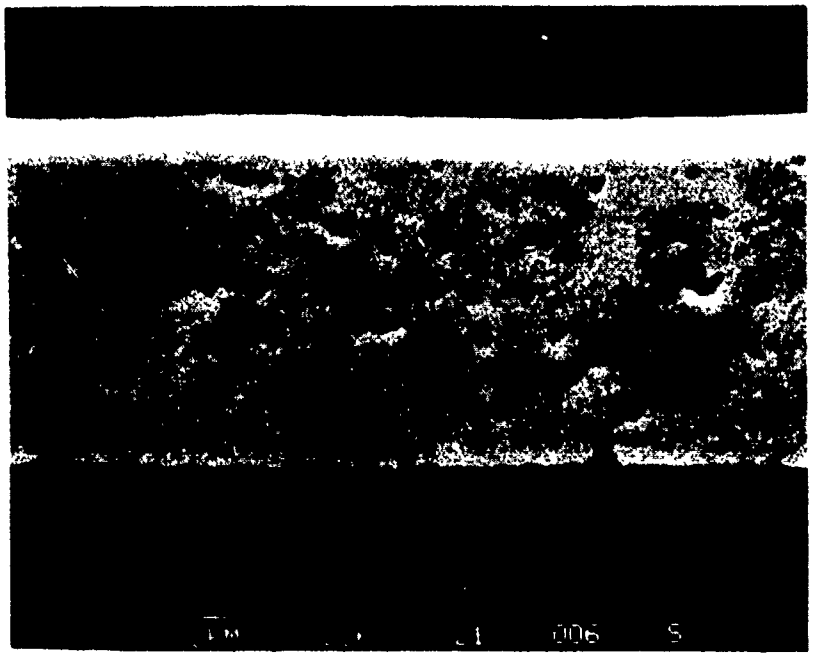


Figure 28. Typical Electromigration Site on 4μ Line, Silicon Wafer 2, Sample S-2-1-1-1

7.2 AUGER ANALYSIS

AUGER depth profiles of selected samples were done to gain insight into the voiding process. Figures 29 and 30 are profiles taken of unstressed samples from wafers 2 and 3. The layered Ti/Pt/Au structure of wafer 3 is evident in Figure 29. Wafer 2 is also as expected; the TiW is a single alloy layer between the GaAs and the gold. The thickness of the gold is greater on wafer 2, approximately 50% thicker, confirming the measurements made at deposition.

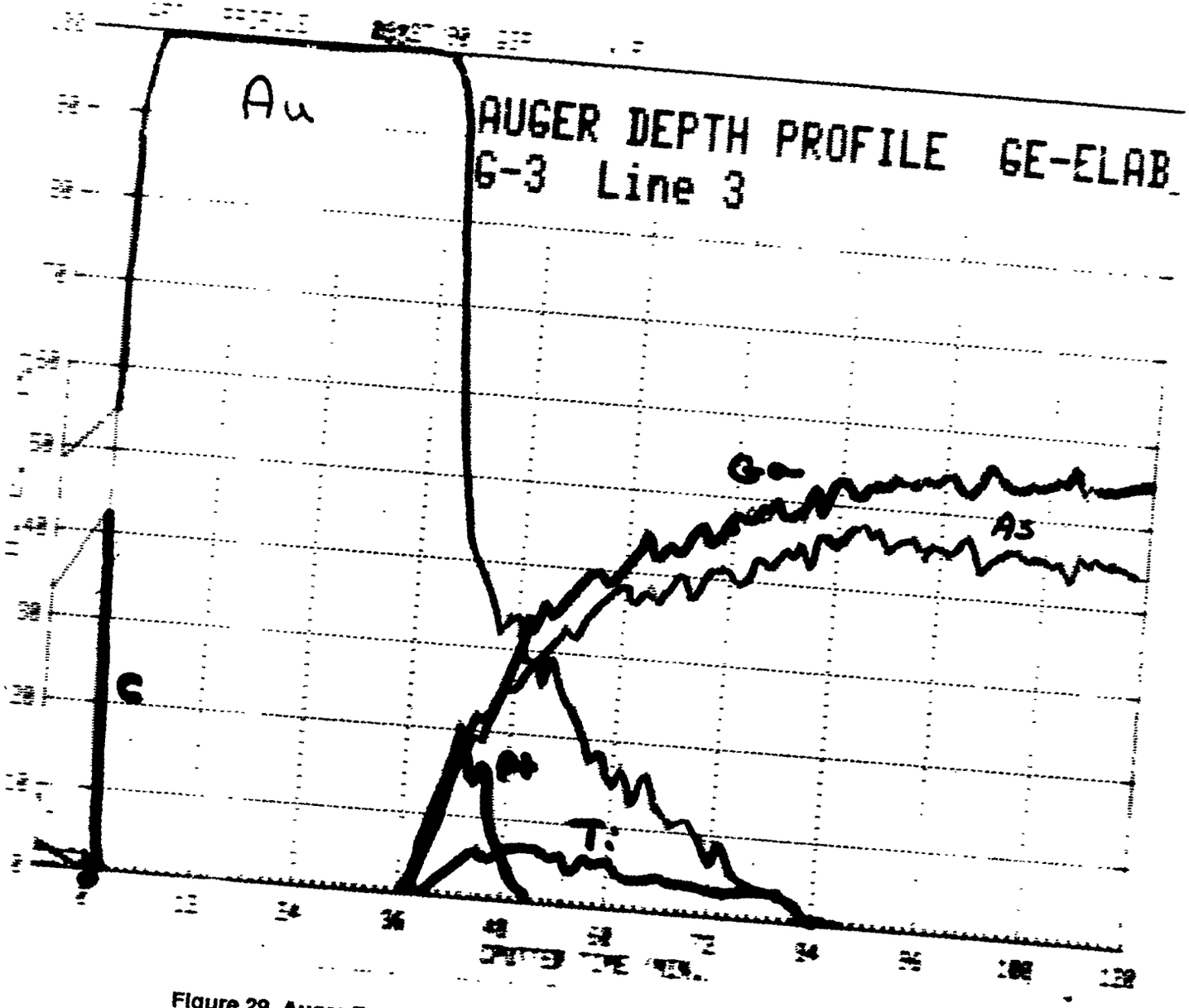


Figure 29. Auger Profile of Unstressed 4μ Line, GaAs Wafer 3

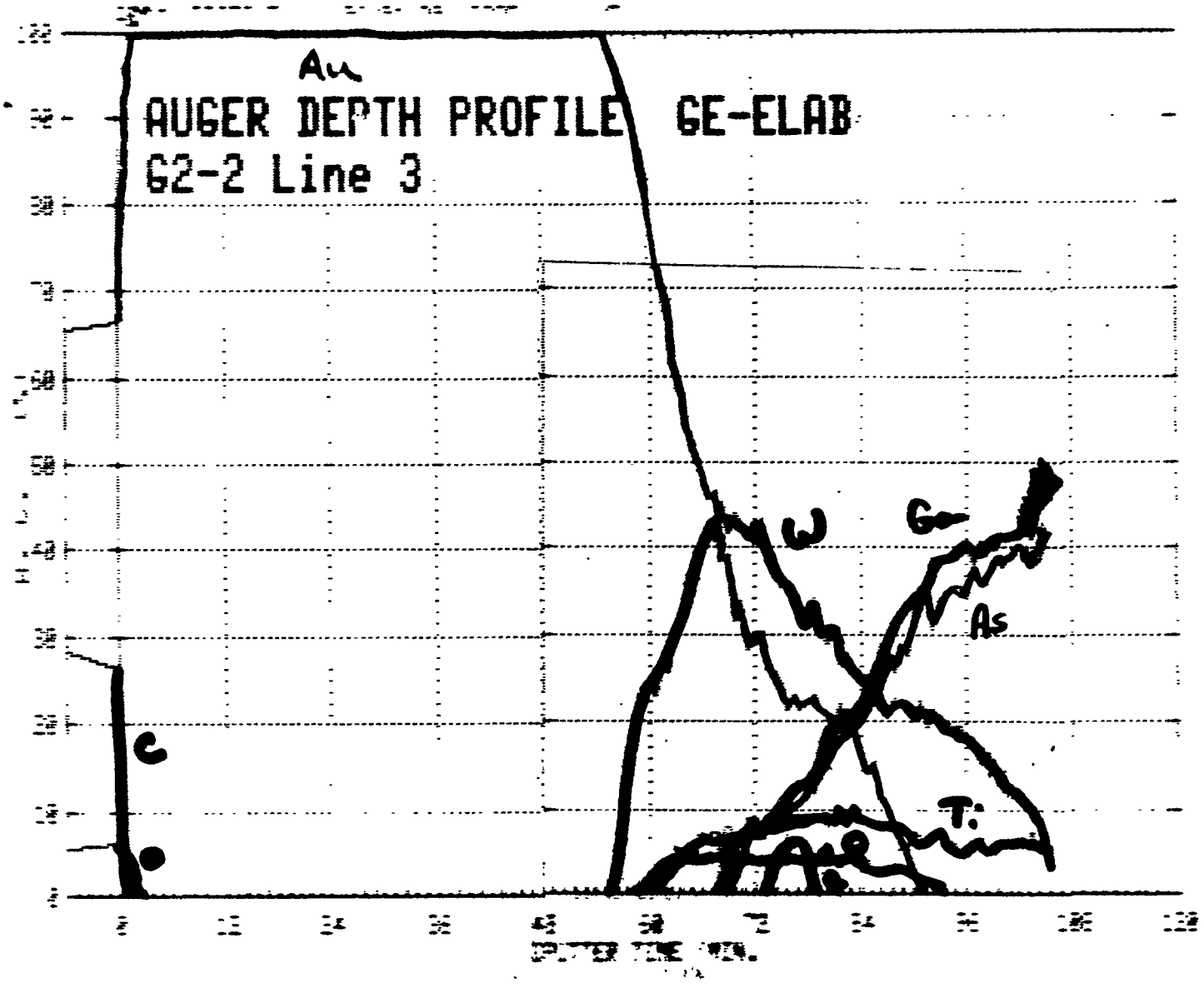


Figure 30. Auger Profile of Unstressed 4μ Line, GaAs Wafer 2

Figure 31 is a SEM photograph of an area on sample G3-1-1-3 which was profiled in the AUGER after the life test. Four points were profiled, as shown. Points 1 and 3 are, respectively, upstream and downstream of the voided area; point 2 is in the vicinity of a void; and point 4 is a hillock. Figure 32 is the profile for point 1, upstream from the voided area. Each of the layers is visible, although the Pt layer is thinner for this wafer. Figure 33 shows the profile for point 3, downstream from the voided area. No Pt or Ti is visible at the interface. Figure 34 shows the profile for point 2, the voided region itself. The gold is thinner, as might be expected, and again there is no evidence of Pt or Ti. Figure 35 is a profile for the hillock which was started after completion of the other profiles. Because of the thicker gold at the hillock, the profile at this spot is just at the interface of the GaAs. A significant amount of Ti is present at the interface, but Pt is not visible. It is possible that the Pt peak has been passed prior to the beginning of this profile. From the above results, it would appear that Ti and Pt have migrated within the line and is missing in the void area.

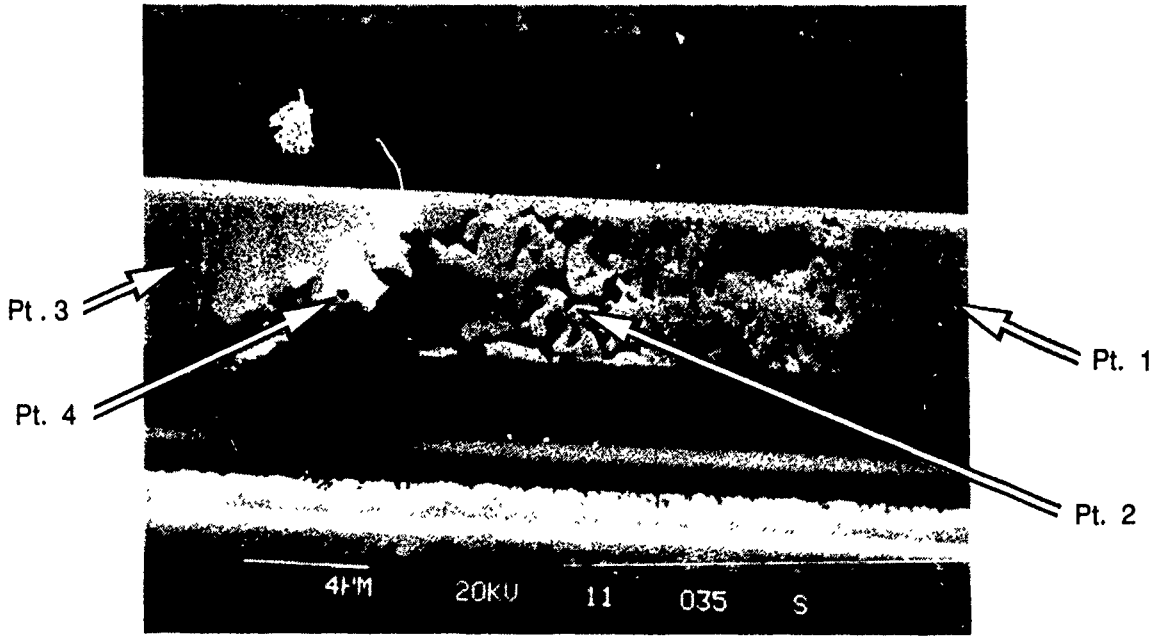


Figure 31. Electromigration Site on 4μ Line, GaAs Wafer 3, Sample G-3-1-1-3. Auger analyses were made at Points 1, 2, 3, and 4.

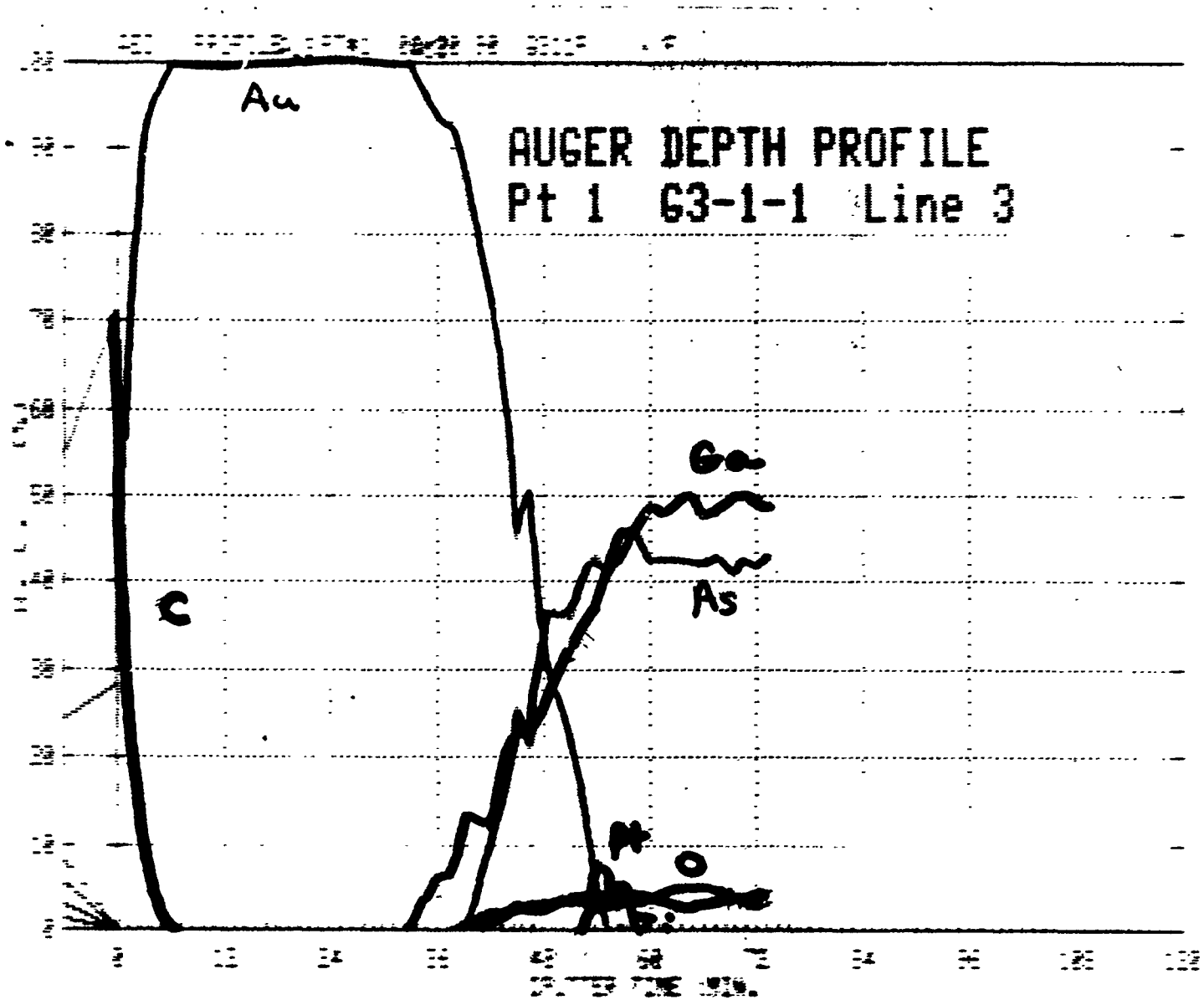


Figure 32. Auger Profile of 4μ Line, GaAs Wafer 3, Sample G-3-1-1-3, Point 1 in Figure 31

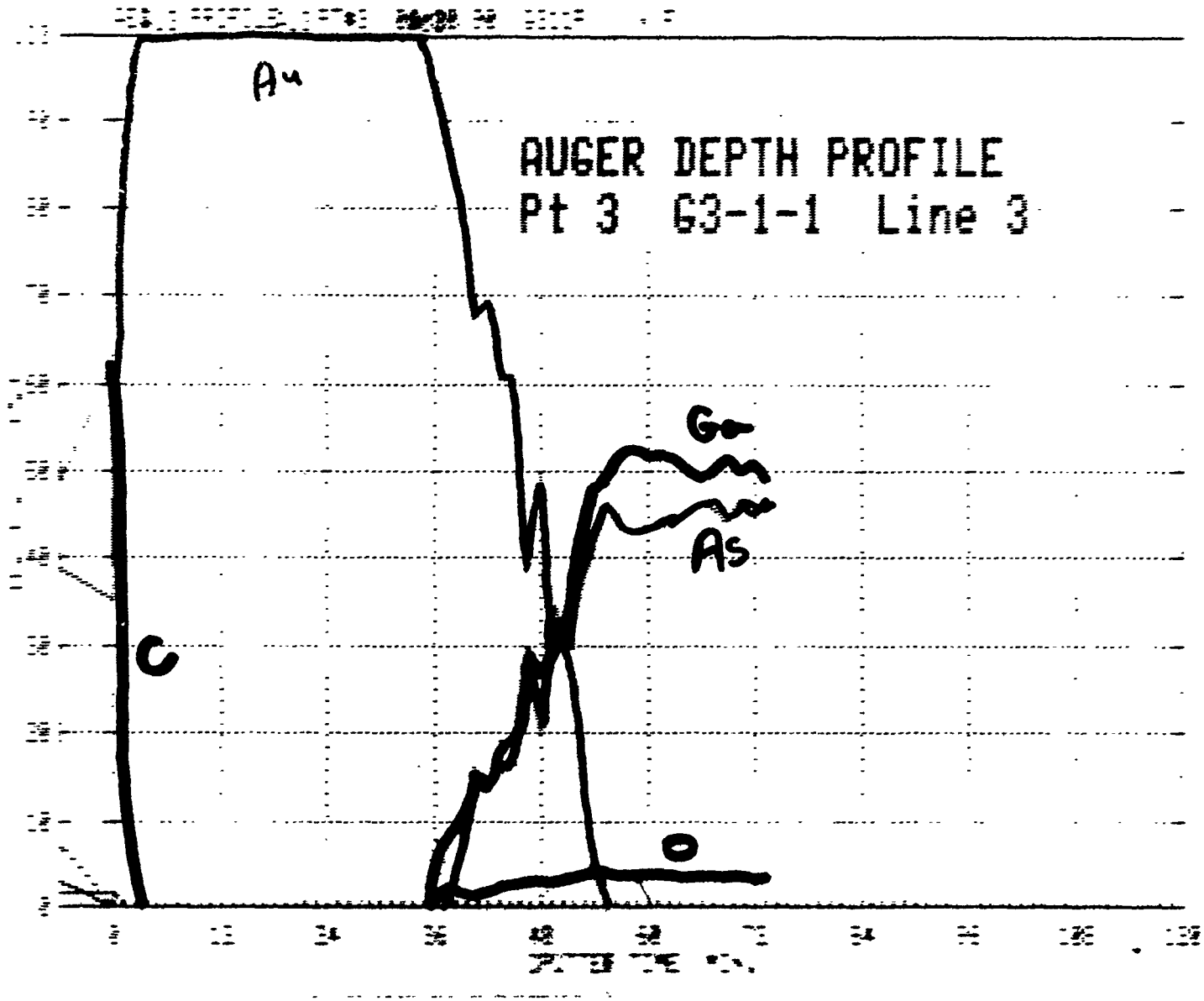


Figure 33. Auger Profile of 4μ Line, GaAs Wafer 3, Sample G-3-1-1-3, Point 3 in Figure 31

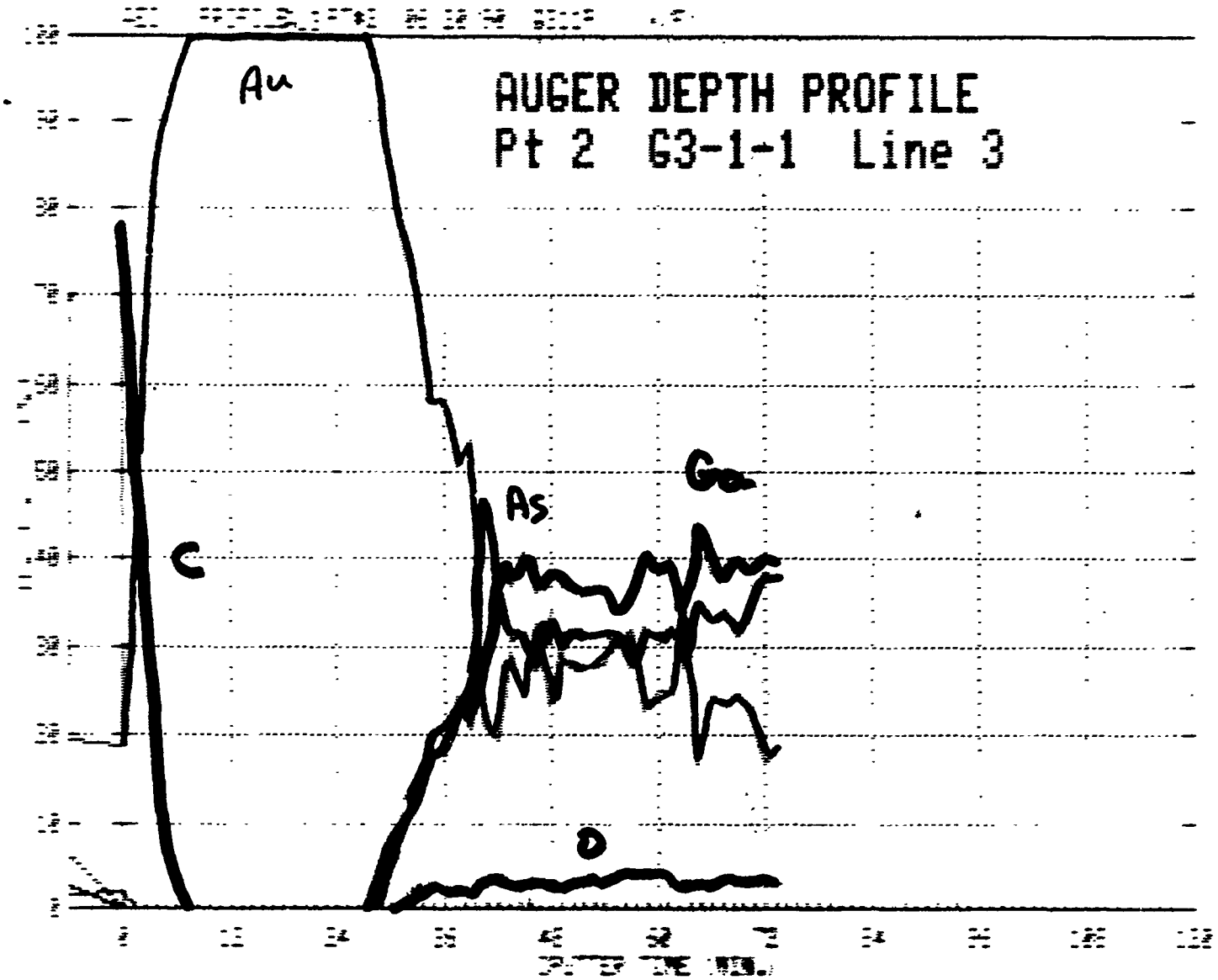


Figure 34. Auger Profile of 4μ Line, GaAs Wafer 3, Sample G-3-1-1-3, Point 2 in Figure 31

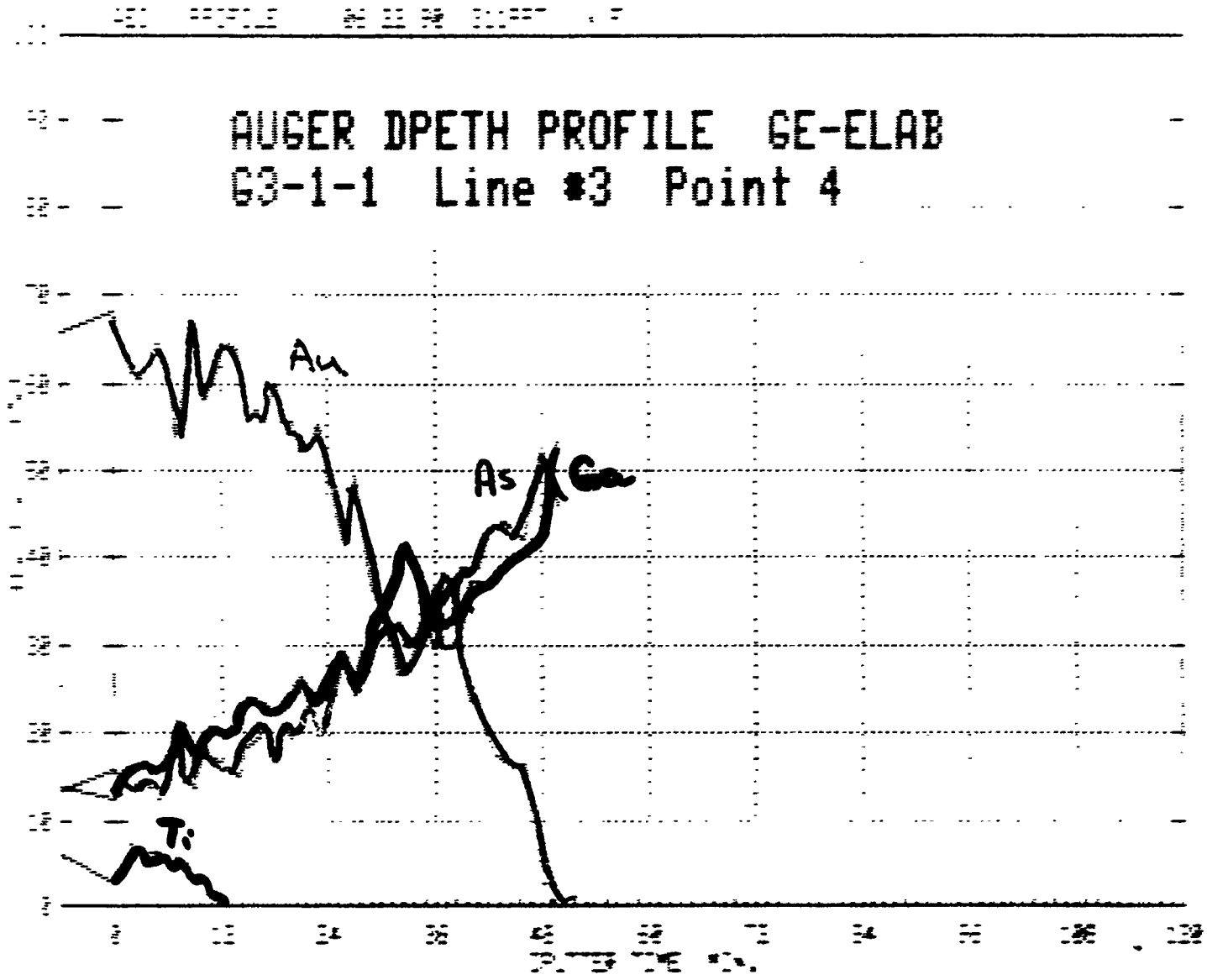


Figure 35. Auger Profile of 4μ Line, GaAs Wafer 3, Sample G-3-1-1-3, Point 4 in Figure 31

Figure 36 is a SEM photograph of a voided area on line G2-2-5-1, a transistor line with a thick TiW barrier layer. Electromigration has led to gross voiding of the gold layer. Since the line is still continuous, the TiW layer must still be intact. A fringe of thin metal exists on the edge of the line, a common feature of all of the TiW lines. In the region of the voiding, this fringe is missing. This sample was AUGER profiled at four points, as shown in the figure. Figure 37 shows the profile for point 1, the center of an island of gold. The TiW layer is clearly visible at the interface. The profile for point 2 is shown in Figure 38. The profile is similar, except for a layer of carbon at the interface. The origin of the carbon is not understood. Figure 39 shows that the metal on the fringe is a thin gold layer with TiW underneath. In the area where the fringe appears to be missing (Figure 40), the gold has migrated away but the TiW remains. There appear to be relatively high carbon levels at the interface of both points 3 and 4.

Gross voiding in the gold occurs for both the TiPt and TiW samples and without the barrier layers the lines would have become discontinuous well before the test was terminated. There is evidence that the TiPt does migrate within the gold, but apparently not sufficiently to cause discontinuities. The TiW appears to be stable. The presence of carbon near the GaAs interface for the TiW sample may be related to the two-step process used in metallizing the samples. Since it was necessary to sputter the TiW and the bulk of the gold is deposited by evaporation, these samples were first sputtered with TiW and a thin layer of gold, removed from the sputterer and put in an evaporator for the final gold build up. The carbon seen at the interface may have been adsorbed on the surface during the interval between sputtering and evaporation when it was exposed to the air.

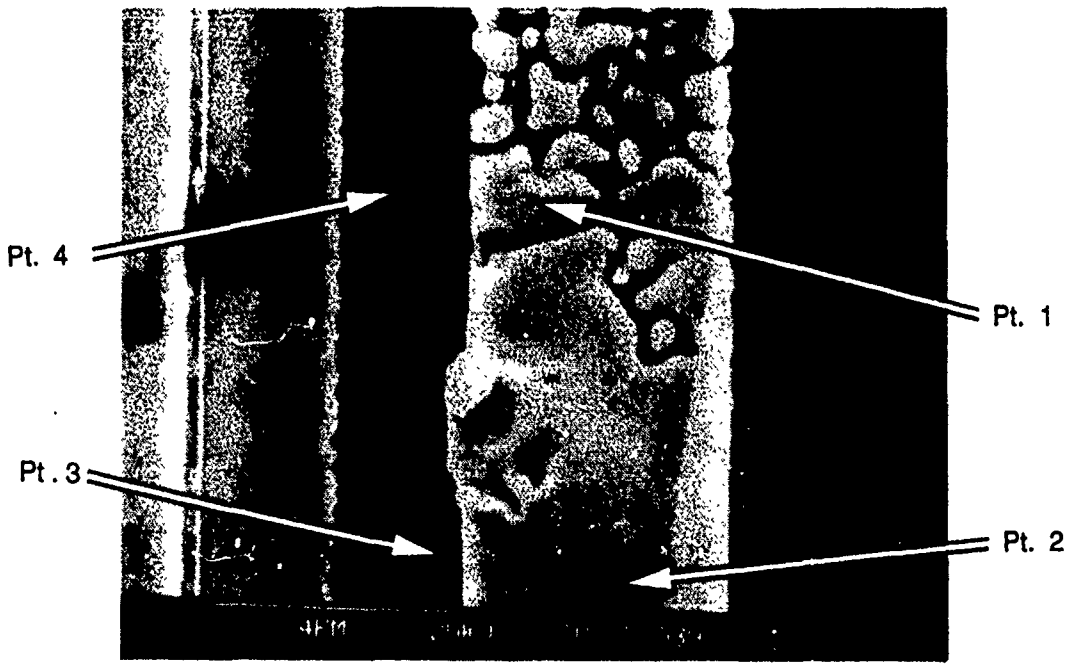


Figure 36. Electromigration Site on 4μ Line, GaAs Wafer 2, Sample G-2-2-5-1. Auger analyses were made at Points 1, 2, 3, and 4.

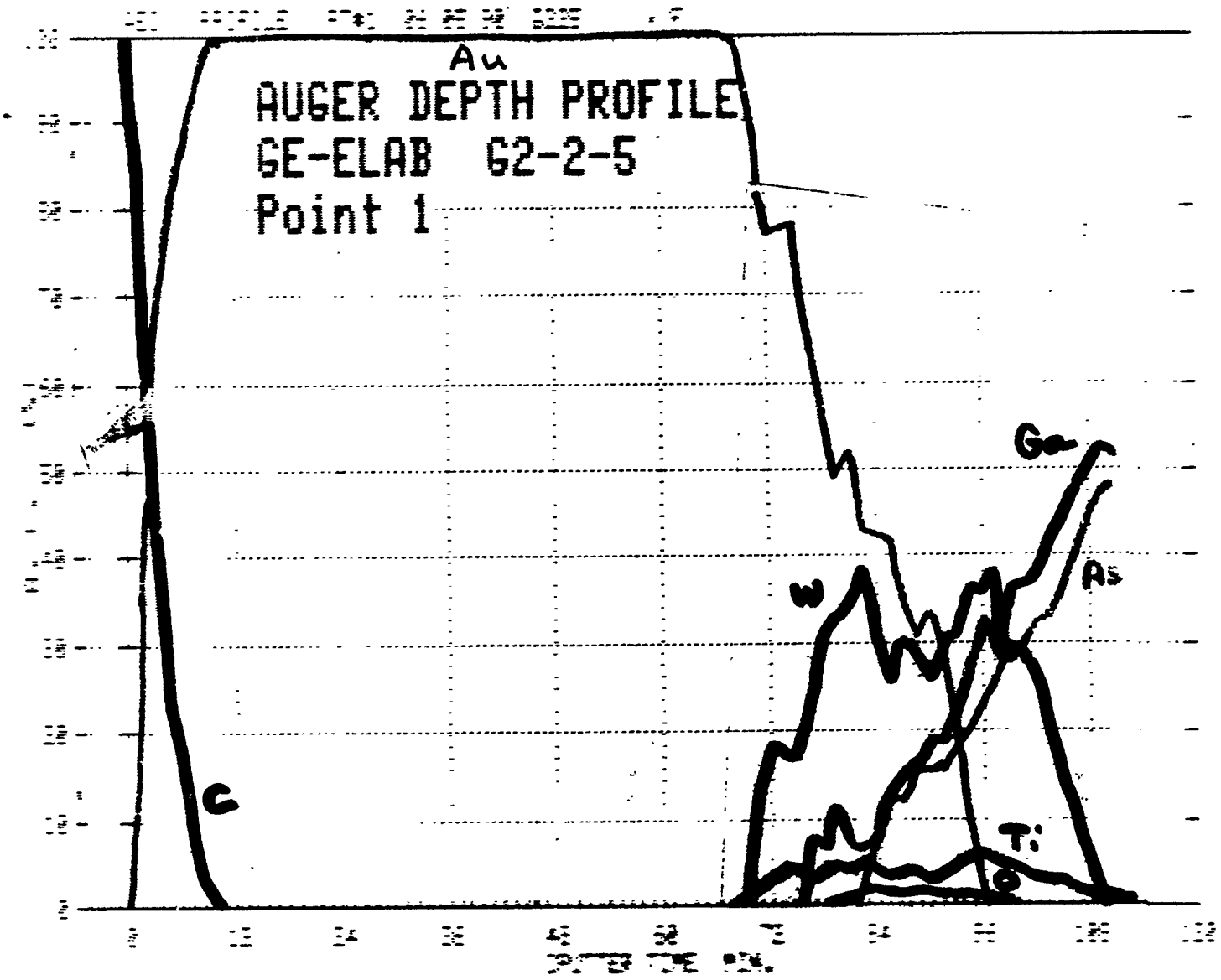


Figure 37. Auger Profile of 4μ Line, GaAs Wafer 2, Sample G-2-2-5-1, Point 1 in Figure 36

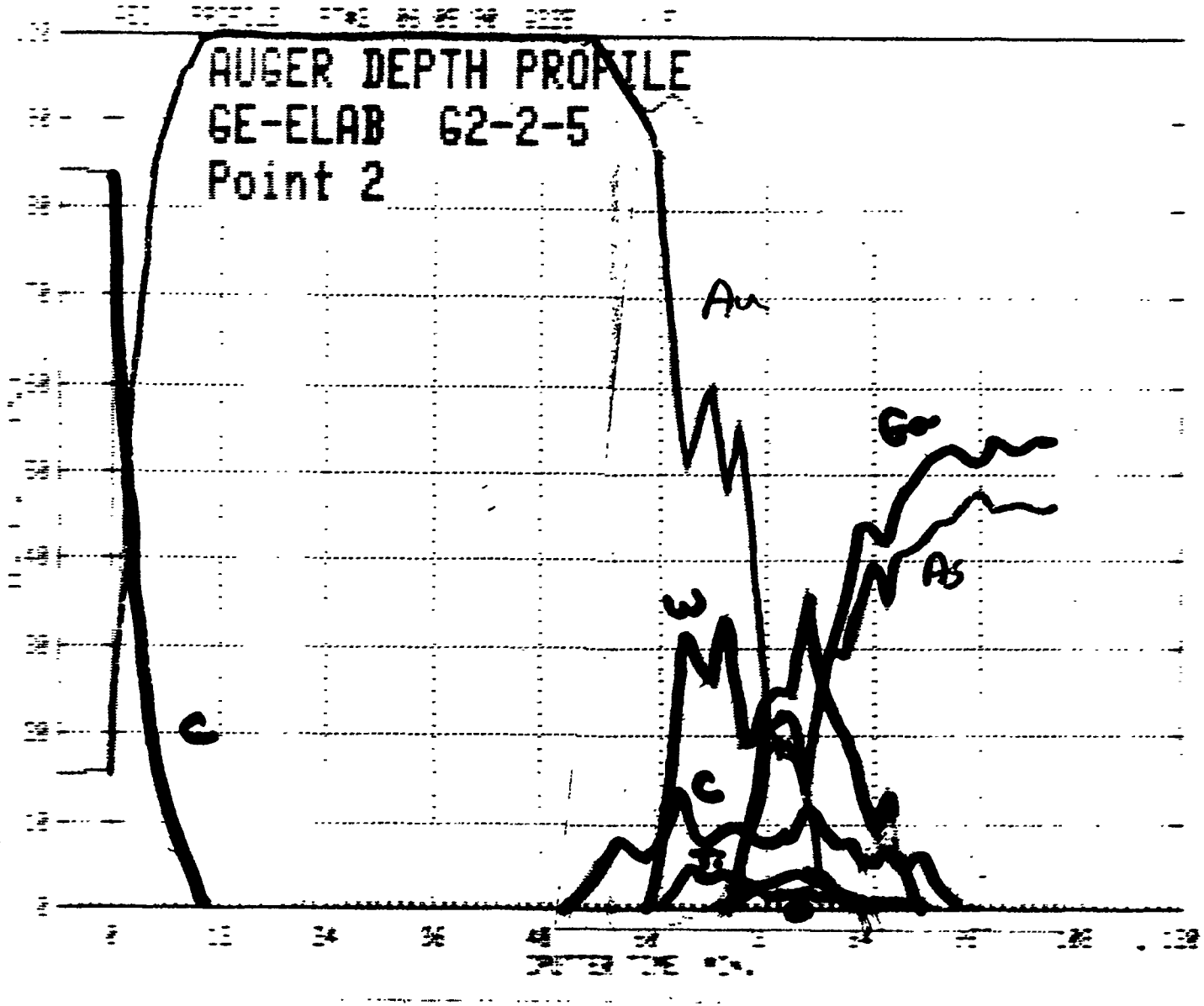


Figure 38. Auger Profile of 4μ Line, GaAs Wafer 2, Sample G-2-2-5-1, Point 2 in Figure 36

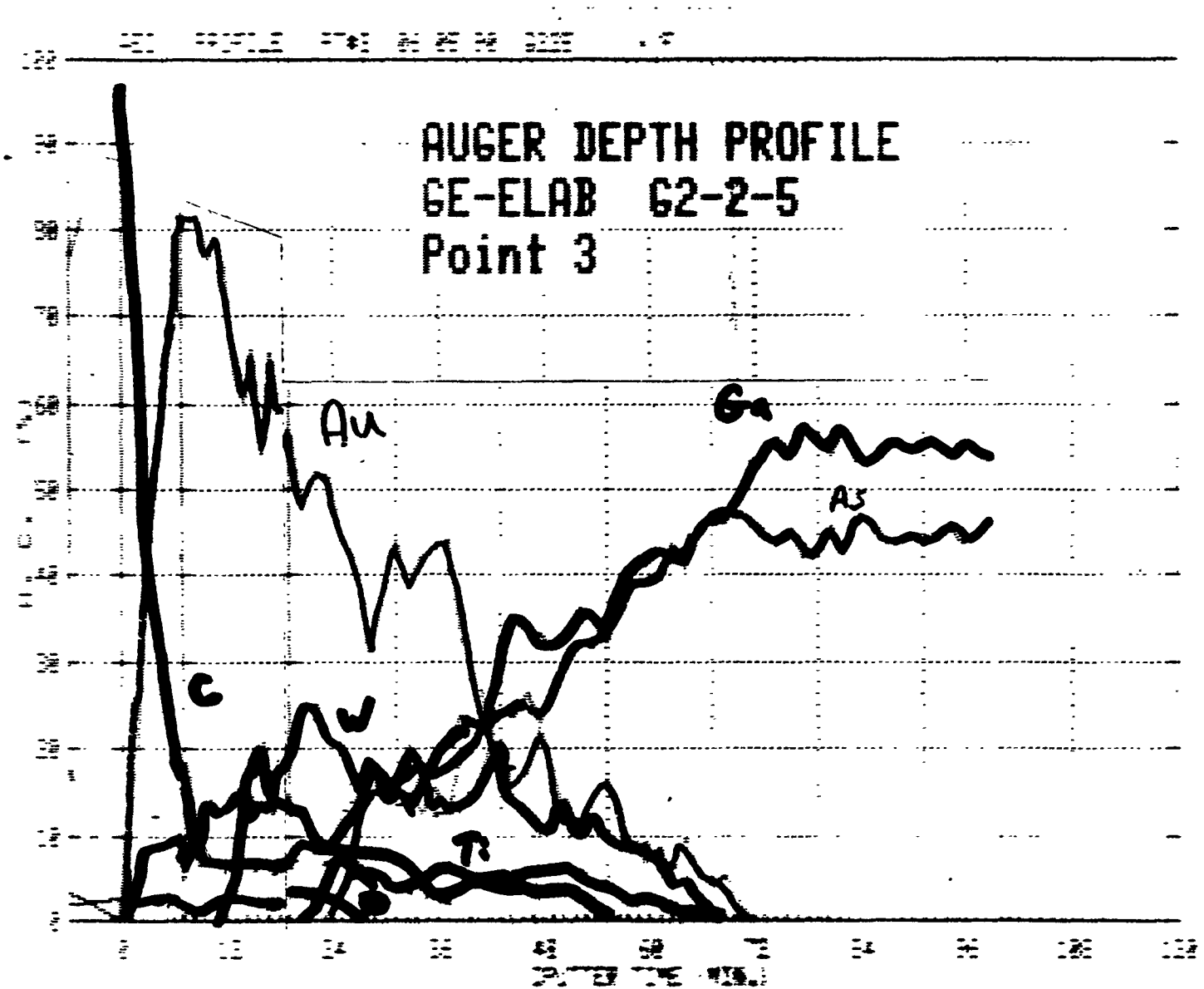


Figure 39. Auger Profile of 4μ Line, GaAs Wafer 2, Sample G-2-2-5-1, Point 3 in Figure 36

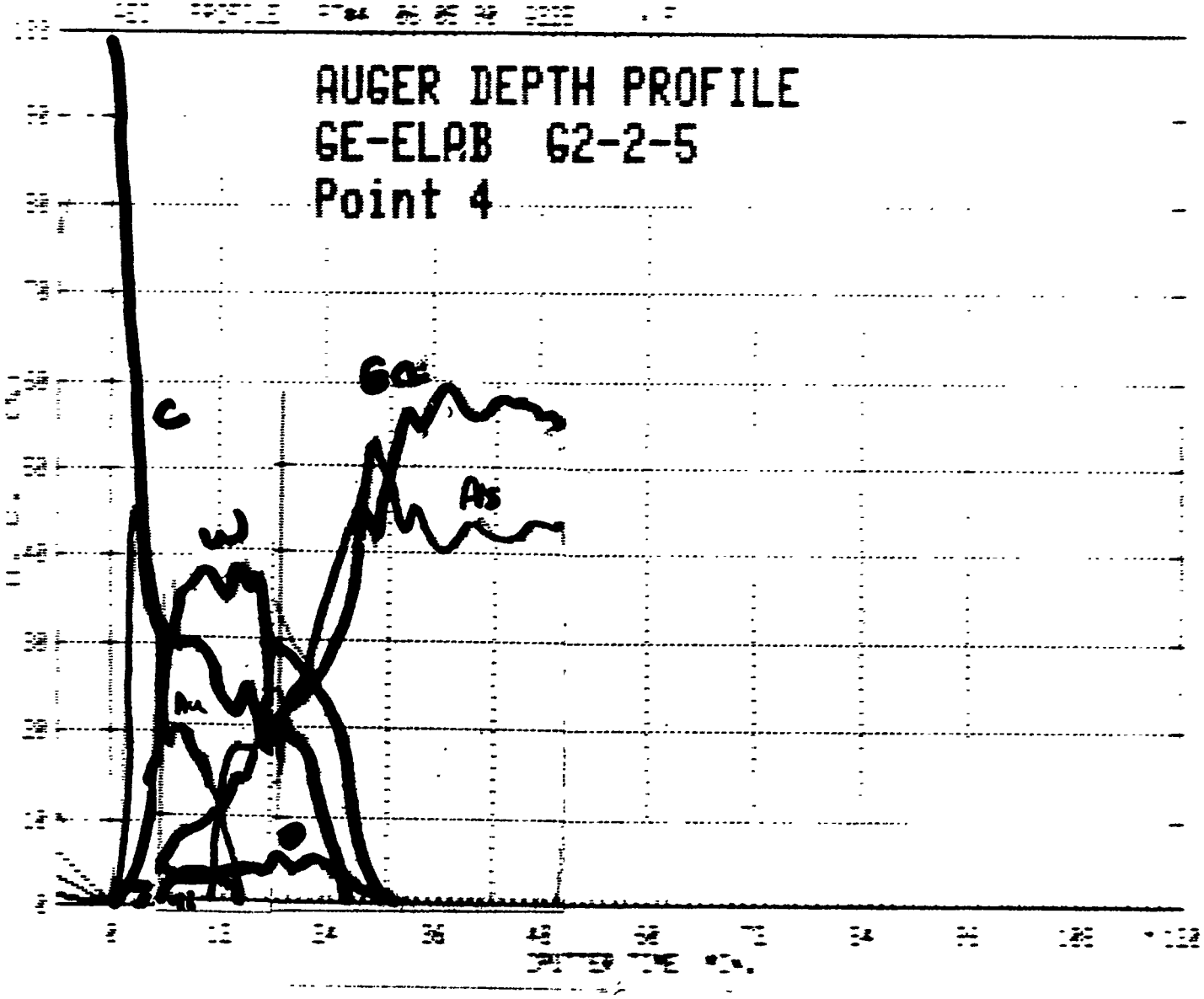


Figure 40. Auger Profile of 4μ Line, GaAs Wafer 2, Sample G-2-2-5-1, Point 4 in Figure 36

8 Conclusions and Recommendations

8.1 VOIDING DUE TO ELECTROMIGRATION

Our results indicate that voiding of gates does not lead to degradation of FETs with TiPt/Au or TiW/Au gates at channel temperatures of 160°C and at current densities of up to 4.5x10⁶A/cm² for durations of 1000 hours. Gross voiding was observed in these samples but, because of the continuity of the barrier layer, the FETs remained functional. The FETs with 1μm long gates were particularly resistant to voiding, showing only very localized notching in some samples. Since these stress conditions are many times more stressful than would be encountered in use, gate voiding due to electromigration should not be a problem for this technology.

Figure 41 is a curve of mean-time-to-failure data for sputtered TiW-Au films published by Blair et al[9] in 1972. This data was taken at a stress temperature of 150°C, similar to that used in the present study. The curve of pure Al lines is also presented for comparison. Unannealed Au films stressed at $3x10^6$ A/cm² failed in a few tens of hours while annealed films survived less than 100 hours. Aluminum films would be expected to fail by 10 hours. These times are much shorter than those observed in the present tests for the same stress conditions.

The reason for this difference lies in the much greater grain size of the films used in the present tests. The samples tested by Blair et al were sputtered films with grain sizes of the order of 0.2μm, while the present films had grain sizes of the order of 1.0μm. Since

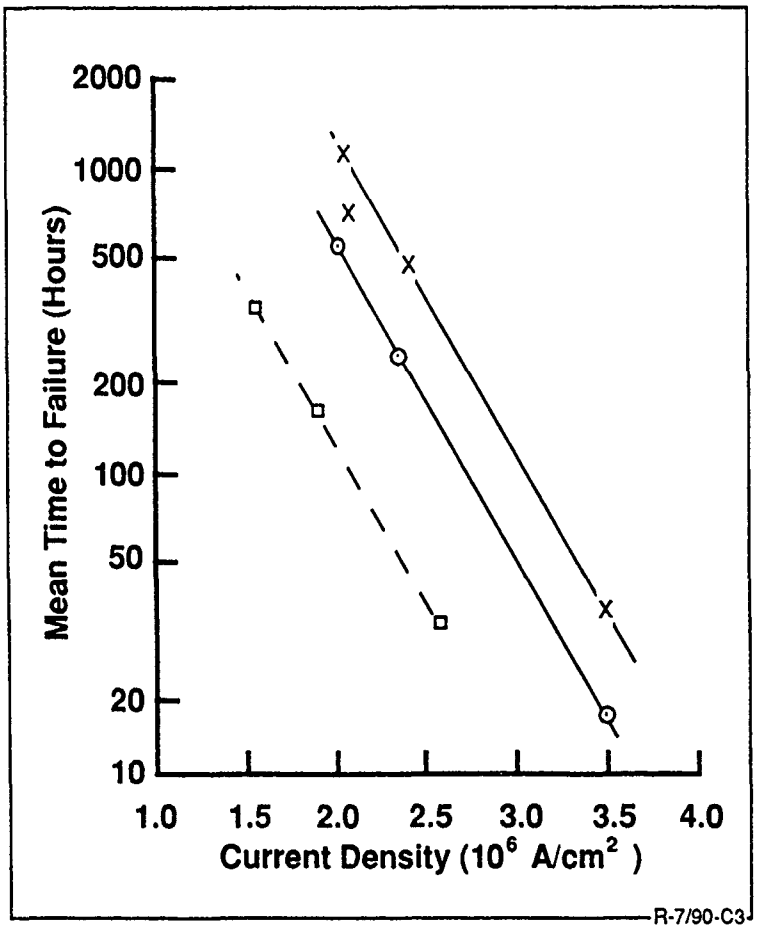


Figure 41. Mean Time to Failure vs. Current Density for Sputtered (18-mTorr Ar Pressure) Gold Films. X—Au-A; Θ—Au-U; data for aluminum films □ are also shown for comparison. Resistor stripes were tested in 150°C ambience.

electromigration at these temperatures is primarily grain boundary migration, the sputtered films would be expected to be much more susceptible to electromigration. The grain size also explains why the 1 micron wide lines had little voiding. Based on the measured grain size distribution, each line should have multiple large grains block grain boundary flow along its length. If the separation of these grains is small enough, i.e., less than the critical length for stress buildup, no electromigration will occur. Our results indicate that for most lines this is the case.

We have observed that the samples with the TiW barrier layers degrade faster than those with the TiPt barrier layers and have more extensive voiding. This is probably related to the different processing used to fabricate these samples. Since lift-off techniques are used to form the gates of the FETs, vapor deposition, not sputtering, is used to deposit the gate metal. Vapor deposited metal will not have good step coverage of the photoresist layer and will therefore allow lift-off to succeed. Since TiW is very refractory, it was necessary to sputter the barrier layer and then remove the wafers from the sputtering unit and transfer them to an evaporator for the bulk of the gold deposition. After sputtering the TiW, a thin Au layer was sputtered on the samples before removing them from the sputtering unit to prevent oxidation and assure good wetting of the evaporated film. This thin layer will have a very small grain size, comparable to that reported by Blair et al. Therefore, while the top of the lines appears to have a large grain size, the metal at the bottom will not and electromigration can progress rapidly through the bottom layer and spread to the top. As indicated in Figure 20, many of the voids appear to start at the bottom of the layer, confirming this hypothesis.

Electromigration of Au on GaAs is not more rapid than that of Au on silicon. The GaAs/TiPt samples degraded slower than the Si/TiPt samples. It was anticipated that, because of the higher thermal conductivity of the silicon, the lines on Si would have less self-heating and less electromigration damage. The self-heating measurements indicate that the opposite is true, the silicon lines are approximately 10°C hotter than the GaAs lines. This is due to the presence of the SiO_2 on the silicon, which has a very low thermal conductivity. Therefore, even though the silicon itself has a higher thermal conductivity than GaAs, this is more than compensated for by the fact that in the GaAs device the metal is deposited directly on the GaAs.

8.2 ELECTROMIGRATION ENHANCED INTERDIFFUSION

There is no evidence that interdiffusion of the gate metal into the GaAs ("gate sinking") is appreciably enhanced by high gate-source current densities at 150°C. The voltage drop across the Schottky junction was changed by a few percent at most, probably within our ability to measure it, and the transistor characteristics and leakage currents changed very little, if any. The gate sinking phenomenon is normally observed at very high temperatures (>225°C) and has an activation energy of about 1.5 ev. Since barrier penetration is involved in both normal gate sinking and electromigration enhanced gate sinking, it may be expected that the same activation energy will apply for both processes. If so, the electromigration enhanced interdiffusion process will occur 500 times faster at 225°C than at 150°C. Since we observed significant FET degradation in 13 hours at 225°C at a current density of 1×10^6 A/cm² in our earlier experiment, we might expect to see a similar effect after 6500 hours at 150°C for the same current density. While the lines in our present experiment were stressed at several times this current density, apparently the acceleration due to increased current density was not sufficient to compensate for the deceleration due to temperature decrease.

It is still possible that the gate sinking process is accelerated by high gate current densities and that this mechanism will limit the life of RF power devices operating at high gate currents. **It is recommended that another experiment be run at temperatures above 200°C in which the time to failure and activation energy of FETs is determined as a function of forward gate current.**

8.3 SUMMARY

Voiding of TiPt/Au and TiW/Au gates due to electromigration is not a life-limiting mechanism, particularly for evaporated gold and gate lengths of 1μm or less. Since GaAs FET gates are deposited directly on the GaAs and not on SiO_2, the self-heating in the

gates is smaller than for similar lines on oxide coated silicon, even though the thermal conductivity of GaAs is lower than that of silicon. Electromigration enhanced interdiffusion of gate metal and GaAs is not significant after 1000 hours at 150°C and with gate source current densities up to 4.5×10^6 A/cm^2. Further evaluation of this phenomenon is needed at higher temperatures.

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