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Full Surface Testing of Grazing Incidence Mirrors

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Third Quarter Report: Introduction and Executive Summary

Having achieved the "Full Surface Testing of Grazing Incidence Mirrors" (FSIS) goals of the first two quarters of this project;

* Prototype design of the FSIS (completed),
* Procurement and testing of components (continuing), and
* Mathematic and algorithm development (continuing),

We are well positioned to achieve project targets for the third and fourth quarters. The third quarter work plan is especially important because it represents the beginning of the integration of the sub-projects which include:

* Procurement and testing of components (continuing),
* Mathematics and algorithm development for aspheric surfaces (continuing),
* Interferogram data reduction algorithms (starting),
* Construction of first prototype (starting),
* Automated operation software development (starting).

During the fourth quarter the above sub-projects will be completed and integration and testing of the prototype will be carried out in the fifth and sixth quarters. Therefore, the third quarter has been a critical period in terms of initiating the project integration, and we report these objectives have been achieved.

Also during the fourth quarter procurement, testing, and integration of components will continue. After this period, a small reserve fund will be kept available for minor procurement during the upgrading, optimization, final testing, and modification phases. These aforementioned tasks will take place during the fifth through eighth quarters.

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Third Quarter Report: Contents

Due to objectives achieved this report is be extended and will reflect the technical progress. Therefore, this report is divided into two parts, A and B. Part A describes:

1. Prototype design and construction and

2. Mathematics development for aspheric surfaces.

Part B is further divided into two sections, I and II. Section I describes automated operation of the hardware of the electrical and digital system which is further divided into two parts:

1. Positioning of the tables and driver and

2. Data acquisition device and controller.

Section II describes the software and is further divided into two parts:

1. Automated operation software development and

2. Data acquisition device driver design.

1.0 PROTOTYPE DESIGN AND CONSTUCTION

During the past period the first design of the interferometric head and mechanical frame has been completed.

Construction of this first head and frame has been initiated. It will be completed during the next quarter period and will be ready for initial testing.

A schematic of the interferometric head is shown in Figure 1 and includes the following principal components:

- Laser Source
- Spatial Filter Assembly
- Collimating Lens L1
- Focusing lens L2
- Beam Splitting Assembly
- Wavefront Shearing Device (Grating)
- Cylindrical Beam Forming Assembly
  (Large Collimating Lens L + Cylindrical Reference Lens CL)
- Imaging Lens L3
- CCD Camera.

The mechanical frame that holds the interferometric head has been constructed with the aid of Klinger X-95 profile components. It will be further ugraded when the head is ready to be mounted and tested during the next quarter period.

2.0 MATHEMATICS FOR ASPHERIC SURFACES

Mathematics are being developed for expressing a far off-axis conic mirror segment. The computation will be completed during the next quarter period.

The mirrors are characterized by a long rectangular, cylindrical-like shape. The surface is being mathematically expressed as a cylindrical function + an expansion that approximates to high order the deviation from the actual conic function. It is this deviation that is being measured in the normal incidence interferometric approach developed here.

Figure 2 shows the geometry of the parent conic and the mirror segment, including the global and local coordinate systems used in the computation.

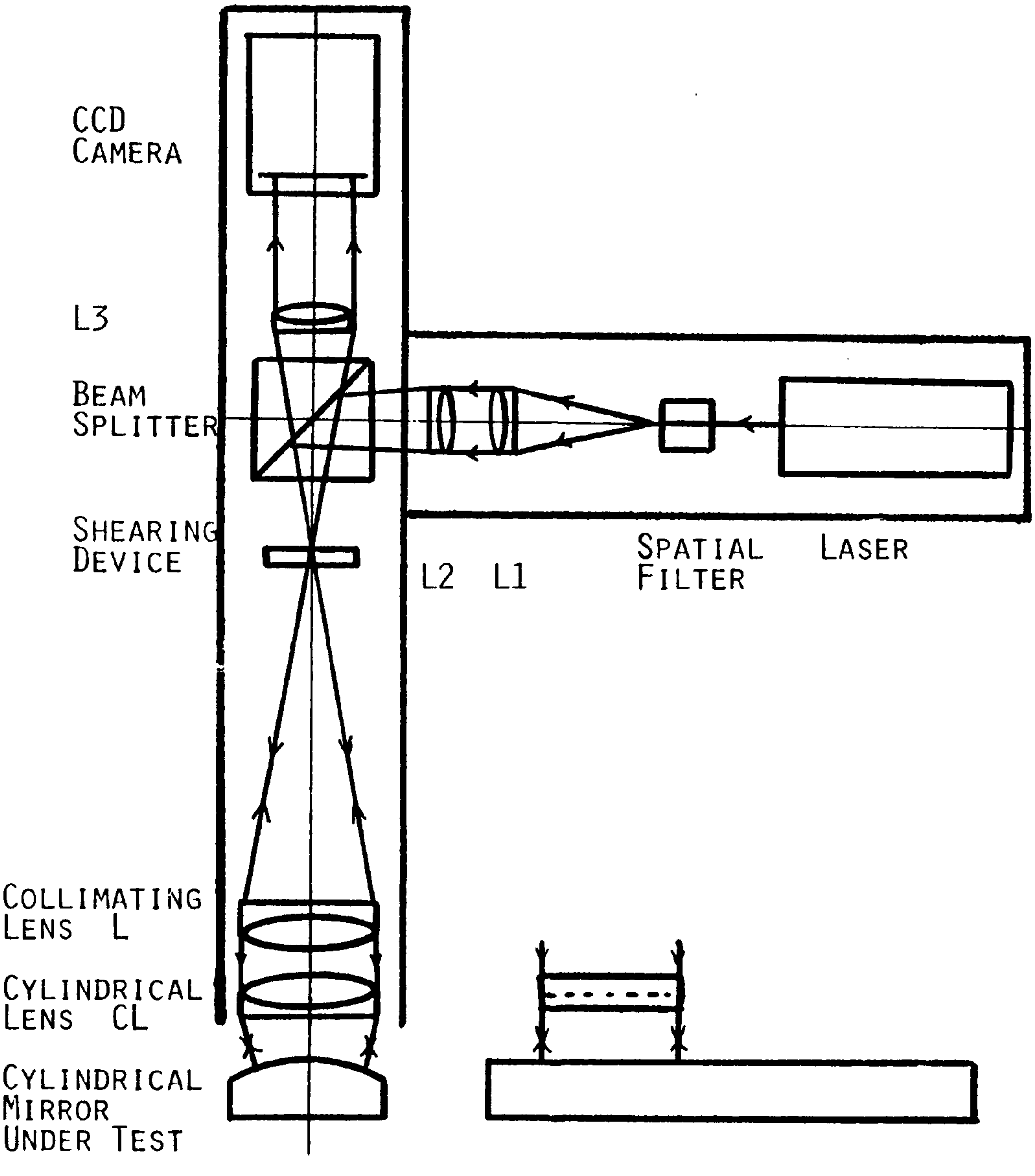


FIGURE 1: SCHEMATIC DIAGRAM OF INTERFEROMETRIC HEAD

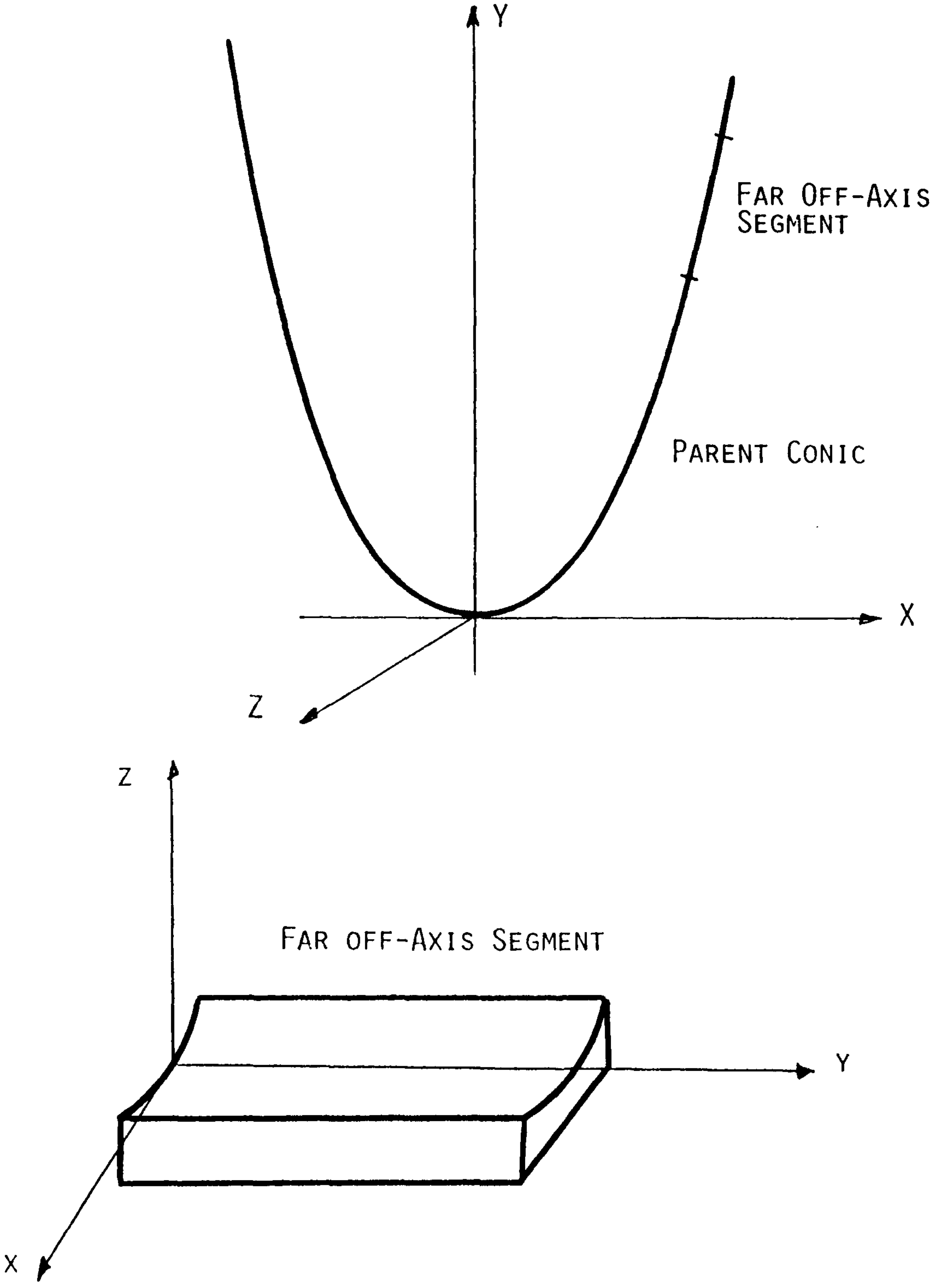


FIGURE 2: GEOMETRY AND COORDINATE SYSTEM FOR OFF-AXIS CONIC SEGMENT

ELECTRICAL AND DIGITAL HARDWARE AND SOFTWARE DESIGN

I. AUTOMATED OPERATION HARDWARE (ELECTRICAL/DIGITAL) SYSTEM

The Automated Operation Hardware System block diagram is shown in figure 1. It includes the positioning device controller and the camera/frame buffer device. The positioning device controller is stepping motor/controller. The block diagram of this controller device is in figure 2. The details of the mechanism of this device will be addressed in the following section. The camera/frame buffer also will be specified.

I-1 Positioning Devices and Driver

The Positioning device which the test mirror is mounted on, is a translation stage, and is equipped with stepping motor. In the following section, I would like to discuss these positioning device in details.

BLOCK DIAGRAM OF THE ELECTRICAL/DIGITAL SYSTEM

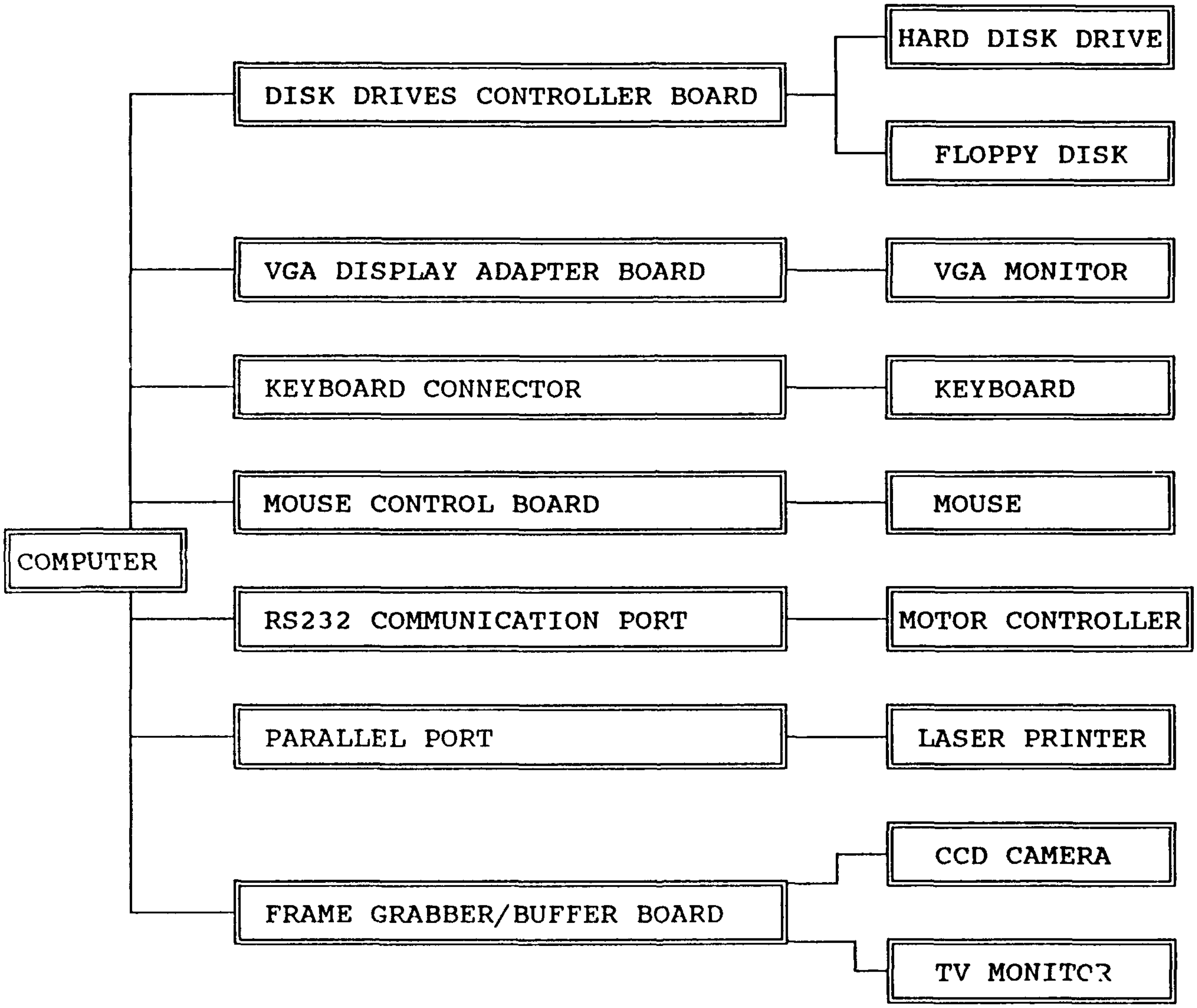


Figure 1. The Block Diagram of the Electrical/Digital System

POSITIONING CONTROL DEVICES BLOCK DIAGRAM

STEPPING MOTOR CONTROLLER SYSTEM

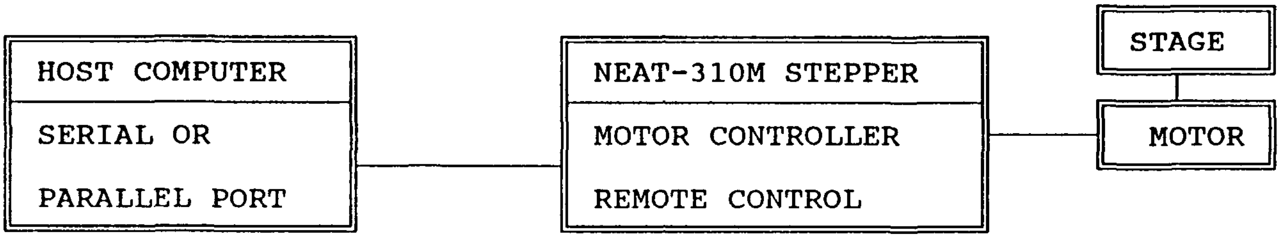


Figure 2. Positioning Control Device Block Diagram

I-1-1 Stepping Motor/Controller

A DC stepping motor is a motor with a rotor and several windings. Applying current to the windings generates a magnetic field which rotates the rotor.

DC stepping motors, by definition, move in a continuous point by point positioning manner and are therefore ideal for micropositioning applications. When at rest, their stop position does not drift. They are held in position by holding torque. Because it is possible to reduce or inhibit the holding torque, stepping motors are more suitable to vacuum applications. Since they operate in open loop, position feedback via an encoder is not necessary for motor control but may be desirable to verify proper functioning. Under normal condition operating conditions, stepping motor accuracy is not influenced by the characteristics of the associated mechanical system.

A basic DC stepping motor controller output DC voltage commutated to windings on the motor. Energizing windings in sequential order moves the rotor to various positions in a step-wise fashion. This commutation is controlled by logic pulses which may be counted to determine the total angular motion. The distance between two stable positions is called a full step and direction of rotation is determined by the order in which the windings are energized. The phase commutation technique applied to four phase stepping is quite simple. The sequence is analogous to counting up to four and starting again with one. For example 1, 2, 3, 4, 1, 2, 3, 4, 1, 2... and so on. The block diagram and the example of switching current sequence for full/half step motor drive are shown in figures 3 and 4. Each count represents one complete step of the motor. Motor operating in two phase/full step and one phase/full step modes have the same stepping resolution, or angular displacement per step. However, two phase/full step mode energizes two winding simultaneously. Although the technique the technique significantly increases the motor torque, system efficiency is greatly reduced. Approximately, 100 percent additional motor power is required to sustain only 40 percent more torque. In many instances the motor assembly becomes noticeably hotter. Therefore, this mode is only recommended for those applications that require more torque from the motor at hand in lieu of upgrading to a larger model.

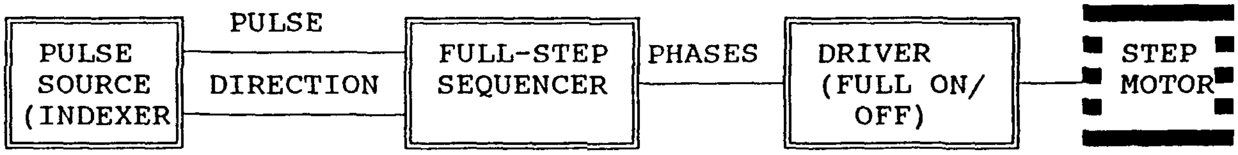
Standard 1.8 degree stepping motor consist of a laminated toothed stator wound with two center tapped coils, surrounding a 50 pole hybrid rotor. The rotor consists of an axially magnetized permanent magnet, with two laminated iron cups. Unlike D.C. motor, applying current to the motor windings generates a torque which resists rotation (the holding torque).

However, by switching coils on and off in a specific four step sequence, the rotor will "step" 1.8 degree per current change. An optional eight step sequence, implemented on stepping motor drives and controls, doubles the resolution to 0.9 degree (400 steps per revolution). Rotation is therefore achieved by simply applying an appropriate sequence of winding current.

Due to the motor rotor inertia, there is a limit to the step rate that can be applied to a stationary motor without it stalling, or failing to follow the step train. This rate, called the STOP-START RATE, is a function of the motor's holding torque, rotor inertia, and load inertia. It ranges from 400 to 1000 full steps per second (2 to 5 revolutions per second); a typical value for a slightly loaded 23 frame motor is 700 full steps per second. To operate at step rates above this value, the step frequency must be accelerated, or "ramped" from a rate below the start-stop rate to the desired top speed. The starting frequency is usually chosen to be above the fundamental resonance and safely below the stop-start rate; a value of 400 full steps per second (2 revolutions per second) is typically employed with 23 frame motors.

BLOCK DIAGRAM OF STEP/SERVO MOTOR CONTROL MODE

STEP MOTOR IN FULL-STEP CONTROL MODE



STEP MOTOR IN MICROSTEPPING CONTROL MODE

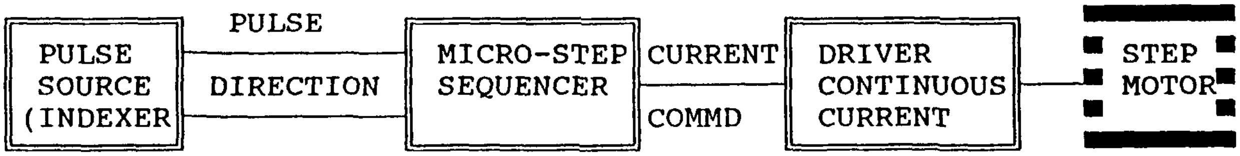


Figure 3. Block diagrams of the motor control principles

STEPPING MOTOR STEP CURRENT SWITCHING SEQUENCE

FULL STEP CURRENT SWITCHING SEQUENCE

	phase 1	phase 2	phase 3	phase 4
step 1	on	on	off	off
step 2	on	off	off	on
step 3	off	off	on	on
step 4	off	on	on	off
step 1	on	on	off	off
step 2	on	off	off	on
:				

HALF STEP CURRENT SWITCHING SEQUENCE

	phase 1	phase 2	phase 3	phase 4
step 1	on	on	off	off
step 2	on	off	off	off
step 3	off	off	off	on
step 4	off	off	off	on
step 5	off	off	on	on
step 6	off	off	on	off
step 7	off	on	on	off
step 8	off	on	off	off
step 1	on	on	off	off
step 2	on	off	off	off
:				

Figure 4. Stepper motor full/half step current switching sequence

In addition to resisting instantaneous start at high step rates, the rotor (and the load) inertia can produce overshoot if the pulse train is abruptly terminated. Accordingly, the stopping point must be anticipated and the motor ramped down to an appropriate frequency (again, 400 full steps/sec. is typical) before stopping. Short moves, which may not reach the programmed top speed, result in triangular moves. The allowable acceleration and deceleration values are determined by the motor's torque, drive type, and the total inertia. The typical speed profile of the stepping motor drive is shown in figure 5.

SPEED PROFILE OF THE STEPPING MOTOR DRIVE

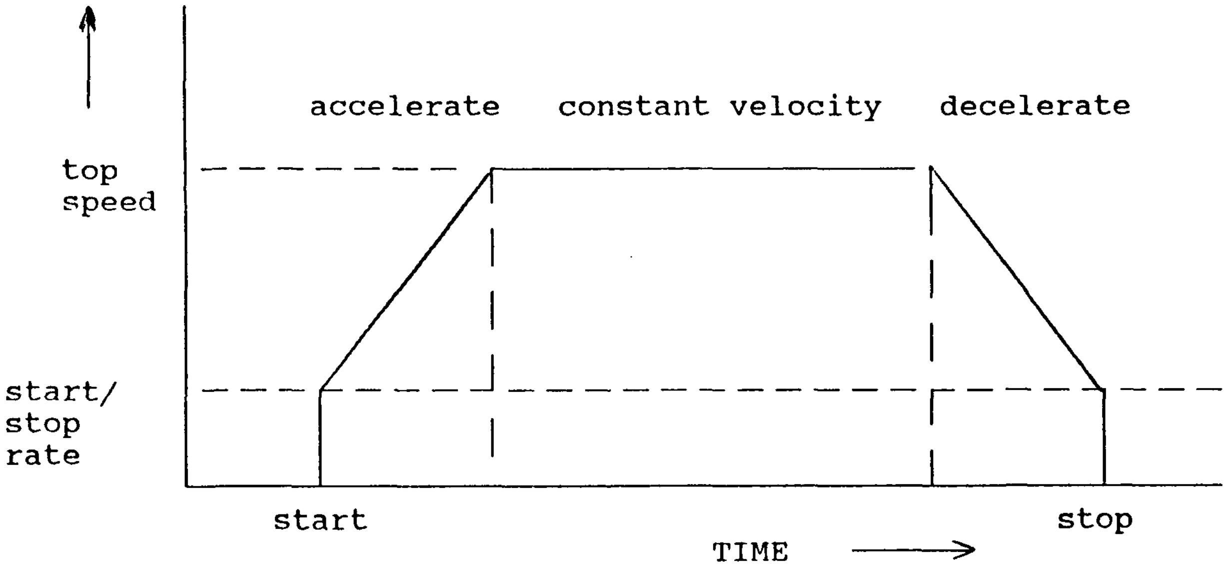


Figure 5. The overall velocity profile of the stepping motor moves

I-2. Data Acquisition Device and Controller

Data acquisition device of the interferometer include a CCD (Charge Coupled Device) camera and a image grabber/buffer. The block diagram is shown in figure 6. They will be described in the following sections.

I-2-1. CCD Camera Specifications

Charge-Coupled Device camera is a solid-state camera. It is silicon semiconductor components capable of performing the general functions of image sensing. There are two formats of the CCD, one is Linear Imaging Device, the other is Area Imaging Device. The CCD camera is a small, rugged, low power TV camera capable to operation in very low light levels such as one-quarter moonlight. The CCD camera used as the image acquisition device is Area camera with RS-170 video signal output. The specifications of the camera are listed as below.

Specifications

Imager:	Single CCD using frame transfer method
Image Area:	8.8 x 6.6 mm (2/3" format)
Active Pixel:	754 x 484
Resolution:	565 horizontal TV line, 350 Vertical TV line
Sensitivity:	.07 lux useable picture, .16 lux at full video
S/N ratio:	60 db

Contrast Variation: < 5% overall @ 25 degree C

Gamma: Jumper selectable

AGC: Jumper selectable

Signal: EIA RS-170

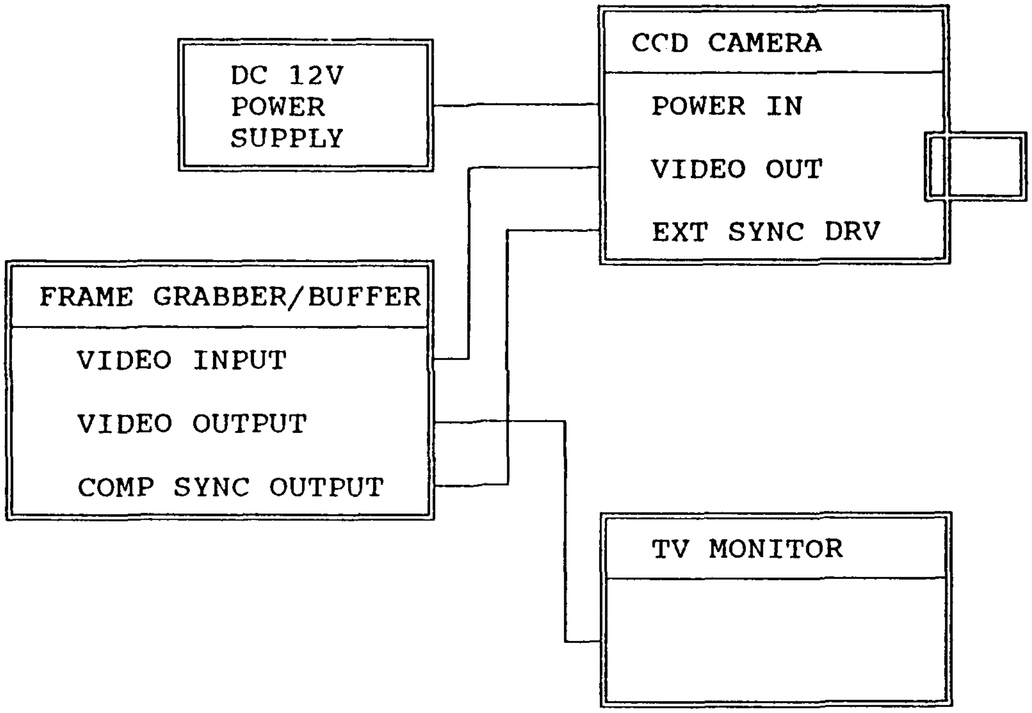
I-2-2. Frame Buffer Specifications

The frame grabber/buffer used as interface of the imaging camera is EPIX Silicon Video Mux. The Silicon Video Mux is a single board frame grabber that allows the PC computer to digitize, process, display, transmit, and archive video information. It can digitize one or several frames from a video camera (ex. CCD camera), allow the PC to process the image data, display the image data on a B&W or RGB monitor. Video data is digitized and displayed at 8 bits per pixel, Silicon Video Mux can contain up to 4 MB of image memory for multiple image buffer storage.

The features of the frame buffer are:

- Variable sampling
- 1 MB or 4 MB image memory
- Video memory address registers
- 752 pixels by 480 pixels maximum resolution
- External pixel clock, horizontal and vertical drive.
- Multiple image storage.
- Video line counters for selection of raster lines to be digitized/display.

BLOCK DIAGRAM OF DATA ACQUISITION SYSTEM



VIDEO AND COMPOSITE SYNC IN/OUT CONNECTOR FOR FRAME GRABBER

Pin(s)	Signal
1	COMP. SYN. IN
2	VIDEO IN 5
3	VIDEO IN 4
4	VIDEO IN 3
5	VIDEO IN 2
6	VIDEO IN 1
7	VIDEO IN 0
8	GREEN OUT
9	BLUE OUT
10	RED OUT
11	COMP SYNC OUT
12	EXTOUT (TTL)
13	EXTIN (TTL)
14-25	VIDEO GROUND

Figure 6. Block diagram of the data acquisition system

II. SOFTWARE

We have initiated the work for the software development on two main projects:

1. **Automated Operation Software Development**
    - A. Positioning devices software driver design
    - B. Data acquisition device driver design

2. **Interferogram Data Reduction Software Algorithm**

II-1. Automated Operation Software Development

The automated operation software development contains: The positioning device software driver development and data acquisition device driver development. The algorithm of both device drivers will be addressed in the following sections.

II-1-1. Positioning Device Software Driver Design

a. Stepping Motor Controller Driver

- Define the communication port between PC and controller
- Define the direction of the movement
- Define the number of steps to move
- Define the pulse train accelerate ramp slope
- Define the pulse train decelerate ramp slope
- Define maximum speed of motor

- Subroutine of pulse train
- Check the limit switch status
- Go

II-1-2. Data Acquisition Device Driver Design

a. Frame Buffer Device Setting and Driver Design

- Camera synchronization status setting
- Memory base address setting
- Lookup table base address setting
- Register base setting
- Image size, sampling interval, offset setting
- Assign image buffers number
- Video digitize/display
- Create command files
- Link SVIP to main program

II-2. Interferogram Data Reduction Software Algorithm

The interferogram data reduction software algorithm is listed as below and the flow charts is shown in figure 7.

- Controlling sequence of the whole system operation
    - . Link the positioning controller driver commands file
    - . Link the frame buffer control driver commands file

- Interferogram for each of the sub-apertures which are captured and stored in the assigned address buffer

- Phase measurement, which yield x, y slope for each sub-aperture

- Digital integration, which yield wavefront shape of each sub-aperture
    - . Resample the x,y slope phase map
    - . The phase map boundary setting
    - . Integration x direction slope
    - . Integration y direction slope
    - . Combine x,y integration yield the surface phase map

- Match the full surface wavefront using least square fit on overlap areas among each adjacent sub-aperture
    - . Assign sub-aperture sequence

. Transform the phase map of sub-aperture to the global coordinator system

. Define overlap areas between sub-apertures

. Compute the phase difference inside the overlap area

. Use least square fit to match the phase data inside the overlap areas

. Generate the complete surface map (resample)

- Analysis the wavefront phase map

  . Polynomial fit the wavefront

  . Print out the coefficients of the polynomial fit

  . Compute the aberration

  . Compare the surface wavefront shape with theoretical designed surface shape of the test mirror

  . Extract the parameters of the test mirror:
  root-mean-square (rms)
  peak-to valley (p-v)

  . Noise filtering to improve accuracy

  . Data averaging to reduce the noise

  . Data editing for scaling, rotation and translation

  . Data storage and transfer to other data formate

- **Display**

  . 3-D isometric plot with scaling variable

  . Thin line (b/w or color) contour map with assigned level in waves or in microns

- Thick contour map (b/w or color) with assigned level in waves or in microns
- Interactive sectional profile display
- Solid modeling display

- **Hard copy**
  - Interferograms can be taken from TV monitor by polaroid camera
  - Interferograms can be printed out by video printer
  - Display and numerical results can be print out by laser printer