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13. ABSTRACT (Maximum 200 words)

The purpose of this project was to develop an advanced computer-aided design (CAD) tool that can be used for the design of microwave and millimeter-wave solid-state integrated circuits. The completed work consists of major improvements to a large-signal, physics based model for GaAs MESFET integrated circuits previously developed at NCSU. New features for the model include a large-signal load-pull algorithm and RF sensitivity and process yield capability. The new algorithms significantly enhance the use of the simulator in design applications. The new capability permits the simulator to be used for both MESFET and RF circuit process yield optimization.

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Final Report

D.E. Stoneking and R.J. Trew

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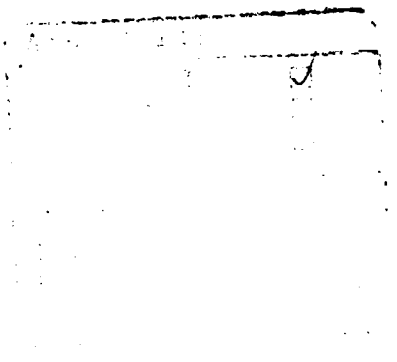

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Abstract

The purpose of this project was to develop an advanced computer-aided design (CAD) tool that can be used for the design of microwave and millimeter-wave solid-state integrated circuits. The completed work consists of major improvements to a large-signal, physics based model for GaAs MESFET integrated circuits previously developed at NCSU. New features for the model include a large-signal load-pull algorithm and RF sensitivity and process yield capability. The new algorithms significantly enhance the use of the simulator in design applications. The new capability permits the simulator to be used for both MESFET and RF circuit process yield optimization.

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This project was an ARO Graduate Student Fellowship program. Two students were supported. The students and degree status are:

W.L. Pribble, M.S.E. degree received May, 1990

D.E. Stoneking, Ph.D. degree to be awarded May, 1991

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Chapter 1

Introduction

This project develops a nonlinear microwave computer aided design tool named TEFLON which analyzes and optimizes a MESFET and its linear embedding circuit. The KT-MESFET model is a process oriented, physically based MESFET model formulated in the time domain [1, 2]. A harmonic balance algorithm interfaces the KT-MESFET model to the embedding circuit. Unlike other circuit simulation models, the KT-MESFET model is based on the physical processes within the device and not on empirically fitted functions and parameters. The KT-MESFET model provides accurate large-signal simulations given physically measurable quantities such as device dimensions, semiconductor material constants, and channel donor atom distributions. TEFLON allows for the nonlinear analysis and optimization of both the MESFET and its linear embedding circuit. TEFLON's present harmonic balance implementation requires all tones to be harmonically related — noncommensurate frequency tones are not permitted.

Specifically, the author advances TEFLON in the following areas:

1. Improvement of the formulation and numerical behavior of the KT-MESFET model.

2. Integration of a GaAs process simulator, SUPREM 3.5, to predict the nonlinear large-signal performance of MESFET devices directly from process variables such as implant dose and energy.

3. Simulation of load-pull contours for MESFET devices with arbitrary doping profiles.

4. Simulation of the variation and sensitivity of large-signal power amplifier figures-of-merit.

5. Nominal and statistical optimization of MESFET device designs with respect to physical process variables.

6. Nominal and statistical optimization of the driving point impedances presented to the MESFET.

The remainder of this report is organized as follows. Section 2 details the software engineering undertaken to more fully utilize the KT-MESFET model. The section begins by describing the software system created by Khatibzadeh. Improvements and additions to the system are then detailed. In section 3, graphical output from the simulator is presented. Section 3 also lists publications produced by the author and others using TEFLON. Section 4 summarizes this report.

Chapter 2

Software Engineering

This work's starting point was the KT-MESFET model with a harmonic balance simulator capable of DC voltage and RF input power sweeps. The software engineering then proceeded in a number of directions. Improvements were made to the KT-MESFET model. An improved nonlinear system of equations solver was inserted for performing the harmonic balance. A load-pull simulation option was implemented. Sensitivity analysis capabilities were added. Nominal and statistical device and circuit optimization completed the software engineering.

2.1 Khatibzadeh's Model and Simulator

The KT-MESFET model has features which make it unique relative to other MESFET models used for circuit simulation [1, 2]. The model provides a computationally efficient solution of the semiconductor device equations in the region directly under the gate. The result of the solution is the device conduction current, a four element capacitance matrix, and device time delay. A schematic of the model is given in Figure 2.1 which shows the relationship of the conduction current source, the capacitance matrix and the device time delay relative to the intrinsic device terminals. Although the capacitance matrix results from the quasi-static solution for each $V_{ds} - V_{gs}$ pair within the solution space, the product of the capacitance matrix and the time derivatives of V_{ds} and V_{gs} models the device displacement currents at the gate and drain terminals. The device time delay is modeled as a source-drain time-of-flight delay which is applied to the gate-source voltage. Application of the delay to the gate-source voltage then models the delay as charging time delay. The analysis of the region under the gate is based on the dimensions of the device, the physical constants of the semiconductor material, and the donor distribution beneath the gate metal. Other features of the intrinsic transistor solution are allowance for deviations in space charge neutrality, carrier 2-D velocity vector, and avoidance of the abrupt depletion approximation.

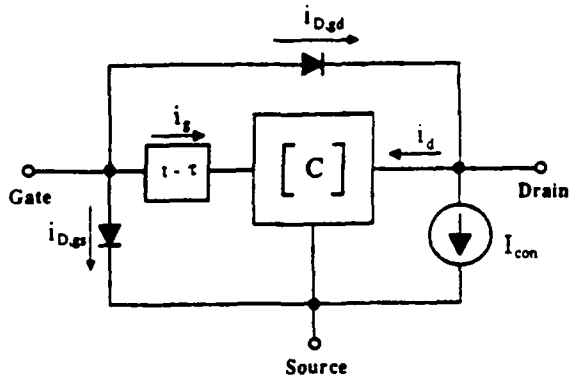


Figure 2.1: Schematic representation of Khatibzadeh-Trew large-signal MESFET model

External to the intrinsic device region various effects are modeled empirically. The primary nonlinear effects are forward conduction of the gate Schottky diode and gate to drain breakdown. Other effects of interest are the parasitic resistances, inductances and capacitances associated with contacts and transport from the intrinsic region to the contacts. The forward conduction and gate-drain breakdown effects are modeled with piecewise linear diode models as shown in Figure 2.1. The parasitic elements were modeled as constant valued resistors, inductors, and capacitors. Figure 2.2 shows the parasitic elements along with the intrinsic MESFET block and the complete linear embedding circuit which can be simulated.

The simulator portion of Khatibzadeh's work was a harmonic balance algorithm for DC and RF simulations [3, 4, 5]. Postprocessing software gener-

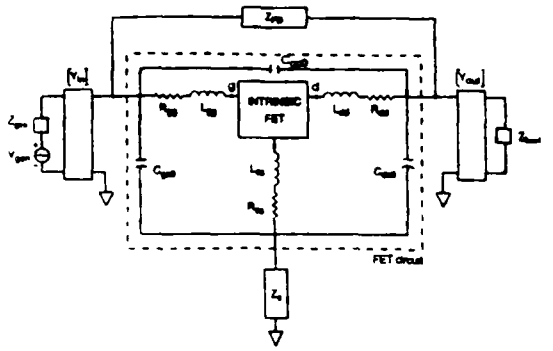


Figure 2.2: Circuit topology of TEFLON harmonic balance simulator showing the intrinsic MESFET model, extrinsic parasitic elements, and linear embedding circuit.

ated graphical results from the simulation. The harmonic balance algorithm used the IMSL nonlinear system of equations solver based on Powell's method [6]. The DC simulations allowed sweeping of both the V_{GS} and V_{DS} voltages over arbitrary ranges. For each applied $V_{GS} - V_{DS}$ combination the DC voltages at the intrinsic nodes of the MESFET are adjusted so that the sum of the DC currents at the gate and drain nodes are zero. For RF simulations, the available power from a single tone RF generator could be swept over an arbitrary range for a fixed DC bias. For each generator power level a harmonic balance is performed by adjusting the DC, fundamental, and harmonic voltage phasors of the gate-source and drain-source voltages until the sum of the current harmonic phasors at those nodes goes to zero. Since the harmonic balance algorithm used a standard 1-D FFT to convert between time and frequency representations of the waveforms at the gate and drain, only harmonics of a single tone could be considered. The postprocessing software allowed plotting of DC I-V curves, equivalent circuit parameter values as a function of DC bias, and RF performance measures, such as, power delivered to load and power added efficiency, versus power available from the generator or the power delivered to MESFET gate.

2.2 MESFET Model Improvement

Deficiencies with the formulation and numerical behavior of the KT-MESFET model were found. These problems initially caused harmonic balance failures and noise in the large-signal optimization figures-of-merits. These problems are enumerated below:

1. device model Newton method failure.
2. discontinuity of device capacitance tables.
3. incorrect formulation of time delay τ_d as V_{d_s} goes to 0.
4. excessive harmonic generation by piecewise linear diode model.
5. incorrect boundary of gate-drain breakdown region.
6. variables for specifying implanted donor distributions inadequate.

These problems with the device model resulted from a variety of causes. The causes of the Newton method failure were extrapolation of device integrals beyond the interval on which integral is splined and the lack of a backtracking method for guaranteeing correctness of the Newton step. The discontinuity of the capacitance tables results from discontinuous gate depletion thickness changes. The discontinuous depletion thickness changes occurred on both the drain end of the gate depletion region. These discontinuities occurred as the model transitions through modes A, B, and C (see [1] for meaning of modes). The incorrect formulation of τ_d was that τ_d went to infinity as V_{d_s} approaches zero. This error resulted from incorrectly modeling the time delay as the electron time-of-flight from source to drain. Under the condition for saturated electron velocity transport over the entire distance from source to drain, which is model mode C operation, the time-of-flight model is adequate. The time delay mechanism is a combination of the distributed nature of wave propagation onto the gate fingers, capacitance charging times, and electron time-of-flight from source to drain. The excessive harmonic generation by the piecewise linear diode model aggravates a fundamental problem with the harmonic balance technique. During iterations of the harmonic balance solution, the MESFET model is unloaded and experiences no circuit damping effects. The discontinuous diode model causes the device current waveforms to have transients which cannot exist when the device is operating within the circuit. The incorrect boundary for the gate-drain breakdown region resulted from assuming that the breakdown mechanism is chiefly avalanche breakdown. This assumption results in the boundary being a line in the $V_{d_s} - V_{g_s}$ plane

along which V_{gd} is a constant. And finally, the problem with implanted donor distribution variables was that the peak doping density, range, and straggle of the distribution were used. For a given implant the range and straggle are not independent. The process variables which primarily determine the peak doping density, range, and straggle are the implant energy and dose.

The solutions applied to KT-MESFET problems were improved numerical techniques and better formulations. Under investigation of the device Newton method failure, extrapolation beyond the computation interval of device integrals was found to represent physically unrealistic solutions. Simple hard limits on spline abscissa values caused extrapolation failures to cease. Insertion of an Armijo backtracking method into the existing Newton method improved convergence at device mode changes and shortened convergence time for all points. We smoothed the device capacitance tables with a local averaging algorithm. An improved formulation of the capacitance values is needed to fix this problem. The complete fix requires a reformulation of the model — a long and difficult task relative to post-process smoothing. The capacitance values not at the mode A, B, and C transitions are however good estimates of the dynamic device capacitances. Under normal power amplifier DC bias and RF drive conditions, the linear operating region is not the first limiting mechanism encountered as the source available power increases. The solution to the problem of excessive harmonic generation by the diode model was to model the diodes with a truncated Taylor series expansion of the diode equation. The number of terms of the Taylor series should be less than or equal to the number of harmonics balanced. Setting the gate-drain breakdown boundary as arbitrary line in the $V_{ds} - V_{gs}$ plane provided an improved phenomenological the breakdown model [7]. Incorporating SUPREM 3.5, a GaAs process modeling program, provided better modeling of the implant and other process variables [8]. This linkage of SUPREM 3.5 and TEFLON extends the usefulness of both programs greatly.

2.3 Harmonic Balance Algorithm Improvement

The KT-MESFET model problems caused harmonic balance failure and erroneous calculations of figure-of-merit during optimization. Development of MK-SMWB, a nonlinear system of equations solver, improved harmonic balance convergence. The MK-SMWB algorithm is a Broyden quasi-Newton method. The Sherman-Morrison-Woodbury formula provides efficient computation of the inverse Jacobian.

2.4 Load-Pull Simulations

A load-pull simulation characterizes the effect of load impedance on various circuit performance measures (i.e., power delivered to the load, power added efficiency, gain, etc.). We implemented a load-pull algorithm for investigating these effects on the power delivered to the load. During a load-pull, the load model is either a series RL or RC circuit. The impedance and reactance of the load circuit at the fundamental frequency are the pull variables. TEFLON currently does not handle arbitrary harmonic load impedance pulls.

The load-pull algorithm consists of two parts. The first part is an optimization algorithm for locating the load resistance and reactance for which maximum power is delivered. The optimization algorithm used is Powell's direction set method [9]. During the optimization phase, the load resistance and reactance are varied to maximise the output power deliveried to the load. The second part locates contours of constant load output power by searching along rays emanating from the point of maximum power transfer. This search is finding the root of a nonlinear equation in one variable. The nonlinear function is the load output power and the variable is the length of the ray. The angle of the ray is changed to locate other points on the contour. The root finding algorithm is the Van Wijngaarden-Dekker-Brent method [9].

2.5 Sensitivity Analysis

Sensitivity analysis characterises the effect of device or circuit parameter changes upon some operating figure-of-merit (FOM). Sensitivity is usually defined as [10]

$$S_p^F = \frac{p}{F}\frac{\partial F}{\partial p} = \frac{\partial \ln F}{\partial \ln p} \quad F, p > 0 \qquad (2.1)$$

where F is the FOM and p is the parameter.

This definition provides a scale free value for the sensitivity. Sensitivity analysis allows evaluation the tolerance of a design's performance due to variation in circuit components.

TEFLON computes the sensitivity of a given FOM versus the device or circuit parameters by a perturbation method. A parameter sweep generates the change in the FOMs of interest. A Hermite spline provides interpolation of the FOM and its partial derivative. The variation and sensitivity of the FOM are output to the standard output from the spline.

The optimization FOMs are grouped into four categories: linear gain, FOMs associated with gain compression levels, FOMs associated with the maximum power added efficiency of the circuit, and FOMs associated with the maximum drain efficiency. For linear gain the only FOM is the linear gain. For the 1 dB, 3dB, and 6dB gain compression levels the FOMs are the circuit input power, output power, gain, and output power-gain product at the gain compression level. For the maximum power added efficiency, the FOMs are the maximum power added efficiency and the input power, output power, gain, and output power-gain product at the maximum power added efficiency. And for the maximum drain efficiency, the FOMs are the same as those for the maximum power added efficiency with the exception that maximum drain efficiency replaces maximum power added efficiency. A further perturbation of the available FOMs is that either the power available from the source or the power delivered to the MESFET can be considered to be the input power.

The KT-MESFET model optimization parameters are numerous and are not listed here (see [11]). The linear circuit optimization parameters are the harmonic impedances of the blocks labeled Z_{gen}, Z_{load}, Z_s, and Y_{fb} in Figure 2.2.

2.6 Nominal and Statistical Optimization

Nominal optimization improves the performance of a single device or amplifier circuit. Statistical optimization seeks to improve the performance of an ensemble of devices or circuits which result from fabricating a nominal design. For nominal optimization, TEFLON uses a single FOM from those listed in section 2.6. For statistical optimization, TEFLON maximizes the design parametric yield.

Both nominal and statistical optimization use the same optimization algorithm. Several optimization algorithms were implemented and tested:

1. Levenberg-Marquardt least mean square (LM-LMS) code. [12, 13, 14].
2. Unconstrained Broyden, Fletcher, Goldfarb, and Shanno (BFGS) code [14].
3. Projected gradient without variable gradient step size (PGSD) [14].
4. Bilbro tree based simulated annealing code (B-TBSA) [15].
5. the Gilmore-Kelley projected gradient steepest descent code with variable gradient step size (GK-PGSDVGS) [16].
6. the Gilmore-Kelley BFGS code with variable gradient step size (GK-BFGSVGS) [16].
7. A symmetric rank one update (SR1) code [17].
8. A symmetric rank one update code with variable gradient step (SR1VGS) [16].

The requirements on our optimizers are that they be a constrained optimizers, that they be robust in the prescence of multiple basins, and that they behave well under conditions of large noise amplitude. Penalty functions on calculated variables are necessary to allow computation of optimization FOMs. The penalty function variables are the pinch-off voltage (V_{po}), the condition that the MESFET not deliver power to the linear input network, and the gain at the maximum power added efficiency. Constrained codes are necessary because many device and circuit parameters cannot assume certain values. Robustness is necessary due to the numerical noise and the possibility of multiple basins in the FOMs. The numerical noise was initially an unfortunate reality. KT-MESFET model development eliminated much of the noise, but the noise still defeats most optimizers.

The LM-LMS code did not work because optimization of a single error measure or FOM is not a LMS formulation. The BFGS code failed because setting gradient step size to root machine precision gives information only on FOM local structure. The algorithm is known to converge only to near local minima. The PGSD code failed because it is unconstrained and also finds only local minima. The B-TBSA code, while being slow, was constrained and could handle FOM noise and multiple minima. The GK-PGSDVGS code was the most successful. Decreasing the gradient step, using a backtracking method, and checking for optimization over all scales enable the GK-PGSDVGS code to find minima in the presence of even impulsive type noise. Convergence becomes markedly slower

and less probable under impulsive or strong numerical noise. The GK-BFGSVGS code can withstand the noise, but it does not give a speed up over GK-PGSDVGS. The SR1 code provides robustness when the optimisation FOM exhibits negative curvature. SR1 does not give the expected speedup over the GK-PGSDVGS code. And, SR1 does not behave better than GK-PGSDVGS in the presence of noise. SR1VGS code does navigate the noise, but it also does not give the expected speedup over the GK-PGSDVGS code.

Chapter 3

TEFLON Results

This section details TEFLON results with graphs and publications derived from TEFLON.

Postprocessing software generates plots form tabular TEFLON data in the standard output. Example TEFLON data plots are given in this section and are listed below:

1. DC I-V curves with V_{DS} as the abscissa and V_{GS} as a parameter.
2. DC small signal equivalent circuit elements with V_{DS} as the abscissa and V_{GS} as a parameter.
3. RF input power sweeps with P_{out}, G_{op}, G_{trans}, PAE_{op}, PAE_{trans}, η_{drain}, HB_{error} versus either $P_{in,inc}$ or $P_{in,dlv}$.
4. RF voltage and current waveforms.
5. RF active load line plots which is the sequence of Id-Vds data superimposed on the DC I-V curves plotted with V_{DS} as the abscissa.
6. Spectra plots of RF voltage and current waveforms.
7. Load-pull contours on a Smith chart.
8. Variation and sensitivity of linear gain and large-signal FOMs versus MESFET and circuit parameters.
9. 3-D plots of large-signal FOM surfaces.
10. Histograms of yield estimates.

Figure 3.1 shows a comparison of measured and simulated DC I-V curves [1]. the device is an ion implanted MESFET with the parameter values given in Table 3.1. The match is good in both the linear and saturation regions. At the current knees, the match deteriorates because the model does not account for thermal effects. The increased slope of the characteristics in the saturation region results from not modeling substrate current effects. The measured data shows no gate-drain breakdown current.

Device parameter	Value	Units
peak doping	2.1×10^{17}	cm^{-3}
range	0.075	μm
straggle	0.093	μm
gate width	1000	μm
gate length	0.42	μm
D-G BD point	V_{dsbd} at V_{po}	22 V
D-G BD slope	1.0	V_{ds}/V_{gs}

Table 3.1: Parameter values for DC I-V data shown in Figure 3.1.

Figure 3.2 shows a the RF performance of the device. The device is an ion implanted MESFET with the following extracted parameter values given in Table 3.2. Excellent agreement exists between simulated and measured data of the output power delivered to the load, the device operating gain, and the power added efficiency.

Figure 3.3 gives RF current and voltage waveforms for a class B power amplifier as the MESFET input power increases. The ion implanted MESFET parameter values are given in Table 3.3.

Figure 3.4 has I_d vs V_{ds} Lissajous curves, or dynamic load line curves, superimposed on the device DC I-V curves [18]. The device parameter values are the same as given for Figure 3.3. The Lissajous

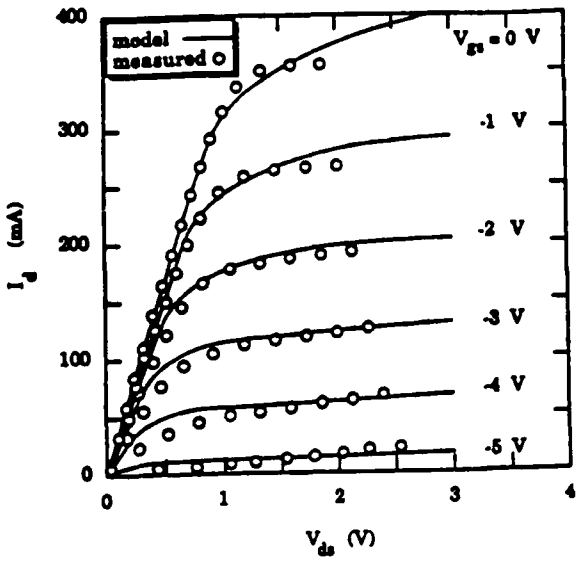


Figure 3.1: Measured and simulated DC I-V curves.

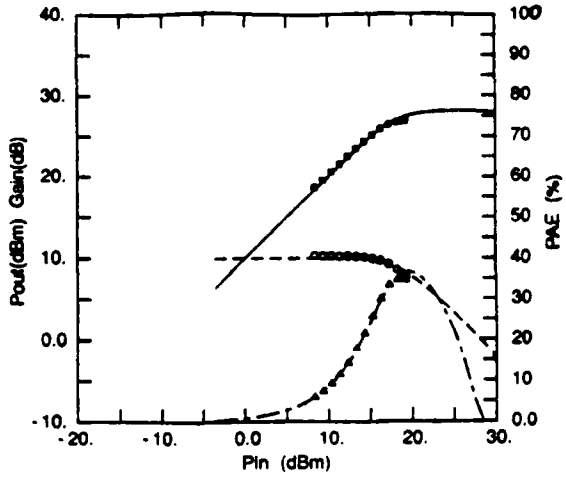


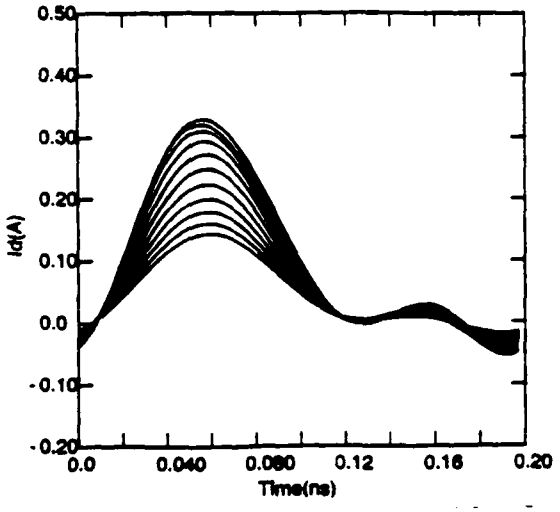
Figure 3.2: Measured and simulated RF power sweep results. Pin is the power delivered to the device.

Device parameter	Value	Units
peak doping	1.0×10^{17}	cm^{-3}
range	0.101	μm
straggle	0.153	μm
gate width	1047	μm
gate length	0.496	μm
D-G BD point	V_{dsbd} at V_{po}	12.6 V
D-G slope	1.0	V_{ds}/V_{gs}
HB f_t	5	GHz

Table 3.2: Parameter values for RF input power sweep data shown in Figure 3.2.

Device parameter	Value	Units
peak doping	1.6×10^{17}	cm^{-3}
range	0.079	μm
straggle	0.109	μm
gate width	1200	μm
gate length	0.5	μm
D-G BD point	V_{dsbd} at V_{po}	12.6 V
D-G BD slope	1.0	V_{ds} V_{gs}
HB f_t	5	GHz

Table 3.3: Parameter values for RF waveforms shown in Figure 3.3.



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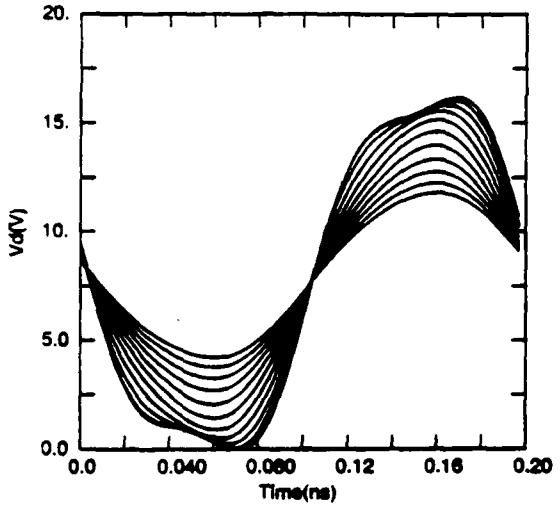


(b)

Figure 3.3: RF current and voltage waveforms for different RF power drive levels for an ion implanted device optimized for maximum power added efficiency at 5 GHz and biased class A. (a) Current waveform (b) Voltage waveform

Device parameter	Value	Units
doping	1.0×10^{17}	cm^{-3}
channel thickness	0.3	μm
gate width	1000	μm
gate length	0.42	μm
D-G BD point	V_{dsbd} at V_{po}	12.6 V
D-G BD slope	1.0	V_{ds}/V_{gs}
HB f_1	5	GHz

Table 3.4: Parameter values for RF load-pull data shown in Figure 3.5.

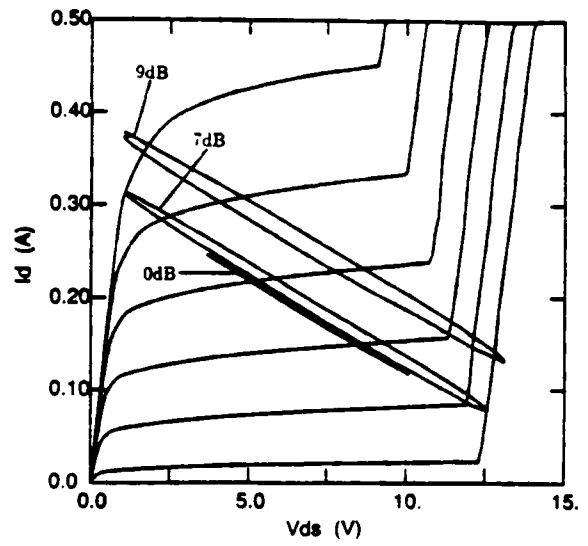
curves are for the given RF drive levels with class A DC biasing. The two figures compare the effect of load matching on Lissajous angle and area.

Figure 3.5 gives load-pull simulation results for uniform channel MESFET [19]. The device parameter values are given in Table 3.4.

The two figures compare the difference between device when operated at linear RF drive levels and when operated into gain compression. Before the onset of gain compression the level contours of power delivered to the load are circles as predicted by the linear theory. After the onset of gain compression the level contours distort from circles, and the conjugate match point moves towards the real axis of load reflection coefficient.

Figure 3.6 are example plots of the variation and sensitivity of large-signal FOMs [20]. The device values not under analysis are those given for Figure 3.2. Figure 3.6a illustrates the effect of implant straggle variation on maximum power added efficiency, η_{max}. Note the well defined optimum in the maximum power added efficiency at 0.075 μm. Figure 3.6b shows how peak doping effects on η_{max}. Again, η_{max} exhibits a optimum value. Figure 3.7a plots η_{max} and its sensitivity versus the gate-drain breakdown voltage. This figure is particularly interesting because increasing breakdown voltage beyond 20 V does not improve the maximum η_{max} obtainable. Figure 3.7b shows the effect on η_{max} of gate width.

Figure 3.8 is 3-D graph of the linear gain FOM surface. The plateau at the highest and lowest val-



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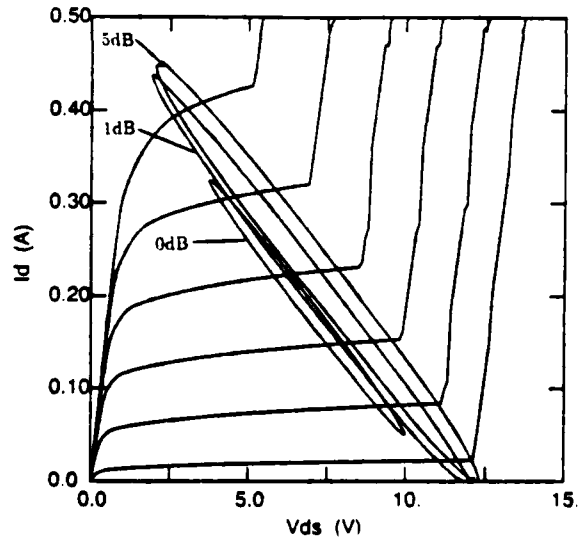
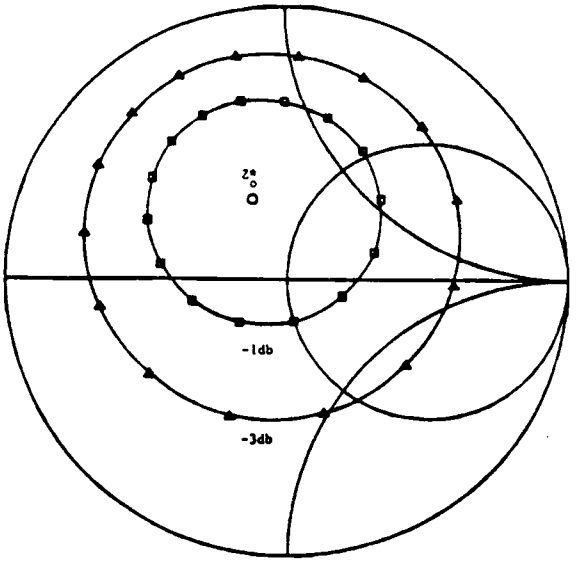


(b)

Figure 3.4: Dynamic load line plots of ion implanted device operated at 10 GHz with class A bias. (a) Dynamic load lines for 50 Ω load. (b) Harmonically matched load.



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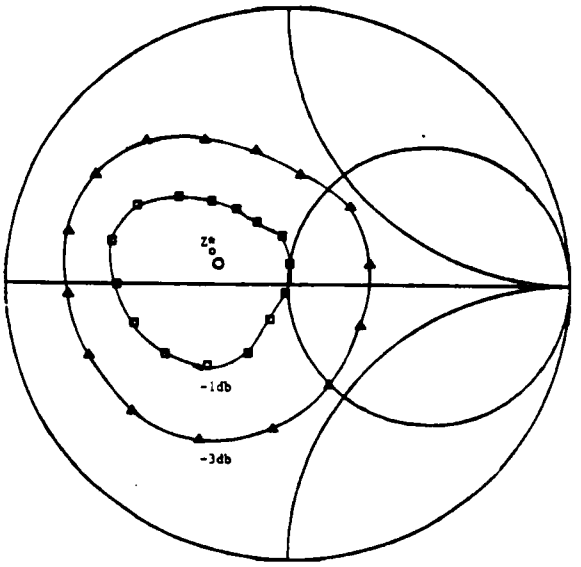
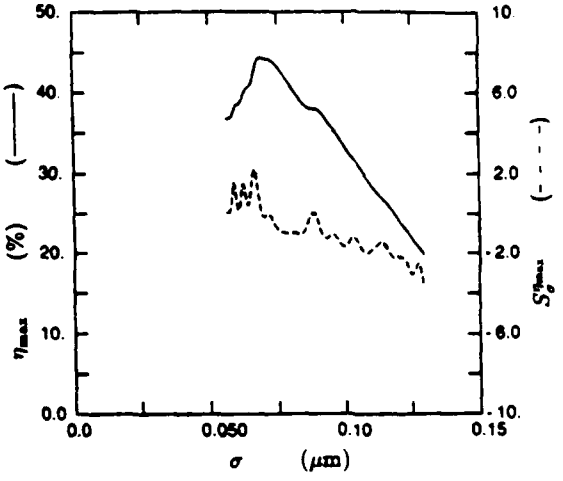
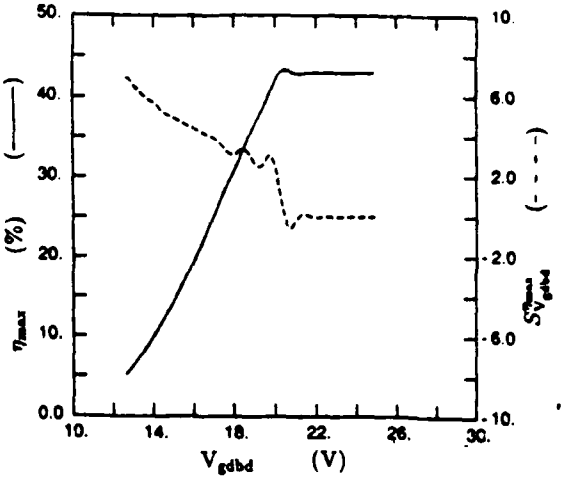


(b)

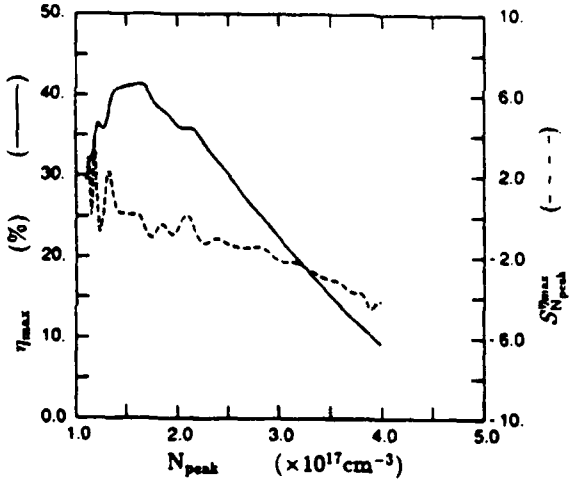
Figure 3.5: Load pull simulations of a uniform channel MESFET operated at 10 GHz with class A bias. (a) Linear operation at input power equal to 5.6 dBm. (b) Gain compression operation at input power equal to 17.6 dBm



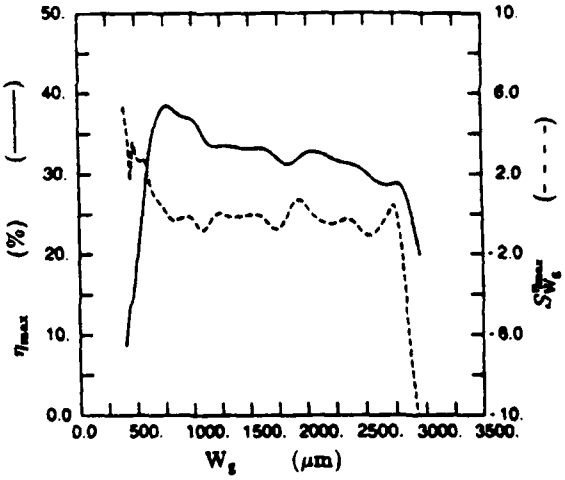
(a)



(a)



(b)



(b)

Figure 3.6: Variation and sensitivity of TEFLON large-signal figures-of-merit due to changes in device parameters. (a) Variation and sensitivity of the maximum power added efficiency versus implant straggle. (b) Variation and sensitivity of the maximum power added efficiency versus peak channel doping.

Figure 3.7: Variation and sensitivity of TEFLON large-signal figures-of-merit due to changes in device parameters. (c) Variation and sensitivity of the maximum power added efficiency versus gate-drain breakdown voltage. (d) Variation and sensitivity of the maximum power added efficiency versus gate width.

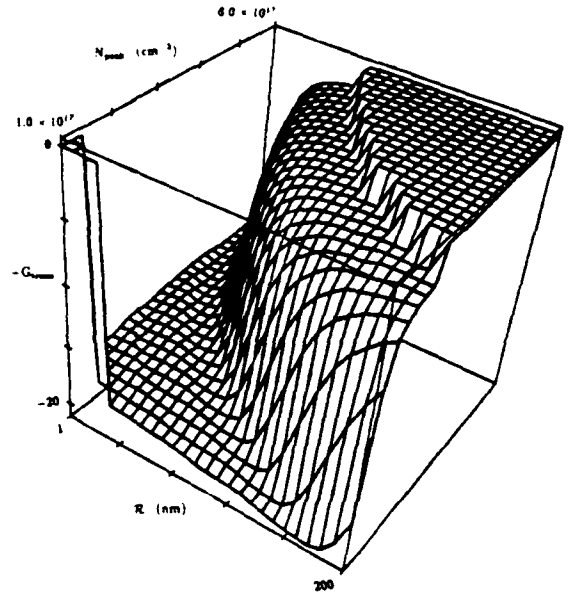


Figure 3.8: Linear gain FOM response surface versus peak channel doping and implant range.

ues of range and peak doping is the V_{po} penalty function. The remainder of the surface is the linear gain. Note the numerical noise on the response surface floor. This noise necessitates application of robust optimizers.

Figure 3.9 shows several histograms of 1000 devices for several nominal device designs with the same statistical model of process disturbances. The 3.9a design is clearly not optimum, and the FOM variance is small in that region of space. The 3.9b design corresponds to the device given in Table 3.4. The 3.9c design is the result of a yield optimization using peak channel doping, implant range, implant straggle, gate width, and gate length as optimization variables. The pass-fail threshold for the yield estimate was a small-signal transducer gain of 7.

Other results of this work are publications by the author and others working on TEFLON [18, 22, 21, 23, 24, 25, 26].

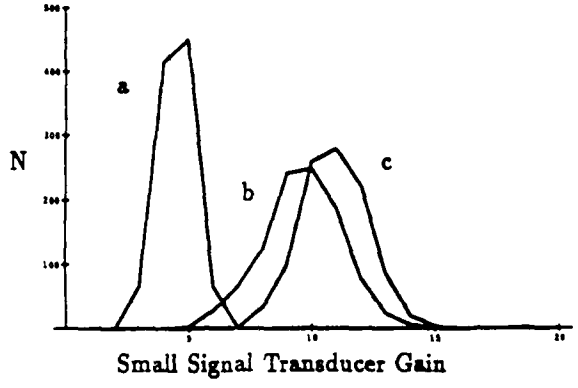


Figure 3.9: Simulated histograms of 1000 devices fabricated with the same statistical model of process disturbances but different nominal designs. (a) An unoptimized design. (b) Design with better gain. (c) A design resulting from yield optimization with small-signal transducer gain threshold of 7.

Chapter 4

Conclusion

A nonlinear microwave CAD tool, called TEFLON, for the analysis and optimization of power amplifiers was developed. The tool provides DC simulations, RF power sweep simulations, load-pull level contours of output power delivered to the load, sensitivity analysis of large-signal figures-of-merit, and optimization of large-signal figures-of-merit over the device and circuit parameter space. Either nominal or statistical optimizations are available. The statistical optimization maximizes the device parametric yield.

Graphical data is presented to illustrate TEFLON's analysis capabilities. These plots include DC voltage sweep analysis, RF input power sweep, RF large-signal waveforms as RF input power is swept, dynamic load line plots, RF load-pull contours of constant power delivered to the load,

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