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**SELECTABLE LIGHTWEIGHT ATTACK MUNITION OPERATING
COMPONENT OF THE GATE ARRAY**

Nanette M. Shoenfelt

April 1991



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13. ABSTRACT (Maximum 200 words) <p>The selectable lightweight attack munition (SLAM) is a small explosive armament. It can be used similarly to a mine where it can be placed on the ground to detonate when the magnetic signature of the desired target is detected. It can also be used with a tripline or to detonate after a set period of time. The operation of the SLAM is controlled by electronics with the majority of functions on a gate array. The functions of the gate array that control the operation of the SLAM are described in this report.</p>				
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it to become activated. At this point, the system performs a self-test. When the safety pin is removed, the timing for the system begins. Depending on the mode of operation that has been selected, the SLAM electronics is alerted for the appropriate signal in which it is to fire or self-neutralize.

All of the functions of the SLAM except for the use with a blasting cap are controlled by the system electronics. The SLAM uses surface mount technology with most of the functions of the munition on a gate array. This gate array is a highly customized application specific integrated circuit (ASIC).

Gate Array

The gate array logic has been divided into two parts: the operating and testing components. The operating component has been partitioned into functional blocks to facilitate the design and analysis of the system. The functional blocks can be combined to provide the logic for the entire gate array chip. The functional blocks for the operating component of the system are as follows:

A timer string	timing string type a
B timer string	timing string type b
Time out	timing for the safe separation period
Clock check	logic for checking if the main clock is fast or slow
Self check	logic for performing the system self-check
Input processor	logic for latching and processing input signals
Antidisturbance processor	logic for processing the antidisturbance sensor
Safety pin processor	logic for processing the safety pin status
Output control	logic for performing the electronic enable

The description and drawing of each functional block follows. The interconnection of the blocks is also shown.

FUNCTIONAL BLOCKS

A Timer String

The gate array contains two types of timing strings. These are the A_TIMER_STR and the B_TIMER_STR. Each string is made of six stages of ripple counters which are used to provide the timing for the entire chip. A A_TIMER_STR is the first block of each string with the remainder of the string made of B_TIMER_STR.

The A_TIMER_STR (fig. 1) is composed of six D flip-flops. The output of a D flip-flop is the same as the input; however, it is delayed one clock cycle. When these flip-flops are put into a string with the complement of the output of one used as the input to the next, the delay times increase exponentially. For example, the output of the first flip-flop is delayed one (or 2^0) clock pulse from the reset of the system (fig. 2). The output of the second flip-flop is 2^1 clock pulses. Likewise, the output of the third flip-flop is delayed 2^2 . This continues up the string, so that the output to the sixth flip-flop is delayed 2^5 clock cycles. After each of the flip-flops have been toggled, the signal is carried out as the input to the B_TIMER_STR.

B Timer String

The B_TIMER_STR (fig. 3) is very similar to the A_TIMER_STR in that it is composed of six flip-flops in a string. The outputs are again delayed in the same exponential fashion. The main difference is that the B_TIMER_STR has a test input. It is very difficult to test a long timing string since the timing gets so large. Therefore, this functional block includes a method for testing the string. The first flip-flop in the string is a selectable flip-flop. It is a D flip-flop, in which there is a choice of the SO or the PO input. If the selectable input SE is high, then SO is used as the input. But if the SE input is low, then the input that the flip-flop sees is PO. When the test signal is high, then the SE input is also high. This forces the system to use SO which makes the system similar to the A_TIMER_STR. In this way it can be tested to work just like the previous system, using only 2^5 clock cycles to get through the string. However, if there is no test input, then the PO input, which is the output of the A_TIMER_STRING, is used. This causes the string to continue with delays established in the prior block. These B_TIMER_STR blocks can be strung together to create long strings. In this arrangement, outputs can be taken from each stage of each string which makes it possible to obtain almost any time interval desired.

Time Out

The TIME_OUT functional block (fig. 4) is used to determine when the safe separation period of the SLAM has expired, thus allowing the munition to become active. The inputs to this block are four timing signals and the CARRYB_IN which is the CARRYB_OUT output from the B_TIMER_STR. The CARRYB_IN must toggle two flip-flops before being ANDed with the other timing signals. This signal then toggles the final flip-flop to show that the timing sequence has taken place.

Clock Check

There are two crystal oscillators in the SLAM that check each other. The one that provides the timing for the gate array is the primary time base (PTB); the other timer is the test time base (TTB). The CLK_CHK functional block is used in two places in the gate array. Time checks are made to see if the PTB is faster than the TTB, and the other tests if it is slower. This depends on which time base is used for which input to the block.

The CLK_CHK block (fig. 5) has the master reset, the CLK1, and the CLK2 as inputs. The CLK1 is the clock input to a four stage timing string. The output of this string is the clock signal to two flip-flops assimilated so that two sequential clock pulses will cause the output of the second flip-flop to go high. The CLK2 is also applied to the clock input of a four stage flip-flop string. The outputs of these flip-flops enter a fifth flip-flop configured so that the output of this flip-flop is a high pulse that is one clock period wide. This pulse is one clock pulse after the fourth flip-flop is toggled. The pulse is used as the reset to the two flip-flops that are run by the CLK1 string. The result of this is that if the clocks are close to the same frequency, then the flip-flops will be reset before the clock signal appears. This will in turn cause the CLK_ERROR output to remain low. If, however, the CLK2 has a lower frequency than the CLK1, the clock will occur before the flip-flops are reset causing the CLK-ERROR output to go high. This shows that the CLK2 is slow with respect to the CLK1. This check is an ongoing check for the time the chip is operating.

Self Check

A number of elements in the SLAM system are checked when the battery is initiated and the gate array chip is activated (fig. 6). The items which are inputted to be checked are the safety pin (RPIN and RPINB), the firing capacitor (CAP), the low voltage detector (LVD), the fast and slow clock checks (FAST and SLOW), the settings on the selector switch (LATCH BAD), the safety switch not in the shipping position (SHIP), and the output of the boundary scans BS_IN_CELL, which are the tests of the enable, self-neutralize, and fire outputs of the gate array (ENIST, SNIST, and FTST). If any part of the self check fails, then the firing output will be disabled.

The RPIN and RPINB inputs should be in opposite states. The CAP should be low. This represents no charge on the timing capacitor. A transistor external to the gate array verifies whether there is voltage or not on the capacitor. The LVD should be low. A low voltage detector circuit, off the chip, will give a high signal if the battery voltage drops below a certain amount. The FAST and SLOW inputs should be low. These are the outputs of the two CLK-CHK functional blocks of the gate array. The LATCH BAD signal should be low to pass the self check. It is the LATCH BAD output of the INPUT_PROC functional block. This shows that the switch position is selected and stored. The SHIP input should be low. If the SLAM's battery is activated when the selector switch is in the shipping position, then the system will fail the self-check and it will fail over. If all of these tests pass, then the second flip-flop will toggle to make the SELF_CHK OK output go high.

Input Processor

The input block (fig. 7) is used to store the switch positions in memory just after the master reset for the gate array is administered. It also is used to detect any changes in the switch positions that take place after the system is enabled. The two flip-flops in the upper left-hand corner of the diagram are used to create a signal pulse that is one PTB width in duration and begins one PTB period after the TRIGGER signal. This pulse is used as the POWER UP inputs which initiate the AD_PROC and the PIN_PROC blocks. It is also used to clock four flip-flops in this functional block. These flip-flops are employed to latch the three selector switch lines (SEL0, SEL1, and SEL2) to give the settings on the selector switch. The outputs of each of these flip-flops go to Exclusive OR gates which are the outputs of each of these gates being ANDed together. This signal goes into another flip-flop, such that if the inputs and outputs of each of the flip-flops agree, then the input to the final latch will be high. The output of this flip-flop will be high if the switch settings did not successfully latch. This is the LATCH BAD output that is tested in the SELF_CHK part of the gate array. The three switch selection lines (SEL0, SEL1, and SEL2) go into a three-to-eight decoder, providing the outputs of the block. The SHIP output is the shipping setting; the ENA settings are as follows: time demolition times of 15, 30, 45, and 60 minutes, and self-neutralization time of 4, 10, and 24 hours.

The ARM ENA input comes from the OUTPUT_CONTROL block. It is used to relatch the switch states just prior to the system enabling. If the switches are changed after this time, then the TAMPER output will go high. Therefore, the function of the SLAM will be determined by the switch settings when the battery is initiated. The switch can be changed from this time until the time the munition is enabled without any change to the mission. This can be used to hide the actual switch setting. If, however, the switch position is changed after the system is enabled, then the antitamper feature will cause the munition to detonate.

Antidisturbance Processor

This block (fig. 8) has inputs from the PTB, the 2^{12} delay from the timing string, the master reset, the power up pulse created by the INPUT_PROC block, and the antidisturbance (AD) switch input. To help facilitate the rejection of false AD detection and increase the reliability of the AD switch, this block provides the algorithm. The user desires that the SLAM not detonate with vibrations on the ground. When the AD switch is activated by a movement of the system, the ball inside the switch moves and sends a signal to this functional block. This input is again observed after a certain amount of time is determined by the timing string at the top of the diagram. If there is no change in position at this time, then no disturbance is detected. However, if there has been some additional movement in the munition, then the AD switch is addressed again after the next part of the timing string has taken place. If there is no change in the state of the AD switch at this point, then the munition will remain unchanged. If there is a change in the switch, then the AD_PROC block will output a high signal on the AD_OUT to the FIRE_SAFE block.

Safety Pin Processor

This component of the gate array is used to determine when the safety pin has been released (fig. 9). To start the timing of the gate array, a safety pin on the SLAM unit must be pulled. This pin is positioned next to a mechanical switch. Normally the safety pin microswitch is not depressed. The PIN input will be low, while the PINB will be high. This causes the RPIN to be low and the RPINB to be high. These are inputs to the SELF_CHK block which tests to see that they are in opposite states. With a low signal on the PIN input, the timing chain of flip-flops at the upper right corner of the block will not get a reset signal. Therefore, the output of the string will be low. This signal goes into an AND gate with the output remaining low. This low signal propagates to the RELEASE output showing that the safety pin has not been released.

When the safety pin is pulled, the microswitch is depressed. This means that the PIN input is high, while the PINB is low. This is also true for the RPIN and RPINB outputs. With the PIN input high, the flip-flops in the timing string will reset, and the input into the AND gate will be high. However, the low signal on the PIN input continues to the other input on the AND gate. This will still keep the RELEASE output low.

When the safety pin is completely removed, the microswitch is no longer depressed. This makes the PIN input low again. The same thing will occur as before, except that the output from the timer string is now high from the previous step. The high PIN input now gives a high signal on the other input to the AND gate making the RELEASE output high indicating that the safety pin has been removed. This output goes to start the timing sequences in another part of the gate array.

Output Control

This segment of the gate array is very important in that this is the part that determines whether or not the munition will enable the system to self-neutralize or fire (fig. 10). There are a number of timing inputs that are used to determine the times required for each event. There are also inputs for the PTB, master reset, self-test (SELF_CHK, OK), the seven ENA settings from the selector switch, the result of the low voltage detector that is still operating after the self-test occurs (LVD), the output of the off-the-chip delta-sigma modulator (VEH), and the outputs of the INPUT PROC (TAMPER), AD_PROC (AD), CLK_CHK (FAST and SLOW), and TIME_OUT (TIME_OUT). The timing is also controlled in this part of the circuit to charge the firing capacitor in order to initiate a piston actuator (CHARGE). There is also the PRE_ENA output that initiates the piston actuator that unlocks the safe and arm device. FIRE is the signal that initiates the piston actuator to move the rotor in line so that the warhead can be detonated. The SN signal is the signal that fires the rotor when it is out of line so that the rotor will be forced out of the encasement of the munition. This gives a visible means of displaying that the system has self-neutralized.

If one of the time demolition modes has been selected (i.e., ENA15, ENA30, ENA45, or ENA60 is high) and the appropriate timing has toggled the flip-flop, then the NAND gate will output high. This high signal will continue through to the CHARGE and FIRE outputs providing that the system has passed the self-test and it has not been self-neutralized. There are, however, four other methods for initiating the SLAM to fire. If the selector switch has been changed after the system has been enabled no matter what mode the munition is operating, then the antitamper feature will detonate the system. Another method of causing a high fire signal is if the munition is moved when it is in tripline mode or any other nontime demolition modes. In this case, the AD switch signal will be high which will propagate to the fire line in this block. This will detonate the munition. A third means for causing the SLAM to fire is to detect a vehicle when the mine is not in the tripline mode or any time demolition mode. The final method of firing the system is if there is a clock error or low battery after 15 min of activation, if in time demolition mode.

There are three channels for the SLAM to become self-neutralized. If the selector switch is set to one of the self-neutralization times (ENA4, ENA10, ENA24), and the appropriate time has passed, a high signal will spread to the SN output. In time demolition mode, the system will self-neutralize if a clock error or low battery is encountered within the first 15 min of activation. It will also transpire if a clock error or low battery voltage occurs anytime in one of the self-neutralization modes.

SLAM GATE ARRAY

The entire gate array (fig. 11) shows the interconnection of each of the functional blocks in the operating component of the gate array as well as the testing component. There are inputs for the timing from the crystal oscillators, the switch settings, the safety pin position, the antidisturbance switch, the low voltage detector, the firing capacitor, the delta-sigma modulator, and the test access port controller. The outputs are CHARGE, which fires the capacitors; ARM_ENABLE, which unlocks the rotor on the safe and arm device; FIRE, which detonates the warhead; SN, which self-neutralizes the munition; and TAP_MONITOR, which gives serial data as to the output of the testing function.

CONCLUSIONS

The operating component of the gate array for the SLAM has been described in detail. The gate array controls the timing for the system by receiving inputs from two crystal oscillators. The two oscillators are used to check each other to make sure that the primary time base oscillator is not too fast or slow. This primary time base is used in the timing strings to get all of the desired time delays. The gate array also locks in the switch settings and determines if they have been tampered with. The algorithm for the antidisturbance switch is also in the gate array. The primary function of the gate array is to determine when the system will fire or self-neutralize. The chip will send a signal to the firing capacitors to charge, to enable the system by unlocking the safe and arm device, to fire the piston actuators to detonate the warhead or self-neutralize the munition.

This munition is still in the full scale development stage, and there may still be minor changes to the unit before the design is finalized.

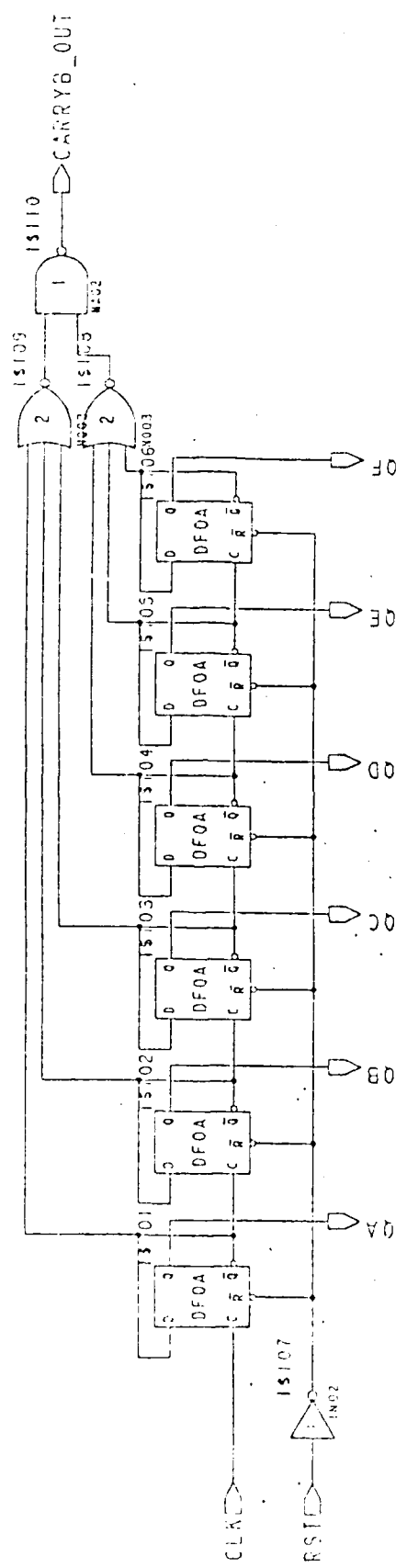


Figure 1. A timer string

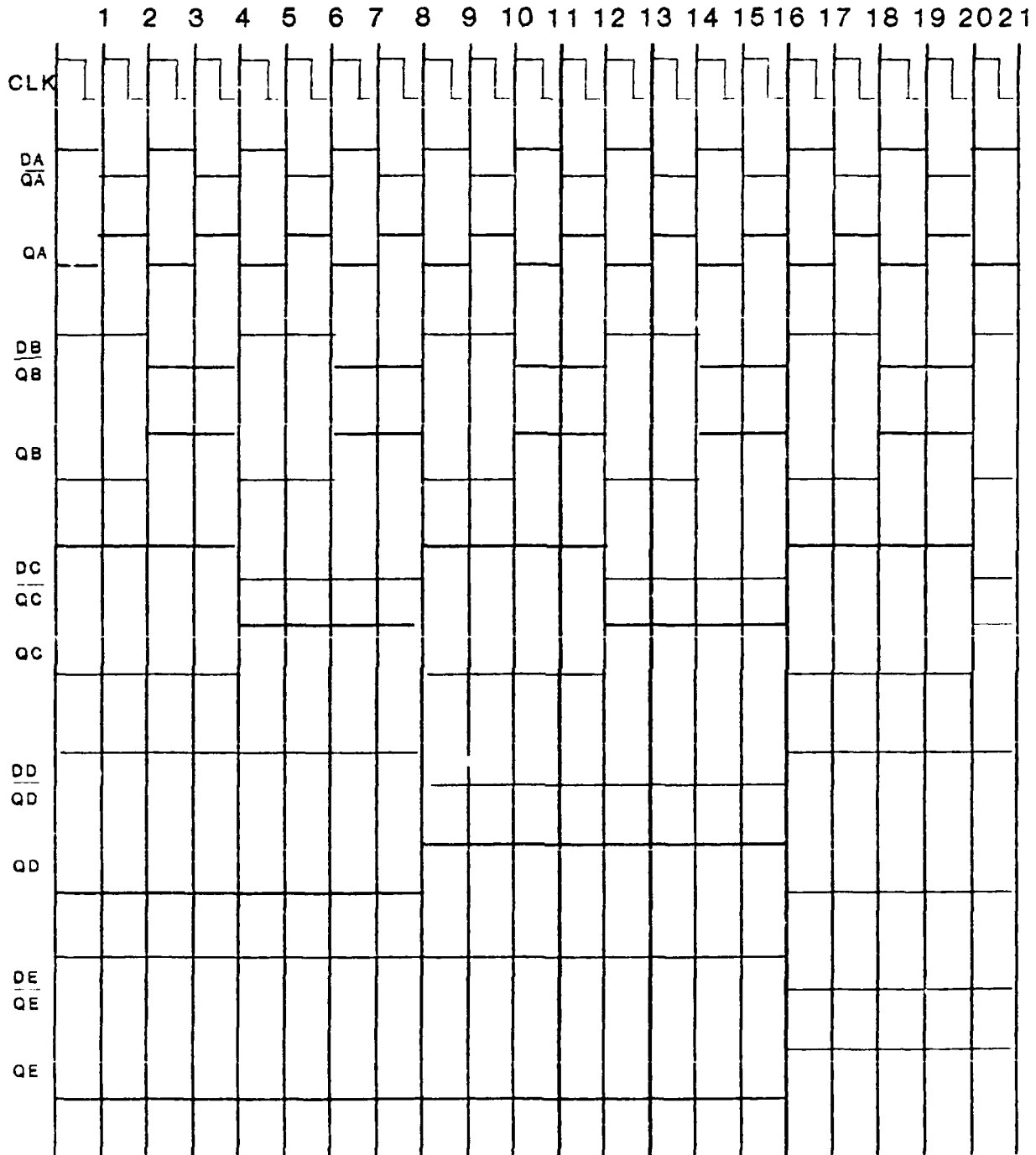


Figure 2. Timing sequence for the A timer string

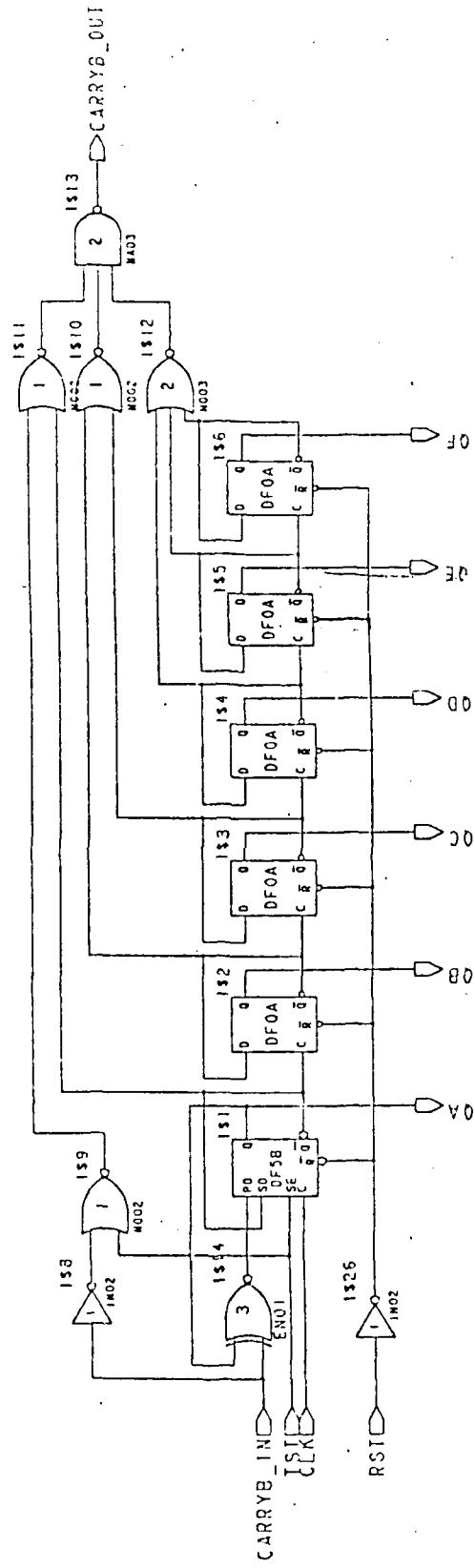


Figure 3. B timer string

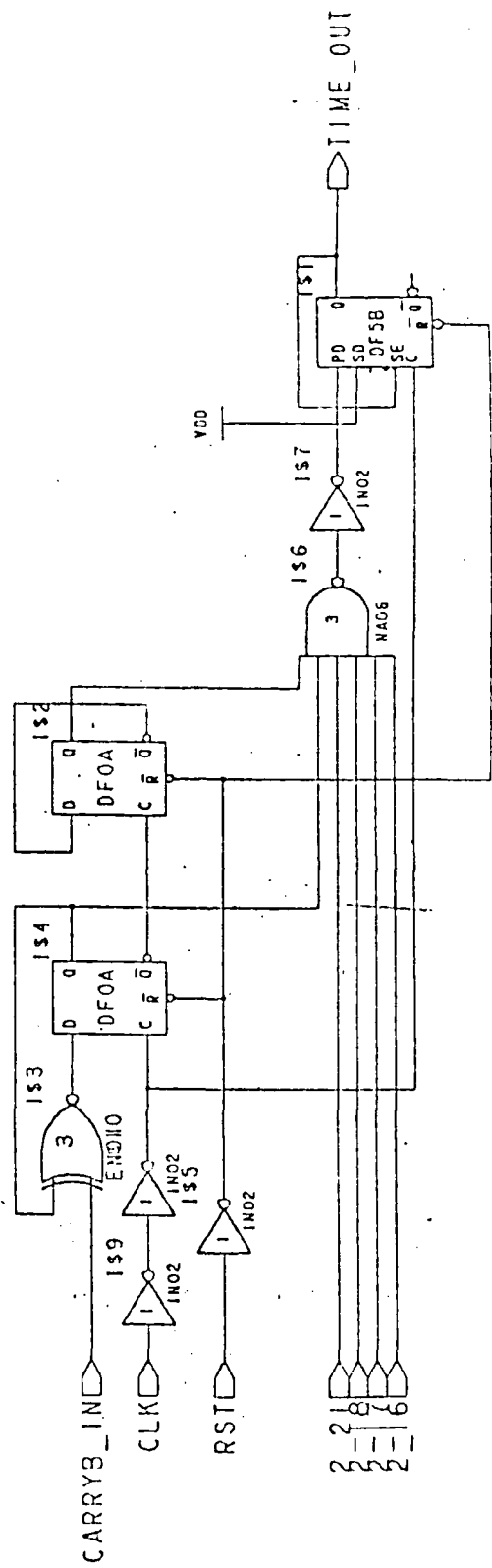


Figure 4. Time out

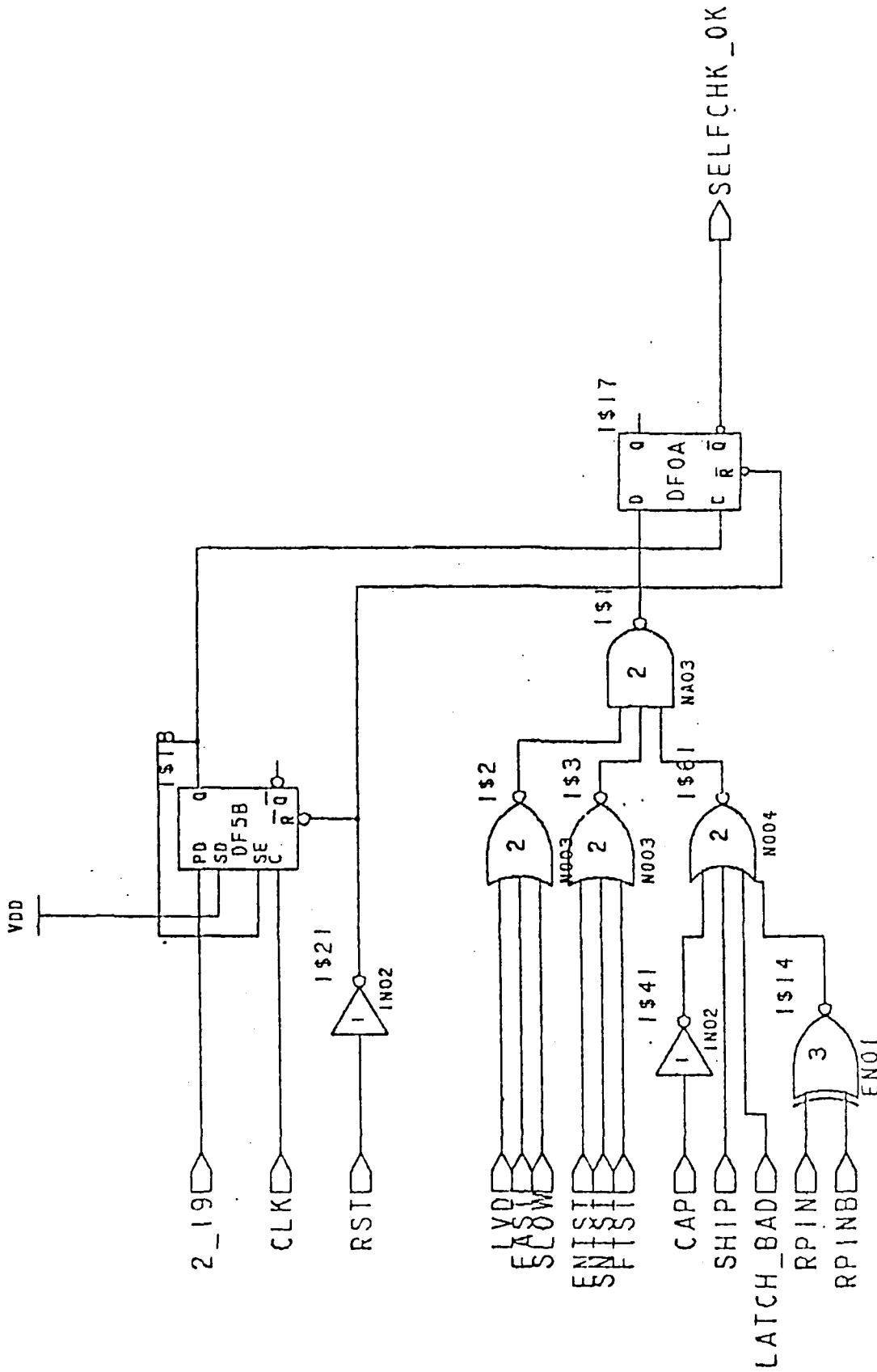


Figure 6. Self check

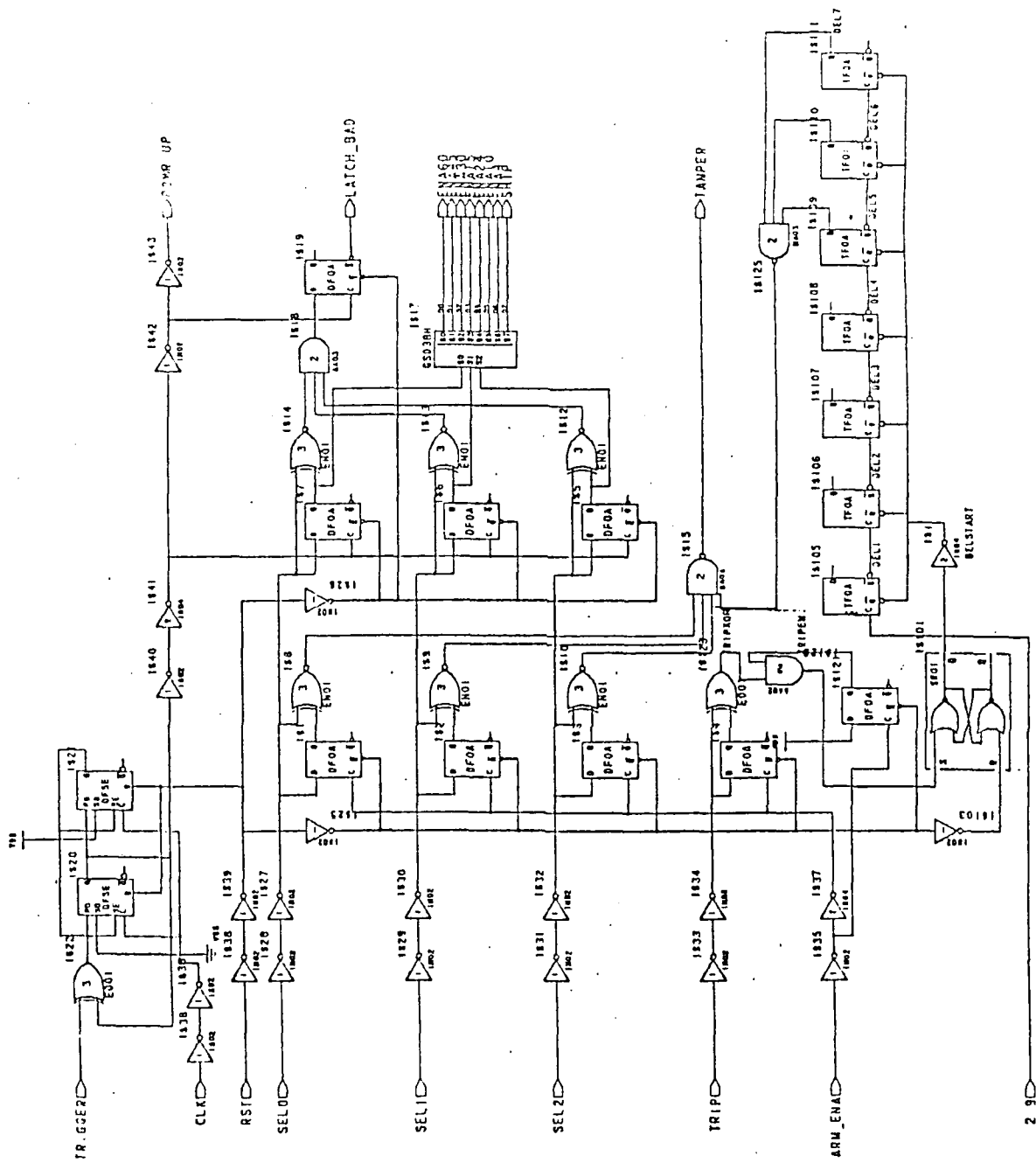


Figure 7. Input processor

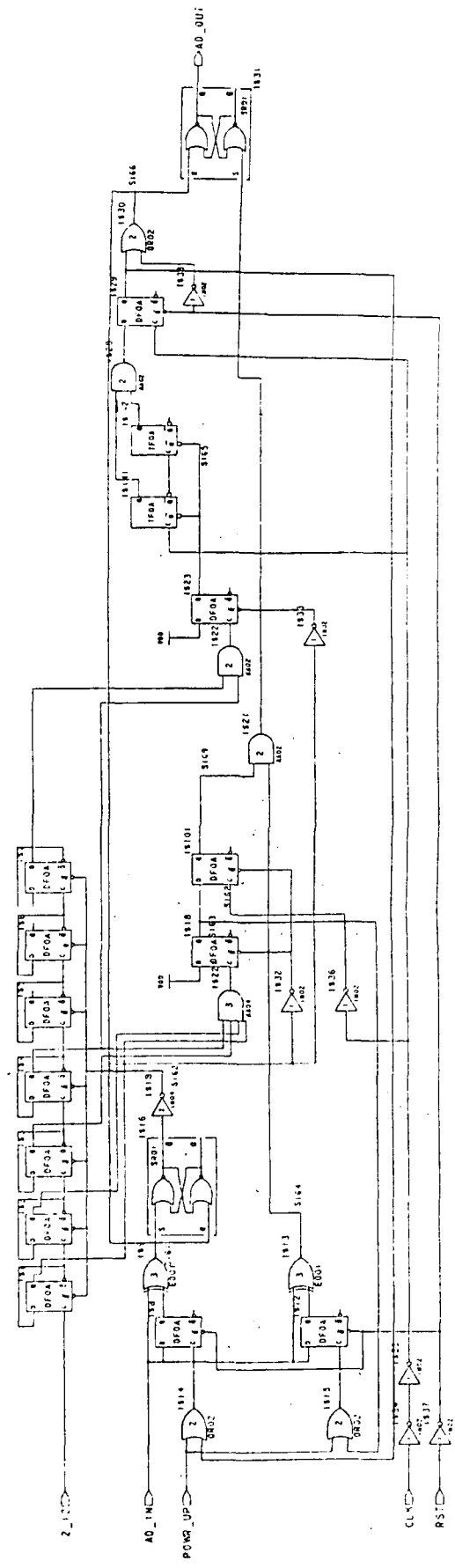


Figure 8. Antidisturbance processor

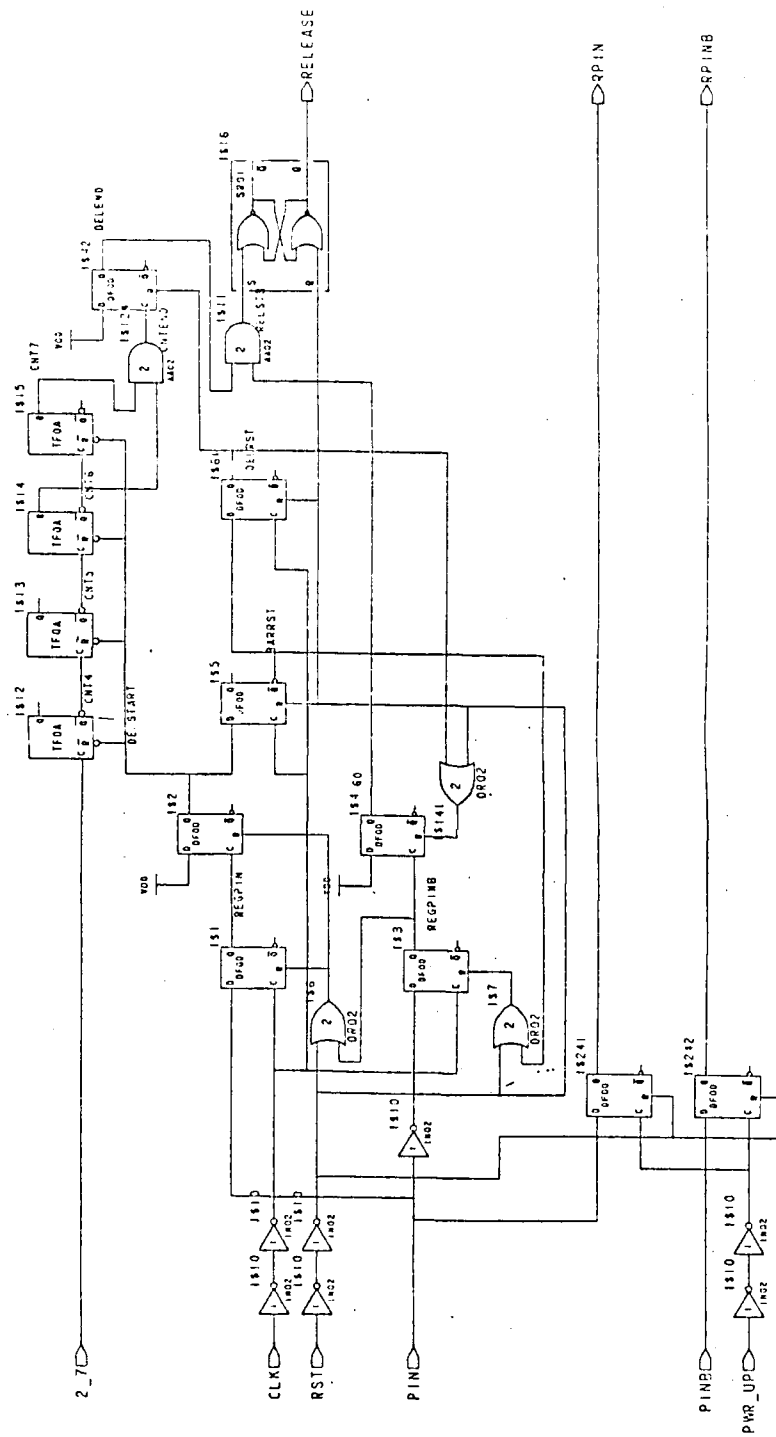


Figure 9. Safety pin processor

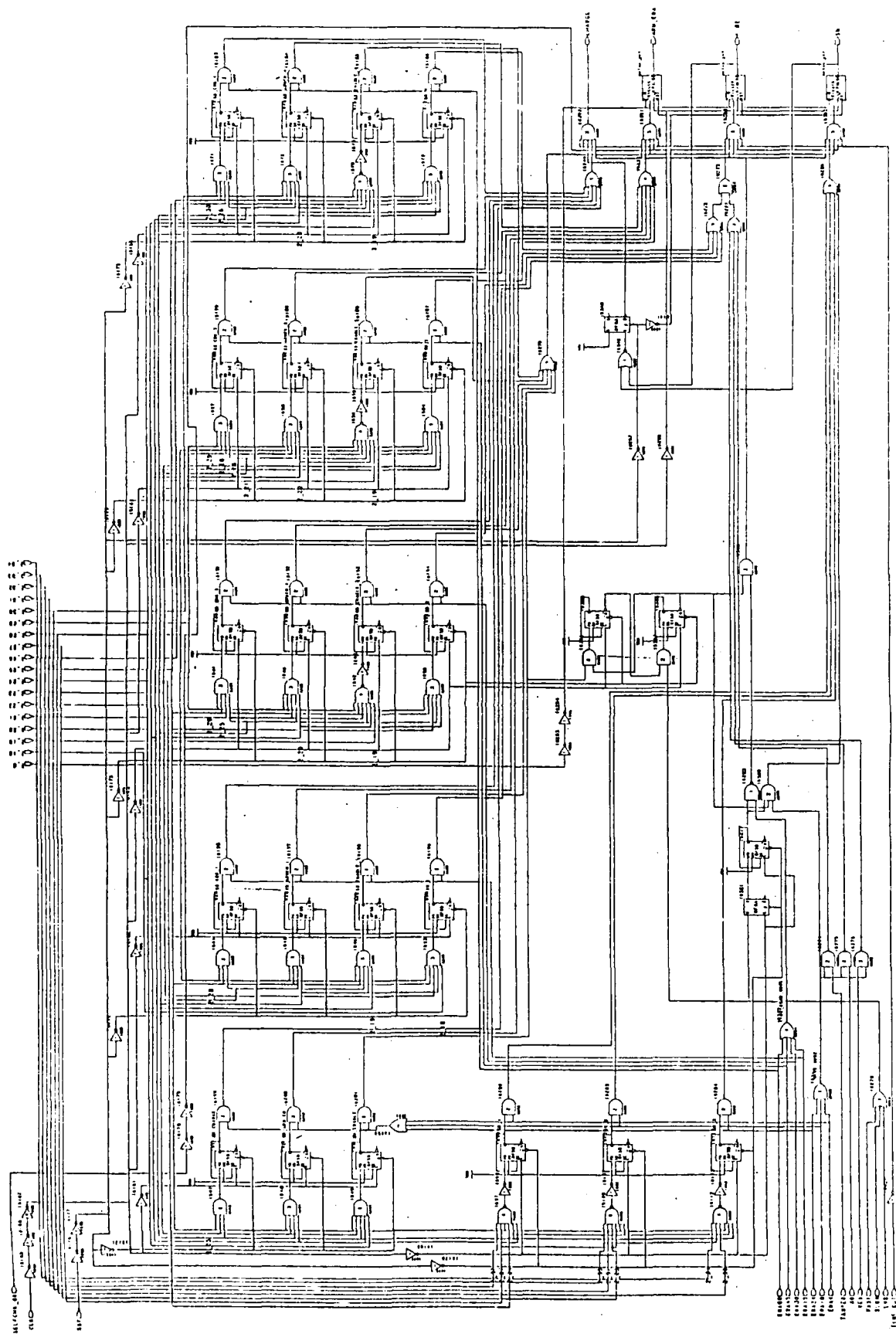


Figure 10. Output control

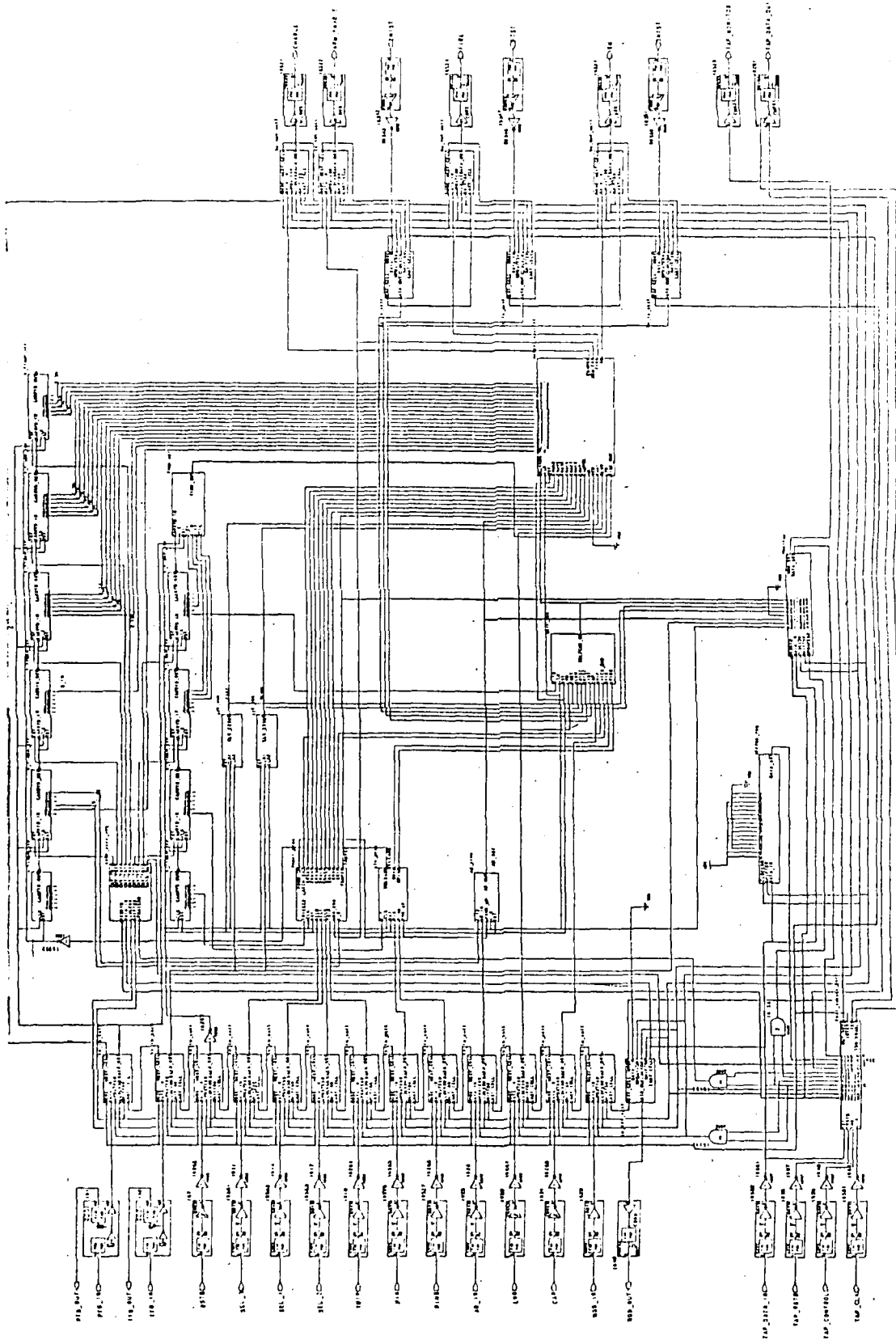


Figure 11. SLAM gate array

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2. SLAM Schematic Drawings, Alliant TechSystems, Edina, MN, 1990.

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