Electronic GaAs-on-Silicon Material for Advanced High-Speed Optoelectronic Devices

Final Report

Michael G. Mauk

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A new technology for the heteroepitaxial growth of GaAs films on silicon substrates is developed. The process utilizes a combined close-spaced vapor transport (CSVT) and liquid-phase epitaxy (LPE) technique. A thin film of GaAs is grown directly on silicon by a close-spaced vapor transport reaction using water vapor as the transport agent. This initial layer is used to seed the subsequent growth of additional layers of GaAs or AlGaAs by LPE. Selective modes of growth on oxide-masked silicon substrates were optimized. Stable light-emitting diodes were fabricated in GaAs-on-silicon material. The process is being scaled for 3-inch diameter substrates.

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ELECTRONIC GaAs ON SILICON MATERIAL FOR ADVANCED HIGH-SPEED OPTOELECTRONIC DEVICES

Contract No. DAAL03-88-C-0023

FINAL REPORT

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SUMMARY

A new method for the heteroepitaxial growth of GaAs films on silicon substrates has been developed. The approach utilizes a combination of chemical vapor deposition and liquid-phase epitaxy (LPE). Specifically, a simple chemical vapor deposition technique, known as Close-Spaced Vapor Transport (CSVT) is used to grow a thin (approximately 1 micron) film of GaAs directly on silicon. This initial GaAs layer is used to enhance the nucleation of higher quality films grown by LPE. Both non-selective and selective growth modes were successfully developed. Optoelectronic devices were fabricated in these films. The CSVT and LPE processes were scaled-up for 3-inch diameter wafers.

In the CSVT technique, growth of GaAs films on silicon is achieved by a transport reaction which produces volatile precursors of GaAs. A GaAs "source" wafer is placed over a silicon substrate, with a separation of approximately 1 mm. The source and seed wafers are individually heated to establish a temperature gradient between the source and seed. The optimum temperatures for growth were determined to be 850 °C for the source and 825 °C for the silicon substrate. A small amount of water vapor (2000 ppm_v) is added to the hydrogen/nitrogen ambient. The water vapor oxidizes the GaAs source wafer to form volatile Ga_2O and As_2. These species diffuse to the silicon substrate, where they recombine in the reverse of the oxidation reaction to form GaAs. Under these conditions, the film growth is epitaxial, with growth rates on the order of 0.1 microns/min. On patterned, oxide-masked silicon substrates, selective growth occurs such that GaAs grows preferentially in openings of the oxide mask. The CSVT GaAs films grown on silicon substrates were n-type with electron concentrations of approximately 5×10^{17} cm^{-3}. This was attributed to silicon donors from the substrate. Electron mobilities as high as 2000 $cm^2/V\text{-}s$ were measured.

The GaAs films on silicon substrates formed by CSVT were used to seed the subsequent growth of additional GaAs and AlGaAs layers by liquid-phase epitaxy. (The CSVT-grown films were necessary to enhance the nucleation of layers grown by LPE. The direct growth of GaAs on silicon by LPE was deemed impractical due to the relatively large lattice mismatch.) Normally, LPE utilizes a gallium-rich solvent for the growth of GaAs and AlGaAs compounds. In this work, a bismuth-rich solvent was used instead. Bismuth has better wetting properties, more favorable GaAs solubility, and less susceptibility to oxidation than gallium. Silicon is also much less soluble in bismuth than in gallium and this was useful for minimizing etchback of the silicon substrate. Bismuth does not adversely affect the optical or electrical properties of the GaAs or AlGaAs films. The segregation of tin (donor) and germanium (donor or acceptor) in GaAs or AlGaAs grown from bismuth-rich melts was also determined.

LPE growth of GaAs on 1-micron thick GaAs nucleation enhancement layers formed by CSVT was optimized. The best growths were achieved on (111) oriented substrates at a temperature of 825 °C, with a 15 °C supercooling. If the thickness of the LPE layer was less than 1 micron, the films were reasonably smooth and crack-free. Thicker films tended to be rougher and more susceptible to fracture and peeling. This was attributed to thermal stress effects. In fact, thermal stress was the critical phenomenon which limited thickness of the heteroepitaxial film. Selective LPE growth on CSVT mesas (with mesa areas ranging in size from 25 x 25 microns^2 to 100 x 100 microns^2) reduced thermal cracking problems considerably. It was concluded that a selective mode of growth was best suited for this type of heteroepitaxy.

LEDs and photodetectors were fabricated in heteroepitaxial GaAs-on-silicon films grown by CSVT/LPE. Stable light-emission was observed from AlGaAs/GaAs LEDs made by this process.

The CSVT process was successfully scaled up for 3-inch diameter silicon wafers. Uniform epitaxial films of GaAs were grown on (111) 3-inch diameter silicon substrates. Presently, LPE is being scaled-up to 3-inch diameter wafers.

PREFACE AND ACKNOWLEDGEMENTS

This work was funded by the Strategic Defense Initiative Organization (SDIO) as a Phase II award under the Small Business Innovation Research (SBIR) program. The contract ran from August 1988 to August 1990. The project manager was Mr. James B. McNeely. Mr. McNeely was also principal investigator from August 1988 to January 1989. Ms. Nancy E. Terranova was the project engineer from August 1988 to December 1989. Dr. Michael G. Mauk was the principal investigator and project engineer from January 1989 to August 1990. Mr. Jeffrey E. Cotter, Mr. Louis C. DiNetta, Mr. John C. Cummings, and Ms. Lara Garrett were process and device development engineers. Mr. Paul Sims was the process equipment engineer, and Mr. Philip Rabinowitz and Mr. Robert Jones were instrumentation engineers. In addition, Mr. Cotter was responsible for materials characterization and device evaluation. Ms. Margaret H. Hannon was the epitaxial growth engineer. Mr. James P. Curran, Mr. Bryan W. Feyock, and Ms. Janet L. Houser were epitaxy and processing technicians.

The assistance of Dr. Michael A. Littlejohn of the U.S. Army Research Office (Research Triangle Park, NC) is greatly appreciated, as is the advice of Mr. William D. Martin of the U.S. Army Strategic Defense Command (Huntsville, Alabama).

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1.0 INTRODUCTION

This final report summarizes progress on the "Electronic GaAs-on-Silicon Material for Advanced High-Speed Optoelectronic Devices" program conducted by AstroPower, Inc. from August 1988 to October 1990. This Phase II Small Business Innovation Research contract (# DAAL033-88-C-0023) was sponsored by the U.S. Army Research Office. Work has centered on developing a novel crystallization technology for producing heteroepitaxial films of gallium arsenide on silicon substrates. This technique was invented and demonstrated on a small scale (1 cm^2) in the Phase I period of this program [1]. The Phase II work included: 1) improving material quality, 2) material characterization and optimization of process parameters, 3) scale-up, and 4) developing the commercial potential of the process. The broad objective of the Phase II program was to develop a low-cost technology for the production of 3-inch diameter GaAs-on-silicon surrogate substrates with primary application to optoelectronic devices.

The approach is based on a combined CVD (Chemical Vapor Deposition) and LPE (Liquid Phase Epitaxy) technique. CVD is used to provide a thin (less than 1 micron) single crystal film of GaAs grown directly on silicon. The initial GaAs film functions as a nucleation enhancement layer to seed the growth of subsequent layer(s) by LPE (**Figure 1**). This "interlayer" bridges the lattice mismatch between the substrate and the GaAs layers grown by LPE. The LPE process yields films of high quality with respect to both purity and defect density. Unfortunately, the direct growth of GaAs on silicon by liquid-phase epitaxy is difficult due to the relatively large lattice-mismatch. Therefore, the GaAs interlayer formed by CVD is necessary to facilitate liquid-phase epitaxy. In general, CVD is less sensitive to lattice-mismatch than LPE. A simple CVD process, known as Close-Spaced Vapor Transport (CSVT), is used to grow the GaAs interlayer. The CVD process, as implemented here, is somewhat limited in material quality and doping, and the additional LPE step is required to improve material quality and achieve the desired impurity levels needed for high performance optoelectronic devices.

Another aspect of this program is the use of selective epitaxial growth (SEG) and epitaxial lateral overgrowth (ELO) on patterned, oxide-masked silicon substrates. In selective epitaxy, the silicon substrate is masked with a thermal oxide. Openings in the oxide, called vias, are etched in the masking layer using standard photolithography techniques (**Figure 2a**). The areas of exposed silicon at each via serve as sites of preferential nucleation during CSVT (**Figure 2b**). In this case, subsequent LPE is also selective in that its growth is limited to areas of selectively-grown CSVT (**Figure 2c**). SEG is useful for device isolation and reducing thermal stress. The thermal stress is related to the area of the selectively-grown film. Small area films exhibit less thermal stress and can therefore be made thicker

without cracking or peeling [2]. Also, the oxide film produces a compressive counterstress which will compensate the tensile stress induced by the GaAs film. With judicious selection of oxide thickness, the silicon wafer bowing can be eliminated using SEG [3].

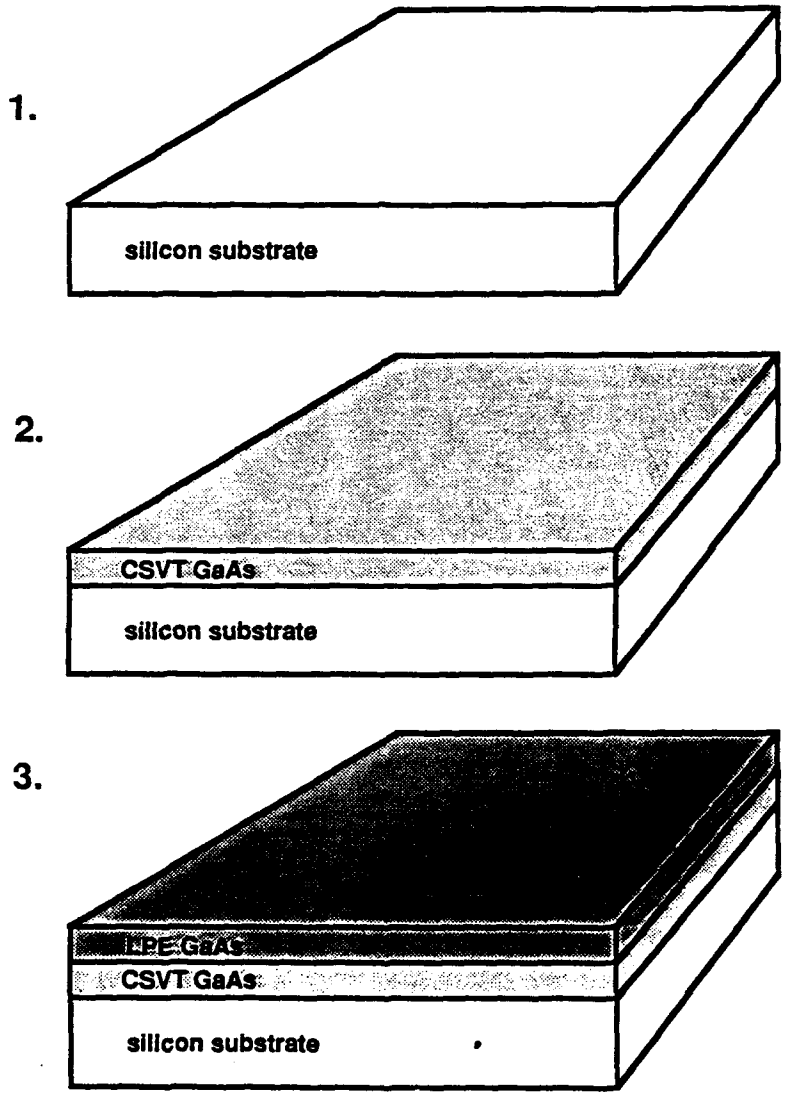


Figure 1. GaAs-on-silicon heteroepitaxy: Use of a GaAs nucleation enhancement interlayer grown by CSVT to facilitate the growth of a second GaAs layer by LPE.

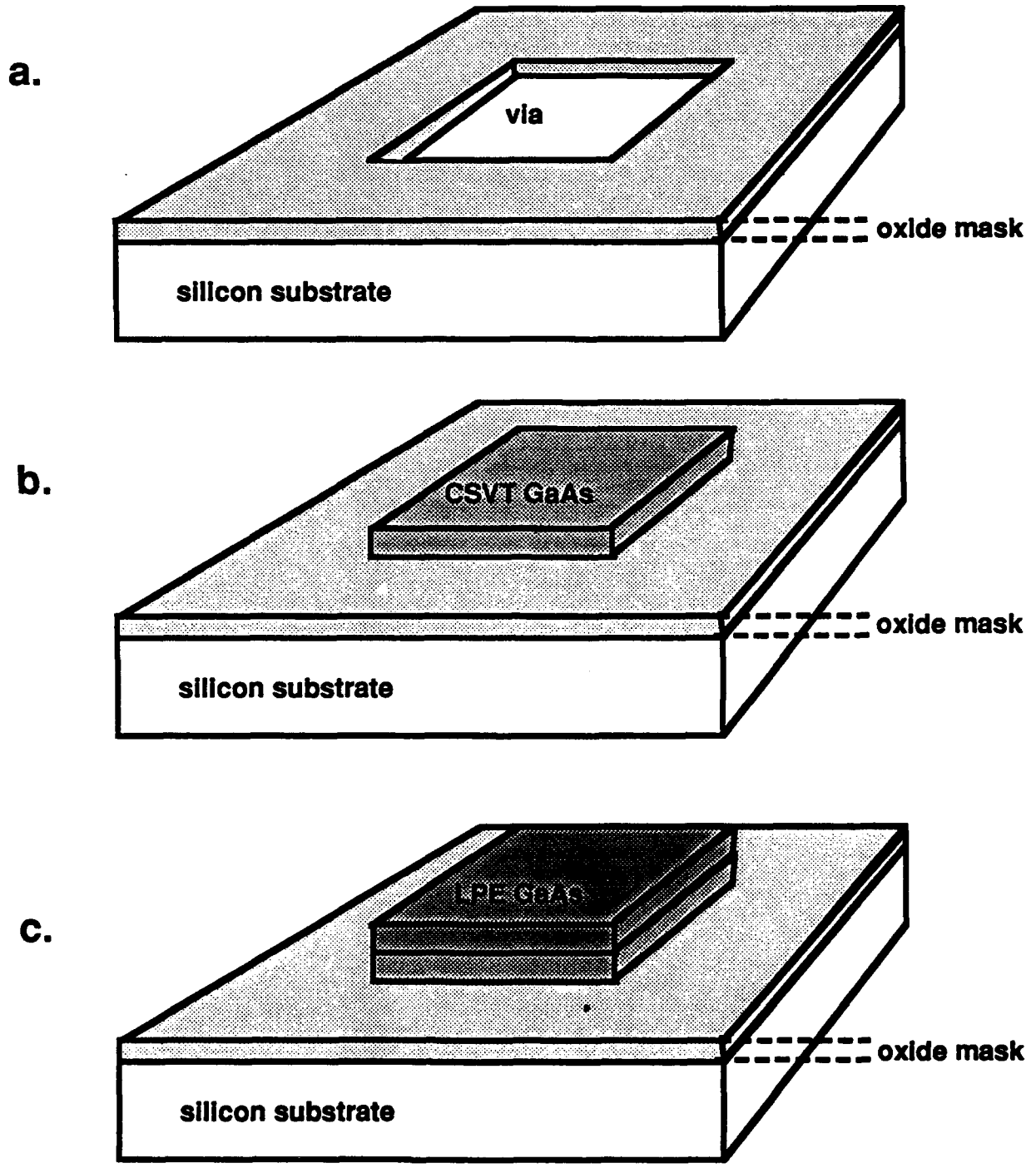


Figure 2. Selective epitaxial growth: **a.** masking and patterning of silicon wafer, **b.** selective growth of GaAs by CSVT, **c.** selective growth of GaAs by LPE.

Epitaxial Lateral Overgrowth (ELO) is an extension of SEG. LPE growth conditions are optimized such that the initial selectively-grown GaAs laterally overgrows the oxide mask and impinges to form a continuous film. For ELO, a periodic pattern of stripe vias, 5 microns in width with spacings varying from 25 to 250 microns, is commonly used (**Figure 3a**). The mask via geometry, dimensions, and its orientation on the substrate are important parameters which are addressed in the experimental optimization of ELO. The primary motivation for ELO is based on the observation that threading dislocations originate at the GaAs-silicon interface and tend to propagate vertically, normal to the plane of the substrate. In liquid-phase epitaxial lateral overgrowth, areas of the film which are overgrown on the oxide mask tend to be virtually free of dislocations [4]. This feature has been demonstrated in liquid-phase homoepitaxy of silicon-on-silicon [4,5], GaAs-on-GaAs [6], and GaP-on-GaP [7]. It is anticipated that the benefits of ELO, namely the reduction of dislocations in areas of the film grown over the oxide mask, would translate to heteroepitaxial systems as well. Lateral overgrowth also provides a certain degree of electrical isolation between the substrate and epitaxial film.

The approach of the Phase II effort may be summarized as follows. A relatively low-quality GaAs interlayer is grown directly on silicon by CSVT. CSVT provides an initial GaAs film to seed the subsequent growth of high-quality GaAs films grown by LPE. Selective epitaxial growth and epitaxial lateral overgrowth are utilized to provide device isolation and to improve material quality by ameliorating deleterious thermal stress effects and reducing the propagation of misfit dislocations.

There are several advantages of this combined CSVT/LPE approach to GaAs-on-silicon heteroepitaxy. Both CSVT and LPE are simple, inexpensive processes. Capital equipment costs are relatively low, about $20,000 for the CSVT system and $50,000 for the LPE system. No ultra-high vacuum conditions are required, which simplifies maintenance and results in a near continuous utilization of the equipment. A typical CSVT growth takes about thirty minutes and an LPE run requires about three hours. Significantly, neither process uses any toxic or pyrophoric gases, such as arsine or trimethylgallium. Both CSVT and LPE exhibit excellent selectivity, which is required for SEG and ELO. In general, GaAs films produced by liquid-phase epitaxy are of high quality with respect to both purity and defect density. Some reasons for this are discussed in **Section 4.1**. It was anticipated that many of the advantages characteristic of LPE in general would be observed in heteroepitaxial GaAs films on silicon substrates.

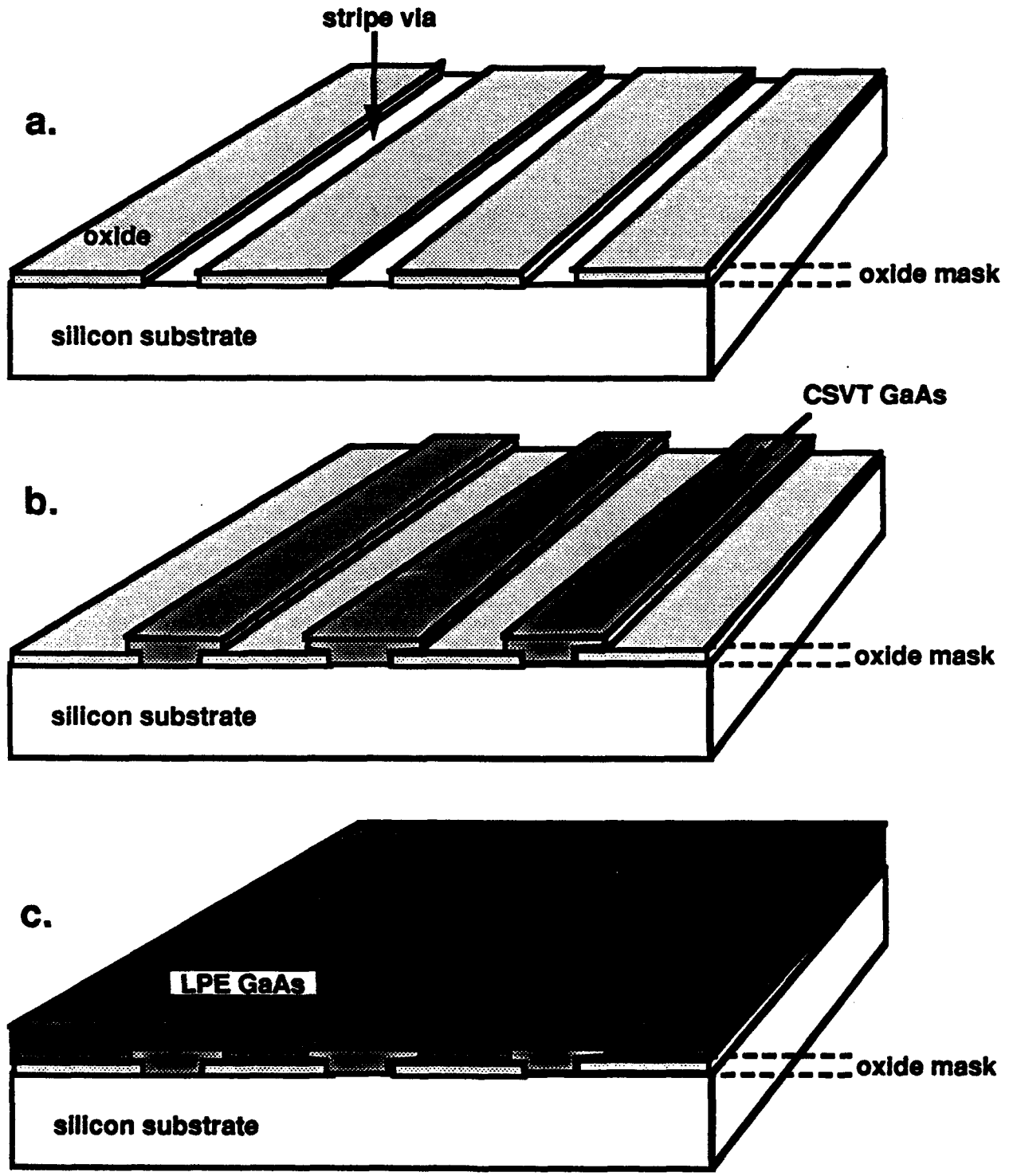


Figure 3. Epitaxial lateral overgrowth: **a.** masking and patterning of silicon wafer with stripe vias, **b.** nucleation at vias, **c.** impinging overgrowth.

Composite GaAs-on-silicon structures will serve as surrogate substrates to replace GaAs wafers. The primary intended application is optoelectronic devices, such as laser diodes, light-emitting diodes (LEDs), photodiodes, and solar cells, and other minority carrier devices such as bipolar transistors. Therefore, emphasis has been placed on achieving low dislocation densities and high minority carrier recombination lifetimes. The minority carrier lifetime, which is strongly dependent on impurity concentration and dislocation density, determines the operating efficiency of optoelectronic devices. Dislocation density is also important since the most common degradation phenomena in these devices are mediated by dislocations. Thermal stress, resulting from the unequal contraction of the GaAs film and silicon substrate upon cooling from the growth temperature to room temperature, also generates a high concentration of dislocations. Some recent evidence suggests that thermal stress may, in fact, be the dominant source of dislocations in GaAs-on-silicon films [2].

A significant part of the Phase II effort was concentrated on the scale-up of this heteroepitaxy process to 3-inch diameter substrates. This was a formidable task since there has been little previous development work on large-scale LPE or CSVT. Difficulties in scaling-up LPE involve problems associated with maintaining thickness and doping uniformity over the entire area of the substrate. The LPE process is particularly sensitive to variations in temperature and solution composition, and to convection phenomena in the solution. These issues were addressed in the scale-up work.

Section 2 reviews the scope of the Phase II work and highlights significant results. **Section 3** provides background on this topic including a brief exposition of relevant theory and a review of other similar CSVT and LPE work. **Section 4** presents an overview of the technical approach and its general features. **Section 5** describes a theoretical model for GaAs-on-silicon CSVT and its experimental verification. **Section 6** presents results of liquid-phase epitaxy experiments and the optimization of the process for the growth of GaAs films on GaAs-on-silicon produced by CSVT. **Section 7** describes the fabrication of light-emitting diodes on silicon substrates using the CSVT/LPE process. **Section 8** discusses future work and areas for improvement in the process and closes with a brief summary.

2.0 SCOPE OF WORK AND SIGNIFICANT RESULTS

The Phase II project was a device-oriented experimental program with emphasis on developing a low-cost technology for producing GaAs-on-silicon material suitable for optoelectronic applications. The major tasks of the Phase II program included:

1. The development of a Closed-Spaced Vapor Transport technique for the direct growth of GaAs films on silicon. Processes are optimized to achieve smooth, uniform, crack-free GaAs films. Growth rate as a function of process parameters has been determined.

2. Selective epitaxial growth of GaAs on silicon using CSVT. Oxide-masked silicon substrates are patterned with stripe vias. The CSVT process is optimized for selectivity and uniformity.

3. Evaluation of GaAs-on-silicon films grown by CSVT. Chemical and electrical characterization of CSVT films is performed to determine the feasibility of employing this material as an active component of semiconductor devices. The degree of electrical isolation between the CSVT film and the silicon substrate is measured.

4. Scale-up of the CSVT GaAs-on-silicon process for 3-inch diameter substrates.

5. Liquid-phase epitaxial growth of GaAs and AlGaAs films on GaAs-on-silicon structures formed by CSVT. Conventional LPE is modified to optimize the epitaxial growth of GaAs films on CSVT-grown GaAs-on-silicon layers. Novel solution compositions are investigated along with the effects of various growth parameters.

6. Selective liquid-phase epitaxial growth of GaAs and AlGaAs films on selective GaAs on silicon grown by CSVT.

7. Epitaxial lateral overgrowth of GaAs on selectively-grown GaAs CSVT.

8. Electrical characterization of GaAs and AlGaAs films grown by liquid-phase epitaxy on GaAs-on-silicon interlayers.

9. Fabrication and testing of an LED on GaAs-on-silicon prepared by a combined CSVT/LPE technique.

10. Liquid-phase epitaxy of GaAs films on 3-inch diameter silicon wafers with GaAs interlayers formed by CSVT.

Objectives 1 through 6 were successfully met. With regard to part of Objective 3 concerning electrical isolation between silicon substrate and CSVT film, the isolation provided by the (CSVT) GaAs-silicon junction was found to be unreliable. Objective 7 was met but reproducibility and uniformity of epitaxial lateral overgrowth remains a problem. Objectives 8 and 9 were both met. At present, Objective 10 is still being undertaken. The significant results of the Phase II program included:

- A reliable, consistent method of growing GaAs films directly on silicon using CSVT was developed. Smooth, uniform films of GaAs were grown on silicon with film thicknesses ranging from 0.2 to 1.4 microns. A selective mode of CSVT was also demonstrated where epitaxial films of GaAs were deposited in vias of oxide-masked substrates and virtually no GaAs was deposited on the masking layer. Although the CSVT films were not intentionally doped, they were invariably n-type which was most probably due to outdiffusion of silicon from the substrate into the GaAs film. Electron mobilities as high as 2000 $cm^2/V-s$ were measured in CSVT GaAs films on silicon. The effects of various process parameters on film quality were studied.

- GaAs-on-silicon films were produced by CSVT on three-inch diameter silicon wafers.

- GaAs-on-silicon films grown by CSVT were successfully used to seed the growth of subsequent GaAs layers by LPE. Optimum growth temperatures and supercoolings were determined. Selective LPE growth on selectively-grown CSVT GaAs was also demonstrated. SEG was somewhat limited by the edge-effects. Specifically, film growth was significantly thicker around the border than in the center of the via.

- p-AlGaAs/n-GaAs light-emitting diodes were fabricated on heteroepitaxial films grown by a combined CSVT/LPE technique.

- Design and development of an LPE system for 3-inch diameter wafers is complete and the system is operational.

3.0 BACKGROUND

Heteroepitaxy of GaAs-on-silicon is one of the most active areas of semiconductor materials research. There are two main objectives of this work. The first is to provide surrogate substrates to replace GaAs wafers for microwave and digital integrated circuits, solar cells, and other discrete optoelectronic devices. The second is the integration of GaAs-based devices with silicon circuitry, often referred to as monolithic GaAs-on-silicon (MGS). MGS devices are of interest for optical interconnects. For example, laser diodes, LEDs, and photodetectors can be grown on silicon circuits for free-space, or fiber optic interconnections between chips, boards, or processors. Another application of MGS is the partitioning of integrated circuits into GaAs-based sections for fast processing and silicon sections for high density. The Phase II program was more focused on surrogate substrate applications, although the heteroepitaxy techniques developed here are relevant to most MGS applications.

The limitations of presently-available GaAs wafers may be the most serious impediment to the further development of GaAs-based semiconductor devices [8]. Compared to commercial silicon wafers, conventional GaAs wafers are limited in size (less than 4 inches in diameter), fragile, poor thermal conductors, and have relatively high defect densities. GaAs on silicon surrogate substrates will circumvent many of these problems. **Table 1** compares presently-available Si, GaAs, and GaAs-on-Si substrates. Some of the specifications for GaAs-on-silicon substrates are speculative at present.

Table 1

Comparison of Si, GaAs, and GaAs-on-Si Substrates
(after Jordan, Pearton, and Hobson [9])

	Silicon	GaAs	GaAs/Si
Diameter (inches)	8	4	6
Density (g/cm^3)	2.3	5.3	2.3
Thermal conductivity (W/cm K)	1.4	0.42	1.4
Fracture stress (10^9 dyne/cm)	15-50	1	
Resistivity (ohm-cm)	$<10^4$	$<10^8$	10^0
Dislocation density (cm^{-2})	0	$<10^5$	$>10^6$
Bowing (microns)	<20(4")	<20(3")	
Price (1988 US$)	20(4")	200(3")	750(3")

The comparisons of **Table 1** are well-known and are compelling reasons for a GaAs-on-silicon technology. Clearly, GaAs-on-silicon surrogate substrates have good potential for significant improvements in performance over GaAs wafers. In **Table 1**, the cost of the GaAs-on-silicon surrogate substrate is more than three times greater than a similar size GaAs wafer. (Price comparisons such as these at this stage of development are somewhat speculative, however.) Therefore, an inexpensive heteroepitaxy technique is needed to realize potential cost advantages.

3.1 Fundamental Issues of GaAs-on-Silicon Heteroepitaxy.

There are several critical issues which must be addressed in formulation of a GaAs-on-silicon heteroepitaxy technology. These are now briefly reviewed.

a. Lattice mismatch. The room temperature lattice constants of GaAs and silicon are 0.5653 and 0.5431 nm, respectively. This corresponds to a lattice mismatch of about 4.1%. Lattice-mismatch is a fundamental source of strain, and misfit dislocations form to partially relieve the stress. Taking into consideration the thermal expansion of the lattice, it is noted that at growth temperatures in the range of 700 to 850 °C, the lattice mismatch is still approximately 4%. As mentioned, this difference in lattice constants tends to impede nucleation of the heteroepitaxial film, especially in the case of LPE. For example, in heteroepitaxial systems with experimentally variable lattice constants, such as InGaAsP grown on InP, the degree of lattice mismatch is observed to have a profound effect on the nucleation and morphology of the film [10]. Lattice mismatches greater than 1% appear to inhibit nucleation from the liquid phase, at least under the conditions normally encountered in conventional LPE. Film smoothness is noticeably rougher at even smaller lattice mismatches. Terracing, hillocks, and stacking faults are seen when the lattice mismatch exceeds even a fraction of one percent. These features are worsened by thermal stress effects.

b. Thermal stress. Thermal strain is another source of stress and dislocations, and also leads to wafer bowing and film cracking. In addition, highly-strained layers exhibit altered optical and transport properties. Thermal stress is due to the unequal contraction of the epitaxial film and substrate upon cooling from the growth temperature to room temperature (**Figure 4**). The slopes of the curves in **Figure 4** are the thermal expansion coefficients (TECs) for GaAs (α_{GaAs}) and silicon (α_{Si}). The total stress in a heteroepitaxial film, due to both lattice mismatch and thermal contraction, is given by [11]

$$\sigma = (1 - \eta)\ f + \eta\ (\alpha_{GaAs} - \alpha_{Si})\ \Delta T\ (E / 1 - \nu_p)$$

where σ is the thermal stress, f is the fractional lattice mismatch, ΔT is the difference between the growth temperature and room temperature, E is Young's modulus (of GaAs), and ν_p is the Poison ratio (of GaAs). η is the fractional stress relief which occurs by plastic deformation of the film and the generation of misfit dislocations. The lattice mismatch places the GaAs film in compression; the thermal expansion mismatch puts the GaAs film in tension. Experimentally, it is observed that the thermal expansion mismatch is the dominant component of stress, and the GaAs film is in tension when cooled to room temperature. (Most of the lattice-mismatch stress, typically up to 90%, is relieved by the formation of misfit dislocations at the growth temperature [12], and therefore η is close to unity). According to the above equation, the thermal stress increases proportionately with growth temperature. Therefore, there is much incentive for lowering growth temperatures in order to reduce thermal stress.

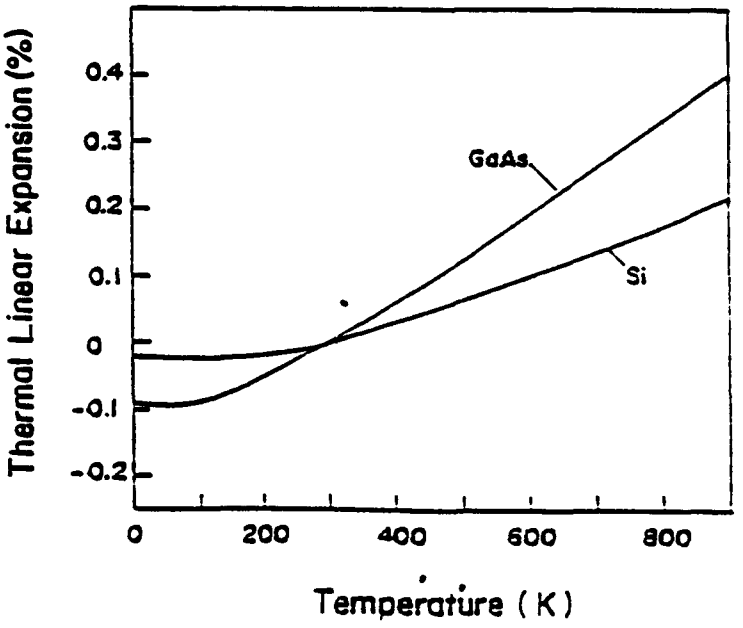


Figure 4. Thermal expansion as a function of growth temperature (from ref. 13).

For a given stress, thick films show a more pronounced tendency to fracture than thin films. This is the most critical constraint on film thickness. A theoretical prediction of film fracture is difficult. Experimental observations show that film cracking occurs at thicknesses as small as 1 micron when the growth temperature exceeds 800 °C. Lower growth temperatures can produce thicker (up to 4 microns or more) film thicknesses. Many device structures require total thicknesses at least this large. The dislocation density decreases with film thickness, because dislocations tend to annihilate as they propagate through the film from the interface to the top surface. Therefore, thicker films will exhibit lower dislocation densities than thin films.

Thermal stress is reduced when the film is grown selectively. The size of the selectively-grown area must be fairly small, however. For instance, Yamaguchi et al. [2] have shown that for GaAs-on-silicon heteroepitaxy, the stress and dislocation density are reduced by about a factor of 10 when the film area is 100 microns^2. On the other hand, selectively-grown films with areas of 10^4 microns^2 showed nearly the same stress and dislocation density as large-area, non-selectively grown films. This observation, incidently, has led these workers to conclude that thermal stress is the primary cause of strain and dislocations in GaAs-on-silicon heteroepitaxial films.

c. Formation of APDs. The growth of a polar semiconductor (e.g. GaAs) film on a non-polar semiconductor (e.g. silicon) substrate can lead to the formation of anti-phase domains. GaAs has two distinct sublattices, one consisting of Ga atoms and the other of As atoms. The sublattice allocation is determined by the first monolayer on the silicon substrate, which due to chemical bonding considerations is entirely Ga or As. Steps on the silicon surface will lead to domains with incompatible sublattice allocations (see **Figure 5**). The boundaries between these "anti-phase domains" are two-dimensional structural defects which lower carrier mobility and decrease minority carrier lifetime.

d. Charged interfaces. The interface between a polar semiconductor (with cation and anion constituents) and a nonpolar semiconductor (with a neutral constituent) can be highly charged, depending on the crystallographic orientation of the interface. It is postulated that the very strong electric field created by this charging is sustained in the growing film. At high growth temperatures, the field may cause disruption of the lattice, resulting in a high density of defects.

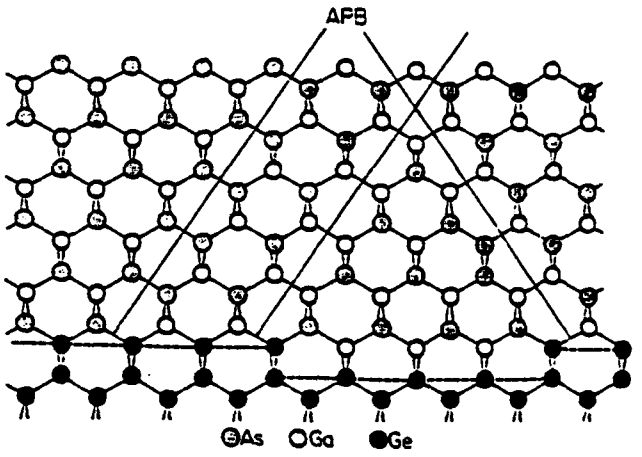


Figure 5. Antiphase domains for GaAs on (100) silicon (from ref. 14).

e. Cross-doping. Cross-doping refers to the outdiffusion of substrate silicon into the heteroepitaxial film, and the in-diffusion of Ga and As from the film into the substrate. All three of these impurities are electrically active in their respective host crystal, and may result in excessively-doped films or unwanted junctions between the substrate and GaAs film.

f. Substrate isolation. A unique advantage of GaAs (and InP) substrates is that they can be rendered semi-insulating by incorporation of transition metal impurities, which introduce deep level trapping states. A similar phenomena is not evident with silicon. Substrate isolation is important for high-speed integrated circuits, but is not critical for discrete optoelectronic devices and MGS applications.

g. Surface smoothness and film uniformity. Heteroepitaxial films tend to be rougher than homoepitaxial films grown under similar conditions. This may be a consequence of lattice-mismatch, thermal stress, non-uniform nucleation and growth, or some combination of these. Surface smoothness is needed for subsequent processing, especially for integrated circuit applications where fine-line photolithography is critical.

3.2 Mechanisms of GaAs-on-Silicon Heteroepitaxy.

Detailed descriptions of heteroepitaxial growth mechanisms are specific to the method of epitaxy (MBE, CVD, ALE, or LPE), the crystallographic orientation of the substrate, and various experimental conditions such as the growth temperature, growth rate, and surface cleanliness. Therefore, it is probably not possible at the present level of understanding to formulate a useful theoretical model of heteroepitaxy with general applicability to all situations of interest. Nevertheless, there are fundamental phenomena which appear to be common to all GaAs-on-silicon heteroepitaxy. A description of these phenomena is valuable in understanding the sources of deleterious defects such as dislocations, APDs, twins, and stacking faults; and other effects such as thermal stress and film fracture, poor surface morphology, and cross-doping.

The most studied instance of heteroepitaxy is the MBE growth of GaAs on critically-misoriented (100) silicon substrates. In-situ analysis, such as RHEED and Auger spectroscopy and electron microscopy, has revealed a detailed picture of the growth mechanisms. The case of main interest in this work is, however, the growth of GaAs films on silicon substrates using a combined CSVT/LPE process. There have been no similar fundamental experimental studies of either CSVT or LPE for the growth of GaAs on silicon. The extent to which models derived from these MBE experiments are applicable to CSVT/LPE on (100) or (111) substrates is not certain. The surface of a silicon substrate or GaAs film under ultra-high vacuum (as in MBE) is almost certainly different than the surface in contact with a liquid metal (as in LPE) or atmospheric pressure of hydrogen (as in CSVT). Most of the in-situ measurement techniques utilized for MBE are not possible with CSVT or LPE. Therefore, growth mechanisms must be conjectured by observing post-growth specimens and correlating their features with growth parameters.

In general, there are three distinct modes of nucleation/growth in epitaxy. These are depicted in **Figure 6** and are designated as [15,16]:

a. Frank-van der Merwe (also called layer-by-layer growth, monolayer growth, or two-dimensional growth). Growth occurs by adatom attachment to kinks in atomic steps on the surface of the substrate and proceeds laterally in monoatomic layers.

b. Volmer-Weber: (also called discrete growth, island growth, or three-dimensional growth). Under sufficient supersaturation, random agglomerations of adatoms become stable and grow. These nuclei eventually coalesce to form a continuous film.

c. Stranski-Krastanov: several atomic layers of two-dimensional growth followed by three-dimensional growth.

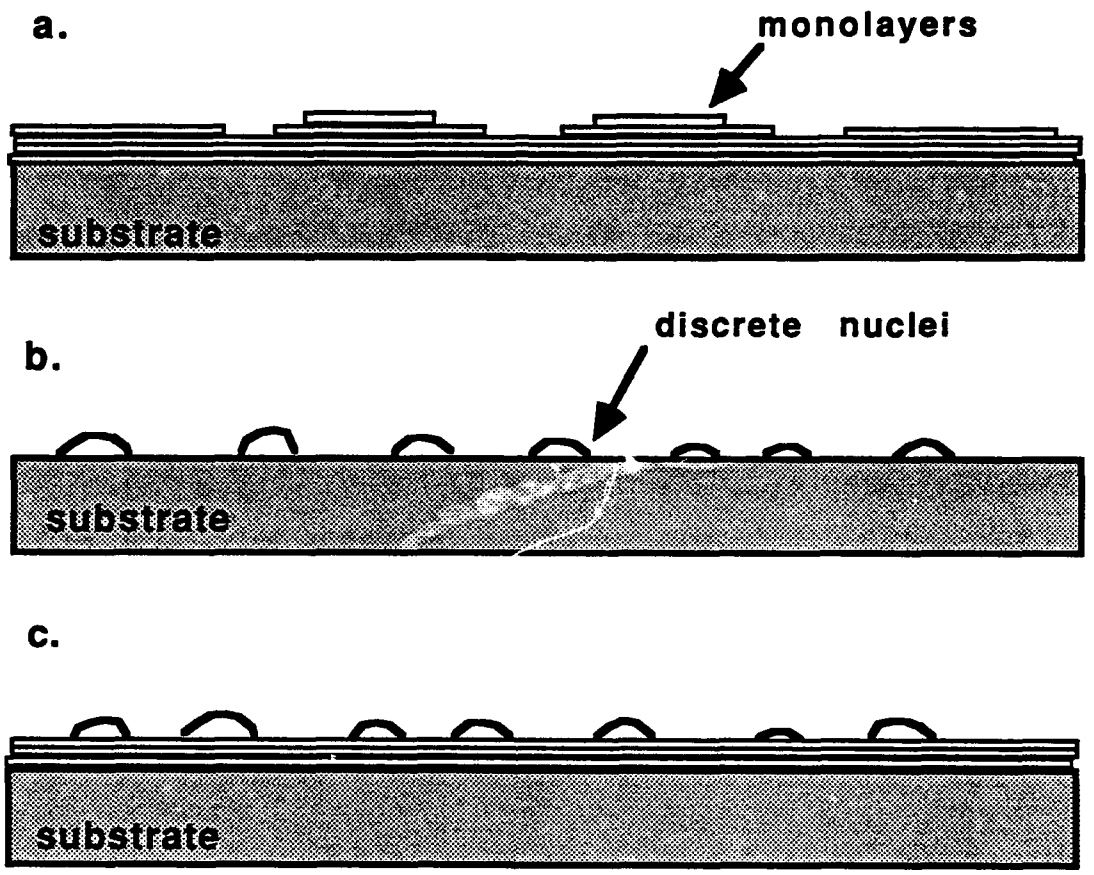


Figure 6. Modes of growth in epitaxy: **a.** Frank-van der Merwe, **b.** Volmer-Weber, **c.** Stranski-Krastanov.

Bauer [17] has formulated a criteria for determining which mode of growth is favored, based on surface energies of various interfaces. This criteria was modified by Markov and Kaischew [17,18] and may be stated as

$$\gamma_s - \gamma_{hkl} - \gamma_i + \Delta\mu \,/\, k_i\, b \quad \begin{cases} < 0 & \text{(island growth)} \\ > 0 & \text{(layer growth)} \end{cases}$$

For clarity, these interface energies are indicated in **Figure 7.** γ_s is the surface energy of the substrate in contact with the growth ambient. γ_{hkl} is the surface energy of the nucleated crystallite for a crystallographic orientation **(hkl)**. $\Delta\mu$ is the change in chemical potential associated with super-saturation. γ_i is the interfacial strain energy between the nucleated crystal, in this case GaAs, and the (silicon) substrate. This will depend on the degree of lattice mismatch. k_1 is a geometric factor. **b** is the substrate nearest neighbor atomic spacing. k_1 is 1 for (100) oriented substrates and $\sqrt{3}/2$ for (111) oriented substrates. Some generalizations can be made about growth modes using the above equation: When the surface energy of the substrate is larger than that of the overgrown film, layer growth is favored. Island growth is favored with high interfacial energies, such as those associated with lattice mismatch. High supersaturations tend to favor layer growth. For identical growth conditions, layer growth is more likely on (100) than (111) oriented substrates.

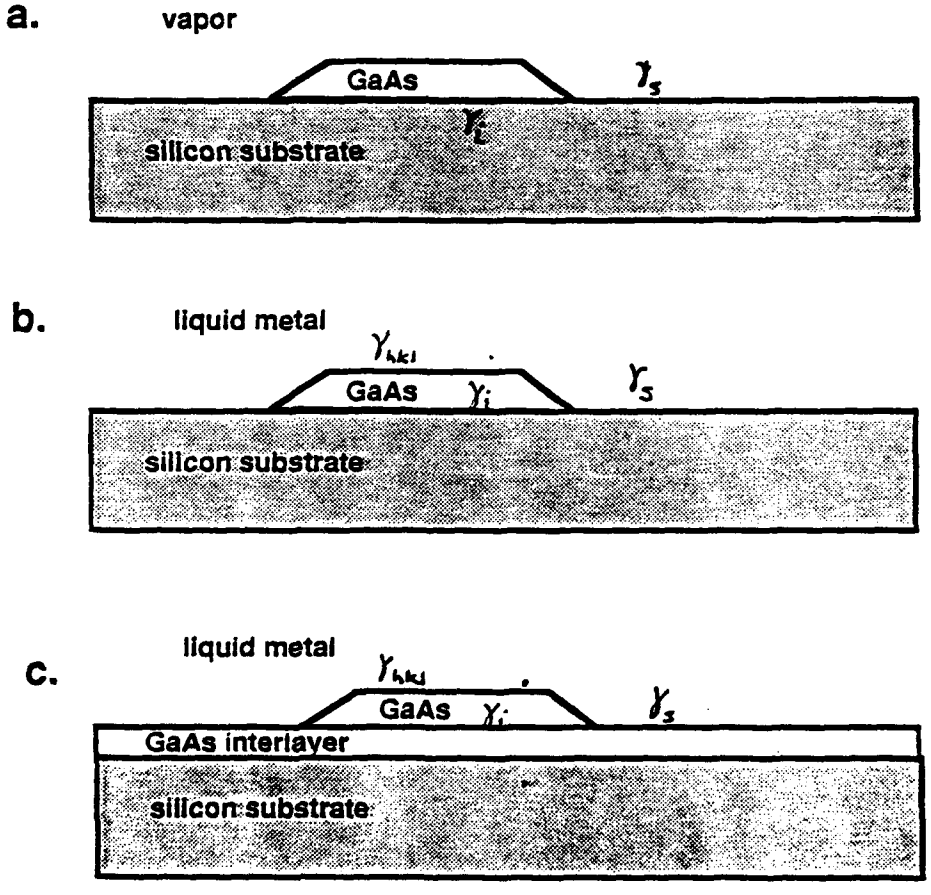


Figure 7. Relevant interfacial energies for heteroepitaxy: **a.** GaAs-on-silicon from the vapor phase, **b.** GaAs-on-silicon from the liquid-phase, **c.** GaAs-on-Si (with a GaAs interlayer) from the liquid-phase.

For a comparison of LPE and CVD (including CSVT) rough estimates of surface energies can be made. These are summarized in **Table 2**. For the case of CSVT/LPE, the interfacial strain energy σ_i, which is proportional to the degree of lattice mismatch, is much lower than for the cases of direct growth of GaAs on silicon. The reduction of σ_i favors two-dimensional growth.

Table 2

Approximate Interfacial Energies for GaAs-on-Silicon CVD and LPE

(100)Si/vapor	1600	[ergs/cm^2]
(111)Si/vapor	1400	
(100)GaAs/vapor	430	
(111)GaAs/vapor	250	
Si/liquid-Ga	390	
Si/liquid-Bi	690	
GaAs/liquid-Ga	470	
GaAs/liquid-Bi	390	

These rough estimates indicate 2-dimensional, layer-by-layer growth is favored for LPE of GaAs on silicon *with* a GaAs interlayer. In contrast, 3-dimensional, island growth is favored for LPE of GaAs directly on silicon, and for CVD of GaAs directly on silicon.

There is a general consensus that a 2-dimensional, layer-by-layer mode of nucleation/growth is superior to 3-dimensional, island growth [19]. In 3-dimensional growth, areas of impingement where discrete nuclei coalesce to form a continuous film are characterized by a variety of defects including stacking faults, antiphase domain boundaries, low angle grain boundaries, twinning, and dislocations.

Bauser et al. [20] have reported convincing experimental evidence that liquid-phase epitaxy occurs by a 2-dimensional, layer-by-layer mode of growth, at least in lattice-matched systems. As mentioned above, in lattice-mismatched systems, three-dimensional nucleation/growth is more likely.

Initially, the GaAs film grows pseudomorphically; i.e. strained such that the in-plane GaAs lattice constant is the same as that of silicon with no misfit dislocations. This is true for both 2-and 3-dimensional growth. When the film exceeds a critical thickness h_c, the strain is partially relieved by the formation of misfit dislocations. The critical thickness h_c, for GaAs on

silicon as determined by the Matthews-Blakeslee theory for a 4% lattice mismatch is about 5 nm. In actuality, there may be kinetic constraints in forming dislocations, and the critical thickness for pseudomorphic growth can exceed 5 nm. Nevertheless, in all practical cases of CSVT, it may be assumed that the GaAs film has lost its coherency with the silicon substrate and has a high level of strain-relieving dislocations. As a result of stress relaxation in heterostructures a three-dimensional dislocation network forms.

The dominant mode of dislocation formation in heteroepitaxial films with large lattice mismatches is not completely clear. Four mechanisms of dislocation generation are generally observed in heteroepitaxy [21,22]:

1. **Threading dislocations.** With small lattice mismatches (0.01 to 0.1%), a primary source of dislocations can be threading dislocations originating in the substrate. This is not considered significant in GaAs-on-silicon heteroepitaxy because the substrate dislocation density is very low.

2. **Misfit dislocations.** When the film thickness exceeds the critical thickness, the strain corresponding to the lattice mismatch is partially relieved by the formation of misfit dislocations. Misfit dislocations may form by the glide of threading dislocations originating in the substrate. More likely in the case of GaAs-on-silicon heteroepitaxy, dislocations nucleate at the free surface of the GaAs film, most probably at surface steps in the film. In 3-dimensional island growth, misfit dislocations can nucleate at the periphery of an island and propagate to the substrate-film interface.

3. **Thermal-stress-induced dislocations.** Strain-induced by unequal contraction of the film and substrate upon cooling from growth temperature will be partially relieved by the formation of dislocations. As mentioned previously, some recent experiments by Yamaguchi et al. [2] have implied that thermal stress is the main source of dislocations in GaAs-on-silicon films. Again, it seems most likely that thermal stress induced dislocations are nucleated at the free surface of the heteroepitaxial film.

4. **Stacking faults.** Contaminants on the growth surface will often lead to the stacking faults in the epitaxial film. "When the misfit between the epilayer and the substrate is large, a portion of the misfit may be accompanied by the dissociation of threading dislocations into two Shockley partials. One of the partials undergoes misfit induced glide away from the epi-substrate interface, leading to the formation of a stacking fault [21]." This mechanism is very prominent in systems with large lattice mismatch.

3.3 Previous GaAs-on-Silicon Work by Others.

A review of heteroepitaxy growth techniques up to about 1972 has been given by Milnes and Feucht [23]. This early work on heteroepitaxy included halide-transport CVD with iodine or HCl, hydride CVD with arsine, close-spaced vapor transport with water vapor, thermal and flash vacuum evaporation, sputtering, and solution growth using a tipping or slideboat technique or a traveling solvent or vapor-liquid-solid method. More recent work concerning GaAs-on-silicon has utilized MBE or MOCVD, and to a lesser extent hydride CVD. This work is extensively documented in the Proceedings of the Materials Research Society Symposia, the Journal of Applied Physics, Applied Physics Letters, the Journal of Crystal Growth, and the Journal of Electronic Materials. It will not be reviewed in detail here except where specifically relevant to the technology of this program.

3.3.1 Previous Work on Liquid-Phase Epitaxy.

Although liquid-phase epitaxy of GaAs on silicon has been reported, its use for this application remains infrequent at best. Liquid-phase epitaxy is the growth of semiconductor films from liquid-metal solutions. It is a mature, well-established technology and remains the primary method of epitaxy for production of discrete optoelectronic devices such as laser diodes and LEDs [8]. Research and advanced development of liquid-phase epitaxy appears to be especially active in the Soviet Union [24]. Detailed descriptions of conventional liquid-phase epitaxy are available in the literature [11,25,26]. Recent developments in liquid-phase epitaxy include the growth of quantum wells [27] and superlattices [28]. This work indicates some of the characteristics of LPE are not as limiting as once thought.

Most types of liquid-phase heteroepitaxy have involved combinations of films and substrates which are both closely lattice-matched and are chemically similar, e.g. AlGaAs/GaAs or InGaAsP/InP. These two considerations are the overwhelming criteria for the achievement of high quality films. The use of liquid-phase epitaxy for growth of chemically dissimilar materials with large lattice mismatches (> 1%), as in the case of GaAs on silicon, is challenging. Some work along these lines is reviewed.

Liquid-phase heteroepitaxy of GaP on silicon has been reported by Rosztoczy and Stein [29], and Beneking et al. [30]. Although chemically dissimilar, GaP is closely lattice-matched to silicon. Rosztoczy and Stein [29] described the growth of 10-micron thick GaP layers grown on silicon from both tin and lead at temperatures ranging from 850 °C (for tin) to 950 °C (for lead). Both (100) and (111) silicon substrates were used, but no preferred orientation was claimed. The liquid-metal solutions were saturated with silicon prior to growth, in order to prevent meltback of the silicon substrate. Consequently, the GaP film was degenerately

doped with silicon. (Another source of silicon dopant is out-diffusion from the substrate.) Similarly, Beneking et al. [30] grew GaP films on silicon from solutions of tin saturated with GaP and silicon. They investigated (100), (110), and (111) orientations and observed that (111) silicon substrates yielded the best GaP film morphology.

In somewhat related work, Negley [31] described a technique for growing a graded layer of GaAsP for liquid-phase heteroepitaxy of GaAs on silicon. Initially, the composition of film is GaP (closely lattice-matched to silicon), the As fraction is gradually increased over a thickness of two microns until the top of the layer is GaAs. This technique was difficult to control due to the high temperatures (> 1050 °C) required.

The growth of germanium on silicon represents a combination of two materials which are chemically similar but have relatively large lattice mismatches (4%). Donnelly and Milnes [32] described the growth of germanium on silicon from a tin-silicon solution. Trah [33], Sukegawa et al. [34], and Hansson et al. [35] also reported on the growth of Ge and SiGe alloys on silicon by LPE.

The direct growth of GaAs on silicon from liquid-metal solutions was achieved by Nakano [36] in 1967. Nakano's work was based on a travelling solvent method where liquid gallium was used as the molten zone, silicon as the substrate, and GaAs as the source material. A 20- to 50-micron thick GaAs-on-silicon film was grown at 880 °C for two to ten hours. Control of film thickness and uniformity would appear to be difficult with this technique.

Brovkin et al. [37] investigated the possibility of GaAs liquid-phase epitaxy on silicon substrates from lead-silicon-gallium-arsenic and tin-silicon-gallium-arsenic solutions. Growth on (111), (211), (311), (100), (210), (110), (331), and (221) oriented silicon substrates was studied. Best results were achieved on (100) substrates. A ramp-cooling mode of growth from 925 °C to 800 °C was used with a cooling rate of 1 to 2.5 °C per minute. The solution composition was selected such that growth occurred close to the GaAs-Si eutectic composition. The main drawback to this approach was the simultaneous growth of silicon prior to or coincident with the growth of GaAs, although this problem was minimized on (100) orientations. It was concluded that the direct liquid-phase epitaxial growth of GaAs on silicon proceeds by a three-dimensional mode of nucleation. The heteroepitaxial GaAs films were not characterized.

The high temperatures, long growth times, and large temperature excursions used in the work of Nakano [36] and Brovkin et al. [37] mentioned above imply a large impedance to nucleation, thereby necessitating high supersaturations to effect growth from the liquid phase. This is a direct consequence of lattice mismatch. Unfortunately, LPE is best operated as a near-

equilibrium process. Large departures from equilibrium result in poor film morphology, solvent inclusion, lack of film thickness control, and generally inferior material quality.

Zolper and Barnett [38] described the liquid-phase selective epitaxial growth of germanium on silicon, followed by the LPE growth of GaAs on germanium-on-silicon. In their work, germanium or SiGe interlayers were first grown to bridge the lattice mismatch between silicon and GaAs which promoted subsequent growth of GaAs by LPE. They explored a variety of solvents including bismuth, indium, lead, and several alloys. Zolper and Barnett emphasized the importance of metal solvent compositions and temperature programs which would minimize meltback of the silicon. Interestingly, Ge and GeSi crystals grown on silicon showed a well developed, faceted morphology. GaAs crystals grown using the germanium interlayers appeared somewhat irregular. Zolper and Barnett stated that the exact role of the Ge interlayer was not clear and suggested some type of wetting enhancement in addition to lattice-mismatch bridging. The selectively-grown GaAs crystals were zinc diffused to form a pn junction from which stable, room temperature infrared emission was observed under forward bias.

The use of germanium interlayers was a common technique for MOCVD growth of GaAs on silicon. Later it was concluded that the germanium interlayer was neither necessary nor desirable [39]. A high concentration of germanium in the GaAs film was unavoidable due to the high vapor pressure of germanium. Furthermore, interlayers to bridge lattice mismatch are evidently not needed in vapor phase growth. At any rate, germanium interlayers for the liquid-phase epitaxial growth of GaAs on silicon are rather limited in use. A survey of phase diagram data suggests that all common metallic solvents which will dissolve a sufficient amount of GaAs will also dissolve an excessive amount of germanium. Therefore, germanium interlayers will tend to dissolve upon contact with the solution from which GaAs is grown.

GaAs "interlayers" grown by molecular beam epitaxy on silicon to facilitate subsequent growth by liquid-phase epitaxy represent an alternate approach. This technique has been described by two groups. Sakai et al. [40-43] utilized GaAs interlayers, 2 to 3 microns thick, grown on (100) silicon by MBE. These interlayers were masked with an oxide and patterned with stripe vias 10, 20, and 50 microns wide. GaAs layers, 2 to 15 microns thick, were selectively grown in the stripe vias by liquid-phase epitaxy using a gallium solvent. Optimum growth conditions were determined to be 800 °C with a supercooling of 10 °C. They determined that the dislocation density in the LPE-grown layers was as low as 5×10^6 cm^{-2}, which was two orders of magnitude lower than in the MBE-grown GaAs interlayer [42]. Significantly, the photoluminescence intensity measured from the LPE-grown layer was 60 times stronger than from the MBE-grown interlayer [43].

van der Ziel et al. [44] grew four layer AlGaAs/GaAs double heterostructures on (100) silicon substrates. A three micron thick GaAs layer was first grown by MBE at 560 °C. The double heterostructure was grown by LPE at 700 °C and had a total thickness of 4 microns. Gallium was used as the solvent. Electroluminescence was observed from these structures, but the efficiency was low. This was attributed to excessive doping of the active layer by silicon due to etchback of the substrate from pinholes and other defects in the MBE grown film.

3.3.2 Previous Work on CSVT.

The CSVT technique was invented almost simultaneously by Sirtl [45] and various RCA groups (Nicoll [46], Robinson [47], and Gottlieb and Corbay [48]) in 1963. Detailed reviews of CSVT have been published [49-51]. In the present application, CSVT is basically a method of vapor-phase epitaxy in which GaAs precursors (e.g. Ga_2O, GaI_3 or GaCl, and As_2 and/or As_4) are transported to a substrate, where they react to form a film of GaAs. The precursors are generated in-situ by a reaction between a GaAs source wafer and a transport agent such as water vapor or hydrogen chloride. The precursors diffuse from the source wafer to the seed due to a concentration gradient which is determined in part by the respective temperatures of the source and seed. Details of the CSVT process, as applied to GaAs-on-silicon will be discussed in **chapter 5**. The CSVT technique has been used grow films of GaAs, GaP, InP, InAs, GaAsP, ZnS, ZnSe, ZnTe, CdS, CdSe, CdTe, HgCdTe, Si, Ge, SiC, SnTe, Zn_3P_2, and $CuInS_2$ [49,50]. To date, there have been no reports of CSVT applied to the heteroepitaxial growth of GaAs on silicon. With the exception of a combined CSVT/LPE technique developed by Igarashi for GaP-on-silicon heteroepitaxy [52], CSVT not been utilized to provide nucleation enhancement layers for subsequent epitaxial growth by other methods. However, CSVT growth of heteroepitaxial combinations with small lattice mismatch, such as GaP on silicon [53-55] and GaAs on Ge [45-48], and large lattice mismatch, such as GaP on GaAs [46,56,57] and InP on GaAs [47], has been reported.

3.4 Requirements of Heteroepitaxial GaAs-on-Silicon Films.

The requirements of heteroepitaxial GaAs-on-silicon films depend on the specific device application. Maximum dislocation densities and thermal stresses for several semiconductor devices are suggested in **Figure 8**. As a comparison, commercially-available GaAs wafers show dislocation densities on the order of 10^4 cm^{-2}. Presently, the best quality GaAs-on-silicon films have dislocation densities of approximately 10^6 cm^{-2}. This implies that about a two order of magnitude reduction in defect density is required for minority carrier device applications. However, Kroemer et al. [58] point out that certain minority carrier devices fabricated in heteroepitaxial films appear to tolerate higher dislocation densities than similar devices fabricated in homoepitaxial films.

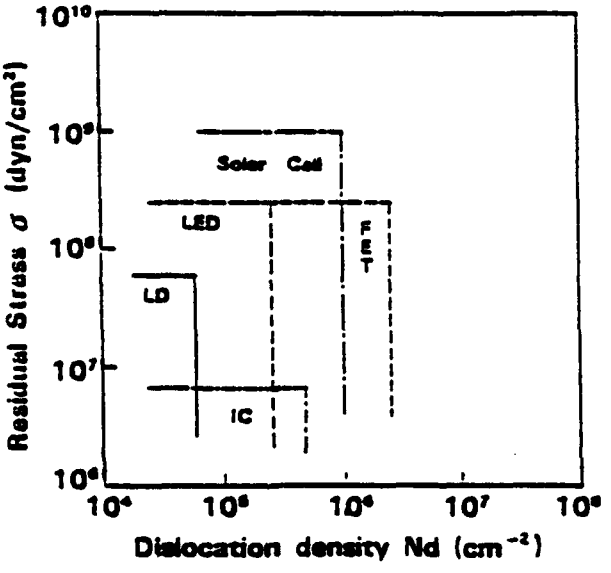


Figure 8. Stress and dislocation density requirements of GaAs-on-silicon heteroepitaxial films for various device applications (after ref. 59).

4.0 OVERVIEW OF CSVT/LPE GaAs-ON-SILICON HETEROEPITAXY

As mentioned, the direct growth of GaAs on silicon by liquid-phase epitaxy is difficult due to the relatively large (4%) lattice mismatch between GaAs and silicon. Therefore, intermediate nucleation enhancement layers, between the silicon substrate and the GaAs film grown by LPE were employed.

Both (111) and (100) silicon substrates were utilized for heteroepitaxy. The choice of substrate orientation is not trivial. Most of the Phase II work concentrated on the (111) orientation for the following reasons. It was observed that for both CSVT and LPE, higher nucleation densities and better film quality were achieved with the (111) orientation. Specifically in the case of LPE, films grown on (111) oriented substrates showed better surface morphology than that of films on (100) substrates for similar conditions; inadequate nucleation was often observed on (100) substrates. This was in marked contrast to the general consensus that (100) substrates yield better film morphologies than (111) substrates. Second, other work has indicated that anti-phase domains do not occur with epitaxial films of GaAs (or GaP) grown on (111) silicon [60]. Third, due to anisotropic growth rates, epitaxial lateral overgrowth works best on (111) substrates. However, significant lateral overgrowth is also possible on (100) silicon substrates.

4.1 Advantages of CSVT/LPE Approach.

Since the approach taken here is rather unique, its demonstrated and potential advantages are now briefly reviewed.

Liquid-phase epitaxy produces high-quality GaAs films. This may be attributed to: 1) the preferential segregation of impurities to the liquid phase which results in very pure films, 2) the availability of high purity metallic solvents, 3) the reduction in point defects, 4) the ability to anneal out threading dislocations originating from the substrate, 5) the high mobility of adatoms in the liquid phase compared to the slower surface diffusion upon which vapor-phase and vacuum epitaxy techniques rely, and 6) the fact that growth takes place very close to thermodynamic equilibrium. Stringfellow [61] has noted that LPE produces GaAs with the most Ga-rich stoichiometry: "Thus, defects such as Ga vacancies and As atoms on Ga sites (the As antisite) are virtually non-existent in LPE material. The As antisite defect is believed to be related to the deep electron trap denoted EL2, which is known to have a deleterious effect on several materials properties." Another advantage of LPE is the wide selection of dopants available.

The advantages of CSVT are also significant. CSVT is a simple process using relatively inexpensive equipment. CSVT exhibits excellent selectivity and good film uniformity. The process does not require or produce any highly toxic substances. CSVT is an easily controlled process with a small number of growth parameters. More specifically, growth rates are diffusion-controlled and the rate of diffusion is determined foremost by the source and substrate temperatures, which are easily regulated. The diffusion of growth precursors occurs in a stagnant ambient between the source and seed. Therefore, complexities of flow and mass transfer, which complicate other CVD techniques, do not limit CSVT. These factors facilitate scale-up to large-diameter wafers.

5.0 GaAs-ON-SILICON CSVT

Experimental studies undertaken in this work have shown that the phenomenon of Close-Spaced Vapor Transport for the growth of GaAs films on silicon substrates is very similar to that reported for CSVT growth of GaAs on GaAs. The model of Perrier et al. [49] and Cote et al. [50,51] is especially useful in understanding the mechanisms of CSVT growth. The chief difference between GaAs-on-Si CSVT heteroepitaxy and GaAs-on-GaAs CSVT homoepitaxy is the propensity for the silicon substrate surface to oxidize. Obviously, such oxidation is highly undesirable and its avoidance places certain constraints on CSVT growth parameters.

A GaAs source wafer and silicon substrate are placed in close proximity, separated by a distance of about 0.35 mm. In the thin space between the source and seed wafer, a transport agent (in this case water vapor) is introduced. The source and seed wafers are separately heated to establish a temperature difference of about 25 °C, with the seed wafer being colder than the source. The GaAs source wafer is oxidized by water vapor to form volatile gallium oxide (Ga_2O) and arsenic (As_2 and As_4).

$$2\ GaAs + H_2O \rightleftharpoons Ga_2O + As_2\ (\text{or } 1/2\ As_4) + H_2$$

These volatile species diffuse to the seed wafer where they recombine to form GaAs in the reverse of the above reaction, which is favored at lower temperatures. Provided parameters are optimized, a smooth, uniform epitaxial film of GaAs can be grown on the substrate. The important growth parameters of this process are: 1) the time-temperature program of the source and seed wafers (heat-up, steady-state "peak" time, and cool-down), 2) the spacing between the source and seed, 3) the water vapor pressure, and 4) the crystallographic orientation of the seed wafer. Parameters of lesser importance include the flow rate of ambient gas carrying the transport agent, and the orientation and surface condition of the source wafer.

One feature of CSVT which should be noted is that the transport agent is recycled by the reverse reaction at the seed wafer. Therefore, once the correct water vapor concentration is established, it will remain constant during the growth process. This simplifies control of the CSVT process, relative to other vapor-phase epitaxy techniques, since the replenishing of growth precursors is not necessary.

According to the model of Cote et al. [50,51], the CSVT growth rate is determined by the flux **J** of Ga_2O molecules incident on the seed surface. This flux originates from the concentration gradient resulting from the relatively high partial pressure of Ga_2O at the source wafer and the lower partial pressure of Ga_2O at the seed. (In accordance with the above reaction, Ga_2O is being produced at the source wafer and consumed at the seed wafer.) It is assumed that reaction kinetics and surface diffusion are not rate limiting.

$$J = D \, \Delta C_{Ga2O} / d$$

where **J** is the Ga_2O flux [moles/cm^2-s], **D** is the diffusivity of Ga_2O in the growth ambient [cm^2/s], **d** is the separation of the source and seed [cm], and **ΔC** is the Ga_2O concentration difference between the source and seed [moles/cm^2]. The concentration of Ga_2O is related to the partial pressure of Ga_2O from the ideal gas law, which in turn may be estimated from equilibrium relations for the above reaction.

$$C = p / R T$$

where **p** is the partial pressure of Ga_2O [atm], **R** is the gas constant [atm-l/mole-K], and **T** is the temperature [K]. The partial pressure of Ga_2O may be estimated from equilibrium considerations using the relation.

$$K(T) = P_{Ga2O} \; P_{As2} \; P_{H2} / P_{H2O} = \exp(-\Delta G(T) / RT)$$

where **K(T)** is the temperature-dependent equilibrium constant for the CSVT reaction and **ΔG(T)** is the temperature-dependent free energy change of the reaction. Hydrogen is a component of the carrier gas, and its partial pressure is taken as a constant. The partial pressure of water vapor, relative to hydrogen, is an experimentally controllable parameter **r** which is defined as

$$r = P_{H2O} / P_{H2}$$

and therefore, assuming $P_{Ga2O} = P_{As2}$

$$K(T) \; r = (P_{Ga2O})^2 = r \exp(-\Delta G / R T)$$

The partial pressure of Ga_2O can thus be related to the source and seed temperatures. The Ga_2O flux is therefore

$$J = (D_{Ga2O} / d) \{ [r K(T_2)]^{1/2} / R T_2 - [r K(T_1)]^{1/2} / R T_1 \}.$$

The growth rate **GR** [microns/min] is related to the net Ga_2O flux

$$GR = J M (60 \times 10^4) / \rho$$

where **M** [g/mole] is the molecular weight of GaAs and ρ is the density of GaAs [g/cm^3]. The growth rate depends on the temperatures of the source (T_2) and seed (T_1), the spacing between the source and seed **d**, and the ratio of water vapor pressure to hydrogen pressure **r**. For the case of GaAs homoepitaxy, this functional dependence of growth rate on parameters T_1, T_2, **d**, and **r** has been verified [50].

In this work, the dependence of **GR** on temperature has been investigated in two ways. In the first case, the source and seed temperature are varied, keeping ΔT constant. For the relatively small range of temperatures (approx. 800 to 900 °C) investigated, the growth rate will then vary with substrate temperature as

$$\log GR = C_1 / T_1 + C_2$$

where C_1 and C_2 are constants. This is a direct consequence of transport controlled by an equilibrium displacement. For small ΔT ($\Delta T = T_2 - T_1$), and constant substrate temperature T_1, the growth rate is proportional to ΔT

$$GR \propto \Delta T$$

These two relations were verified in the experimental work (**Section 5.2**) for GaAs-on-silicon CSVT.

5.1 CSVT Apparatus.

Two types of CSVT reactors were used: a horizontal tube system in which the source and seed wafers are individually heated with external infrared lamps in an enclosed furnace, and a belljar system where the source and seed are mounted on a fixture and heated by electric resistance elements. Results were substantially similar for both systems. The horizontal tube system had a faster turn-around time since it cooled more quickly than the belljar system. The horizontal tube system thus permitted a larger number of experiments and was therefore used in studies to optimize growth parameters. These experiments utilized small area (approximately 1 cm^2) substrates and determined the optimum parameters (time-temperature program of the source and seed wafers, water vapor concentration, gas flow rate, etc.) for the best film quality. On

the other hand, substrate size is limited in the horizontal tube system by the diameter of the tube and furnace. The belljar system was more amenable to scale-up, and was used for the 3-inch diameter substrates. These systems are now described.

The horizontal tube system is shown in **Figure 9**. The heating fixture which holds the source and seed is shown in **Figure 10**. It consists of two graphite plates in contact with the source and seed wafer which are separated by a quartz ring. A quartz-sheathed type K (Omega) thermocouple is embedded in each graphite plate. The tube furnace (Research, Inc., Minneapolis) has four infrared lights which are separately controlled to individually heat the source and seed wafer. The heated length of the furnace is 25 cm and the total length of the tube is 150 cm. The tube is sealed with stainless steel compression fittings. Fittings to accommodate the thermocouples, heater leads, and gas inlet and outlet were machined into the end seals. The infrared lights were powered by "zero-cross" 220V/20A SCRs which were controlled by LFE programmable microprocessor-based controllers. Control of each heater was based on the differential input between the set-point temperature of the program and the signal of the thermocouple embedded in each graphite plate. The time-temperature program of the source and seed could be controlled within 2 °C.

The belljar system is shown in **Figure 11**. The gas flow arrangement, and heater control and power are the same as in the horizontal tube system.

5.2 CSVT Procedure and Process Parameters.

The silicon substrates were nominally on-axis (111), n-type phosphorus-doped (0.02 to 0.05 ohm-cm) wafers obtained from Unisil, Inc. (lot # N13). The silicon thickness was 13 to 17 mils. For most experiments, the three-inch diameter wafers were scribed into smaller rectangles (1 x 2.5 cm^2). Several experiments which investigated the effect of crystallographic orientation on growth characteristics used silicon wafers from other vendors (Aurel and Monsanto). The source was a nominally undoped, high resistivity (100) GaAs wafer supplied by ICI Wafer Technology, Inc.

Prior to growth, silicon substrates were cleaned with a 10 minute immersion in boiling 1:1 H_2SO_4 (conc): H_2O_2 (30%), rinsed for 5 minutes in a DI water cascade, dipped for 10 seconds in a 1:1 HF:H_2O solution, and given a final rinse in a DI water cascade until a water resistivity of 18 megohm was achieved. Initially, the GaAs source wafer was cleaned by immersion in a H_2SO_4:H_2O_2 etch and rinsed. It was not cleaned between growth runs. The silicon substrate and source were then loaded into the CSVT system. The system was purged for ten minutes with dry forming gas (85% N_2, 15% H_2; dew point = -50 °C = 40 ppm_v H_2O) before initiating the heating cycle. The forming gas was dried using a packed bed of anhydrous $CaSO_4$ crystals as a desiccant (Drierite Corp, Model L68GP).

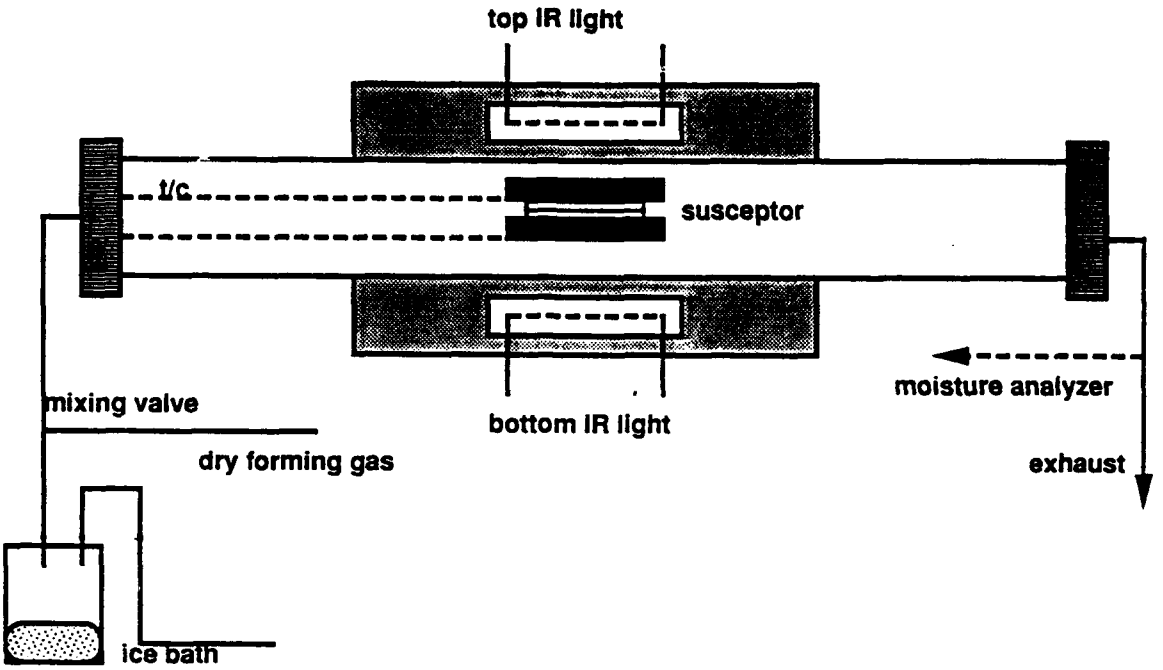


Figure 9. Horizontal tube system for CSVT.

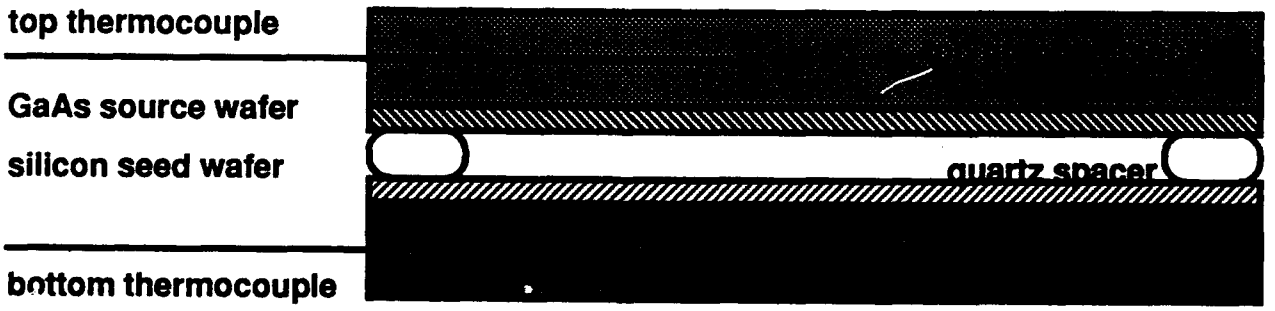


Figure 10. Heating fixture for CSVT system.

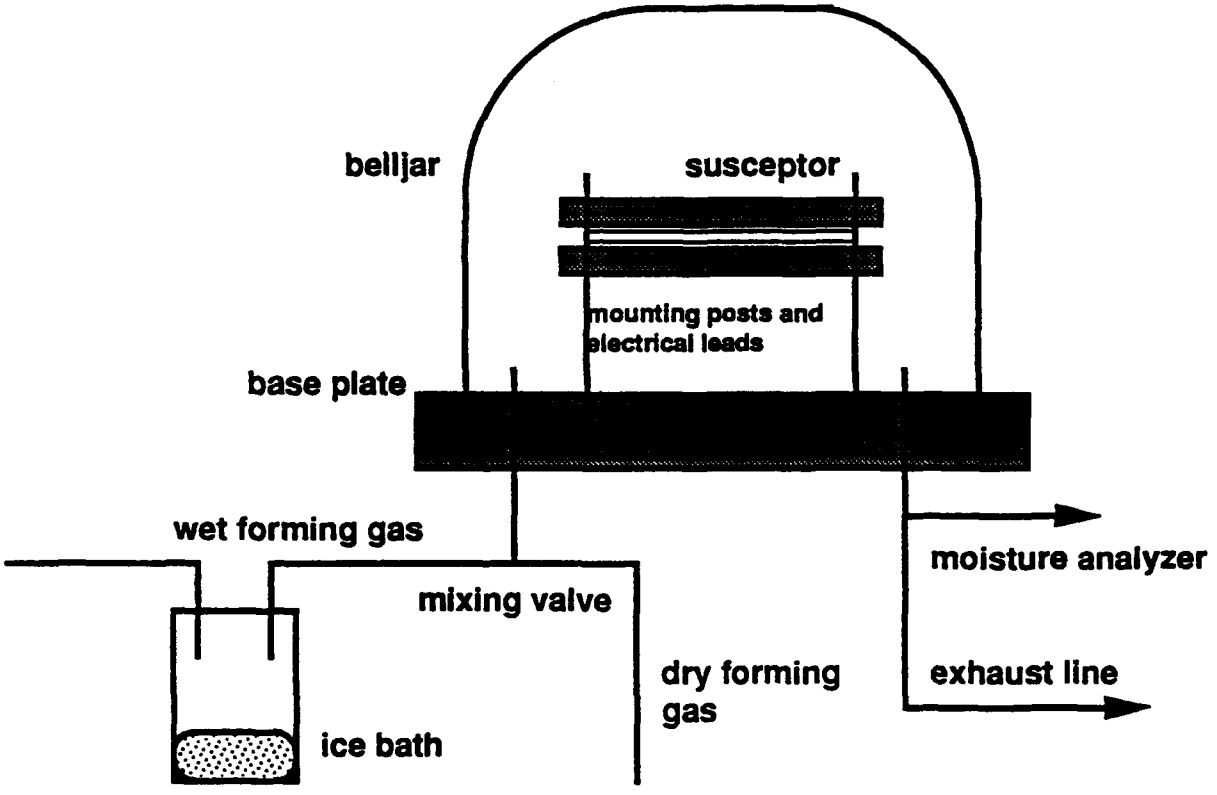


Figure 11. CSVT belljar system schematic.

Before initiating the heat-up, the forming gas was mixed with a small amount of water vapor. As might be expected from the stoichiometry of the oxidation reaction, the concentration of water vapor was an important growth parameter. The forming gas was saturated with water vapor by passing it over an ice and water bath held at 0 °C. This wet forming gas was mixed with a dry forming gas in proportions needed to yield the desired dew point and a total flow rate of about 2.8 liters/min. The moisture content of the forming gas, after exiting the growth chamber, was monitored with an electronic dew point meter (Vaisala Model HMI33). The accuracy of the dew point measurement was within 1%. Dew points

ranging from -20 °C (1000 ppm$_v$ H_2O) to 0 °C (6000 ppm$_v$ H_2O) were investigated. The optimum dew point was found to be -11.5 °C ±0.7°C (= 2200 ppm$_v$ ± 100). The effect of water vapor on film quality is discussed on page 33.

A fused quartz ring was used to separate the source and seed wafer. The growth rate is inversely proportional to this spacing. The separation between the source and seed was also observed to have some effect on film morphology. Spacer thicknesses of 5, 10, 20, 30 and 40 mils were investigated. An optimum spacer thickness of 15 mils (0.37 mm) was determined.

A typical time-temperature program for the source and seed is shown in **Figure 12**. This plot defines the heat-up, peak-time, and cool-down. The heat-up is especially critical since it is presumed that in this stage the nucleation of the film begins. The initial nucleation of the film is the major determinant of film quality. The driving force for nucleation is related to the temperature difference between the source and seed, ΔT. ΔT can be quite large during the heat-up cycle and therefore the relative source and seed temperatures must be carefully controlled. During the cool-down, the source and seed should ideally be kept at the same temperature in order to prevent extraneous growth at low temperatures which would be of poor quality. The optimum source and seed temperatures (at peak) were determined to be 850 and 825 °C, respectively. The source and seed were heated to their peak temperatures in less than three minutes, and the difference in temperature of the source and seed during heat-up did not exceed 150 °C.

Figure 13 is a photomicrograph of CSVT growth of GaAs on silicon. This sample is typical of growths obtained under optimized conditions.

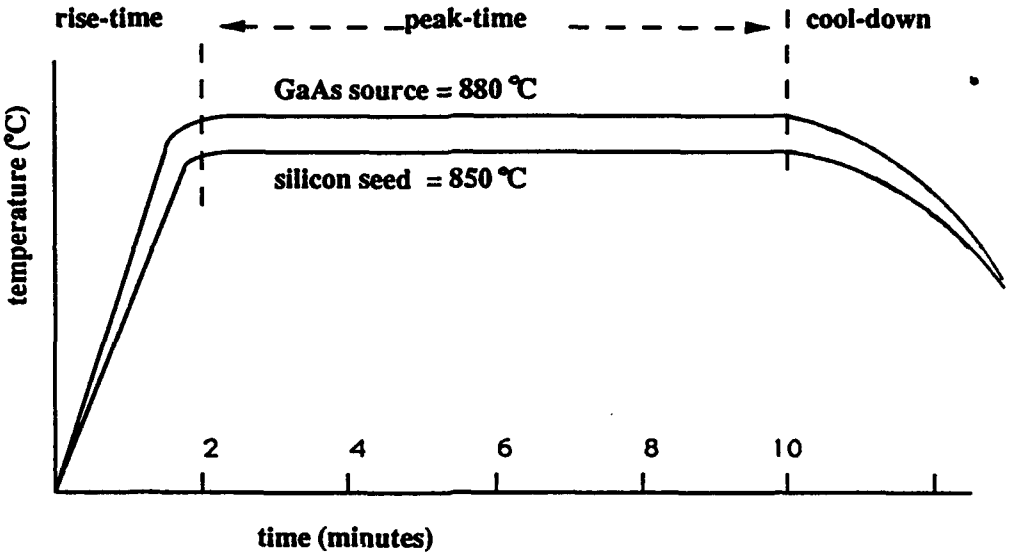


Figure 12. Typical time-temperature program for CSVT.

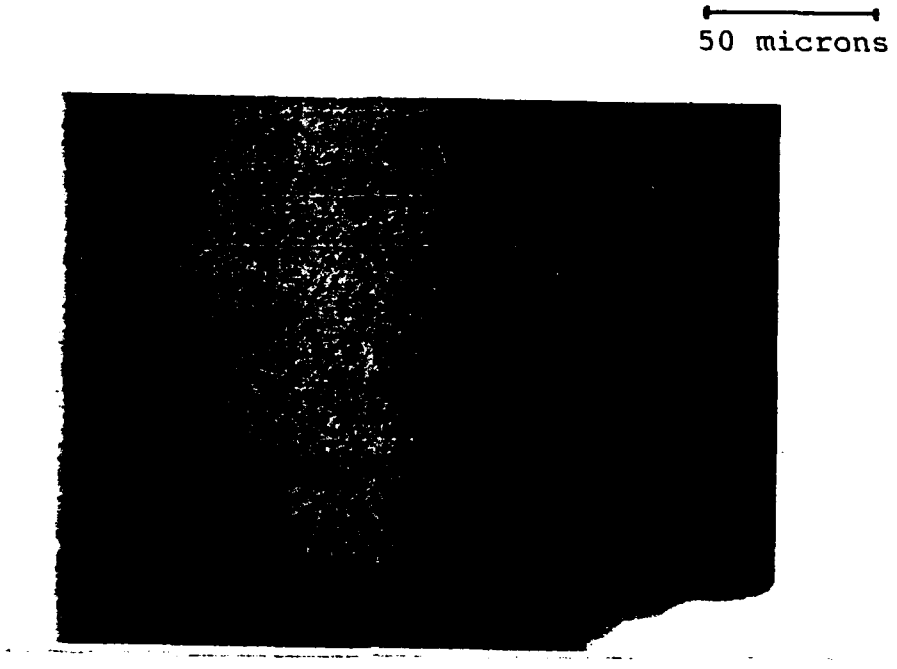


Figure 13. Photomicrograph of GaAs-on-silicon film grown by CSVT.

Figures 14a to **14e** show thicknesses of planar CSVT GaAs films grown on unmasked (111) silicon substrates as a function of (peak) growth time. The film thickness was measured with a Tencor Alfa-step 100 surface profiler. Growth thickness is proportional to peak growth time (as defined in **Figure 12**), and the non-zero growth thickness at a peak time extrapolated to zero is assumed to be growth which occurs during the heat-up and cool-down segments of the time-temperature program. The growth rate is determined as the slope of the thickness versus peak-time curve, and is indicated in each figure. Five cases are shown corresponding to different combinations of source and seed temperatures (source/seed = 825/800, 850/825, 900/875, 925/900, and 950/925 °C). Note that the temperature difference is the same in each case (i.e. 25 °C). The growth rates as a function of silicon substrate temperature are summarized in **Figure 15** and show that the logarithm of growth rate varies inversely with temperature as predicted in **Section 5**.

Figures 16a to 16e show film thicknesses as a function of (peak) growth time for several **ΔTs**, the temperature difference between the source and seed. **Figure 17** shows the growth rate of GaAs as a function of temperature difference between the source and seed. For this series of experiments, the seed temperature was 800 °C and the source temperature was varied to give the desired temperature difference. The growth rate is proportional to **ΔT**, at least for temperature differences up to 100 °C. This data confirms that the growth model developed for CSVT of GaAs-on-GaAs is also valid for GaAs-on-silicon. Growth rates are controlled by the diffusion of gallium oxide and arsenic across the space between the source and seed wafer. Evidently, reaction kinetics and surface diffusion of adatoms have little effect on growth rates. Since the reactants are in equilibrium with the source and substrate, the growth rate is controlled primarily by the source and seed temperature. This situation compares favorably with other vapor-phase growth methods where an interplay of reaction kinetics and fluid dynamics complicates control of film uniformity.

As mentioned previously, water vapor concentration is an important growth parameter. Water vapor concentration also influences the stoichiometry of the GaAs film. **Figure 18** shows the deviations from ideal stoichiometry, as determined by an EDAX analysis, as a function of water vapor concentration. Films which were grown under low water vapor concentrations showed a deficiency of gallium. Since gallium is transported as Ga_2O, the product of the water vapor reaction, this result is not surprising. Another aspect of this study was that above 6000 ppm_v water vapor (dew point 0 °C), a blue oxide was observed on the silicon surface. The optimum water vapor concentration determined on the basis of stoichiometry also corresponded to the best film quality subjectively evaluated on the basis of color and surface morphology. Not coincidentally, CSVT films grown at optimum water vapor concentration were also the most useful in seeding subsequent layers by LPE.

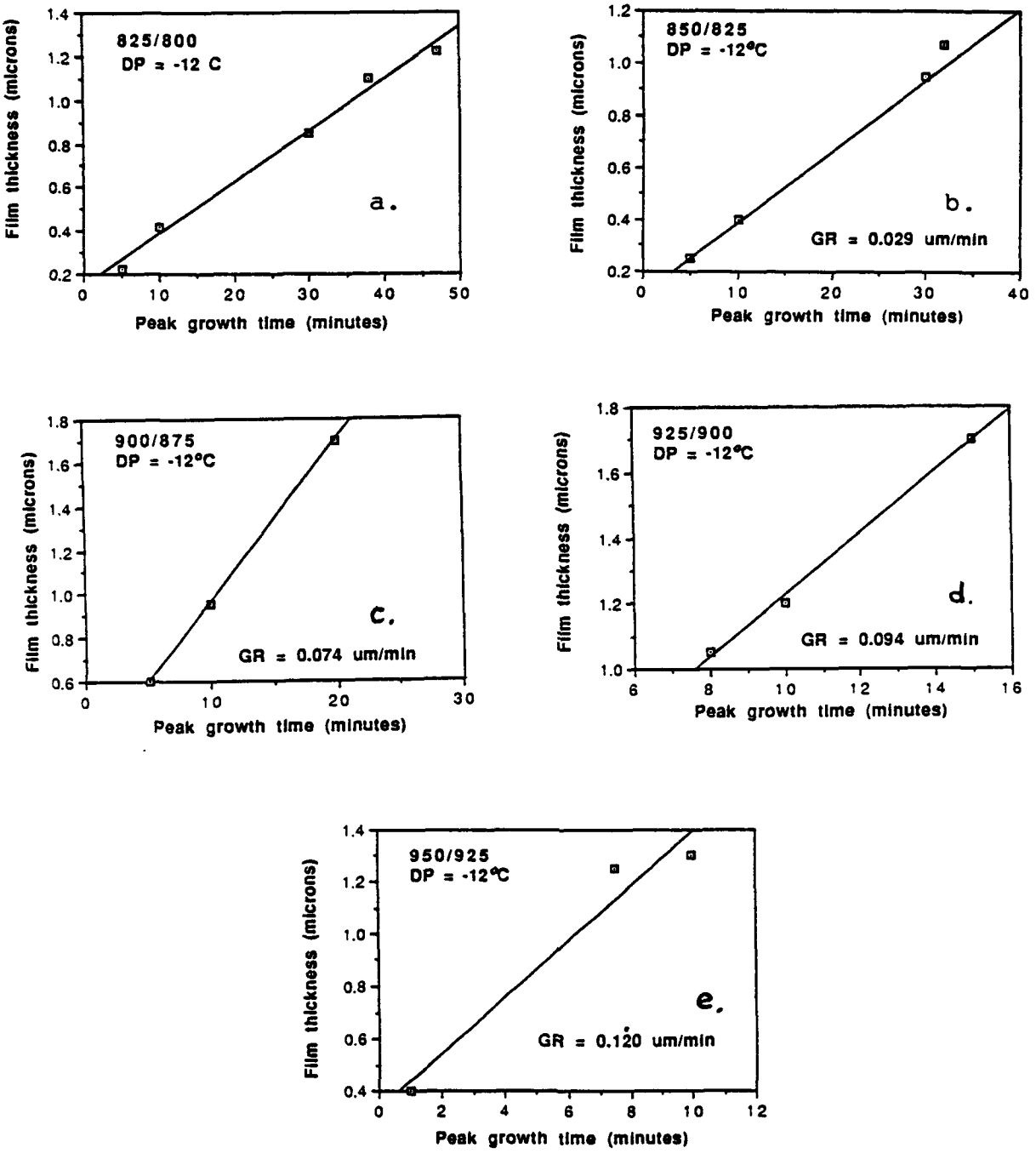


Figure 14. Film thickness as a function of peak growth time for several source/seed temperature combinations: **a.** 825/800, **b.** 850/825, **c.** 900/875, **d.** 925/900, **e.** 950/925 °C.

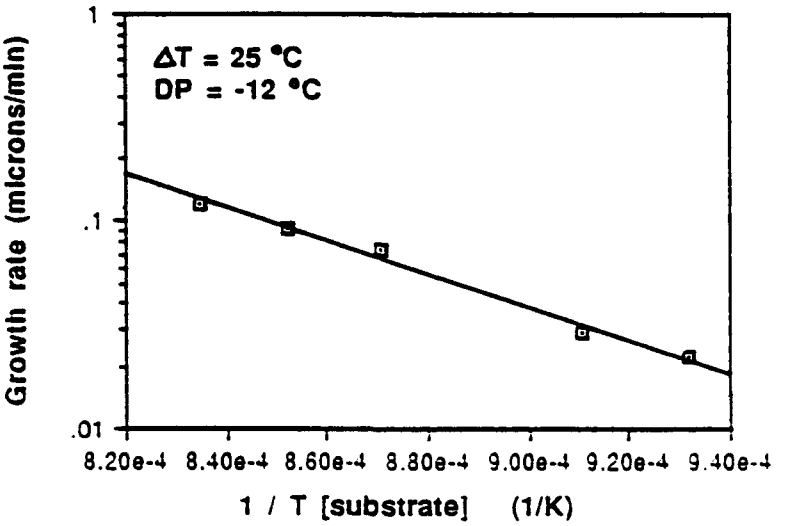


Figure 15. CSVT GaAs-on-silicon growth rate as a function of substrate temperature.

In view of the high temperatures involved and the presence of water vapor, it is somewhat surprising that the silicon substrate does not oxidize. A clean, oxide-free seed surface is a prerequisite for epitaxial growth. The high affinity of silicon for oxygen and water would seem to preclude the success of any CSVT technique which utilized water vapor as a transport agent. **Figure 19** shows the chemical activity of a silicon surface in a oxygen/water vapor environment. Of main interest are the conditions whereupon the silicon substrate surface remains free of silicon dioxide. Passivity does not, however, imply that the silicon does not oxidize. For instance, at low oxygen or water vapor concentrations, the formation of volatile silicon monoxide is favored over solid silicon dioxide. In this case, although the silicon is oxidized the surface remains free of a tenacious oxide film. Furthermore, the formation of silicon monoxide may be limited by slow mass transfer in the vapor phase.

The conditions for surface oxidation (as shown in **Figure 19**) are estimated from a semi-empirical model proposed by Smith and Ghidini [62,63]. Their estimates were determined for high vacuum. The oxidation conditions of **Figure 19** were instead calculated for conditions representative of the CSVT ambient: hydrogen partial pressure of about 0.15 atm and nitrogen partial pressure of 0.85 atm. Details of these calculations are given in **Appendix 1**.

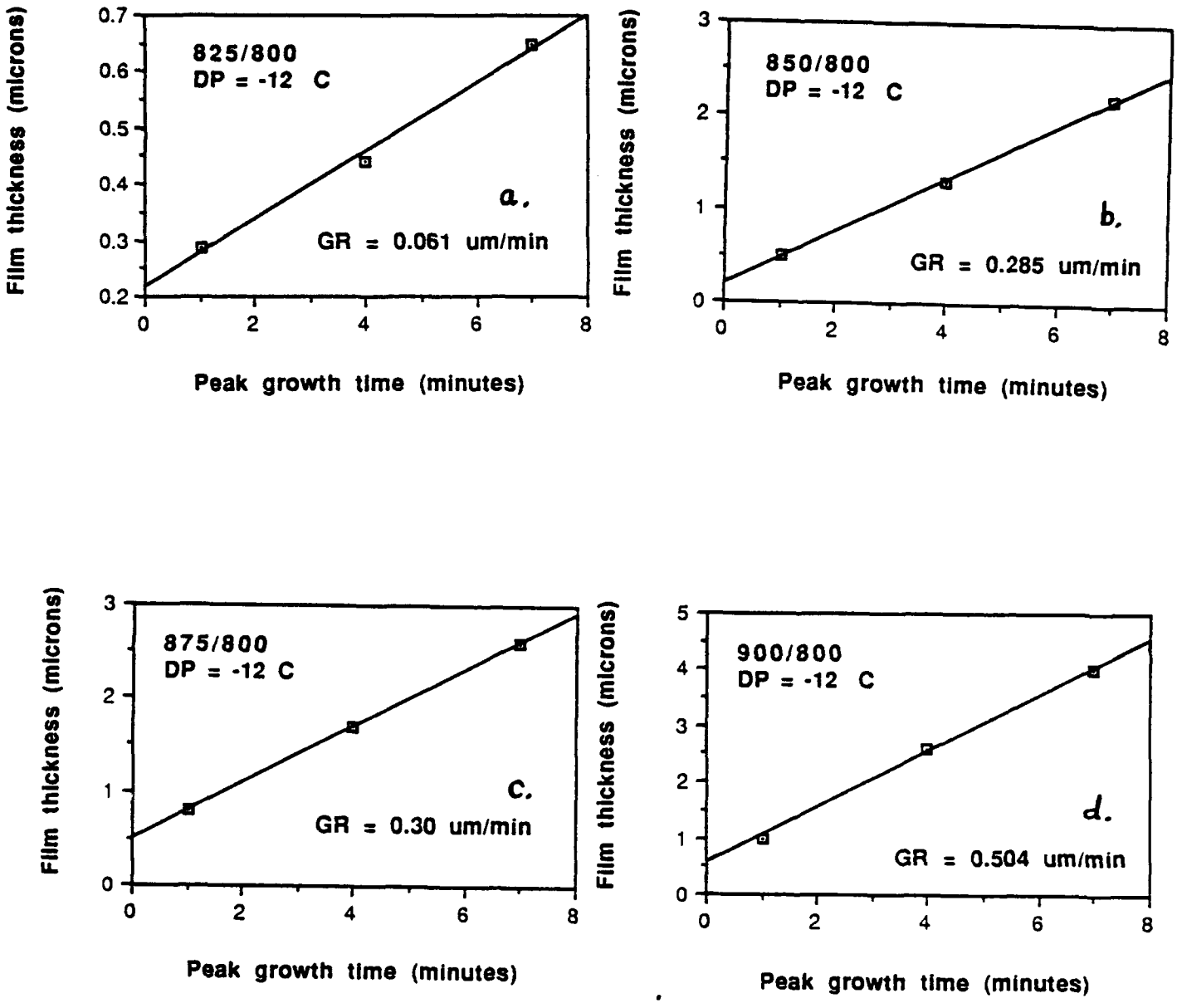


Figure 16. Film thickness as a function of (peak) growth time for several combinations of source/seed temperature: **a.** 825/800, **b.** 850/800, **c.** 875/800, **d.** 900/800 °C.

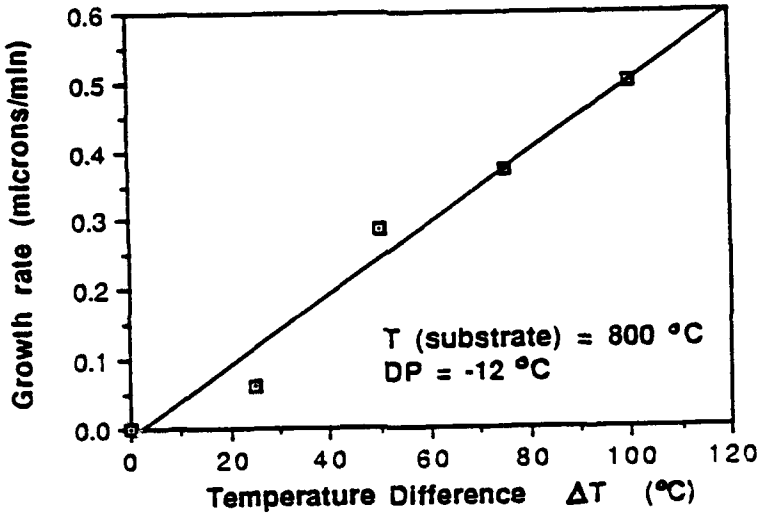


Figure 17. CSVT growth rates as a function of source/seed temperature difference.

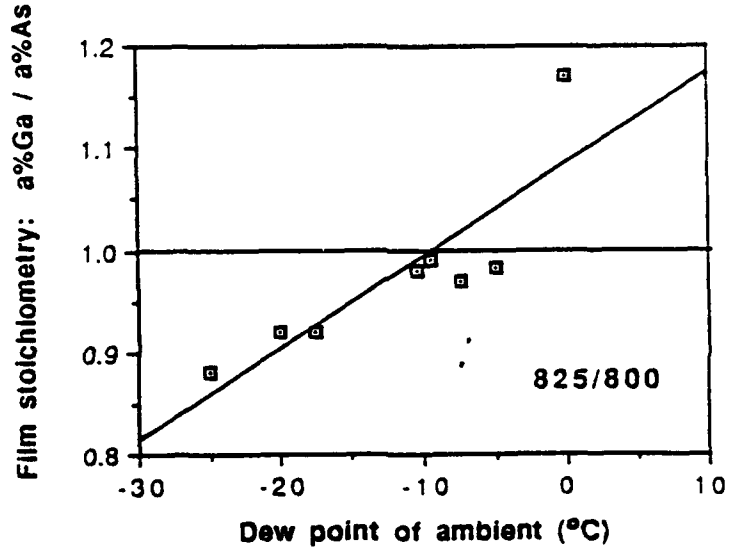


Figure 18. GaAs stoichiometry as a function of water vapor concentration.

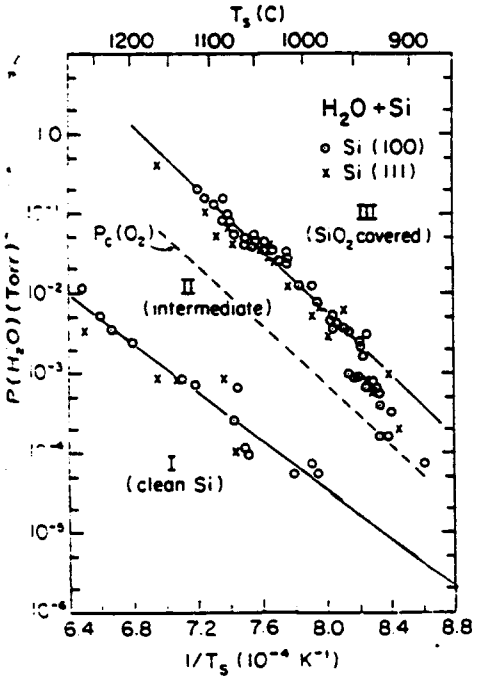


Figure 19. Oxidation of a silicon surface in a water vapor ambient typical of CSVT (from ref. 63).

The conditions required for an oxide-free surface, as suggested by **Figure 19**, are within the range of typical CSVT parameters. Therefore, the formation of silicon monoxide at the expense of silicon dioxide is a plausible explanation of the experimental observation that surface oxides do not inhibit the CSVT process. Nevertheless, considering the uncertainties of the model (**Appendix 1**), a definitive conclusion concerning the oxidation of silicon during CSVT (with a water vapor transport agent) is not warranted. Other modes of oxide removal may also be operating. For instance, the flux of Ga_2O on the surface may reduce surface oxides on the silicon substrate.

5.3 Characterization of CSVT GaAs-on-Silicon.

GaAs-on-silicon films grown by CSVT were characterized structurally, chemically, and electrically. **Figure 20** is an Energy-Dispersive X-ray analysis depth profile of a 3-micron thick GaAs-on-silicon sample. It is evident that the interface region between the silicon substrate and GaAs film is diffuse, and the transition region extends over a distance of about 1 micron. The non-abruptness of the GaAs-silicon junction may be attributed to the diffusion of substrate silicon into the GaAs film, and the diffusion of arsenic and gallium from the film into the silicon substrate. To a large extent, this auto- or cross-doping phenomenon is unavoidable but can be minimized by reducing the time and temperature of the CSVT, LPE, and subsequent processing steps. In this respect, CSVT is advantageous since the total time at high temperature exposure is small relative to other epitaxy techniques. As the film becomes thicker, the concentration of silicon

diminishes. This confirms a diffusion model of cross-doping; the primary source of silicon in the heteroepitaxial film is diffusion from the substrate. Silicon is not incorporated, to any appreciable degree, from the growth ambient. This may be contrasted with MOCVD GaAs on silicon, where side reactions between the precursor reagents and silicon substrate result in silicon incorporation from the vapor phase.

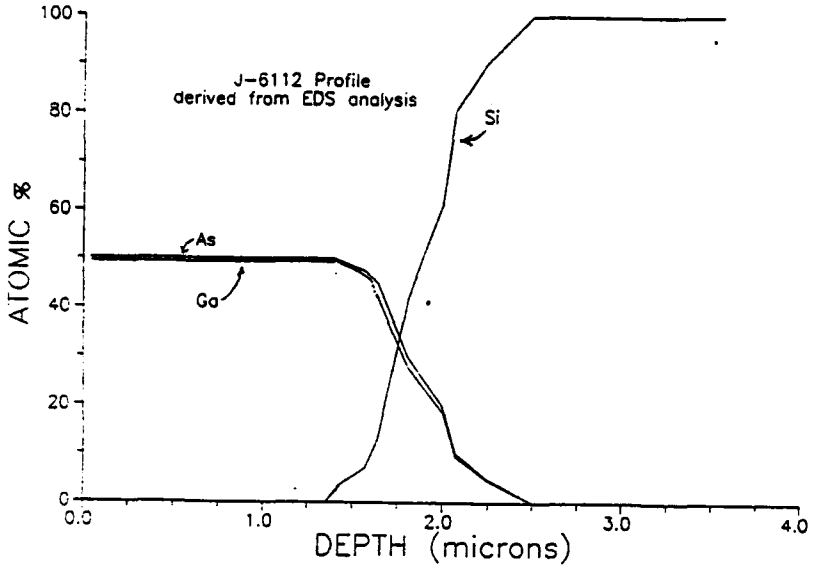


Figure 20. EDAX depth profile of GaAs-on-silicon film.

The incorporation of silicon in GaAs is complicated [25]. Generally, only a fraction of the silicon dissolved in GaAs is electrically-active, i.e. ionized. The remaining silicon is evident as neutral complexes or is precipitated microscopically as a silicon-rich phase dispersed throughout the host material. Silicon is an amphoteric dopant in GaAs. Silicon substituted on a gallium site of the host lattice acts as a donor, while silicon substituted on an arsenic site acts as an acceptor. At high silicon concentrations, the GaAs is closely compensated. The net doping, and therefore the conductivity type (n or p), depends on the growth temperature and the concentration of silicon (or silicon precursors) in the growth ambient. N-type conductivity is favored at high growth temperatures.

The effects of silicon incorporation in GaAs were determined by Hall-effect and resistivity measurements. Net ionized impurity concentration, majority carrier mobility, and bulk resistivity of GaAs-on-silicon films grown by CSVT were measured and are summarized in **Table 3**. The source and seed growth temperatures are also included. All GaAs on silicon films were n-type. These data represent values averaged over the entire film thickness.

Table 3

Electrical Properties of GaAs-on-Silicon Films Grown by CSVT

Sample	(T_2/T_1) (°C/°C)	thickness (microns)	doping (cm^{-3})	resist. (ohm-cm)	mobility ($cm^2/V-s$)
X7539*	875/850	1.15		3.2e-3	
X7541*	875/850	0.65		5.5e-3	
X7568	900/825	0.33	9.5e17	2.4e-2	274
X7602	875/850	0.44	6.5e17	6.0e-2	160
X7603	875/850	0.41	5.5e17	7.5e-2	151
X7606	875/850	0.47	6.6e17	3.2e-2	224
X7607	875/850	0.49	7.5e17	1.5e-2	575
X7752	825/800	0.32	6.4e17	1.1e-2	842
X7755	850/825	0.31	5.4e17	8.4e-3	1360
X7756	900/875	0.76	4.0e17	1.0e-2	1543
X7757	825/800	1.10	4.7e17	6.4e-3	1997
X7760	825/800	0.95	5.4e17	6.0e-3	1902

*Film cracking prevented further characterization.

Over the temperature range studied, there was no apparent dependence of net ionized donor concentration on growth temperature (**Figure 21**). For seed temperatures in the range of 800 to 875 °C, the net donor (or electron) concentration, averaged over the entire film thickness, appears to be consistently in the range of 4 to 10 x 10^{17} cm^{-3}. There is a weak dependence of net ionized donor (or electron) concentration with film thickness (**Figure 22**). Thicker films tend to have a slightly lower average ionized dopant concentration. Finally, the majority carrier (electron) mobility increases with film thickness (**Figure 22**). Film quality undoubtedly improves with distance from the GaAs-silicon interface. The interface region is characterized by charged and uncharged impurities and defects, which scatter free carriers and lower mobility. The top surface region of thick films is of higher quality. Therefore, the averaged mobility for a thick (1.0 micron) film is higher than that for a thin (0.3 to 0.5 microns) film. The electron mobility of almost 2000 $cm^2/V-s$ at a doping concentration of about 5 x 10^{17} cm^{-3} (samples **X7757** and **X7760**) is relatively close to the "literature" [64] value of 3500 $cm^2/V-s$ for high quality GaAs at this doping level. Considering the simplicity of the CSVT technique and that the heteroepitaxial film is grown under conditions of large lattice mismatch and high thermal stress, this result is surprisingly good.

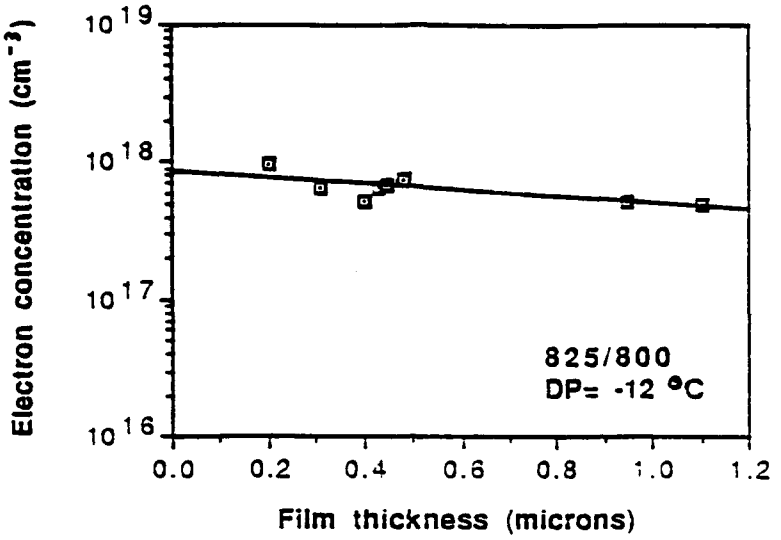


Figure 21. Electron concentration as a function of CSVT growth temperature.

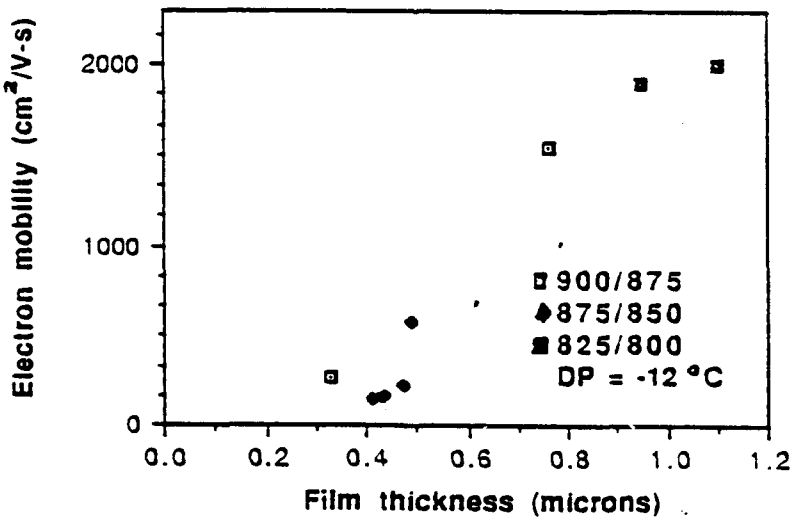


Figure 22. Electron mobility as a function of CSVT film thickness.

In order to separate material quality issues intrinsic to the CSVT process from those related to heteroepitaxy on silicon, it is useful to compare the data of **Table 3** with previously published data for the CSVT growth of GaAs films on GaAs substrates. Using similar process parameters, Mimila-Arroyo et al. [65] reported electron mobilities as high as 3600 $cm^2/V-s$ for samples doped at approximately the same donor concentrations.

5.3.1 Electrical Characterization of GaAs-Silicon Interface.

The GaAs-silicon interface was characterized by forming ohmic contacts to the CSVT GaAs film and the silicon substrate. The contact to the n-type CSVT film was a 200-nm thick Au:Ge alloy annealed at 470 °C. Test structures were isolated as mesas (400 x 400) by masking and etching the GaAs film. Both p- and n-type silicon substrates were used. **Figure 23** shows the i-v curve for CSVT GaAs on a p-type silicon substrate. The substrate resistivity was 1 to 5 ohm-cm. **Figure 24** shows the i-v curve for CSVT GaAs on n-type 0.02 to 0.05 ohm-cm silicon. The GaAs film on the n-type substrate showed an ohmic characteristic while the GaAs film on the p-type substrate was rectifying. This may be explained by assuming that both Ga and As diffuse from the heteroepitaxial film into the silicon substrate. However, the solid solubility of As in silicon is about 100 times higher than the solid solubility of Ga in silicon. Since arsenic is a donor in silicon, an n-type silicon region is formed under the GaAs film. Therefore, the i-v curve of **Figure 23** is really that of a pn silicon homojunction formed by the diffusion of arsenic into p-type silicon. Similarly, the i-v curve of **Figure 24** is that of a isotype n-GaAs/n-silicon heterojunction.

5.4 Selective GaAs-on-Silicon CSVT Heteroepitaxy.

Selective epitaxial growth (SEG) was described in **Section 1**. A recent review of selective vapor-phase growth on patterned substrates is available [66]. Several regimes of vapor-phase growth can be commonly observed. These types of growth are delineated by the seed temperature and the degree of supersaturation in the vapor phase. At very low supersaturations, no deposition is expected. At low temperatures and low supersaturations, a polycrystalline film growth results in the vias. At higher supersaturations, the selective growth occurs with preferential epitaxy on the vias and no deposition on the oxide mask. At still higher supersaturations, the growth is non-selective with polycrystalline deposit over the oxide mask. This optimum "window" of growth parameters has been verified for the CSVT growth of GaAs-on-silicon. These features were verified for GaAs-on-silicon selective heteroepitaxy.

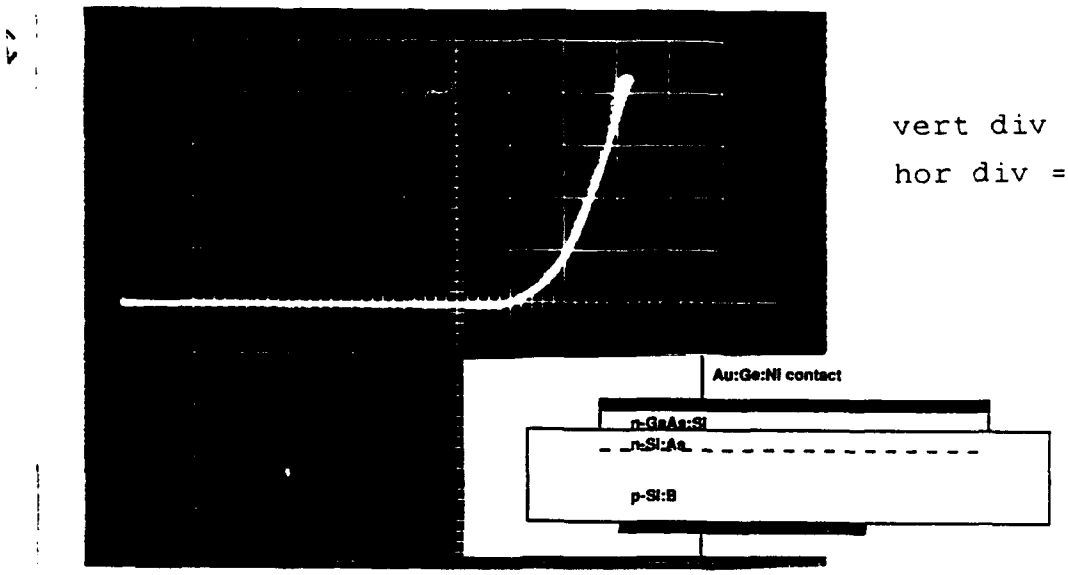


Figure 23. Current-voltage characteristic for heterojunction between (n-type) CSVT GaAs film and p-type silicon substrate.

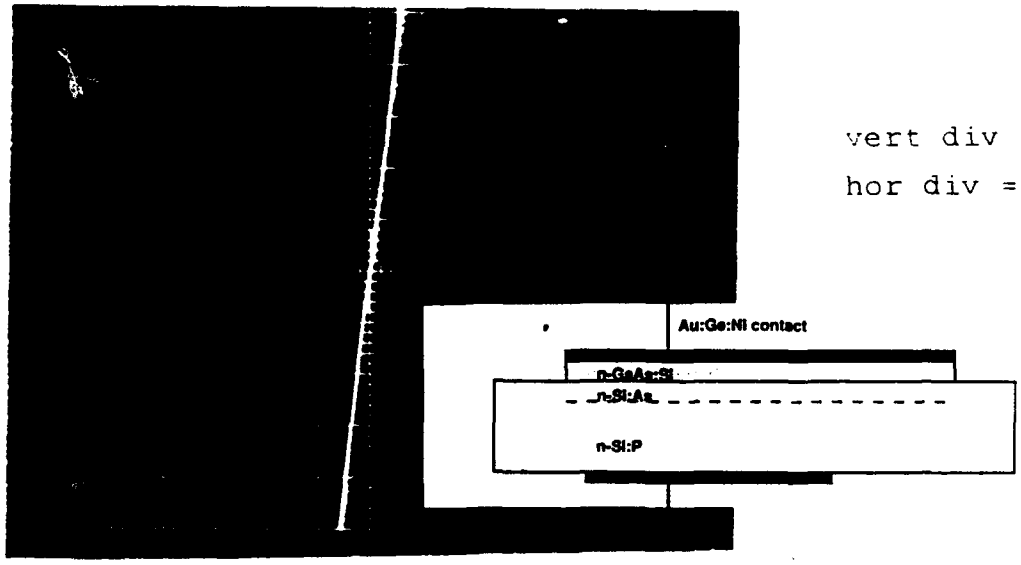


Figure 24. Current-voltage characteristic for heterojunction between (n-type) CSVT GaAs film and n-type silicon substrate.

5.4.1 Experimental Procedure for Selective GaAs-on-Silicon CSVT.

Silicon substrates were masked with an oxide film by thermal oxidation in a dry oxygen ambient at 850 °C for six hours. (Dry oxidations were observed to yield denser, less porous oxide masks than wet oxidations.) The oxide films were about 200 nm thick and exhibited a characteristic blue color. The oxide-masked substrates were patterned by standard photolithographic techniques. Minimum mask feature sizes were approximately 5 microns. The vias were etched in the oxide mask using semiconductor-grade buffered hydrofluoric acid (Olin-Hunt) for 90 seconds. The wafers were then rinsed in a DI water cascade to 18 megohm, blown dry with nitrogen, and loaded into the CSVT system.

Figures 25 and **26** are photomicrographs of GaAs films selectively grown in vias on oxide-masked silicon. **Figure 27** is a scanning electron micrograph of selective GaAs-on-silicon. The optimum parameters for selective growth were the same as those determined for non-selective growth.

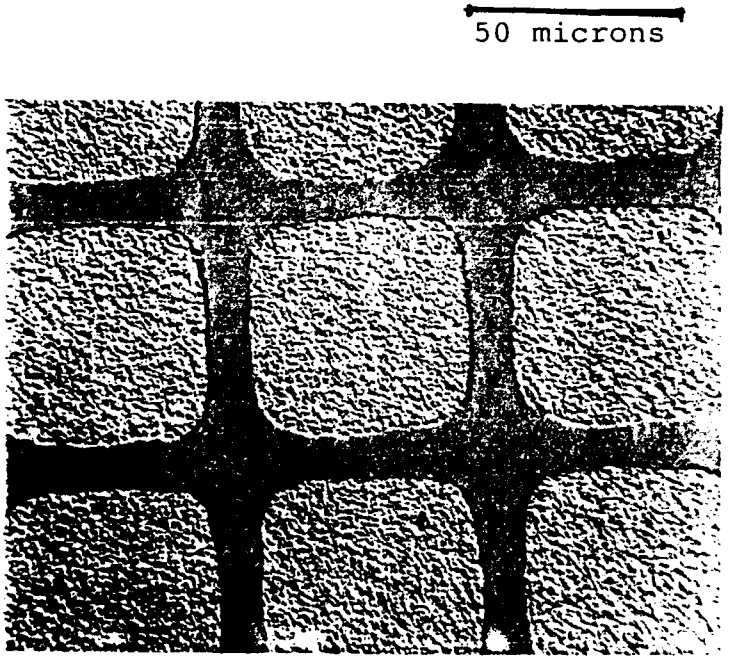


Figure 25. Selective CSVT GaAs-on-Silicon film (I).

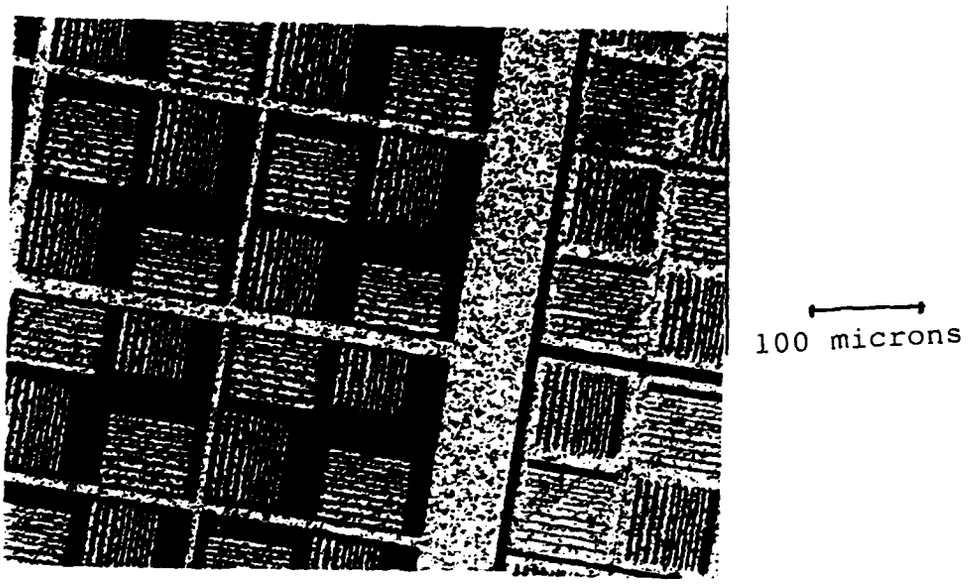


Figure 26. Selective CSVT GaAs-on-silicon film (II).

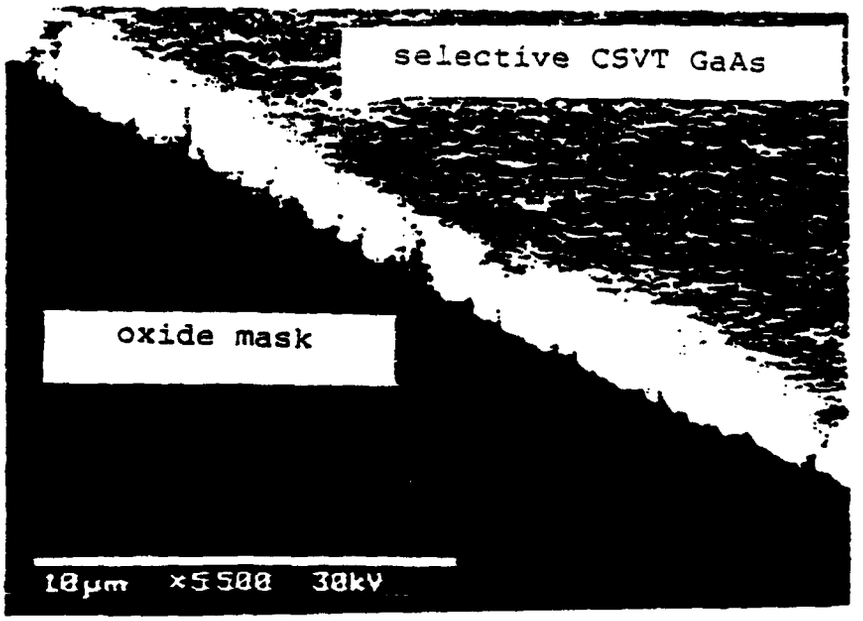


Figure 27. Scanning electron micrograph of selective GaAs-on-silicon film.

5.5 Scale-up of CSVT for 3-inch Diameter Wafers.

Scale-up of the CSVT process for 3-inch diameter wafers was done in the belljar system. Basically, scale-up involved simply fabricating a larger fixture and heating elements to accommodate 3-inch diameter source and seed wafers. A photograph of the belljar system is shown in **Figure 28**. Optimum experimental parameters for 3-inch CSVT were the same as those determined for small area substrates.

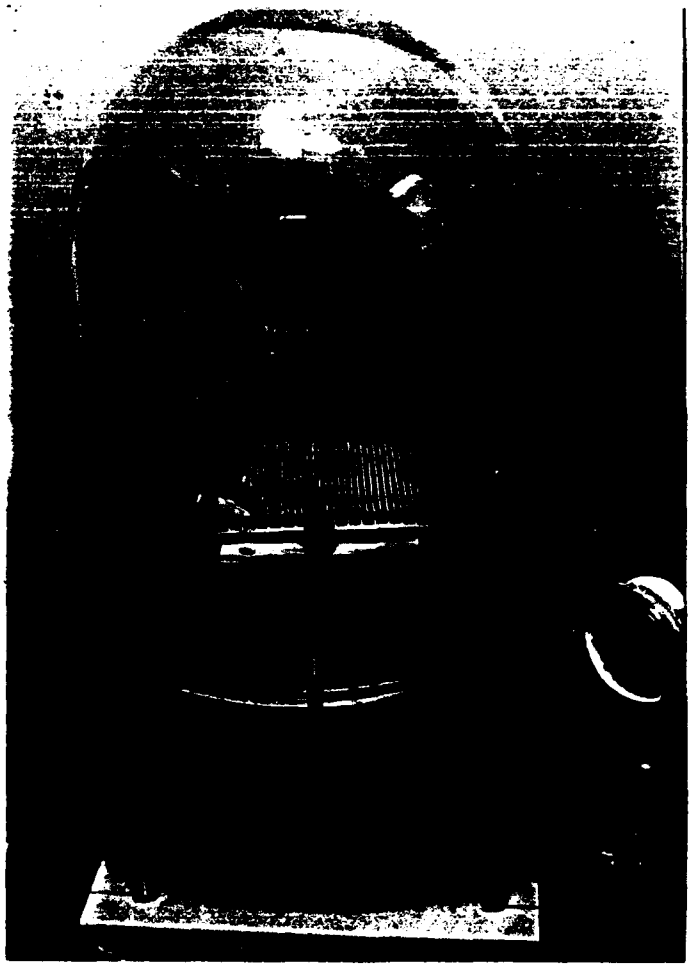


Figure 28. CSVT belljar system for 3-inch substrates.

6.0 LIQUID-PHASE EPITAXY FOR GaAs ON SILICON.

The liquid-phase epitaxial growth of GaAs films on GaAs-on-silicon interlayers formed by CSVT is now described.

6.1 Liquid-Phase Epitaxy System.

The horizontal slideboat technique was used for the liquid-phase epitaxy [25]. A schematic of the graphite slideboat is shown in **Figure 29**. The slideboat was machined from high purity graphite (Poco, Inc., Decatur, TX). The furnace system is shown in **Figure 30**. The liquid-metal solutions, or "melts," are contained in a well and the slidebar brings a source and substrate "seed" in and out of contact with the melt. The GaAs source wafer is used to saturate the melt with GaAs prior to growth.

The slideboat is placed in an 8-foot long 50 x 55 mm fused quartz tube which is situated in a three-zone horizontal electric furnace (Applied Test Systems, Butler, PA). Each zone is separately controlled by a microprocessor-based, programmable PID controller (LFE). A quartz-sheathed type K thermocouple (Omega) is inserted through the base of the slideboat to monitor its temperature. The temperature of the boat can be controlled to within 0.5 °C. The quartz tube is sealed at both ends with stainless steel compression fittings (Key High Vacuum). Smaller compression fittings (Swagelok) are tapped into the flanges of these endcaps to accommodate the thermocouple, pushrod, and inlet and exhaust gas lines.

6.2 Growth of GaAs from Bismuth.

In liquid-phase epitaxy, GaAs films are normally grown from gallium-rich melts. A novel feature of this work is the growth of GaAs from bismuth-rich melts; gallium and arsenic are minor constituents of the melt. Bismuth is used instead of gallium for the following reasons.

1. Silicon is highly soluble in gallium. Therefore, any exposed areas of the silicon substrate, such as at pinholes in the CSVT film or in the masking oxide, or at the edges of the substrate would be severely etched back by a gallium melt. By comparison, silicon is only sparingly soluble in bismuth.

2. Bismuth is less susceptible to oxidation than gallium, and therefore long bake-outs to remove residual oxides or moisture are not necessary.

3. Bismuth is a solid at room temperature (melting point = 271 °C), whereas gallium is a liquid (melting point = 30 °C). Handling of the bismuth melts is easier.

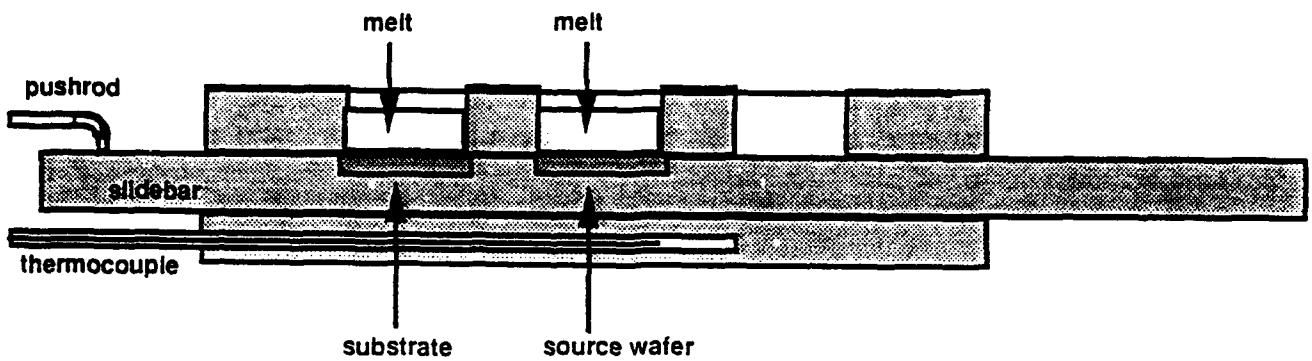


Figure 29. LPE slideboat.

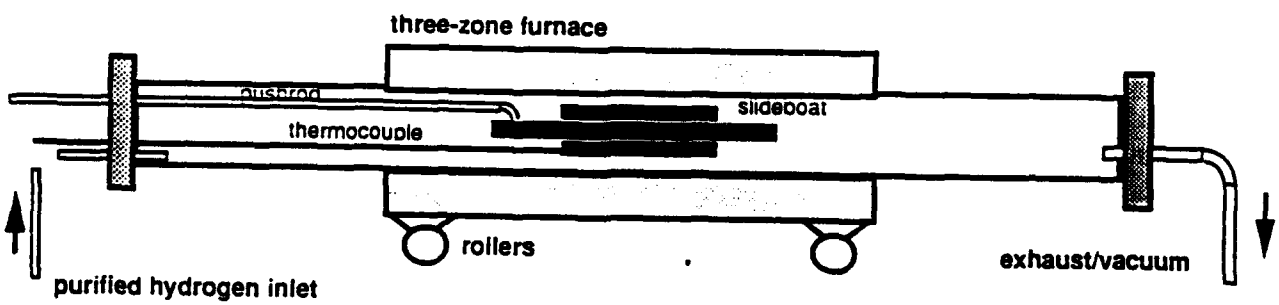


Figure 30. LPE Furnace system.

4. GaAs is less soluble in bismuth than gallium (see **Figure 31**). More specifically, the slope of the liquidus is smaller which provides better control of film thickness, especially for the growth of thin layers.

5. Bismuth has a lower surface tension than gallium. (At the growth temperature, the surface tension of bismuth is approximately 350 dyne/cm and the surface tension of gallium is 600 to 700 dyne/cm). As a consequence, bismuth wets the substrate better than gallium, and this leads to smoother, more uniform films.

The solubility of GaAs in liquid bismuth has been reported by Rubinstein [67], and Leonhardt and Kuhn [68]. Solubility as a function of temperature is shown in **Figure 31**. (Other possible solvents for GaAs are included for comparison.) The solubility curve (the liquidus) can be fit to a "regular" solution model [69]. This is useful for generalizing the solubility data for alloy solvents and for the growth of AlGaAs from bismuth-rich melts. The equation of the liquidus for a binary solid (GaAs) in equilibrium with a liquid-metal solution (Ga-As-Bi) is [25]

$$R\,T \ln \left[\gamma_1(T)\ \gamma_2(T)\ x_1\ x_2 \right] - R\,T_f \ln \left[\gamma_{s1}(T_f)\ \gamma_{s1}(T_f) / 4\right] = \Delta S_o(T_f)\ \left[T_f - T\right]$$

where subscripts **i** refer to Ga (**1**), As (**2**), and Bi (**3**); **R** is the universal gas constant, **T** is the absolute temperature, γ_i is the liquid-phase activity coefficient of component **i**, x_i is the atomic fraction of component **i** in the liquid phase, T_f is the fusion temperature of GaAs, $\Delta S_o(T_f)$ is the heat of fusion of GaAs at the fusion temperature. The superscript **sl** refers to the stoichiometric liquid phase of GaAs ($x_1 = 0.5$; $x_2 = 0.5$). The dependence of the liquidus on bismuth fraction (x_3) is implicit in γ_1 and γ_2. The activity coefficients for the ternary liquid may be estimated as [70]

$$R\,T \ln \gamma_1 = \alpha_{12}\,x_2^2 + \alpha_{13}\,x_3^2 + (\alpha_{12} + \alpha_{13} - \alpha_{23})\,x_2\,x_3$$

$$R\,T \ln \gamma_2 = \alpha_{12}\,x_1^2 + \alpha_{13}\,x_3^2 + (\alpha_{12} + \alpha_{23} - \alpha_{13})\,x_1\,x_3$$

where α_{ij} is an interaction parameter between components **i** and **j** in the liquid phase. The relevant data for these phase equilibria calculations are summarized in **Table 4**.

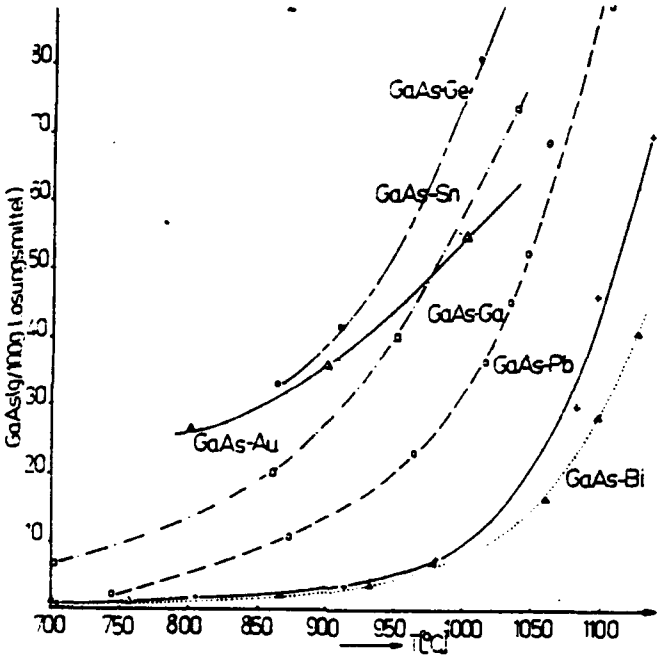


Figure 31. Solubility of GaAs in various liquid metals (from ref. 68).

Table 4

Parameters for Calculating the Solubility of GaAs in Ga-As-Bi Solutions
(after refs. 25, 68, 69, and 71)

T_f = 1511 [K]
ΔS = 16.64 [cal/mole-K]
α_{12} = 5160 - 9.16 T [cal/mole]
α_{13} = 3970 [cal/mole]
α_{23} = 1669 [cal/mole]

For a specified temperature **T**, the equilibrium values of x_1 (Ga), x_2 (As), and x_3 (Bi) can be determined using the above equations. The bismuth-rich melts used in this work are of slightly different composition than those of previous workers [72,76]. In this work, a small amount of gallium was added to the melt to improve wetting and provide an excess of gallium in the liquid-phase. Gallium can improve wetting by reducing native oxides which impede solid-liquid contact. It is also speculated that excess gallium in the melt would suppress the formation of gallium vacancies and arsenic antisite defects. Typical melts consisted of about 7 g of bismuth and 100 to 500 mg of gallium.

Therefore, the initial liquid-phase atomic fractions of bismuth vary from 0.82 to 0.96. The initial atomic fractions of gallium vary from 0.04 to 0.18. Arsenic and additional gallium enter the melt upon saturation with the GaAs source wafer.

6.2.1 Properties of GaAs Grown from Bismuth-Rich Solutions.

Although the growth of GaAs from bismuth-rich solutions has been previously reported, the material was not adequately characterized. Therefore, measurements of electrical properties of GaAs films (doped p- and n-type) grown from bismuth-rich melts were undertaken in order to determine the influence of bismuth on material quality. The effect of bismuth depends on its degree of incorporation in the GaAs film and the electrical activity of bismuth impurities when dissolved in solid GaAs. Bismuth is isoelectronic with arsenic, and it is presumed that bismuth substitutes for arsenic in GaAs and acts as neither a donor nor acceptor. This has been verified for GaAs grown from pure bismuth [72], and in the case of GaP grown from bismuth [73] and for the isoelectronic Group V impurity Sb incorporated in GaAs [74]. Based on measurements of the lattice parameter of GaAs grown from bismuth, Rubinstein [67] concluded there was no significant alloying of bismuth with GaAs. There are no known solid-phase ternary alloys of bismuth and GaAs with a significant fraction of bismuth. The segregation coefficient for bismuth in melt-grown GaAs is also very small ($K = 10^{-5}$ to 5×10^{-3}) [75]. These data indicate the solid solubility of bismuth is very low. This is probably due to the large difference in atomic radii between arsenic and bismuth.

Panek et al. [76] measured electrical and optical properties of GaAs grown from Ga-rich solutions with 2 atomic percent bismuth. Measured carrier concentrations (9×10^{15} to 2.5×10^{16} cm^{-3}) and Hall mobilities (3900 to 5700 $cm^2/V\text{-}s$) did not differ appreciably from GaAs grown from gallium solutions without bismuth. The photoluminescence and absorption spectra were nearly identical for GaAs films grown from gallium solutions with and without bismuth. Yakusheva et al. [72] reported electron mobilities (295 K) as high as 6840 $cm^2/V\text{-}s$ for GaAs grown from pure bismuth at 640 to 700 °C.

To determine the electrical activity of bismuth in GaAs, GaAs films were grown from bismuth-rich melts (7.0 g Bi, 500 mg Ga, saturated with GaAs at 805 °C) at 800 °C by a step cooling technique [25,26] with a 5 °C supercooling. Tin was added to the melts to determine a segregation coefficient for tin doping of the GaAs film. Tin is an n-type impurity in GaAs. The results of these experiments are summarized in **Table 5**. A similar set of experiments was performed to determine the segregation and electrical activity of germanium in GaAs grown form bismuth-rich melts. These data are summarized in **Table 6**.

Table 5
Properties of Sn-Doped GaAs Grown from Bi-rich Melts

Sample	Sn (mg)	resistivity (ohm-cm)	doping (cm^{-3})	mobility ($cm^2/V-s$)
J-7502	none	1.90e-2	8.0e16	4216
J-7505	5.0	1.08e-2	1.8e17	3092
J-7506	50	6.30e-3	7.9e17	3400
J-7404	520	5.58e-4	5.0e18	1469

Notes: Melt composition: 7.0 g Bi; 500 mg Ga; saturated with GaAs at 805 °C, **Growth temperature:** 800 °C; **Step-cooling:** 5 °C.

Table 6
Properties of Ge-Doped GaAs Grown from Bi-rich Melts

Sample	Ga (mg)	Ge (mg)	type	doping (cm^{-3})	mobility ($cm^2/V-s$)
J-8119	0.0	1.0	N	8.5e17	1900
J-8120	0.0	10.0	N	2.5e18	635
J-8315	0.0	50.0	N	2.6e18	487
J-8121	0.0	100.0	N	1.5e18	419
J-8316	0.0	500.0	N	2.0e18	37
			(with gallium)		
J-8122	200	1.0	N	1.0e17	1652
J-8317	200	5.0	N	2.6e18	1221
J-8201	200	10.0	(nearly compensated)		
J-8318	200	50.0	P	8.0e17	66
J-8202	200	100.	P	1.1e18	108
J-8319	200	500.	P	3.8e18	77

Notes: Melt composition: 7.0g Bi, with or without Ga as listed, saturated with GaAs at 805 °C; **Growth temperature:** 800 °C; **step-cooling:** 5 °C.

All tin-doped films were n-type. The n-type conductivity observed when no tin was added to the melt (sample J-7502) is probably due to residual impurities in the liquid-phase epitaxy system (silicon is a likely candidate). For each doping, the mobilities are within 25% of the nominal values quoted for GaAs [64]. The data indicate that bismuth is not an electrically-active impurity in GaAs. This observation is consistent with the hypothesis that bismuth substitutes for arsenic on the GaAs lattice and that since bismuth is isoelectronic with arsenic, it acts as neither a donor nor acceptor. Donor concentration as a function of tin atomic fraction in the melt is shown in **Figure 32**. The slope of this line is the segregation coefficient for tin at 800 °C.

With no gallium in the melt, Ge-doped samples were n-type over the entire concentration range. With 200 mg of gallium in the melt, GaAs was n-type for low germanium concentrations in the melt, and p-type for high germanium concentrations in the melt. This situation is similar to that observed with silicon doping of GaAs grown from Ga-rich melts, and is consistent with the potential amphoteric doping behavior of Group IV impurities in III-V compounds. It is noted when GaAs is grown from Ga-rich melts (with no bismuth) at 800 °C, Ge always behaves as an acceptor (i.e. substitutes on an As site). The observation that a small amount of gallium in a bismuth-rich melt changes Ge from a donor to an acceptor could be explained in several ways. Ga may be gettering impurites which act as donors and otherwise compensate Ge acceptors. Ga may also influence the the concentration of Ga vacancies, which in turn determines for which site (Ga or As) the Ge atom substitutes. This phenomenom warrants further study. At any rate, the impurity segregation studies show that both p and n-type GaAs can be grown from bismuth-rich melts.

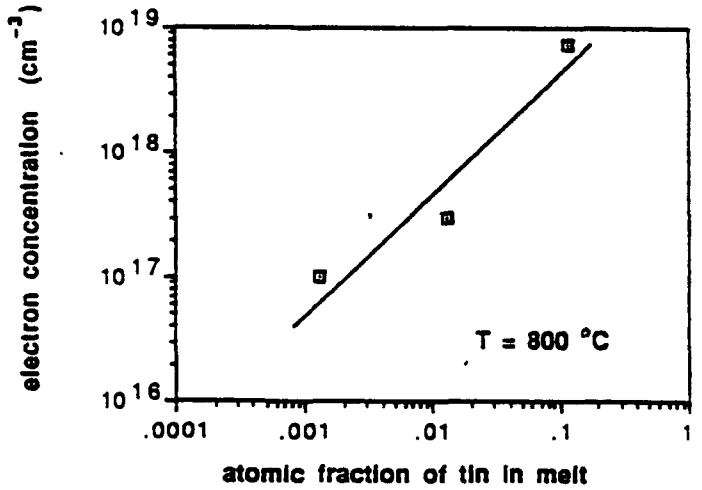


Figure 32. Segregation of Sn in GaAs grown from Bi-rich melts at 800 °C.

The optical properties (absorption and luminescence spectra) of III-V compound semiconductors can be significantly altered by isoelectronic impurities. For example, bismuth in GaP forms a deep trap which changes the luminescence spectra [77]. Similar behavior might be expected when bismuth is incorporated in GaAs. To investigate any differences in luminescence efficiency between GaAs grown from bismuth and GaAs grown from gallium, light-emitting diodes were grown, processed, and tested. LEDs grown from bismuth-rich melts had nearly identical performance (current-voltage characteristics and light emission efficiency) to similar LED structures (pn homojunctions) grown from gallium-rich melts. It was concluded that for LED applications, bismuth is an acceptable alternative to gallium as a metallic solvent for LPE.

6.3 Liquid-Phase Epitaxy of GaAs on GaAs(CSVT)-on-Silicon.

Planar (non-selective) and selectively-grown CSVT GaAs-on-silicon films were used to seed the liquid-phase epitaxy of GaAs and AlGaAs layers. CSVT film thicknesses in the range of 0.4 to 1.5 microns functioned best as interlayers.

It can be assumed that there is some degree of residual strain in the CSVT GaAs-on-silicon films. This effective lattice mismatch will impede the nucleation of the epitaxial film grown from the liquid-phase. To increase the thermodynamic driving force for nucleation, a step-cooling mode of growth [25,26] is used which results in a high degree of initial super-saturation. In the step-cooling technique, the melt is saturated with GaAs (using a GaAs source wafer) at a specified equilibration temperature T. The source wafer is then separated from the melt and the melt is supercooled by some degree ΔT. Epitaxial growth occurs when the seed wafer is contacted with the melt. The thickness of the film is proportional to ΔT and the square root of the contact time.

The free energy change ΔG [Joules/mole GaAs] for a supercooled solution is given approximately by

$$\begin{aligned} \Delta G &= R\,T \ln [1 + \Delta x / x_e] \\ &\approx R\,T\,\Delta x / x_e; \qquad \Delta x \ll x_e \\ &\approx R\,T\,m\,\Delta T / x_e \end{aligned}$$

where R is the universal gas constant [Joules/mole GaAs], T is the equilibrium temperature [K], x_e is the equilibrium concentration of arsenic in the liquid metal solvent, Δx is the degree of supersaturation, m is the slope (dx_e/dT) of the liquidus (arsenic solubility curve) at the growth temperature. ΔG is the change in free energy of a solution when it is supercooled. ΔG may be interpreted as a rough estimate of the driving force for nucleation as a function of growth temperature T and supercooling ΔT.

6.3.1 Liquid-Phase Epitaxy Experimental Procedure.

The GaAs-on-silicon wafers were cleaned in organics (TCE, acetone, methanol), rinsed in DI water, etched for 1 minute in a solution of H_2SO_4 (conc) : H_2O_2 (30%) : H_2O (2:16:1000). The etch rate for this solution is about 100 nm/min. Next, the wafers were rinsed in a DI water cascade until a water resistivity of 18 megohms was achieved. Finally, the seed wafer was blown dry with nitrogen and loaded into the LPE boat.

Melts were composed of 7.0 g of bismuth and 50 to 200 mg of gallium. For n-type doping, tin was added to the melt. The melt was equilibrated with an undoped GaAs source wafer at a specified temperature for at least 60 minutes, insuring saturation with arsenic. After equilibration, the source wafer was separated from the melt and the melt was step-cooled for a specified **ΔT**. The substrate was then contacted with the supercooled melt. Because of the large supercooling, relatively short contact times ranging from 20 seconds to 3 minutes yielded layer thicknesses in the range of 0.3 to 3 microns. For the growth of AlGaAs (AlAs fraction = 20%), 2 mg of aluminum was added to the melts.

6.3.2 Optimization of LPE Parameters for GaAs-on-Silicon.

The optimization of LPE parameters (specifically growth temperature **T** and degree of step-cooling **ΔT**) was investigated. This constituted the largest part of the Phase II experimental work. A narrow "window" of growth parameters which yielded acceptable results was observed. General trends may be summarized as follows. Low growth temperatures result in inadequate nucleation and poor film morphology. Similarly, low supercoolings, even at high temperatures, produced discrete nucleation. While increasing the supercooling improved nucleation, excessively high supercooling resulted in poor film morphology and defects such as solvent inclusion and cellular-type growth. This was partly due to growth instabilities associated with high super-saturation conditions. In addition, film thickness is difficult to control with high supercoolings. Higher growth temperatures improve both nucleation and film morphology. However, the associated increased thermal stress results in film fracture and peeling. These observations are consistent with the theoretical understanding of liquid-phase epitaxy in a system with both lattice and thermal expansion mismatch. Basically, the experimental work consisted of determining the growth temperature, supercooling, and growth time which yield an acceptable compromise between these effects. Examples of LPE-grown GaAs films on CSVT GaAs-on-silicon for several growth conditions are shown in the photomicrographs of **Figures 33 a** to **f**). The temperature **T**, supercooling **ΔT**, and film thickness **h** are shown with each photomicrograph. The growth area is restricted to a 200 x 200 micron openings in an oxide-masked silicon substrate. In all cases a 1-micron thick CSVT GaAs film was selectively grown to seed the growth of the LPE GaAs layer.

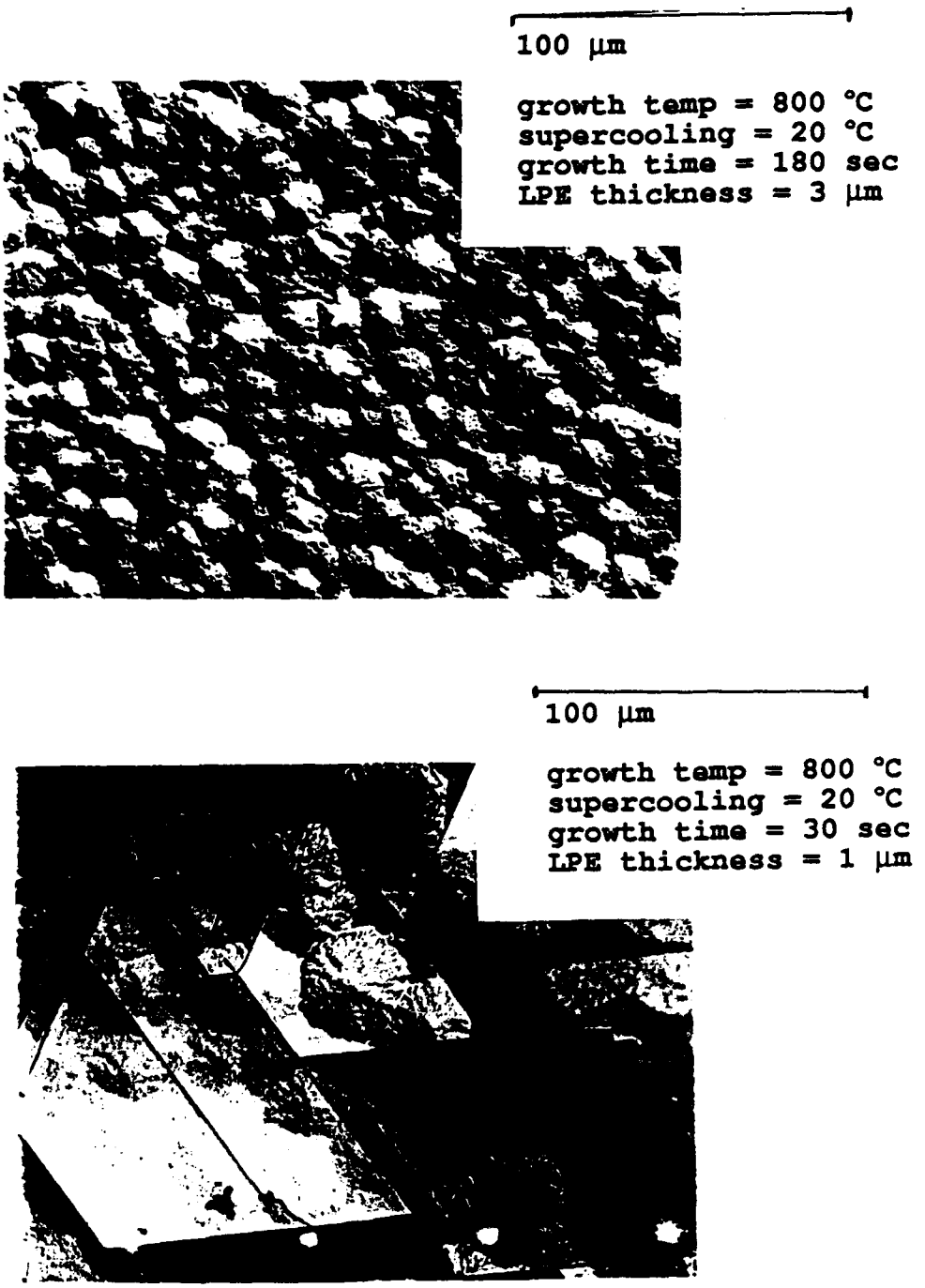
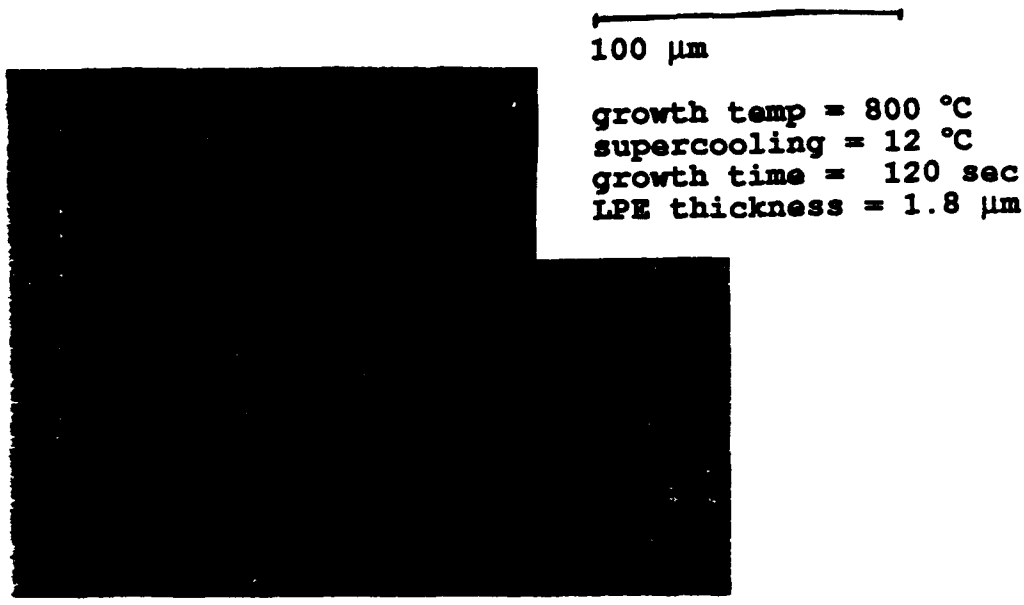


Figure 33a and **b**. Photomicrographs of LPE Growth of GaAs on CSVT GaAs-on-silicon.



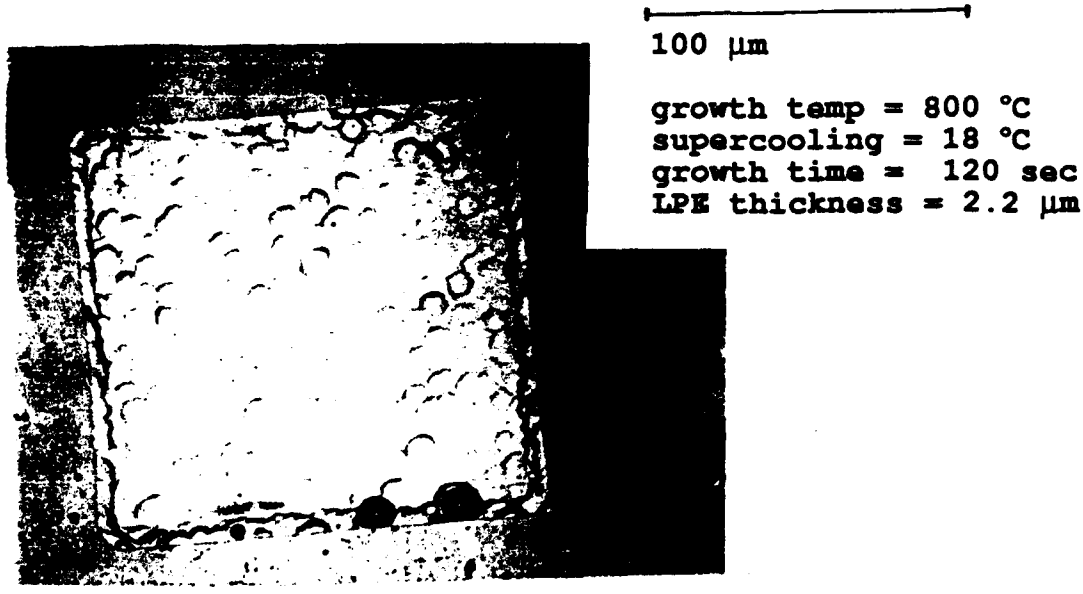
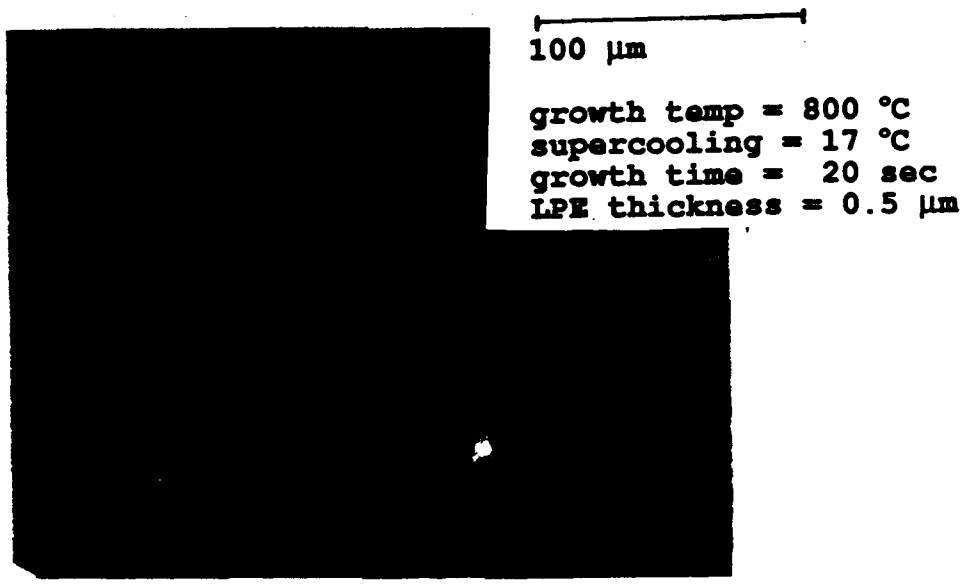


Figure 33 (cont.) **c** and **d.**



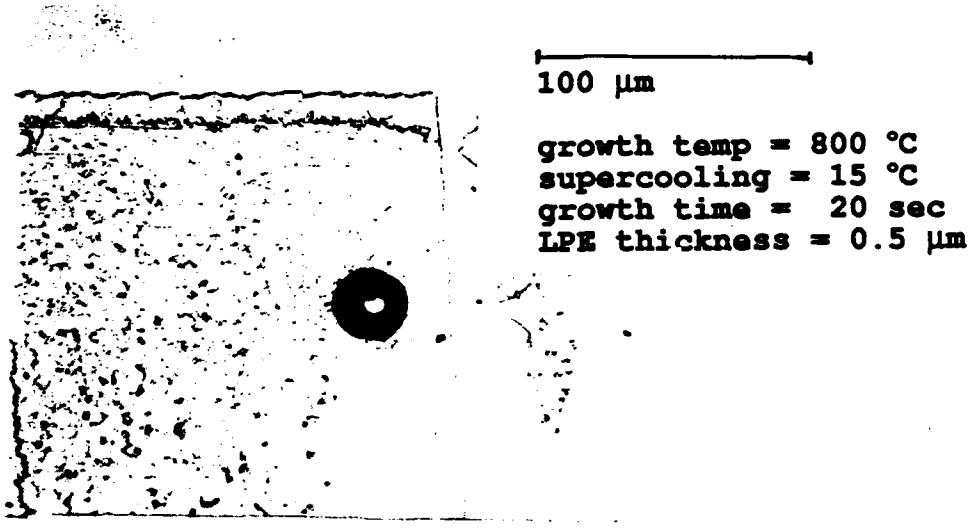


Figure 33 (cont.) **e** and **f**.

The best growths were achieved with growth temperatures of 825 °C and with a stepcooling between 15 and 18 °C. Selective liquid-phase epitaxial growth on selectively-grown CSVT GaAs-on-silicon was also studied. The optimum growth parameters were the same. As mentioned, selective growth was useful for reducing the effects of thermal stress. **Figures 34** and **35** are selectively-grown GaAs layers on selectively-grown CSVT GaAs on silicon. In **Figure 34** the mesa size is 100 x 100 micron, while in **Figure 35** the mesa size is 25 x 25 micron. The smooth, crack-free morphology of the smaller mesas, despite a total film thickness exceeding 4 microns, is noteworthy. **Figure 36** shows epitaxial lateral overgrowth, using a 10 micron wide via on a 250 micron spacing. Although some areas of the sample showed smooth, continuous overgrowth, in general, impingement of adjacent vias is difficult to achieve consistently over the entire sample area. Since it has been experimentally determined that the primary cause of defects and poor surface morphology is thermal stress, the possible advantages of ELO are not clear. It is reasonable to expect that a large-area film overgrown on an oxide will be subjected to the same thermal stress as non-selectively grown films. In total, over 300 LPE runs were performed to optimize the growth.

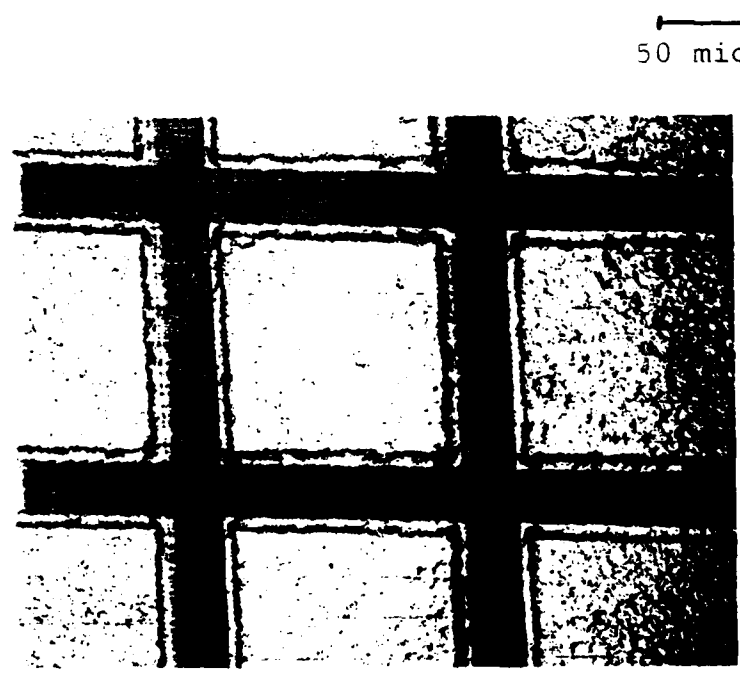


Figure 34. Selectively-grown LPE GaAs on selectively-grown CSVT GaAs-on-silicon mesas (mesa size = 100 x 100 microns).

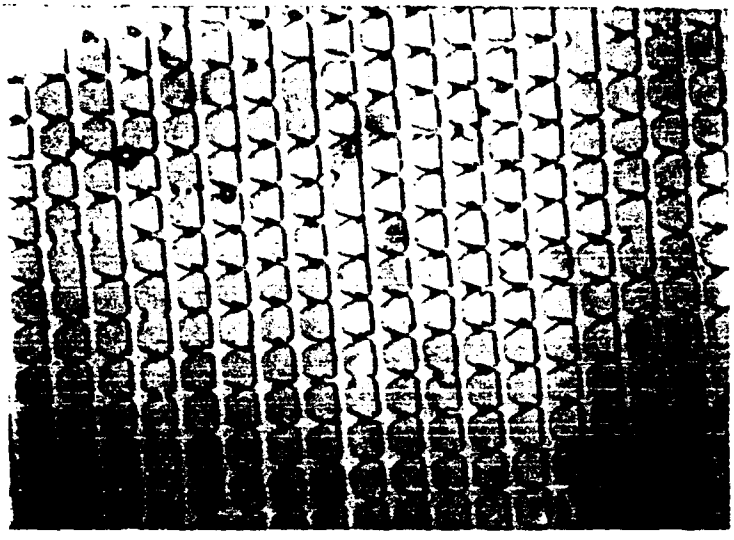


Figure 35. Selectively-grown LPE GaAs on selectively-grown CSVT GaAs-on-silicon mesas (mesa size = 25 x 25 micron).

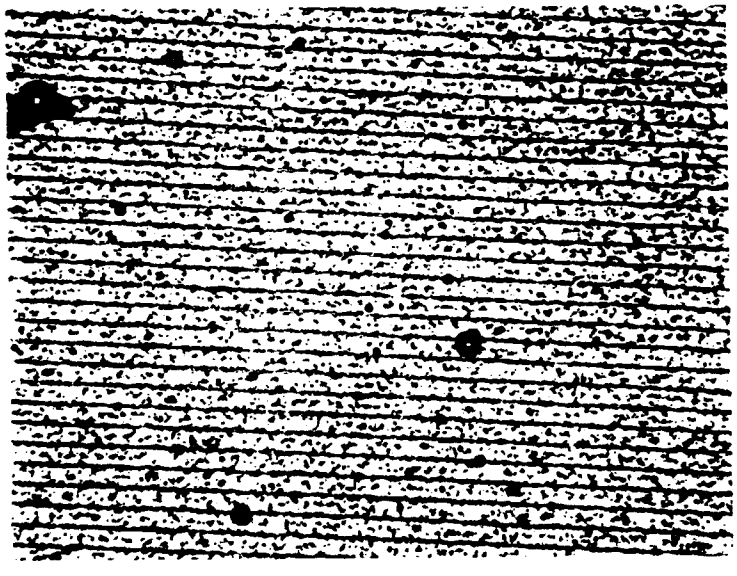


Figure 36. (Near-impinging) liquid-phase epitaxial lateral overgrowth on selectively-grown CSVT GaAs-on-silicon.

6.4 Scale-up of Liquid-Phase Epitaxy.

A scaled-up LPE system was designed and constructed for three-inch diameter wafers. The slideboat was custom made by Poco Graphite, Inc. (Decatur, Texas) using their DFP3-grade graphite and is shown in **Figure 37**. This graphite has a density of 1.88 grams/cm^3 and an average pore size of 0.4 microns. The slideboat was purified after machining by high temperature annealing under vacuum. The slideboat has been designed for the growth of two layers, using either a step-cooling or ramp-cooling technique, or some combination of these techniques.

The furnace system is shown in **Figure 38** and **39**. A three-zone 100-cm long horizontal transparent "gold" tube furnace (TransTemp Co., Chelsea, MA) was employed. The center zone has a length of 50 cm and the two end zones are 25 cm in length. The transparent furnace is made with two coaxial glass tubes. The outer tube has a 50 nm thick gold coating which is highly reflective for infrared radiation but partially transparent for visible light. This reflector provides the thermal insulation of the furnace. On the outside of the inner tube, a rigid coil resistance heating element is wound for each zone. This type of furnace is characterized by its low thermal mass and fast response time. The visibility of the slideboat while centered in the furnace is convenient for alignment and positioning. A University of Illinois group has reported unique advantages of this type of furnace for liquid-phase epitaxy [78]. They observed a flat temperature profile (± 0.1 °C) over the length of the slideboat and no temperature overshoot. In contrast to conventional furnaces, the multiple internal reflections effected by the gold reflector provide uniform heating both radially and longitudinally.

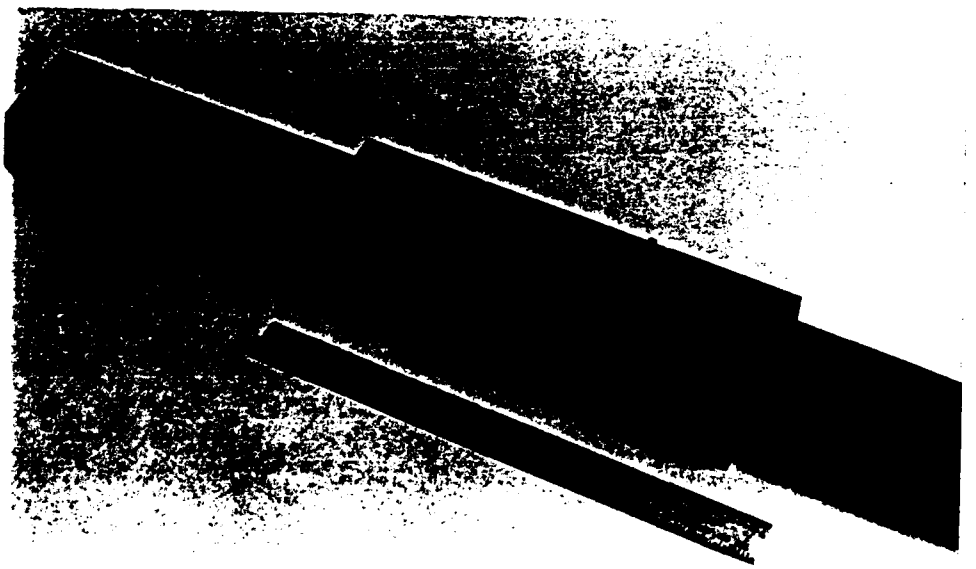


Figure 37. LPE slideboat for 3-inch diameter wafers.

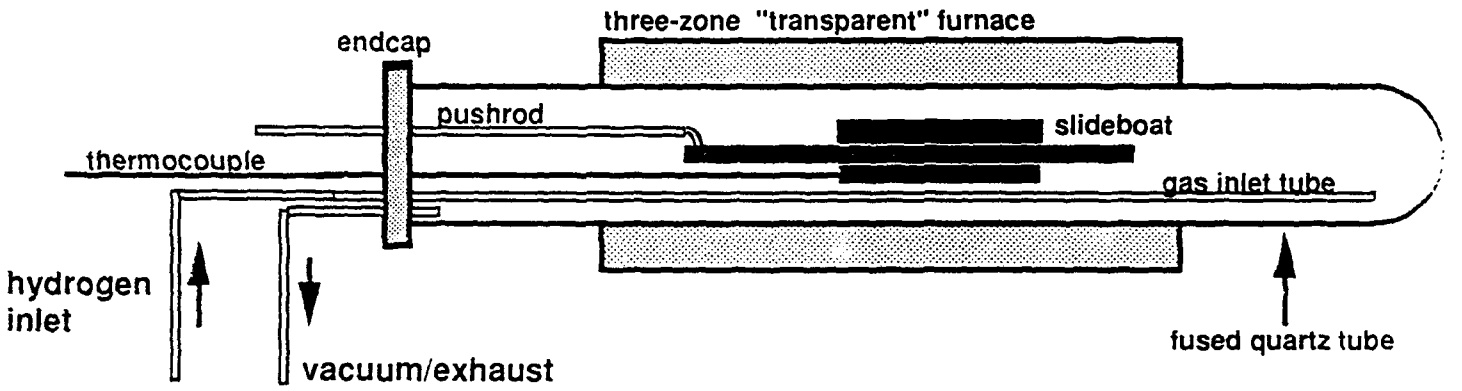


Figure 38. Schematic of furnace system for LPE on 3-inch diameter wafers.

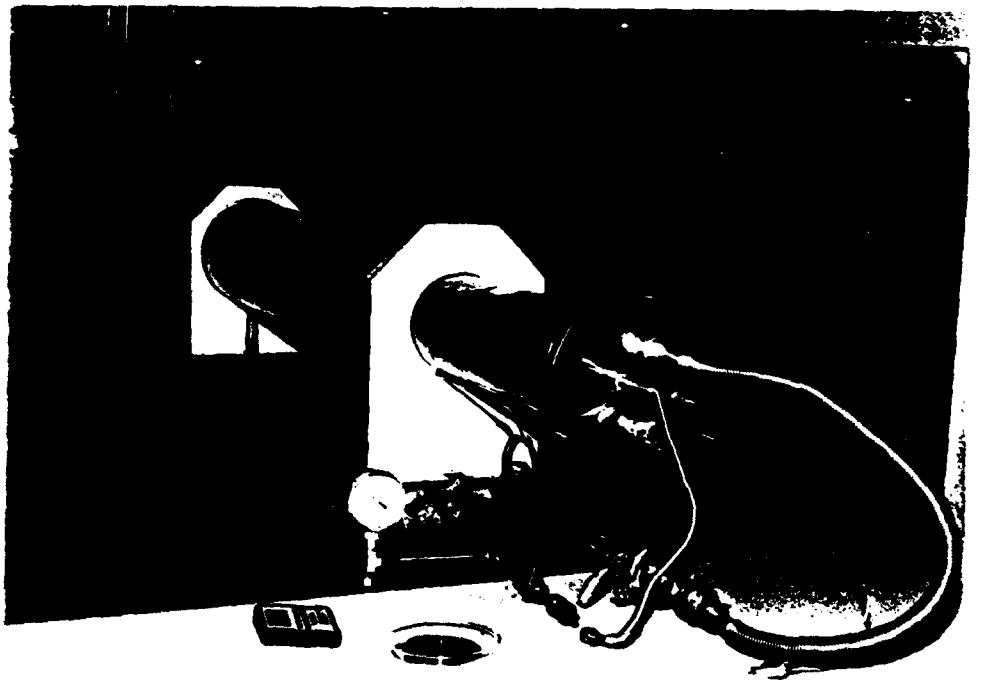


Figure 39. Furnace system for LPE on 3-inch diameter wafers.

The slideboat is positioned in a 115 x 120 mm, 1.65 meters long fused-quartz tube (General Electric) with one end sealed and the other fused with a 160 mm quartz flange. A stainless steel endcap closes the flanged end of the tube. The endcap is clamped to the flange and a vacuum-tight seal is achieved with an intervening O-ring. Stainless steel compression fittings (Swagelok) are machined into the endcap to accommodate the pushrod, thermocouples, inlet and exhaust gas lines.

Each furnace zone is powered by a 220V/20A single-phase SCR circuit (Model 1025, Control Concepts Inc., Eden Prairie, MN). The SCRs are regulated with microprocessor-based PID controllers (Chino, Inc., Tokyo). The two end-zone controllers (Chino Model DB) are slaved to the center master controller (Chino Model KP). The setpoint of the master controller follows the "ramp and soak" time-temperature schedule programmed by the user. The setpoints of the program are transmitted to the end controllers. The control of each zone is based on a differential signal between the setpoint and a voltage signal from a thermocouple in each zone. The gas handling system, vacuum purge, and other support is similar to that of the small-scale LPE system described in **section 6.1**.

7.0 CSVT/LPE GaAs-ON-SILICON OPTOELECTRONIC DEVICES.

Light-emitting diodes were fabricated as mesa structures which were selectively grown by CSVT/LPE on patterned, oxide-masked silicon substrates. A silicon wafer was masked with a 200 nm thick thermally-grown oxide. A 100-micron wide stripe opening was defined by photolithography and etched with buffered hydrofluoric acid. A 1.5-micron thick film of n-GaAs:Si was grown in the stripe via by CSVT. Next, the CSVT was masked with a 200-nm thick silica film deposited by e-beam evaporation. A 100 x 100 micron via, coincident with the stripe, was defined in this second oxide mask. In this via, a 1.2-micron thick p-AlGaAs:Ge (AlAs fraction = 0.2) layer was selectively grown. The CSVT GaAs film functioned as the luminescent base layer of the LED, while the LPE AlGaAs layer was the emitter. The LED structure is shown in **Figure 40**. A Au:Ge contact dot was formed for ohmic contact to the p-AlGaAs emitter, and a Au:Zn contact stripe was deposited for ohmic contact to the n-GaAs base. Stable light emission was observed from these devices. The current-voltage characteristic is shown in **Figure 41**. These results demonstrate the viability of the CSVT/LPE technique for the fabrication of AlGaAs/GaAs optoelectronic devices on silicon substrates.

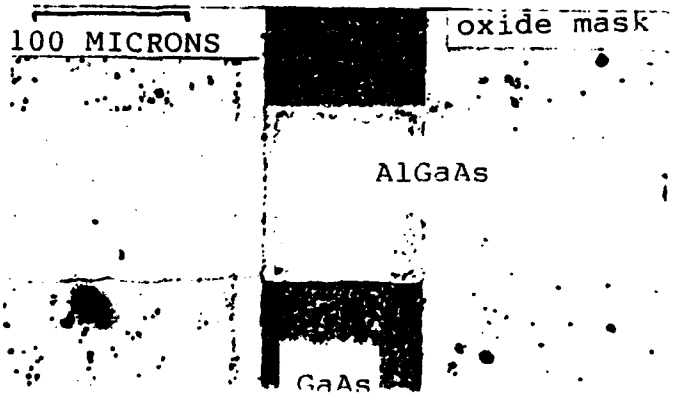
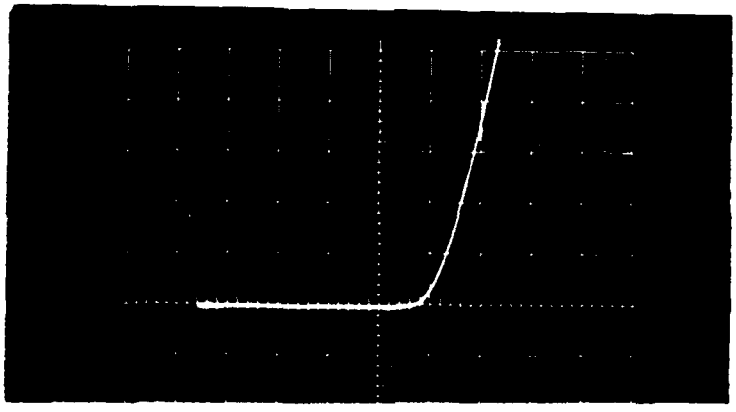


Figure 40. AlGaAs/GaAs LED structure grown by CSVT/LPE.



scales: horizontal 1 V/div
vertical 2 mA/div

Figure 41. Current-voltage characteristic of AlGaAs/GaAs LED on silicon substrate.

8.0 DISCUSSION AND SUMMARY.

Thermal stress effects remain the dominant problem in this heteroepitaxy technology. The relatively high growth temperatures utilized in this method, compared to competing heteroepitaxy technologies, is problematic. Further optimization of the CSVT/LPE technique may lead to lower growth temperatures. A general consensus is forming that thermal stress effects are the major problem of heteroepitaxy. In recent years, selective modes of growth are being employed to circumvent thermal stress effects. The present work supports this view, and selective-grown films by CSVT/LPE exhibited reduced stress and excellent morphology compared to non-selectively grown films. Selectively-grown mesas, with mesa sizes of 25 x 25 micron, showed remarkably smooth surfaces, despite thicknesses exceeding 4 microns. It is a recommendation of this work that future device applications of this heteroepitaxy technology should exploit this type of selectively-grown structure.

The CSVT/LPE technique for GaAs-on-silicon heteroepitaxy is a viable alternative to other heteroepitaxy techniques such as MOCVD and MBE. CSVT/LPE is attractive due to its simplicity, low cost, and safe operation. Reproducible GaAs-on-silicon films were routinely achieved. The CSVT process was optimized for the growth of smooth, uniform layers. For majority carrier devices such as FETs, the CSVT GaAs-on-silicon film appears very promising. For optoelectronic and other minority carrier devices, additional layers grown by LPE are necessary.

Both the CSVT and LPE process are scaleable for 3-inch diameter wafers. Uniform GaAs-on-silicon films were grown on 3-inch diameter silicon wafers using a belljar system. Development of LPE for 3-inch diameter wafers is continuing.

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APPENDIX 1: Oxidation of Silicon During CSVT

As described in **Section 5.2**, it is absolutely crucial that the silicon substrate remain free of surface oxides during CSVT growth. The conditions necessary to avoid the formation of a silica film are now considered.

The oxidation of silicon is determined for conditions which are representative of the CSVT ambient, using forming gas (85% N2, 15% H2) as the carrier and water vapor as the transport agent for the CSVT reaction. These may be stated as:

Temperature: 700 to 1000 °C
Total system pressure: approx. 1 atm
Hydrogen pressure: 0.15 atm
Nitrogen pressure: 0.85 atm
Water vapor concentration: 2000 ppm_v

For a silicon wafer in the above ambient, the predominant chemical species are silicon (solid), silicon dioxide (solid), silicon monoxide (vapor), hydrogen, oxygen, and water vapor. Nitrogen is also present but is not a reactant or product of any of the chemical reactions. Possible chemical reactions involving these species are:

$$Si + O_2 \rightleftharpoons SiO_2 \qquad \text{(A-1)}$$

$$Si + SiO_2 \rightleftharpoons 2\ SiO \qquad \text{(A-2)}$$

$$H_2 + (1/2)\ O_2 \rightleftharpoons H_2O \qquad \text{(A-3)}$$

$$Si + H_2O \rightleftharpoons SiO + H_2 \qquad \text{(A-4)}$$

$$2\ Si + O_2 \rightleftharpoons 2\ SiO \qquad \text{(A-5)}$$

$$SiO + (1/2)\ O_2 \rightleftharpoons SiO_2 \qquad \text{(A-6)}$$

$$Si + 2\ H_2O \rightleftharpoons SiO_2 + 2\ H_2 \qquad \text{(A-7)}$$

$$SiO + H_2O \rightleftharpoons SiO_2 + H_2 \qquad \text{(A-8)}$$

Only three of these reactions are independent. The equilibrium concentrations may be determined by applying the law of mass action to the first three equations (**A-1**, **A-2**, and **A-3**)

$$a_{SiO2} / a_{Si}\ P_{O2} = \exp(-\Delta G_1/RT) \qquad \text{(A-9)}$$

$$P^2_{SiO} / a_{Si}\ a_{SiO} = \exp(-\Delta G_2/RT) \qquad \text{(A-10)}$$

$$P_{H2O} / P_{H2}\ P^{1/2}_{O2} = \exp(-\Delta G_3/RT) \qquad \text{(A-11)}$$

where ΔG_1, ΔG_2, and ΔG_3 are the Gibbs Free Energies [Joules/mole] of reactions **A-1**, **A-2**, and **A-3**. These are given by [79]

$$\Delta G_1 = 40{,}540 + 3.08\ T \log T - 29.71\ T \qquad \textbf{(A-12)}$$

$$\Delta G_2 = 51{,}530 - 9.92\ T \qquad \textbf{(A-13)}$$

$$\Delta G_3 = 13{,}683 - 1.07 \log T - 0.53\ T \qquad \textbf{(A-14)}$$

The activities of the volatile species are shown as partial pressures and the activities of the solid species may be taken as using equations **A-9** to **A-14**, the partial pressures of volatile species in equilibrium with silicon can be determined. These are listed in **Table A1**.

Table A1

Partial Pressures of Volatile Species in Equilibrium with Silicon (partial pressures in atmospheres)

	Temperature (°C)			
species	**800**	**900**	**1000**	**1100**
H_2	1.0	1.0	1.0	1.0
H_2O:	6e-9	3e-8	2e-7	7e-7
O_2:	1e-35	1e-31	1e-28	1e-25
SiO:	1e-8	3e-7	4e-6	4e-5

The equilibrium data indicate that the partial pressures of water vapor and oxygen must be exceedingly low to prevent oxidation of the silicon surface.

Wagner [80] has suggested that the conditions needed for an oxide-free surface are not as stringent as the above equilibrium analysis would indicate. The oxidation of the silicon surface is instead determined by the diffusion of volatile silicon monoxide through a surface boundary layer. According to this model, a silicon surface will remain free of oxides provided the oxygen partial pressure does not exceed a maximum given by

$$P_{O2}\ (\max) = (1/2)\ (D_{SiO} / D_{O2})^{1/2}\ P_{SiO}(eq) \qquad \textbf{(A-15)}$$

$$= 0.4\ P_{SiO}(eq)$$

where D_{SiO} and D_{O2} are the diffusivities of silicon monoxide and oxygen through the boundary layer and p_{SiO} (eq) is the equilibrium partial pressure of silicon monoxide determined from **Table A1**.

A kinetic model of silicon oxidation has also been developed [63,64,81,82]. The model is based on determining various rate-limiting steps in the oxidation of silicon. Molecular oxygen dissociates into atomic species when adsorbed on the silicon surface.

$$(1/2)\ O_2 \text{ ------> } O\ (ads) \qquad \textbf{(A-16)}$$

which occurs irreversibly. Oxygen can be removed from the surface by evaporation of silicon monoxide which does not form associated molecules.

$$Si + O\ (ads) \text{ -----> } SiO\ (g) \qquad \textbf{(A-17)}$$

Alternatively, the adsorbed oxygen atoms can react to form silica.

$$Si + 2\ O\ (ads) \text{ ----> } SiO_2 \qquad \textbf{(A-18)}$$

Reaction **A-17** is favored at low oxygen concentrations and high temperatures, and reaction **A-18** is favored at high oxygen concentrations and low temperatures. Using this model, Smith and Ghidini [63] determined the conditions under which a silicon surface will remain free of surface oxides. The model was extended to determine the critical water vapor concentrations required to maintain a clean silicon surface at various elevated temperatures [64]. The results of this model, as applied to conditions typical of CSVT, are shown in **Figure 19**.

APPENDIX 2: Key Personnel

Michael G. Mauk was the Principal Investigator from January 1989 to the completion of the program. Dr. Mauk received Bachelor of Chemical Engineering and Bachelor of Electrical Engineering degrees from the University of Delaware in 1981. He received his Doctorate in Applied Sciences, Electrical Engineering from the University of Delaware in 1986. His dissertation concerned the design and analysis of thin-film crystalline silicon solar cells with optical enhancement and their fabrication by solution growth. From 1987 to 1988, Dr. Mauk was a visiting researcher at the Interuniversity Microelectronics Center (IMEC) in Leuven, Belgium. At IMEC, Dr. Mauk's research included AlGaAs/GaAs solar cells and AlGaAs/GaAs heterojunction bipolar transistors fabricated by molecular beam epitaxy, chemical surface passivation of GaAs, and heavy-doping effects in GaAs and silicon. From 1989 to the present, Dr. Mauk has been the principal investigator for research programs on monolithic optical interconnects, GaAs-on-silicon heteroepitaxy, high-speed LEDs, and liquid-phase electroepitaxy of silicon and III-V compound semiconductors.

James B. McNeely was the Project Manager (August 1988 to November 1990) and Principal Investigator from August 1988 to December 1988. Mr. McNeely has run major GaAs and GaAsP manufacturing facilities for several companies. Mr. McNeely has an M.S. in Chemical Engineering from the Massachusetts Institute of Technology and an M.A. in Solid State Chemistry from Washington University. Mr. McNeely has been responsible for major research and development efforts in III-V compound semiconductor bulk crystal growth and epitaxy for Monsanto, Litronix, and M/A-COM Laser Diode Laboratories. He was partially responsible for Monsanto's position as the world's leading supplier of III-V compounds in the 1960s. Since joining AstroPower, Mr. McNeely has been involved with the epitaxy of GaAs, GaAsP, and GaP on a variety of substrates.

Brown F Williams is Vice President and Director of the High-Performance Products Division of AstroPower, within which the Phase II program was conducted. Dr. Williams has a Ph.D. in Physics from the University of California, Riverside. Dr. Williams has more than twenty-five years of technical and business experience in applied research and product development. Dr. Williams was Vice President, Solid State at the RCA David Sarnoff Laboratories, where he was responsible for the management and growth of diverse technical programs with revenues over $35 million. At RCA, Dr. Williams was also Staff Vice President for Display, Solid-State Power, Picture Tube, and Energy Systems (1980-84); Director for Optoelectronic, Solid-State Power, Energy Systems Laboratories (1977-79); Director for Energy Systems Research Laboratories (1975-77); Head, Quantum Electronics Research (1973-75); and held several research and management positions within the RCA Industrial Tube Division (1966-73).

Allen M. Barnett is the President of AstroPower, Inc. and is a Professor of Electrical Engineering at the University of Delaware. Dr. Barnett has a Ph.D in Electrical Engineering from the Carnegie Institute of Technology. He has successfully led three different organizations (a start-up company, a major industrial research laboratory, and a university applied research institute) into positions of technical leadership. Dr. Barnett is an experienced inventor and is the recipient of four IR-100 awards for the development of industrial products. Dr. Barnett holds thirteen patents and has authored or co-authored 115 technical publications. As a Professor of Electrical Engineering, Dr. Barnett has established undergraduate and graduate level semiconductor device design and fabrication programs for both silicon and III-V compound materials. Dr. Barnett's current research interests include heteroepitaxial growth of silicon and compound semiconductors and silicon-on-ceramic film technology for application to optoelectronics and photovoltaic devices.

Jeffrey E. Cotter is a device development engineer. Mr. Cotter has Master and Bachelor degrees in Electrical Engineering from the University of Delaware. Mr. Cotter's research activities include systems studies of optical and electrical interconnects, and electronic packaging engineering. Mr. Cotter was responsible for materials characterization of epitaxial films and processing and measurements of devices fabricated in GaAs-on-silicon material. In addition, Mr. Cotter was involved in the development of the CSVT process.

James P. Curran is an epitaxy and device processing technician. Mr. Curran operated the liquid-phase epitaxy system for the Phase II program, and was involved in equipment and process development. Mr. Curran has over five years of laboratory experience in liquid-phase epitaxy. Prior to joining AstroPower, Mr. Curran was employed for 18 years as a technician at the Franklin Mint, Franklin Center, Pa. Mr. Curran is presently pursuing an associates degree in Electronics Technology from Delaware Technical and Community College.

Bryan W. Feyock is an epitaxy and processing technician. Mr. Feyock has a B.S. in Physics from the University of Delaware. At AstroPower, Mr. Feyock has been involved in silicon film solar cell development and chemical vapor deposition of GaAs on silicon. For the Phase II program, Mr. Feyock performed a large part of the CSVT experimental work including equipment and process development of the large-scale (3-inch diameter substrate) CSVT system.

Margaret S. Hannon is an epitaxy engineer. Ms. Hannon has a B.S. in Ceramic Engineering from Rutgers University. She has over two years experience in the research and development of compound semiconductors including GaAs, AlGaAs, InP, and InGaAsP. Ms. Hannon conducted experiments for the liquid-phase epitaxy of GaAs and AlGaAs films on GaAs-on-silicon structures prepared by CSVT.

Paul E. Sims is an epitaxy engineer. Mr. Sims attended Arizona State University and has a Bachelor of Mechanical Engineering degree from the University of Delaware. At AstroPower, Mr. Sims is developing epitaxy technology for AlGaAs LEDs. For the Phase II program, Mr. Sims was involved in engineering for scale-up of CSVT and LPE.

Nancy E. Terranova was the project engineer from August 1988 to December 1988. Ms. Terranova has a bachelors degree in Electrical Engineering from the University of Delaware. Her research activities have included development of homojunction and heterojunction III-V compound solar cells, and GaAs-on-silicon heteroepitaxy. Ms. Terranova was instrumental in the initial conceptualization of this program's technology, i.e. the combined CSVT/LPE technique.