BURIED SILICIDE INTERCONNECTIONS WITH BONDED WAFERS

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February 1991

Final Report for Period May 1990 - February 1991

Contract DASG60-90-C-0037

Approved for Public Release; Distribution Unlimited

U.S. Army Strategic Defense Command
P.O. Box 1500
Huntsville, AL 35807-3801

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

REPORT SECURITY CLASSIFICATION: unclassified	1b RESTRICTIVE MARKINGS
SECURITY CLASSIFICATION AUTHORITY	3 DISTRIBUTION/AVAILABILITY OF REPORT: Approved for public release, distribution unlimited
DECLASSIFICATION/DOWNGRADING SCHEDULE	
PERFORMING ORGANIZATION REPORT NUMBER(S)	5 MONITORING ORGANIZATION REPORT NUMBER(S)
NAME OF PERFORMING ORGANIZATION: Implant Sciences Corporation; 6b OFFICE SYMBOL (If applicable)	7a NAME OF MONITORING ORGANIZATION: U.S. Army Strategic Defense Command CSSD-AT-P
ADDRESS (City, State, and ZIP Code): 35 Cherry Hill Drive, Danvers, MA 01923	7b ADDRESS (City, State, and ZIP Code): P.O. Box 1500, Huntsville, AL 35807
NAME OF FUNDING/SPONSORING ORGANIZATION: U.S. Army Strategic Defense Command; 8b OFFICE SYMBOL (If applicable)	9 PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER
ADDRESS (City, State, and ZIP Code): P.O. Box 1500, Huntsville, AL 35807	10 SOURCE OF FUNDING NUMBERS: PROGRAM ELEMENT NO. / PROJECT NO. / TASK NO / WORK UNIT ACCESSION NO

11. TITLE (Include Security Classification)
Buried Silicide Interconnections with Bonded Wafers

12. PERSONAL AUTHOR(S)
S.N. Bunker

13a. TYPE OF REPORT	13b. TIME COVERED	14. DATE OF REPORT (Year, Month, Day)	15. PAGE COUNT
final	FROM 5/15/90 TO 2/15/91	91/2/15	15

16. SUPPLEMENTARY NOTATION

17. COSATI CODES			18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
FIELD	GROUP	SUB-GROUP	

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

Complex monolithic integrated circuits are increasingly limited by the needs of device interconnections. Existing materials take up valuable real estate on the die, limit current and are subject to parasitic capacitances. The use of multilevel and 3D structures has been suggested in order to avoid some of these problems. Formation of conductors by ion implantation shows promise for providing such connections if certain practical problems can be overcome. Novel implementation techniques are proposed which would demonstrate the practicality of complex interconnection patterns.

20. DISTRIBUTION/AVAILABILITY OF ABSTRACT	21. ABSTRACT SECURITY CLASSIFICATION
☒ UNCLASSIFIED/UNLIMITED ☐ SAME AS RPT ☐ DTIC USERS	unclassified
22a. NAME OF RESPONSIBLE INDIVIDUAL: William D. Martin	22b TELEPHONE (Include Area Code): 205-955-1533; 22c OFFICE SYMBOL: CSSD-AT-P

DD Form 1473, JUN 86 — Previous editions are obsolete — SECURITY CLASSIFICATION OF THIS PAGE

Section 1. Introduction

The purpose of the research effort described in this report was to investigate the fabrication of deeply buried conducting lines in a silicon wafer. The method proposed was to form the conducting paths by ion implantation of cobalt to form cobalt silicide. The lines would be widely separated from the device layer using the method of wafer bonding, in which 2 wafers are fused together, followed by subsequent thinning of the "top" wafer. A thin silicon oxide layer at the joint provides isolation, and access would be through an etched via. The technique offers the possibility of increasing wiring density by adding an extra plane, as well as permitting space and improved thermal dissipation for high currents along key paths.

The technology was expected to be difficult to implement. Bonded wafers are not yet a commercial item. The ion implantation of high dose cobalt is a recent technology which could be expected to present surprises, and the precision etching to thin the top wafer has often exhibited variable results.

The initially planned process consisted of the following steps. For convenience, the designation "top" wafer refers to the wafer to be thinned, the one which will eventually contain devices. The "bottom" wafer, sometimes called a handle wafer, is intended to serve as the base and is to remain intact. The bottom wafer contains the cobalt silicide lines in this program.

The following lists contain a summary of the originally proposed process.

Top Wafer Preparation

1. 10 ohm-cm, n-type, 4" polished (100) wafer, nominally 18 mils thick.
2. Ion implant boron, 200 keV, $1x10^{16}$ atoms/cm^2, for an etch stop layer.
3. Anneal wafer, 850°C, 15 minutes, in order to regrow the silicon.
4. Grow 6 microns of silicon by epitaxy, undoped.
5. Dry furnace oxide growth, 500 Angstroms thick.

Bottom Wafer Preparation

1. 10 ohm-cm, n-type, 4" polished (100) wafer, nominally 19 mils thick.
2. Grow 5000 Angstroms of polysilicon on the wafer, undoped.
3. Furnace grow 1000 Angstroms of silicon oxide, dry.
4. Ion implant cobalt through a mask, 190 keV, $3x10^{17}/cm^2$, plus 60 keV, $0.5x10^{17}/cm^2$ at an ambient temperature of 500-550°C.
5. Remove excess furnace oxide with HF.
6. Low temperature CVD oxide wafer back, 3 microns.

Combined Top/Bottom Process

1. Bond wafers at Duke University, Department of Mechanical Engineering.
2. Thermal anneal weakly bonded structure to fix bond.
3. Etch sandwich using EDP, 100°C under reflux, nominally 1 micron/minute.
4. Etch to final thickness using ion milling for slow etch.
5. Etch vias by ion milling through a mask.

The next section will describe the result of 4 attempts to produce the desired structure. No attempt was fully successful, although each try provided information enabling further penetration through the process. When the work had to be terminated, bonded wafers were being etched to the final thickness.

Section 2. Program Results

Cobalt silicide has been recognized as a useful candidate material for the fabrication of buried conducting lines. $CoSi_2$ is closely lattice matched to silicon, and with the addition of cobalt atoms to silicon, the compound forms naturally above 550°C. In studies of high dose ion implantation of cobalt, it has been regularly demonstrated that when sufficient cobalt is present, annealing above 800°C results in discrete buried lines of $CoSi_2$. This approach has been studied for the formation of buried conductors, but due to the high atomic number of cobalt, the buried conductors are always quite shallow in depth.

The approach studied here, using wafer bonding to effectively bury the lines, is potentially far more powerful. No damage to the device silicon occurs, conducting lines can be any desired width, and high currents can be accommodated. Good line-to-line and line-to-substrate isolation can be obtained relatively easily. The negative side is that a complex, as yet not well developed, technology must be pursued, and the risk of initial failure is high.

Implant Sciences has had experience with most of the technologies required to produce the desired structures. We have ion implanted cobalt as part of our implant service work, and the high temperature heater stage was available. We have performed commercial wafer bonding and etching, although most of the work has been with a glass-to-wafer structure for x-ray lithography pellicles. Because of this experience, it was hoped that the proposed structure would be relatively straight-forward to fabricate.

2.1 Sputtering Studies

Initially, it was recognized that the cobalt ion beam would cause excessive sputtering to occur because of the high dose involved. Since a non-flat surface could result, there was a concern with providing too thick a sacrificial layer during implantation. The problem consisted of a tradeoff between layer thickness and sputtering coefficient. Most desireable would be a low

sputter coefficient material which could easily be deposited on the bottom wafer prior to implantation.

The natural choice is SiO_2 because it is so easily formed. However, although the sputtering coefficient of Cobalt on SiO_2 is not published, projections suggested that it would be unacceptably high. If the coefficient is too high, the coating erodes rapidly, thus shifting the location in depth of the peak of the buried cobalt distribution. The rapid position shift prevents a sufficient local cobalt concentration to be built up without resorting to a complex, multi-energy process.

Initial estimates were made using Implant Sciences' Profile Code™, a commercial program which predicts implanted depth distributions. The best sacrificial coating appeared to be a thin carbon layer, as shown in the calculations of Figure 1.

In practice, carbon could not be the only coating because it is so difficult to remove. Thus, a two layer experimental coating of 250 Angstroms of SiO_2 covered by 750 Angstroms of carbon was fabricated. The oxide was grown as a dry furnace oxide. At the same time, a sample with 1000 Angstroms of SiO_2 only was grown for comparison tests.

The samples were mounted on a high temperature stage, which was used for all subsequent high temperature implantations. The stage consisted of a carbon strip heater covered by a silicon wafer. The barrier wafer is supported by a graphite plate, which has a 4" hole in it. The barrier wafer serves as an IR-transparent shield. The actual wafer is mounted above the shield wafer with a vacuum gap in between. Clamps can be added to shadow the front wafer and provide a mask edge for profilometer measurements.

After the accumulated dose, a profilometer measures the step between nearby implanted and unimplanted regions. If one assumes that no volumetric change occurs because of the reactions to form $CoSi_2$, the sputtering coefficient is given by

$$S.C. = rho * N_{AV} * t/M/dose/cos(A)$$

where S.C. = sputtering coefficient

rho = silicon density, 2.33g/cm^3

N_{AV} = Avogadro's number, 6.02×10^{23} atoms/mole

t = step height in cm

M = molecular weight of silicon, 28.05

dose = ion dose at one energy in atoms/cm^2

cos(A) = cosine of the angle of incidence (11° for this work)

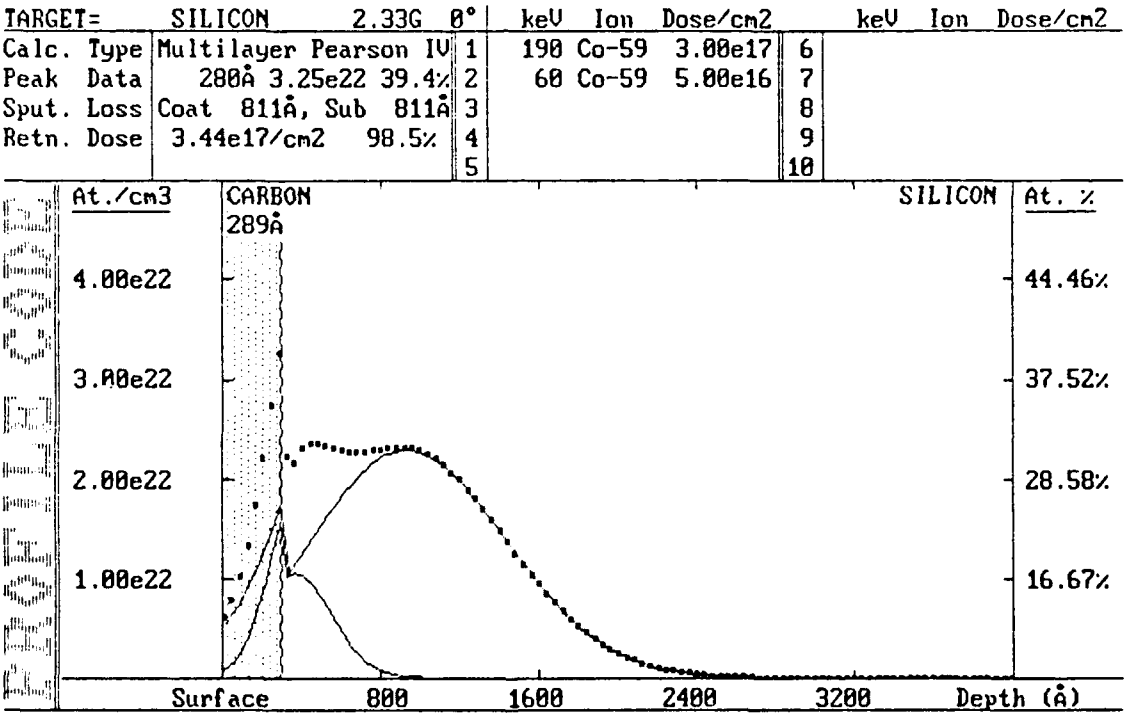

Figure 1. Theoretical prediction of implanted Cobalt distribution using a 1000 Angstrom carbon sacrificial coating. The solid squares are the sums of the contributions from the two energies shown. After implantation, just under 300 Angstroms of coating remains.

Three samples were exposed to the beam. Because the results for SiO_2 were surprising, a second sample was prepared and the measurement repeated. Table 1 shows the results of the measurements. Obviously, SiO_2 is the best choice, and surprisingly, carbon is quite poor. Considering the ease with which the SiO_2 could be formed, this was a fortuitous result. In fact, the sputtering coefficient for carbon used in Figure 1 is essentially the same as for SiO_2, and the energies/doses of the figure could be used without modification.

TABLE 1. Sputtering Coefficient Results

energy (keV)	Silicon	SiO_2	Carbon
190	1.75	.93 (.89)	2.48
60	2.90	1.13	3.48

2.2 Implant Studies

A second early concern was for a diagnostic technique to show the location of the buried cobalt silicide lines. During bonding, there is little control over the orientation of the wafers. Since the metal lines are buried during bonding, a method was needed to guide the registration of via masks.

It was suspected that the conductive buried lines would be opaque to infrared radiation if they were thick enough. A test was made with an infrared video system, which we also use to analyze wafer bonding quality. The gap caused by a dust particle trapped between bonded surfaces creates an optical interference pattern known as Newton's rings, which is quite visible in infrared. Here, the same camera shows the relative transparency between pure silicon and cobalt-containing silicon.

The original tests were performed using test chips. A later picture, shown in Figure 2, shows a patterned wafer that was made for bonding. The test pattern, the so-called happy face

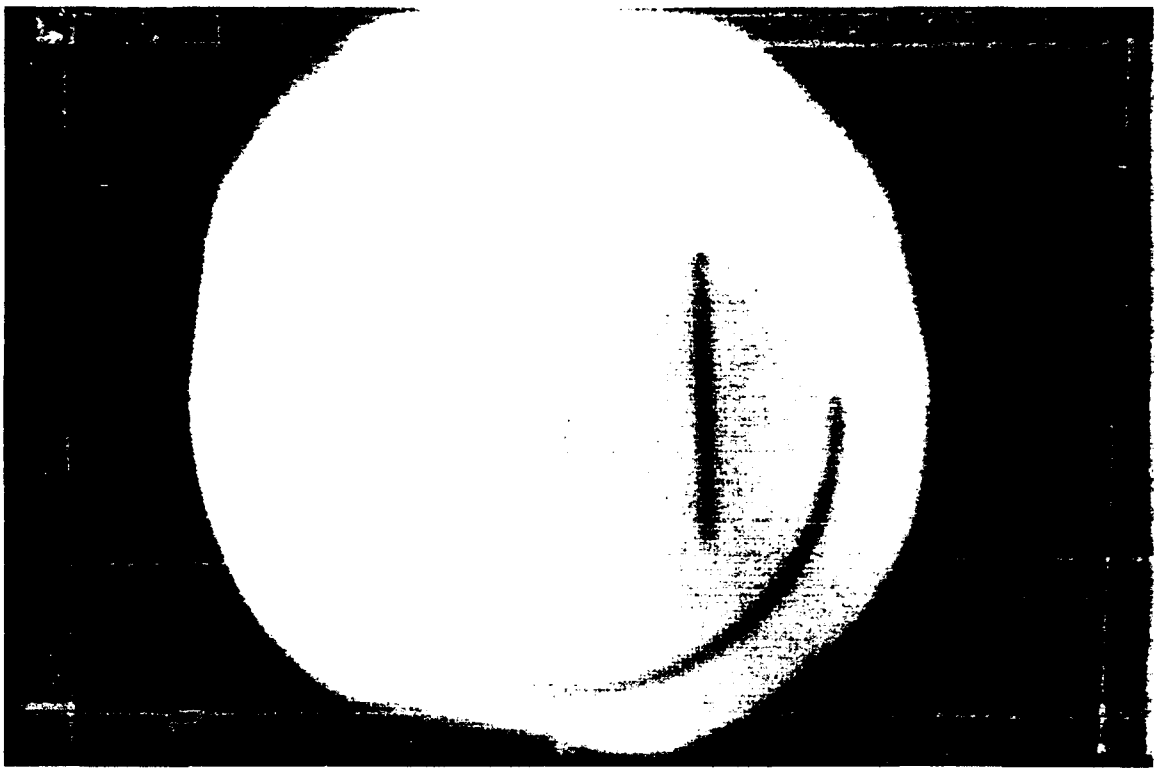

Figure 2. Infrared transmission video image of a cobalt-implanted wafer ($3x10^{17}/cm^2$) demonstrating identification of line location.

arrangement of lines, clearly stands out and can be identified readily. Other tests showed that a backlit or infrared microscope is also adequate to permit accurate registration of the image.

2.3 Sample Set #1

2.3.1 Top Wafer Preparation

The top wafers were generally all made using the same process with only small modifications. The wafer parameters were given in Section 1. The wafers were first ion implanted with boron, which is well-known to form an etch-stop when certain acids are used. A concentration of boron typical of a dose of $1x10^{16}/cm^2$ at 200 keV is required to produce a

sufficient ratio of etching rate between unimplanted and implanted layers. This dose has been reported by others and used successfully at Implant Sciences.

After implantation, a brief anneal is required to regrow the silicon crystal. This is not to anneal the boron, because that will occur automatically in the next step. Thus, only 800° for 15 minutes was used in a flowing nitrogen ambient.

The etch stop is highly boron doped and thus unsuitable for device fabrication. Thus, a thick layer of device-grade material must be added on top of the etch stop. When the wafers are bonded, this layer will become the "top" of the structure. The silicon was grown with CVD epitaxy. Since some autodoping from the etch stop zone was expected, no doping of the 6 micron epi layer was used. The thickness was selected to minimize autodoping in the device region.

The only optional part of the process is the addition of a thin, dry furnace oxide layer at this point. This was done on the first batch of top wafers making a 500 Angstrom layer. The reason is that either the top or the bottom wafer needs to have an isolating oxide surface. Since it was expected that the sacrificial oxide of the bottom wafer would be removed to planarize the surface, this required the oxide to be on the top. In the second lot of top wafers, no oxide was grown since the bottom wafer retained its oxide.

Figure 3 shows a sample of a top wafer from the first batch. Some color fringes are apparent around the rim, particularly at four points related to mounting on the furnace boat. The apparent surface texture on the wafer, which may not be clearly visible in the reproduction, is an artifact of the photography and was not on the wafer. The color fringes around the rim suggest a variation of several hundred angstroms in oxide thickness. It is not known if this may have affected the subsequent failure to bond properly.

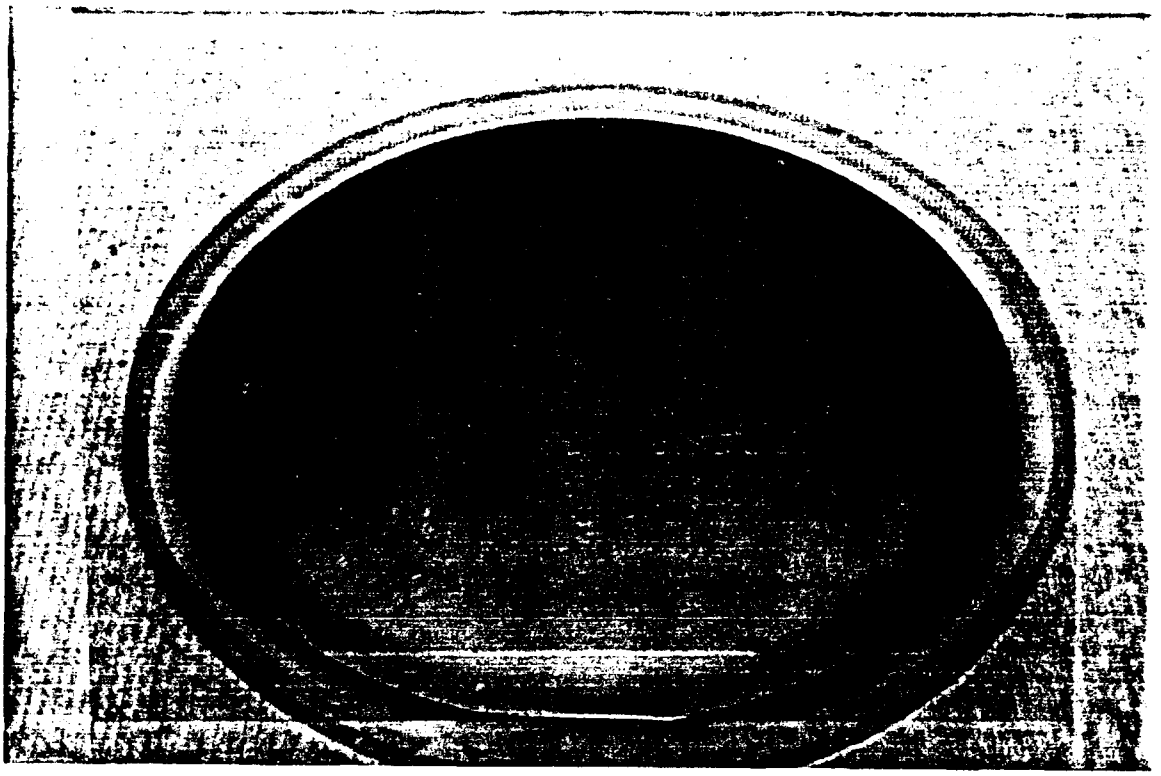

Figure 3. Top wafer used in batch #1 processing. The dark rim area indicates non-uniformity in the oxide.

2.3.2 First Bottom Wafer Preparation

Bottom wafer preparation varied considerably. There were 3 separate batches as process problems were recognized. The preparation for the first batch is described here.

A standard polished wafer was coated with 5000 Angstroms of polysilicon. This was thought to be a useful economy since there was no requirement for single crystal silicon in the bottom wafer. Isolating the conductive lines from each other is technically difficult, and intrinsic polysilicon provides a low cost method of creating side-to-side insulation. Although not used here, it was expected that the polysilicon would be grown on a SiO_2 layer, which in turn would be grown on the bottom wafer first. Thus, complete 3D isolation could be produced at low cost.

The bottom wafer was dry furnace oxidized to a 1000 Angstrom thickness. This still left

adequate thickness for the cobalt implant depth, which penetrated 2500 Angstroms below the oxide/polysilicon interface. This oxide layer was the sacrificial layer that would be locally eroded by the cobalt sputtering.

The implant used was always $3x10^{17}/cm^2$ at 190 keV followed by $0.5x10^{17}/cm^2$ at 60 keV. The second, low energy implant was used to "fill in" the distribution near the oxide/silicon interface. The implant was performed through a graphite mask that was undercut at the windows to minimize thickness. This was found to be simpler than doing lithography. When the wafers were finished being implanted, the mask pattern was clearly visible in the oxide on the surface, as shown in Figure 4. This pattern was the result of different color optical interference layers due to the difference in thickness caused by sputtering in the implanted areas.

The next step was to re-planarize the wafer by etching away the SiO_2 sacrificial coating. Since some oxide, about 250 Angstroms, remained in the implanted lines, total oxide removal would restore flatness at the silicon interface.

When the HF etch was complete, the line pattern was gone, as expected. However, we were unable to find any electrical conductivity where the line had been located. Infrared imaging was also negative. A profilometer scan showed channels 2000 Angstroms deep where the lines had been.

The obvious interpretation, confirmed by checking some chemistry texts, was that the HF acid dissolved the $CoSi_2$. In this application, unlike previous published research making buried $CoSi_2$ layers, the $CoSi_2$ intentionally reaches the silicon surface at full concentration. This geometry provides a thicker conducting layer. However, the geometry also exposes the $CoSi_2$ to process chemicals until after the bond is complete.

Once identified, a variety of possible solutions could be applied. We chose to maintain the $CoSi_2$ thickness and relax our demand for uniform planarity of the wafer. This choice wwa based on the assumption that the find lines normally encountered in lithography would be

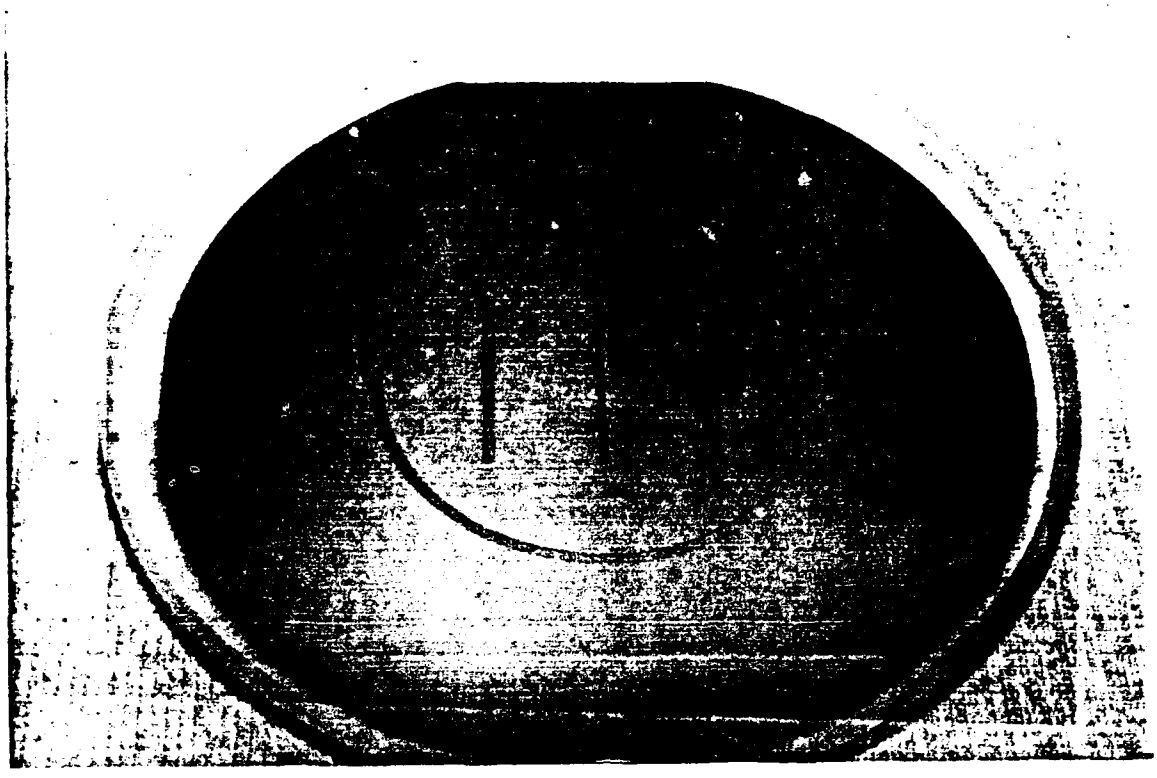

Figure 4. Ion implanted cobalt pattern in bottom wafer. The pattern is visible due to optical interference differences in the oxide coating.

unimportant in affecting the bonding process. In addition, a minor process step was eliminated. Subsequent results showed that the assumption was correct.

2.3.3 Second Bottom Wafer Preparation

The second set of 4 bottom wafers were processed like the first except that the final HF dip was deleted. These wafers were sent to Duke University, Department of Mechanical Engineering.

2.3.4 Batch #1 Bonding

Professor Goesele of Duke University supervised the bonding using his flowing water bonding process. He was totally unsuccessful in getting any of the wafers to bond. He informed

us that his process performs best with new, single crystal wafers. He tried a variety of tricks, including removal of the suspect top wafer oxide, but could find no combinations that would bond.

Although there was no obvious fault to correct, we speculated that the use of polysilicon resulted in either a loss of flatness at the microscopic level or possibly that the mis-matched crystal planes were important. Professor Goesele could not confirm this speculation, but it was decided to try again using solely single crystal material.

2.4 Sample Set #2

This was the same as the top wafers for set #1 except that the final oxide layer was not added.

2.4.2 Bottom Wafer Production

The starting material was intrinsic silicon wafers. These polished 4" wafers had a resistivity of 1000 ohm-cm and were (100). Three wafers were prepared. The same oxide layer and ion beam parameters as previously used were employed. The oxide showed a normal image of the mask, and the oxide was not removed. Shading, as shown by infrared imaging, showed that a conductive layer was present. Similar shading on test chips correspond to 15 ohms between two points 1 inch apart.

2.4.3 Wafer Bonding

Of the three sets of wafers prepared, 2 pairs successfully bonded and 1 broke.

2.4.4 Thinning to the Etch Stop

The process of etching down to the boron etch stop is a slow procedure. The acid used,

well documented in the literature, is EDP (ethylene diamine pyrocatechol). The acid performs best in a solution at 100°C. Since the acid is thinned with water, the concentration changes with time unless the steam is collected and returned to the solution. Thus, the etch is performed under reflux conditions. The etch rate is nominally 1 micron per minute, which would result in complete removal of the top wafer in 7 hours. In practice, the etch rate varies considerably with local regions etching slowly and others etching much more quickly. As the etch stop layer is reached, it is common for thick islands of silicon to still be present as the mirror surface of the etch stop is exposed.

The first wafer pair had etched for 12 hours when suddenly the bottom wafer began etching rapidly. Since fumes from EDP are hazardous, the wafer is checked irregularly at long intervals, so the exact rate of loss of the bottom wafer was unknown. Also, since this was unexpected, we were not looking for the effect. The 12 hours that the top wafer took to etch was surprisingly long, but not all that unusual. The very short time to lose the bottom wafer was very unusual. Figure 5 shows the remains of the wafer. No conductive line are identifiable by infrared as shown in Figure 6. However, the negative IR image may also be an artifact of the high brightness contrast affecting the video automatic gain control.

The second wafer pair was further coated on the back of the bottom wafer in an attempt to further hinder break through of the rear oxide layer. A sputtered layer was added, but induced stresses resulted in cracking of the wafer pair. Sections were still large enough to try the EDP etch again.

Once again the thinning of the top wafer proceeded slowly. This time the bottom wafer broke through and the dissolution was so rapid, that all material was consumed within 45 minutes. Thus, this confirmed the extreme difference between etch rate in the top and bottom wafer material. It is speculated that intrinsic silicon etches in EDP at a rate in excess of 20 times faster than doped wafers. If this is true, there could be several methods of resolving the etching problem. These will be discussed in the next section.

Figure 5. Remains of first bonded wafer pair after start of rapid dissolution of bottom wafers.

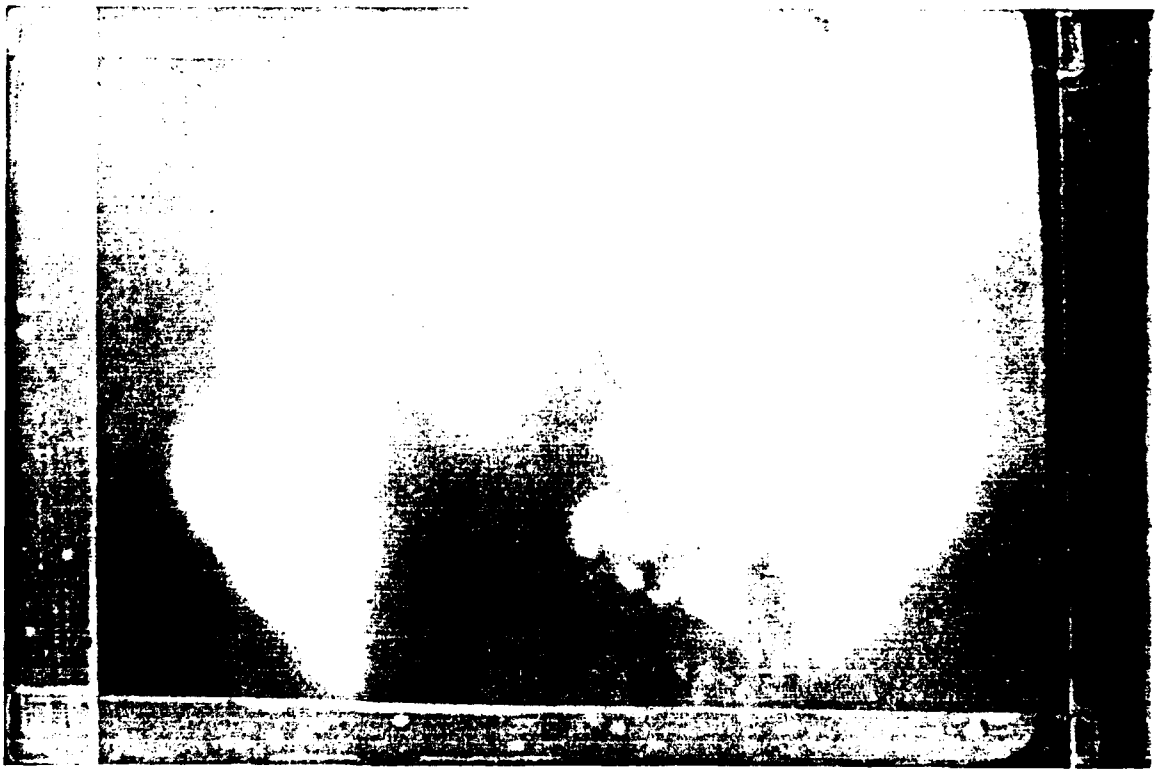

Figure 6. Infrared scan of the wafer of Figure 5. No conductive cobalt lines are visible.

Section 3. Comments and Suggestions.

The most important practical observations made during this research are the following:

1. SiO_2 provides the best sputtering coefficient of the possible common coatings.
2. $CoSi_2$ is sensitive to surface processing with acids.
3. Surface topography caused by sputtering does not have a strong effect on bonding, but polycrystalline material is not usable.
4. High resistivity silicon is dissolved by EDP at a rate at least 10-20 times faster than doped material.

The problem encountered with the EDP etch could be solved using any of several obvious techniques. The bottom wafer could be made of ordinary doped material with a thin intrinsic epi layer grown on its surface. This would mean using starting material structured exactly like the top wafer except that the boron implant would not be present. The doped substrate would etch slowly if the rear cap were breached. Similarly, the use of a thick low temperature CVD oxide cap on the back of the bottom wafer would increase the protection from the acid.

Later process steps were never attempted, and it is not certain whether any unforseen problems might develop. Specifically, the ion milling to be used for final thinning and via cutting is not a technology with which we have had experience.

It is the belief of the Principal Investigator that this technology can be shown to work successfully, even though we were unable to demonstrate meeting our Phase I goals. The problems encountered were not of a fundamental nature, and only the time limit of the Phase I effort prevented us from completing the process. We recommend that this technique merits further exploratory research at a later date.