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HOT ELECTRON STRESS TESTING OF SUBMICRON TRANSISTORS

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13. ABSTRACT *(Maximum 200 words)*

Hot electrons are a major reliability concern for submicron metal-oxide-semiconductor (MOS) transistors. This report details experimental results of long-term hot electron degradation. Theoretical explanation of test results is provided. The implications of these results with respect to the validity of long-term reliability predictions is also discussed.

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1.0 INTRODUCTION

As the channel length of MOS transistors decreases, the magnitude of the electric field between the source and drain increases. As a result of the increased field strength, carriers moving through the channel become more energetic and are said to be "hot". The channel electric field is strongest near the drain and scattering in this region can deflect the hot carriers toward the gate oxide where they may generate interface states at the $Si-SiO_2$ barrier or are trapped in the gate oxide. Trapped charge in the oxide will affect the threshold voltage, saturation current and transconductance of the device. An increase in the number of interface states will reduce the transconductance and subthreshold swing. The long term effect of this process is transistor parameter drift.

2.0 DISCUSSION

Test structures consisting of transistors with drawn gate lengths of 0.65 to 10 microns (N-channel) and 0.75 to 10 microns (P-channel) were packaged and subjected to hot carrier stress. Four different drain voltages were utilized in an attempt to extrapolate device lifetime information from accelerated stress conditions. The gate bias was selected to provide maximum substrate current. This substrate current is a result of impact ionization in the channel and is indicative of the relative quantity of hot carriers present in the channel. Figures 1 through 16 demonstrate the behavior of the substrate current as a function of gate voltage. The substrate current increases first with Vg, reaches a maximum, then decreases. The maximum in I_{sub} can be explained as follows. Assuming that the impact ionization occurs uniformly in the pinch-off region, the substrate current can be written as I_{sub}=Id*A*Lp where Id is the drain current; A is the ionization coefficient, the number of electron hole pairs generated per unit distance; and Lp is the length of the pinch-off region. For a given Vd, as Vg increases, both Id and Vdsat increase. When Vdsat increases, the lateral field (Vd-Vdsat)/L decreases, causing a reduction of A. Thus there are two conflicting factors. The initial increase of I_{sub} is caused by an increase of drain current with Vg, and at larger Vg, the decrease of I_{sub} is due to the decrease of A. Maximum I_{sub} occurs where the two factors balance.[1] Table 1 lists the gate and drain bias voltages selected for maximum substrate current for the N- and P-channel transistors.

The transistors were stressed for many hours at -55°C. The low temperature enhances the hot carrier effect as a result of an increase in the electron trap density in the oxide[2] and an increase in the carrier mean free time between collisions.[1] The increase in mean free time between collisions allows the carriers

to gain more momentum between collisions and thus they become "hotter".

Table 1. Transistor bias conditions for maximum substrate current.

N-channel devices		P-channel devices	
Drain Voltage (v)	Gate Voltage (v)	Drain Voltage (v)	Gate Voltage (v)
4.5	2.1	-4.5	-1.7
4.2	1.9	-4.2	-1.6
3.9	1.8	-3.9	-1.5
3.6	1.7	-3.6	-1.4

All device characterization was performed with an HP4062B Semiconductor Parametric Test System under the control of an HP9836 computer. Threshold voltage was determined by extrapolation of the Id vs. Vg curve at Vd=0.1 volt. Transconductance and subthreshold slope were also measured with Vd=0.1 volt. Saturation current was measured at Vg=Vd=3.3 volts. C-V profiling of the individual gate to channel capacitors was not possible as the test structures utilized a common gate connection. Prior to each characterization, all devices were left at room temperature with all pins grounded for at least 24 hours. This was done because it has been shown that device characteristics are not stable immediately after stressing.[3] Grounding all device pins for an additional 24 hours resulted in no further change of device characteristics.

3.0 N-CHANNEL DEVICES

Figures 17 through 28 demonstrate the change in dc characteristics such as threshold voltage, saturation current and transconductance for N-channel devices subjected to hot electron stressing. For sake of brevity, plots for devices bias at 3.6 volts and devices with channel lengths greater than 0.9 micron are not included. The plots not included showed no appreciable change in parameters with time. Figures 17 through 28 show various amounts of degradation depending on bias conditions and channel length. One trend which is apparent in all of the plots is that there is a gradual saturation of the degradation. The probable cause is the accumulation of electrons in the oxide near the drain which would alter the electric field so as to force the drain current deeper into the substrate and thereby decrease the number of hot

electrons near the $Si-SiO_2$ interface. The accumulated electrons cause an increase in the threshold voltage and a decrease in both saturation current and transconductance. Cham, et al, hypothesize that enough charge accumulates near the drain to form a depletion layer and thereby increases the series resistance of the device.[4] If this was true, then for P-channel transistors the depletion layer formed would decrease the effective gate length and move the drain closer to the source. Continuation of this process would lead to source-drain punch-through.

4.0 P-CHANNEL DEVICES

Figures 29 through 43 show the change in dc characteristics for P-channel devices subjected to hot electron stressing. As with the N-channel devices, plots are omitted for devices biased at -3.6 volts and devices with channel lengths greater than 1.4 microns, as these devices showed no discernible change with time. Similar to the N-channel devices, the degradation seems to saturate. However, the degradation in the P-channel devices saturates much more abruptly. The accumulation of electrons in the oxide decreases the magnitude of the threshold voltage and also increases the saturation current and transconductance. The increase in current means there is a greater number of hot electrons near the $Si-SiO_2$ interface available to degrade the device. The sudden stop in degradation implies that there are a limited number of sites available for electron trapping and once these sites are filled, no further degradation occurs. These data show that filling of the available traps occurs before a depletion region is formed and the effective gate length is reduced.

5.0 ANNEALING

In an attempt to assess annealing characteristics of degraded devices, other than the short term ones mentioned in reference 3, various approaches were tried. First, a high temperature bake (24 hours at $150^{o}C$) with all pins grounded was performed. Post bake characteristics were identical to those of devices before baking. The next anneal consisted of putting de-lidded devices in a UV EPROM eraser for one hour. This also had no effect on the trapped electrons.

6.0 HOT HOLE INJECTION

For N-channel MOSFETs, it is possible to inject hot electrons or hot holes into the gate oxide by varying the bias conditions.[5] With this in mind, an N-channel transistor was first subjected to hot electron injection (Vd=5.5 volts and Vg=2.6 volts) and subsequently to hot hole injections (Vd=5.7 volts and Vg=0.6 volt). A

higher drain voltage was selected for hot hole injection to completely compensate for the previously injected hot electrons.[6] Figure 44 shows that the hot electron induced threshold voltage and saturation current shifts can be recovered by hot hole injection. These two parameters are very sensitive to trapped charge in the gate oxide and relatively insensitive to interface states. Transconductance and subthreshold swing are also sensitive to trapped charge and very sensitive to the presence of interface states. Figure 45 shows the transconductance and subthreshold swing for the same device. It can be seen that the shifts of these two parameters do not completely recover during hot hole injection. It is believed that interface states are responsible for the unrecovered portions of these parameter shifts.

For P-channel devices, hot hole injection is not possible, but one may conclude that the degradation is similarly caused by both electron trapping and generation of interface states.

7.0 CONCLUSIONS

This work has shown a saturation effect for hot carrier degradation in both N- and P-channel transistors. The implication of this saturation is that device lifetime predictions based on short term high stress test conditions may be overly pessimistic. If the device parameters can drift to the point of failure before saturation, then extrapolated short term testing is valid. However, if the degradation saturates before the failure point, the extrapolated short term testing gives overly pessimistic results. Testing for hot electron effects in MOSFETs must be performed to the point of failure or until the degradation saturates.

This work has also shown that bias conditions can affect the type of hot carrier degradation in MOSFETs. Hot electrons or hot holes can be injected in N-channel MOSFETs while only hot electrons can be injected in P-channel MOSFETs. In all cases, there is an irreversible generation of interface states in the devices.

Not included in this work is the effect of dynamic stimulus on hot carrier degradation. Hot carrier degradation has been shown to be dependent on the transition time of the stimulus.[7] For the purpose of demonstrating the degradation saturation effect proven herein, dynamic stimulus was not required. However, the effects of dynamic stimulus and degradation saturation must be taken into account when performing a hot carrier reliability evaluation as these can have a serious impact on life time predictions for a dynamic circuit.

Currently hot carrier effects are controlled by: using lightly doped drain structures, by scaling power supply voltages, or both. As MOSFET technology advances even further below the one

micron gate, hot carriers will become a greater reliability concern and the need for accurate assessment of their potential impact will become critical.

8.0 ACKNOWLEDGMENT

The author would like to thank Mr. Drew Brocking of the Electronics Technology and Devices Laboratory for his assistance in packaging the test structures used in this study.

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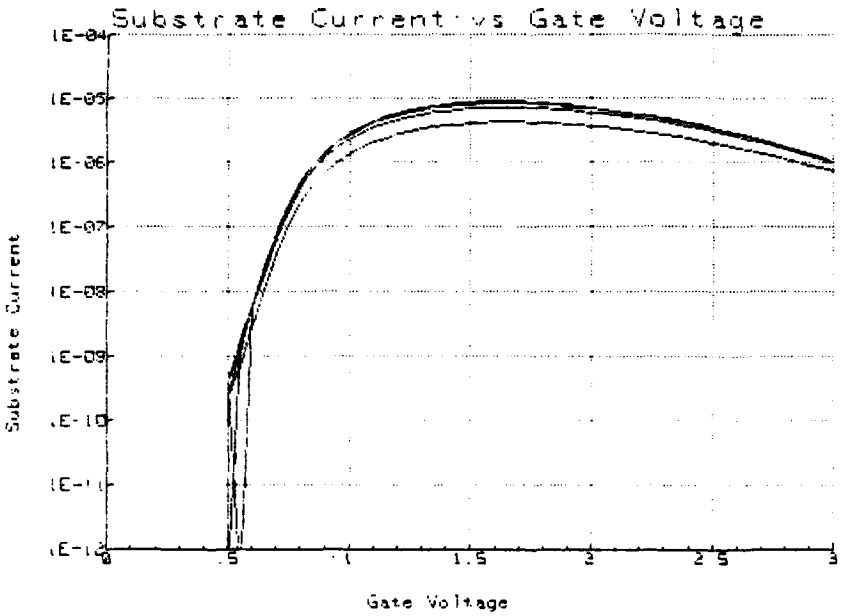

Figure 1. Substrate current vs. gate voltage for long N-channel FETs with Vds = 3.6 volts. W/L = 50/1.3, 50/1.6, 50/3.0, 50/10.0 (microns).

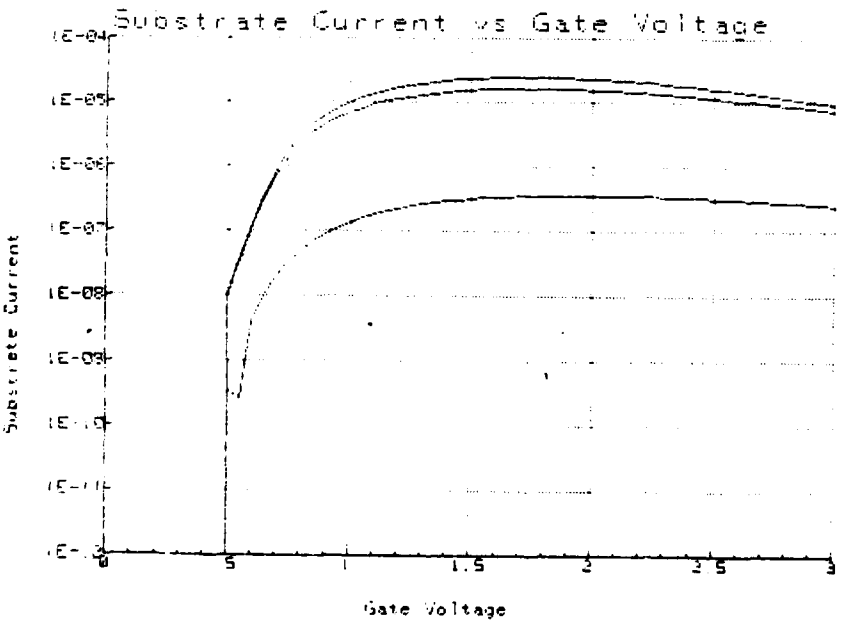

Figure 2. Substrate current vs. gate voltage for short N-channel FETs with Vds = 3.6 volts. W/L = 50/0.65, 50/0.9, 2.7/0.65 (microns).

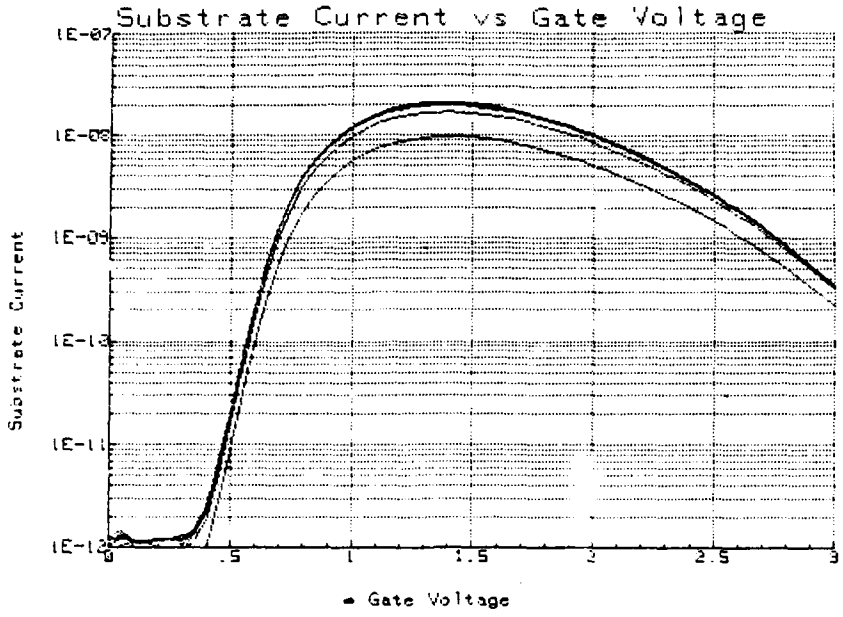

Figure 3. Substrate current vs. gate voltage for long P-channel FETs with Vds = -3.6 volts. W/L = 50/1.4, 50/1.6, 50/3.0, 50/10.0 (microns).

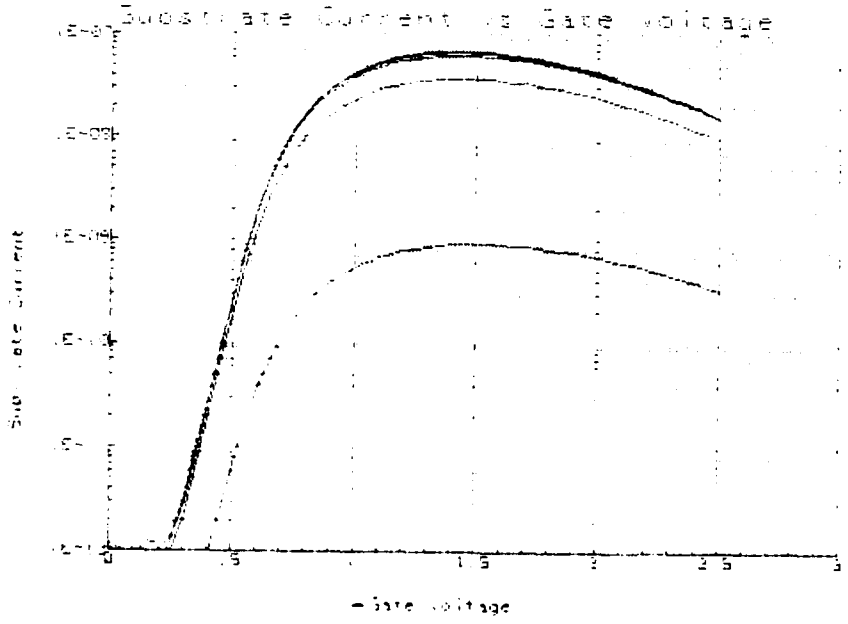

Figure 4. Substrate current vs. gate voltage for short P-channel FETs with Vds = -3.6 volts. W/L = 50/0.75, 50/0.9, 50/2.6, 2.7/0.75 (microns).

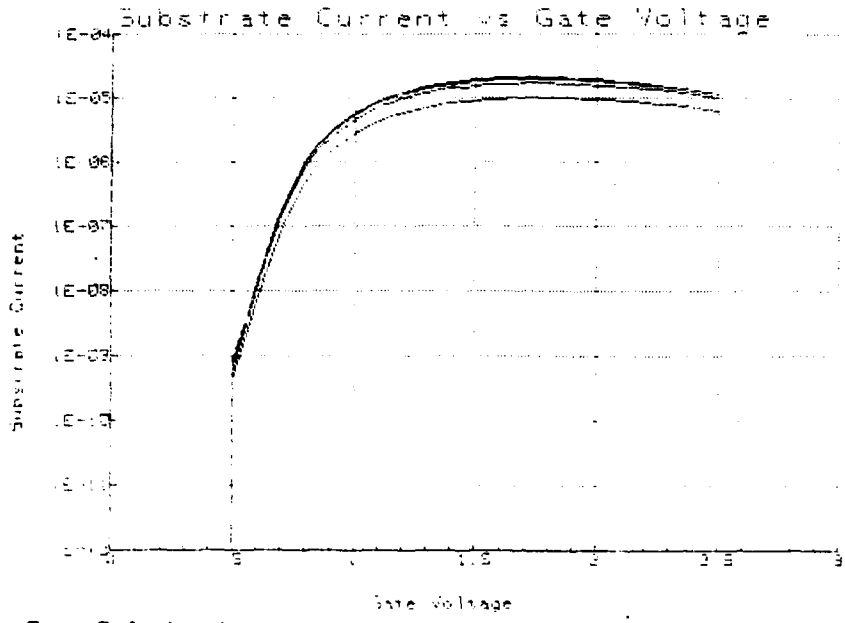

Figure 5. Substrate current vs. gate voltage for long N-channel FETs with Vds = 3.9 volts. W/L = 50/1.3, 50/1.6, 50/3.0, 50/10.0 (microns).

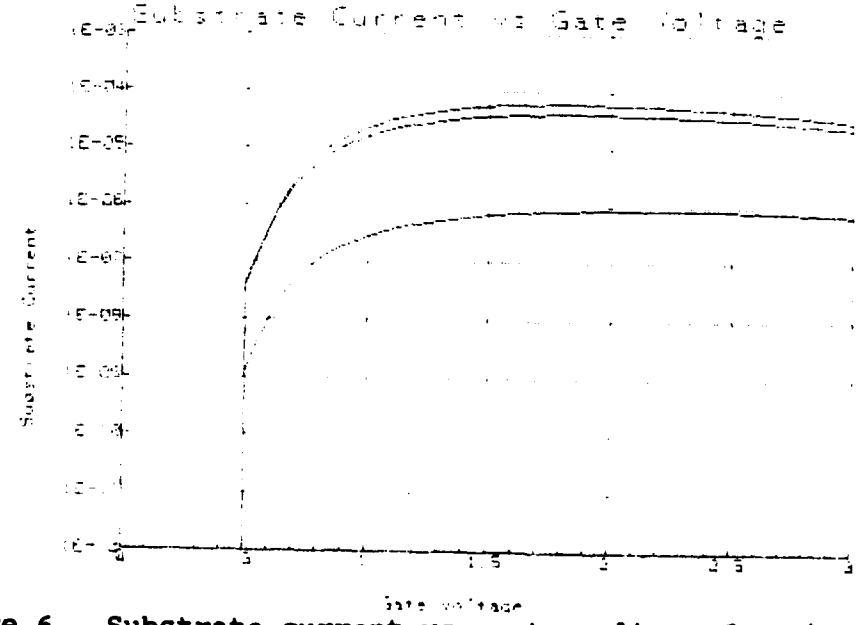

Figure 6. Substrate current vs. gate voltage for short N-channel FETs with Vds = 3.9 volts. W/L = 50/0.65, 50/0.9, 2.7/0.65 (microns).

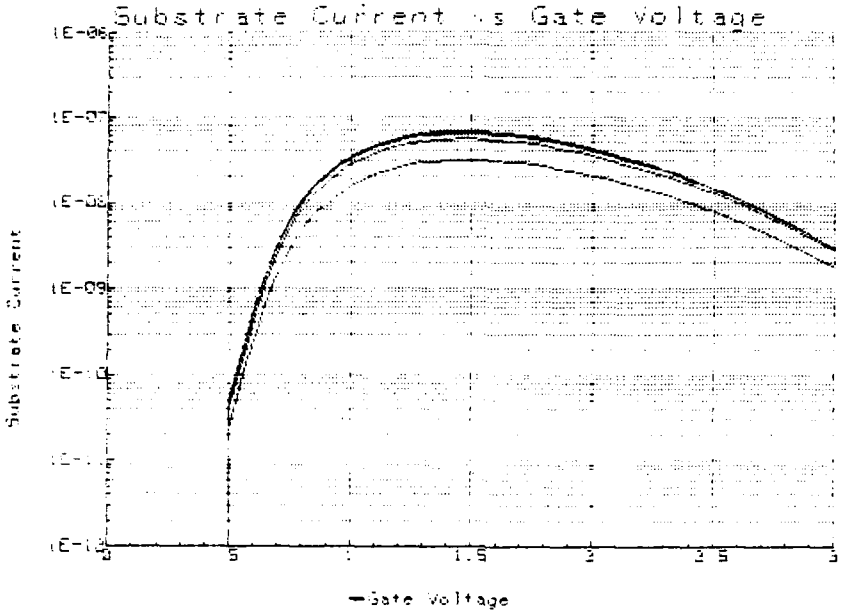

Figure 7. Substrate current vs. gate voltage for long P-channel FETs with Vds = -3.9 volts. W/L = 50/1.4, 50/1.6, 50/3.0, 50/10.0 (microns).

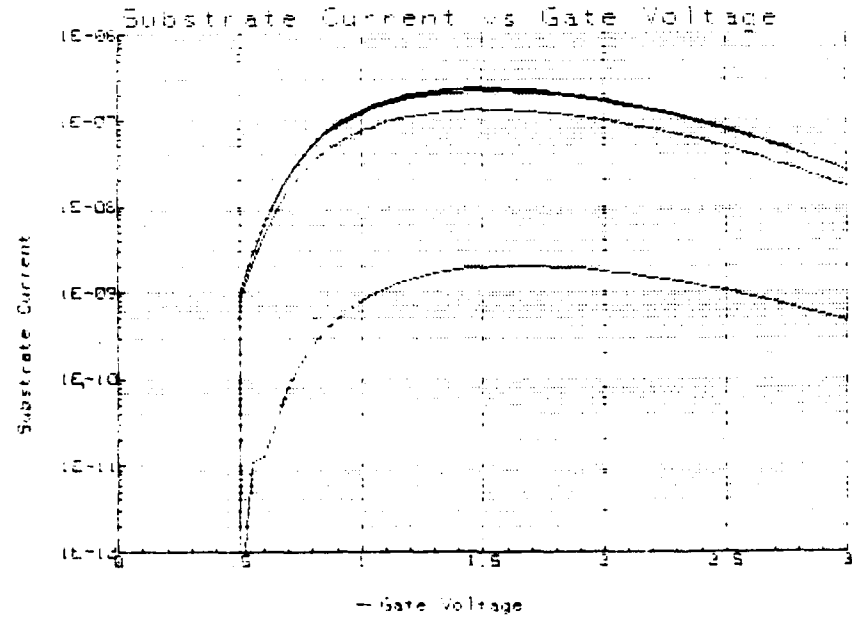

Figure 8. Substrate current vs. gate voltage for short P-channel FETs with Vds = -3.9 volts. W/L = 50/0.75, 50/0.9, 50/2.6, 2.7/0.75 (microns).

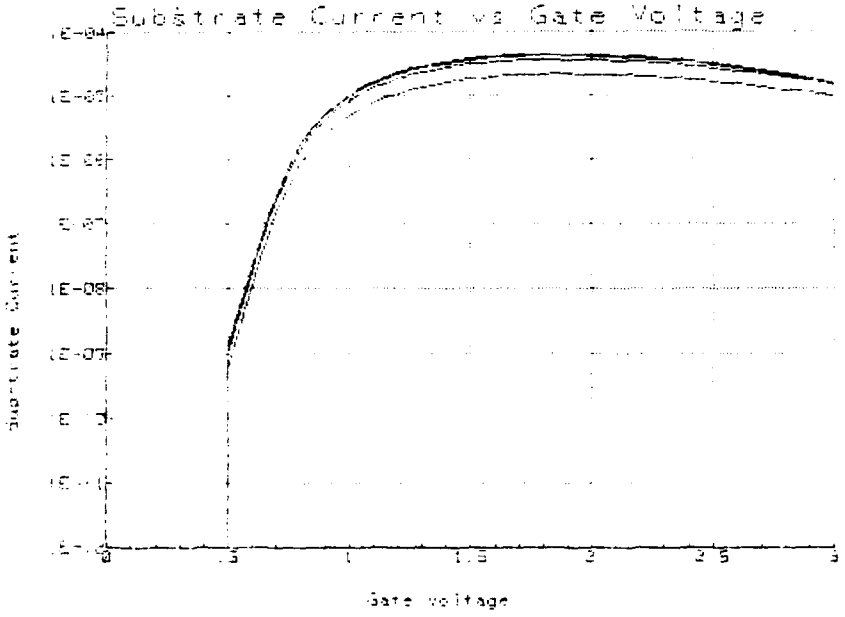

Figure 9. Substrate current vs. gate voltage for long N-channel FETs with Vds = 4.2 volts. W/L = 50/1.3, 50/1.6, 50/3.0, 50/10.0 (microns).

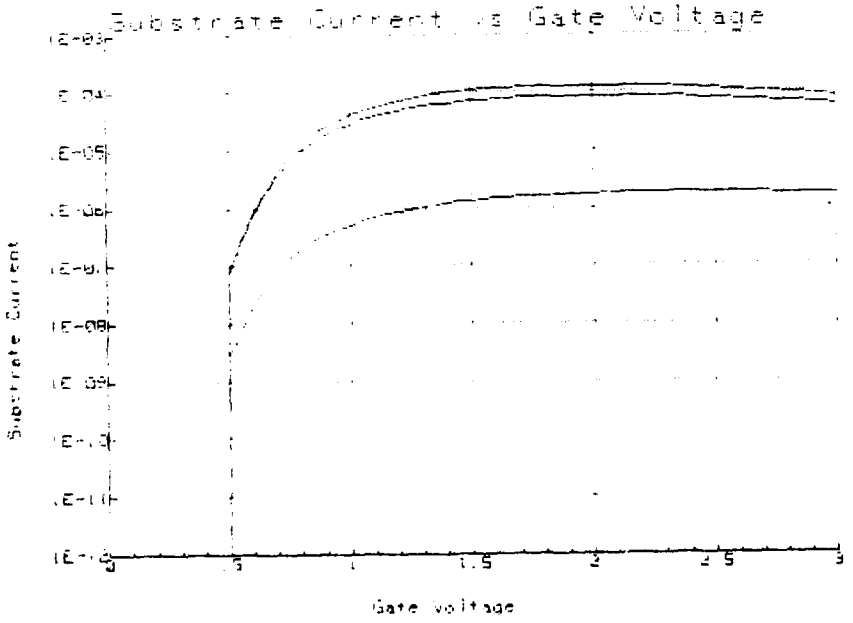

Figure 10. Substrate current vs. gate voltage for short N-channel FETs with Vds = 4.2 volts. W/L = 50/0.65, 50/0.9, 2.7/0.65 (microns).

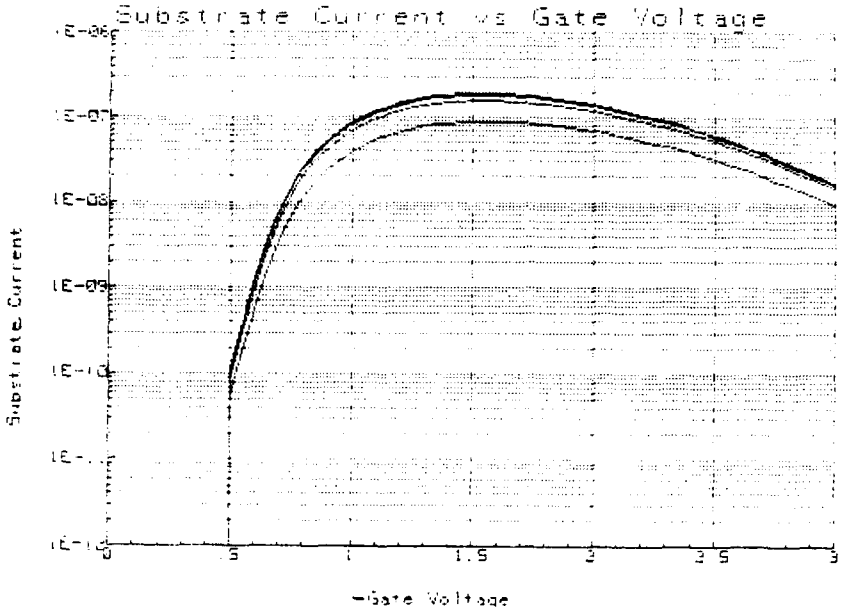

Figure 11. Substrate current vs. gate voltag for long P-channel FETs with Vds = -4.2 volts. W/L = 50/1.4, 50/1.6, 50/3.0, 50/10.0 (microns).

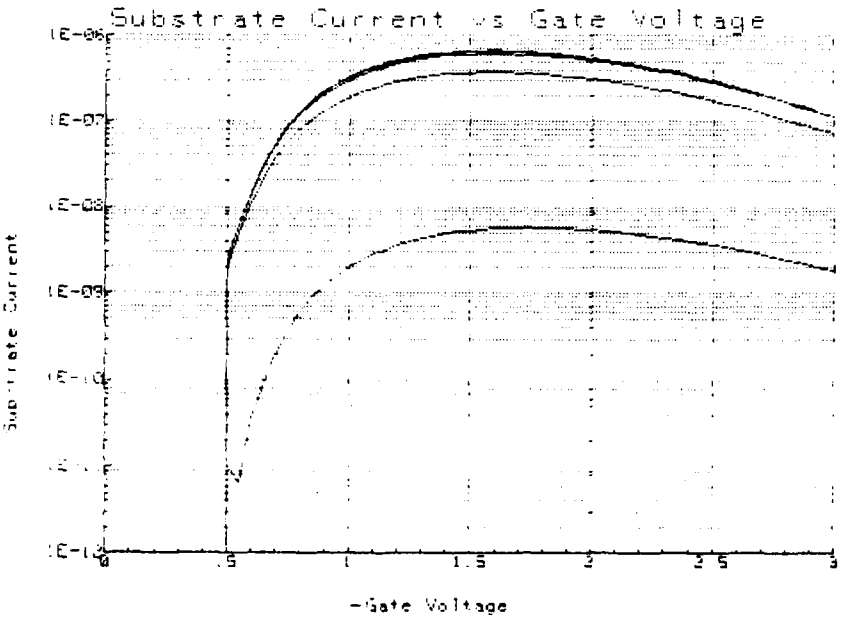

Figure 12. Substrate current vs. gate voltage for short P-channel FETs with Vds = -4.2 volts. W/L = 50/0.75, 50/0.9, 50/2.6, 2.7/0.65 (microns).

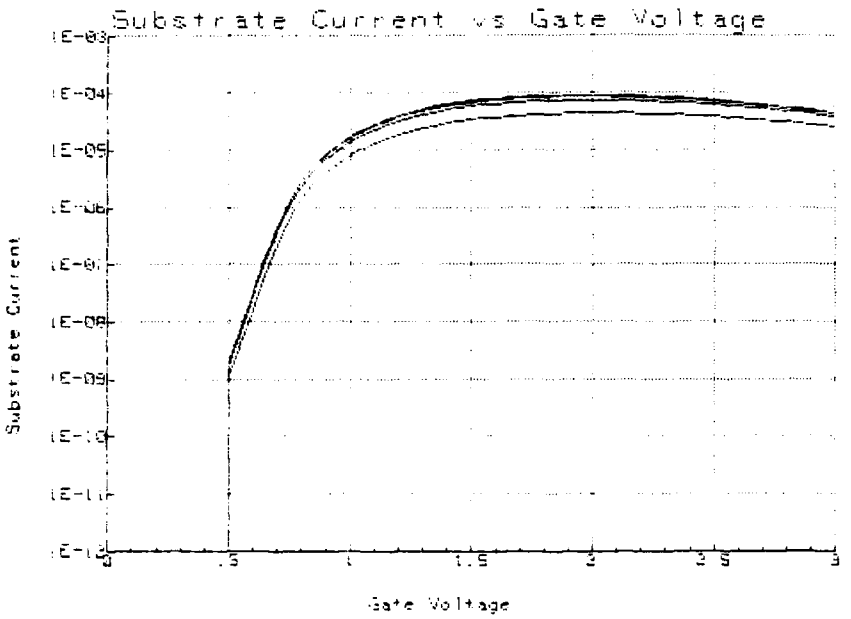

Figure 13. Substrate current vs. gate voltage for long N-channel FETs with Vds = 4.5 volts. W/L = 50/1.3, 50/1.6, 50/3.0, 50/10.0 (microns).

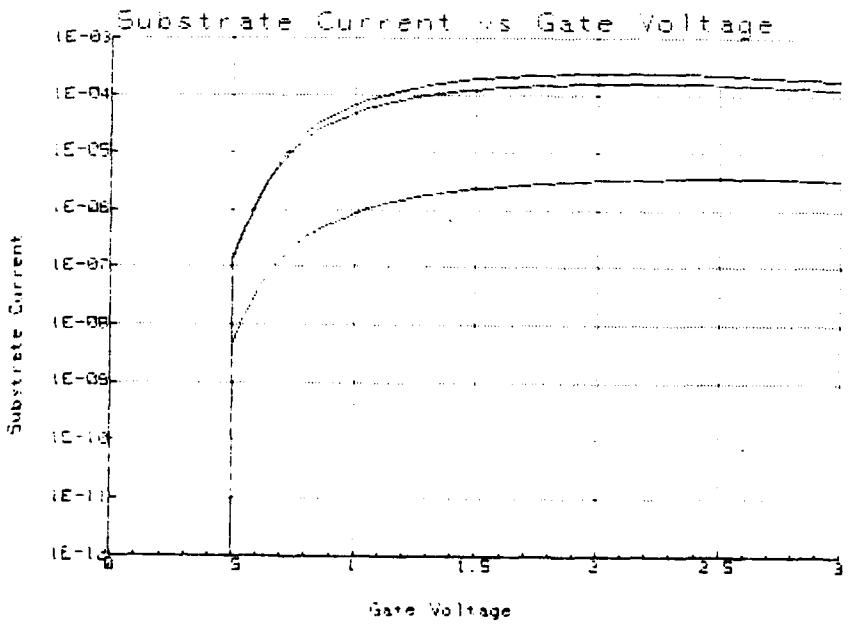

Figure 14. Substrate current vs. gate voltage for short N-channel FETs with Vds = 4.5 volts. W/L = 50/0.65, 50/0.9, 2.7/0.65 (microns).

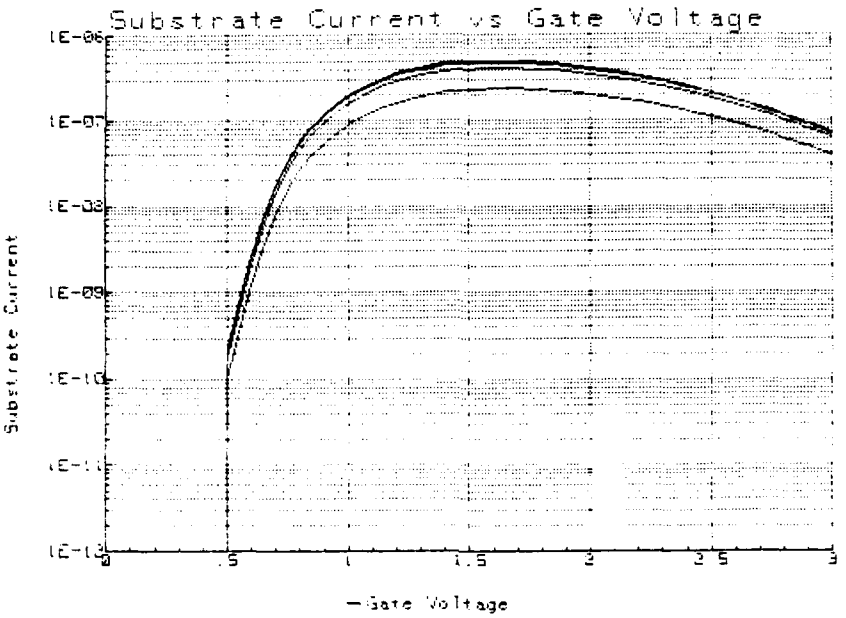

Figure 15. Substrate current vs. gate voltage for long P-channel FETs with Vds = -4.5 volts. W/L = 50/1.4, 50/1.6, 50/3.0, 50/10.0 (microns).

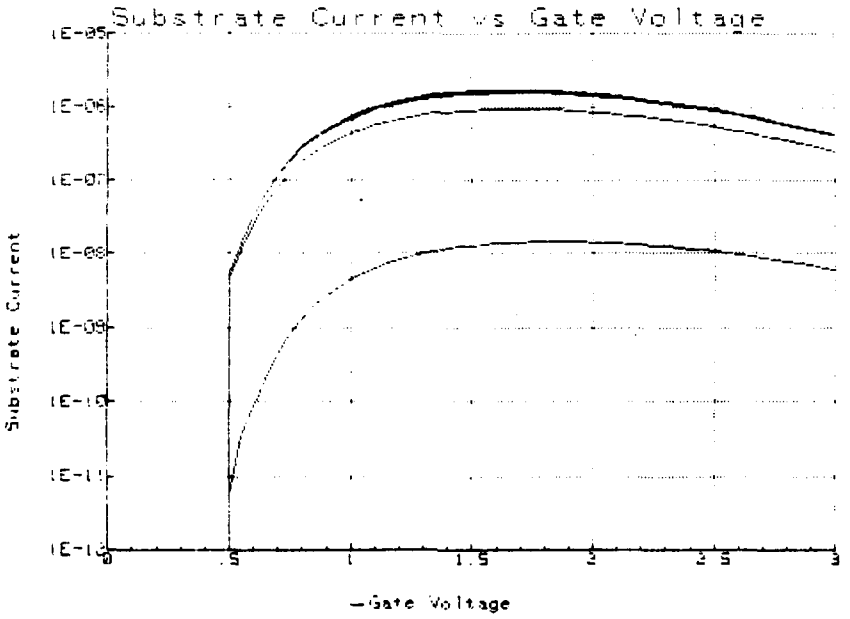

Figure 16. Substrate current vs. gate voltage for short P-channel FETs with Vds = -4.5 volts. W/L = 50/0.75, 50/0.9, 50/2.6, 2.7/0.65 (microns).

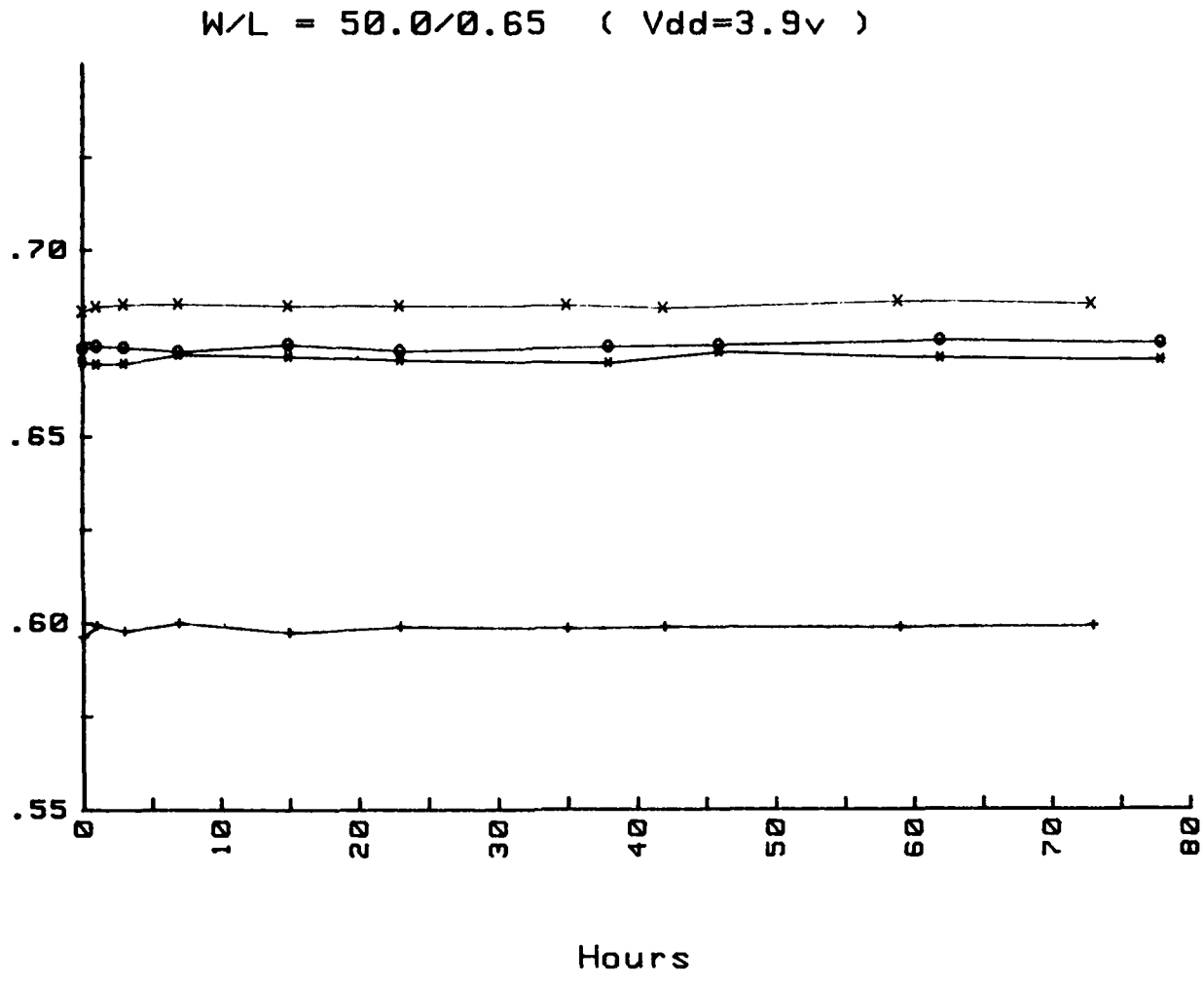

Figure 17. Threshold voltage vs. time for N-channel devices with W/L = 50/0.65 (microns) and Vd = 3.9 volts.

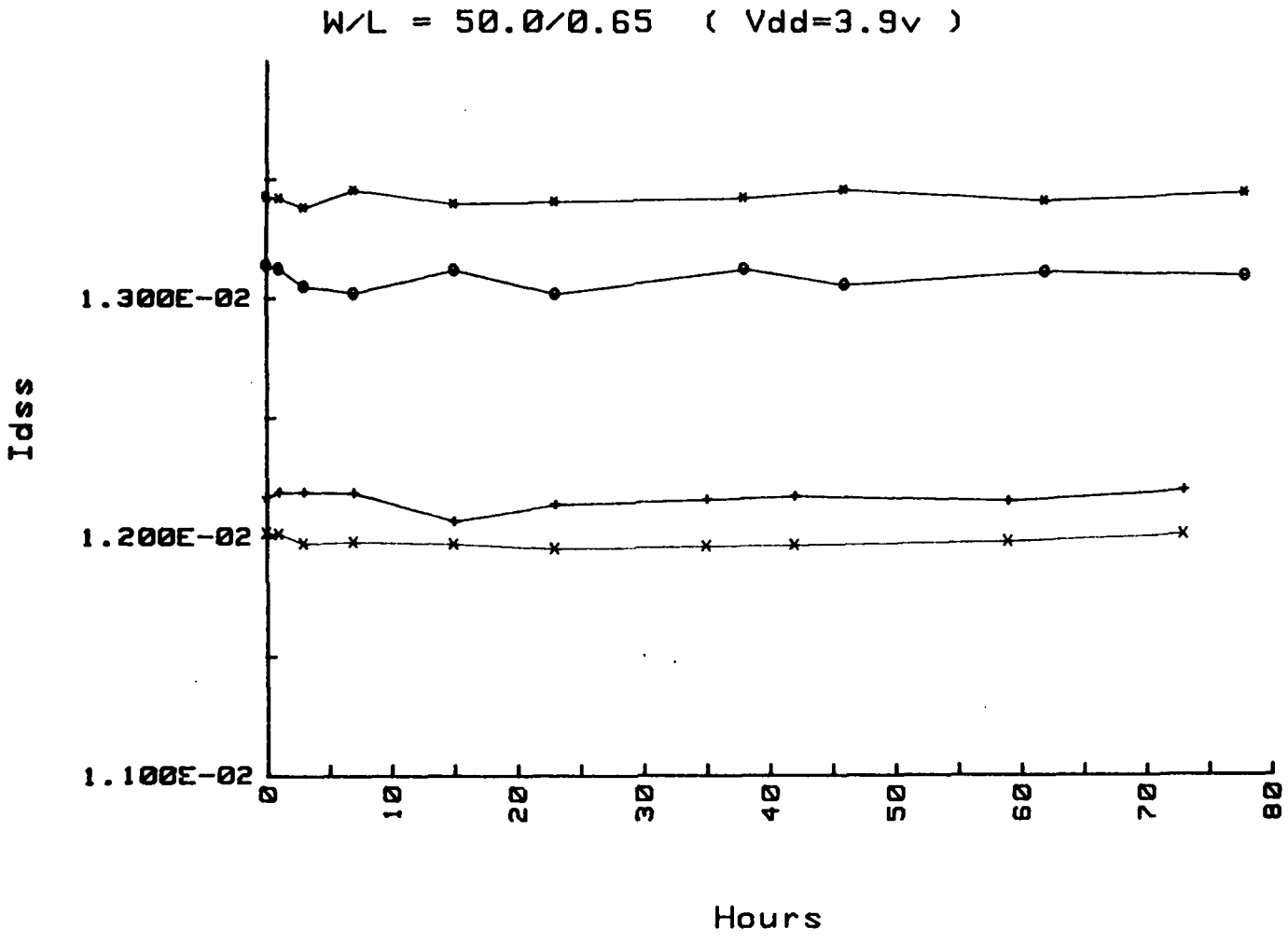

Figure 18. Saturation current vs. time for N-channel devices with W/L = 50/0.65 (microns) and Vd = 3.9 volts.

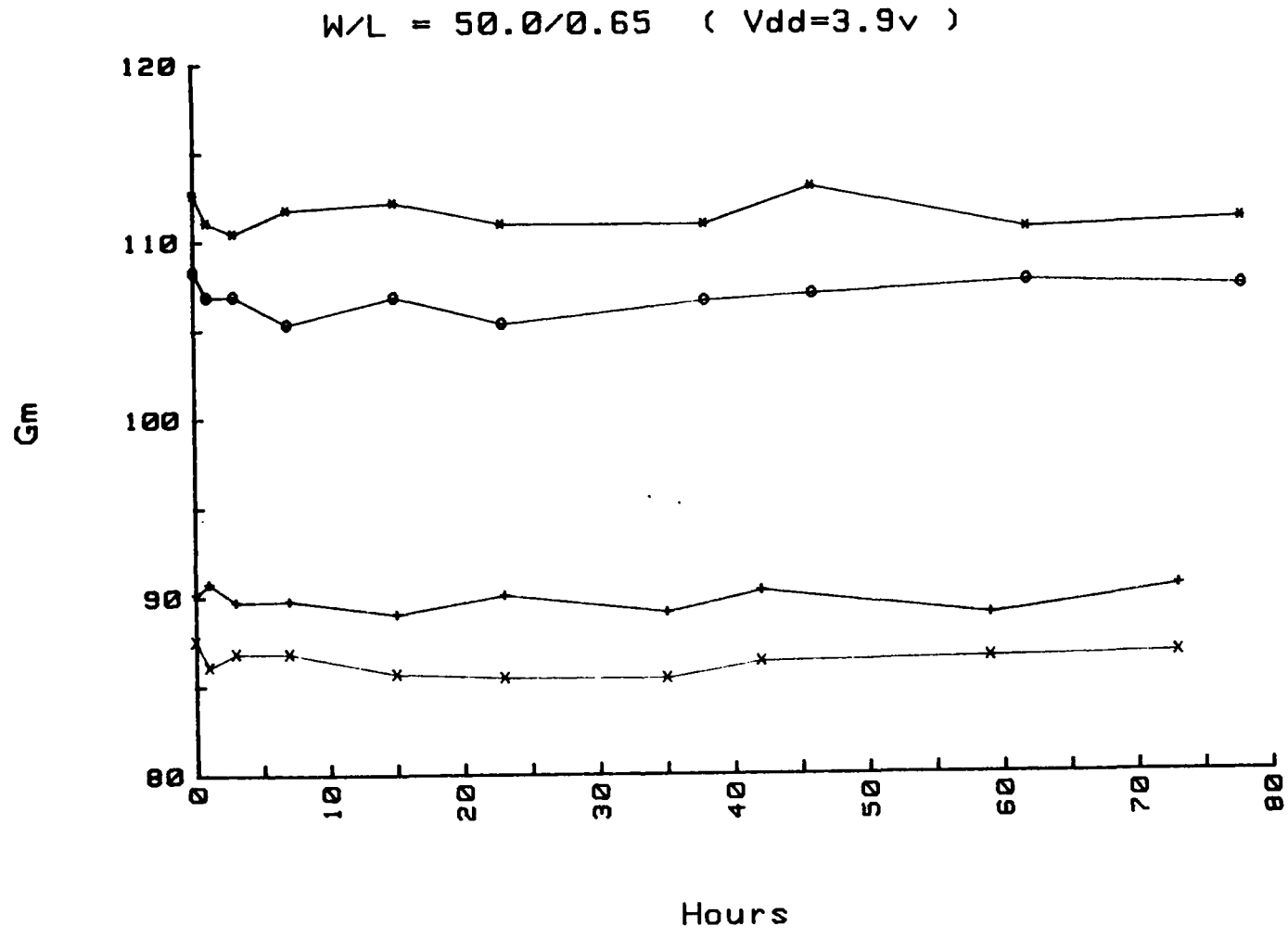

Figure 19. Transconductance vs. time for N-channel devices with W/L = 50/0.65 (microns) and Vd = 3.9 volts.

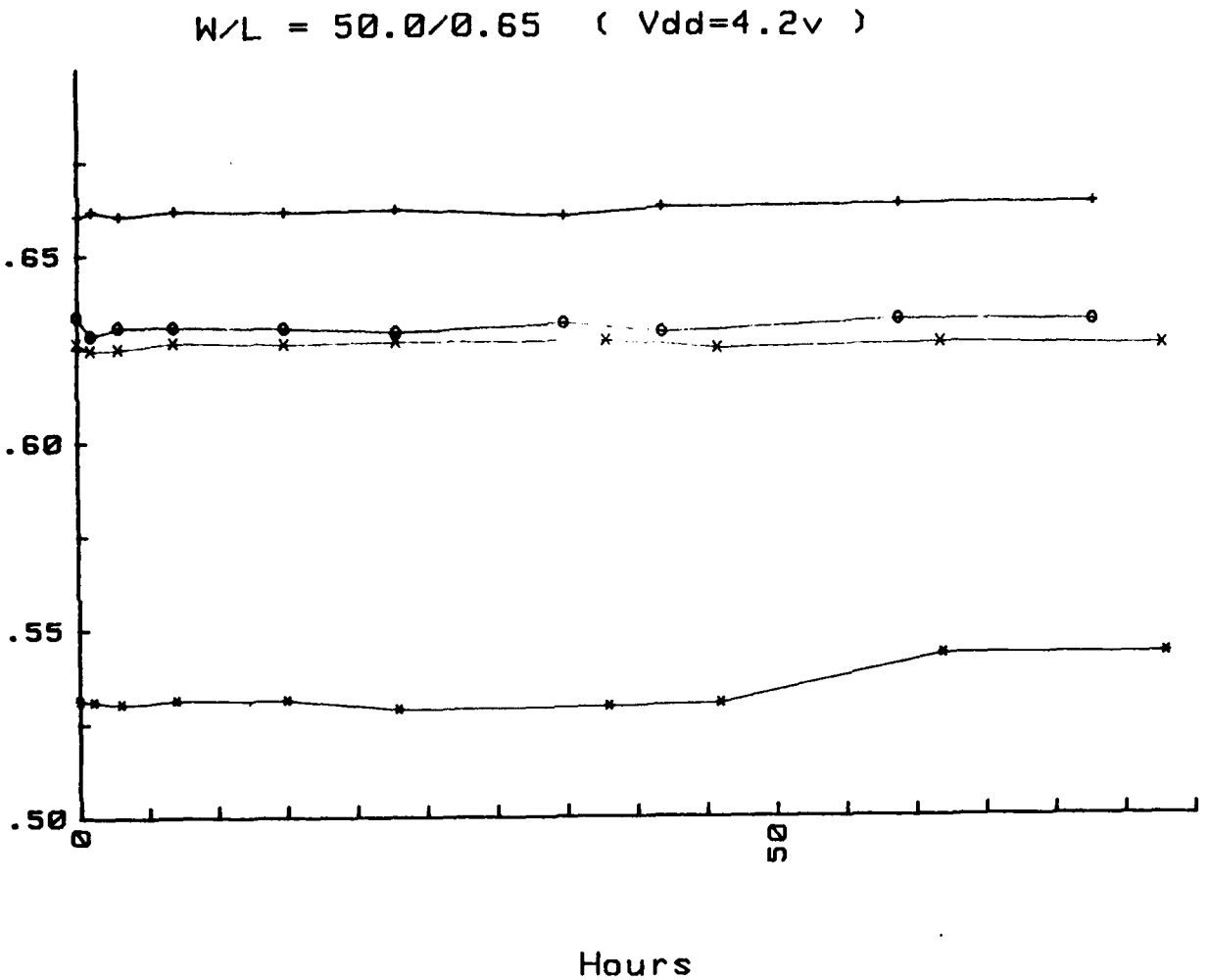

Figure 20. Threshold voltage vs. time for N-channel devices with W/L = 50/0.65 (microns) and Vd = 4.2 volts.

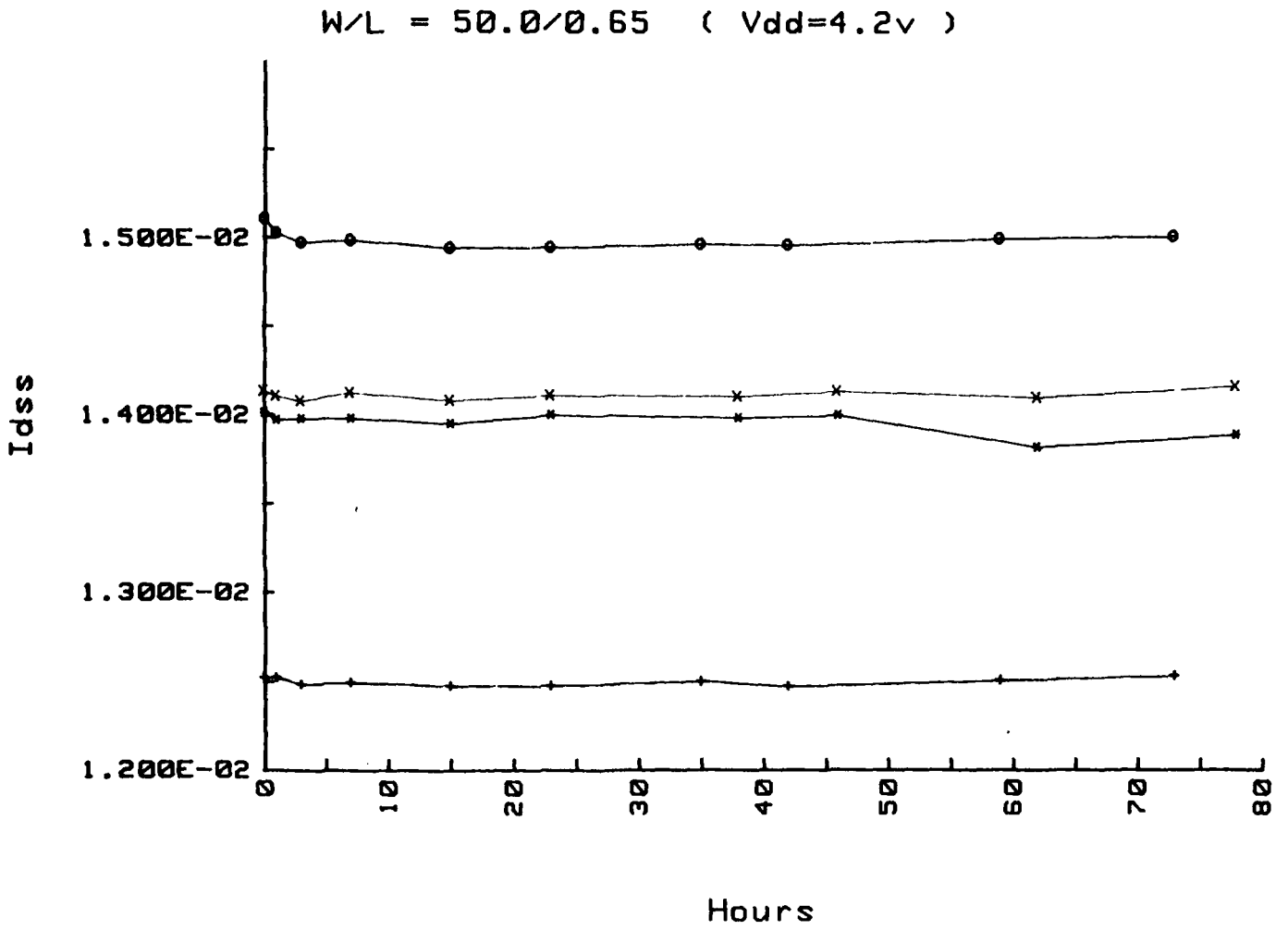

Figure 21. Saturation current vs. time for N-channel devices with W/L = 50/0.65 (microns) and Vd = 4.2 volts.

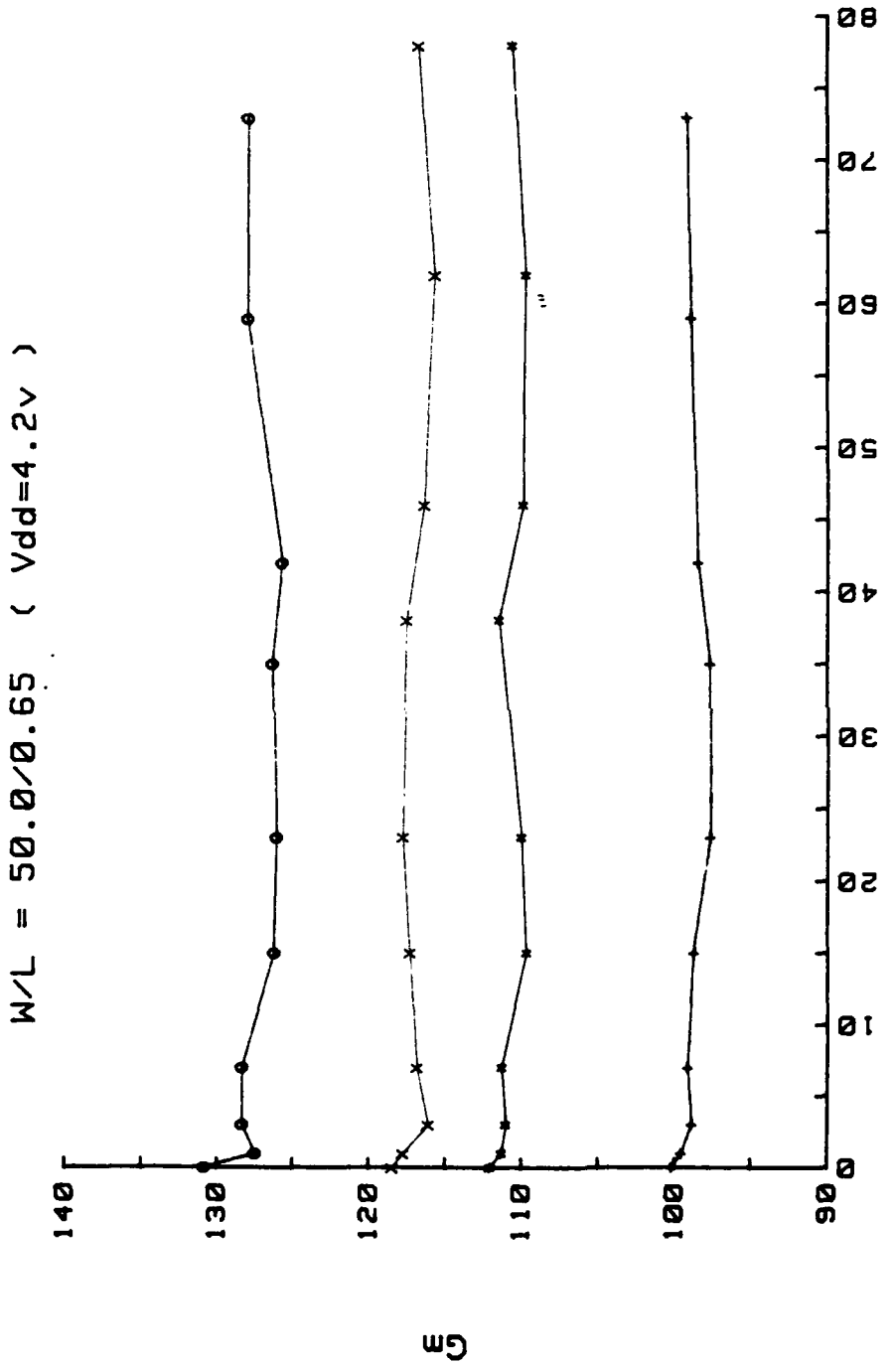

Figure 22. Transconductance vs. time for N-channel devices with W/L = 50/0.65 (microns) and Vd = 4.2 volts.

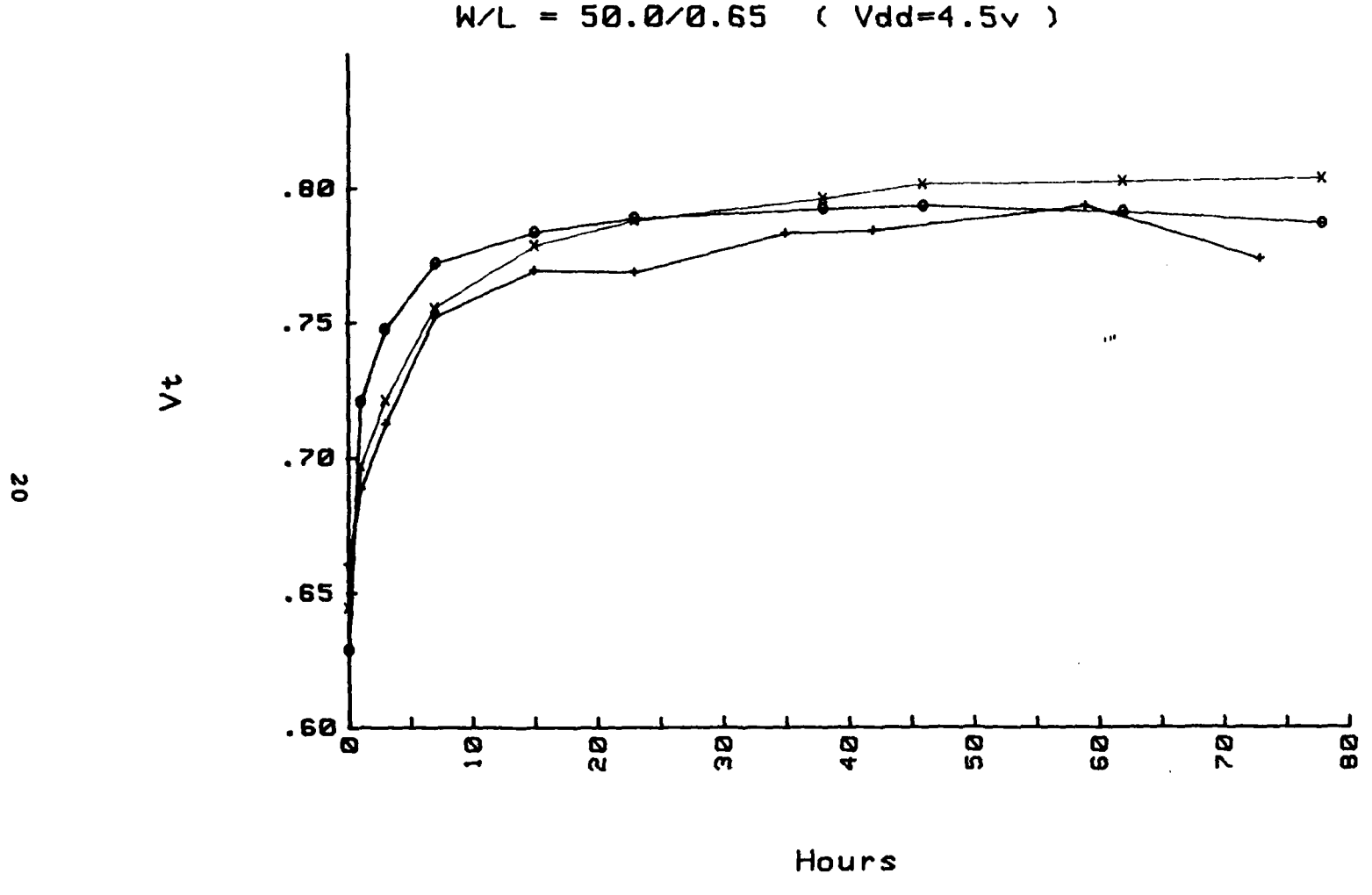

Figure 23. Threshold voltage vs. time for N-channel devices with W/L = 50/0.65 (microns) and Vd = 4.5 volts.

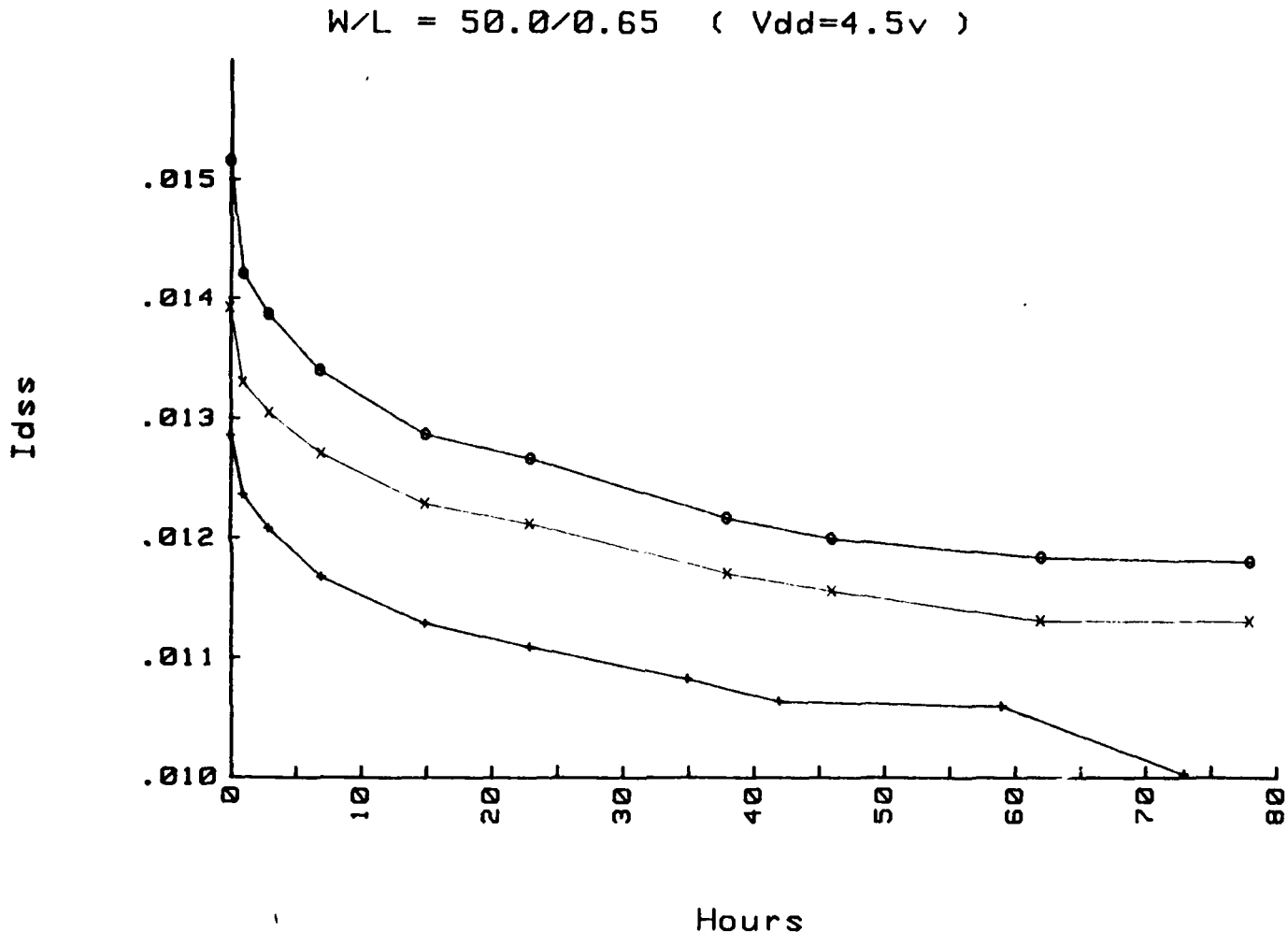

Figure 24. Saturation current vs. time for N-channel devices with W/L = 50/0.65 (microns) and Vd = 4.5 volts.

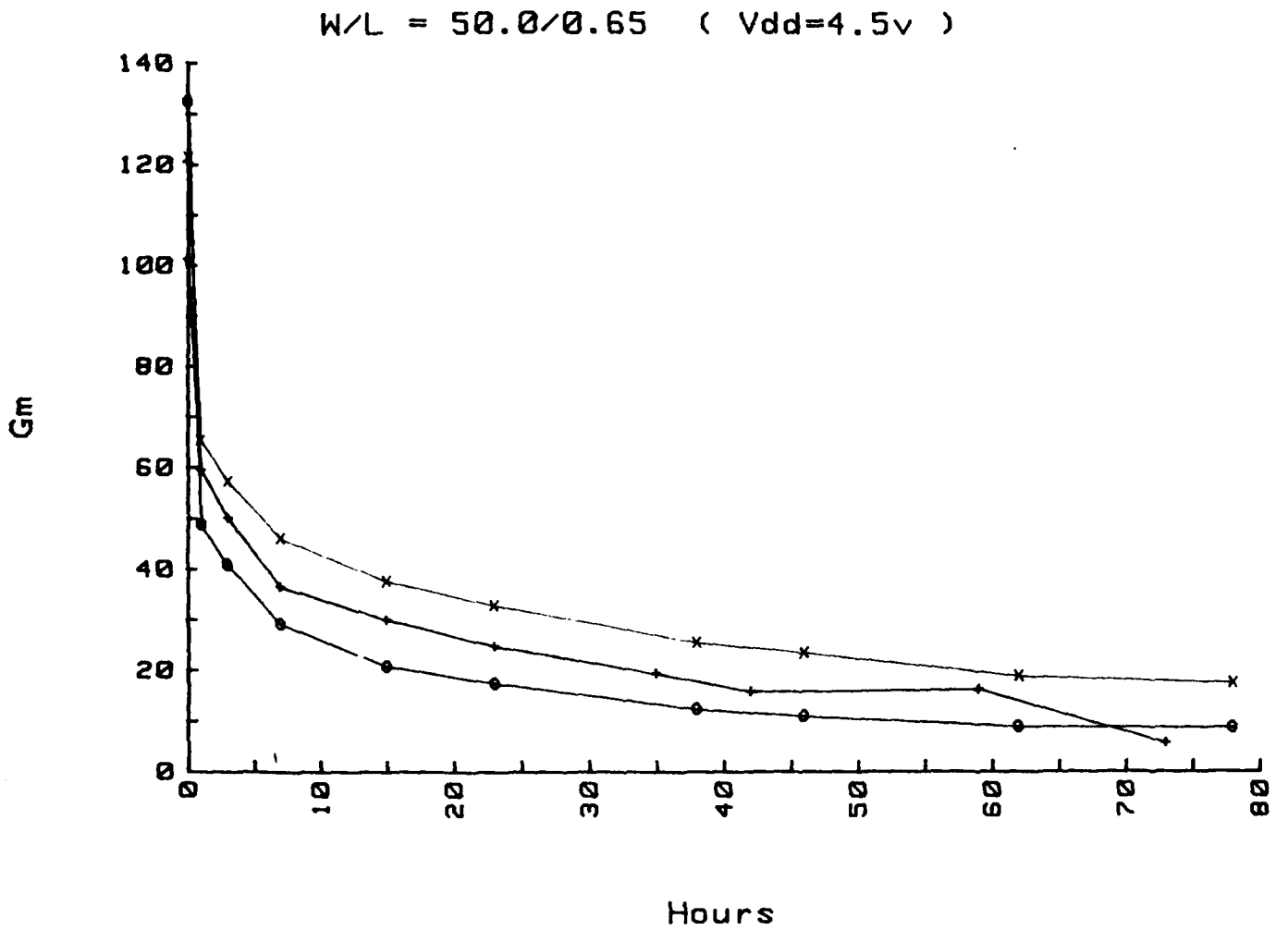

Figure 25. Transconductance vs. time for N-channel devices with W/L = 50/0.65 (microns) and Vd = 4.5 volts.

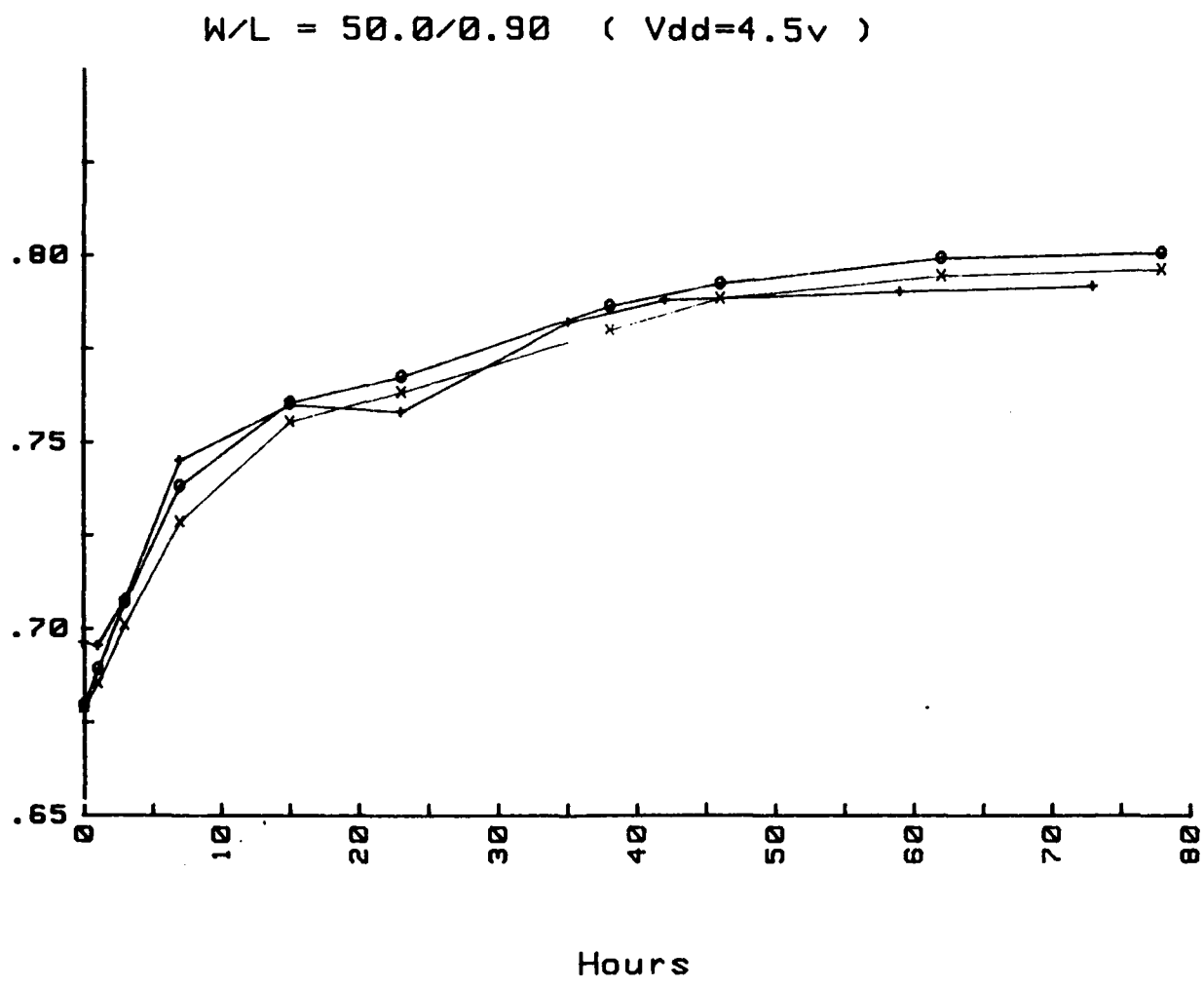

Figure 26. Threshold voltage vs. time for N-channel devices with W/L = 50/0.9 (microns) and Vd = 4.5 volts.

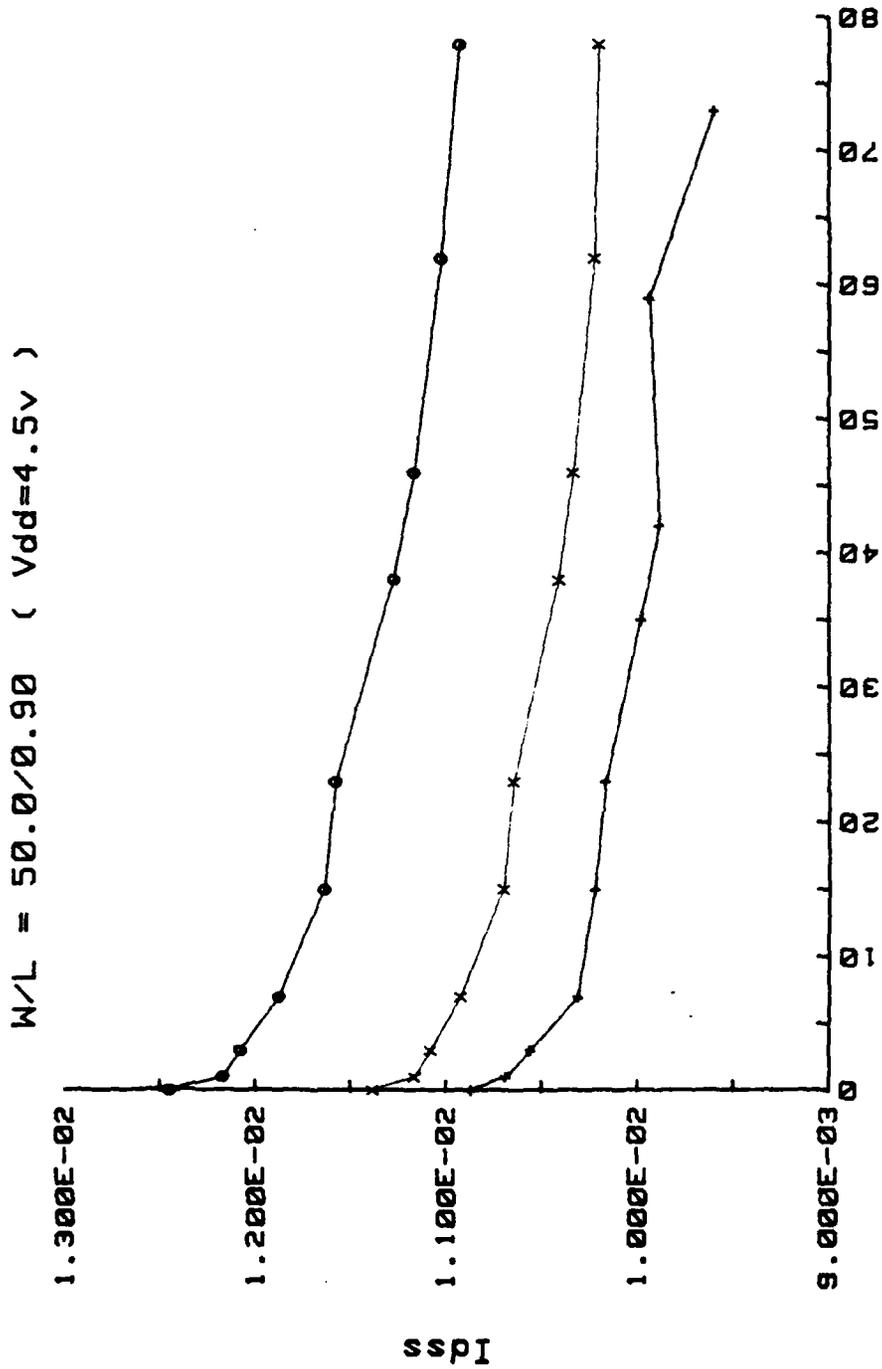

Figure 27. Saturation current vs. time for N-channel devices with W/L = 50/0.9 (microns) and Vd = 4.5 volts.

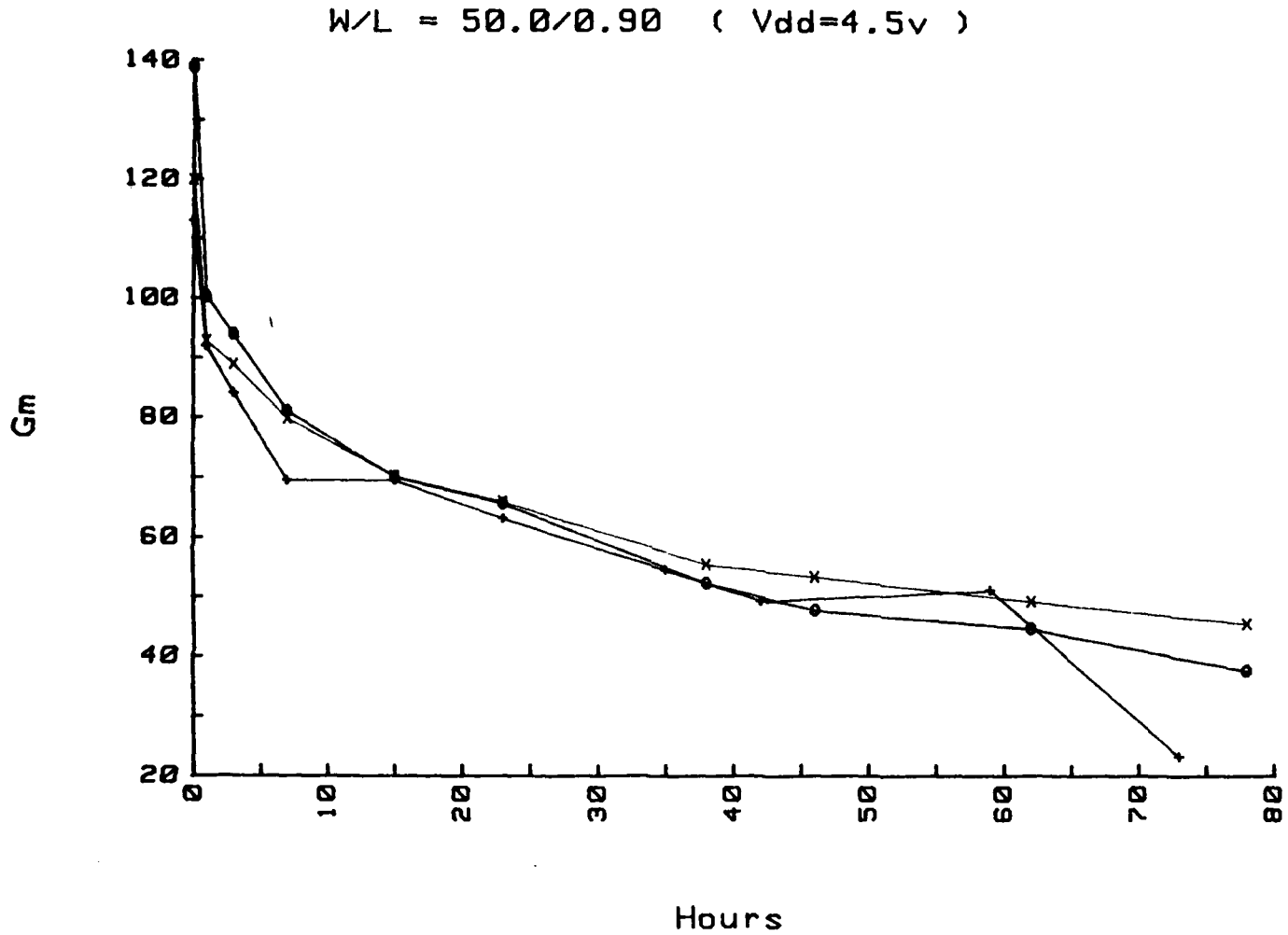

Figure 28. Transconductance vs. time for N-channel devices with W/L = 50/0.9 (microns) and Vd = 4.5 volts.

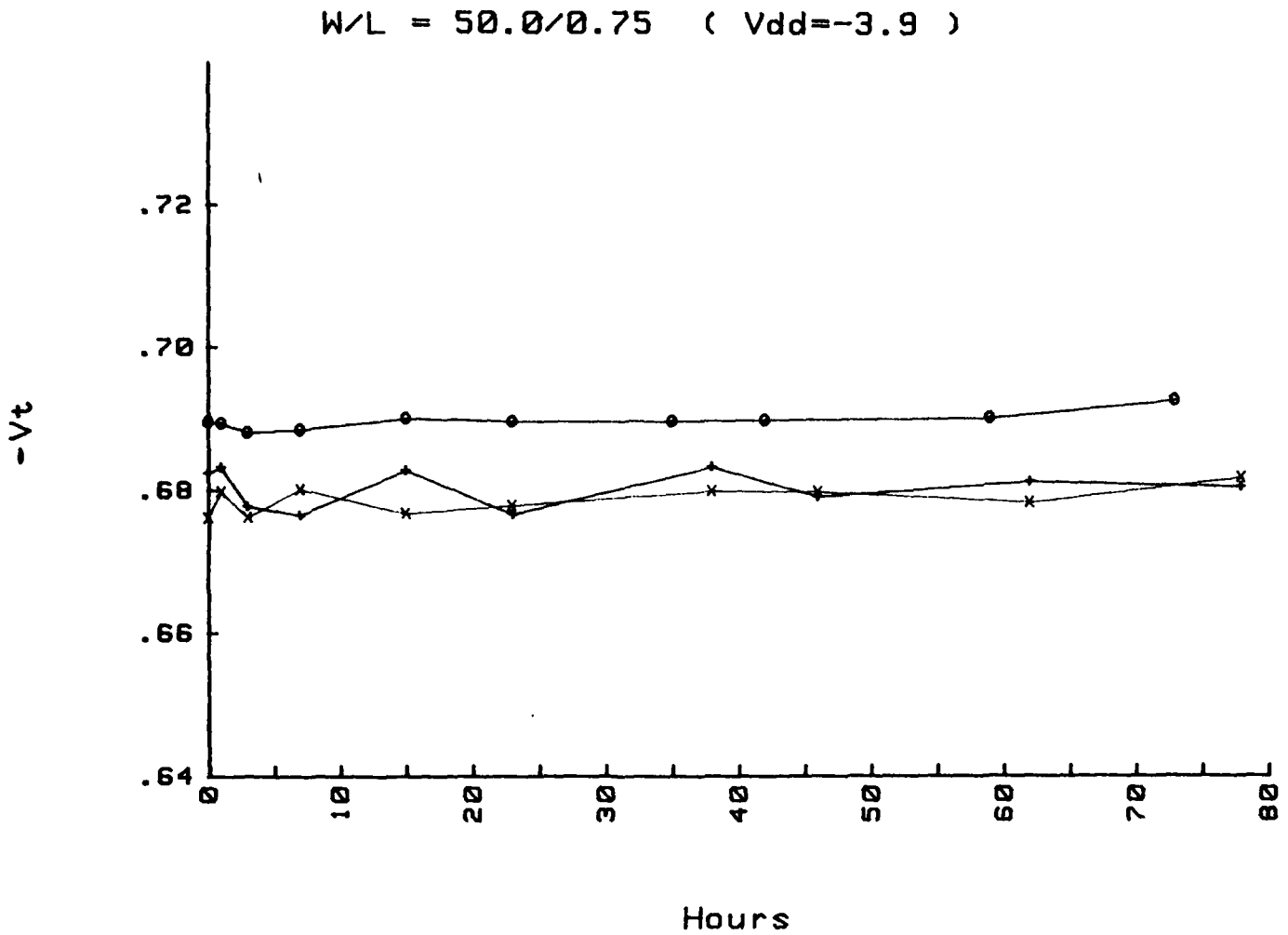

Figure 29. Threshold voltage vs. time for P-channel devices with W/L = 50/0.75 (microns) and Vd = -3.9 volts.

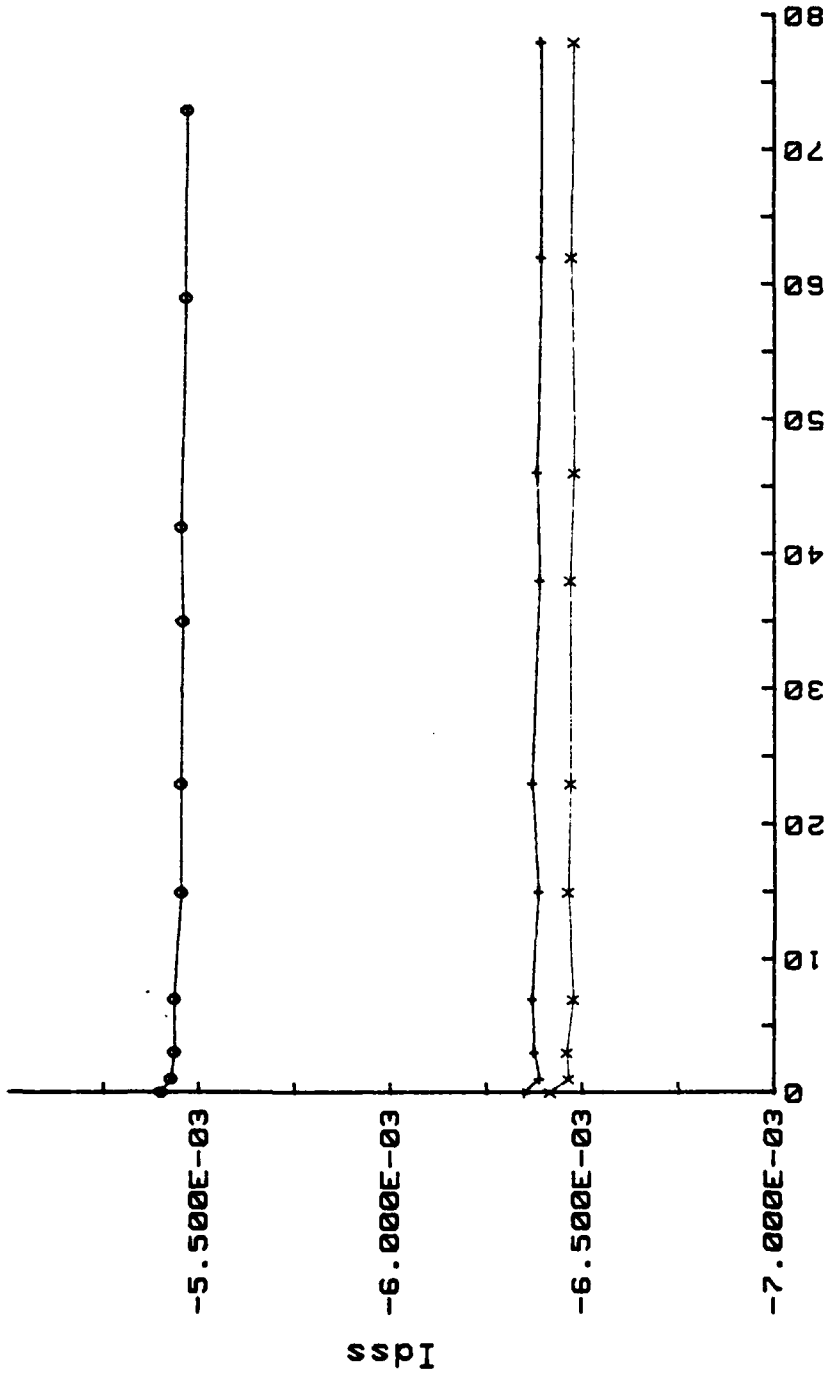

Figure 30. Saturation current vs. time for P-channel devices with W/L = 50/0.75 (microns) and Vd = -3.9 volts.

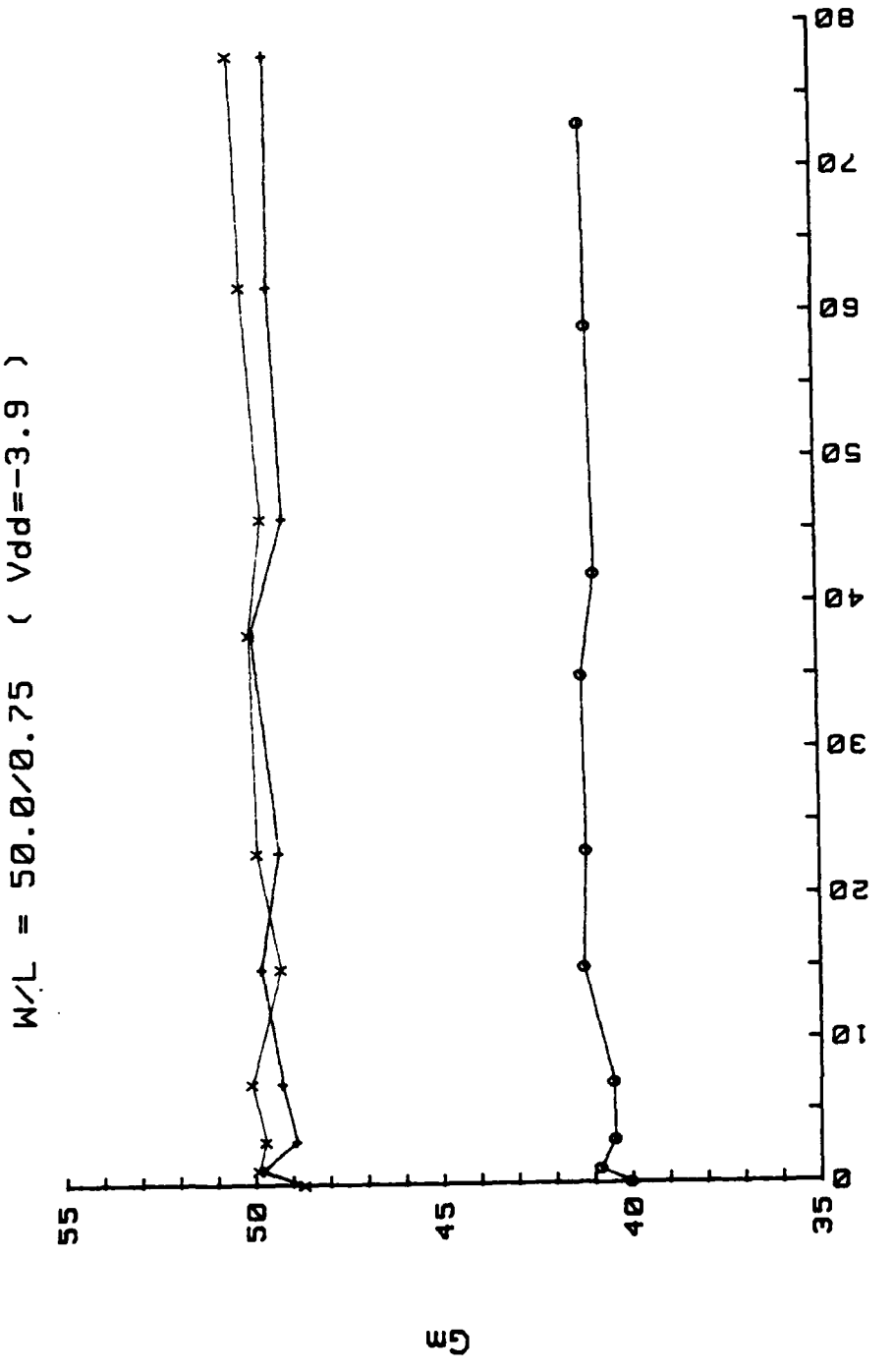

Figure 31. Transconductance vs. time for P-channel devices with W/L = 50/0.75 (microns) and Vd = -3.9 volts.

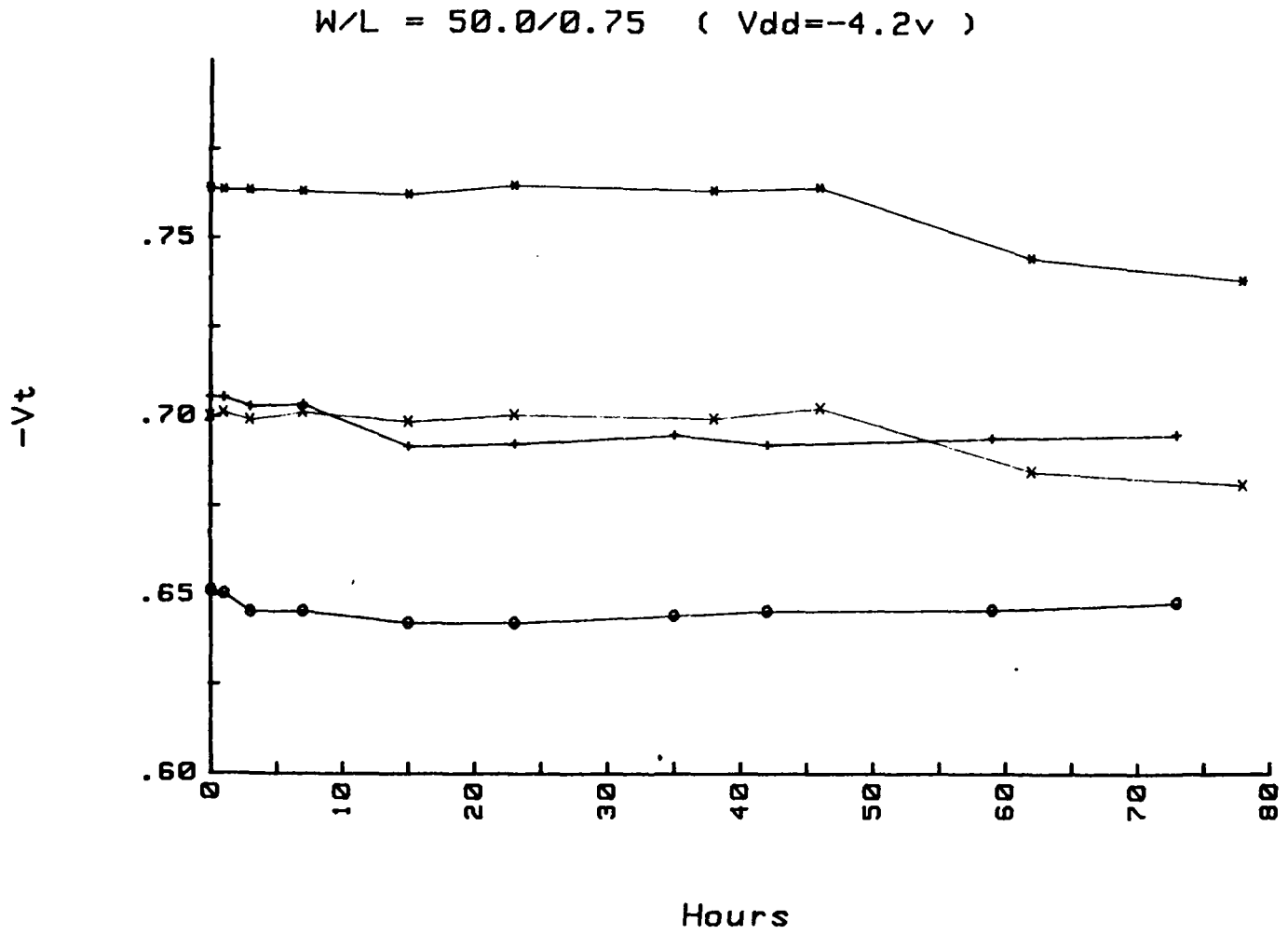

Figure 32. Threshold voltage vs. time for P-channel devices with W/L = 50/0.75 (microns) and Vd = -4.2 volts.

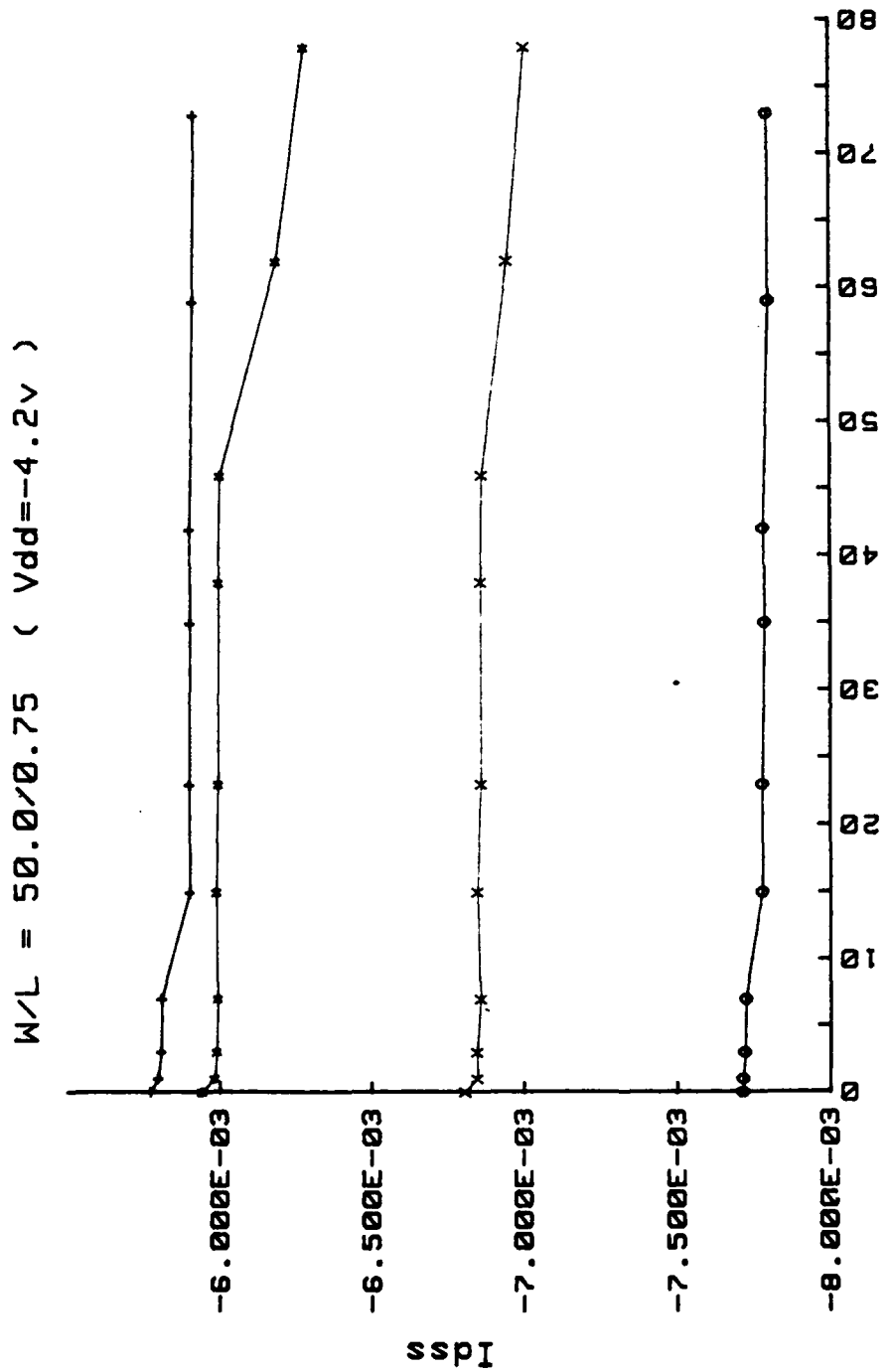

Figure 33. Saturation current vs. time for P-channel devices with W/L = 50/0.75 (microns) and Vd = -4.2 volts.

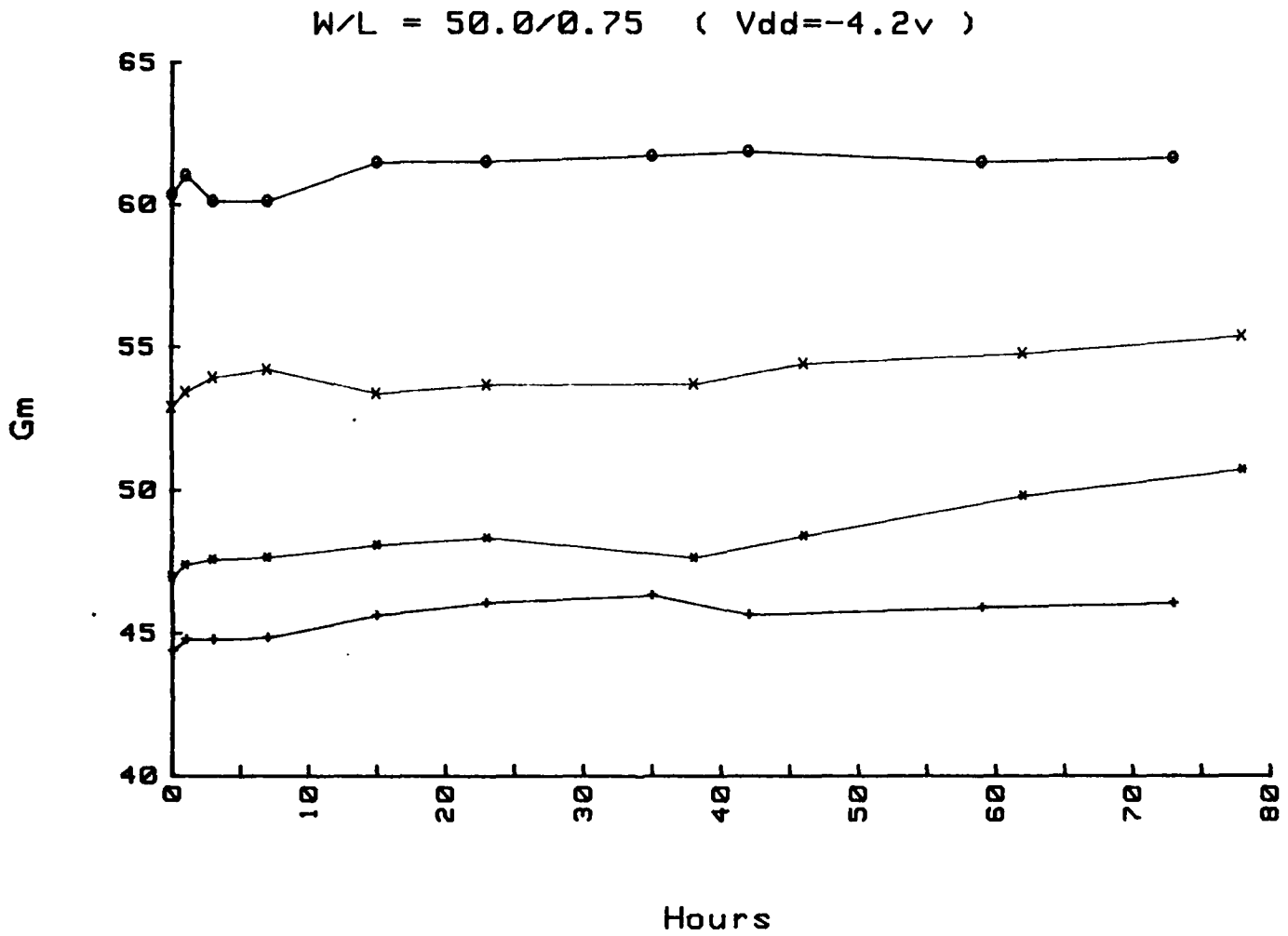

Figure 34. Transconductance vs. time for P-channel devices with W/L = 50/0.75 (microns) and Vd = -4.2 volts.

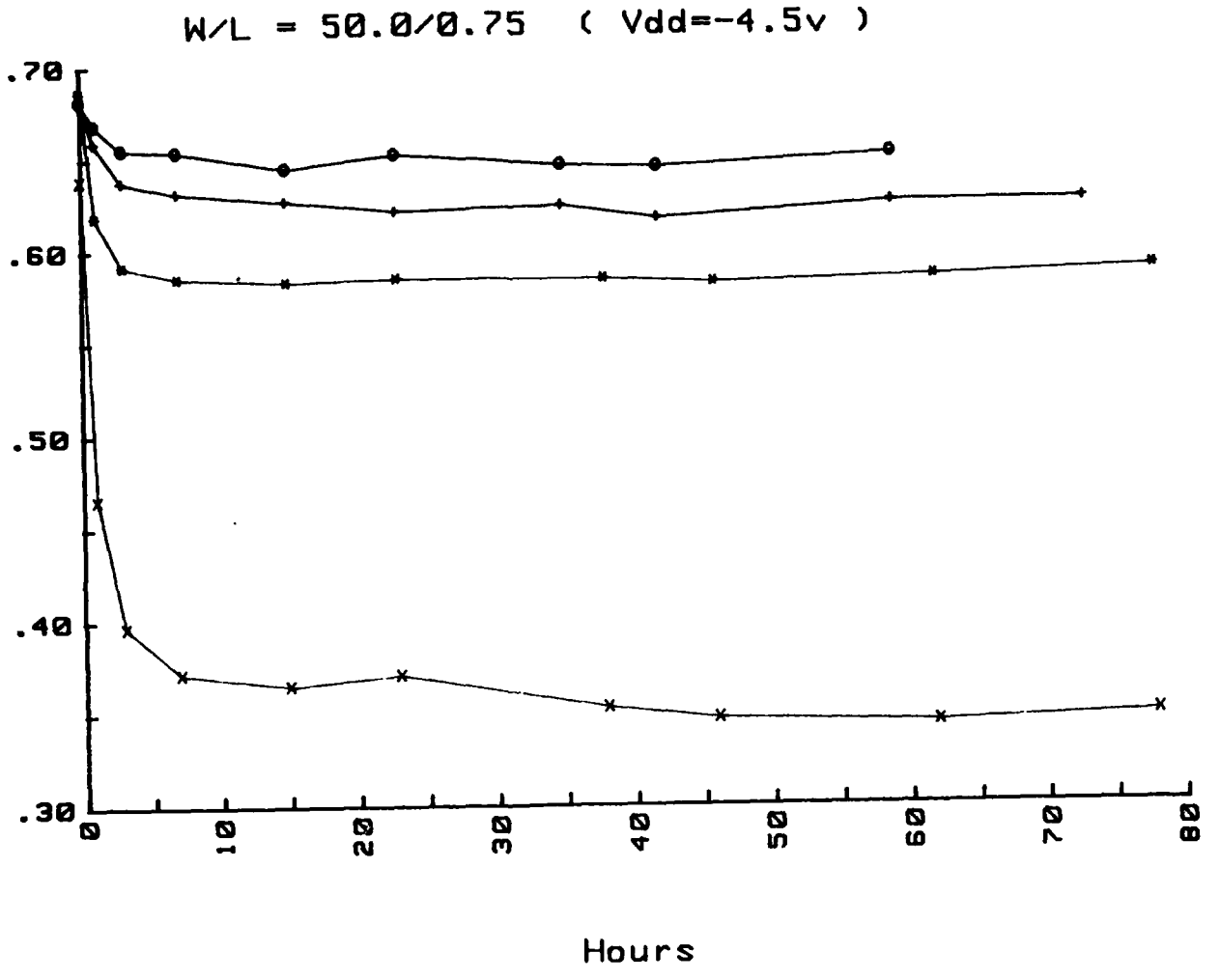

Figure 35. Threshold voltage vs. time for P-channel devices, with W/L = 50/0.75 (microns) and Vd = -4.5 volts.

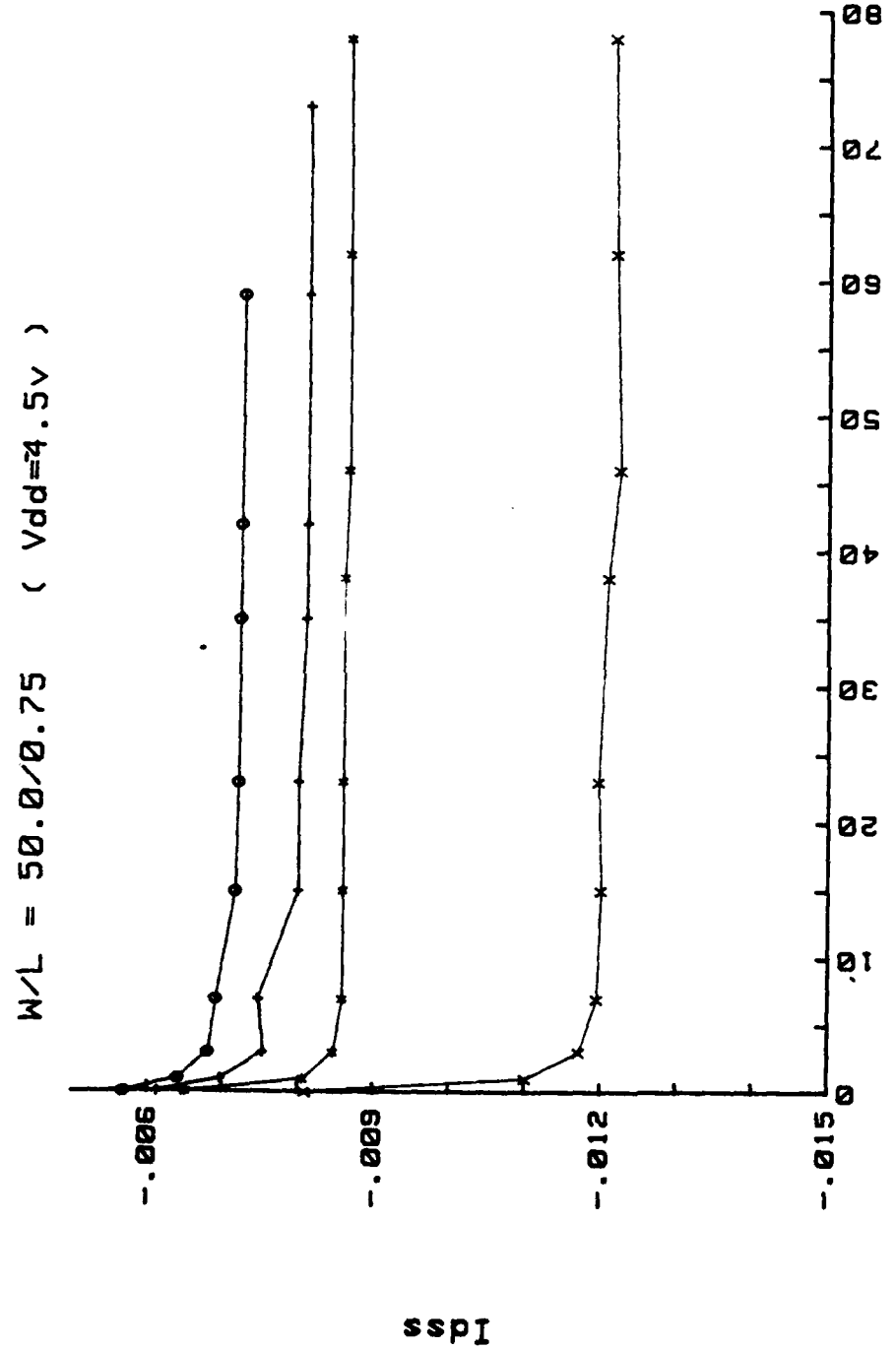

Figure 36. Saturation current vs. time for P-channel devices with W/L = 50/0.75 (microns) and Vd = -4.5 volts.

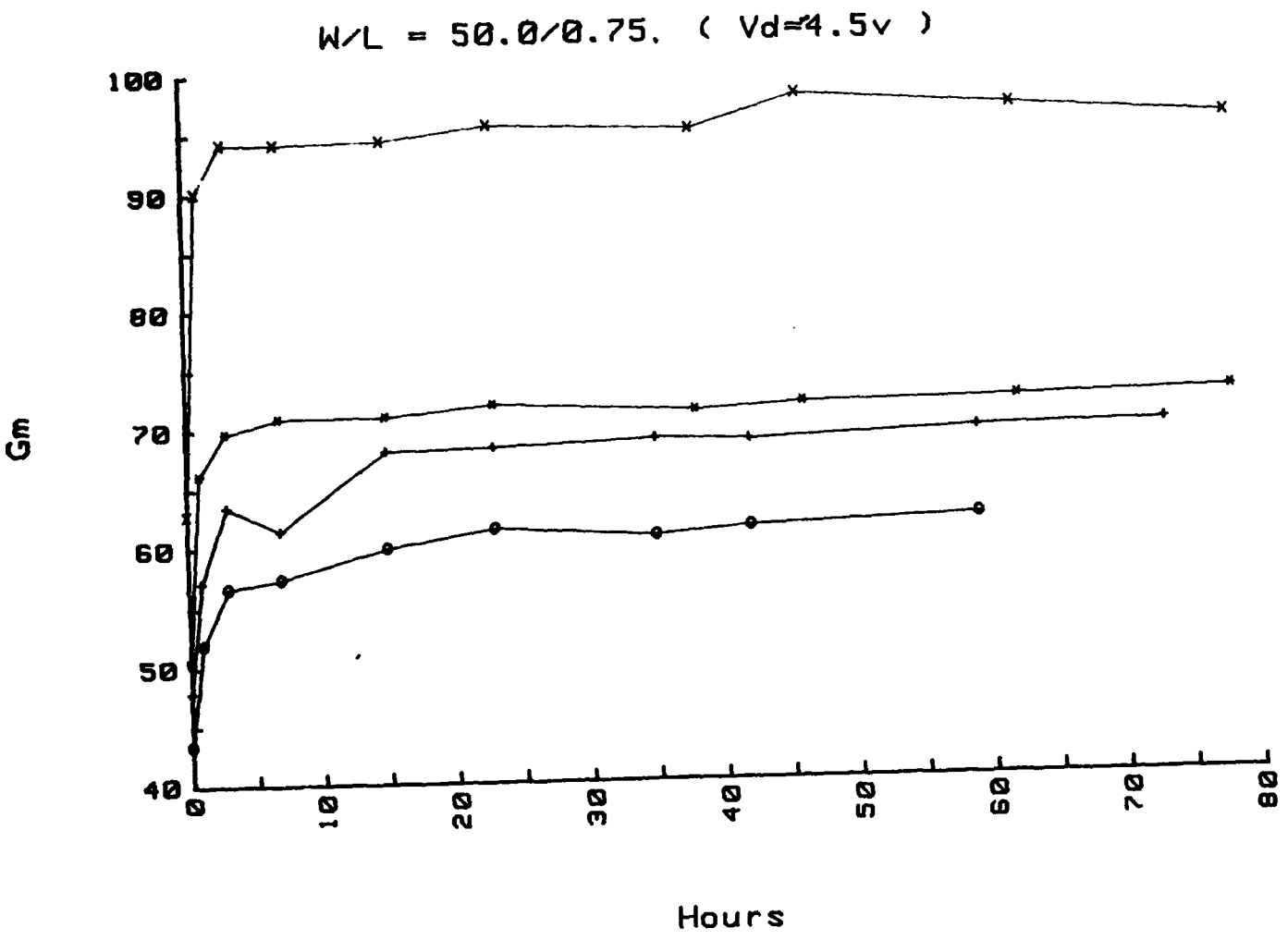

Figure 37. Transconductance vs. time for P-channel devices with W/L = 50/0.75 (microns) and Vd = -4.5 volts.

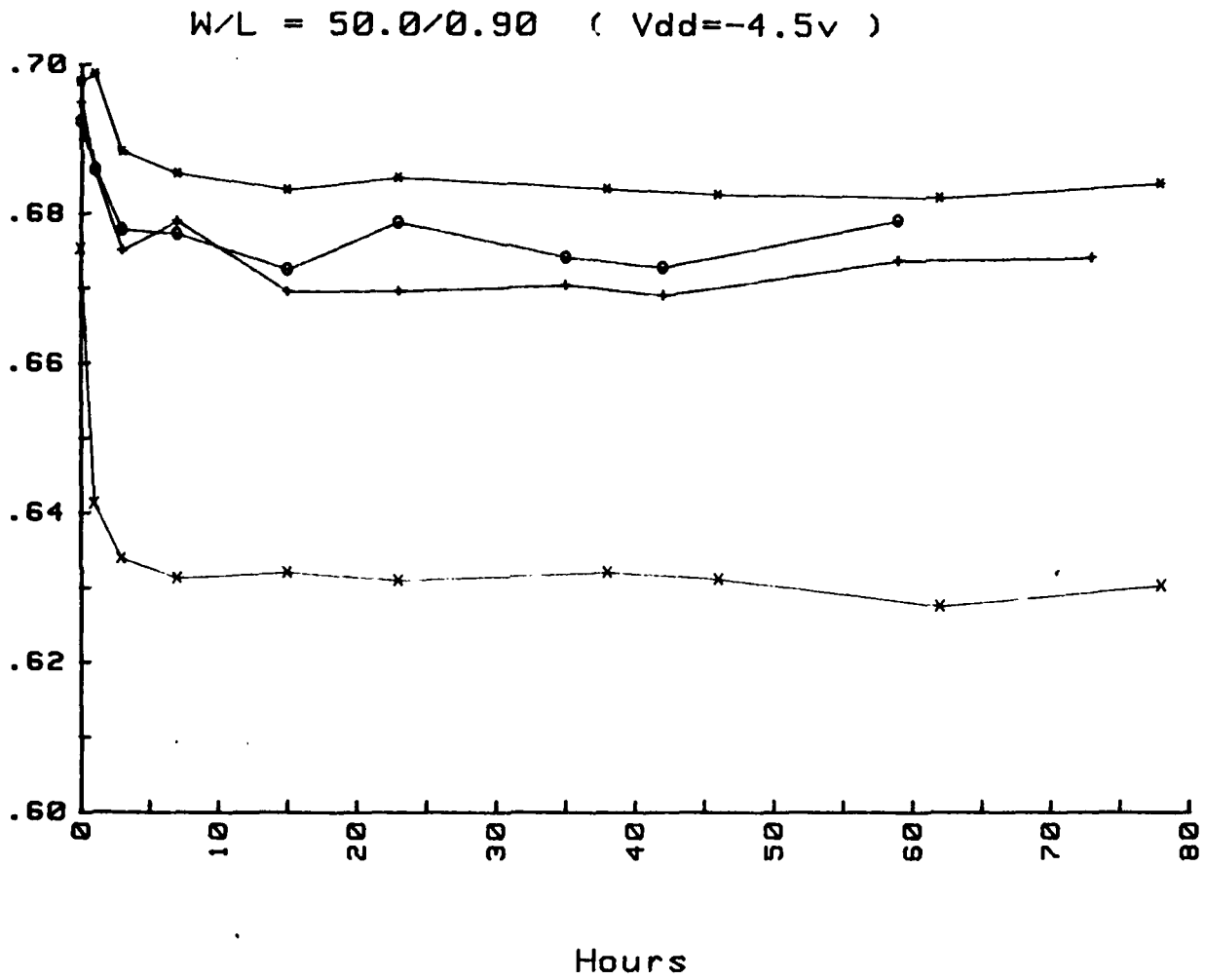

Figure 38. Threshold voltage vs. time for P-channel devices with W/L = 50/0.9 (microns) and Vd = -4.5 volts.

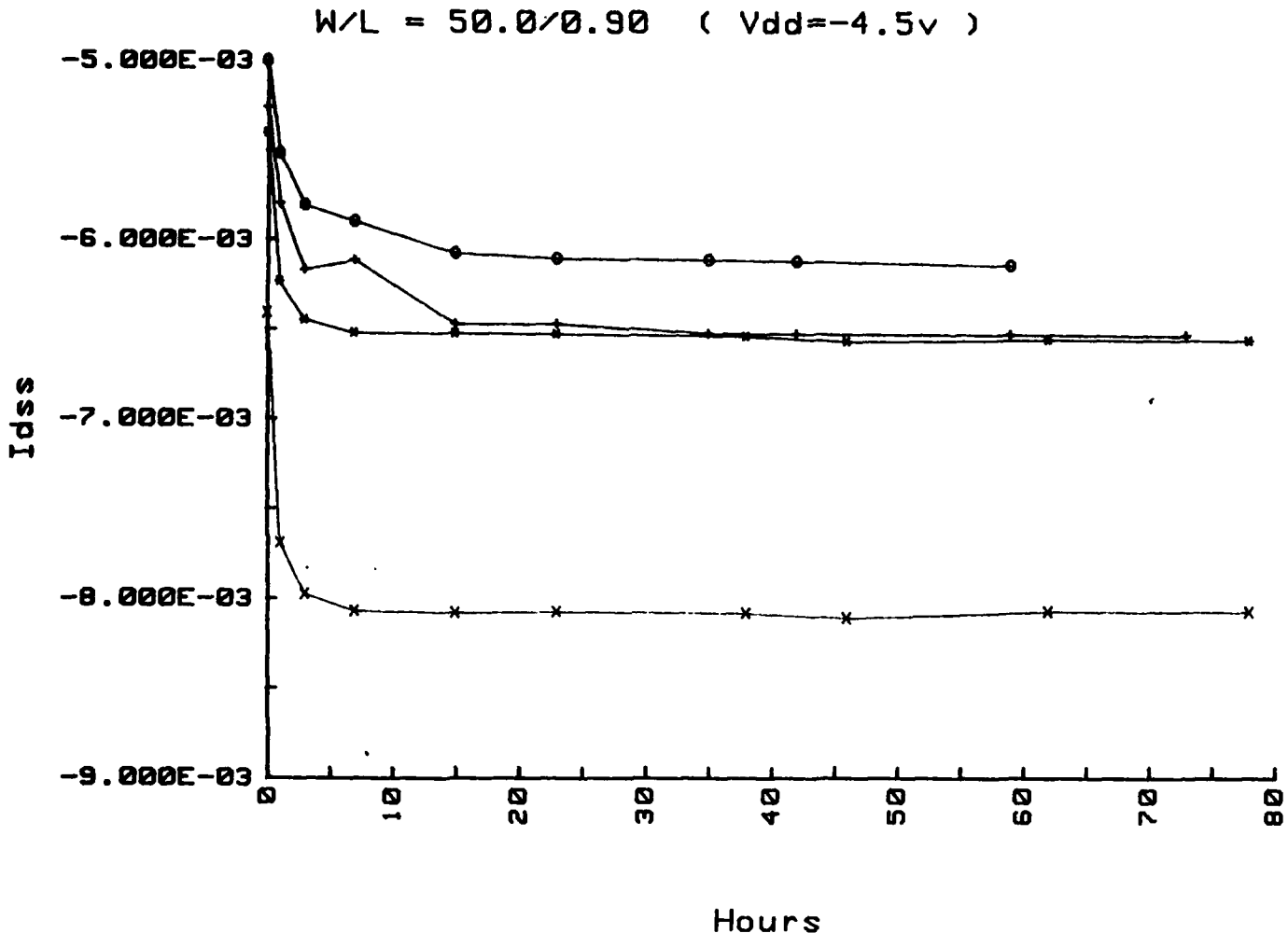

Figure 39. Saturation current vs. time for P-channel devices with W/L = 50/0.9 (microns) and Vd = -4.5 volts.

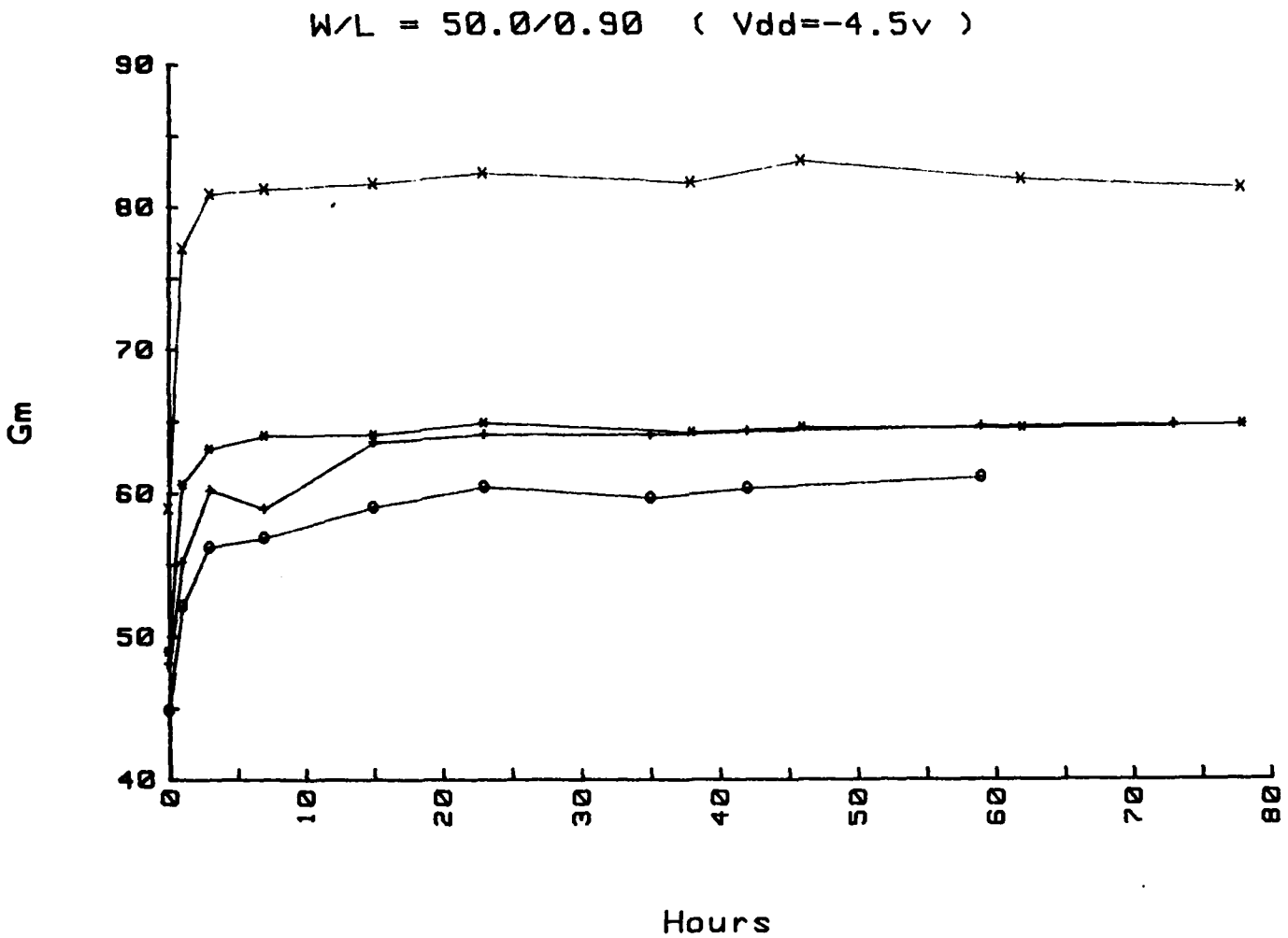

Figure 40. Transconductance vs. time for P-channel devices with W/L = 50/0.9 (microns) and Vd = -4.5 volts.

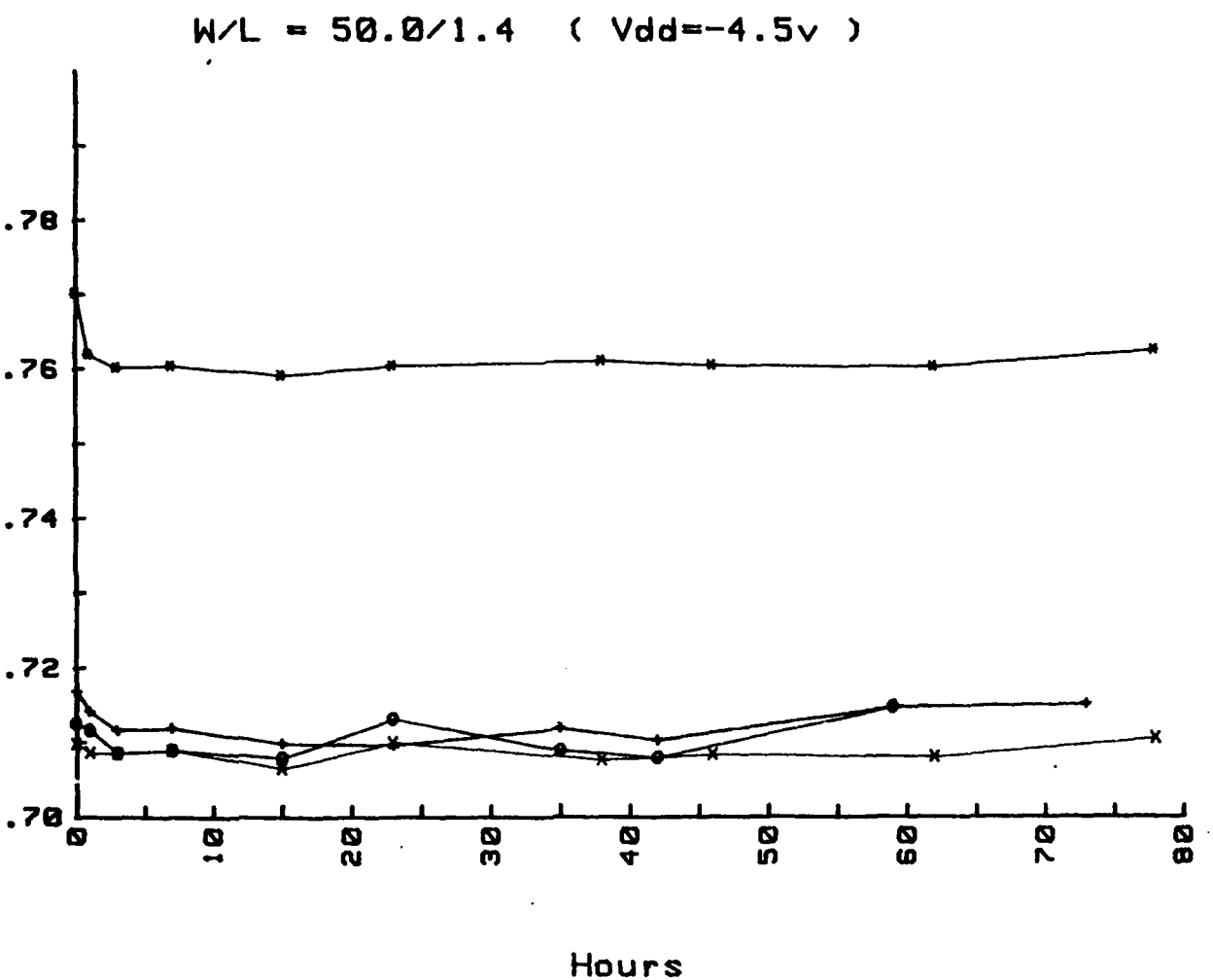

Figure 41. Threshold voltage vs. time for P-channel devices with W/L = 50/1.4 (microns) and Vd = -4.5 volts.

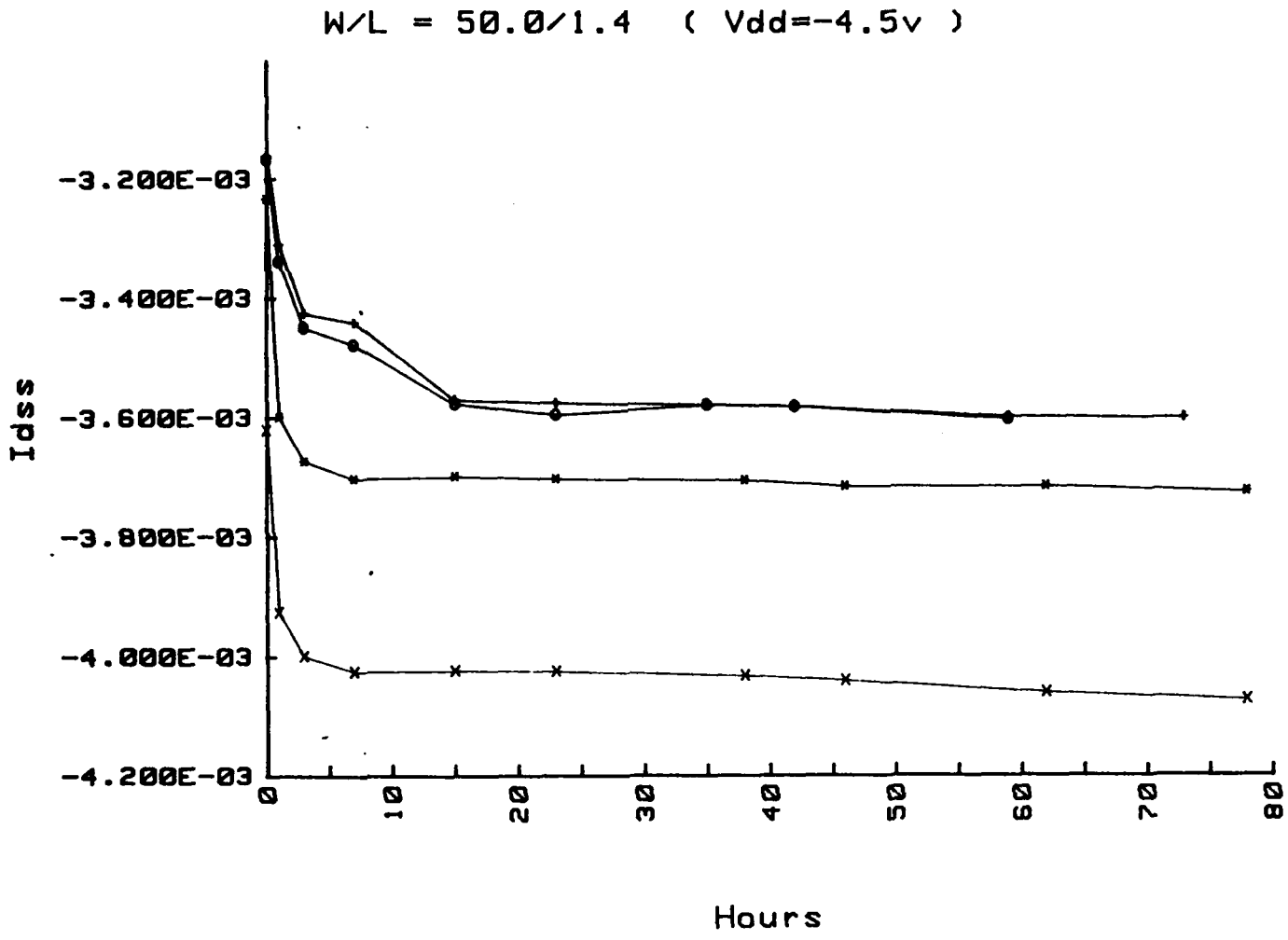

Figure 42. Saturation current vs. time for P-channel devices with W/L = 50/1.4 (microns) and Vd = -4.5 volts.

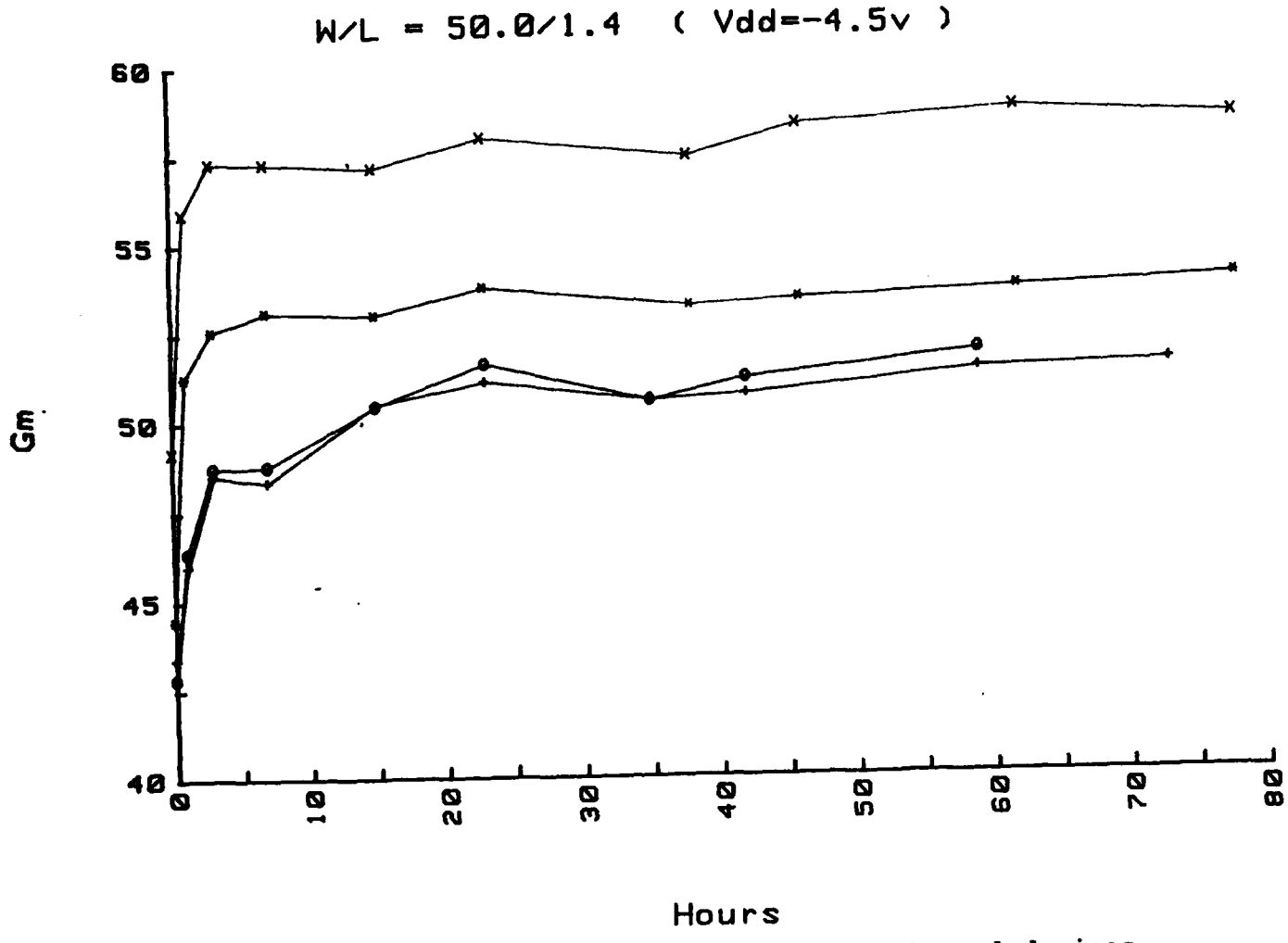

Figure 43. Transconductance vs. time for P-channel devices with W/L = 50/1.4 (microns) and Vd = -4.5 volts.

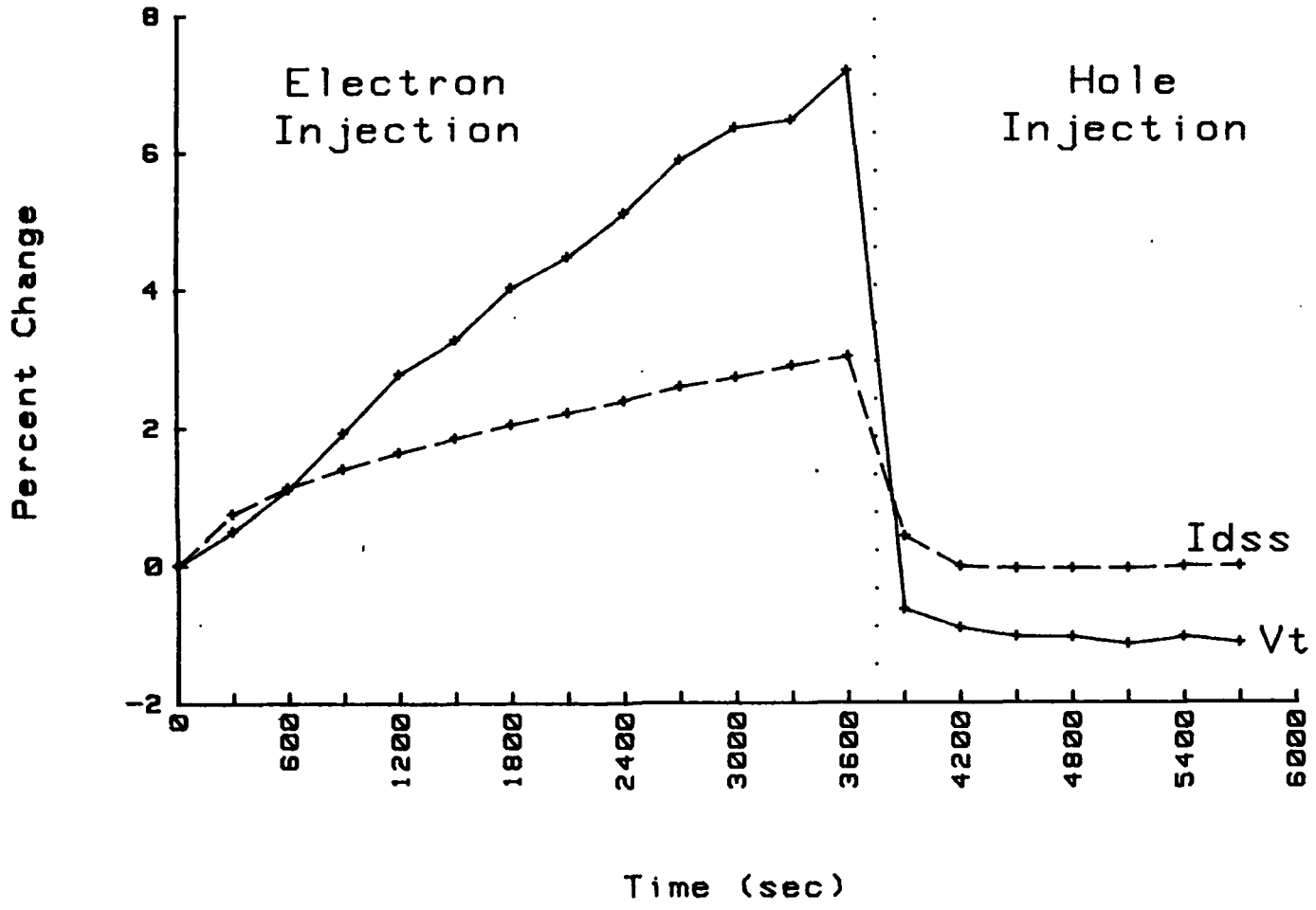

Figure 44. Threshold voltage and saturation current shift for electron injection and subsequent recovery for hole injection.

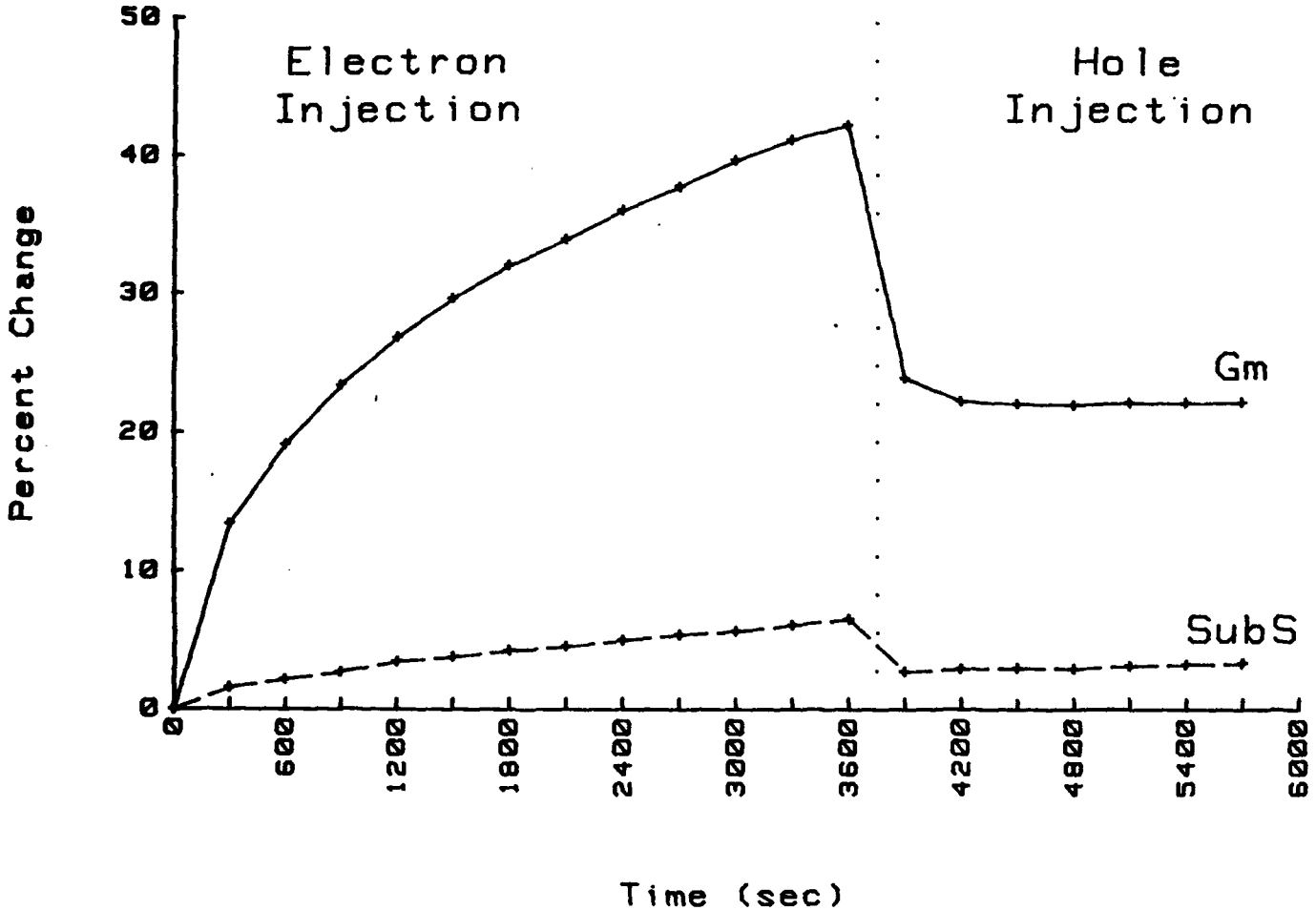

Figure 45. Subthreshold swing and transconductance shift for electron injection and subsequent partial recovery for hole injection.

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