BACK-CONTACT VERTICAL-JUNCTION SOLAR CELL

THESIS

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THESIS

Presented to the Faculty of the School of Engineering

of the Air Force Institute of Technology

In Partial Fullfillment of the

Requirements for the Degree of

Master of Science in Electrical Engineering

M. Wayne Carver

Captain, USAF

March 1988

Preface

In a flourishing country like the United States, people often take for granted the most important necessities of life. The dependence this country has on energy is no exception. I can remember as a teenager in 1974 waiting in gas lines for 4 hours. It was then that my interest in using the sun as an alternative source of energy was aroused. Solar cells were of special interest, for I felt they were the answer to our dependence on foreign energy sources. Improving the efficiency of the solar cell has since been a dream of mine.

This thesis attempted to improve the efficiency of the silicon solar cell by combining two of the most efficient solar cell concepts. They are the vertical-junction solar cell and the interdigitated back-contact solar cell.

I would like to thank Major Edward S. Kolesar for his enthusiastic support in this effort. His guidance, knowledge, and encouragement were greatly appreciated. I would also like to thank my committee members Major Donald Kitchen, Dr. Yeo, and Mr. Joseph Wise for their help and support. I am grateful to Don Smith and Bill Trop for their laboratory assistance during the fabrication of the solar cells. I am also grateful to Dave Via and Geoffrey Trammel at the Avionics Laboratory for their assistance in cutting Rubylith.

I am especially thankful for the love and support of my wife, Gina, and her help in typing this thesis. I am also thankful for the patience and understanding of my two daughters, Angie and Lauren, who gave up playing with Daddy so he could work on his thesis.

Most of all I thank God, who made all things, for allowing me to work and live in His magnificent creation.

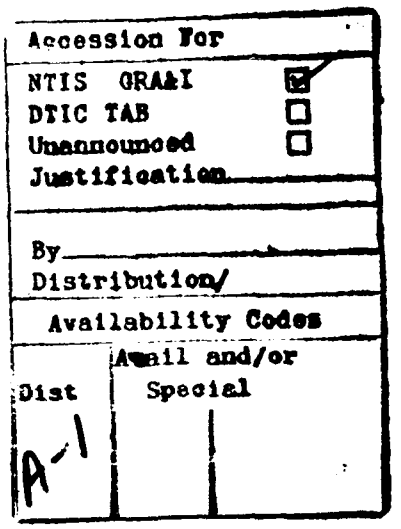


Table of Contents

List of Figures

List of Tables

Abstract

The objective of this thesis was to improve the efficiency of silicon solar cells by designing and fabricating a solar cell which synergistically combines the advantages of the interdigitated back-contact solar cell with the advantages of the wedged-channel vertical-junction solar cell. Solar cell designs which combine the two concepts were proposed and evaluated. A final design was chosen which consisted of vertical grooves anisotropically etched from the frontside to the backside of a (110) oriented silicon wafer. The groove side walls etched verticaly and the end walls etched on a taper. As the grooves reached the backside, the end walls tapered together forming a small slit where the connections to the back contacts occured. A theoretical equation relating the groove length, width, and depth was developed. Grooves ranging from 5 um to 100 um wide, and 870 um to 1,140 um long were anisotropically etched into a 300 um thick (110) wafer to verify the equation and determine the optimum groove length and width for the final design. The final design consisted of grooves 5 um wide, 1000 um long, and 290 um deep. The groove centers were spaced 1 mil (25.4 um) apart. A five-level mask set was designed and fabricated. A fabrication procedure for the final design was specified, and solar cells were fabricated. The results of the

fabrication steps are discussed and evaluated. The fabricated cells demonstrated the feasibility of the design. However, improvements in efficiency could not be determined due to short circuits between the doped regions. Recommendations for improving the fabrication procedures are given.

BACK-CONTACT VERTICAL-JUNCTION SOLAR CELL

I. Introduction

The objective of this thesis was to improve the efficiency of silicon solar cells by designing and fabricating a solar cell which synergistically combines the advantages of the interdigitated back-contact solar cell with the advantages of the wedged-channel vertical-junction solar cell. Solar cell designs which combine the two concepts were proposed and evaluated. A final design was chosen which consisted of vertical grooves anisotropically etched from the frontside to the backside of a (110) oriented silicon wafer. The groove side walls etched vertically and the end walls etched on a taper. As the grooves reached the backside, the end walls tapered together forming a small slit where the connections to the back contacts occured. A theoretical equation relating the groove length, width, and depth was developed. Grooves ranging from 5 um to 100 um wide, and 870 um to 1,140 um long were anisotropically etched into a 300 um thick (110) wafer to verify the equation and determine the optimum groove length and width for the final design. The final

design consisted of grooves 5 um wide, 1000 um long, and 290 um deep. The groove centers were spaced 1 mil (25.4 um) apart. A five-level mask set was designed and fabricated. A fabrication procedure for the final design was specified, and solar cells were fabricated. The results of the fabrication steps are discussed and evaluated. The fabricated cells demonstrated the feasibility of the design. However, improvements in efficiency could not be determined due to short circuits between the doped regions. Recommendations for improving the fabrication procedures are given.

This chapter examines the background of the vertical-junction solar cell and the stages of its evolution. The interdigitated back-contact solar cell concept is also discussed. Next, the problem statement, the summary of current knowledge, assumptions, scope, approach, and the sequence of presentation are all discussed.

Background

The vertical-junction (VJ) solar cell had its beginning in the early 1970s. Joseph Wise of the Air Force Wright Aeronautical Laboratory (AFWAL) proposed the vertical junction hardened solar cell [1] as a possible solution for reducing the degradation of solar cells in space due to radiation damage. At first, the VJ solar cell was called

the vertical multijunction (VMJ) solar cell. The first VMJ solar cell was constructed from a slab of epitaxially grown silicon composed of numerous, very thin, alternating p-regions and n-regions, as shown in Figure 1-1a. The contacts were placed on the back surface such that the p-regions were all connected with one common conductor and the n-regions with another, as shown in Figure 1-1b. Rahilly [2] showed that the VMJ solar cell could have superior radiation resistance if 2000 junctions per centimeter were employed. The original VMJ solar cell had three major problems. These problems included: (1) a large recombination current due to the very large surface periphery of the junction; (2) poor short wavelength efficiency unless a very low upper surface recombination velocity was maintained; and (3) fabrication difficulties, such as the metallization of the closely spaced layers [3:194].

Smeltzer, Kendall, and Varnell [3] proposed three possible solutions to the original VMJ solar cell. The proposed designs shown in Figure 1-2 were called the Type I, Type II, and Type III VMJ solar cell. Smeltzer and others developed the fabrication procedures for these three cell types, with the Type III VMJ being the simplest. A few preliminary cells were fabricated with efficiencies up to 5.5% [3:195].

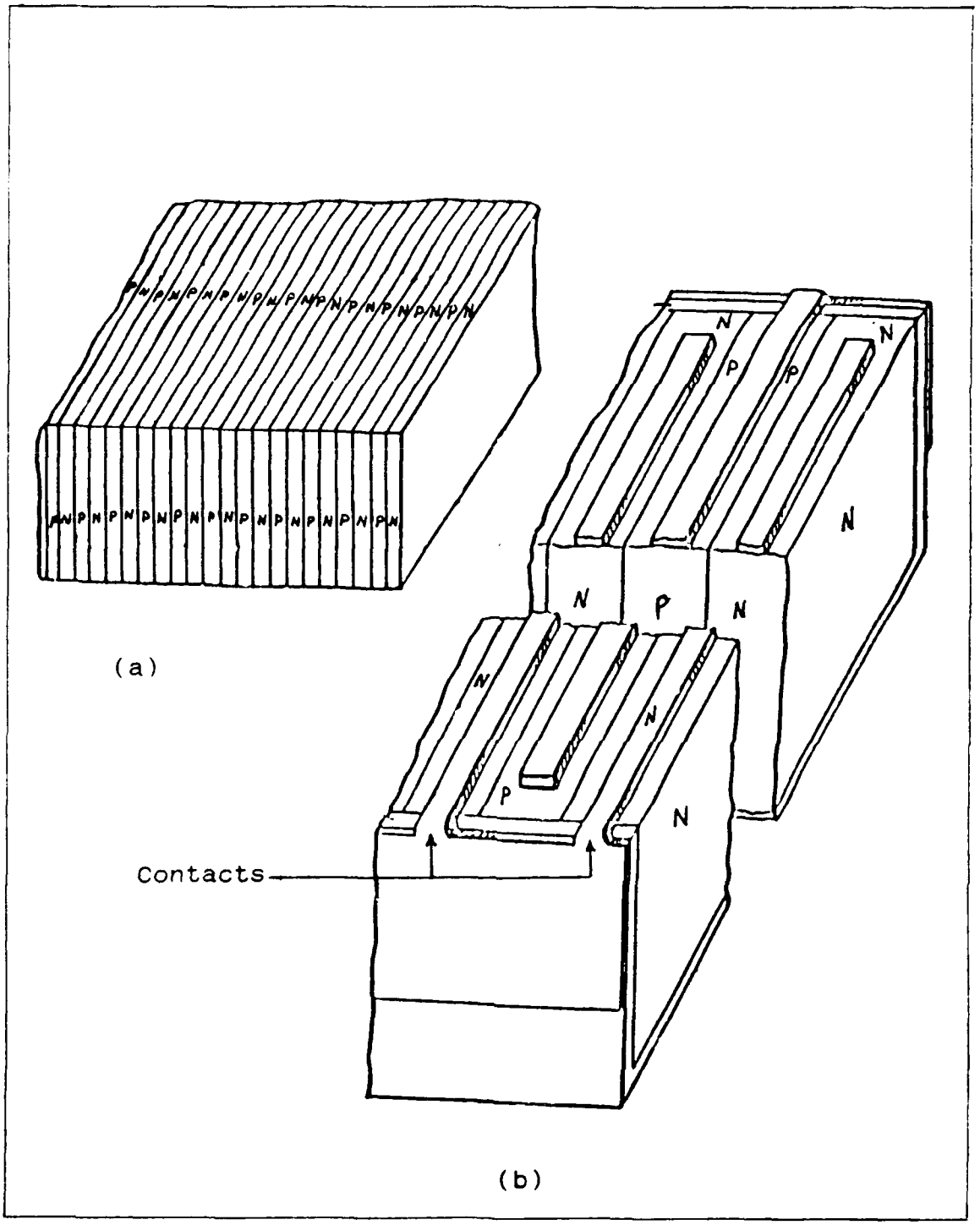


Figure 1-1. Vertical multijunction (VMJ) solar cell: (a) Epitaxially grown alternating p- and n-regions, (b) P-regions connected with one common conductor and n-regions with another [1:1].

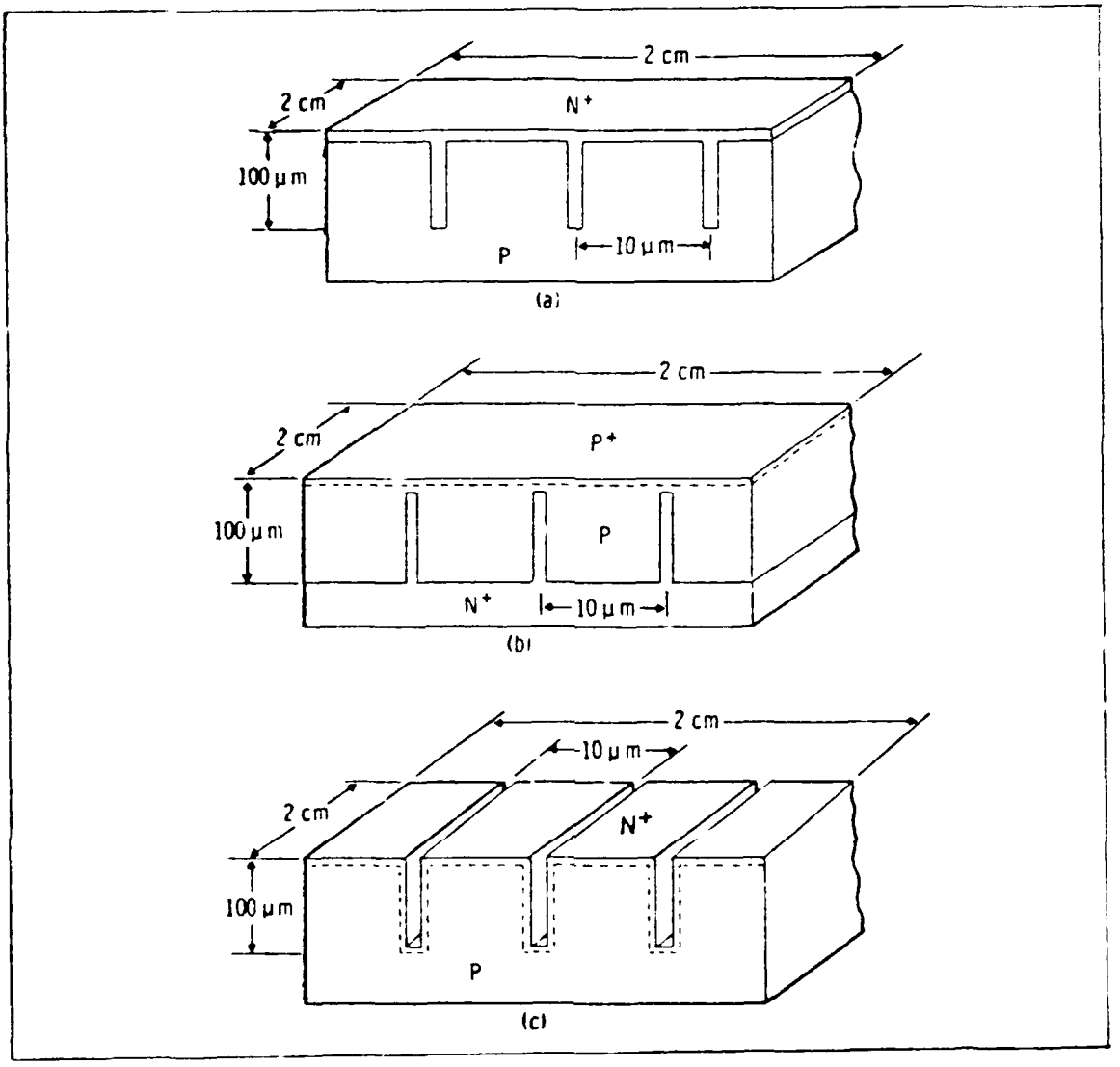


Figure 1-2. Three designs for vertical multijunction solar cells: (a) Type I, (b) Type II, and (c) Type III [3:195].

Texas Instruments Incorporated selected the Type III design for further research due to predicted improvements in the long-wavelength response anc tolerance to electron bombardment [4]. In addition, they discovered a process which converts the top surface into an effective blackbody

absorber by etching the walls to a point. The result of this process is shown in Figure 1-3. Light entering a groove is totally absorbed by multiple reflections. Cells with 9.3% efficiencies were produced [4:44].

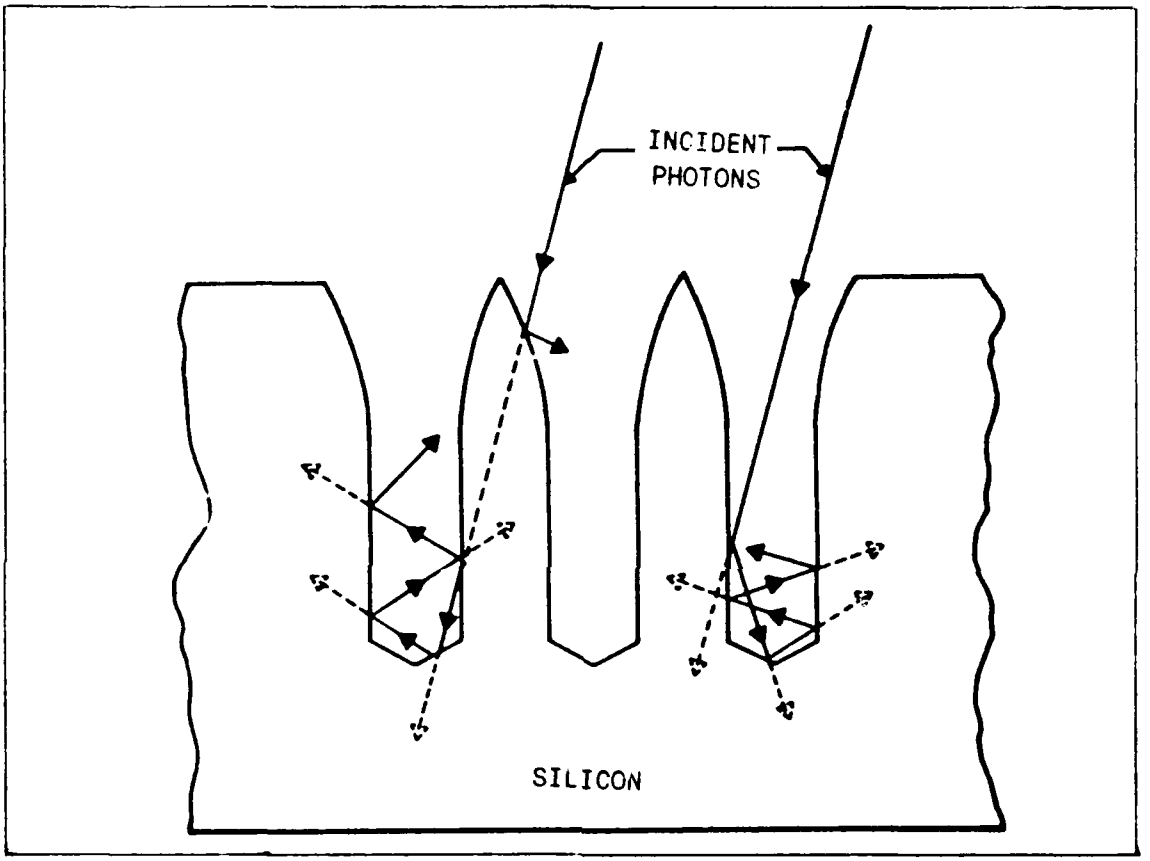


Figure 1-3. Schematic cross-section of the groove structure in a vertical multijunction solar cell illustrating how multiple reflection can lead to total absorption [4:9].

Around the mid-70s, the VMJ solar cell consisted of many long grooves. The top electrical contact ran parallel to the grooves and was spaced approximately every fourth groove, as shown in Figure 1-4b. This cell design had poor

conversion efficiency due to a high series resistance resulting from the long path the charge needed to travel through the top diffusion layer before reaching a grid finger [5]. Also, this cell was very fragile and tended to break along the grooves.

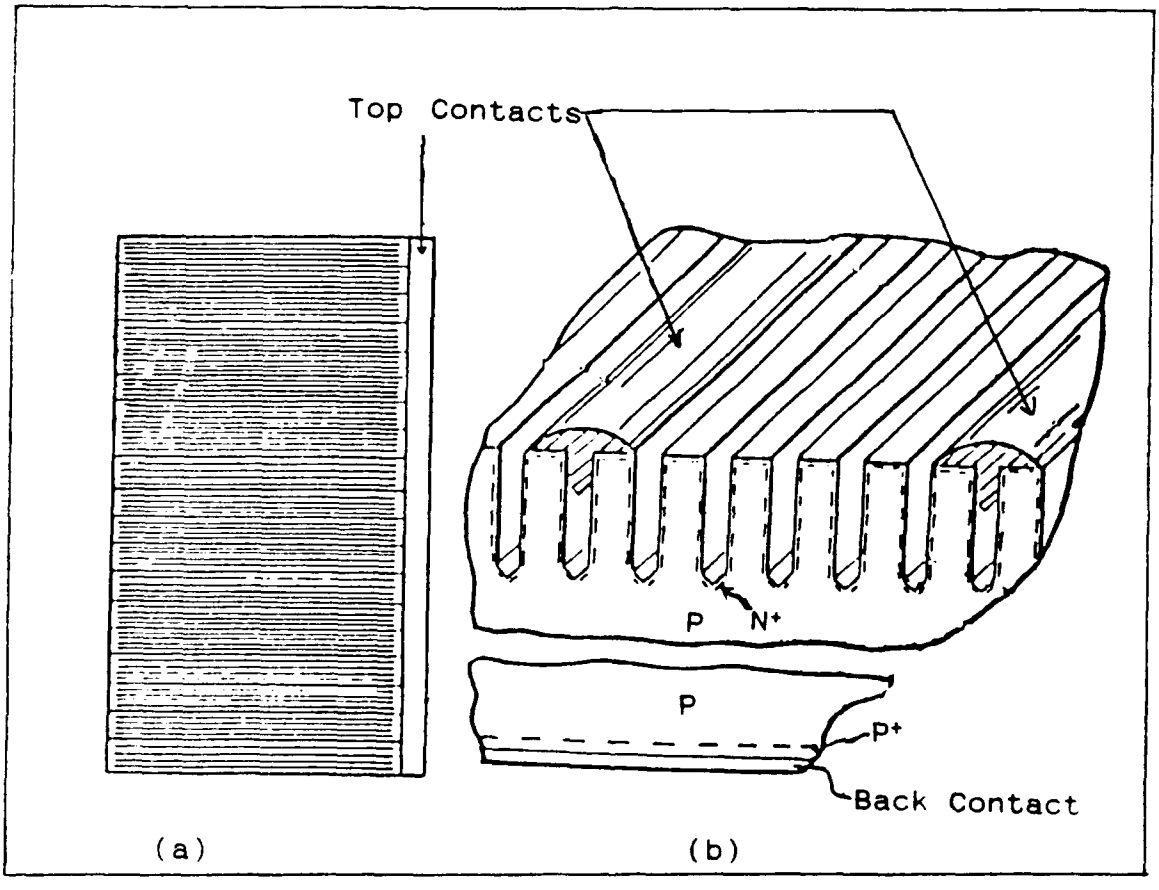


Figure 1-4. Vertical multijunction solar cell of the mid-70s: (a) Top view, (b) Cross-sectional view [5:1].

Rahilly proposed improving the VMJ solar cell with the rib-and-channel vertical multijunction solar cell [5] shown in Figure 1-5. In this cell, the grooves forming the

vertical junctions are relatively short instead of running the full length of the cell. These short parallel grooves had perpendicular ribs separating them. The electrical grid ran along the top of the rib and joined an electrical header. This cell showed improved efficiency and mechanical strength.

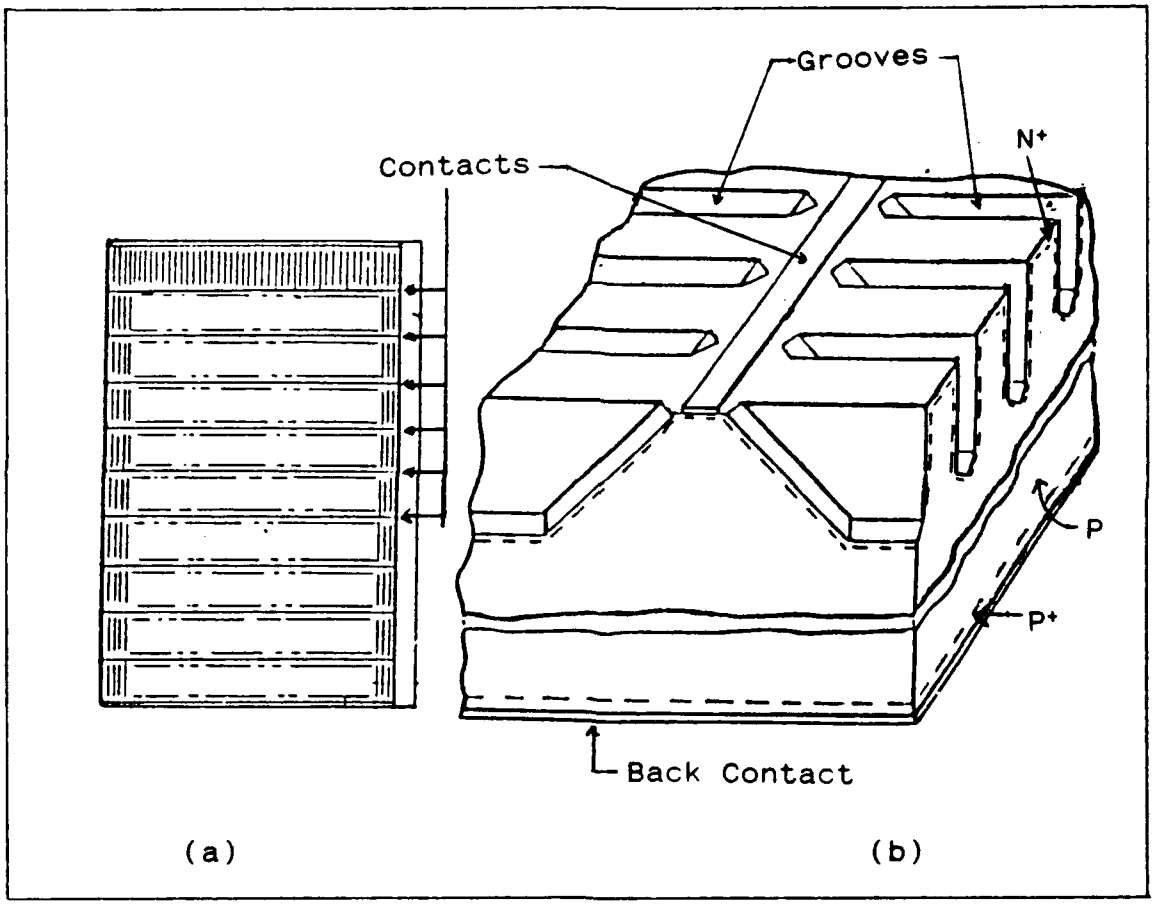


Figure 1-5. Rib-and-channel vertical multijunction solar cell: (a) Top view, (b) Cross-sectional view [5:1].

Solarex, under contract to AFWAL, performed considerable research toward optimizing the VJ solar cell.

Their efforts produced efficiencies greater than 15% [6:i]. However, reliability tests showed that the walls of the cells would fracture when thermally cycled between liquid nitrogen temperatures and 100 °C [7:1].

Wise and Holt [8], and Holt [9], proposed two possible methods to further improve the mechanical strength of the cell. One option was referred to as the wedged-channel vertical-junction solar cell [8] shown in Figure 1-6. The other option was referred to as the hole-matrix vertical-junction solar cell [9] shown in Figure 1-7. Since no available way of etching deep holes in silicon was available in the AFWAL laboratory, the wedged-channel VJ solar cell was chosen [7:2]. These cells had a slightly higher resistance than the older Solarex design due to an increased surface resistance. Therefore, efficiencies were slightly lower (1-2%) [7:i]. However, the wedged-channel VJ solar cell had better mechanical strength than the rib-and-channel VJ solar cell.

Another type of high efficiency solar cell, the interdigitated back-contact solar cell [10], has one significant advantage compared to the VJ solar cell. This advantage is the elimination of self-shading which results from the top grid connection shading the solar cell. Figure 1-8 shows the interdigitated back-contact design. However, one disadvantage of this cell is the requirement of long

diffusion lengths which make it inherently more radiation sensitive.

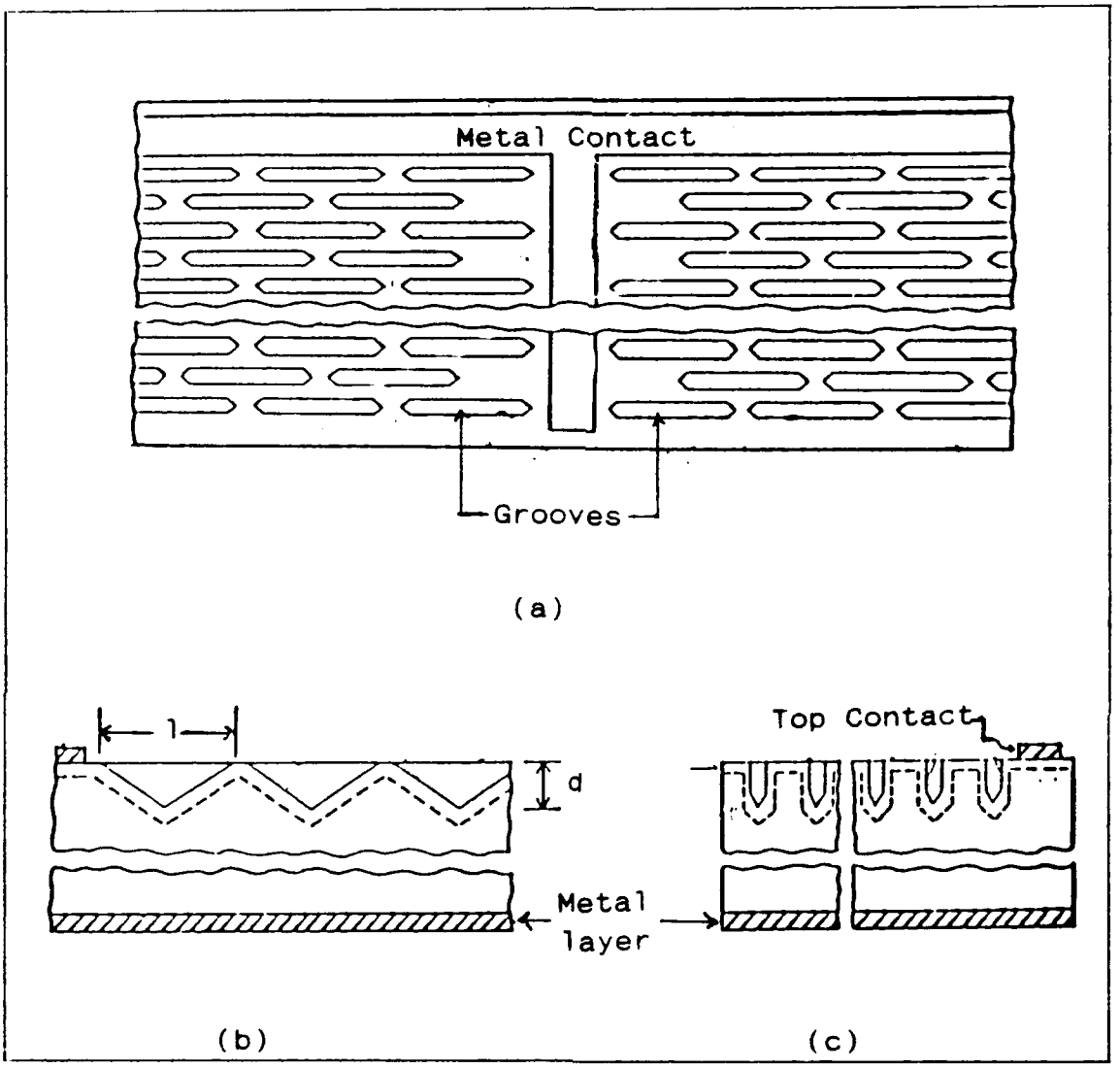


Figure 1-6. Wedge-channel vertical-juntion solar cell: (a) Top view, (b) Front-side view, (c) End view [8:1].

An increase in efficiency without sacrificing radiation resistance may be possible by combining the vertical-junction concept with the interdigitated back-contact

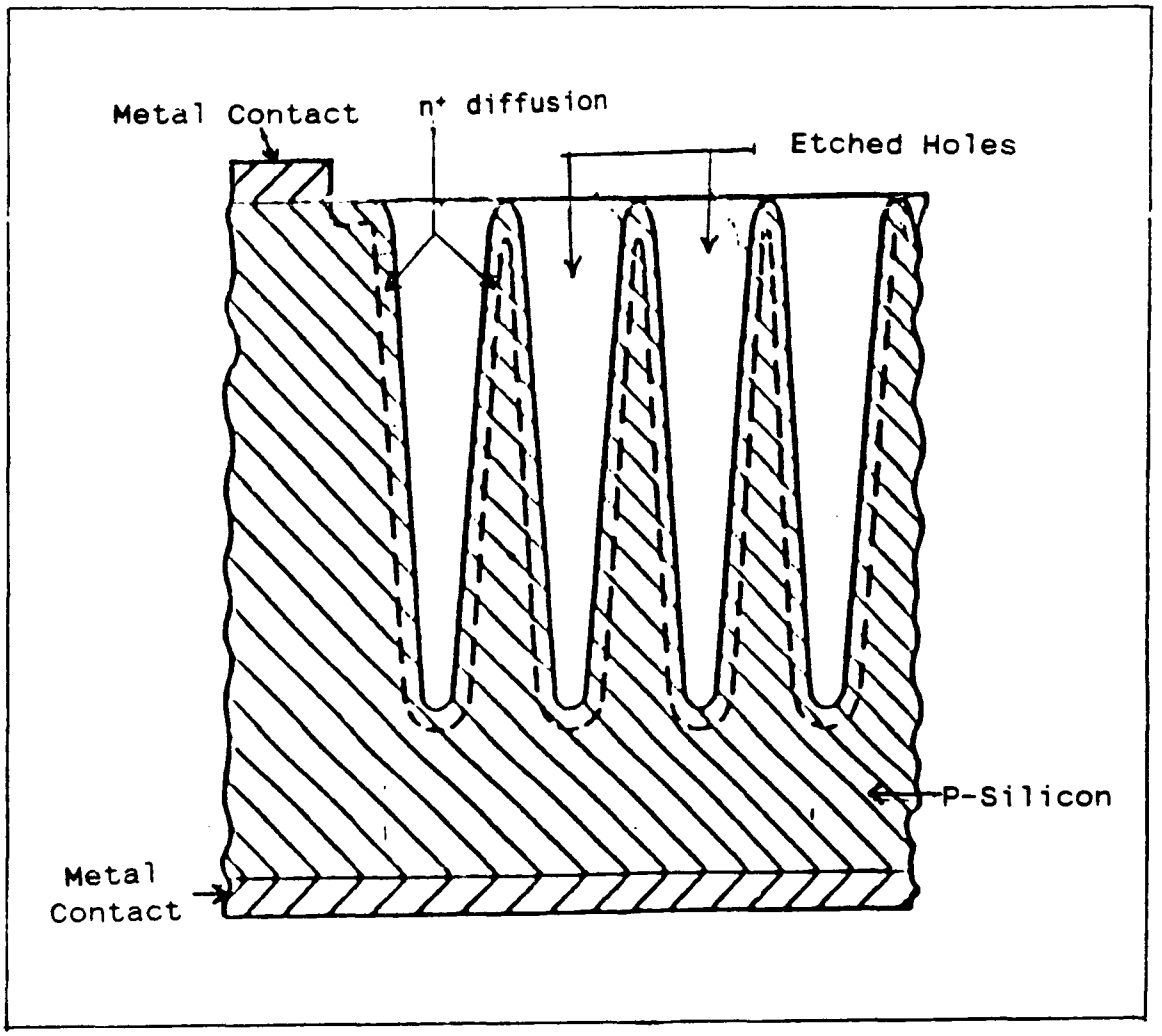


Figure 1-7. Hole-matrix vertical-junction solar cell [9:1].

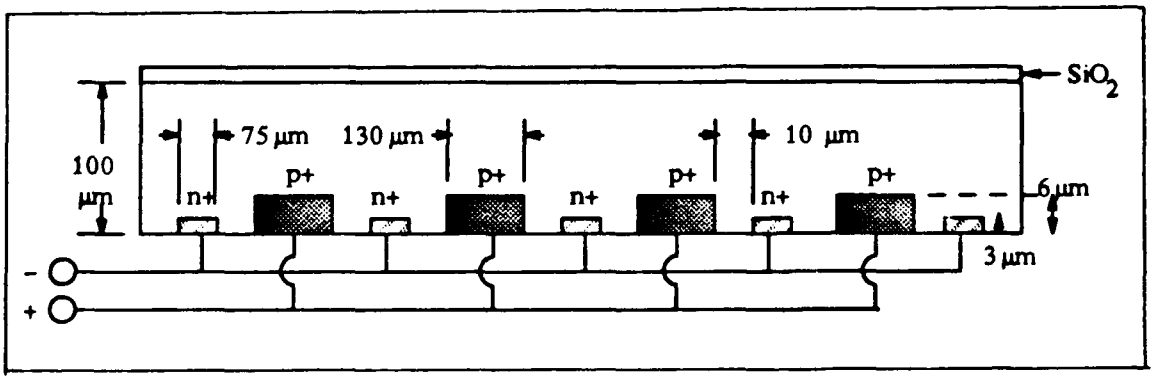


Figure 1-8. Interdigitated back-contact solar cell. There is no top-surface grid, and thus, no self-shading [16:22].

concept. The result would be no shading, low reflection, and a minimal requirement for minority carrier diffusion length (Chapter II discusses how these parameters affect solar cell efficiency).

Problem Statement

The question to be answered in this thesis is can the efficiency of a silicon solar cell can be increased by combining into one cell, the advantages of both the interdigitated back-contact solar cell and the vertical-junction solar cell. In order to evaluate the feasibility of this concept, a silicon solar cell with both vertical junctions and back contacts will be designed, fabricated, and evaluated. Finally, recommendations for further improvements will be made.

Summary of Current Knowledge

The physics of operation of a basic conventional solar cell are well known and documented . Vertical-junction solar cell optimizations have been performed by the Solarex Corporation (Rockville, Maryland) [6 and 11]. Information concerning anisotropic etching of silicon is available from many sources [12 and 13]. Lt Ali Kaba (GE-85J-2 graduate) attempted to improve the efficiency of VJ solar cells [14]. This study describes the fabrication procedures used to achieve a VJ solar cell with 14.4% AMO (at zero atmosphere

attenuation) efficiency. In addition, designs utilizing the interdigitated back-contact concept have yielded solar cells with efficiencies as large as 20% in concentrated sunlight [15]. Finally, several patents and reports mentioned in the background section are available which discuss the fabrication of the VJ solar cell.

Assumptions

This thesis effort relies on previous vertical-junction solar cell design optimizations [6 and 11] sponsored by the AFWAL Power and Components Branch (AFWAL/POOC). It also relies upon previously published work concerning the fabrication of interdigitated back-contact cells, and literature regarding the unique anisothropic etching characteristics of (110) silicon wafers.

Scope

The scope of this effort includes the following: (1) develop a solar cell design which combines the back-contact and the vertical-junction concepts for the purpose of increasing the efficiency of the cell; (2) determine the fabrication procedure for this design; (3) verify the fabrication procedure and design by fabricating solar cells; (4) test the fabricated solar cells to determine their efficiency; and (5) make recommendations for improving the performance of the design.

Approach

The approach to be used in this thesis is to first develop an overall design which combines the advantages of the back-contact concept and the vertical-junction concept. Figure 1-9 shows a sketch of a proposed design. One of the critical fabrication steps in the design is etching the grooves. The length of a groove determines the depth of a groove. Therefore, the groove length must be determined so

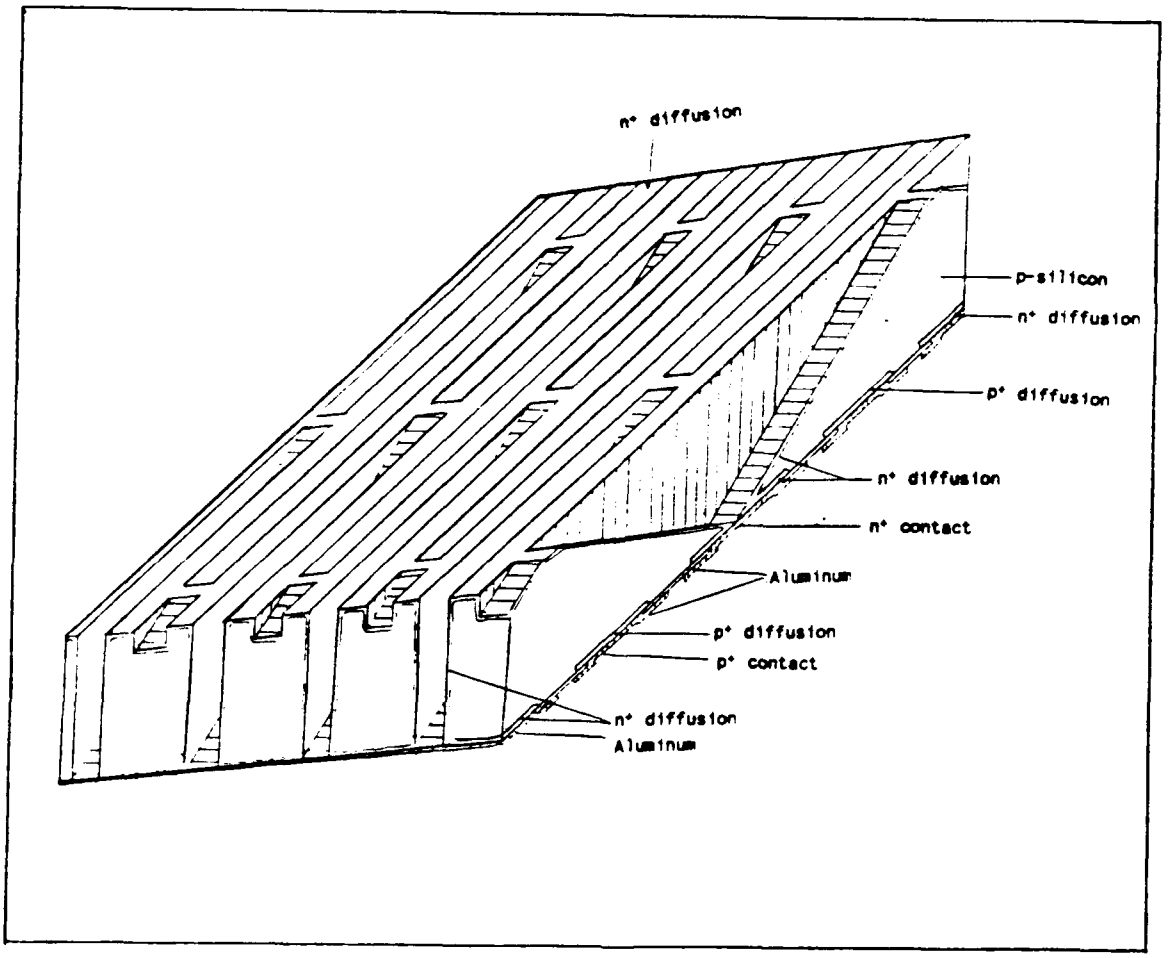


Figure 1-9. Sketch of the back-contact vertical-junction solar cell design.

that the bottom tip of a groove just reaches the backside of the wafer. This will result in the slit on the backside being as small as possible.

In order to determine the proper groove length, the theoretical length-to-depth ratio will be determined by calculating the angles associated with various planes within walls of the groove. These calculations will be verified by fabricating a test groove mask from the pattern shown in Figure 1-10. The groove length will be varied in 20 um steps up to 100 um on either side of the calculated length. The length is based on a groove depth of 300 um. The theoretical dimensions are calculated in Chapter III. The optimal length and width will be determined experimentally by etching a test wafer using the test groove mask. The actual mask set will then be designed and fabricated using the optimal length and smallest possible width.

The detailed fabrication procedures will be determined based on past solar cell optimizations done by Solarex Corp. and reported in the literature [6 and 11].

Sequence of Presentation

The sequence of this thesis is presented in the following order. Chapter II begins with the basic theory of a conventional silicon solar cell followed by factors which affect the efficiency of a solar cell. Next, Chapter II

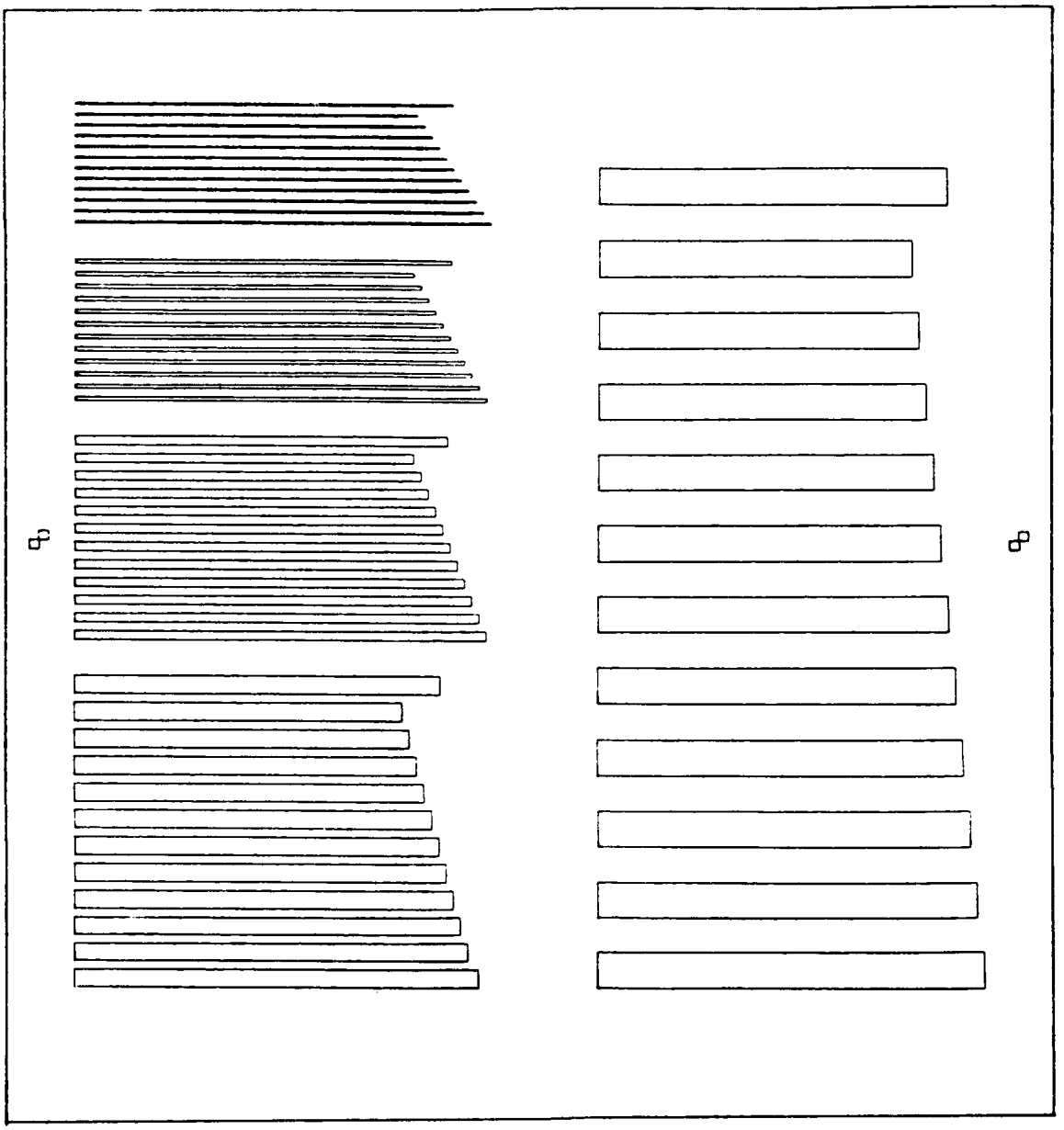


Figure 1-10. Test groove pattern (dimensions calculated and given in Chapter III).

discusses two innovative cell designs which overcome certain efficiency limitations of the conventional solar cell. The two designs are called the vertical-junction solar cell and the interdigitated back-contact solar cell. Chapter II

concludes with a discussion of the concept for combining these two innovative designs into one cell design for the purpose of further increasing the efficiency. The new cell design was given the name back-contact vertical-junction solar cell.

Chapter III discusses the different design considerations with emphasis on the final design and why it was chosen. Chapter III also develops a theoretical equation relating the length of a groove to the width and depth of a groove which was needed to optimize the final design. This equation was verified experimentally by etching a test-groove pattern into a wafer. The results of the test-groove etching are given in Chapter V.

Chapter IV discusses the fabrication of the back-contact vertical-junction solar cell, and Chapter V discusses the results obtained following each major fabrication step. Also, the final performance evaluation of the solar cell design is given.

Chapter VI discusses the conclusions made from the experimental results followed by recommendations for further improvements.

II. Theory and Literature Review

The back-contact vertical-junction (BCVJ) solar cell is a proposed design which attempts to synergistically combine two innovative solar cell concepts. The two cell concepts are the vertical-junction and the interdigitated back-contact designs. Each concept has certain unique features which afford it a higher efficiency than that of a conventional planar solar cell. By combining the positive features of both cells into one cell, a highly efficient and radiation tolerant solar cell may be realized. To explain the BCVJ solar cell, the following will be discussed: (1) basic solar cell theory; (2) factors affecting solar cell efficiency; (3) unique characteristics of both innovative cell designs which result in an increase in cell efficiency; and (4) how these advantages can be combined into one design called the back-contact vertical-junction solar cell for the purpose of further increasing efficiency.

Basic Solar Cell Theory

A solar cell, shown in Figure 2-1, is a semiconductor device which converts light energy into electrical energy by means of the photovoltaic effect. When light is incident on a semiconductor such as silcon, the impinging photons create electron-hole pairs in and near the surface of the silicon.

These electron-hole pairs can be separated by a potential barrier such as a pn-junction. The separated charge creates a potential difference between the p-side and n-side. This voltage can be transported to an external load via electrical contacts.

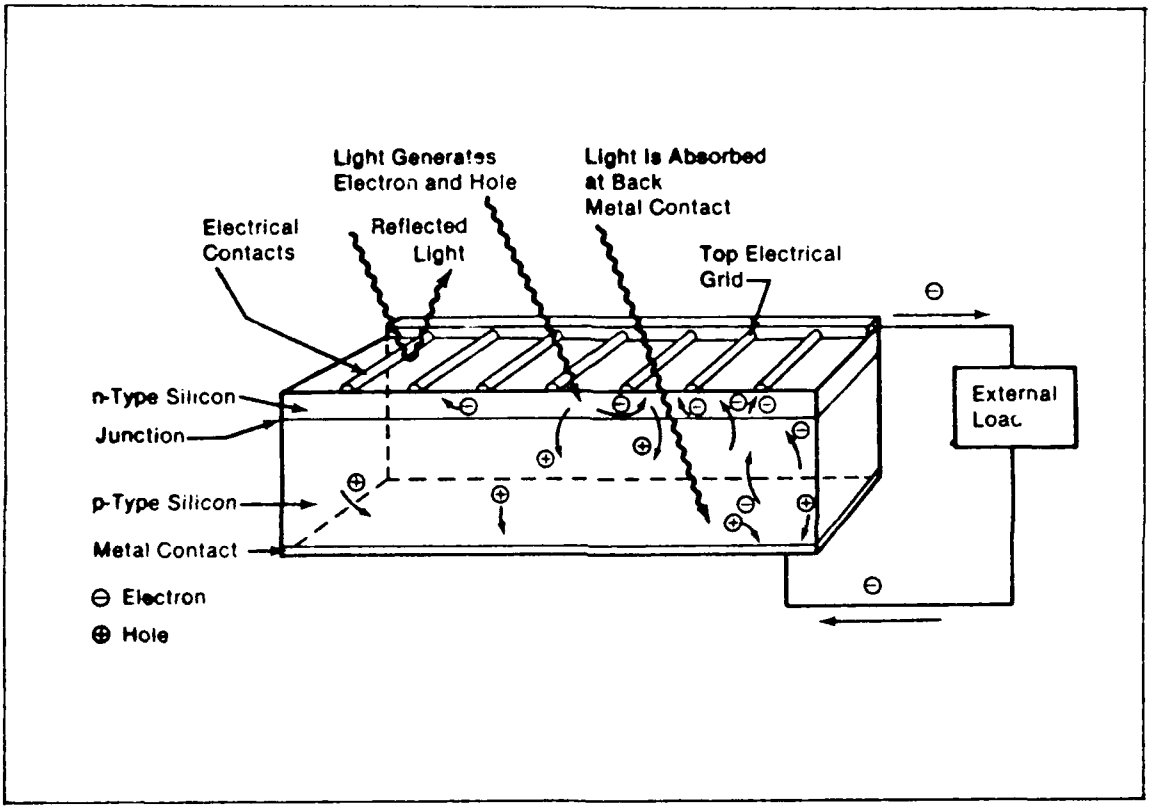


Figure 2-1. Light incident on the cell creates electron-hole pairs, which are separated by the potential barrier, creating a voltage that drives a current through an external circuit [16:22].

The solar cell is not a new idea, but has been around since 1839 when Edmond Becquerel, a French physicist, first observed the photovoltaic effect [16:6]. Since the advent

of the space age, solar cells have provided electricity for space vehicles. Since scientists are virtually certain that the demand for energy will increase, while the expendable sources of energy decrease, an inexhaustible and nonpolluting source of energy is needed. This source is the sun.

The theory of the single-crystal solar cell is based upon three principles: (1) generating electron-hole pairs by means of photon energy; (2) separating the electrons and holes by introducing a potential barrier, and (3) collecting the separated charge by electrical contacts for transfer to an external load. The voltage created by separating photon generated electron-hole pairs is called the photovoltaic effect [16:10].

Photovoltaic Effect. The photovoltaic (PV) effect is the basis for converting light to electricity in a solar cell [16:10]. The PV effect results from a concept of modern physics which postulates that light has properties of both particles and waves. The particle nature of light is called the photon. In general, an electromagnetic light wave is composed of an ensemble of photons, and each photon has an energy:

$$E = hf = hc/\lambda, \text{ eV} \qquad (1)$$

where h = Planck's constant (4.13572×10^{-15} eV-second),

f = the frequency in Hertz,

c = the speed of light (2.998 x 10^8 m/sec), and

λ = the wavelength in meters.

If the intensity of light is increased, the number of photons increases, but the energy of each photon remains the same as long as its frequency remains constant.

When a photon impinges upon a semiconductor such as silicon, the photon may be reflected, transmitted, or be absorbed. The photons which are absorbed may collide with an atom, free electron, or a valence electron. A photon absorbed by colliding with an atom produces heat (phonon) since the atom will vibrate. Since silicon has four valence electrons per atom, and the number of silicon atoms in a unit volume of silicon is 5 x 10^{22} atoms/cm^3, then the number of valence electrons is 20 x 10^{22} valence electrons/cm^3 [19:6]. In heavily doped silicon, the number of free electrons is approximately 10^{19} cm^{-3}; therefore, the number of valence electrons is more than 1000 times the number of free electrons. Since the concentration of valence electrons is much greater than the concentration of free carriers in even heavily doped semiconductors, the probability of a photon interacting with a free electron carrier is negligible. Therefore, photons which interact with electrons, are most likely to interact with the valence electrons. If a photon with energy (E) greater than the

semiconductor's bandgap energy (E_g), collides with a valence electron, the electron is excited from its bound position in the crystal lattice and produces an electron-hole pair, as shown in Figure 2-2. Another perspective is that when a photon with energy greater than E_g interacts with a valence electron, the valence electron is promoted to the conduction band where it can move freely and participate in the conduction of electricity. By accomplishing this change, the electron leaves behind a hole, which is the absence of an electron. A hole can also participate in the conduction process as it moves from one valance bond to another. Figure 2-3 shows how carriers are generated when photons enter a semiconductor crystal. Photons with energy less than E_g create heat within the lattice without significantly altering the electrical properties of the material. That is, low-energy light impinging upon a silicon crystal causes the atoms to vibrate and rotate in their bound positions; but the vibrating atoms preserve their covalent bonds [16:12]. Likewise, if the energy of a photon is greater than the bandgap energy, the lattice absorbs the extra energy as a phonon or heat.

The generation of electrons and holes by photons is the central process in the overall PV effect, but it does not itself produce current. If no other mechanism were involved, the light-generated electron-hole pairs would

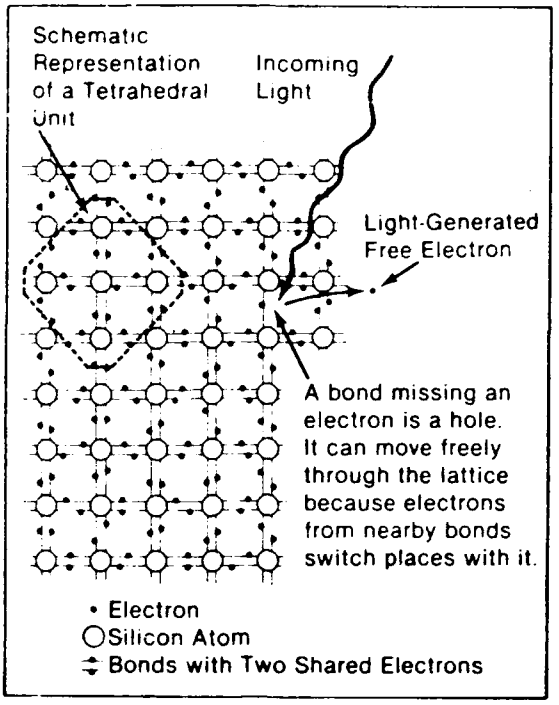


Figure 2-2. Light of sufficient energy can generate electron-hole pairs in silicon. The electrons and holes can then move freely throughout the crystal [16:13].

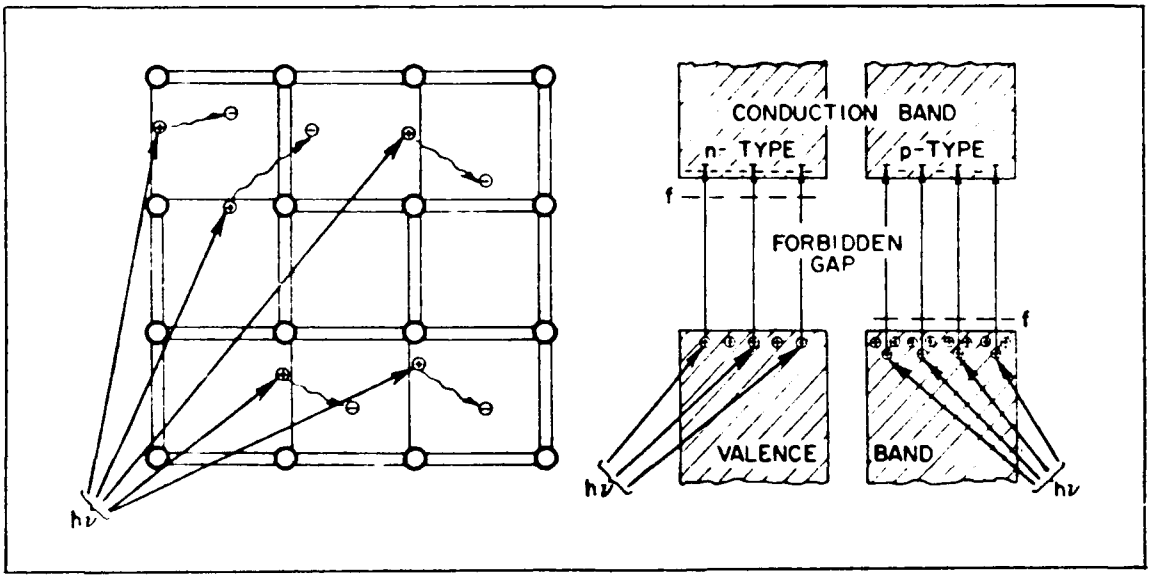


Figure 2-3. Electron-hole production by photons requires a photon with an energy greater than or equal to E_g [18:15].

merely randomly diffuse or scatter throughout the crystal for a time, τ, called the mean-free recombination time. To capitalize on the efficiency of the generated electron-hole pairs to produce a current, another mechanism called the "built-in potential barrier" is required.

Potential Barrier Concept. In order to separate the electrons and holes so they may contribute to an electric current, a potential barrier is needed. The potential barrier can be formed by a pn-junction, as found in a conventional diode. To explain how the pn-junction separates the electrons and holes, one must understand the physics of a semiconductor pn-junction.

To explain this phenomenon, Figure 2-4a depicts separated n-type and p-type semiconductors which are assumed to be at room temperature. The n-type semiconductor is doped with donor atoms, which have five valence electrons. Since only four valence electrons are needed to form covalent bonds with four adjacent silicon atoms, the extra electron will readily absorb the energy required to excite it into the conduction band. As a result, the electron becomes a free electron and can easily move under the influence of an electric field. The free electrons in the n-type semiconductor are primarily the result of ionized donor atoms and are called majority carriers. The n-type semiconductor also contains electron-hole pairs created by

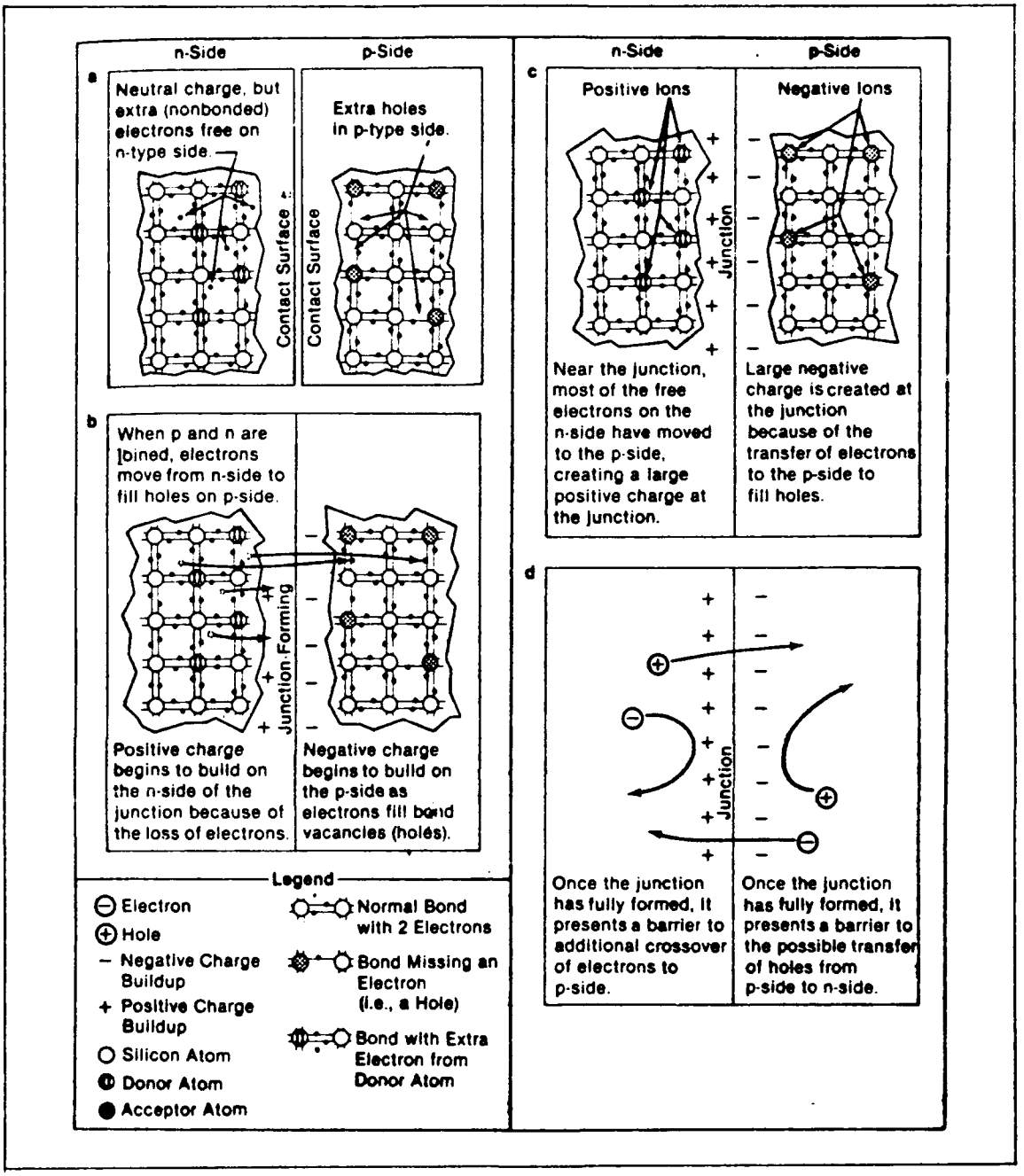


Figure 2-4. During junction formation, electrons move from the n-type silicon into the p-type, while holes move in the opposite direction. Movement of electrons into the p-type silicon and holes into the n-type silicon establishes a fixed potential barrier at the junction which opposes the further movement of free carriers and creates a state of equilibrium [16:19].

thermal or light energy. The holes are minority carriers in n-type silicon and also move under the influence of an electric field.

The p-type semiconductor is doped with acceptor atoms. Acceptor atoms have only three valence electrons resulting in one incomplete covalent bond or hole. As a result, an electron from the valence band requires very little energy to be excited into the hole. When this happens, holes are formed in the valence band of the p-type semiconductor and become majority carriers. Free electrons also exist in the p-type material in a much smaller quantity due to thermal electron-hole pair generation. The electrons are minority carriers and are also free to move under the influence of an electric field.

Thus, in the n-type semiconductor, we have a large number of free electrons and a small number (by comparison) of holes; conversely, in the p-type semiconductor, we have a large number of holes and a small number (by comparison) of free electrons.

Next, if the two semiconductors are brought together, as shown in Figure 2-4b, the interface dividing the n-type from the p-type silicon establishes the position of a potential barrier essential to the operation of the solar cell. To understand what takes place when the two semiconductors come together, it is beneficial to consider

the cross-sectional area in the immediate proximity of the two surfaces. In the p-type material, there are excess holes; in the n-type material, excess electrons. When the n-type and p-type materials are brought together, free electrons in the n-type material adjacent to the many holes in the p-type material at the junction will diffuse into the p-type material and combine with the holes. Also, valence band electrons in the n-type side diffuse into holes on the adjacent p-type side, which is equivalent to a hole moving over to the n-type material. This charge transfer processs happens rapidly along the interface (junction), sending large numbers of electrons to the p-type side and holes to the n-type side. Since the charge carriers recombine along the junction, they lose their freedom of movement creating a charge imbalance at the junction: negative ions along the p-type interface and positive ions along the n-type interface, as shown in Figure 2-4c. Since there are very few free electrons in the p-type material to be pulled back to the n-type material, and very few free holes in the n-type material to be transferred back to the p-type material, the charge imbalance remains fixed. Consequently, an electric field is developed between these two groups of immobile ions that reduces the diffusion of majority carriers across the junction, as shown in Figure 2-4d. The

voltage associated with this field is called the potential barrier (V_B) [19:73]:

$$V_B = kT/q \ln (N_A N_D / n_i^2) \text{ volts} \quad (2)$$

where k = Boltzmann's constant (1.38066×10^{-23} J/K),

T = the temperature in degrees Kelvin,

q = elementary charge unit (1.602×10^{-19} C),

N_A = the acceptor concentration (cm^{-3}),

N_D = the donor concentration (cm^{-3}),

n_i = intrinsic carrier concentration ($1.45 \times 10^{10} cm^{-3}$ at room temperature).

As soon as the electric field is established, the dynamics associated with the minority carriers becomes important. The holes in the n-material and electrons in the p-material that wander into the field established by the immobile ions are immediately swept to the other side of the junction. Therefore, electrons are forced into the n-material and holes into the p-material. This action reduces the net charge on each side of the junction and reduces the magnitude of the potential barrier. The flow of minority carriers across the junction constitutes drift current, which is often called the reverse saturation current (I_o).

If light is incident on the junction, photons with energy greater than or equal to E_g may generate

electron-hole pairs. If this occurs in the p-type material, the free electron is a minority carrier and only has a relatively short time during which it is free, because it is very likely to recombine with one of the numerous holes in the p-type material. Therefore, solar cells must be designed such that the probability is high that the electron will wander into the junction and be swept to the n-side before recombining. Once the electron reaches the n-material, the probability of recombining is much less since the number of holes in the n-material is small. Also, there is a very small chance that the electron will return to the p-material since it would have to surmount the potential barrier established between the p-semiconductor and the n-semiconductor.

The hole partner of this electron-hole pair will remain in the p-material, since the electric field at the junction is opposing the movement of holes from the p-material to the n-material. The hole is not likely to recombine either, since there are few electrons in the p-material with which to recombine.

Similarly, if photons with energy greater than E_g are incident on the n-material, an electron-hole pair can be generated in the vicinity of the junction. The hole produced must be swept to the p-material before it recombines with the numerous electrons in the n-material.

Once the hole reaches the p-material, it does not have sufficient energy to surmount the electric field established by the immobile ions, and therefore, remains on the p-side. Also, the hole is not as likely to recombine in the p-material since there are very few free electrons with which it can recombine.

The net result of electron-hole pairs being produced in or near the potential barrier is electron movement to the n-material and hole movement to the p-material. Since illumination and charge separation cause the presence of uncombined excess negative charges in the n-type material and excess holes in the p-type material, a charge imbalance exists in the cell [16:22]. If external conductors (electrical grids), as shown in Figure 2-5, are attached to the n-material and p-material to collect the excess charge, and the conductors are connected to an external load, a current will flow from the solar cell through the load, producing electrical power. If the output terminals are instead shorted, the current, I_s, flowing from p-material to n-material is due to the photon-generated minority carriers. This current will be used in developing the equivalent circuit of a solar cell in the next section.

Equivalent Circuit of a Solar Cell. In order to understand the operational characteristics of the solar cell, one must first understand a simple unbiased

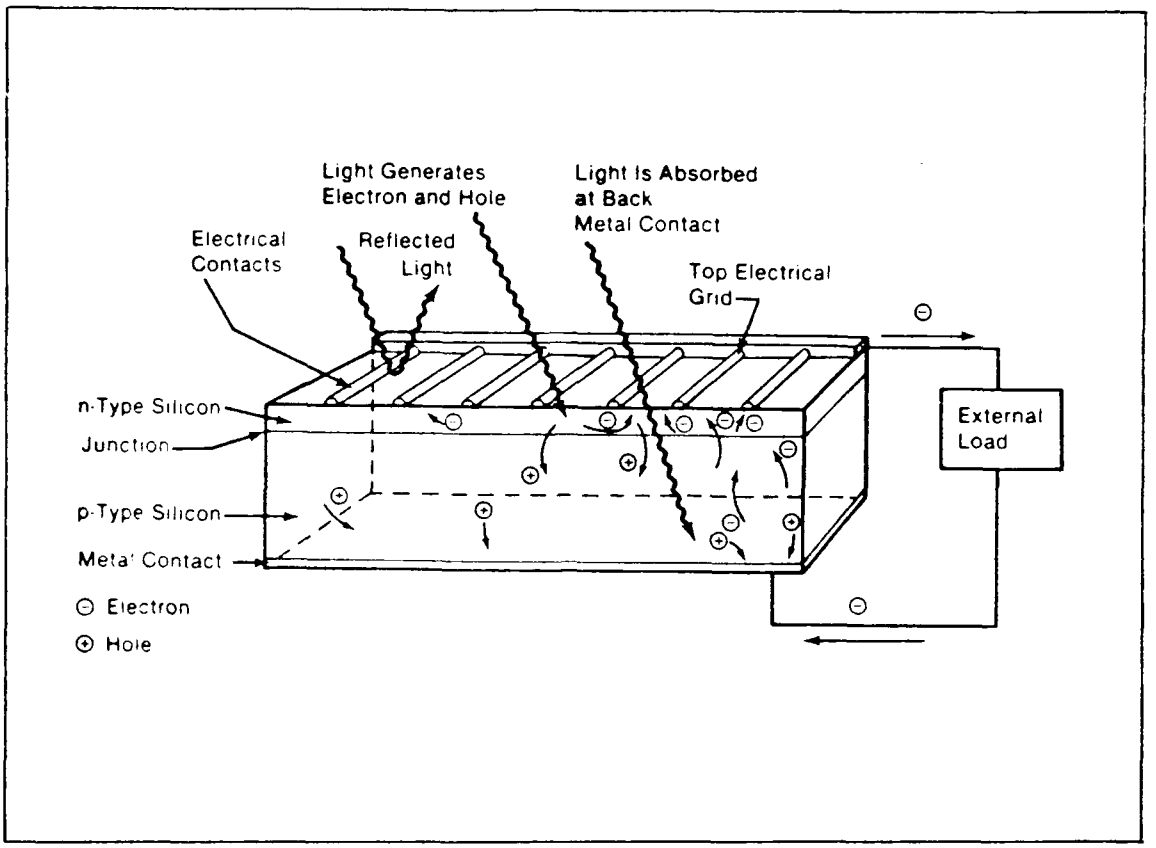


Figure 2-5. Light incident on the cell creates electron-hole pairs, which are separated by the potential barrier, creating a voltage that drives a current through an external circuit [16:22].

pn-junction diode. In the last section, the process by which carriers drift and diffuse across a pn-junction was discussed. In this section, the current equation for an unbiased diode will be developed.

In order to develop a current equation for an unbiased diode, the energy band diagram shown in Figure 2-6a will be considered. At zero current (equilibrium), the diffusion of electrons from one side of the junction to the other, and

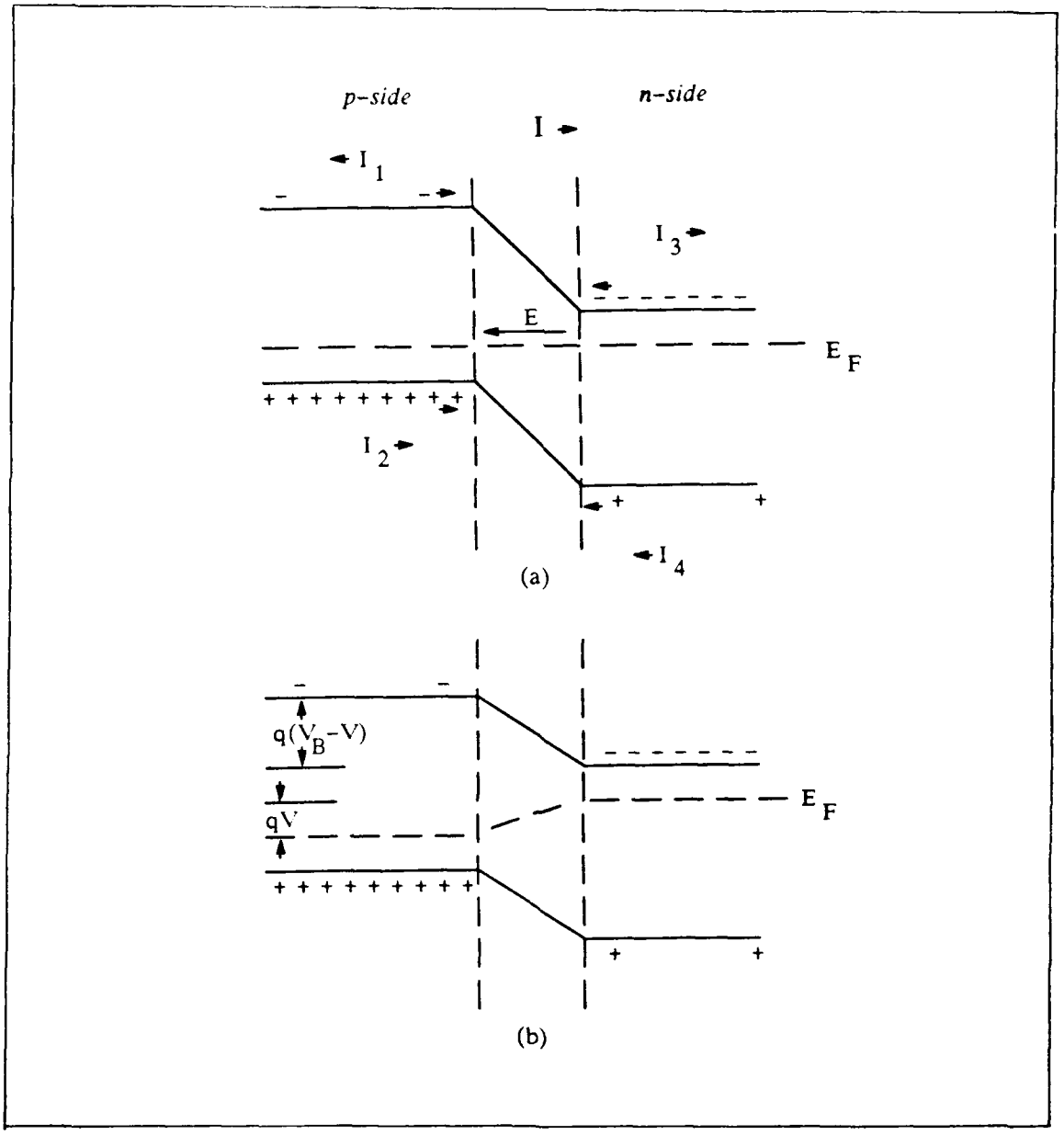


Figure 2-6. Energy-level diagram of a junction diode. (a) Equilibrium, (b) Forward biased [17:179].

vice versa, must be at an equal rate, and this condition is realized if, and only if, the Fermi level (E_F) is aligned across the junction. Using the convention that positive current flow is from the p-material to the n-material, then

I_1 = electron current (A) from p-side to n-side,

I_2 = hole current (A) from p-side to n-side,

I_3 = electron current (A) from n-side to p-side,

I_4 = hole current (A) from n-side to p-side,

n_p = density of electrons (cm^{-3}) in the p-side,

p_p = density of holes (cm^{-3}) in the p-side,

n_n = density of electrons (cm^{-3}) in the n-side,

p_n = density of holes (cm^{-3}) in the n-side, and

I = net current flow (A) from p-side to n-side.

Thus according to [17:180],

$$I_1 = K_1 n_p \text{ amperes} \quad (3)$$

$$I_2 = K_2 p_p \exp [-qV_B/kT] \text{ amperes} \quad (4)$$

$$I_3 = K_3 n_n \exp [-qV_B/kT] \text{ amperes} \quad (5)$$

$$I_4 = K_4 p_n \text{ amperes} \quad (6)$$

where q = the elementary charge of (1.602×10^{-19}C),

V_B = the total contact potential between the p-side and the n-side neutral regions at thermal equilibrium in volts,

k = Boltzmann's constant (1.38066×10^{-23}J/K),

T = the temperature in degrees Kelvin (K), and

K_1, K_2, K_3, K_4 are constants with units $A \cdot cm^3$.

From Figure 2-6a,

$$I = -I_1 + I_2 + I_3 - I_4$$

$$= -(K_1 n_p + K_4 p_n) + (K_2 p_p + K_3 n_n) \exp [-qV_B/kT]. \quad (7)$$

Since I = 0 at equilibrium, then

$$K_1 n_p + K_4 p_n = (K_2 p_p + K_3 n_n) \exp [-qV_B/kT]. \quad (8)$$

If a positive voltage (V) is applied to the p-side, the energy level diagram becomes that shown in Figure 2-6b. In this instance, I_1 and I_4 are not changed since electrons going from the p-side to the n-side, and holes going from the n-side to the p-side are still going downhill. However, a larger fraction of holes (exp $[-q(V_B-V)/kT]$) going from the p-side to n-side, and electrons going from n-side to p-side have sufficient energy to surmount the potential barrier. The net current becomes:

$$I = -(K_1 n_p + K_4 p_n) + (K_2 p_p + K_3 n_n) \exp [-q(V_B-V)/kT]. \quad (9)$$

Equation (9) is also true for negative values of V. If V is significantly negative, then the exponential term approaches zero and the second term in equation (9) becomes negligible. Under this circumstance, the current becomes:

$$I = -(K_1 n_p + K_4 p_n) = I_o \quad (10)$$

This current (I_o) is called the reverse saturation current. Using equations (8) and (10), equation (9) can be written as the well-known theoretical diode equation:

$$I = I_o [\exp (qV/kT) - 1]. \qquad (11)$$

A plot of I versus V is illustrated in Figure 2-7.

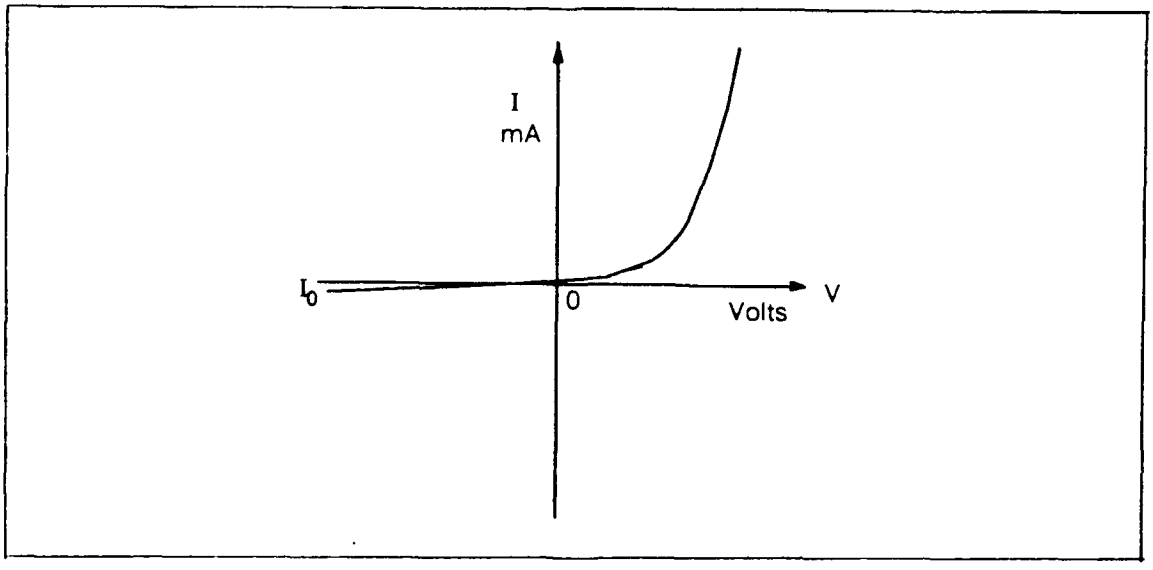


Figure 2-7. Current of a junction diode versus applied voltage [17:185].

Next, a solar cell is considered which is essentially a diode with a large surface to facilitate the production of photon-generated minority carriers. If the two terminals of a solar cell are shorted together, the current (I_s) is due to the diffusion of photon-generated minority carriers across the junction. Although the currents I_1, I_2, I_3, and I_4 are still present, they sum to zero, since V = 0, and do not contribute to the external current.

If an external load is placed between the two output terminals of the solar cell, a voltage is produced across the load and the solar cell. This voltage (V) begins to forward bias the junction and cause the majority currents (I_2 and I_3) to increase. The minority currents (I_1 and I_4) and the photon-generated current (I_s) remain constant. The external load current (I_L) is:

$$I_L = I_s + I_1 + I_4 - I_2 - I_3$$
$$= I_s - I_o [\exp (qV/kT) - 1]. \quad (12)$$

This equation can be represented by the equivalent circuit of a solar cell shown in Figure 2-8. It is noted that the solar cell behaves like a dc current generator connected in parallel to a diode which is connected, unfortunately, in a direction allowing the bypass of the photon-generated current. A plot of I_L versus V is shown in Figure 2-9a for different values of I_s, which is a function of the light intensity. As the voltage (V) increases, the current through the load (I_L) decreases. Also, one might note that at different points along this curve, the power to the load is simply $P = I_L V$. Therefore, there is a power (P_m) where $I_L V$ is a maximum. The maximum power (P_m) can be determined graphically by noting that the largest rectangle beneath the curve in Figure 2-9b results when V and I_L are at the knee of the curve. The voltage and current at maximum output

power are called V_m and I_m, respectively. The voltage which occurs when the output is open circuited ($I_L = 0$) is called the open circuit voltage (V_{oc}).

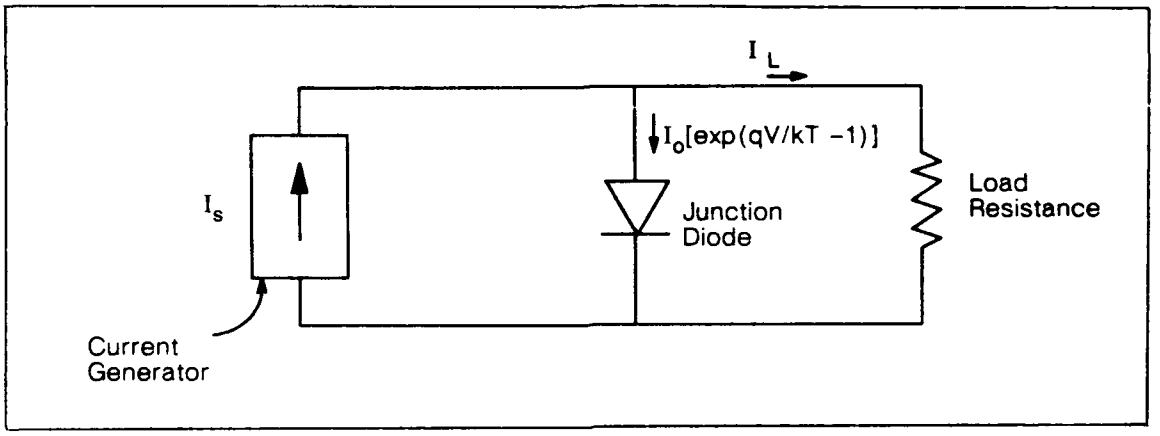


Figure 2-8. Equivalent circuit of a solar cell.

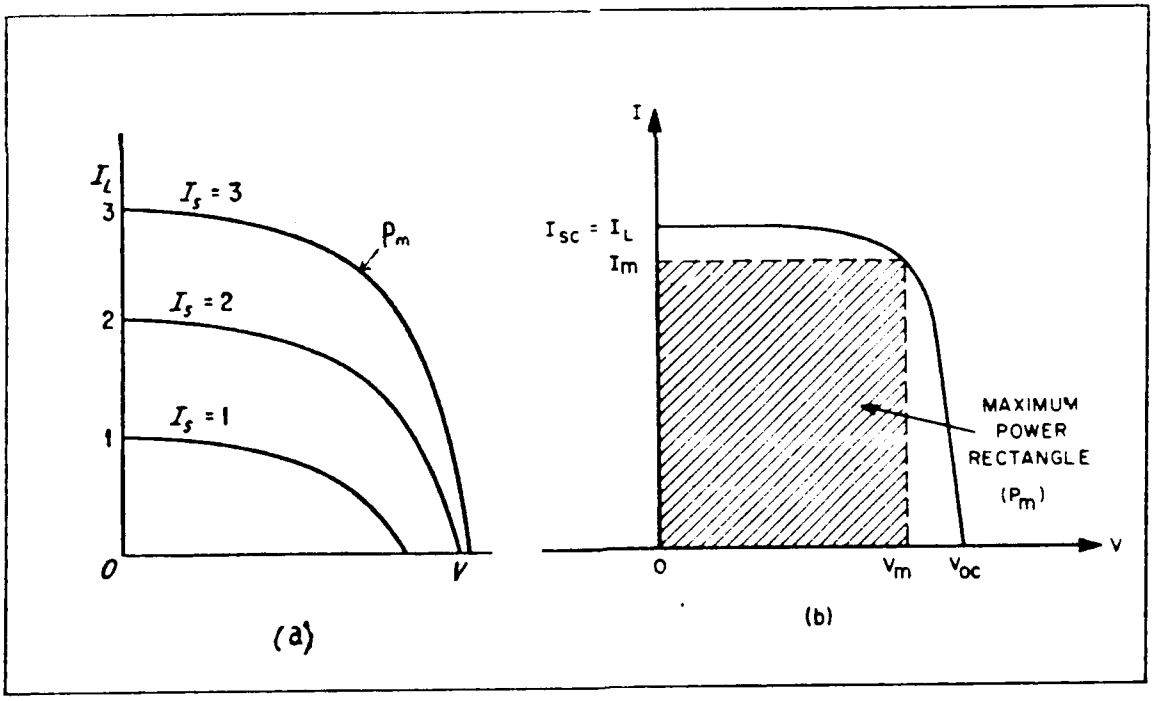


Figure 2-9. Plot of I_L versus V: (a) Effect of light intensity on the load current [17:185], (b) Maximum power (P_m) occurs when $I_s = I_m$ and $V = V_m$ [19:795].

The expression for V_{oc} can be found by setting $I_L=0$ in equation (12) and solving for V:

$$V_{oc} = (kT/q) \ln (I_s/I_o + 1). \quad (13)$$

The current which flows when the output of the solar cell is shorted (V = 0) is called the short circuit current (I_{sc}). Likewise, the expression for I_{sc} can be found by settting V = 0 in equation (12):

$$I_{sc} = I_s. \quad (14)$$

These parameters are used in the next section to develop an equation for the efficiency of a solar cell.

Conversion Efficiency. The conversion efficiency of a solar cell is calculated by dividing the output electrical power by the input power of the incident light. Since the maximum output power occurs at $I_L = I_m$ and $V = V_m$, then an expression for I_m and V_m must be developed. The output power can be expressed as:

$$P = VI_L = V\{I_s - I_o [\exp (qV/kT) - 1]\}. \quad (15)$$

The maximum power (P_m) can be found by differentiating P with respect to V and setting the result equal to zero as follows:

$$0 = I_s - I_o [\exp (qV/kT) - 1] - (qVI_o/kT) \exp (qV/kT). \quad (16)$$

Solving for V yields:

$$V_m = kT/q \ln \{[(I_s/I_o) + 1)]/[1 + (qV_m/kT)]\}. \quad (17)$$

Since the first two terms of equation (16) equal I_L, then when I_L equals the maxmimum current, (I_m) is:

$$I_m = I_s - I_o[\exp(qV_m/kT) - 1]$$
$$= (I_o qV_m/kT)\exp(qV_m/kT). \quad (18)$$

Therefore, the maximum power, P_m, is:

$$P_m = I_m V_m = I_o V_m \exp(qV_m/kT) \ln[((I_s/I_o)+1)/(1+(qV_m/kT))]. \quad (19)$$

The conversion efficiency is defined as [19:292],

$$\eta = I_m V_m/P_{in} = FF\ I_{sc} V_{oc}/P_{in} \quad (20)$$

where P_{in} is the incident power and FF is the fill factor which is a term commonly introduced to relate P_M to the product $I_{sc}V_{oc}$ as follows:

$$FF = I_m V_m/I_{sc} V_{oc} = P_M/I_{sc} V_{oc}. \quad (21)$$

In order to maximize the efficiency in equation (20), FF, I_{sc}, and V_{oc} should be maximized.

The incident power (P_{in}) in watts (W) can be written [17:189]:

$$P_{in} = NqE_{ph} \quad (22)$$

where N is the number of incident photons per second, E_{ph} is the average photon energy in electron volts, and q is the fundamental electron charge (1.60218×10^{-19} C). If

K_a = the fraction of incident photons which are not reflected,

K_b = the fraction of non-reflected photons which create an electron-hole pair sufficiently close to the junction to cause them to be separated before recombining, then

$$I_s = qNK_aK_b \quad [17:189]. \tag{23}$$

Consequently, equation (20) can be written as [17:189]:

$$\eta = K_aK_b(V_mI_m/E_{ph}I_s). \tag{24}$$

In order to maximize K_a, the surface of a solar cell must reflect as little light as possible. To maximize K_b, the electron-hole pairs should be created as close to the junction as possible. These two factors significantly influenced the design of the back-contact vertical-junction solar cell. These and other factors which affect the efficiency of a solar cell will be discussed next.

Factors Affecting Solar Cell Efficiency

A solar cell's efficiency varies depending on the frequency of light incident on the cell. Therefore, it is important to have a standard light source by which the efficiency can be determined. The standard most often used is the solar constant, which is defined as the intensity of solar radiation in free space at the average distance of the Earth from the sun [19:289]. Since sunlight is attenuated by the atmosphere, the power output of a solar cell will vary depending on the distance the light travels through the atmosphere. The degree to which the atmosphere affects the sunlight received at the Earth's surface is determined by the air mass [19:289]. The air mass zero (AMO) condition exists outside the Earth's atmosphere. The air mass one (AM1) condition exists at sea level with the sun directly overhead. The intensity of the sun at AMO is 1353 W/m^2 and at AM1 is 925 W/m^2 [19:289]. Normally, the efficiency is determined at either AMO or AM1; however, many systems today utilize concentrators and determine efficiency at the number of equivalent suns incident on the cell.

The efficiency of a typical solar cell ranges from 10 to 15 percent and may exceed 30 percent for complex cell designs. Several factors which limit a solar cell's efficiency can be changed by improving the design. Others

are inherent and cannot be changed. The major factors which limit a solar cell's efficiency include [16:24]:

1. Reflection from the cell's surface.
2. Light that is not energetic enough to separate electrons from their atomic bonds.
3. Light that has extra energy beyond that needed to separate electrons from bonds.
4. Light-generated electrons and holes that randomly encounter each other and recombine before they can contribute to cell performance.
5. Light-generated electrons and holes that are brought together by surface and material defects in the cells.
6. Resistance to current flow.
7. Self-shading resulting from top-surface electrical contacts.

Factor (1) will be discussed first, (2) and (3) will follow under the heading Photon Energy Utilization, (4) and (5) under Recombination Losses, and (6) and (7) will be discussed under Resistance Effects and Self-Shading, respectively.

Reflection. Sunlight incident on an untreated silicon wafer may reflect 36% (or more) of the light [16:24]. This loss would seriously affect a solar cell's efficiency. Therefore, solar cells are normally treated with an

antireflection (AR) coating such as SiO_2 or SiO [16:64]. Also, the solar cell surface can be textured as shown in Figure 2-10a [16:46]. If the light has an 80%

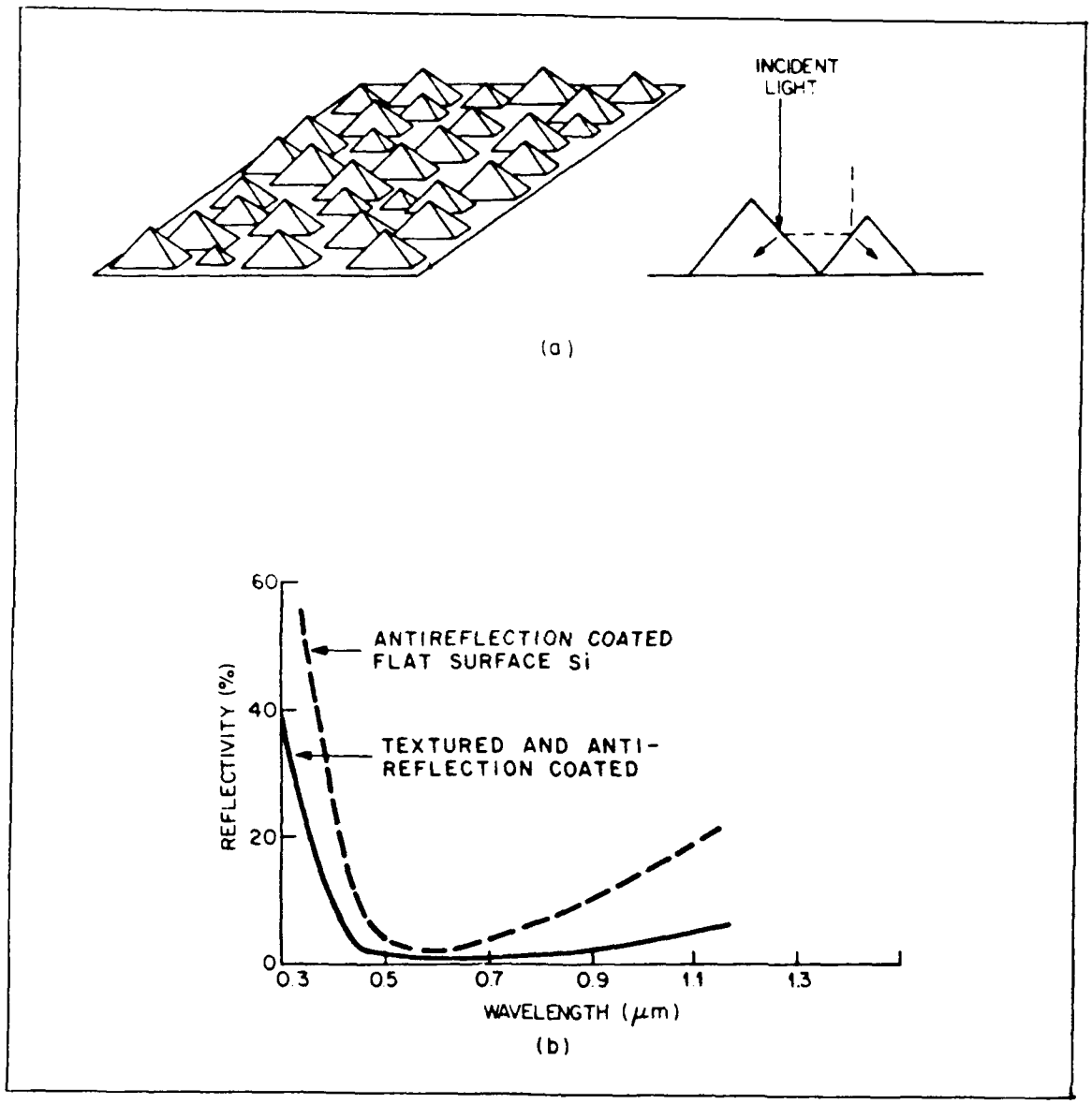


Figure 2-10. Effect of textured surface on reflection: (a) Textured cell with pyramidal surfaces, (b) Reflectivity versus wavelength for a flat surface cell and a textured cell [20:813].

probability of being absorbed on one bounce, and 80% on the second, then the total probability of reflection after two bounces is (0.2 x 0.2) = 0.04. Consequently, texturing the surface rasies the probability of absorption from 80% to 96% [16:47]. Figure 2-10b shows how the reflectivity varies as a function of wavelength for a flat surface cell and a textured cell with AR coatings. An AMO efficiency of over 15% has been obtained using the textured surface [20:812].

Photon Energy Utilization. The energy in a photon of light is given by [17:177]:

$$E = hf = hc/\lambda, \text{ eV} \qquad (25)$$

where h = Planck's constant (4.13572×10^{-15} eV - s),

f = the frequency of light in Hertz,

c = the speed of light (2.99792×10^{8} m/s), and

λ = the wavelength of the light in meters.

When a photon of light enters a solar cell, it can do one of the following [16:25]:

1. Go right through it.
2. Be absorbed, generating heat in the form of atomic vibrations (phonons).
3. Separate an electron from its atomic orbital, producing an electron-hole pair.
4. Produce an electron-hole pair but have an excess of energy, which then becomes heat.

Only (3) represents a near perfect means of transforming sunlight into electrical energy.

The minimum energy required to produce an electron-hole pair in a semiconductor is the bandgap energy (E_g). This can be observed from the band diagram of Figure 2-3b. Therefore, photons with energy less than E_g are wasted energy. Also, photons with energy greater than E_g will produce an electron-hole pair, but the excess energy is wasted. Only photons with the wavelength:

$$\lambda = hc/E_g \tag{26}$$

can produce electron-hole pairs with no wasted energy.

Since the sun's spectrum is composed of an ensemble of energies and intensities, the key is to match a material and its characteristic bandgap energy with the spectrum so that the maximum amount of energy in the sun's spectrum matches or falls just above the characteristic bandgap energy [16:26]. Figure 2-11 shows how the maximum solar cell efficiency varies as a function of the material's bandgap energy (E_g) and the concentration (C) of the sunlight. Silcon (Si) is an excellent material for a solar cell since it has the highest efficiency in concentrated light for its bandgap energy of 1.12 eV.

The production of electron-hole pairs is essential to successful operation of a solar cell. Without this process,

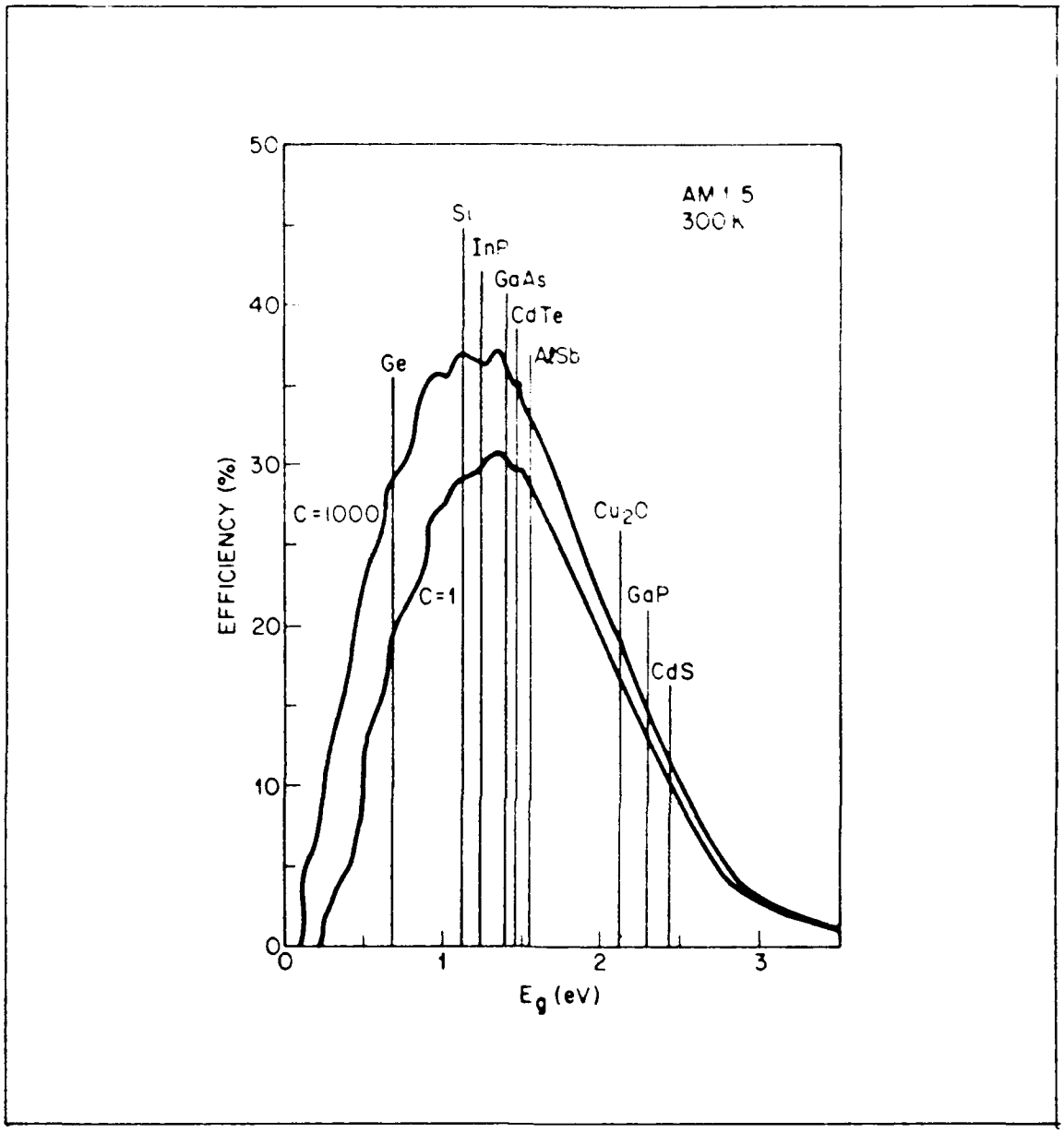


Figure 2-11. Ideal solar-cell efficiency at 300 K for 1-sun and for a 1000-sun concentration [20:798].

no voltage or current can be produced. Factors (1) and (2) are a total loss mechanism, while (3) and (4) produce a finite number of electron-hole pairs, although some of the incident light is converted to heat (phonons) in (4).

Overall, the losses associated with these effects are approximately 55% of the input. Furthermore, these losses are the largest single reason why conventional solar cells cannot produce an output equal to the energy of light incident on the cell [16:27].

Recombination Losses. Once an electron-hole pair is created in the solar cell, the electron must be separated from the hole to produce useful energy. If an electron-hole pair is created within the space charge region, the electron is immediately swept to the n-side and the hole to the p-side. Since the n-side has many orders of magnitude more electrons than holes, the probability of an electron recombining on the n-side is small. The same is true for a hole on the p-side. However, most electron-hole pairs created by photon absorption are not generated within the space-charge region [18:121]. Therefore, the probability of separating an electron and hole before they recombine will depend on how close the elctron-hole pair is created to the pn-junction. If an electron-hole pair is created on the p-side, the electron has a high probability of recombining with the numerous holes on the p-side. Likewise, when an electron-hole pair is created on the n-side, the hole has a high probability of recombining with the numerous electrons on the n-side. Therefore, the probability of separating electrons and holes is also dependent on the minority

carrier diffusion lengths in the n-materials and p-materials. The minority diffusion lengths in the n-materials (L_n) and p-materials (L_p) are [19:59]:

$$L_n = (D_n \tau_n)^{1/2} \tag{27}$$

and

$$L_p = (D_p \tau_p)^{1/2} \tag{28}$$

where τ_n and τ_p are the minority carrier lifetimes in the n-materials and p-materials (with units of seconds), and D_n and D_p are the diffusion coefficients for minority carriers in the n- and p-materials, respectively (with units cm^2/s). Typical values for diffusion lengths in Si are on the order of 100 um. One might note that if a solar cell was made very thin, the electron-hole pairs would always be created very close to the junction. However, thin solar cells are very fragile, and do not completely absorb all incident light (a portion is transmitted) which results in additional loss. A thin solar cell which traps the light within the cell might, however, increase the efficiency.

Recombination of electron-hole pairs in silicon are caused primarily by indirect recombination. The actual mechanisms which cause electron-hole recombinations are empty, or dangling bonds from impurities or defects, which can capture free electrons or holes [16:29].

Radiation in space is the primary source for causing defects in satellite solar cells. When a high energy particle impinges upon the silicon substrate, it may displace a silicon atom from the lattice, and thus create a dangling bond in the vincinty of the vacancy. Consequently, the greater the number of defects, the shorter the diffusion length of minority carriers, and the greater the probability of recombination. Figure 2-12 shows the effect of electron damage on three

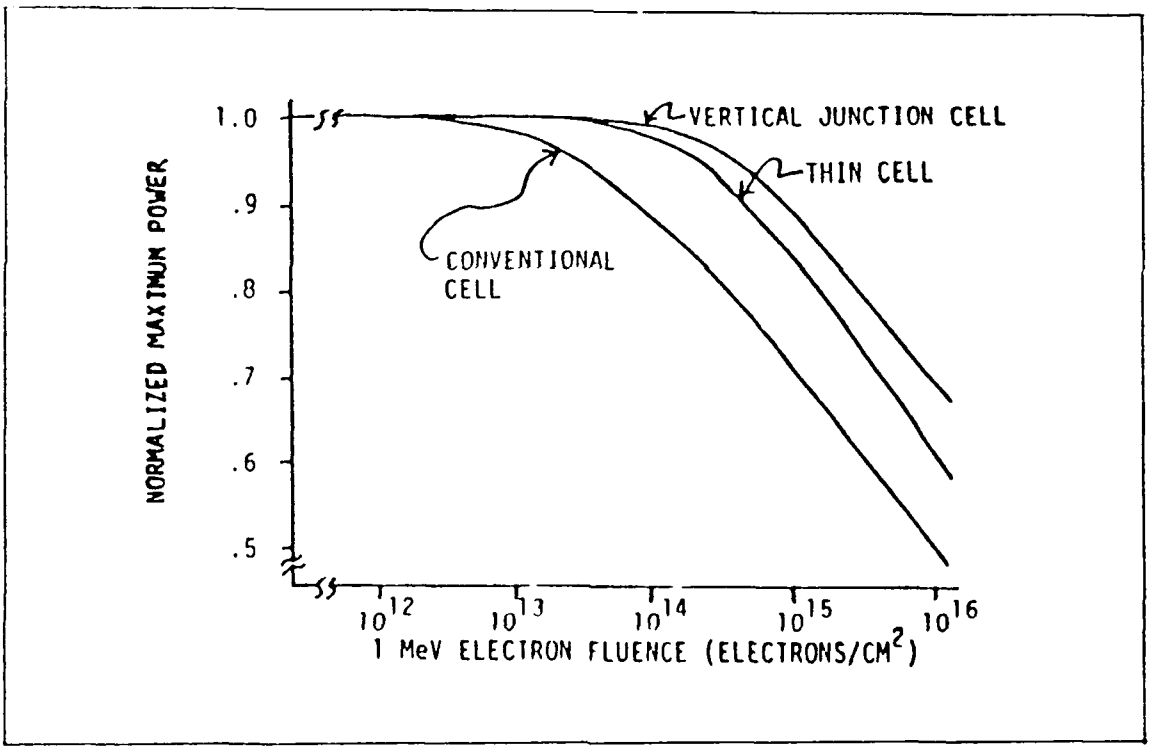


Figure 2-12. Solar cell geometry effects versus electron damage [24:379].

different types of solar cells. The surface of a solar cell is also a primary source of dangling bonds and defects;

therefore, it is notorious for creating recombination centers.

Resistance Effects. Resistance losses in solar cells are contributed from: (1) the bulk of the base material, (2) the thin top-surface layer typical of many cells, and (3) the interface between the cell and the electrical contacts, as shown in Figure 2-13 [16:30].

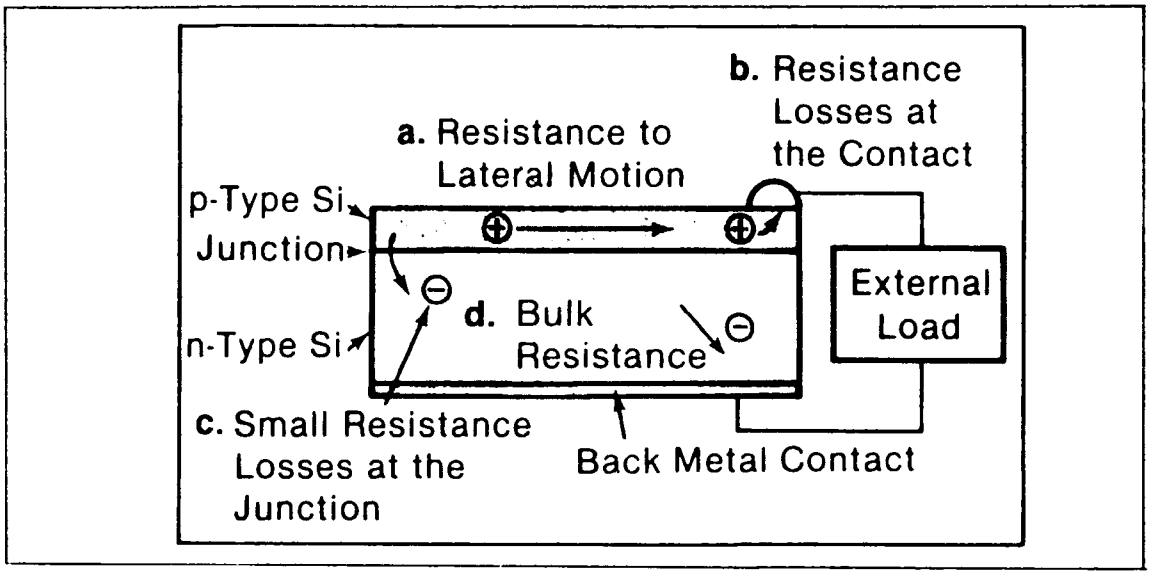


Figure 2-13. Most pn-junction cells have a very thin top layer. The resistance to lateral current flow is large for electric charges in this thin layer (a). Similarly, resistance losses are large at the electric contact (b), because of the poor interface between materials where disruptions in the atomic structure obstruct movement of charge carriers. There is even some resistance loss at the junction (c) where the carriers, although accelerated, may lose some energy. The bulk of the material also has a finite resistance (d) [16:31].

Resistance losses lower the voltage to the load and enhance the chance of recombination of electron-hole pairs, and

thus, reduces the current [16:30]. Usually it is better to highly dope the semiconductor to reduce resistance; however, large doping concentrations can decrease the mobility and shorten the diffusion lengths [16:30]. Figure 2-14 shows the effect of doping concentration on the mobility of minority carriers in Si.

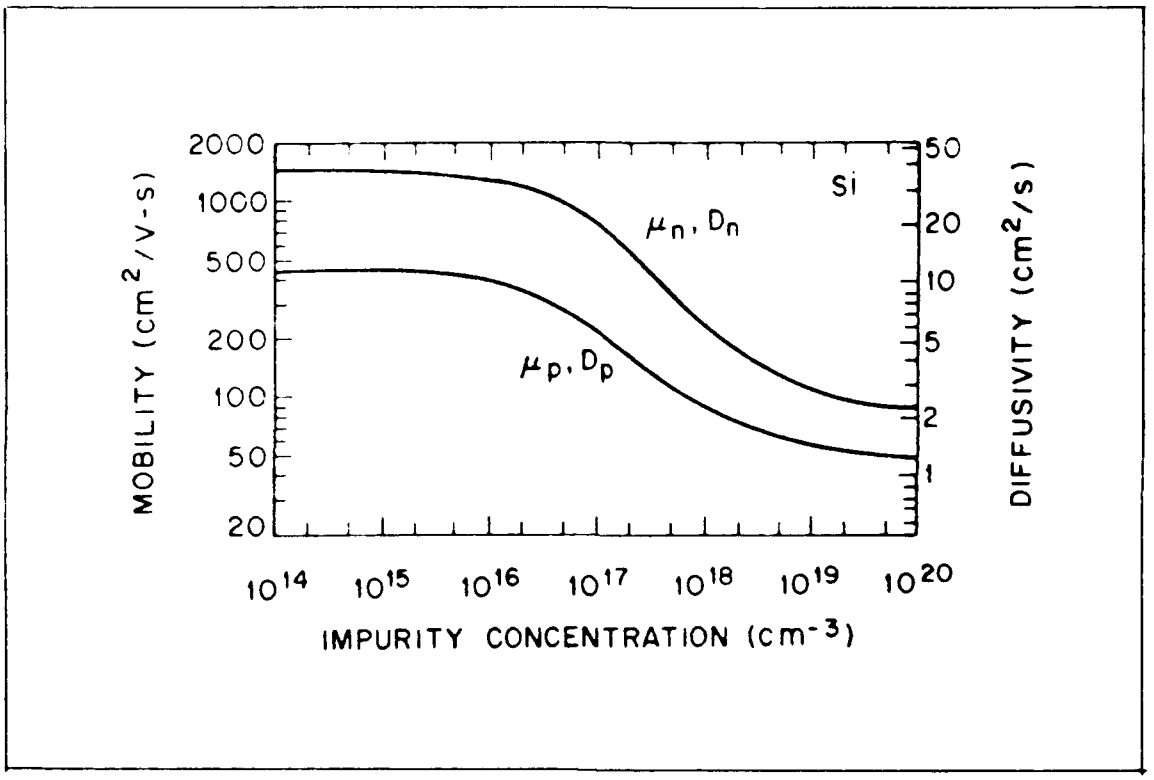


Figure 2-14. Mobility and diffusivity in silicon at 300 K as a function of impurity concentration [19:34].

A series resistance of only 5 ohms can reduce the available power of solar cells to less than 30% of the maximum power [19:294]. Reducing the spacing between the elements in the electrode grid structure decreases the

resistance losses in the top surface; however, the result is self-shading which is itself a source of inefficiency.

Self-shading. To prevent the loss of power due to resistance in the top surface, a trade-off between resistance and shading must be made. Normally, a solar cell's top surface is covered with an electrode structure consisting of narrow conducting fingers (Figure 2-1). This electrode arrangement allows charge carriers to reach a low resistive medium quickly after generation and separation. However, these grid like structures are generally metallic materials which reflect a large portion of the incident light shading the silicon. Losses due to shading range from 3% to 20% of the incident light; a typical value is approximately 8% [16:32]. Some innovative solar cell designs place the contacts on the backside of the solar cell. Thus, no loss due to shading occurs. One such cell is the interdigitated back-contact solar cell [10:337]. Such a cell was shown in Figure 1-8.

Two Innovative Solar Cell Designs

The back-contact vertical-junction solar cell concept combines the features of two innovative designs. The two solar cell designs are the vertical-junction solar cell, and the interdigitated back-contact solar cell. Of primary concern is how the features of these two cell designs

compensate for particular factors which ordinarily would decrease the efficiency of a solar cell. It is these features that the back-contact vertical-junction solar cell will take advantage of. Each design will be discussed separately.

Vertical-Junction Solar Cell. In the last section, the factors which effect the efficiency of a solar cell were discussed. Now, the vertical-junction (VJ) solar cell will be described. Of major significance is its construction which minimizes certain efficiency limitations which are characteristic of the conventional planar solar cell. However, first a description of the present day VJ solar cell will be presented.

Description. The vertical-junction solar cell is fabricated using a (110)-oriented silicon wafer. The grooves are anisotropically etched in the top surface using a solution of heated potassium hydroxide (KOH) in water. This etching procedure is described by Kendall [12]. The resulting grooves are approximately 5 microns wide, and spaced 15 to 20 microns apart [6:1]. This pattern has evolved to the wedged-channel vertical-junction pattern (shown in Figure 1-6) which has improved the cell's mechanical strength. The depth (d) of the grooves is related to their length (l) by a relationship approximating $d = l/((2)(3)^{1/2})$ [8]. Figure 1-6b and 1-6c show the cross

section of the VJ solar cell viewed from two different angles. The side walls and the end walls are all {111} planes. Since the {111} planes etch much slower than the {110} planes, the grooves stop etching when the {111} planes meet. The top surface is doped so that the diode junction follows the surface of the groove walls, as shown in Figure 1-6 . Electrical contacts are spaced periodically to provide contact to the top diffusion layer.

Efficiency Improvements. The major factors which improve efficiency in the VJ solar cell are as follows:

1. reduced reflection of incident light,
2. electron-hole pair recombination is reduced, and
3. the cell is less susceptible to degradation due to radiation damage.

Reduced Reflection. One advantage the VJ solar cell structure offers is that light normal to the surface enters a groove and is completely absorbed as a result of the inner angles of the groove walls. Figure 1-3 illustrates the principle of multi-reflection inside the grooves and how it can lead to total absorption, and hence, to a "black surface" [4:5]. The grooves are pointed by performing a short planar etch following the orientation dependent etch (ODE). Figure 2-15 shows how the grooves appear before and after a texture or planar etch is accomplished to point the top of the groove walls. Because

of the cell's excellent absorption characteristics, it is often called the nonreflecting vertical-junction solar cell [22].

Reduced Recombination. A major advantage of the VJ solar cell compared to conventional planar cells is the short distance minority carriers must travel to reach a pn-junction. One problem the planar cell has is that electron-hole pairs may be created deep in the bulk of the cell at a distance several diffusion lengths from the junction. Therefore, the minority carrier would have a small probability of moving both in the right direction and far enough before recombining. Since the walls of the VJ solar cell are very thin, carriers generated in the walls by incident light are always close to the collecting junction [23:1]. Therefore, the junction is always well within a diffusion length. The result is a higher probability of utilizing electron-hole pairs before they recombine. For silicon solar cells at 300 K, a 25% reduction in efficiency can occur due to recombination [19:295]. Therefore, the VJ solar cell offers a large improvement due to the reduced recombination of minority carriers.

Improved Radiation Resistance. When radiation damage occurs in a silicon lattice, the atomic structure is disturbed, resulting in defects and dangling bonds within the bulk of the silicon. These defects provide

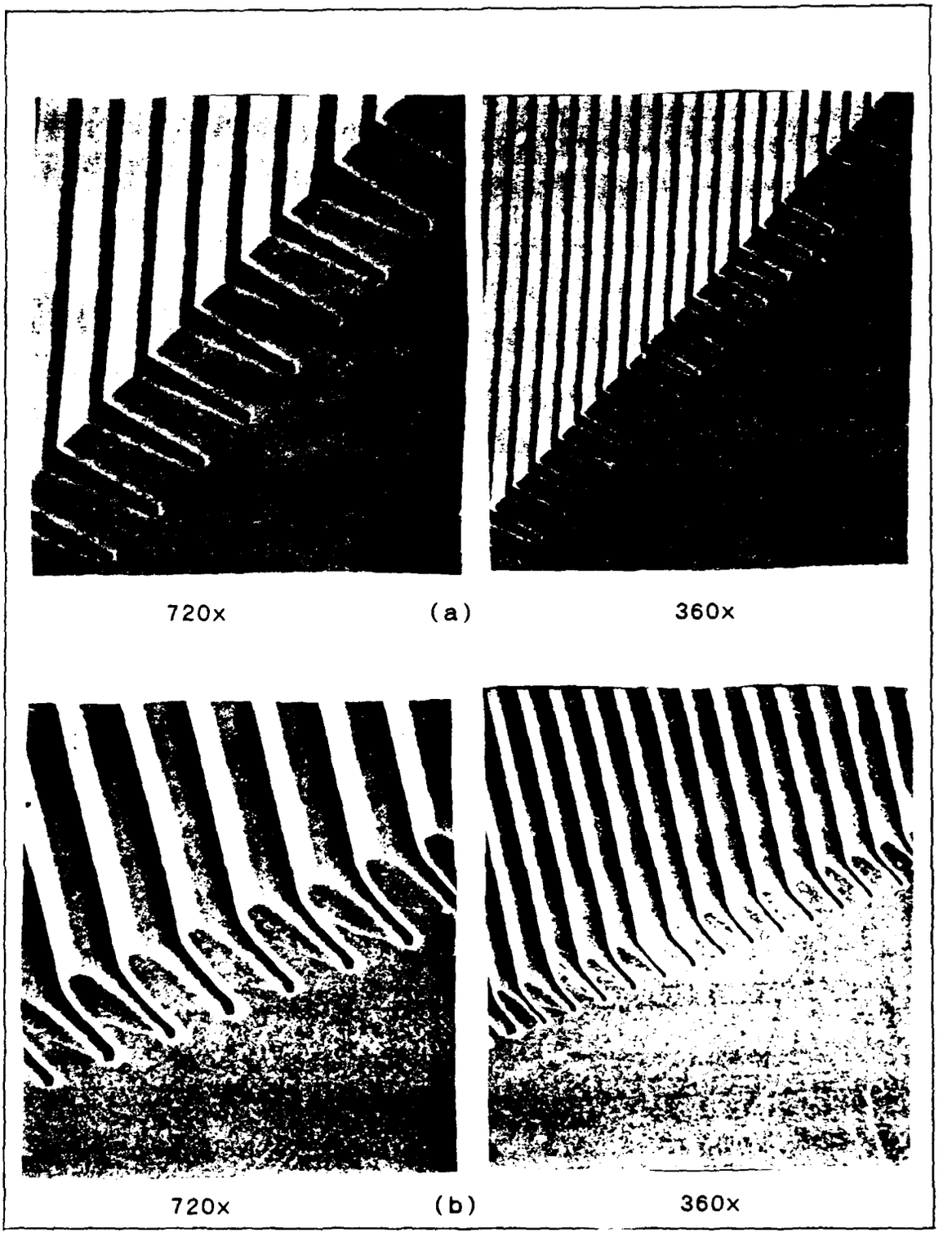


Figure 2-15. SEM pictures of wall rounding: (a) Before texture etch, (b) After texture etch [6:10-11].

recombination centers and decrease the minority carrier lifetime. Consequently, diffusion lengths are shortened and fewer electron-hole pairs are separated, since the probability of recombination is higher. This effect, of course, degrades the efficiency of the solar cell.

The VJ solar cell has such short distances between junctions, that even if the diffusion length is shortened, the efficiency is not seriously affected. Research by the Solarex Corporation has shown that VJ solar cells have the best end-of-life efficiencies of any current solar cell design [23:65]. Figure 2-12 illustrated a comparison of a conventional cell, a thin cell, and a VJ solar cell output after irradiation at various fluences (electrons/cm^2). The vertical-junction solar cell had the highest output power after irradiation.

Interdigitated Back-Contact Solar Cell. The interdigitated back-contact solar cell [10:337] design represents an effort to improve the efficiency by locating all metal contacts on the backside of the device. In the conventional cell, a metallic grid electrode pattern is placed on top of the cell to lower the internal resistance of the thin diffused surface layer. However, the addition of the metal grid results in shading of the solar cell which decreases its efficiency. The interdigitated back-contact solar cell, shown in Figure 1-8, organizes all contacts on

the backside. Therefore, losses due to shading are eliminated.

A disadvantage of this design is that most electron-hole pairs are generated near the top surface of the cell. Consequently, the electrons and holes must diffuse through the bulk of the cell before reaching the potential barrier (pn-junction) which separates them. This long diffusion distance results in an increased probability of electron-hole recombination due to material defects and radiation damage, which can lower the solar cell's efficiency. Another disadvantage is that the solar cell's top surface must be treated with an anti-reflection coating, or else 36% (or more) of the incident light is reflected [16:24]. In spite of these disadvantages, solar cells using the interdigitated back contact design have achieved efficiencies of 20% when exposed to light concentrated to 88 suns [15:661]. However, these high-efficiency cells would be of little use after exposure to radiation in space.

Combining the Two Solar Cell Designs

The proposed back-contact-vertical junction solar cell is a design which attempts to combine the best features of the vertical-junction solar cell with the interdigitated back-contact cell. This proposed design is hoped to render a solar cell with no reflection, low internal resistance,

short diffusion lengths, low degradation due to radiation damage, a lower probability of electron-hole recombinations, and no self-shading. If sucessful, these improvements point toward a highly efficient and radiation tolerant solar cell.

The primary difficulty in combining the two cell designs is connecting the front diffusion layer to the back metallic grid pattern. This can be accomplished by etching the grooves from the cell's top surface to the bottom surface. Since the side walls are vertical and the end walls etch at approximately 30° (discussed in Chapter III) with respect to the plane containing the cell's surface, the length of the groove determines the depth of the groove. By starting with a groove of the proper length, it can be etched through the silicon so that, just as the groove etches through the backside of the wafer, etching will cease. Etching ceases because all planes within the groove are {111}-oriented planes, which etch approximately 400 times slower than the plane of the cell's surface, which is oriented (110) [12]. Contact can now be made to the front surface diffusion layer through a small slit created when the groove etches through the backside. If the grooves are properly sized and spaced, the slits will align, and a metal conductor can be used to connect them. This metal conductor forms the (n^+)-contact point. The (p^+)-contact can be placed between the (n^+)-conductors in parallel with the rows

of small slits. The proposed back-contact vertical junction solar cell design is shown in Figure 1-9. The top of the solar cell is essentially a black body since all light entering a groove is absorbed.

III. Design of a Back-Contact Vertical-Junction Solar Cell

In this chapter, a method of combining the vertical-junction solar cell and the interdigitated back-contact solar cell into a single cell design, and optimizing that design, is discussed. Since combining the best features of these two solar cell designs did not result in an inflexible design, several options are discussed. Consideration of these design options revealed potential advantages and disadvantages which ultimately led to the a final design. The final design is discussed in detail. To optimize the final design, a specific groove length had to be specified. This length was determined theoretically and verified experimentally with a test-groove pattern. The test-groove pattern was etched into a silicon test wafer. Although the results of the test-groove etching experiment were used to optimize the final design and determine its feasiblity, the results are not presented until Chapter V along with the solar cell fabrication results.

Design Considerations

The initial concept for configuring the back-contact vertical-junction solar cell is shown in Figure 3-1. This design consists of grooves that are etched into the backside of a (110) wafer and are on the order of 25 um wide and

200 um deep. Each groove was doped with n+ to form a junction along the surface of the groove wall. A p+ diffusion pattern was positioned between each of the grooves to minimize the distance holes must flow to reach a metal contact. Aluminum contacts were thermally evaporated (or sputtered) on the backside and etched so that the metal was left only on the p+ patterns and n+ walls of the grooves. An anti-reflection (AR) coating was placed on the top surface to minimize reflection.

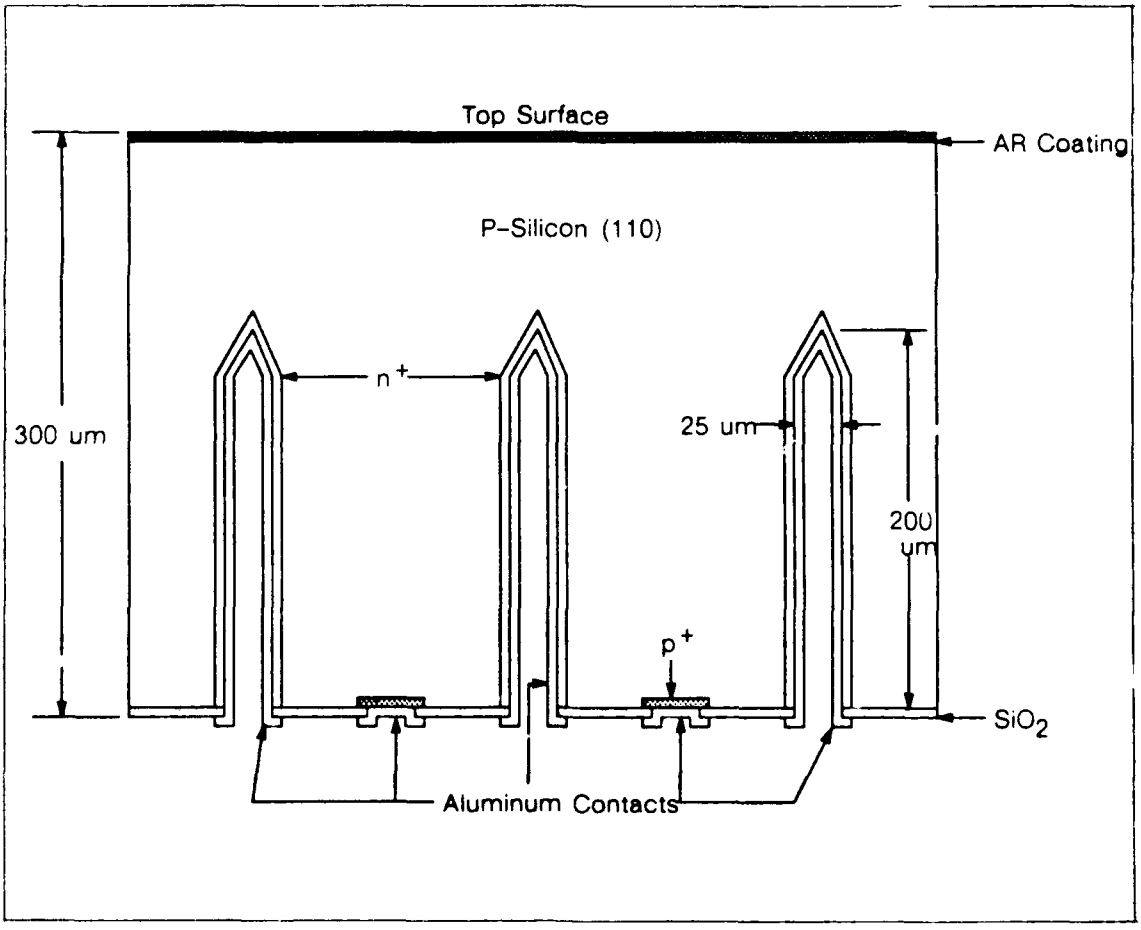


Figure 3-1. First design iteration.

This design has the advantage of no shading since the contacts are on the backside. Another advantage is that the distance minority electrons have to diffuse to reach a junction is less, provided an electron-hole pair is created deep in the bulk of the cell. However, 50% of the sunlight incident on silicon is absorbed in the first 3 micrometers of the silicon substrate [16:45]. Therefore, most of the electron-hole pairs are created near the top of the cell. To take advantage of this fact, a second design iteration was made.

Figure 3-2 shows the result of the second design iteration. The difference between this design and the first design is that the n+ grooves are etched all the way to the top surface, and the p+ runs are now inside a groove that is etched approximately two-thirds the distance toward the top surface. This design had an n+ layer on the top surface to take advantage of the large number of electron-hole pairs created in this region. Since the n+ grooves contacted the top diffusion layer, no electrical contacts were needed on the top surface. This design iteration essentially combined a planar cell with the vertical junction and interdigitated back-contact cell designs.

This second solar cell design possessed several disadvantages. One disadvantage was the possibility of shorting between the closely spaced contacts on the

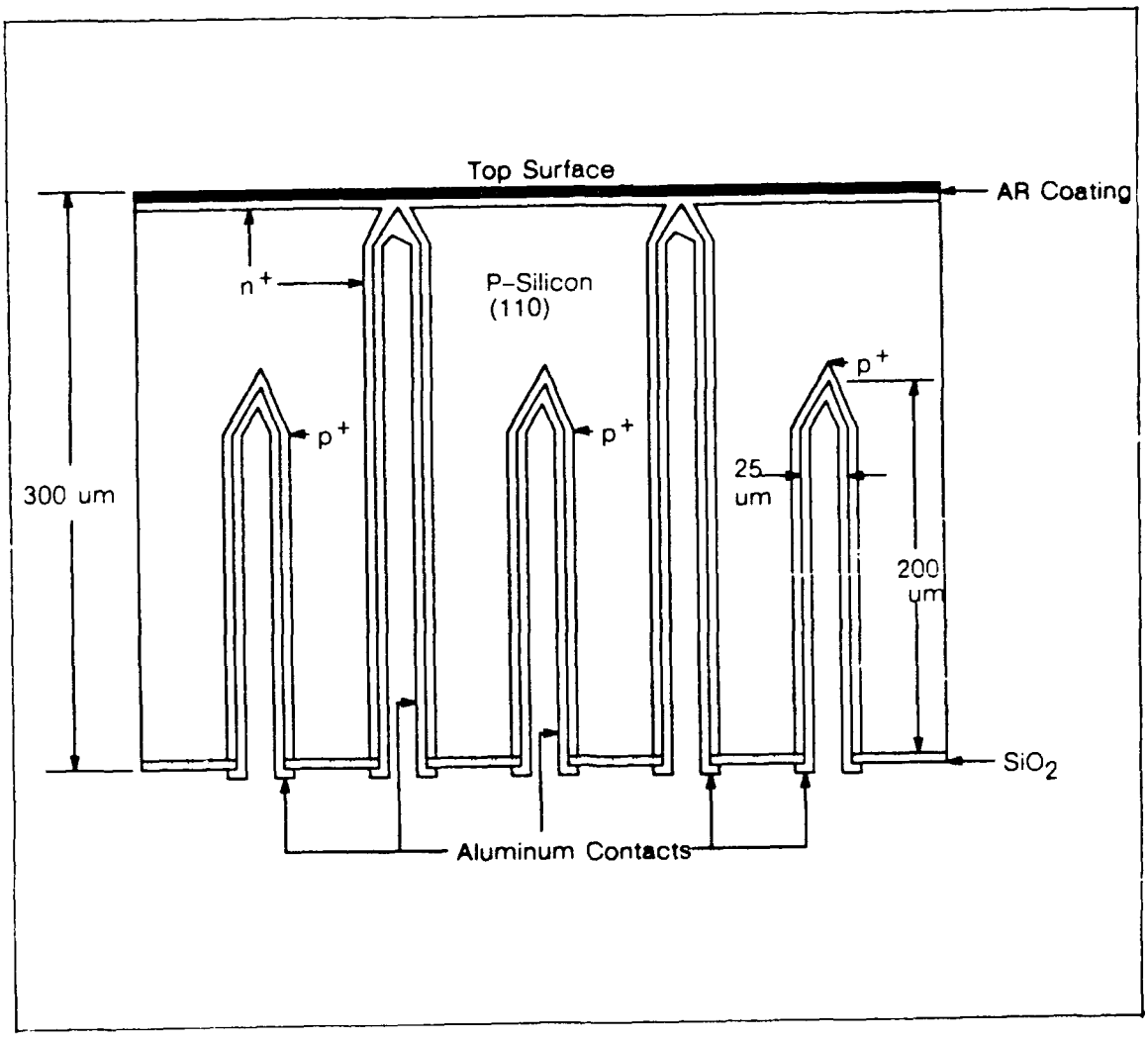


Figure 3-2. Second design iteration

backside. Therefore, the grooves need to be spaced far enough apart to prevent shorting between the n+ contacts and the p+ contacts. However, increasing the distance between the grooves defeats the purpose of the grooves, since the minority carrier electrons must now diffuse a longer distance. Consequently, recombination would be increased which lowers the solar cell's efficiency. Another

disadvantage concerns the fabrication of this design. In order to diffuse (p+) and (n+) into the same surface, photoresist would have to be applied to mask the interior of the grooves. This photoresist may be difficult to remove, and any residue will cause problems. A third disadvantage was the fact that the top surface was just like a planar cell which, unless properly treated with several anti-reflection coatings, is highly reflective. Consequently, a third design iteration was accomplished to resolve these deficiencies. This iteration is referred to as the "final design" and is described in the next section.

Final Design

One of the major advantages of the vertical-junction solar cell is its ability to absorb virtually all incident light. Since the walls of the grooves can be easily pointed, any light striking a vertical-junction solar cell enters a groove and is trapped. This feature was shown in Figure 1-3 (Chapter I). In order to capitalize upon this advantage, the grooves should be positioned on the topside of the solar cell. Therefore, the third design iteration utilized this concept. This design was given the name back-contact vertical-junction (BCVJ) solar cell. Figure 3-3 shows how the grooves on the BCVJ solar cell are configured on the topside to yield enhanced structural

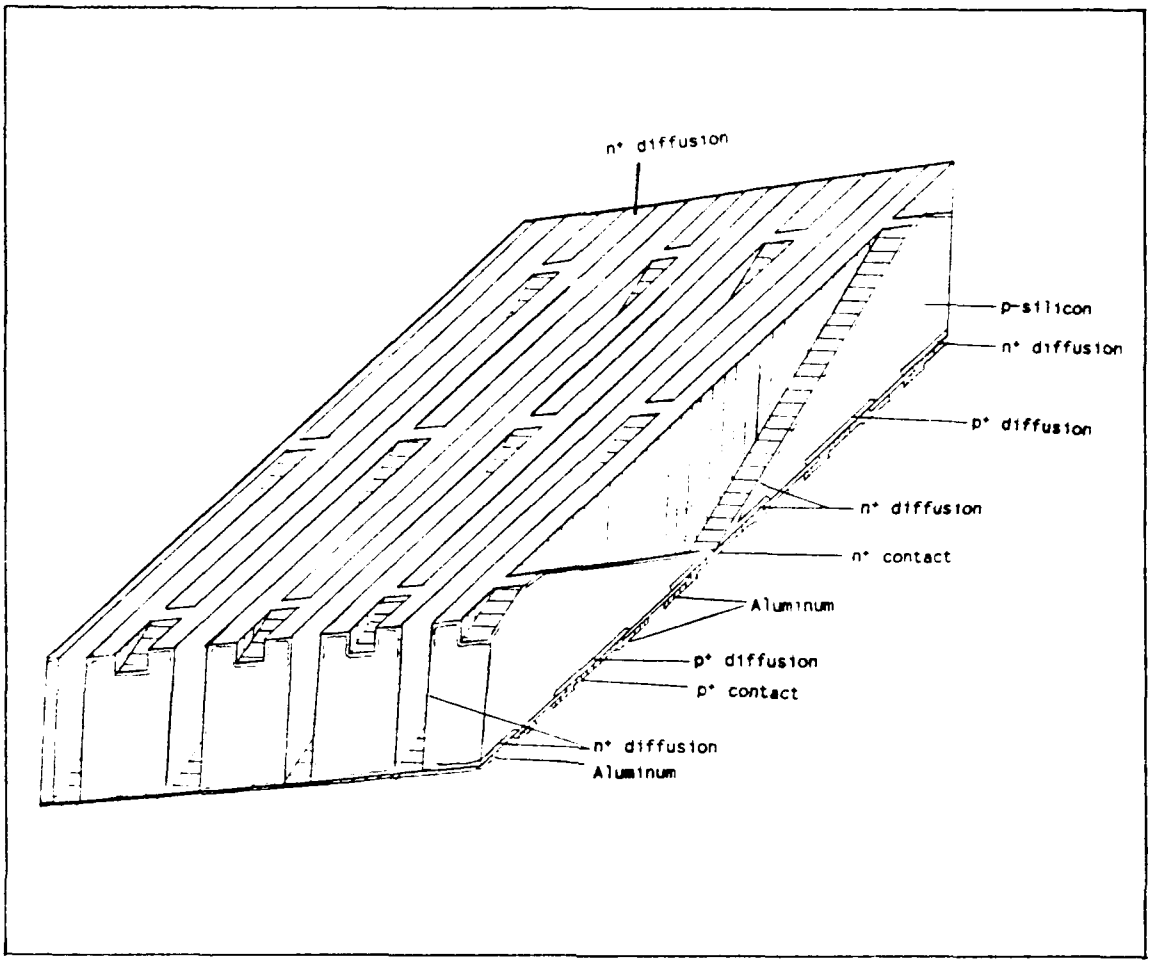


Figure 3-3. Final back-contact vertical-junction solar cell design with the grooves positioned on the top surface.

stability by using the concept of the wedged-channel vertical-junction solar cell described in Chapter I (see Figure 1-6). The grooves are all doped n+ and are etched so that they just barely reach the backside before all the {111} planes converge. The connection to the top surface is made through a diffusion path around each slit at the bottom of each groove. Since the slits etch through the backside

in a linear array, the slits can easily be connected with an n+ contact and metallization pattern. The p+ contact and metallic conductor is positioned between the linear array of slits. Since the linear arrays of slits are periodically spaced a distance equal to half the length (approximately 500 um) of a groove, the possibility of an n+ metal electrode shorting to a p+ metal electrode is considerably less. Consequently, the width of the groove, as well as the distance between the grooves, can now be decreased without decreasing the distance between the metallic conductors. This feature allows the grooves to be very narrow and the walls to be very thin without seriously affecting the metallization electrode spacing. This design should possess short diffusion lengths and very low reflection.

One major problem with this design was determining the relationship between the depth of a groove versus its length and width. To optimize this design, this relationship had to be determined.

Design Optimization

In order to optimize this design, the exact length of a groove and the smallest possible width that would allow a groove to barely etch through the backside had to be determined. According to the literature, the inside of a groove consists of only {111} planes [13:1188]. However, a

quantitative relationship involving the depth of a groove to its length and width was not found. Therefore, the groove geometry was determined theoretically based on the convergence of the {111} planes. Next an equation relating the depth of a groove to its length and width was developed. Finally, the quantitative relationship was verified experimentally by etching grooves with various lengths and widths. To show how the geometry of the groove was determined, the following will be discussed: (1) the development of a quantitative relationship, and (2) experimental verification of the quantitative relationship with a test-groove pattern. The experimental results of the groove etching is given in Chapter V.

Groove Geometry. To determine the groove geometry, a model was constructed from index cards showing the various {111} planes in a silicon lattice. Figure 3-4 shows the groove geometry and the different planes which define it. The angle (θ) between the two planes with $(h_1 k_1 l_1)$ and $(h_2 k_2 l_2)$ can be calculated using the following formula [25:460]:

$$\theta = \cos^{-1} \frac{(h_1 h_2 + k_1 k_2 + l_1 l_2)}{[(h_1^2 + k_1^2 + l_1^2)(h_2^2 + k_2^2 + l_2^2)]^{1/2}} \quad . \qquad (29)$$

Consequently, the angles between the planes in Figure 3-4 are:

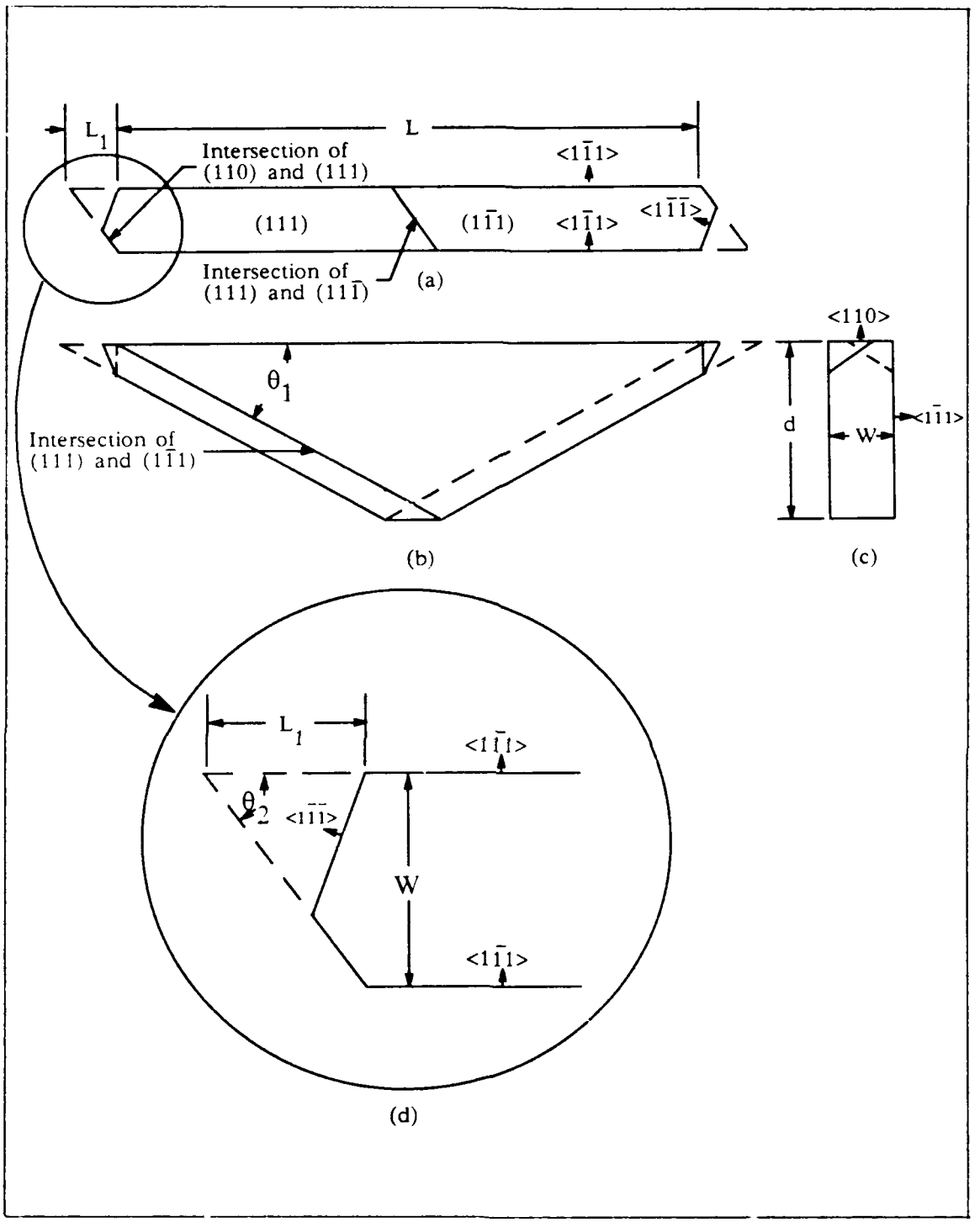


Figure 3-4. Groove geometry necessary to determine the relationship between the depth (d), length (L), and width (W): (a) Top view, (b) Side view, (c) End view, and (d) Enlarged end of top view.

Angle between (110) and (1$\underline{1}$1) = 90°

Angle between (110) " (111) = 35.26°

Angle between (110) " (11$\underline{1}$) = 35.26°

Angle between (110) " (1$\underline{11}$) = 90°

Angle between (111) " (1$\underline{1}$1) = 70.53°

Angle between (11$\underline{1}$) " (1$\underline{11}$) = 70.53°

Angle between (111) " (11$\underline{1}$) = 70.53°

Angle between (1$\underline{1}$1) " (1$\underline{11}$) = 70.53°.

Groove Depth, Length and Width Relationship. To successfully fabricate a solar cell with grooves which barely etch through the backside, an equation relating the depth (d) of the groove to the length (L) and width (W) of the groove was developed. From Figure 3-4:

$$\tan \theta_1 = d/[(L + L_1)/2]. \quad (30)$$

Solving for 'd' yields:

$$d = [(L + L_1)/2] \tan \theta_1. \quad (31)$$

Establishing L_1 in terms of the width (W) implies:

$$\tan \theta_2 = W/L_1 \quad (32)$$

so

$$L_1 = W/\tan \theta_2. \quad (33)$$

Substituting equation (33) into (31) yields:

$$d = \{[L + (W/\tan \theta_2)]/2\} \tan \theta_1 . \quad (34)$$

Rearranging yields:

$$d = (L/2) \tan \theta_1 + (W \tan \theta_1)/(2 \tan \theta_2). \quad (35)$$

In order for this equation to be useful, the angle θ_1 and θ_2 must be determined. These angles are not between specific planes but are between lines where specific planes intersect. Angle θ_1 is located between the intersection of the (110) and (1$\bar{1}$1) planes and the intersection of the (111) and (1$\bar{1}$1) planes, as shown in Figure 3-4. Similarly, angle θ_2 is located between the intersection of the (110) and (111) planes and the intersection of the (110) and (1$\bar{1}$1) planes. The lines or directions of these intersections can be represented as vectors in 3-dimensions as shown in Figure 3-5.

If

a = intersection of the (111) and (1$\bar{1}$1) planes

= -0.5i + 0.5k,

b = intersection of the (110) and (1$\bar{1}$1) planes

= -0.5i + 0.5j + k,

and

c = intersection of the (110) and (111) planes

= -0.5i + 0.5j;

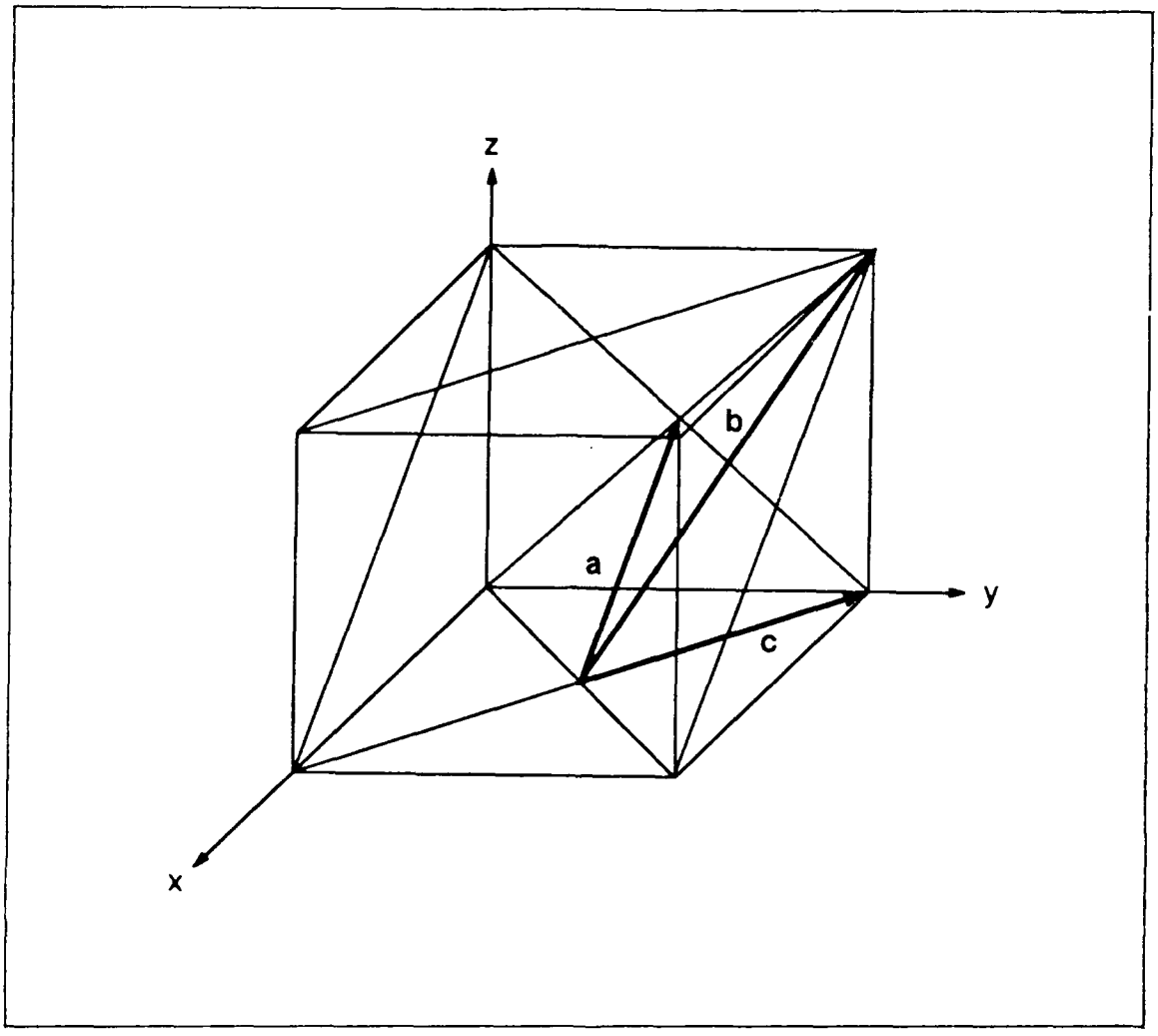


Figure 3-5. Vectors representing the intersection of specified Miller indexed planes.

then the angles between these vectors can be found by vector dot products as follows:

$$\theta_1 = \cos^{-1} (\mathbf{a}\cdot\mathbf{b})/(|\mathbf{a}||\mathbf{b}|) = 30^\circ \qquad (36)$$

$$\theta_2 = \cos^{-1} (\mathbf{b}\cdot\mathbf{c})/(|\mathbf{b}||\mathbf{c}|) = 54.73^\circ . \qquad (37)$$

Calculating the corresponding tangents yields:

$$\tan \theta_1 = \tan 30^\circ = (3)^{-1/2} \quad (38)$$

and

$$\tan \theta_2 = \tan 54.73^\circ = (2)^{1/2}. \quad (39)$$

Substituting equations (38) and (39) into (34) yields:

$$d = [L + W/(2)^{1/2}]/[(3)^{1/2}(2)]. \quad (40)$$

If the thickness (t) of a wafer is known, then equation (40) can be solved for L. The length (L) can be determined by setting d = t and choosing a value for the width (W). Solving for L yields:

$$L = d(2)(3)^{1/2} - W/(2)^{1/2}. \quad (41)$$

To verify this equation, a test-groove pattern was developed. The test-groove pattern was used to make a photolithography mask. This pattern is discussed in the next section.

Test-Groove Pattern. Since equation (41) could not be verified in the literature, it was verified experimentally. In order to verify equation (41), grooves of different widths and lengths were etched into a wafer 300 um thick. The different widths chosen were 5 um, 10 um, 25 um, 50 um, and 100 um. The test-groove pattern is shown in Figure 3-6. The theoretical length for each width was calculated using

equation (41). The results are summarized in Table 3-1. The theoretical length was selected as the length of the first groove in each set (grouped by widths) of grooves investigated. The grooves located under each theoretical value were incremented in 20 um steps above and below the theoretical value. Consequently, the theoretical value (rounded to the nearest ten) was also repeated as the sixth groove from the bottom. The actual test-groove dimensions are shown in Figure 3-6.

Table 3-1. Theoretical length (L) of a groove for a given width (W) and in thickness (t = 300 um).

Length (L) (um)	Width (W) (um)
1036	5
1032	10
1022	25
1004	50
969	100

The test-groove pattern dimensions were enlarged by a factor of 400 and cut from Rubylith at the Air Force Wright Aeronautical Laboratory. The Rubylith mask was reduced by a factor of 40 with the camera reduction equipment in the AFIT Cooperative Electronic Materials and Processes Laboratory located in Building 125, room 1065. Next, the 40x reduction image was reversed by copying. The copy was used to produce

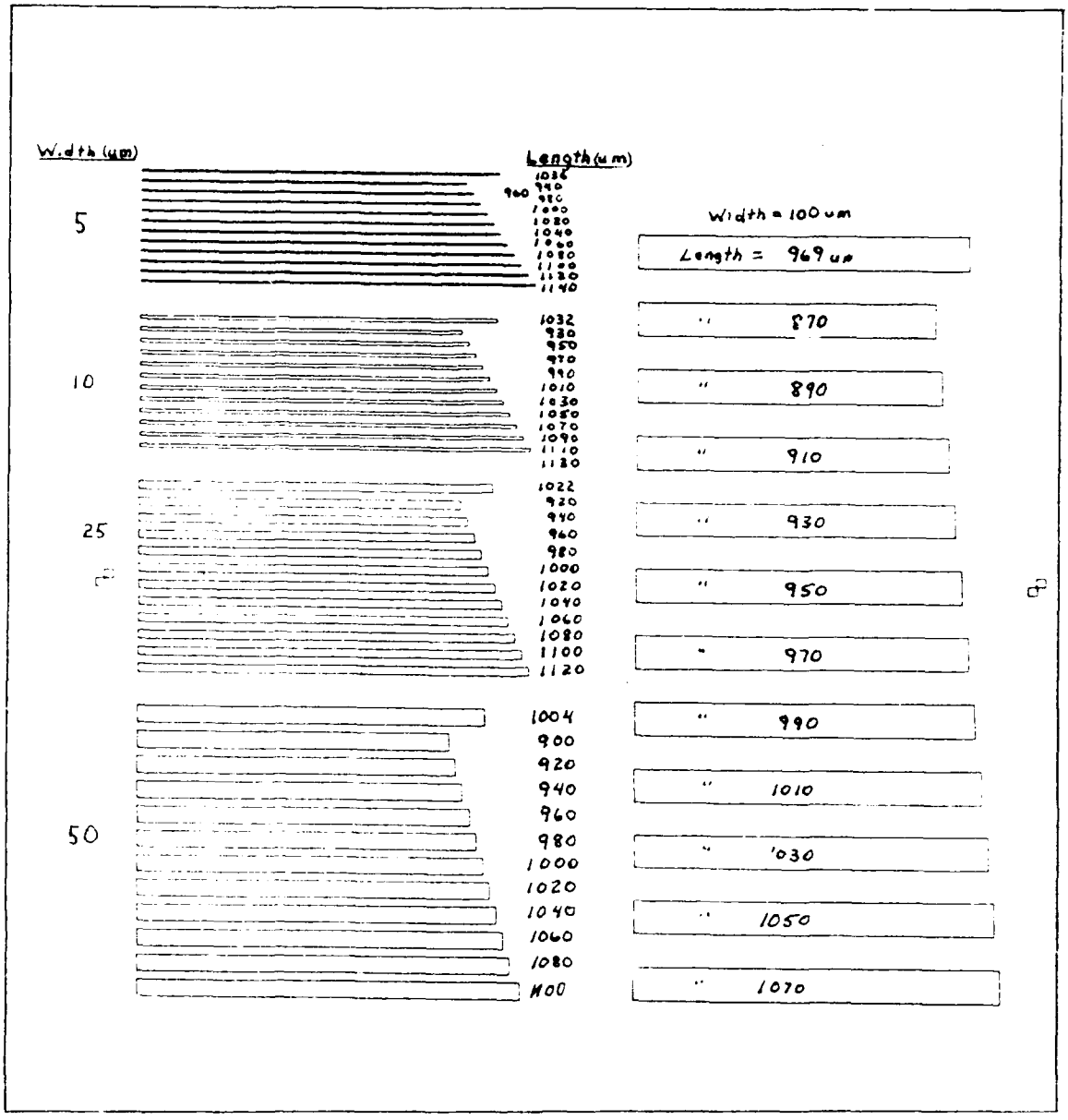


Figure 3-6. Test-groove pattern.

the reticle, shown in Figure 3.7 (for the step-and-repeat process). Since the step-and-repeat process does a 10x reduction, the total reduction was 400x. The test-groove pattern was stepped-and-repeated 64 times to make the photolithography mask shown in Figure 3-8. This mask was

used to form the groove pattern on a test wafer. The fabrication procedure to realize the test-groove wafer is the same as the fabrication of the solar cell, except the test-groove wafer was completed following the orientation dependent etching. The fabrication procedure is discuused in the next chapter.

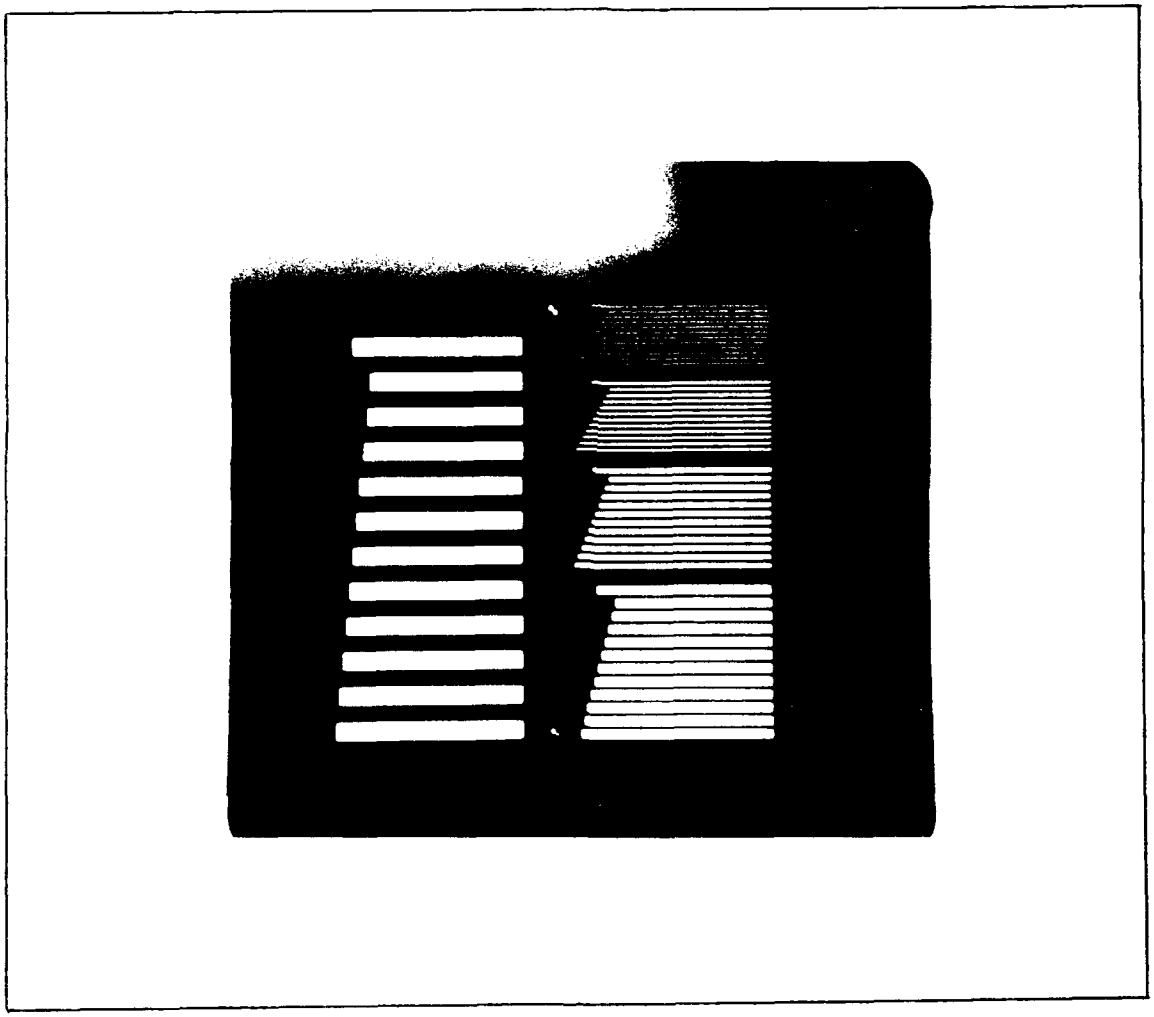


Figure 3-7. Test-groove reticle containing the test pattern which was stepped-and-repeated to produce the photolithography mask shown in Figure 3-8 (magnification 2.3x).

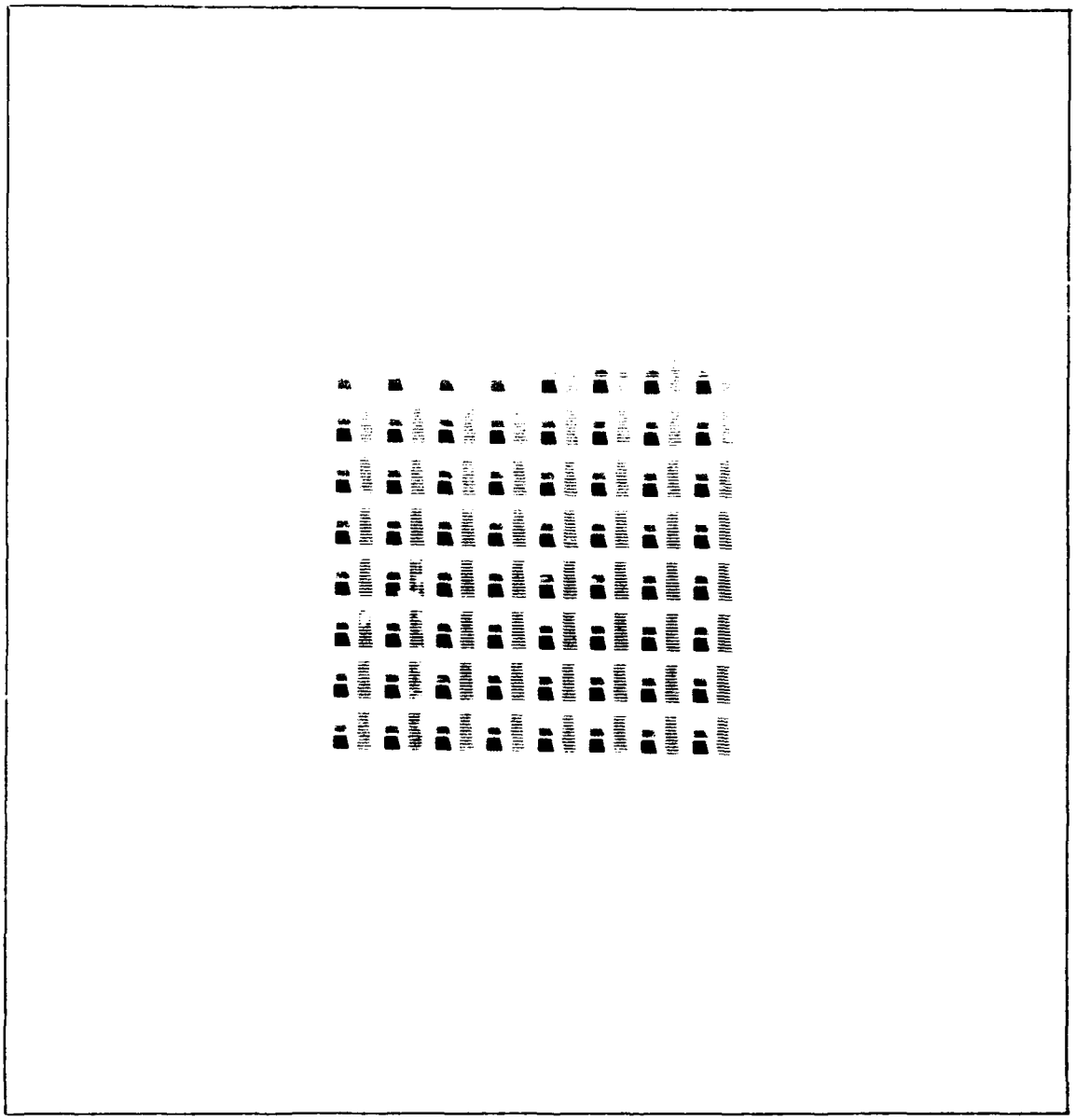


Figure 3-8. Test-groove mask after the step-and-repeat process containing an 8 by 8 array of the test groove pattern (magnification 2.3x).

IV. Fabrication of a Back-Contact Vertical-Junction Solar Cell

In this chapter, the procedures used to fabricate the back-contact vertical-junction (BCVJ) solar cell are described in detail. During the fabrication process, many different fabrication methods were experimentally evaluated and several were determined to be unsuitable. While not all of the unsatisfactory methods are explained in detail, several critical ones are discussed and remedies are proposed. The fabrication steps are described in the order of implementation. The fabrication of the BCVJ solar cell was performed in the AFIT Cooperative Electronic Materials and Processes Laboratory located in Building 125, room 1065. The fabrication results are discussed in Chapter V.

The fabrication of the BCVJ solar cell required a five-level mask set which had to be designed and produced prior to the actual solar cell fabrication. The mask designs and their production were major steps in the overall fabrication process. Therefore, the mask designs and their production are discussed first. Then a description of the BCVJ solar cell fabrication process follows.

Mask Design

The mask design used in the fabrication process was modified several times during preliminary fabrication steps in order to improve the results. For instance, the initial mask set was designed to yield a 1-inch square cell in the center of a 2-inch diameter wafer. However, the probability of a defect in such a large area due to dust motivated a redesign. The new mask set was designed to yield five 0.4-inch square cells on a 2-inch diameter wafer, as shown in Figure 4-1. The final mask designs were fabricated on 4-inch High Resolution Plates (HRPs) and consisted of five mask levels:

Level	Description
1	Groove mask
2	P+ mask
3	N+ mask
4	Contact mask
5	Metal mask

The design of each of these levels will be described next.

Groove Mask. In the groove mask design, the limitations of the mask fabrication equipment were considered. For example, the step-and-repeat equipment only allows stepping-and-repeating in integer increments of mils and is limited to a maximum reticle image of 1.5 inches. It is also fixed at a 10x reduction and has a 4 um resolution.

The first reduction camera operation is limited to a maximum rubylith image dimension of 40-inches and has a resolution of 1 mil.

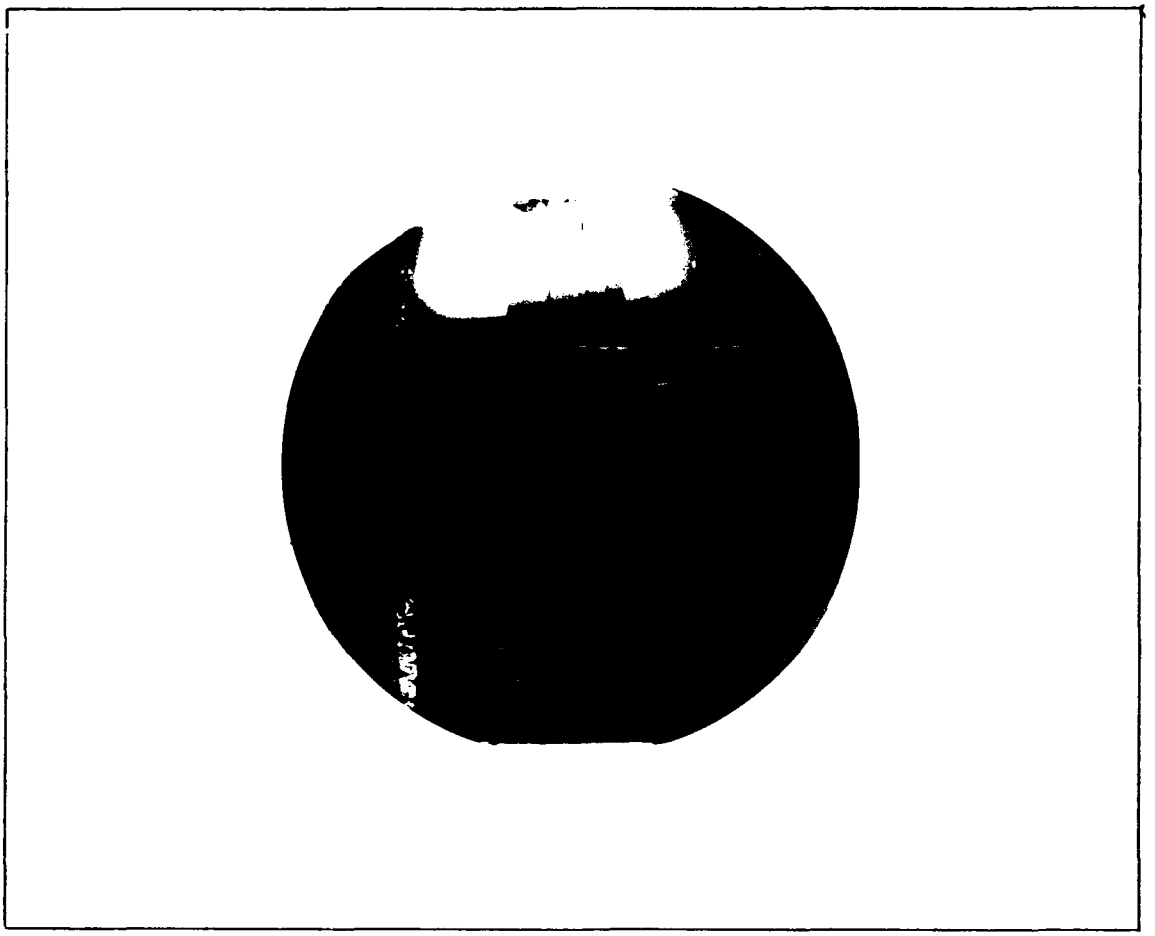


Figure 4-1. Final cell design with five 0.4-inch square cells on a 2-inch diameter wafer (magnification 1.5x).

The first step in designing the groove mask was to determine the optimum groove length, width, and separation. From the last chapter, the groove length and width was shown to be dependent on the depth of the groove. For the BCVJ

solar cell, the depth of the groove is equal to the thickness of the wafer. The thickness of the Virginia Semiconductor (Fredericksburg, Virginia 22401) (VS) wafers ranged from 290 um to 295 um. If both the depth (d) and width (W) are known, then the groove length (L) can be calculated. Since most of the VS wafers were 290 um thick, and those with a thickness slightly greater than 290 um could be chemically polished to 290 um, the thickness chosen was 290 um. This thickness also provides sufficient structural robustness to withstand the rigors of fabrication.

With the groove depth chosen, the next step was to determine the groove width, length, and separation. According to calculations made by Rahilly [2], the number of junctions per centimeter in order to achieve maximum benefit of the groove structure should be approximately 2000. This would require the groove width and separation to be as small as 5 um each, which is significantly smaller than the laboratory equipment and processing limitations. The test groove etching results (discussed in Chapter V) demonstrated that it was possible to produce 5 um wide grooves 300 um deep; however, the groove separation of 5 um was to small. Since grooves smaller than 5 um approach the resolution of the step-and-repeat equipment (4 um), 5 um was chosen for the width. With the groove depth (d = thickness of wafers)

and width (W) determined, the length (L) could be calculated from equation (41) (Chapter III) as follows:

$$L = d(2)(3)^{1/2} - w/(2)^{1/2} = (290)(2)(3)^{1/2} - (5)/(2)^{1/2}$$
$$= 1000 \text{ um.}$$

For the test-groove etching investigation discussed in Chapter III, a groove separation of 25 um was used. Based on the excellent results (discussed in Chapter V) obtained using this separation, it was believed that this separation could be as small as 15 um. However, this dimension was experimentally determined to be to small to keep the walls from etching away due to slight variations in the flat orientation from wafer to wafer. The groove mask was redesigned using a separation between the grooves of 20.4 um, and it yielded excellent results. This dimension also allowed exactly one groove per mil. This made stepping-and-repeating simpler because the step-and-repeat equipment is calibrated in mils.

Since the first reduction camera operation has only a 1 mil (25.4 um) resolution capability, and the groove width chosen was only 5 um, a groove mask could not be made with one reduction. Therefore, the only way to achieve a groove mask with the needed resolution was to step-and-repeat a pattern.

The pattern shown in Figure 4-2 was stepped-and-repeated ten times per row with an exposure spacing of 40 mils (1016 um). The pattern was 100 mils (2540 um) long and 40 mils (1016 um) wide. Each cell contained four rows of the repeated pattern. The rows were spaced 100 mils (2540 um) center-to-center. This procedure produced a continuous pattern of grooves 400 by 400 mils (10,160 um) with each groove dimension being 1000 um long by 5 um wide. The spacing between the grooves was 20.4 um on the sides and 16 um on the ends. The repeated array of grooves formed a kind of brick-laid pattern as shown in Figure 4-3. This was the pattern used in the wedged-channel vertical-junction solar cell discussed in Chapter 1.

The groove mask consisted of five square areas of grooves as shown in Figure 4-4. Each area was 0.4-inches (1.016 cm) square. Therefore, the area of each cell was 0.16 square inches (1.032256 cm^2). A row of grooves 600 mils (15,240 um) long was placed at the bottom of the groove mask to serve as an alignment mark (aligned with wafer flat) for the Virginia Semiconductor wafers. Also, a vertical line was placed to one side as an alignment mark for the Ametek (Sunnyvale, California 94086) wafers. The Ametek wafers had their flat cut perpendicular to the ($1\underline{1}1$) plane. The Virgina Semiconductor wafers had the flat cut parallel to the ($1\underline{1}1$) plane.

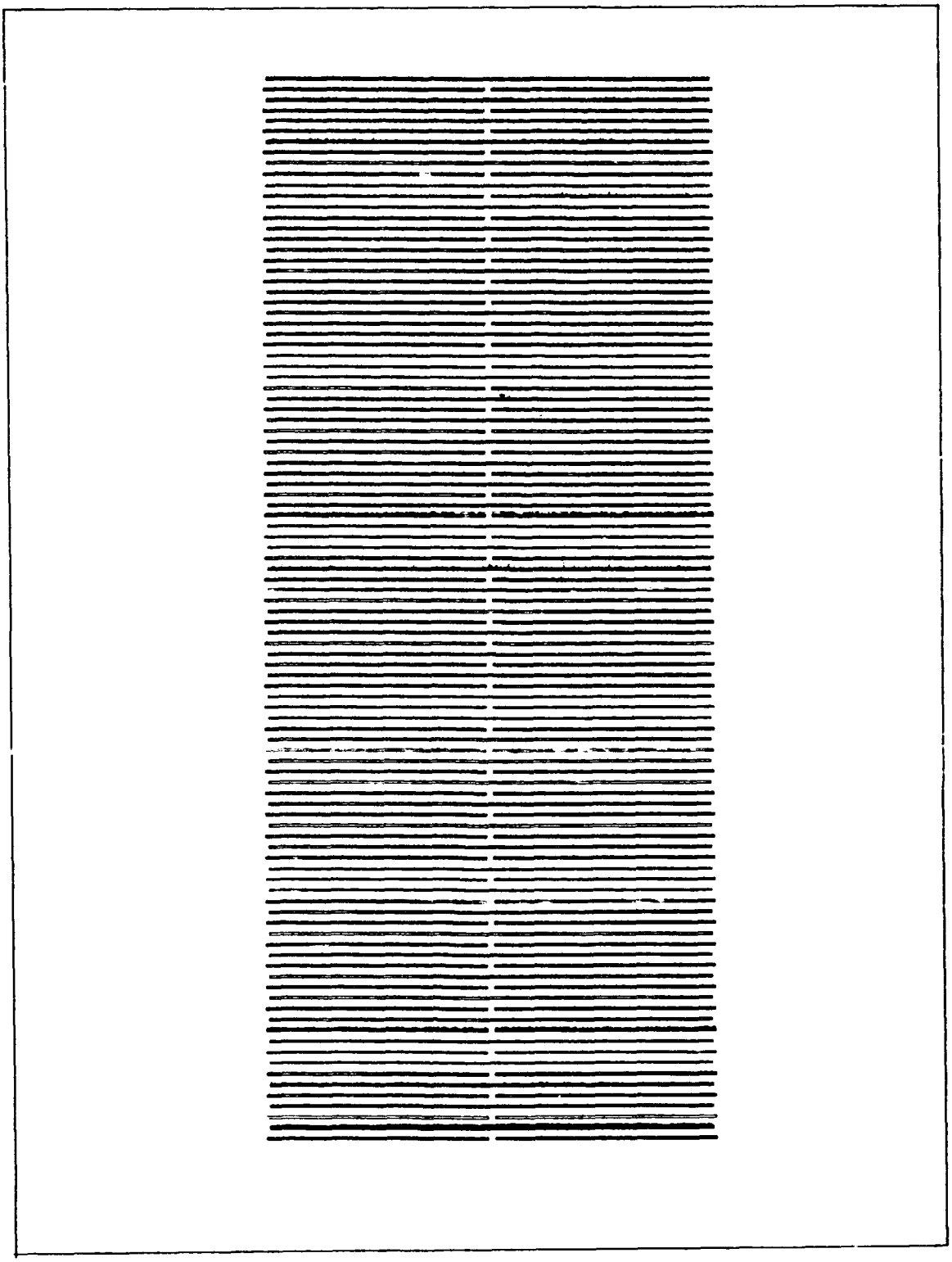


Figure 4-2. Groove pattern used in the step-and-repeat process to produce the groove mask.

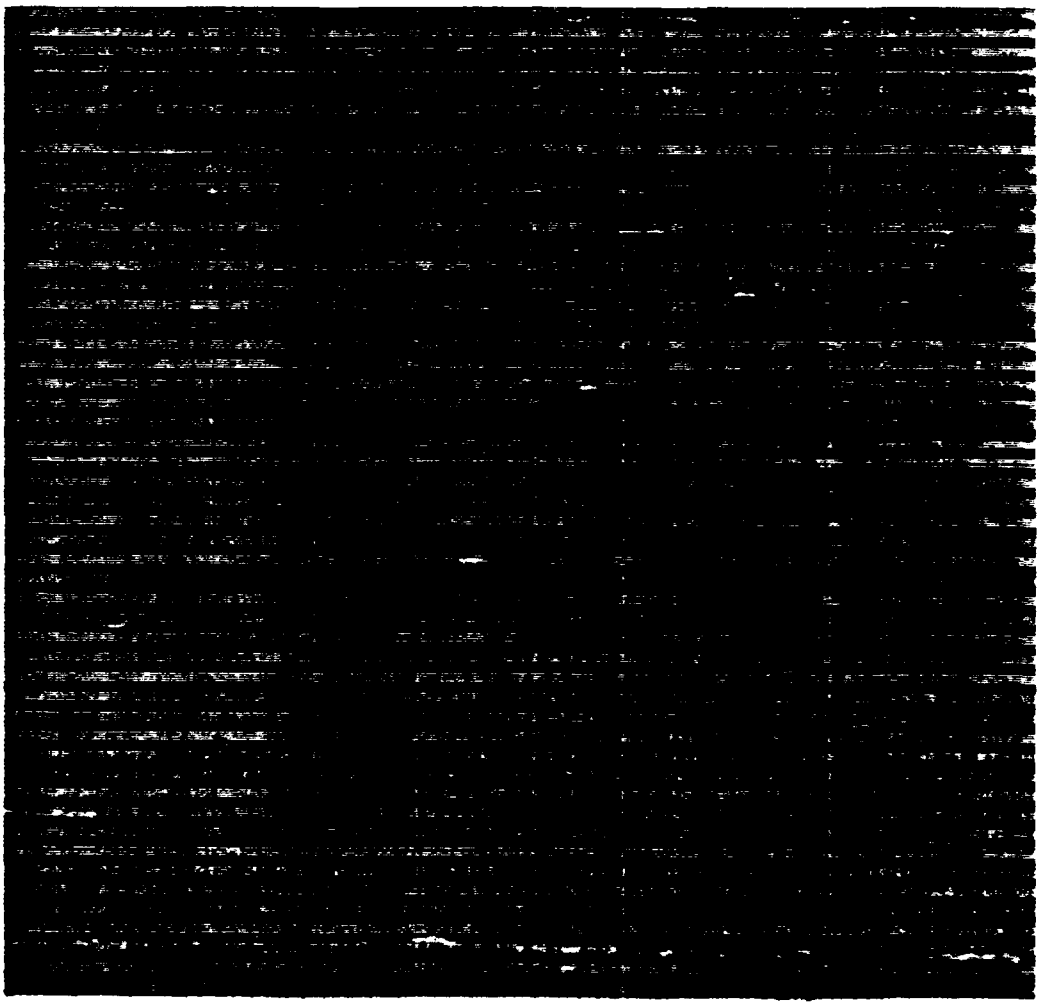


Figure 4-3. Brick-laid pattern of grooves formed by stepping-and-repeating an array of the groove pattern shown in Figure 4-2 (magnification 13.1x).

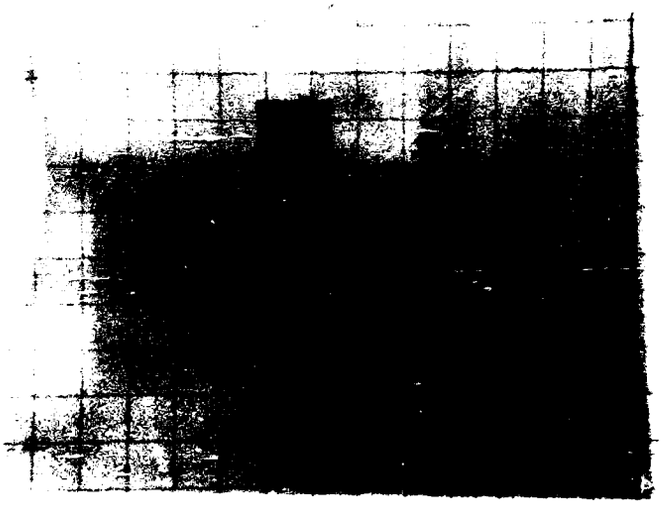


Figure 4-4. Groove mask consisting of five of the groove arrays shown in Figure 4-3 (actual size).

P+ Mask. The p+ mask is shown in Figure 4-5. This mask consisted of five identical cell patterns. An enlarged cell pattern is shown in Figure 4-6. This pattern was designed so that p+ runs could be made between the slits which form on the backside when the grooves etch through. Since the slits occur on the backside below the center of the grooves, a line of slits will occur every 20 mils (508 um). Each cell pattern was made by stepping-and-repeating a 100 mil long by 4 mil (101.6 um) wide line. Each cell consisted of five identical rows of the repeated pattern. Each row contained 20 groove patterns (Figure 4-2) spaced 20 mils (508 um) apart. Each row of the repeated pattern was spaced 100 mils (2,540 um) center-to-center. The result was 20 continuous lines 500 mils (12,700 um) long and spaced 20 mils (508 um) from center-to-center. Since the mask was symetric, alignment marks were also placed on this mask identical to the ones on the groove mask to aid in alignment.

N+ Mask. The n+ mask was identical to the p+ mask with the exception that the n+ mask had one less line. The n+ lines were designed to line up over the slits. Figure 4-7 shows the pattern for one cell. Figure 4-8 shows how the n+ pattern aligns with the p+ pattern. The complete n+ mask, with alignment marks identical to those used on the groove mask, is shown in Figure 4-9.

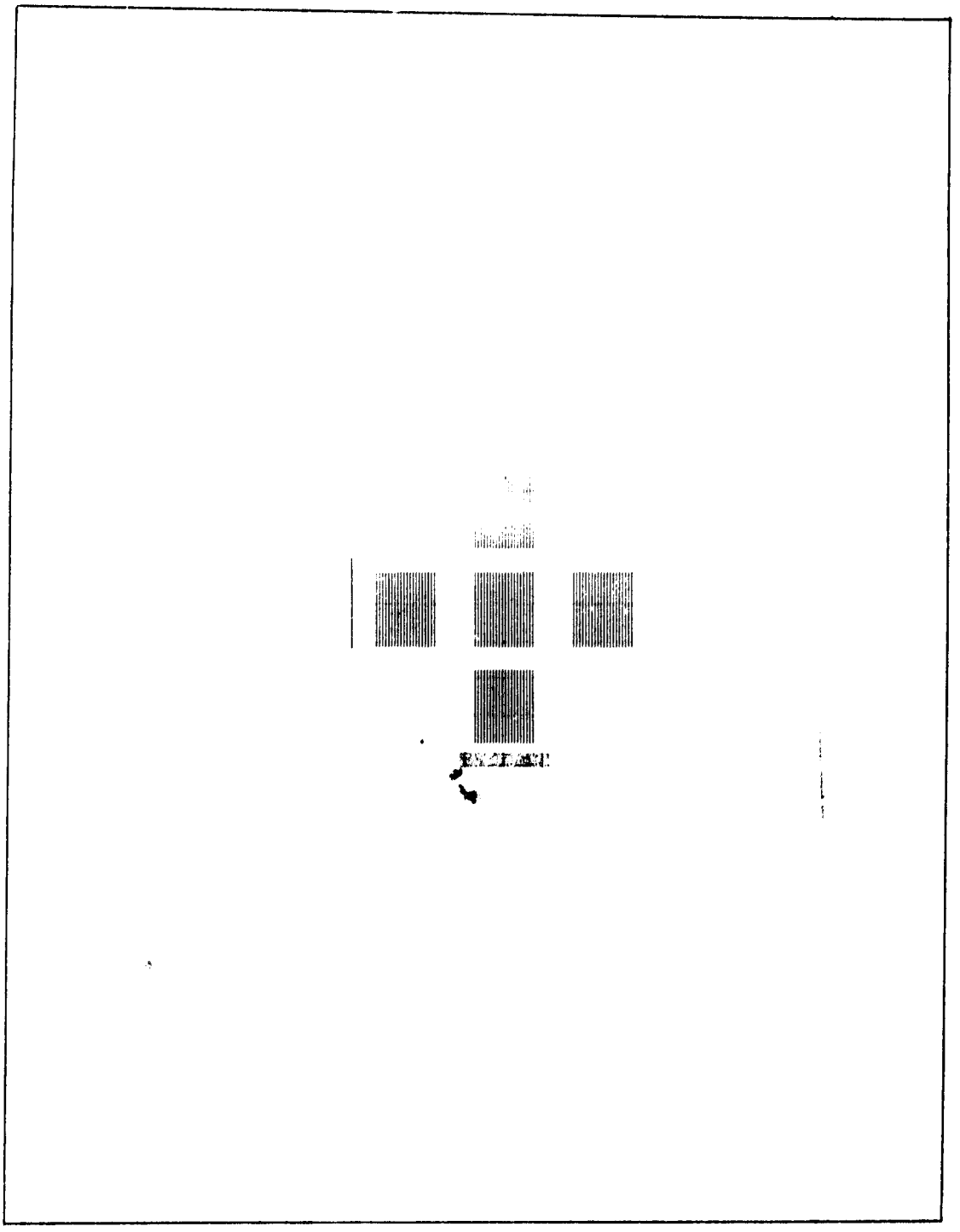


Figure 4-5. P+ mask with five identical cell patterns (actual size).

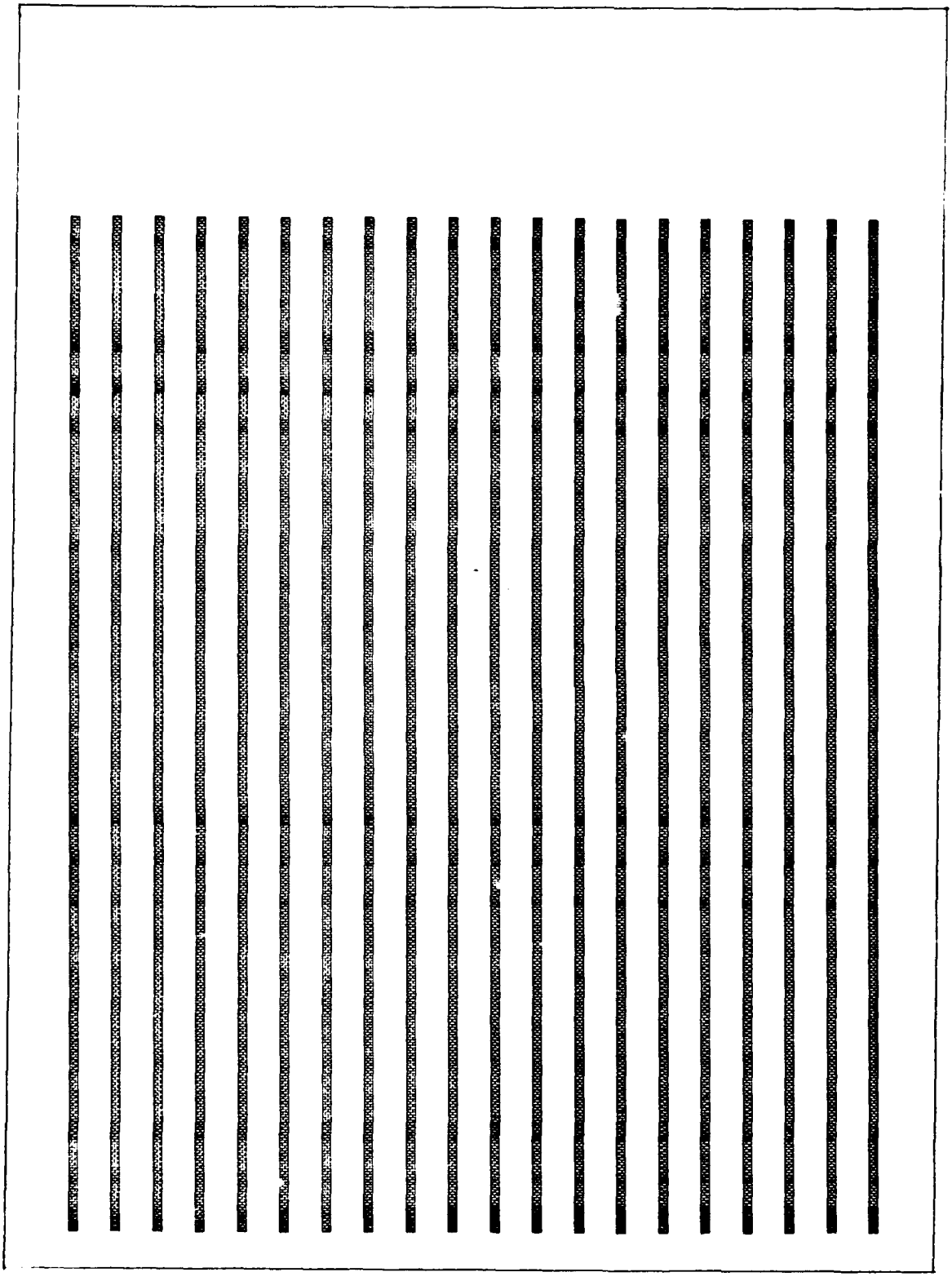


Figure 4-6. Enlarged p+ cell pattern (magnification 13.1x).

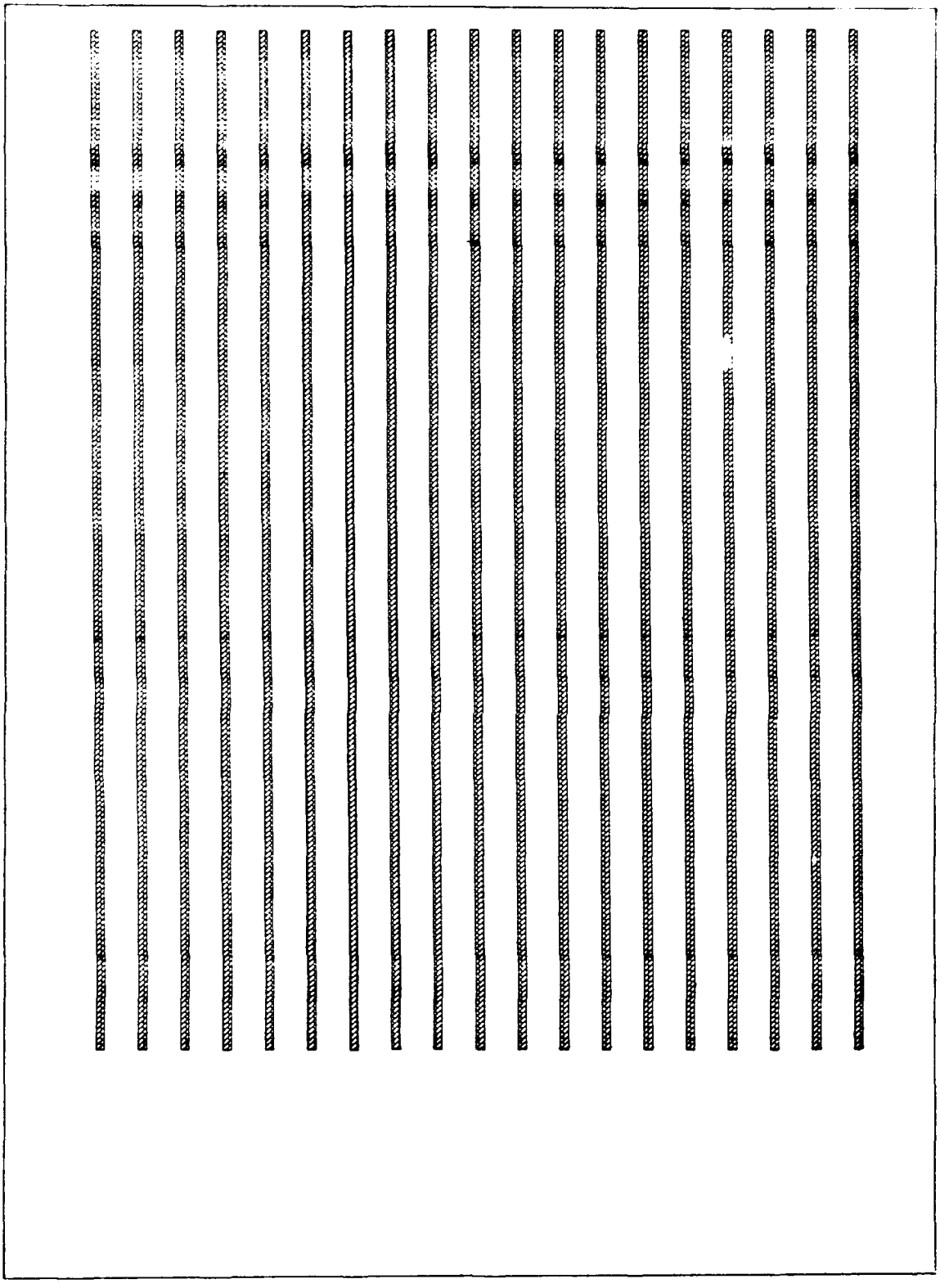


Figure 4-7. N+ pattern of one cell (magnification 13.1x).

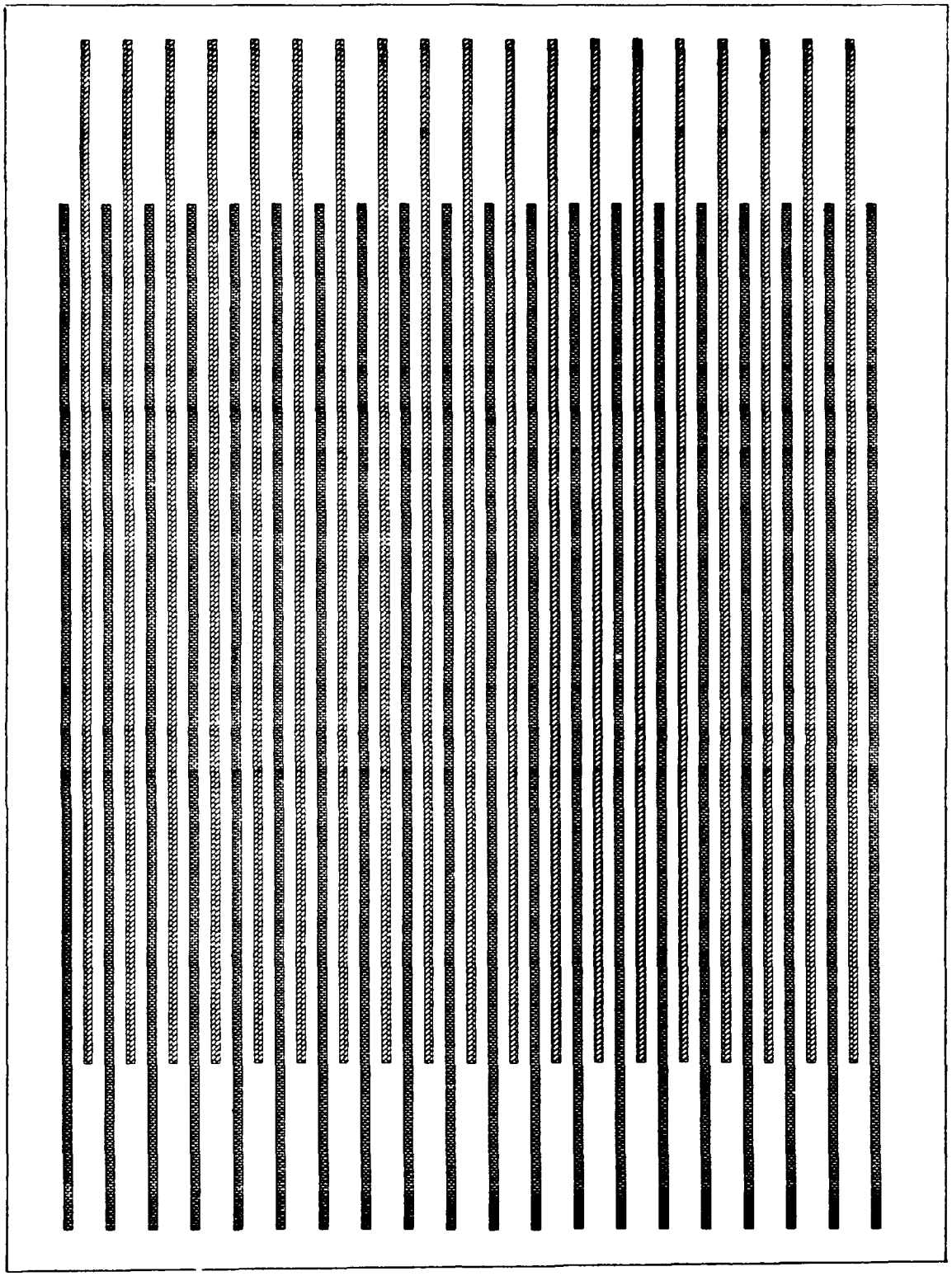


Figure 4-8. Alignment of n+ pattern with p+ pattern (magnification 13.1x).

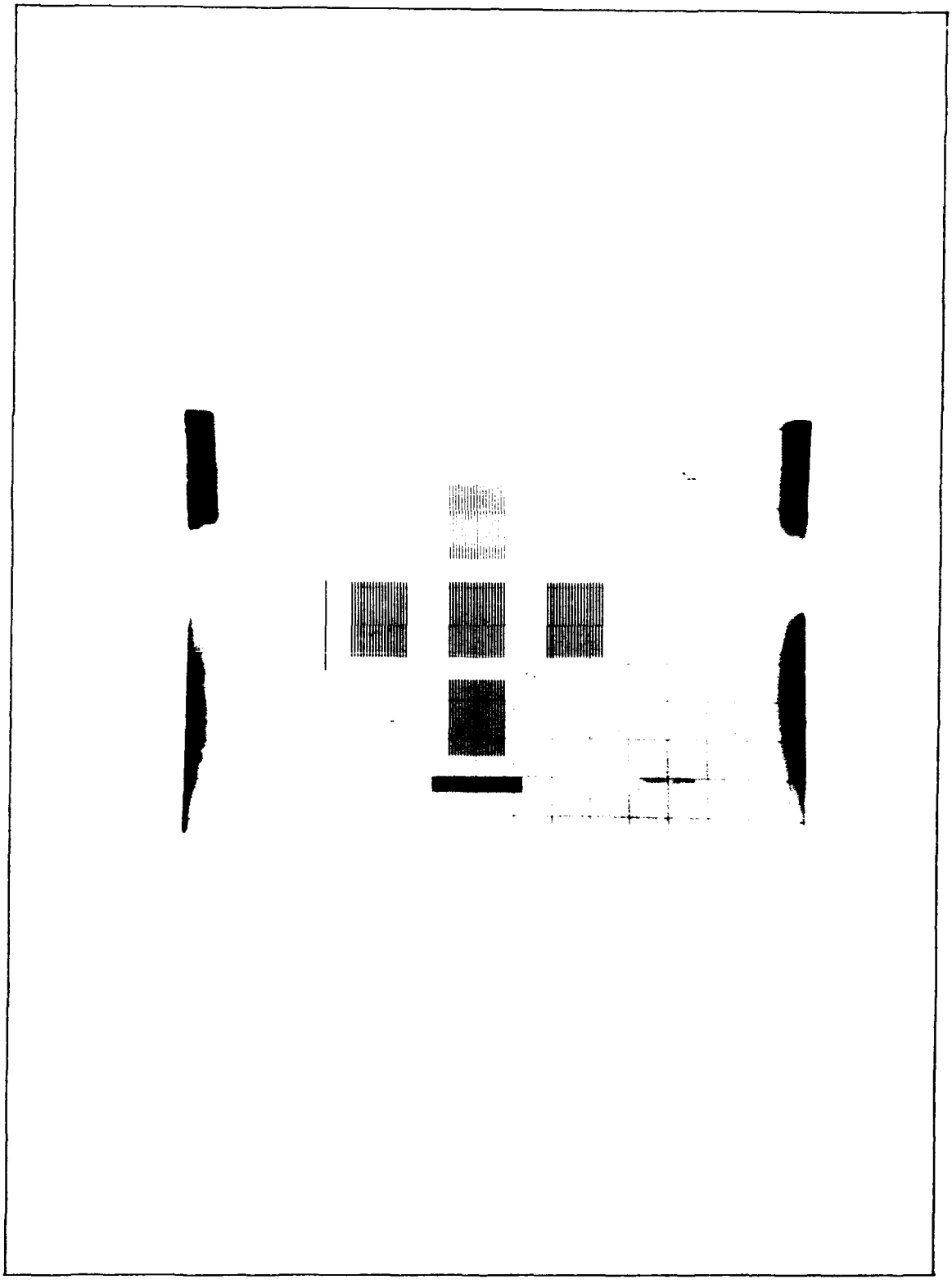


Figure 4-9. N+ mask with alignment marks (actual size).

Contact Mask. The contact mask was designed to ensure that the area contacted by metal on the cell's backside was the exact size of the groove pattern on the front. To compensate for misalignment errors, the contact lines (2 mils or 50.8 um, wide) where made 2 mils (50.8 um) smaller than the diffusion lines (4 mils or 101.6 um, wide). Figure 4-10 shows the contact pattern of one cell. Figure 4-11 shows how the contact pattern aligns with the n+ and p+ patterns. The contact mask, complete with alignment marks, is shown in Figure 4-12.

Metal Mask. The metal mask was made to connect all of the n+ diffusion lines at one end, and all of the p+ diffusion lines at the other. Large metal pads (50 mils by 400 mils) were placed at either end to connect the lines and provide a large area for probing during testing. The metal pattern for one cell is shown in Figure 4-13. Each line was made 6 mils (152.4 um) wide. This width provides low resistance, easy alignment, and covers the back of the cell suffiently to reflect most of the otherwise transmited light back into the cell. Figure 4-14 shows how the metal pattern aligns with the other patterns. The complete mask, including alignment marks, is shown in Figure 4-15.

All of the masks were designed to be used with a negative photoresist with the exception of the metal mask.

The metal mask used a positve photoresist since the chemicals used to remove negative photoresist attack aluminum.

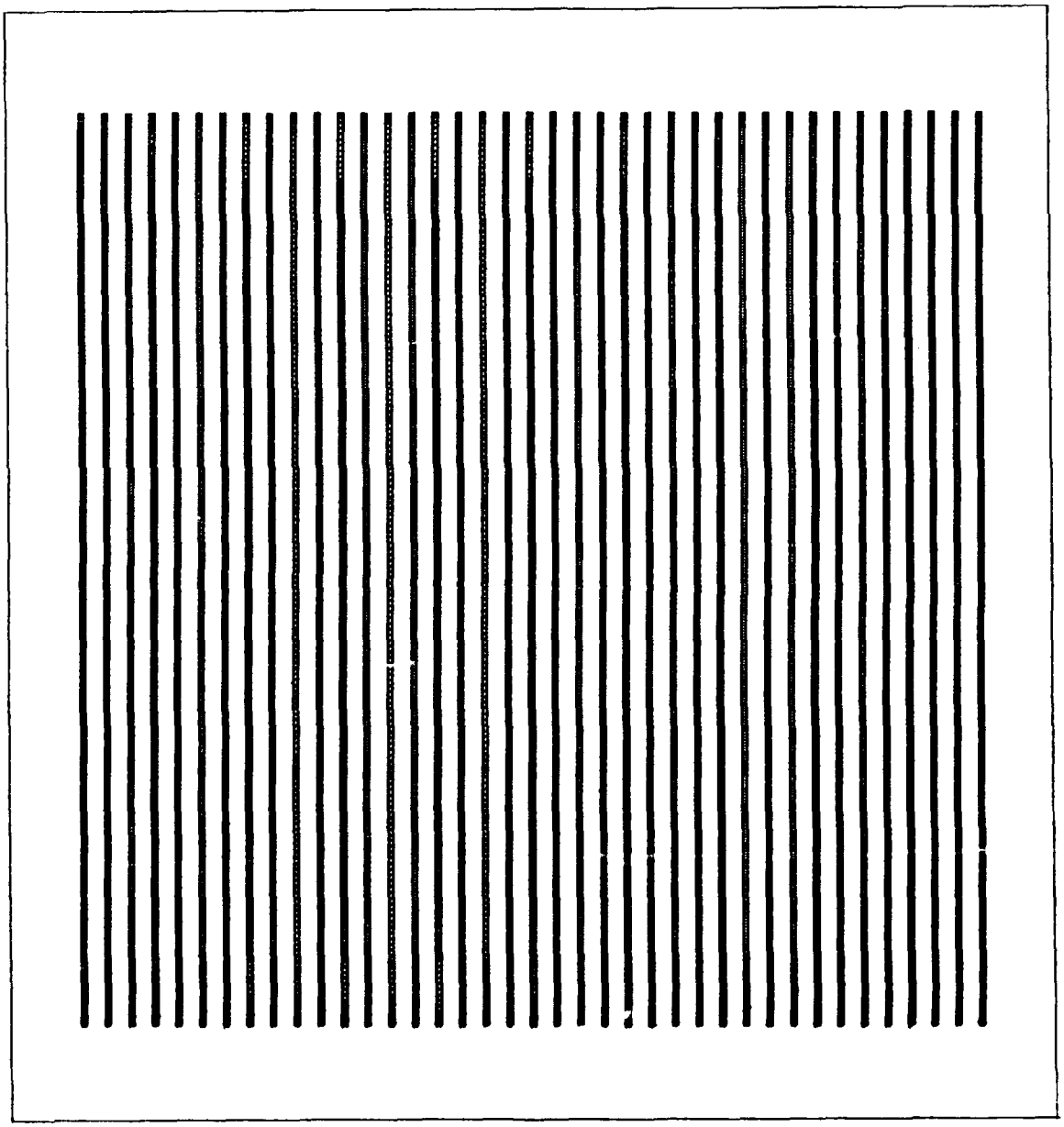


Figure 4-10. Contact pattern for one cell (magnification 13.1x).

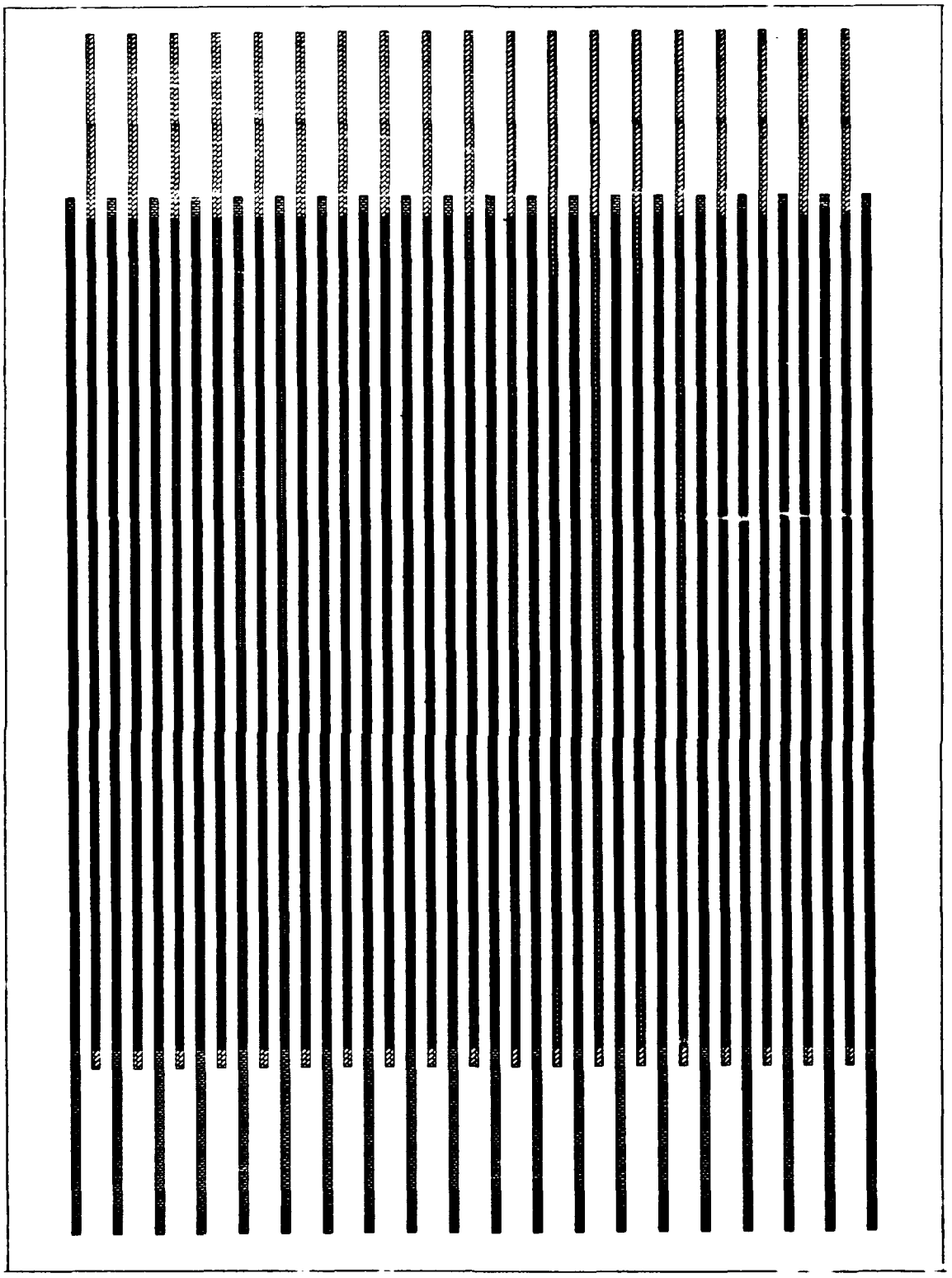


Figure 4-11. Alignment of contact pattern with the n+ and p+ patterns (magnification 13.1x).

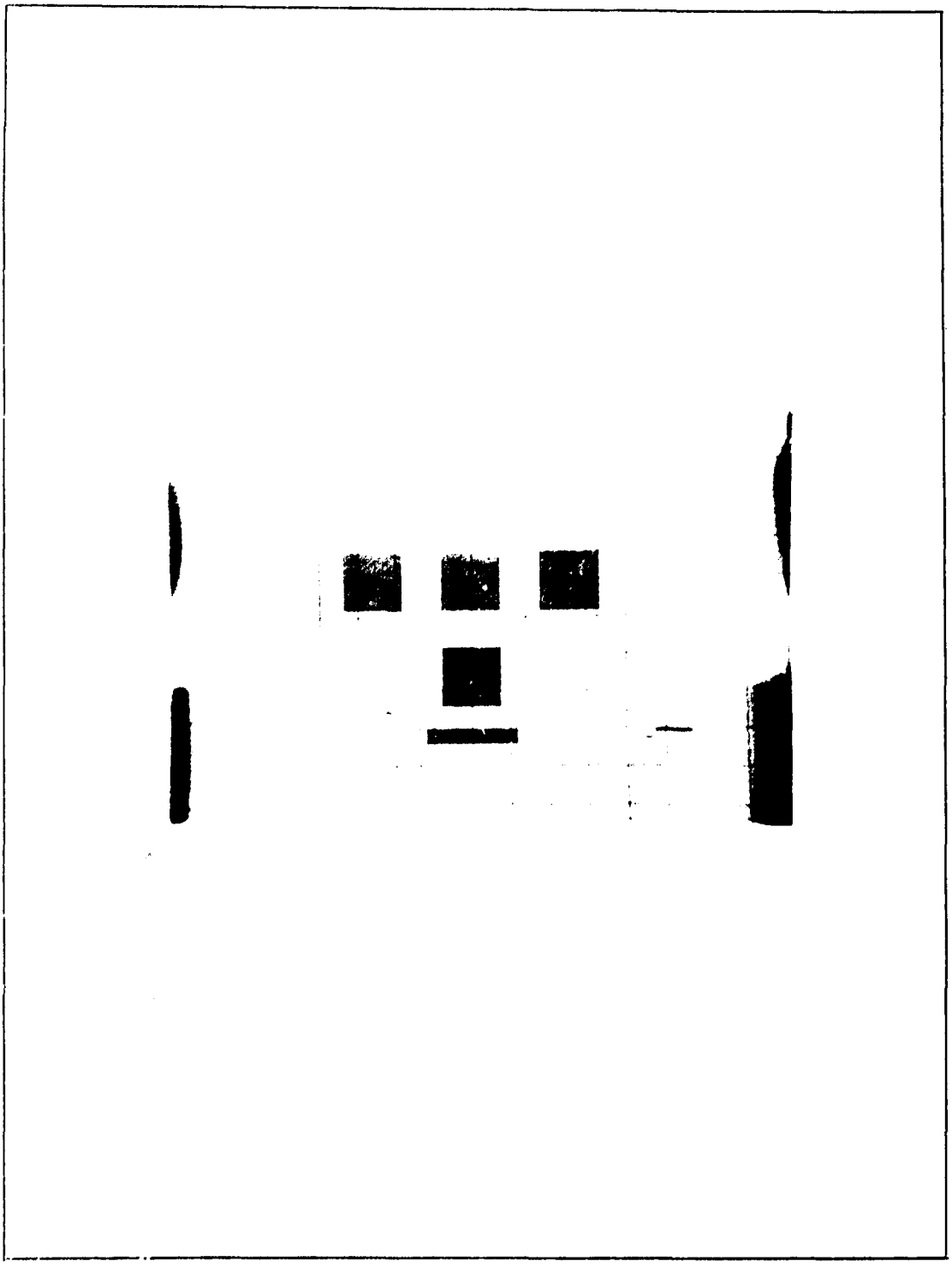


Figure 4-12. Contact mask complete with alignment marks (actual size).

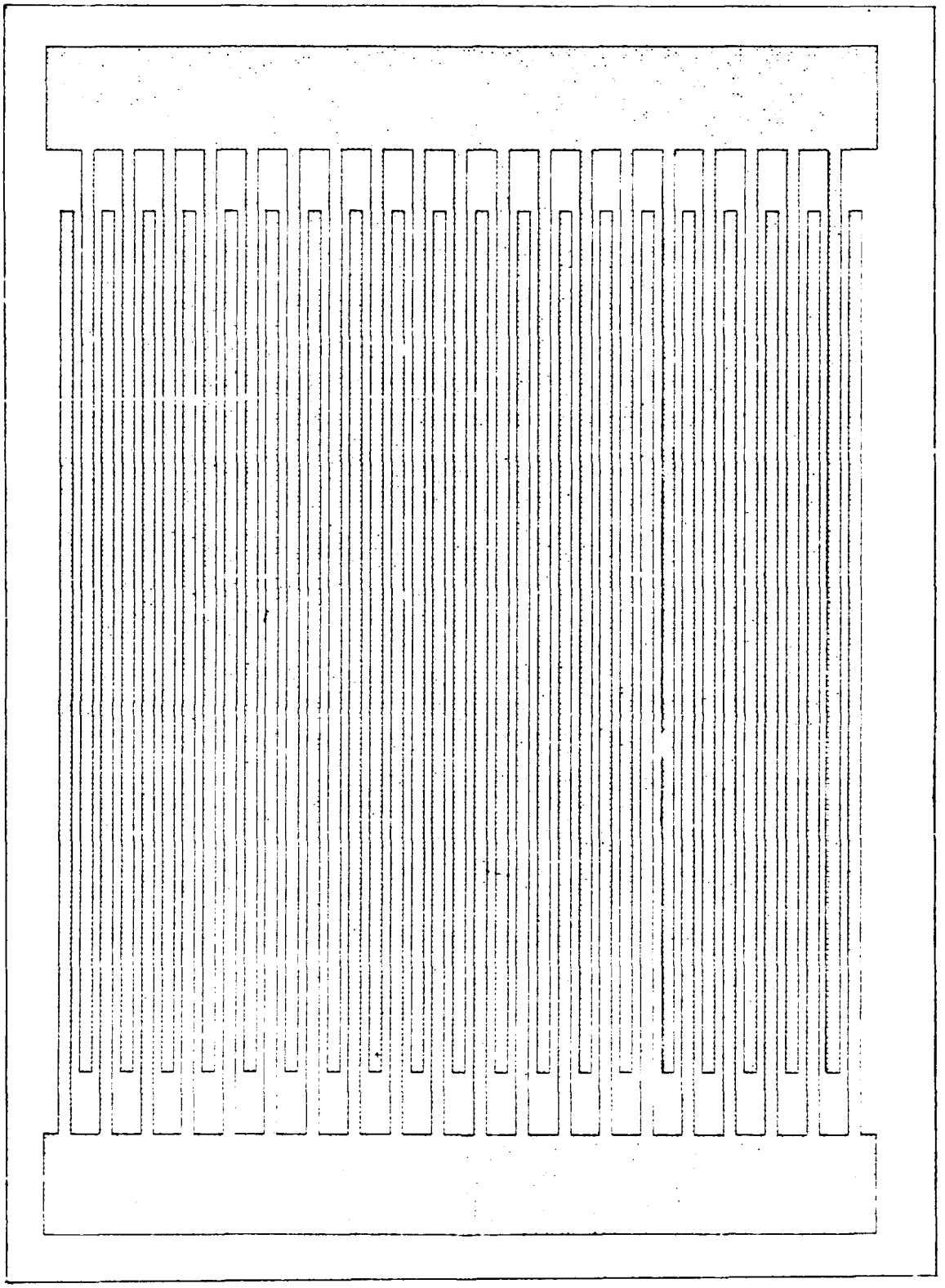


Figure 4-13. Metal pattern for one cell (magnification 13.1x).

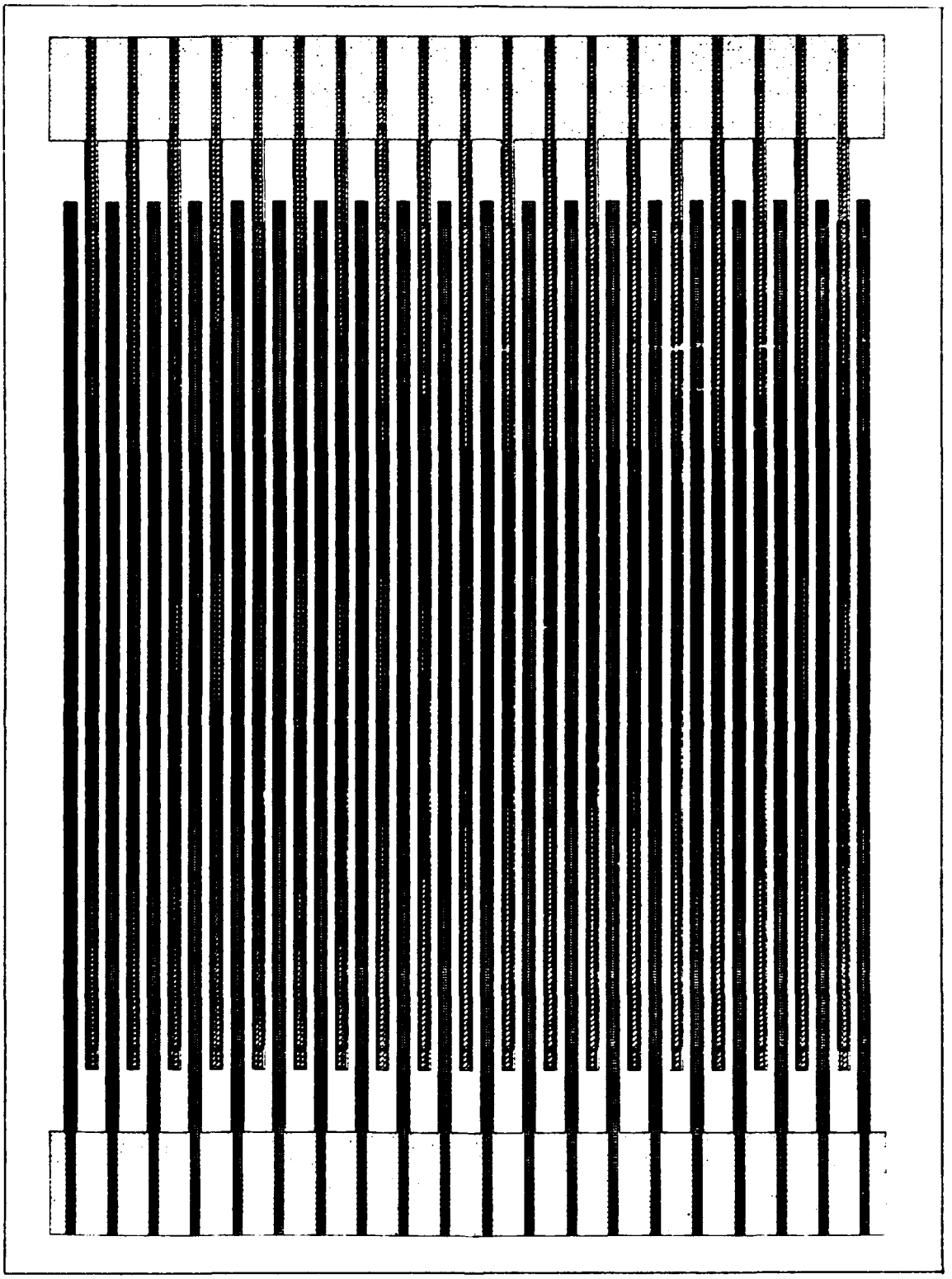


Figure 4-14. Alignment of the metal pattern with the contact, n+, and p+ patterns (magnification 13.1x).

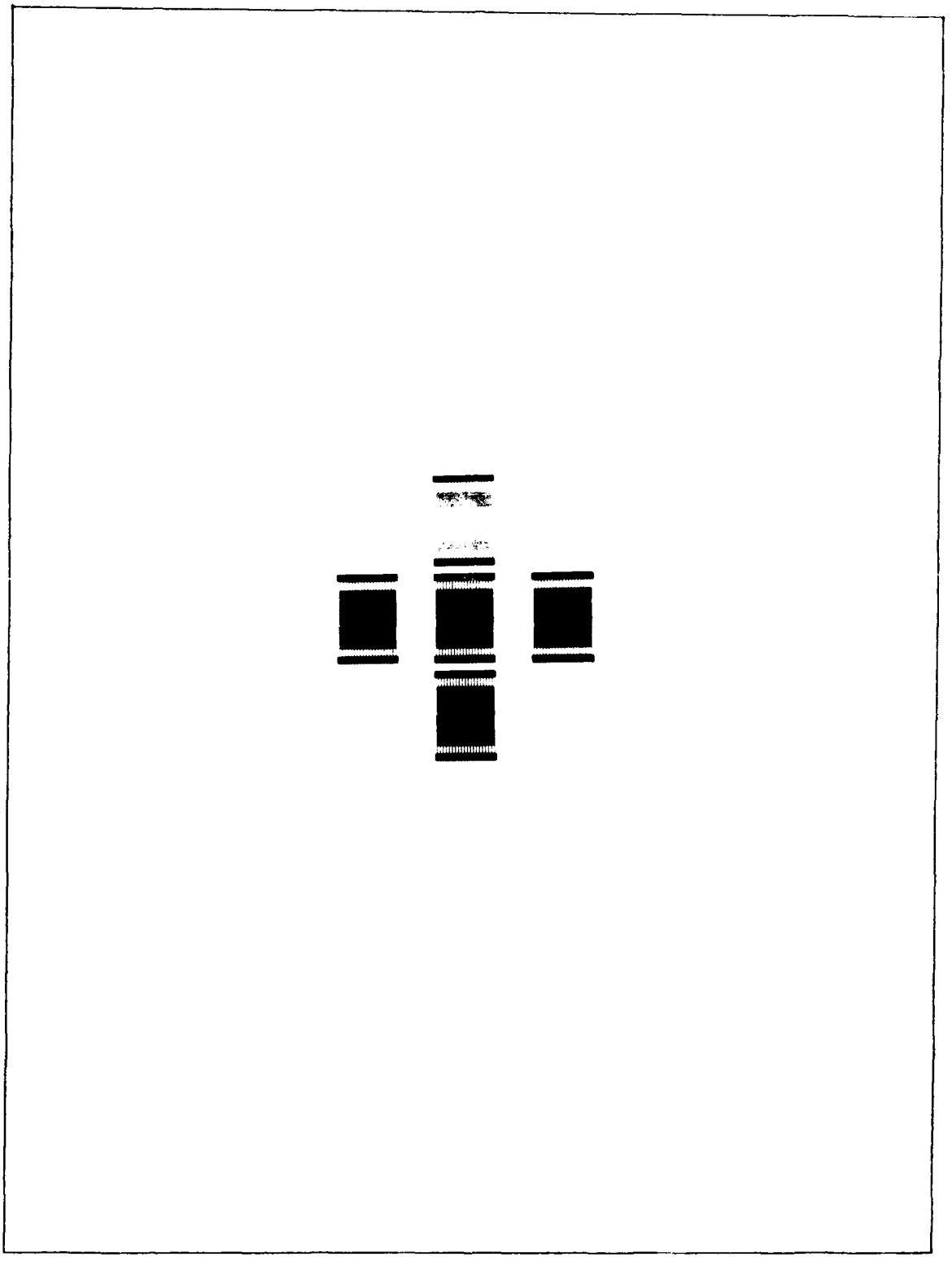


Figure 4-15. Metal mask complete with alignment marks (actual size).

Mask Set Fabrication

Each of the five mask levels was similarly fabricated. First, the Rubylith was cut and peeled. Next, the Rubylith image was photographed and reduced 40 times and printed on a 2-inch HRP plate. A copy was then made to reverse the image. The reversed copy was then used to make a reticle image for stepping-and-repeating. Finally, the image was stepped-and-repeated, and reduced another 10 times to realize a finished product. This process was required five times to realize the five levels discussed in the last section. Each of these steps will now be explained in detail.

Cutting the Rubylith. To provide good resolution and to minimize the cutting and peeling of Rubylith, the Rubylith image was made as large and as simple as possible. Since the first reduction camera has a 40-inch screen, the largest image was limited to 40 inches. The Rubylith image was 400 times the actual size.

The groove Rubylith image was cut at the Air Force Avionics Laboratory. The groove pattern shown in Figure 4-2 was layed out using CALMA (a computer aided design tool), and then transfered to a magnetic tape. The magnetic tape was used to drive the computer controlled coordinatograph plotter table (resolution of plotter is 10 mils or 254 um). A knife blade was inserted in place of the ink pen to cut

the Rubylith. The vertical and horizontal lines had to be layed out as different layers so they could be cut separately. Fiducial marks were placed on the image to facilitate alignment requirements.

The patterns for the contact mask, the p+ and n+ masks, and part of the metal mask were cut from the same sheet of Rubylith. Figure 4-16 shows how the patterns for each of these masks were cut. The three rectangles were cut and then peeled from the smallest to the largest to yield three different sized rectangles. Each rectangle was photographed before the next was peeled. The smallest rectangle was used for the contact mask; the middle sized rectangle was used for the diffusion masks; and the large rectangle was used for the metal mask. This process also insured that the fiducial marks were in the same location for each pattern.

The metal mask required an additional Rubylith image for the pads. This required a 50 by 50 mil (1,270 um) square image. Enlarged 400 times, this pattern would be 20 by 20 inches (50.8 cm). Figure 4-17 shows the square pattern used to form the metal pads.

Except for the groove pattern, all Rubylith was cut in the AFIT Cooperative Electronic Materials and Processes Laboratory in Building 125. The coordinatograph table was used to cut the Rubylith. The resolution of this system is 10 mils (254 um).

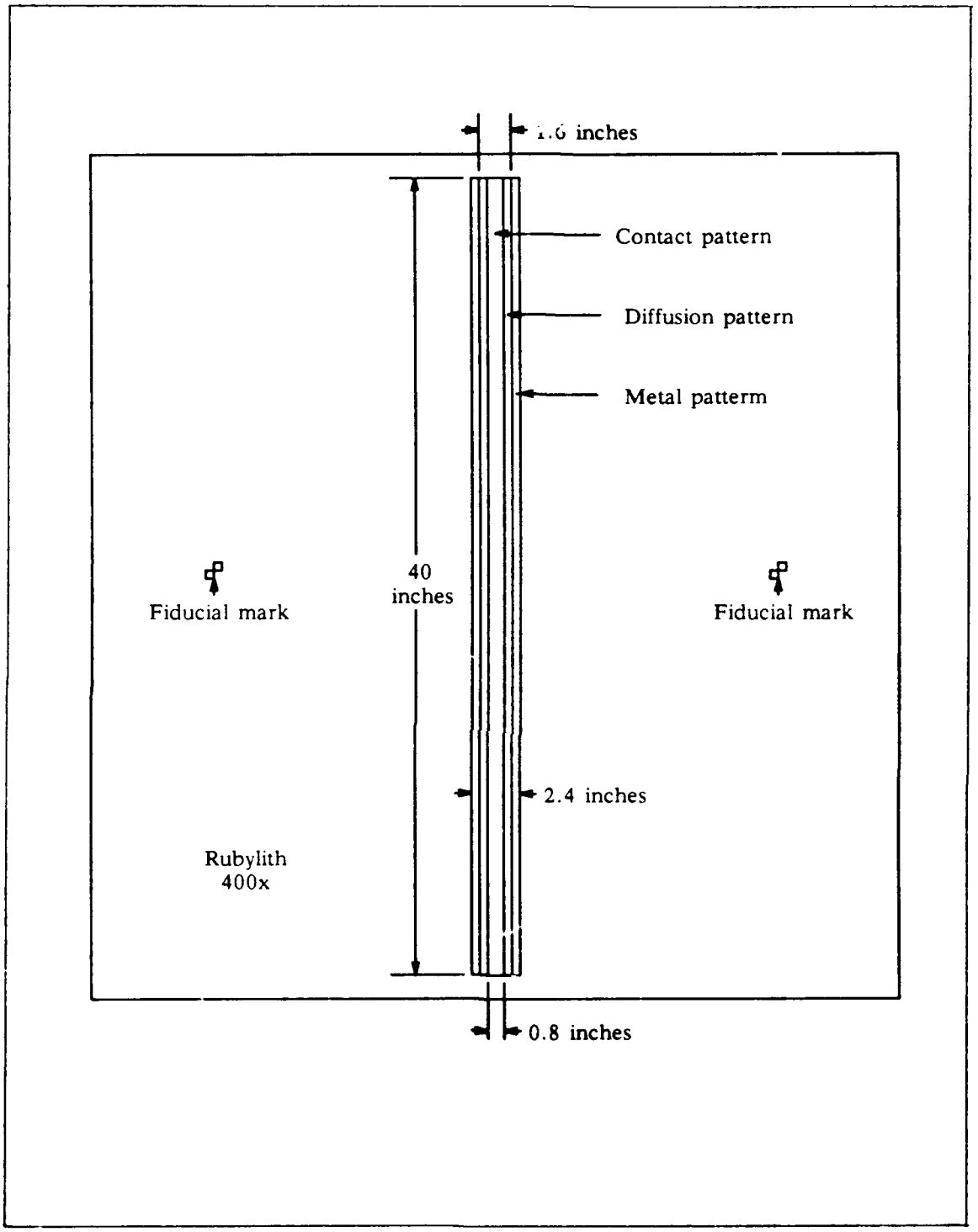


Figure 4-16. Diagram showing how the patterns used to produce the contact reticle, the p+ and n+ reticle, and one of the metal reticles could all be cut from the same sheet of Rubylith.

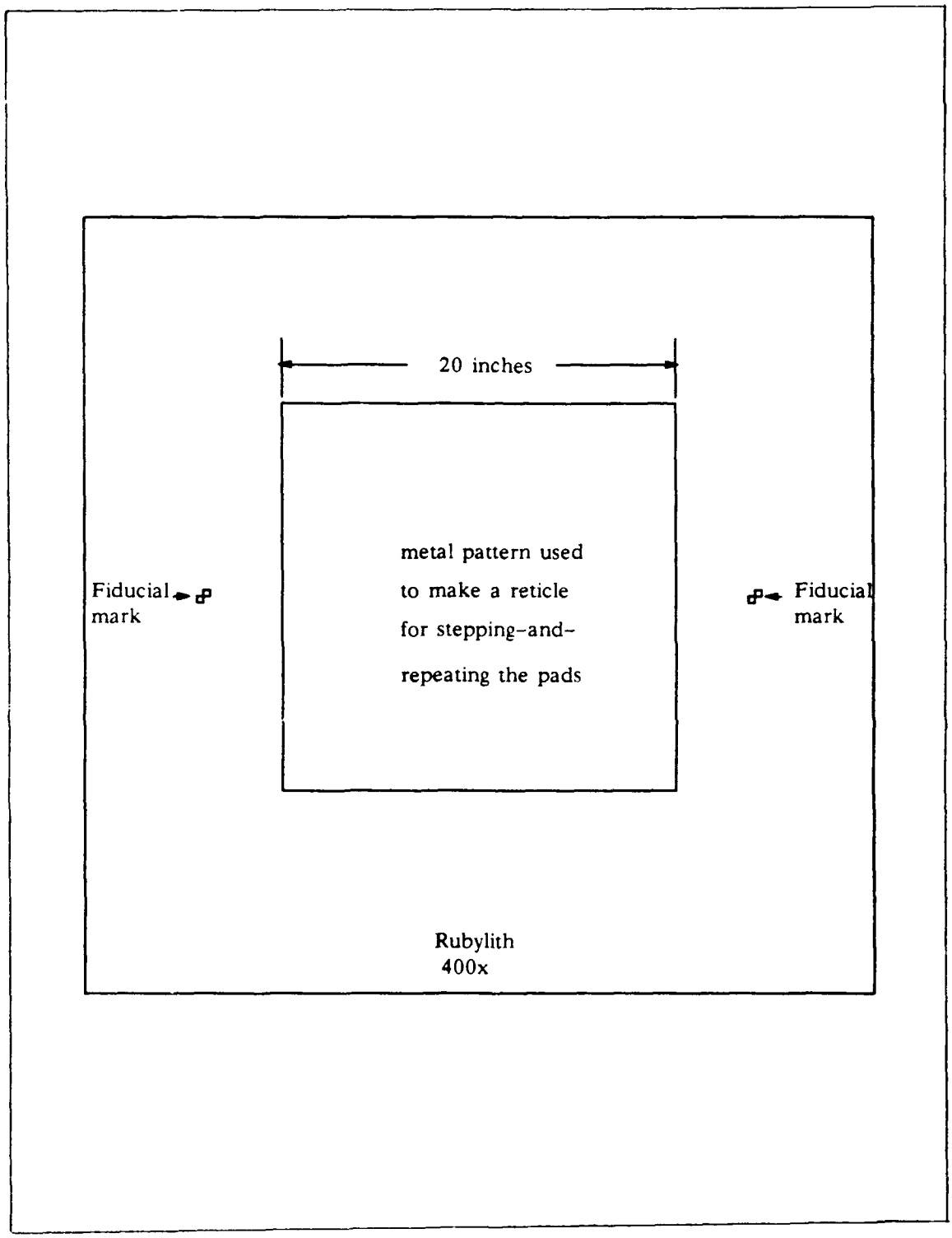


Figure 4-17. Rubylith pattern used to produce a reticle for stepping-and-repeating the metal pads onto the metal mask.

First Reduction. Each of the Rubylith patterns was reduced 40 times using the first reduction camera. The Rubylith was cut from sheets large enough to overlap the vacuum holes on the edges of the reduction screen. The Rubylith was taped securely to the screen and the vacuum system turned on. Care was taken to insure that the Rubylith was flat against the screen. The optimum settings for best resolution, focus, field of view, depth of field, and density were experimentally determined:

Component	Parameter
Lens	3-inch wray
Front box setting	68.1825
Rear box setting	88.2500
F-stop	full open
Exposure time	20 seconds
Plate size	2 inch (Kodak HRP)

The plates were developed using the standard developing process (discussed later). They were then inspected under the optical microscope using backlighting to check for proper focus and development. Next, the plate image was reversed by making a contact copy using the laboratory mask duplicator. This made the outside regions black so that tape could be placed on the plate where stray light might create an unwanted image on the mask. This plate was used to make the reticle.

Making the Reticle. The plate was aligned using the reticle alignment microscope. Alignment was accomplished by focusing on the fiducial marks and aligning the pattern so that it was centered, and the sides of the pattern were parallel to the sides of the holder. The plate was then glued to the holder to form a reticle to be used in the step-and-repeat process. Tape was placed over the fudicial marks and outside regions to insure no stray light from the sides was passed. Each of the reticles is shown in Figure 4-18 through 4-21. The next step was to step-and-repeat the pattern.

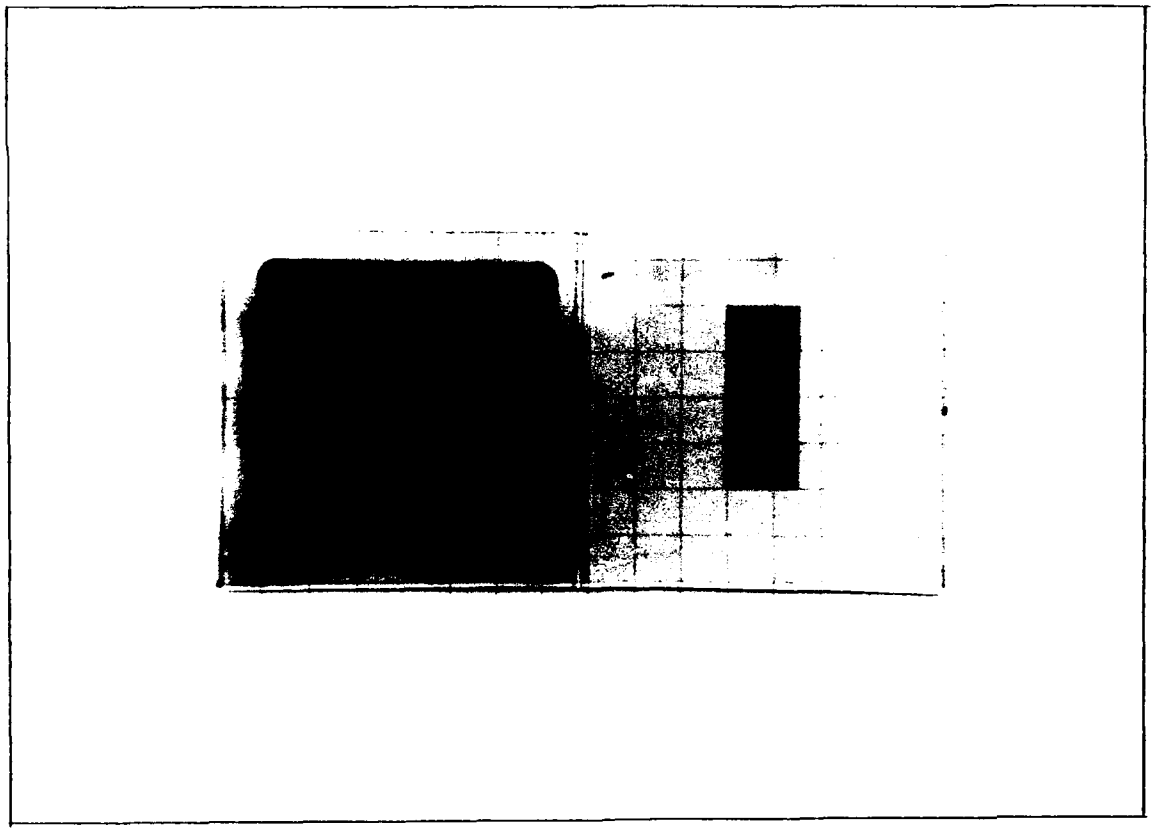


Figure 4-18. Groove reticle (actual size).

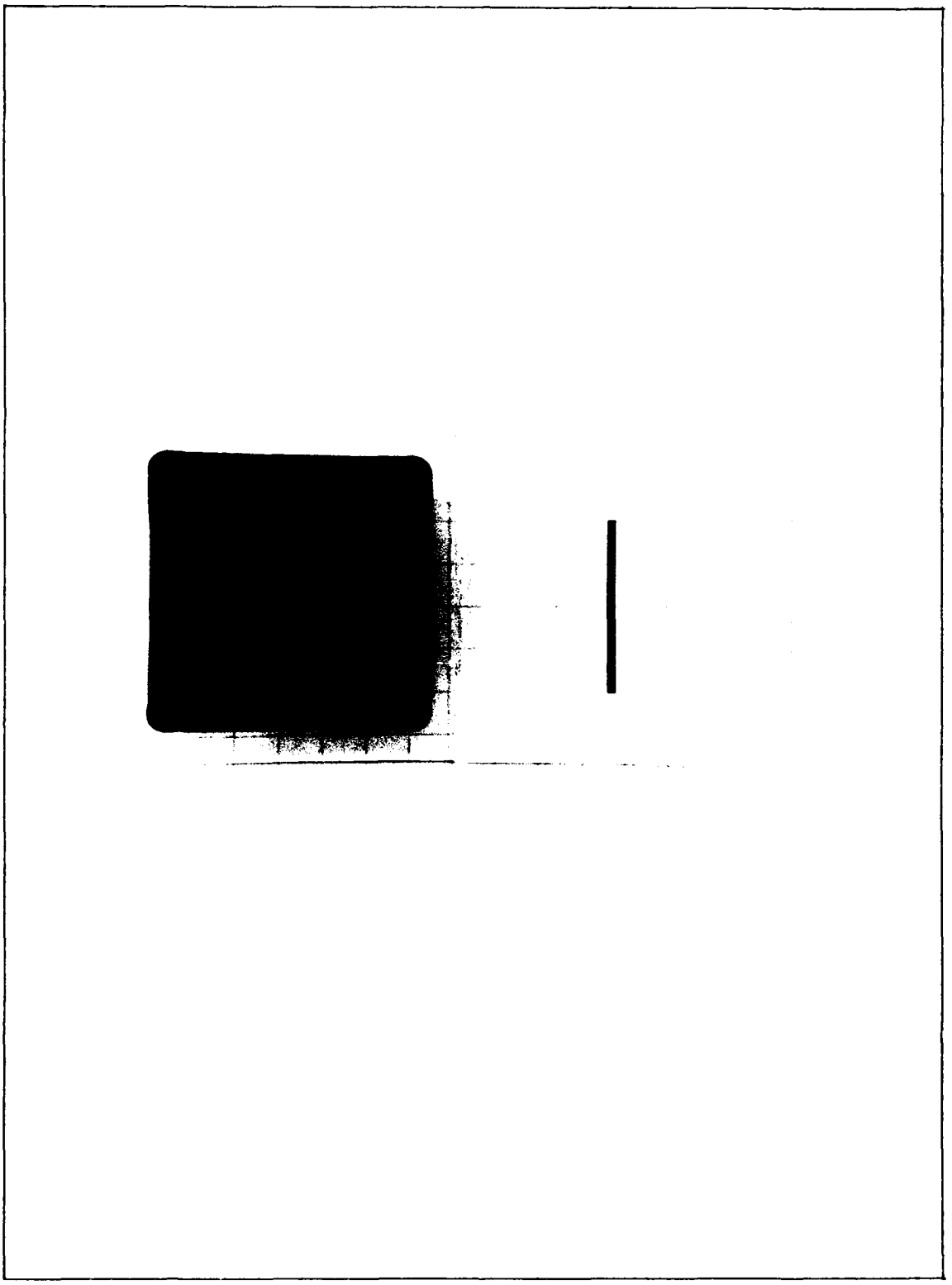


Figure 4-19. N+ and p+ reticle (actual size).

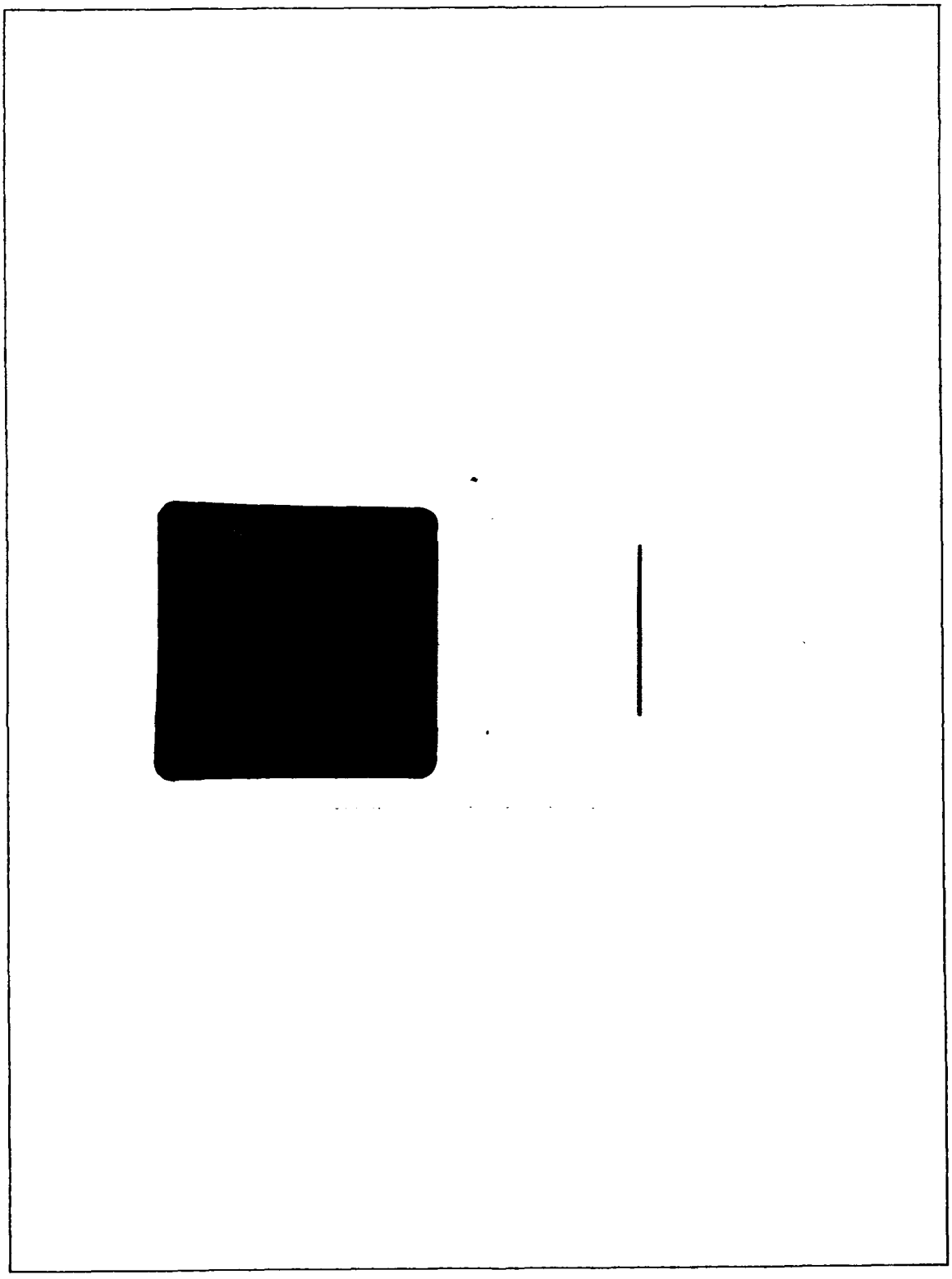


Figure 4-20. Contact reticle (actual size).

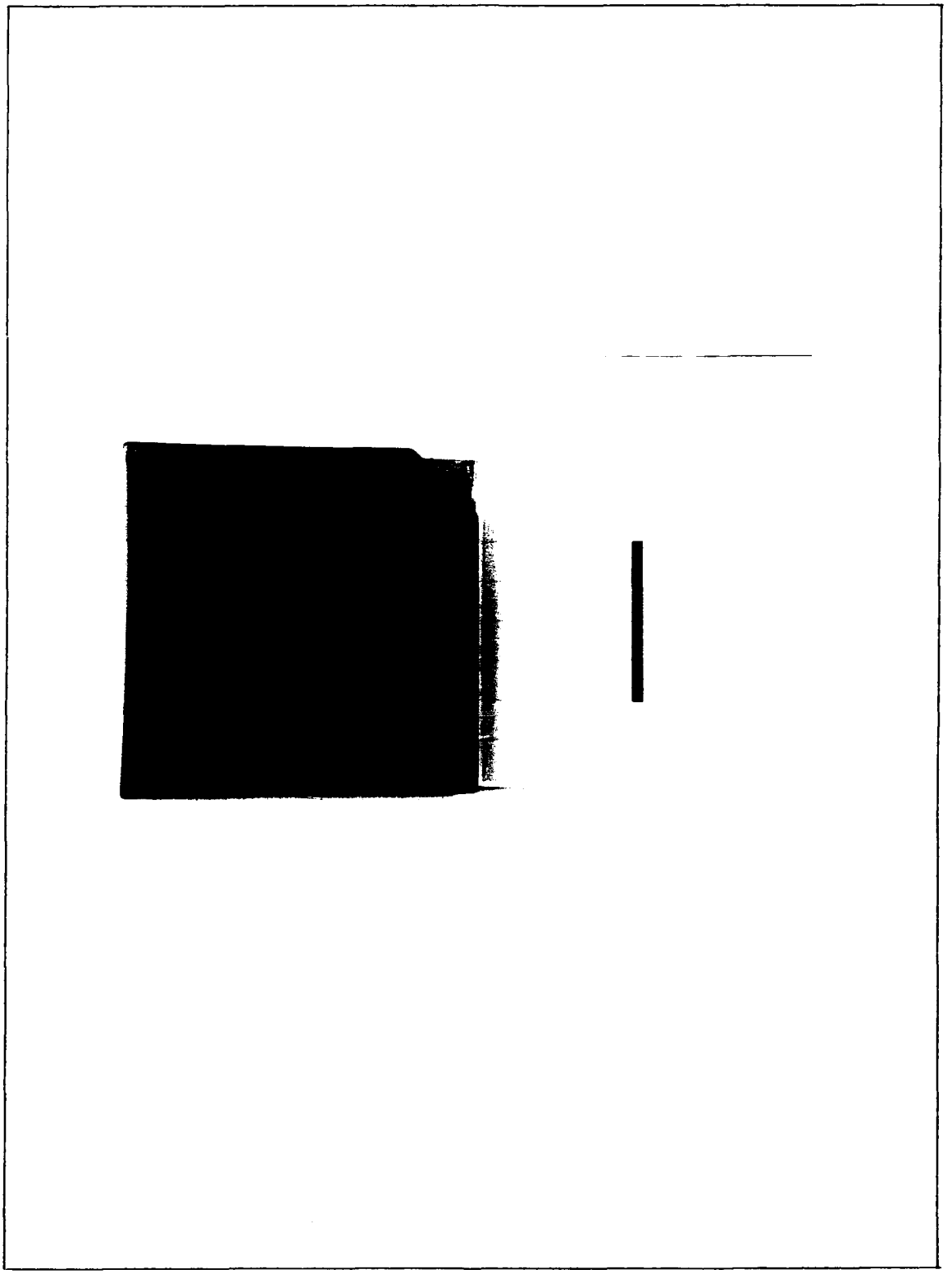


Figure 4-21. Metal reticle (actual size).

Step-and-Repeat Process. The final mask set was made on 4-inch HRP plates. In order to use the laboratory's 4-inch plate holder, three plates had to be placed behind the plate being exposed, otherwise it would slide around in the holder. Changing the plate holder required refocusing the camera, since the camera was focused for the 2-inch plates. The focus was determined experimentally by varying the focus between flashes and then checking under the microscope to detrmine which flash had the best focus. The following settings, common to all five mask levels, were determined to give the best focus, resolution, and density:

Component	Parameter
Flash intensity	medium, 6
Lamp triggers	all on
Auto/manual switch	auto
Inhibit/run switch	run
Power switch	on
F stop	1.8
Focus setting	when turning from low to high, stop at 0.15635

Tables 4-1 through 4-5 summarize the details of how each mask was made. The given x- and y-coordinates are the starting points for each set of exposures. The x-coordinate corresponds to the large 50 mil wheel. The y-coordinate corresponds to the small 25 mil wheel. The reticle, the

exposure spacing, and the exposures per row are given prior to the coordinates and are restated only when they change.

Table 4-1. Groove mask step-and-repeat sequence.

Reticle - groove

Exposure spacing - 40 mils Exposures per row - 10

	x	y		x	y
1.	1.030	0.450	11.	0.380	1.300
2.	"	0.550	12.	1.030	"
3.	"	0.650	13.	1.680	"
4.	"	0.750	14.	0.380	1.400
5.	0.380	1.100	15.	1.030	"
6.	1.030	"	16.	1.680	"
7.	1.680	"	17.	1.030	1.750
8.	0.380	1.200	18.	"	1.850
9.	1.030	"	19.	"	1.950
10.	1.680	"	20.	"	2.050

Alignment marks

Exposure spacing - 40 mils Exposures per row - 15

	x	y
21.	0.930	2.300

Recticle - contact

Exposure spacing - 0 mils Exposures per row - 1

	x	y		x	y
22.	2.251	1.000	25.	2.251	1.300
23.	"	1.100	26.	"	1.400
24.	"	1.200	27.	"	1.500

Table 4-2. P+ mask step-and-repeat sequence.

Exposure spacing - 20 mils Exposures per row - 20

Reticle - diffusion

	x	y		x	y
1.	1.040	0.440	14.	1.690	1.290
2.	"	0.540	15.	0.390	1.390
3.	"	0.640	16.	1.040	"
4.	"	0.740	17.	1.690	"
5.	"	0.840	18.	0.390	1.490
6.	0.390	1.090	19.	1.040	"
7.	1.040	"	20.	1.690	"
8.	1.690	"	21.	1.040	1.740
9.	0.390	1.190	22.	"	1.840
10.	1.040	"	23.	"	1.940
11.	1.690	"	24.	"	2.040
12.	0.390	1.290	25.	"	2.140
13.	1.040	"			

Alignment marks

Exposure spacing - 0 mils Exposures per row - 1

	x	y		x	y
26.	2.252	1.000	29.	2.252	1.300
27.	"	1.100	30.	"	1.400
28.	"	1.200	31.	"	1.500

Recticle - groove

Exposure spacing - 40 mils Exposures per row - 15

	x	y
32.	0.930	2.300

Table 4-3. N+ mask step-and-repeat sequence.

Exposure spacing - 20 mils Exposures per row - 19

Reticle - diffusion

	x	y		x	y
1.	1.050	0.360	14.	1.700	1.210
2.	"	0.460	15.	0.400	1.310
3.	"	0.560	16.	1.050	"
4.	"	0.660	17.	1.700	"
5.	"	0.760	18.	0.400	1.410
6.	0.400	1.010	19.	1.050	"
7.	1.050	"	20.	1.700	"
8.	1.700	"	21.	1.050	1.660
9.	0.400	1.110	22.	"	1.760
10.	1.050	"	23.	"	1.860
11.	1.700	"	24.	"	1.960
12.	0.400	1.210	25.	"	2.060
13.	1.050	"			

Alignment marks

Exposure spacing - 0 mils Exposures per row - 1

	x	y		x	y
26.	2.252	1.000	29.	2.252	1.300
27.	"	1.100	30.	"	1.400
28.	"	1.200	31.	"	1.500

Recticle - groove

Exposure spacing - 40 mils Exposures per row - 15

	x	y
32.	0.930	2.300

Table 4-4. Contact mask step-and-repeat sequence.

Exposure spacing - 10 mils Exposures per row - 39

Reticle - contact

	x	y		x	y
1.	1.050	0.450	11.	0.400	1.300
2.	"	0.550	12.	1.050	"
3.	"	0.650	13.	1.700	"
4.	"	0.750	14.	0.400	1.400
5.	0.400	1.100	15.	1.050	"
6.	1.050	"	16.	1.700	"
7.	1.700	"	17.	1.050	1.750
8.	0.400	1.200	18.	"	1.850
9.	1.050	"	19.	"	1.950
10.	1.700	"	20.	"	2.050

Alignment marks

Exposure spacing - 0 mils Exposures per row - 1

	x	y		x	y
21.	2.251	1.000	24.	2.251	1.300
22.	"	1.100	25.	"	1.400
23.	"	1.200	26.	"	1.500

Reticle - groove

Exposure spacing - 40 mils Exposures per row - 15

	x	y
27.	0.930	2.300

Table 4-5. Metal mask step-and-repeat sequence.

Reticle - metal

Exposure spacing - 20 mils Exposures per row - 19

1. x = 1.050 y = 0.350

Exposure spacing - 10 mils Exposures per row - 39

	x	y		x	y
2.	1.050	0.450	4.	1.050	0.650
3.	"	0.550	5.	"	0.750

Exposure spacing - 20 mils Exposures per row - 20

6. x = 1.040 y = 0.850

Exposure spacing - 20 mils Exposures per row - 19

	x	y		x	y
7.	0.400	1.000	9.	1.700	1.000
8.	1.050	"			

Exposure spacing - 10 mils Exposures per row - 39

	x	y		x	y
10.	0.400	1.100	16.	0.400	1.300
11.	1.050	"	17.	1.050	"
12.	1.700	"	18.	1.700	"
13.	0.400	1.200	19.	0.400	1.400
14.	1.050	"	20.	1.050	"
15.	1.700	"	21.	1.700	"

Exposure spacing - 20 mils Exposures per row - 20

	x	y		x	y
22.	0.390	1.500	24.	1.690	1.500
23.	1.040	"			

Exposure spacing - 20 mils Exposures per row - 19

Table 4-5 continued.

25. x = 1.050 y = 1.650

Exposure spacing - 10 mils Exposures per row - 39

	x	y		x	y
26.	1.050	1.750	28.	1.050	1.950
27.	"	1.850	29.	"	2.050

Exposure spacing - 20 mils Exposures per row - 20

30. x = 1.040 y = 2.150

Reticle - metal square

Exposure spacing - 40 mils Exposures per row - 10

	x	y		x	y
31.	1.035	0.325	36.	0.385	1.525
32.	"	0.875	37.	1.035	"
33.	0.385	0.975	38.	1.685	"
34.	1.035	"	39.	1.035	1.625
35.	1.685	"	40.	"	2.175

Alignment marks

Exposure spacing - 0 mils Exposures per row - 1

	x	y		x	y
21.	2.252	1.000	24.	2.252	1.300
22.	"	1.100	25.	"	1.400
23.	"	1.200	26.	"	1.500

Recticle - groove

Exposure spacing - 40 mils Exposures per row - 15

	x	y
27.	0.930	2.300

Each of the masks had to be stepped-and-repeated in the dark (red light only). Following the step-and-repeat process, the plates were developed. The plate developing process is dicussed next.

Plate Development Process. Kodak HRP plates were used in all phases of the mask making process. The developing process should be done in controlled temperature range of 68-70°F. This process must be accomplished in a dark room with only a low-level of red lighting. The following procedures were implemented:

1. Plate(s) were put in plastic holder
2. 5 minute develop in HRP developer (1:4, developer:deionized water), continuous agitation
3. 30 seconds in stop bath
4. 1 minute fix, some agitation
5. 5 minute wash in DIW
6. Blown dry with N_2.

This completes the mask fabrication process. The back-contact vertical-junction (BCVJ) solar cell fabrication process is discussed next.

BCVJ Solar Cell Fabrication

In the last section, the procedures for generating the mask set were discussed. Next, the details of how this mask set was used along with the processing procedures are discussed. The procedures used for processing the BCVJ solar cell are given in the same sequence they were accomplished. Many of the procedures implemented evolved from various sources, but may have changed slightly due to variations allowed in processing. Others were determined experimentally. Processing steps, not considered common knowledge, will be referenced. During this discussion, one should refer to the Appendix for a step-by-step illustration of the fabrication process. The following processing steps will be discussed in detail:

1. Wafer preparation
2. Oxidation
3. Groove photolithography
4. Orientation dependent etching
5. Pointing the groove walls
6. P+ photolithography and diffusion
7. N+ photolithography and diffusion
8. Contact photolithography
9. Metallization and patterning.

Wafer Preparation. The wafers used in the fabricaion of the BCVJ solar cell were obtained from two different

sources. Twenty-five wafers were initially obtained from AFWAL/POOC. The manufacturer of these wafers was Ametek. An additional 35 wafers were ordered from Virginia Semiconductor (VS). The main differences between the two lots were the orientation of the flat and the initial thickness. The Ametek wafers varied in thickness from 312 to 350 um. The VS wafers were predominantly 290 um thick, but some were as thick as 295 um. The flat on the Ametek wafers was cut perpendicular to the (1$\underline{1}$1) plane while the flat on the VS wafers was cut parallel to the (11^{1}) plane. The Ametek wafers also had a secondary flat parallel to the (1$\underline{1}$1) plane. All the silicon wafers were (110) orientated, Czochralski grown, boron doped, a resistivity of 2-3 ohm-cm, single crystal, and polished on both sides.

Wafer Identification. Before processing any of the wafers, each wafer was identified by scribing a letter and a number on the front side of the wafer just above the primary flat. The letter identified the manufacturer (A for Ametek and V for Virginia Semicondutor). The numbers ranged from 1-25 for both A- and V-wafers. This identificaton procedure was necessary to keep accurate records on the history of each wafer.

To scribe the wafers, each wafer was placed on a hard flat surface. The wafer was scribed using a diamond stylus.

When not being processed, the wafers were stored in a covered wafer holder.

Adjusting Wafer Thickness. Since certain wafers were thicker than the chosen groove depth (d) of 290 um, a method of thinning the wafers was required. A planar chemical etchant composed of $HF:HNO_3:CH_3COOH$ (2:15:5) was used [31:522]. The etchant was mixed in a teflon beaker and allowed to equilibrate for two hours before use. The expected etch rate (one side) was 5 um/min, but was found to decrease as the etchant was used. The method of using this ethant to produce the smoothest polished surface was to place the wafer in a plastic holder, submerge it horizontally, and manually swirl the wafer in a circular motion at about 60 RPM.

The initial thickness (t_i) of a wafer was determined by measuring it with a micrometer. The etch rate determined from the last wafer etched was used to determine the length of time necessary to thin the wafer to 290 um. After the etching procedure was accomplished, the wafer was rinsed in deionized (DI) water. The wafer thickness was re-measured and the process repeated until the desired thickness was achieved.

Wafer Cleaning. Immediately prior to the oxidation and diffusion steps, the wafers were thoroughly cleaned using an immersion process described in Elliott

[26:51]. This cleaning process is described below in Table 4-6.

Table 4-6. Cleaning procedure using immersion.

Step	Procedure
1.	10-20 min in $H_2SO_4:H_2O_2$ (3:2) to remove photoresist or other heavy organic residue
1a.	overflow rinse in DI water to 10 megohms
2.	20 min in $NH_4OH:H_2O_2:H_2O$ (1:1:5) at 80-85°C to remove residual photoresist film or light organic contamination
2a.	overflow rinse in DI water to 10 megohms
3.	60 sec in dilute HF 10:1 at room temperature to remove the thin layer of SiO_2
3a.	overflow rinse in DI water to 10 megohms
4.	20 min in $HCl:H_2O_2:H_2O$ (1:1:5) at 80-85°C to remove inorganic contaminants
4a.	overflow rinse in DI water to 10 megohms
5.	blow dry with N_2

Oxidation. In order to perform the orientation dependent etch (ODE) (to be discussed later), a thick oxide was grown over both sides of each wafer. This oxide must be thick enough to serve as a mask during the etching of the grooves. Also, the oxide following the ODE must be

sufficiently thick to serve as a mask for the subsequent diffusion processes.

To determine the oxide thickness required to serve as a mask during the ODE, the etch rate of (110) silicon (R_{110}) and the etch rate of SiO_2 (R_{ox}) had to be determined. According to Kendall and Guel [27], the etch rates are a function of both the temperature and concentration of the etchant. Figure 4-22 shows the SiO_2 and Si etch data at different KOH/H_2O concentrations and temperatures. The concentration selected was a 50% by weight of both KOH and

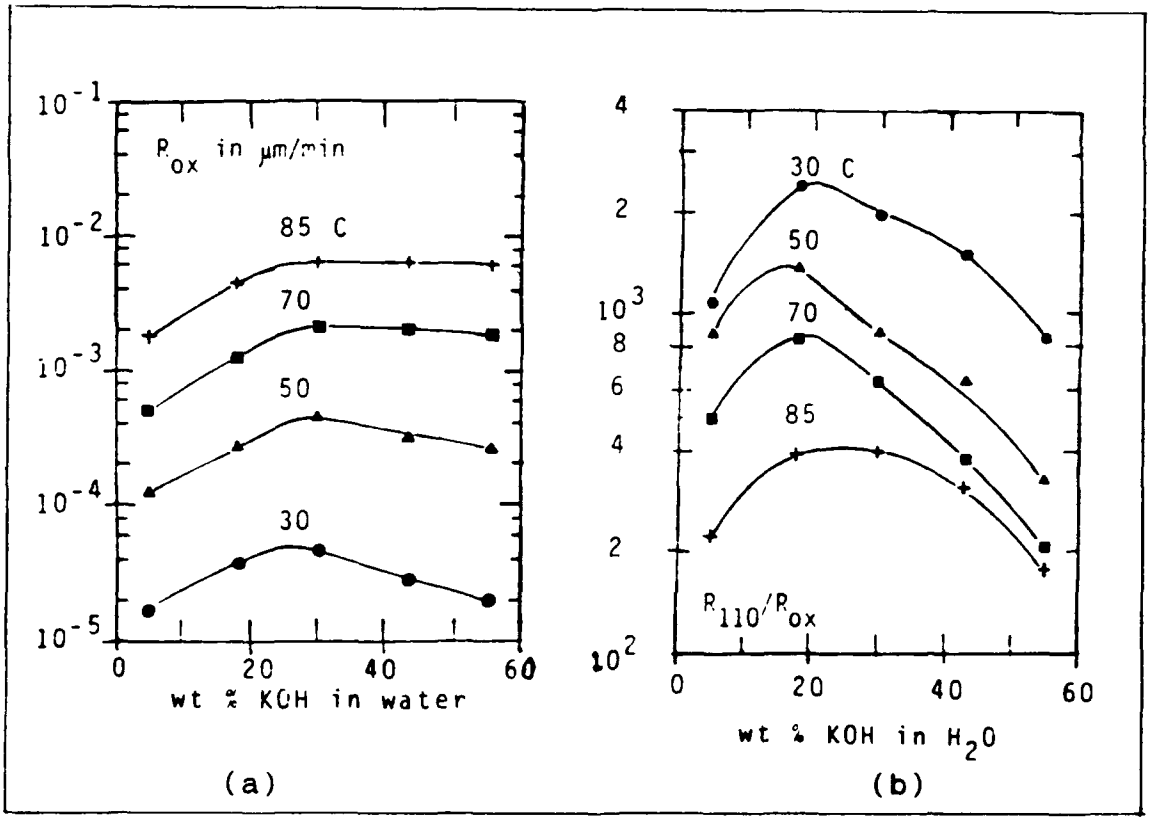


Figure 4-22. Silicon dioxide etch data [27:112].

water, and the temperature selected was 85°C (why these values were selected will be discussed later). The ratio R_{110}/R_{ox} from Figure 4-22b is 230. Therefore, to etch 290 um (depth of grooves) of (110) silicon, an oxide mask at least 290 um/230 = 1.26 um thick is required.

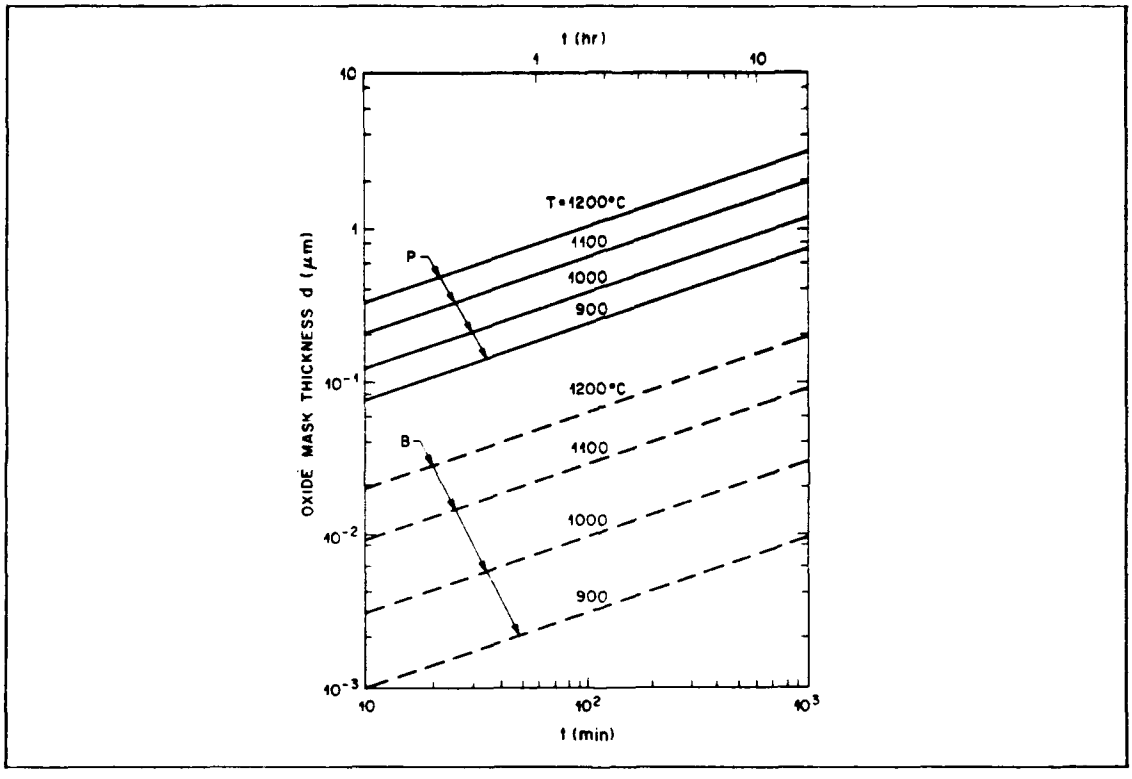


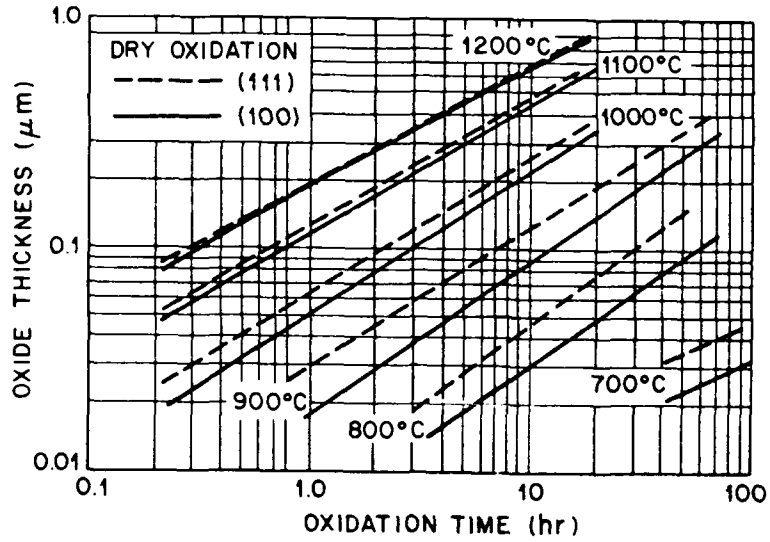
Figure 4-23. Minimum thickness of SiO_2 required to mask against phosphorus and boron as a function of diffusion time with diffusion temperature as a parameter [19:400].

As can be seen from Figure 4-23, 0.7 um is more than enough to mask against either phosphorus or boron diffusions at 900°C. Therefore, the total oxide thickness selected to insure an adequate oxide was the sum of the thicknesses

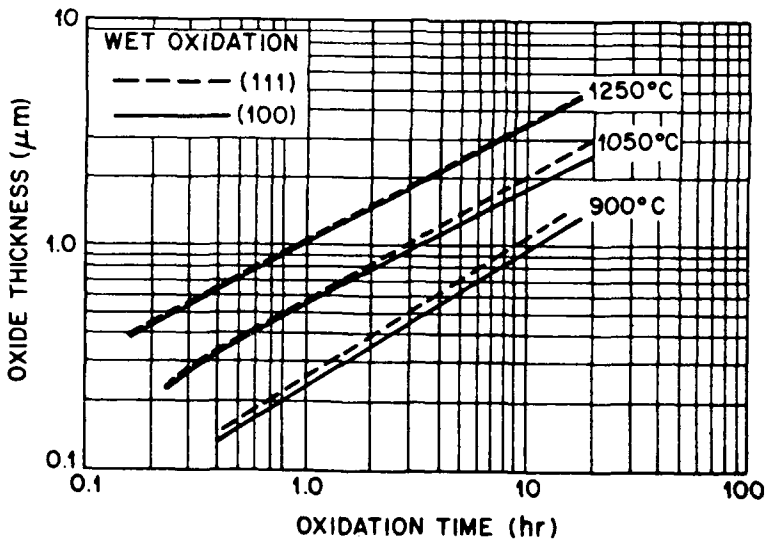
required to mask during the ODE and the thickness required to mask during doping. This thickness is approximately 2 um.

Since solar cells subjected to high doping and oxidation temperatures cause deterioration of the minority carrier lifetimes [7:8], the temperature selected for oxidizing the wafers was 900 °C. To obtain a 2 um oxide thickness in dry oxygen requires an unreasonable amount of time, as can be seen from Figure 4-24a. Therefore, the oxidation was accomplished in wet oxygen. The time required to grow an oxide 2 um thick from Figure 4-24b is approximately 33 hours. To oxidize the wafers, oxygen was bubbled through water heated to 99 °C.

The procedures followed for oxidizing the wafers was to place the wafers in a quartz boat used only for oxidizing. The furnace was purged with dry oxygen. Next, the wafers were pushed slowly into the hot zone of the oxidation furnace at a 1 inch per minute rate. Once the wafers were in the hot zone, the boat was pushed to the center of the furnace. The dry oxygen was then diverted through the bubbler to saturate it with steam. The oxidation in steam was carried out for 33 hours. This required the bubbler to be refilled every 4 to 6 hours. After 33 hours, the steam was turned off and dry nitrogen was allowed to flow for 10 minutes to stop the oxidation process and anneal the wafers.



(a)



(b)

Figure 4-24. Silicon dioxide thickness as a function of reaction time and temperature. (a) Dry oxygen growth, (b) Steam growth [19:350].

The boat of wafers was then pulled to the edge of the hot zone of the furnace and then slowly withdrawn at the 1 inch per minute rate. The wafers were removed from the furnace, allowed to cool, and stored in a covered wafer holder.

Groove Photolithography. The most critical and the most difficult steps in the fabrication process were the groove photolithography steps. Perfecting these steps were the most time consuming of all the processing steps. Success depended on factors which were not within the control of the fabricator, such as laboratory temperature, humidity, equipment availability, ambient air quality, and equipment malfunctions. The steps below are those which were used in the final process:

1. Standard clean
2. Wafer bake
3. Negative photoresist application (front side)
4. Softbake
5. Mask alignment and exposure
6. Photoresist development
7. Hardbake
8. Hexamethyldisilazane (HMDS) application (backside)
9. Positive photoresist application (backside)
10. Hardbake
11. Oxide etch
12. Photoresist removal

These steps will be described in detail.

Standard Clean. This process is accomplished in a 1000 milliliter Pyrex beaker. The wafers were first placed in a polypropylene wafer holder. Next, 300 ml of sulfuric acid (H_2SO_4) was poured into the beaker. Next, 200 ml of hydrogen peroxide (H_2O_2) was poured into the beaker. The wafers were immediately placed into this solution. The solution begins to bubble and evolve heat as the exothermic reaction takes place. This process cleans all organic substances from the wafer. The wafers are immersed for 10 to 20 minutes and then rinsed in DI water to a 10 megohm standard then removed. The excess water was blown off the wafers with dry N_2. The wafers were then placed in a clean quartz boat.

Wafer Bake. The quartz boat of wafers was transferred to an oven heated to 200°C. The wafers were baked at least 30 minutes, but not longer than 4 hours. The purpose of this bake was to drive-off surface moisture prior to resist coating.

Negative Photoresist Application. Since the grooves are only 5 um, a photoresist with fine resolution is necessary. Waycoat Type 3 IC Resist (28 cps, Hunt Chemical Corporation, Palisades Park, New Jersey) with a resolution of 0.05 to 0.1 mil (1.27 to 2.54 um) resolution was chosen. To protect the backside of the wafer from scratches and

contaminates, a piece of lens paper the size of the wafers was placed on the photoresist spinner's chuck. The wafer was then positioned on the chuck. Vacuum was applied and dry N_2 was blown over the wafer to remove dust. A standard bulb dropper (approximately 3/4 full) was used to dispense a puddle of the the photoresist on the center of the wafer. The spinner was started immediately and spun 30 seconds at 5000 rpm. After the spinner stopped, the vacuum was removed and the wafer was placed in a wire boat lined with clean aluminum foil. The boat was also covered with foil, being careful not to allow the foil to contact the freshly coated wafer. The purpose of this cover was to keep dust off the coated wafers.

Softbake. The wafers were softbaked at 65 $\pm$ 5°C for 10 to 20 minutes. This bake was done in a forced air oven to exhaust the evolving photoresist solvent and to insure that the temperature at the surface of the wafer was constant. If the coated wafer was to be stored before exposure, the softbake was postponed until just prior to the exposure operation.

Mask Alignment and Exposure. Several methods of aligning the proper crystal plane of the wafer with the grooves were tried, and the most reliable method was to align the flat of the wafer with an alignment mark on the groove mask. The Virginia Semiconductor wafers were aligned

with the grooves parallel to the wafer flat. The Ametek wafers were aligned with the grooves perpendicular to the wafer flat. The wafers were aligned using the laboratory mask aligner. The best exposure time (t_e) was found experimentally to be a function of the light intensity (I), which according to the light intensity meter, was not always the same. However, the proper exposure time could be calculated by first measuring the intensity (I), and then using the formula:

$$t_e \times I = 3.9 \quad s \cdot mW/cm^2 \qquad (42)$$

where t_e is in seconds and I is in mW/cm^2. Consequently, the intensity was checked on the intensity meter prior to exposing the wafers and the exposure time was calculated. Each wafer was carefully aligned, using the microscope on the mask aligner, and exposed for the calculated time.

Photoresist Development. To obtain fine resolution, the Waycoat Type 3 IC photoresist was developed by an immersion process. The developer chemicals were placed in three 3-inch watch glasses and kept covered when not being used. The following development procedure was used:

Developing Solution	Time (sec)
Xylene	90
Xylene (fresh solution)	15
N-Butyl Acetate	15
Blow dry with Nitrogen	

After developing, each wafer was checked under the optical microscope for oerects due to dust and scratches. If necessary, the resist was stripped using the standard clean process and the necessary processing steps were reaccomplised.

Hardbake. The wafers were placed in the foil lined wire boats, covered with foil, and baked at 135 $\pm$ 5 °C for 15 minutes. The wafers were baked in a forced air oven to insure the temperature of the wafer was constant. If the developed wafers were to be stored before etching the oxide, the hardbake was postponed until all the remaining photolithgraphy steps could be completed.

After the hardbake was completed, the backside of the wafer was coated with a positive resist to protect the oxide. These steps are described next.

Hexamethyldisilazane (HMDS) Application. To prepare the wafer's surface for the positive resist, HMDS was first applied to the surface of the wafer. This material improves the adhesion of the photoresist. The wafer was placed on the photoresist spinner's chuck with the

backside up. A piece of clean lens paper was placed between the wafer and the chuck to protect the topside from being scratched. The spinner's vacuum was applied and the wafer's surface blown off with dry nitrogen. A puddle of HMDS was placed in the center of the wafer using a bulb dropper. The wafer was then spun at 4000 rpm for 30 seconds.

Positive Photoresist Application. When the spinner stopped, a puddle of Shipley M1350J Positive Photoresist was placed in the center of the wafer with a bulb dropper. The wafer was then spun at 5000 rpm for 20 seconds. When the spinner stopped, the vacuum was removed, and the wafer was placed in the foil lined wire boat to hardbake the resist.

Hardbake. Since the backside of the wafer did not require patterning, no softbake or exposure was necessary. Therefore, the positive photoresist was immediately hardbaked. The hardbake was done in a forced air oven at 135 $\pm$ 5 °C for 45 minutes. The wafers were then ready for the oxide etch.

Oxide Etch. In order to anisotropically etch the silicon grooves, windows were isotropically etched into the silicon dioxide to serve as a mask. The isotropic oxide etch was accomplished using a buffered hydrofluoric acid (NH_4OH:HF, 6:1) solution. This etchant must be mixed at least 2 hours before using to allow it to stabilize. A

control wafer, which had been oxidized with those being processed, was first etched in the buffered etch to determine the time required to completely etch through the oxide. Since silicon dioxide is hydrophilic and silicon is hydrophobic, the control wafer could be easily checked for etch completion. The nominal etch rate was expected to be about 0.1 um/min. Since the expected oxide thickness was 2 um, the time required to etch through the oxide was 20 minutes. The test wafer was etched for 18 minutes and then checked every 15 seconds to determine the precise time required to etch through the oxide. Once the required time was determined, the solar cell wafers were etched for this time plus 30 seconds to insure the oxide was completely removed.

Photoresist Removal. To verify that the oxide was etched only where a groove was to be, both photoresists were removed and the wafer was checked under the optical microscope. To remove the photoresists, the wafers were cleaned using the standard clean process used at the beginning of the groove photolithography process. The wafers were now ready for the orientation dependent etch.

Orientation Dependent Etching. The unique anisotropic etching characteristics of (110) silicon wafers has been attributed to the crystallographic properties of the various planes [28:49]. According to Kendall [27:113], grooves of

good uniformity and depth are best achieved with large KOH concentrations. In order to achieve deep but narrow grooves, the etch rate in the <110> direction (R_{110}) must be much greater than the etch rate in the <111> direction (R_{111}). Figure 4-25 shows the ratio R_{110}/R_{111} as a function of the KOH concentration.

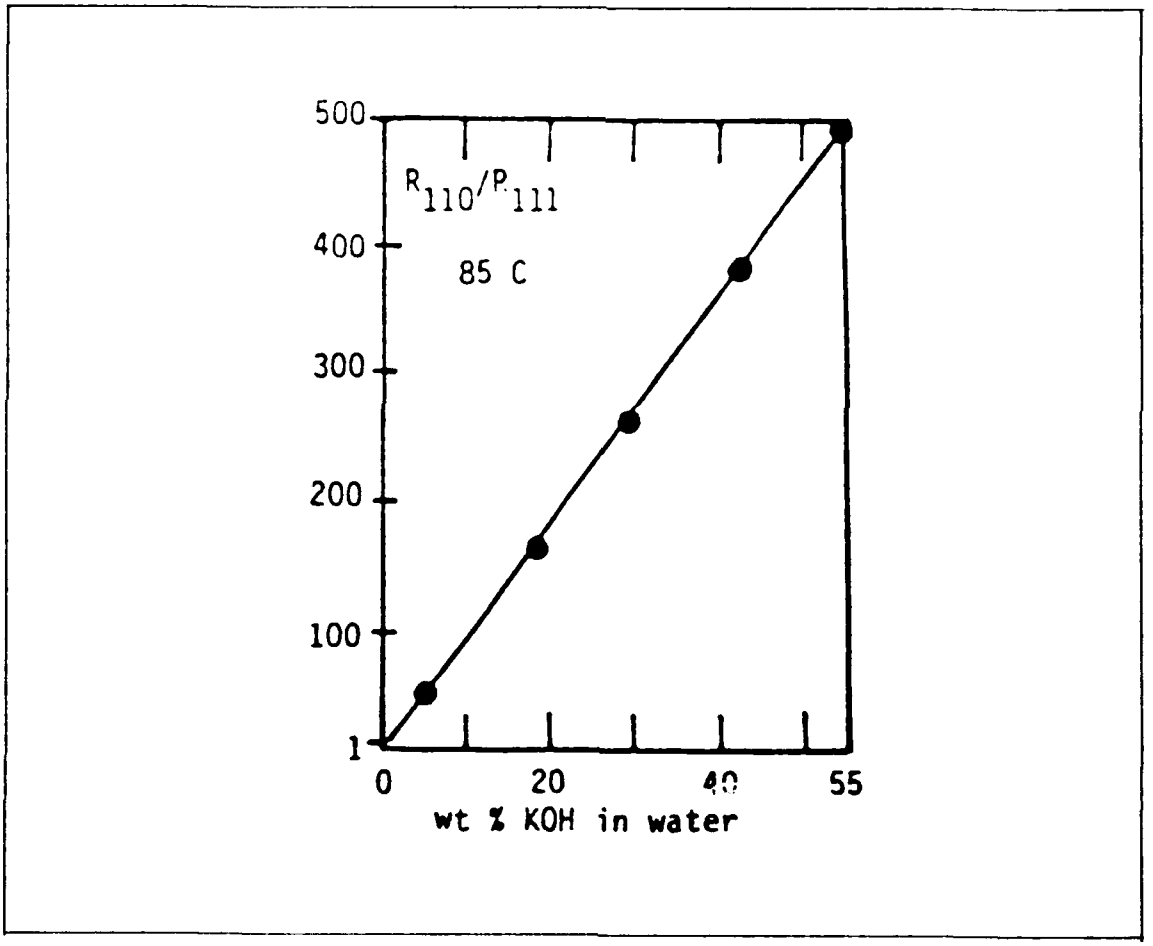


Figure 4-25. The ratio of the silicon etch rate in the <110> direction to the <111> direction versus the potassium hydroxide concentration [27:109].

From this graph, it can be observed that for increasing KOH concentration, the ratio is higher. This graph represents the ratios at 85°C. Lower temperatures yield similar results if the wafer or solution is agitated [27:110]. To etch the grooves, a 50% KOH concentration was selected to achieve good uniformity. Figure 4-26 shows the R_{110} etch rate as a function of the KOH concentration at different temperatures. To etch the grooves faster, the temperature

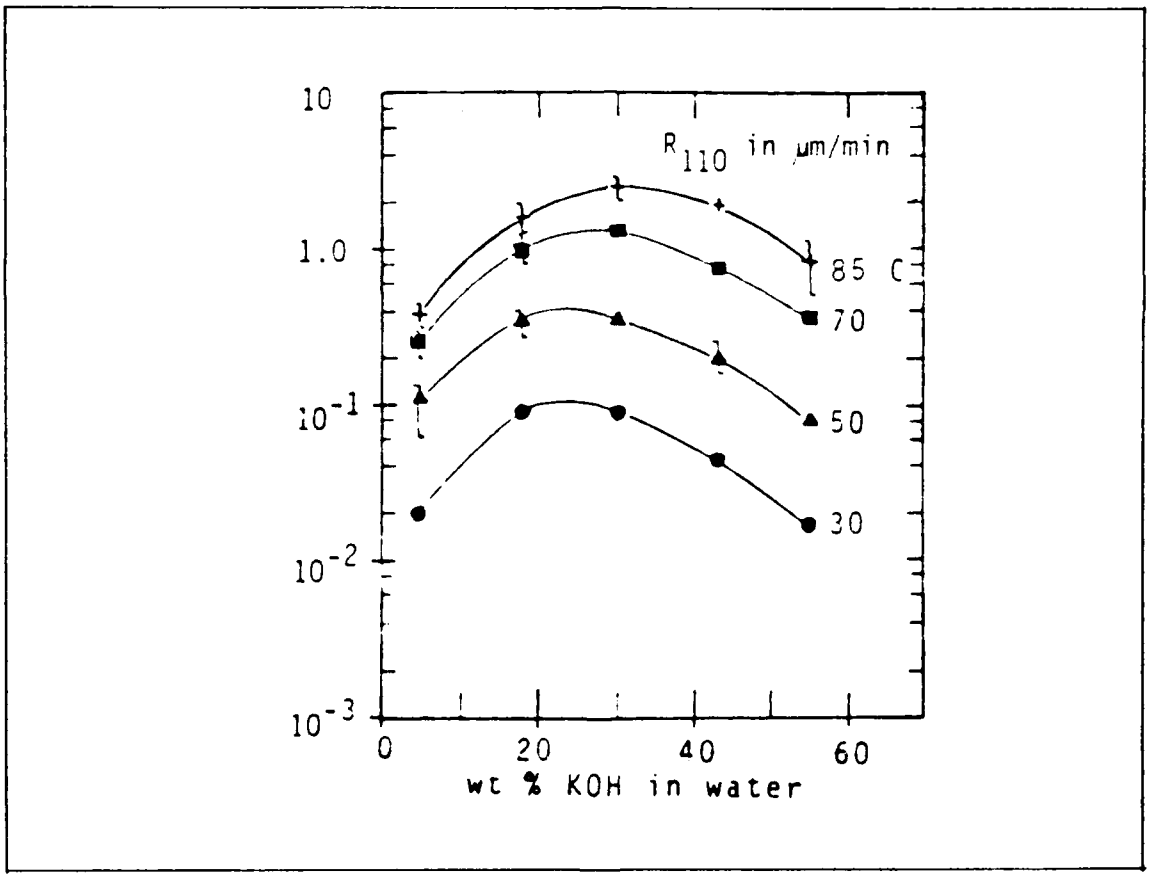


Figure 4-26. The silicon etch rate in the <110> direction as a function of the potassium hydroxide concentration [27:109].

can be increased. However, the disadvantage of etching at a higher temperature is that the oxide etch rate increases faster than the silicon etch rate, as shown in Figure 4-22b. However, lower temperatures require agitation to achieve high R_{110}/R_{111} ratios. Therefore, the temperature chosen for etching was 85°C.

The etching procedure, used in the fabrication of the BCVJ solar cell, utilized the Lufran (Macedonia, Ohio 44056) Superbowl II etching apparatus shown in Figure 4-27. A clean 1000 milliliter teflon beaker was used to hold the etchant. The etchant consisted of 400 grams of DI water and 400 grams of KOH pellets. A plastic cover was placed over the teflon beaker and held in place with a teflon lid as shown in Figure 4-28. The teflon beaker was positioned in the etching apparatus water bath. The bath was filled with DI water until the water level in the etching apparatus was just above the etchant level in the teflon beaker. This arrangement formed a stabilized hot water bath for the etchant. The etching apparatus was set to 85 °C and started. Once the bath reached 85 °C, it was allowed to stand for at least 2 hours to insure the temperature of the etchant in the beaker was stabilized.

Wafers to be etched were secured with a 2-inch polypropylene wafer holder. The wafers were immersed into the etchant in the teflon beaker and covered with the

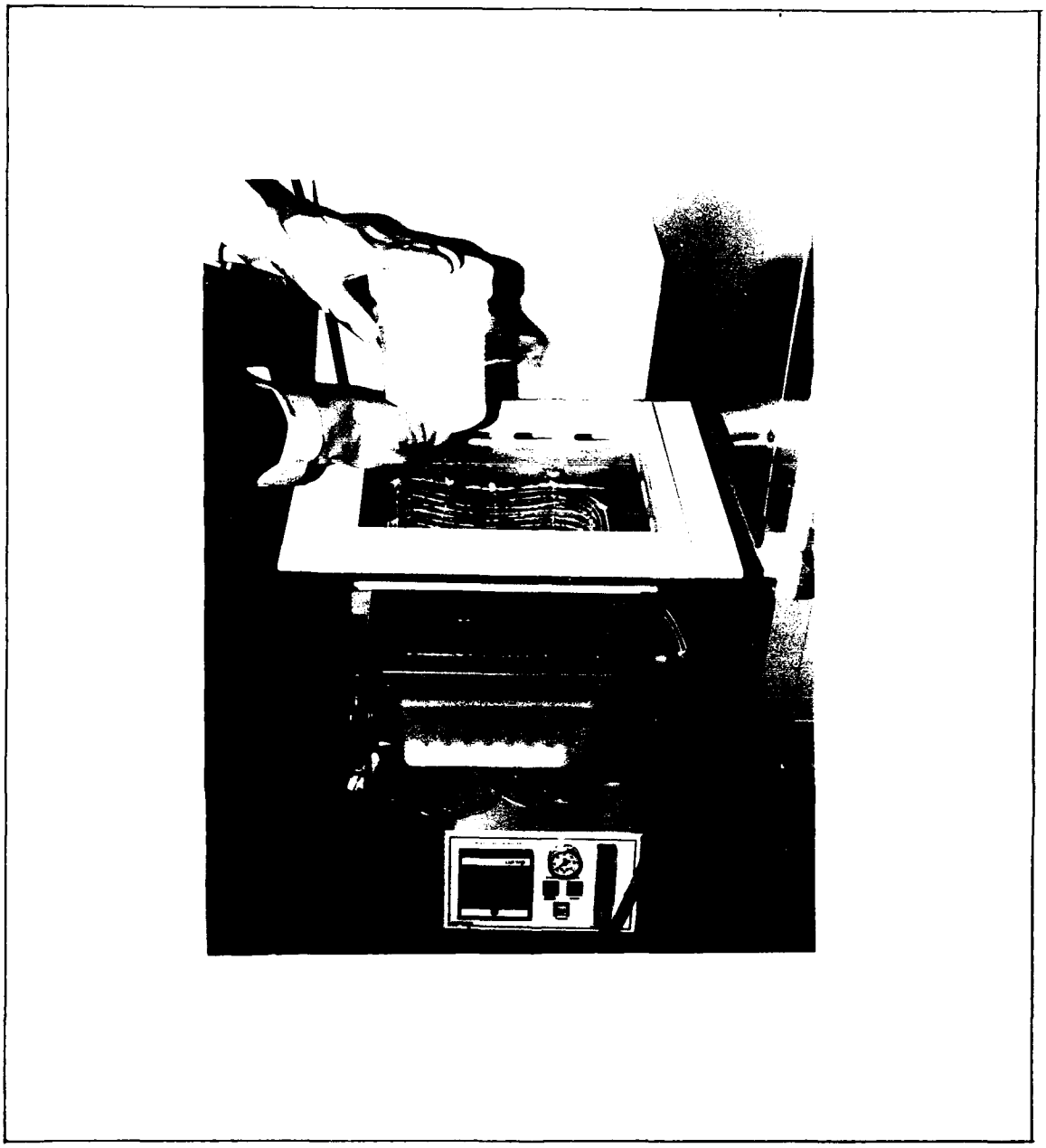


Figure 4-27. Lufran Superbowl II etching apparatus.

plastic and teflon lid. The wafers were then etched for 3 hours. The wafers were removed and rinsed in DI water to a 10 megohm standard. They were then removed from the water and blown dry with nitrogen. The wafers were examined under

the optical microscope for the occurrence of slits appearing on the backside. If etch-through had not occured (no slits on the backside), then the wafers were etched at 15 minute intervals until the slits could be detected under the optical microscope. Barely visible slits could be detected by shining a bright microscope light through the topside while observing the backside with the optical microscope.

Figure 4-28. Teflon beaker with plastic seal under lid.

Pointing the Groove Walls. Although this process was not used on the final cells, the procedures are discussed briefly because it was attempted and the results were promising. The top of the groove walls can be pointed with a planar chemical etch. The etchant was mixed in a 1000 milliliter teflon beaker. The etchant consisted of a $HF:HNO_3:CH_3COOH$ solution in the ratio of 2:15:5 [31:522]. The backside of the wafers must be protected during the planar etching process by some means. A negative photoresist was tried, but it was not compatible with the etchant. The results are discussed in greater detail in Chapter V. Once the backside of the wafer is protected, the oxide on the top of the groove walls is removed in buffered HF. The wafer is then immersed in the planar etchant for 5-6 minutes. The wafer is then rinsed in DI water and gently blown dry with dry nitrogen. If the grooves are well pointed, the grooved area will look darker because light is no longer reflected from the top of the walls.

P+ Photolithograpy and Diffusion. In order to provide a good ohmic contact between the metal the substrate, p+ diffusion runs were diffused into the backside of the wafers. Low temperature boron nitride planar diffusion sources (PDS) were used to dope the wafers. The following list is a summary of the critial procedures and the order of the p+ photolithography and diffusion process:

1. Standard clean
2. Wafer bake
3. Negative photoresist application
4. Softbake
5. Mask alignment and exposure
6. Photoresist development
7. Hardbake
8. Oxide etch
9. Wafer clean
10. Planar diffusion source (PDS) wafer preparation
11. Diffusion boat loading
12. Diffusion furnace settings
13. Predeposition
14. Deglaze and sheet resistance check
15. Oxidation and drive-in

Each step will be described in detail.

Standard Clean. The wafers were cleaned using the $H_2SO_4:H_2O_2$ (3:2) solution for 15 minutes.

Wafer Bake. The wafers were baked at 200°C for 30 minutes to remove surface moisture.

Negative Photoresist Application. Waycoat IC Type III resist (28 cps) (Hunt Chemical Corporation) with a resolution of 0.05 to 0.1 mil was chosen. To protect the front side of the wafer from scratches and contaminates, a piece of lens paper the size of the wafers was placed on the

spinner chuck. The wafer was placed on the spinner with the lens paper sandwiched between it and the chuck. Vacuum was applied and dry N_2 blown over the wafer to remove dust. A bulb dropper was used to place a puddle of the photoresist in the center of the wafer. The spinner was started and spun for 30 seconds at 5000 rpm. Once the spinner stopped, vacuum was removed and the wafer was placed in a wire boat lined with clean aluminum foil. The boat was also covered with foil. The purpose of this cover was to keep dust off the wafer.

Softbake. The wafers were softbaked in a forced air oven at 65 + 5 °C for 10 to 20 minutes. If the coated wafer is to be stored before exposure, the softbake should be postponed until just prior to exposure.

Mask Alignment and Exposure. The p+ diffusion mask was aligned with the slits on the backside so that each run would lie half way between two rows of slits and extend 90 mils past one end and 10 mils past the other end. Figure 4-29 shows the proper alignment of the p+ pattern with the slits. The exposure time was determined as in the groove photolithography "align mask and expose" step.

Photoresist Development. The photoresist was developed using the same process discussed earlier in the groove photolithography "photoresist development" step.

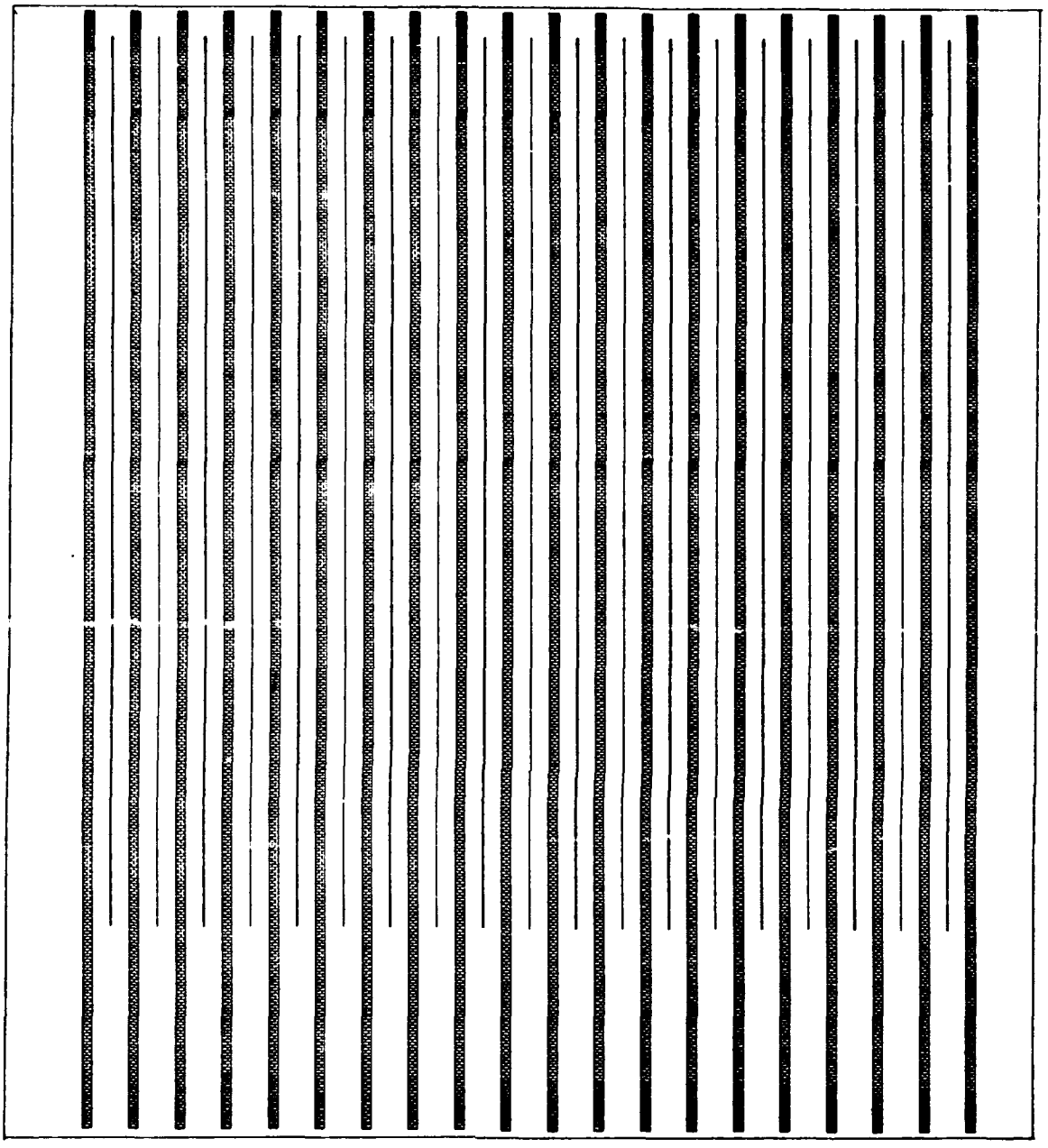


Figure 4-29. P+ pattern alignment with the slits on the backside of the wafer (one cell pattern) (magnification 11.9x).

Hardbake. See the groove photolitography "hardbake" step.

Oxide Etch. The oxide was etched using a 6:1 solution of NH_4F:HF. The time required to etch the oxide was determined by first etching a test wafer which had been through the ODE process. When the wafer went hydrophobic, the etching was complete.

Wafer Clean. This cleaning process was identical to the one used just prior to the initial oxidation step. The wafers were allowed to remain in the DI rinse until the PDS wafers were prepared.

Planar Diffusion Source (PDS) Wafer Preparation. The dopant sources used for the p+ diffusion were Transtar Boron Nitride Low Temperature Planar Diffusion Sources (Grade BN-975) made by the Carborundum Company (Niagara Falls, New York 14302). These dopant sources were not taken from the factory package until just prior to their use. These wafers were prepared according to the manufactures technical data sheet as follows:

Dry

1. Bake.....350-400°C/Dry N_2/1 hr.

Activation

1. Oxidize.....900-950°C/Dry O_2/30 min.
2. Stabilize.....Use temperature/Dry N_2/30 min.

Storage

1. Tube or Special Oven..350-450°C/Dry N_2 or
2. Lab Oven*.....100-250°C/Dry N_2 or
3. Dry Box*.....Room temperature/Dry N_2

*NOTE: Requires daily bake-out at diffusion temperature/dry N_2/30 min.

Diffusion Boat Loading. The planar diffusion sources were loaded into a clean quartz boat used only for boron doping. A blank silicon wafer was placed in the same slot as the wafer to be doped so that it was in contact with the grooved side of the wafer. The purpose of the blank wafer was to prevent the grooved side of the wafer from being doped with boron. The distance between the dopant source slot and the silicon wafer slot was 100 mils. The stacking arrangement is shown in Figure 4-30.

Diffusion Furnace Settings. The large diameter tube, p-dopant furnace was set for 900 +0.5 °C using the laboratory thermocouple. The furnace tube was purged with dry N_2. Once the wafers were in the furnace and the cap was in place, the N_2 flow rate was reduced to the minimum detectable flow.

Predeposition. The loaded boat was slowly pushed into the furnace at rate of 1 inch per minute. Once the boat was in the hot zone, it was pushed to the center of the

furnace. The cap was placed on the end of the furnace tube and the N_2 flow rate was reduced. The wafers were allowed to diffuse in the furnace for 1 hour. They were then pulled to the edge of the hot zone and removed slowly (1 inch per minute). The wafers were removed from the furnace tube and allowed to cool.

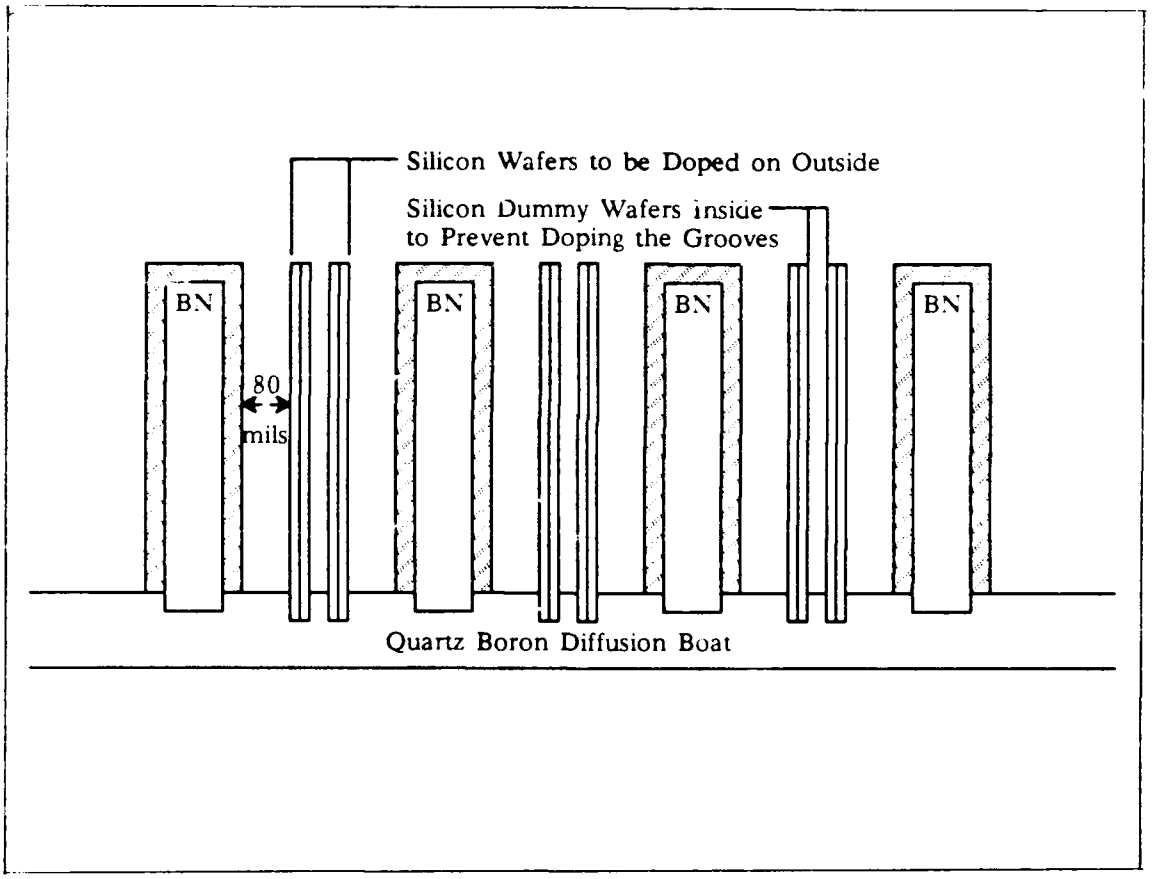


Figure 4-30. Stacking arrangement of the boron nitride planar diffusion sources and the silicon wafers.

Deglaze and Sheet Resistance Check. To remove the borosilicate glass and terminate the introduction of impurites, the wafers were deglazed as follows:

1. The wafers were immersed in a 10:1 DIW:HF solution for 30 seconds and then rinsed thoroughly in DI water.
2. The wafers were boiled for 15 minutes in HNO_3 and rinsed thoroughly in DI water.
3. The sheet resistance of a test wafer was checked using the Veeco (Plainview, New York 11803) AP-150 four-point probe.
4. The wafers were dipped one final time into a 10:1 DIW:HF solution for 30 seconds and rinsed in DI water to a 10 megohm standard.

Oxidation and Drive-in. Since an n+ diffusion is done later, an oxide must be grown over the p-regions to prevent these regions from being over-compensated. However, this will also drive-in the p-dopant and decrease the concentration at the surface. The concentration of the p-dopant at the surface must remain above that necessary to achieve a good ohmic contact (above $10^{19}/cm^3$) [19:170]. Therefore, the thickness of the oxide necessary to mask against phosphorus must first be determined. Next, the time required to grow that amount of oxide can be determined.

Finally, the concentration at the surface after that time can be calculated.

The thickness of oxide necessary to mask against phosphorus was determined from Figure 4-23. Since the phosphorus diffusion will be less than 30 minutes and the diffusion temperature less than 900°C, then an oxide thickness of 2000 to 3000 angstroms is sufficient. From Figure 4-24, the time required to grow an oxide greater than 3000 angstroms is about 2 hours. Further, the dopant concentration at the surface after the oxidation can be calculated from the following equations [19:386-388]:

$$C_s(t) = S/(\pi Dt)^{1/2} \text{ cm}^{-3} \quad (43)$$

and

$$S = 2(Dt/\pi)^{1/2} C_{ss} \text{ cm}^{-2} \quad (44)$$

where $C_s(t)$ is the surface impurity concentration at t, C_{ss} is the solid solubility of boron in silicon at 900°C (approximately 10^{20} atoms/cm^3 [29:22]), D is the diffusion coefficient of boron in silicon at 900 °C (approximately 4×10^{-14} cm^2/sec [29:45]), and t is time in seconds ($2.5 \times 3600 = 9000$ sec). Thus,

$$S = 2(4 \times 10^{-14} \cdot 9000/\pi)^{1/2} \cdot 10^{20} = 2 \times 10^{15} \text{ cm}^{-2}$$

so

$$C_s(t) = 2 \times 10^{15}/(4\pi \times 10^{-14} \cdot 9000)^{1/2} = 6 \times 10^{19} \text{ cm}^{-3}.$$

Therefore, the drive-in/oxidation step can be as long as 2.5 hours at 900°C and still have a sufficient surface concentration to provide a good ohmic contact.

The diffusion boat was reloaded without the diffusion sources and the wafers pushed slowly back into the p+ diffusion furnace. The wafers were allowed to oxidize in dry O_2 for 30 minutes. The wafers were then removed from the diffusion furnace, (1 inch per minute rate) and placed into an oxidation boat. The wafers were placed into the oxidation furnace and oxidized in wet O_2 for 2 hours. The wafers were then removed from the furnace and allowed to cool. This completed the p+ photolithography and diffusion process.

N+ Photolithography and Diffusion. Both sides of the wafers were doped with phosphorus. The backside was doped with 4 mil (101.6 um) wide runs connecting each row off slits. The complete topside, including the grooves, was also doped. This procedure was intended to connect the top n+ layer to the back n+ runs through the diffusion path in each slit. The runs on the backside were designed to overlap the slits by 90 mils (2,286 um) on one end and 10 mils (254 um) on the other end. The 90 mil overlap was opposite the side that the p+ run overlapped 90 mils. Figure 4-11 shows how the contact pattern, n+ pattern, and p+ pattern align. In this figure, the n+ contact region

would represent the region of the slits. The following steps are a summary and order of the n+ photolithography and diffusion process.

1. Standard clean
2. Wafer bake
3. Negative photoresist application
4. Softbake
5. Mask alignment and exposure
6. Photoresist development
7. Hardbake
8. Oxide etch
9. Wafer clean
10. Planar diffusion source (PDS) wafer preparation
11. Diffusion boat loading
12. Diffusion furnace settings
13. Deposition process
14. Deglaze and sheet resistance check

Steps 1 - 9 used identical processing procedures as described in the "P+ Photolitography and Diffusion" process with the following exceptions. The wafers were coated twice with photoresist using a spin speed of 3000 rpm instead of 5000 rpm in order to achieve good uniformity. The wafers were exposed for 100 seconds in the laboratory mask aligner

using the n+ mask in order to completely expose the thicker resist.

(PDS) Wafer Preparation. The dopant sources used for the n+ diffusion process were Phosphorus, PH-950, n-Type, Planar Diffusion Sources (PDS) purchased from the Carborundum Company (Niagara Falls, New York 14302). These dopant sources were not taken from the factory package until just prior to their use. The PDS wafers were prepared according to the manufactures technical data sheet which recommends that, prior to silicon diffusion, new wafers or wafers stored over one month be annealed at 900-950 °C in dry N_2 for 8 hours. Annealing at temperatures below 900 °C is not recommended. If wafers have been stored overnight after a recent anneal, a minimal one hour anneal at the anneal temperature is recommended.

Diffusion Boat Loading. A quartz boat, manufactuered by ASQ Boats (Tustin, California 92680) was specially ordered for the phosphorus diffusion. This boat has a slot for a silicon wafer located between two slots for PDS wafers. The PDS wafers were spaced 100 mils (2,540 um) from the silicon wafer. With a PDS wafer on either side of the silicon wafer, phosphorus could be diffused into both sides of the wafer at one time. Figure 4-31 shows the stacking arrangement of the silicon wafers and the phosphorus diffusion sources.

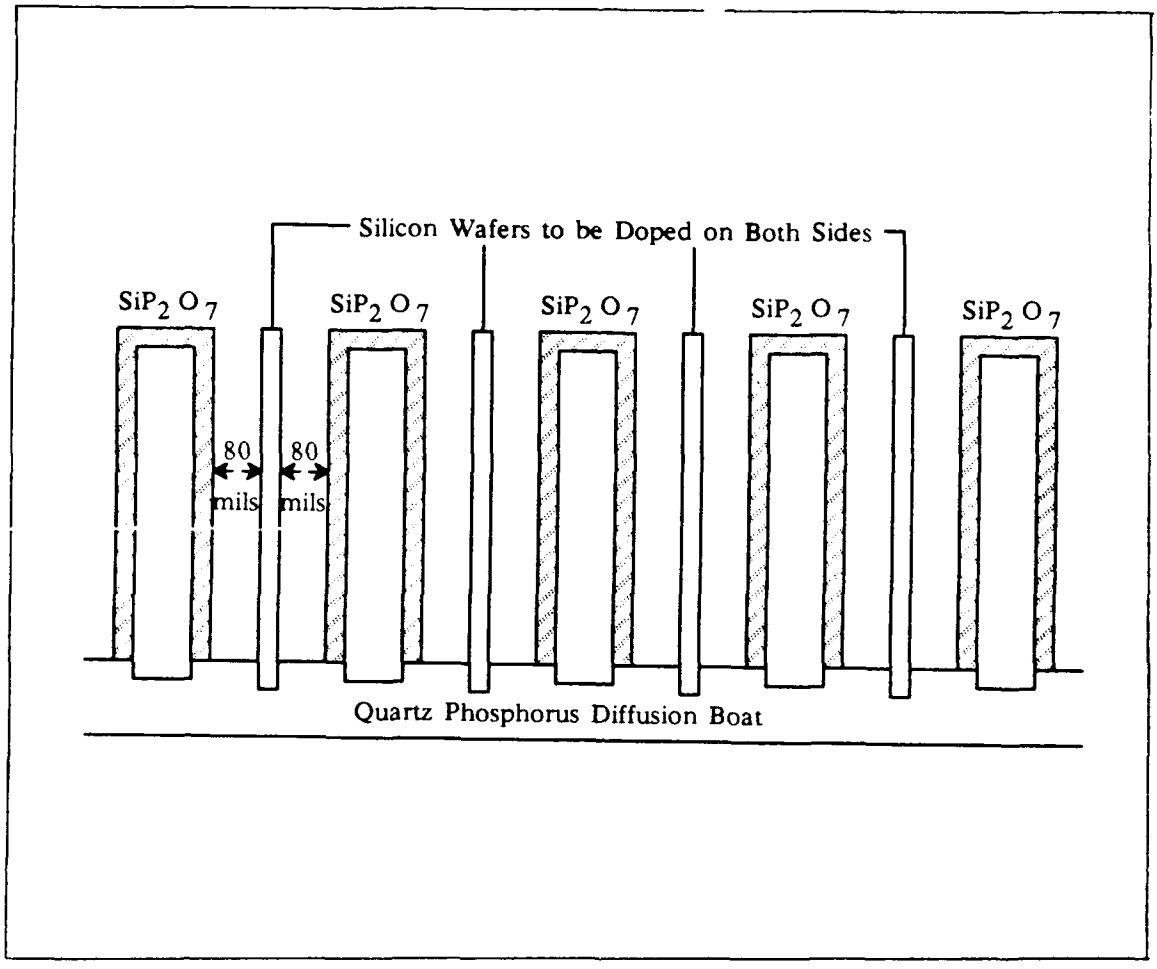


Figure 4-31. Stacking arrangement of the silicon wafers and the phosphorus diffusion sources.

Diffusion Furnace Settings. The furnace temperature was chosen to achieve as shallow a junction as possible. Figure 4-32 shows the manufacturer's specifications for junction depth as a function of diffusion time and temperature. The time chosen was 10 minutes, and the temperature was 875 °C.

Deposition Process. The loaded boat was pushed into the hot zone of the furnace using a 2 inch per minute rate and then pushed into the center of the furnace with dry

N_2 flowing. The furnace was then capped and the N_2 adjusted for a minimal flow. After 10 minutes, the N_2 was turned off and dry O_2 allowed to flow 5 minutes to passivate the wafer's top surface with a thin oxide. The wafers were removed from the furnace using a moderate extraction rate of 3 inches per minute. The wafers were allowed to cool to room temperature before they were placed in their wafer holder.

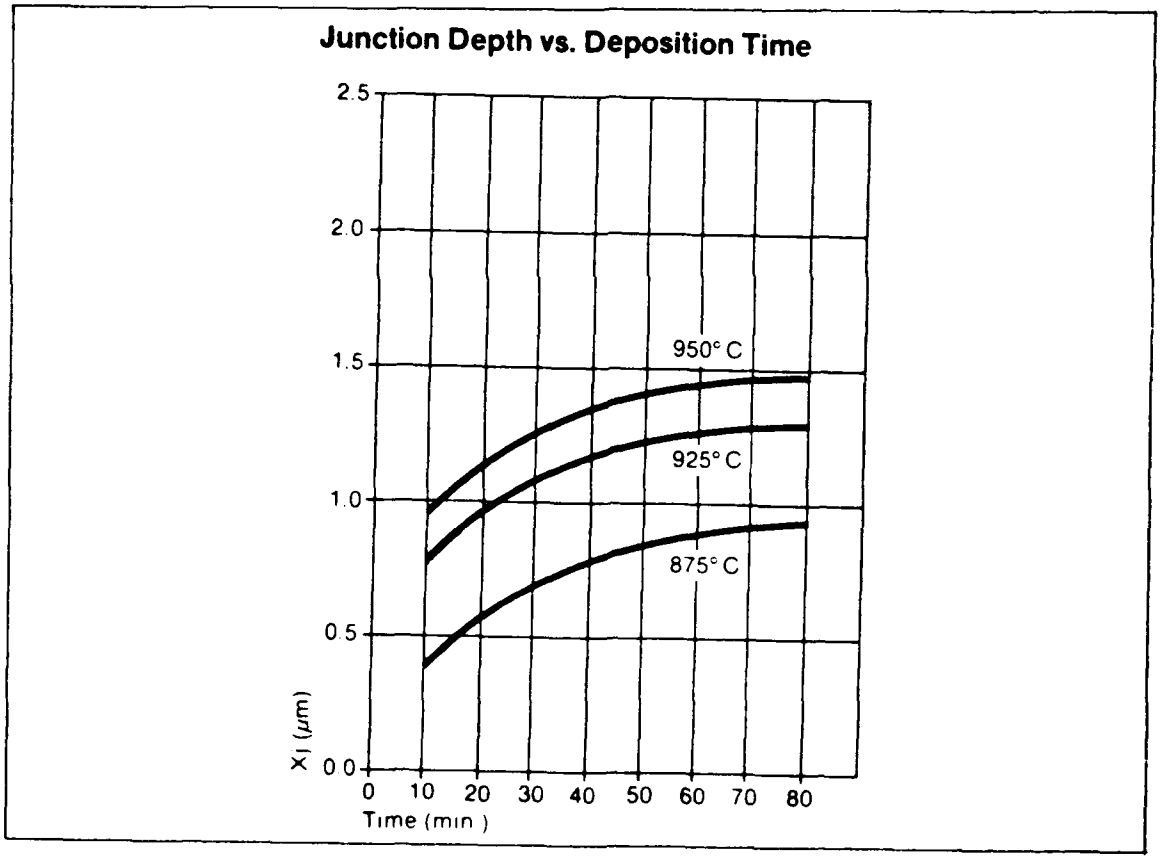


Figure 4-32. Manufacturer's specification for junction depth as a function of time and temperature [29:2].

Deglaze and Sheet Resistance Check. A silicon test wafer which had been processed with the other wafers was deglazed (DIW:HF, 10:1, for 15 seconds) and the sheet resistance checked. According to Kaba [14:C-2], a sheet resistance of 89 ohms/square results in the best efficiency. According to Figure 4-33, a sheet resistance greater than 50 ohms/square is not possible. However, the sheet resistance measured was about 200 ohms/square. Therefore, the wafers were deglazed and the deposition was repeated. The sheet resistance of the test wafer after deglazing was then measured to be 85 ohms/square.

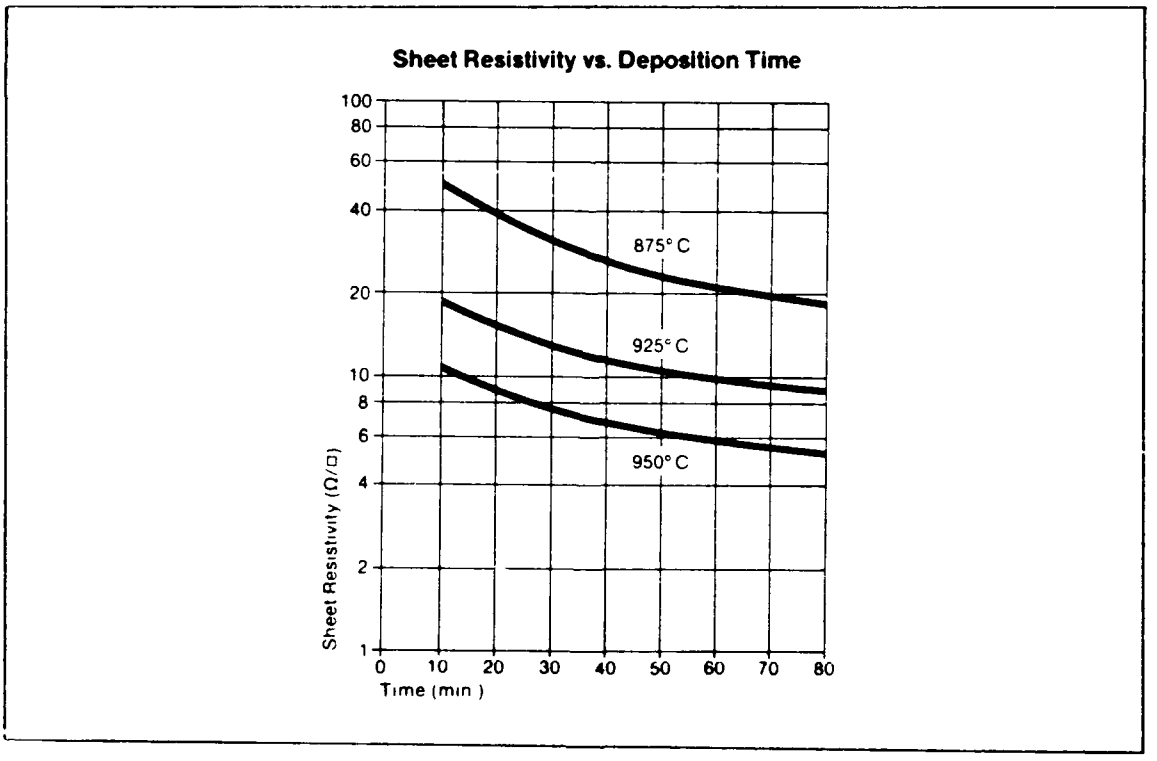


Figure 4-33. Manufacturers specification for sheet resistance as a function of deposition time and temperature [29:2].

Contact Photolithography. The contact photolithography process was identical to the n+ photolithography with the exception that the contact mask shown in Figure 4-11 was used. Figure 4-10 shows how the contact mask aligns with the n+ pattern and the p+ pattern. The contact mask could easily be aligned over the slits on the backside of the wafer. Since the diffusion patterns were 2 mils (50.8 um) larger than the contact pattern, perfect alignment was not critical. The contacts were opened by etching in DIW:HF (6:1) for 5 minutes. The wafers were then checked under the optical microscope to insure that the oxide was completely etched. The following list is a summary of the contact photolithography process:

1. Standard clean
2. Wafer bake
3. Negative photoresist application
4. Softbake
5. Mask alignment and exposure
6. Photoresist development
7. Hardbake
8. Oxide etch

Metallization and Patterning. The metallization process used in the fabrication of the BCVJ solar cell was accomplished by evaporating aluminum over the backside of

the wafer and then selectively removing the metal. The metal was removed by masking the areas were metal was to remain and etching the other areas. The following list is a summary of the metallization and patterning process:

1. Standard clean and deglaze
2. Aluminum evaporation
3. HMDS application
4. Positive photoresist application
5. Softbake
6. Mask alignment and exposure
7. Photoresist development
8. Hardbake
9. Aluminum etch
10. Photoresist removal
11. Aluminum anneal

Standard Clean and Deglaze. Before the aluminum was evaporated, the photoresist from the contact photolithography was removed using a $H_2SO_4:H_2O_2$ (3:2) solution for 15 minutes. The wafers were then rinsed in DI water until the 10 megohms standard was achieved. Next, the wafers were deglazed to provide good contact to the diffused areas were the contacts were cut. The deglazing was done by immersing the wafers in DIW:HF (10:1) for 10 seconds. The

wafers were again rinsed in DI water until the 10 megohm standard was achieved.

Aluminum Evaporation. Aluminum was evaporated onto the backside of the wafers. The thickness of the evaporated aluminum was calculated from the change in the resonant frequency (F) associated with the piezoelectric crystal. The formula used to determine the thickness (T) (in angstroms) is [30]:

$$T = 2F/\rho \tag{45}$$

where ρ is the density of aluminum (2.7 gm/cm^3 [19:374]). Two boats of aluminum where evaporated onto the wafers. The frequency changed by 13,000 Hertz; therefore, the aluminum thickness was 9,629 angstroms.

Hexamethyldisilazane (HMDS) Application. To prepare the aluminum surface for the positive resist, HMDS was first applied to the surface of the wafer. This agent acts to improve the adhesion of the photoresist. The wafer was placed on the photoresist spinner chuck with the backside up. A piece of clean lens paper was sandwiched between the wafer and the chuck to protect the wafer's topside from being scratched. The spinner's vacuum was applied, and the wafer's surface was blown off with dry nitrogen. A puddle of HMDS was placed in the center of the

wafer using a bulb dropper. The wafer was then spun at 4000 rpm for 30 seconds.

Positive Photoresist Application. When the spinner stopped, a puddle of Shipley M1350J Positive Photoresist was placed in the center of the wafer with a bulb dropper. The wafer was then spun at 5000 rpm for 20 seconds. When the spinner stopped, the vacuum was removed and the wafer was placed in the foil lined wire boat.

Softbake. The wafers were softbaked for 20 minutes at 70 $\pm$5 °C in a forced air oven. The wire boats were covered with foil to keep dust off the freshly coated wafers.

Mask Alignment and Exposure. The wafers were exposed in the mask aligner using the metal mask shown in Figure 4-14. The exposure time used was 100 seconds. Figure 4-13 shows how the metal pattern aligns with the diffusion and contact patterns. The metal connects the p+ runs to a large metal pad and all the n+ runs to a separate large metal pad.

Photoresist Development. The positive photoresist was developed on a different spinner. The wafer was placed on the spinner and vacuum was applied. The spinner was accelerated to 1000 rpm. Developer was applied to the surface of the wafer using a squirt bottle. The developer consisted of a 1:1 mixture of the Shipley 512 developer and

DI water. The developer application was followed by a DI water rinse. The spinner was then accelerated to 5000 rpm and blown dry with N_2. The spinner was then stopped and the wafer was removed and placed in a wire foil lined boat.

Hardbake. The hardbake was done at 120 ±5 °C for 15 minutes to harden the remaining resist. After the hardbake, the wafers were examined under the optical microscope to check the process.

Aluminum Etch. An aluminum etchant was mixed in a 100 milliliter Pyrex beaker and allowed to stand 24 hours before using. The etchant consisted of 400 ml of phosphoric acid, 25 ml of glacial acetic acid, 25 ml of nitric acid, and 50 ml of DI water. The etchant was heated to 45 ±5 °C, and the wafers were etched for 3 minutes. Once the etching was complete, the wafers were removed and rinsed in DI water to the 10 megohm standard. The wafers were then blown dry with N_2 and inspected under the optical microscope for etch completion.

Photoresist Removal. To remove the positive photoresist from the wafers, they were immersed in acetone for 30 minutes. To finish the process, fresh acetone was used, and the wafers were soaked overnight in a covered Pyrex dish to remove any remaining resist. The wafers were then rinsed in DI water to the 10 megohm standard.

Aluminum Anneal. To insure a good ohmic contact between the aluminum and the silicon, the wafers were annealed in a diffusion furnace at 450 °C for 18 minutes in dry N_2. The fabricated wafers were stored in a covered container.

This completes the fabrication process for the BCVJ solar cell. Chapter V discusses the results of the fabrication process.

V. Experimental Results

In this chapter, the results of the fabrication processes are discussed. When possible, scanning electron microscope (SEM) pictures were taken to show the results of a fabrication step or combination of steps. These pictures are presented and discussed. Since the test groove etching results were required to finalize the design, the test groove etching results are given first. The results of the mask fabrication process are discussed next, followed by the results of each of the major BCVJ solar cell fabrication steps. This chapter concludes with an electrical performance evaluation of the fabricated solar cells.

Test Groove Etching Results

The test groove pattern (discussed and shown in Chapter III) was etched into a wafer 300 um thick. The etching procedures were given in Chapter IV. Figure 5-1 shows one complete groove pattern etched into the surface of the test wafer. Figure 5-2a shows the backside of the same wafer. It is observed that the grooves which etched through the wafer were longer than or equal to the theoretical value. The center groove and the top groove in each group were the theoretical lengths. Figure 5-2 verifies that the theoretical groove length was the length required to barely

reach the backside of the wafer. Therefore, these experimental results confirmed the theoretical predictions associated with the groove depth. Also, Figure 5-2b shows that even the smallest width grooves (5 um) etched completely through the wafer. Therefore, the width of the grooves selected for the final design was 5 um. Finally, using equation (41) from Chapter III, the groove length could now be calculated based on the width of the groove and the thickness of the wafer.

Figure 5-1. Surface of a silicon wafer showing the test pattern after etching.

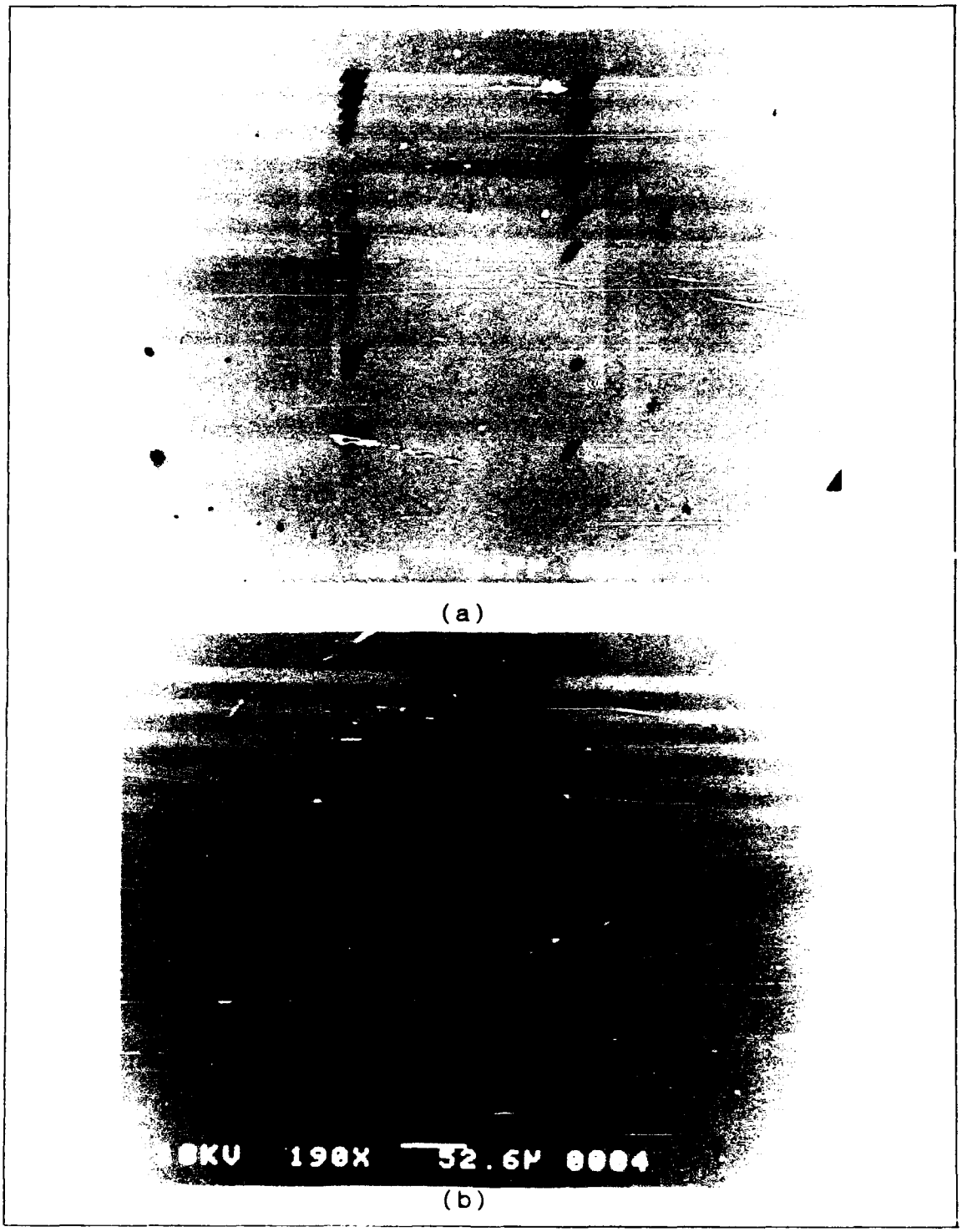


Figure 5-2. Bottom of the silicon wafer showing: (a) Complete pattern of the slits where the grooves etched through the backside, (b) Enlarged view of the slits resulting from the 5 um grooves.

Mask Fabrication Results

Five mask levels were fabricated. The results of each level are described. The five levels are:

1. Groove etch
2. P+ diffusion
3. N+ diffusion
4. Contact etch
5. Metal patterning.

Groove Etch Mask. The groove mask was one of the most critical masks in the fabrication process. Since the mask consisted of 20,000 lines 5 um wide and 20.4 um apart, even small dust particles on either the glass plate or the reticle could seriously effect the orientation dependent etch results. By insuring that the unexposed plate and reticle were blown off with dry nitrogen prior to the step-and-repeat process, the possiblity of achieving a perfect mask was realized. However, the probability of getting a usable mask was still low, even if the reticle is good and no mistakes are made in the step-and-repeat process. By making 5 copies of this mask, a usable mask was obtained. The resolution and focus were excellent. The contrast between the dark and clear areas was also very good. The groove mask is shown in Figure 4-4. An enlarged

view of the groove mask under and optical microscope is shown in Figure 5-3.

In order to achieve these excellent results, the Rubylith must be handled with gloves to keep finger prints off. The fiducial marks on the Rubylith were placed as precisely as equipment tolerances would allow. Focus and high resolution are critical in the step-and-repeat process.

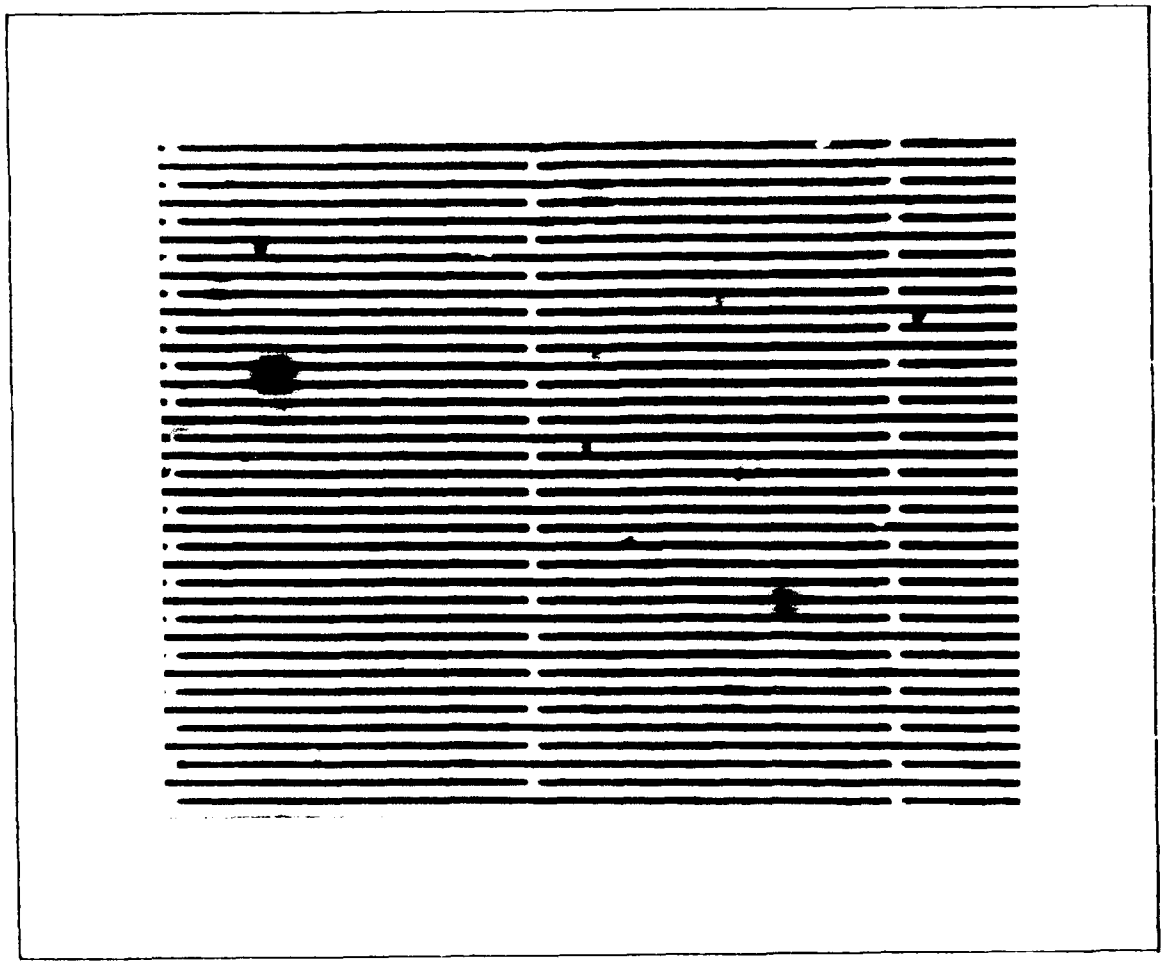


Figure 5-3. Groove mask viewed under an optical microscope (magnification 95x) showing the excellent focus, contrast, and resolution. The groove width is 5 um (0.197 mils).

P+ Diffusion Mask. The p+ diffusion mask is shown in Figure 4-5. Since the lines on this mask were 4 mils (101.6 um) wide, dust was not as serious a problem provided the plates were blown off prior to stepping-and-repeating. The p+ diffusion mask had excellent focus, resolution, and very good contrast. A view of the p+ diffusion mask under the optical microscope is shown in Figure 5-4.

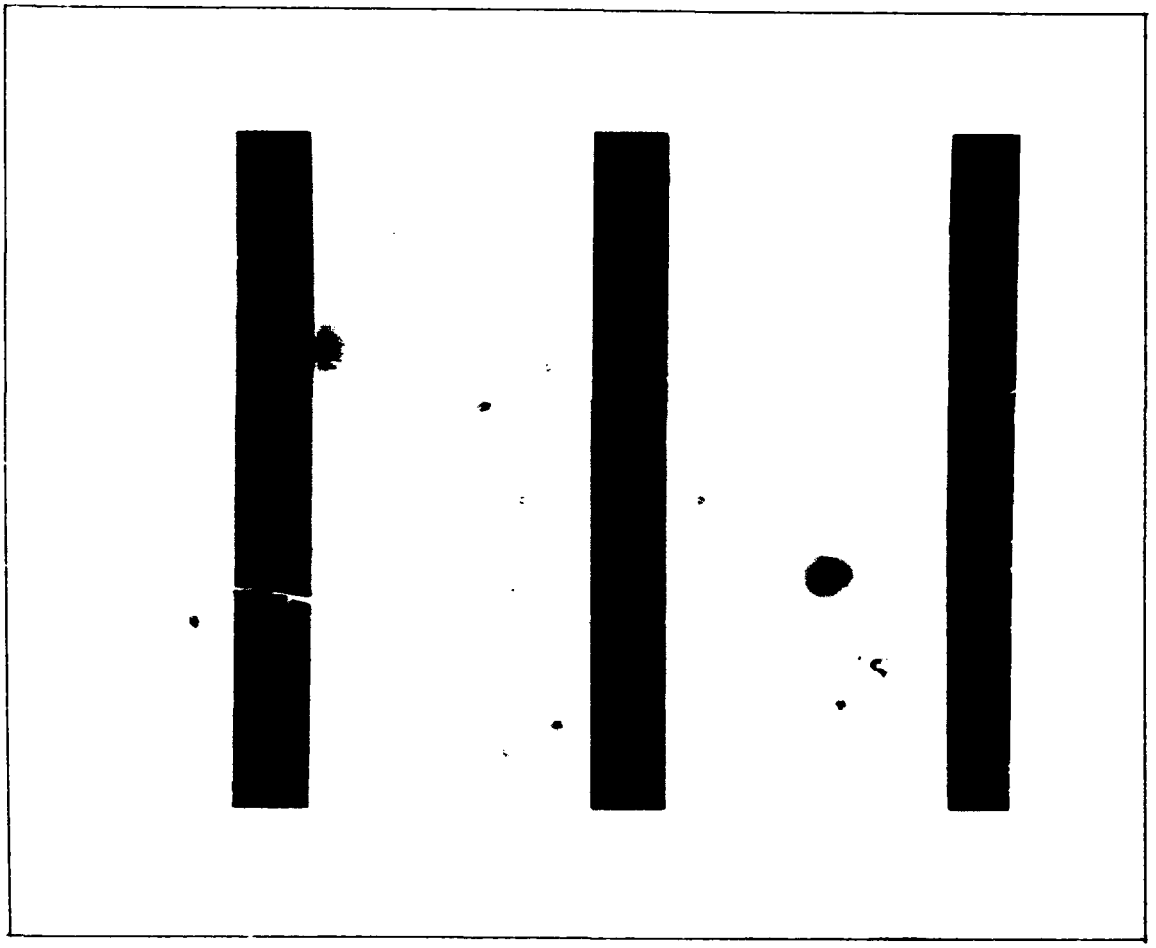


Figure 5-4. P+ diffusion mask viewed under an optical microscope (magnification 187x). The line width is 4 mils (101.5 um).

N+ Diffusion Mask. The n+ diffusion mask is shown in Figure 4-9. The n+ diffusion mask also consisted of 4 mil (101.6 um.) lines. Once again, dust was not a major concern. The n+ diffusion mask had excellent focus and resolution; however, the outside edges of the plate appeared foggy. The patterned area appeared to be acceptable. The contrast was not as good as on the two previous masks. The fogged edges and the lower contrast was a result of the plates being inadvertently exposed to room light by another student. This fact was not known until after the fact. A view of the n+ diffusion mask under the optical microscope is shown in Figure 5-5.

Contact Etch Mask. The contact mask is shown in Figure 4-12. The lines on this mask were 2 mils (50.8 um) wide. Therefore, dust was of greater concern on this mask than on the p+ or n+ diffusion masks. To minimize this potential problem, the unexposed plate was blown off with dry nitrogen. The contact mask was fabricated on the same day as the n+ diffusion mask; therefore, it was fabricated from the same box of HRP plates which had been inadvertently exposed to room light. This caused the clear outside edges of the plate to be foggy. However, the inside patterned area (focus, contrast, and resolution) appeared good so the mask was still used. Figure 5-6 shows the contact mask viewed under the optical microscope.

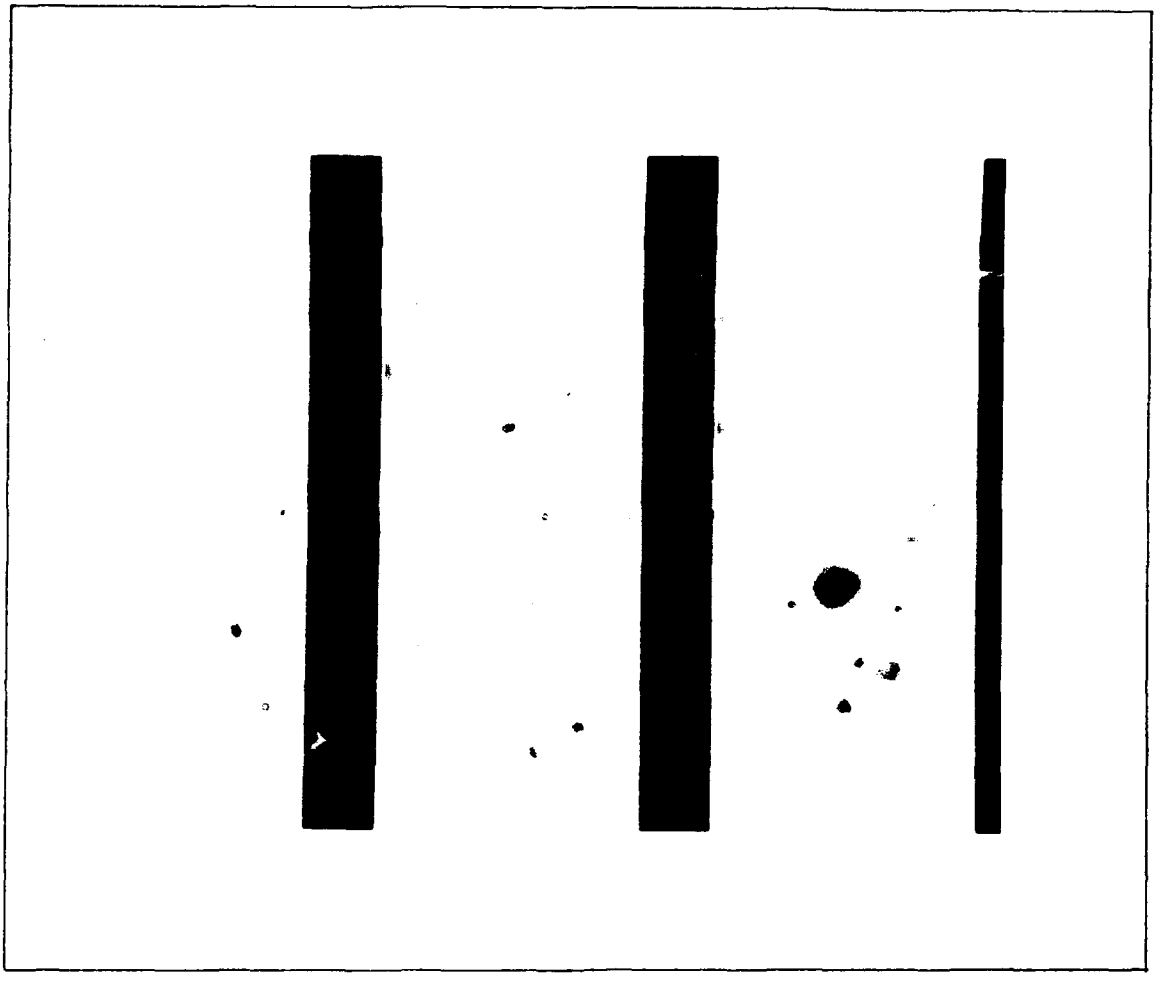


Figure 5-5. N+ diffusion mask viewed under an optical microscope (magnification 187x). The line width is 4 mils (101.5 um).

Metal Patterning Mask. The metal mask is shown in Figure 4-15. The metal mask was the most difficult to step-and-repeat due to the different exposure spacings and number of exposures per row. Also, the pads required another reticle. Since the metal lines were 6 mils (152.4 um) wide, dust was not a serious problem. A fresh box of HRPs was used to print this mask; therefore, the contrast, focus and resolution were excellent. A view of

the metal mask under the optical microscope is shown in Figure 5-7.

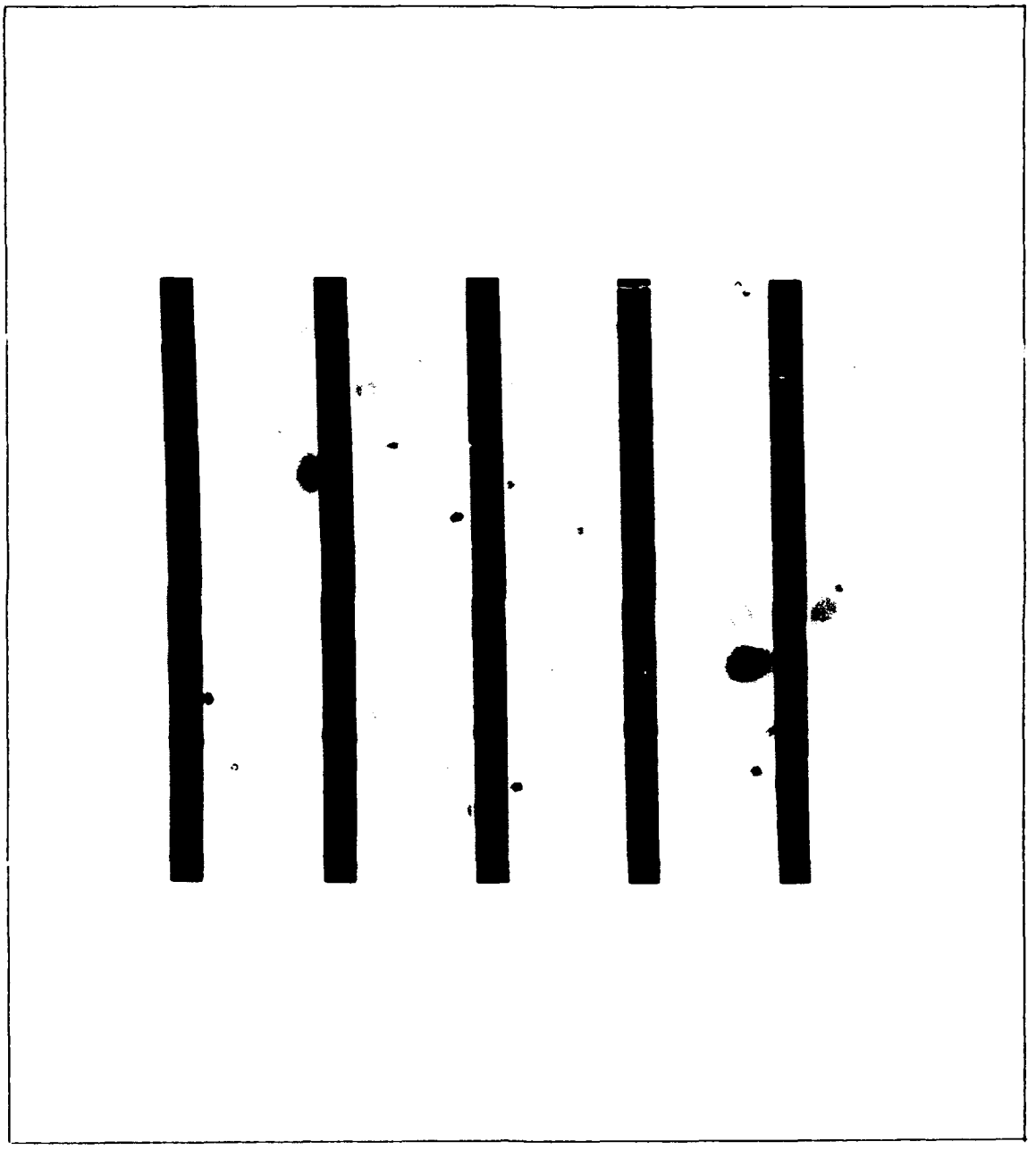


Figure 5-6. Contact mask viewed under an optical microscope (magnification 187x). The line width is 2 mils (50.8 um).

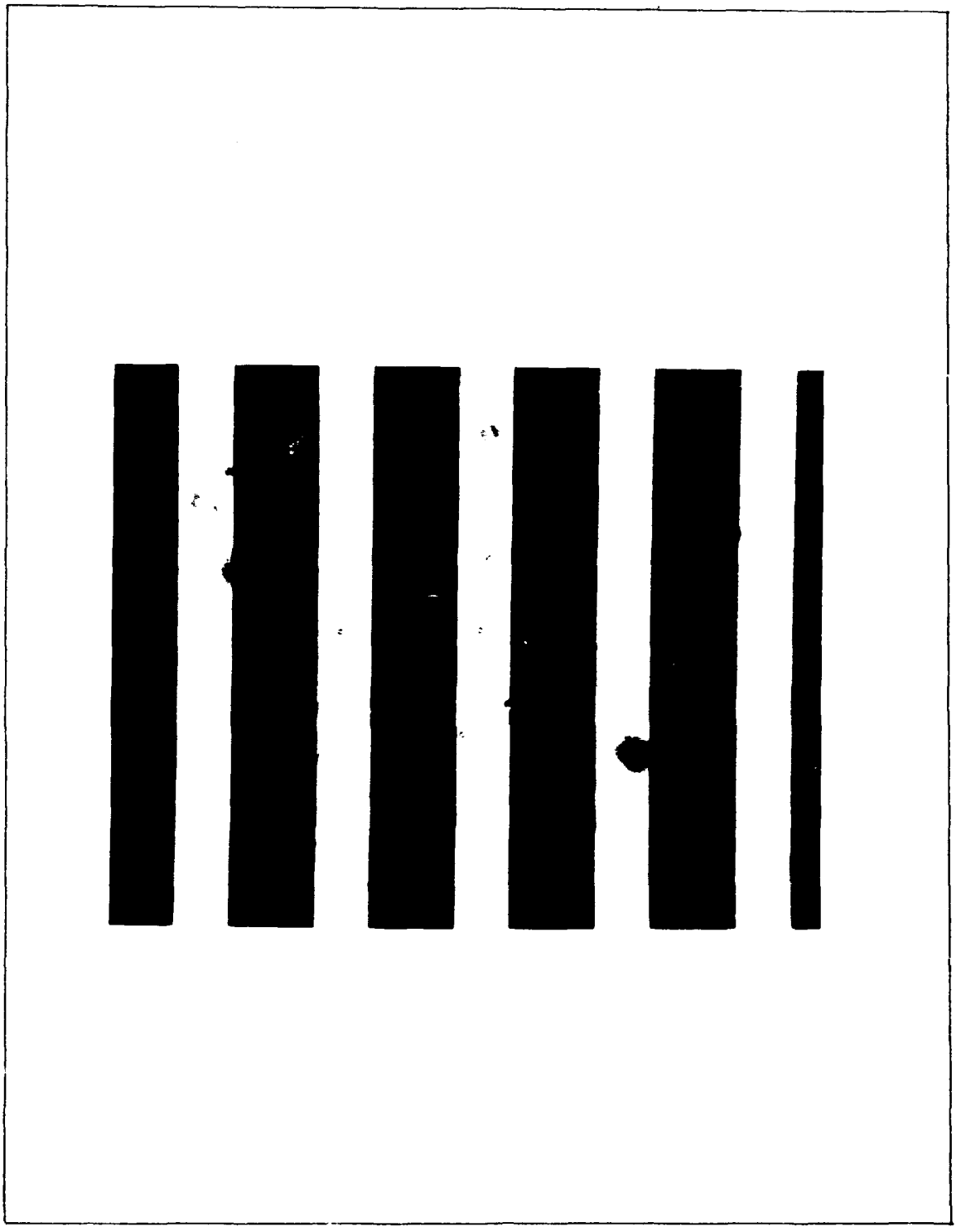


Figure 5-7. Metal mask viewed under an optical microscope (magnification 187x). The line width is 6 mils (152.4 um).

BCVJ Solar Cell Fabrication Results

The results of fabricating the BCVJ solar cell are described in this section. Critical pictures of intermediate results are shown. The results of the fabrication steps are divided into the following categories:

1. Wafer preparation
2. Oxidation
3. Groove photolithography
4. Orientation dependent etching
5. Pointing the groove walls
6. P+ photolithography and diffusion
7. N+ photolithography and diffusion
8. Contact photolithography
9. Metallization and patterning

Wafer Preparation. The wafer preparation included scribing the wafers, ajusting the wafer thickness, and cleaning the wafers. Scribing the wafers just above the flat, made identifying and keeping track of the various wafers easy. (Identifying the Ametek wafers with an A and the Virginia Semiconductor wafers with a V made it easy to tell the difference between the two.) Since the Ametek wafers had the primary flat cut perpendicular to the (1$\bar{1}$1) plane and the Virginia Semiconductor (VS) wafers had the flat cut parallel to the (1$\bar{1}$1) plane, discriminating the

difference was especially critical when the wafers were aligned in the mask aligner. Scribing the wafers with a diamond scribe is readily accomplished without breaking or chipping the wafer. Scribing the wafer just above the wafer flat sometimes interferred with the cell closest to the flat. The scribe marks can be seen in Figure 4-1 which shows a picture of completed wafer. Therefore, the best place to scribe the wafer is 45 degrees to the left or right of the flat.

Adjusting the wafers to a specific thickness was done by swirling the wafer in a circular motion while immersed in a chemical etchant composed of $HF:HNO_3:CH_3COOH$ (2:15:5). If the wafers were not swirled, the surface appeared streaked. This was probably due to the streams of bubbles produced by the chemical reaction between the etchant and the silicon. Ultrasonic agitation also resulted in uneven removal of the silicon. This was apparent by the blurry appearance of reflections observed on the silicon surface. Although the swirling procedure resulted in a smooth polished surface, the wafer was thicker in the center than on the edge. Since the VS wafers required little or no thinning, these wafers had a more uniform thickness. The etch rate of the silicon also decreased as the etchant was expended. The etch rate of fresh etchant was approximately 5 um per minute. The decrease in the etch rate was less than 1 um/minute per

wafer and depended on how long the previous wafer was etched.

Elliott's cleaning process [26:51] was very effective in removing both organic and inorganic contaminates. This was apparent by the fact that when the wafers were rinsed in DI water, a 10-12 megohm standard was readily achieved.

Oxidation. The oxidation at 900 °C for 33 hours in steam produced a 2.35 um oxide thickness which was thick enough to withstand the ODE process and still leave an oxide thick enough to mask against the phosphorus or boron diffusion. The oxide thickness was determined by etching a pattern of 4 mil (101.6 um) wide lines into the oxide and then measuring the thickness with the Dektak stylus profilometer. The strip-chart recording is shown in Figure 5-8. The oxide was uniformly thick across the surface and had a silver appearance resembling unoxidized wafers.

Problems with the oxidation were encountered when the smaller laboratory furnace was used. The wafers barely cleared the top of the furnace. Once the wafers were in the furnace, they evidently expanded just enough to touch the top causing some of them to become wedged in the oven. Therefore, the larger furnace tube should be used. The disadvantage of the larger furnace tube is that a larger volume of steam is required to keep the furnace saturated

with wet oxygen. This meant that the bubbler had to be refilled with DI water every 4 hours.

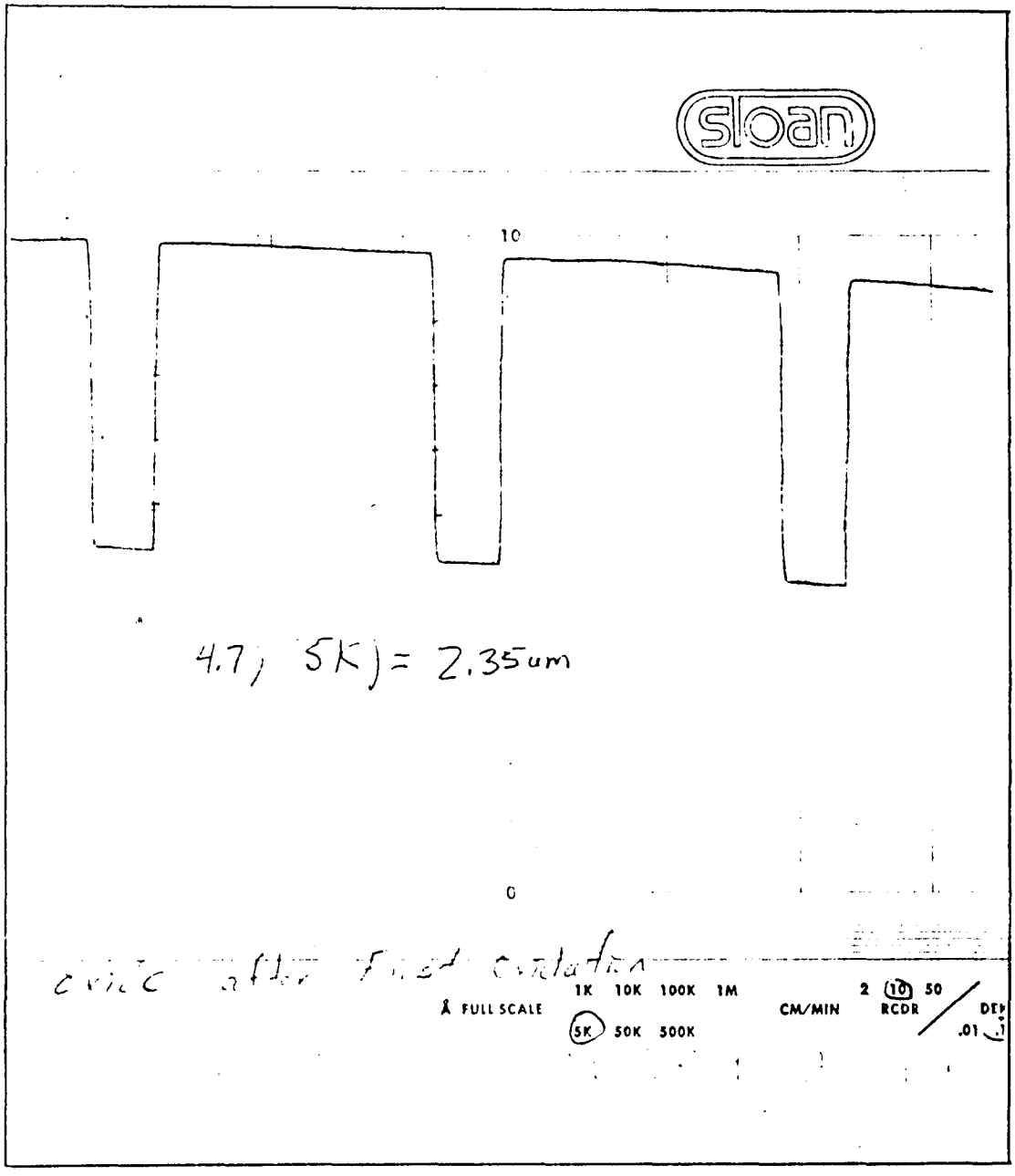


Figure 5-8. Dektak strip-chart recording showing thickness of the initial oxide.

Groove Photolithography. The groove photolithography process results were very good. Lines 5 um wide with excellent resolution were achieved. The greatest concern during the groove photolithography was dust. Dust on the groove mask or wafer could result in a large hole after the ODE was completed. Figure 5-9 shows the result of dust. Therefore, blowing off the mask and wafers during critical processing steps with dry nitrogen was

Figure 5-9. Result of dust on the wafer or groove mask during groove photolitography causes holes in the wafer after orientation dependent etching.

accomplished. Also, the coated wafers were softbaked in a covered boat to keep dust off the surface.

Another problem is ensuring that the mask is properly aligned with the wafer flat. An error of as little as 0.5 degrees can result in the grooves becoming to wide, which can result in the the groove walls being etched away. Figure 5-10 shows the result of misalignment following the ODE. As can be seen from this SFM photograph, the walls have almost completely etched away.

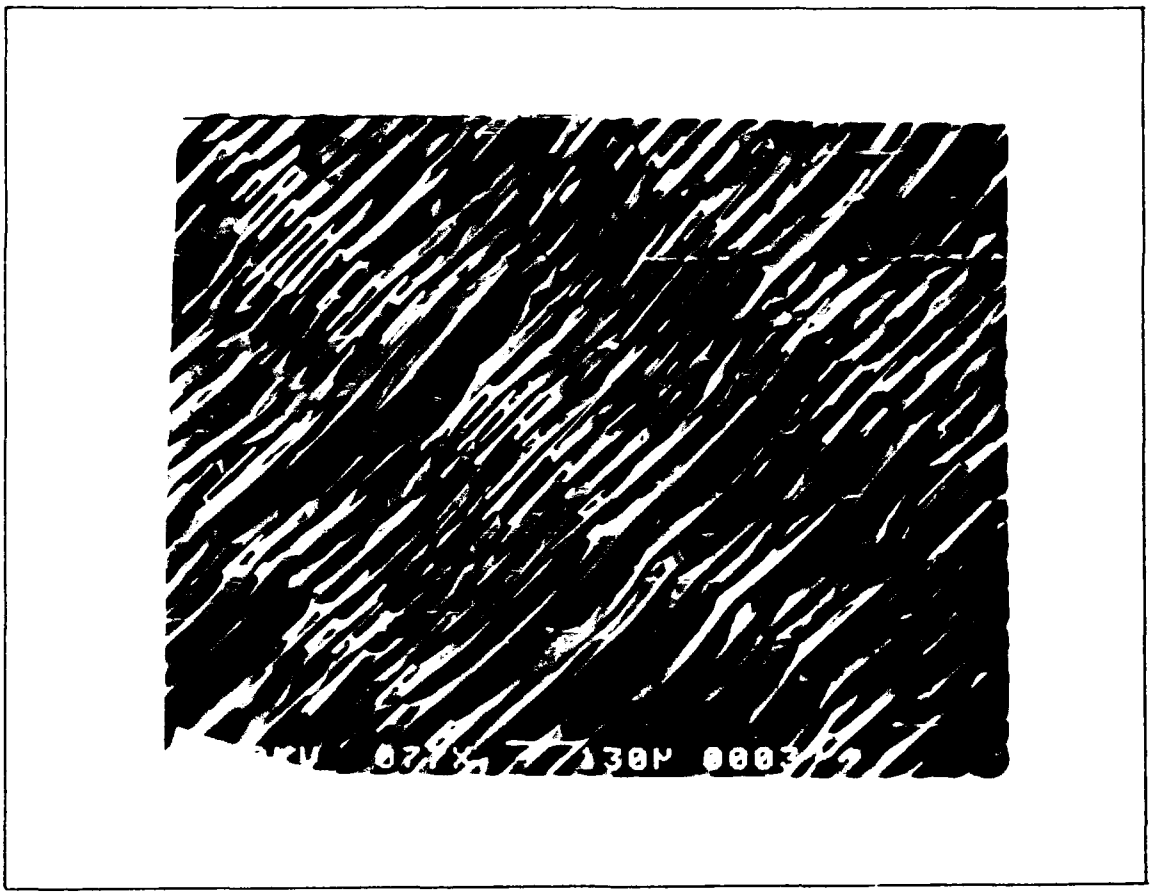


Figure 5-10. Result of the grooves being misaligned with the wafer flat. The groove walls etch away.

The method of placing a piece of lens tissue between the wafer and chuck of the spinner was instrumental in preventing the patterned grooves from being scratched while coating the opposite side. Also, by developing the negative resist by immersion rather than with the spin developer, the positive photoresist on the backside seemed to adhere better. This was due to a film left on the backside where the wafer touched the chuck. Therefore, the positive photoresist did not adhere well to this film. The immersion developing procedure also resulted in better resolution which was extremely important in this step.

Figures 5-11 through 5-14 show the result of the groove photolithography step following the oxide etch step. From Figure 5-14, the under-etching appears to be about half the width of a groove which would be 2.5 um. This is reasonably close to the oxide thickness of 2.35 um. The 6:1 buffered HF etch required approximately 23 minutes to etch through the oxide. Therefore, the oxide etch rate was approximately 1 um per minute.

Orientation Dependent Etching (ODE). The results of the ODE showed that 5 um wide grooves could be etched 290 um deep (provided the grooves were properly aligned with the wafer's flat). The grooves had vertically etched side walls, and the end walls etched at a 30 degree angle with respect to the wafer's surface. Figure 5-15 shows a SEM

picture of a top view of the grooves after ODE with the oxide removed. Figure 5-16 shows a SEM photograph of the groove ends at a tilt.

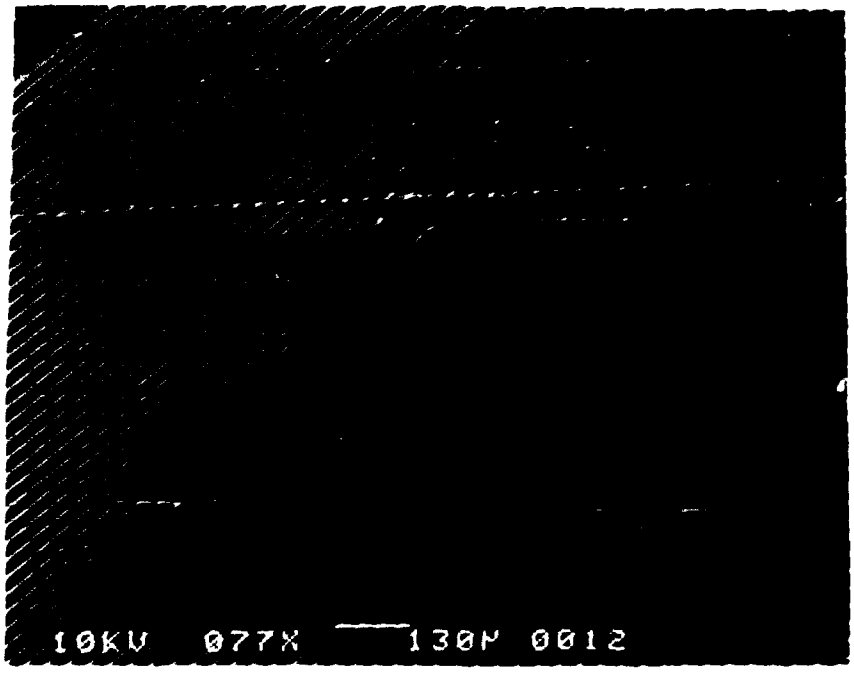


Figure 5-11. Result of the groove photolithography (magnification 77x).

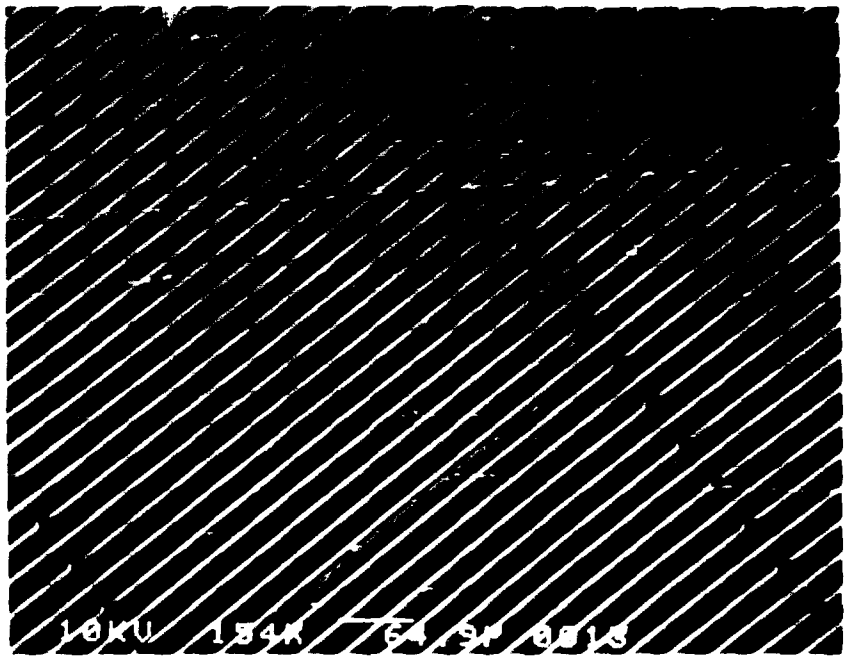


Figure 5-12. Result of the groove photolithography (magnification 154x).

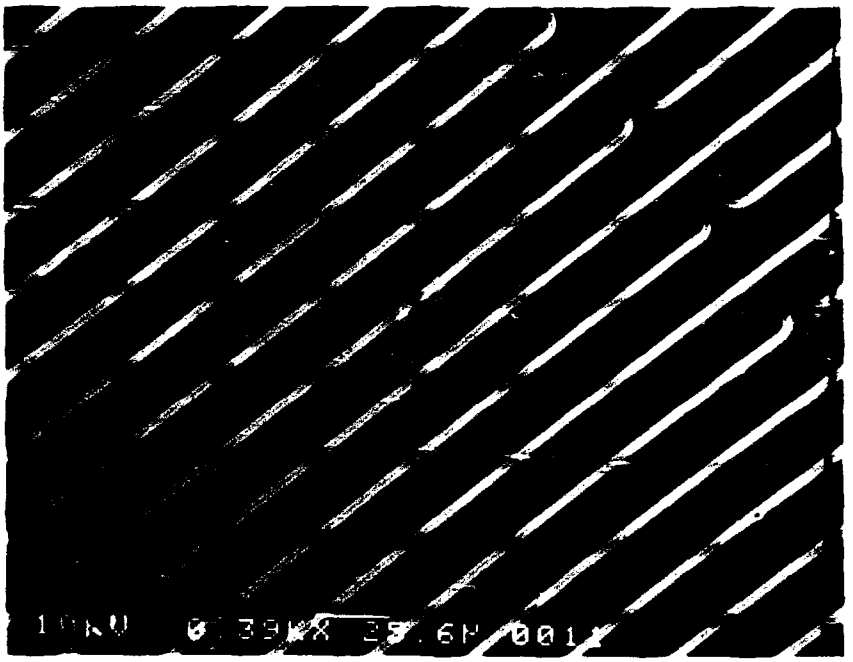


Figure 5-13. Result of the groove photolithography (magnification 390x).

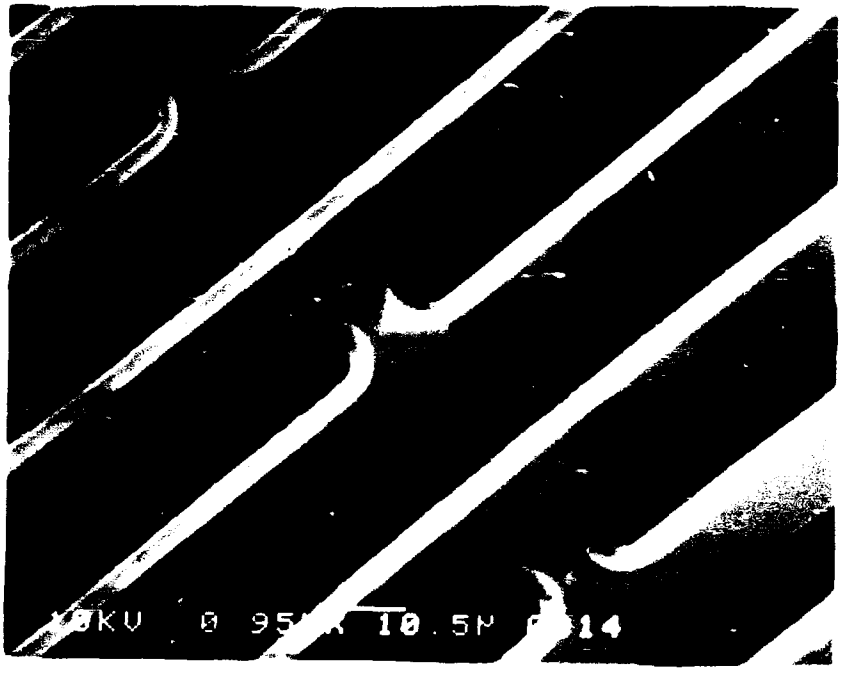


Figure 5-14. Result of the groove photolithography (magnification 950x).

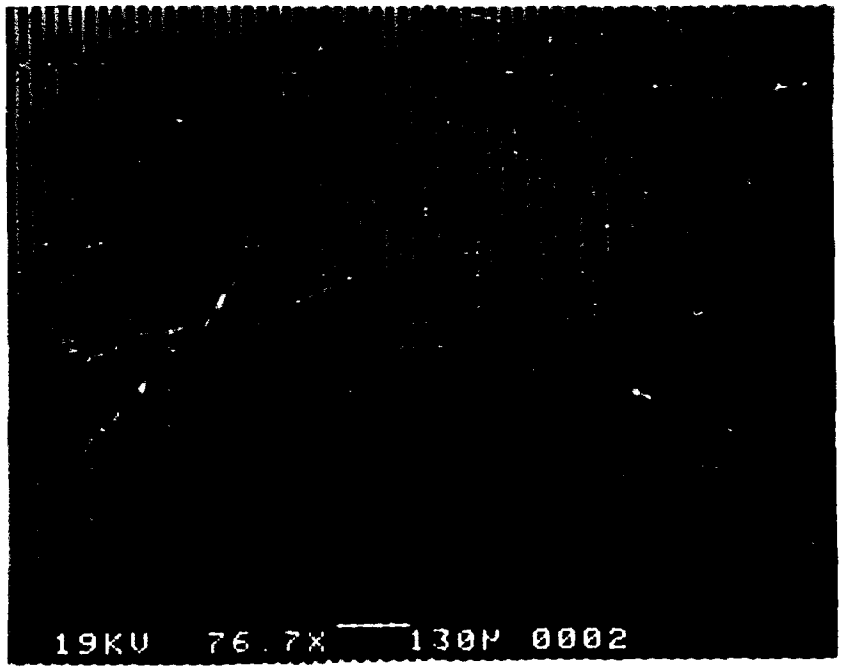


Figure 5-15. Top view of the grooves after orientation dependent etching and the oxide removed.

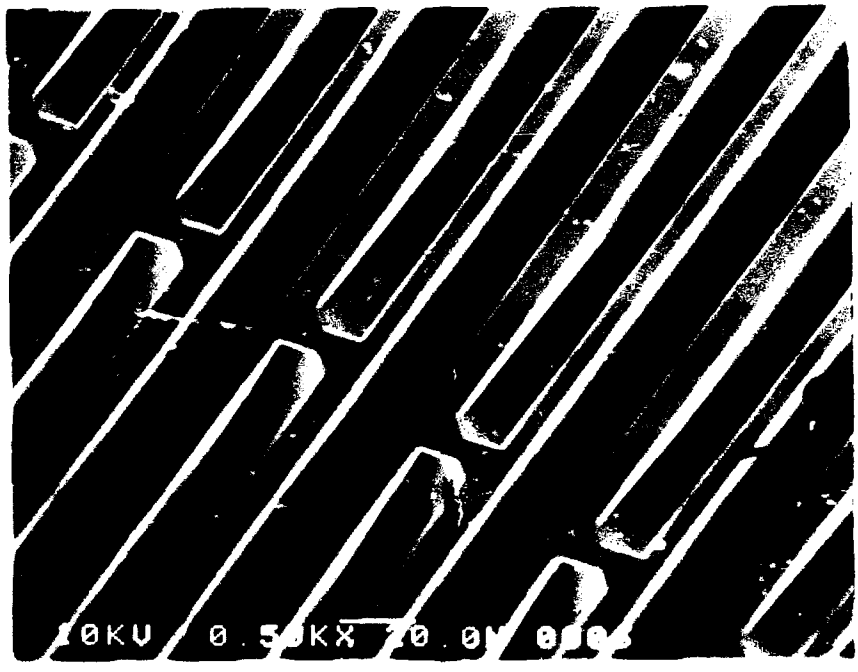


Figure 5-16. Top view of the grooves (tilted) after orientation dependent etching and the oxide removed.

If the thickness of the wafer was exactly 290 um, the groove length 1000 um, and the groove width 5 um, then equation 41 in Chapter 3 was satisfied, and the groove barely etched to the backside of the wafer. Figure 5-17 shows the backside of the wafer. In this instance, the grooves and the backside of the wafer can both be seen at the same time. A small slit forms on the backside of the

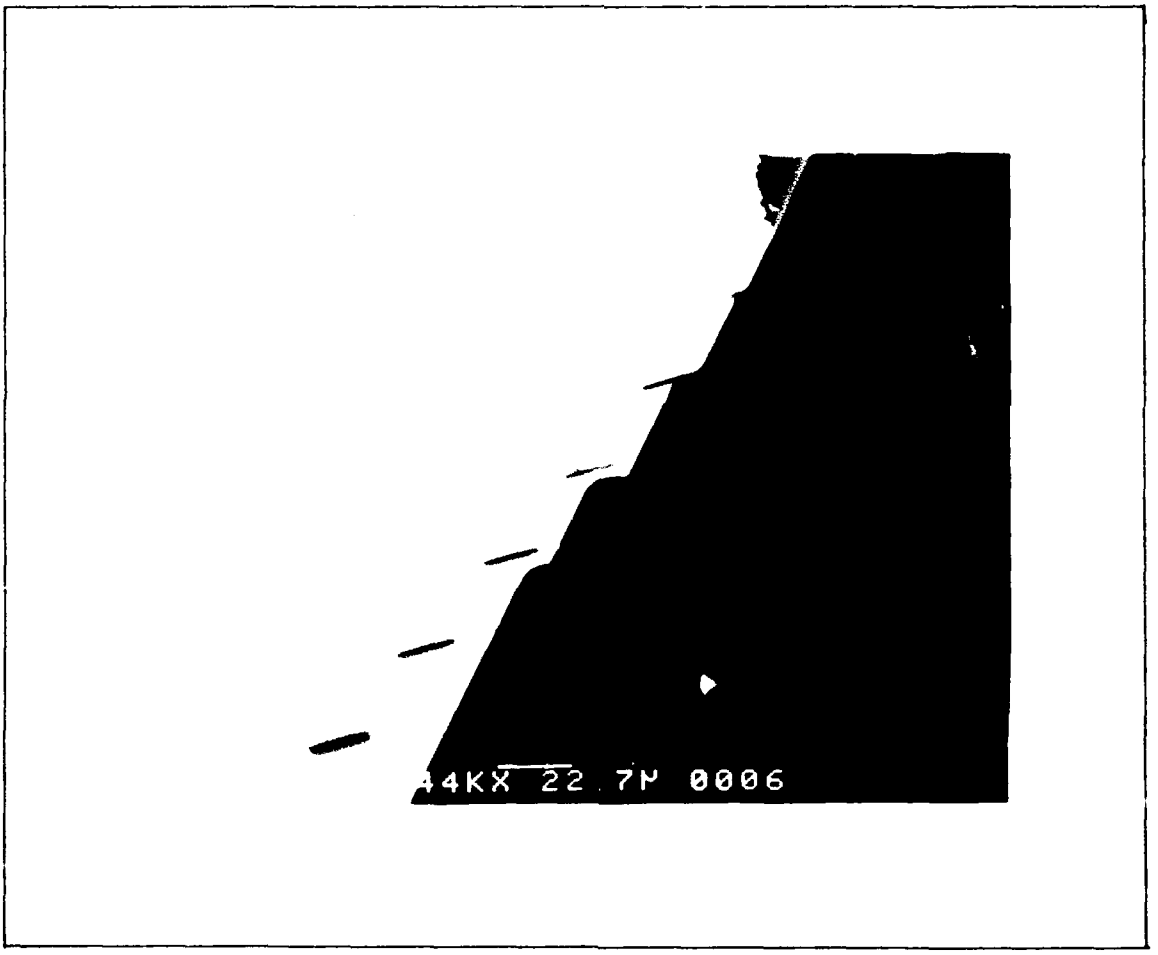


Figure 5-17. Cross-sectional view showing the side and back of a wafer. A small slit occurs where the groove reaches the backside.

wafer where the groove end walls intersect. At this point, all the walls of the groove are {111} planes and etching essentially ceases. Figure 5-18 shows a similar picture from the topside. On the Ametek wafers, the slits on the backside were larger the further they were from the center. This result occurred because these wafers were thinner on their edge compared to the center.

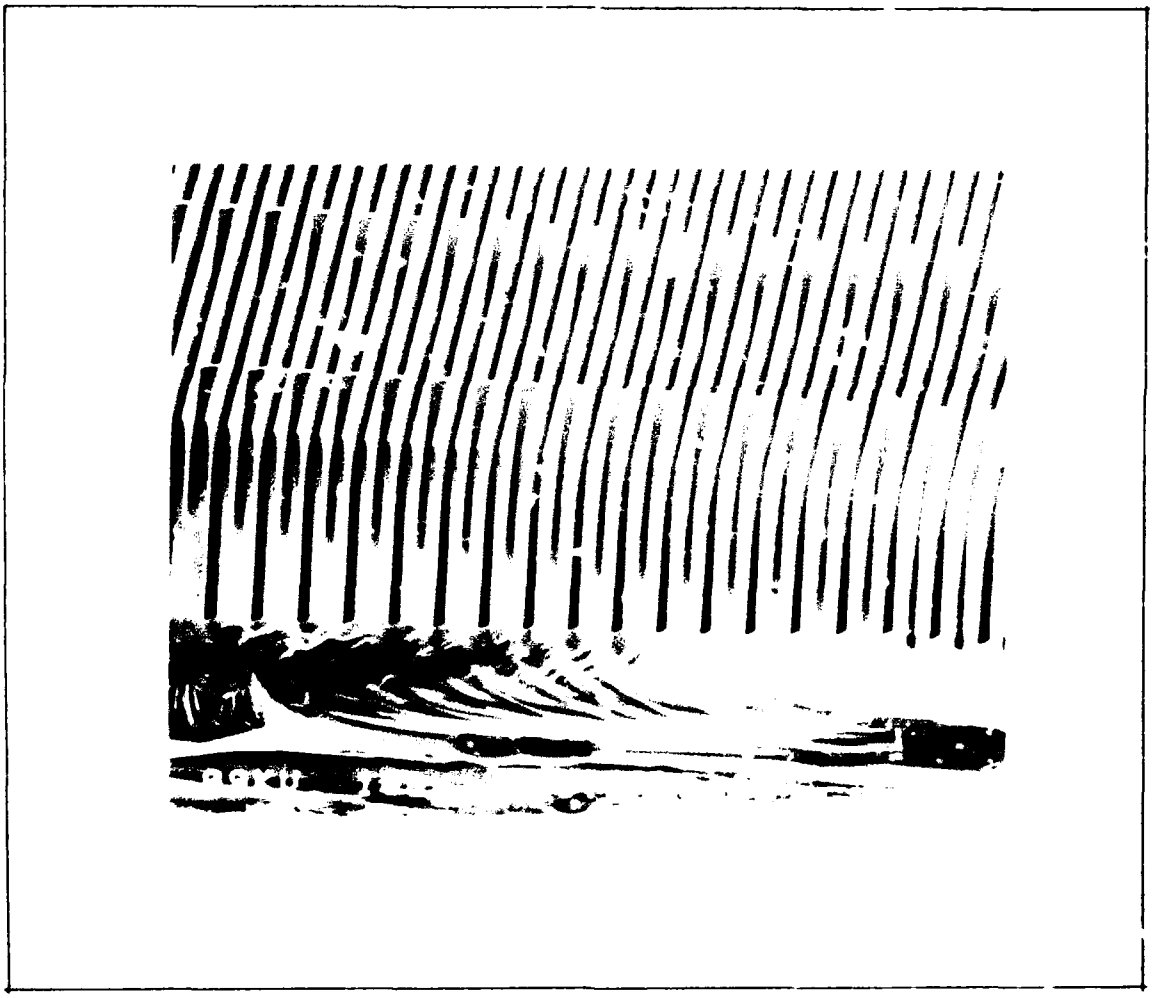


Figure 5-18. Cross-sectional view showing the side and top of an etched wafer.

The wafers were etched in a 50 percent by weight solution of potassium hydroxide (KOH) and DI water at 85 °C for 180 minutes. Etching longer than 180 minutes is not a serious problem, since the etching of silicon is very slow once the {111} planes intersect on the backside. However, etching longer than necessary should be avoided, since the oxide thickness decreases, and the oxide is needed as a mask in the diffusion steps. Also, the walls can begin to slowly etch away and thus weaken the structure.

The concentration of the etchant resulted in good uniformity of groove depths and smooth walls as predicted in [27:113]. The etch rate was approximately (290 um/180 =) 1.6 um per minute. According to Figure 4-28, the etch rate at 85°C and 50 percent KOH is approximately 1.3 um. Lower KOH concentrations were not tried due to the excellent results using 50 percent by weight of KOH and water.

The oxide thickness on the wafers was measured after the ODE by etching runs 4 mils (101.6 um) wide into the oxide. The oxide thickness was measured to be 0.93 um using the Dektak stylus profilometer. Figure 5-19 shows the strip-chart recording of the measurement. Therefore, the amount of oxide removed during the ODE was (2.35 - 0.93 =) 1.42 um. Thus, the oxide etch rate was (1.42 um/180 min =) 0.0079 um per minute, and according to Figure 4-22a, the oxide etch rate should be about 0.006 um per minute.

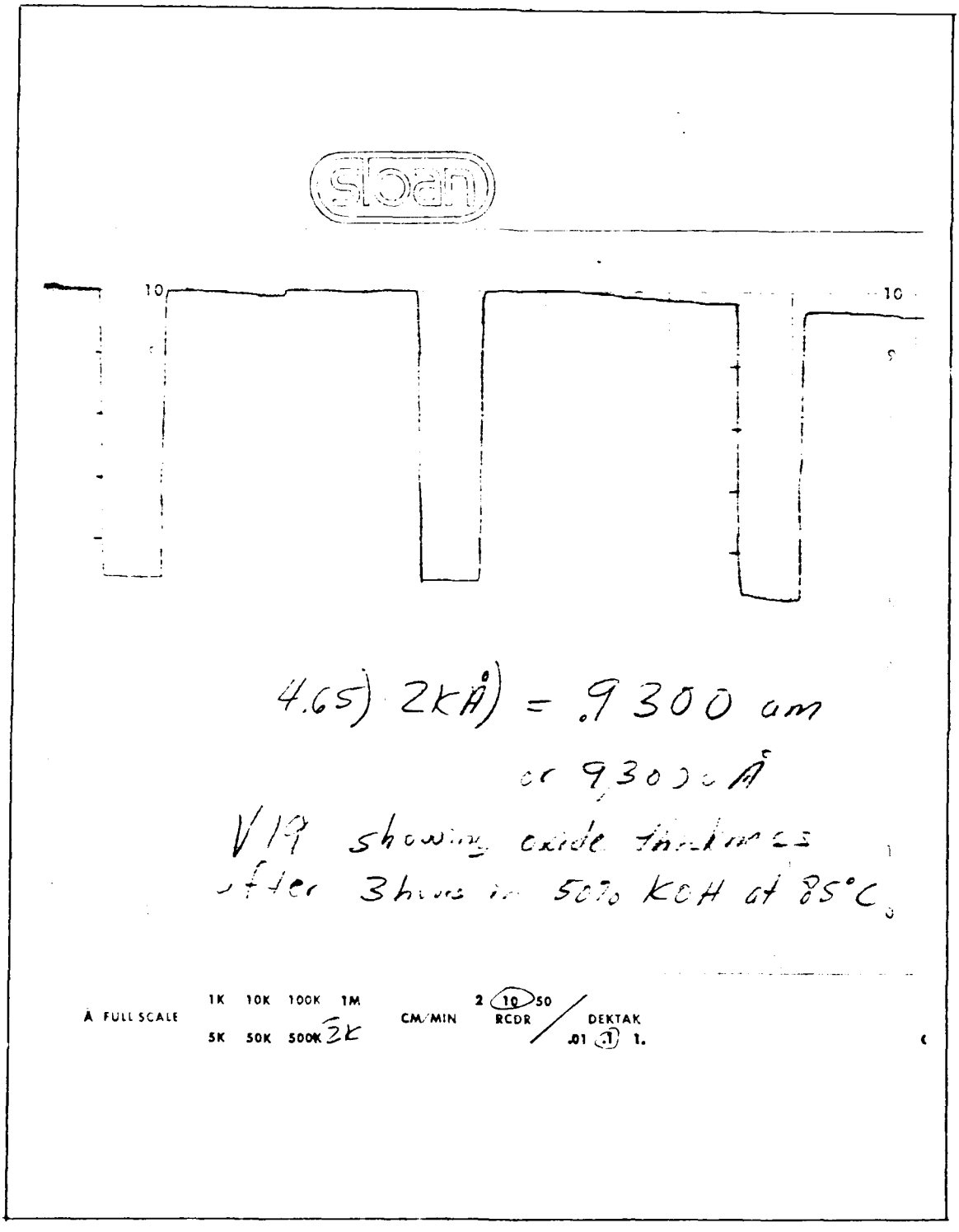


Figure 5-19. Dektak strip-chart recording showing the thickness of the oxide after the orientation dependent etching.

Pointing the Groove Walls. The walls of the grooves can be isotropically etched to produce sharp points at the top of the walls. The advantage of pointing the grooves is to decrease the reflection of light from the top of the walls. The etchant was composed of $HF:HNO_3:CH_3OOH$ in the ratio 2:15:5 [31:522]. A 5-6 minute immersion in the etchant is sufficient to point the grooves. Figure 5-20 shows a SEM photograph of the result following the isotropic

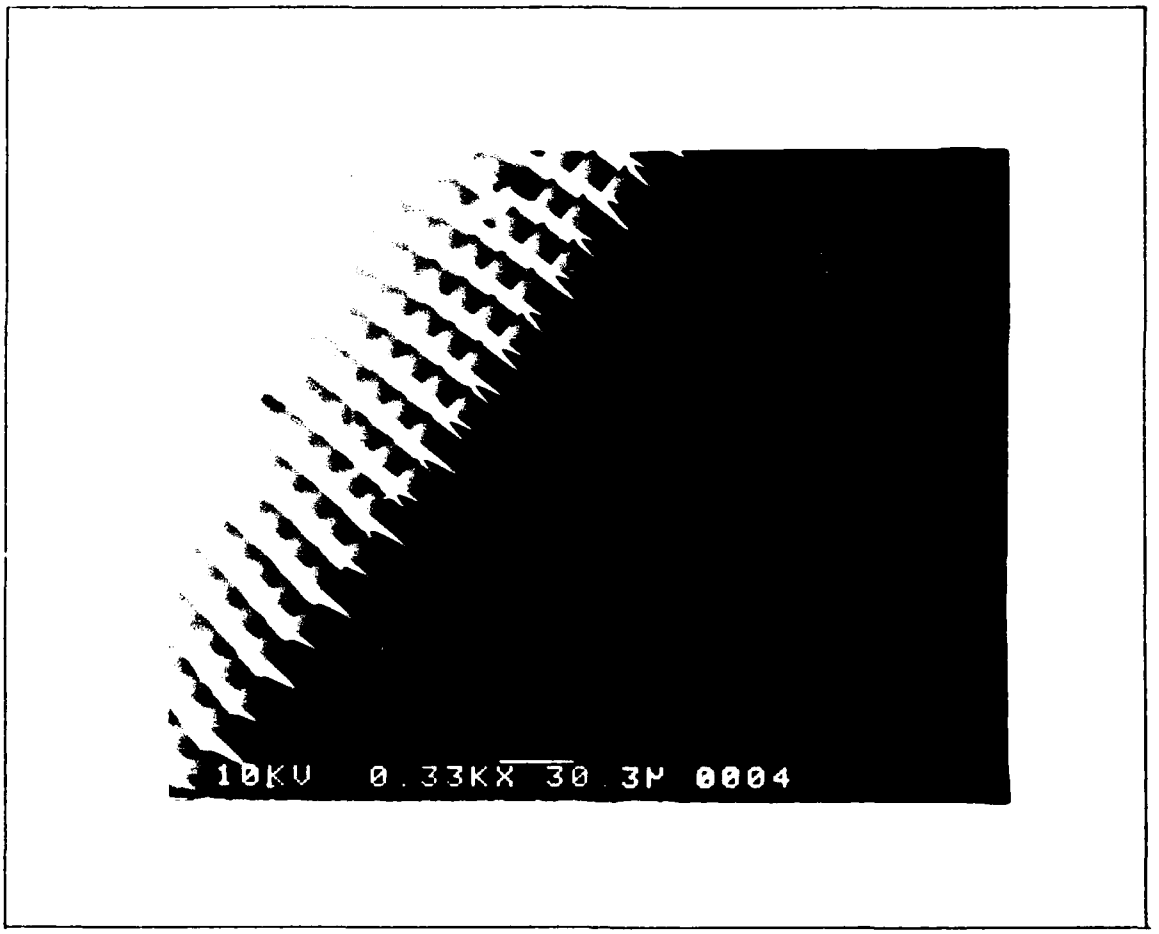


Figure 5-20. Cross-sectional view showing the side and top of a wafer after pointing the grooves.

etch. Figure 5-21 shows one of the pointed groove walls magnified 3600 times. Even at this high magnification, the tip of the point is still quite sharp.

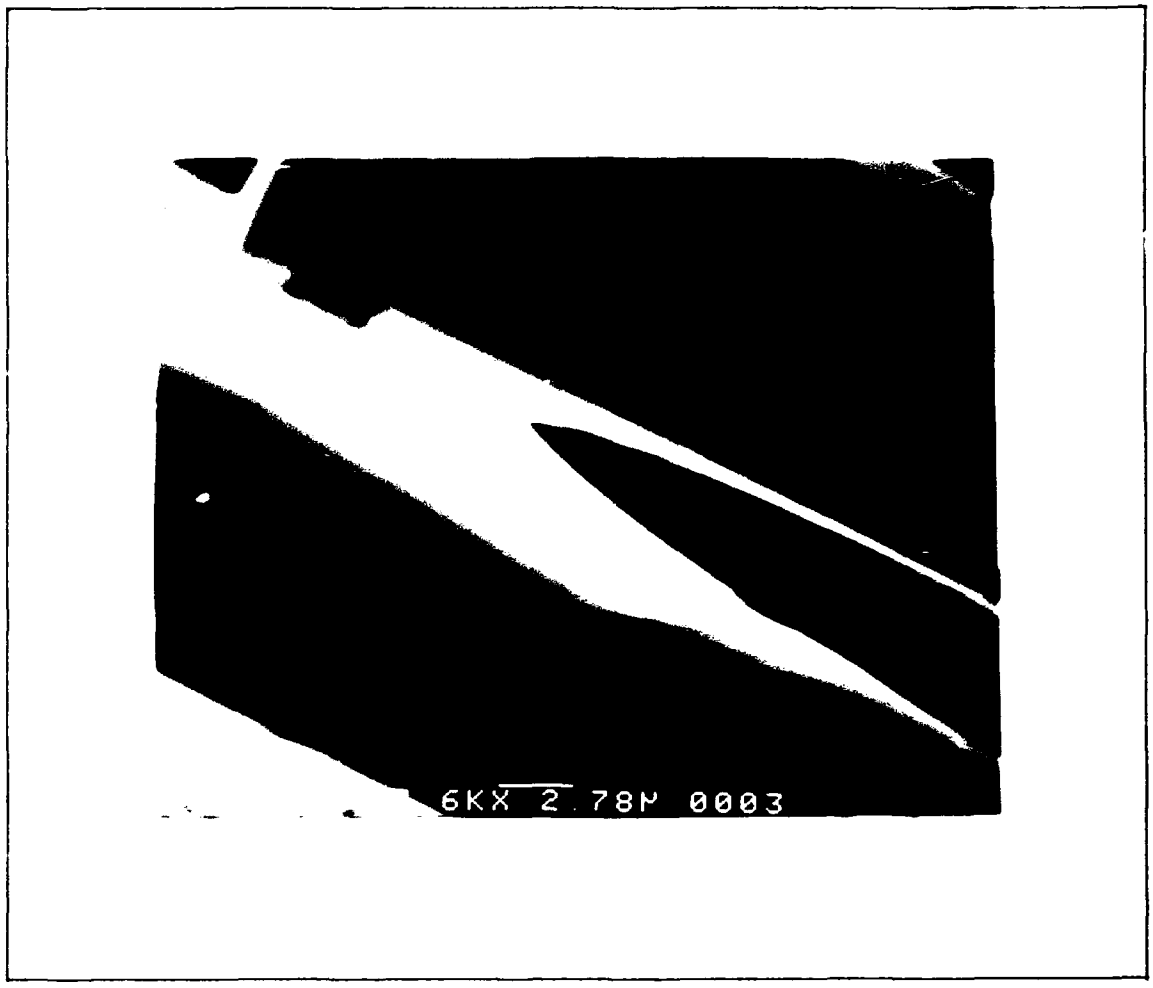


Figure 5-21. Cross-sectional view showing the side and top of a groove wall after pointing.

The major problem associated with pointing the grooves was protecting the backside from the etchant. Both positive and negative resists were tried, but, neither could tolerate

the etchant. Therefore, this step was not included in the final fabrication of the BCVJ solar cell.

P+ Photolithography and Diffusion. The results of the p+ photolithography are shown in Figure 5-22. A magnified view is seen in Figure 5-23. The alignment of the p+ runs between the slits was excellent, and very few defects were noted.

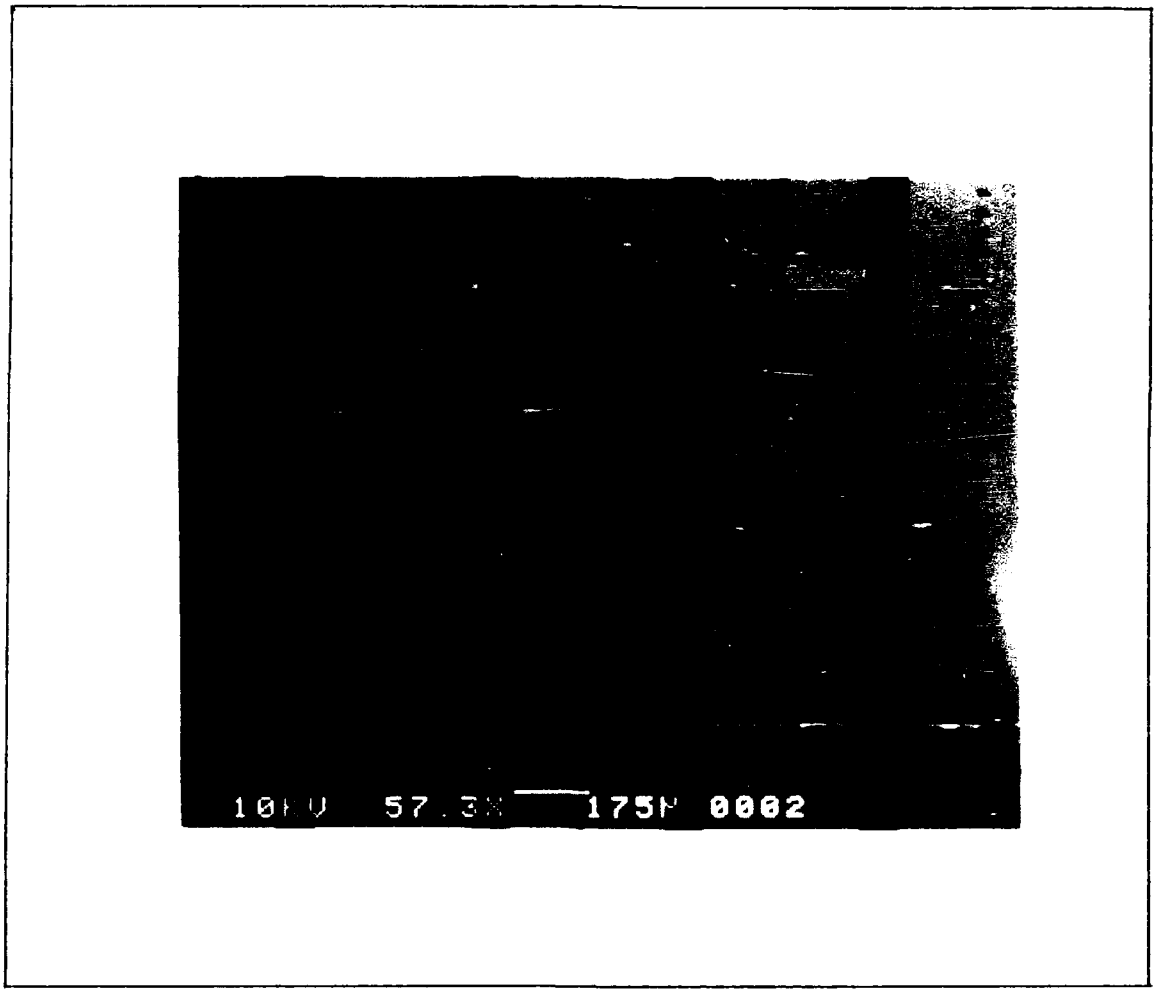


Figure 5-22. Results of the p+ photolitography showing the alignment between the slits.

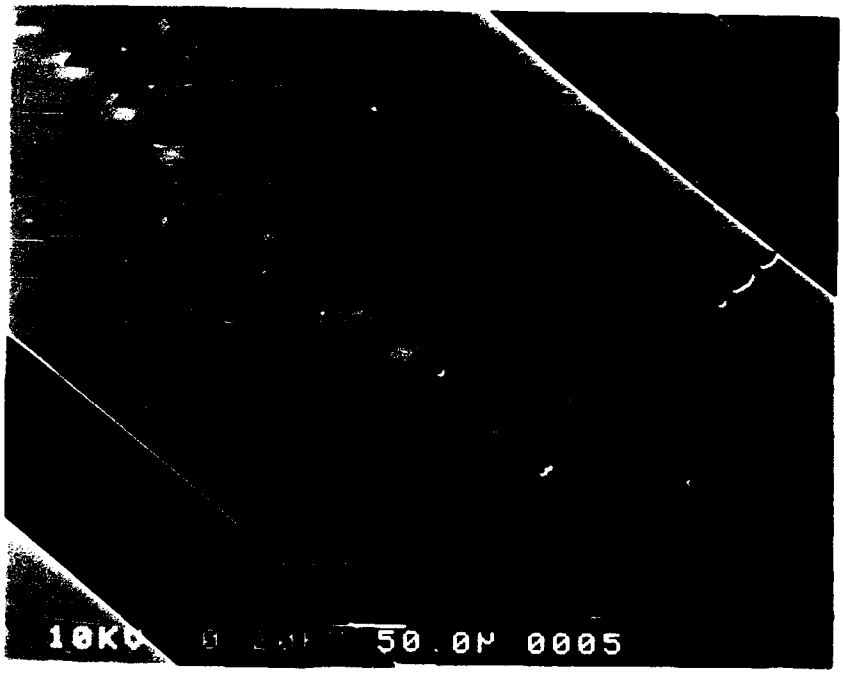


Figure 5-23. Enlarged view showing the slits positioned midway beiween the p+ runs.

One problem encountered with patterning a wafer results when the photoresist flows through the slits when vacuum is applied to the spinner's chuck. The effect of this result is shown in Figure 5-24. In order to prevent this problem, the wafer was completely covered with resist and spun immediately after the vacuum was applied. The problem of the resist being pulled through the slits occured just on

wafers where the slits were extremely large. If the slits are small, the oxide actually remains over the slit, as can be seen by close examination of Figure 5-17. The wafer shown in Figure 5-24 had the oxide removed from the slits as a result of being used in the groove pointing process.

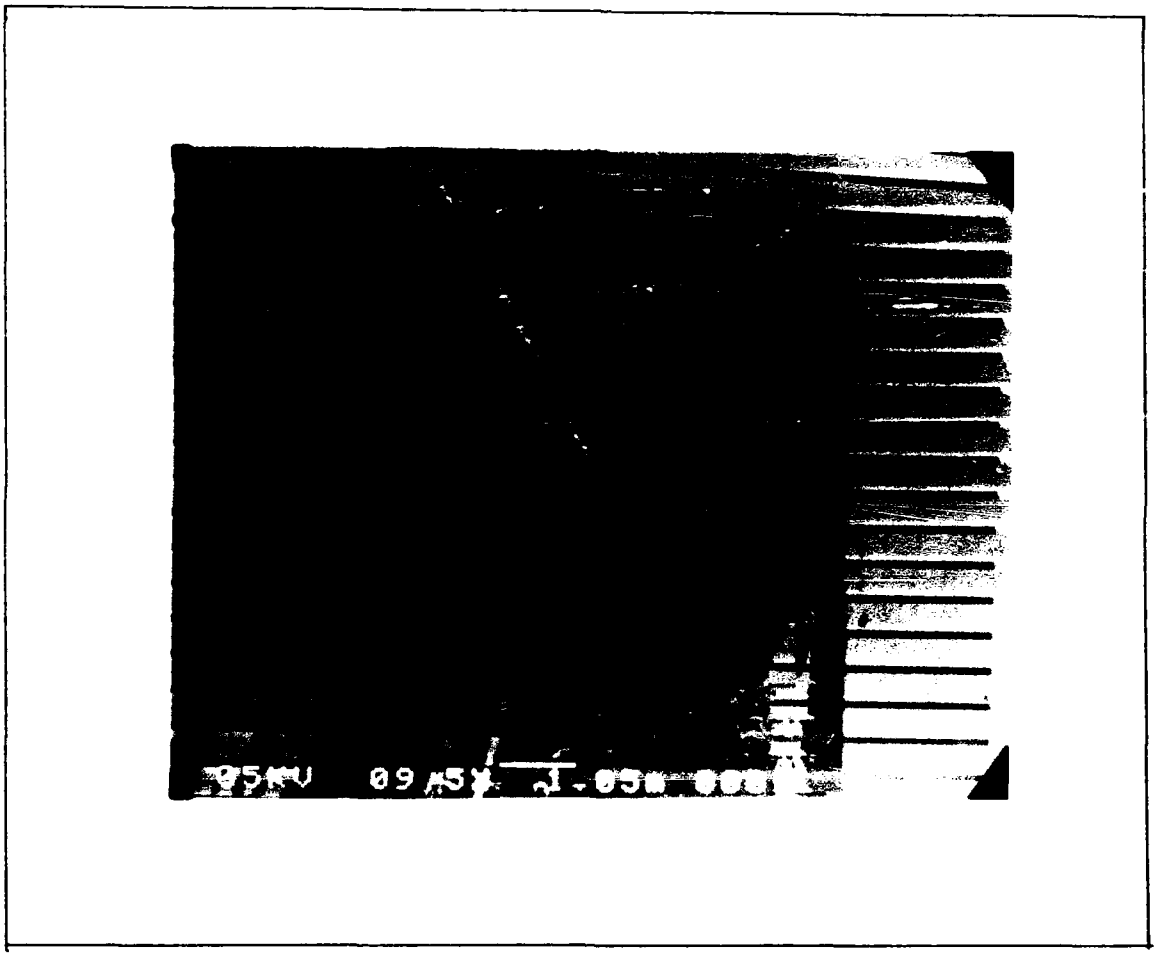


Figure 5-24. Poor p+ photolithography as a result of holes in the wafer and the lack of oxide covering the slits.

One of the major concerns in the fabrication process was whether the groove structure would shatter during high

temperature diffusion. However, this was not a problem. Figure 5-25 shows the grooves following the p+ diffusion and drive-in. Figure 5-26 shows an enlarged view of the groove ends. Small oxide particles remained on the top of the grooves as a result of photoresist being pulled through the slits. Figure 5-27 shows the backside of the wafer following the boron deposition. Once again, no cracks or breakage due to thermal stress was observed.

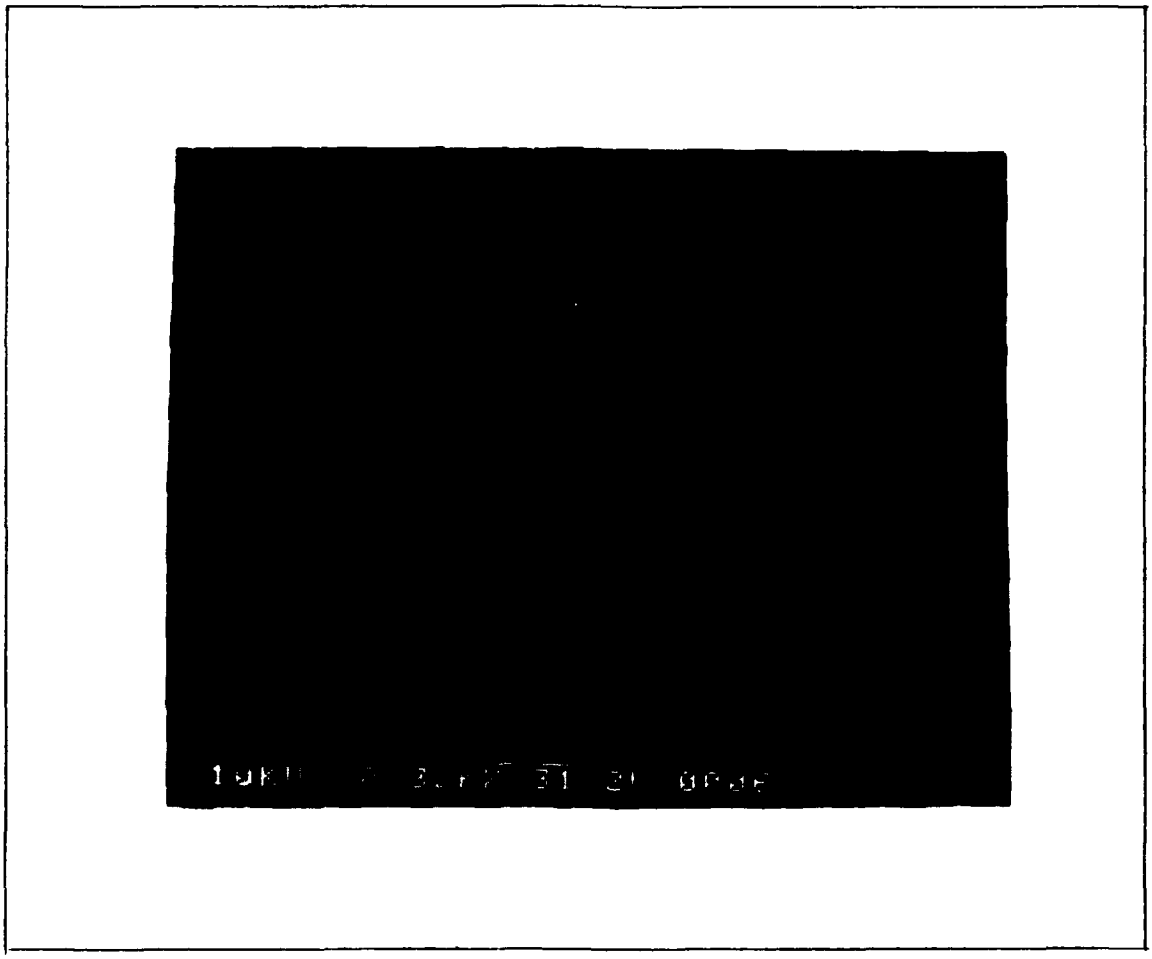


Figure 5-25. Grooves following diffusion at 900°C. No breakage is observed.

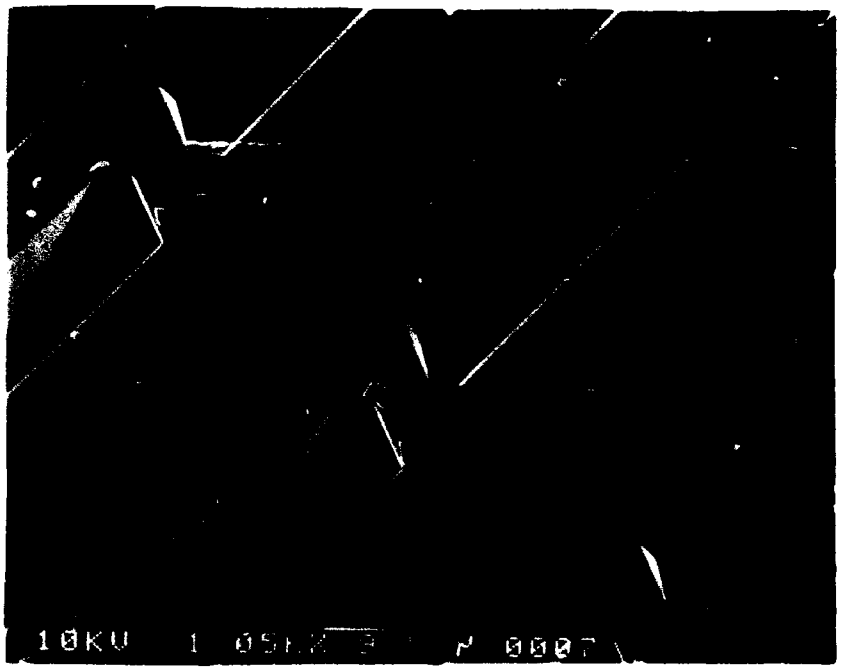


Figure 5-26. Close-up view of grooves following diffusion at 900°C.

A test wafer was doped during the boron deposition, and the sheet resistivity of the wafer was checked using the Veeco AP-150 automatic resistivity probe. The sheet resistivity of a test wafer was 44.57 ohms per square with a standard deviation of 1.54% before boiling in HNO_3. After boiling in HNO_3, the sheet resistivity measured to be 44.55 ohms per square with a standard deviation of 1.44%. The

resistivity of a virgin wafer was also checked using the Veeco AP-150 automatic resistivity probe and measured 100.4 ohms per square with a standard deviation of 2.00%. These measurements demonstrated that the test wafer was doped, since the sheet resistivity was lower in the test wafer compared to the virgin wafer.

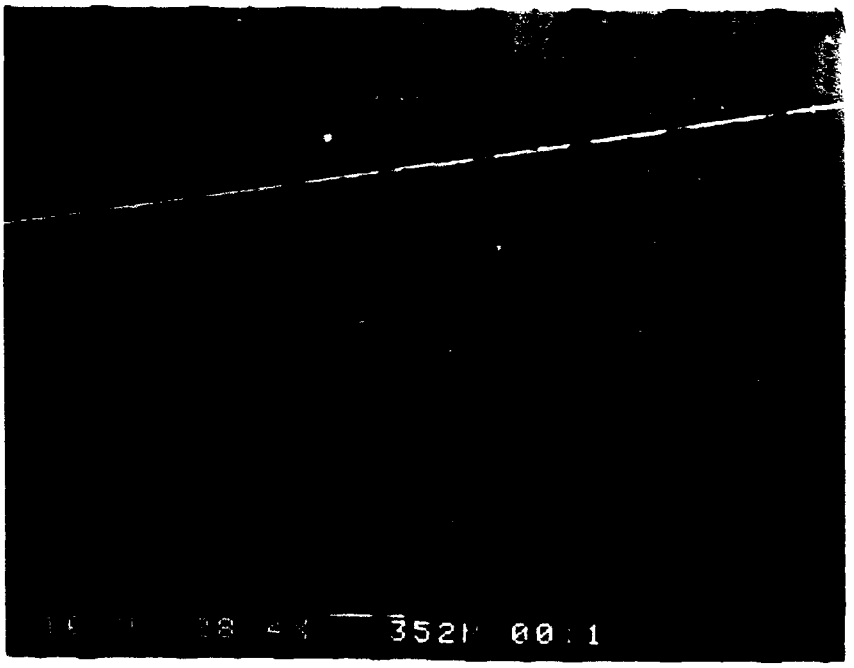


Figure 5-27. Backside of wafer after boron deposition. No crack or breakage due to thermal stress was observed.

N+ Photolithography and Diffusion. Problems were encountered in the n+ photolithography process possibly due to the mask being inadvertently exposed to room light prior to its fabrication. The problem was that the negative photoresist failed to fully crosslink upon exposure and remain after developing. In an attempt to get a complete exposure, the exposure time was increased first to 50 seconds and then to 100 seconds. After developing, the runs looked like they might be satisfactory for the 100 second exposure. However, as was later observed in subsequent processing, this step may have been detrimental to the electrical performance of the solar cell. Since the laboratory SEM was malfunctioning, no pictures were made following this step.

The sheet resistivity of a control wafer that was doped, along with the other processed wafers, was checked using the Veeco AP-150 automatic resistivity probe. The average sheet resitiviy was measured to be 84.77 ohms per square with a standard deviation of 8.63%.

Contact Photolithography. Since the contact mask was fabricated from the same box of inadvertently exposed HRP plates as the n+ mask, the exposure time had to also be increased in order to completely expose the areas to remain. An exposure time of 100 seconds was again used. This long exposure resulted in some line narrowing and undercutting of

the mask. However, the results were believed to be acceptable, since the contact runs are not seriously affected by being narrower.

Metallization and Patterning. The metallization procedure was to evaporate aluminum over the backside of the wafer and selectively remove regions in order to pattern the metal. This method required a positive photoresist and an etchant which would remove the exposed metal but not the silicon or silicon dioxide. The etchant was described in Chapter IV in the Metallization and Patterning section (see Aluminum Etch).

The thickness of the evaporated metal was calculated from the change in resonant frequency of a piezoelectric quartz crystal microbalance which was mounted in the same plane as the wafers. The calculation made in the last chapter yielded a result of 1 um (9,629 Angstroms) of aluminum.

The metal was patterned to yield a set of 6 um wide interdigitated conductors. The metal lines contacting the n+ regions ran the length of the cell and connected to a 50 mil (1270 um) wide by 410 mil (10,414 um) bonding pad. The metal lines contacted the regions were the slits came through the solar cells backside, as shown in Figure 5-28. Similarly, the metal contacting the p+ regions ran the

length of the cell and connected to a common bonding pad of the same dimensions.

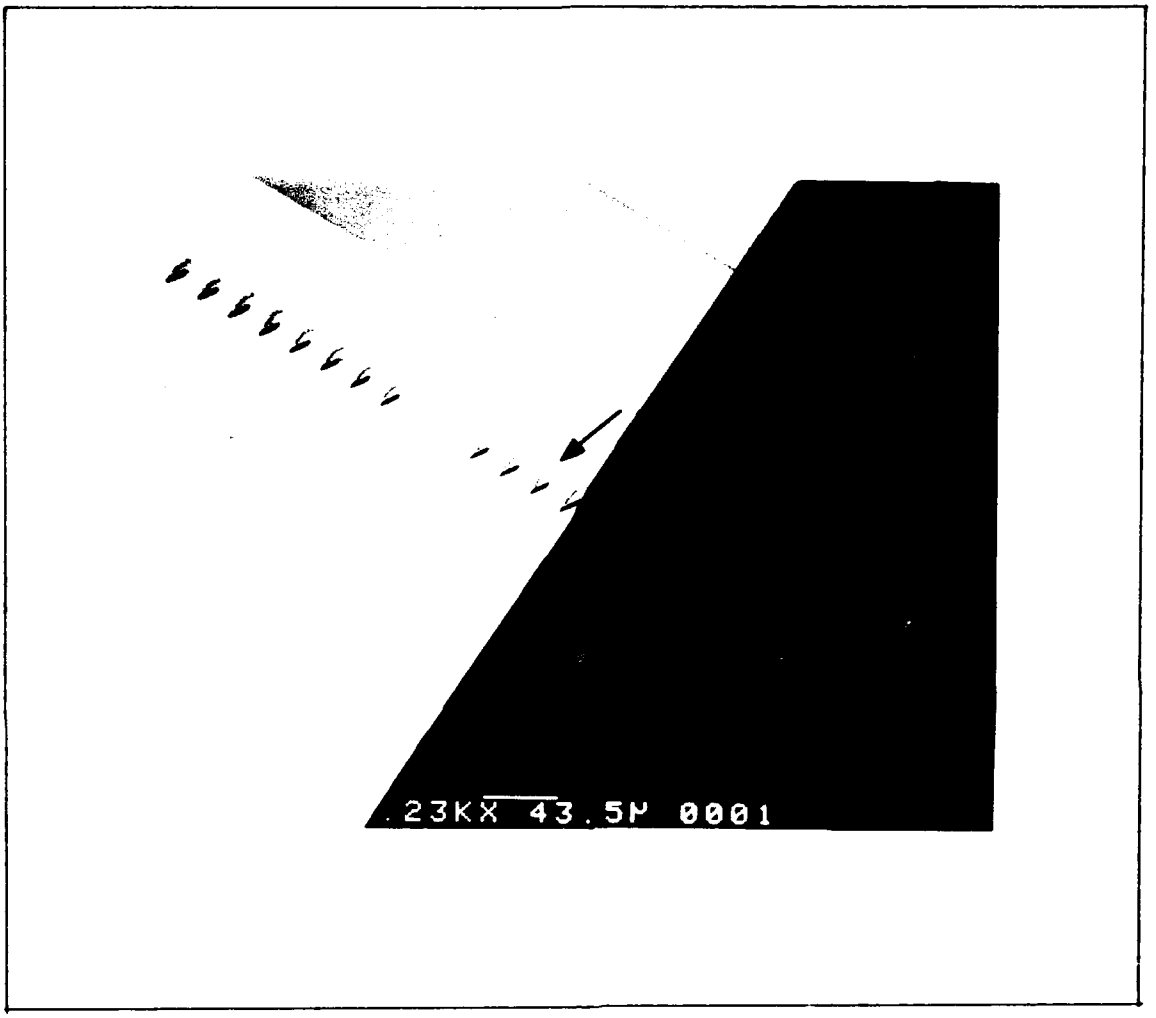


Figure 5-28. The metal contacting the n+ region was centered on the slits.

One problem associated with the metal patterning is seen in Figure 5-29. This SEM photograph shows a magnified view of how a metal line contacts the n+ doped regions were the slits come through the backside of the wafer. As can be

seen, the metal near the slit was removed. This was believed to be a result of the photoresist being very thin along the edges of the slit. Therefore, the aluminum etchant undercut the positve photoresist around the slits. This was not a serious problem since the area around the slits is a highly doped n+ region which provides a low resistance path to the metal. Figure 5-30 shows the backside of a wafer containing five solar cells. Figure 5-31 shows the topside of the same wafer.

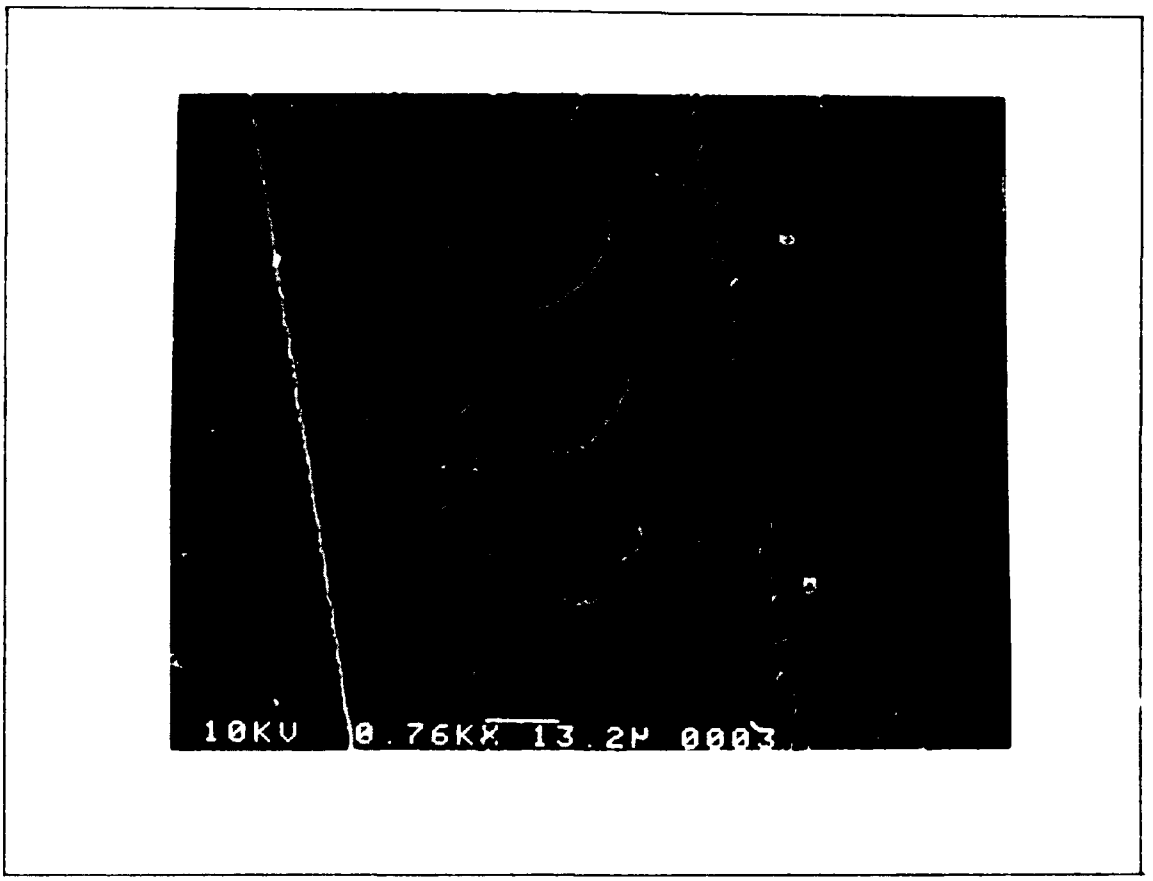


Figure 5-29. SEM photograph showing how metal around the slit was etched.

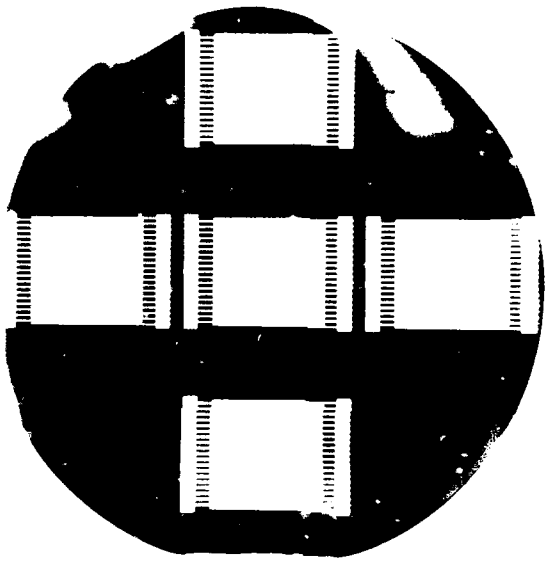


Figure 5-30. Photograph showing the backside of a completed wafer with five separate solar cells (magnification 1.5x).

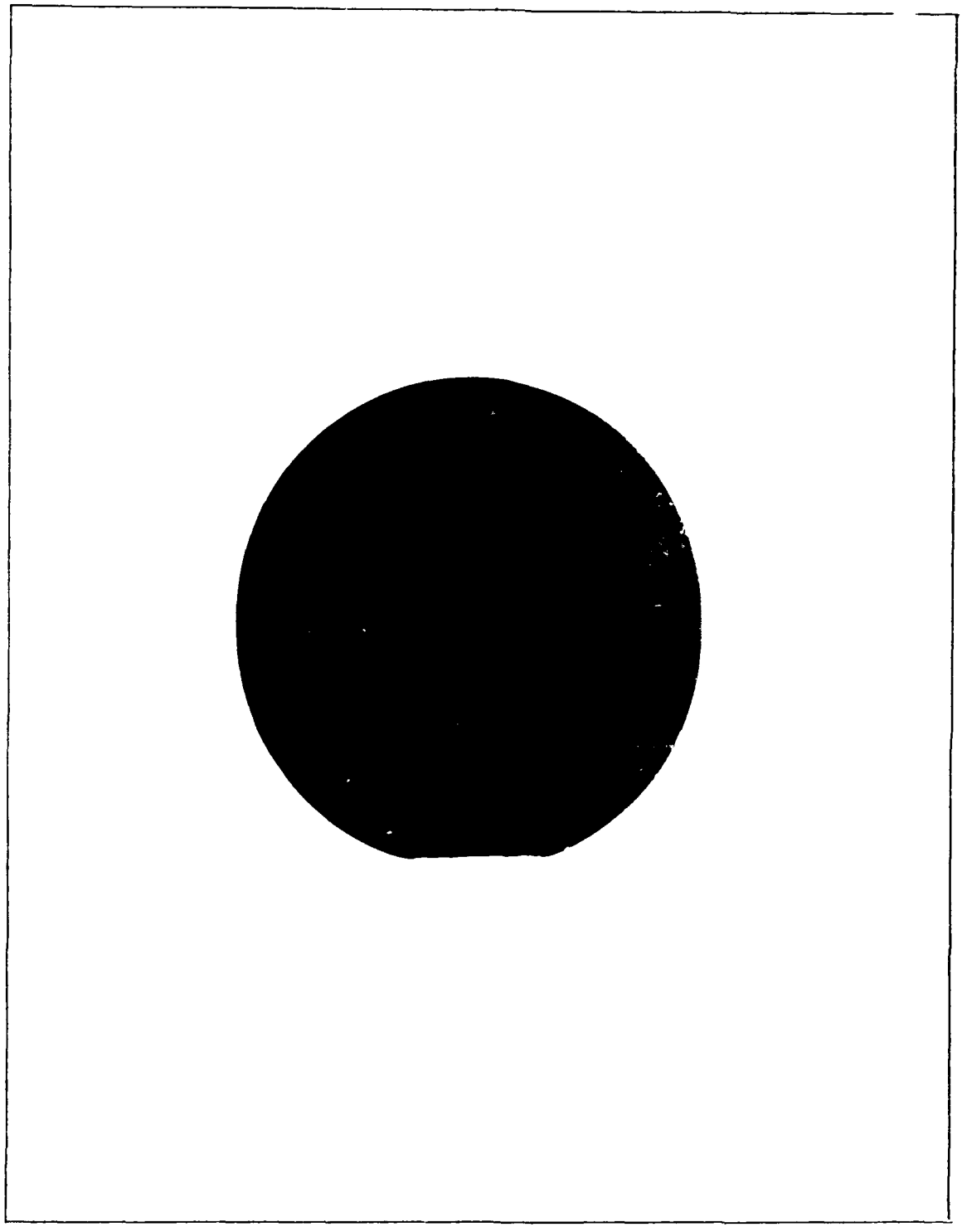


Figure 5-31. Photograph showing the front side of a completed wafer with five separate cells (magnification 1.5x).

Solar Cell Performance Evaluation

In this section, the electrical performance of the BCVJ solar cell will be discussed. For completeness, the solar cell's performance was analyzed to determine the cause of its poor efficiency.

Five wafers survived the fabrication process. Each wafer contained five cells (as shown in Figures 5-30 and 5-31). The wafers were screened visually for poor metallization and and holes which might cause breaks or shorts in the metal runs.

Next, the cells were tested with an ohmmeter to determine which ones were shorted and which had good action. Diode action was ascertained if a higher resistance was measured in one direction compared to the other. In other words, the solar cell pads could be gently probed with small wires connected to the ohmmeter leads. The leads could easily be reversed to determine if diode action was present. No diode action could be detected. The resistance was approximately 1.2 ohms regardless of the lead orientation.

The best cells (determined visually) were all on wafer A15. These cells were tested under an AM0 solar simulator, and the efficiency determined. All cells were less than 0.1 percent efficient which would be expected since no diode action could be detected.

In order to determine the reasons for the poor efficiency, the metal and all the oxide was stripped from one of the better wafers. This was done by immersing the wafer in a DI water:HF (10:1) solution. Next, the backside was stained to accentuate the n- and p-doped regions. The backside was stained by placing a few drops of a 3:1:10 solution of HNO_3:HF:CH_3OOCH on the wafer and shinning a microscope light on the wafer for about 15 seconds. The wafer was then rinsed and examined under an optical microscope. Figure 5-32 shows the results of the staining procedure. The light areas are the phosphorus (n+) doped regions, the dark areas are the boron (p+) doped regions, and the area between the dark and light regions is the substrate (lightly p-doped).

The runs were examined for breaks which might cause a short between the two regions. A break in a p+ run would not create a short, since the purpose of the p+ region was to provide a better ohmic contact to the substrate. However, a break in an n+ run would result in a short between the substrate and the n+ regions when the metal was applied. When inspected carefully, numerous areas were found were breaks occurred in the n+ runs. Figure 5-33 shows two such breaks. These are belived to be the result of over-exposing the negative photoresist during the n+ photolithography which resulted in undercutting the runs.

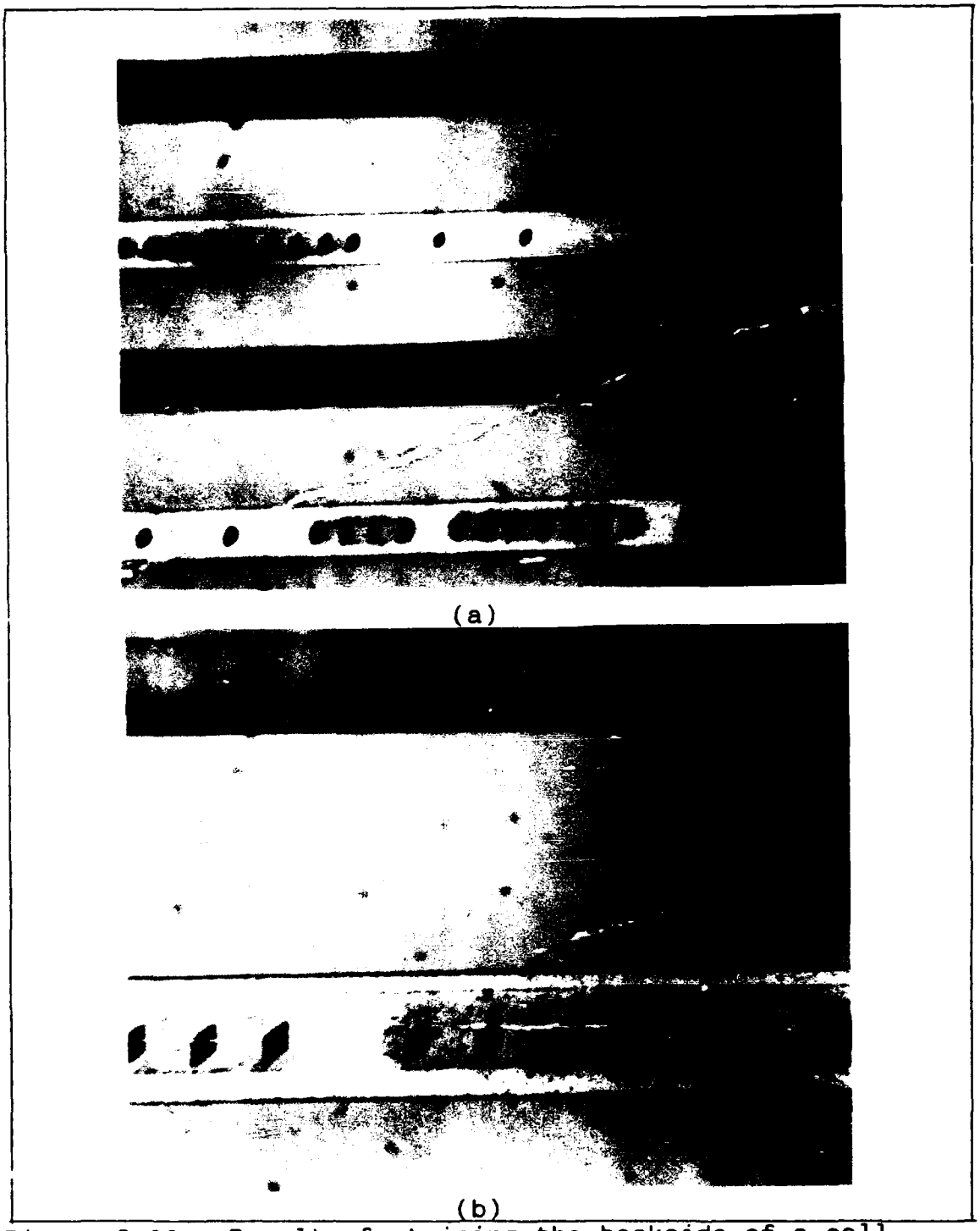


Figure 5-32. Result of staining the backside of a cell. The dark area is the boron doped region, the light area is the phosphorus doped region, and the area between is the substrate: (a) magnification 90x, (b) magnification 220x.

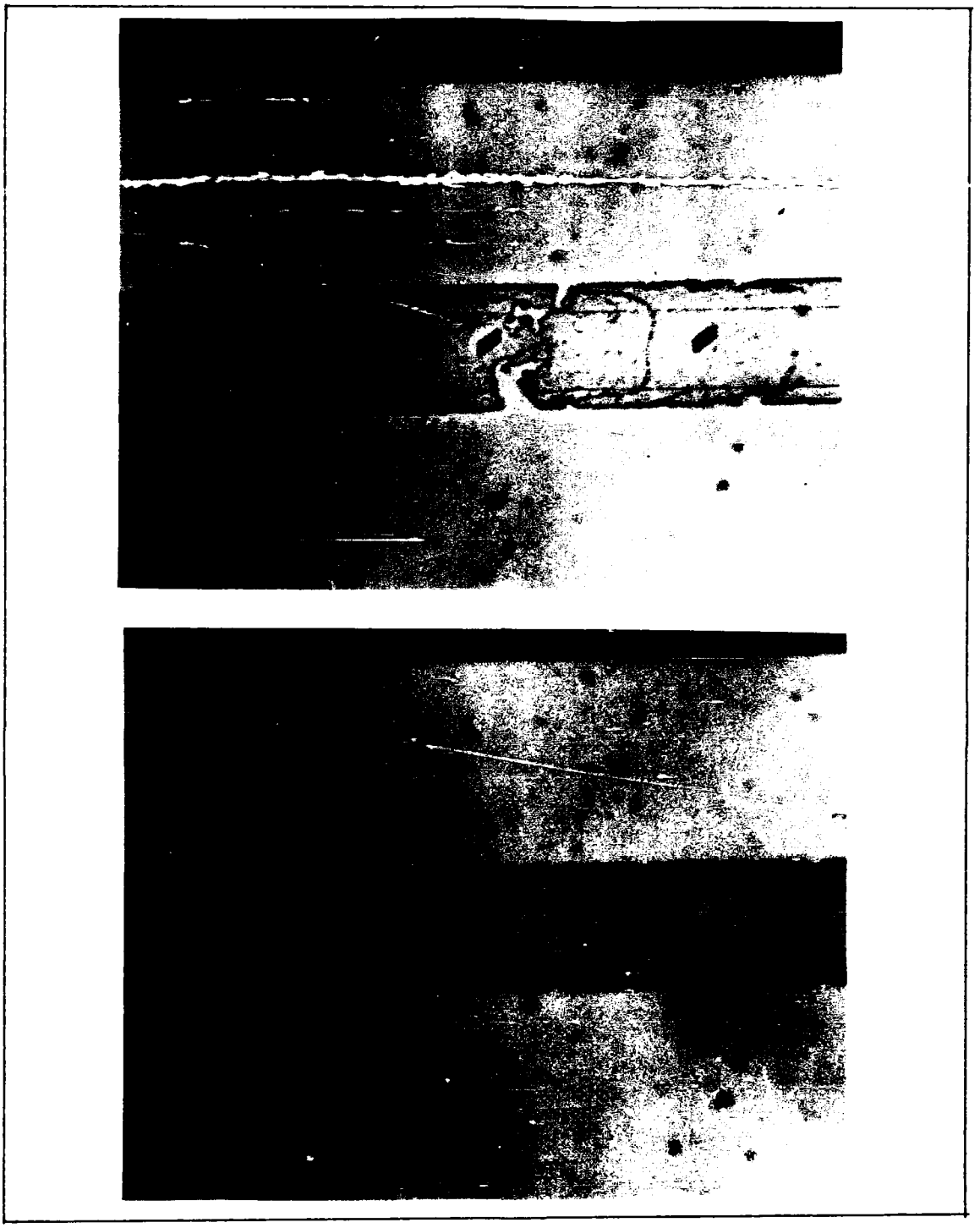


Figure 5-33. Two examples of breaks in the n+ runs which caused the n+ region to short to the substrate when the metal was applied (magnification 220x).

Another problem discovered during the failure analysis is shown in Figure 5-34. This SEM photograph shows that oxide remained on the grooves. Therefore, the groove walls would not be completely doped. Figure 5-35 shows the inside of the grooves. From this SEM photograph, the oxide can be seen to completely cover the walls 30 um below the top of the groove. This problem could be attributed to the fact

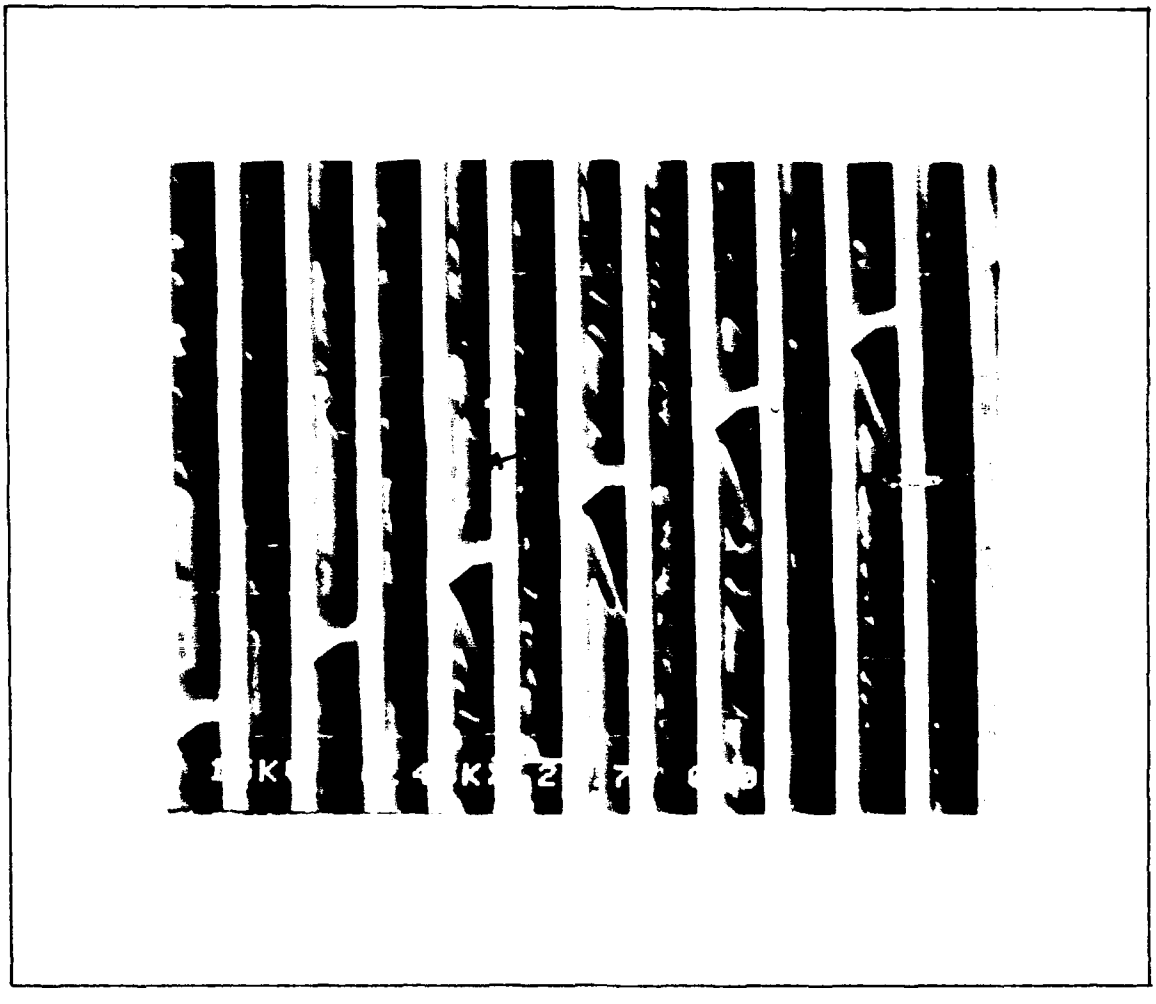


Figure 5-34. Grooves after the cell was completed showing the oxide on the walls of the grooves.

that buffered HF did not get into the grooves in sufficient concentration to remove the oxide. This may have been the result of surface tension which may be remedied by finding a compatible wetting agent for the buffered HF etchant.

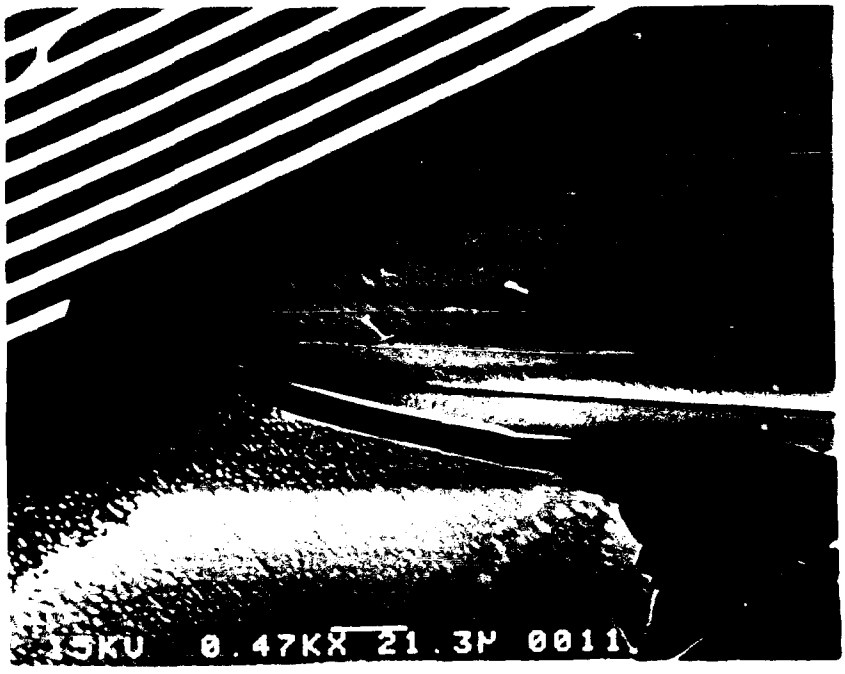


Figure 5-35. Grooves after the cell was completed showing oxide covering the walls approximately 30 um below the top surface.

VI. Conclusions and Recommendations

In the preceding chapters, a solar cell design was proposed which synergistically combines the advantages of both the interdigitated back-contact solar cell concept and the vertical-junction solar cell concept. The proposed design, called the back-contact vertical-junction (BCVJ) solar cell, was fabricated and evaluated to determine the feasibilty of the design. This chapter presents a summary of the findings as they pertain to the successful fabrication of the design. Recommendations for further efforts aimed toward improving the fabrication procedures and producing an operative and efficient solar cell are given.

Conclusions

The following are the significant conclusions of this research based on the results obtained:

1. Chemically polishing wafers more than 10 um should be avoided because the wafers tend to polish slower near the center. This results in wafers which are not uniformly thick.

2. If properly aligned, grooves 5 um wide can be etched 300 um deep into a (110) silicon wafer. The groove spacing before etching can be as close as 20.4 um.

3. The depth of the groove is a function of the length and width of the groove, and, it can be accurately determined from equation 40 in Chapter 3.

4. If the thickness of the wafer is equal to or slightly less than the calculated depth (by 1-3 um) , a small slit occurs on the backside of the wafer where the bottom tip of the groove intersects the backside of the wafer.

5. An oxide mask thickness of 2.35 um is sufficient to protect against a 50% by weight solution of KOH and water at 85 °C for the time required to etch the 290 um deep grooves into the (110) silicon. The remaining oxide after ODE is still thick enough to be used as a diffusion mask.

6. Dust or scratches on the groove mask or wafer can result in the walls of the grooves being destroyed during ODE. If the scratches or particles are large, holes will be made which may destroy the cell.

7. Placing a piece of lens tissue between the wafer and photoresist spinner chuck protects the groove pattern from being scratched while coating it with photoresist.

8. Over etching during the ODE is not a serious problem, since the etching essentially ceases at the same time the groove reaches the backside. The etching ceases because the grooves are completely bounded with {111} planes.

9. If the wafer is thinner than the calculated groove depth (d), the slits on the backside become longer. If the slits are large, the backside photolithography becomes more difficult because photoresist is pulled into the slits.

10. The grooves can be pointed by immersing the grooved structure into an isotropic silicon etchant. However, the backside of the wafer could not be protected from this etchant with either positive or negative photoresist.

11. The grooved structure has very good structural integrity and can withstand high temperature diffusion without fracturing.

12. The p+ and n+ runs can be easily aligned using the slits on the backside of the wafer.

13. The n+ mask was slightly fogged requiring a longer exposure. This longer exposure may have caused the masked areas to be exposed, and thus preventing complete oxide removal. When the contacts were cut and metal layer added, the substrate shorted to the n+ diffusion through the overlaying metal. This rendered the solar cells inoperative.

14. The contact mask and metal mask could be aligned using the slits and diffusion runs on the backside.

15. The oxide in the grooves was not completely removed prior to n+ diffusion due to surface tension between the

silicon and the buffered HF etchant. Therefore, the grooves were not completely doped.

Recommendations

Although the fabricated solar cells were inoperative, the results were extremely encouraging. The following recommendations are given in hope that further research will be done to determine the feasibility of the back-contact vertical-junction solar cell. With the arrival of new equipment, the sucessful fabrication of the BCVJ solar cell should be even more likely.

1. Use unexpired HRP plates to fabricate all five mask levels. Insure each mask has excellent contrast and is not foggy. An even better alternative would be to have chromium masks fabricated commercially.

2. Use wafers with stringent specifications of uniform thickness, flat orientation, and the exact thickness desired.

3. Consider the silicon consumed in the oxidation process when calculating the required thickness of the wafers.

4. Examine several wetting agent candidates which are compatible with HF and which will decrease the surface tension allowing the buffered HF to flow into the narrow grooves. A drop of liquid soap might do the trick.

5. Find a method of protecting the backside of the wafer while pointing the grooves with an isotropic etchant. Contact various manufacturers of photoresists to determine if a photoresist exists which is resistant to the planar etchant. Another possiblity is to cover the backside with a thin sheet of plastic wrap which clings to glass well.

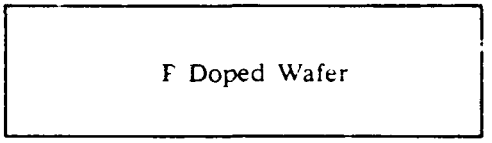
6. Fabricate cells without grooves first to perfect the diffusion and metallization processes, then fabricate cells with grooves and compare the efficiencies. A suggested processing sequence for cells with out grooves is to first grow an oxide (approximately 1 um) on bothsides of a silicon wafer and then complete steps 9-30 from the Appendix.

Inspect the n+ windows carefully, following the oxide etch in step 17, to insure the windows are completely and uniformly etched. Also, strip the oxide from a wafer, following the n+ diffusion (step 19), and perform a stain to determine if the runs are completely and uniformly doped.

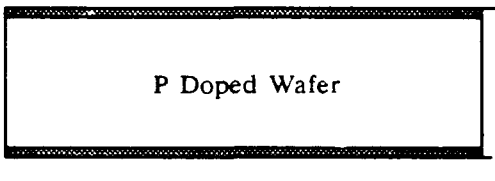
APPENDIX

BACK-CONTACT VERTICAL-JUNCTION SOLAR CELL FABRICATION STEPS

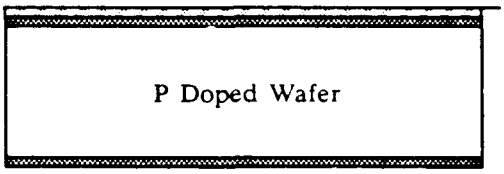
FABRICATION STEPS:

1. 

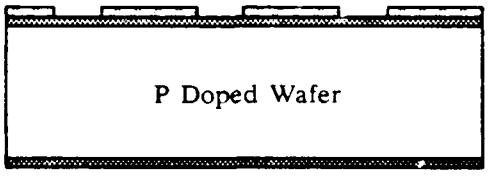
Start with a Czochralski grown, 2-inch diameter silicon wafer, polished on both sides, thickness 290 um, resistivity 1-3 ohm-cm, boron doped.

2. 

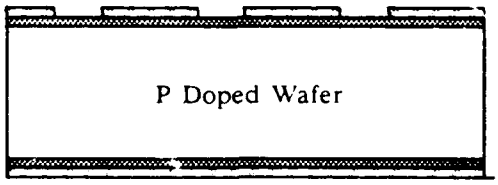
Grow thick oxide on both sides of wafer.

3. 

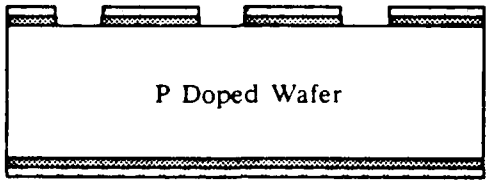
Apply negative photoresist to topside of wafer and softbake.

4. 

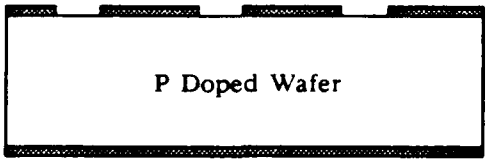
Align with groove mask, expose, develop, and hardbake.

5. 

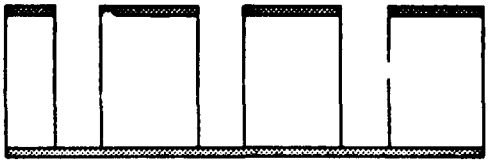
Apply HMDS and positive photoresit to backside and hardbake.

6. 

Etch oxide.

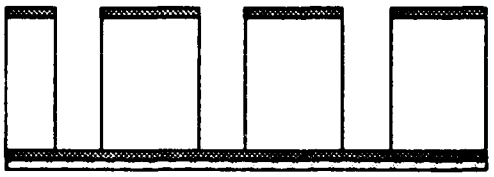
7. 

Remove photoresist from both sides.

8. 

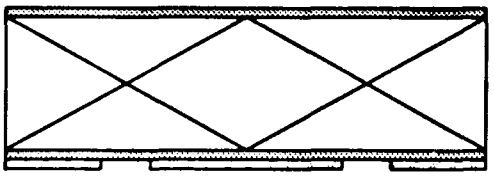
Orientation dependent etch in KOH and water to produce grooves on the wafer's topside.

FABRICATION STEPS CONTINUED:

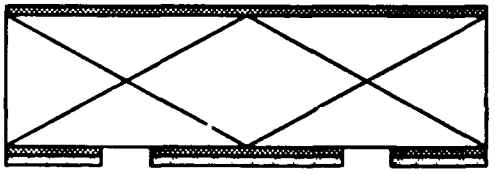
9. 

Apply negative photoresist to backside and softbake.

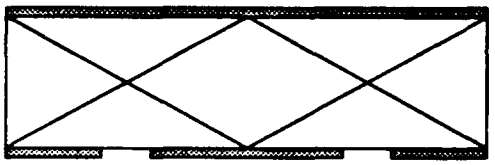
PICTURES FROM THIS POINT ARE ROTATED 90°

10. 

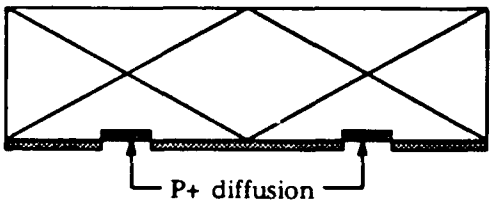
Align with p+ mask, expose, develop, and hardbake.

11. 

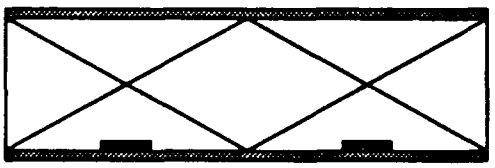
Etch oxide.

12. 

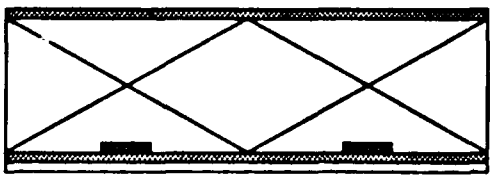
Remove photoresist.

13. 

Perform p+ diffusion.

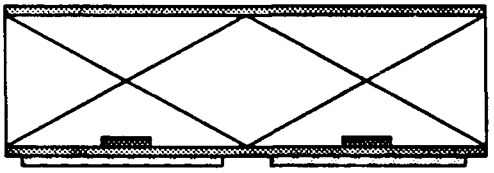
14. 

Grow oxide over p+ areas and drive-in the dopant.

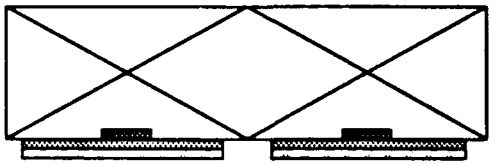
15. 

Apply negative photoresist to backside and softbake.

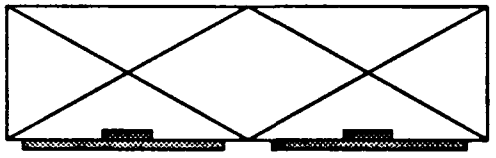
FABRICATION STEPS CONTINUED:

16. 

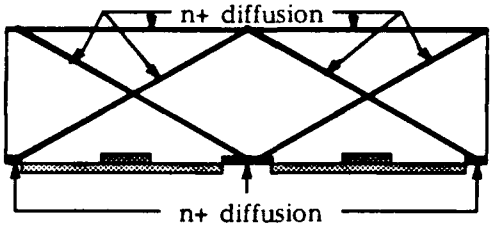
Align with n+ mask, expose, dvelop, and hardbake.

17. 

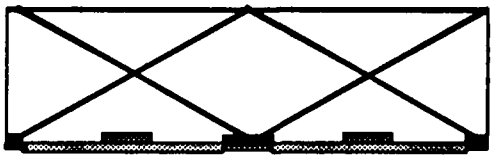
Etch oxide.

18. 

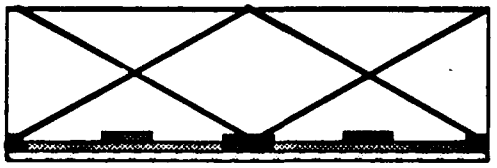
Remove photoresist.

19. 

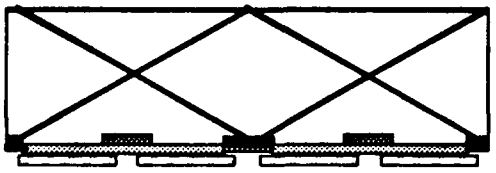
Preform n+ diffusion.

20. 

Grow a thin oxide over exposed silicon.

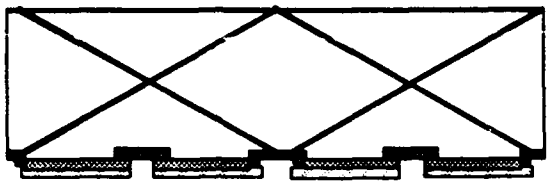
21. 

Apply negative photoresist and softbake.

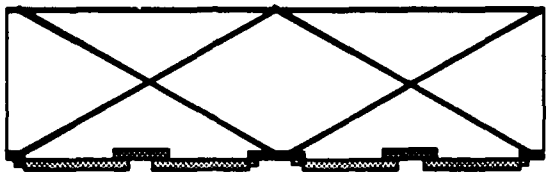
22. 

Align contact mask, expose, develop, and hardbake.

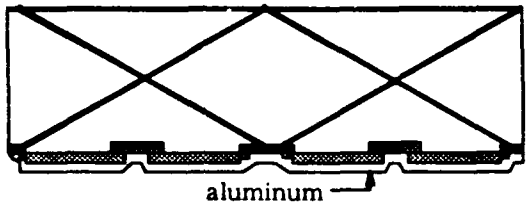
FABRICATION STEPS CONTINUED:

23. 

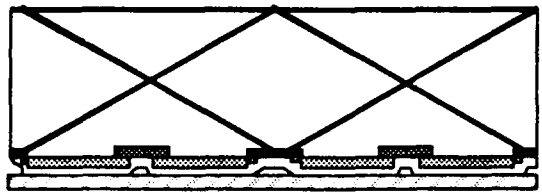
Etch oxide.

24. 

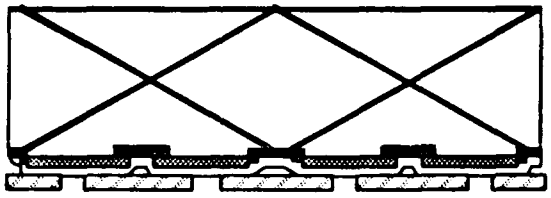
Remove photoresist.

25. 

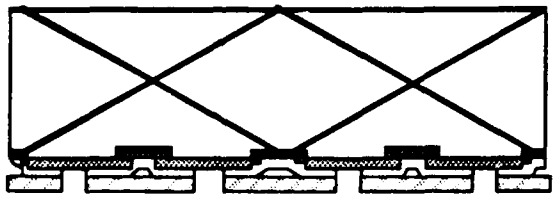
Evaporate aluminum over backside of wafer.

26. 

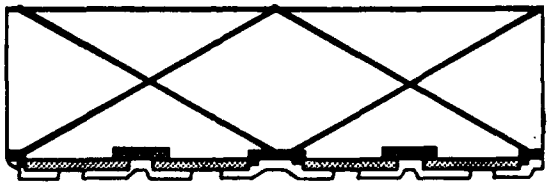
Apply HMDS, positive photoresist, and softbake.

27. 

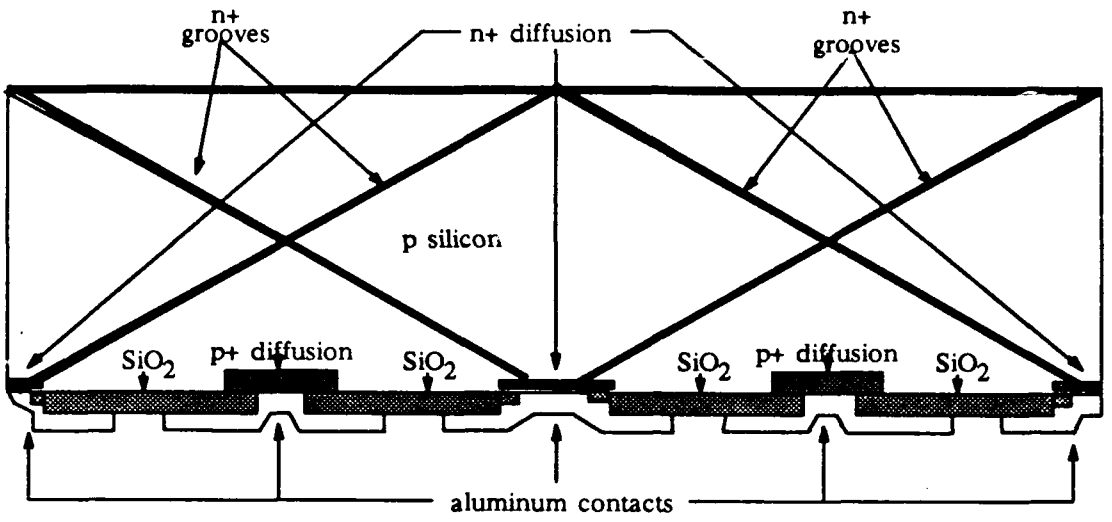
Align with metal mask, expose, develop, and hardbake.

28. 

Etch aluminum.

30. 

Remove photoresist.



COMPLETED BCVJ SOLAR CELL

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Vita

M. Wayne Carver was born August 8, 1956 in Greenville, South Carolina. He graduated from Greenville Senior High School June 4, 1974. He enlisted in the United States Air Force in March 1975. Following Basic Training, he married his high school sweetheart, Gina E. Freeman, on May 17, 1975. He then attended Electronic Instrumentation Technical School at Lowry Air Force Base Denver, Colorado for nine months. After technical school, he worked for three years as an Instrumentation Technician in the FM Ground Station at the Vandenberg Tracking Station, Vandenberg Air Force Base, California. In Feburary 1979, he transfered to the Air Force Flight Dynamics Laboratory at Wright Patterson Air Force Base, Ohio. In June 1980, after being accepted into the Air Force Education and Commissioning Program, he attended the University of Tennessee at Knoxville. In June 1983, he graduated with high honors with a Bachelor of Science Degree in Electrical Engineering. After graduating from Officer Training School on September 30, 1983, he was assigned to the Air Force Electronic Warfare Center at Kelly Air Force Base, Texas. In June 1986, he entered the Air Force Institute of Technology's Masters Degree Program in the electronic devices and the VLSI design sequences. He has two children Angela, 10, and Lauren, 5.

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SECURITY CLASSIFICATION OF THIS PAGE

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1a. REPORT SECURITY CLASSIFICATION Unclassified	1b. RESTRICTIVE MARKINGS
2a. SECURITY CLASSIFICATION AUTHORITY	3. DISTRIBUTION/AVAILABILITY OF REPORT Approved for public release: Distribution unlimited
2b. DECLASSIFICATION/DOWNGRADING SCHEDULE	
4. PERFORMING ORGANIZATION REPORT NUMBER(S) AFIT/GE/ENG/88M-4	5. MONITORING ORGANIZATION REPORT NUMBER(S)
6a. NAME OF PERFORMING ORGANIZATION School of Engineering 6b. OFFICE SYMBOL (If applicable) AFIT/ENG	7a. NAME OF MONITORING ORGANIZATION
6c. ADDRESS (City, State, and ZIP Code) Air Force Institute of Technology (AU) Wright-Patterson AFB, Ohio 45433-6583	7b. ADDRESS (City, State, and ZIP Code)
8a. NAME OF FUNDING/SPONSORING ORGANIZATION Air Force Wright Aeronautical Laboratories 8b. OFFICE SYMBOL (If applicable) AFWAL/POOC-2	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER
8c. ADDRESS (City, State, and ZIP Code) Wright-Patterson AFB, Ohio 45433	10. SOURCE OF FUNDING NUMBERS PROGRAM ELEMENT NO. / PROJECT NO. / TASK NO / WORK UNIT ACCESSION NO.

11. TITLE (Include Security Classification)

BACK-CONTACT VERTICAL-JUNCTION SOLAR CELL (UNCLASSIFIED)

12. PERSONAL AUTHOR(S)

Michael Wayne Carver, Captain USAF

13a. TYPE OF REPORT	13b. TIME COVERED	14. DATE OF REPORT (Year, Month, Day)	15. PAGE COUNT
MS Thesis	FROM _____ TO _____	March 1988	238

16. SUPPLEMENTARY NOTATION

17. COSATI CODES			18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
FIELD	GROUP	SUB-GROUP	
10	02		vertical junction, solar cell, back contact, silicon, anisotropic etching, vertical groove, efficiency, mask fabrication, potassium hydroxide, solar cell fabrication.

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

Title: BACK-CONTACT VERTICAL-JUNCTION SOLAR CELL (UNCLASSIFIED)

Thesis Chairman: Edward S. Kolesar, Major, USAF
Assistant Professor of Electrical Engineering

20. DISTRIBUTION/AVAILABILITY OF ABSTRACT ☒ UNCLASSIFIED/UNLIMITED ☐ SAME AS RPT ☐ DTIC USERS	21. ABSTRACT SECURITY CLASSIFICATION Unclassified
22a. NAME OF RESPONSIBLE INDIVIDUAL Edward S. Kolesar, Major, USAF	22b. TELEPHONE (Include Area Code) (513) 255-2024 22c. OFFICE SYMBOL AFIT/ENG

DD Form 1473, JUN 86 *Previous editions are obsolete.* SECURITY CLASSIFICATION OF THIS PAGE

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OCK 19

The objective of this thesis was to improve the efficiency of silicon solar cells by designing and fabricating a solar cell which synergistically combines the advantages of the interdigitated back-contact solar cell with the advantages of the wedged-channel vertical-junction solar cell. Solar cell designs which combine the two concepts were proposed and evaluated. A final design was chosen which consisted of vertical grooves anisotropically etched from the front side to the backside of a (110) oriented silicon wafer. The groove side walls etched vertically and the end walls etched on a taper. As the grooves reached the backside, the end walls tapered together forming a small slit where the connections to the back contacts occured. A theoretical equation relating the groove length, width, and depth was developed. Grooves ranging from 5 um to 100 um wide, and 870 um to 1,140 um long were anisotropically etched into a 300 um thick (110) wafer to verify the equation and determine the optimum groove length and width for the final design. The final design consisted of grooves 5 um wide, 1000 um long, and 290 um deep. The groove centers were spaced 1 mil (25.4 um) apart. A five-level mask set was designed and fabricated. A fabrication procedure for the final design was specified, and solar cells were fabricated. The results of the fabrication steps are discussed and evaluated. While the fabricated cells demonstrated the feasibility of the design, improvements in efficiency could not be determined due to short circuits between the doped regions. Recommendations for improving the fabrication procedures are given.