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PROTOTYPE INSTRUMENTATION AND DESIGN STUDIES

Alan C. Huber
John O. McGarity
John A. Pantazis
A. Wallace Everest
David J. Sperry
Scott J. Moran
M. Paul Gough
Ernest G. Holeman

AMPTEK, INC.
6 De Angelo Drive
Bedford, MA 01730

May 14, 1990

Scientific Report No. 2

GEOPHYSICS LABORATORY
AIR FORCE SYSTEMS COMMAND
UNITED STATES AIR FORCE
HANSCOM AIR FORCE BASE, MASSACHUSETTS 01731-5000

"This technical report has been reviewed and is approved for publication."

(Signature)
MARILYN R. OBERHARDT
Contract Manager

(Signature)
DAVID A. HARDY
Branch Chief

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(Signature)
RITA C. SAGALYN
Division Director

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Alan C. Huber
John O. McGarity
John A. Pantazis
A. Wallace Everest
David J. Sperry
Scott J. Moran
M. Paul Gough
Ernest G. Holeman

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6 DeAngelo Drive
Bedford, MA 01730

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Flight prototype sensor systems using spherical sections and electrostatic deflection are being developed, fabricated, tested and calibrated. The detectors will measure the flux of ions and electrons over a 100° x 10° angular fan and in 32 discrete energy levels from 10 eV to 10 KeV. This report describes the sensor system design for an instrument package for shuttle flight as well as a correlator to look for wave-particle interactions.

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PROTOTYPE INSTRUMENTATION AND DESIGN STUDIES

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NESTED HEMISPHERE ESA DESIGN

A fabrication error in the aluminum hemispheres (6061-T6) that were received last quarter was discovered. One of the hemisphere sizes was not completely formed to a full 2π. That particular size was returned to the manufacturer for completion or replacement.

A theroretical mechanical stress analysis was performed by an Air Force contractor (Assurance Technology Corp.) on the proposed designs of the various assemblies of the prototype ESA. Those assemblies were the nested tri-quadraspherical electrostatic analyzer (Q^3ESA), the Data Processing Unit (DPU), the Rotary Table Motor (RTM), and the Flight Data Recorder FDR).

To support such an analysis, the individual assemblies had to be detailed and designed to a level that identified wall thickness, mounting holes and placement, weight and power distributions, and major internal sub-assemblies. Most of the past quarter has been spent extending our preliminary design to a level that could be modeled and evaluated for space shuttle flight worthiness. Electrical details, cabling, connectors, signal flows, were proposed. The analysis in turn suggested design changes that would enhance flight reliability. For example, the capture ring on the RTM was doubled in thickness to ½ inch to insure that it could retain the rotary table and sensor assemblies if the motor shaft sheared. The wall thickness and assembly screw sizes for the FDR were increased to allow an additional safety margin for the pressurized tape recorder assembly. Drawings of these four assemblies in their latest proposed configurations are attached.

The ESA (Q^3ESA) design was further refined. The housing adjacent to the apertures was redesigned to avoid shadowing of the aperture inlets by the housing structure. The foot print was changed to minimize the rotary table diameter necessary to mount the instrument. The MCP shape was reduced slightly and a larger radius of curvature was used to feather the corners of the MCP array. An anode assembly and MCP housing/mount was designed. A tentative printed circuit layout for the anode and amplifiers was generated.

Many details of the DPU were evolved including the power supply area, the bottom frame structure, the motherboard mechanical design, the number and shape of DPU printed circuit cards, and the location and type of interface electrical connectors.

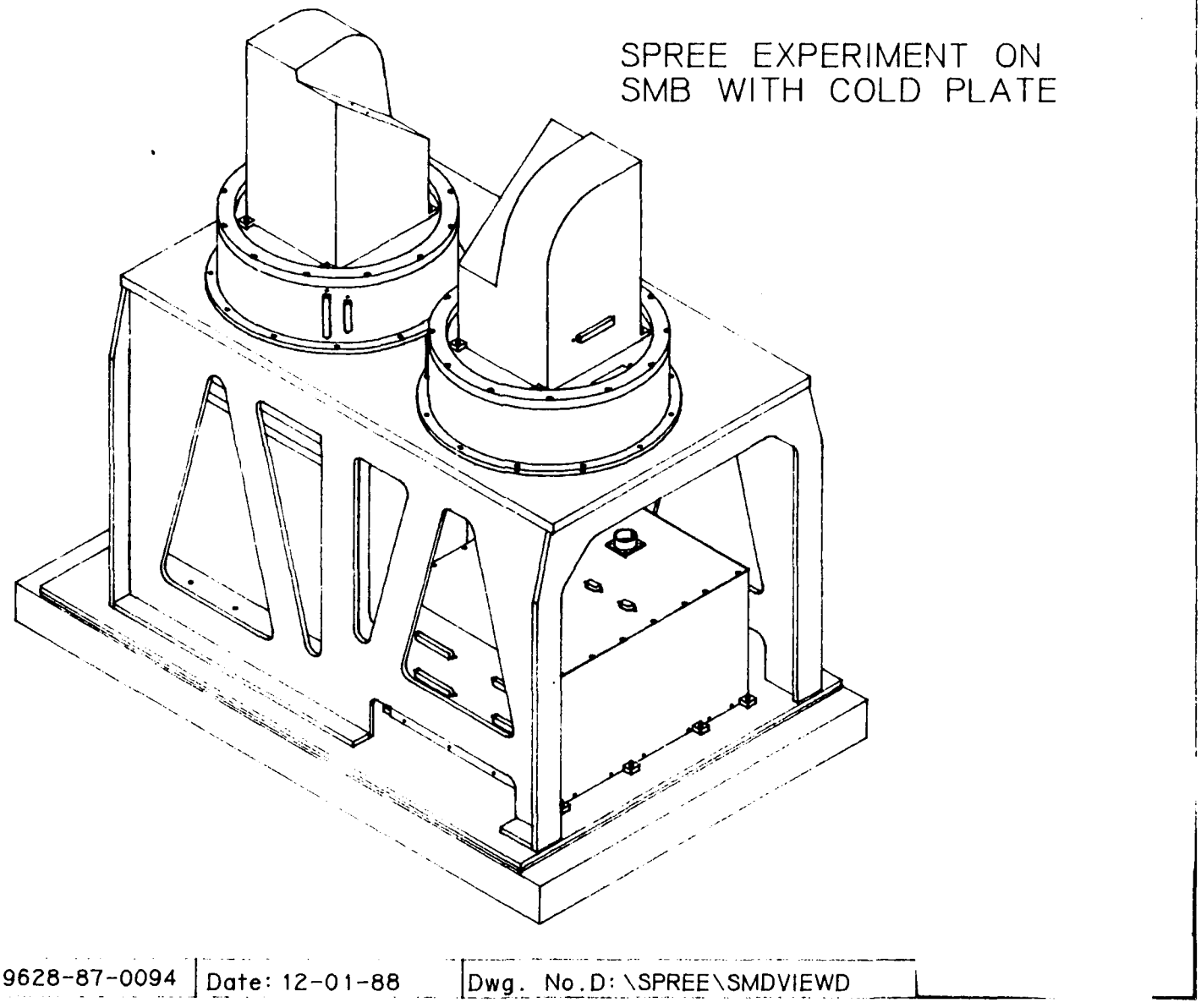
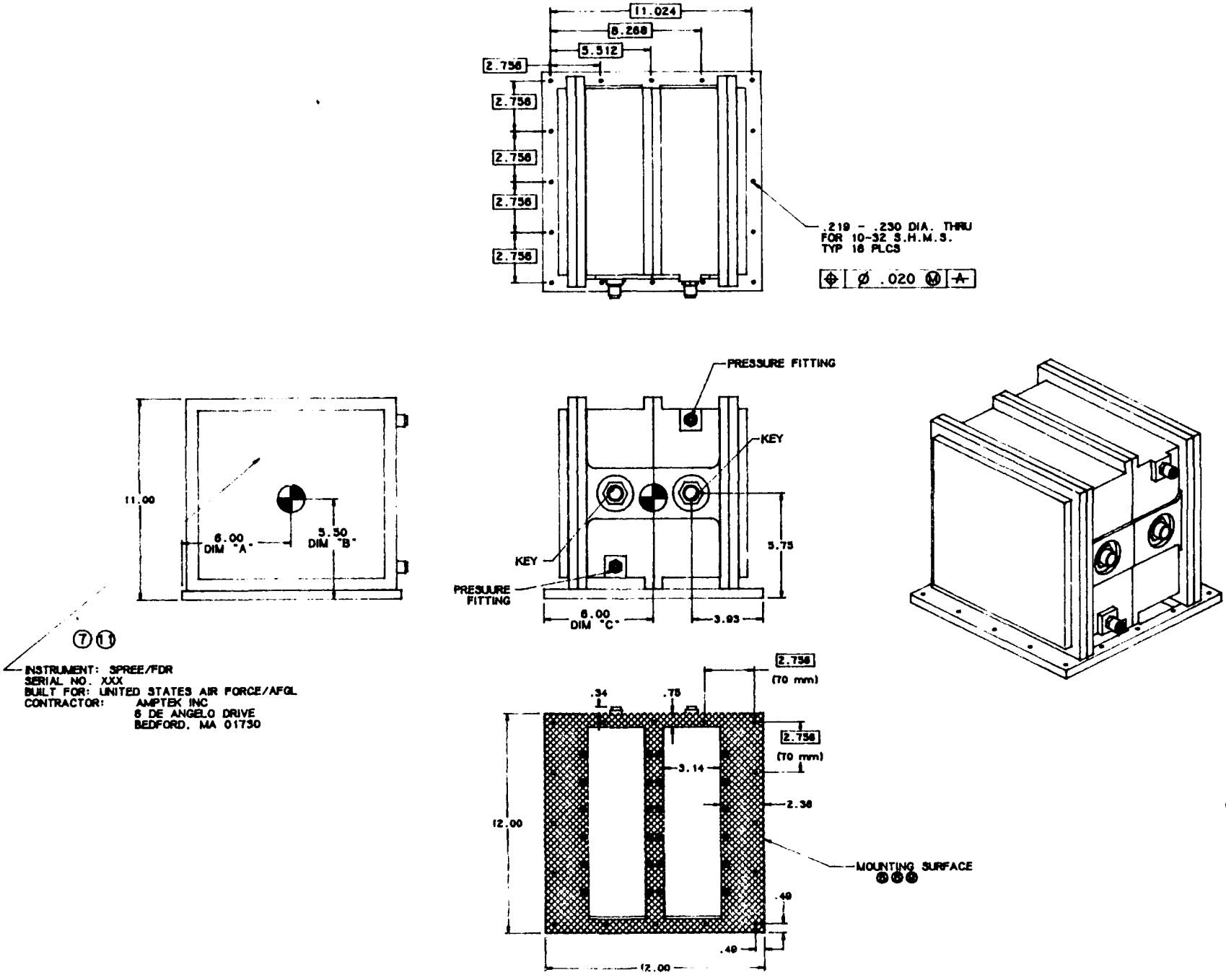

SPREE EXPERIMENT ON
SMB WITH COLD PLATE
Project No: F19628-87-0094
Date: 12-01-88
Dwg. No.D:\SPREE\SMDVIEWD

FIGURE QR5-1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8.268
5.512
2.756
2.756
2.756
2.756
2.756
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FOR 10-32 S.H.M.S.
TYP 16 PLCS
Ø .020 M A
11.00
6.00
DIM "A"
5.50
DIM "B"
⑦⑪
INSTRUMENT: SPREE/FDR
SERIAL NO. XXX
BUILT FOR: UNITED STATES AIR FORCE/AFGL
CONTRACTOR: AMPTEK INC
8 DE ANGELO DRIVE
BEDFORD, MA 01730
PRESSURE FITTING
KEY
KEY
PRESSURE
FITTING
5.75
6.00
DIM "C"
3.93
2.756
(70 mm)
.34
.78
2.756
(70 mm)
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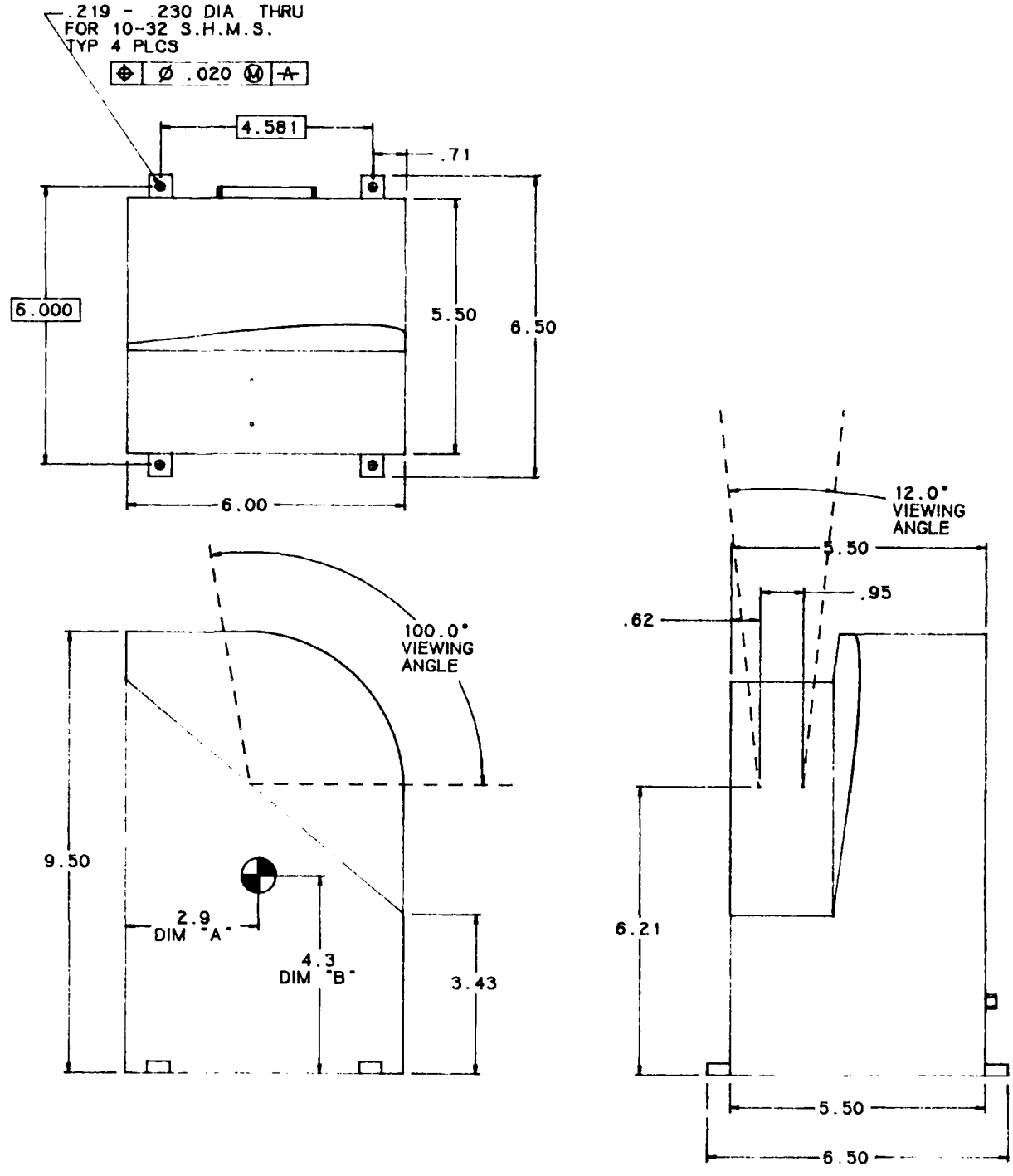
2.36
12.00
MOUNTING SURFACE
❹❺❻
.40
.40
12.00

FIGURE QR5-2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FOR 10-32 S.H.M.S.
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6.50
6.00
100.0°
VIEWING
ANGLE
9.50
2.9
DIM "A"
4.3
DIM "B"
3.43
12.0°
VIEWING
ANGLE
5.50
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.62
6.21
5.50
6.50

FIGURE - QR5-3

70 Watt Power Supply
(heaviest object in the DPU)
weight 140 grams (.31 lbs)

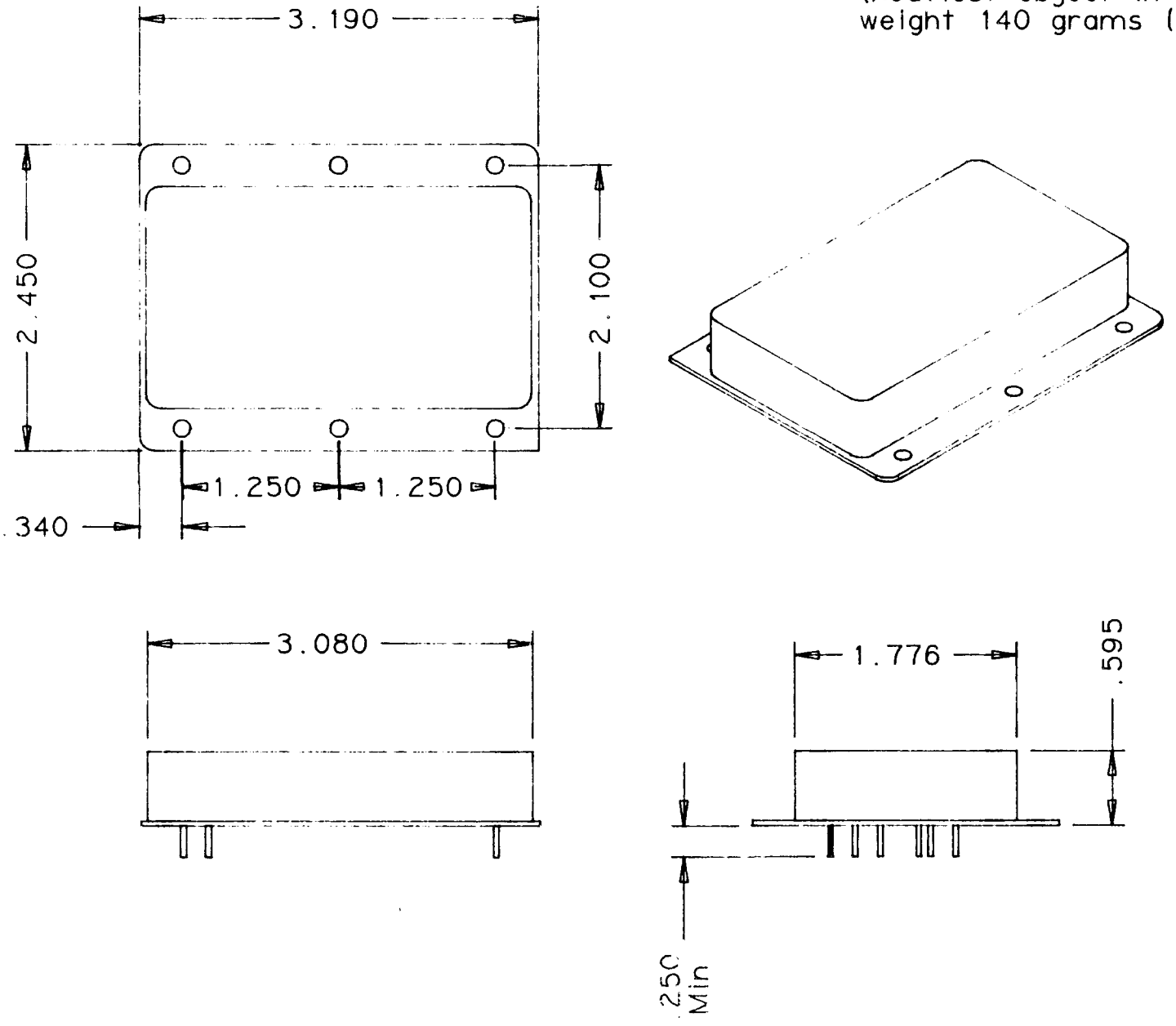
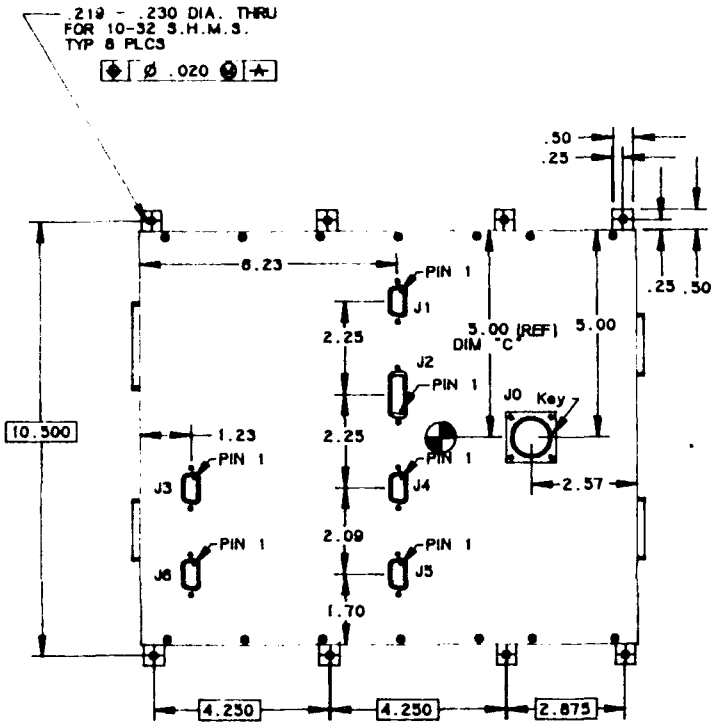


FIGURE QR5-4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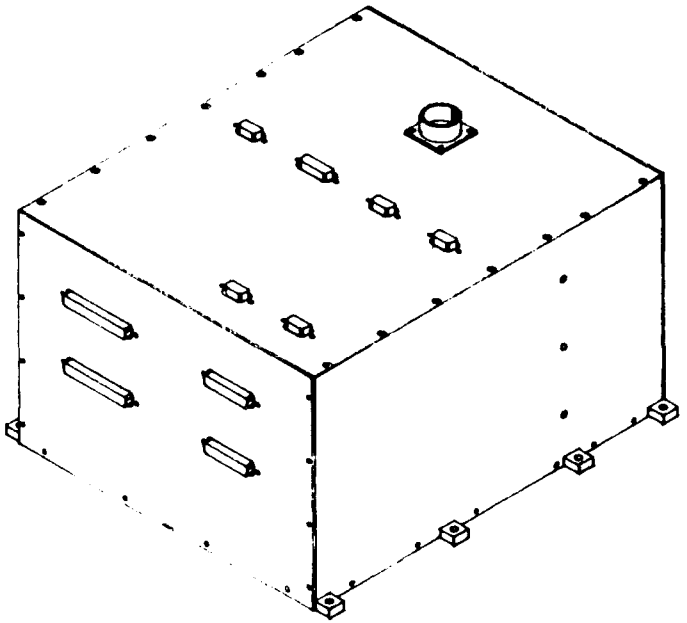
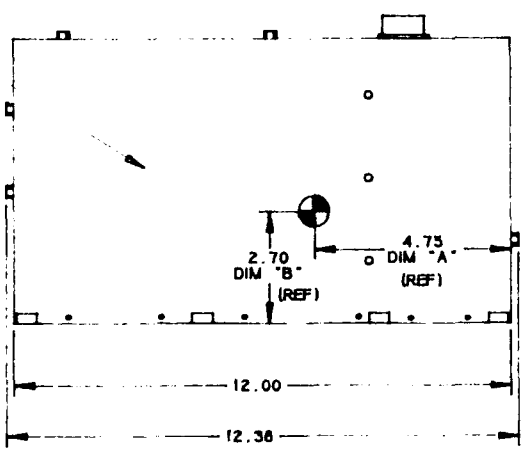
FOR 10-32 S.H.M.S.
TYP 8 PLCS
Ø .020
.50
.25
6.23
PIN 1
J1
2.25
5.00 (REF)
DIM "C"
5.00
.25 .50
J2
PIN 1
J0 Key
10.500
1.23
2.25
PIN 1
J3
PIN 1
J4
2.57
2.09
PIN 1
J6
PIN 1
J5
1.70
4.250
4.250
2.875

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(REF)
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DIM "A"
(REF)
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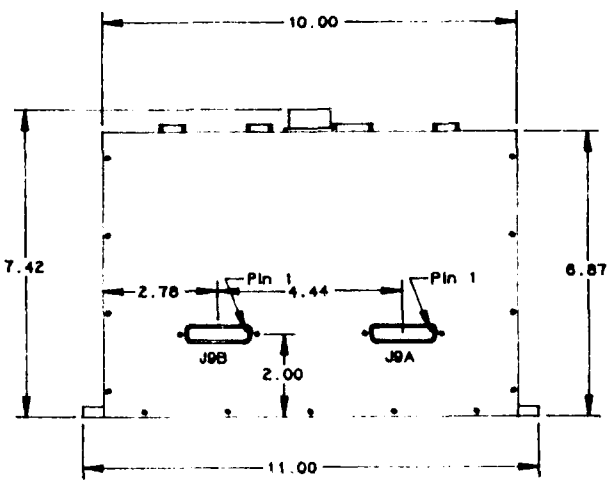
12.36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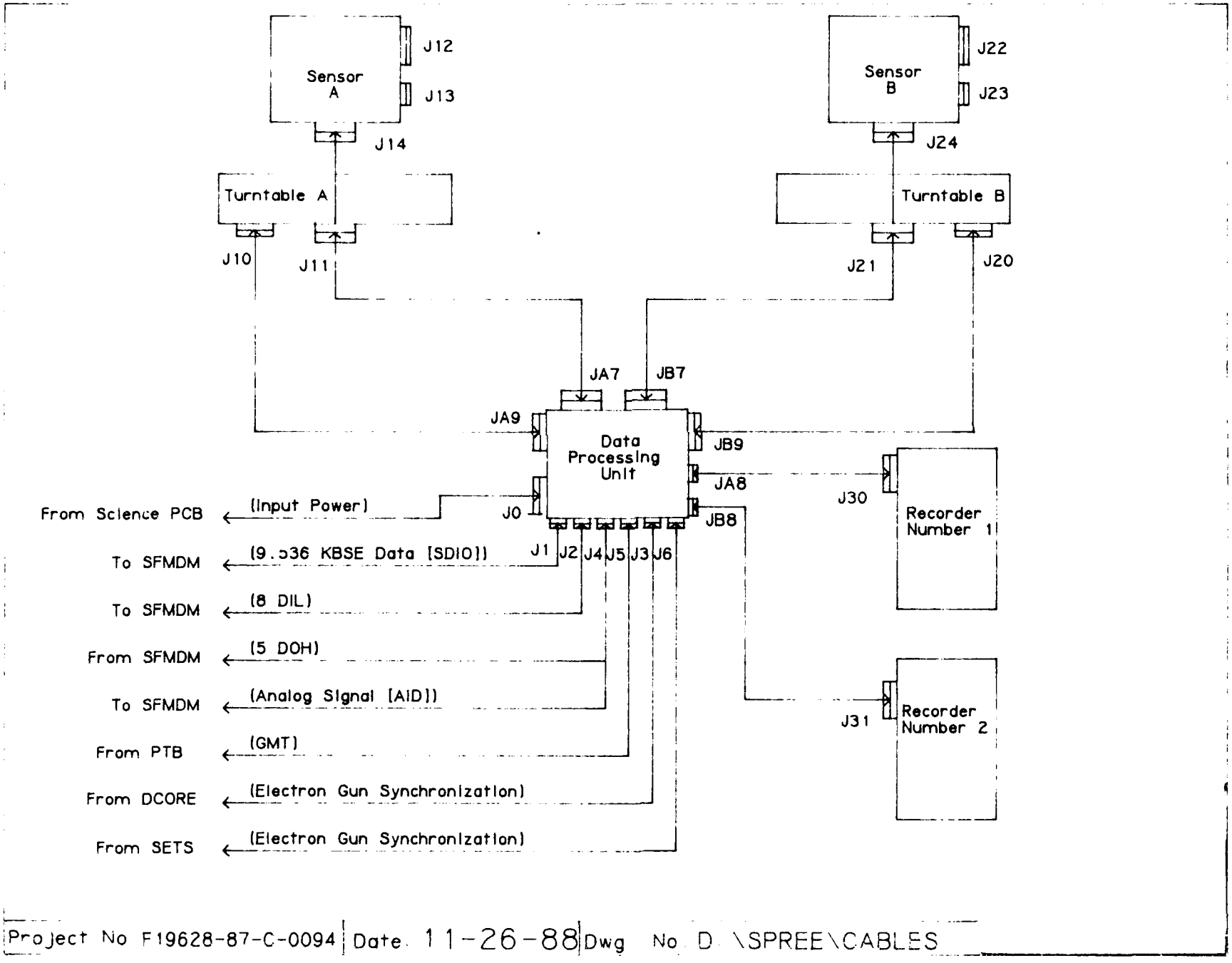
4.44
Pin 1
6.87
J9B
J9A
2.00
11.00

FIGURE QR5-5



Project No F19628-87-C-0094 | Date 11-26-88 | Dwg No D:\SPREE\CABLES

FIGURE QR5-6

ROTARY MOTOR TABLE DRIVE

Work completed for the past quarter consisted of determining and obtaining the proper size stepper motor and appropriate drive circuitry.

After determining torque and power requirements a Densei stepper motor was obtained and close coupled to the Harmonic Drive. The stepper motor / Harmonic Drive was then tested for torque characteristics using various discrete motor drive circuitry.

It was found that drive and motor efficiency could be greatly improved by using motor current chopping techniques. If current chopping is used, the average power consumed is greatly reduced. This decrease in power is accompanied by a decrease in motor torque. Fortunately, maximum torque is only required when the motor changes direction. The chopper control can be turned off during direction changes allowing for full torque/power when needed. By disabling the chopper only at these times efficient operation is maintained.

A motor control drive module manufactured by SGS Thomson was located and obtained for testing. The module replaces all of the discrete circuitry and has current chopping capabilities. The motor control drive module's electrical specifications and drive capabilities were tested and the results were excellent. Thermal tests on the module have not been completed.

SPREE
ROTARY TABLE
ASSEMBLY

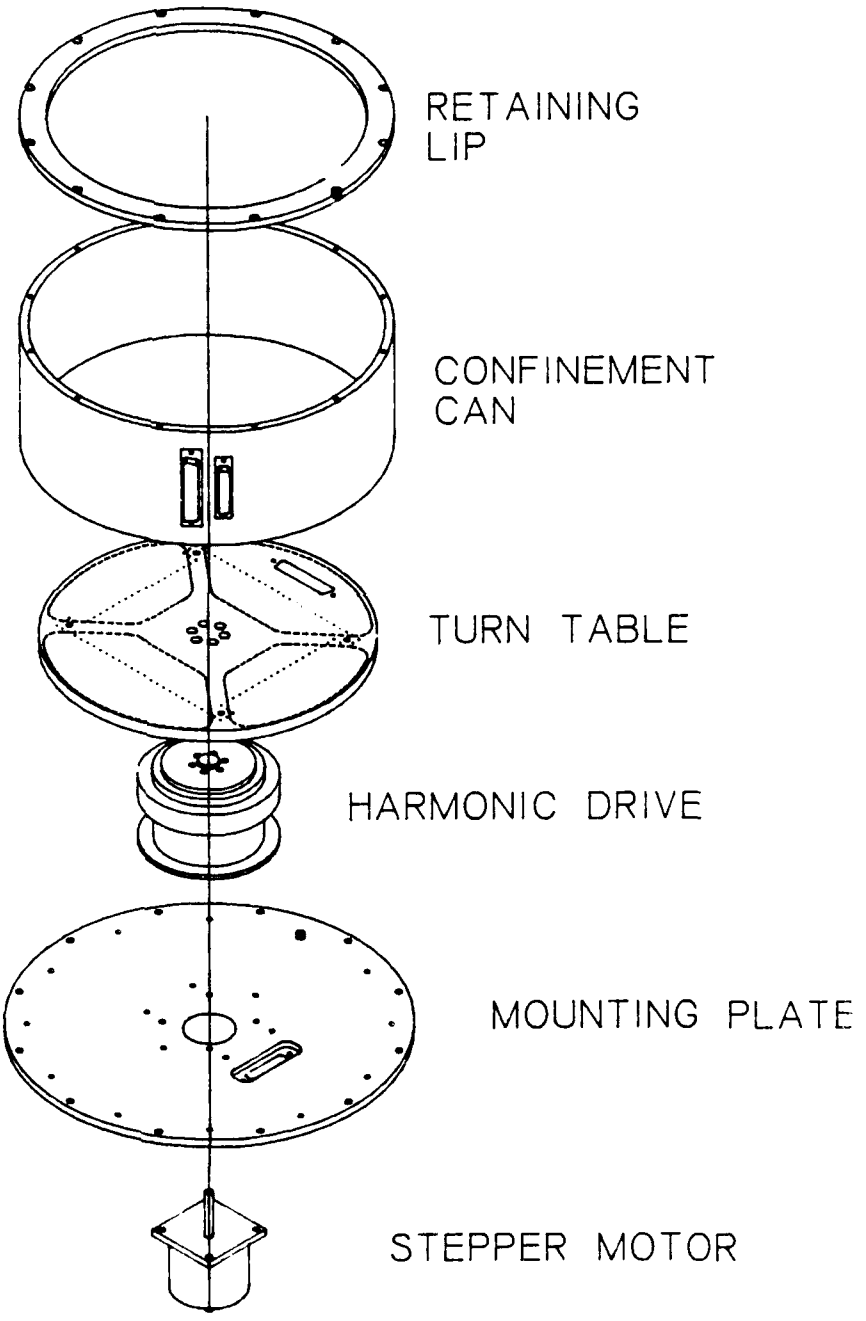
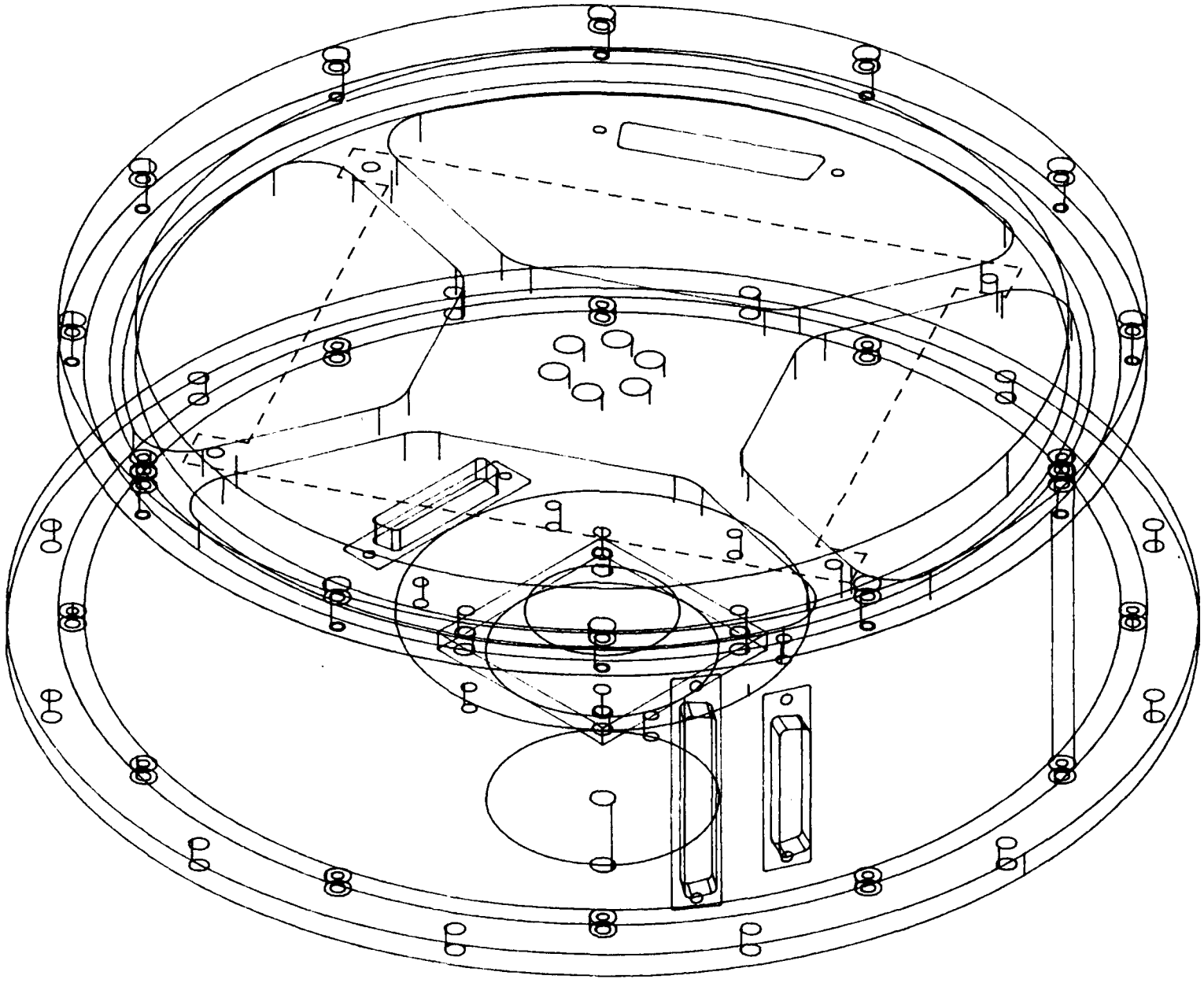


FIGURE QR5-7



ROTARY TABLE WIRE FRAME VIEW

FIGURE QR5-8

DATA PROCESSING UNIT FOR 270 DEGREE NESTED SENSORS

The major milestone of this quarter was the fabrication and testing of the CPU PC boards. Although only two boards are required for the final DPU, ten boards were manufactured to allow for testing and spares.

One board was socketed and filled with components for testing. Software was written to exercise the memory and the peripheral chips. Several problems surfaced involving noise immunity. These problems were corrected by replacing certain PC board tracks with appropriately routed wire which was epoxied to the board. More thorough testing needs to be performed to verify these fixes are satisfactory, but preliminary testing indicates that they are.

The design of the SPACE microcontroller boards is nearing completion, as is the SPACE CPU board and the accumulator board. The PC board layouts for all four of these boards will be completed next quarter.

In addition, the PC board layout for the backplane is nearly completed. The backplane, which is necessary for testing the inter-board communications, will be completed and fabricated once several design concepts are verified.

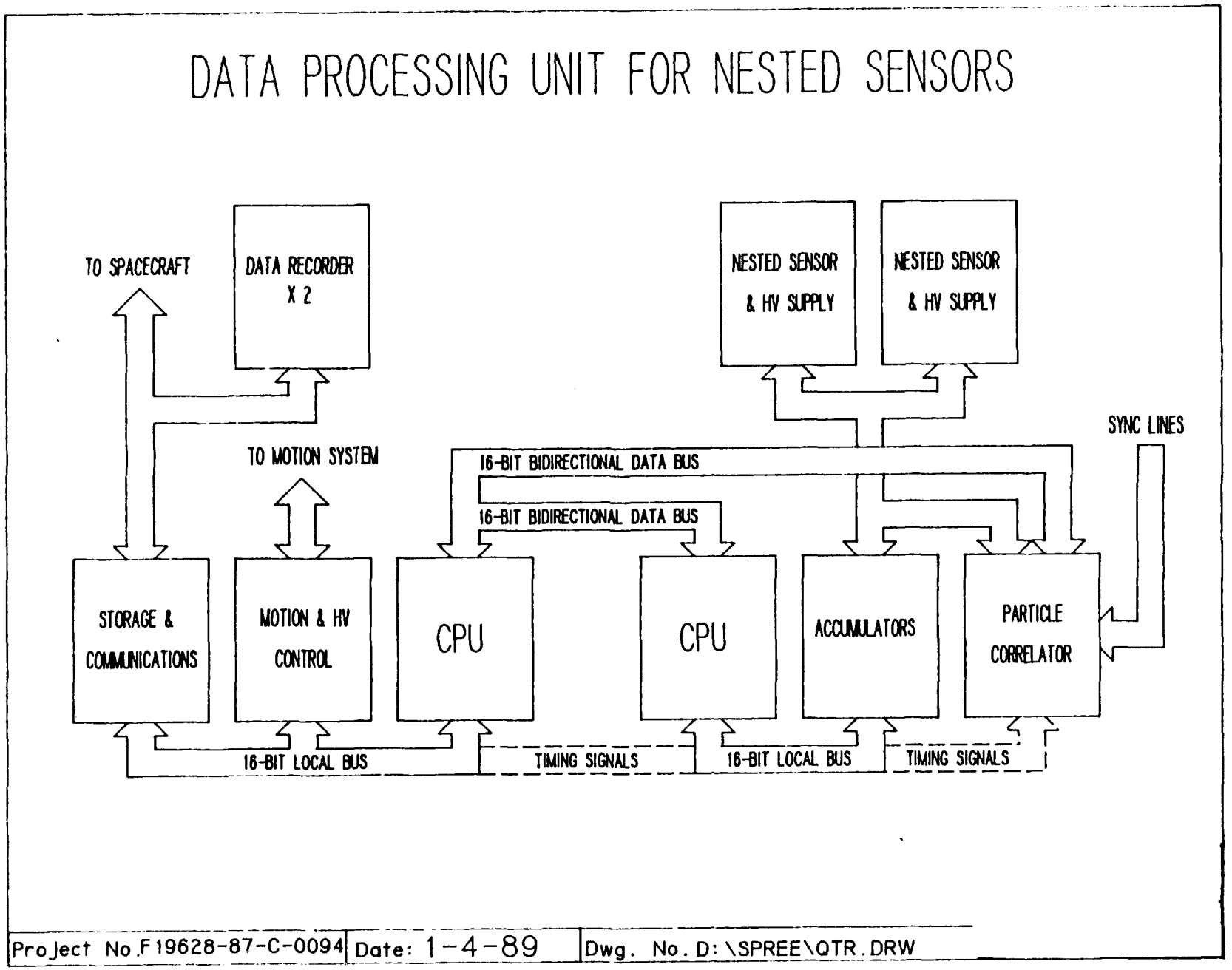

DATA PROCESSING UNIT FOR NESTED SENSORS
TO SPACECRAFT
DATA RECORDER X 2
NESTED SENSOR & HV SUPPLY
NESTED SENSOR & HV SUPPLY
SYNC LINES
TO MOTION SYSTEM
16-BIT BIDIRECTIONAL DATA BUS
16-BIT BIDIRECTIONAL DATA BUS
STORAGE & COMMUNICATIONS
MOTION & HV CONTROL
CPU
CPU
ACCUMULATORS
PARTICLE CORRELATOR
16-BIT LOCAL BUS
TIMING SIGNALS
16-BIT LOCAL BUS
TIMING SIGNALS
Project No.F19628-87-C-0094
Date: 1-4-89
Dwg. No. D:\SPREE\QTR.DRW

FIGURE QR5-9

SPACECRAFT PARTICLE CORRELATOR EXPERIMENT

Work of consultant: Dr. Paul Gough, Brighton, UK

A) Low Frequency Correlator

It has now been decided that the low frequency correlators will be best constructed with each one consisting of a 80C31 microcontroller with an associated EPROM plus 2k x 8 RAM. This option is significantly cheaper and easier to implement quickly than the previously selected EDH707C31, although taking up more board space.

Selection of the 80C31 has a number of implications:

1) The best crystal is 16MHz for fast enough software algorithms, and pulse counting.

2) The input pulses need stretching to 750nS.

3) Both timers T0 and T1 are needed for the ACF calculation: one as the pulse counter and the other to generate sample timing. This limits the correlator to CPU serial communications baud rate to either 0.25MHz, 0.5MHz or 1.33MHz.

B) High Frequency Buncher

The H.F. buncher is best to implement with 16-bit event counting because of the high event rate in low frequency ranges when the count rate is high. 16-bit wide RAM would directly match the 80C86 data bus.

C) Low Frequency Software

Most of the effort is now being spent designing the overall 80C31 correlator software. Particular attention is being paid to the time critical S/W modules.

SPREE FLIGHT RECORDER

The current revision of the prototype Flight Data Recorder (FDR) is designated FR30. Recent work has modified the recorder for the shuttle's vibration and thermal environments.

The following figure shows an enlarged thermal footprint over the previous design, FR20. The load on the cover bolts has also been reduced to provide a greater margin of safety.

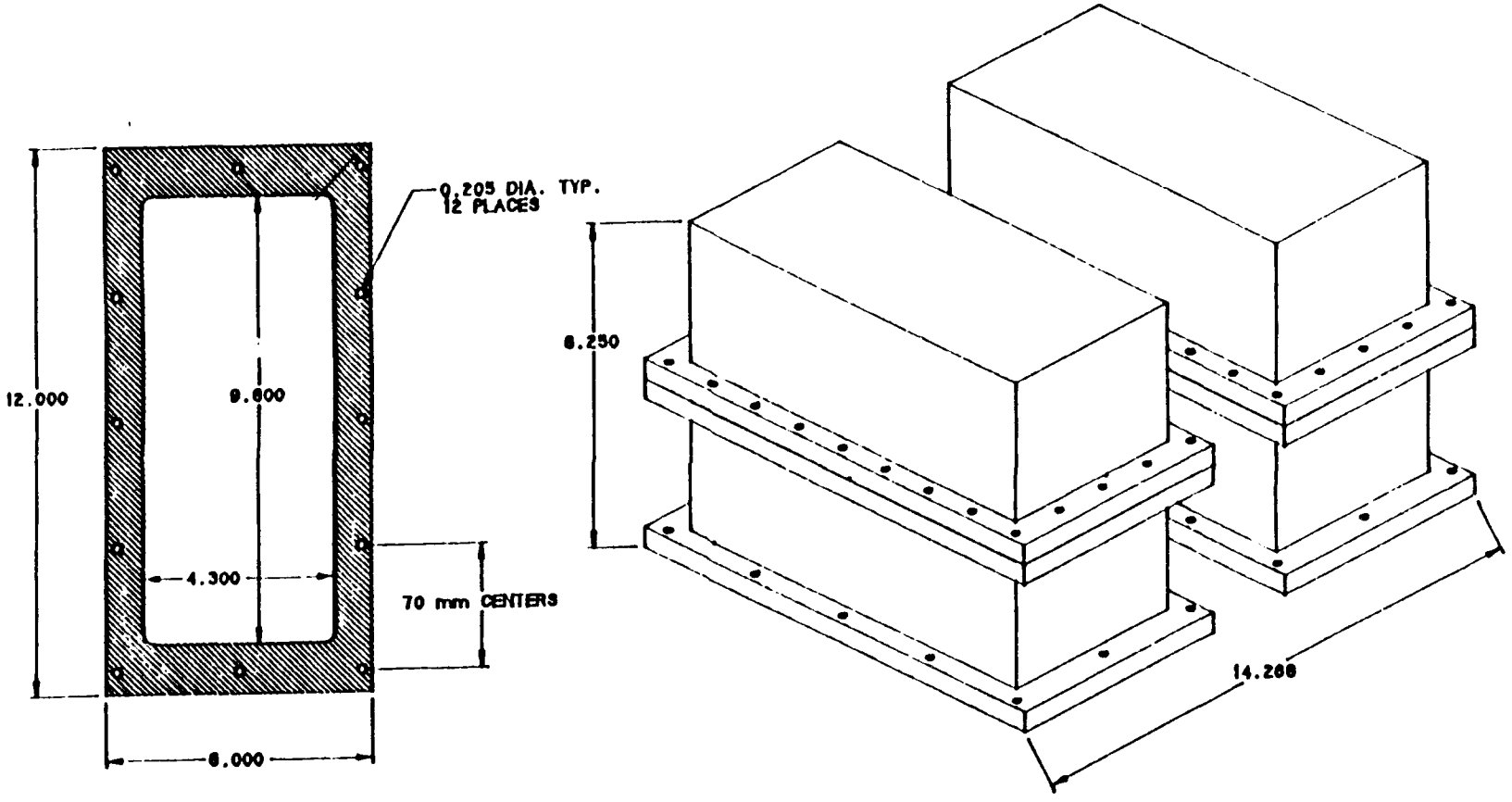
Internally, modifications to key mounting brackets have been planned. Vibration tests at AFGL detected a low frequency resonance in the tape transport assembly. A stiff support is being designed to raise this mode above 140Hz.

Electrically, the hermetic enclosure will be tied to signal ground so the use of an internal Faraday cage has been abandoned.

HIGH VOLTAGE OPTOCOUPLER

Prototypes of a 7kV optocoupler are presently under test. These units use a seven-junction stack of 1000V diodes illuminated by three LEDs. Results show greater than 100uA output current for 20mA of input current. Typical efficiencies are 12% with a CTR of 0.5%.

The prototypes are encased within a tubular epoxy casting. Future efforts will attempt to utilize a ceramic package for heat conduction purposes.



Footprint: 29.1 sq.in

PRDA-QR6

PROTOTYPE INSTRUMENTATION AND DESIGN STUDIES

AMPTEK, INC.
6 De Angelo Drive
Bedford, MA 01730

March 10, 1989

R&D Status Report no. 6
December 5, 1988 through March 4, 1989

Contract #F19628-87-C-0094

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ESD/PKR

Prepared for:

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Air Force Systems Command
United States Air Force
Hanscom Air Force Base, Massachusetts 01731-5000

NESTED HEMISPHERE ESA DESIGN

The manufacturer of the aluminum hemispheres used for deflection plates in the SPREE ESA (Q^3ESA) has corrected the fabrication error that was discovered in one hemisphere size. All of the necessary spheres are now on hand awaiting final machining.

An order was placed with Galileo Electro-Optics for ten (10) sets of trapezoidal shaped microchannel plates(MCP's). Delivery is scheduled during the next quarter (late May or early June).

The printed circuit art work for the MCP anode and MCP electrical mount was produced and these two boards are presently being manufactured. The MCP mechanical mount and holder are presently being machined from Kel-F. These parts must be completed so that they are available to Galileo to use for testing the MCPs. Galileo will use the flight mounts to test their MCPs prior to delivery to Amptek. This saves the time and expense of manufacturing special test fixtures and also minimizes handling of the very fragile MCPs.

The Q^3ESA housing was revised to simplify its fabrication. Changes have also been made to accommodate the MCP thickness as ordered from Galileo. Machine drawings are being prepared so that the ESAs may be built.

The thermal modeling of the Q^3ESA was completed. The design qualification lower temperature limit was lowered to -30 C. It is not felt that this will present a problem. The Q^3ESA housing will be nickel plated and covered with a thermal blanket. except for the aperture plate and anode cover. These surfaces will be painted with a flat black conductive material.

Several changes have been made to the SPREE DPU to accommodate a maturing design. The connectors going to the FDR have been moved to the top of the DPU so that they may be mounted on the PC card that interfaces the FDR. This avoids passing high speed data on the mother board.

The connector holding the DOH (Digital Output High) lines has been moved to the power supply board since the DOHs will be used for power control on the SPREE.

The connector housing the SDIO lines to the SFMDM has been enlarged to 25 pins to allow the possible interface of up to three SDIO interfaces. At some part of the mission we are supposed to be able to use the 8 Kbit data line used by the Tethered satellite until deployment. At present, where this extra data capacity comes from is not clear. The 25 pin configuration should be able to handle almost any scenario.

A Critical Design Review (CDR) for the SPREE was held in late December 1988. The results of the CDR are still being closed, but should be over by the end of March. Fabrication has begun on some of the assemblies.

DATA PROCESSING UNIT FOR 270 DEGREE NESTED SENSORS

Buying parts was one of the major activities for this quarter. Nearly all of the flight parts for the DPU and for the particle correlator have been purchased. All purchasing of flight parts will be completed during the third quarter.

Telemetry allocations and formatting were determined in an Amptek/AFGL meeting. It was decided that the SPREE instrument will record 16,000 bytes of data per second, to be divided between the SPREE DPU and the particle correlator based on the operating mode. Preliminary major and minor formats were developed, including housekeeping data and time tagging. These formats will be finalized during the upcoming quarter.

The accumulator board went through a second layout to accommodate various design changes. It will be manufactured early in the third quarter.

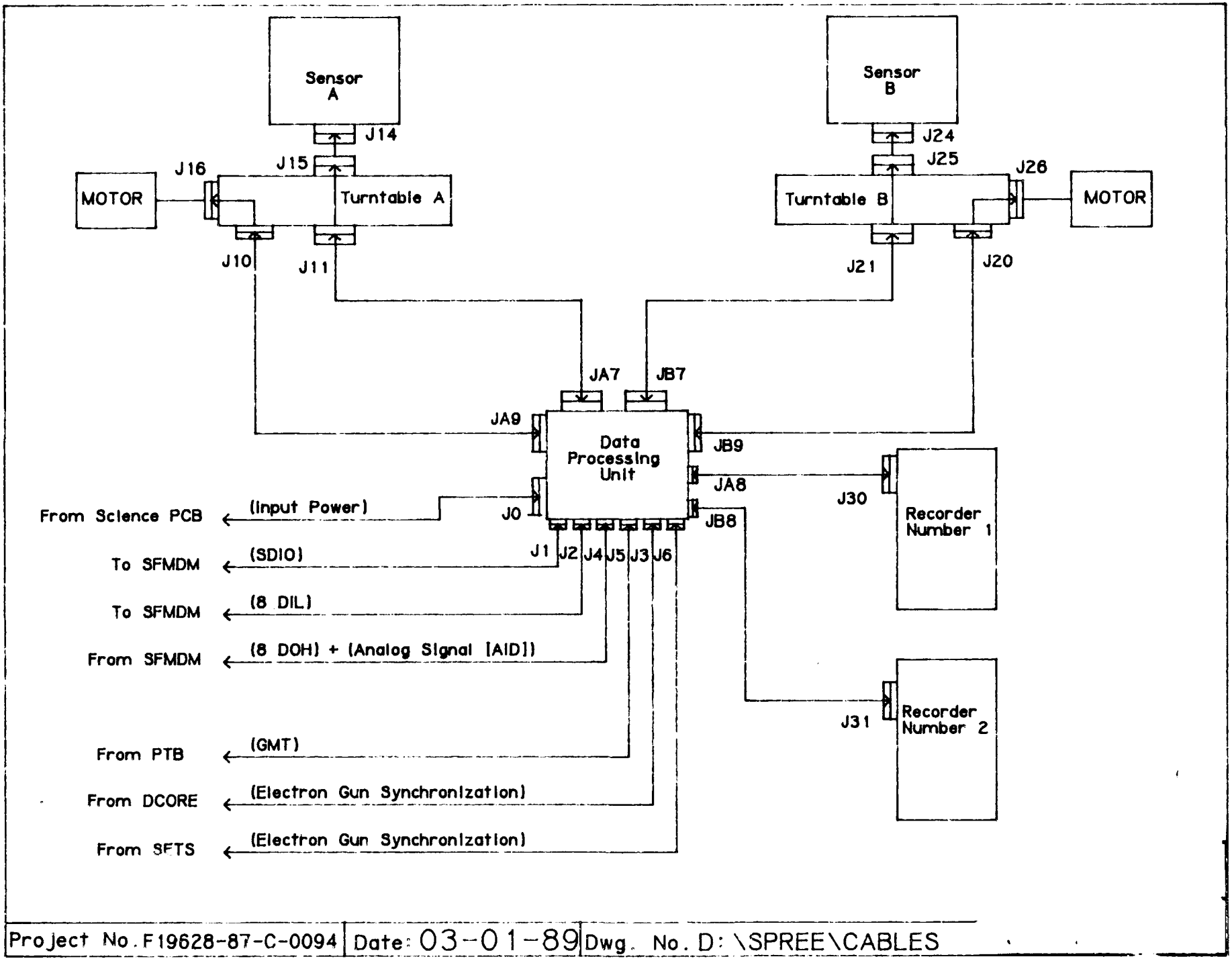
The main section of the recorder interface was breadboarded and satisfactory results were obtained. The remainder of the interface will be tested and the board layout will be completed near the middle of third quarter.

The layout of the back plane was put on hold until some design issues were resolved. These issues included the number and location of the analog signals, the location of the recorder connectors, the type of motor controllers to be used, and a review of the power distribution and control system. The first revision back plane will be fabricated this quarter after a complete resolution of these questions.

A second revision of the CPU board will probably be performed late this quarter. It will incorporate the means to easily modify the board according to whether it will be used as the primary CPU, secondary CPU or the SPACE CPU. It will also incorporate several minor changes.

The MCU boards for the particle correlator will be ready for layout once the operation of a prototype module has been verified by Dr. Paul Gough.

The high-frequency buncher board for the particle correlator still requires a fair amount of design work. It is complete conceptually, and the memory map of the board has been assigned, but the actual implementation of the modules in programmable logic has not been completed. The design of this board is scheduled to be completed late this quarter.



Project No. F19628-87-C-0094 | Date: 03-01-89 | Dwg. No. D:\SPREE\CABLES

SPREE DPU HOUSING

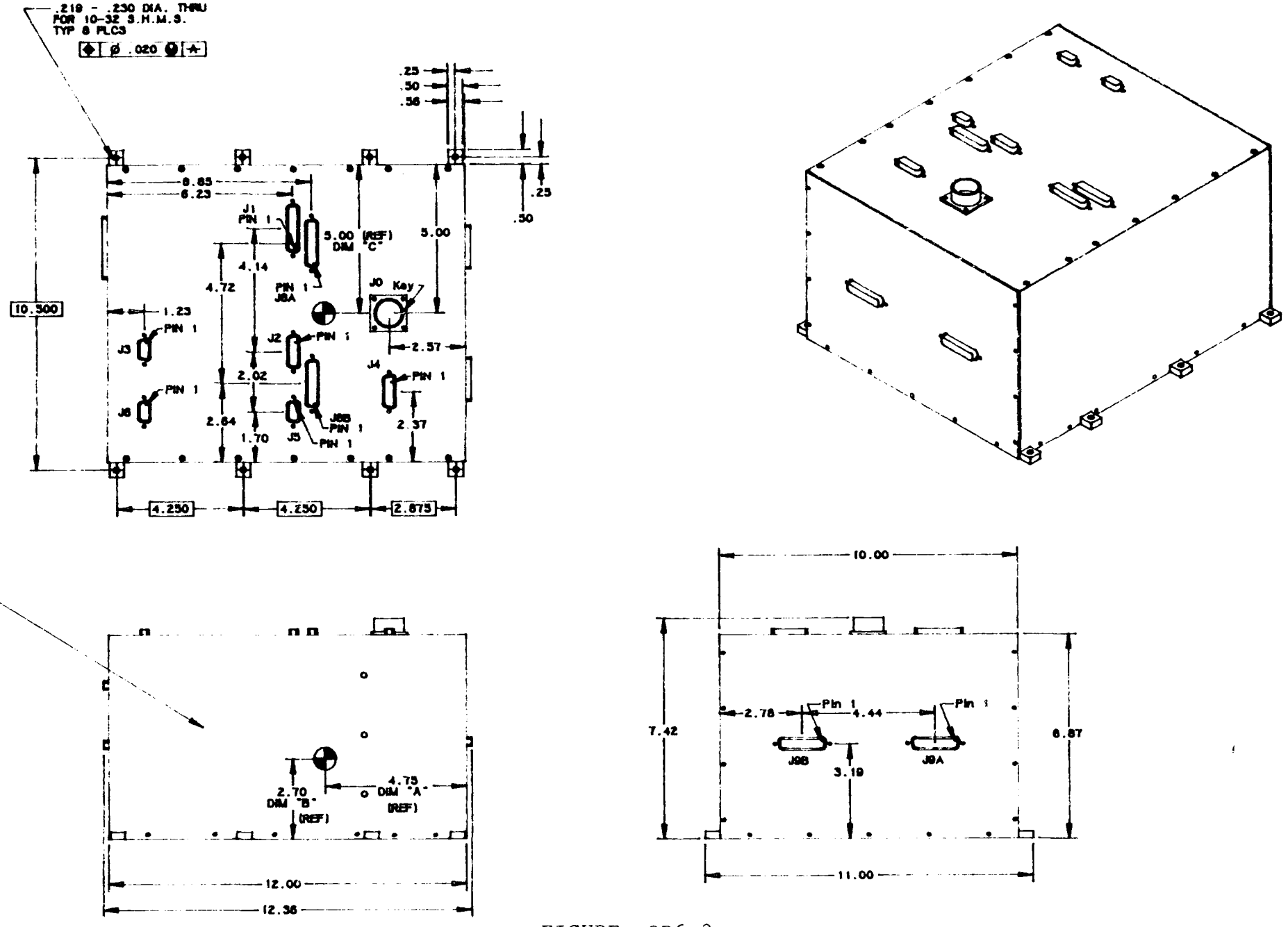


FIGURE QR6-2

PARTICLE CORRELATOR

Work of consultant: Dr. Paul Gough, Brighton, UK

A) Mission Planning

At a recent meeting with Amptek & AFGL personnel, a timetable for development and testing was decided. Amptek will provide engineering models late March/April for software development in U.K. Developed software will be returned for initial flight unit tests about June, with integration of the flight units taking place in late summer. Instrument fabrication should be complete by December 1989.

B) Documentation

A full description of the SPREE particle correlator is in the process of being drafted, to follow immediately after this report. This includes operation modes and scientific aims.

C) Standard Operating Cycle

In common with the other experiments a standard operating cycle (SOC) has been defined. This is based on the fact that the SPREE sensors are being rotated through 180 degrees every 30s. The analyzers are either swept once per second or ten times per second. For each 30s rotation three zones are selected for analysis. Over a 90s period zones 1,4,7 are studies for 30s; then zones 2,5,8; then zones 3,6,9. Alternate 90s periods start off one zone different (2,5,8; 3,6,9; 4,7,10) to give coverage of all 10 zones. The high frequency correlator has three frequency ranges (10MHz, 2.5MHz & 625kHz). These are cycled through over 3 x 90s.

The complete standard operation cycle is therefore 270s. This mode is unaffected by the choice of 1 or 10 energy sweeps per second. That selection only changes the quantity of data transmitted and the summation periods.

SPREE FLIGHT RECORDER

Development of the FDR's bridge controller (BC) is underway. This two-board electronic package will be merged with the tape transport mechanism and command data flow with the DPU. Environmental heating is also controlled by the BC. Hardware breadboarding is nearly complete and software development has begun. The prototype FDR should be interfaced to an IBM-PC for debugging within three months.

HIGH VOLTAGE OPTOCOUPLER

Sixteen prototypes of a white epoxy optocoupler have been built. Solvent/catalyst interaction with the polyimide passivation promoted leakage in the high voltage section of some devices. Further contamination and thermal cycle tests are being planned with other encapsulations. The development of the optocoupler will be complete when a suitable high purity encapsulation is found.

SMARTFLEX INTERFACE.

Revised schematics have been completed for interfacing SPREE to Space Lab. Further investigation is required before finalizing the serial data channel.

The SPREE payload will be flown on SFMDM's maiden voyage. Ongoing discussions between Amptek, Martin Marietta, and McDonnel Douglas will finalize the interface specification as defined in SPAH Appendix G. Prototype assembly will commence soon after.

The recent acquisition of a GSE for SPREE will enable emulation of the SFMDM. SPREE will therefore be able to calibrate and verify operation in an environment similar to that of Space Lab.

ROTARY MOTOR DESIGN

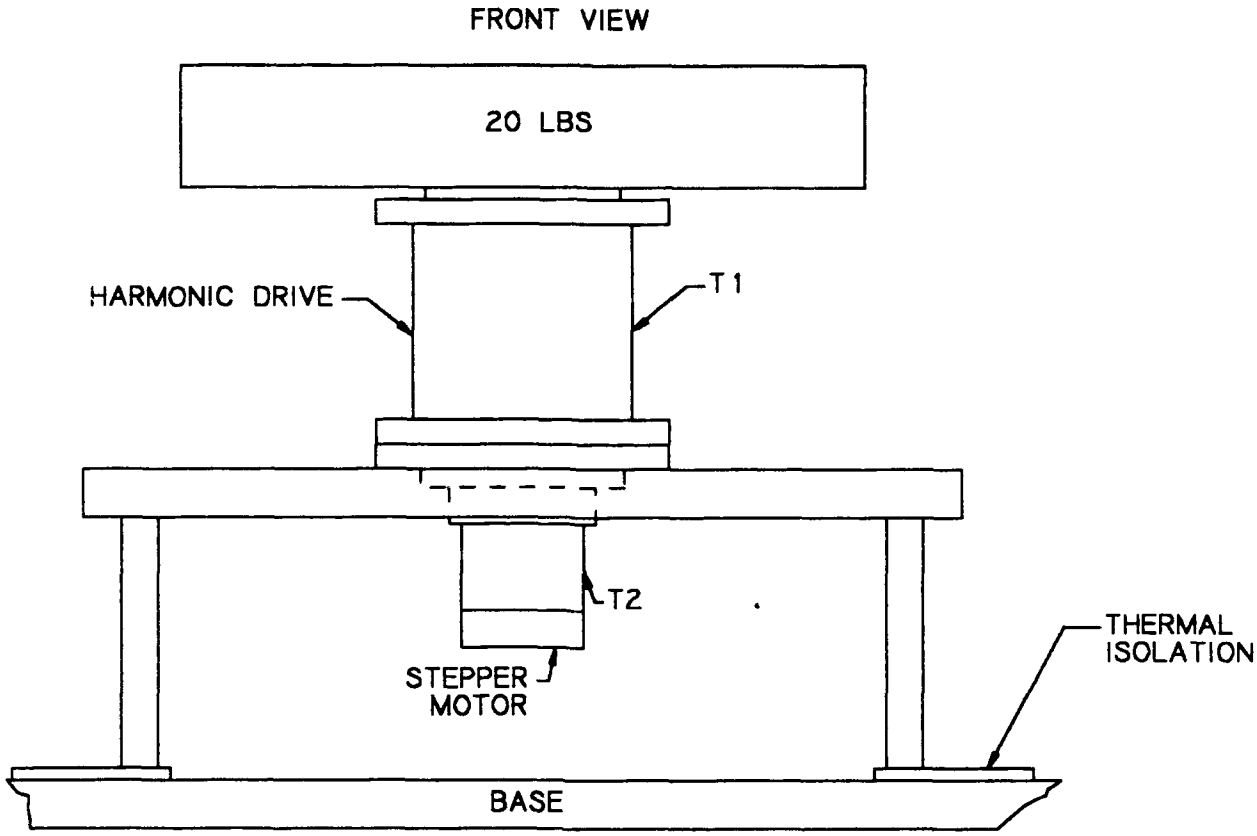
Work continued this quarter on optomizing the motor/harmonic drive/motor control. The SGS-Thomson control module was tested and proved to work better than any previously attempted discrete circuit. Unfortunately the SGS-Thomson controller is only available in a commercial version that cannot meet military temperature ranges or be compatible for vacuum out gassing specifications.

A Densei steppermotor and a Harmonic drive were vacuum tested for thermal characteristics. The motor was close coupled to theHarmonic drive and a 20 pound load was used on the drive. This assembly was then continuously operated in a vacuum of 140 microns while thermal data was taken. The SGS-Thompson motor drive module was used to power the drive unit during this test. The module was also evaluated for its thermal characteristics in vacuum.

Using the SGS-Thomson module performance as a bench mark, a new discrete circuit was designed and tested. At present the RTMD assembly delivers 3.1 foot-pounds of torque using approximately 2 watts of power. The simplified unipolor drive circuit incorporates current chopping. This circuit's motor drive capabilities were tested. The unipolor drive circuit will replace the more complex bipolor design previously used. The unipolor design offers equivalent drive capabilities with a reduced parts count. The motor voltage may also be increased to allow reduced operating current which should decrease the probability of EMI problems. The parts used in the unipolor design are readily available in military temperature versions. The performance of the RTMD meets or exceeds design goals and will meet mission requirements.

Optical detectors used for position sensing of the rotary table have been ordered. Next quarter will be spent ordering flight hardware and re-conditioning the motors and harmonic drives for vacuum operation. This includes disassembly, cleaning and gas relieving trapped volumes, and lubricating with a flight approved low out gassing lubricant. Reassembly and thermal vacuum testing will follow.

VACUUM TEST SETUP



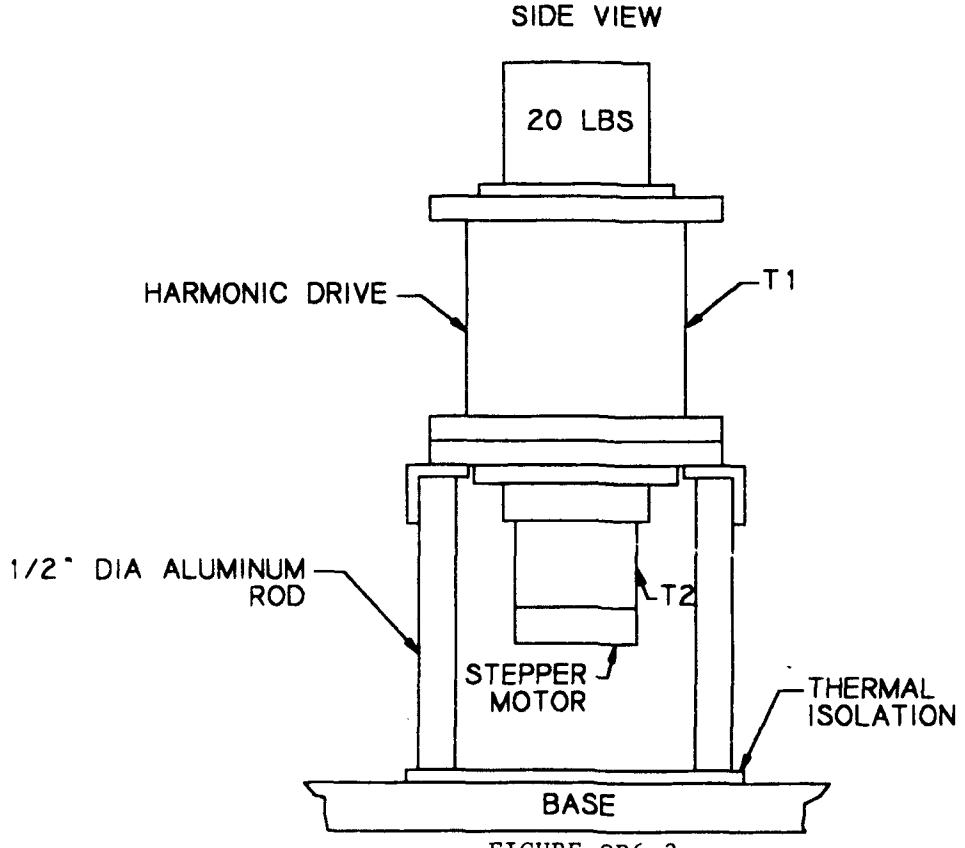


FIGURE QR6-3

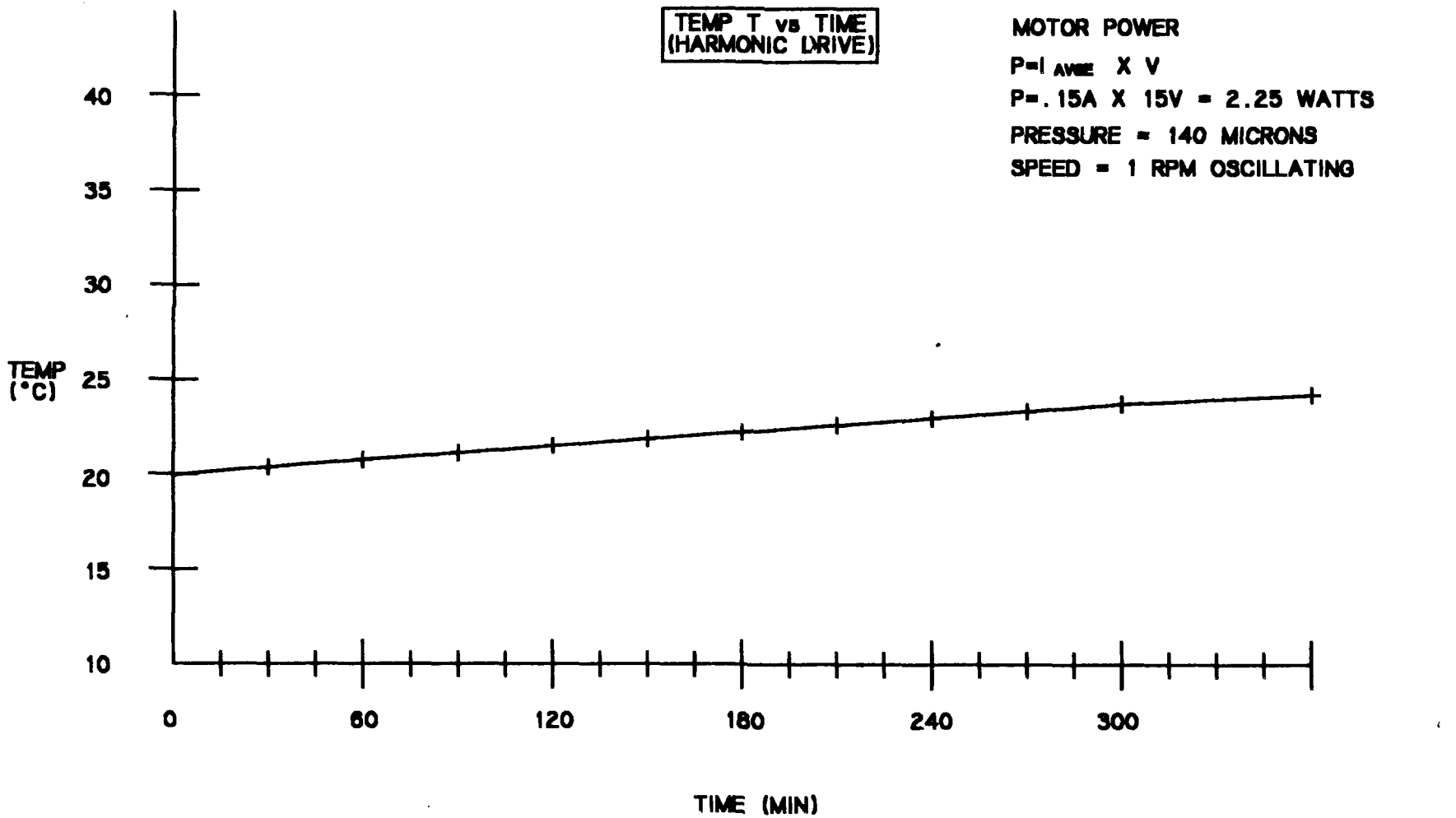

TEMP T vs TIME
(HARMONIC DRIVE)
MOTOR POWER
P=I AVGE X V
P=.15A X 15V = 2.25 WATTS
PRESSURE = 140 MICRONS
SPEED = 1 RPM OSCILLATING
TEMP (°C)
40
35
30
25
20
15
10
0
60
120
180
240
300
TIME (MIN)

FIGURE QR6-4

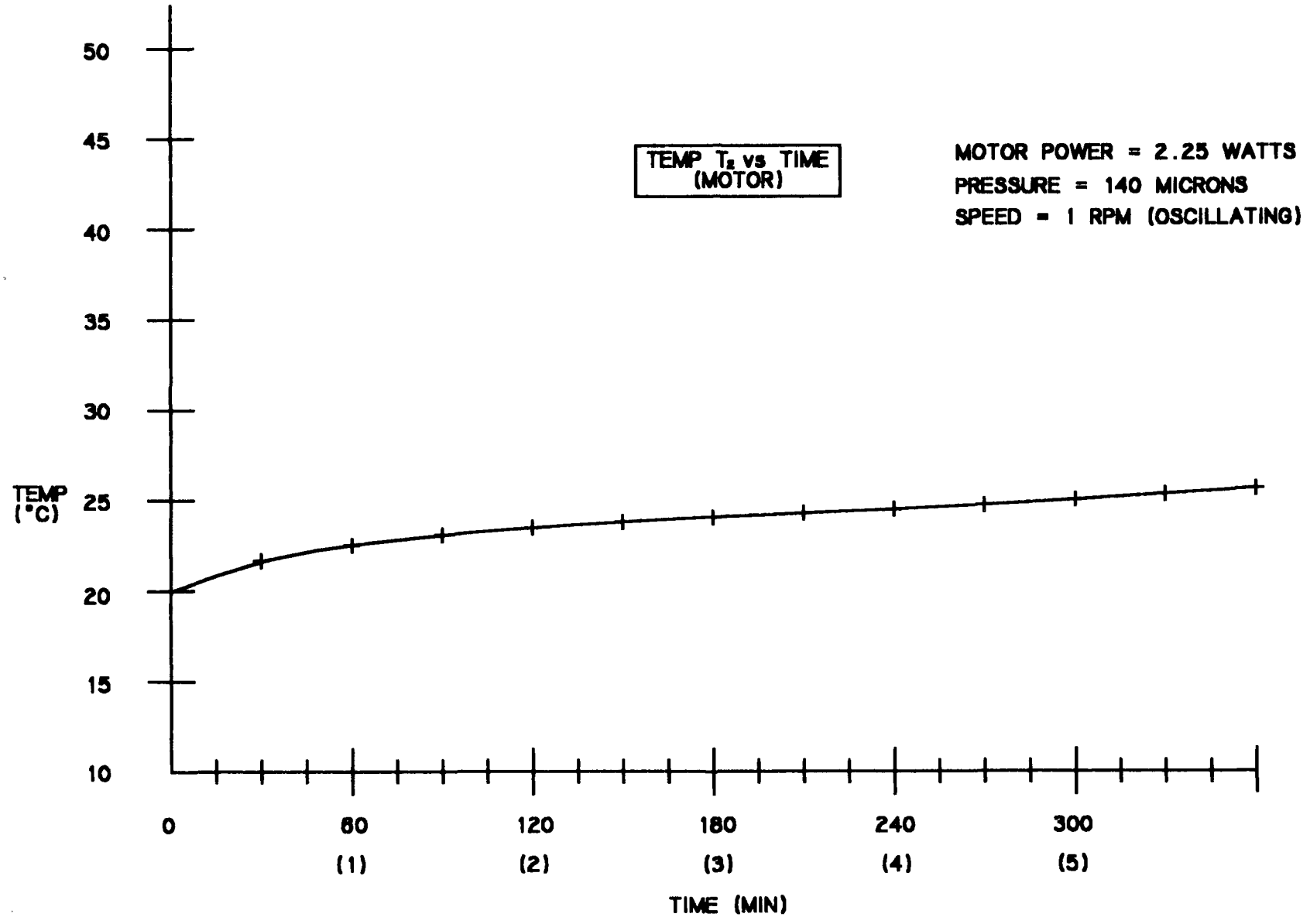
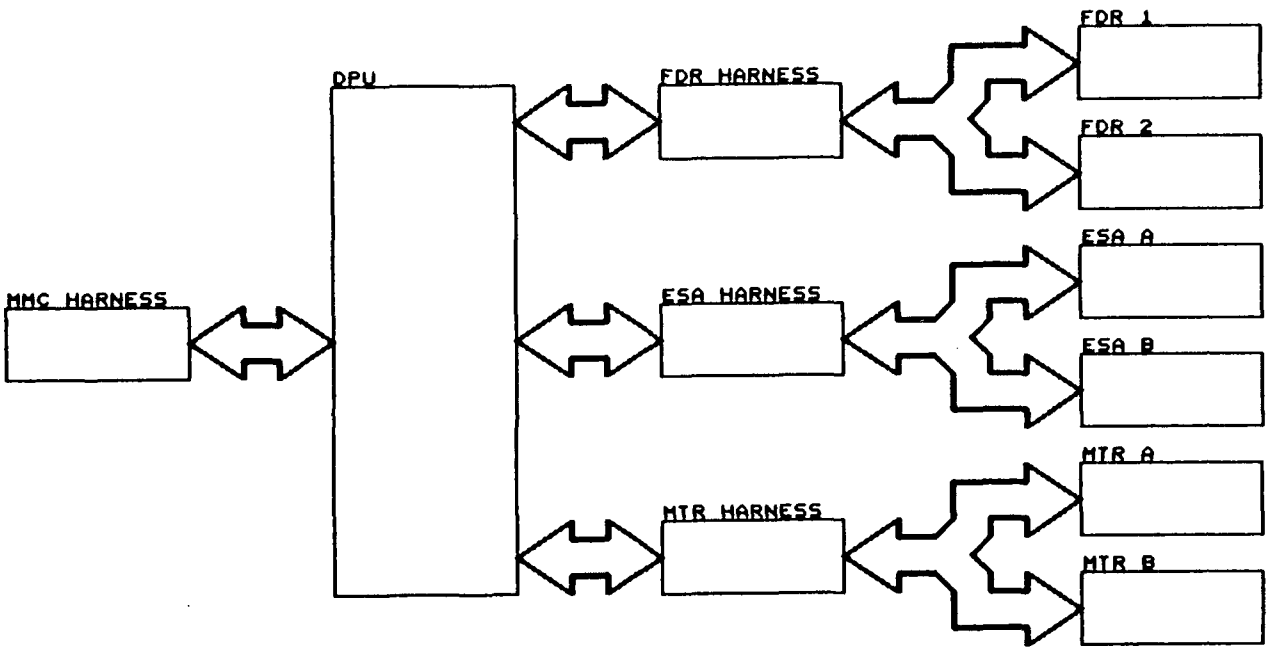

TEMP T_z vs TIME
(MOTOR)
MOTOR POWER = 2.25 WATTS
PRESSURE = 140 MICRONS
SPEED = 1 RPM (OSCILLATING)
TEMP (°C)
50
45
40
35
30
25
20
15
10
0
60
120
180
240
300
(1)
(2)
(3)
(4)
(5)
TIME (MIN)

FIGURE QR6-5

The following attached figures document the current status and design of all parts of the SPREE experiment. Included is a preliminary parts list. This data base will be expanded and corrected as the design and fabricated experiment matures. These sheets represent the status at CDR.

SHUTTLE POTENTIAL & RETURN ELECTRON EXPERIMENT BLOCK DIAGRAM



PAGE

DPU
- DIL INTERFACE
- DCORE/SETS INTERFACE
- DOH INTERFACE
- AID INTERFACE
- FDR INTERFACE
- BACKPLANE
- POWER SUPPLIES
- SDIO INTERFACE

ESA HARNESS
MTR HARNESS
MMC HARNESS
FDR 1
FDR 2
ESA A
- HV SUPPLY

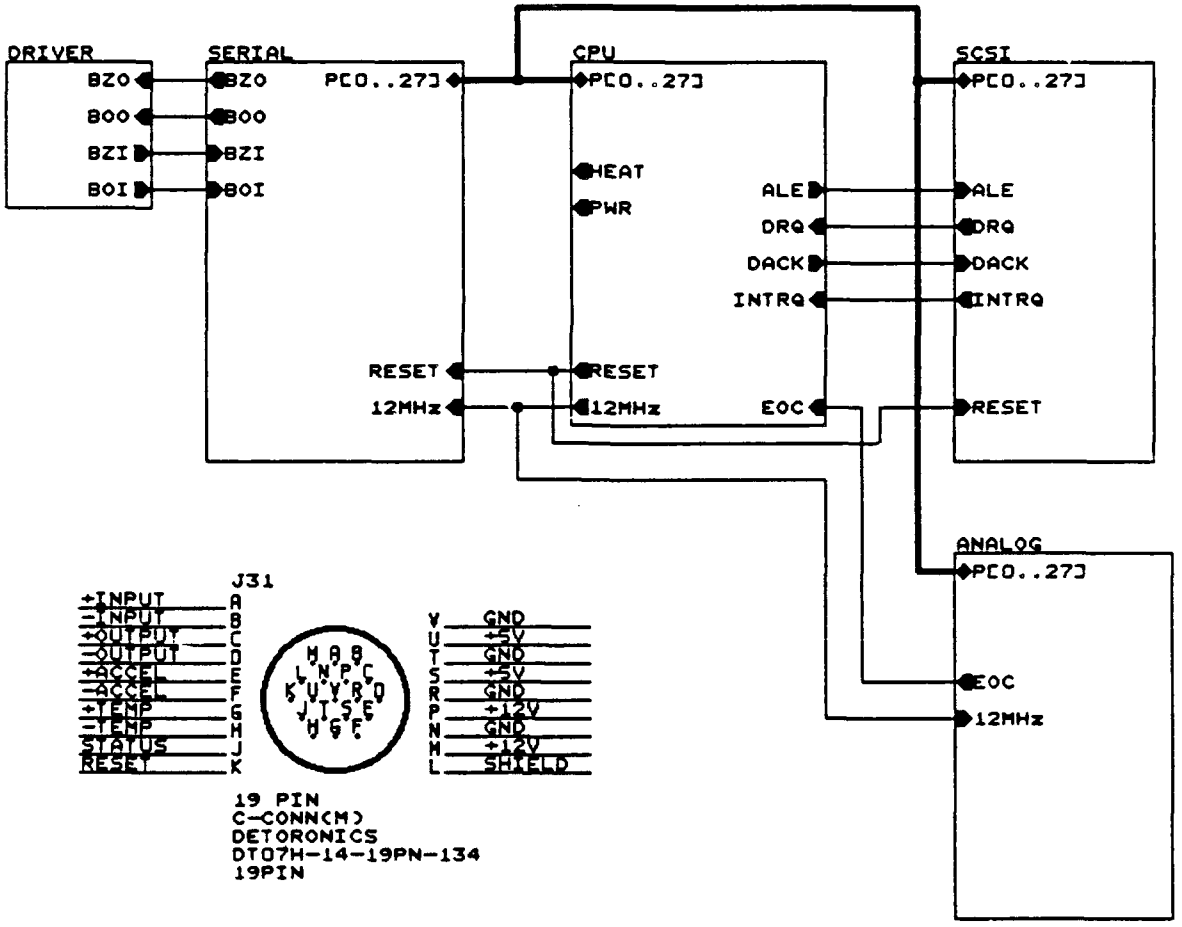
ESA B
- HV SUPPLY

MTR A
MTR B
FDR HARNESS

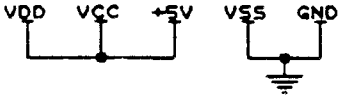
FIGURE QR6-6

AMPTEK, INC. 6 DE ANGELO DRIVE BEDFORD, MA 01730 617/275-2242	
Title SHUTTLE POTENTIAL & RETURN ELECTRON EXP.	
Size A	Document Number REV A
Date: March 8, 1989	Sheet 1 of 43

ADDRESSING	A15	A14	A13
uC <> RAM	0	0	0
uC <> ANALOG	0	0	1
uC <> SERIAL	0	1	0
uC <> SCSI	0	1	1
SERIAL > RAM (DMA)	1	0	0
RAM > SERIAL (DMA)	1	0	1
RAM > SCSI (DMA)	1	1	0
SCSI > RAM (DMA)	1	1	1

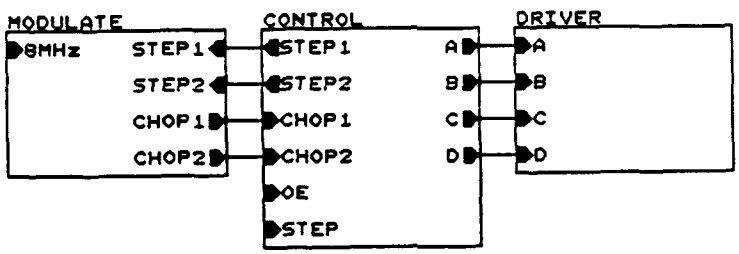


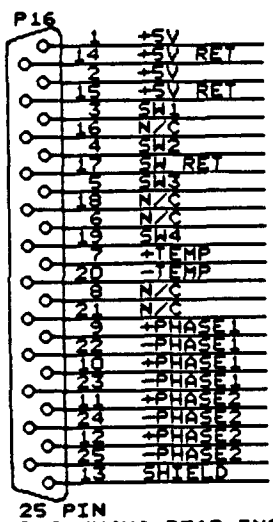
19 PIN
C-CONN(M)
DETORONICS
DT07H-14-19PN-134
19PIN



AMPTEK, INC.		
Title: ~~BRIDGE CONTROLLER~~ FDR 2		
Size: D	Document Number:	REV
Date: March 7, 1989	Sheet 2 of 43	

FIGURE QR6-7

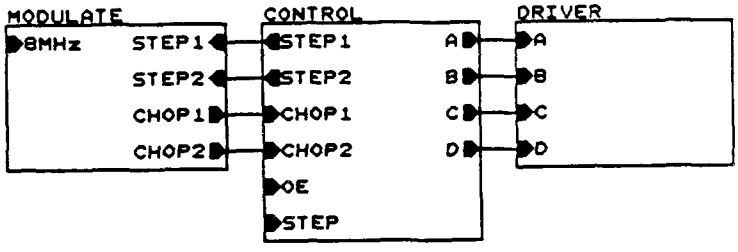


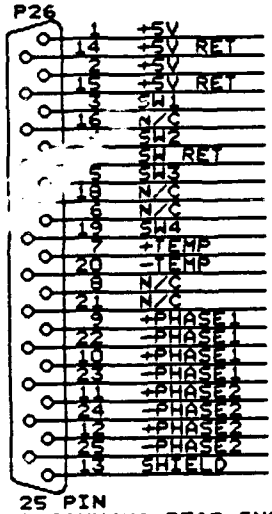


25 PIN
D-CONN(M) REAR INS CABLE
CANNON
DBMA-25P-NMB-K56
25PIN

FIGURE QR6-8

AMPTEK, INC.		
Title: RAMP CONTROLLER		
Size: D	Document Number:	REV:
Date: March 7, 1989	Sheet 8 of 43	





25 PIN
D-CONN(M) REAR INS CABLE
CANNON
DBMA-25P-NMB-K56
25PIN

FIGURE QR6-9

AMPTEK, INC.		
Title: RAMP CONTROLLER		
Size: D	Document Number	REV
Date: March 7, 1989	Sheet 12 of 43	

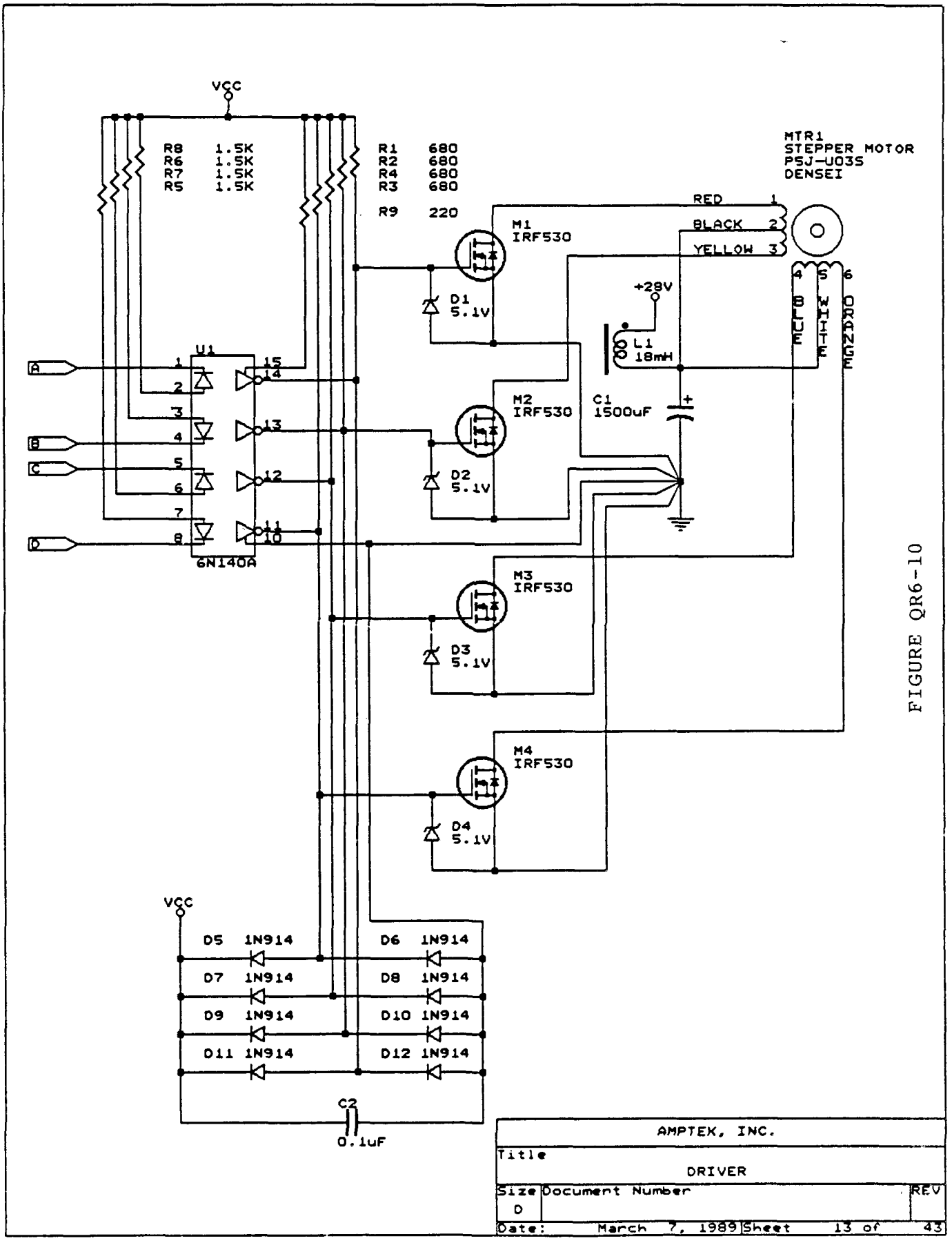


FIGURE QR6-10

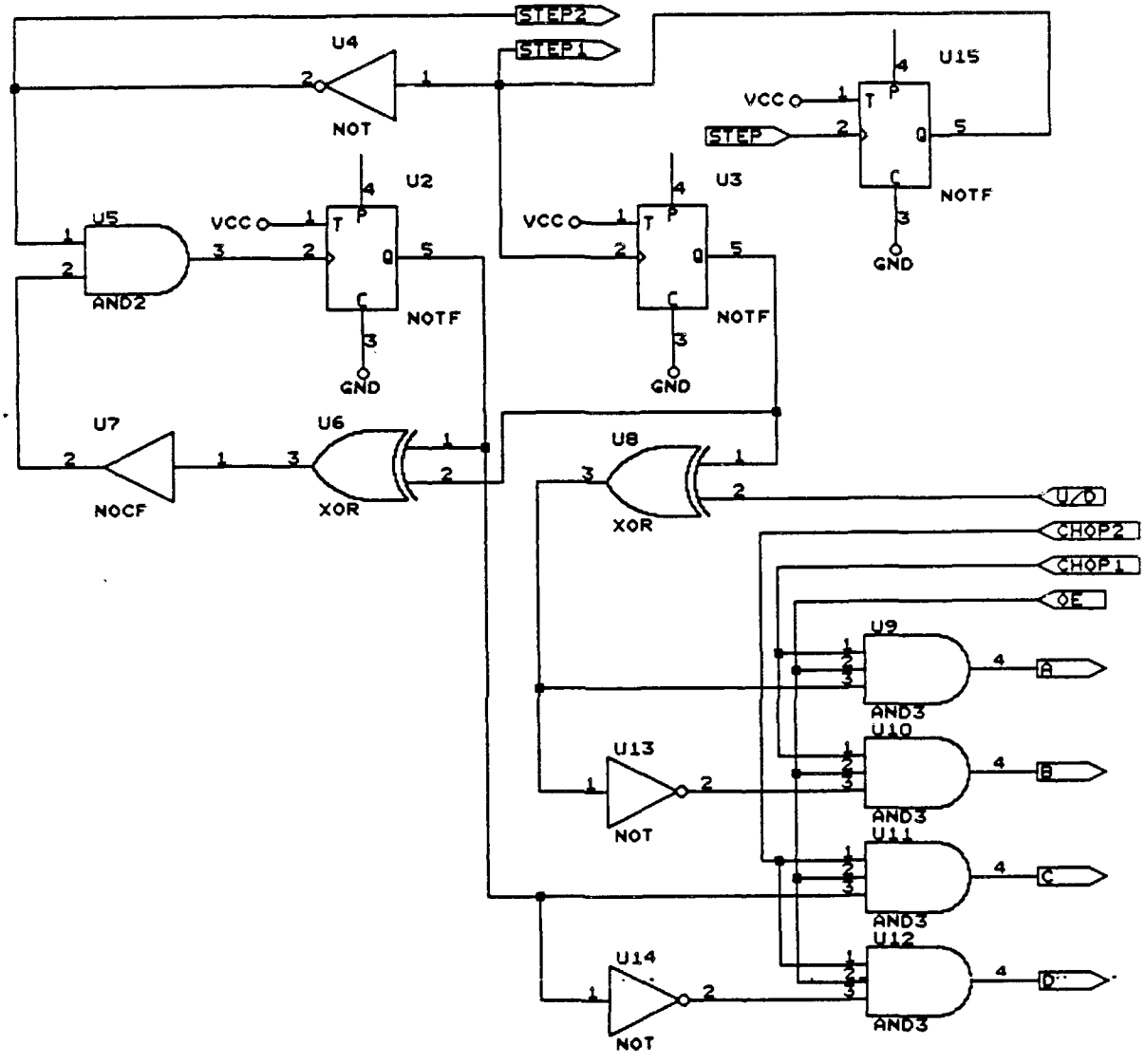


FIGURE QR6-11

AMPTEK, INC.		
Title: CONTROL		
Size: D	Document Number	REV
Date: March 7, 1989	Sheet 14 of 43	

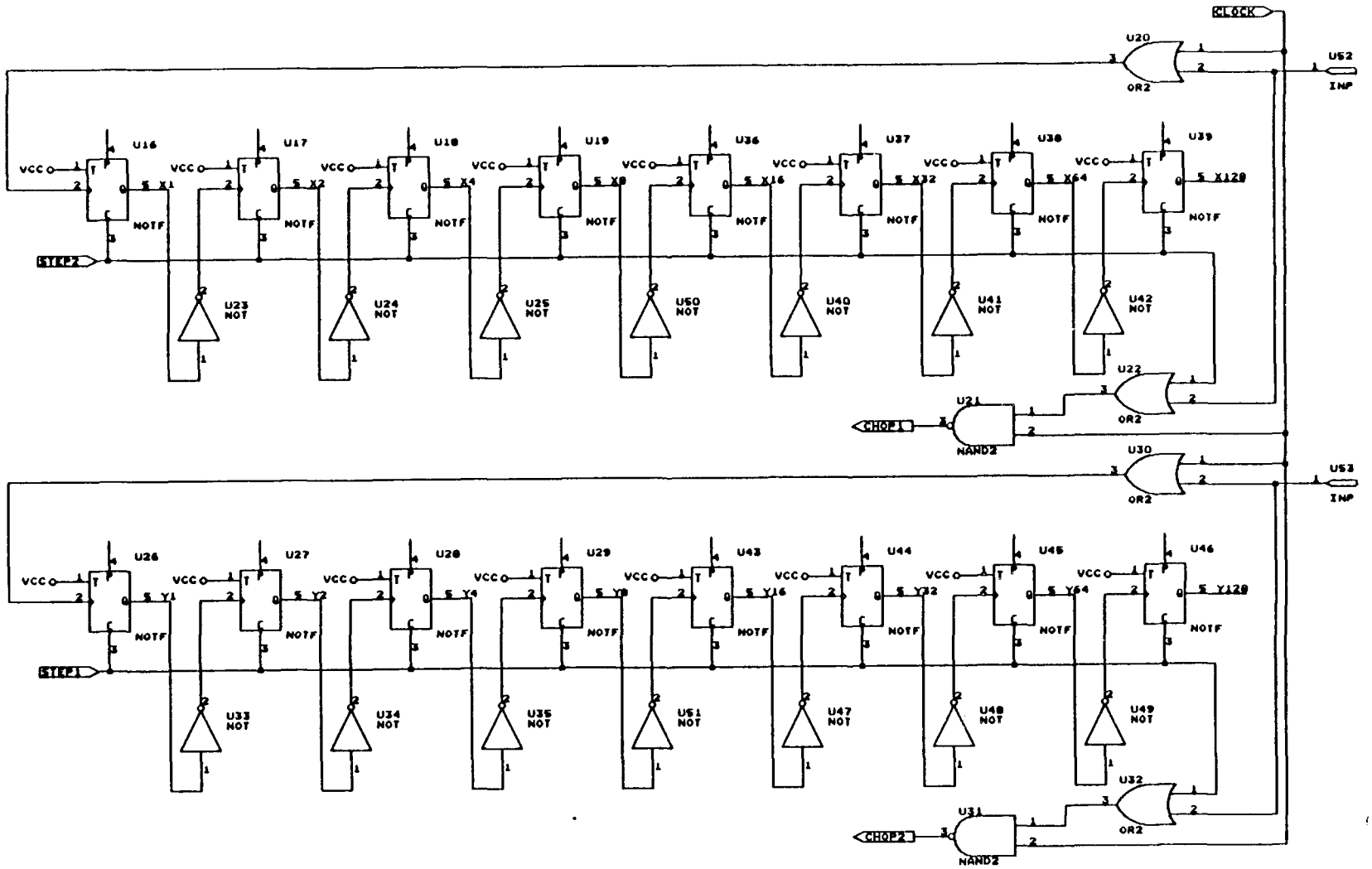


FIGURE QR6-12

CHOP IS INHIBITED BY HOLDING CLOCK LOW

AMPTEK, INC.		
Title: MODULATE		
Size: B	Document Number:	REV:
Date: February 24, 1989	Sheet: 15 of 43	1

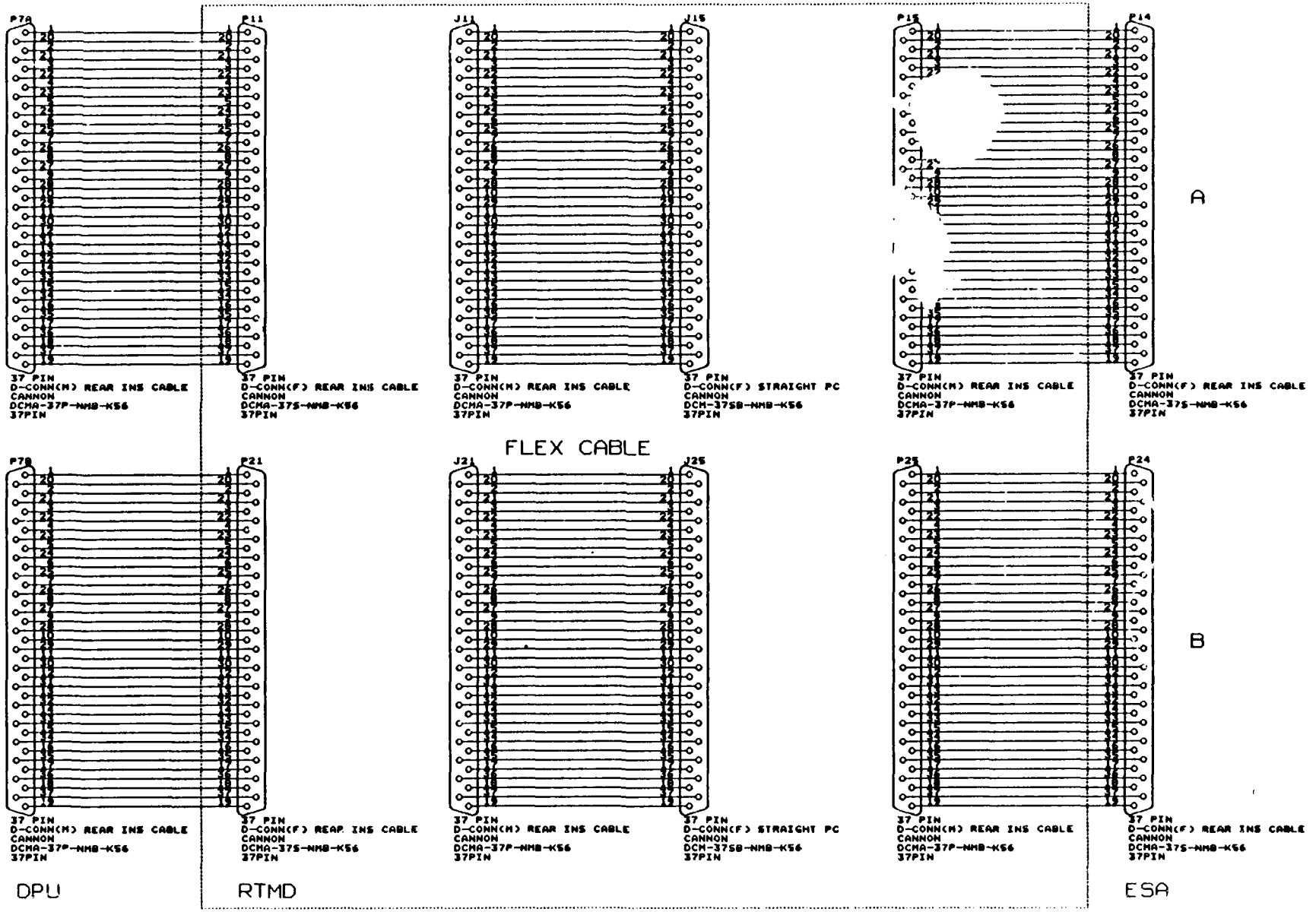


FIGURE QR6-13

AMPTEK, INC.	
Title: ESA HARNESS	
Size: B	Document Number: REV
Date: March 1, 1989	Sheet 16 of 43

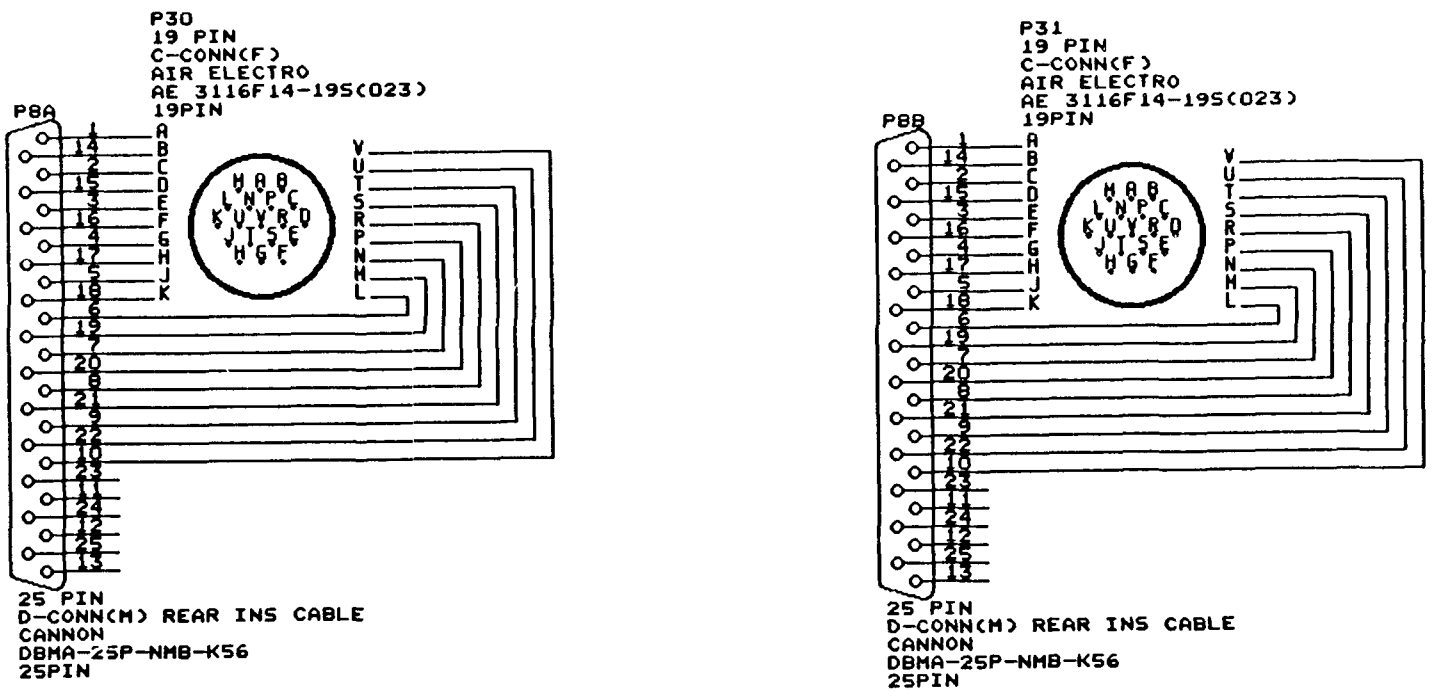


FIGURE QR6-14

AMPTEK, INC.		
Title: FDR HARNESS		
Size: A	Document Number:	REV
Date: March 2, 1989	Sheet 17 of 43	

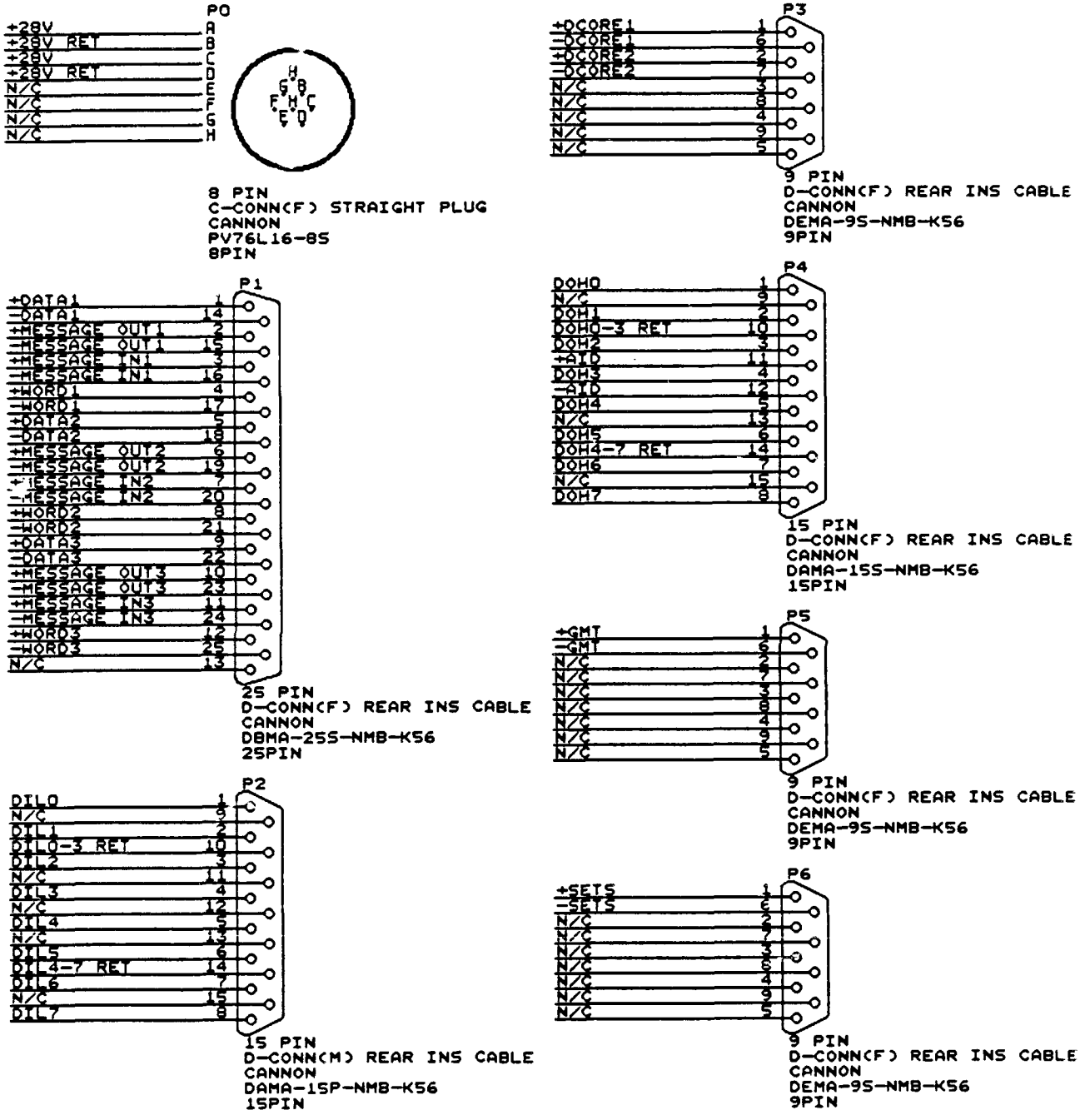


FIGURE QR6-15

ADDRESSING	A15	A14	A13
uC <> RAM	0	0	0
uC <> ANALOG	0	0	1
uC <> SERIAL	0	1	0
uC <> SCSI	0	1	1
SERIAL > RAM (DMA)	1	0	0
RAM > SERIAL (DMA)	1	0	1
RAM > SCSI (DMA)	1	1	0
SCSI > RAM (DMA)	1	1	1

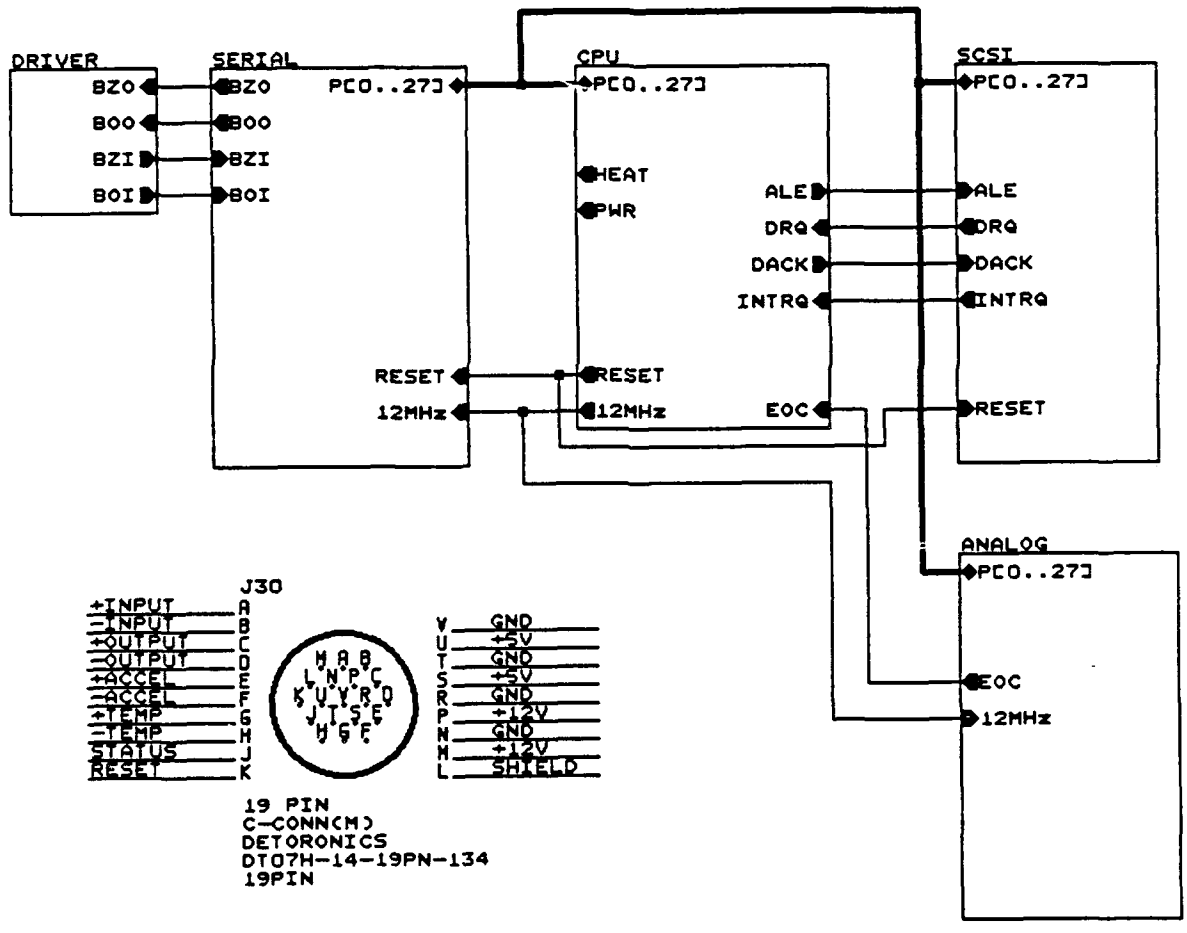
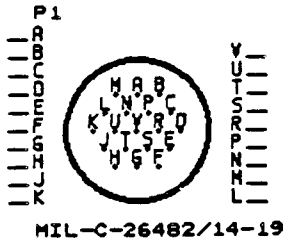


FIGURE QR6-16

VDD VCC +5V VSS GND

AMPTEK, INC.		
Title: ~~BRIDGE CONTROLLER~~ FDR 1		
Size: D	Document Number	REV
Date: March 7, 1989	Sheet 19 of 43	



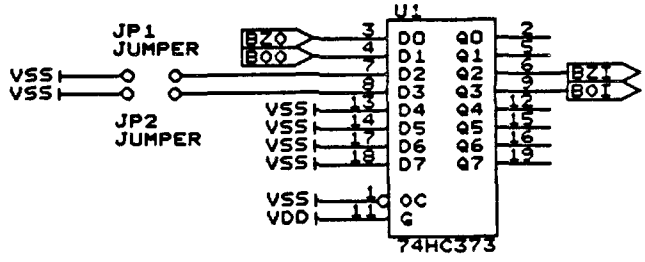


FIGURE QR6-17

AMPTEK, INC.		
Title: DRIVER		
Size: D	Document Number:	REV
Date: March 7, 1989	Sheet 20 of 43	

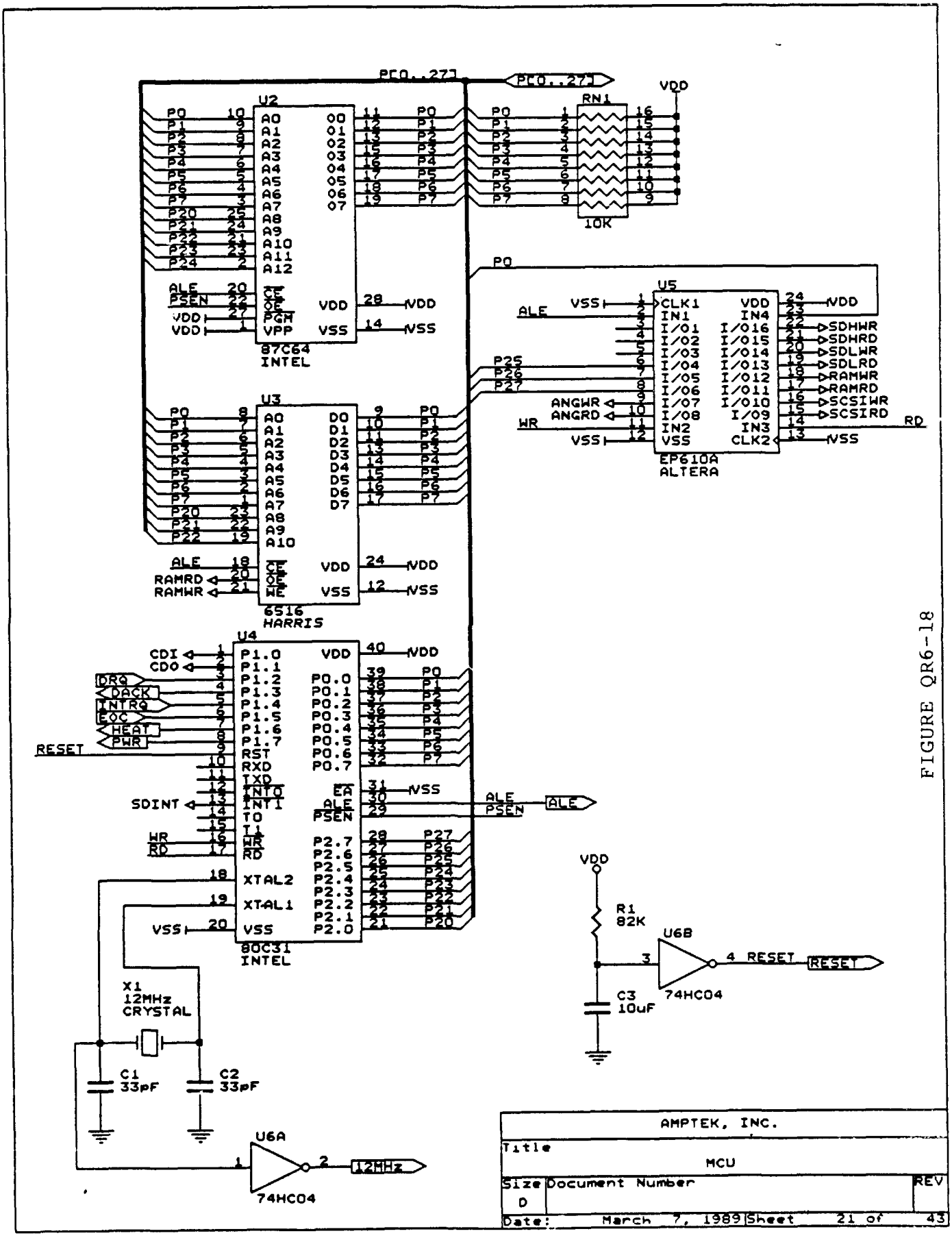


FIGURE QR6-18

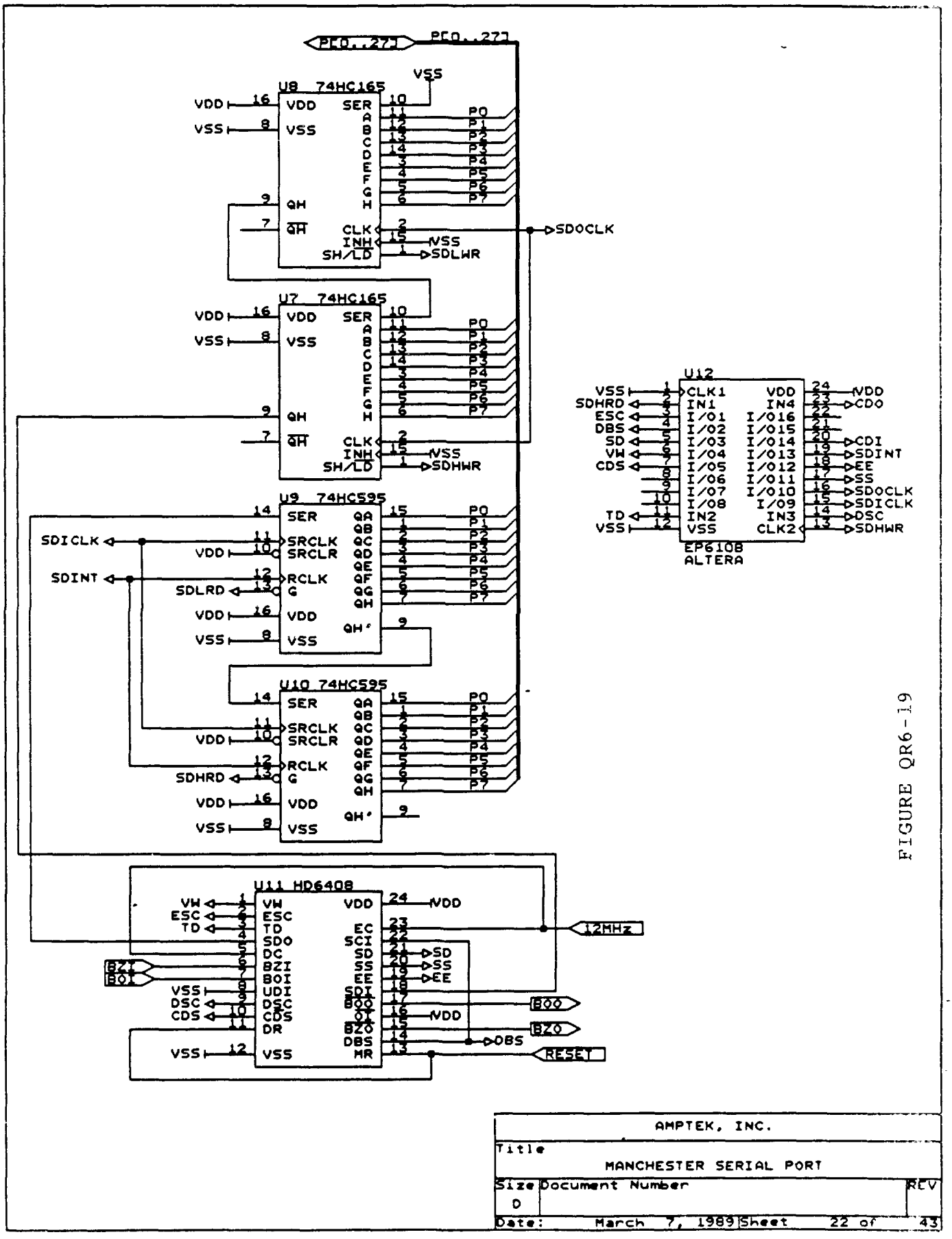


FIGURE QR6-19

AMPTEK, INC.		
Title: MANCHESTER SERIAL PORT		
Size: D	Document Number:	REV
Date: March 7, 1989	Sheet 22 of 43	

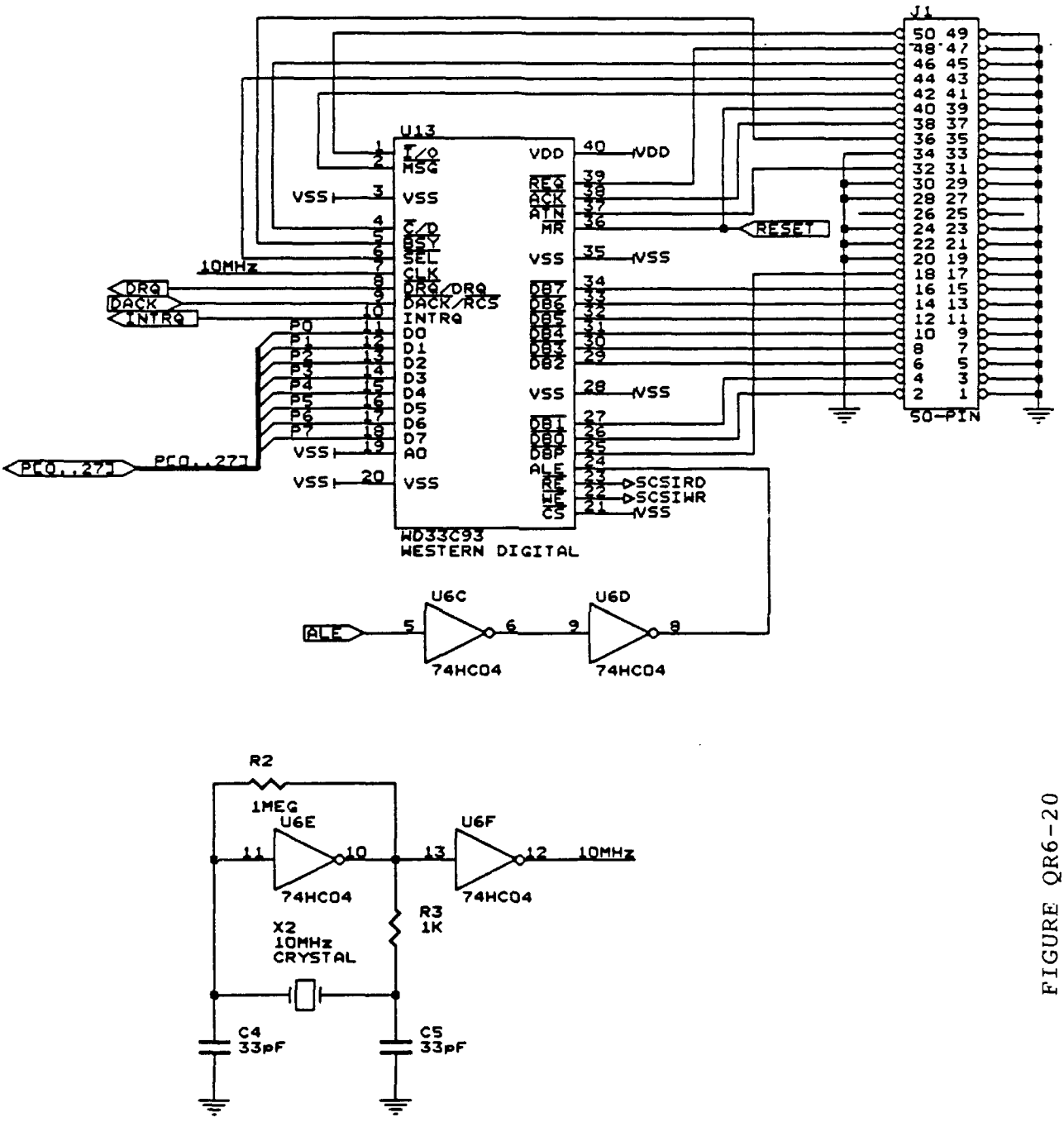


FIGURE QR6-20

AMPTEK, INC.		
Title: SCSI		
Size: D	Document Number:	REV
Date: March 7, 1989	Sheet 23 of 43	

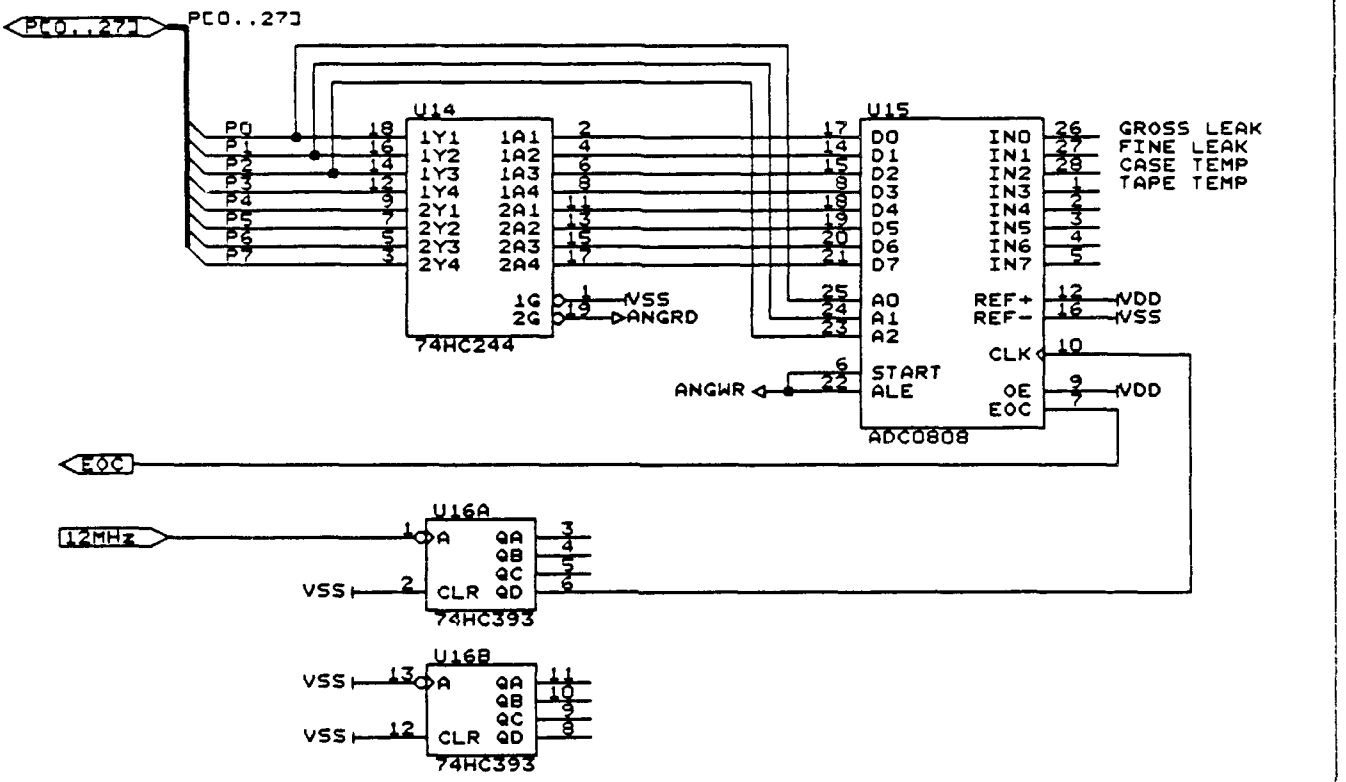


FIGURE QR6-21

AMPTEK, INC.		
Title: ANALOG		
Size: D	Document Number:	REV
Date: March 8, 1989	Sheet 24 of 43	

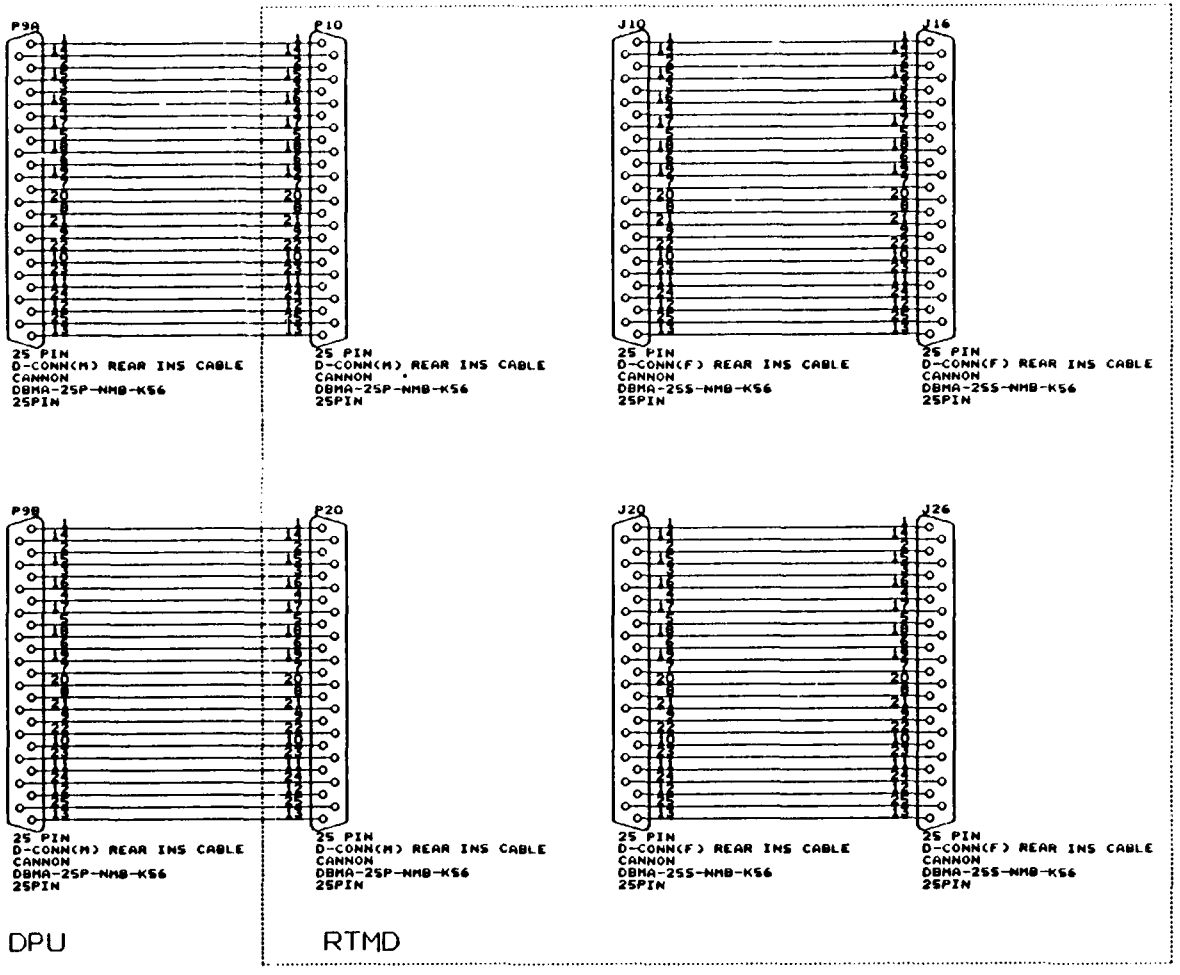


FIGURE QR6-22

AMPTEK, INC.		
Title: MTR HARNESS		
Size: B	Document Number:	REV
Date: March 1, 1989	Sheet 25 of 43	

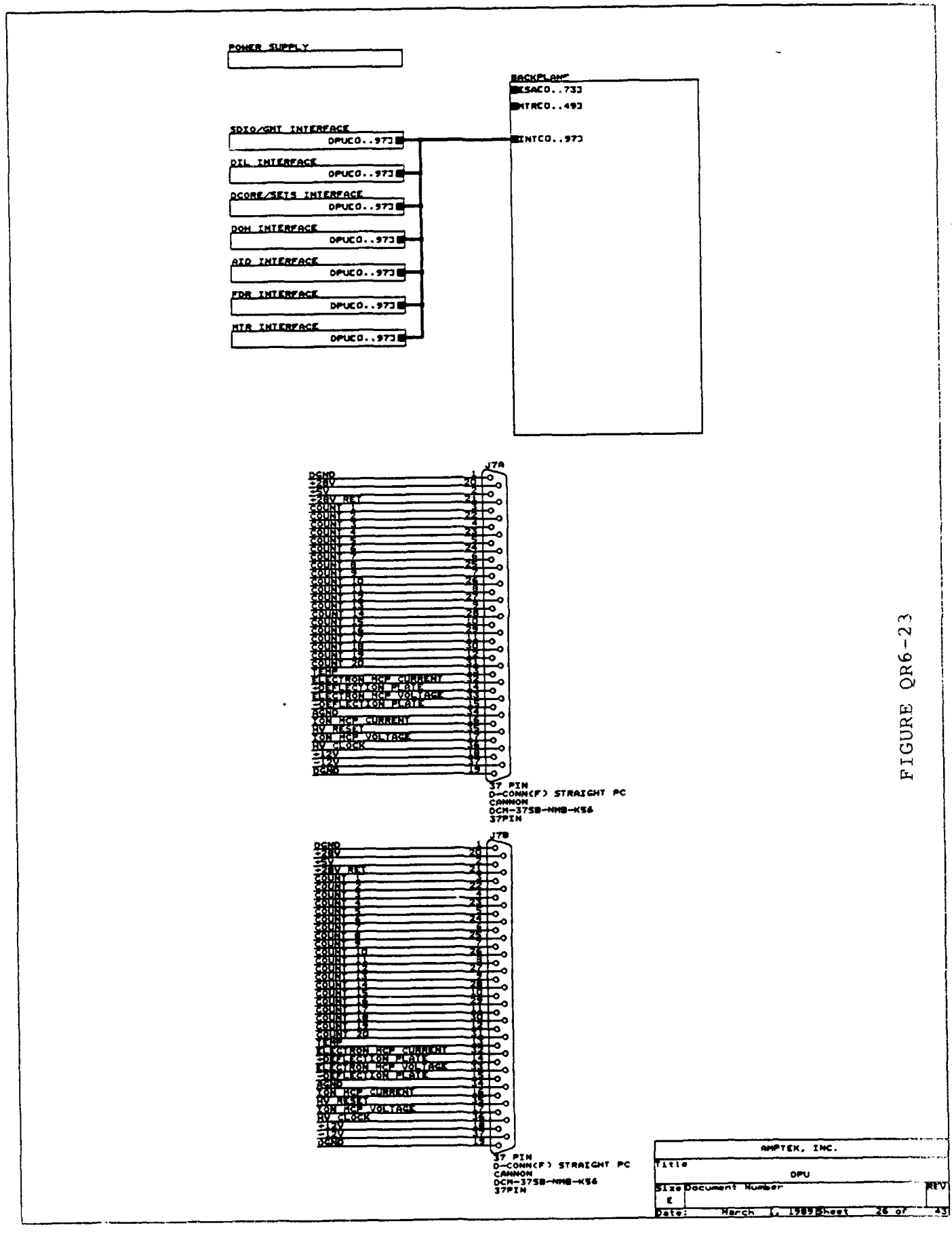
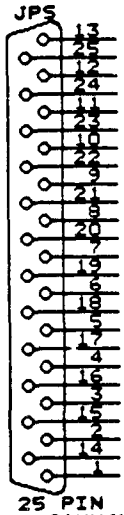


FIGURE QR6-23



25 PIN
D-CONN(M) STRAIGHT PC
CONNON
DBM-25PB-NMB-K56
25PIN

FIGURE QR6-24

AMPTEK, INC.		
Title: BACKPLANE		
Size: D	Document Number	REV
Date: March 2, 1989	Sheet 27 of 43	

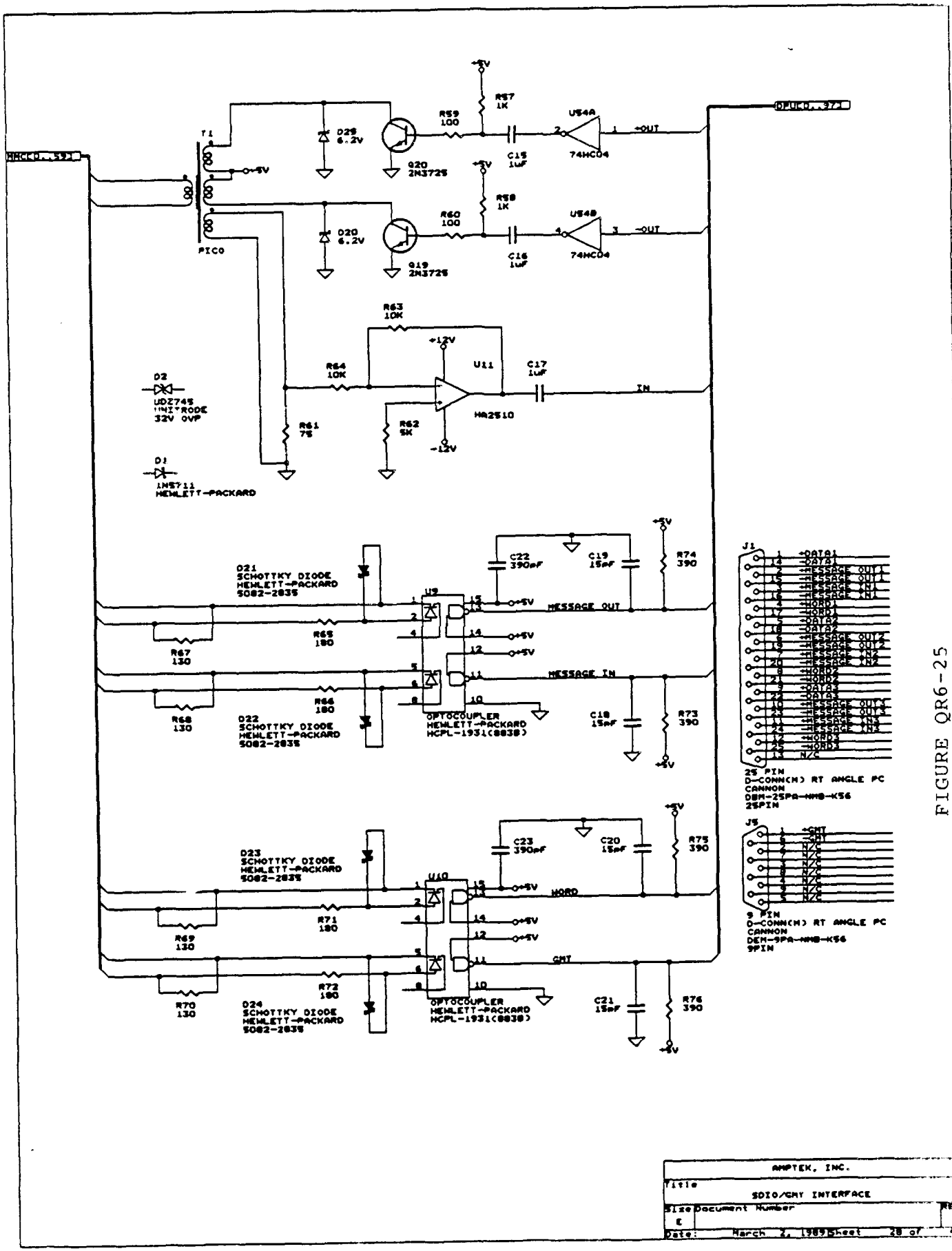


FIGURE QR6-25

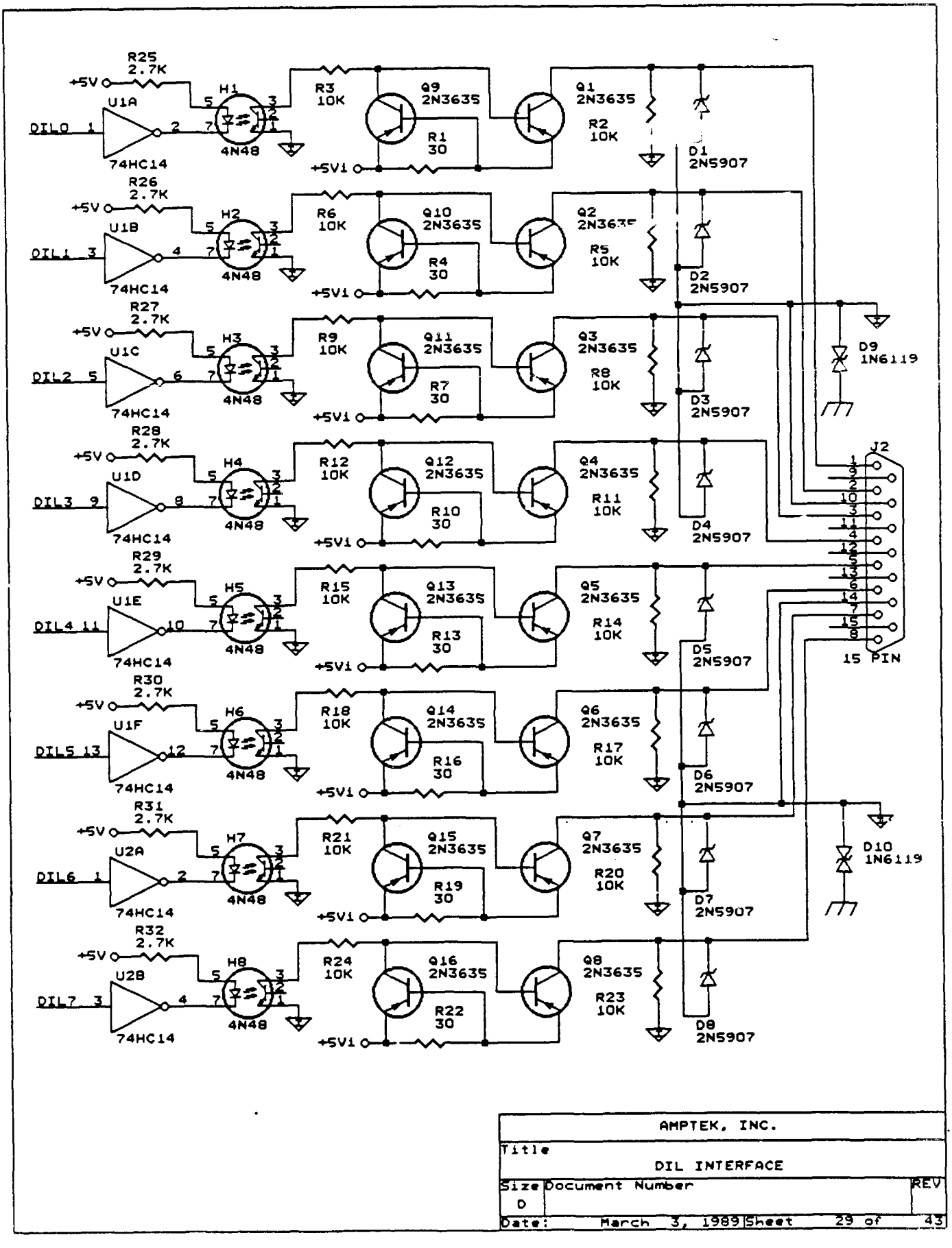


FIGURE QR6-26

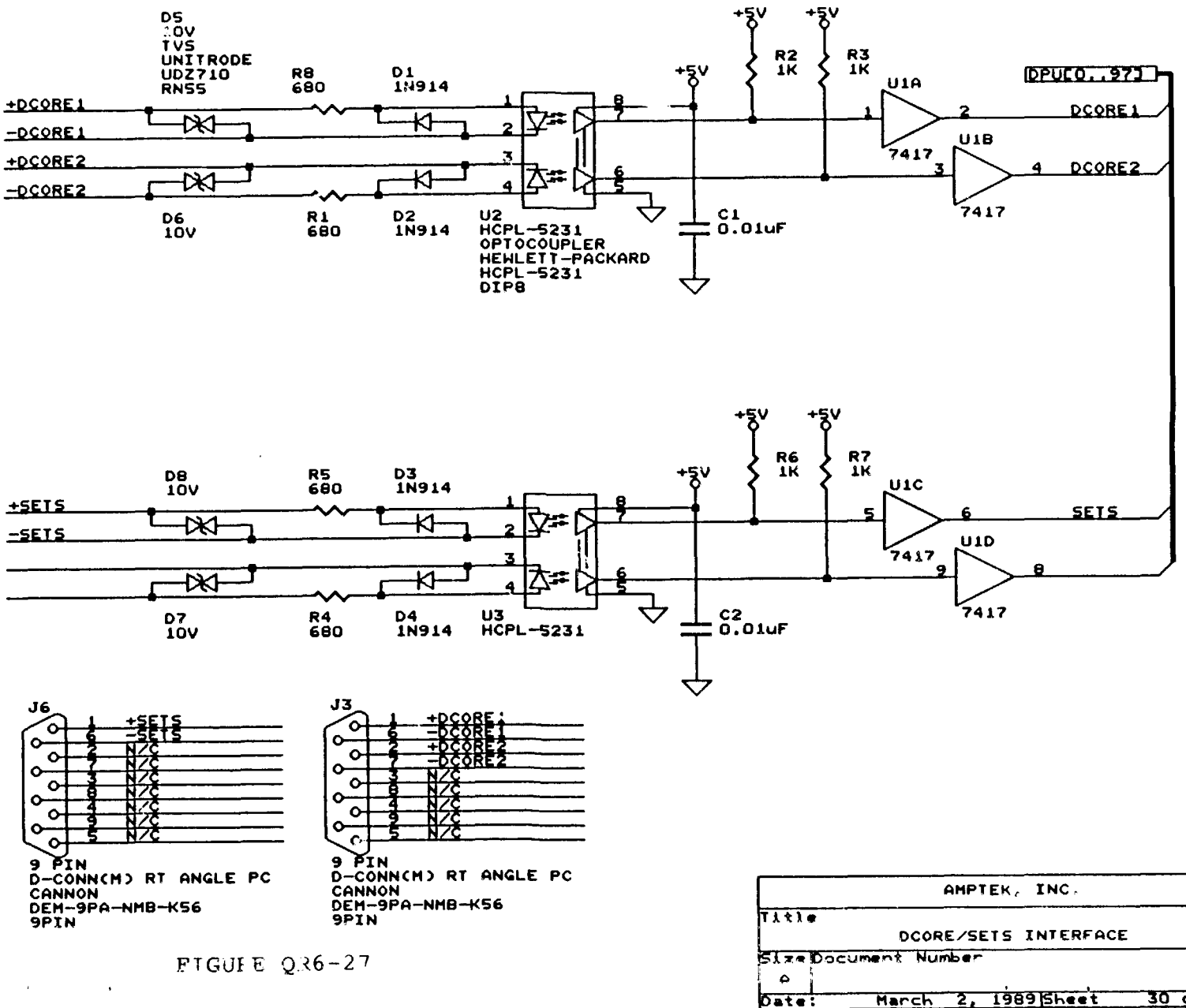


FIGURE QR6-27

AMPTEK, INC.		
Title: DCORE/SETS INTERFACE		
Size: A	Document Number:	REV
Date: March 2, 1989	Sheet 30 of 43	

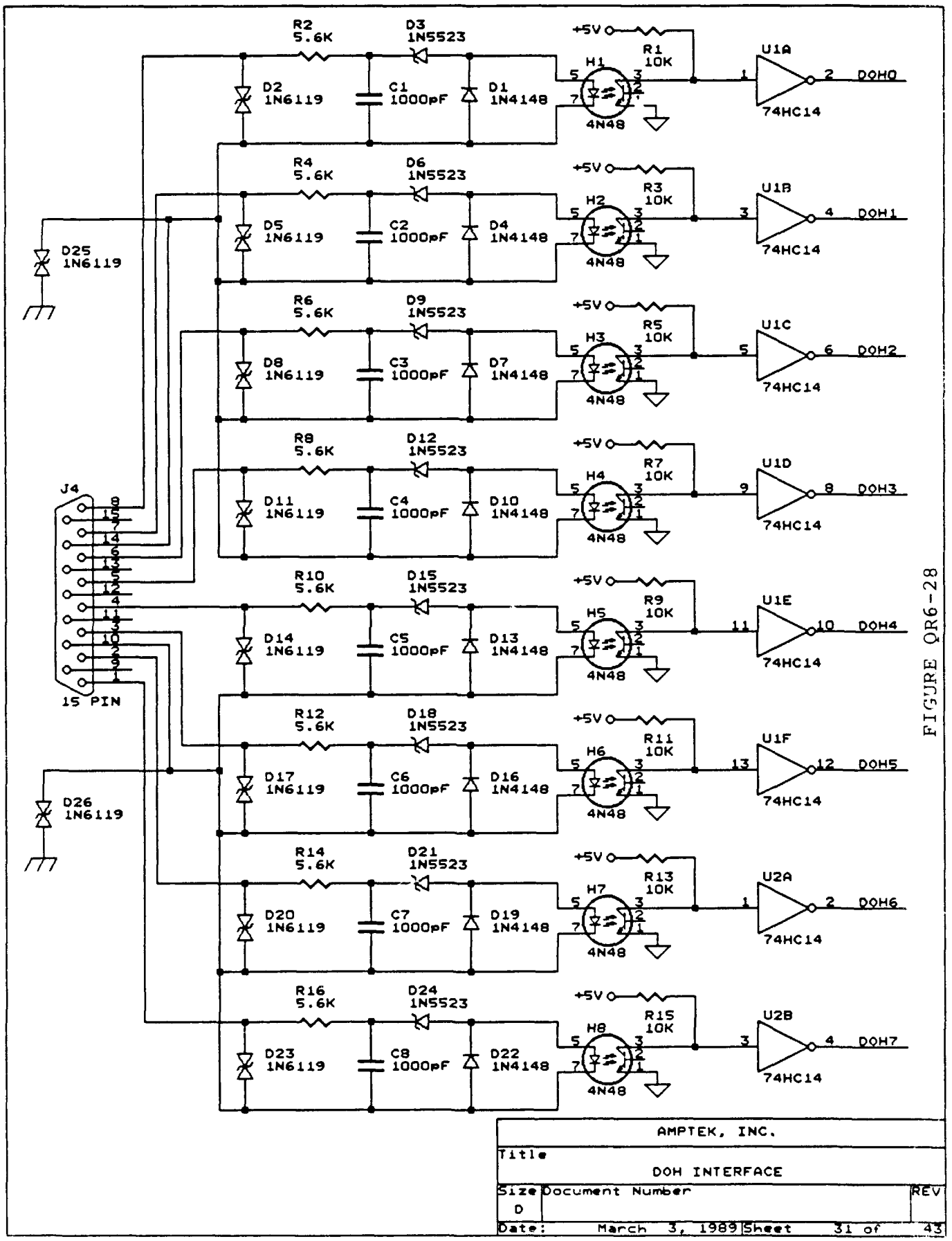


FIGURE QR6-28

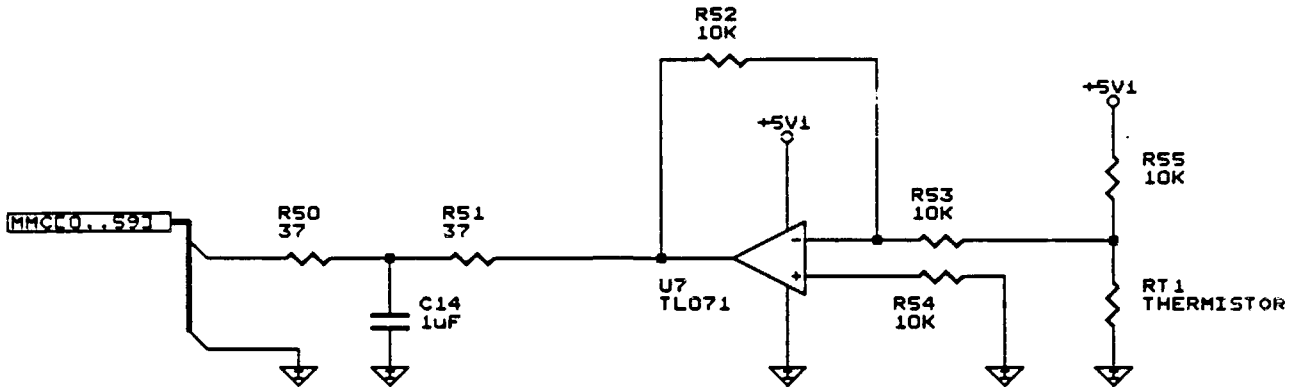
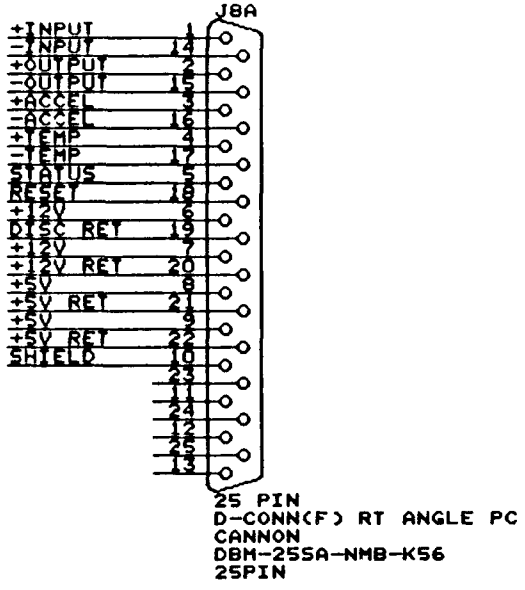


FIGURE QR6-29

AMPTEK, INC.		
Title: AID INTERFACE		
Size: D	Document Number:	REV:
Date: March 8, 1989	Sheet 32 of 43	



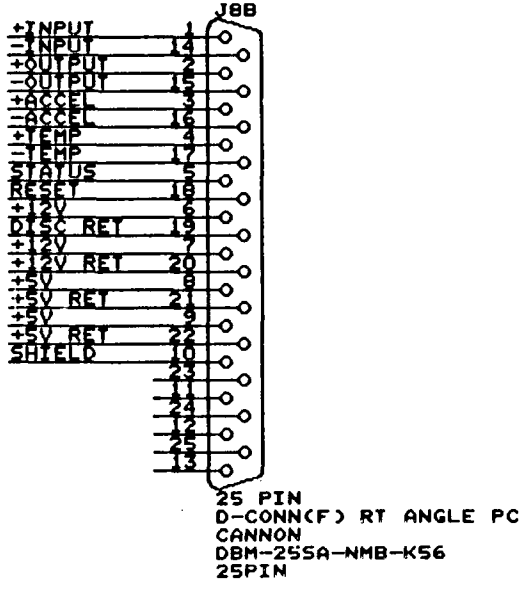


FIGURE QR6-30

AMPTEK, INC.		
Title: FDR INTERFACE		
Size: A	Document Number	REV
Date: March 1, 1989	Sheet 33 of 43	

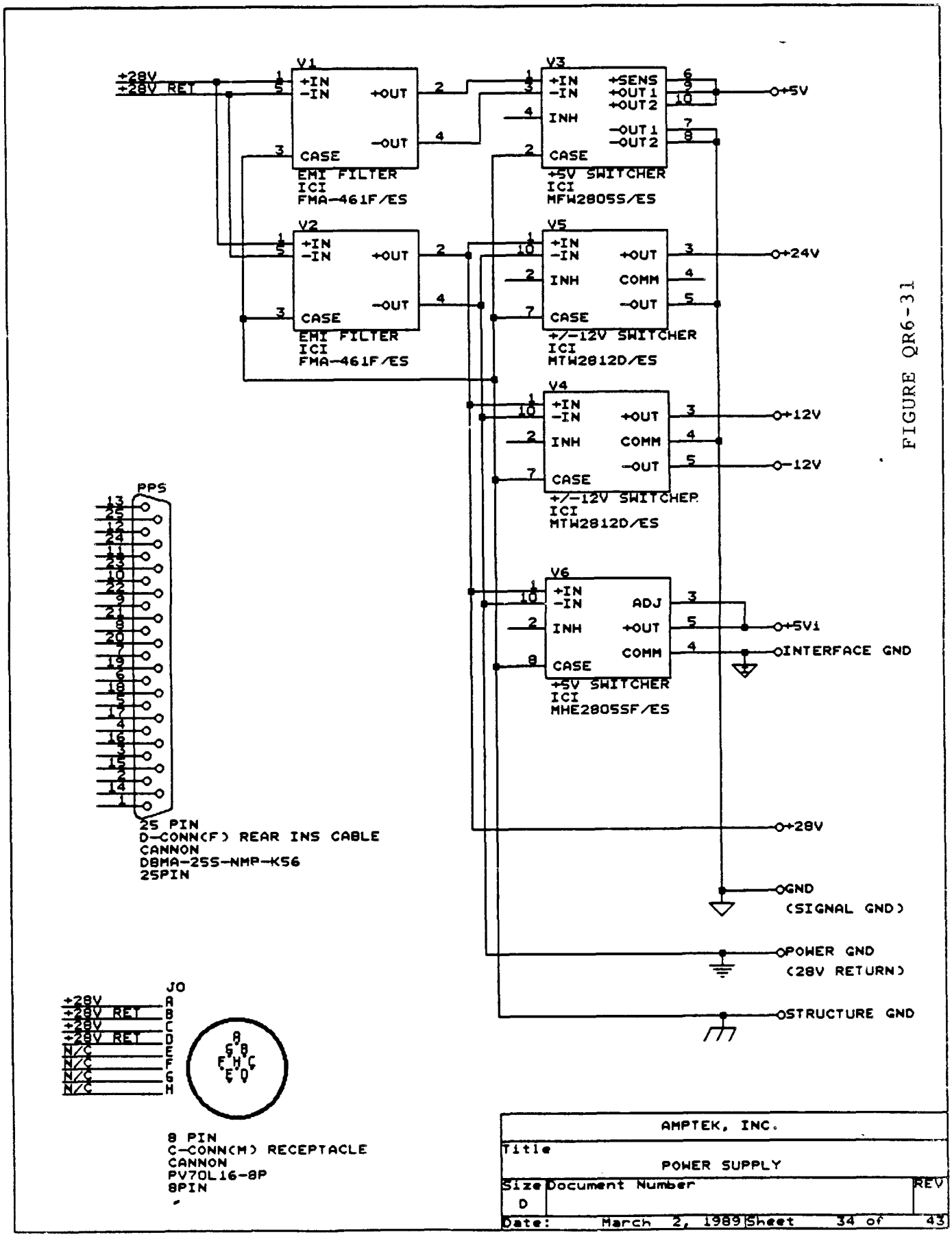


FIGURE QR6-31

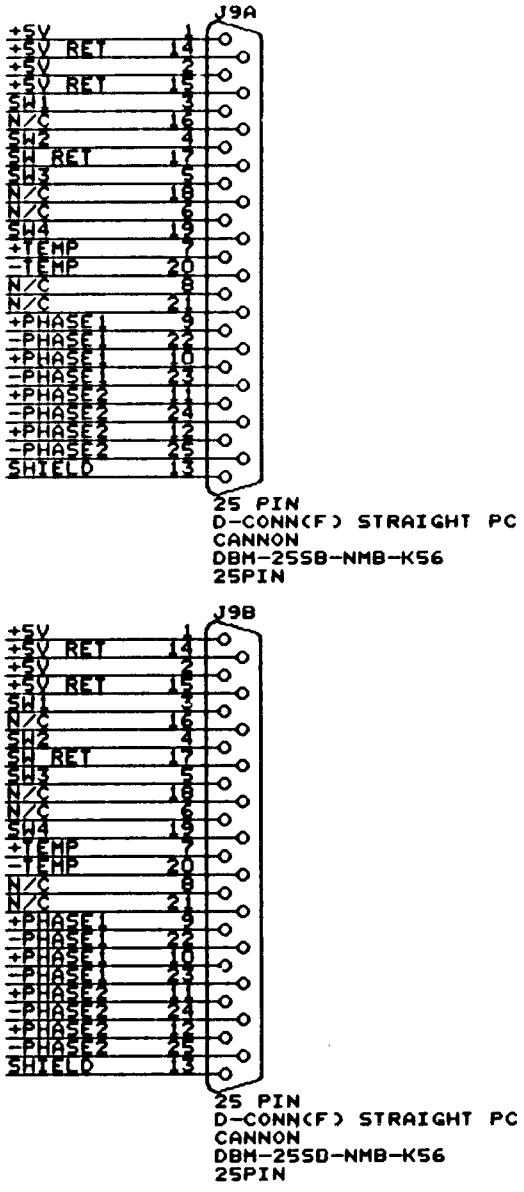


FIGURE QR6-32

AMPTEK, INC.		
Title: MTR INTERFACE		
Size: A	Document Number	REV
Date: March 1, 1989	Sheet 35 of 43	

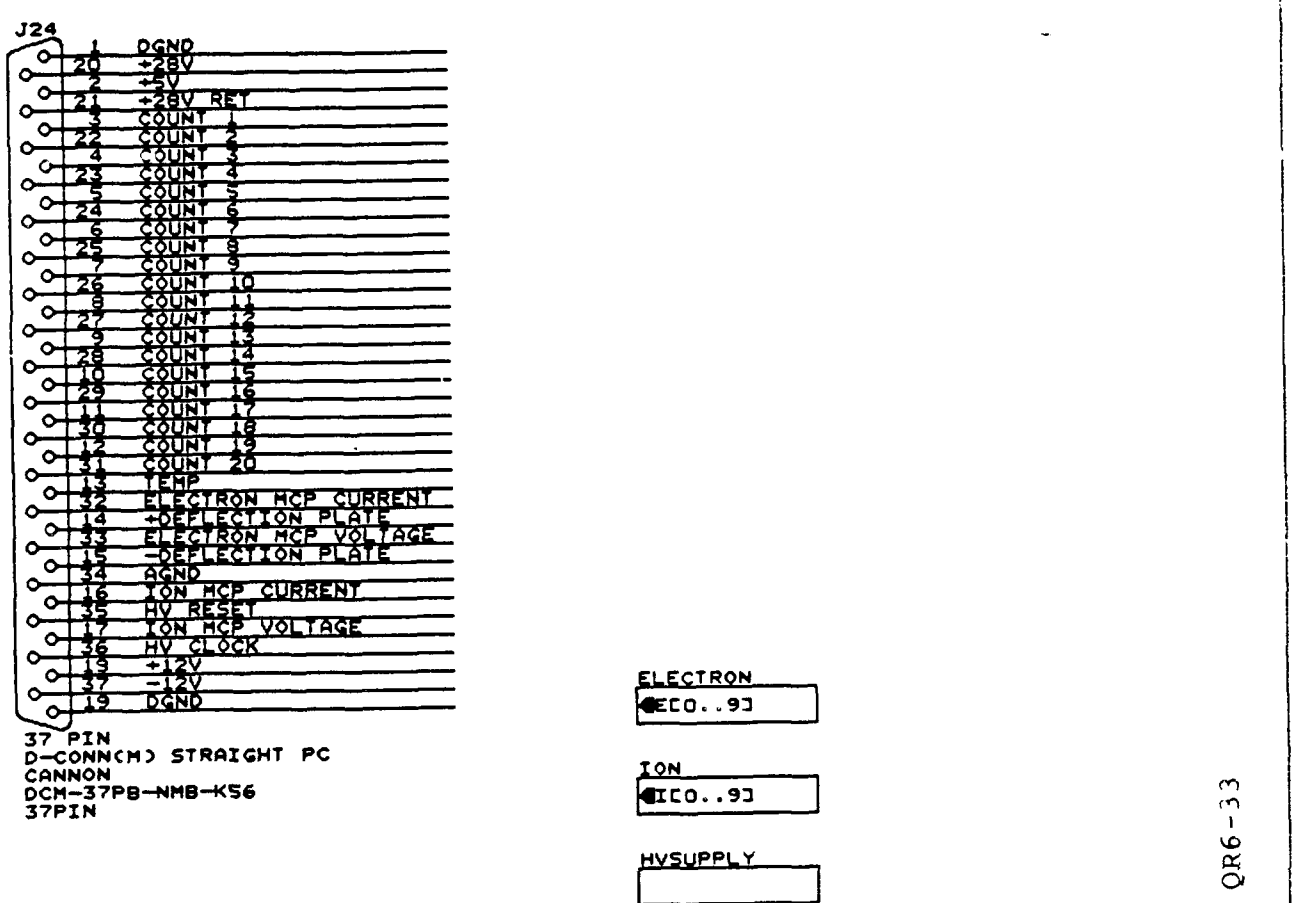


FIGURE QR6-33

AMPTEK, INC.		
Title: ESA B		
Size: D	Document Number:	REV
Date: March 7, 1989	Sheet 36 of	43

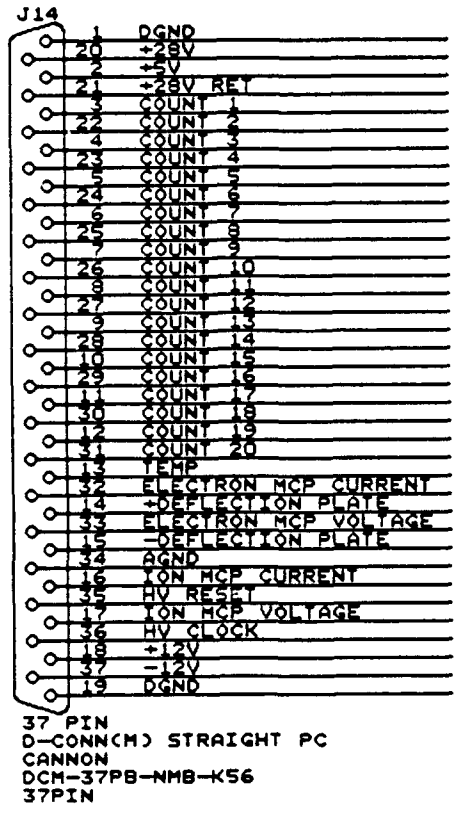


FIGURE QR6-34

AMPTEK, INC.		
Title: ESA A		
Size: D	Document Number:	REV
Date: March 7, 1989	Sheet 40 of 43	

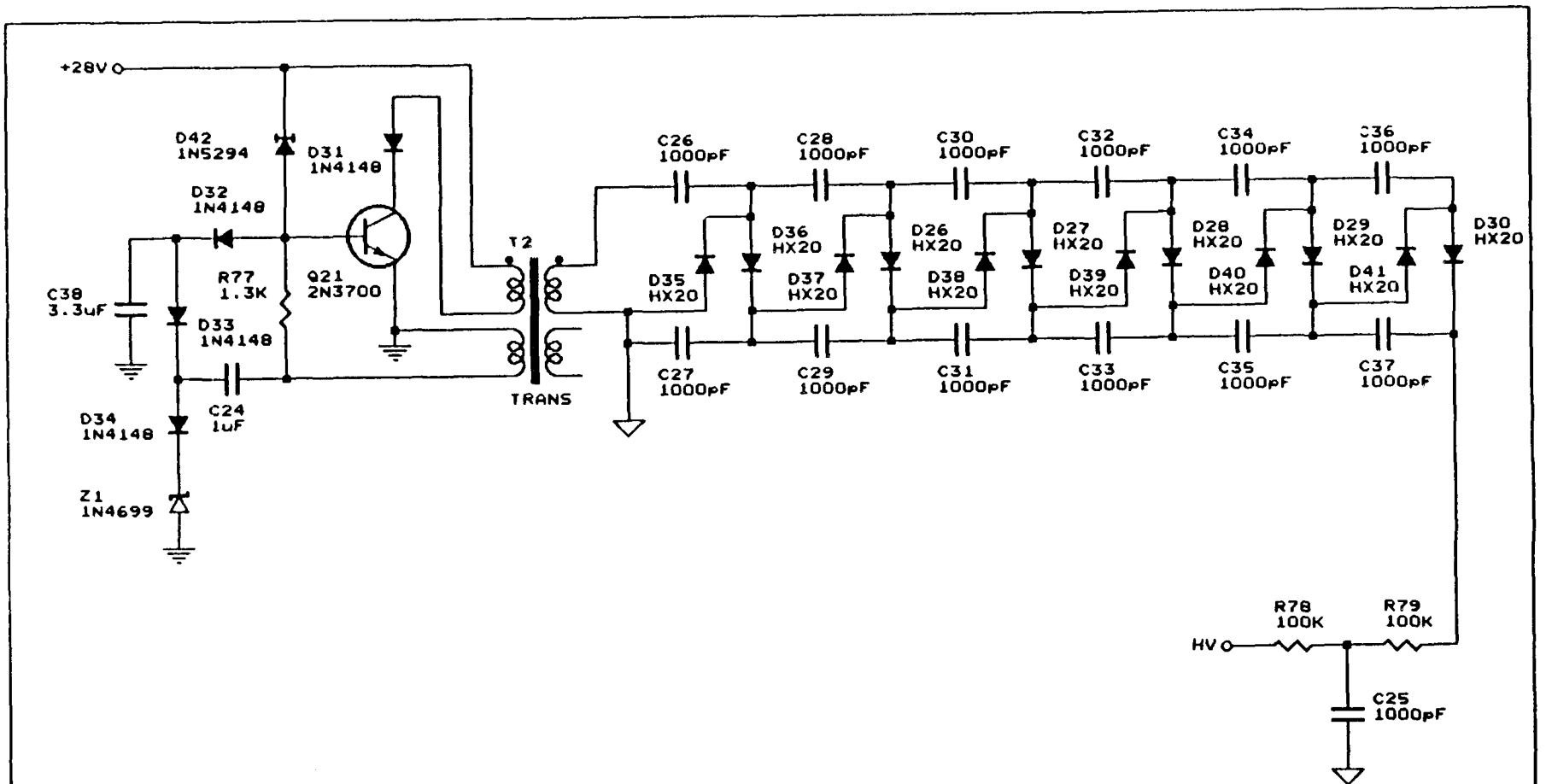


FIGURE QR6-35

AMPTEK, INC.		
Title: HV SUPPLY		
Size: A	Document Number	REV
Date: March 7, 1989	Sheet 41 of 43	

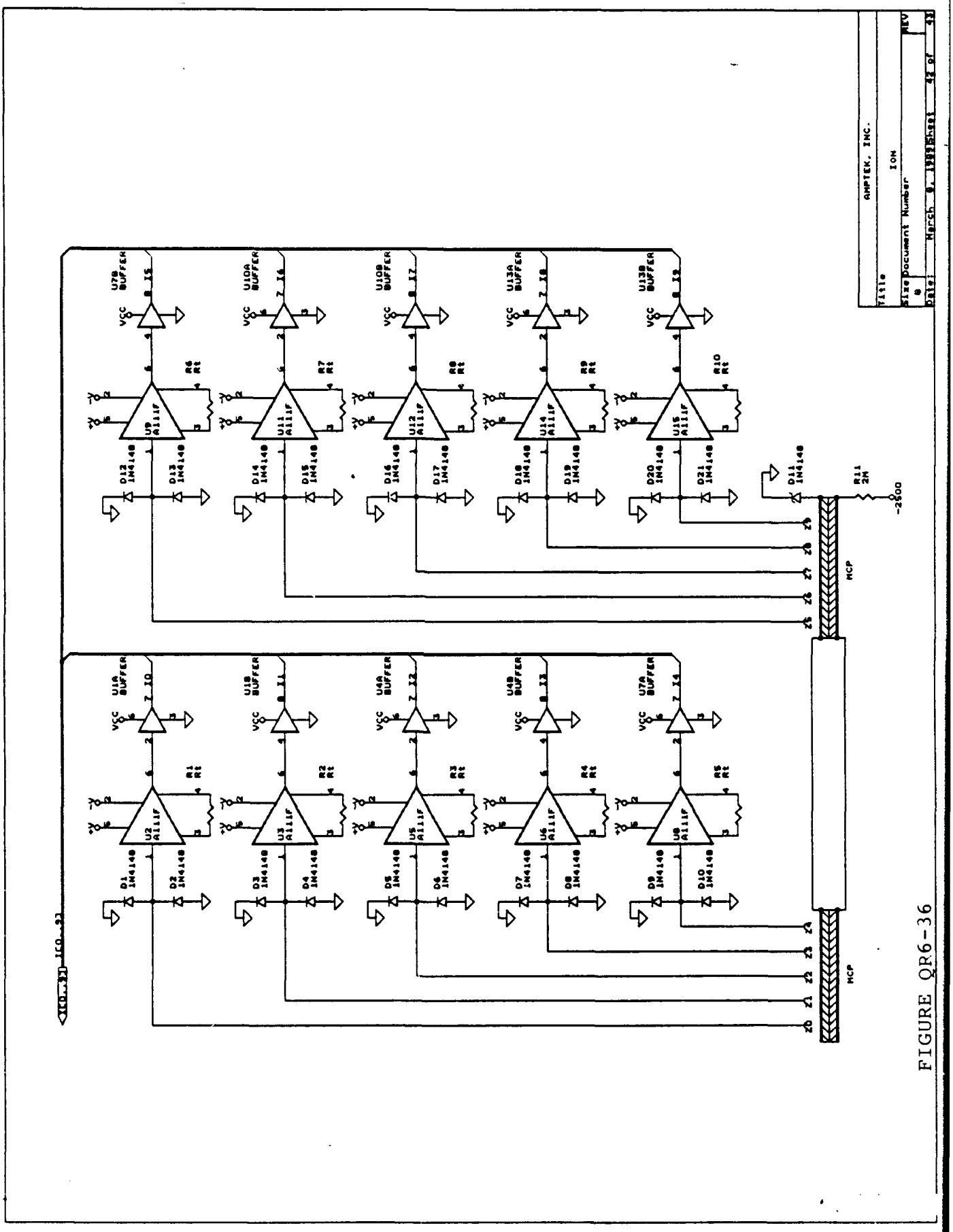


FIGURE QR6-36

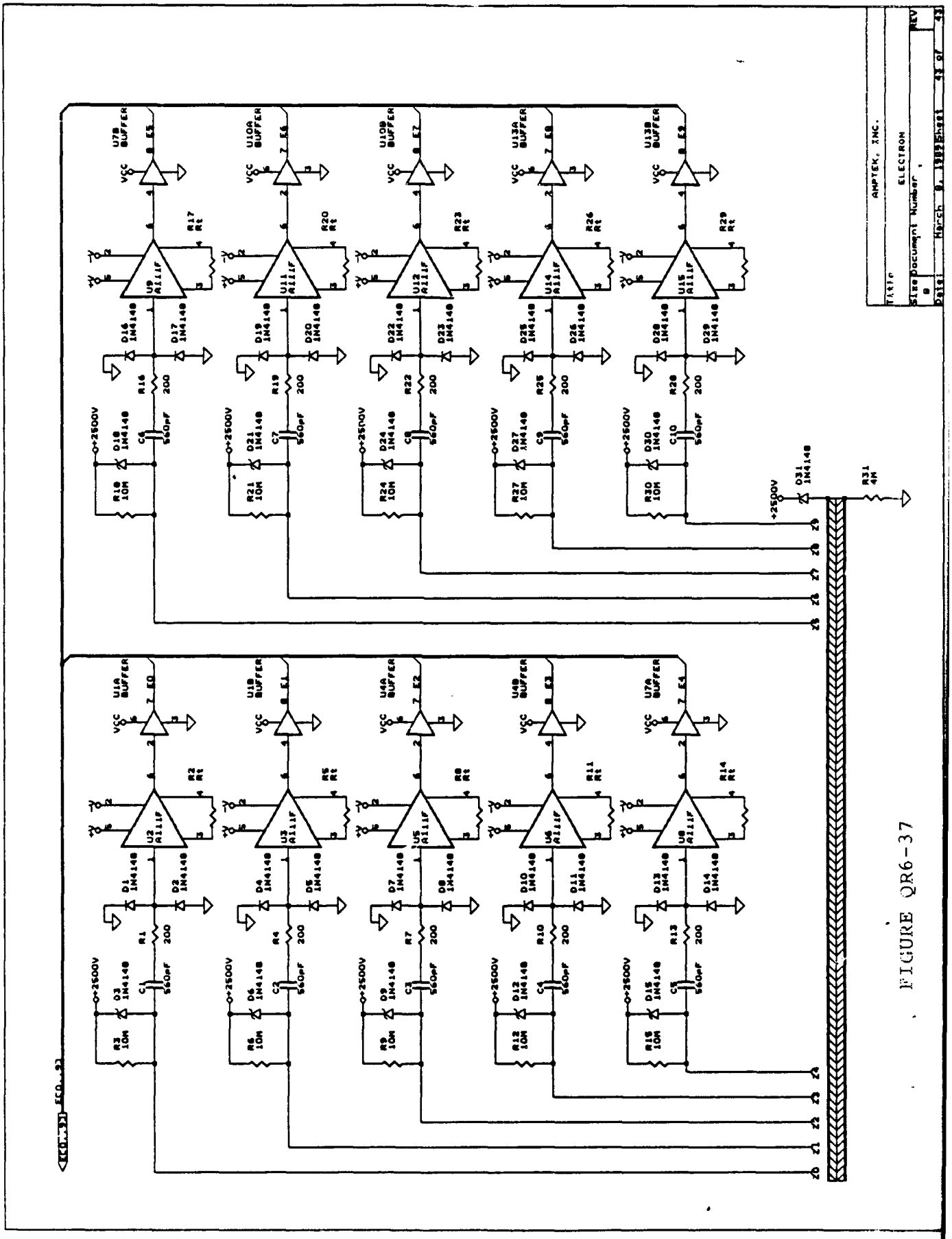


FIGURE QR6-37

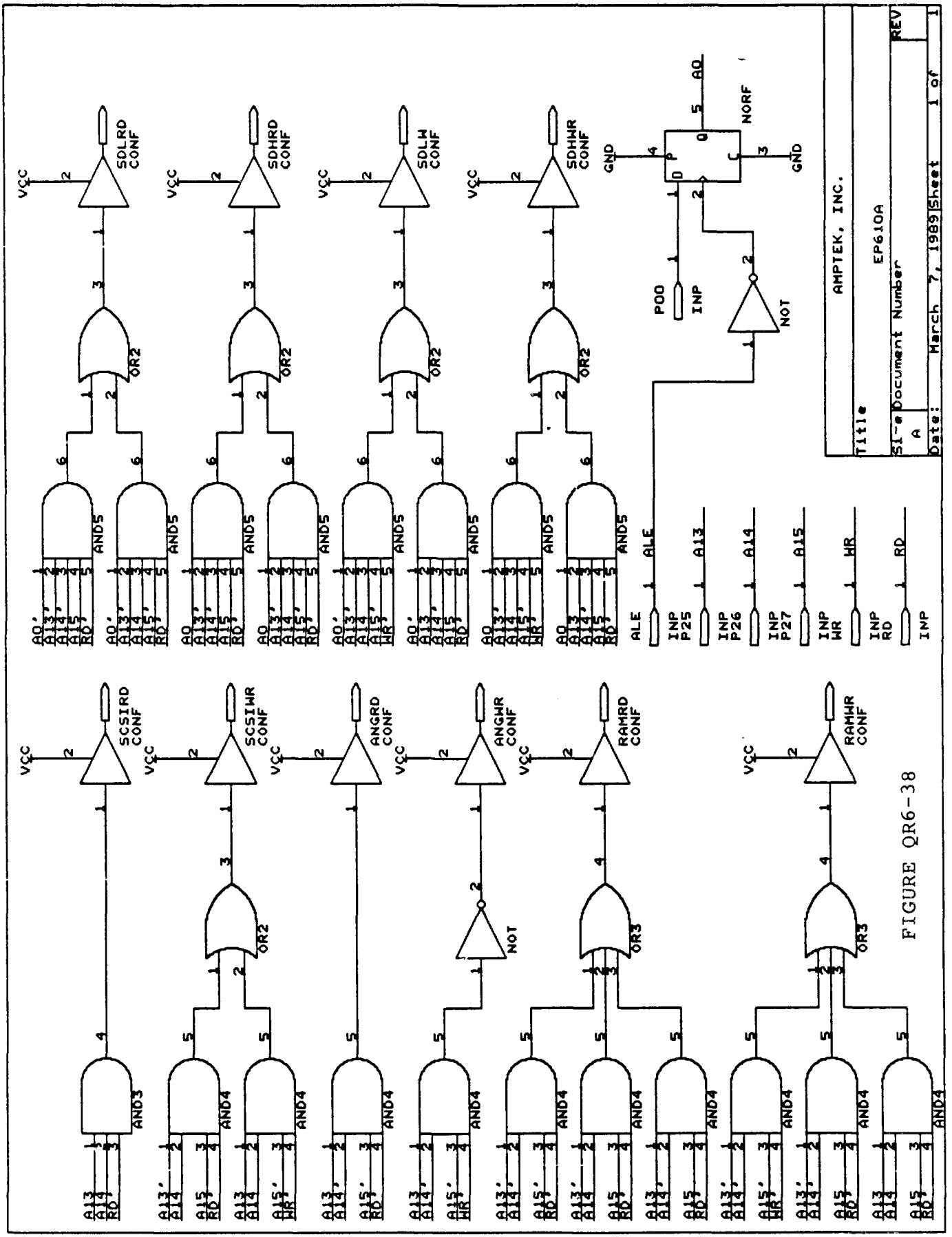


FIGURE QR6-38

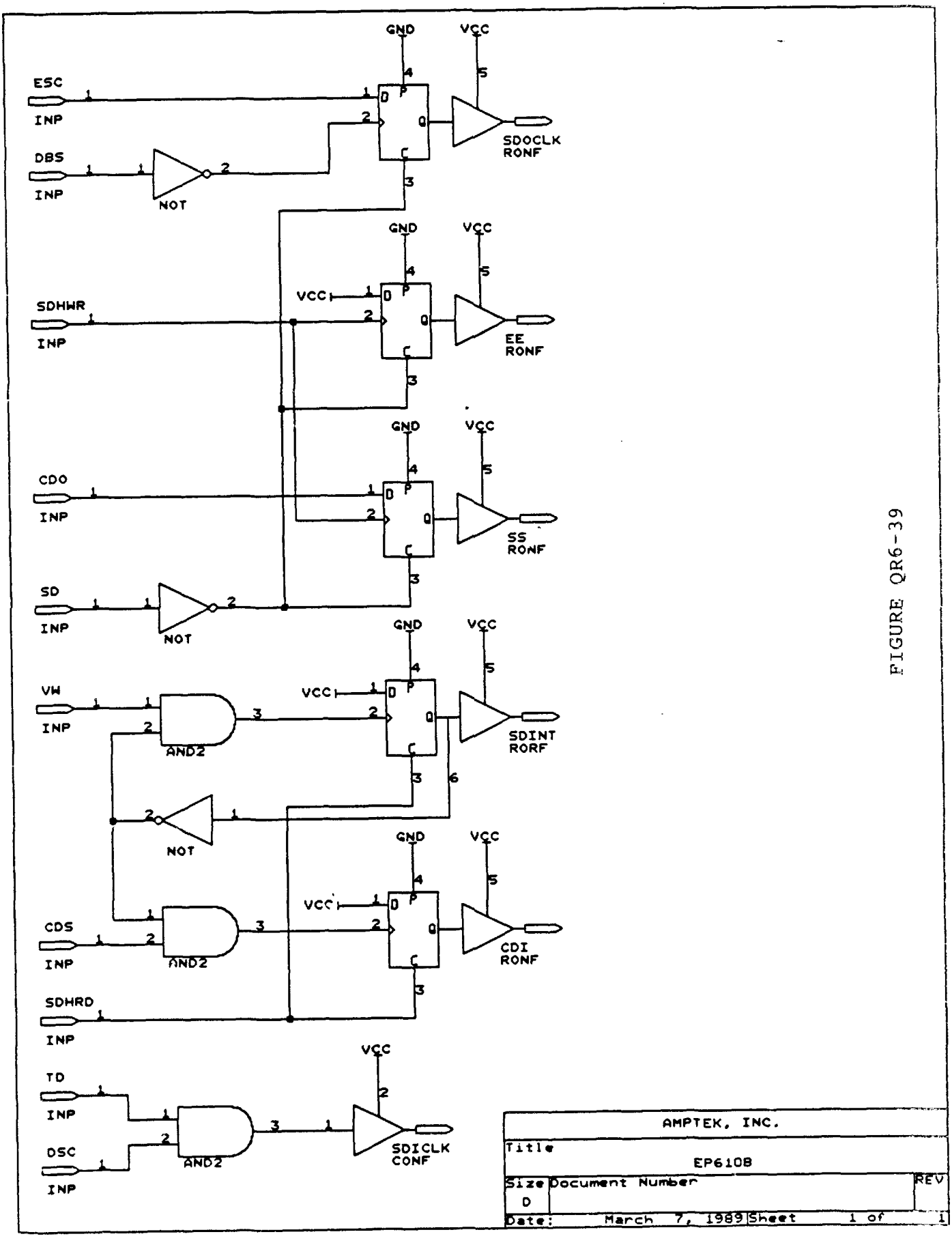


FIGURE QR6-39

Item	Quantity	Reference	Part
1	21	C1,C2,C3,C4,C5,C6,C7,C8, C25,C26,C27,C28,C29,C30, C31,C32,C33,C34,C35,C36, C37	1000pF
2	10	C1,C2,C3,C4,C5,C6,C7,C8, C9,C10	560pF
3	4	C1,C2,C4,C5	33pF
4	2	C1,C2	0.01uF
5	1	C1	1500uF
6	1	C2	0.1uF
7	1	C3	10uF
8	5	C14,C15,C16,C17,C24	1uF
9	4	C18,C19,C20,C21	15pF
10	2	C22,C23	390pF
11	1	C38	3.3uF
12	4	D1,D2,D3,D4	5.1V
13	12	D1,D2,D3,D4,D5,D6,D7,D8, D9,D10,D11,D12	1N914
14	34	D1,D2,D3,D4,D5,D8,D7,D8, D9,D10,D11,D12,D13,D14, D15,D16,D17,D18,D19,D20, D21,D22,D23,D24,D25,D26, D27,D28,D29,D30,D31,D32, D33,D34	1N4148
15	8	D1,D2,D3,D4,D5,D6,D7,D8	2N5907, 5V TVS, GENERAL SEMICONDUCTOR, 2N5907JTX, DO-13
16	8	D1,D4,D7,D10,D13,D16,D19, D22	1N4148 DIODE, , ,
17	1	D2	UDZ745, UNITRODE, 32V OVP, ,
18	9	D2,D5,D8,D9,D10,D11,D14, D17,D23	1N6119, 36V TVS, GENERAL INSTRUMENT, JTX1N6119A,
19	8	D3,D6,D9,D12,D15,D18,D21, D24	1N5523, 5.1V ZENER, MOTOROLA, 1N5523AJTX, DO-35
20	4	D5,D6,D7,D8	10V, TVS, UNITRODE, UDZ710, RN55

Item	Quantity	Reference	Part
21	1	D1	1N5711, HEWLETT-PACKARD, , ,
22	1	D20	1N6119, 36V TVS, GENERAL INTSTRUMENT, JTX1N6119A,
23	2	D20,D25	6.2V
24	4	D21,D22,D23,D24	SCHOTTKY DIODE, HEWLETT-PACKARD, 5082-2835, ,
25	2	D25,D26	1N6119, 36V TVS, GENERAL INSTRUMENT, JANTX1N6119A,
26	12	D26,D27,D28,D29,D30,D35, D36,D37,D38,D39,D40,D41	HX20
27	1	D42	1N5294
28	8	H1,H2,H3,H4,H5,H6,H7,H8	4N48, OPTOCOUPLER, TEXAS INSTRUMENTS, JANTX 4N48, TO-8
29	1	J0	8 PIN, C-CONN(M) RECEPTACLE, CANNON, Pv70L16-8P, 8PIN
30	1	J1	50-PIN
31	1	J1	25 PIN, D-CONN(M) RT ANGLE PC, CANNON, DBM-25PA-NMB-K56, 25PIN
32	1	J2	15 PIN, D-CONN(F) RT ANGLE PC, CANNON, DAM-15SA-NMB-K56, 15PIN
33	3	J3,J5,J6	9 PIN, D-CONN(M) RT ANGLE PC, CANNON, DEM-9PA-NMB-K56, 9PIN
34	1	J4	15 PIN, D-CONN(M) RT ANGLE PC, CANNON, DAM-15PA-NMB-K56, 15PIN
35	4	J7A,J7B,J15,J25	37 PIN, D-CONN(F) STRAIGHT PC, CANNON, DCM-37SB-NMB-K56, 37PIN
36	2	J8A,J8B	25 PIN, D-CONN(F) RT ANGLE PC, CANNON, DBM-25SA-NMB-K56, 25PIN
37	2	J9A,J9B	25 PIN, D-CONN(F) STRAIGHT PC, CANNON, DBM-25SB-NMB-K56, 25PIN
38	6	P1,J10,J16,J20,J26,PP3	25 PIN, D-CONN(F) REAR INS CABLE, CANNON, DBMA-25S-NMB-K56, 25PIN
39	6	P7A,P7B,J11,P15,J21,P25	37 PIN, D-CONN(M) REAR INS CABLE, CANNON, DCMA-37P-NMB-K56, 37PIN
40	2	J14,J24	37 PIN, D-CONN(M) STRAIGHT PC, CANNON, DCM-37PB-NMB-K56, 37PIN
41	2	J30,J31	19 PIN, C-CONN(M), DETORONICS, DTO7H-14-19PN-134, 19PIN
42	2	JP1,JP2	JUMPER
43	1	JP3	25 PIN, D-CONN(M) STRAIGHT PC, CANNON, DBM-25PB-NMB-K56, 25PIN
44	1	L1	18mH
45	3	L1,L2,L3	L
46	4	M1,M2,M3,M4	IRF530

Item	Quantity	Reference	Part
47	1	MTR1	STEPPER MOTOR, DENSEI, P5J-U03S, ,
48	1	P0	8 PIN, C-CONN(F) STRAIGHT PLUG, CANNON, PV76L16-8S, 8PIN
49	1	P1	MIL-C-26482/14-19
50	1	P2	15 PIN, D-CONN(M) REAR INS CABLE, CANNON, DAMA-15P-NMB-K56, 15PIN
51	3	P3,P5,P6	9 PIN, D-CONN(F) REAR INS CABLE, CANNON, DEMA-9S-NMB-K56, 9PIN
52	1	P4	15 PIN, D-CONN(F) REAR INS CABLE, CANNON, DAMA-15S-NMB-K56, 15PIN
53	8	P8A,P8B,P9A,P9B,P1C P16, P20,P26	25 PIN, D-CONN(M) REAR INS CABLE, CANNON, DBMA-25P-NMB-K56, 25PIN
54	4	P11,P14,P21,P24	37 PIN, D-CONN(F) REAR INS CABLE, CANNON, DCMA-37S-NMB-K56, 37PIN
55	2	P30,P31	19 PIN, C-CONN(F), AIR ELECTRO, AE 3116F14-19S(023), 19PIN
56	16	Q1,Q2,Q3,Q4,Q5,Q6,Q7,Q8, Q9,Q10,Q11,Q12,Q13,Q14, Q15,Q16	2N3635, TRANSISTOR, MOTOROLA, 2N3635JTX, TO-39
57	2	Q19,Q20	2N3725
58	1	Q21	2N3700
59	6	R1,R2,R3,R4,R5,R8	680
60	10	R1,R4,R7,R10,R13,R16,R19, R22,R25,R28	200
61	17	R1,R2,R3,R4,R5,R6,R7,R8, R9,R10,R11,R14,R17,R20, R23,R26,R29	Rt
62	8	R1,R4,R7,R10,R13,R16,R19, R22	30, RESISTOR, , , RN55
63	19	R1,R2,R3,R5,R6,R7,R8,R9, R11,R12,R13,R14,R15,R17, R18,R20,R21,R23,R24	10K, RESISTOR, , , RN55
64	1	R1	82K
65	1	R2	1MEG
66	6	R2,R3,R6,R7,R57,R58	1K
67	8	R2,R4,R6,R9,R10,R12,R14, R16	5.6K, RESISTOR, , , RN55
68	10	R3,R8,R9,R12,R15,R18,R21,	10M

Item	Quantity	Reference	Part
		R24,R27,R30	
69	4	R5,R6,R7,R8	1.5K
70	1	R9	220
71	1	R11	2M
72	8	R25,R26,R27,R28,R29,R30, R31,R32	2.7K, RESISTOR, , , RN55
73	1	R31	4M
74	2	R50,R51	37
75	7	RN1,R52,R53,R54,R55,R63, R64	10K
76	2	R59,R60	100
77	1	R61	75
78	1	R62	5K
79	4	R65,R66,R71,R72	180
80	4	R67,R68,R69,R70	130
81	4	R73,R74,R75,R76	390
82	1	R77	1.3K
83	2	R78,R79	100K
84	1	RT1	THERMISTOR
85	1	T1	PICO
86	1	T2	TRANS
87	1	U1	6N140A
88	2	U1,U2	74HC14, INVERTER, , , DIP14
89	1	U2	87C64, INTEL, , ,
90	10	U2,U3,U5,U6,U8,U9,U11, U12,U14,U15	A111F
91	19	U2,U3,U15,U16,U17,U18, U19,U26,U27,U28,U29,U36, U37,U38,U39,U43,U44,U45, U46	NOTF

Item	Quantity	Reference	Part
92	2	U2,U3	HCPL-5231, OPTOCOUPLER, HEWLETT-PACKARD, HCPL-5231, DIP8
93	1	U3	6516, HARRIS, , ,
94	1	U4	80C31, INTEL, , ,
95	17	U4,U13,U14,U23,U24,U25, U33,U34,U35,U40,U41,U42, U47,U48,U49,U50,U51	NOT
96	5	U1,U4,U7,U10,U13	BUFFER
97	1	U5	EP610A, ALTERA, , ,
98	1	U5	AND2
99	2	U6,U8	XOR
100	2	U6,U54	74HC04
101	1	U7	TL071
102	1	U7	NOCF
103	2	U7,U8	74HC165
104	4	U9,U10,U11,U12	AND3
105	2	U9,U10	OPTOCOUPLER, HEWLETT-PACKARD, HCPL-1931(883B), ,
106	2	U9,U10	74HC595
107	1	U11	HA2510
108	1	U12	EP610B, ALTERA, , ,
109	1	U1	74HC373
110	1	U11	HD6408
111	1	U13	WD33C93, WESTERN DIGITAL, , ,
112	1	U14	74HC244
113	1	U15	ADC0808
114	1	U1	7417
115	1	U16	74HC393
116	4	U20,U22,U30,U32	OR2
117	2	U21,U31	NAND2

Item	Quantity	Reference	Part
118	2	U52,U53	INP
119	2	V1,V2	EMI FILTER, ICI, FMA-461F/ES, ,
120	1	V3	+5V SWITCHER, ICI, MFW2805S/ES, ,
121	2	V4,V5	+/-12V SWITCHER, ICI, MTW2812D/ES, ,
122	1	V6	+5V SWITCHER, ICI, MHE2805SF/ES, ,
123	1	X1	12MHz, CRYSTAL, , ,
124	1	X2	10MHz, CRYSTAL, , ,
125	1	Z1	1N4699

PRDA-QR7

PROTOTYPE INSTRUMENTATION AND DESIGN STUDIES

AMPTEK, INC.
6 De Angelo Drive
Bedford, MA 01730

June 12, 1989

R&D Status Report no. 7
March 5, 1989 through June 4, 1989

Contract #F19628-87-C-0094

Distribution: AFGL/PHP
DCASMA/ACO
ESD/PKR

Prepared for:

GEOPHYSICS LABORATORY
Air Force Systems Command
United States Air Force
Hanscom Air Force Base, Massachusetts 01731-5000

SPREE Integrated Package

A new schedule has been developed with the delivery date moved from December 1989 to May 1990. This delay results from a general space shuttle launch schedule.

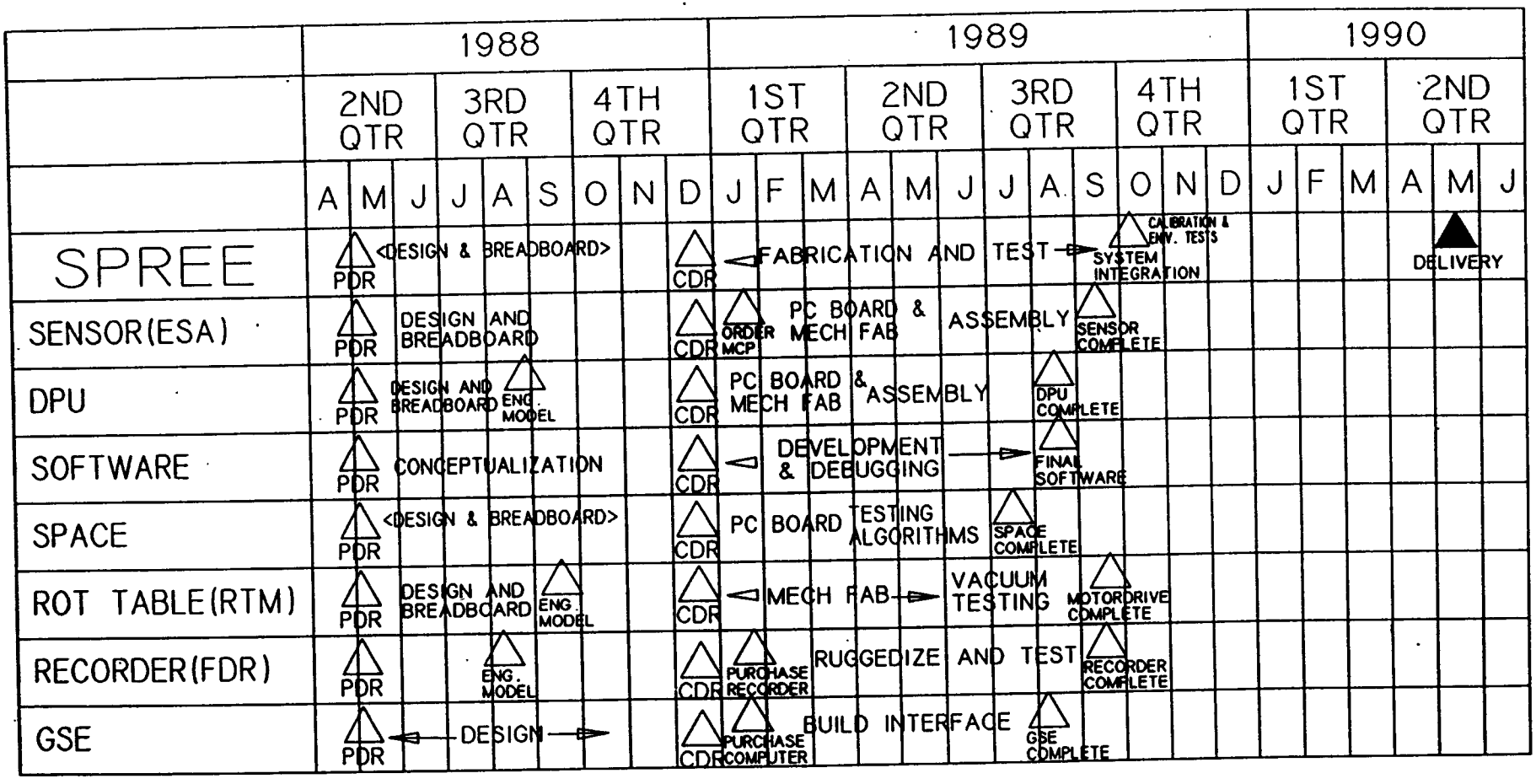
All the SPREE instruments' ICDs were updated to reflect current status and to incorporate grounding studs or threaded holes on each package.

The flight electrical connectors for SPREE were ordered and received this quarter.

The power supply converters and filters were selected and finalized this past quarter. An order was placed and the flight power supplies have been received.

A SPREE flight assembly and storage area has been created. This area will be used to store SPREE flight equipment and spares. Final assembly and initial bench testing will be conducted in a clean bench area of this room. Flight parts and compliance certificates will be inventoried and controlled from this area. An as built drawing file is being assembled.

SPREE SCHEDULE



PDR - MAY '88 / CDR - 3RD WEEK DEC '88 / DELIVERY - MAY '90 / FLIGHT - JAN '91

FIGURE QR7-1

Project No. F19628-87-C-0094	Date: 05-30-89	Dwg. No. D:\SPRFF\SCHEDULE

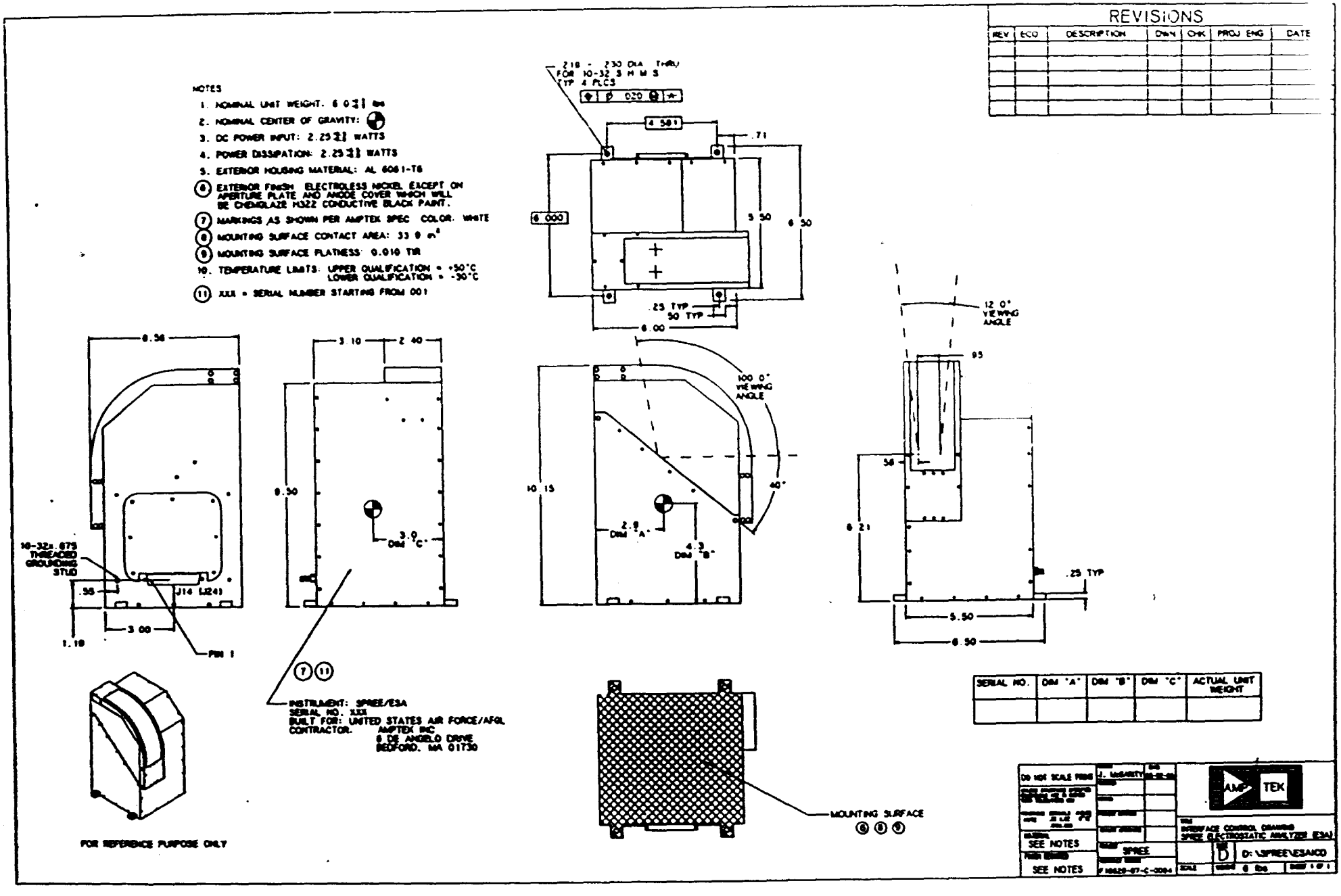

REVISIONS
REV | ECO | DESCRIPTION | DWN | CHK | PROJ ENG | DATE
NOTES
1. NOMINAL UNIT WEIGHT: 6 0 ± 1 lbs
2. NOMINAL CENTER OF GRAVITY:
3. DC POWER INPUT: 2.25 ± 1 WATTS
4. POWER DISSIPATION: 2.25 ± 1 WATTS
5. EXTERIOR HOUSING MATERIAL: AL 6061-T6
6. EXTERIOR FINISH: ELECTROLESS NICKEL EXCEPT ON APERTURE PLATE AND ANODE COVER WHICH WILL BE CHEMGLAZE M322 CONDUCTIVE BLACK PAINT.
7. MARKINGS AS SHOWN PER AMPTEK SPEC COLOR: WHITE
8. MOUNTING SURFACE CONTACT AREA: 33.9 in²
9. MOUNTING SURFACE FLATNESS: 0.010 TIR
10. TEMPERATURE LIMITS: UPPER QUALIFICATION = +50°C LOWER QUALIFICATION = -30°C
11. XXX = SERIAL NUMBER STARTING FROM 001
.218 - .230 DIA THRU FOR 10-32 S M M S TYP 4 PLCS
.020
4.501
.71
6.000
5.50
6.50
.25 TYP
.50 TYP
6.00
8.56
3.10
2.40
8.50
3.0 DIM "C"
10-32±.675 THREADED GROUNDING STUD
.55
J14 (J24)
3.00
1.19
PIN 1
100.0° VIEWING ANGLE
10.15
40°
2.9 DIM "A"
4.3 DIM "B"
12.0° VIEWING ANGLE
.95
.56
6.21
.25 TYP
5.50
6.50
7 11
INSTRUMENT: SPREE/E3A
SERIAL NO. XXX
BUILT FOR: UNITED STATES AIR FORCE/AFGL
CONTRACTOR: AMPTEK INC
6 DE ANGELO DRIVE
BEDFORD, MA 01730
FOR REFERENCE PURPOSE ONLY
MOUNTING SURFACE
6 8 9
SERIAL NO. | DIM "A" | DIM "B" | DIM "C" | ACTUAL UNIT WEIGHT
DO NOT SCALE PRINT
SEE NOTES
SEE NOTES
J. McGARITY
SPREE
AMPTEK
INTERFACE CONTROL DRAWING
SPREE ELECTROSTATIC ANALYZER (E3A)
D: \SPREE\E3AICD
D

FIGURE QR7-2

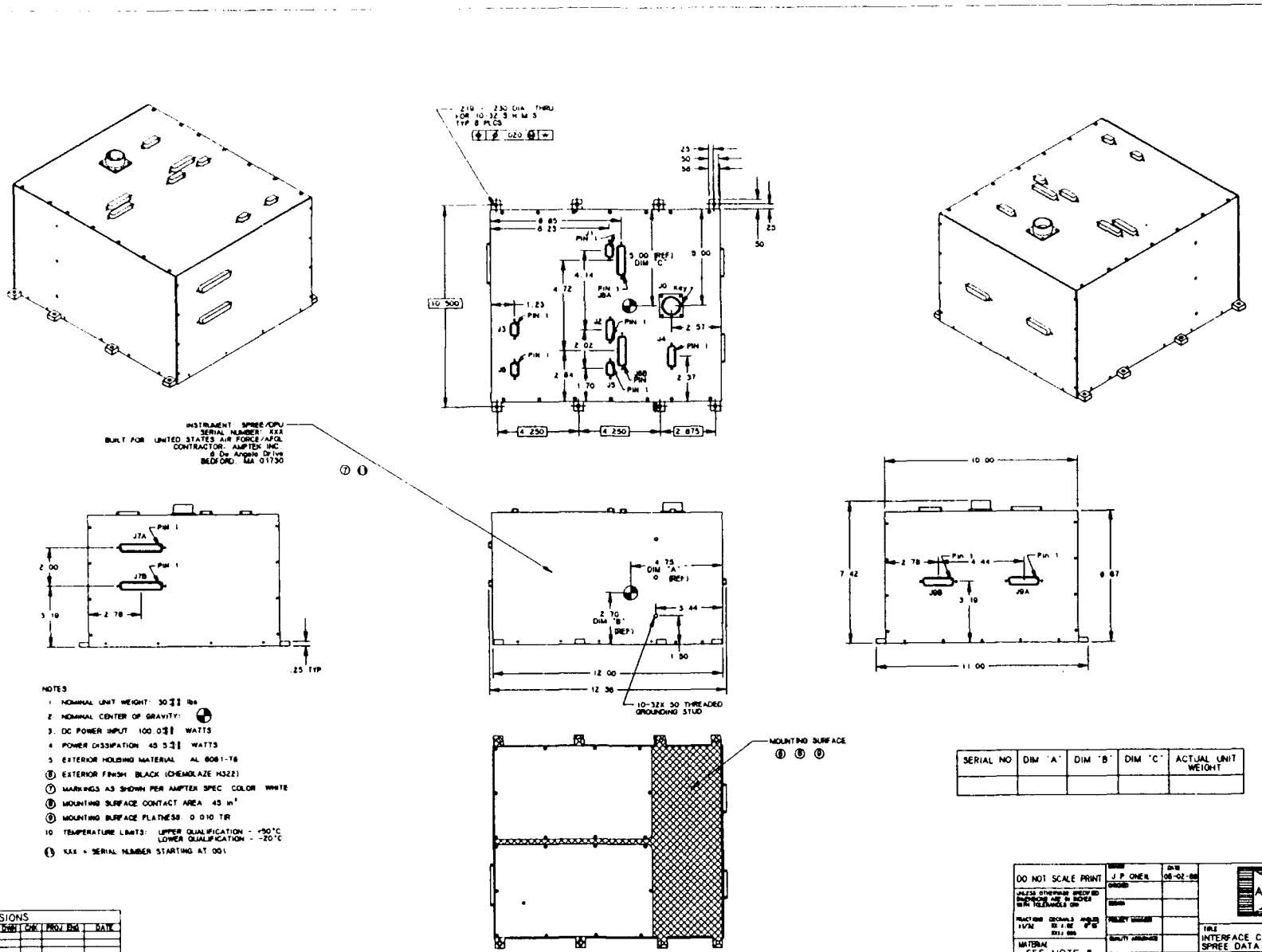
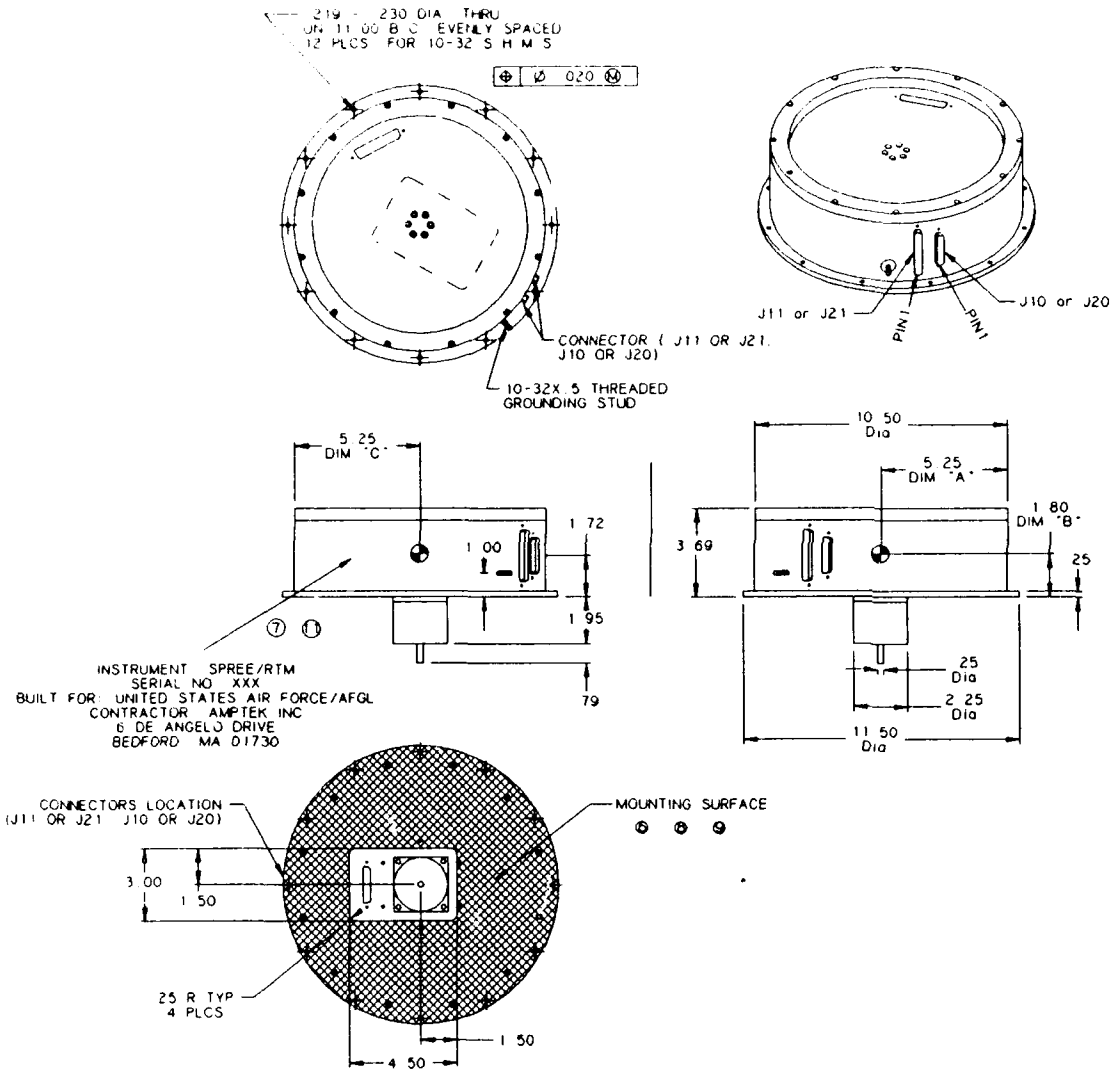

INSTRUMENT SPREE/DPU
SERIAL NUMBER: XXX
BUILT FOR UNITED STATES AIR FORCE/AFOL
CONTRACTOR: AMPTEK INC.
6 De Angelo Drive
BEDFORD, MA 01730
NOTES
1 NOMINAL UNIT WEIGHT: 30 ± 1 lbs
2 NOMINAL CENTER OF GRAVITY:
3. DC POWER INPUT 100.0 ± 1 WATTS
4 POWER DISSIPATION 45 5 ± 1 WATTS
5 EXTERIOR HOUSING MATERIAL AL 6061-T6
6 EXTERIOR FINISH BLACK (CHEMOLAZE H322)
7 MARKINGS AS SHOWN PER AMPTEK SPEC COLOR WHITE
8 MOUNTING SURFACE CONTACT AREA 45 in²
9 MOUNTING SURFACE FLATNESS 0 010 TIR
10 TEMPERATURE LIMITS: UPPER QUALIFICATION - +50°C
LOWER QUALIFICATION - -20°C
(11) XXX = SERIAL NUMBER STARTING AT 001
10-32X .50 THREADED GROUNDING STUD
MOUNTING SURFACE
SERIAL NO
DIM "A"
DIM "B"
DIM "C"
ACTUAL UNIT WEIGHT
REVISIONS
DO NOT SCALE PRINT
J P ONEIL
06-02-88
MATERIAL
SEE NOTE 5
FINISH REQUIRED
SEE NOTE 6
SPREE
F19628-87-C-0094
AMPTEK
TITLE
INTERFACE CONTROL DRAWING
SPREE DATA PROCESSING UNIT (DPU)
SIZE
D
D:\SPREE\DPUICD
SCALE
WEIGHT
SHEET 1 OF 1

FIGURE QR7-3



REVISIONS						
REV	ECO	DESCRIPTION	DWN	CHK	PROJ ENG	DATE

NOTES:

1. NOMINAL UNIT WEIGHT 14 7/8 lbs
2. NOMINAL CENTER OF GRAVITY ⊕
3. DC POWER INPUT 2.25 WATTS
4. POWER DISSIPATION: 2.25 WATTS
5. EXTERIOR HOUSING MATERIAL: AL 6061-T6
6. EXTERIOR FINISH: ELECTROLESS NICKEL
   TURNTABLE: BLACK (CHEMGLAZE H322)
   MOUNTING PLATE TOP: BLACK (CHEMGLAZE H322)
   STEPPER MOTOR CASE: BLACK ANODIZE
7. MARKINGS AS SHOWN PER AMPTEK SPEC COLOR WHITE
8. MOUNTING SURFACE CONTACT AREA 88.9 in^2
9. MOUNTING SURFACE FLATNESS: 0.010 TIR
10. TEMPERATURE LIMITS: UPPER QUALIFICATION = +50°C
    LOWER QUALIFICATION = -30°C
11. XXX = SERIAL NUMBER STARTING AT 001
12. THE ROTARY TABLE IS COUPLED TO THE STEPPING MOTOR USING A 100:1 HARMONIC DRIVE. THIS LARGE STEP-UP / STEP-DOWN RATIO PROVIDES ANTI ROTATION TO THE ROTARY TABLE WHEN POWER IS OFF DUE TO THE BACK EMF INDUCED IN THE MOTOR WINDINGS BY ANY TABLE MOTION

SERIAL NO	DIM "A"	DIM "B"	DIM "C"	ACTUAL UNIT WEIGHT

DO NOT SCALE PRINT

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES WITH TOLERANCES ON

FRACTIONS ±1/32 DECIMALS .X ±.02 .XX ±.01 ANGLES ±1° .XXX ±.005

MATERIAL: SEE NOTES

FINISH REQUIRED: SEE NOTES

DRAWN: J P ONEIL 08-02-89

CHECKED

ENGR

PROJECT MANAGER

QUALITY ASSURANCE

PROJECT: SPREE

CONTRACT NUMBER: F19628-87-C-0094

AMPTEK

TITLE: INTERFACE CONTROL DRAWING SPREE ROTARY TABLE (RTM)

SIZE: D

D:\RTM\RTMICD

SCALE

WEIGHT: 14 lbs

SHEET 1 OF 1

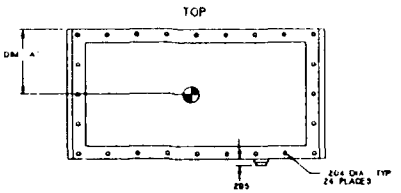
FIGURE QR7-4

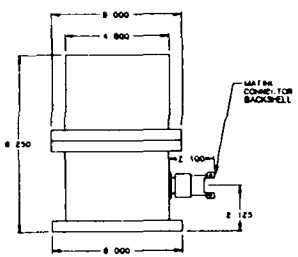
REVISIONS					
REV	ECO	DESCRIPTION	CHK	PROJ ENG	DATE

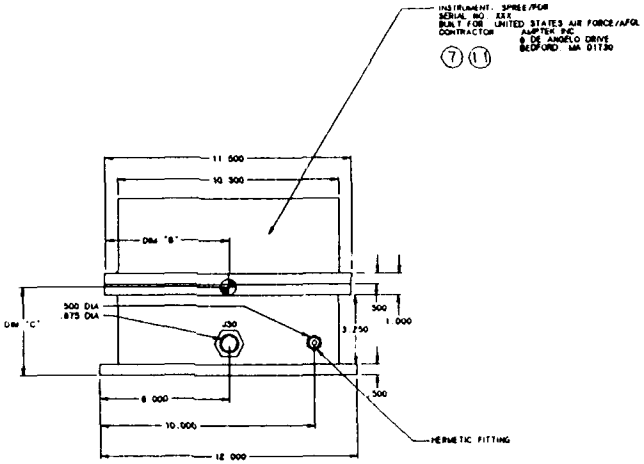
NOTES

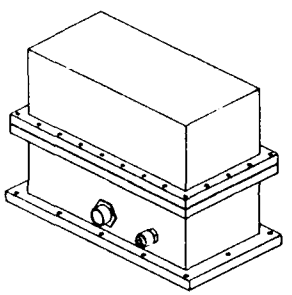
1. NOMINAL UNIT WEIGHT 27 +3.0 -3.0 lbs
2. NOMINAL CENTYER OF GRAVITY ⊕
3. DC POWER INPUT 40.0 +0.0 -2.0 WATTS
4. POWER DISSIPATION 40.0 +0.0 -2.0 WATTS
5. EXTERIOR HOUSING MATERIAL AL 6061-T6
6. EXTERIOR FINISH ELECTROLESS NICKEL
7. MARKINGS AS SHOWN PER AMPTEK SPEC COLOR WHITE
8. MOUNTING SURFACE CONTACT AREA 29.1 in^2
9. MOUNTING SURFACE FLATNESS 0.010 TIR
10. TEMPERATURE LIMITS UPPER QUALIFICATION = +50°C
    LOWER QUALIFICATION = -6°C

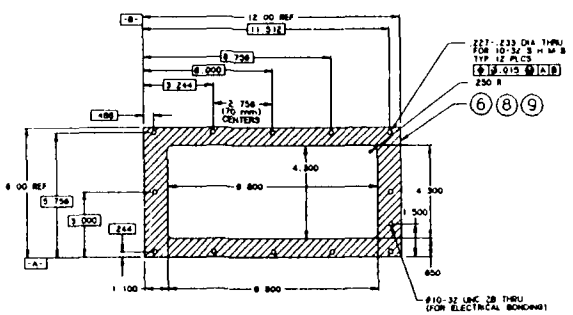
(11) XXX = SERIAL NUMBER STARTING AT 001











BOTTOM

SERIAL NO	DIM "A"	DIM "B"	DIM "C"	ACTUAL UNIT WEIGHT
	3.00	5.75	4.125	

FIGURE 0R7-5

DO NOT SCALE PRINT	DRAWN J P O'NEIL	DATE 08-02-88	AMPTEK
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES WITH TOLERANCES ON	CHECKED		TITLE INTREFACE CONTROL DRAWING SPREE FLIGHT DATA RECORDER (FDR)
FRACTIONS DECIMALS ANGLES ±1/32 .XX ±.02 ±1° .XXX ±.005	ENGR W EVEREST	10-24-88	
MATERIAL AL 6061-T6	QUALITY ASSURANCE		SIZE D
FINISH REQUIRED SEE NOTE 6	PROJECT SPREE		D:\FDR\FDRICD
	CONTRACT NUMBER F19628-87-0094		SCALE 1:1 WEIGHT 13.5 LBS SHEET 1 OF 1

NESTED HEMISPHERE ESA DESIGN

The aluminum deflection plates were machined this quarter. A dimensional error was discovered during assembly which has required the re-work of one hemisphere size. The machining for the rest of the nested hemisphere assembly is complete and is ready for surface treatment and plating to minimize scattering inside the plates.

The production of the trapezoidal microchannel plates (MCPs) by Galileo Electro-Optics seems to be on schedule. Amptek, Inc. is providing test fixtures to evaluate the MCPs. These test fixtures are simply the anode holders intended for the flight units and prototype.

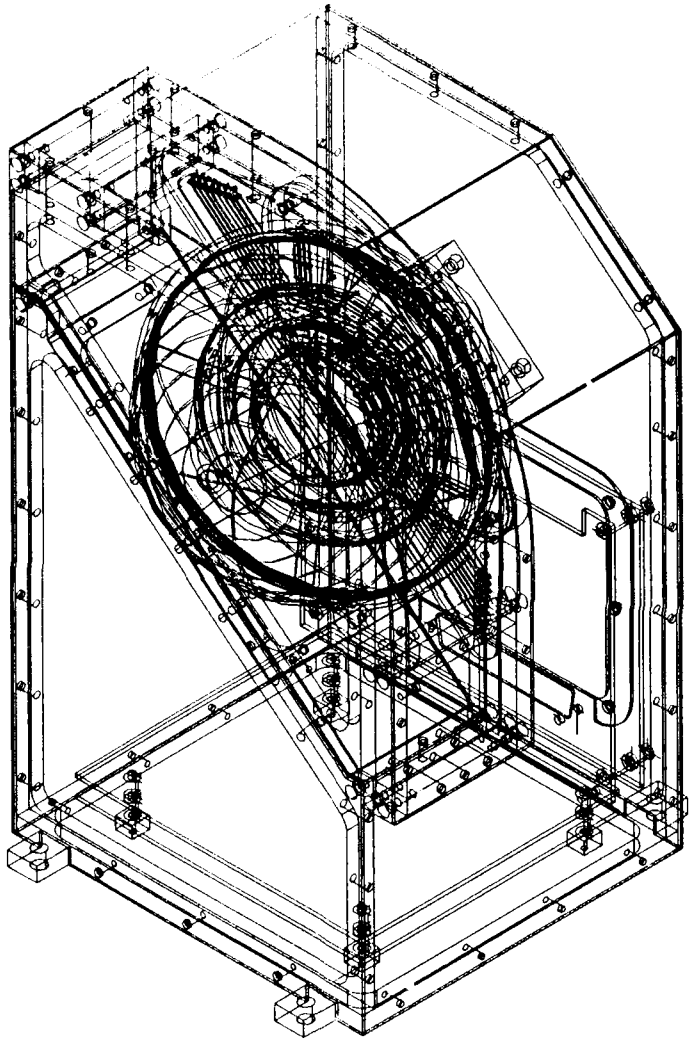
The anode and ground plane printed circuit boards have been manufactured as well as the MCP mount and holder. Dummy MCPs have been made from glass to test the holders mechanical characteristics before committing to the mounting of expensive flight MCPs. The glass dummy MCPs seem to work fine and the structure is rugged enough for spaceflight.

Due to new calculations of particle trajectories in orbit, a screened structure was placed in front of the ESA design. The Debye length at this altitude turns out to be of the same order as the ESA dimensions, and this could cause serious trajectory distortions to particles flying close to the anode cover plate. The added screens extend the instrument's ground sheath to an area above the anode cover plate, thus minimizing perturbing incoming particle trajectories.

A grounding stud was added to the ESA housing to insure proper housing grounding during flight.

All of the ESA housing components have been designed and are being machined.

The amplifier/buffer card for the ESA was designed and fabricated. It is undergoing tests for cross talk and shielding.



SPREE ESA WIRE FRAME MODEL

FIGURE QR7-6

DATA PROCESSING UNIT FOR 270 DEGREE NESTED SENSORS

Much of this quarter was spent building and testing SPACE components. The SPACE CPU engineering model was built and tested. A prototype of a MCU module was built and tested. Both of these units are being evaluated by Paul Gough and upon his approval, flight boards will be manufactured.

Attached to this report is a copy of functional descriptions and technical details of the Space CPU and MCU. This document was provided Dr. Gough as part of the engineering models.

The design of the high-frequency buncher modules is nearly complete. One will be sent to Paul Gough for evaluation early this quarter.

A preliminary Software Requirements Document (SRD) was written for SPACE. It defines the memory map, control port operations and other necessary details. It will continue to evolve as the hardware is completed.

A single-chip data compressor was designed and tested. It will be used to compress telemetry and recorder data, and will be included on the recorder interface board.

The entire recorder interface has been breadboarded and a layout will be performed pending operational verification.

The high-speed high voltage sweep rate for the analyzers has been changed from 10 sweeps/sec to 8 sweeps/sec. A number of factors led to this decision, including processing overhead, SPACE data bandwidth, and telemetry formatting.

An updated ICD drawing for the DPU showing correct connector types and locations was generated and forwarded to MMAG.

Spacecraft Particle Correlator Experiment (SPACE)

I. Overview

Data Rates

There are two data rates for the particle correlator, depending on which operating mode the analyzers are in. The telemetry is broken down as follows:

The DPU/Recorder interface operates at 16,384 bytes/sec (131,072 bits/sec). Of this, 384 bytes/sec (3072 bits/sec) are set aside as overhead in the form of sync words, frame counters, housekeeping data, GMT and magnetometer data. This leaves 16,000 bytes/sec (128,000 bits/sec) available to be shared by the analyzers and SPACE.

In the 8 sweep/sec mode, the analyzers generate 10,240 bytes/sec (81,920 bits/sec). [2 units x 2 species x 10 zones x 32 steps/sweep x 8 sweeps/sec x 1 byte/sample][1]. In this mode, SPACE is allocated 5,760 bytes/sec (46,080 bits/sec) which is the difference between the data rates of the recorders and the analyzers.

In the 1 sweep/sec mode, the analyzers generate 1,280 bytes/sec (10,240 bits/sec). [2 units x 2 species x 10 zones x 32 steps/sweep x 1 sweep/sec x 1 byte/sample]. In this mode, SPACE is allocated 14,720 bytes/sec (117,760 bits/sec).

Any data which is to be included in the real-time data stream is included in these allocations. The R/T data will be extracted from the SPACE data stream. The size of the R/T data block and its location in the data is TBD.

To summarize:

	1 sweep/sec	8 sweep/sec
Recorder data rate	16,000 bytes/s	16,000 bytes/s
Analyzer data rate	1,280 bytes/s	10,240 bytes/s
SPACE data rate	14,720 bytes/s	5,760 bytes/s

THESE ALLOCATIONS ARE EXACT AND INCLUDE ALL SPACE OVERHEAD, SUCH AS SYNC WORDS OR FRAME COUNTERS. Any handshaking or sync data which does not need to be recorded is not counted in this allocation.

II. SPACE CPU

The SPACE CPU is a single-board microcomputer based on the Harris 8 MHz 80C86 microprocessor. It consists of:

(1) 80C86-2, the microprocessor
(1) 82C84A, the clock generator
(2) EP320, the memory decoding logic
(2) 54AHCT373, the address latches
(2) 54HC245, the data bus transceivers
(2) 27C64, the 8k x 8 EPROMs for program storage and lookup tables
(2) HM8832, the 32k x 8 RAMs for data storage and buffering
(2) 82C54, the triple counter/timers
(1) 82C59A, the interrupt controller
(2) 7130/7140, the dual-port RAMs used for communicating with SPREE's primary CPU
(1) 54HC423, a monostable multivibrator used as a watchdog timer

CPU Tasks

The tasks of the SPACE CPU will be:

Gather data from the MCUs, the HF buncher modules and the beam counters
Select operating frequency for the HF bunchers
Select beam mode for beam counters
Assemble recorder and R/T data frames
Transmit data frames to primary CPU

[1] Each 16-bit count is log-compressed into a 4-bit exponent and a 4-bit mantissa to form 1 byte.

Translate magnetometer data
Synchronize all modules to HV clock
Write current HV step to MCUs
Select which zones are fed to all modules
Average data, if necessary

Memory Map

The memory map for SPACE is defined from 00000h through 1FFFFh, which stems from the fact that only address lines A0-A16 are decoded; A17-A19 are ignored.
The memory map for SPACE consists of the following (in hex):

00000-0FFFF[2]	RAM (32Kx16)
10000-107FF	82C59A-1 (Even addresses)
11000-117FF	82C54-1 (Odd addresses)
11800-11FFF	82C54-2 (•)
12000-127FF	MCU board #1 (See MCU description for details)
12800-12FFF	MCU board #2 (•)
13000-137FF	Beam counter board (See Beam description)
14000-15FFF	H.F. Buncher board (See HF Buncher description)
1B000-1B7FF	Watchdog timer (Even addresses)
1B800-1BFFF[3]	Dual-port RAM (1Kx16)
1C000-1FFFF[4]	EPROM (8Kx16)

Data transfer between the SPACE CPU and the primary SPREE CPU will occur in a block format through the dual port RAMs. Most likely, the data transfer will be initiated by the HV step clock, such that in the 8 sweep/sec mode, a transfer takes place at the end of a HV sweep (or the beginning of the next sweep). [This yields 720 bytes/block]. In the low speed mode, a transfer should take place after every four energy steps (8 transfers/sec). [This yields 1840 bytes/block].

The SPACE CPU should use the D.P. RAM interrupt word to signal the primary CPU that it is finished loading the data block. The interrupt word can also be used to transfer mode information, frame counters or other TBD data. Likewise, the primary CPU will use the interrupt word to signal mode changes, HV sweep information, AMAG data if available, and other TBD data. It will also acknowledge transfers through this word. The actual handshaking is TBD.

Timer and Interrupts

Each of the 82C54s contains three counters. Channel 0 of counter #2 (U9) is used as a prescaler; that is, it divides the 4 MHz input clock to something more manageable and feeds it to the other 5 channels. A divisor of 125_{10} gives an output of 32,000 Hz which is a convenient frequency. Timer mode 3 generates a square wave, which is probably appropriate for most uses.

The outputs of the other 5 channels can be used for various purposes. Channel 1 of U9 drives IR2 of the 82C59A and also drives the backplane. Channel 2 drives IR2 (currently the highest priority clock interrupt.) The three channels of U14 all drive the backplane. The table below shows the timer channels and their destinations:

[2] The first 64 bytes are reserved for interrupt vectors; the last 256 bytes are reserved for the system stack.

[3] Writing to the last word of D.P. RAM generates an interrupt at the main CPU. Reading from the last word resets the interrupt from the main CPU. See D.P. RAM data sheet for details.

[4] EPROM locations 1FFF0-1FFFF are reserved for the system reset vector.

Timer & Channel	Destination
U9:0	Prescaler; drives other counters
U9:1	IR2 and J1.42
U9:2	IR1
U14:0	J1.8[5]
U14:1	J1.10
U14:2	J1.12

The 82C59A interrupt control has 8 interrupt inputs. The table below shows the source of each interrupt:

Interrupt Level	Source
IR0	IRQ0 (Backplane)
IR1	U9, Channel 2
IR2	U9, Channel 1
IR3	HVCLK (HV step from SPREE)
IR4	IRQ2 (Backplane)
IR5	IRQ3 (Backplane)
IR6	Dual-port RAM interrupt
IR7	DR (serial Interrupt from MCUs)

The 82C59A interrupt controller is a very flexible peripheral; as such, it has numerous configuration options.[6] The recommended configuration is:

1. ICW1=00010011b. This selects the edge triggered interrupt mode and a single 82C59A. Edge triggering is mandatory since the interrupt signals from the clocks may have very long pulse widths.
2. ICW2=00001000b. This tells the 82C59A to generate interrupt vectors 8-15 for IR0-7. This is because the 80C86 reserves INT 0-INT 7 for internal interrupts such as *NMI* and *Overflow*.[7]
3. ICW3=N/A. This Initialization Command Word isn't needed.
4. ICW4=00000001b. This selects the Non-buffered Mode, the Normal End-of-Interrupt (EOI) Mode, and the 8086 mode. (The Automatic EOI may be appropriate is some circumstances. It should be used if possible because of its reduced overhead and ease of use.)

It should be noted that the Data Ready (DR) interrupt from the MCUs is generated by OR'ing together the DR outputs of the 82C52s on both MCU boards. Thus the interrupt routine needs to keep track from which MCU it expects data. This should be easy since the MCUs only send data after it is requested from them.

III. MCU Boards

The particle correlator contains two Microcontroller Unit (MCU) boards Both are constructed from identical PC boards with jumpers used to differentiate between them. Each consists of six MCU modules with appropriate interface logic.

Each MCU module consists of the following:

(1) 80C31BH-1, an 8-bit 16MHz CMOS microcontroller
(1) 87C64-1, an 8Kx8 CMOS EPROM
(1) 6116, a 2Kx8 CMOS SRAM
(1) 54HC373, an address latch

[5] The three channels of U14 can be independently gated and connected to the backplane by shorting the appropriate jumper between JP1 and JP8. Shorting all six jumpers enables all three counters and connects their outputs to the backplane. R7-R9 are not necessary when the corresponding jumpers are installed.

[6] See the 82C59A data sheet for a full explanation.

[7] See the 80C86 data sheet for details.

(1/2) 54HC423, a monostable for stretching the input pulses
(1/4) 54HC08, for address decoding

The interface logic consists of:
(1) 82C52, a serial port for I/O between the MCUs and the CPU
(1) 16.000 MHz crystal oscillator
(1) EP320, an EPLD for address decoding and control
(1) EP600, an EPLD for generating control signals

All communications between the SPACE CPU and the MCUs is through a serial channel controlled by the 82C52. The MCUs should be programmed to operate in serial mode #2, at 500 kHz. The 82C52 should use a divisor of 2 (16 MHz/2=8 MHz, which is internally divided by 16 to produce 500 kHz), 8 data bits, 2 stop bits and no parity [UCR=00111111b, BRSR=10000000b, MCR=00100000b][8]. Note that the 80C31 operates with 9 data bits in mode #2. Since the 82C52 doesn't support 9 data bits, it replaces the 9th bit with a stop bit (logic one). This means the 80C31 will always receive a one for bit 9. More importantly, bit 9 must be set high when the 80C31 transmits; otherwise the 82C52 will not correctly interpret the first stop bit.

The SPACE CPU sends commands to the MCUs via the 82C52. These commands include requests for serial data and information about the energy level. Because the serial output from the 82C52 is common to all six MCUs, it can broadcast the energy level with a single serial byte. For a serial request, however, the upper three bits should be decoded as an address by the individual MCUs. A possible command scheme is as follows:

Function	Serial Command
New energy level (all MCUs)	000xxxxxb ('xxxxx' is the energy level)
MCU #1 serial request	00100000b
MCU #2 serial request	01000000b
MCU #3 serial request	01100000b
MCU #4 serial request	10000000b
MCU #5 serial request	10100000b
MCU #6 serial request	11000000b
Broadcast command (all MCUs)	111yyyyyb ('yyyyy' is a specific command)

Other MCU commands can be created as needed by replacing the lower 5 bits with the appropriate code.

Note: at 500 kHz, it takes about 20uS to transmit a byte. If the serial port is used to signal a new HV step, the MCU won't recognize it until after the CPU has transmitted it and the MCU has received it [maybe as much as 40-50uS]. A more accurate timing method might be to use an interrupt pin to indicate a step has occurred, and use the serial command to verify the current HV level.

The EP320s are the main control logic for the MCU board. They generate MCU resets and demultiplex the serial outputs. The table below indicates how to perform these functions[9].

[8] Refer to Harris 82C52 data sheet for details. DR and TBRE are used as interrupt inputs of the 82C59A on the CPU board. INTR is not used which implies that serial exceptions (PE, FE, OE, RBRK) are ignored.

[9] Because only A0-A5 and A11-A16 are decoded for the MCUs, this address sequence will repeat itself every 32 bytes throughout the decoded address range.

MCU Base Address+	Read	Write
0,8[10]	82C52 RBR	82C52 TBR
2,10	82C52 USR	82C52 UCR
4,12	82C52 MCR	82C52 MCR
6,14	82C52 MSR	82C52 BRSR
16	Select MCU #1	Reset MCU #1
18	Select MCU #2	Reset MCU #2
20	Select MCU #3	Reset MCU #3
22	Select MCU #4	Reset MCU #4
24	Select MCU #5	Reset MCU #5
26	Select MCU #6	Reset MCU #6

IV. High-Frequency Buncher Board

The high-frequency buncher board consists of six high-frequency buncher modules (HFB), plus interface logic. Although the final design has not been completed, each HFB will most likely consist of:
(1) EP1800, an EPLD
(1) EP600, another EPLD
(2) 6116, 2k x 8 CMOS SRAMs
(1) EP320, programmed as an 8-bit counter

HFB Memory Map

The HFB board is mapped as follows:

Address	Function
14000-14FFF	Selected HFB memory
15000	HFB control port #1 (8-bit)
15001	HFB control port #2 (8-bit)

Each HFB module contains 2k x 16 static RAM, which accumulates data in the following format:

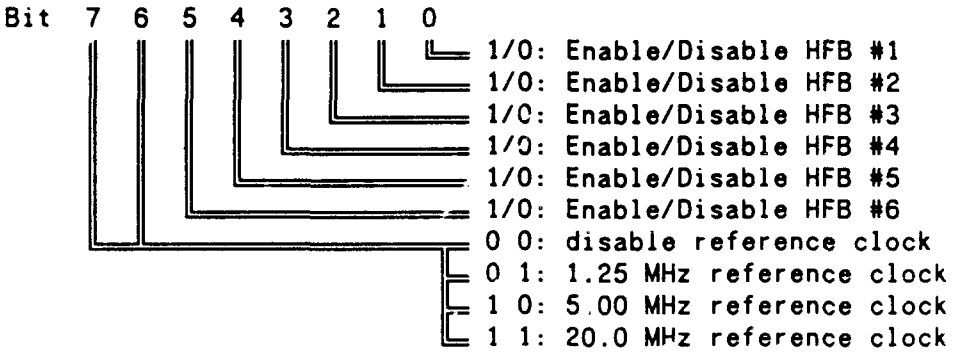
Address	Value
14000	Lag 0, Energy 0 (16-bit word)[11]
14002	Lag 1, Energy 0 (16-bit word)
14004	Lag 2, Energy 0 (16-bit word)
.	
1407E	Lag 63, Energy 0 (16-bit word)
14080	Lag 0, Energy 1 (16-bit word)
14082	Lag 1, Energy 1 (16-bit word)
.	
14FFC	Lag 62, Energy 31 (16-bit word)
14FFE	Lag 63, Energy 31 (16-bit word)

(i.e. Address = Base + (Energy * 80h) + (Lag * 2)

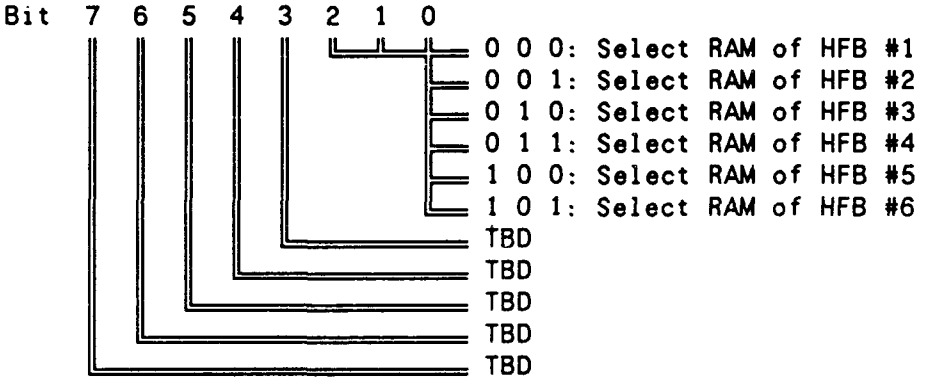
The control ports are write-only; that is, their status cannot be read back. Control port #1 is decoded as follows:

[10] Refer to the Harris 82C52 data sheet for addressing details. Also, because A0 is not used in addressing the 82C52, and because the 82C52 is located on the lower half of the data bus, all accesses to it must be at an even address. The addressing is redundant because A3 is not decoded by the 82C52.

[11] The LSB will be at even addresses (which is the lower half of the data bus) and the MSB will be at odd addresses (the upper half).



(i.e. Port=00h: clock and HFBs disabled; port=FFh: 20 MHz clock, HFBs enabled)
Control port #2 is decoded as follows:



V. Beam Modulation and Zone Select Board

This board hasn't been finalized yet. It will also have to contain the beam sync interfaces and the beam select logic. I'll do my best to squeeze everything onto the board, but I suspect something will have to shrink, i.e the number of beam counters. As of yet, the address space and content of this board are TBD.

Operational Notes for the SPACE MCU Prototype

1. I've included some wirewrap connectors so you can connect this module to whatever system you like.
2. I tried to make the addressing of the MCU as generic as possible. There are 3 address lines (A1-A3), /RD, /WR and 5 chip select lines. Three of the CS lines are active high, the other 2 are active low. All five have pull-ups or pull-downs into their active state. You can use whatever you like for these signals (i.e. upper address lines, etc.) and leave the unused ones disconnected. You should use at least one of the CS lines, though, or the module will always be selected.
3. The 82C52 is selected when A3 is high and the CS lines are properly conditioned.
4. The MCU is reset by a write to address 0 (A3=A2=A1=0), or by an external RESET.
5. /INT0, /INT1, and T1 have pull-ups and RESET has a pull-down. They can be left unconnected if they are not used.
6. The COUNT line fires a 750 nS one-shot on the rising edge. Any reasonable frequency or duty cycle can be used.
7. The actual one-shot pulse widths are longer than shown on the schematic. You should check these if the widths are critical to you.
8. Make sure you use the 87C64 EPROM, not the 27C64. The 87C64 has address latches built into it. For your EPROM programmer you should select '27C64' or '2764A' when programming the 87C64 or the 27C64.
9. Refer to the SPACE hardware overview for the recommended 82C52 configuration.
10. One nice trick is to use the port 1 pins to trigger your scope or logic analyzer to aid in debugging. For instance if you want the logic analyzer to trigger when an interrupt routine is finished, have the routine toggle one of the pins. It's much easier than triggering on an address, etc.

Operational Notes for the SPACE CPU Engineering Model

These notes are intended to clear up some questions that the schematic doesn't answer and to provide some hints as to how to make the thing work!

1. The ROM sockets are marked 'L' and 'H'. The 'L' refers to 'LOW' and means this ROM should contain data at even address, which is equivalent to the low half of the data bus (D0-D7). The 'H' refers to 'HIGH', and that ROM should contain data for the odd addresses, or the high half of the data bus (D8-D15). If this isn't clear, the 80C86 data sheet explains how the processor decodes memory accesses using A0 and BHE to condition the bus.
2. The empty chip locations in the middle of the board are for SPREE PROMs, which aren't needed for SPACE.
3. The empty locations next to the 82C59A is for a second 82C59A. It shouldn't be necessary for SPACE, but it can be included if it is needed.
4. I have included two Hypertronics connectors for use when the CPU board is being operated by itself. The connector for J2 straps /CS, /RD, /WR and the address inputs of the dual-port RAMs to +5v. (This connector has a clip on it which should be connected to the +5v side of C27). The connector for J1 straps the IRQx inputs to ground. These connectors are polarized so you can tell which one goes where.
5. The watchdog timer is simply a one-shot with a long timer period. The software periodically resets the timer by performing a read at the watchdog address. If the timer is not reset, it will perform a Non-Maskable Interrupt (NMI). The duration of the one-shot is about one second; i.e. the timer must be reset more often then once per second to keep the timer from firing. It is probably inconvenient to use the timer during software development, so removal of JP5 will disable it.
6. JP4 controls the timing of wait-state generation. You should leave it open unless I tell you otherwise. (Or you discover it is necessary.)
7. Don't be too concerned about the ratty appearance of this board. It's only an engineering model!
8. **If you find it necessary to make any changes on the board, please document them carefully and let me know about them!**
9. I've included photocopies of the artwork in case you need to make modifications. Refer to note 8!
10. U24 is used to buffer control signals to the backplane. It currently has 5 unused buffers so feel free to use it if necessary. Most likely a slower part will replace this because this family of parts is so fast they tend to cause noise problems on the ground tracks. (T_{pd}=4.5nS Typ, with very fast rise and fall times)
11. JP3 is to be used to connect signals to the unused pins of J1 if desired.
12. R7-R9 are needed only if you decide to disable one or all of the U14 counters. Otherwise they are not needed.
13. If you want to use one of the counters to track the HV step, you would:
    A. Disable the output by inserting the appropriate resister (R7-R9)
    B. Cut the trace which connects U9 pin 10 to the clock input.
    C. Connect the HVCLK signal to the clock input.
    D. Strap the gate input (G0-G2) appropriately.
    E. Program the counter.
    (You might need to invert HVCLK, depending on its polarity, which is currently TBD)
14. I've included for your reference the diagnostic software I wrote. The easiest way to verify its operation is to watch timer 2 channel 2 with a scope. The frequency starts at 1 Hz, doubles every second for 16 seconds, then starts over. This is what the software does:
    A. Initialize the segment registers.
    B. Initialize the interrupt table.
    C. Initialize the counters. Counter 2 channel 0=32kHz. Counter 2 channel 1=1 Hz (This is used to generate interrupt 2.)

D. Initialize the interrupt controller.
E. Start the watchdog timer and perform a memory test on the dual-port RAMs.
F. Perform a memory test on the main RAM.
G. Loop to step E.

In the mean time, Counter 2 channel 1 generates an interrupt once per second. The interrupt routine doubles the frequency of counter 2 channel 2 until it reaches 16 kHz, at which point it starts over at 1 Hz.

A failure in either memory test will place the CPU in a HALT condition. If the output of the watchdog timer is enabled, it will restart the program after a crash. (You can simulate a crash by shorting two data lines together.)

15. Segmentation is a very tricky subject. After quite a bit of experimentation, I think the best way to set up your memory segments is as follows:

A. Use a 'segment at 0' statement to set up any variables or tables you want to keep in memory that you would like to access by variable name. (Not necessary for objects you address directly.)

B. Use a 'segment at 1000h' statement to set up the ports for the peripherals.

C. Use a plain 'segment' statement to set up the executable part of the code. This doesn't explicitly define which segment the code will occupy, which is OK. The memory decoding is what locates this segment. When programming the EPROMs, program locations 0000h-3FFFh. The reset vector is what actually tells the CPU in which segment the code is located. The JMP 1C00:0100 statement sets CS=1C00 and IP=0100. (i.e. the code starts at address 100h in the EPROMs. You can change the offset as you see fit).

D. The 'assume' statement can reduce the overall size of the code if used correctly. The assume statement doesn't generate any code. Rather it informs the assembler where the segment registers are pointing. In my diagnostic program, the first assume statement is 'assume cs:code,ds:data,es:data,ss:data.' This means that I set CS=1C00 (my code segment) and that I set ds=es=ss=0000 (my data segment).

The reason the assume statement is necessary is that all instructions use a particular segment register by default. For example, all jump and call instructions calculate the physical address relative to the Code Segment (CS). All memory address references using the BX, SI or DI registers are made relative to the Data Segment (DS). All string instructions using the DI register (STOS, SCAS, MOVS, CMPS) are made relative to the Extra Segment (ES). Finally, all stack operations are made relative to the Stack Segment (SS).

The way in which the assume statement can reduce program size is as follows:

Say, for example, that the following program is being assembled.

```
data        segment at 0
variable    dw      ?
.
.
data        ends
.
code        segment
.
.
mov         word ptr [variable],ax
.
.
code        ends
```

If DS=0 (the location of the segment 'data') and the statement 'assume ds:data' was issued, then the statement is assembled normally. If the assume statement isn't there or isn't referenced to 'data' then the assembler would use whichever segment referenced 'data'. For example, if 'assume ds:nothing,es:data' was entered, the following instruction would be assembled:

```
mov             word ptr es:[variable],ax
```

which requires an extra byte of program space. The most important aspect of the assume statement is to make sure that you set the segment registers so they agree with your assume statements (or make your assume statements agree with the register assignments).

Warning: Be very careful changing the segment registers while interrupts are enabled. If an interrupt handler is referencing memory relative to a segment register which has the wrong value, a crash is imminent!

[I included this discussion because the assume statement is the most confusing aspect of 8086 programming I came across. Whether this helps or further confuses the issue I'm not sure!]

Give me a call if you have any questions on this. I undoubtedly left something out, so good luck!

Particle Correlator

Work of consultant: Dr. Paul Gough, Brighton, UK

The hardware design is nearly done. Breadboard models are expected soon to arrive from the United States. These bread boards will be used to verify the software. At this time the 80C51 software is fully written but untested. Work has been begun on the 80C86 software code for the particle correlator.

Attached is a full description of the SPREE particle correlator including operational modes and scientific aims.

SHUTTLE-TETHER : SPREE PARTICLE CORRELATOR

ABSTRACT

This document describes the particle correlator component of the SPREE Instrument to be flown on the Shuttle Tether Mission. These instruments measure electrons and ions with energies from a few eV to a few tens of keV. SPREE will be located in the Shuttle bay during the Tether mission scheduled for the first quarter of 1991. The aim is to make plasma and wave-particle diagnostic measurements when the tethered satellite is deployed and during the operation of the FPEG and DCOR electron guns, also located in the shuttle bay. This mission involves some 30+hours of operation with data being stored on-board.

The particle correlators will study wave-particle interactions, both those occurring naturally, and those man-made as a result of the electron guns, the space tether, and the shuttle plasma interaction.

BACKGROUND

Wave-particle interactions are important as they are one of the few processes by which energy can be exchanged between the different particle populations in the collisionless plasma at shuttle altitudes. Much work has been done on the naturally occurring electron and ion beam plasma interactions, e.g. auroral beams and conics. Active shuttle experiments using particle correlators with particle spectrometers as diagnostic tools enable wave-particle interactions to be studied under controlled, or partially controlled conditions. Such measurements will therefore contribute significantly towards our understanding of naturally occurring geophysical phenomena.

When particles are in velocity resonance with waves, either particle energy is transferred to the waves resulting in wave amplitude growth and particle dececeleration, or wave energy is transferred to the particles resulting in particle acceleration and wave damping. In either case particles in velocity resonance will become phase bunched with the wave. This is observable as fluxes at the resonant energy being modulated at the relevant frequency. Measurements of these modulations as a function of frequency, energy level, particle charge, and direction of arrival, allows us to identify directly by experiment those regions of particle velocity space contributing to wave-particle interactions.

In the case of the shuttle tether mission there will be both natural and artificial electron populations contributing to these interactions. Furthermore the electron guns are modulated in time. Modulations are therefore expected at the natural wave frequencies determined by the local plasma parameters, at the beam modulating frequencies, and at periods determined by the electron beam geometry in the geomagnetic field (gyration, local reflection, and magnetic field bounce times).

Several methods of analysis are included here to cover the frequency ranges and to utilise on-board the actual beam modulation waveform.

The SPREE Spectrometers

There are two separate SPREE spectrometer units located in the shuttle bay. Each unit consists of combined electron and ion analysers which are rotated through 180o every 30s. Analysers are of the 270o type ,having fields of view of 100o by 10o using ten detection zones of 10o x 10o. As a result of their wide entrance fan and their rotation, the field of view approaches the maximum of 2 pi, subject to limits imposed by shaddowing from other units in the shuttle bay. All four analysers provide ten (angular) fast detection pulse streams to the particle correlators for analysis. Three streams from each analyser are chosen with each stream being analysed by the three techniques described below. (Only two techniques for the ions) The choice of stream is either by a sequence designed to give a complete scanning of all angles, or can be chosen by the controlling DPU to study a particular direction: e.g. along the field line, parallel to the active electron gun, perpendicular to the field line, perpendicular to the active gun.

Expected Frequencies and Techniques

As stated above the type of correlation method depends on the expected frequencies of modulation:

a)High Frequency 0-10 MHz

Electrons(only) are expected to undergo interactions with waves at these high frequencies: the local upper hybrid frequency, Fuh (1-7MHz), the local electron gyro-frequency, Fg (1-1.5MHz location dependant),and associated Bernstein waves(n+1/2)Fg. At these high modulation frequencies the one bit 'buncher' mode is ideal.

This method involves the measuring of the time separation between successive electrons being detected in units of a 20MHz clock(for 10MHz) Histograms of the number of occurrences of separations measured in units of 50ns are accumulated for the different electron energy levels. This method is equivalent to averaging many one bit autocorrelation functions, each with only two bits set. As autocorrelation functions essentially measure periods this technique will also measure the times between electron gun pulses and returning electrons, either after one gyration or after any local reflection by shuttle related sheath fields. FPEG gun modulation patterns have been designed with this 'electron radar mode' in mind.

The clock rate is selectable between 20,5,&1.2MHz to give frequency ranges of 0-10,0-2.5,& 0-0.625MHz respectively. As these autocorrelation functions are 64 lags long the above ranges correspond to measuring periods 0-3.2us, 0-12.8us, and 0-51.2us, with 50ns, 200ns,and 800ns resolutions respectively.

The hardware for this buncher analysis is based on ALTERA programmable logic arrays to measure time separations with static RAMs to hold the accumulated histograms.

b)Low Frequency 0-10kHz

This lower frequency range contains both the lower hybrid frequency, flhr and the ion gyrofrequencies, fgh+, fgo+, e.t.c. Naturally occurring modulations are expected both in the ion and electron count rates. One bit autocorrelation functions are calculated by separate single chip microcomputers. Each stream is connected to a 80C31 with an external 8Kx8 ROM and 2Kx8 RAM. These units use their internal event counters to sample the fast pulse streams as input to the ACFs. Data is output to the DPU via serial interfaces.

The frequency range of these ACFs is selectable: 0-10kHz,0-5kHz,0-1.25kHz, with respective frequency resolutions 320Hz,160Hz,40Hz, or period ranges 0-1.6ms,0-3.2ms,0-12.8ms with respective time resolutions 50us,100us,and 400us. These time periods also include typical electron bounce periods at the equator. (for a 1keV electron, 100km takes 0.5ms) Again FPEG gun modulation patterns have been designed to optimise this 'electron radar mode'.

c)Gun electron modulations

The FPEG electron gun can be modulated with a series of fast modulation patterns. Since the pattern is available on-board in real time it can be used to search in particle velocity space for gun related modulations. This may be the returning beam itself, or low energy secondaries produced by the beam, or particles that have been modified by beam generated waves.

Selected fast pulse streams are gated into two 16bit counters. One counter is enabled during gun on; the other being enabled during gun off Each pair of 16bit counters is provided by a single D400 (quad 8bit counters) directly accessed by the DPU. A separate D400 is used to count a reference (DPU) clock to determine precisely the proportion of time spent with the gun on. With the two measured counts for each selected stream it is then a relatively simple calculation by the DPU to estimate statistically the significance of any excess counts during gun on, assuming Poisson counting statstics.

Summary of Measurements

Frequency range	F	dF	Time period	T	dT	Distance	S(1keV electron)	dS
Low frequency:								
0- 1.25kHz		40Hz	0-12.8ms		400us	0-256km		8km
0- 5kHz		160Hz	0- 3.2ms		100us	0- 64km		2km
0- 10kHz		320Hz	0- 1.6ms		50us	0- 32km		1km
High frequency:								
0- 625kHz		10kHz	0-51.2us		800ns	0-1024m		16m
0- 2.5MHz		40kHz	0.25-12.8us		200ns	0- 256m		4m
0- 10MHz		160kHz	0.25 -3.2us		50ns	0- 64m		1m

SPREE modes and data

SPREE data is to be stored on-board in a EXABYTE digital (video) cassette drive at a rate of 128kbits/s or 16kbytes/s. The quantity of of this rate available to the particle correlators depends on the operation mode. There are two main SPREE modes envisaged:

i)10 energy sweeps per second
In this mode most of the data recorded is normal SPREE data. Some 2.2kbytes/s are still available for particle correlation data.

ii)1 energy sweep per second
In this mode most of the data recorded is particle correlator data. Some 14.8kbytes/s are used for particle correlation data.
There is also a direct real-time telemetry link to ground of 9.5kbits/s.

The use of these data rates is calculated here by first estimating the natural data blocks or frames of each technique:

Beam modulation:

2units x 3zones x 2species x (32 energy x 2bytes + 4 auxillary)= 816bytes

Low frequency:

2units x 3zones x 2 species x 32 energy x (32lag +4auxillary)= 13824bytes

High frequency:

2units x 3zones x 1 species x 32 energy x (64lag +4auxillary)= 13056bytes

Next the data quantity available per 180o rotation, 30s is calculated for the two sweep rate modes:

10sweep/s:	30s at 2.2kbytes/s	gives a total of	66 kbytes total
1sweep/s:	30s at 14.8kbytes/s	gives a total of	444 kbytes total

Then the allocation per technique and the resulting resolutions in time and rotation angle can be calculated:

10 sweeps/second

high frequency-	2 frames / 180o	sum over 15s or 90o	26112bytes
low frequency-	2 frames / 180o	sum over 15s or 90o	27648bytes
beam mod.	-16 frames / 180o	sum over 1.9s or 11o	13056bytes
		total=	66816bytes

66816bytes/30s = 2227 bytes/s or 17816bits/s

1 sweep/second

high frequency-	16 frames / 180o	sum over 1.9s or 11o	208896bytes
low frequency-	16 frames / 180o	sum over 1.9s or 11o	221184bytes
beam mod.	- 16 frames / 180o	sum over 1.9s or 11o	13056bytes
		total=	443136bytes

443136bytes/30s =14771bytes/s or 118170bits/s

These are examples of how such a data allocations might be used. The final figures depend on how much data the normal SPREE measurements need

Real-time telemetry link

Some 3-4kbits/s(say) are available for the correlator to transmit some status information or low time resolution data. Since the DPU has access to all data it may be best to transmit in turn the most recent frame from each of the three techniques. In this way the correct operation can be checked in real-time and the EGSE data display might also provide sufficent information to enable operating configurations to be modified during the mission. If the DPU was to send long time period averages the interesting data would probably be averaged out.

Standard Operating Cycle

The simplest Standard Operating Cycle SOC will be to cycle through all possible combinations of zones and frequency ranges. This SOC is largely independant of the SPREE 1 or 10 sweep/s mode. The zones selected cycle over a period of 3 sensor rotations (90s). Zones selected are 1,4,7; 2,5,8; & 3,6,9 over 90s, and alternate 90s periods start off offset by 1 zone: 2,5,8; 3,6,9; 4,7,10; to cover all 10 zones. The low and high frequency correlators are cycled in frequency range every 90s, over their 3 possible ranges.

Thus the SOC duration is 270s or 4min 30s. In normal geophysical studies such a SOC duration would be considered too long compared with the timescales of natural phenomena. However on the Shuttle-Tether mission most of the expected effects are man-made and repeated identically several times. The main geophysical parameters are the geomagnetic co-ordinates, e.g. in relation to distance to conjugate point, and location relative to the south atlantic anomaly.

Note that during the fast sweeping 10sweeps/s the lowest ACF frequency range is avoided(*) and the 10khz range repeated .

start time	zones selected	high frequency ACF	low frequency ACF
0s	1,4,7	10Mhz	10KHz
30s	2,5,8	"	"
60s	3,6,9	"	"
90s	2,5,8	2.5MHz	5kHz
120s	3,6,9	"	"
150s	4,7,10	"	"
180s	1,4,7	625kHz	1.25kHz*
210s	2,5,8	"	"
240s	3,6,9	"	"
270s	etc		

Other Operation Cycles

It is envisaged that this cycle can be modified to create operation modes more specific to particular studies. One such mode would be to select zones to study angles parallel and perpendicular to the electron gun directions, or to the earth's magnetic field line. Another would be to concentrate studies automatically where significant modulation effects are found. These will be considered as possible future additions to the DPU software.

In these cases the above schedule of operations would be adhered to until say the fan of zones included the gun beam direction or the magnetic field. Then one or more zones would be dedicated to specific studies of that direction.

The most important operation cycle will probably remain as the general SOC described above, which should cover all phenomena in some detail.

Particle Correlator Implimentation

At the present time most of the electronics has been designed. A total of five electronics boards will contain all of the particle correlator functions. Two boards will contain the MicroComputer Units (MCU), 80C31 used to make the low frequency ACFs.Since the event counter of the 80C31 is used to count the particle arrivals the fast pulses need to be stretched to 750ns.(Not for the H.F. ACFs). One board will be dedicated to the high frequency ACFs using Altera PLA. Another board will have the D400 counters used for beam modulation and the zone selection logic. The fifth board will have a 80C86 DPU to calculate beam modulations and to collate the results from the three techniques. This data is transmitted to the SPREE DPU (and control information is received from the SPREE DPU) via dual port RAMs.

Interfaces

Most of the interfaces are directly with the main SPREE instrument:

i) 40 fast pulse streams = 2 units x 2 species x 10 angular zones These are randomly occurring 5v pulses output from the D111 amplifiers at the output of each zone. Usually these are 250ns duration.
ii) Data is transferred to and control received from the SPREE DPU by dual port RAM. This data also includes magnetic field orientation information and whether FPEG or DCOR guns are on (and which one).

Other interfaces are needed to obtain the gun firing sequences:

i) FPEG modulation pattern as a single bit toggled in phase with the gun on.
ii) DCOR modulation pattern.

Construction Timescale

Complete SPREE instrument fabrication must be complete by December 1989 for a shuttle launch in the first quarter of 1991. Therefore SPREE instrument integration must be late summer, august.

Since most of the electronics has been designed hardware construction is now begining in the US and software is being written in the UK (80C31s & 80C86). A single 80C31 MCU board will be sent to the UK early in march 1989 for low frequency correlator software testing and verification. The 80C86 DPU mother board will be sent late march 1989 similarly for DPU software testing and verification.

The particle correlator should be pre-integrated in the US in early summer june/july before the whole instrument integration.

Function testing & EGSE

The main SPREE Electrical Ground Support Equipment (EGSE) will probably be a Toshiba T3200 (80286). Software will be written to access the different correlator outputs and display accordingly. This unit will be used for instrument integration and ground monitoring during the mission.

Programmable pulse generators will be constructed to generate patterns that verify the correct operation of each of the correlation types of processing. These generators will be directly controlled by the EGSE pc.

N.B. Please note that this document was originally produced on a word processor. In order to transfer to mainframe for EMAIL an ASCII dump (spool) was done. Unfortunately this has lost much of underlines etc. Especially superscript o for degrees has dropped e.g. 90o = 90 degrees!

HIGH VOLTAGE POWER SUPPLY

Work is continuing on the optical drivers in the power supply. LEDs from Opto Diode Inc. have been received. High voltage glass encapsulated diodes from Microsemi Inc. are due by August. Prototype ceramic packages have been ordered from Cercoa Inc.. Optocouplers for breadboarding will be available in August Testing of flight units has been scheduled for September. Other phases of design, including DC-DC converters and feedback elements will begin in August.

MOTOR DRIVE

The printed circuit board for the motor controller has been designed and is being tested. The layout for the PCB and it's mounting bracket are shown. Each motor will require 15V @ 200mA. The motor is expected to dissipate half the power while the other half will be coupled to the controller's heat sink. Harmonic reduction drives have been received. Stepping motors will arrive in July.

INTERFACE

The hardware interface definition between SPREE and the MMAG wiring harness is complete. The included diagram shows seven (7) connectors for power and data I/O.

The Software Requirements Document (SRD) is complete. The document specifies all measurements and commands SPREE will communicate. The document also defines the display format for the DDCU on the aft flight deck, and the displays in the POCC at JSC. SPREE has defined 1602 measurements, 321 of which will be displayed at the POCC and 74 at the DDCU. SPREE has also defined 180 commands. The following diagrams show SPREE's orientation in the shuttle bay, a summary of the data measurements, and sample displays for the DDCU and POCC.

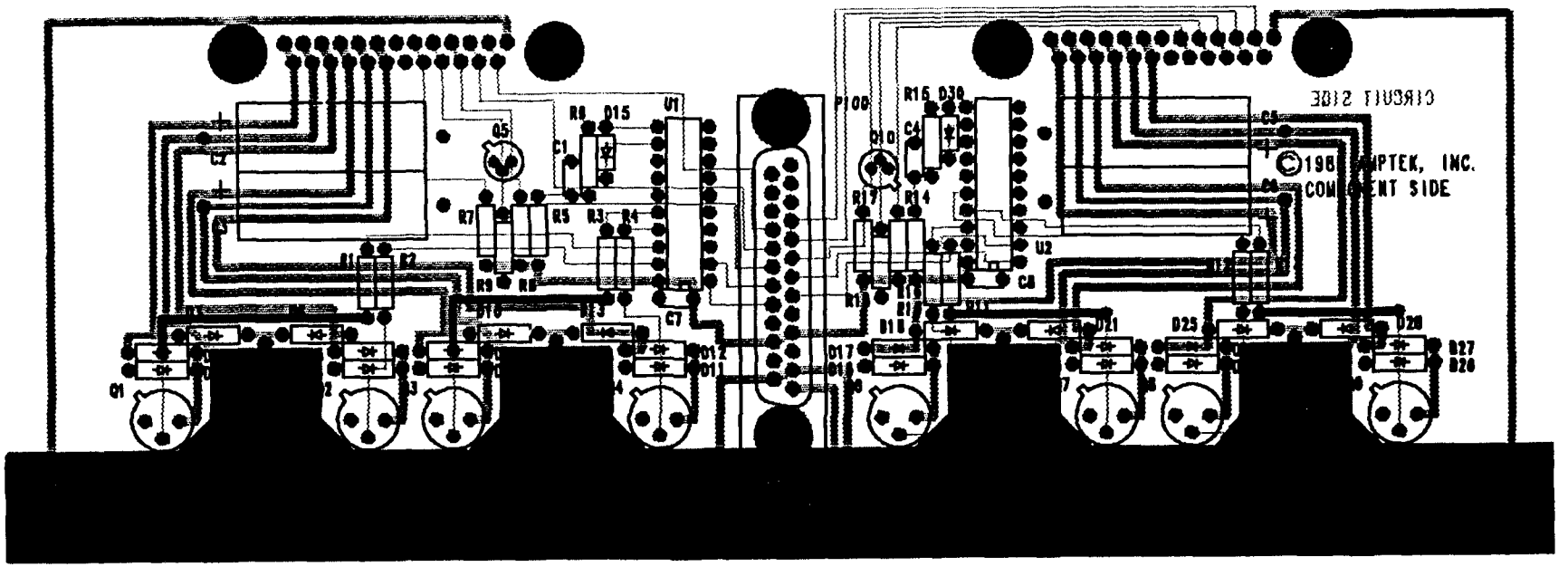
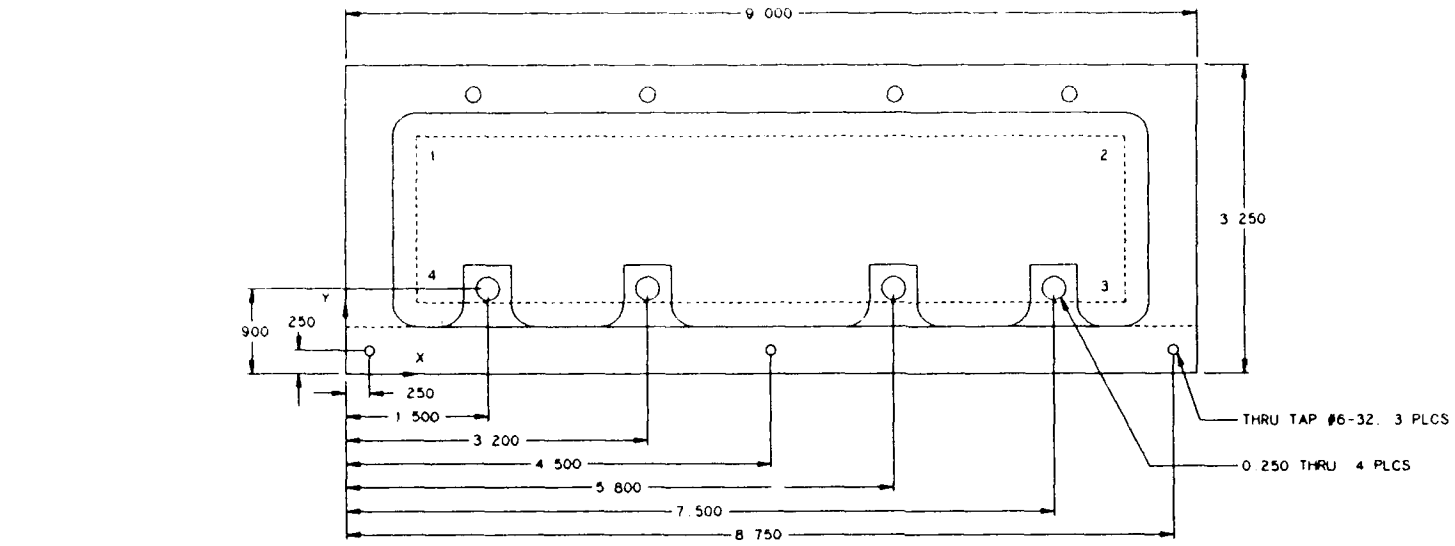


FIGURE QR7-7

MOTOR DRIVE PRINTED CIRCUIT BOARD



N C LOCATIONS

	X	Y	
1	0 750	2 500	0 313 DEPTH
2	8 250	2.500	
3	8 250	0.750	
4	0 750	0 750	
5	0 000	0 750	0 188 DEPTH
6	1 000	0.750	
7	1 000	1 400	
8	2 000	1 400	
9	2 000	0.750	
10	2 700	0.750	
11	2 700	1 400	
12	3 700	1.400	
13	3 700	0 750	
14	5 300	0 750	
15	5 300	1.400	
16	6 300	1.400	
17	6 300	0 750	
18	7 000	0 750	
19	7 000	1.400	
20	8 000	1 400	
21	8 000	0.750	
22	9 000	0.750	

ADDITIONAL CUTS REQUIRED TO EXPOSE RIM

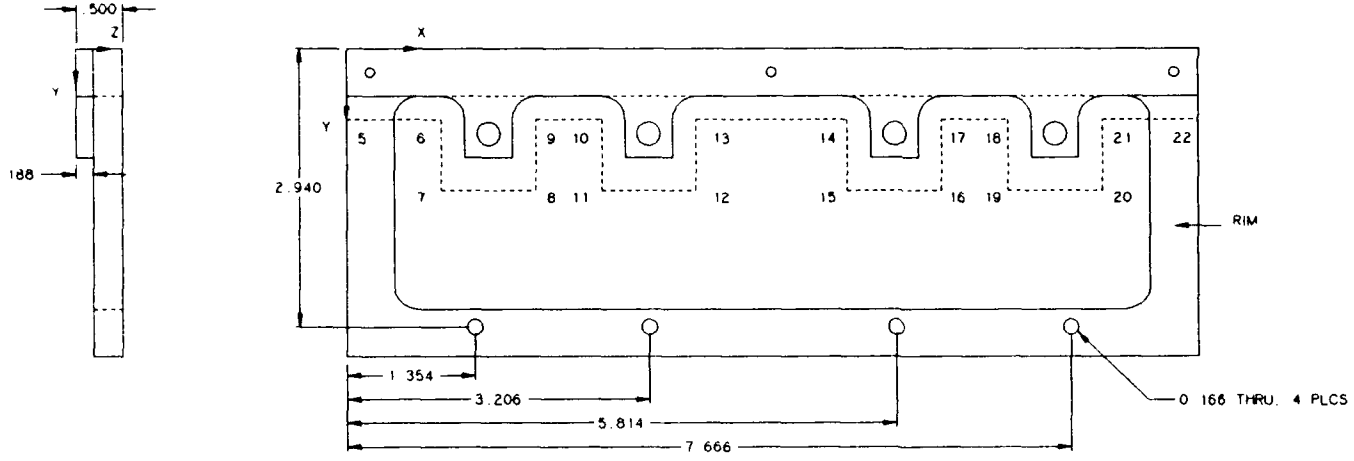


FIGURE QR7-8

DO NOT SCALE PRINT	DRAWN W EVEREST	DATE 6-5-89	AMP TEK
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES WITH TOLERANCES ON: FRACTIONS ±1/32 DECIMALS XX ± 02 XXX ± 005 ANGLES 0° 15'	CHECKED		TITLE: MOTOR CONTOLLER MOUNT
	DESIGN W EVEREST	6-5-89	
	PROJECT MANAGER		
	QUALITY ASSURANCE		
MATERIAL Al 6061-T6	PROJECT PRDA		SIZE C MCM
FINISH REQUIRED 64 micro inches	CONTRACT NUMBER		SCALE 1 1 WEIGHT LBS SHEET 1 OF 1

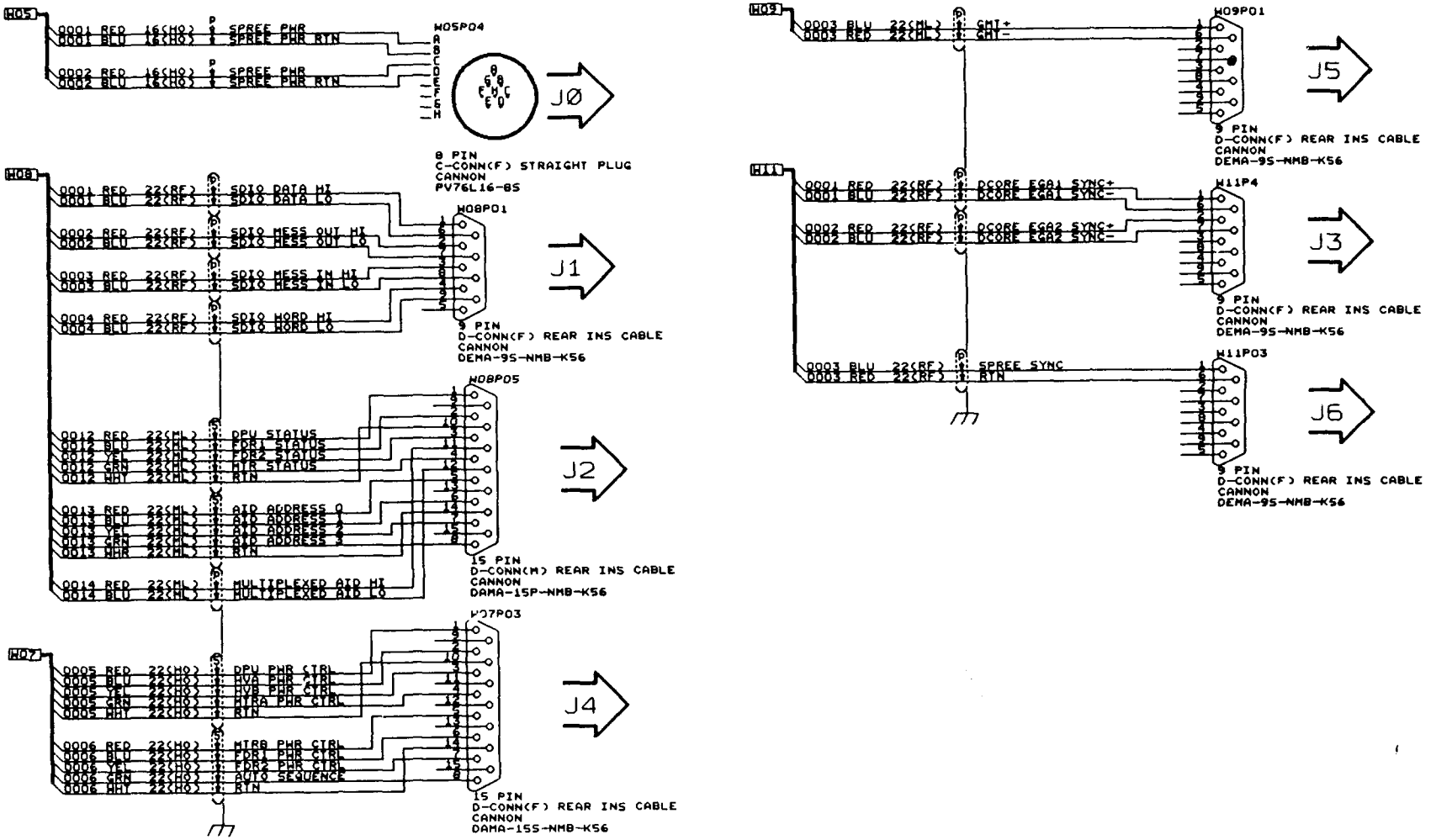


FIGURE QR7-9

AMPTEK, INC.		
Title: MMC HARNESS		
Size: B	Document Number:	REV
Date: May 23, 1989	Sheet 18 of 43	

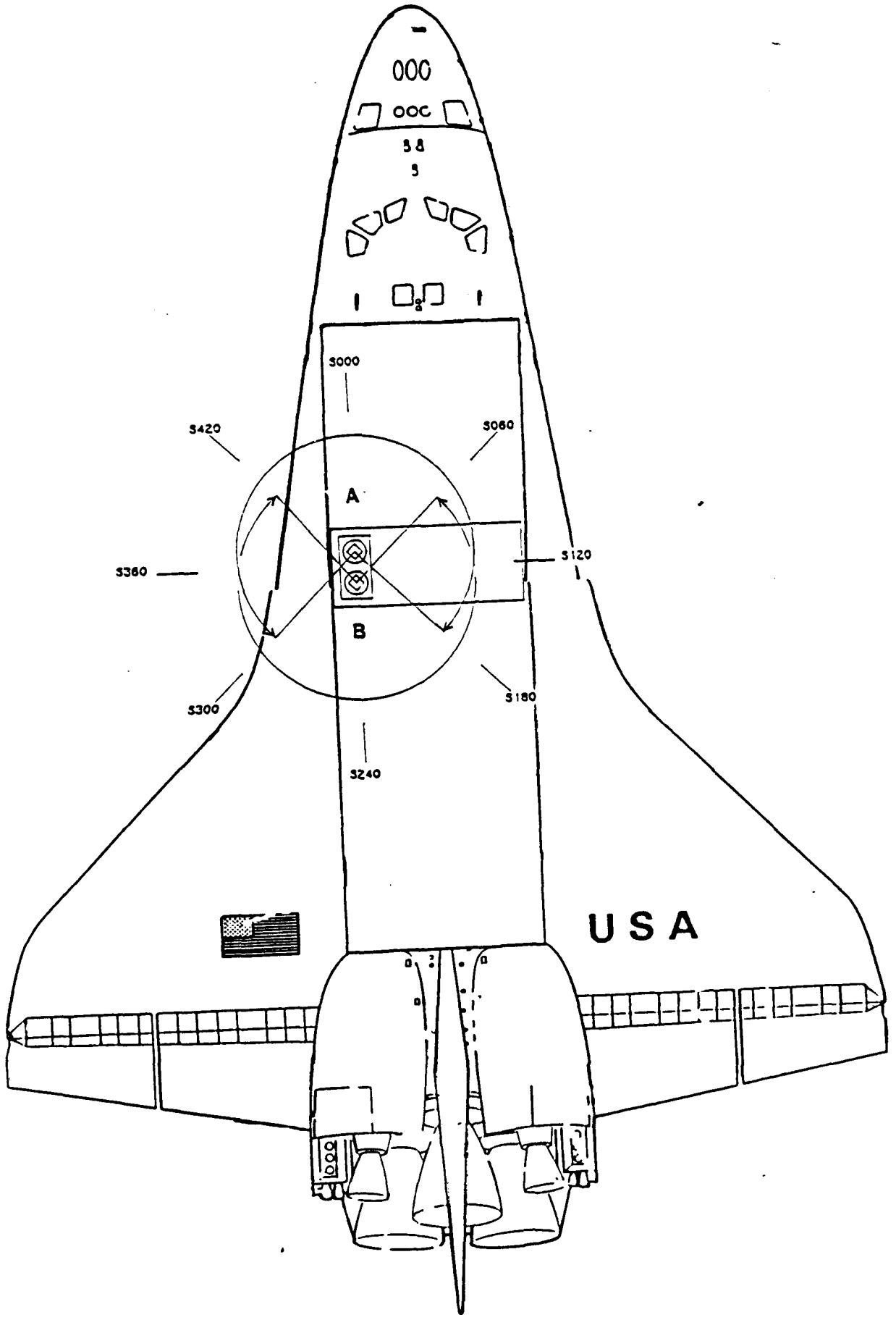


FIGURE QR7-10

SPREE SHUTTLE BAY LOCATION WITE SECTOR DEFINITION

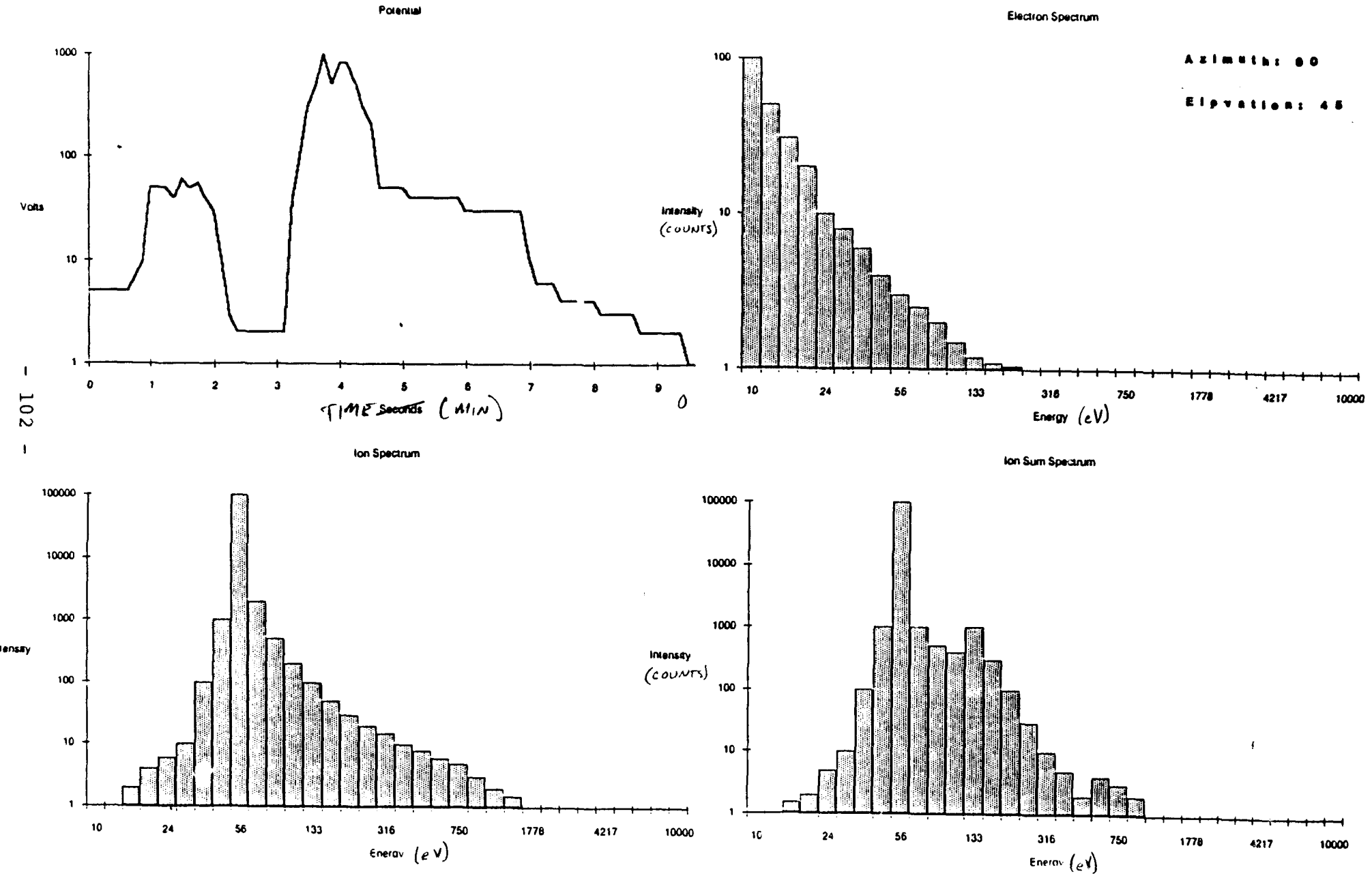


FIGURE QR7-11 **POSSIBLE AFT FLIGHT DECK DISPLAY**

PRDA-QR8

PROTOTYPE INSTRUMENTATION AND DESIGN STUDIES

AMPTEK, INC.
6 De Angelo Drive
Bedford, MA 01730

September 15, 1989

R&D Status Report no. 8
June 5, 1989 through September 4, 1989

Contract #F19628-87-C-0094

Distribution: AFGL/PHE
DCASMA/ACO
ESD/PKR

Prepared for:

GEOPHYSICS LABORATORY
Air Force Systems Command
United States Air Force
Hanscom Air Force Base, Massachusetts 01731-5000

SPREE Integrated Package

Attached is a schedule showing the progress of the instrument through the presently scheduled delivery date in May 1990. Work is progressing as planned, with the flight hardware completed by January 1990, leaving the next 5 months for testing and software assessment.

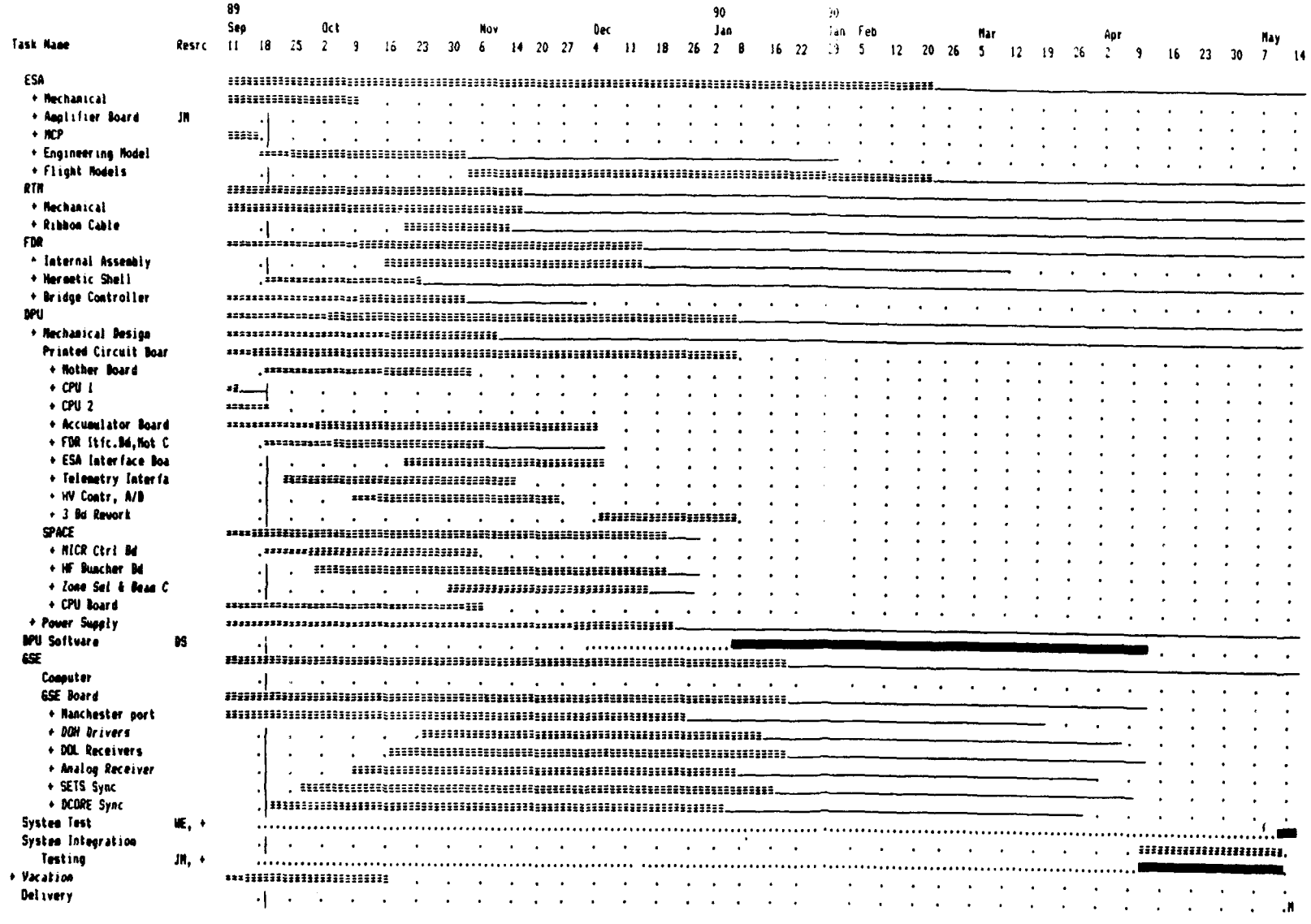
Preliminary drawings of the SPREE Mounting Bracket (SMB) were received from Martin-Marietta this quarter. More detail will be needed to allow constructing a mechanical mock-up that will allow Amptek to build the intra-SPREE cable harness.

The SPREE project documentation is being maintained using an hierarchical drawing system showing the various level assemblies, their inter-connects and some specific details. The current configuration schematics are provided as part of this quarterly report. The drawings are presented on adjacent pages as various SPREE sub-systems are discussed.

Schedule Name : Spree Master Schedule
Responsible : John McGarity
As-of Date : 19-Sep-89 Schedule File : D:\TL3\DATA\SPREE

Amptek Internal Schedule

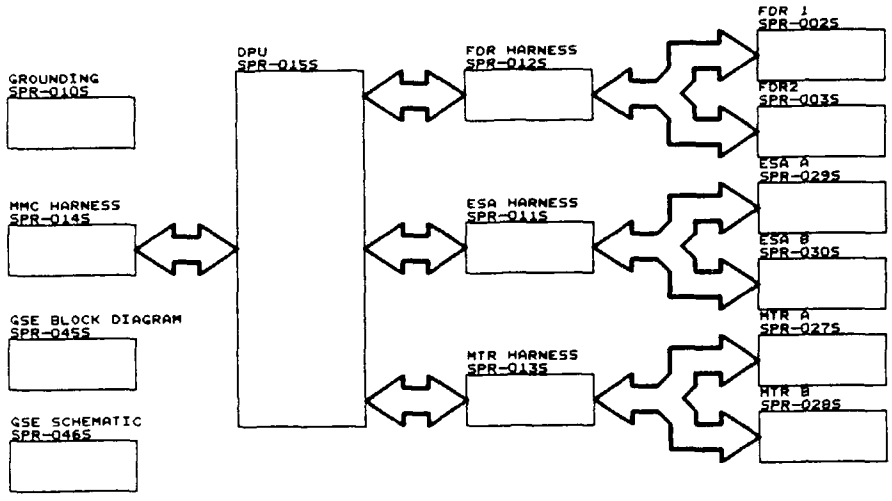
Dependencies : *Fabrication*



Detail Task ##### Summary Task M Milestone
(Started) ==### (Started) ››› Conflict
(Slack) ###__ (Slack) .. Resource delay

Scale: 1 day per character

SHUTTLE POTENTIAL & RETURN ELECTRON EXPERIMENT BLOCK DIAGRAM



DOCUMENT	NAME
SPR-001S	SPREE
SPR-002S	FDR 1
SPR-003S	FDR 2
SPR-004S	CPU
SPR-005S	SERIAL
SPR-006S	DRIVER
SPR-007S	SCSI
SPR-008S	ANALOG
SPR-009S	D-PU/FDR INTERFACE TIMING
SPR-010S	GROUNDING
SPR-011S	ESA HARNESS
SPR-012S	FDR HARNESS
SPR-013S	MTR HARNESS
SPR-014S	MMC HARNESS
SPR-015S	DPU
SPR-016S	PWR HARNESS
SPR-017S	SDIO INTERFACE
SPR-018S	DIL INTERFACE
SPR-019S	DCORE/SETS INTERFACE
SPR-020S	DOH INTERFACE
SPR-021S	AID INTERFACE
SPR-022S	FDR INTERFACE
SPR-023S	INVERTERS
SPR-024S	MOTOR DRIVER
SPR-025S	MOTOR CONTOL A
SPR-026S	MOTOR CONTROL B
SPR-027S	MTR A
SPR-028S	MTR B
SPR-029S	ESA A
SPR-030S	ESA B
SPR-031S	HV SUPPLY
SPR-032S	ION PREAMPLIFIER
SPR-033S	ELECTRON PREAMPLIIFER
SPR-034S	SENSOR INTERFACE
SPR-035S	BEAM COUNT/ZONE SELECT
SPR-036S	HIGH FREQUENCY BUNCHER
SPR-037S	MCU2
SPR-038S	MCU1
SPR-039S	SPACE CPU
SPR-040S	ACCUMULATOR
SPR-041S	SECONDARY CPU
SPR-042S	PRIMARY CPU
SPR-043S	MTR INTERFACE
SPR-044S	A/D, HV CONTROL
SPR-045S	GSE BLOCK DIAGRAM
SPR-046S	GSE SCHEMATIC
SPR-047S	PSPICE SIMULATION OF SDIO DATA

FIGURE QR8-1

PRELIMINARY

AMPTEK, INC.
6 DE ANGELO DRIVE
BEDFORD, MA 01730
617/275-2242

Title
SHUTTLE POTENTIAL & RETURN ELECTRON EXP.

Size	Document Number	REV
E	SPR-001S	A

Date: September 7, 1989 Sheet 1 of 42

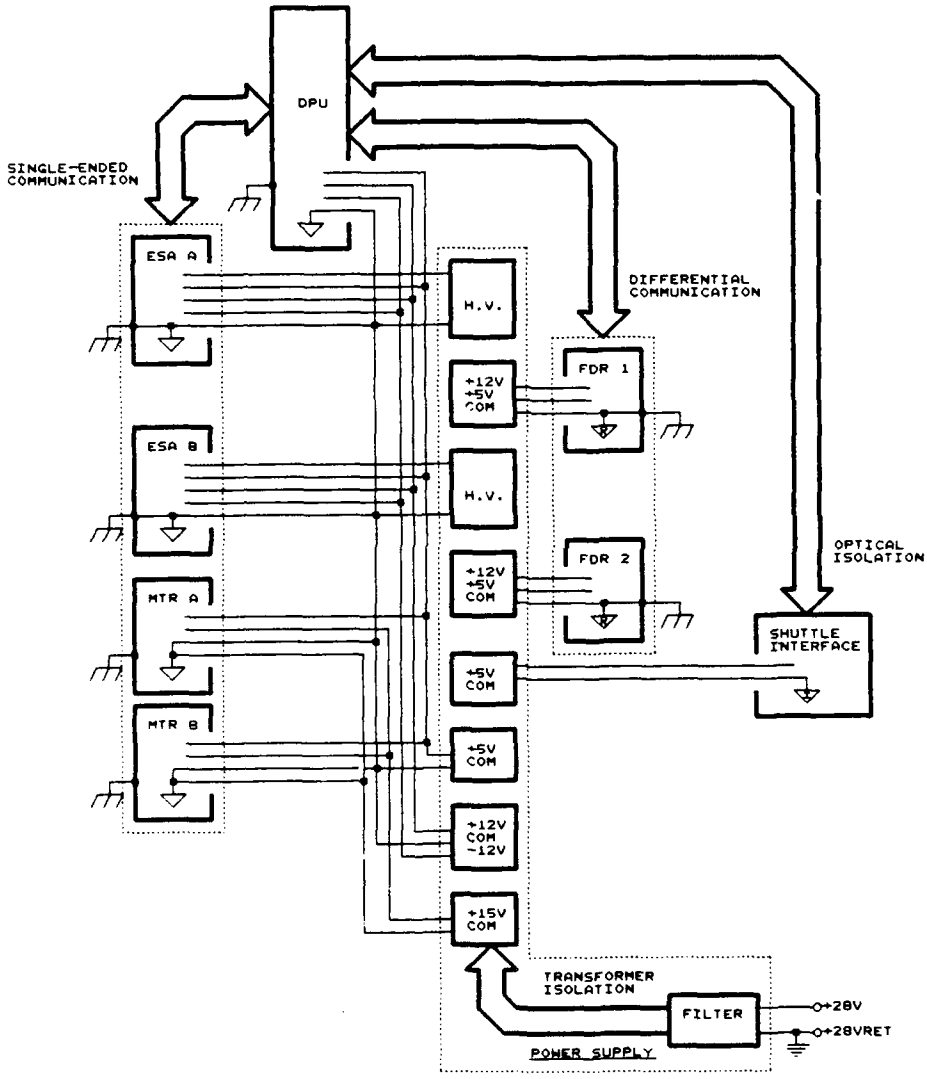


FIG. RI QR8-2

AMPTEK, INC.		
Title: GROUNDING		
Size: E	Document Number: SPR-0105	REV: A
Date: September 5, 1989	Sheet 10 of 42	

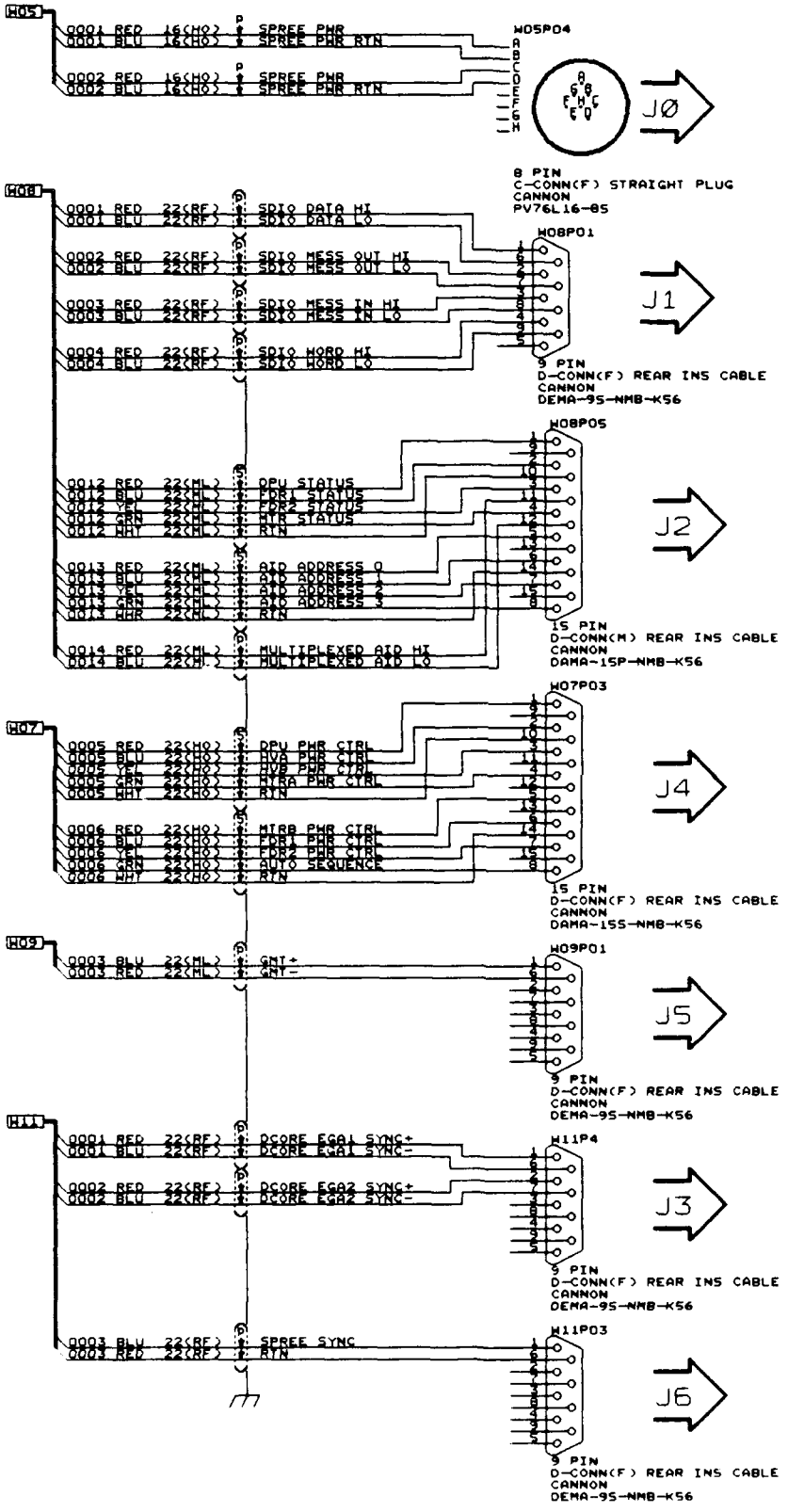


FIGURE QR8-3

AMPTEK, INC.		
Title: MMC HARNESS		
Size: E	Document Number: SPR-0145	REV: A
Date: September 5, 1989	Sheet 11 of 42	

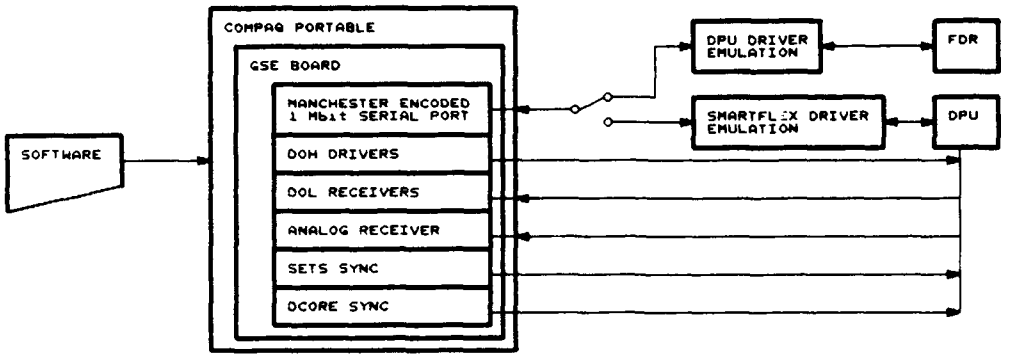


FIGURE QR8-1

AMPTEK, INC.		
Title: GSE BLOCK DIAGRAM		
Size: E	Document Number: SPR-0455	REV: A
Date: September 7, 1989	Sheet: of	

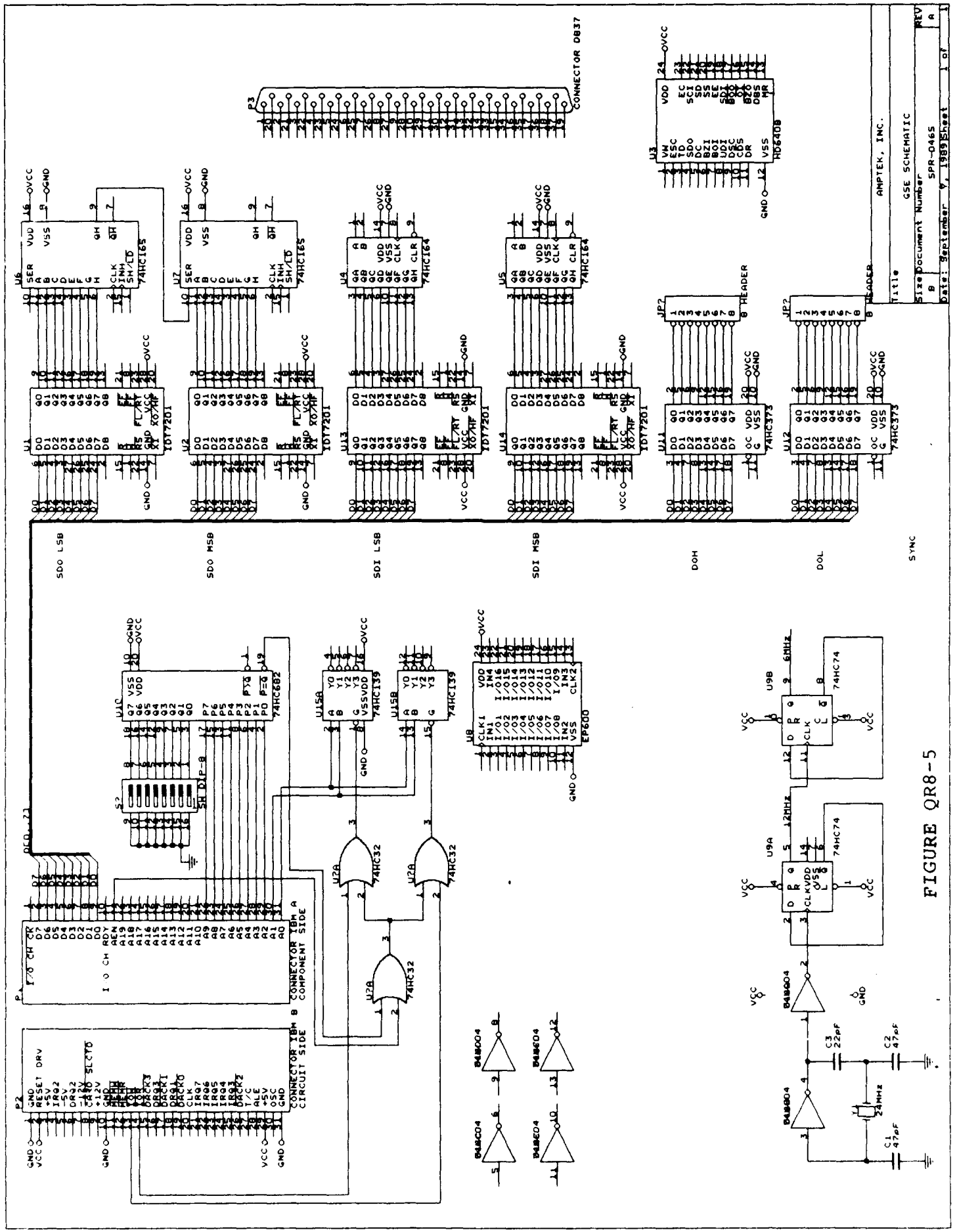
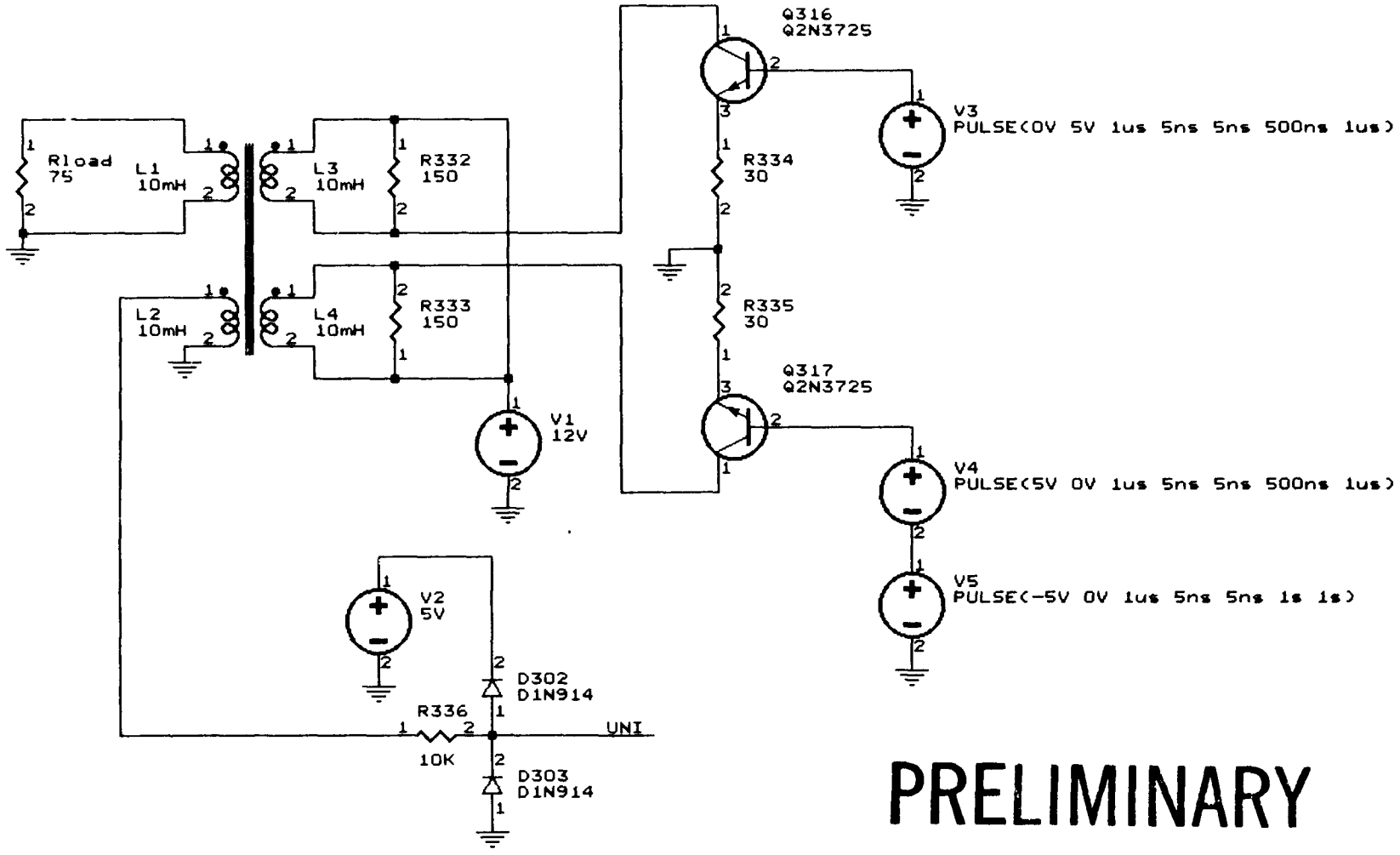

SDO LSB
SDO MSB
SDI LSB
SDI MSB
DOH
DOL
SYNC
CONNECTOR D837
AMPTEK, INC.
GSE SCHEMATIC
SPR-0465
74HC165
74HC164
IDT7201
74HC373
74HC139
74HC32
74HC74
74HC04
HD6408
EP600
74HC682
CONNECTOR IBM A
COMPONENT SIDE
CONNECTOR IBM B
CIRCUIT SIDE
12MHz
6MHz
24MHz
47pF
22pF

FIGURE QR8-5

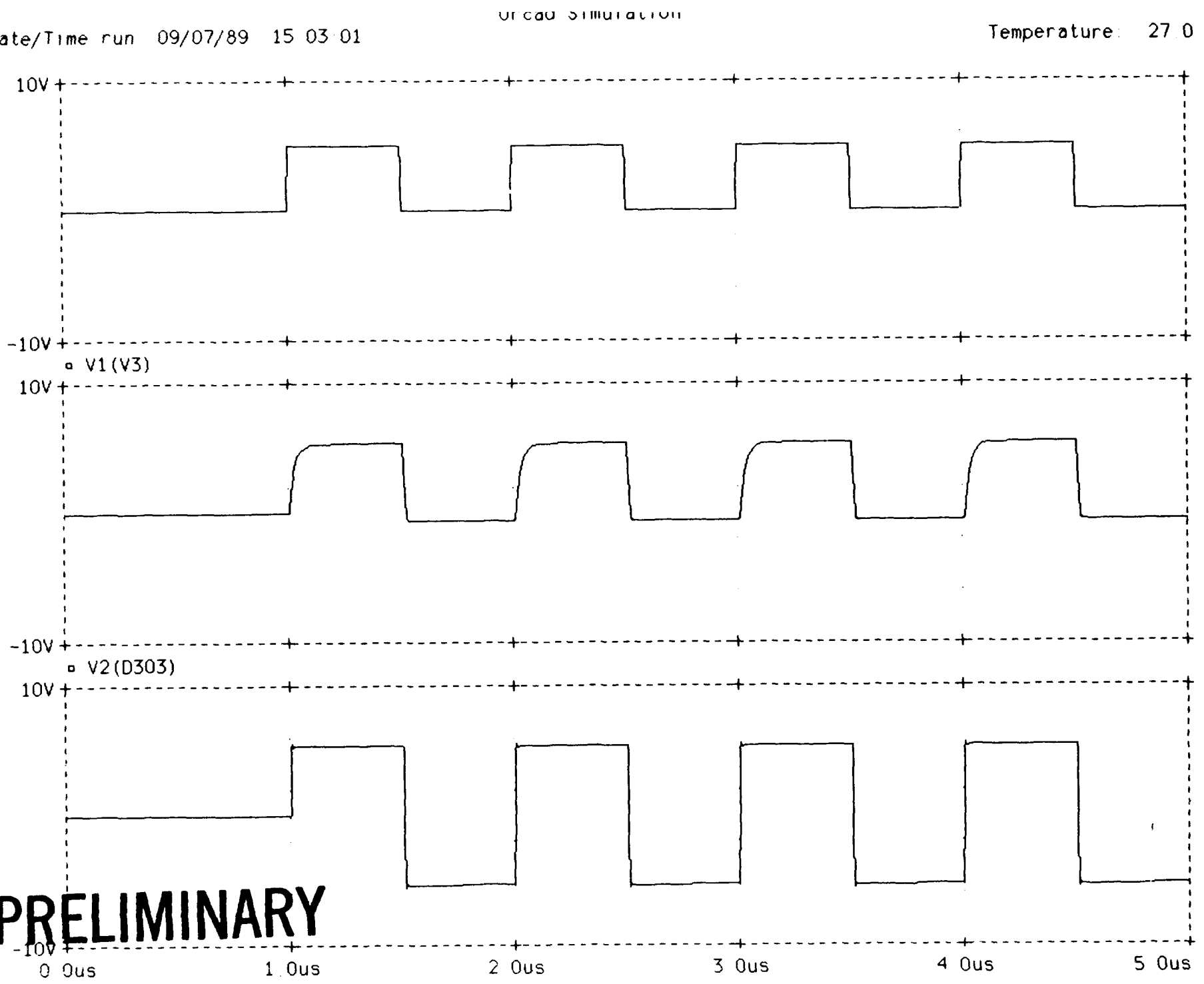


PRELIMINARY

```
;.PROBE
;.OPTIONS ITL5=0
;.MODEL Q2N3725 NPN(Is=1.608p Xti=3 Eg=1.11 Vaf=100 Bf=169 Ne=1.29 Ise=1.608p
;+ Ikf=.9625 Xtb=1.5 Br=19.18m Nc=2 Isc=0 Ikr=0 Rc=.6 Cjc=9.293p
;+ Mjc=.256 Vjc=.75 Fc=.5 Cje=52.8p Mje=.4351 Vje=.75 Tr=3.85u
;+ Tf=300.5p Itf=.45 Vtf=6 Xtf=1.5 Rb=10
;.MODEL D1N914 D(Is=0.1p Rs=16 CJO=2p Tt=12n Bv=100 Ibv=0.1p)
;.TRAN 5us 5us
;K1 L1 L2 L3 L4 .99999
```

FIGURE QR8-6

AMPTEK, INC.		
Title: PSPICE SIMULTATION OF SDIO DATA		
Size: A	Document Number: SPR-0475	REV: A
Date: September 7, 1989	Sheet 1 of 1	



PRELIMINARY

FIGURE QR8-7

NESTED HEMISPHERE ESA DESIGN

All of the flight parts for the SPREE ESA's have been machined. The parts have been checked by partial assembly and one set has been nickel plated for use on the engineering sensor. Plating of the two flight units is being delayed to allow testing of the engineering model to assure the design.

A preliminary set of microchannel plates was received from Galileo Electro-Optics. These plates had a lower strip current than specified and were provided by the manufacturer at no cost so that Amptek could begin the engineering unit evaluation. It has been discovered during testing that these plates were cut such that the bias angle (11 degrees) was aligned so that the plates cannot be mounted in a chevron assembly. This prevents the plates from being used electrically since they would suffer massive ion feedback if operated with full bias potential.

The plates will be used as mechanical samples to evaluate the MCP mounting design. They will be used for vibration testing of the mounting hardware and the sphere sub assembly.

An amplifier board has been assembled and tested to use with the engineering unit. The A111F charge sensitive pre-amplifiers for the engineering and flight sensors were ordered and received. The engineering amplifier board has been assembled using Augat sockets for the A111F pre-amps to avoid soldering. 50 A111F's were purchased, 40 of which will be used for the two flight sensors. The remaining 10 will act as flight spares and be used in the engineering model.

The amplifier board has been tested and works properly.
The engineering unit is assembled and awaiting microchannel plates to begin testing. The engineering sensor unit will not have high voltage supplies to provide deflection potentials and MCP biasing. These are provided externally via 4 high voltage cables. This arrangement allows full control and adjustment during the preliminary testing phase.

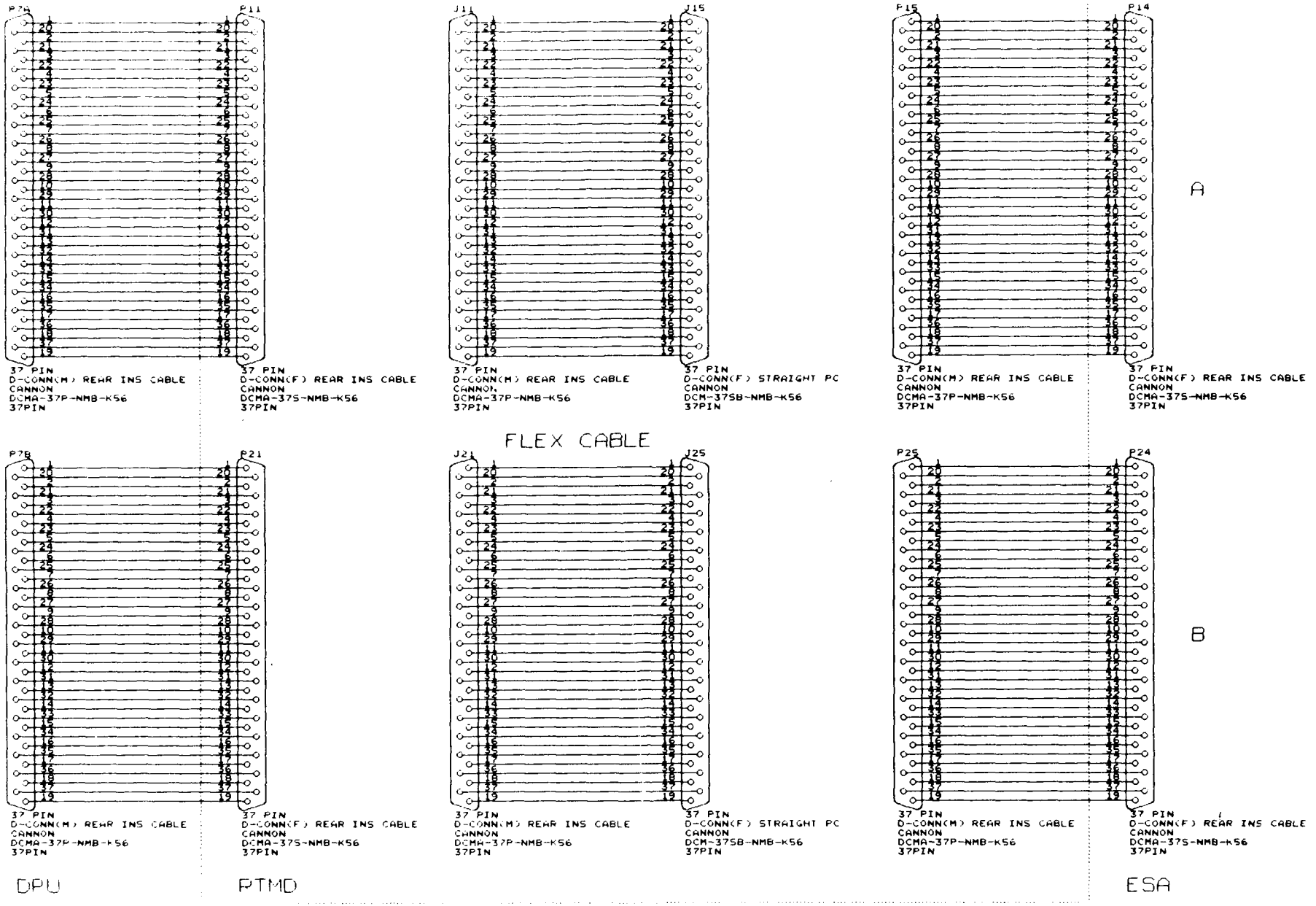


FIGURE QR8-8

AMPTEK, INC.		
Title: ESA HARNESS		
Size: B	Document Number: SPR-011S	REV: A
Date: August 31, 1989	Sheet 24 of 42	

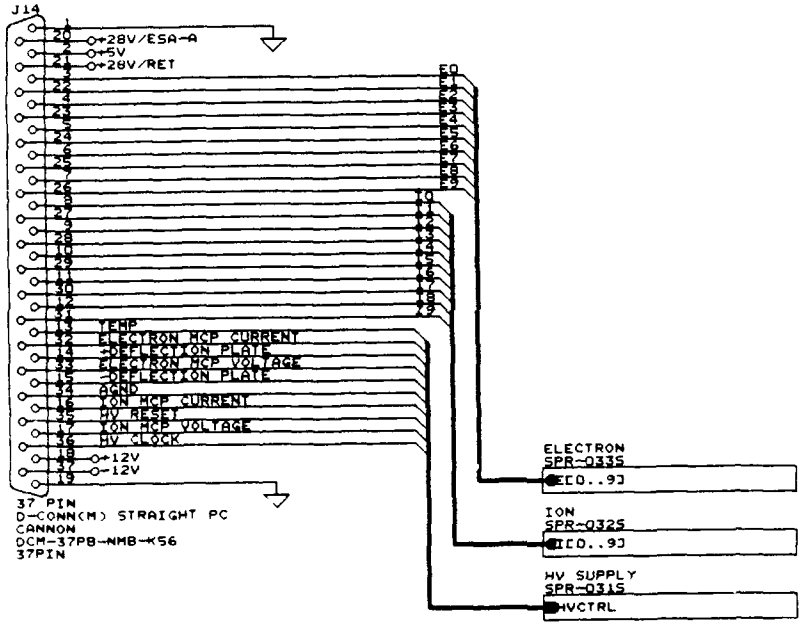


FIGURE QR8-9

	AMPTEK, INC.	
Title	ESA A	
Size E	Document Number SPR-029S	REV A
Date: September 5, 1989	Sheet 33 of 42	

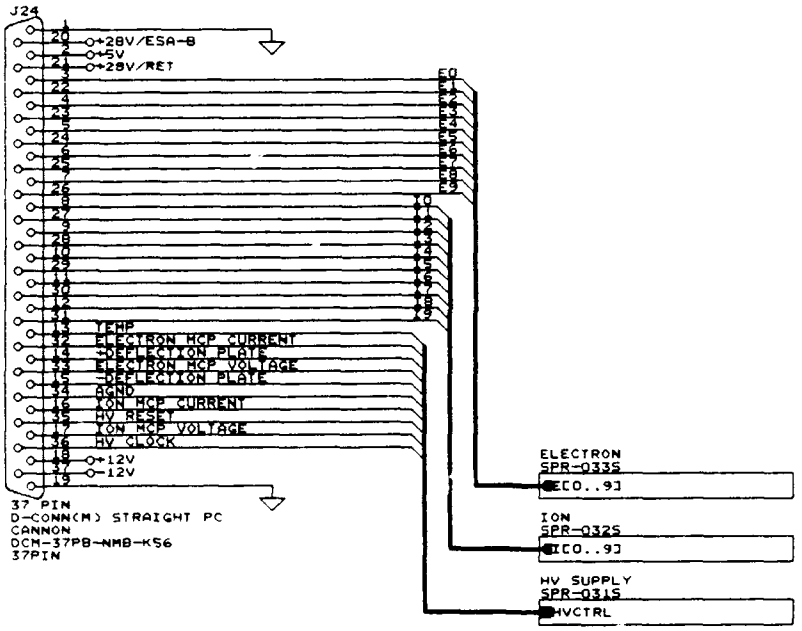


FIGURE QR8-10

AMPTEK, INC.		
Title: ESA B		
Size: E	Document Number: SPR-030S	REV: A
Date: September 5, 1989	Sheet 33 of 42	

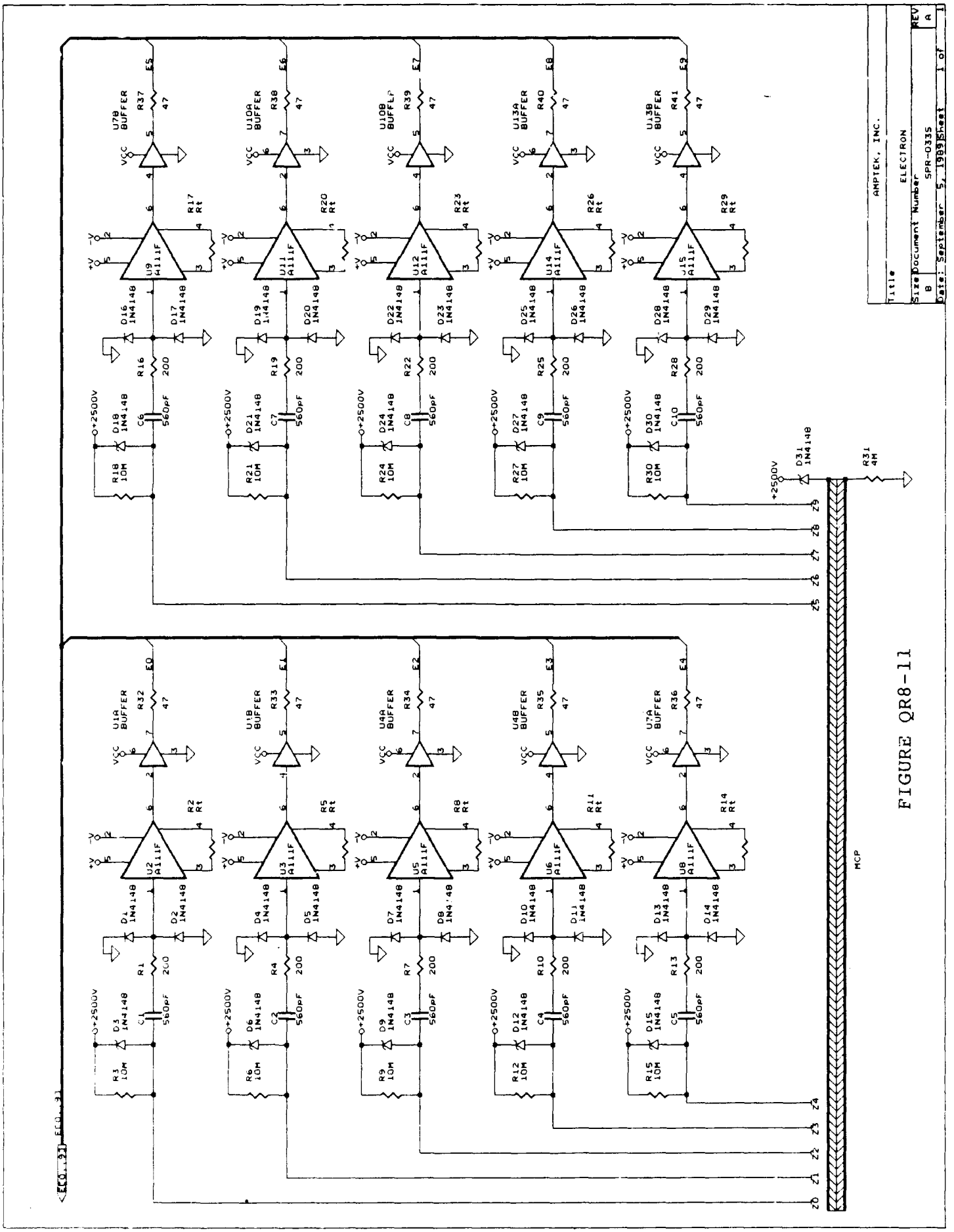


FIGURE QR8-11

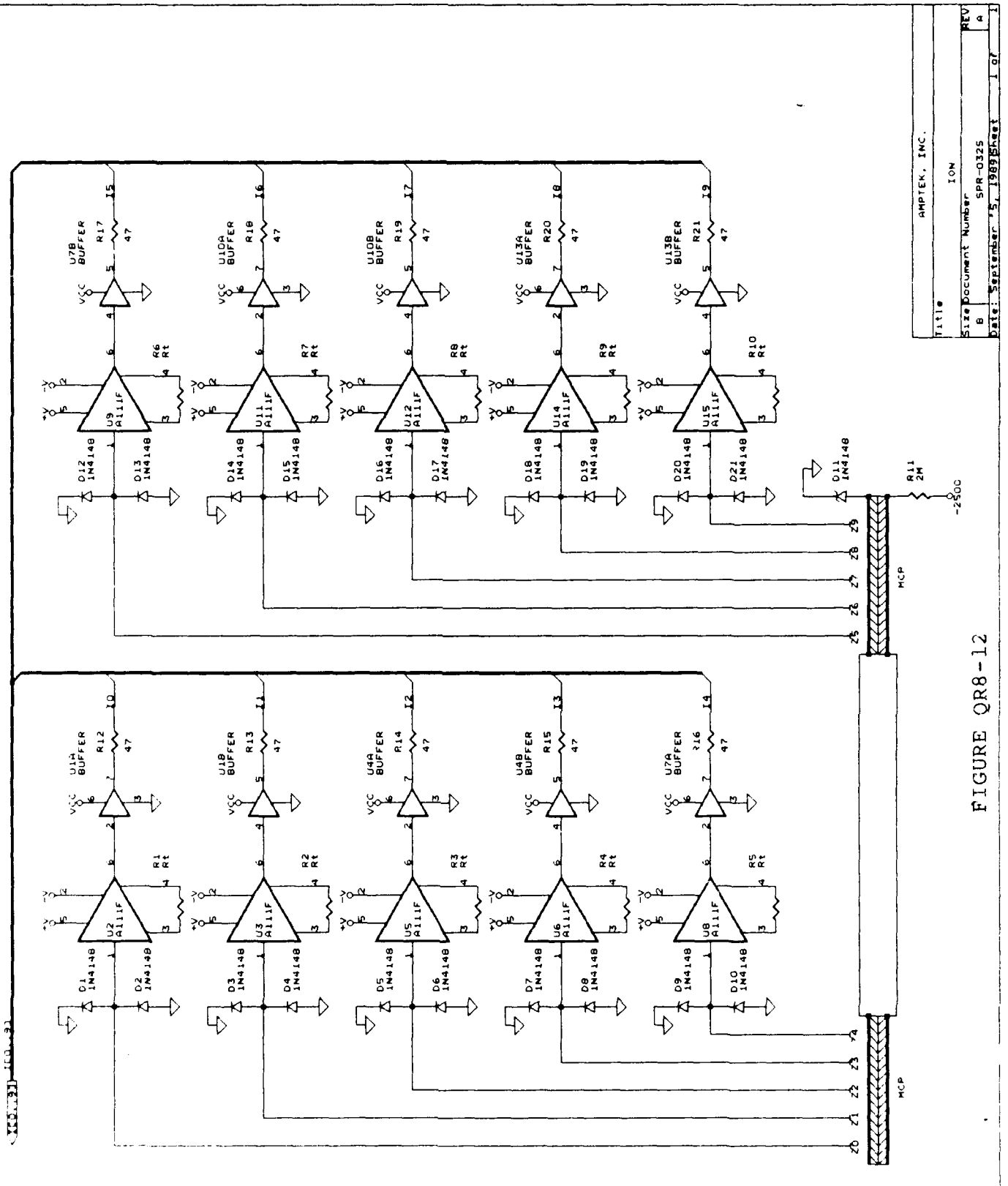


FIGURE QR8-12

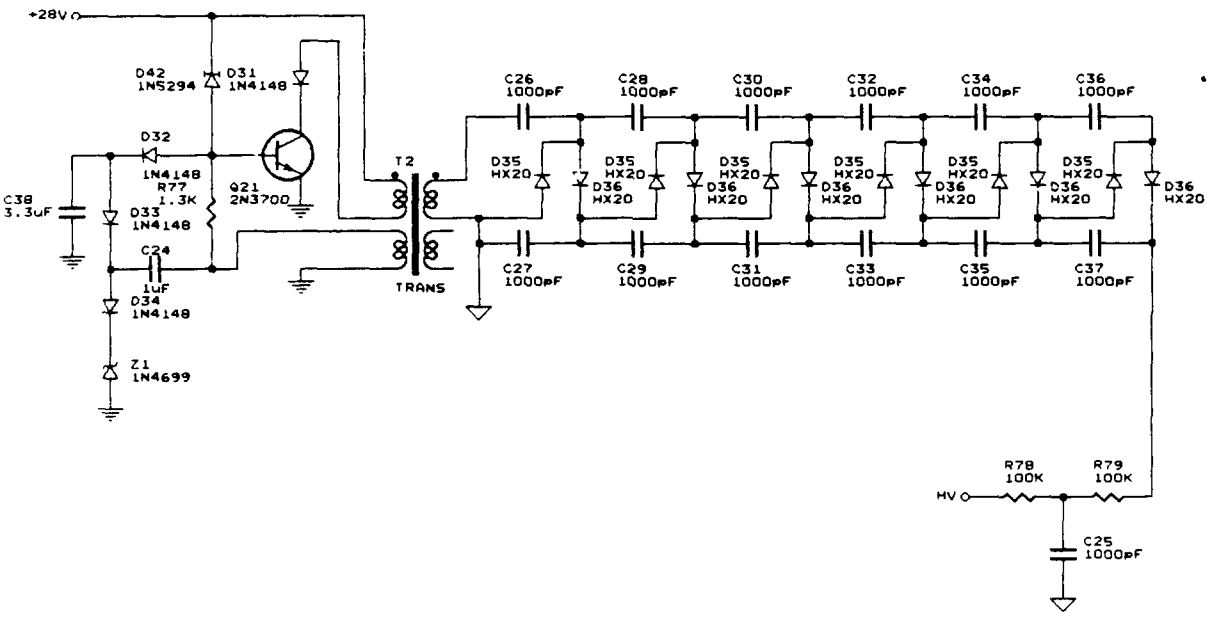


FIGURE QR8-13

AMPTEK, INC.		
Title: HV SUPPLY		
Size: E	Document Number: SPR-0315	REV: A
Date: August 31, 1989	Sheet 40 of 42	

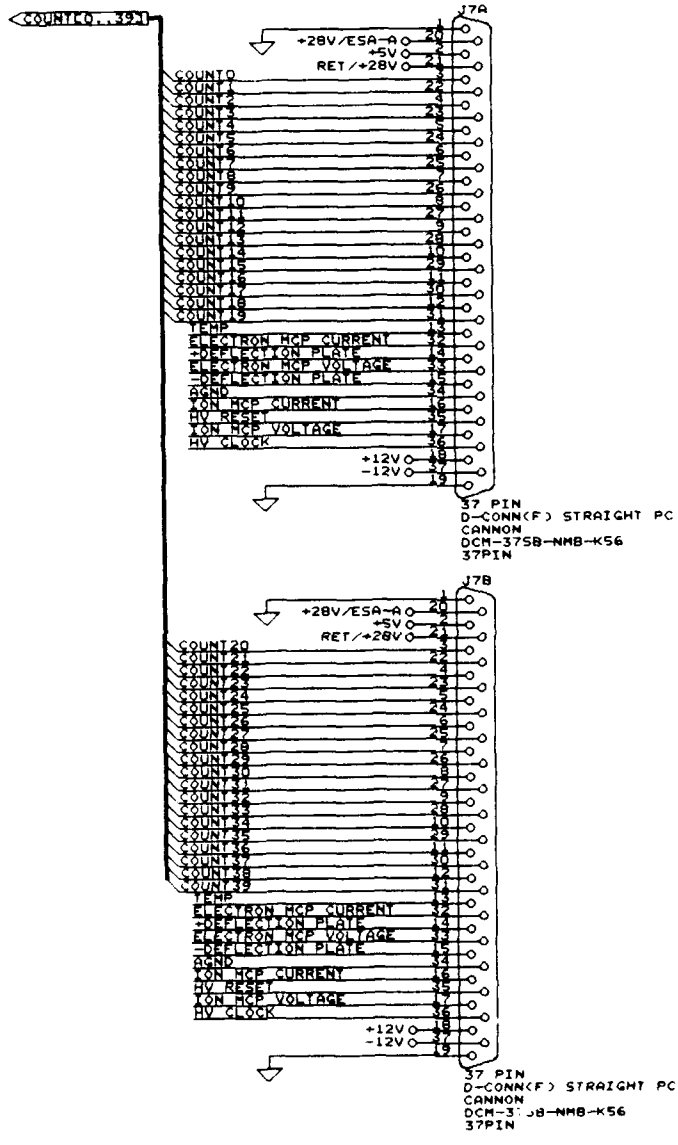


FIGURE QR8-14

AMPTEK, INC.		
Title: SENSOR INTERFACE		
Size: E	Document Number: SPR-0345	REV: A
Date: September 6, 1989	Sheet: of	

DATA PROCESSING UNIT FOR 270 DEGREE NESTED SENSORS

Several PC boards were fabricated this quarter. The accumulator board has been built and will be tested when the backplane is available. Likewise, the recorder/motor controller was completed after the interface circuits were breadboarded and tested.

The design and layout of the backplane has been completed and it is in the process of being fabricated. Its availability will allow the testing of the boards mentioned above, plus the testing of the inter-cpu communications port.

The SPACE control CPU and the MCU prototype are still being evaluated by Paul Gough. These designs should be finalized very soon, with boards following shortly thereafter.

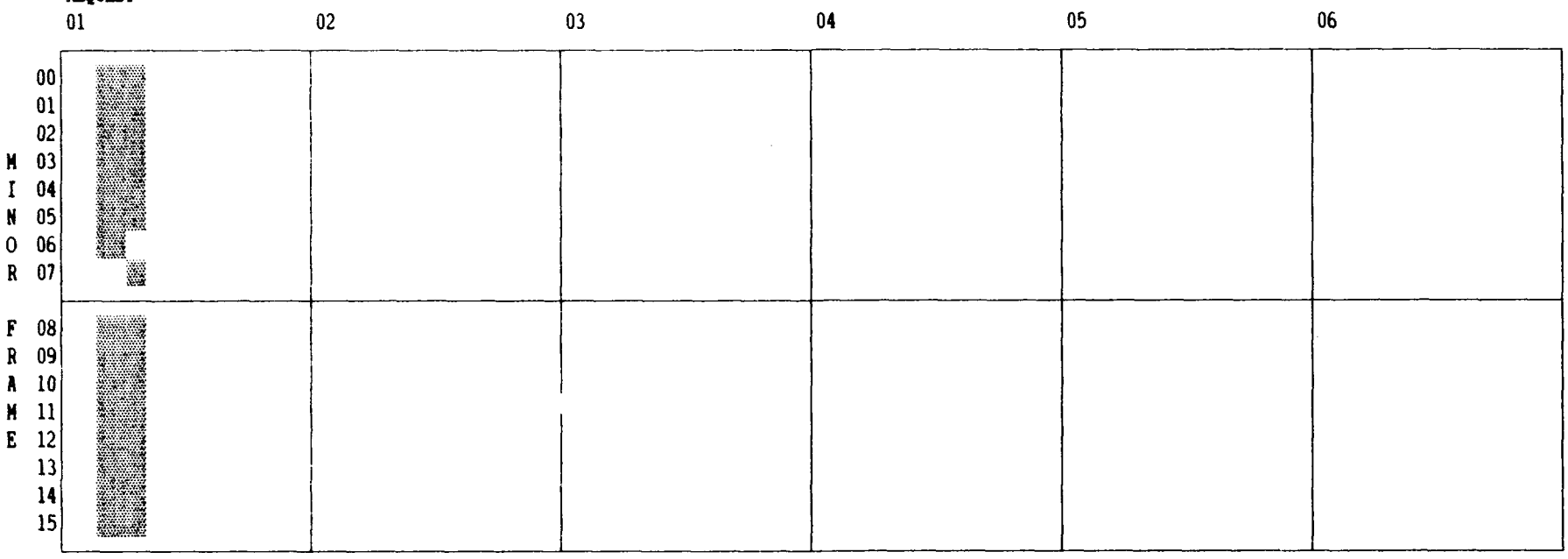
The current schedule calls for all DPU boards to be completed during this upcoming quarter, with the beginning of software development coinciding with final hardware testing.

TELEMETRY

The telemetry format between SPREE and the SFMDM has been changed. SPREE will now operate at a high data rate (9.216 kbit) at all times. Data will be organized into 16 minor frames every two seconds. Requests for data will be periodic in 24 byte packets. The leading bytes in each request will contain DDCU display data. Information from both analyzers will be displayed at the DDCU.

The Software Requirements Document (SRD) that defines the interface has been completed by Amptek and delivered to AFGL. The Air Force is to add general information to the document and forward to MMAG. A copy of the SRD as delivered to the Air Force is attached to this report.

MINOR FRAME REQUEST STRUCTURE



▒ DDCU DATA = 75 BYTES (TOTAL)

FIRST REQUEST PER MINOR FRAME

	BYTE 01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
	00	A55Ah		00h	A31	A30	A29	A28	A27	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
	01	A55Ah		01h	A26	A25	A24	A23	A22	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
	02	A55Ah		02h	A21	A20	A19	A18	A17	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
M	03	A55Ah		03h	A16	A15	A14	A13	A12	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
I	04	A55Ah		04h	A11	A10	A09	A08	A07	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
N	05	A55Ah		05h	A06	A05	A04	A03	A02	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
O	06	A55Ah		06h	A01	A00	MODE	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
R	07	A55Ah		07h	DATA	DATA	DATA	AZIMUTHA		DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
F	08	A55Ah		08h	B31	B30	B29	B28	B27	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
R	09	A55Ah		09h	B26	B25	B24	B23	B22	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
A	10	A55Ah		0Ah	B21	B20	B19	B18	B17	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
M	11	A55Ah		0Bh	B16	B15	B14	B13	B12	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
E	12	A55Ah		0Ch	B11	B10	B09	B08	B07	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
	13	A55Ah		00h	B06	B05	B04	B03	B02	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
	14	A55Ah		0Eh	B01	B00	POTL	ELEV	CONF	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
	15	A55Ah		0Fh	UCNT	CCNT	LCNT	AZIMUTHB		DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA

SECOND REQUEST PER MINOR FRAME

	BYTE 25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
	00	A55Ah		00h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
	01	A55Ah		01h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
	02	A55Ah		02h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
M	03	A55Ah		03h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
I	04	A55Ah		04h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
N	05	A55Ah		05h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
O	06	A55Ah		06h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
R	07	A55Ah		07h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
F	08	A55Ah		08h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
R	09	A55Ah		09h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
A	10	A55Ah		0Ah	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
M	11	A55Ah		0Bh	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
E	12	A55Ah		0Ch	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
	13	A55Ah		00h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
	14	A55Ah		0Eh	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
	15	A55Ah		0Fh	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA

THIRD REQUEST PER MINOR FRAME

		BYTE 49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72
	00	A55Ah		00h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
	01	A55Ah		01h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
	02	A55Ah		02h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
M	03	A55Ah		03h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
I	04	A55Ah		04h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
N	05	A55Ah		05h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
O	06	A55Ah		06h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
R	07	A55Ah		07h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
F	08	A55Ah		08h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
R	09	A55Ah		09h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
A	10	A55Ah		0Ah	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
M	11	A55Ah		0Bh	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
E	12	A55Ah		0Ch	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
	13	A55Ah		0Dh	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
	14	A55Ah		0Eh	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
	15	A55Ah		0Fh	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA

FOURTH REQUEST PER MINOR FRAME

		BYTE 73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96
	00	A55Ah		00h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
	01	A55Ah		01h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
	02	A55Ah		02h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
M	03	A55Ah		03h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
I	04	A55Ah		04h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
N	05	A55Ah		05h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
O	06	A55Ah		06h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
R	07	A55Ah		07h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
F	08	A55Ah		08h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
R	09	A55Ah		09h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
A	10	A55Ah		0Ah	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
M	11	A55Ah		0Bh	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
E	12	A55Ah		0Ch	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
	13	A55Ah		0Dh	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
	14	A55Ah		0Eh	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
	15	A55Ah		0Fh	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA

FIFTH REQUEST PER MINOR FRAME

		BYTE 97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120
	00	A55Ah		00h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
	01	A55Ah		01h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
	02	A55Ah		02h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
M	03	A55Ah		03h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
I	04	A55Ah		04h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
N	05	A55Ah		05h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
O	06	A55Ah		06h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
R	07	A55Ah		07h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
F	08	A55Ah		08h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
R	09	A55Ah		09h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
A	10	A55Ah		0Ah	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
M	11	A55Ah		0Bh	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
E	12	A55Ah		0Ch	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
	13	A55Ah		00h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
	14	A55Ah		0Eh	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
	15	A55Ah		0Fh	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA

SIXTH REQUEST PER MINOR FRAME

		BYTE 121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144
	00	A55Ah		00h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
	01	A55Ah		01h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
	02	A55Ah		02h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
M	03	A55Ah		03h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
I	04	A55Ah		04h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
N	05	A55Ah		05h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
O	06	A55Ah		06h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
R	07	A55Ah		07h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
F	08	A55Ah		08h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
R	09	A55Ah		09h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
A	10	A55Ah		0Ah	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
M	11	A55Ah		0Bh	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
E	12	A55Ah		0Ch	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
	13	A55Ah		00h	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
	14	A55Ah		0Eh	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
	15	A55Ah		0Fh	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA

DEFINITION OF ENTRIES 8/3/1989

A00 through A31:
Encoded particle count at thirty-one energy levels. Measurements are from analyzer A. (8 bits)

A31 - R00U000S MF:00 BYTE:04	A15 - R00U016S MF:03 BYTE:05
A30 - R00U001S MF:00 BYTE:05	A14 - R00U017S MF:03 BYTE:06
A29 - R00U002S MF:00 BYTE:06	A13 - R00U018S MF:03 BYTE:07
A28 - R00U003S MF:00 BYTE:07	A12 - R00U019S MF:03 BYTE:08
A27 - R00U004S MF:00 BYTE:08	A11 - R00U020S MF:04 BYTE:04
A26 - R00U005S MF:01 BYTE:04	A10 - R00U021S MF:04 BYTE:05
A25 - R00U006S MF:01 BYTE:05	A09 - R00U022S MF:04 BYTE:06
A24 - R00U007S MF:01 BYTE:06	A08 - R00U023S MF:04 BYTE:07
A23 - R00U008S MF:01 BYTE:07	A07 - R00U024S MF:04 BYTE:08
A22 - R00U009S MF:01 BYTE:08	A06 - R00U025S MF:05 BYTE:04
A21 - R00U010S MF:02 BYTE:04	A05 - R00U026S MF:05 BYTE:05
A20 - R00U011S MF:02 BYTE:05	A04 - R00U027S MF:05 BYTE:06
A19 - R00U012S MF:02 BYTE:06	A03 - R00U028S MF:05 BYTE:07
A18 - R00U013S MF:02 BYTE:07	A02 - R00U029S MF:05 BYTE:08
A17 - R00U014S MF:02 BYTE:08	A01 - R00U030S MF:06 BYTE:04
A16 - R00U015S MF:03 BYTE:04	A00 - R00U031S MF:06 BYTE:05

MODE:
Present operating mode of the SPREE instrument package. (8 bits)
MODE - R00U032S MF:06 BYTE:06

AZIMUTHA:
Encoded azimuth of analyzer A. (16 bits)
AZIMUTHA - R00U033S MF:07 BYTE:07,08

B00 through B31:
Same as A00 through A31 except measurements are from analyzer B. (8 bits)

B31 - R00U034S MF:08 BYTE:04	B15 - R00U050S MF:11 BYTE:05
B30 - R00U035S MF:08 BYTE:05	B14 - R00U051S MF:11 BYTE:06
B29 - R00U036S MF:08 BYTE:06	B13 - R00U052S MF:11 BYTE:07
B28 - R00U037S MF:08 BYTE:07	B12 - R00U053S MF:11 BYTE:08
B27 - R00U038S MF:08 BYTE:08	B11 - R00U054S MF:12 BYTE:04
B26 - R00U039S MF:09 BYTE:04	B10 - R00U055S MF:12 BYTE:05
B25 - R00U040S MF:09 BYTE:05	B09 - R00U056S MF:12 BYTE:06
B24 - R00U041S MF:09 BYTE:06	B08 - R00U057S MF:12 BYTE:07
B23 - R00U042S MF:09 BYTE:07	B07 - R00U058S MF:12 BYTE:08
B22 - R00U043S MF:09 BYTE:08	B06 - R00U059S MF:13 BYTE:04
B21 - R00U044S MF:10 BYTE:04	B05 - R00U060S MF:13 BYTE:05
B20 - R00U045S MF:10 BYTE:05	B04 - R00U061S MF:13 BYTE:06
B19 - R00U046S MF:10 BYTE:06	B03 - R00U062S MF:13 BYTE:07
B18 - R00U047S MF:10 BYTE:07	B02 - R00U063S MF:13 BYTE:08

817 - R00U048S MF:10 BYTE:08
816 - R00U049S MF:11 BYTE:04
801 - R00U064S MF:14 BYTE:04
800 - R00U065S MF:14 BYTE:05

POTL:
Encoded Shuttle potential. (8 bits)
POTL - R00U066S MF:14 BYTE:06

ELEV:
Elevation of potential measurement. (8 bits)
ELEV - R00U067S MF:14 BYTE:07

CONF:
Confidence factor of potential determining algorithm. Eighth bit indicates which analyzer was selected by the algorithm. (8 bits)
CONF - R00U068S MF:14 BYTE:08

UCNT:
Encoded count at the energy adjacent and above the peak energy. (8 bits)
UCNT - R00U069S MF:15 BYTE:04

CCNT:
Encoded count determining the peak energy. The peak was detected at the indicated azimuth and elevation. (8 bits)
CCNT - R00U070S MF:15 BYTE:05

LCNT:
Encoded count at the energy adjacent and below the peak energy. (8 bits)
LCNT - R00U071S MF:15 BYTE:06

AZIMUTHB:
Encoded azimuth of analyzer B. (16 bits)
AZIMUTHB - R00U072S MF:15 BYTE:07,08

Table M-1 Measurement Signal I/F Definition (SPREE)

Measurement Number	Nomenclature	IF ID	PL ID	Src	Sig Def	IOM Typ	Slot No	Slot Ch	MajF Rate	mF	mFB	St Bit	Bit Len	DDCU	POCC
R00U000S	Energy A31	S	13	R00	SI	SI	20	02	01	000	0004	00	08	X	X
R00U001S	Energy A30	S	13	R00	SI	SI	20	02	01	000	0005	00	08	X	X
R00U002S	Energy A29	S	13	R00	SI	SI	20	02	01	000	0006	00	08	X	X
R00U003S	Energy A28	S	13	R00	SI	SI	20	02	01	000	0007	00	08	X	X
R00U004S	Energy A27	S	13	R00	SI	SI	20	02	01	000	0008	00	08	X	X
R00U005S	Energy A26	S	13	R00	SI	SI	20	02	01	001	0004	00	08	X	X
R00U006S	Energy A25	S	13	R00	SI	SI	20	02	01	001	0005	00	08	X	X
R00U007S	Energy A24	S	13	R00	SI	SI	20	02	01	001	0006	00	08	X	X
R00U008S	Energy A23	S	13	R00	SI	SI	20	02	01	001	0007	00	08	X	X
R00U009S	Energy A22	S	13	R00	SI	SI	20	02	01	001	0008	00	08	X	X
R00U010S	Energy A21	S	13	R00	SI	SI	20	02	01	002	0004	00	08	X	X
R00U011S	Energy A20	S	13	R00	SI	SI	20	02	01	002	0005	00	08	X	X
R00U012S	Energy A19	S	13	R00	SI	SI	20	02	01	002	0006	00	08	X	X
R00U013S	Energy A18	S	13	R00	SI	SI	20	02	01	002	0007	00	08	X	X
R00U014S	Energy A17	S	13	R00	SI	SI	20	02	01	002	0008	00	08	X	X
R00U015S	Energy A16	S	13	R00	SI	SI	20	02	01	003	0004	00	08	X	X
R00U016S	Energy A15	S	13	R00	SI	SI	20	02	01	003	0005	00	08	X	X
R00U017S	Energy A14	S	13	R00	SI	SI	20	02	01	003	0006	00	08	X	X
R00U018S	Energy A13	S	13	R00	SI	SI	20	02	01	003	0007	00	08	X	X
R00U019S	Energy A12	S	13	R00	SI	SI	20	02	01	003	0008	00	08	X	X
R00U020S	Energy A11	S	13	R00	SI	SI	20	02	01	004	0004	00	08	X	X
R00U021S	Energy A10	S	13	R00	SI	SI	20	02	01	004	0005	00	08	X	X
R00U022S	Energy A09	S	13	R00	SI	SI	20	02	01	004	0006	00	08	X	X
R00U023S	Energy A08	S	13	R00	SI	SI	20	02	01	004	0007	00	08	X	X
R00U024S	Energy A07	S	13	R00	SI	SI	20	02	01	004	0008	00	08	X	X
R00U025S	Energy A06	S	13	R00	SI	SI	20	02	01	005	0004	00	08	X	X
R00U026S	Energy A05	S	13	R00	SI	SI	20	02	01	005	0005	00	08	X	X
R00U027S	Energy A04	S	13	R00	SI	SI	20	02	01	005	0006	00	08	X	X
R00U028S	Energy A03	S	13	R00	SI	SI	20	02	01	005	0007	00	08	X	X
R00U029S	Energy A02	S	13	R00	SI	SI	20	02	01	005	0008	00	08	X	X
R00U030S	Energy A01	S	13	R00	SI	SI	20	02	01	006	0004	00	08	X	X
R00U031S	Energy A00	S	13	R00	SI	SI	20	02	01	006	0005	00	08	X	X
R00U032S	Mode	S	13	R00	SI	SI	20	02	01	006	0006	00	08	X	X
R00U033S	Azimuth A	S	13	R00	SI	SI	20	02	01	007	0007	00	16	X	X

Measurement Number	Nomenclature	IF ID	PL ID	Src	Sig Def	IOM Typ	Slot No	Ch	MajF Rate	mF	mFB	St Bit	Bit Len	DDCU	POCC
R00U034S	Energy B31	S	13	R00	SI	SI	20	02	01	008	0004	00	08	X	X
R00U035S	Energy B30	S	13	R00	SI	SI	20	02	01	008	0005	00	08	X	X
R00U036S	Energy B29	S	13	R00	SI	SI	20	02	01	008	0006	00	08	X	X
R00U037S	Energy B28	S	13	R00	SI	SI	20	02	01	008	0007	00	08	X	X
R00U038S	Energy B27	S	13	R00	SI	SI	20	02	01	008	0008	00	08	X	X
R00U039S	Energy B26	S	13	R00	SI	SI	20	02	01	009	0004	00	08	X	X
R00U040S	Energy B25	S	13	R00	SI	SI	20	02	01	009	0005	00	08	X	X
R00U041S	Energy B24	S	13	R00	SI	SI	20	02	01	009	0006	00	08	X	X
R00U042S	Energy B23	S	13	R00	SI	SI	20	02	01	009	0007	00	08	X	X
R00U043S	Energy B22	S	13	R00	SI	SI	20	02	01	009	0008	00	08	X	X
R00U044S	Energy B21	S	13	R00	SI	SI	20	02	01	010	0004	00	08	X	X
R00U045S	Energy B20	S	13	R00	SI	SI	20	02	01	010	0005	00	08	X	X
R00U046S	Energy B19	S	13	R00	SI	SI	20	02	01	010	0006	00	08	X	X
R00U047S	Energy B18	S	13	R00	SI	SI	20	02	01	010	0007	00	08	X	X
R00U048S	Energy B17	S	13	R00	SI	SI	20	02	01	010	0008	00	08	X	X
R00U049S	Energy B16	S	13	R00	SI	SI	20	02	01	011	0004	00	08	X	X
R00U050S	Energy B15	S	13	R00	SI	SI	20	02	01	011	0005	00	08	X	X
R00U051S	Energy B14	S	13	R00	SI	SI	20	02	01	011	0006	00	08	X	X
R00U052S	Energy B13	S	13	R00	SI	SI	20	02	01	011	0007	00	08	X	X
R00U053S	Energy B12	S	13	R00	SI	SI	20	02	01	011	0008	00	08	X	X
R00U054S	Energy B11	S	13	R00	SI	SI	20	02	01	012	0004	00	08	X	X
R00U055S	Energy B10	S	13	R00	SI	SI	20	02	01	012	0005	00	08	X	X
R00U056S	Energy B09	S	13	R00	SI	SI	20	02	01	012	0006	00	08	X	X
R00U057S	Energy B08	S	13	R00	SI	SI	20	02	01	012	0007	00	08	X	X
R00U058S	Energy B07	S	13	R00	SI	SI	20	02	01	012	0008	00	08	X	X
R00U059S	Energy B06	S	13	R00	SI	SI	20	02	01	013	0004	00	08	X	X
R00U060S	Energy B05	S	13	R00	SI	SI	20	02	01	013	0005	00	08	X	X
R00U061S	Energy B04	S	13	R00	SI	SI	20	02	01	013	0006	00	08	X	X
R00U062S	Energy B03	S	13	R00	SI	SI	20	02	01	013	0007	00	08	X	X
R00U063S	Energy B02	S	13	R00	SI	SI	20	02	01	013	0008	00	08	X	X
R00U064S	Energy B01	S	13	R00	SI	SI	20	02	01	014	0004	00	08	X	X
R00U065S	Energy B00	S	13	R00	SI	SI	20	02	01	014	0005	00	08	X	X
R00U066S	Potential	S	13	R00	SI	SI	20	02	01	014	0006	00	08	X	X
R00U067S	Elevation	S	13	R00	SI	SI	20	02	01	014	0007	00	08	X	X
R00U068S	Confidence	S	13	R00	SI	SI	20	02	01	014	0008	00	08	X	X
R00U069S	Upper Count	S	13	R00	SI	SI	20	02	01	015	0004	00	08	X	X
R00U070S	Center Count	S	13	R00	SI	SI	20	02	01	015	0005	00	08	X	X
R00U071S	Lower Count	S	13	R00	SI	SI	20	02	01	015	0006	00	08	X	X
R00U072S	Azimuth B	S	13	R00	SI	SI	20	02	01	015	0007	00	16	X	X

TABLE A: CORRESPONDENCE OF SPREE MEAS #R00U066S TO SHUTTLE POTENTIAL

VALUE OF R00U066S	POTENTIAL IN kV
0	-0.01
1	-0.01
2	-0.02
3	-0.02
4	-0.03
5	-0.03
6	-0.04
7	-0.05
8	-0.06
9	-0.08
10	-0.10
11	-0.12
12	-0.15
13	-0.19
14	-0.23
15	-0.29
16	-0.35
17	-0.44
18	-0.55
19	-0.68
20	-0.84
21	-1.00
22	-1.30
23	-1.60
24	-2.00
25	-2.50
26	-3.10
27	-3.80
28	-4.70
29	-5.90
30	-7.30
31	-9.00

TABLE 8: SPREE MODE DISPLAY ALGORITHM

Mode strings needed for DDCU:
Measurement Number R00U032S

MSB	LSB	Description
XXXX	XXX0	Analyzer A Off
XXXX	XXX1	Analyzer A On
XXXX	XX0X	Analyzer A Parked
XXXX	XX1X	Analyzer A Rotating
XXXX	X0XX	Analyzer A 1 Sweep/Second
XXXX	X1XX	Analyzer A 8 Sweeps/Second
XXXX	0XXX	Analyzer B Off
XXXX	1XXX	Analyzer B On
XXX0	XXXX	Analyzer B Parked
XXX1	XXXX	Analyzer B Rotating
XX0X	XXXX	Analyzer B 1 Sweep/Second
XX1X	XXXX	Analyzer B 8 Sweeps/Second

X=Don't Care

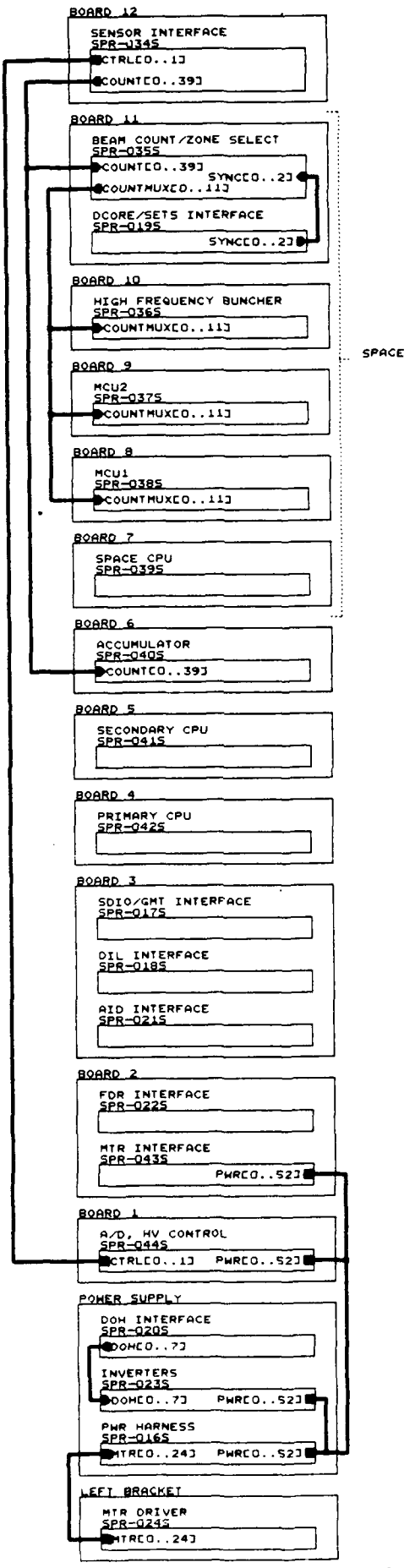


FIGURE QR8-15

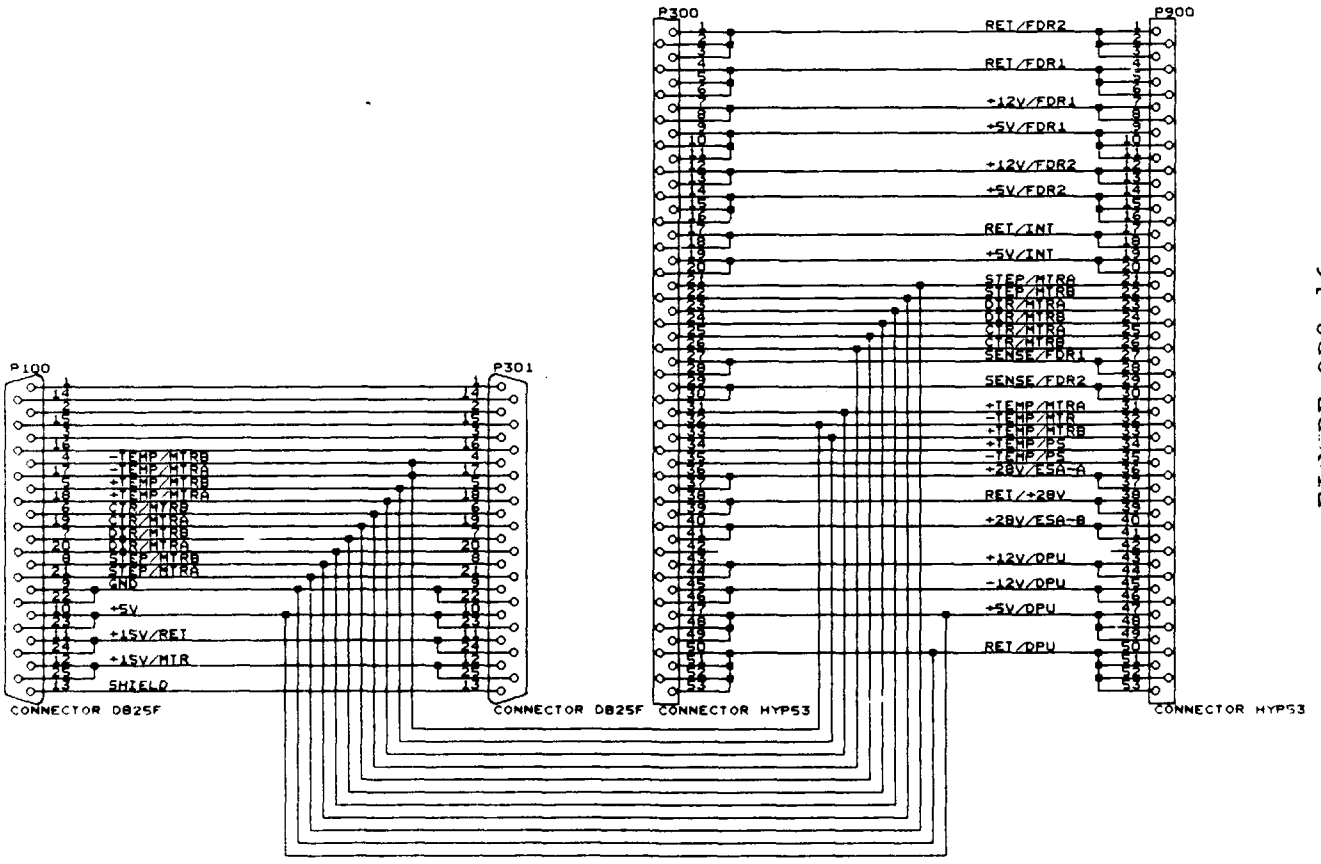


FIGURE QR8-16

AMPTEK, INC.		
Title: PWR HARNESS		
Size: E	Document Number: SPR-0165	REV: A
Date: September 5, 1989	Sheet: 23 of 42	

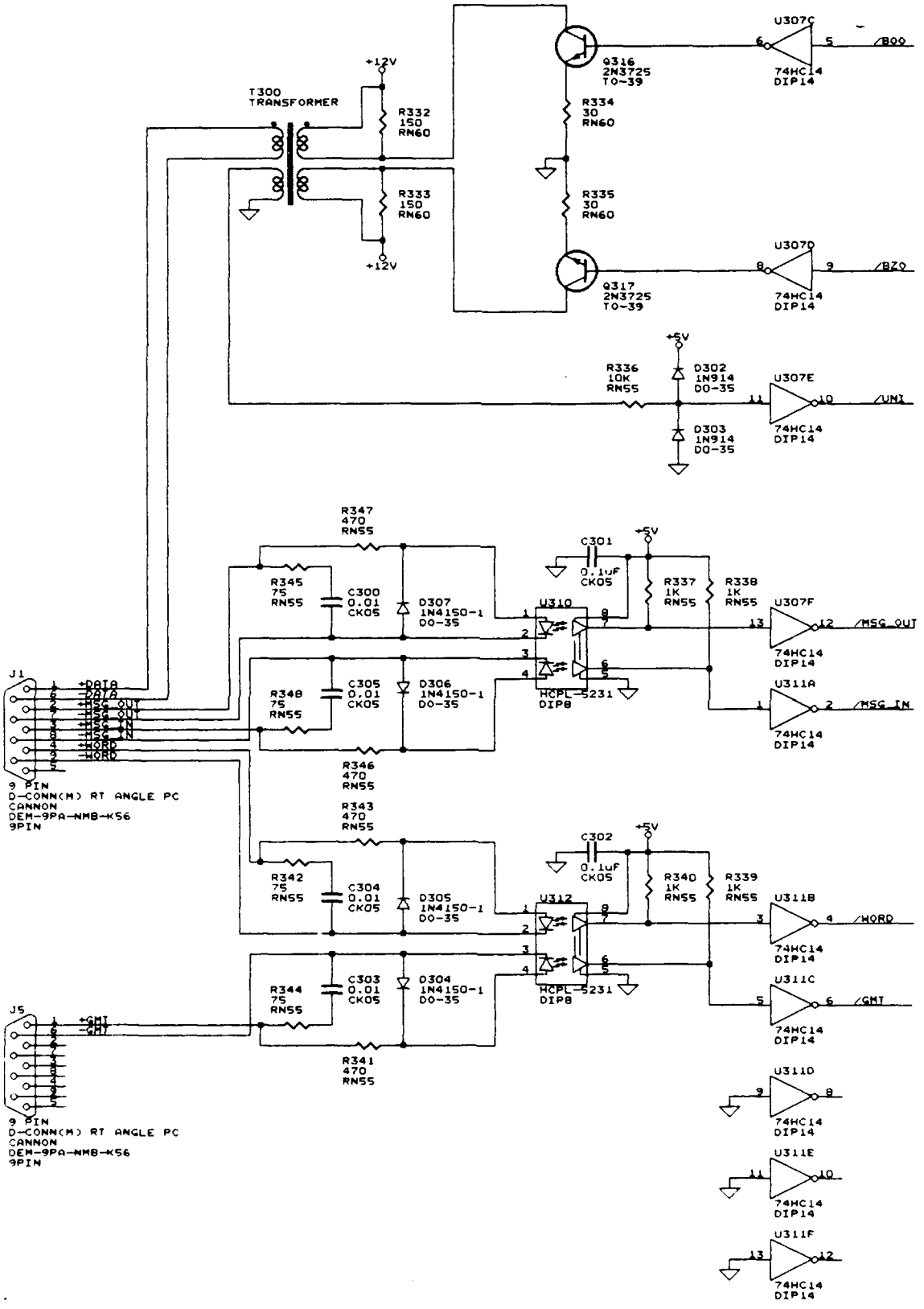


FIGURE QR8-17

PSPICE SIMULATION OF SDIO DATA
SPR-0475

AMPTEK, INC.		
Title: SDIO/GMI INTERFACE		
Size: E	Document Number: SPR-0175	REV: A
Date: September 8, 1989	Sheet 2 of 2	

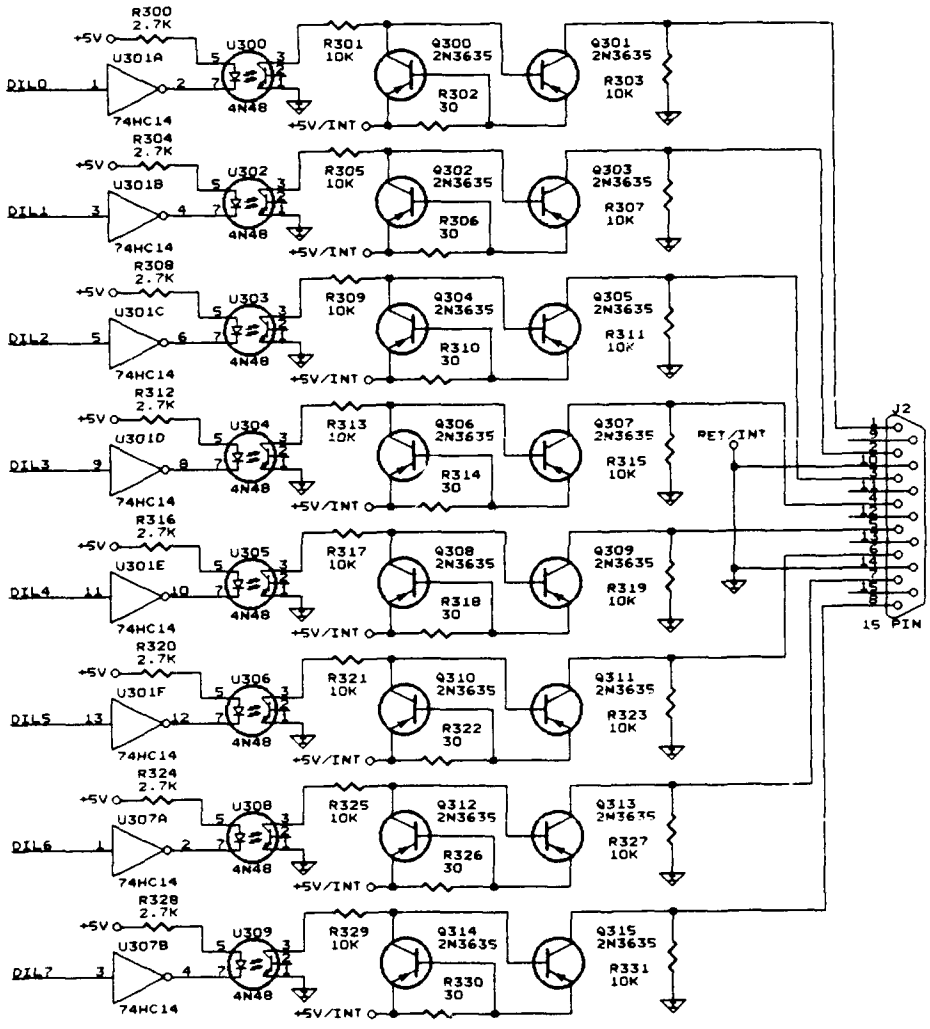


FIGURE QR9-18

AMPTEK, INC.		
Title: DIL INTERFACE		
Size: E	Document Number: SPR-0185	REV: A
Date: September 6, 1989	Sheet 1 of 2	

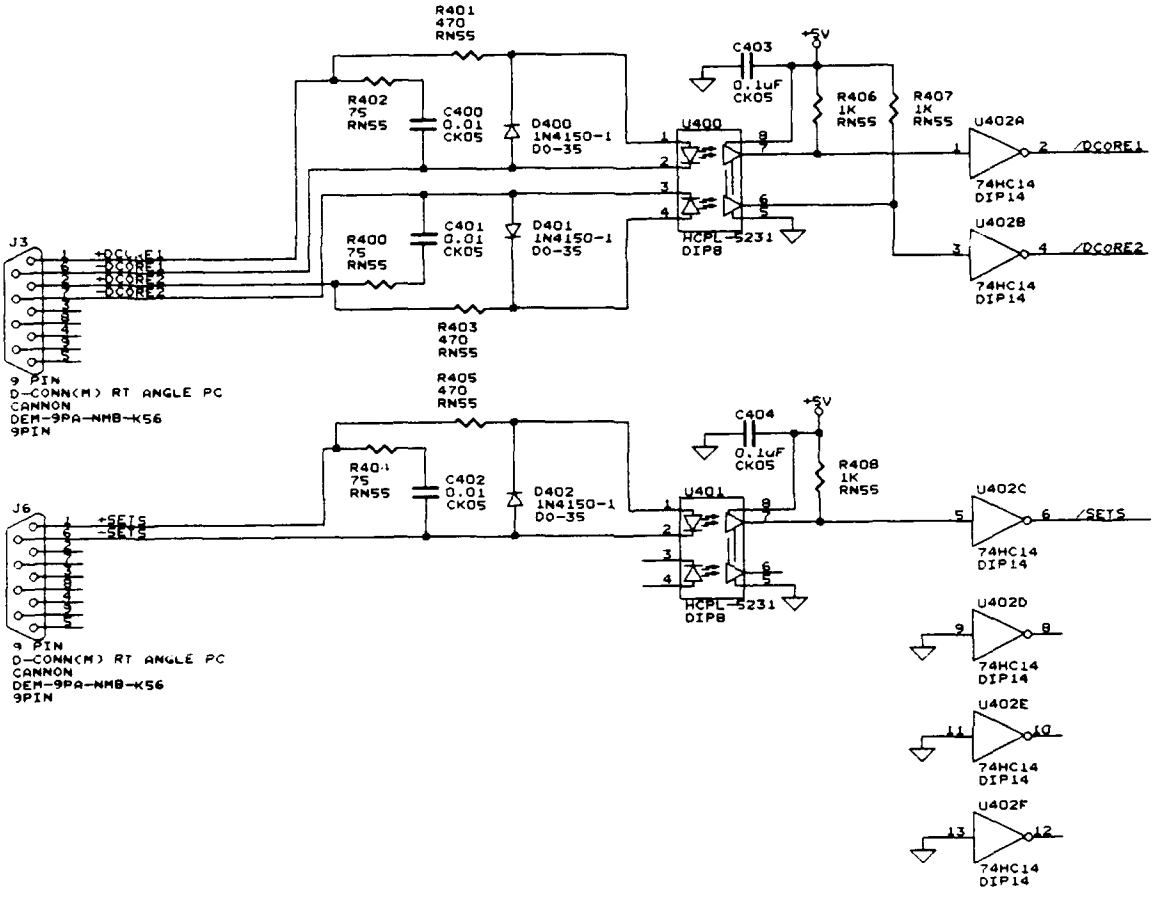


FIGURE QR8-19

AMPTEK, INC.		
Title: DCORE/SETS INTERFACE		
Size: E	Document Number: SPR-0195	REV: A
Date: September 8, 1989	Sheet 1 of 1	

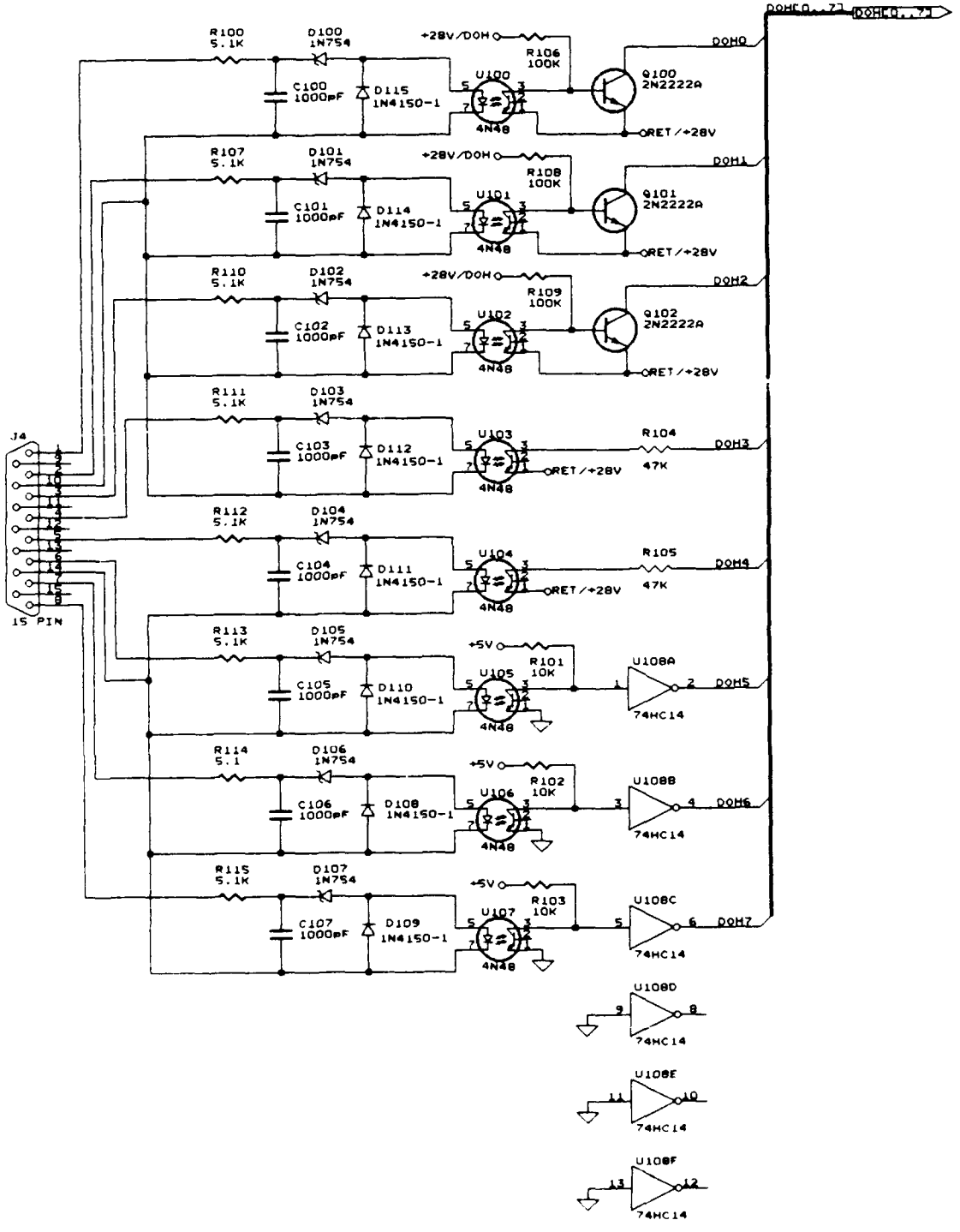


FIGURE QR8-20

AMPTEK, INC.		
Title: DOH INTERFACE		
Size: E	Document Number: SPR-0205	REV: A
Date: September 6, 1989	Sheet 1 of 2	

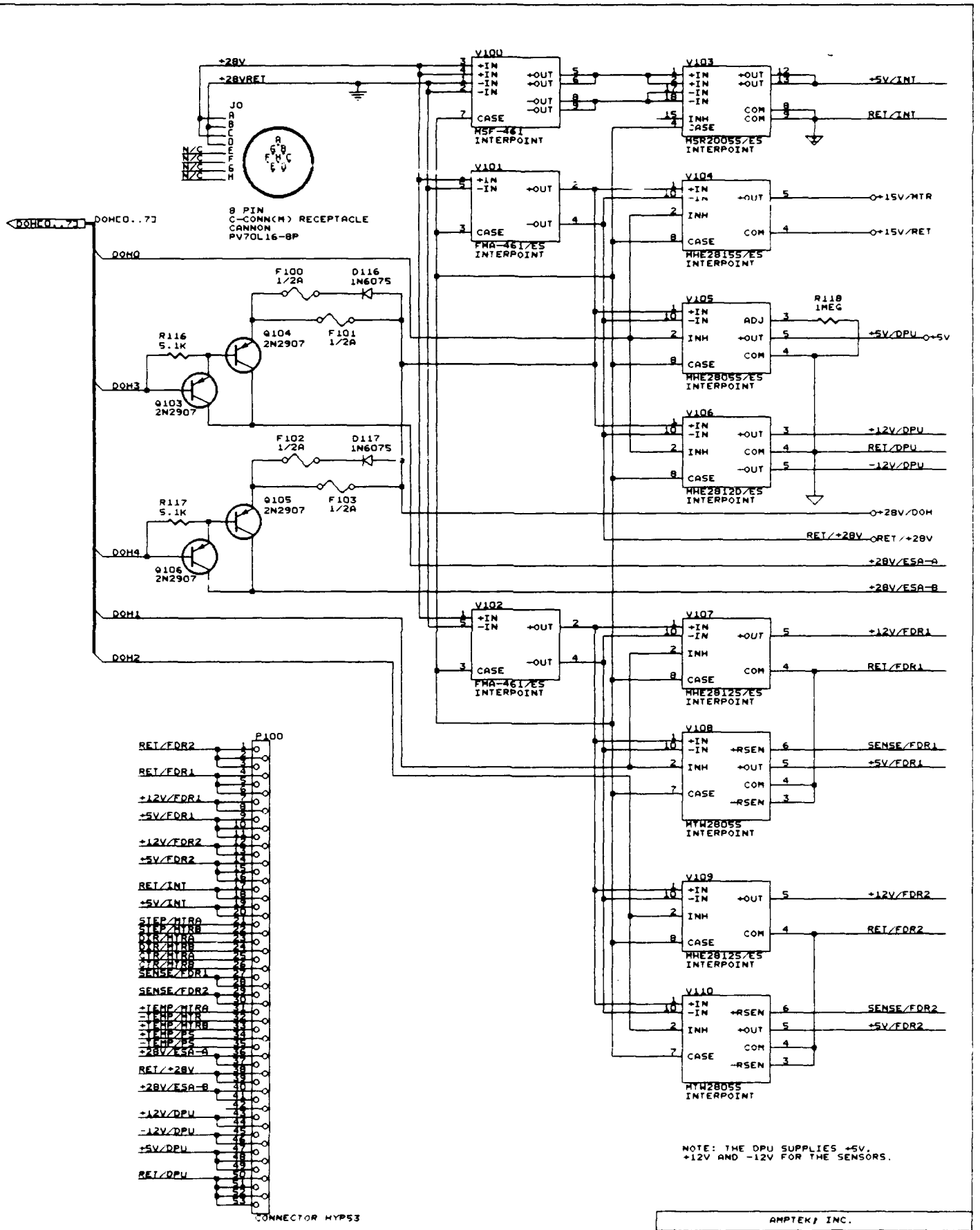


FIGURE QR8-21

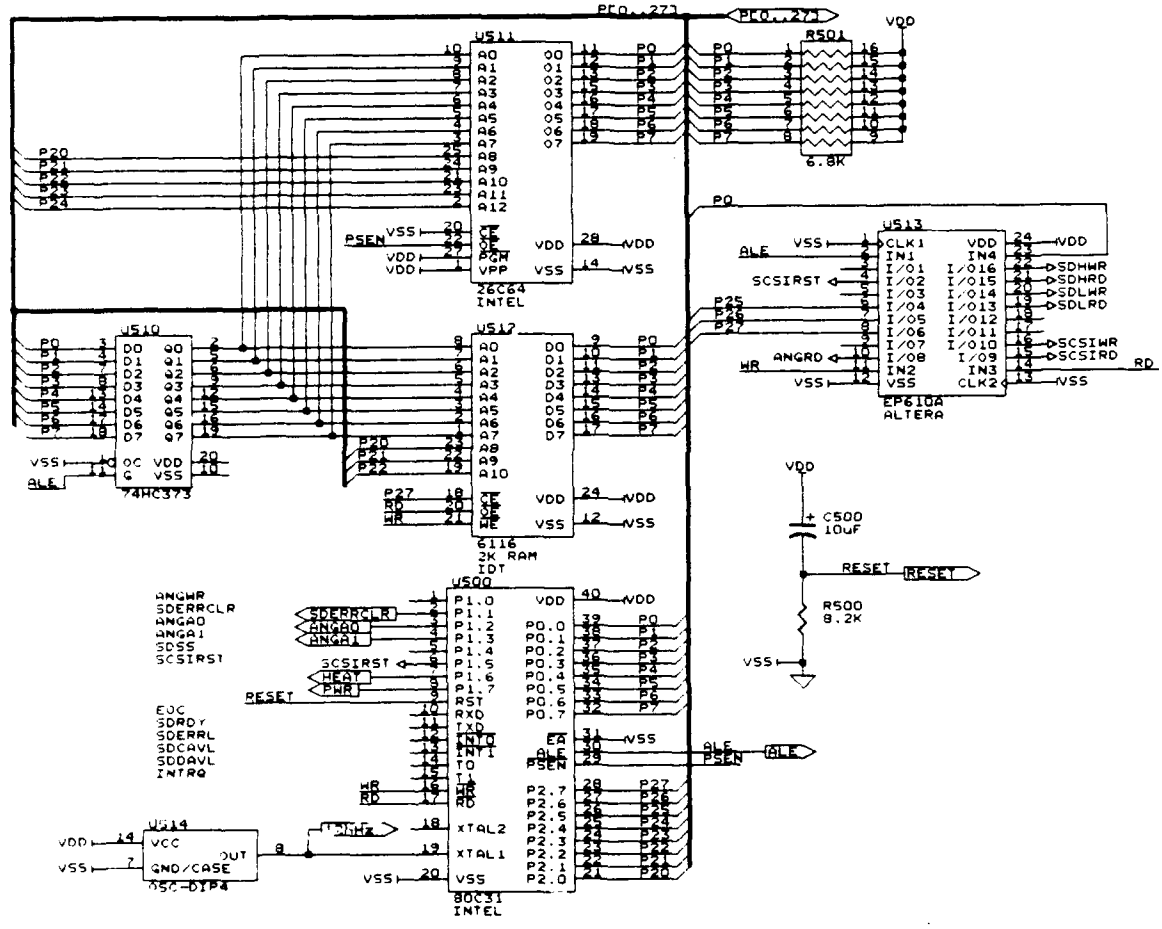


FIGURE QR8-22

	AMPTEK, INC.	
Title	CPU	
Size E	Document Number SPA-0045	REV A
Date: September 1, 1989	Sheet 30 of	42

DPU/FDR INTERFACE TIMING
SPR-0095

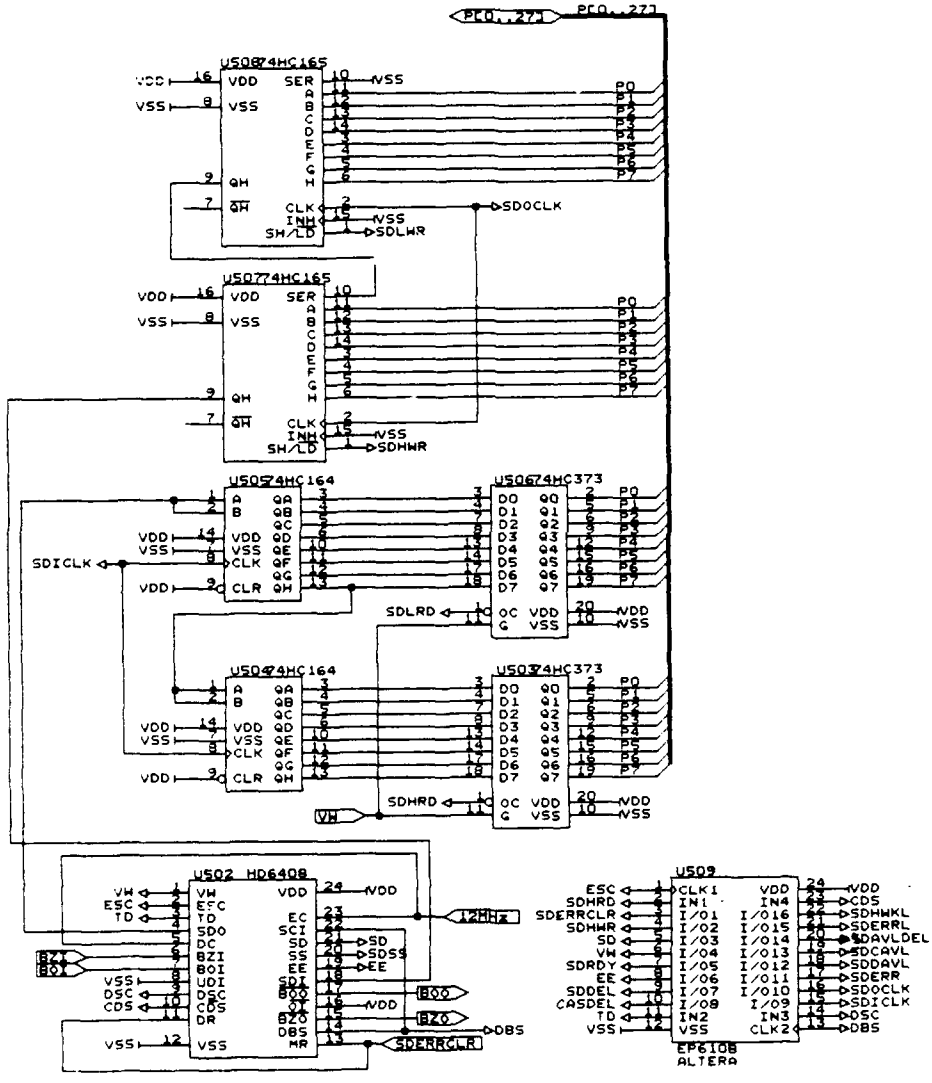


FIGURE QR8-23

AMPTEK, INC.		
Title: MANCHESTER SERIAL PORT		
Size: E	Document Number: SPR-0055	REV: A
Date: September 1, 1989	Sheet 28 of 42	

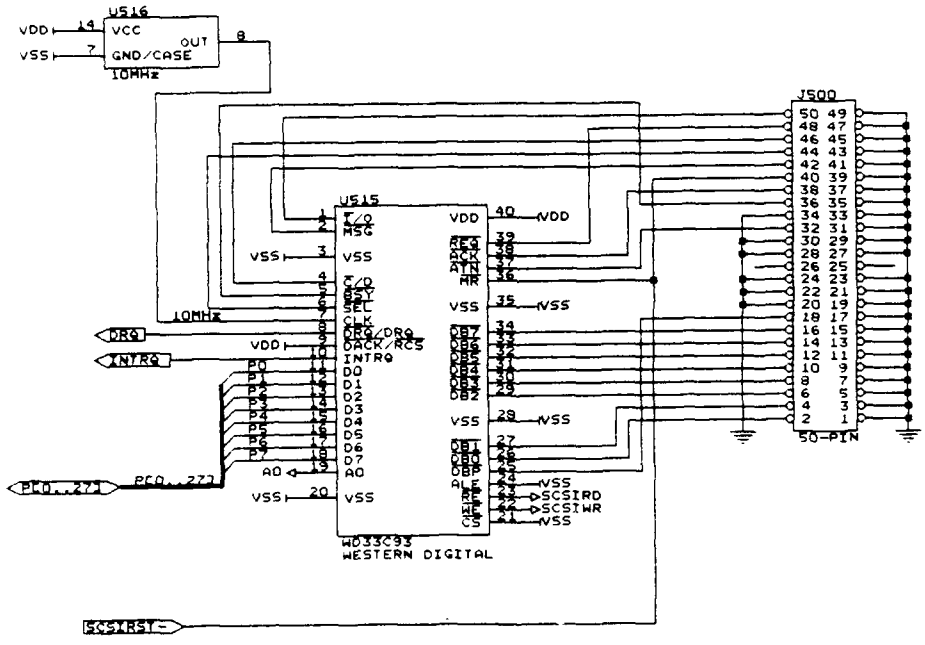


FIGURE QR8-24

AMPTEK, INC.		
Title: SCSI		
Size: E	Document Number: SPR-0075	REV: A
Date: September 1, 1989	Sheet 31 of 42	

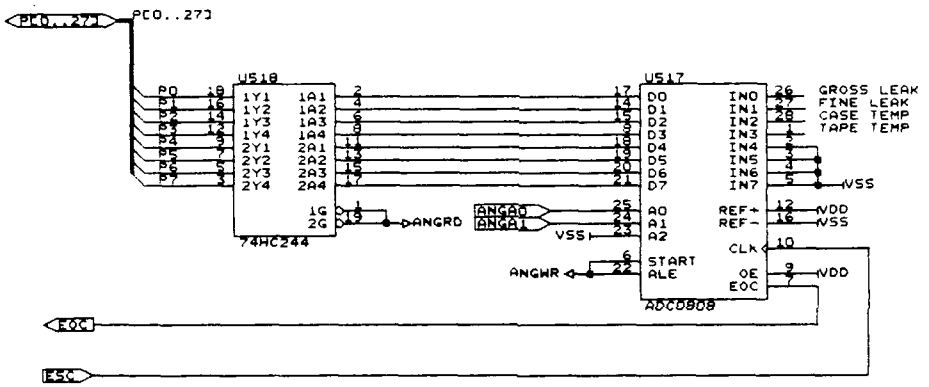


FIGURE QR8-25

AMPTEK, INC.		
Title: ANALOG		
Size: E	Document Number: SPR-0085	REV: A
Date: September 1, 1989	Sheet 32 of 42	

SPACE

(Consulting services of Dr. M.P. Gough, University of Sussex.)

Breadboard models of the SPACE CPU (80C86) and Low Frequency Correlator (MMU-80C51) have arrived in the UK for software verification.

At this time the 80C51 software is fully written and tested, while the 80C86 software implementation is 80% complete. The 80C86 software should be finished by mid-September.

Although a little behind our original schedule we are still hoping to have an initial SPACE function verification this autumn, with SPACE integration with the SPREE instrument occurring in time for the completion of the whole instrument by around December 1989.

HIGH VOLTAGE SUPPLY.

Designs for the high voltage supply are being breadboarded. The supply will sweep logarithmically through 256 energy steps, 32 for each energy channel. Current monitors are no longer being considered in the design. Optocouplers are under test.

MOTOR DRIVE

The motor drive electronics are complete and have been tested with the DPU prototype. Position sensing has been demonstrated successfully.

INTERFACE

Feedback from the Stanford group has confirmed the use of optical isolation between SETS and SPREE. It is assumed that DCORE will follow shortly. Working schematics have been issued to MMAG. Stan Smith intends to double check switching characteristics and distribute.

FDR

A consultant, Andrew Gruber, was retained to assist in the design of the Bridge Controller (BC). Mr. Gruber delivered an i8051 microcontroller design with sample software routines. Amptek will build a hardware prototype and resume software integration in January.

EGSE

A preliminary design has been completed for the Experiment Ground Support Equipment The EGSE will be contained on an IBM PC card. Power supplies will be external. A prototype wirewrap board has been started and discrete interface have been tested.

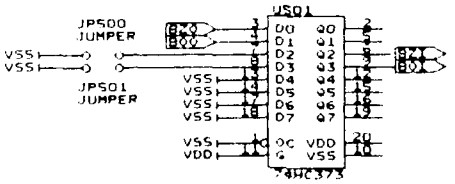


FIGURE QR8-26

AMPTEK, INC.		
Title: DRIVER		
Size: E	Document Number: SPR 0065	REV: B
Date: September 1, 1984	Sheet 27 of 42	

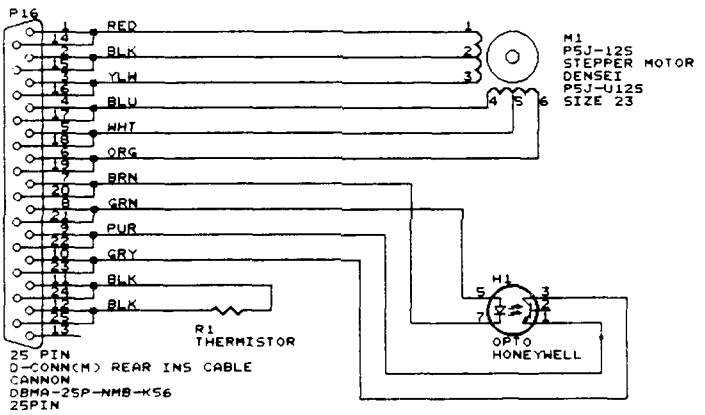


FIGURE QR8-27

AMPTEK, INC.		
Title: MTR A		
Size: E	Document Number: SPR-0275	REV: A
Date: September 6, 1989	Sheet 41 of 42	

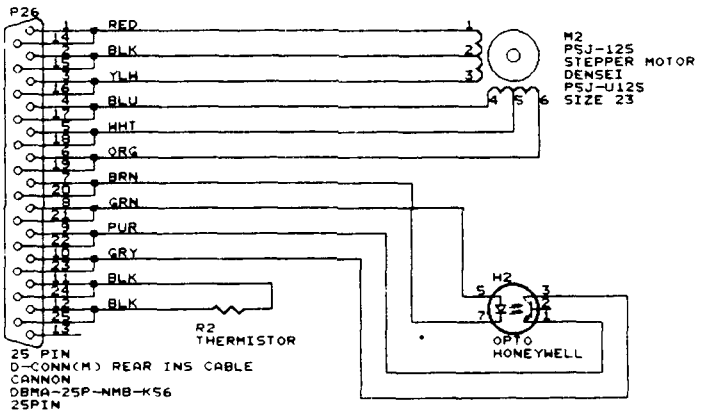


FIGURE QR8-28

AMPTEK, INC.		
Title: MTR B		
Size: E	Document Number: SPR-0285	REV: A
Date: September 6, 1989	Sheet 41 of 42	

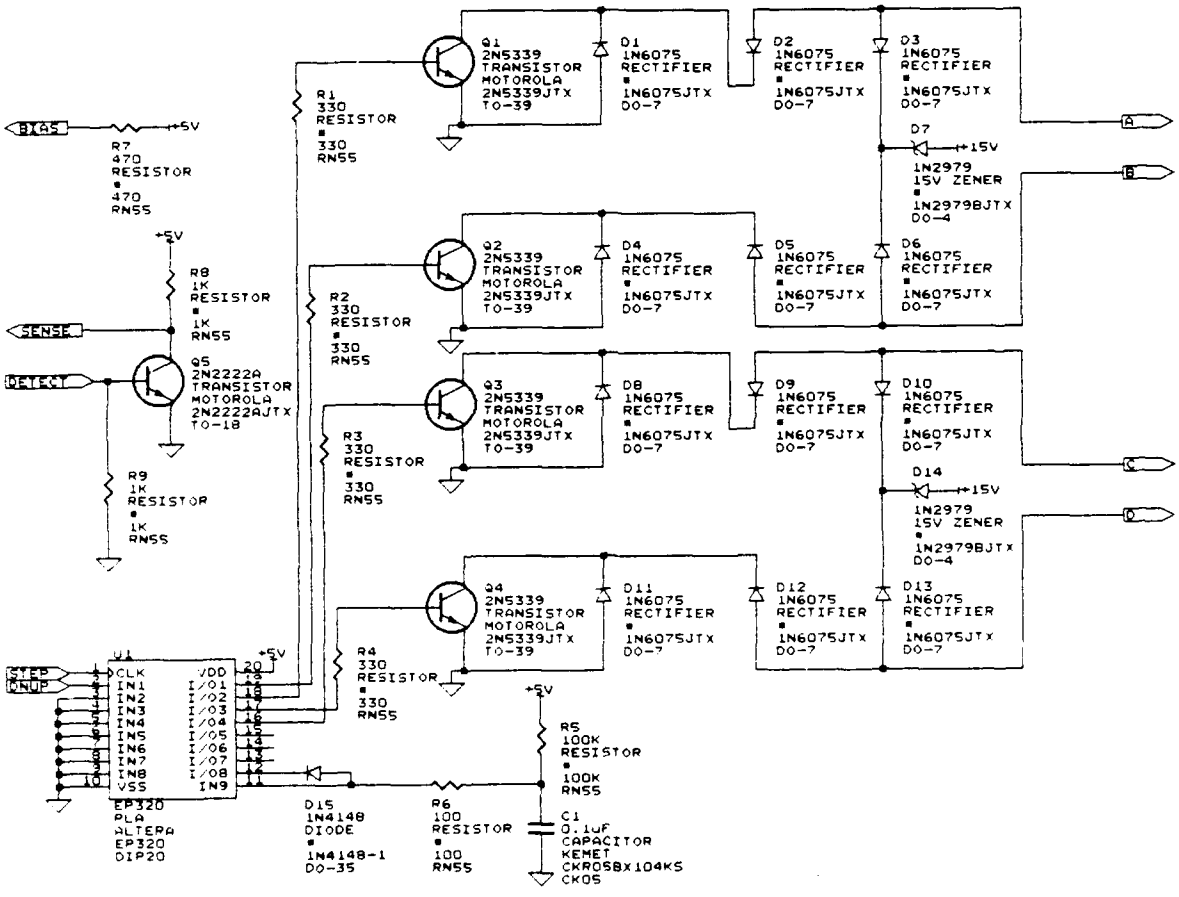


FIGURE QR8-29

AMPTEK, INC.		
Title: MOTOR CONTROL A		
Size: E	Document Number: SPR-0255	REV: A
Date: September 1, 1989	Sheet 19 of 42	

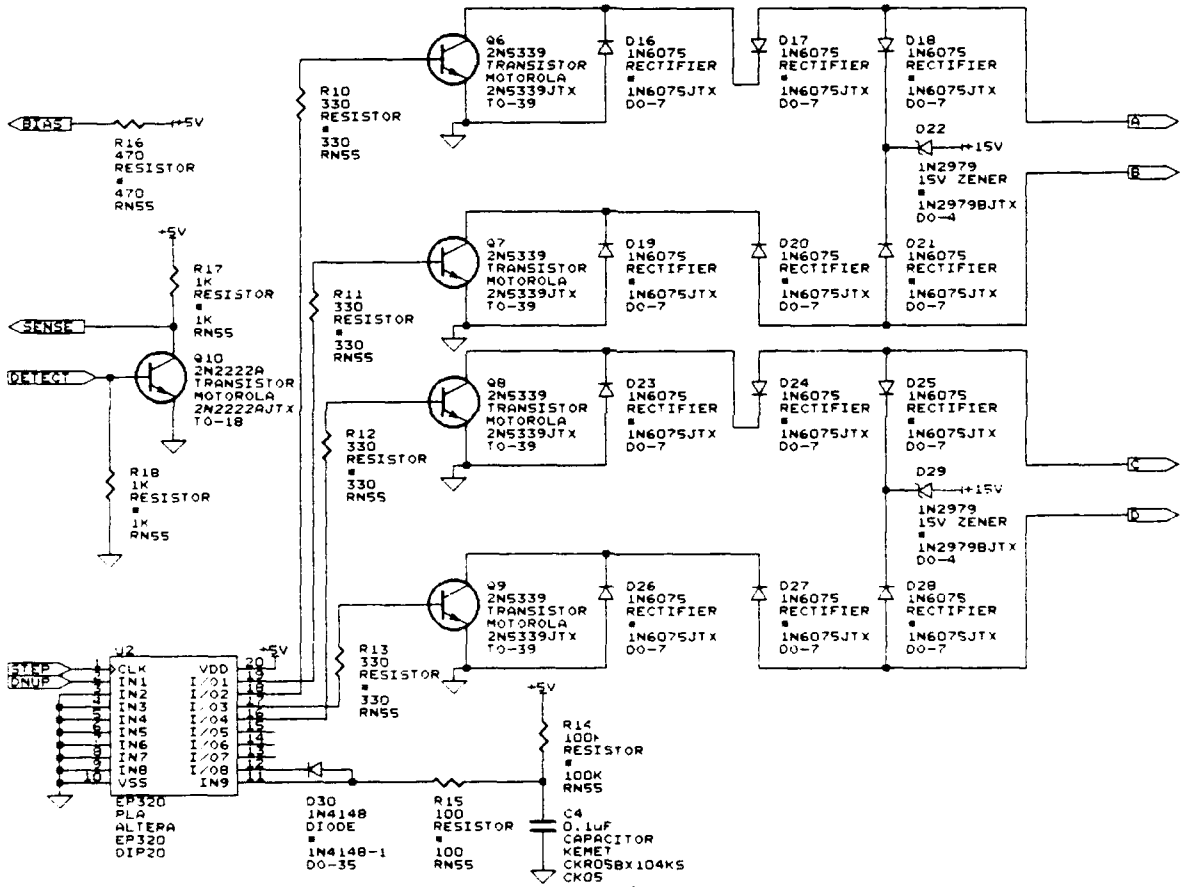


FIGURE QR8-10

AMPTEK, INC.		
Title: MOTOR CONTROL B		
Size: E	Document Number: SPR-0265	REV: A
Date: September 1, 1989	Sheet 20 of 42	

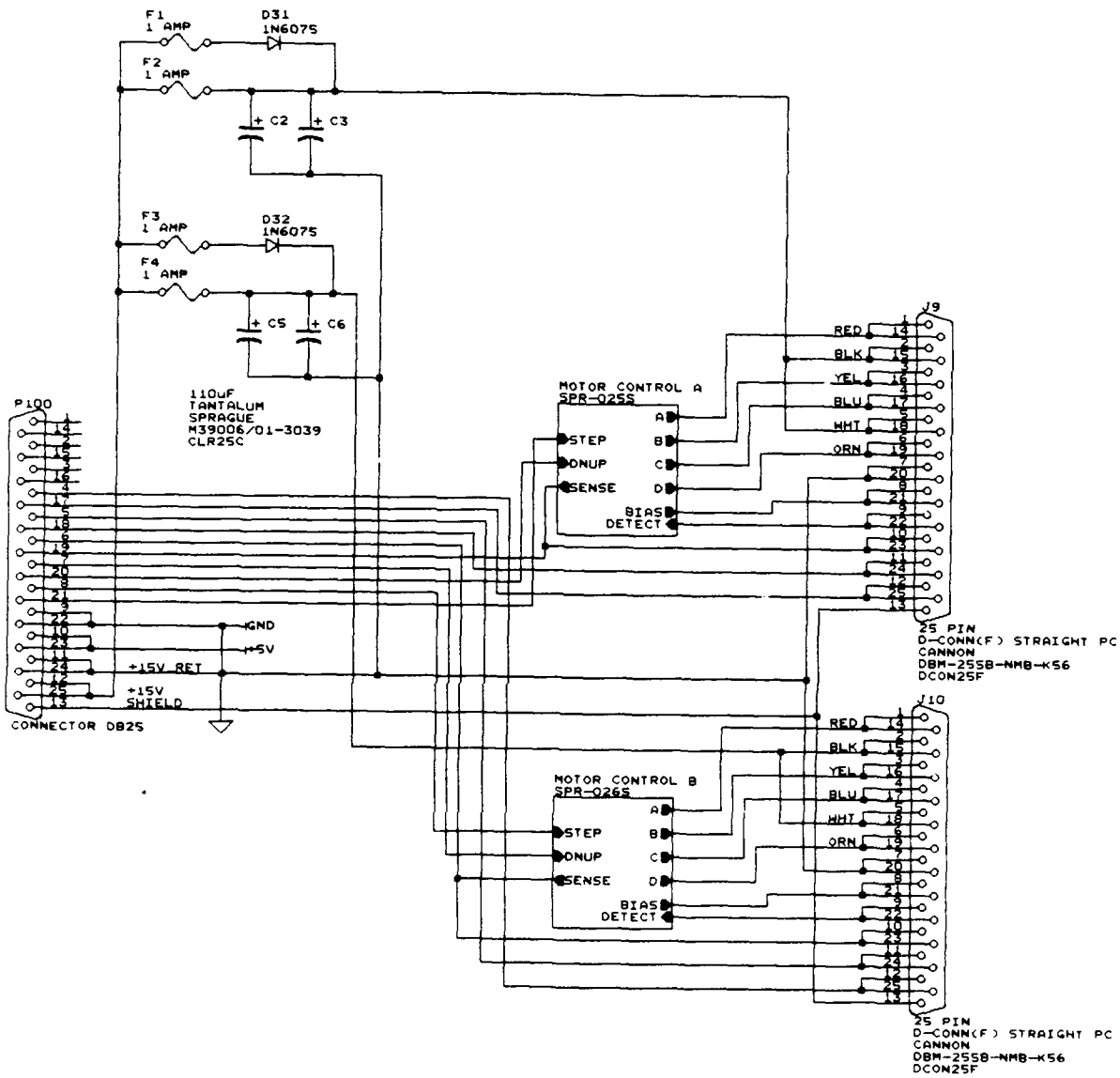


FIGURE QR8-31

AMPTEK, INC.		
Title: MTR INTERFACE		
Size: E	Document Number: SPR-0245	REV: A
Date: September 1, 1989	Sheet 18 of 42	

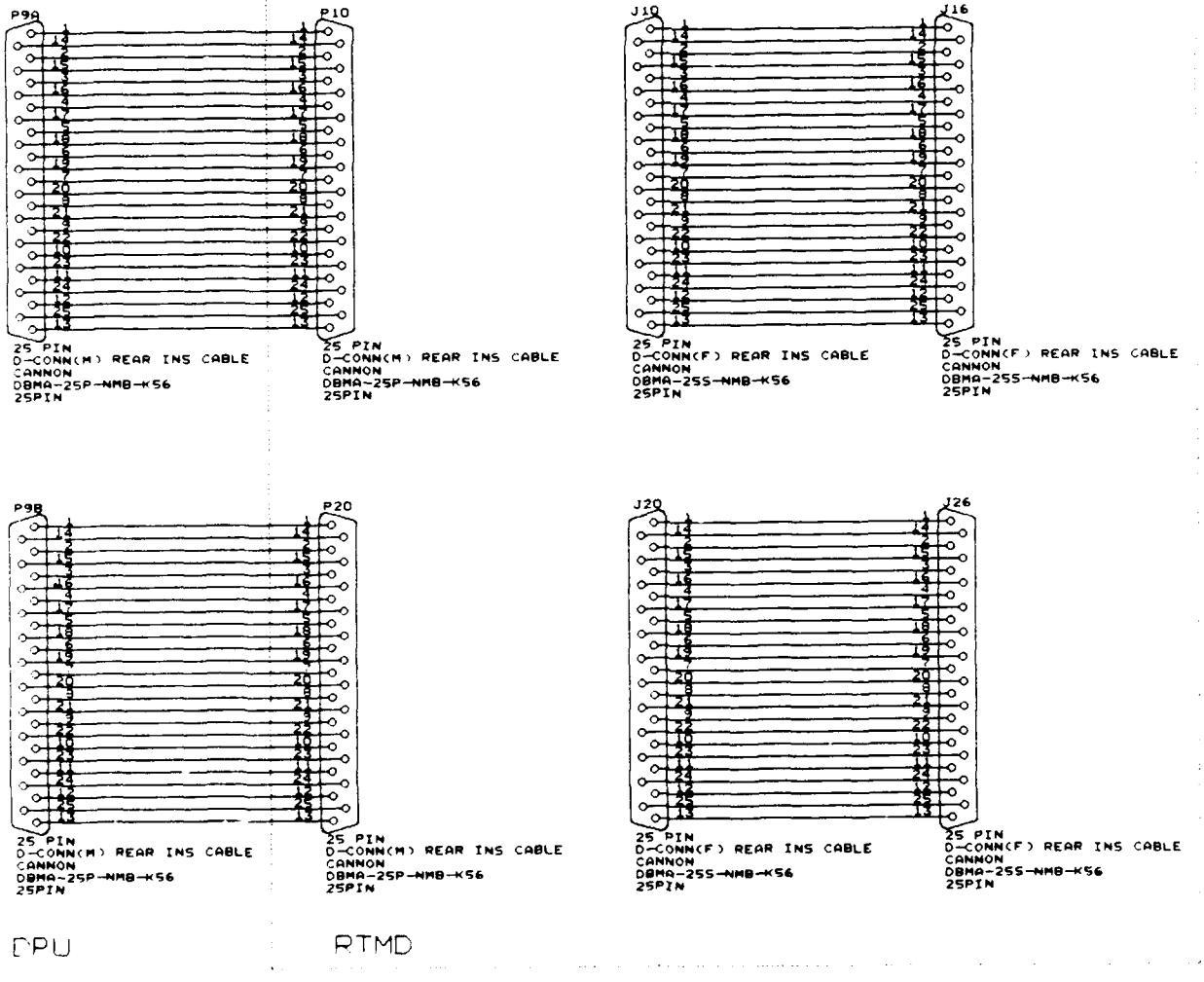


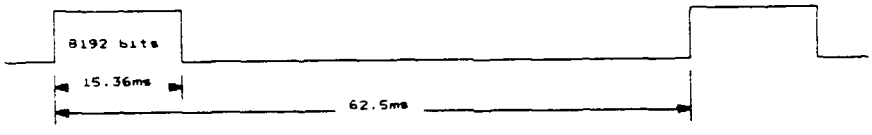
FIGURE QR8-32

AMPTEK, INC.		
Title: MTR HARNESS		
Size: E	Document Number: SPR-0135	REV: A
Date: September 5, 1989	Sheet 25 of 42	

SPREE DPU TO FDR INTERFACE

TRANSMISSION LINE:

CONTROLLER CLOCK	8 MHz
BIT RATE	667 kbps
REQ'D BANDWIDTH	30 MHz
DATA RATE	533 kbps
WORD SIZE	16 bits (MSb FIRST)
WORD RATE	30us/WORD
FRAME SIZE	8192 bits
FRAME RATE	16 FRAMES/s
DUTY CYCLE	25%



2 ANALYZERS x (IONS + ELECTRONS) x 10 SECTORS x
32 ENERGIES/SWEEP x 8 bit RESOLUTION = 10240 bits/sweep

REQUIREMENTS:

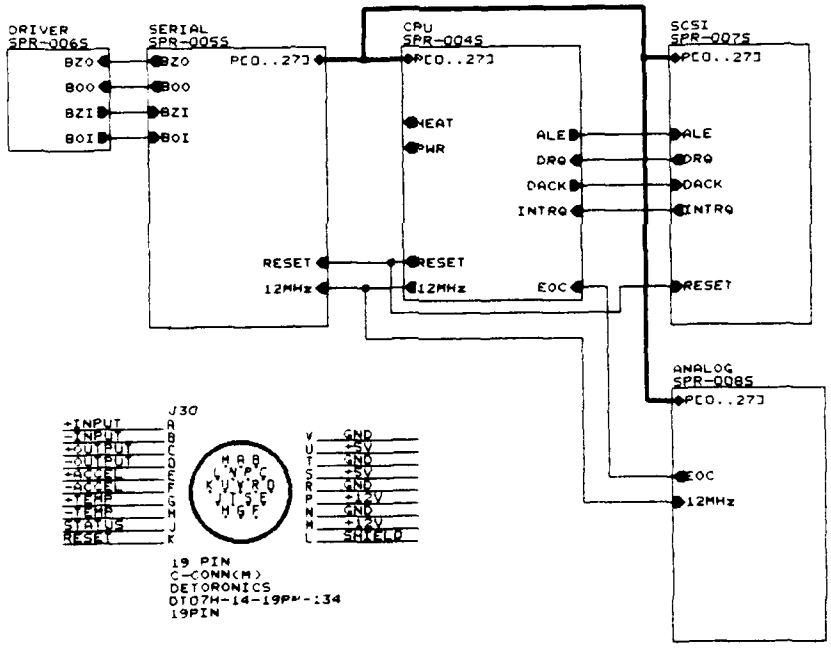
MODE	1 SWEEP/s	10 SWEEPS/s
SPREE	10,240 bps	102,400 bps
SPACE	117,760 bps	25,600 bps
	128,000 bps	128,000 bps
	+	
HOUSE KEEPING	3072 bps	3072 bps
	131,072 bps	131,072 bps

SYNC WORD	4 BYTES
FRAME COUNTER	3 BYTES
GMT (EVEN)/ANALOG & MODE (ODD)	11 BYTES
MAGNETOMETER (EVEN)/RECORDER (ODD)	6 BYTES
HOUSE KEEPING	24 BYTES/FRAME

FIGURE QR8-33

AMPTEK, INC.		
Title: DPU/FDR INTERFACE TIMING		
Size: E	Document Number: SPR-0095	REV: A
Date: September 1, 1989	Sheet 29 of 42	

ADDRESSING	A15	A14	A13
uC <> RAM	0	0	0
uC <> ANALOG	1	1	1
uC <> SERIAL	1	0	1
uC <> SCSI	1	1	0
SERIAL > RAM (DMA)	0	0	1
RAM > SERIAL (DMA)	0	0	1
RAM > SCSI (DMA)	1	1	0
SCSI > RAM (DMA)	0	1	0



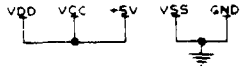


FIGURE QR8-34

AMPTEK, INC.		
Title: FDR 1		
Size: E	Document Number: SPR-002S	REV: A
Date: August 31, 1989	Sheet 2 of 42	

ADDRESSING	A15	A14	A13
uC <> RAM	0	0	0
uC <> ANALOG	0	0	1
uC <> SERIAL	0	1	0
uC <> SCSI	0	1	1
SERIAL > RAM (DMA)	1	0	0
RAM > SERIAL (DMA)	1	0	1
RAM > SCSI (DMA)	1	1	0
SCSI > RAM (DMA)	1	1	1

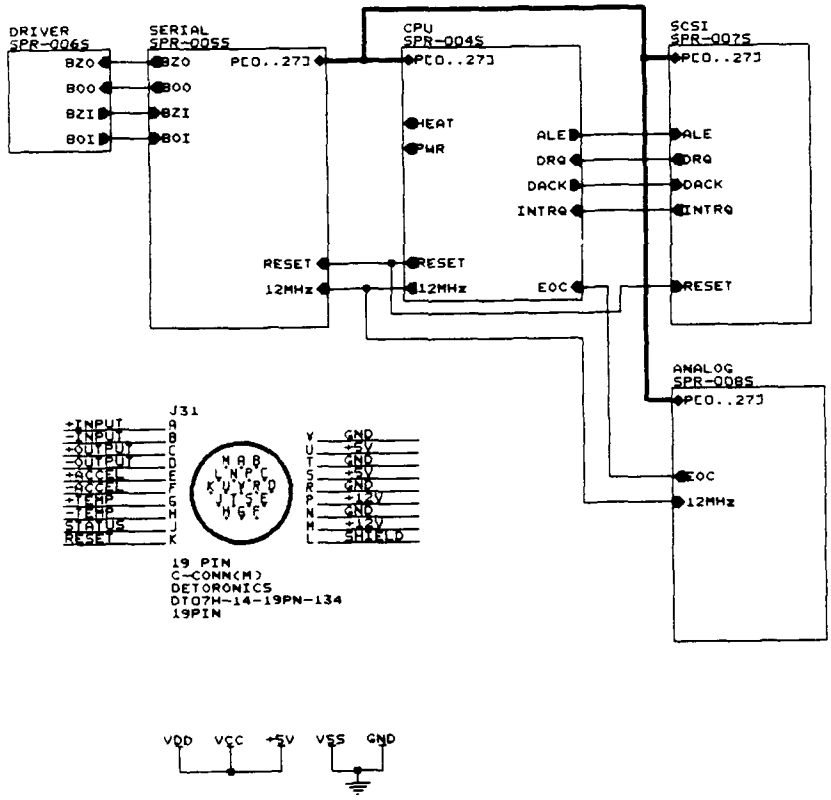


FIGURE QR8-35

AMPTEK, INC.		
Title: FDR 2		
Size: E	Document Number: SPR-0035	REV: A
Date: September 1, 1989	Sheet 26 of 42	

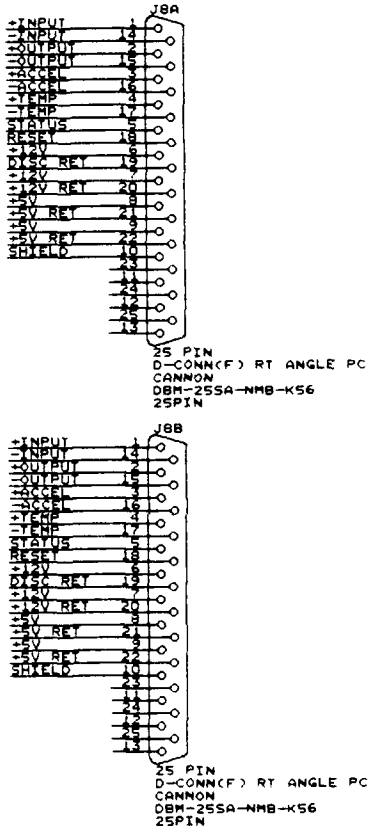


FIGURE QR8-36

AMPTEK, INC.		
Title: FDR INTERFACE		
Size: E	Document Number: SPR-0225	REV: A
Date: August 31, 1989	Sheet: 17 of 42	

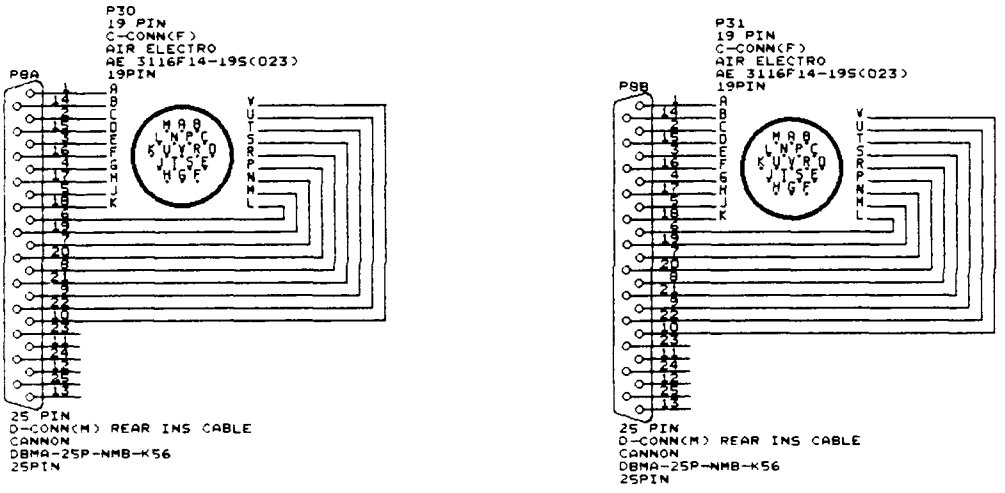


FIGURE QR8-37

AMPTEK, INC.		
Title: FOR HARNESS		
Size: E	Document Number: SPR-0125	REV: A
Date: August 31, 1989	Sheet 9 of 42	