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AN EXAMINATION OF RADIATION-INDUCED BIT-UPSET PATTERNS IN SEMICONDUCTOR MEMORIES

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T. Cousins and E.L. Karam
Nuclear Effects Section
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ABSTRACT

The interaction of photon radiation with semiconductor memories is known to corrupt data stored within by a 'bit-flip' process. Using a MOSAID MS2200 memory tester system, experiments were carried out to determine the number and location of these errors for two DRAMs and one SRAM exposed to LINAC and ^{60}Co sources. The results showed that the errors are not, in general, randomly located and are highly dependent on chip architecture. This is particularly true for the DRAMs where the bits adjacent to decoder and ground lines were observed to be the first to flip.

RÉSUMÉ

L'interaction des photons dus aux radiations sur les mémoires à semi-conducteur peut causer des erreurs en inversant certains bits. Des mesures ont été prises à l'aide d'un testeur de mémoires MOSAID MS2200 pour caractériser ce genre d'erreur pour les mémoires RAM statiques (SRAM) et dynamiques (DRAM). Un accélérateur linéaire d'électron à impulsion (LINAC) et le ^{60}CO ont été utilisés comme sources. Les résultats démontrent qu'en général les erreurs ne sont pas aléatoires mais dépendent de l'architecture de la mémoire. Il a été ainsi observé dans le cas des DRAMs que les bits adjacents au décodeur et aux lignes à la terre sont plus sensibles aux erreurs.

EXECUTIVE SUMMARY

Experiments have been carried out to determine the location and number of radiation-induced semiconductor memory errors. A MOSAID MS2200 memory tester system allowed examination of memory contents prior to, during and after LINAC and ^{60}Co gamma-ray irradiations. Two DRAMs and one SRAM were tested, with all proving extremely sensitive to the LINAC pulses. The error patterns in the DRAMs (from LINAC irradiations) were dominated by bits adjacent to decoder and ground lines, while the SRAM upset patterns appeared random. It was also observed that previously irradiated DRAMs suffer data decay at a much faster rate, and in a more non-random mode than non-irradiated chips.

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LIST OF TABLES AND FIGURES (Continued)

1. Introduction

The susceptibility of modern semiconductor memories to transient radiation effects on electronics (TREE) has been well-documented for the entire gamut of battlefield (1,2,3), outer space (4) and even ambient environments (5). Generally, these effects have been observed by analyzing the performance of the memory as a whole - which can be thought of as an integral mode analysis. The primary reason for this was, of course, the lack of the sophisticated hardware and software necessary to access bit-by-bit information on the irradiated memory. Recent developments, however, now make this possible - and a differential mode of experimental analysis can be undertaken.

In particular, Defence Research Establishment Ottawa (DREO) has recently purchased the MOSAID MS2200 system (6) which provides real-time bit maps of memories before, during and after irradiation. This report details some experimental work conducted by DREO to examine the bit-by-bit response of three particular memory types to electron linear accelerator (LINAC) and ^{60}Co gamma-ray irradiation. The question of memory response to high LET (cosmic-ray) radiation will be left for other DREO work.

2. Radiation Effects on Memory Technologies

The deleterious effects of ionizing radiation on any semiconductor memory are, stated as simply as possible, the removal or alteration (i.e. corruption) of data stored therein. However, the physical processes which cause this data removal are variant with the type of incident radiation and the type of memory technology.

2.1 Memory Technology Types

The two basic memory technology types to be considered here are the dynamic random access memory (DRAM) and the static random access memory (SRAM). Each of these MOS technologies has certain advantages which relate strongly to their differing methods of storing data, and these differing methods govern their respective radiation sensitivities.

The basic memory cell of the DRAM is a storage capacitor which may be accessed through a single gating transistor. The basic DRAM storage cell is shown in fig 1. The cell is written to by establishing the bit line level on the capacitor through the gating transistor. Reading occurs by connecting the capacitor to the bit line, again through the gating transistor, and then sensing the change induced by detecting a quasi-dc voltage shift on the bit line voltage. The major drawback with the use of DRAM memories is the loss of stored data at the cellular level - caused by both the reading of data and the loss of stored charge on the capacitor due to junction leakage currents. Thus the charge must be periodically reinforced or 'refreshed'. The present standard requirement is to refresh all memory cells every 2 ms (7).

This necessity for refresh results in the limiting of time available for data storage and retrieval and in the need for constant power being applied to the memory.

1

The basic memory cell of the SRAM is the bistable flip-flop. A typical four transistor static storage cell is shown in fig 2. In the memory array, all cells in a column share the bit lines while all cells in a row are selected by a common word line. When the potential of the word line is raised, the gates of transistors Q3 and Q4 allow the proper connection to be made to their respective bit lines, enabling the state of the storage cell to be read. The write operation is similarly carried out by turning on Q3 and Q4 and setting the logic state desired to correspond to voltages on the two bit lines. Since either transistor Q1 or Q2 is always turned on, the cell is constantly dissipating power - even when not being accessed. Thus the SRAM is characterized by higher power dissipation and a much larger cell structure than the DRAM.

2.2 Physical Processes of Radiation Interaction

From the discussion above, it should be readily apparent that data loss in a DRAM means loss of functionality of a capacitor, while for an SRAM a (set of four) transistor is the key element.

The effects of radiation on the capacitor will involve any mechanism which will exacerbate the process of charge loss from the cell element. The charge held on the bit cell capacitor is of the order of 10^{-13} Farad (7). When one considers that one Rad of (gamma-ray) irradiation can create 1.5×10^{14} electron-hole pairs per 1 cm^3 in Silicon (8) and that only 3.6 eV are necessary to produce 1.6×10^{-19} Coulomb, the susceptibility of DRAMs is not surprising. For the experiments considered here, charge may be removed either by direct ionization (^{60}Co) or by the internally generated photocurrents (LINAC).

The effects of photon irradiation on MOS transistors have been investigated comprehensively in a previous DREO report (9). The damage mechanism is creation and subsequent trapping of holes at or near the silicon/silicon dioxide interface. Thus for the case of the SRAM irradiated with ^{60}Co the principal cause of error would appear to be threshold voltage shifts arising from these trapped charges. The case of dose-rate effects (LINAC irradiation) is quite different however. Here a model called ' rail span collapse ' (10,11) has been successfully used to predict damage in CMOS SRAM memories. In this process the induced photocurrent causes a reduction in the differential supply voltage (V_{DD} - V_{SS}) across an individual RAM cell due to the matrix of RAM cells around it. The bit signature of this effect is errors beginning in one corner of the memory array (nearest V_{DD}) and progressing across the array with increasing dose rate.

The SRAM used in these experiments was of NMOS type. NMOS is known to be more radiation sensitive than PMOS or CMOS due to the trapped charge drifting toward the oxide interface as opposed to the gate metallization. The susceptibility of NMOS to rail-span collapse has never been completely documented.

Table (1) lists some documented radiation sensitivities of various memories (from 8)

TABLE 1

RADIATION SENSITIVITY THRESHOLDS OF SEMICONDUCTOR MEMORIES

(a) Total Dose	
Memory	Threshold (rad(Si))
NMOS DRAM	8E2-8E3
NMOS SRAM (1k and 4k)	8E2-8E3
CMOS/SOS RAM	1E3
PMOS SRAM	1E4-1E5
NMOS (hardened)	1E5-1E6
(b) Dose Rate	
Memory	Threshold (rad(Si)/s)
NMOS SRAM	5E6-5E7
NMOS DRAM	5E6-3E8
CMOS SRAM	5E7-8E7
CMOS/SOS	8E9-3E10

It should be pointed out that as the memory density increases, the sensitive elements, such as the oxide thickness on transistors and the size/charge held on capacitors will shrink in magnitude. Thus more densely packed memory arrays can be expected to be more sensitive to radiation.

2.3 Mosaid MS2200 Memory Tester

Fig 3 shows a block diagram of the Mosaid MS2200 memory tester system. The system is capable of testing SRAM, DRAM and ROM-family member IC's up to 4 mega-words deep by 8 bits wide. Either logical or physical bit maps may be displayed and pre-programmed patterns entered into the memory array. As radiation upsets occur, they are indicated on the screen. This pattern of bit errors may be saved for future analysis.

The Mosaid MS2200 memory tester system is made up of the following components; the main system unit, bit map display monitor, test head unit, and an AT compatible computer.

The main system unit houses the system control circuitry, power supply and electrical connections to the rest of the system's components. This unit also allows the user to program the system test procedure through the front control panel.

The test head connects to the main system unit and provides additional circuitry and connectors to interface with the Device Under Test (DUT).

3

The Bit Map Display Monitor is a vector mapped CRT, which provides the user with a real-time view of the data from the DUT.

DREO has built additional hardware and interface electronics to allow remote hook-up of the DUT to the system through a 75 foot cable. This allows the system to be placed in a shielded control room while the DUT is beiw exposed at a remote site to various radiation sources.

The entire set-up is controlled by an AT compatible type computer with built-in hardware and software to interface with the MS2200. The computer allows complete control over the main system unit, and test setup through a Windows type environment. In addition the computer allows display and mass storage of DUT data through a Fast Capture Ram (FCR) option. This allows the computer to store and display DUT data after it has been read by the main system unit, and also allows post-numerical analysis of DUT data.

3. Experimental

3.1 Memory Devices

Three NMOS memories were used for this work. They were:

a)   Advanced Micro Devices AM2167 16k x 1 SRAM (AMD)
b)   Nipon Electric Corporation NEC μ41256 256k x 1 DRAM (NEC)
c)   Texas Instruments TMS4256 256k x 1 DRAM (TI)

The abbreviations in brackets will be used to refer to these memories throughout the balance of the report. The AMD and NEC descrambling codes were acquired by DREO (from Semiconductor Insights Inc.) which allowed a topologically accurate physical display of the memory contents. As will be seen later the TI scramble did not appear too complex, and the logical map and physical map did not differ greatly.

3.2 Irradiation Facilities

The irradiation facilities used here were:

i)   The DREO on-site GB150C ^{60}Co gamma-ray source (9). This source is capable of giving militarily significant (> 1 kRad(Si)) doses in a few hours in an extremely well-calibrated environment. It is a useful simulator for both (delayed) initial radiation and fallout studies.

ii)   The Mevex Corporation LINAC (9). This machine is capable of producing 160 mA of 8 MeV electrons in a 2 microsecond wide   pulse. One major attraction is the extremely large irradiation area, allowing a great variation in dose rate using simple $1/r^2$ considerations.

iii)   The Chalk River Nuclear Laboratories PHELA LINAC (9). This 200 mA, 10 MeV machine has the advantage of variable pulse width from 100 nanoseconds to 3 microseconds. The irradiation area, however, is somewhat cramped resulting in the necessity of the use of scatterers to cut down on dose rate, which of course influences the energy spectrum. Both LINACs can simulate the prompt gamma-ray component of a weapon's burst, although neither approaches the DREO standard pulse width of 20 nanoseconds (12).

3.3 Dosimetry

Both gamma-ray and electron dosimetry were accomplished using the DREO CaF_2:Mn Thermoluminescent Dosimeter (TLD-400) portable system, using the Harshaw 2080/200A detector system (13). The system has recently been modified to allow storage of glow-curves on PC media (14).

The irradiation area at PHELA has been well-mapped in previous DREO work (15), and shot-by-shot dosimetry is generally not needed. The MEVEX irradiations required dosimetry before the experiments to verify machine reproducibility, which proved good to +/- 10%. The GB150C environment is so well-calibrated that dosimetry was only needed occasionally as a check.

4 Experimental Results

4.1 Integral Results

The integral response of the chips, i.e. total number of errors regardless of their location, does not require equipment as sophisticated as the MS2200, however there is still valuable physical information to be garnered from such numbers which come automatically with the bit maps.

Fig 4 gives the observed number of errors as a function of dose rate for the three devices for 100 ns pulses at the PHELA facility. Several features are immediately obvious. Firstly, there is an extremely sharp threshold-to-total error band for all three devices (roughly 1.9-3.2 x 10^7 Rad(Si)/s for the DRAMs and 6 x 10^6 -3 x 10^7 Rad(Si)/s for the SRAM - i.e. the 'slope' in errors-s/rad is much sharper for the DRAM). These rates are in rough agreement with other experiments as listed in table (1).Secondly, the five TI devices tested showed very similar upset patterns - i.e. great consistency from device to device. Thirdly, and surprisingly, the SRAM proved more sensitive than the two DRAMs. Finally these devices are extremely sensitive in terms of total dose - note that 1 x 10^7 Rads/s in 100 ns corresponds to only 1 Rad.

It is always a good policy to relate experimental results to real threat conditions. This is done in fig 5. The experimental results are compared to theoretical predictions from the computer code ATR (12) for the cited weapon. Note that the right hand y-axis is the total tissue kerma for the same ground ranges as the dose rates. The memories corrupt at militarily insignificant total doses, which is palpable evidence of the need for balanced hardening criteria.

When dealing with MOS circuitry, the question of whether a given effect observed for a short pulse is truly a dose rate (i.e. generated photocurrent) or a 'pulse-width dependent total dose' effect must always be considered. For the PHELA experiments this can easily be investigated by simply varying the pulse width. The results of these analyses are presented in tables 2-4. (These results represent only one device per table).

TABLE 2

DOSE-RATE SENSITIVITY OF NEC DEVICE

Pulse Width (ns)	Total Dose (Rad(Si))	Dose Rate (Rad(Si)/S)	# of bit errors
100	1.92	1.92×10^7	2466
200	3.38	1.70×10^7	256 k
100	2.82	2.82×10^7	256 k

TABLE 3

EFFECT OF SEGMENTING DOSE ON NEC DEVICE RESPONSE
(TOTAL DOSE = 2.43 RAD, 100 ns PULSES)

Time Between Two Shots	# of errors
0	104160
5 ms	13356
100 ms	10030
2 s	11525
10 s	10635

TABLE 4

DOSE FRACTIONATION EFFECTS ON NEC DEVICE
(ALL 100 ns PULSES, 2 s BETWEEN EACH MULTIPLE SHOT)

# of shots	Total Dose (Rad(Si))	# of errors	# of errors per Rad(Si)
1	2.03	4282	2109
1	3.04	131799	43355
1	4.06	256 k	6w67
2	4.06	14025	6909
3	6.09	40032	6573
4	8.12	83982	10343
5	10.15	124055	12222

The tables deal exclusively with the NEC device, however the observed trends apply to the other two.

Table 2 demonstrates conclusively that the error causing mechanism is not a purely dose rate effect, but relies upon the total dose deposited in the memory, whether or not it occurs over a 100 ns or 200 ns time frame. However, tables 3 and 4 demonstrate that the time frame over which the dose is deposited is important. From table 3 a 'critical' time between pulses for maximization of bit-flipping is seen to be less than 5 ms (the minimum time between pulses available on PHELA). This behaviour is consistent with short-term and annealing processes observed by DREO in irradiated MOSFETs (9). For the case of a DRAM an explanation is offered here of a critical charge (Q_c) being needed to cause some fixed number of errors as,

$$Q_c = K\ D_c \qquad\qquad t < t_c$$
$$Q_c = K\ D_c\ \exp\ (-t/t_c) \qquad t > t_c$$

where D_c = Critical dose necessary for error production
         t = Width of pulse
         t_c = Device time constant
and K = constant

Clearly an annealing process is taking place which allows the charges generated near the storage capacitor to recombine or drift away, without affecting the stored charge. The process may be one of recombination (which will occur in picoseconds) or drift (which occurs over a much more protracted time scale). A complete analysis requires more time and possibly temperature-dependent work, and will be pursued in the future.

Table 4 shows that as the total dose is increased, a weakening of the device radiation resistance occurs, allowing more errors per Rad for the four and five shot cases. This may be indicative of incomplete annealing or, more likely, partial charge removal during the first three shots.

4.2 MS2200 FCR Display

Fig 6 (a) shows a FCR Display of an non-irradiated memory which has been programmed with a checkerboard pattern of 'ones' (darker squares) and 'zeroes' (lighter squares). Each whole square here is an 8-bit by 8-bit segment of the memory. Fig 6(b) shows the same (DRAM), following a 3 minute period of data decay due to refresh being turned off. Note that the errors here are denoted by darker or lighter bits at the error locations. Note also that the decay appears random in nature. The same conventions for FCR displays will be used throughout the report, although in some cases the chip was programmed with either all 'ones' or all 'zeroes'.

4.3 Linac Irradiations

4.3.1 DRAM Results

The extremely sharp rise from threshold to saturation in the total number of errors for the DRAMs would perhaps be suggestive of the same mechanism being responsible for all error creation - and thus a random distribution.
Figs 7 and 8 for the two DRAMs show that this is definitely not the case. The TI FCR represents a logic map since the descrambling code for this memory was not available. The NEC FCR is a physical map (i.e. real space) using the acquired descrambling code. The similarity in error patterns suggests not only similar technologies but also the fact that the TI scramble is very limited and the physical and logic maps must be almost identical. Both FCRs here were chosen to

examine the error patterns for roughly 15,000 errors - with the exact numbers shown on the FCR displays.

An explanation for the error patterns is immediately obvious upon examination of the physical layout of the NEC device structure, as shown in Fig 9. Note that for the FCR plots the eight discrete memory segments have been artificially joined, i.e. the decoder lines do not appear. Clearly the bits nearest the x- and y-decoders, the ground lines and the periphery circuitry such as sense amplifiers are the most sensitive. This implies that these lines offer the path of least resistance for generated currents, and that these currents only travel a short distance away from the word or bit lines, subsequently changing the charge state on the capacitors to produce errors. As one increases the total dose more errors are seen to occur in areas more 'remote' from the metallic decoder circuitry as shown in fig 10.

In order to examine the progression of error patterns through the DRAM structure, it was decided to collimate the beam so as to only irradiate a specific area of the memory. Toward this end, a 1/16 inch diameter hole was drilled into a 1/2 inch thick slab of lead and the resulting upset patterns observed for irradiations of the (i) an area centrally located in one of the eight memory segments and (ii) the area at the central intersection of the x- and y-decoders.

Figs 11 through 17 show the progression of the upset patterns as the dose is increased for case (i) above. In fig 11 the first bits to corrupt are along the x-decoder and ground lines, even though the beam is centred between these two, as figs 12 and 13 clearly indicate. In the last two figures it is believed that direct deposition of charge accounts for the central errors, while the photocurrents cause the 'border' errors. Note that in figs 14 and 15 the growth of the central error pattern is constrained by the decoder and ground lines, while the 'border' pattern progresses around the entire chip. Finally in Figs 16 and 17, the central pattern can breakthrough into other octants, but the 'border' pattern is still the most significant contribution.

Figs 18 through 22 show a similar irradiation sequence for case (ii). For the first two figures, the decoder-line errors again prove most sensitive, with little evidence of the actuw shape of the collimator. Only at higher doses does a direct error pattern become evident, but again is over-shadowed by the decoder line propagation.

4.3.2 SRAM Results

Fig 23 gives the physical layout of the AMD device used in this work. Fig 24 gives the error pattern following a 10^7 Rad(Si)/s, 100 ns wide pulse at the PHELA facility. The non-random nature of the bit-flip pattern is attributed here to an incorrect de-scrambling code. However it is believed that the scramble is accurate enough to show that the process of 'rail span collapse' is not evident, as this would manifest itself in a preponderance of errors at the physical top of the chip (furthest from V_{SS}). Clearly the direct total dose sensitivity of the NMOS device is greater than the dose-rate sensitivity observed in CMOS structures.

Figs 25 through 28 show the effects of the collimated irradiation of the AMD device. The beam is centred slightly above and to the right of the chip centre. Note that the area of affected bits is roughly the same as the beam size, and spreads slightly with increasing dose (keep in mind here the incorrect

descrambling code). There is no evidence for propagation of errors along the decoder line. In figs 26 and 27 an interesting blockage of the error spread at the horizontal chip centre line occurs, which may indicate some form of structure not reported in the layout.

The response to collimated beams of these devices has implications for radiography which will be explored in future DREO work.

4.4 Steady-State Irradiations

4.4.1 Error Upset Patterns

The responses of the NEC and AMD devices to ^{60}Co irradiation was examined at the DREO GB150C source. Here, both devices were irradiated in a field of known intensity of 100 kRad(Si)/h (27 Rad(Si)/s) and the upset patterns observed. Table (5) lists the integral results here.

TABLE 5

STEADY-STATE IRRADIATION RESULTS

Device	Dose (kRad(Si))	# of errors	errors/Rad(Si)
AMD	7.3	3808	0.52
AMD	10.9	0032	0.73
AMD	14.5	8467	0.58
NEC	14.5	230	0.016
NEC	18.2	6833	0.37
NEC	21.8	32737	1.50
NEC	25.4	101555	3.99
NEC	27.2	120018	4.41
NEC	29.1	151166	5.19
NEC	30.8	200292	6.50
NEC	32.7	235598	7.20

The most glaring difference between steady-state and pulsed irradiation is the huge difference in absolute sensitivity (errors per unit dose) which is readily apparent from a comparison of tables 4 and 5.

In comparing the relative DRAM and SRAM responses it is apparent that the SRAM error rate is relatively uniform with increasing dose, while the DRAM exhibits a marked increase in this parameter as dose increases. This increase may be due to some synergistic effects within the DRAM or creation of a relatively weaker path for charge decay from the DRAM capacitors, as dose increases. The SRAM corruption is of course due to trapping of (radiation-induced) holes at the gate-oxide interface and would appear to be an independent effect for each transistor, presumably governed by such well-known factors as oxide thickness, local applied voltage, etc(9).

Fig 29 shows the bit upset pattern for the AMD SRAM for the 7.3 kRad irradiation. Note here that errors occur preferentially from the right hand side of the chip and progress toward the left. As there is no obvious physical difference in the two sides of the chip (from fig. 23) the reason may well lie in the manufacturing process - perhaps a thicker gate oxide on the right-hand-side of the device.

Figs 30 through 33 show the observed error patterns as a function of increasing dose for the NEC DRAM. Note that the broad pattern originates in the lower left and spreads in both directions, however there are definite patterns associated with the decay, specifically along rows. This would be consistent with the creation of a charge path, allowing an increased rate in error formation as dose increases. It is interesting to note that the upset patterns here differ dramatically from those caused at the LINAC, which may be expected as the effective pulse width is much larger here.

4.4.2 Radiation Imprinting

The response of the NEC DRAM to turning off refresh was examined for devices which had been exposed to ^{60}Co irradiation. Figs 34 and and 35 show the FCR results here. Firstly an examination of the total errors as a function of time shows that the rate of error formation greatly exceeds that of the non-irradiated device (see fig 6(b)), which is direct evidence for permanent damage. Of greater interest is the upset patterns themselves, which mimic very closely the upset patterns arising from LINAC irradiations. Clearly weakened pathways for charge transport have been created, and the bits closest to the decoder and ground lines may decay more readily. This 'imprinting' provides a unique way of ascertaining the amount of radiation damage an irradiated memory has sustained.

4.5 Sensitivity of Logic States

Both the AMD and NEC devices were examined to ascertain any differences in the relative sensitivities to electron pulses for '0' and '1' logical levels. To do this each device was alternately programmed with all '0' followed by all '1' entries at the MEVEX facility and a careful measure of the dose was made with TLDs. Table 6 summarizes the results here.

TABLE 6

RELATIVE SENSITIVITIES OF '0' AND '1' LEVELS
(ALL EXPOSURES TO 2 MICROSEC LINAC PULSE)

(a) AMD irradiations				
Device	'0' level dose (Rad(Si))	errors/Rad	'1' level dose (Rad(Si))	errors/Rad
1	.672	54	.70	3890
2	.811	7077	1.26	6605
3	.803	4753	.872	8864
4	.798	0	.764	1192
5	.623	80	.623	3530
6	.621	4400	.662	8372
7	.600	117	.600	2135
(b) NEC irradiations				
Device	'0' level dose (Rad(Si))	errors/Rad	'1' level dose (Rad(Si))	errors/Rad
1	1.60	39834	1.60	25382
2	3.6	25571	3.6	25541

The results here are inconclusive as to whether the '0' or '1' logic states are more radiation sensitive. The SRAM results show great variation, but the '0' level may be slightly harder. Means of the two results give (2354 +/- 2979) errors/Rad for the '0' level, and (4941 +/- 3026) errors/Rad for the '1' level. The major problem here is that, as already discussed, the effects are both dose rate and total dose dependent. Thus a very high degree of reproducibility in shot-to-shot is required for meaningful tests. This degree of reproducibility is not acheivable at Mevex with the current set up.

The DRAM results show no conclusive sensitivity differences.

5.0 Conclusions

The experimental results presented here show that the loss of stored data in semiconductor memories following radiation exposure is an extremely complex function of not only the radiation time frame, but also the device topography. The MOSAID MS2200 has shown to be very capable in analyzing data-upset patterns in both the integral and discrete modes. The observed upsets lead immediately to suggestions for improving radiation hardness by varying manufacturing processes which may include, for example, modification of decoder lines.

Although this work has dealt exclusively with photon irradiation, the extension to other (higher LET) particles such as neutrons and heavy ions is a natural step. Only a full examination of all possible radiation sources will guarantee total radiation hardness of semiconductor memories.
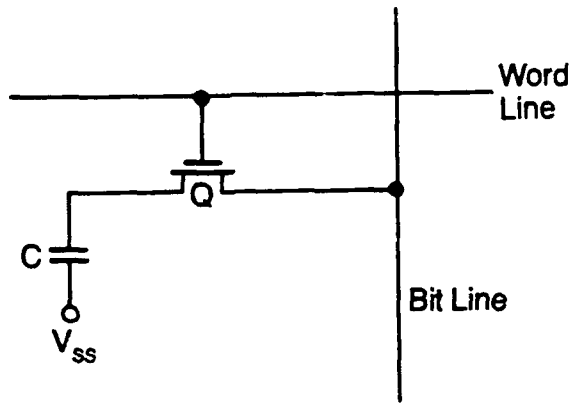
Figure 1: Basic DRAM storage cell, consisting of storage capacitor and gating transistor.
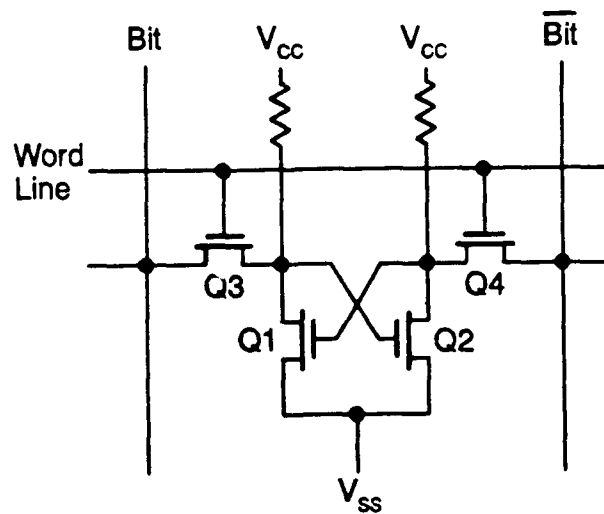
Figure 2: Basic SRAM storage cell, consisting of four transistor bistable flip-flop.
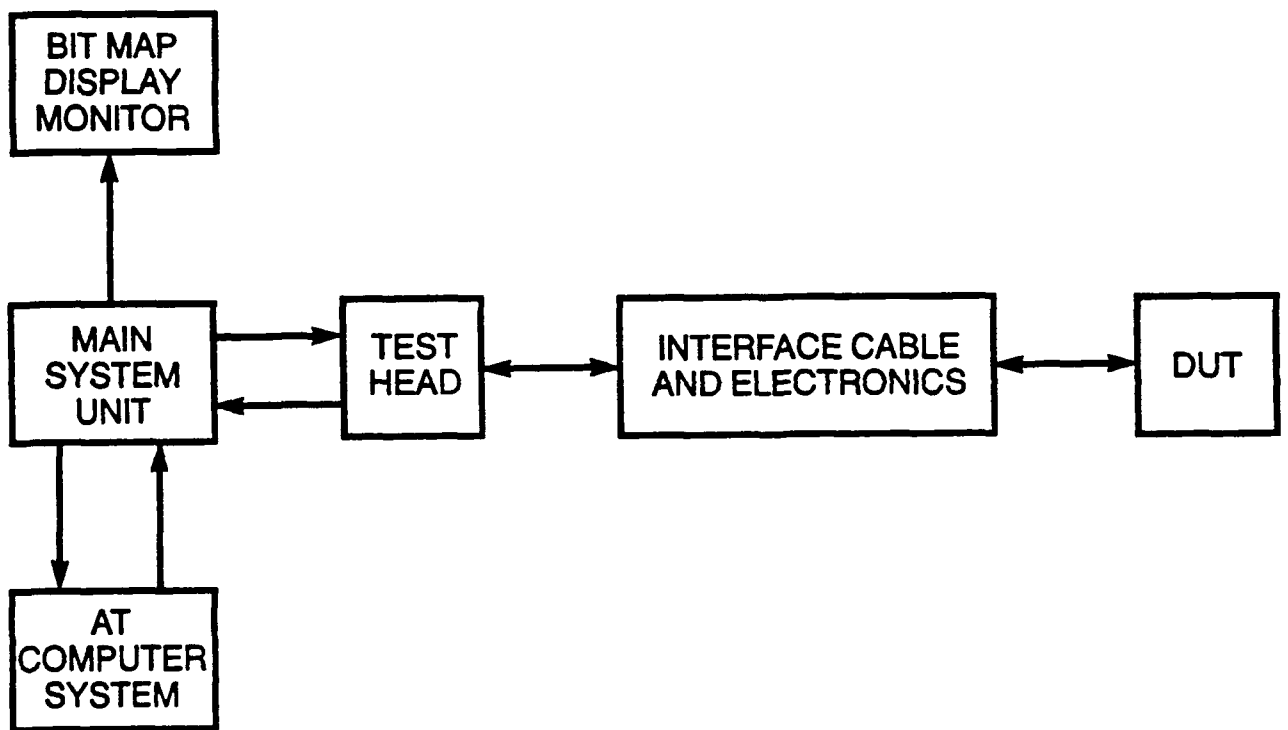
Figure 3: Block diagram of MOSAID MS2200 memory tester system.

INTEGRAL MEMORY RESPONSES
all for 100 ns pulse width

Figure 4: Measured errors for the three memory types examined in this work as a function of dose rate at the PHELA facility. All electron pulses were 100 ns wide here. (Five different TI devices were used, but only one each of NEC and AMD).

DREO RESULTS (EXPT VS PREDICTED THREAT)
10 kT BURST AT 129 m
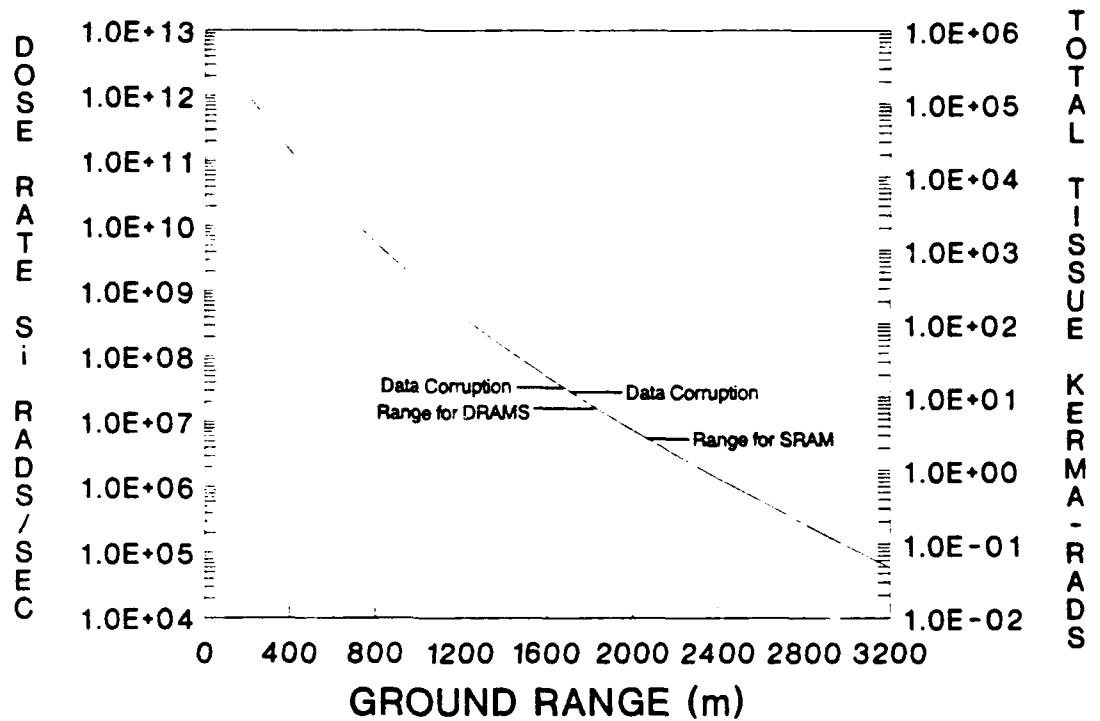
Figure 5:   Relation of dose rate results (Figure 4) to theoretical weapon
scenario.

0   80   100   XAdd

0

80

100

180

YAdd

Error Count   0

Figure 6 (a):   FCR display of non-irradiated (NEC) memory programmed
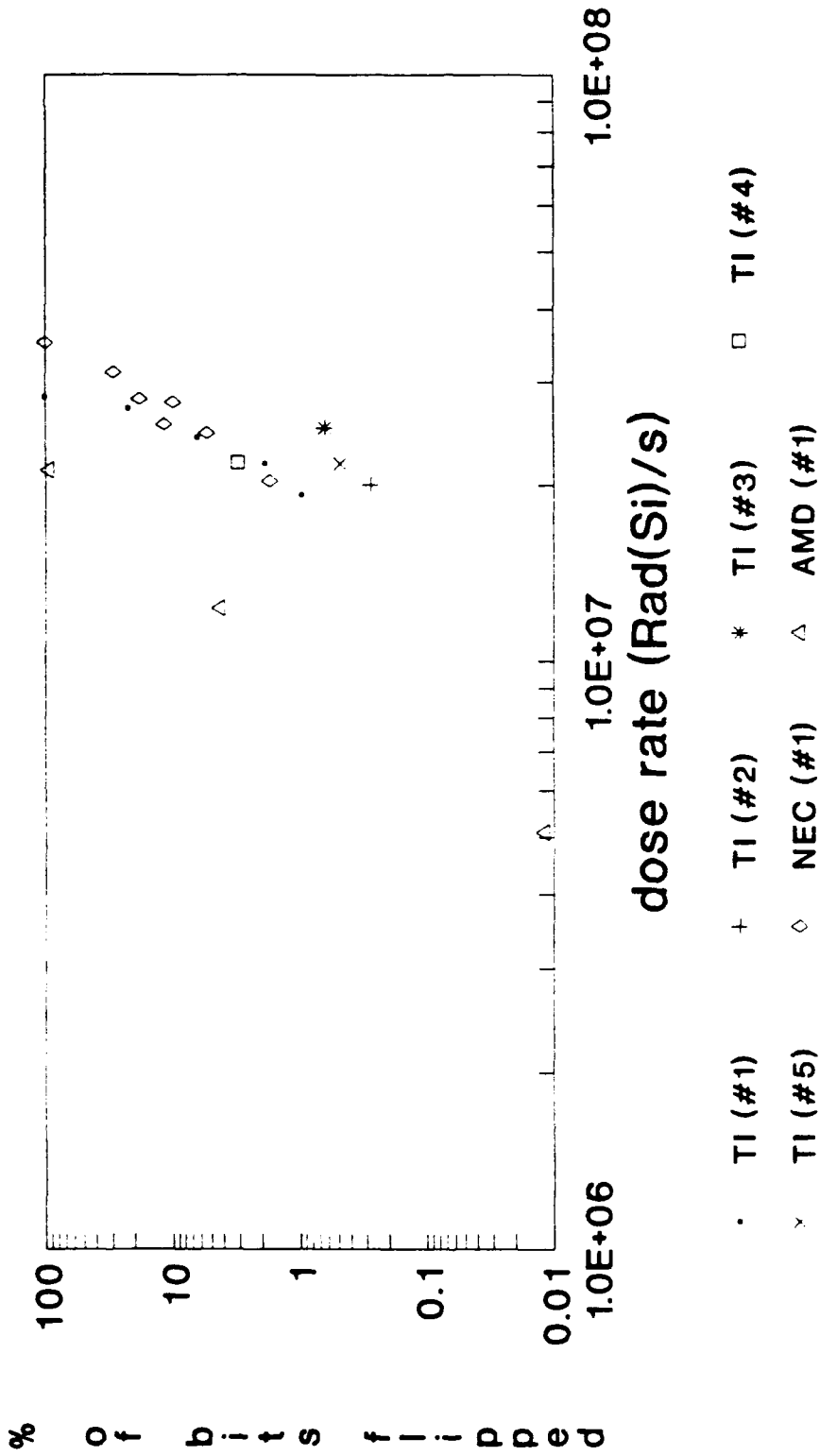with a checkerboard pattern of 'ones' (darker squares)
and 'zeros' (lighter squares).

0   80   100   XAdd

0

80

100

180

YAdd

Error Count   1561
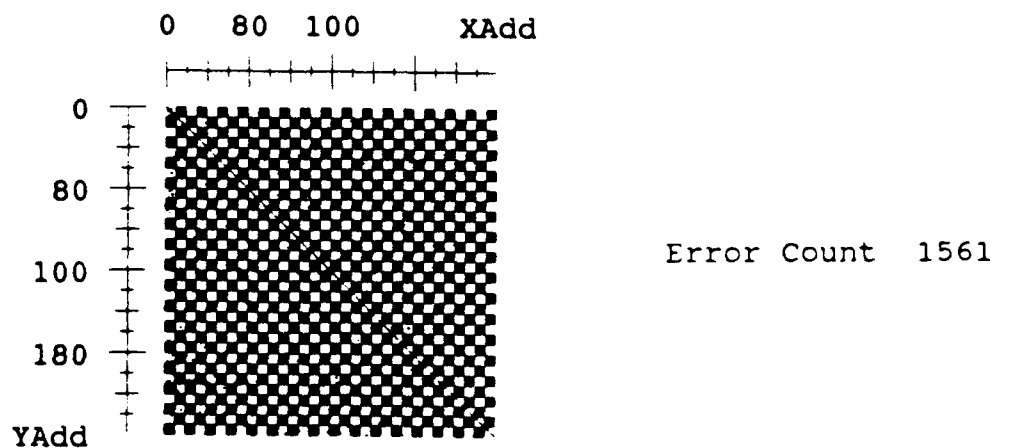
Figures 6 (b):   Same FCR (NEC) display as in Figure 6(a), following a
time interval without refresh. Note the random nature of
errors, denoted by individual darker elements in the
lighter ('ones') squares.

16

Error Count   16286

Figure 7:   FCR display of the TI DRAM following LINAC irradiation
             (Dose Rate — 2.4×10^7 Rad(Si)/s).

Error Count   13775
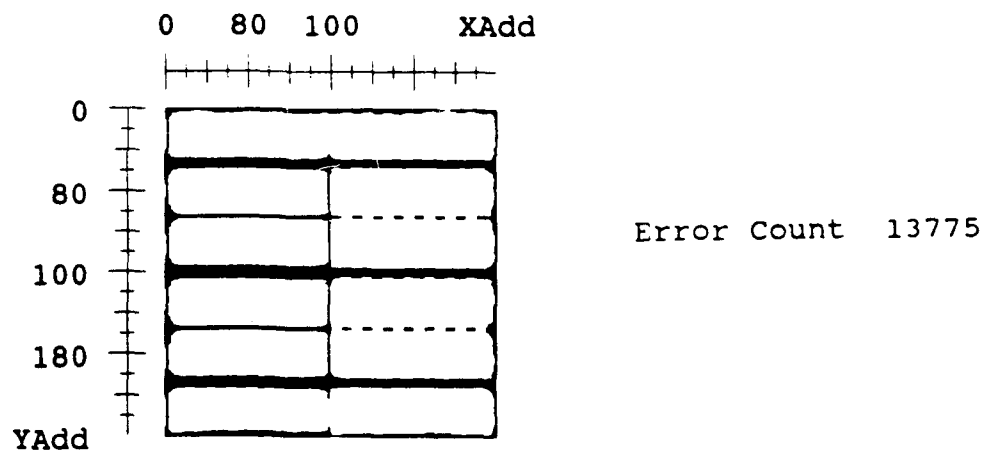
Figure 8:   FCR display of the NEC DRAM following LINAC irradiations
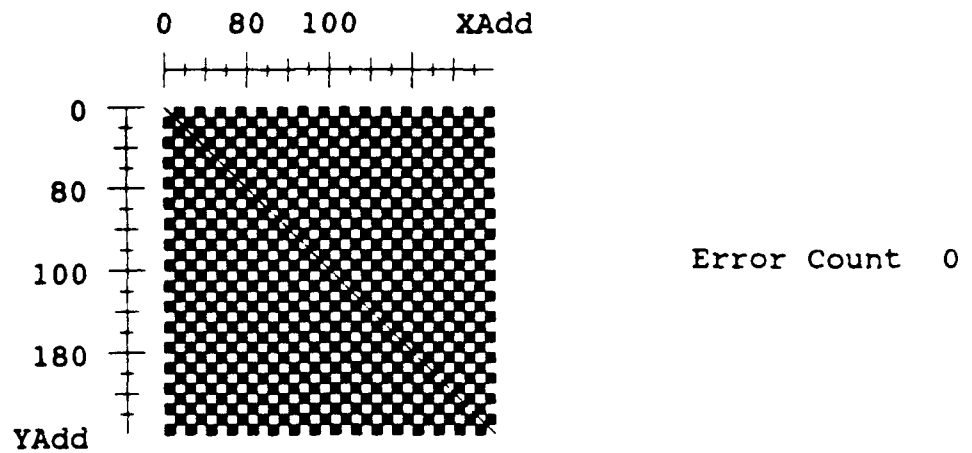   (Dose Rate — 2.45×10^7 Rad(Si)/s). The display here
             represents a physical map, using the supplied
             descrambling code.   The similarity with the TI
             device is clearly evident.
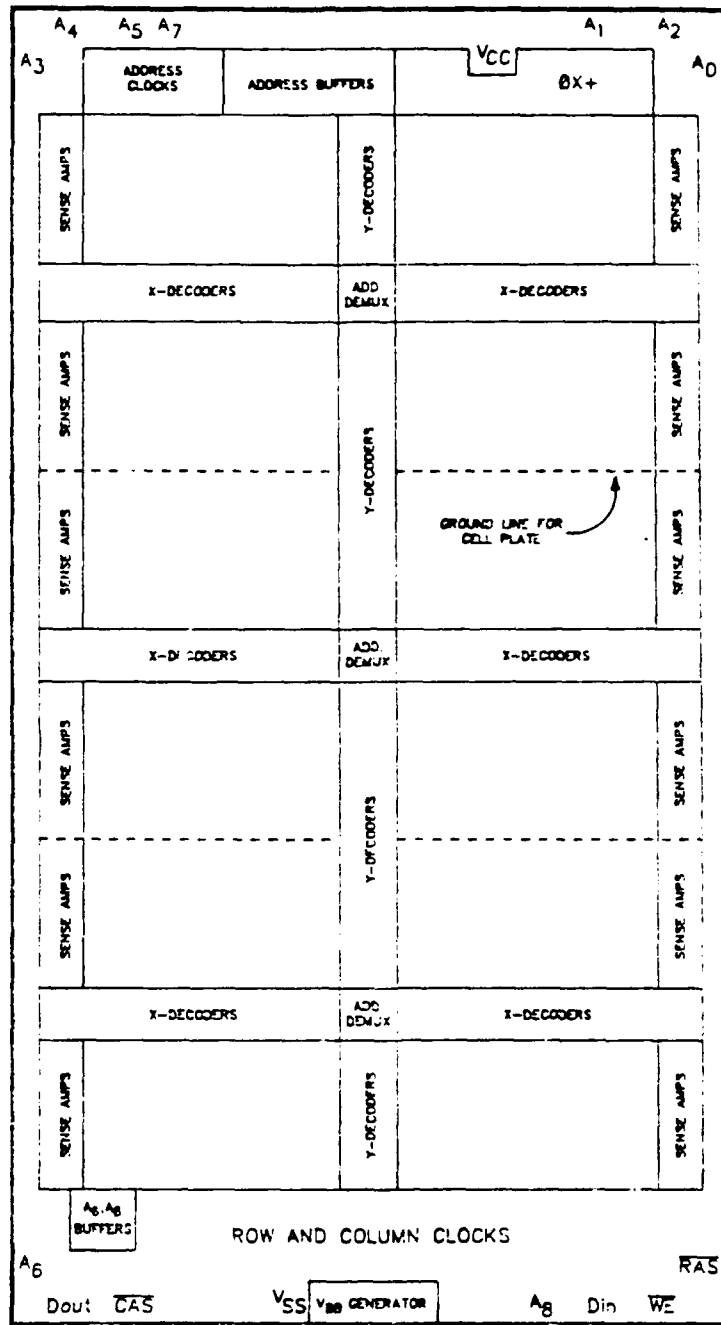
Figure 9:   Physical layout of NEC device structure.

0   80   100   XAdd

Error Count   75004

YAdd

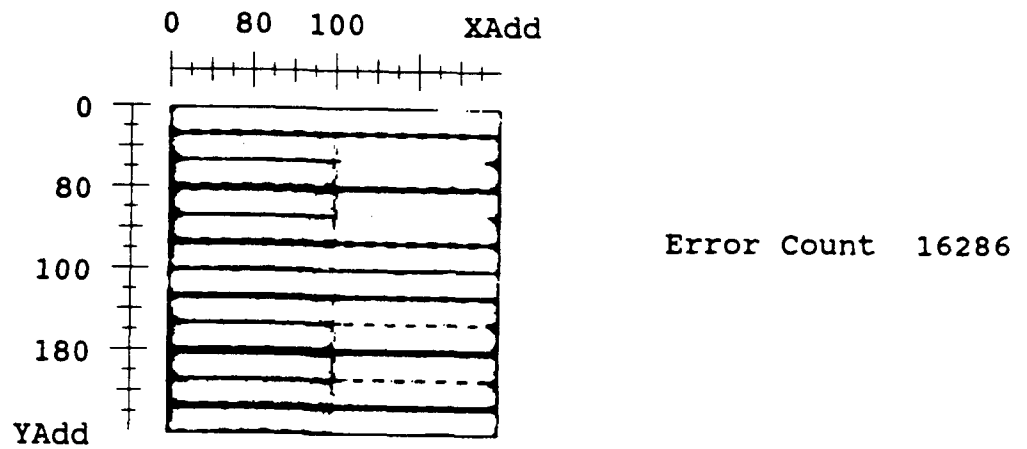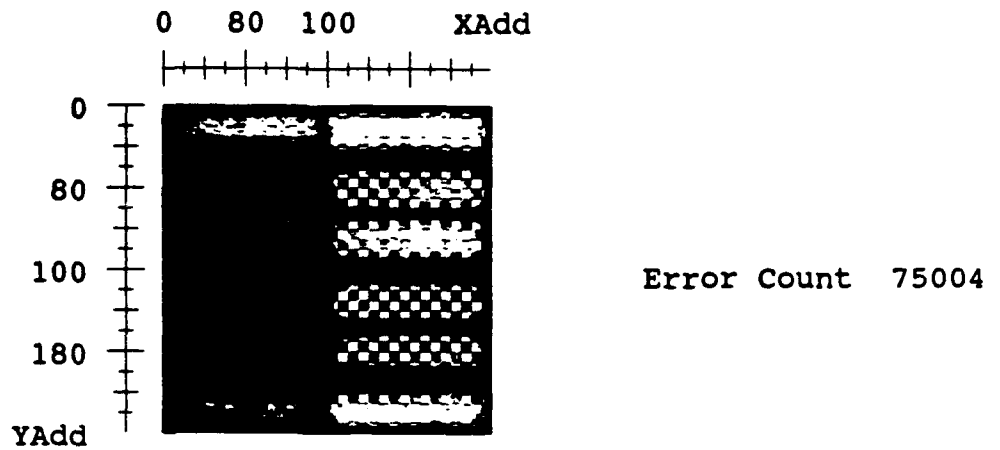Figure 10:   FCR display of the NEC DRAM following higher dose
rate (3.1×10^7 Rad(Si)/s)) than in Figure 8. Note that
areas 'remote' from word and bit lines show errors.

0   80   100   XAdd

Error Count   54

YAdd
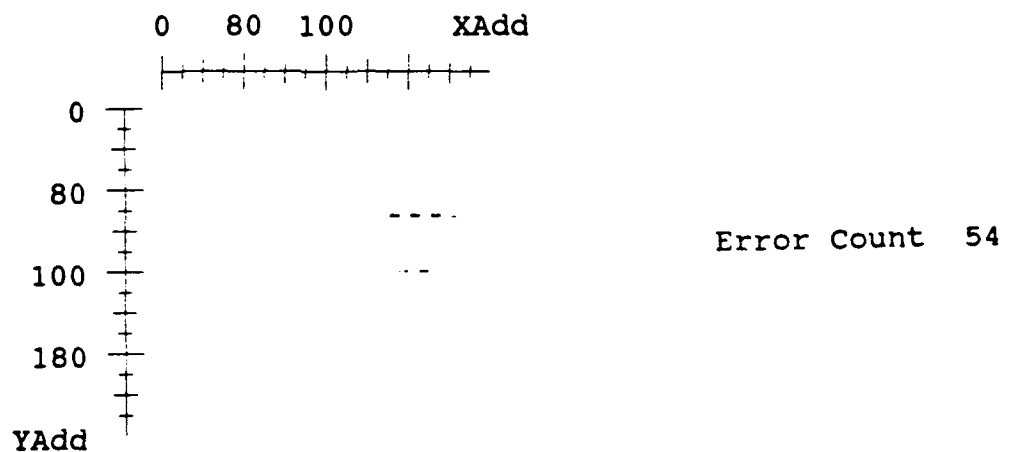
Figure 11:   FCR display of the NEC DRAM following LINAC irradiation centred
in the memory segment above and to the right hand side of the
chip centre. Note that the errors still occur first along
decoder and ground lines (beam current ≈ 20 mA, pulse
width ≈ 300 ns).

0   80   100   XAdd

Error Count   517
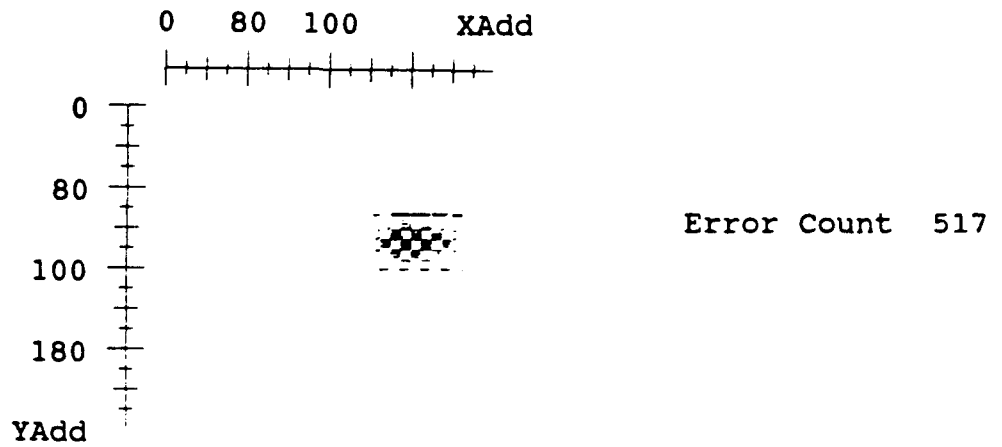
Figure 12:   FCR display of the NEC DRAM following slightly higher dose
             (beam current = 20 mA, pulse width = 350 ns). Note that
             error formation at centre of collimated beam is beginning.

0   80   100   XAdd

Error Count   9047
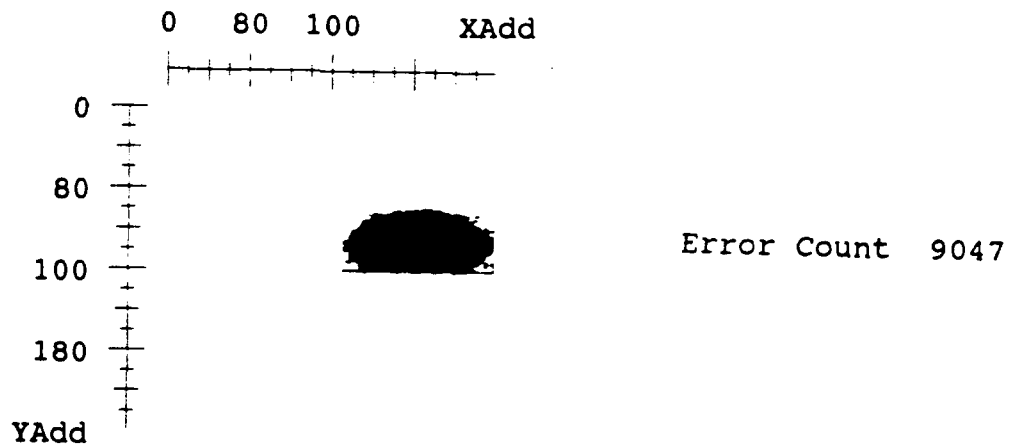
Figure 13:   FCR display of the NEC DRAM following still higher dose
             (beam current = 20 mA, pulse width = 500 ns). Note the
             increased area of 'direct hit' errors.

Error Count   13998

Figure 14:   FCR display of the NEC DRAM following still higher dose (beam
current − 20 mA, pulse width − 700 ns). Note that errors are
now propagating along different ground and decoder lines.

Error Count   27739

Figure 15:   FCR display of the NEC DRAM following still higher dose (beam
current − 20 mA, pulse width − 1.5 μs). 'Central' errors are
constrained by the ground and decoder lines, while errors
along the lines themselves continue to propagate.

21

0   80   100   XAdd

0

80   Error Count   49210

100

180

YAdd

Figure 16: FCR display of the NEC DRAM following still higher dose (beam
            current ─ 200 mA, pulse width ─ 500 ns). The central errors
            have now 'broken out', while the border errors continue to
            grow.

0   80   100   XAdd

0

80   Error Count   68950

100

180

YAdd
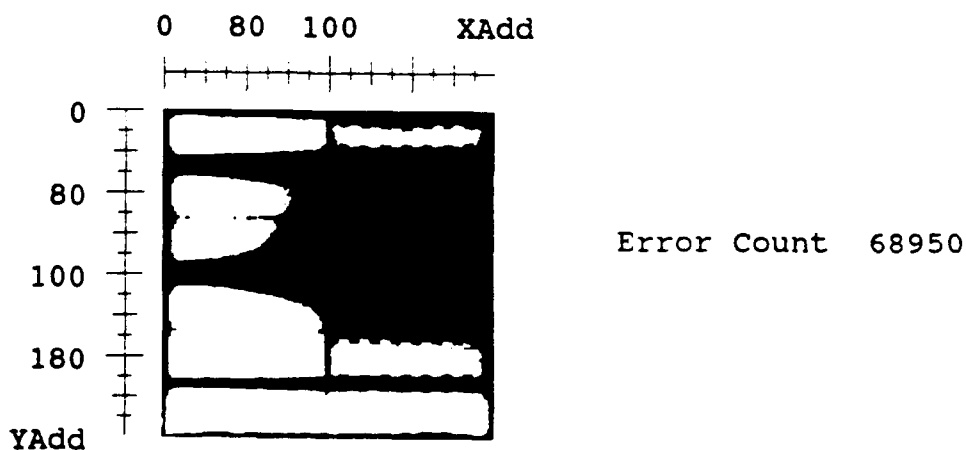
Figure 17: FCR display of NEC DRAM following highest dose used here (beam
            current ─ 200 mA, pulse width ─ 2 μs). The trends above   '
            continue.

```
         0   80  100        XAdd
         |++++|++++|++++|++++

    0  ┬
       ┼
   80  ┼
       ┼
  100  ┼            ⌐          Error Count   15
       ┼
  180  ┼
       ┼
 YAdd  ┴
```
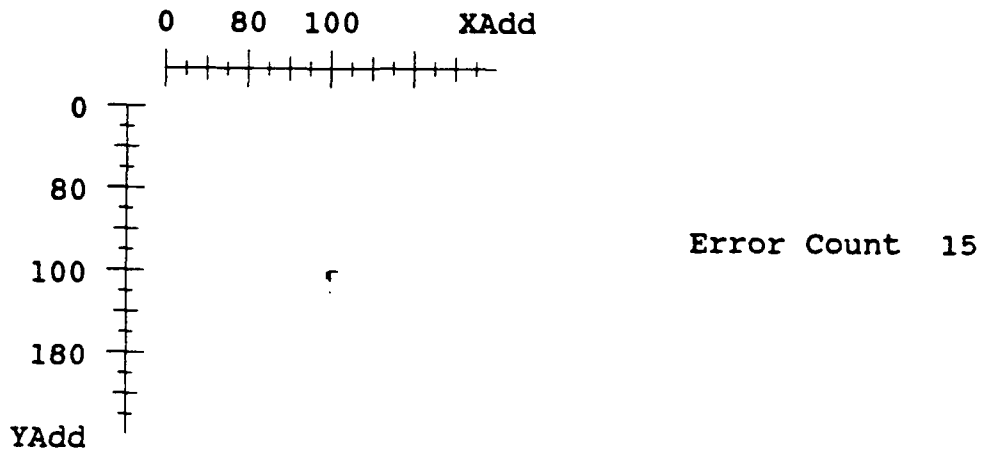
Figure 18:   FCR display of NEC DRAM following collimated beam LINAC
              irradiation at chip centre (beam current — 20mA, pulse
              width — 200 ns).   Note the errors move outward along the
              decoder lines from chip centre.

```
         0   80  100        XAdd
         |++++|++++|++++|++++

    0  ┬
       ┼
   80  ┼
       ┼
  100  ┼         - - ┬ -       Error Count   116
       ┼            |
  180  ┼
       ┼
 YAdd  ┴
```
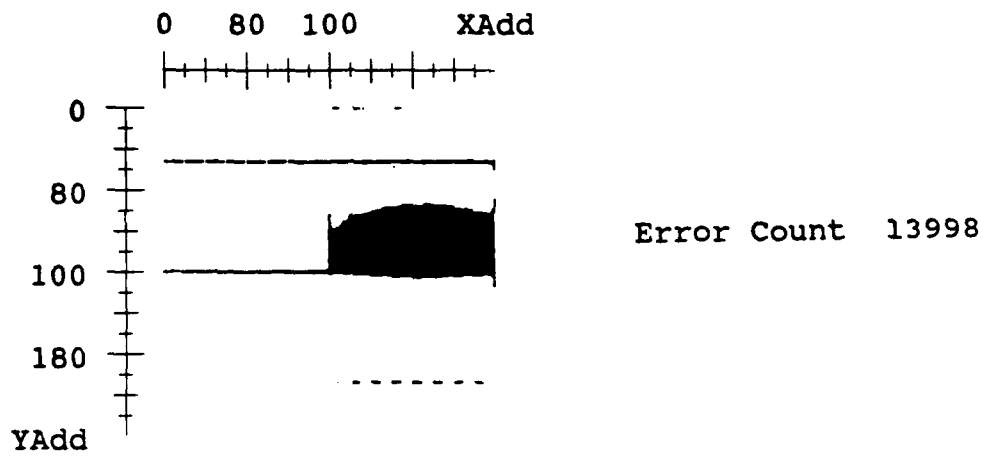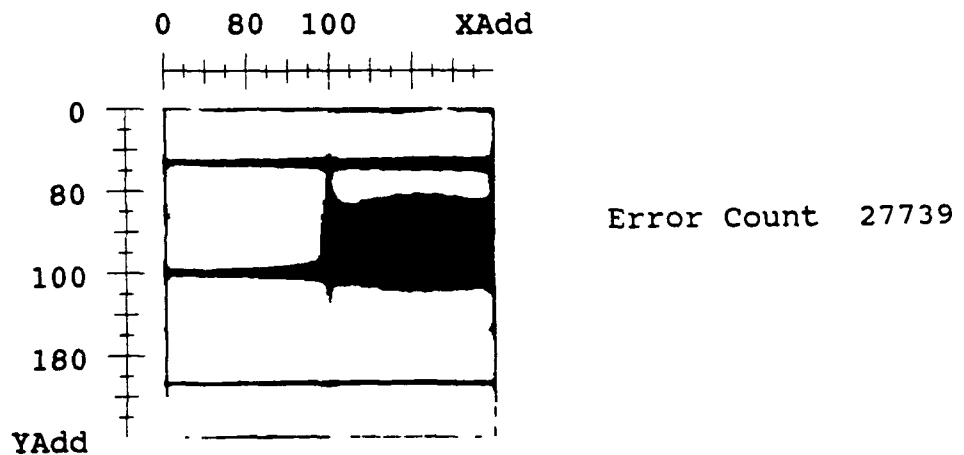
Figure 19:   FCR display of NEC DRAM following still higher dose (beam
              current — 20mA, pulse width — 300ns). No 'central' errors are
              seen yet, as propagation along lines dominates.

23

```
 0   80  100      XAdd
|++++|++++|++++|+++|

  0 ┬
    ┼
 80 ┼
    ┼
100 ┼         ─ ┳ ─ ─
    ┼          ┃
180 ┼
    ┼
YAdd ┴
```
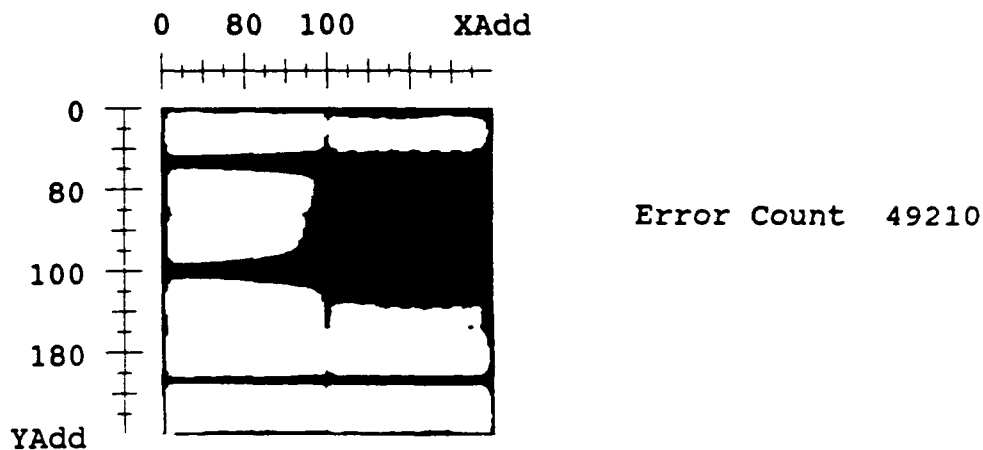
Error Count   195
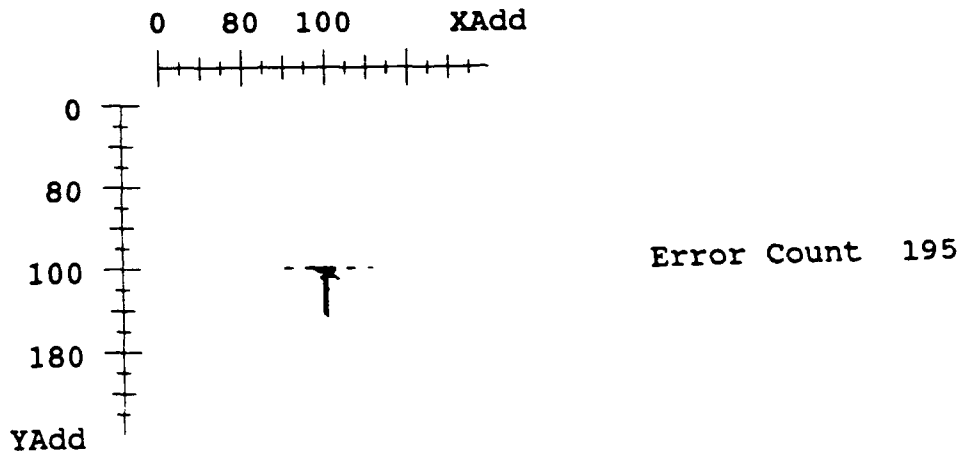
Figure 20:   FCR display of NEC DRAM following still higher dose (beam
              current = 20 mA, pulse width = 350 ns). The central errors are
              finally beginning to show.

```
 0   80  100    XAdd
|++++|++++|++++|+++|

  0 ┬
    ┼
 80 ┼
    ┼
100 ┼      ● ▰▰▰ ─
    ┼          ▮
180 ┼
    ┼
YAdd ┴
```

Error Count   1721
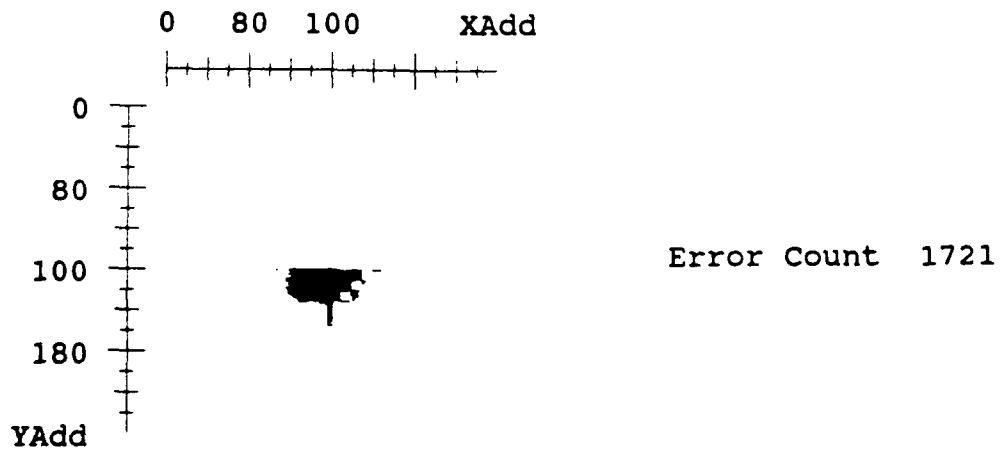
Figure 21:   FCR display of NEC DRAM following still higher dose (beam
              current = 20 mA, pulse width = 400 ns). Now the central
              (direct hit) errors dominate.
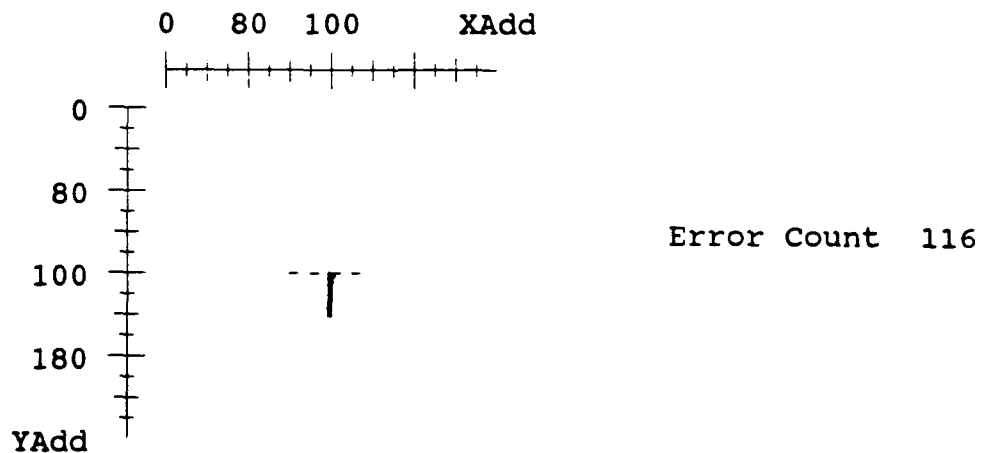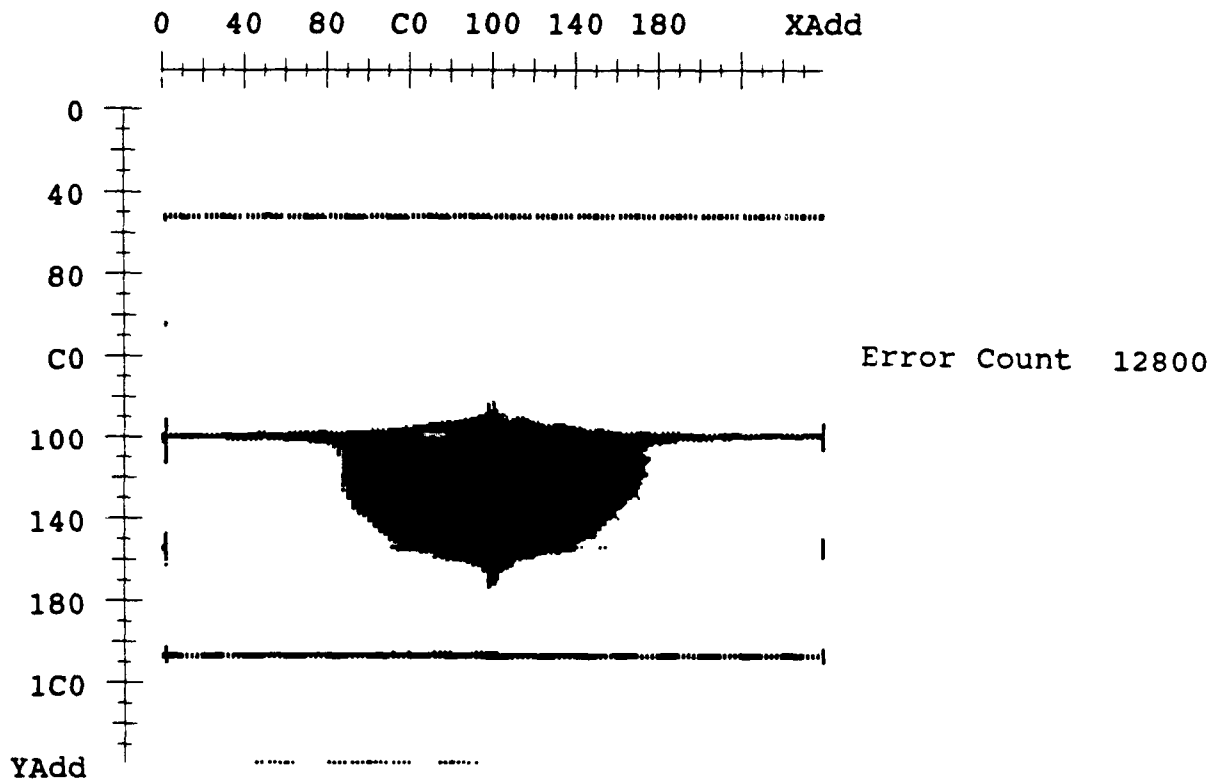
Figure 22:   FCR display of NEC DRAM following still higher dose (beam
              current = 20 mA, pulse width = 800ns). Note that the error
              propogation along the lines is now clearly visible, along with
              the central direct hit area.
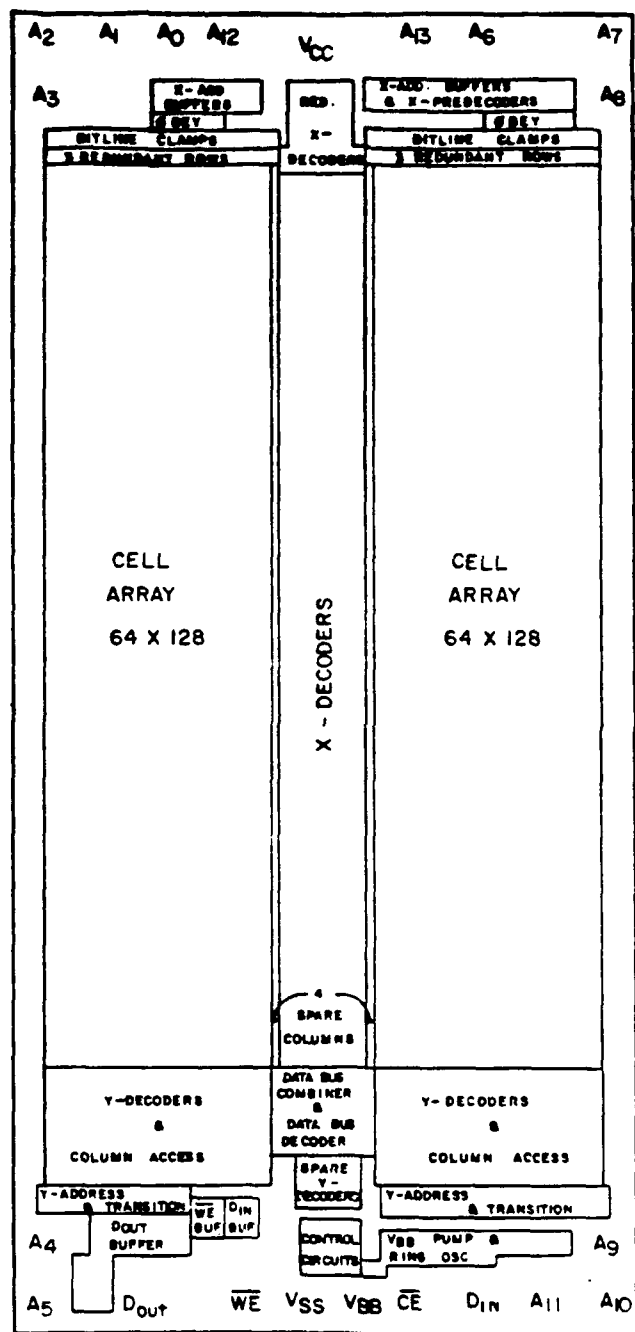
Figure 23: Physical layout of the AMD SRAM used in this work.

26

0   20   40   XAdd

Error Count   7772

YAdd
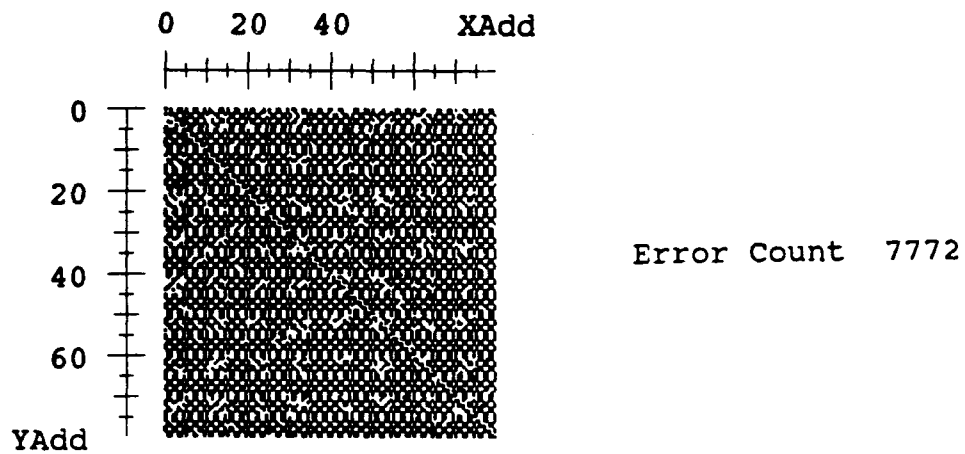
Figure 24:   FCR display of AMD SRAM following 5.7 x 10^6 Rad(Si)/s LINAC
irradiation with 1000 ns pulse.   Note the random nature of
error formation.

0   20   40   XAdd

Error Count   471

YAdd
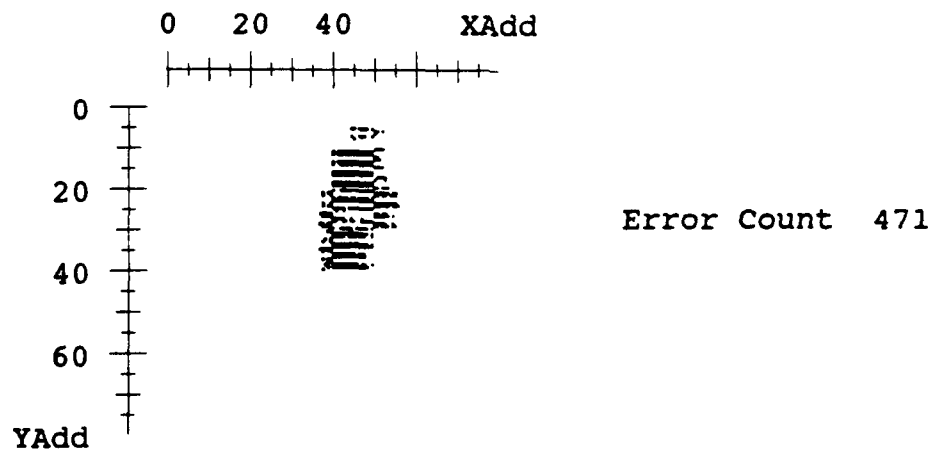
Figure 25:   FCR display of AMD SRAM following irradiation with 1/16"
collimated LINAC beam (beam current - 20 mA, pulse
width - 250 ns).   The error pattern mimics the circular
collimator when the aspect ratio is taken into account.

```
     0    20   40      XAdd
     |+++|+++|+++|+++|+++|+

  0 ┬
    ┼
 20 ┼                       Error Count   853
    ┼
 40 ┼
    ┼
 60 ┼
    ┼
YAdd ┴
```
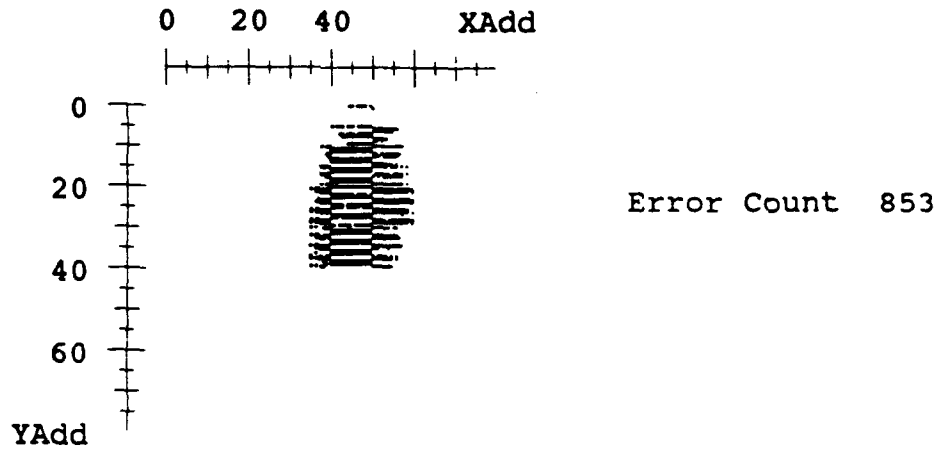
Figure 26:   FCR display of AMD SRAM following still higher
              dose (beam current - 20 mA, pulse width - 350 ns).
              Note that the beam is truncated in the vertical
              direction at the chip centre.


```
     0    20   40      XAdd
     |+++|+++|+++|+++|+++|+

  0 ┬
    ┼
 20 ┼                       Error Count   1053
    ┼
 40 ┼
    ┼
 60 ┼
    ┼
YAdd ┴
```
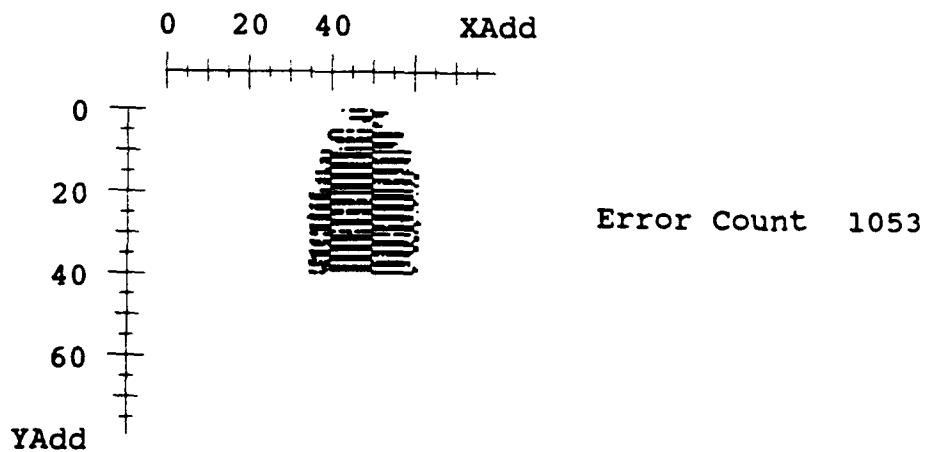
Figure 27:   FCR display of AMD SRAM follwing still higher dose
              (beam current - 20 mA, pulse width - 450 ns). The
              truncation is more apparent

28

Error Count   1357
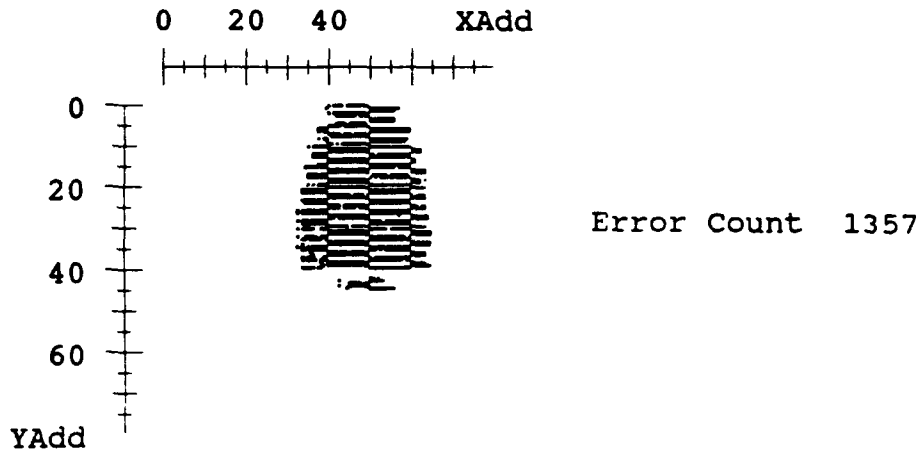
Figure 28:   FCR display of AMD SRAM following highest dose used here (beam current — 20 mA, pulse width — 700 ns). Note that the pattern is now extended to the lower half of the chip.

Error Count   3808
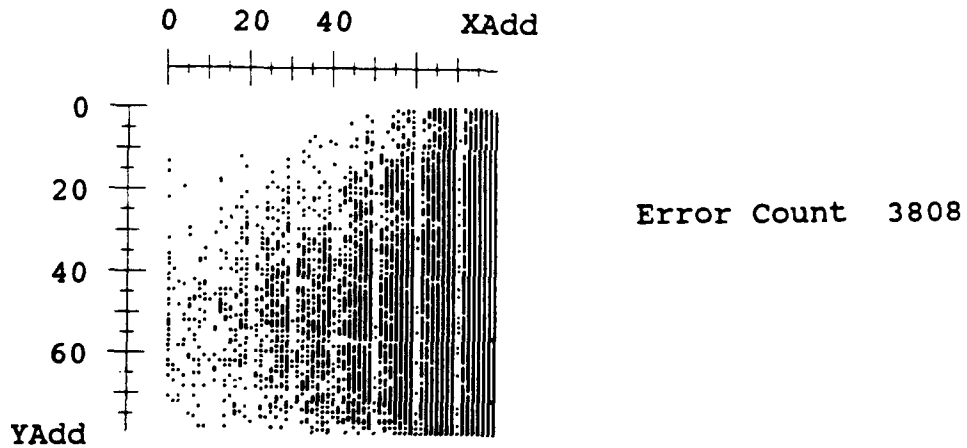
Figure 29:   FCR display of AMD SRAM following 7.3 kR exposure at the DREO GB150C ^{60}Co facility. Note the error pattern is biased toward the right hand side of the chip.

```
 0    80   100      XAdd

 0

80

100                        Error Count   230

180      — ··  ·

YAdd
```
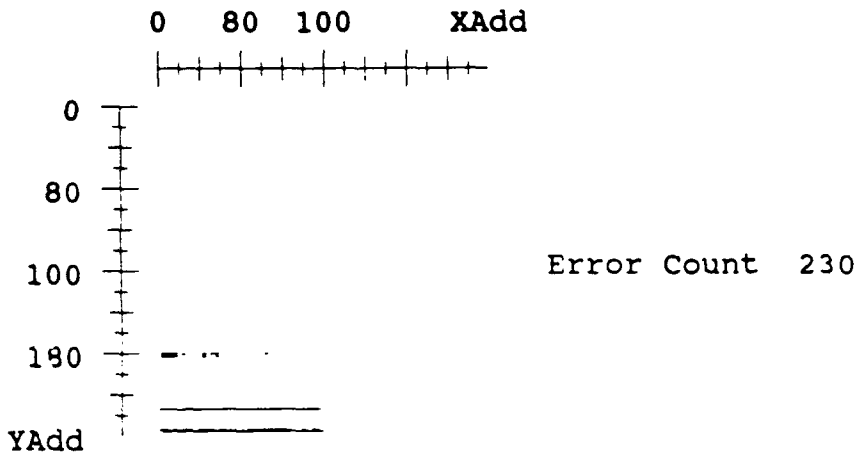
Figure 30:   FCR display for NEC DRAM following 14.5 kR exposure at the
             DREO GB150C ^{60}Co facility. Note the lower left proves most
             susceptible.

```
 0    80   100      XAdd

 0

80                         Error Count   32737

100

180

YAdd
```
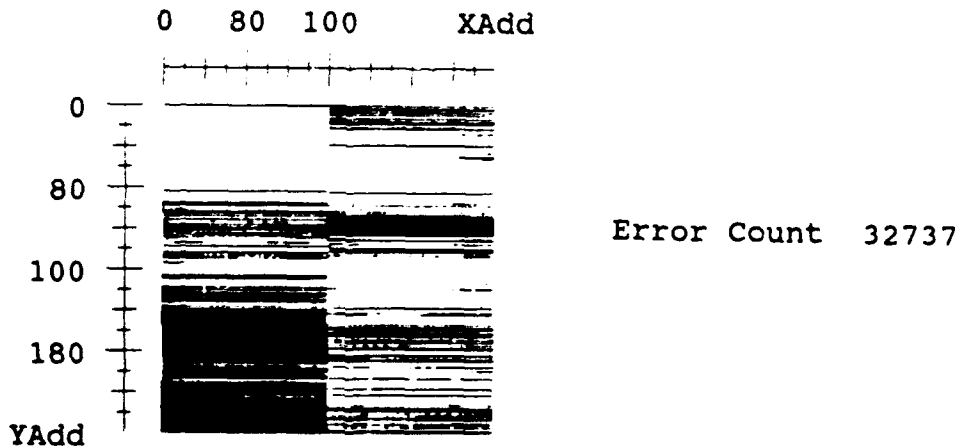
Figure 31:   FCR display for NEC DRAM following 21.8 kR irradiation at
             the DREO GB150C ^{60}Co facility. Note that the pattern
             propogates up and to the right, but along rows.

0   80   100   XAdd

Error Count   120018

YAdd
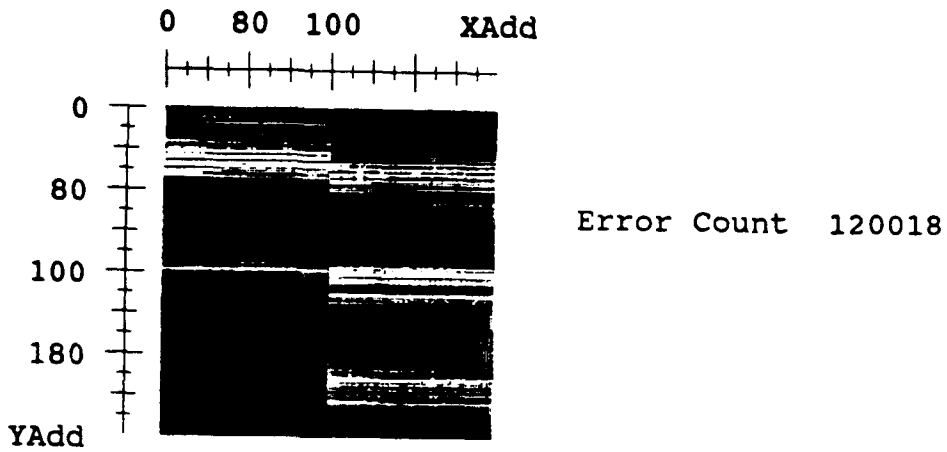
Figure 32:   FCR display for the NEC DRAM following 27.2 kR exposure at the DREO GB150C ⁶⁰Co facility. The propogation of errors continues.

0   80   100   XAdd

Error Count   200292

YAdd
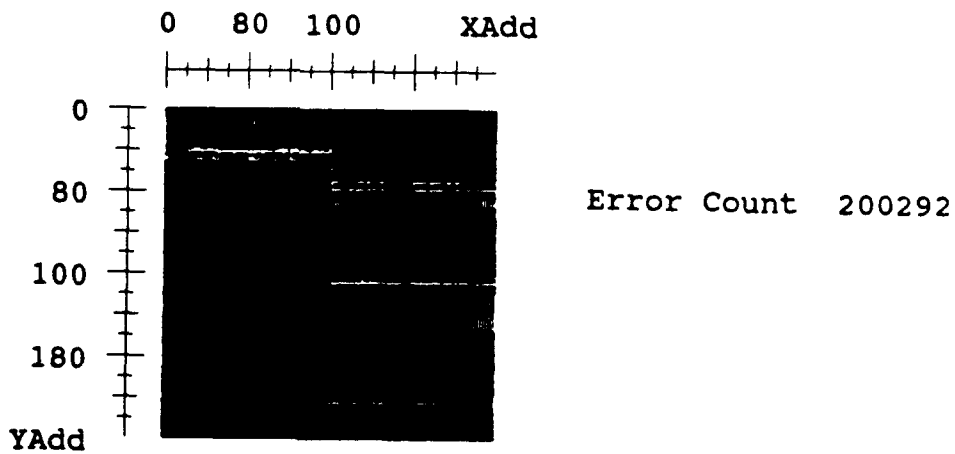
Figures 33:   FCR display for the NEC DRAM following 30.8 kR exposure at the DREO GB150C ⁶⁰Co facility. The propogation of errors continues.

```
    0   80  100      XAdd
   |++|++|++|++|++|
  0 ╤
    ╎
 80 ┼
    ╎
    ╎                              Error Count    4010
100 ┼
    ╎
180 ┼
    ╎
YAdd ┴
```
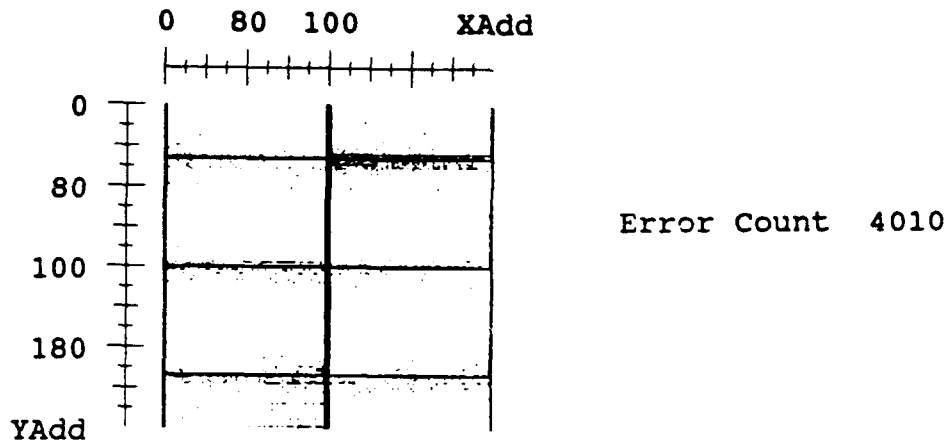
Figure 34:   FCR display of previously exposed NEC DRAM with
              refresh turned off for 2s. Note that decays occur
              much faster than for the non-irradiated device and
              along ground and decoder lines. (Compare with
              Figure 6(b)).

```
    0   80  100      XAdd
   |++|++|++|++|++|
  0 ╤
    ╎
 80 ┼
    ╎
    ╎                              Error Count    33216
100 ┼
    ╎
180 ┼
    ╎
YAdd ┴
```

Figure 35:   FCR display of previously exposed NEC DRAM with
              refresh turned off for 3s. Again note non-random
              decay patterns.

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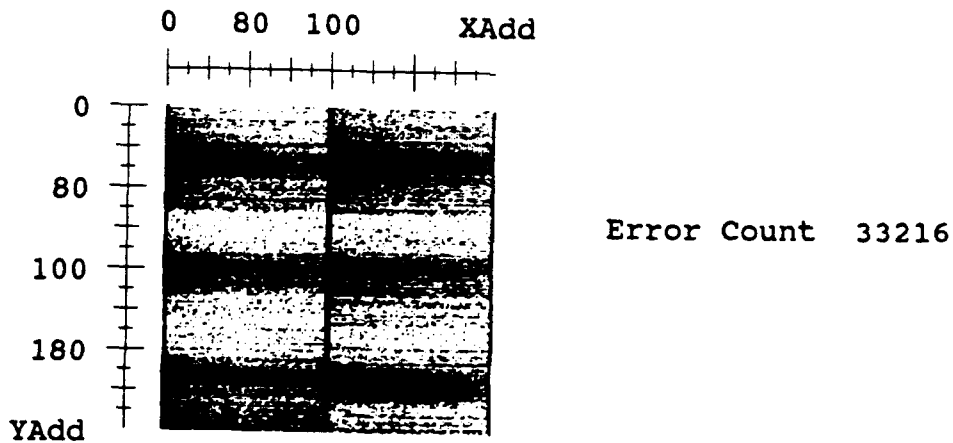3.   Massengill L.W., S.E. Diehl-Nagle and T.F.Wrobel, "Analysis of
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The interaction of photon radiation with semiconductor memories is well known to cause errors in the memory contents by a 'bit-flip' process. Using a MOSAID MS2200 memory tester system, experiments were carried out to determine the number and location of these errors for two DRAMs and one SRAM exposed to LINAC and ^{60}Co sources. The results showed that the errors are not, in general, randomly located and are highly dependent on chip architecture. This is particularly true for the DRAMs where the bits adjacent to decoder and ground lines were observed to be the first to flip.

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SRAM
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Dose
Dose Rate
Gamma Ray
Electron Linac