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GALLIUM ARSENIDE PILOT LINE FOR HIGH PERFORMANCE COMPONENTS

Contract No. F29601-87-C-0202

Semiannual Technical Report for April, 1989 through September, 1989

January 16, 1990

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GALLIUM ARSENIDE PILOT LINE FOR HIGH PERFORMANCE COMPONENTS

Semiannual Technical Report
October, 1989

1. INTRODUCTION (S. F. Nygren)

The Gallium Arsenide Pilot Line for High Performance Components (Pilot Line III) is to develop a facility for the fabrication of GaAs logic and memory chips. The first thirty months of this contract are now complete, and this report covers the period from March 27 through September 24, 1989. During this period, all of the aspects of this program began to come together. Our "User Friendly" CAD system, HCAD, is almost complete. Extensive diagnostics on the fully functional, PT-2M 256-bit SRAM have pointed the way toward the design of the 4K SRAM, for which masks will be purchased in October, 1989. We are beginning to get test results from the second and third logic circuit demonstration vehicles, wafer fab for the fourth will start in October, and the remaining two designs are well underway. And processing variations are being reduced so that increasingly consistent circuits are being fabricated. Unfortunately, there have been time consuming problems with our MBE machines in the last six months, so we have not been able to process as many wafers as we planned.

The first release of HCAD has been delivered to AT&T. HCAD is built within the Design Framework provided by Cadence and is thereby consistent with the mainstream of modern CAD tools. It supports full-custom, standard cell, and cell array (gate array) styles of design. Each style has tested by independent users: custom design by designers at Hughes Microelectronics Center, standard cell by using HCAD to design the Transversal Filter Chip (a contract deliverable), and cell array by using HCAD to design the cell array version of the Casino Test Chip (another contract deliverable).

The PT-2M 256-bit SRAM was intended as a stepping stone toward full understanding of our SARGIC HFET technology. It has served this purpose extremely well. First, in these six months alone, we have fabricated 929 PT-2M SRAMs where all 256 bits work at 50 MHz at 40°C. These devices have served as deliverables to DARPA and have allowed us to extensively characterize the properties of our devices and the adequacy of our device and circuit models. And they have served as a proving ground for substantial yield enhancement through laser programming. Based on our experience with PT-2M, we have designed the first iteration of our 4K SRAM as 1K by 4, using 64 rows and 16 columns in each section. We will use the radiation hardened memory cell developed in PT-2M. We have enlarged the memory cell to comply with the latest design rules, and we have redesigned the output drivers and some other sections.

In logic circuits, we have wrapped up our work on the standard cell Casino Test Chip and the PT-2 Logic Tester Chips. As described in the last Semiannual Technical Report, we never found a standard cell Casino Test Chip where all the subcircuits functioned simultaneously, and we don't expect to. Work on it has been terminated since there is no customer for this chip.

Similar to the PT-2M SRAM function for memories, the six logic circuits of PT-2L and PT-2M have served their functions as stepping stones toward the custom, standard cell, and cell array logic circuits. All but one of these circuits was "right first time;" the remaining circuit had a layout error due to a bug in the design rule checker that has since been fixed. The working devices all function over the full temperature range from -55° to 125°C. They all comfortably meet the 200 MHz requirement. They do not solidly conform to the required input and output voltage levels, particularly Vih. But we know that these circuits were designed with the older design models and that they came from an era where the DFET thresholds were often not on target. Both problems will be corrected for future circuits.

We are beginning to get test data from two new logic circuits, a 1K Cell Array (the first iteration of the required 5K-gate cell array), and the full-size, full-custom ALU (one of the two required full-custom circuits). Both designs are "right first time." The early data from the ALU shows that it easily meets the speed requirement, but there may be problems with the input voltage levels. We shall be studying this carefully as more data becomes available.

The remaining required logic circuits are in various stages of design. We have completed the third standard cell design, the Transversal Filter Chip. Wafer fabrication will begin in October, 1989. While there has been a two month schedule slip, design is well under way for the second full custom circuit, a 32-bit Floating Point Multiplier. And design has started for the 5K-gate cell array version of the Casino Test Chip. The latter two circuits should enter wafer fabrication before the end of 1989.

We have now delivered six sets of circuits to DARPA. The most recent two lots contained PT-2M memories in TriQuint MLC-44 packages; PT-2L ALUs, Dual 8-bit Multipliers, and Quad 4-bit Adders in Interamics 64/88 packages; and full-size, full-custom ALUs in TriQuint MLC-196 packages.

During this six month period in the processing area, 319 MBE wafers were delivered to the wafer fabrication line, 291 wafers started into wafer fabrication, and 238 wafers were completed and PCM tested. For the GaAs Pilot Line program and other AT&T GaAs programs, the total wafer fabrication starts averaged 20 per week. This is lower than the previous reporting period because of prolonged periods of unexpected MBE machine downtime. Statistical quality control procedures are a built-in feature of our Pilot Line. There are presently 72 control charts, of which 52 have statistical control limits, and 44 are fully under shop control. Most charts not yet under shop control are from either MBE or wafer probe. In a typical week, at least 90% of the data points are within statistical process control limits. In addition, we are now implementing two new indices (Cp and Cpk) to show how well actual processes conform to the specification limits.

Three improvements in wafer fabrication processes have led to major reductions in wafer-to-wafer variations of FET characteristics. First are daily calibrations of MBE layer thickness and doping, and tighter specifications on doping. Second is tighter control over the furnace annealing process. Last is better control over the composition of the tungsten silicide gate metal alloy. The resulting tighter distributions of FET threshold voltages made it clear, for the first time, that the average thresholds were more positive than the target values. Accordingly, we made an adjustment in the MBE layer thicknesses. To improve processing yields, we have concentrated effort on solving processing problems like WSi rings, spots, scratches, and missing top metal.

We have developed a simple screening procedure for selecting processed wafers suitable for further testing. We use data from the Process Control Modules and select wafers based on the resistance of a via chain tester and on the DFET and EFET Ids currents. The procedure works

well for PT-2L wafers, and we are extending it to other circuits.

We are beginning to get test data from preliminary versions of advanced technology circuits. To accelerate the schedule, these use gold-based metallization rather than the aluminum that will finally be used. Initial results show that the revised logic family is faster that the standard SFFL logic family, as planned. Meanwhile, the aluminum metallization process for the advanced technology is near completion. Process development has overcome initial problems like corrosion, sections missing from patterned lines, and aluminum stringers. WSi is used as a barrier to separate aluminum from the gold-based ohmic contacts and prevent purple plague. In reliability studies, we have aged via chain structures 1000 hours at 200°C in air. There are 250,000 vias in the chain, connecting the gold-based ohmic contact metal with the aluminum bottom metal. WSi is used as a barrier between gold and aluminum. Resistance decreases exponentially at first, then linearly. After 2000 hours, the resistance is about 80% of the original value.

Transient ionizing dose measurements were made on the PT-2M SRAMs. The standard memory cells had an upset threshold of $5x10^9$ rad(GaAs)/sec, where the radiation hardened cells reached $1x10^{10}$ rad(GaAs)/sec. For both transient ionizing dose and SEU measurements, we find increased sensitivity in the accessed rows.

2. HCAD: A USER FRIENDLY CAD SYSTEM (L. Fisher, M. Nguyen, C. Tong)

The fifth half year of the Pilot Line III program saw substantial advances made in the development of HCAD, the CAD System for DARPA's Pilot Line III, including the delivery of the first version of the software to AT&T.

The delivery to AT&T included:

1. Tape 1 - This cartridge tape contains integration software and a sample execution run of HCAD on a small circuit. This tape is in Unix "tar" format and is for installation on a Cadence workstation.
2. Tape 2 - This cartridge tape contains the AT&T HCAD GaAs macrocell library. This tape is in Unix "tar" format and is for installation on a Cadence workstation.
3. Tape 3 - This cartridge tape contains the AT&T HCAD GaAs gate array library. This tape is in Unix "tar" format and is for installation on a Cadence workstation.
4. Tape 4 - This reel (1600 BPI) contains the HITS integration software. This tape is in "COPY" format and is for installation on the Vax/VMS as part of HCAD.
5. The HCAD Users Manual
6. The HCAD - AT&T Macrocell Library Reference Manual (Volume I, II, III)
7. The HCAD Primitive Library Reference Manual
8. The HCAD Macrocell Library Development Guide
9. The HCAD Software Development Notebook - This notebook contains the functional and design specifications to the integration software developed over the course of the project.

This first version fully supports both full custom and macrocell styles of layout. In addition, the 1K gate array library is included, although it is not intended to be used in production. The 5K gate array library is currently in development.

The standard cell capabilities of HCAD have been well exercised by the designers of the Transversal Filter Chip. Enhancements have been made to the system based on their results. The full custom capabilities of HCAD have been exercised by the HCAD developers (setting up the standard cell library) and independently by designers at the Hughes Microelectronics Center. The Gate Array tools and their integration have been exercised during the process of hosting the 1K cell array and now the 5K cell array.

The AT&T HCAD macrocell library has been extensively checked, including design rule checks, device level extraction and layout-to-logic verification, logic simulation, fault simulation, and timing simulation.

The Hughes TEST (HTEST) tools have been integrated into HCAD. These tools support the design of chips that include testability enhancing features such as set scan registers. Elements in the macrocell library have been designed to support scan design methodology.

A set of model parameters have been developed in support of HSPICE, the circuit-level simulator in HCAD. Six sets of parameters are provided: two temperatures (25°C and 125°C) and three process conditions (nominal, fast, and slow). In addition, the HSPICE interface has been extended to provide a "macro model" capability, allowing the inclusion of a gate resistance term in the model.

The technology files in HCAD have been updated as necessary to track new developments and changes in the Pilot Line III technology and to provide additional functionality.

HCAD is built within the Design Framework provided by Cadence. This Framework has allowed a full-featured design system to be provided in support of DARPA's AT&T Pilot Line III. Table 1 highlights some of the key features of HCAD and indicates which tools are used.

Table 1 — Summary of HCAD Capabilities and Tools

Function	Tool
CAD Framework	Cadence Design Framework
Schematic Editor	Cadence Schematic Editor
Logic Simulation	SILOS
Fault Simulation	SILOS
Test Vector Generation	HITS
Behavior/Functional Simulation	Zycad/Endot N.2
Gate Array Place and Route	Mentor GateStation
Std. Cell Place and Route	Cadence StandardEdge
Full-Custom Layout	Cadence Graphics Editor
Static Timing Analysis	Cadence TA
Post Layout Simulation	SILOS, TA, HSPICE
Circuit Simulation	HSPICE
Layout Verification	Cadence PDCheck, PDExtract, PDCompare
Design-For-Test	Hughes HTEST

CAD technology, just like process technology, does not stand still. Thus there is room for improvement of HCAD. Future directions with HCAD include:

- Adding support for VHDL - the DoD mandated hardware description language.
- Completing the addition of support for the 5K gate array.

In summary, HCAD has been developed and the first release has now been delivered to AT&T. This release provides full support for full custom and standard cell designs (including the AT&T macrocell library) and tool support for gate array designs.

3. DEMONSTRATION VEHICLES

3.1 Memory Design Issues (W. E. Werner)

PT-2M Analysis

We used liquid crystal techniques to locate hot spots in PT-2M 256-bit clocked SRAMs. Detailed visual inspection identified the hot areas as decoder circuits, especially the areas where top metal crossed over a bottom-metal-to-ohmic via. A new top metal reticle was generated to eliminate this crossing. Test results from wafers with this modification show no signs of shorts in the decoder area.

Additional simulations were run to discover why measurements of PT-2M circuits did not agree with the original simulation results. New SargicS.15 models were used for these simulations. The switch point of an input buffer circuit was simulated under nominal conditions and found to be .75 volts. The measured switch point of PT-2M circuits with nominal processing was closer to .80 volts. Simulations run with the older SargicS.11 models predicted a .65 volt switch point. This shows the inaccuracy of the SargicS.11 model predictions and gives more confidence in the SargicS.15 models which were used in the design of the 4K SRAM.

Despite modeling inaccuracy, the PT-2 memory test results have been encouraging. The best wafer had greater than 30% functional chip sites, and 3 packages from the September deliverable group were found to be functional over the -55°C to 125°C temperature range.

4K SRAM Design Issues

In the 4K SRAM design, a major concern has been subthreshold leakage currents in the EFETs used as bilateral switches. Characterization work on test sites has uncovered some peculiarities on the narrow width EFETs. It appears that 3μm wide devices show appreciably higher subthreshold leakage currents than 18μm devices. Investigations will continue until these affects are understood.

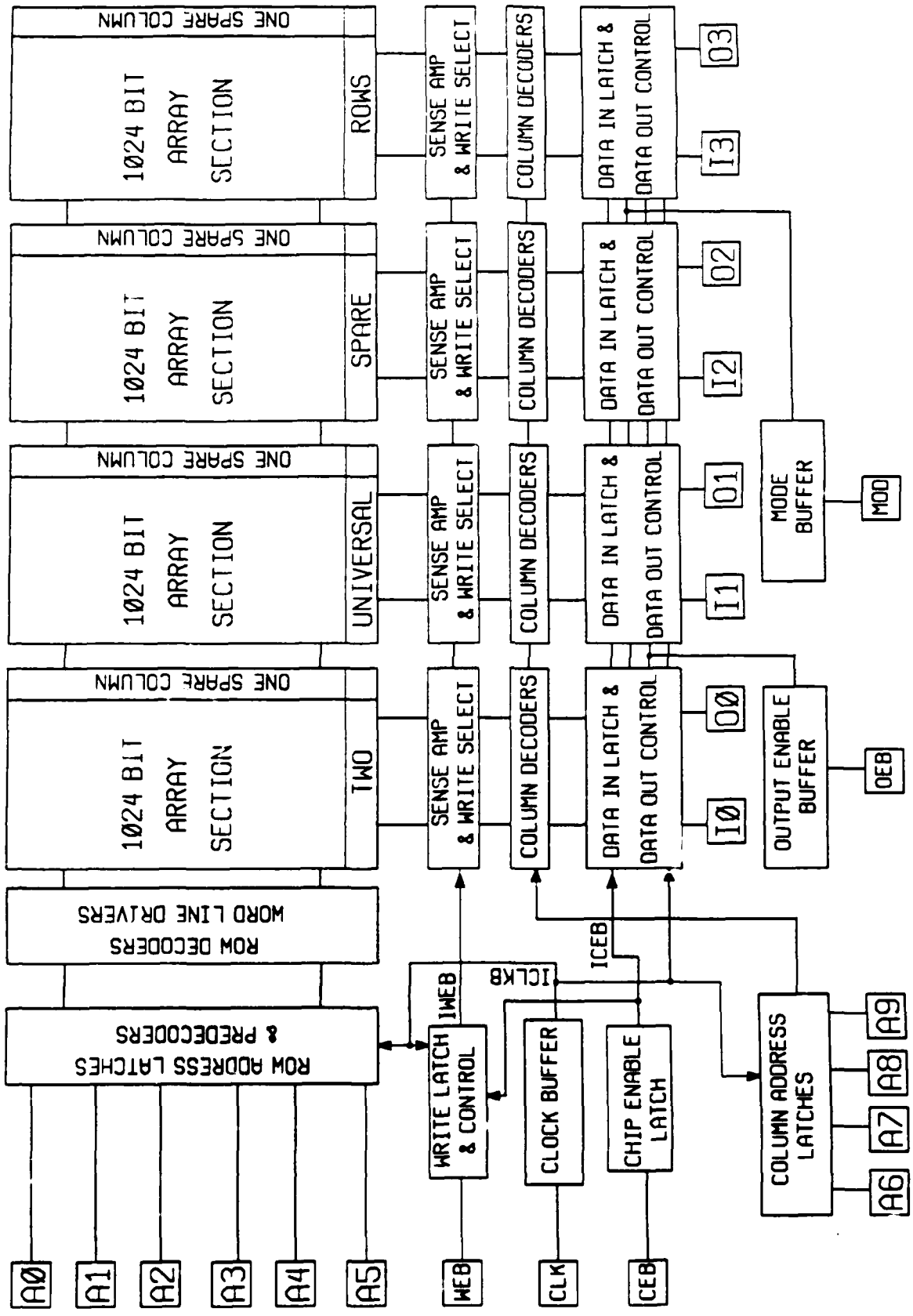
Several architectural options were evaluated for the 4K SRAM. The final decision is to have each of the 4 array sections organized as 64 rows by 16 columns. A block diagram of the 1K x 4 clocked GaAs SRAM is shown in Figure 1. Another decision was to use only the radiation-hardened cell array based on radiation test results from PT-2M. The cell size was increased to avoid areas where shorts or opens could occur because of top metal crossings.

Concerns about the output low level on PT-2M prompted redesign of the output driver section of the 4K SRAM. Also the write select circuit was modified to reduce the subthreshold leakage contribution of the write transfer EFETs. Full chip simulations were run on the 4K SRAM with layout extracted capacitance values. Some minor circuit modifications were needed to drive the capacitive load of long parallel runners. The final 4K SRAM Engineering Specification Document was prepared and submitted to DARPA for approval.

3.2 PT-2M Memory Test Results (W. R. Ortner)

Summary of Significant Test Results

Twenty PT-2M 256-bit SRAM Packages, fully functional at 200 MHz (25°C, Vdd=2.0V), were delivered to DARPA in September. As described in Section 3.1, three of the packages functioned over the entire -55°C to 125°C temperature range at 50 MHz (at some Vdd between 1.8v and 2.2v). This is a significant milestone for the project.



1K x 4 Clocked GaAs SRAM

Figure 1.

Wafer Test Results

During the current six month interval (April through September, 1989) nine PT-2M lots with a total of 42 wafers have been tested at the Cedar Crest Memory Test Facility. All wafers were tested at 40°C; lots 3280 and 3288 had exceptionally good yield, as shown in Table 2, and were subjected to further testing at 80°C, 100°C and 125°C. Access Time was found to lengthen significantly with increasing temperature; however, a total of 63 chips are still fully functional at 50 MHz and 125°C. No chips functioned at 200 MHz and 125°C.

Device Characterization

We used data from the twenty delivered packages to characterize device performance and to relate performance to temperature and EFET threshold. As seen in Figure 2, Ripple Mode Access Time (Tar), which ultimately determines the maximum pipeline cycle rate, is a minimum at -55°C and increases gradually with increasing temperature until 80°C, where it increases rapidly beyond 5 ns. Speed and power are maximum at -55°C. (In this figure and Figures 3, 5, and 6, the dashed lines indicate the specification limits.)

In Figure 3, for 25°C, we show that access times and currents correlate well with EFET threshold. Devices having lower thresholds are observed to be faster and to consume more power. Since lower threshold results in higher drain current for a given drive level, this result is expected. The distribution of access time (Tar) indicates there will be some yield loss for 200 MHz operation.

The EFET threshold, measured at the open source DOUT signal lead, decreases with increasing temperature (see Figure 4). At first, this might seem incompatible with the observed speed and power sensitivity to threshold (i.e., speed and power are maximum at -55°C). However, other physical mechanisms, like free carrier mobility, come into play as temperature varies, and they dominate behavior with temperature.

Figure 5 shows in the input and output voltages as a function of temperature. The minimum voltage for a logic "1" and the maximum voltage for a logic "0" are well within specification. That is, Voh > 1.0V, Vol < 0.2V. As described in Section 3.1, there is a problem with the input switchpoint. PT-2M was designed for a 0.6V switchpoint, but the SargicS.11 model was somewhat inaccurate. The actual switchpoint is about 0.8V, leading to some devices that fail the requirement for Vih < 0.9V. (All devices pass the requirement for Vil > 0.3V.) We are confident that the newer SargicS.15 models are much better, and the input switchpoint in the 4K SRAM should be near the desired 0.6V.

As shown in Figure 6, the input Setup and Hold Times generally meet the specification. There will be some yield loss for hold time.

Table 2 — PT-2M Wafer Test Results - Current Six Month Interval

Wafer†	°C	Number of Working†† Chips			
		Ripple		Pipeline	
		50 MHz	200 MHz	50 MHz	200 MHz
32503	40	34	3	13	9
32504	40	2	0	0	0
32505	40	5	1	1	2
32508	40	3	1	2	1
32691	40	4	0	4	2
32743	40	31	0	23	8
32792	40	18	0	3	0
32793	40	7	0	4	0
32794	40	6	0	1	0
32795	40	35	0	21	1
32796	40	19	0	10	0
32803	40	65	1	58	9
32803	80	61	0	57	0
32803	100	58	0	54	0
32803	125	32	0	30	0
32804	40	11	0	6	0
32805	40	8	0	1	0
32806	40	47	0	39	5
32881	40	180	35	170	47
32881	80	24	0	24	1
32881	100	1	0	1	0
32882	40	200	10	194	82
32882	80	178	15	176	21
32882	100	139	0	136	0
32882	125	7	0	8	0
32883	40	14	0	16	2
32883	80	24	0	24	1
32883	100	25	0	26	1
32883	125	21	0	25	0
32885	40	156	26	156	47
32885	80	40	2	36	16
32885	100	2	0	2	0
32885	125	0	0	0	0
32886	40	84	17	93	19
32886	80	41	0	43	3
32886	100	14	0	15	0
32886	125	9	0	10	0
Total	40	929	94	815	234

† There are 543 chips per wafer.

†† Work at 40°C over the entire Power Supply Range (1.8v to 2.2v).

PT-2M: Speed and Power vs. Temperature

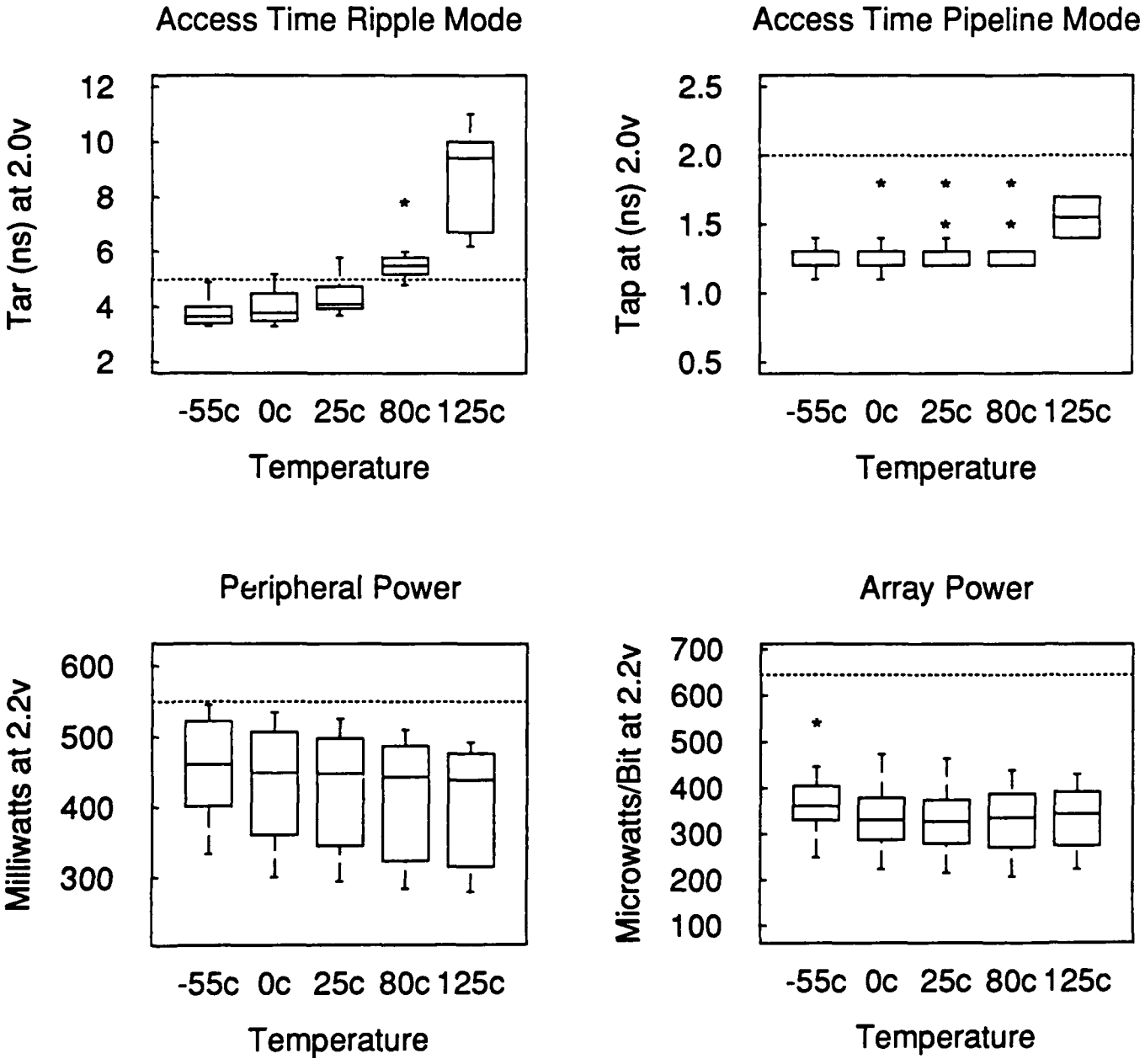


Figure 2.

PT-2M: Speed and Power vs. Effective Threshold (Vgs) at 25°C

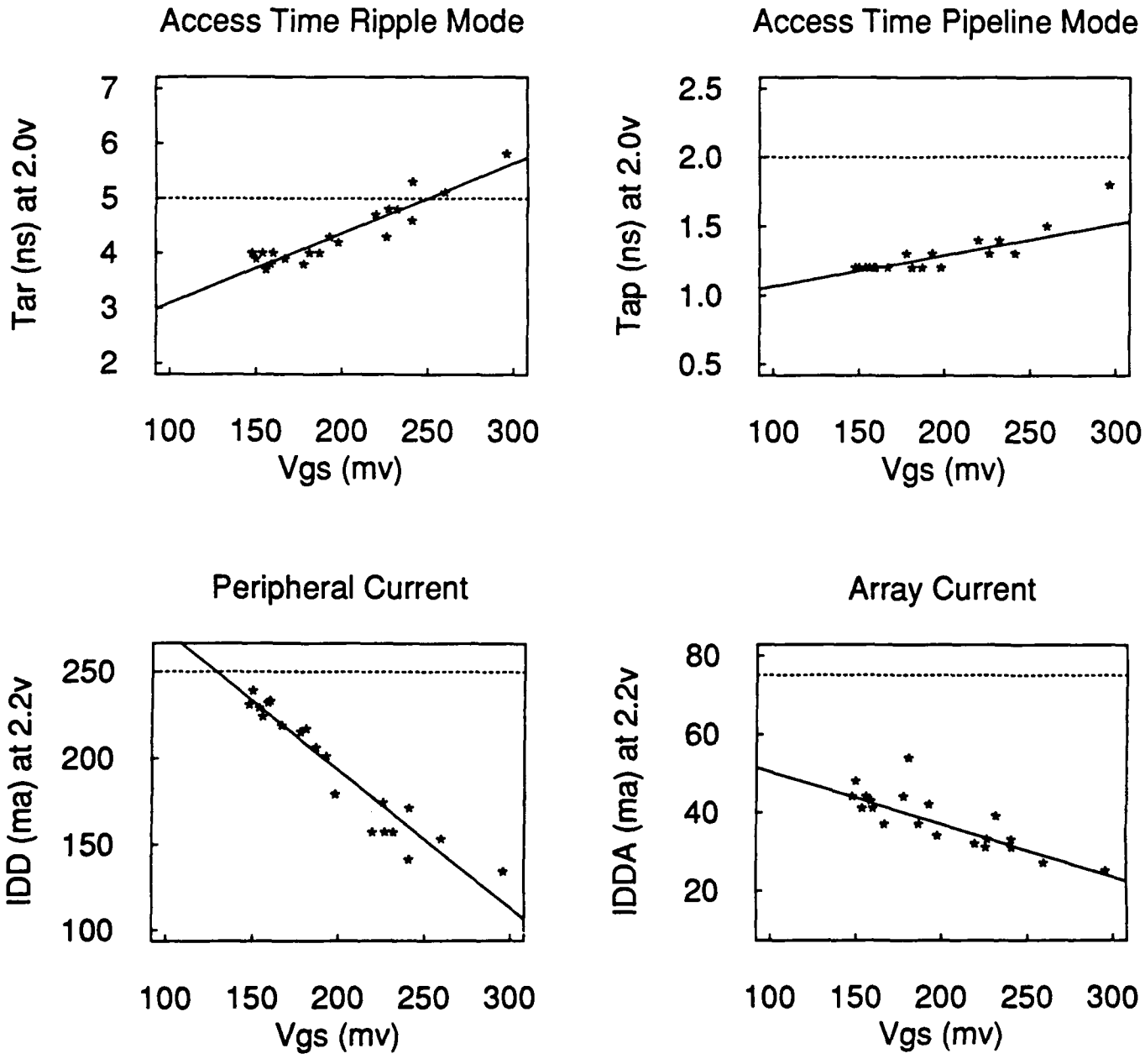
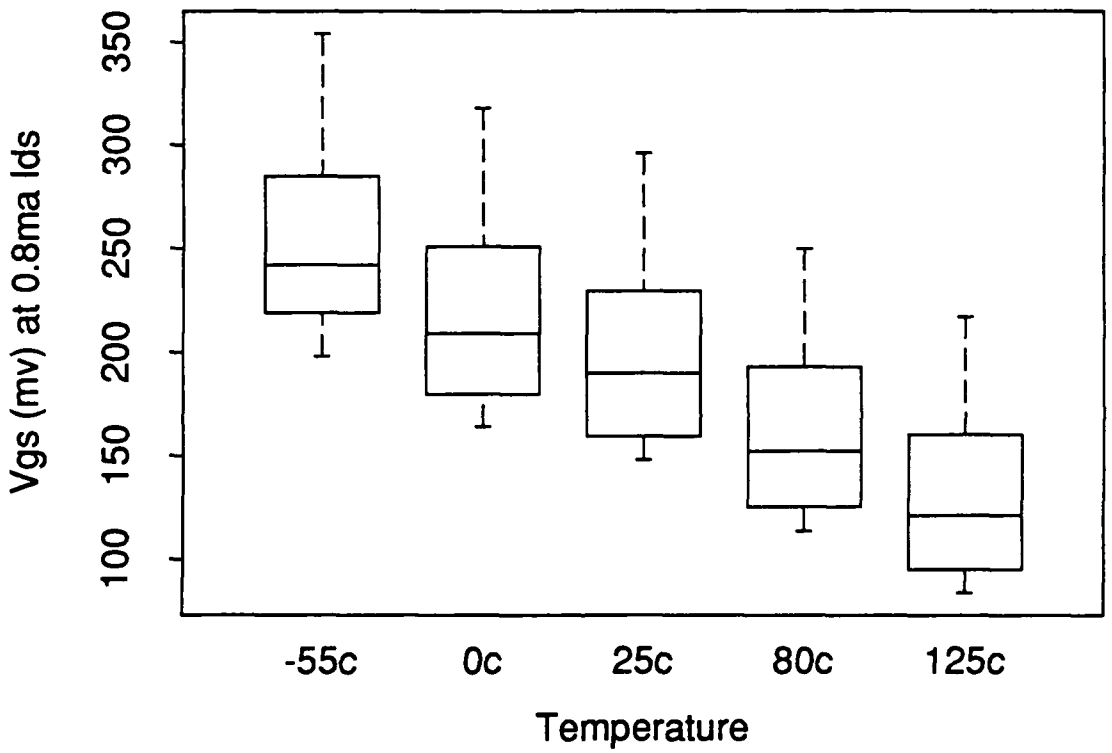


Figure 3.

PT-2M: EFET Effective Threshold (Vgs) vs. Temperature



Vgs is Measured On Each Device Using The DOUT Signal Lead
(The Output is an Open Source EFET)

Figure 4.

PT-2M: Input and Output Signal Levels vs. Temperature

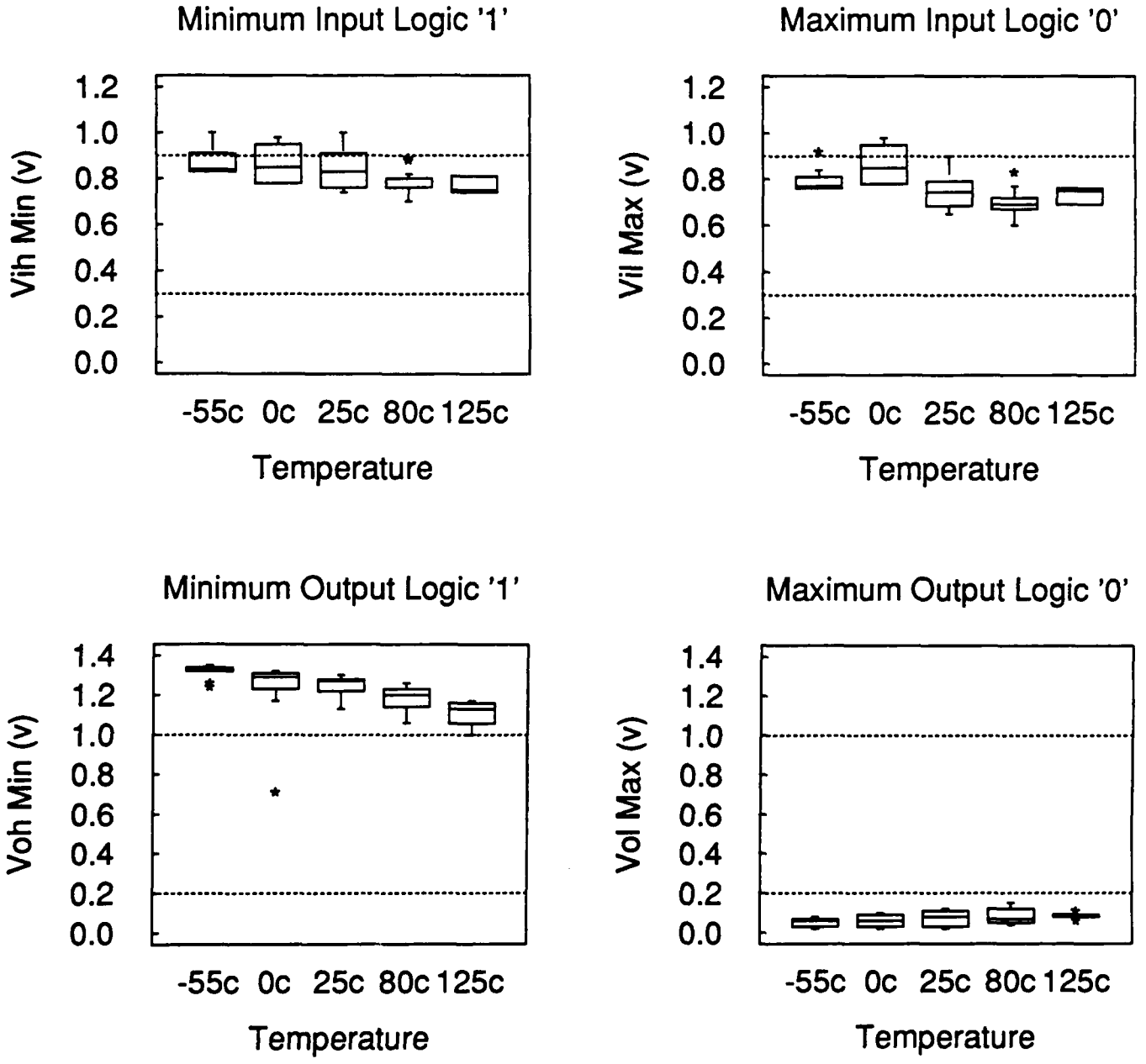


Figure 5.

PT-2M: Setup and Hold Time vs. Temperature and vs. EFET Effective Threshold (Vgs) at 25°C

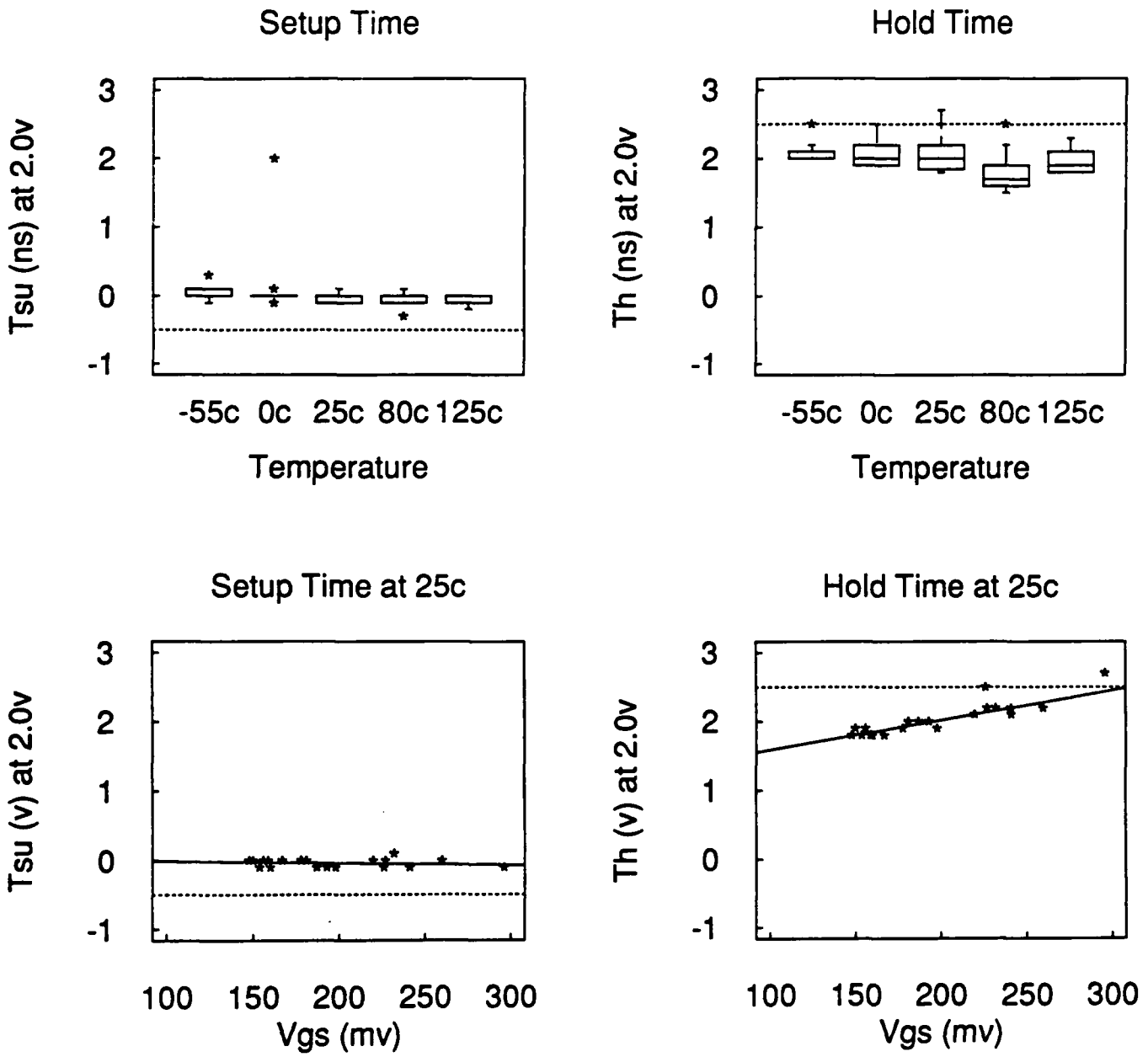


Figure 6.

3.3 Laser Programming (R. T. Smith)

The main objectives during this reporting period were to establish and verify automated laser repair of PT-2M memories; to laser repair PT-2M wafers for deliverables inventory and reliability studies; and to issue design rules for laser programming the 4K SRAMs. All three objectives were successfully accomplished.

Laser repair of PT-2M memories was demonstrated successfully for the first time on April 20, 1989, by Fred Fischer and Shaulong Chin. Automated, off-line repair was proved in two weeks later on May 3, six weeks ahead of schedule. Since that time, PT-2M wafers have been routinely laser programmed for deliverables inventory and to provide models for radiation testing and reliability studies. This activity will continue as long as PT-2M lots are processed in the Pilot Line. Although the automated laser programming process was proved in on both Teradyne M118M and ESI 8000C laser systems, using repair menus generated off-line on the Teradyne J937 test system, the ESI equipment has been used for the majority of the PT-2M models. Either system is capable of doing the job. Results on the best wafer so far, Number 32881, were as follows. Of the 274 functional chips (56% yield), 176 were initially functional, and 98 were successfully laser repaired from a potentially repairable population of 116. The repair rate was 84%, which is highly respectable in an off-line process which precludes the possibility of using spare replace spare techniques.

Design rules for laser programming the 4K SRAMs were issued on August 8, 1989, two weeks behind schedule, but early enough to have no impact on the mask shop submittal. During the summer, Professor Leonard Scarfone of the University of Vermont was engaged as a consultant on laser-materials interactions in the GaAs/dielectric/Au multilayer structure representative of the links used in programming PT-2M devices.

3.4 PT-2 Logic Test Results (C. E. Reid, L. Ackner, C. H. Tzinis)

Since the last semiannual report, a total of 53 PT-2L wafers from nine lots have been tested. Five of the lots tested produced working devices and are summarized in Table 3.* Not shown are lots 31960, 32140, 32180, and 32300 which produced zero yield. Processing information indicated that the EFET and DFET thresholds for these lots were not within specifications, and this probably caused the poor wafer yield.

The high wafer test yield for lot #31870 was due to preconditioning before the actual stimuli used for functional test. (That is, the circuit was exercised with one or more sets of test vectors before data were actually taken.) This strategy proved successful. However, lots processed after lot #31870 did not seem sensitive to preconditioning. This may be due to improvements in control of materials and wafer processing. We will not investigate preconditioning further unless the need for it reappears.

Tables 4-6 show test data for the PT-2L ALU, Quad 4-bit Adder, and Dual 8-bit Multiplier. The propagation delays are shorter than the program requirement by comfortable margins. The requirement is 200 MHz operation for 15-20 gate delays (5 ns propagation delay). We find 5.3 ns (189 MHz) for the ALU (33 gates plus input/output buffers), 2.3-3.3 ns (303-435 MHz) for the Adder (9 gates plus input/output buffers), and 7-10 ns (100-143 MHz) for the Multiplier (40 gates plus input/output buffers).

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* Working means successfully passing all test vectors at 1 MHz at Vdd=2.0V.

Few of the devices tested in this period conform to all I/O levels; the primary failure mode is high Vih. This is consistent with data from the previous reporting period, where circuits were close to the borderline of the Vih specification. There are two reasons for this. First, the input switch points were incorrectly simulated by the SargicS.8 model files used to design PT-2L; actual switch points are 0.2V higher than simulated. Second, during this period our DFETs had thresholds near -200 to -300mV instead of the -500mV design target. In combination, these two problems shift Vih to unacceptably high levels. While PT-2L was being fabricated, we were already attacking these problems. We adjusted the MBE structure to bring the DFET threshold closer to target, and we tightened the growth specifications to reduce the DFET threshold variation. We also upgraded our models, ending up with SargicS.15. Section 3.1 has already discussed the improvement in simulation accuracy given by these models. Having learned what we wanted from PT-2L, we have moved on to other circuits. So while PT-2L will never see the benefits of these improvements, the other circuits will.

Of the nine lots tested, there was no functional Memory Tester Chip. Failure mode analysis was performed using the Sentry IDS 5000 electron beam prober and the Advantest T3340 test system. We found the failure was a layout error in the B section of the clock/reset logic. There is identical clock/reset logic for section A. These clock and reset signals are used by two identical counters, A and B. A bug in the design rule checker allowed two metal runners butting at the corners to pass as a connection. At wafer fabrication, these two metal runners separated and became an open circuit. As a result, there was no clock signal to counter B, but the reset signal was present. The bug in the design rule checker was fixed and this problem should not occur again. Since this device was not a deliverable part to DARPA, a mask fix was not initiated.

Data for packaged devices are shown in Table 7. Some of these devices were delivered to DARPA. All these devices worked over the temperature range of -55°C to 125°C. Again the propagation delays are shorter than the program requirement by comfortable margins. Likewise, all the circuits work at or below the required Vdd $\leq$ 2.0V.

In summary, PT-2L served its originally planned purposes:

- Prove-in of design tools for custom, standard cell, and cell arrays; the design tools were used successfully in all circuits except the memory tester, and the software has been fixed to avoid recurrence of the memory tester's layout error.
- Prove-in of test hardware for medium complexity circuits (up to 2K gates, 64 I/Os).
- Utilization of diagnostic tools and data analysis for problem identification and expedient solution.
- Understanding of device models and areas where model needed improvement for better simulation accuracy.

Finally, PT-2L served well as a "stepping stone" (just as planned) toward full size deliverables.

Table 3 - PT-2L Wafer Yield Summary For Logic Circuits

Wafer #	Yield / Wafer				
	Date Tested	8-bit Multiplier	4-bit Adder	Memory Tester	32-Bit ALU
31722		1	5	0	0
31723	11/9/88	2	7	0	0
31724		0	10	0	0
31871		7	11	0	6
31872		9	16	0	6
31873	2/9/89	16	14	0	8
31874		6	8	0	5
31876		0	2	0	1
31877	5/30/89	2	13	0	9
32231		1	2	0	0
32233-8	4/13/89	0	0	0	0
32401		1	0	0	0
32402		0	0	0	0
32403	4/13/89	5	6	0	0
32404		2	3	0	0
32406-8		0	0	0	0
32871		1	5	0	2
32872	6/22/89	5	5	0	7
32874		0	3	0	1
32875		0	2	0	1
32875	7/11/89	0	0	0	0

There are 30 test sites per device per wafer.

Lots #31960 #32140 #32180 and #32300 had zero yield.

Table 4 - PT-2L 32-BIT ALU WAFER TEST RESULTS AT 1 MHz

	Mean ± σ	
	LOT 31870	LOT 32870
Prop. Delay (ns)	NA	5.29 ±1.07
Dyn. Idd (A)	1.34 ±0.19	1.57 ±0.26
Min. Vdd (V)	1.94 ±0.32	1.92 ±0.16

Data was obtained from 4 wafers for lot 31870 and 4 wafers for lot 32870

NA: Not Available

Table 5 - PT-2L 4-BIT ADDER WAFER TEST RESULTS AT 1 MHz

	Mean ± σ		
	LOT 31720	LOT 31870	LOT 32870
Prop. Delay (ns)	3.34 ±0.03	2.34 ±0.06	2.95 ±0.41
Dyn. Idd (mA)	411 ±6.9	496 ±67.5	736 ±79.5
Min. Vdd (V)	1.59 ±0.03	1.49 ±0.03	1.60 ±0.08

Data was obtained from 2 wafers for lot 31720 and 4 wafers for lot 31870 and lot 32870

NA: Not Available

Table 6 - PT-2L 8-BIT MULTIPLIER WAFER TEST RESULTS AT 1 MHz

	Mean ± σ		
	LOT 31720	LOT 31870	LOT 32870
Prop. Delay (ns)	10.28 ±1.01	7.11 ±0.67	7.92 ±1.04
Dyn. Idd (A)	1.04 ±0.11	1.25 ±0.19	1.71 ±0.9
Min. Vdd (V)	1.82 ±0.43	1.65 ±0.09	1.93 ±0.19

Data was obtained from 2 wafers for lot 31720 and 32870 and 4 wafers for lot 31870

NA: Not Available

Table 7 - PT-2L PACKAGE TEST RESULTS (25°C)

Circuit	Wafer #	# of Pkgs	Average Propagation Delay (ns)	Average Performance (MHz)	Average Dynamic Current (A 1 MHz)	Minimum Vdd (V)
32-bit ALU	31872	3	NA	NA	1.146	1.588
	31873	4	NA	NA	1.401	1.589
	31874	3	NA	NA	1.302	1.603
	31877	4	5.500	180	1.382	1.878
4-bit Adder	31872	4	3.812	260	0.490	1.390
	31873	4	3.625	276	0.641	1.474
	31877	5	2.275	440	0.663	1.646
8-bit Mult	31873	9	7.747	129	1.371	1.632
	31874	2	8.187	122	1.389	1.677
	31877	1	6.875	145	1.408	1.688
	32403	2	6.375	157	1.359	1.690

NA: Not Available

3.5 1K Cell Array Testing (W. Satre)

Testing of the 1K Cell Array wafers was started on the HP82000 verification tester. This was the first trial of the wafer probing apparatus supplied with this machine, and mechanical problems were immediately encountered. It was necessary to return the fixture to the manufacturer for rework, so a program was prepared for testing the wafers on the Advantest T3340. This test program had an error which allowed the functional test to pass only the first 4367 vectors. When the problem was fixed we were able to probe the 17 wafers which were on hand. Based upon shmoo plot data obtained during the program debugging, we chose a set of test voltages which gave the widest margin for passing the greatest number of vector cycles. Using a Vdd supply voltage of 2.5 volts, a Vih/Vil range of 2.0 volts to 0.2 volts, and Voh/Vol values of 0.8 volts each, functional testing was performed at 10.0 MHz. At this preliminary phase of testing no strict adherence to the design intent of I/O levels was attempted rather identifying functional devices for packaging, where a more elaborate study and FMA is underway.

Of the 17 wafers probed (83 sites per wafer) there were 125 sites which passed all 5648 test vectors; 120 of these functional devices were on 7 of the wafers, and there were 7 zero yield wafers. Table 8 compares the circuit yields to the PCM data. Like the full-custom, full-size ALU and five of the six PT-2 logic circuits, this design is "right first time." This relatively low yield is because we chose to test wafers with marginal PCM data in order to verify the correctness of the design. To expedite the packaging of functional devices which could be tested at speed on the HP82000, only this low speed functional test and a quiescent power supply current test were performed at this time. The Idd current of the 2.5 volt supply was consistent with the simulated values and was typically 400 to 600 milliamps. A total of 46 devices from three of the better yield wafers has been packaged and will be extensively tested for DC parametrics and maximum operating speed.

Table 8 — 1K Cell Array Wafer Yield Summary

Wafer Number	Functional Sites	PCM Data		
		Via Resistance	E-Ids	D-Ids
33081	0	Good	Poor	Good
33082	0	Good	Poor	Poor
33084	18	Good	Fair	Good
33085	16	Good	Good	Good
33086	19	Good	Good	Good
33121	0	Good	Poor	Poor
33122	31	Good	Fair	Good
33123	18	Good	Fair	Good
33124	10	Good	Fair	Good
33125	9	Good	Fair	Good
33126	0	Good	Poor	Poor
33191	0	Good	Poor	Fair
33193	0	Good	Poor	Poor
33194	0	Good	Fair	Poor

3.6 Custom ALU Test Results (L. Ackner, W. B. Leung, C. H. Tzinis)

The full-size, full-custom ALU is a digital circuit with about 3.5K gate complexity. It is one of the deliverable circuits specified in the contract, and the circuit layout is in custom style. Circuit design was completed in February 1989, and two lots were processed and tested through September, 1989. Working devices (pass all 170 vectors correctly) were found in both lots. The PCM data of these wafers were used to predict the yield, as shown in Table 9. For lot 3281, the PCM screen properly predicts the wafers with good yield. Surprisingly, despite the poorer PCM data, lot 3309 also produced some good yields; we found that these wafers had regions with good PCM data, although the wafer average PCM data was poorer. The best wafer has 7 functional sites out of a total of 51 sites, corresponding to 14% yield.

Several packages from these two first lots were assembled for September deliverables. Figure 7 shows the ranges of the input and output voltages for these devices.* For each device, a given pin is measured while all the others are held at a nominal value. The requirements for voltage levels are:

Inputs:	Min Vih < 0.9V
	Max Vil > 0.3V
Outputs:	Min Voh > 1.0V
	Max Vol < 0.2V

The boxplots show that the medians of the inputs are within 0.3-0.9V (where they should be); and the medians of the outputs are outside the 0.2-1.0V region, as designed (except for circuit #10). As there are considerable spreads around the medians, these devices do not meet their full specifications. To fix this problem, we will have to improve the uniformity of our processing.

To our surprise the package test data were not exactly the same as the wafer probe data, especially in terms of input levels and minimum Vdd. Preliminary diagnostic analysis showed two substantial differences between the two tests. First, without intentional temperature control, the packaged circuits operate much hotter than the circuits at wafer probe. Second, the testing algorithms are different. We are presently working to make wafer testing a better predictor of package data.

The propagation delay would easily meet the contract requirement. Average value for lot 33090 is 3.68 ns delay for 26 gates, corresponding to 142 ps delay per gate. The best delay value is 2.9 ns, corresponding to 112 ps per gate. While these results are obtained at an ambient temperature of 25°C, the junction temperature is much higher beca se the power dissipation is about 5 W.

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* The middle line in a boxplot is the median of the data, and the upper and lower boundaries of the box show the two quantiles surrounding the median. The dashed vertical lines above and below the box show the remainder of the data, except we plot individually those points more than 1½ times the interquartile distance from the quartile boundary.

Table 9 — Custom ALU Wafer Yield Summary

Wafer Number	Date Tested	Func Sites	PCM Data		
			Via Resistance	E-Ids	D-Ids
32811		0	Short	Good	Fair
32812		6	Good	Good	Good
32813	6/20	7	Good	Good	Good
32814	1989	0	Short	Good	Fair
32815		2	Good	Fair	Poor
32816		3	Good	Good	Good
33094		6	Good	Poor	Fair
33095	7/18	2	Good	Poor	Poor
33096	1989	7	Good	Poor	Fair

E-Ids and D-Ids are EFET and DFET currents.

3.7 Transversal Filter Chip Design (S. W. White, R. J. Betancourt-Zamora)

The Transversal Filter Chip (TFC), implemented with the macrocell library developed by AT&T, is one of the contract's deliverable standard cell circuits. This chip, having a complexity in excess of 5K gates, implements a digital filter intended for use in infrared signal processing systems. The design and masks have been completed, and the first wafer lot has recently entered the processing line. A summary of circuit design data appears in the following table.

- Signal/Supply Pins: 105/68
- Number of Transistors: 41,334
- Predicted Power Dissipation: 6.3 W
- Predicted Performance: 160 MHz
- Critical Path: 23 gates
- Die Size: 9.1 X 9.2 mm
- Package: TriQuint 196/128 Leaded Chip Carrier

At the beginning of this reporting period, efforts were concentrated on optimizing the TFC's layout. To ensure proper circuit operation, the power distribution scheme features center power buses along with cell row buses that are 25% wider than their standard size. HCAD's Interactive Global Router has been used extensively to implement this scheme in a manner which minimizes chip area. Maximum worst case voltage drops of 110 mv have been achieved on these buses while maintaining current densities well below electromigration limits.

The final layout was generated through an iterative process driven by feedback obtained from HCAD's TA static timing analyzer. Initial post-layout timing simulations revealed that key control signals within the TFC's multiplier were more heavily loaded than expected. In order to speed up the circuit, signal buffers were added and higher routing priorities were specified for

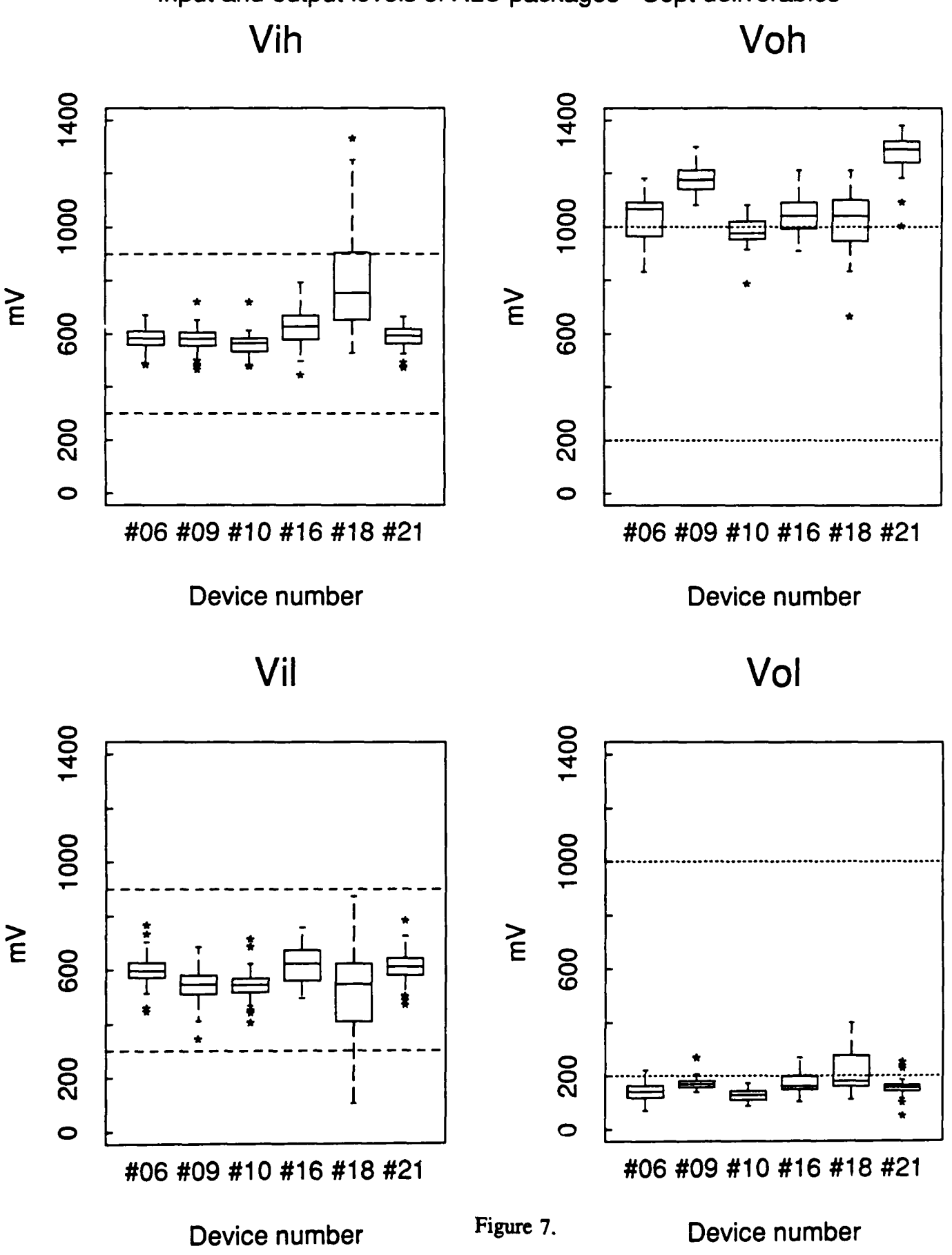

Input and output levels of ALU packages - Sept deliverables
Vih
Voh
Vil
Vol
mV
0
200
600
1000
1400
#06 #09 #10 #16 #18 #21
Device number

Figure 7.

these nets. In addition, other critical signals including the clock nets were optimized by specifying their topology with the Interactive Router. Through this process, the circuit's performance improved by approximately 20%.

The layout verification process consists of running design rule checks and layout vs. schematic checks using tools provided by HCAD. These were initially run at the macrocell level, in which only the interconnections between cells were examined, and later at the artwork level, in which devices and their physical geometries within the layout were checked. Following verification, AT&T discovered that the database contained a number of occurrences of polygon abutment. AT&T implements a compensation of the artwork layers before masks are made in order to account for the effects of photolithography and other processing steps. Consequently, polygons which connect by abutment can pull apart during the compensation process. To avoid potential problems with open circuits, a program was run which creates layout patches on top of all polygon abutment regions. The final layout, including these patches, has been reverified prior to the making of masks. In addition, minor modifications have been made to cell abstract representations within HCAD to avoid future occurrences of this problem.

In preparation for wafer-probe testing of the TFC, a probe card has been designed and is currently being manufactured by Microprobe. A metallized wafer patterned with the bonding pad layer has been fabricated and is being used to facilitate the probe card development. Test vectors have been compiled on the Advantest tester and will soon become part of a complete test program to be used for both wafer-probe and packaged-part testing.

3.8 32-bit Multiplier Design (L. R. Tate)

To apply the SARGIC HFET process to a mainstream application, we chose a circuit which addresses a data processing bottleneck in high performance scientific workstations: namely, the floating point multiplier. The floating point multiplier used in the design of high performance floating point processors cannot be pipelined without loss of system performance for applications with dataset dependencies. Therefore, it has an inherent high gate depth and hence low I/O bandwidth. The low I/O bandwidth allows the use of this gallium arsenide circuit to improve the performance of a practical system composed primarily of mainstream MOS and ECL integrated circuits.

During this reporting period, we developed a detailed specification which included the essential features of commercially available circuits. The 32-bit IEEE Floating Point Multiplier accepts two 32-bit floating point basic single IEEE format operands and generates a 32-bit IEEE format product in less than 15 nanoseconds (67 MFLOPS). The 50,000 transistor chip may be used as a building block in floating point systems which support IEEE standard 754 or as a multiplier in signal processing systems. Referring to the architectural block diagram of Figure 8, note the flow-through architecture employed to minimize total latency and thereby allow full performance even in applications with dataset dependencies (registers are used only on the inputs and outputs). Booth recoding is employed to reduce the number of partial products and thereby reduce circuit complexity and power consumption. To obtain absolute maximum speed without sacrificing layout regularity, a binary tree of 4-2 adders is used to reduce the Booth recoded partial products. This results in a time optimum (proportional to Log n) architecture. Features which support IEEE standard 754 include IEEE basic single format operands and results, implementation of all four IEEE rounding modes, and exceptions processing in conformance with the standard. The exceptions processing for IEEE mode is fully described by the table in Figure 9. This table shows the flags and output data types that are generated as a function of the input operand data types. Seven status flags are provided (overflow, underflow, inexact, invalid operation, rounded up, not-a-number, and denormal operand).

Figure 8.

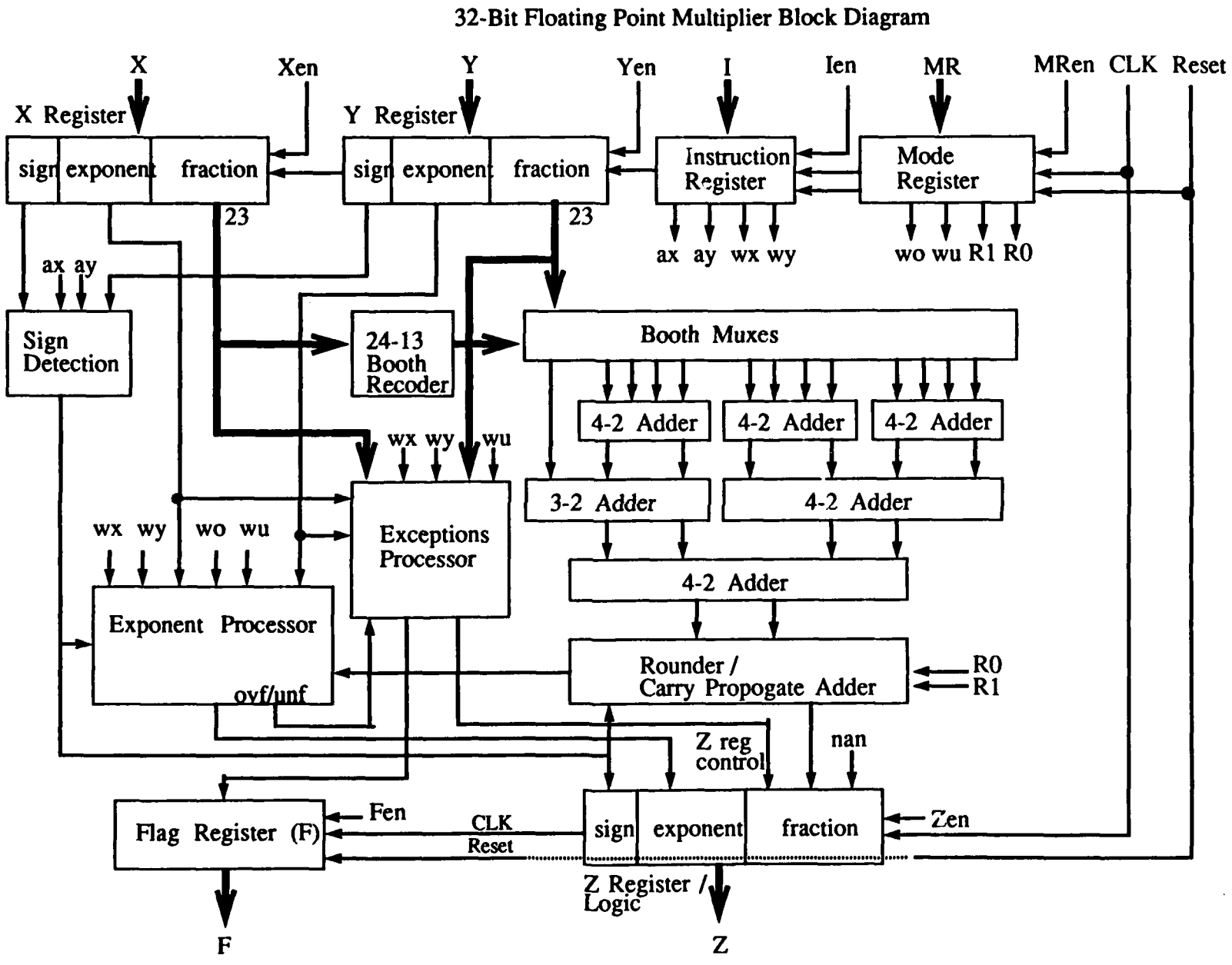

32-Bit Floating Point Multiplier Block Diagram
X
Xen
Y
Yen
I
Ien
MR
MRen
CLK
Reset
X Register
Y Register
sign
exponent
fraction
23
Instruction Register
Mode Register
ax ay wx wy
wo wu R1 R0
ax ay
Sign Detection
24-13 Booth Recoder
Booth Muxes
4-2 Adder
3-2 Adder
wx wy wu
wx wy wo wu
Exceptions Processor
Exponent Processor
ovf/unf
Rounder / Carry Propogate Adder
R0
R1
Z reg control
nan
Flag Register (F)
Fen
CLK
Reset
Zen
Z Register / Logic
F
Z

Table for Exceptions for IEEE Compatible Mode (WU bit set)

X Operand

Y Operand	ZERO	DNRM	WRAP	NRM	NaN_S	NaN_Q	INF
ZERO	none/0	DEN/0	none/0	none/0	INV,NaN/ NaN-Q	NaN/NaN-Q	INV,NaN/ NaN-Q
DNRM	DEN/0	INX,DEN/0	INX,DEN/0	INX,DEN/0	INV,NaN/ NaN-Q	NaN/NaN-Q	DEN/INF
WRAP	none/0	INX,DEN/0	INX,none/0	none/NRM, UNF/WRAP, none,UNF/0	INV,NaN/ NaN-Q	NaN/NaN-Q	none/INF
NRM	none/0	INX,DEN/0	none/NRM UNF/WRAP none,UNF/0	OVF/{WRAP, INF, NRM.MAX}, none/ NRM, UNF/WRAP	INV,NaN/ NaN-Q	NaN/NaN-Q	none/INF
NaN_S	INV,NaN/ NaN-Q	INV,NaN/ NaN-Q	INV,NaN/ NaN-Q	INV,NaN/ NaN-Q	INV,NaN/ NaN-Q	INV,NaN/ NaN-Q	INV,NaN/ NaN-Q
NaN_Q	NaN/NaN-Q	NaN/NaN-Q	NaN/NaN-Q	NaN/NaN-Q	INV,NaN/ NaN-Q	NaN/NaN-Q	NaN/NaN-Q
INF	INV,NaN/ NaN-Q	DEN/INF	none/INF	none/INF	INV,NaN/ NaN-Q	NaN/NaN-Q	none/INF

Figure 9.

The possible data types are zero (0), denormal (DNRM), wrapped underflow (WRAP), normalized (NRM), signalling not-a-number (NaN_S), quiet not-a-number (NaN_Q), and infinity (INF). The output flags are listed first, then a "/" (slash), and then the possible data types are listed - curly braces enclose the data field when more than one data type is possible. In some case multiple flag and data type combinations are possible. When no flags are generated the word "none" appears in the flag field.

Support for IEEE gradual underflow (denormals) is provided when the multiplier is in "wrapped underflow" mode via a "wrapped underflow" datatype. A "Fast" mode where denormal results are set to zero is also provided for signal processing applications. The architecture employs separate multiplier, multiplicand, instruction, and mode input ports, each with an asynchronous enable for maximum flexibility. Three state output ports are provided for the product and flag registers. The circuit operates from a single 2 volt power supply and is packaged in a 196 pin controlled impedance MLC package.

During this reporting period, a project team of five engineers and one layout designer completed the system design (detailed chip specification) and also completed the logic design, circuit design, layout, and layout verification of 36000 of the 50000 transistors needed to implement the above specification. In addition, a detailed chip plan was developed to guide the placement and routing of the individual subcircuits. We completed first pass logic design of all of the system sub-blocks in the detailed block diagram of Figure 10 except the exceptions processor, and we designed and simulated a few candidate I/O buffers.

3.9 Cell Array Casino Test Chip Design (W. Oswald)

Having completed the 1K gate array, we began work on the 5K Casino Test Chip (CTC) gate array. The 5K CTC (which is functionally identical to the standard cell CTC) is approximately five times larger, in gate count as well as area, than the 1K. This design will be jointly developed by AT&T Bell Laboratories and Hughes Aircraft Corporation. The Hughes team is headed by Spencer White, who was responsible for the standard cell CTC. To manage a design effort that includes two companies separated by 3000 miles, we used a September 26 and 27, 1989, meeting at Hughes to develop a methodology that would allow both locations to interchange data so that the design could be independently verified. AT&T will provide the basic floor plan and cell personalizations to Hughes. Hughes will use HCAD to place and route the CTC and provide AT&T with the completed design as well as the critical path information. AT&T and Hughes will independently verify the design. AT&T will do critical path analysis. This methodology will give us double coverage; triple if we also use DRACULA (ECAD) to verify the design. The only data which needs to be transmitted between locations is the geometric design database, ASCII net list, and vector files. Another concern was the size of the 5K CTC. We were not sure how HCAD would react to a device of that size, so LeRoy Fisher (responsible for HCAD) and his colleagues conducted tests using the 1K design. The tests were successful.

To design this circuit a new family of devices was created. This family is based upon the standard cell "E" family of devices developed at AT&T. A naming convention was established so there could be no confusion between the gate array and standard cell families. The first letter of the name (except the clock driver and signal driver) signifies the drive capability of that device. This creates sub families within the library. For example, an NINRB is an inverter without a drive buffer, an MINRB has a medium drive buffer, and an HINRB has a high drive buffer. This allows us to pick and choose the best device for most design situations. Additionally, the OAI22 sub family was redesigned to eliminate dual gates and the 2 input nand gates were eliminated from the design (because they contain dual gates). The main gate array family includes the following: inverters, 2-5 input nor gates, I/O buffers, a clock driver, a signal driver, D type latches, 2 to 1 multiplexers, and OAI22 gates.

The 5K CTC design contains approximately 3700 gates which will require 4221 cell sites (528 islands). The floor plan (see Figure 11) contains 5040 possible sites (630 islands). When the 5K is complete, we will have used 84% of the available sites. The over all dimensions are 11,748μm X 11,744μm (just over one square cm). We anticipate a power consumption of over

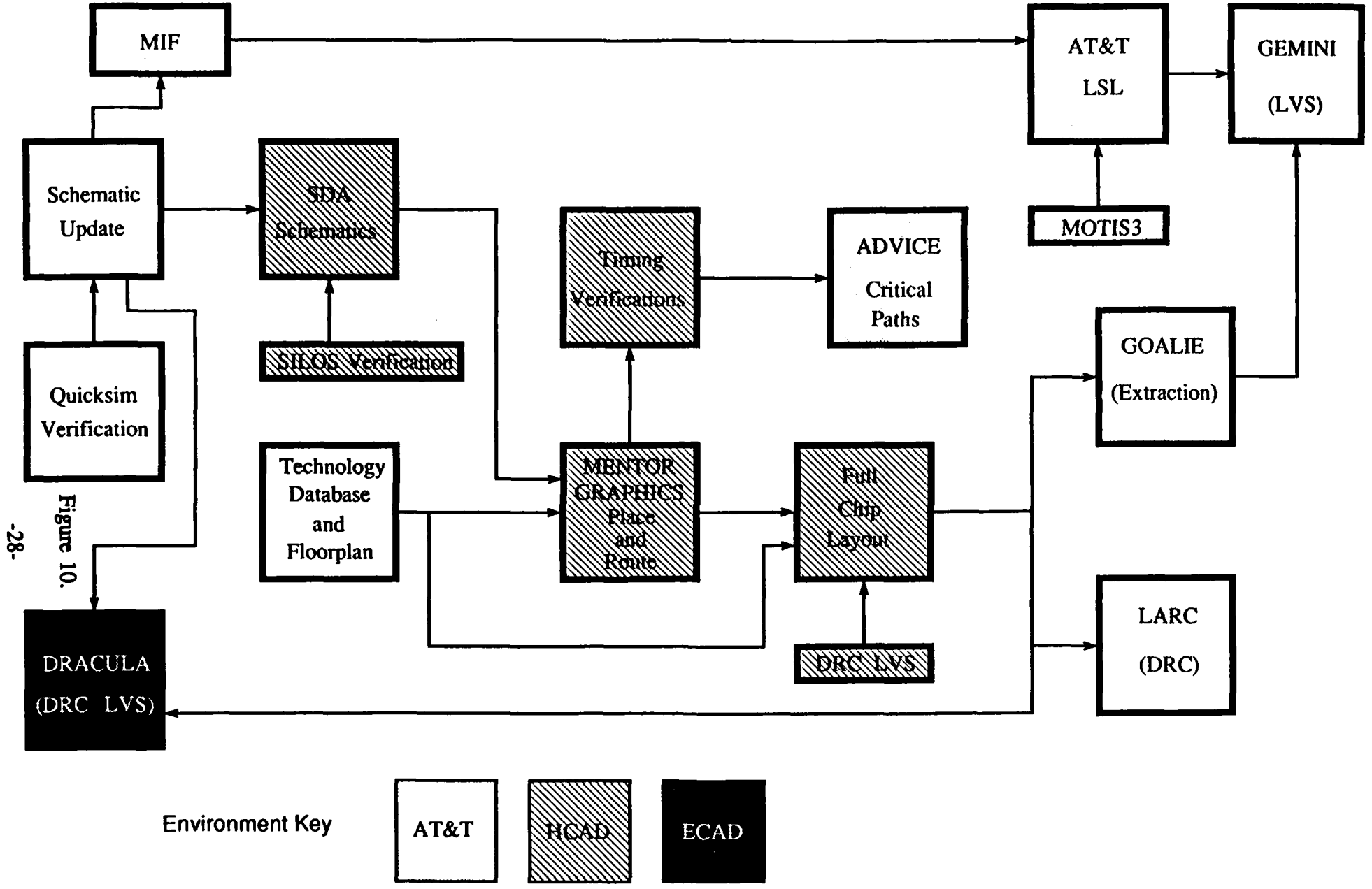
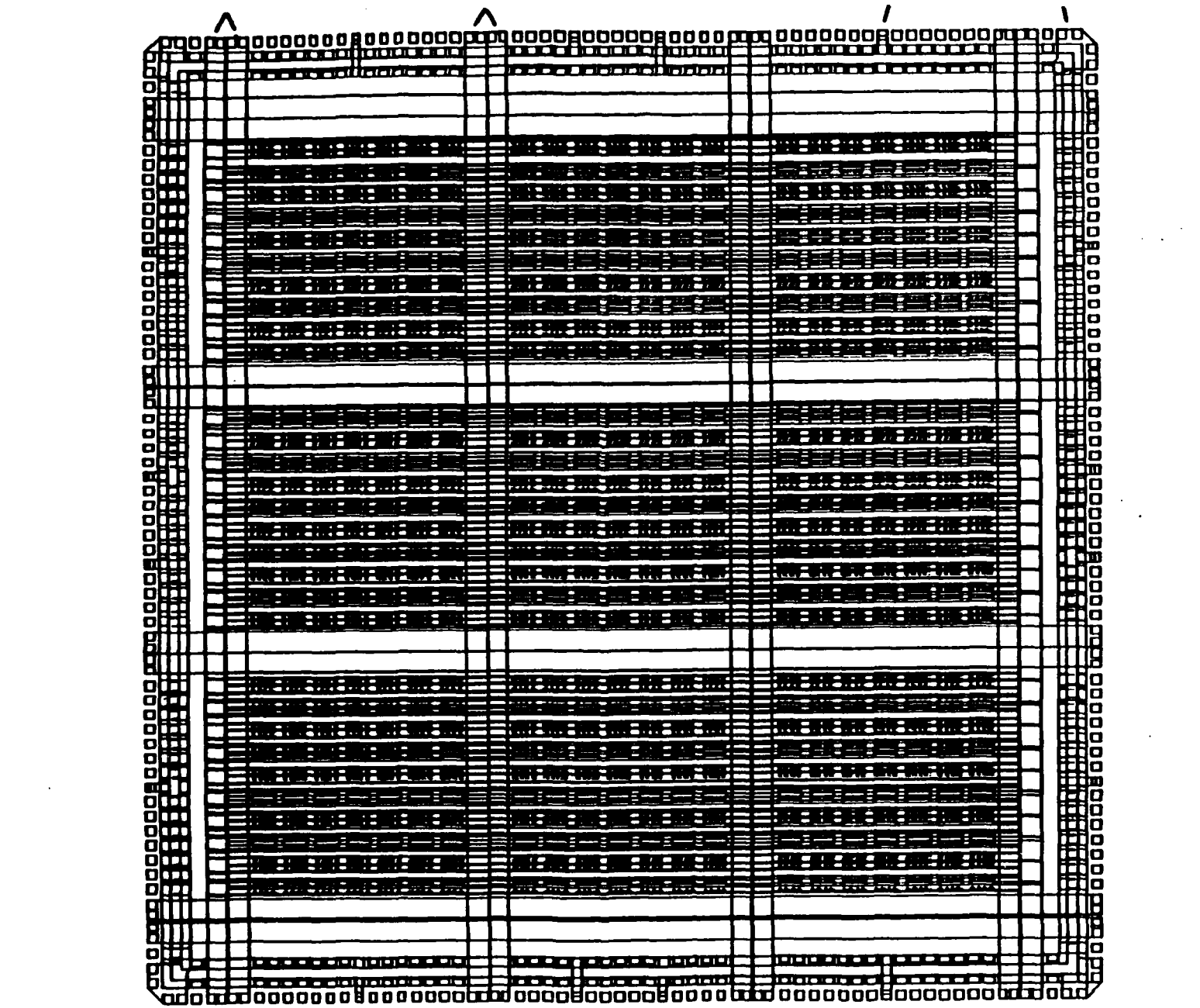


Figure 10.

Design Flow for 5K Cell Array Casino Test Chip



5K Casino Test Chip Cell Array Floorplan

Figure 11.

6 watts (based on the standard cell CTC), so all internal logic is supplied with separate power and ground connections. These connections (which are 250μm each) are brought directly out to the frame at 12 locations spaced evenly around the inner power ring. The I/O is fed by twenty 100μm power and ground leads spaced evenly around the frame.

4. PILOT PRODUCTION

4.1 MBE Process Status and Modified Process (J. M. Parsey Jr., C. L. Reynolds)

During the last six months, 489 wafers were grown for the DARPA program, and 319 of these were delivered to the processing line. Several equipment failures occurred, resulting in unscheduled maintenance work during this time. These were most likely related to heavy use of our MBE systems. For example, some of the failures included the CAR (substrate holder in the growth chamber) bearings, a leaking CAR feedthrough, failed heater clips, and the main growth chamber shutter.

As mentioned in the last report, daily doping calibrations were initiated using the Polaron Electrochemical C-V profiler; we have now tightened the specifications on doping levels from ±10% to ±5% with a predicted factor of two reduction in threshold voltage variation.

With the sustained improvement in threshold voltage control during the March to July time period, it was found that the threshold voltage needed to be centered better within the target window to obtain good circuit yield. The layer thicknesses were adjusted accordingly, and wafers were delivered to the processing line. On the basis of preliminary data, the threshold voltage has shifted in the appropriate direction.

Considerable effort was expended toward understanding device characteristics of FETs fabricated from wafers using the UV ozone MBE process. There is considerable reduction of sidegating due to removal of carbon at the substrate/epitaxy interface. It was found that the devices exhibited less abrupt pinch-off and excessive channel current due to the reduction in change compensation by carbon. SIMS analysis of numerous wafers revealed that in addition to carbon at the interface there is also a considerable amount of silicon contamination. Using the standard MBE process with a relatively high level of carbon, there is little impact on device characteristics from the Si. However, with the modified MBE process using the UV ozone clean, the presence of the silicon is predicted to have an impact on the threshold voltage. The source of the silicon contamination is under active investigation.

4.2 Pilot Line Throughput, Interval, and Yield (J. H. Duchynski, S. S. Patel)

In this semiannual period, 291 DARPA Pilot Line wafers were started. Two hundred thirty-eight wafers were completed and PCM tested in the same period. Starts were made in the baseline SARGIC technology for PT-1, PT-2L, PT-2M, Custom ALU, 1K Cell Array, Standard Cell ALU, Transversal Filter Chip (TFC), and in the advanced SARGIC technology for APT-2. Wafers were completed for both baseline and advanced SARGIC technology. Table 10 summarizes the starts and completions by reticle set for this reporting period.

Table 10 — Pilot Line Activity

Reticle Set	Wafers Started	Wafers Completed
PT-1	6	7
PT-2L	56	47
PT-2M	68	76
Custom ALU	62	41
1K Cell Array	52	36
Std. Cell ALU	12	0
TFC	6	0
APT-1	0	26
APT-2	29	5
	291	238

Good, fully-functional circuits have been realized on the Custom ALU and 1K Cell Array wafers which were started for the first time during this reporting period. Completed advanced technology wafers are being tested for circuit functionality and interconnect evaluation. Figure 12 shows the cumulative DARPA Pilot Line starts and completions up to September, 1989. Additional wafers were started for other AT&T projects in SARGIC as well as other technologies on the pilot line. Total cumulative starts up to September, 1989 in the Pilot Line were almost 2100 wafers (all starts) and more than 1000 wafers were completed for PCM testing. Wafer starts combined for all projects averaged 20 wafers/week for this period, down from 30 wafers/week for the last reporting period. Starts were lower due to unavailability of MBE wafers resulting from prolonged periods of MBE machine downtime in July, August and September.

Fabrication interval as shown in Figure 13 for the month of September, 1989 was 28 days, down from 40 days at the start of the reporting period. After a drop in April, the interval rose to about 36 days due to gate metal and SiON deposition equipment downtime in May and thermal annealing furnace downtime in July. Prove-in of the new tungsten silicide target in August also had a negative impact on interval time.

Figure 14 shows the wafer throughput or fabrication yield (wafers ready for PCM testing compared to wafers started in the fab line). Lower yields in May and June, 1989 were due to scrapping of four lots which were started as experimental lots for prove-in of a new MBE structure, and three lots which showed defects at EFET etch resulting from aluminum concentration problems during MBE growth. A drop in yield in August was due to scrapping two additional experimental lots with the new MBE structure.

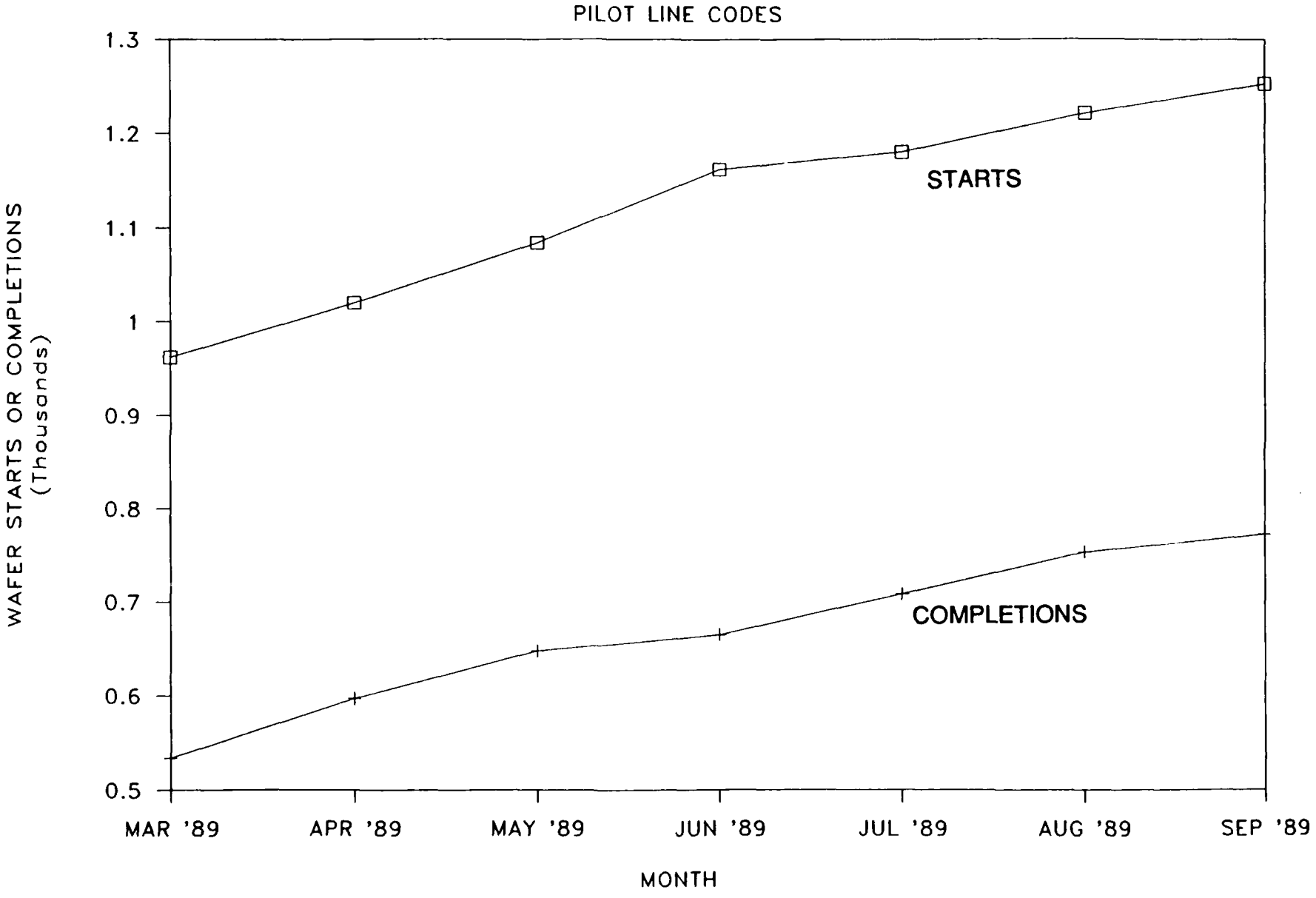
4.3 Baseline Technology, Threshold Control, and PCM and Circuit Yield (H-H Vuong, Y-C Shih)

Process Control

Since March 1989, the process control of the baseline technology has been improved significantly, as shown in Figure 15. For example, the standard deviation, σ, of the inter-wafer variation of the EFET Threshold Voltage (Vth) is reduced from 100 mV to 30 mV, and σ of DFET Vth is reduced from 160 mV to 100 mV. The improvements resulted from tighter control of key processes, many of which were identified by the focus team set up for this purpose. The key processes were:

Figure 12.

Pilot Line III Wafer Fab: Cumulative Starts and Completions



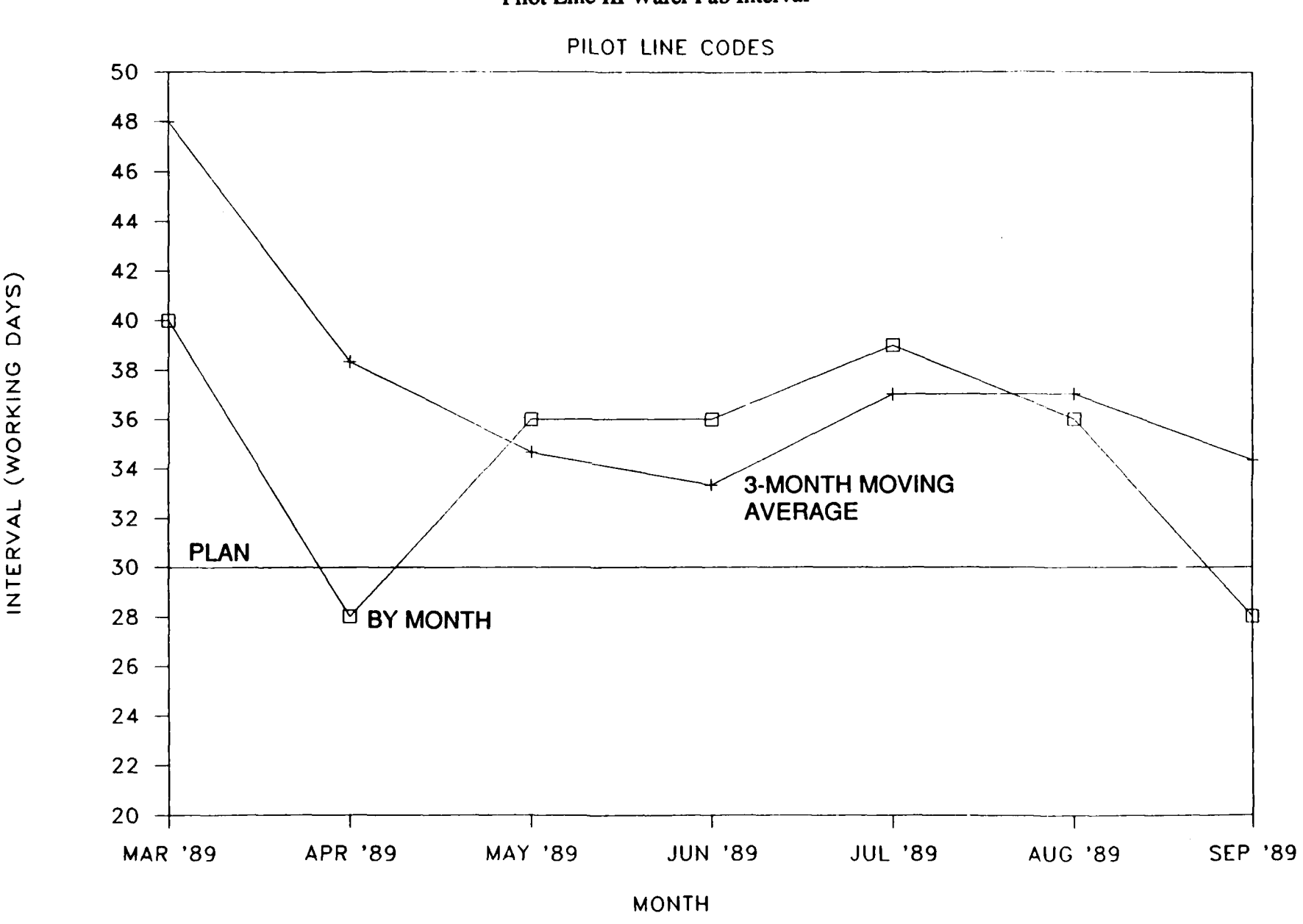
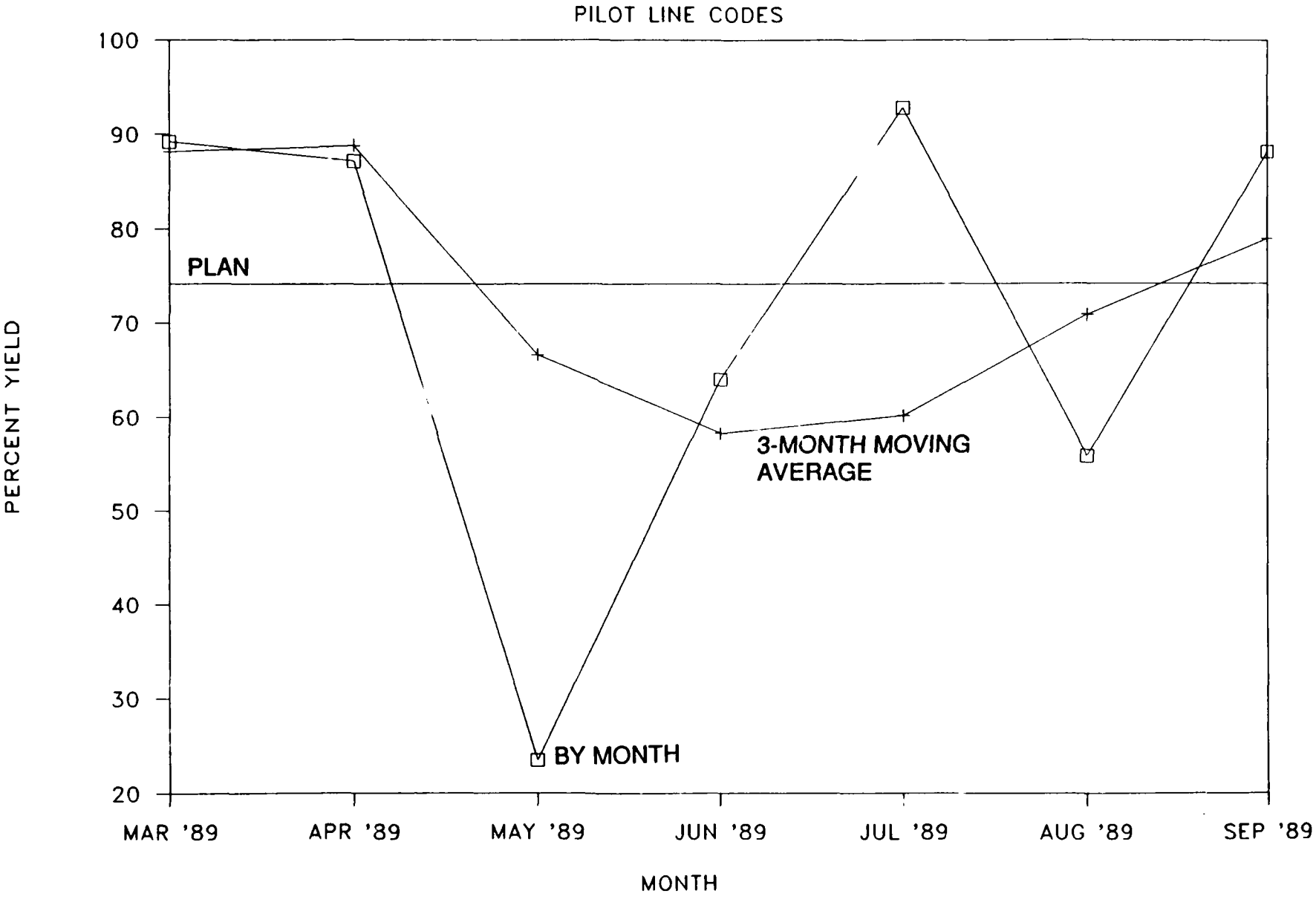

Pilot Line III Wafer Fab Interval
PILOT LINE CODES
INTERVAL (WORKING DAYS)
50
48
46
44
42
40
38
36
34
32
30
28
26
24
22
20
PLAN
BY MONTH
3-MONTH MOVING AVERAGE
MAR '89
APR '89
MAY '89
JUN '89
JUL '89
AUG '89
SEP '89
MONTH

Figure 13.

Figure 14.

Pilot Line III Wafer Fabrication Yield



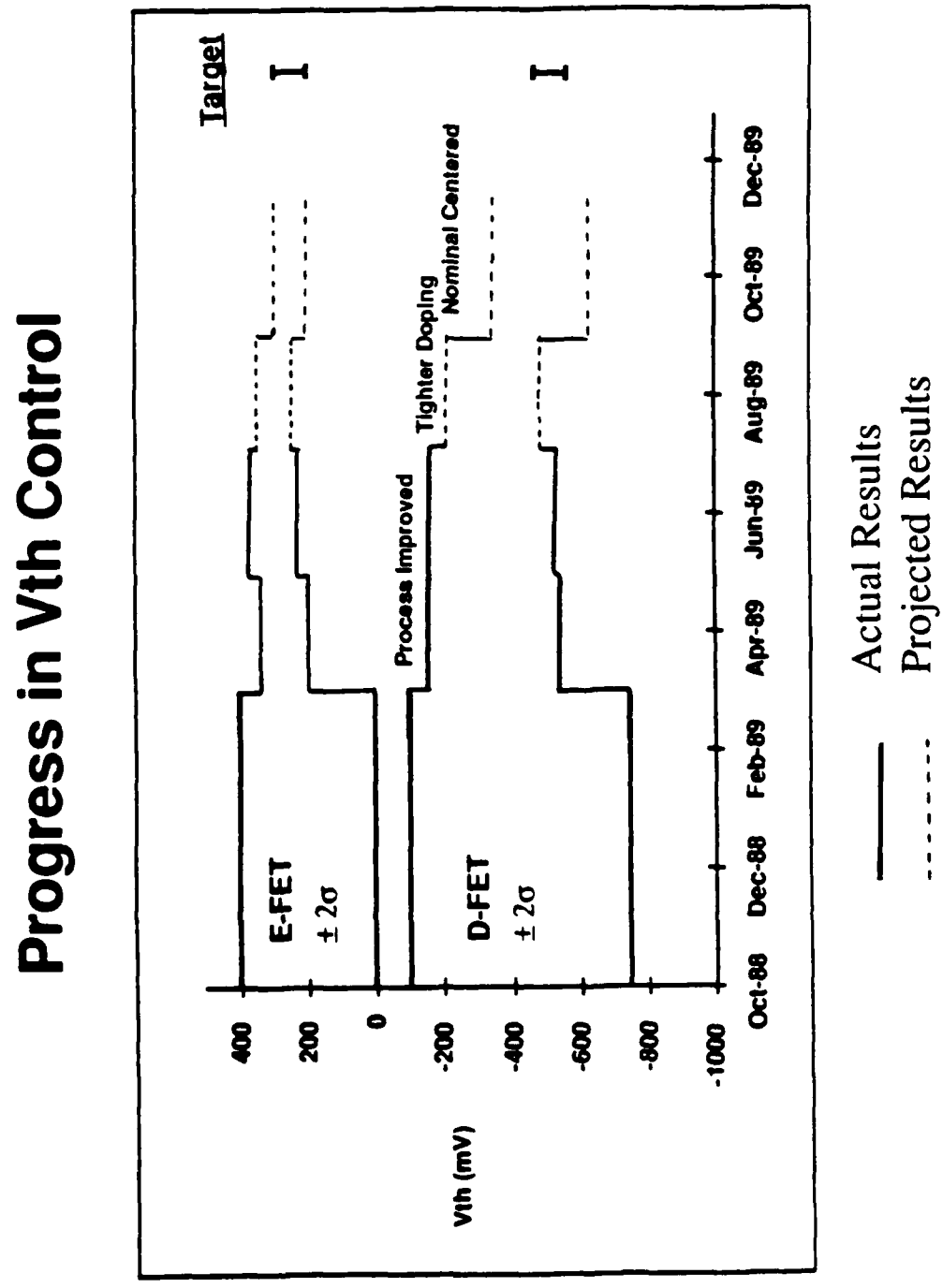

Progress in Vth Control
Target
E-FET
± 2σ
D-FET
± 2σ
Process Improved
Tighter Doping
Nominal Centered
Vth (mV)
400
200
0
-200
-400
-600
-800
-1000
Oct-88
Dec-88
Feb-89
Apr-89
Jun-89
Aug-89
Oct-89
Dec-89
Actual Results
Projected Results

Figure 15.

1. MBE growth, which has implemented daily calibration of layer thicknesses and doping, and which has stringent criteria based on these and other parameters for shipping wafers into the processing line.
2. Furnace anneal, where a dependence of Vth with wafer position in the furnace boat was identified and eliminated by avoidance of certain positions and by keeping a constant thermal mass during each run.
3. Gate metal deposition. It was found that the gate metal composition varied at the end of a gate target life, thereby introducing additional Vth variation. Daily calibration of the gate metal composition is now implemented.

In addition, the second isolation process has been proven-in under our change control procedure. It has been shown to be effective in reducing sidegating without introducing any negative side-effects. It has now been incorporated into the baseline process.

Finally, after the tighter control of the baseline process was established, it was determined that the average value of Vth was more positive than targeted. Therefore, we used our MBE model to calculate adjusted MBE layer thicknesses. The MBE structure was adjusted, and the results of the first few lots show Vth values close to target. This is indicated in Figure 14.

Circuit Yield

A correlation between the circuit yield and the Process Control Monitor (PCM) data was established. The figure of merit for the PCM is the fraction of the total PCM sites which is within the desired window. The desired window is defined as following:

$$65 < \text{D-Ids} < 105 \text{ mA/mm}$$
$$40 < \text{E-Ids} < 70 \text{ mA/mm}$$
$$4\text{K} < \text{R-via} < 20\text{K Ohm}$$

where Ids is the current measured on the standard DFETs and EFETs of the PCM, and Ids is proportional to Vth (the transconductance being nearly constant); and where R-via is the resistance of a chain of 4000 via hole connection, and is the figure of merit for the interconnect.

The wafers are ranked "good", "fair", or "poor" according to how many of the PCM sites measured have results within the above window for Ids and R-via values. As shown in Figure 16, the "good" wafers have the highest circuit yield (8% fully functional circuits in PT-2L and PT-2M wafers), followed by "fair" and "poor" wafers. Therefore, this ranking of the wafers is used to rank priority for primary circuit wafer probing. In addition, it shows unequivocally the importance of good process control to obtaining high circuit yield.

4.4 Program for D_0 Analysis and Reduction (C. H. Tzinis, P. F. Sciortino)

In this period, we formalized a D_0 identification program consisting of two parts: (a) investigation of defects during the wafer fabrication process (with no active feedback from testing results) and (b) investigation of defects identified from active feedback after the wafers have been tested. The D_0 program has been facilitated by the recent high yield PT-2M wafers - as well as PT-2L, custom ALU and 1K Cell Array mask sets - although the relatively small size of the 256 bit memory increases the density and therefore the amount of information that can be analyzed per unit area.

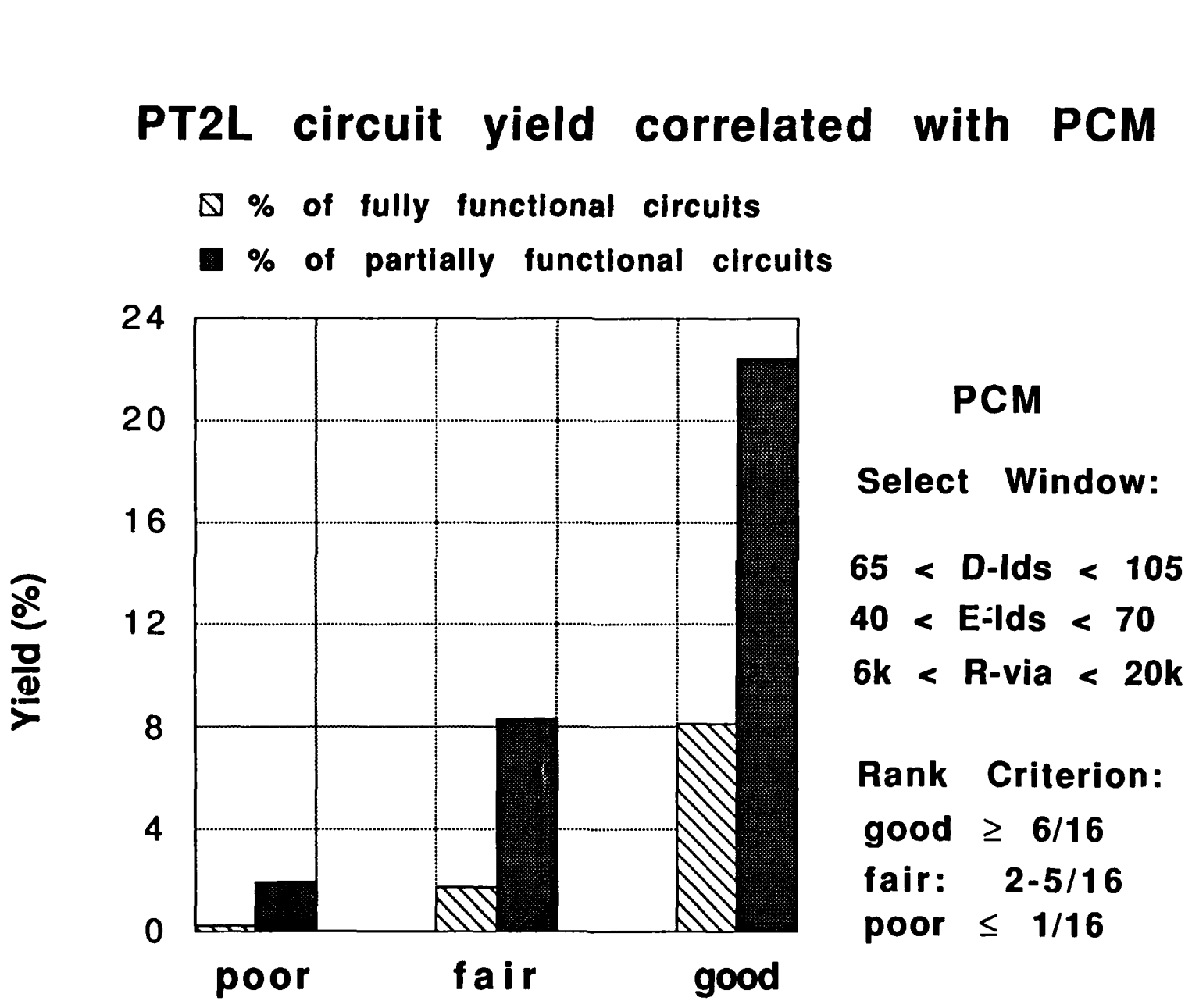

PT2L circuit yield correlated with PCM
% of fully functional circuits
% of partially functional circuits
24
20
16
12
8
4
0
Yield (%)
poor
fair
good
PCM
Select Window:
65 < D-Ids < 105
40 < E-Ids < 70
6k < R-via < 20k
Rank Criterion:
good ≥ 6/16
fair: 2-5/16
poor ≤ 1/16

Figure 16.

As Table 11 shows, fourteen possible individual mechanisms have been identified from optical (50 - 1000X) and limited SEM inspections during the course of wafer fabrication at the four metal levels.

Table 11 — Visual Analysis Catalogue (D_0)

Description	Process observed	Process impacted	Comment
Oval defect	Start	All	Random
Spots	Start	All	Edge + 15mm
Dirt particle	All	All	Random
Scratch	All	All	Random
E-tub particle	E-tub etch	Gate,Ohmic	Megasonic
E-tub defect	E-tub etch	Gate,Ohmic	Material
WSi ring	WSi RIE etch	Gate,Ohmic	Sputter clean
Anneal particle	N^+, O_2 anneal	Gate, E-tub	Furnace
Metal missing	Gmt,Omt,Bmt,Tmt	Gmt,Omt,Bmt,Tmt	Lift-off
Metal burrs	Omt,Bmt,Tmt	Omt,Bmt,Tmt	Lift-off
Metal short	Gmt,Omt,Bmt,Tmt	Gmt,Omt,Bmt,Tmt	RIE, Lift-off
Diel. particle	Via1, Via2, Passiv.	Gmt,Omt,Bmt,Tmt	Deposition, RIE
Diel. bubble	Via1, Via2, Passiv.	Omt,Bmt,Tmt	Deposition, RIE
Via connection	Via1, Via2	Gmt,Omt,Bmt,Tmt	Resist, RIE

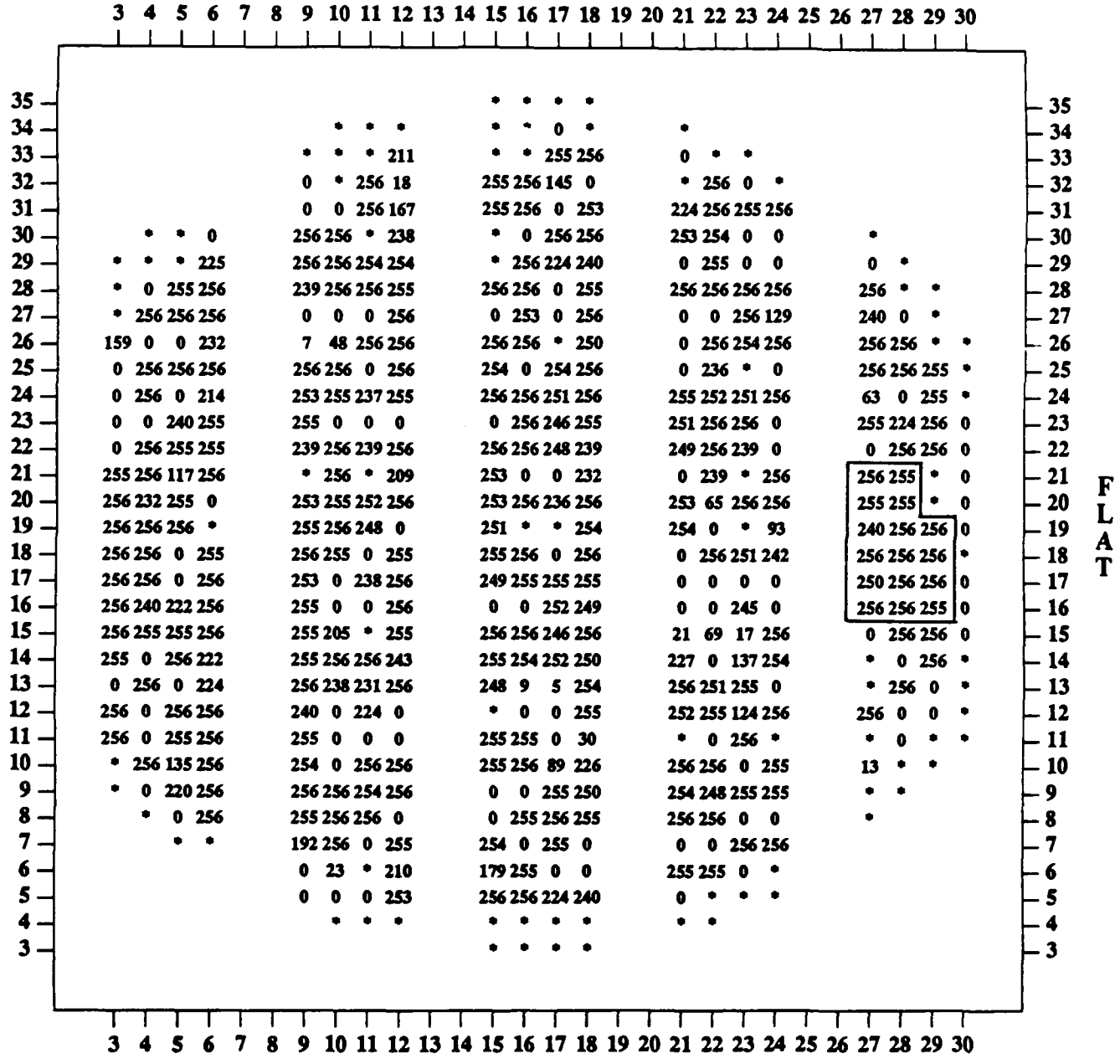
Gmt,Omt,Bmt,Tmt: Gate, Ohmic, Bottom, Top metal levels
RIE: Reactive ion etching
Diel.: Dielectric

After the classification was completed, extensive documentation (including photos, description and drawings) was made available to the manufacturing line personnel for training, data collection, cause-and-effect analysis, and corrective action. Analysis of the data led us to concentrate on the four areas most likely to respond to our efforts to reduce D_0:

Defect mechanism	Source	Action
WSi rings	Sputtering equipment	Rigorous cleaning schedule
Spots	Pre MBE cleaning	Improve cleaning procedure
Scratches	Batch processing	Separate wafers
Top metal missing	Lift-off equipment	Adjustment of spray pressure

In parallel with the wafer inspection program, a separate effort compares testing results (presented as wafer maps) with visual (and limited SEM) inspection to identify defects that give rise to reduced performance. This effort has been made possible having the PT-2M test results (bit maps plus wafer maps) available in an accessible computer database. Of special interest are dice with most bits working in the neighborhood of devices with all 256 bits working (see Figure 17). Such sites have correct parametrics, and D_0 defects are responsible for the reduced performance. Inspection of all 543 sites showed that (a) within the area containing working circuits, WSi rings (defects caused by WSi particles at gate metal sputtering) were responsible for almost half (46%) of the non-working dice and (b) several dice with WSi rings had 256 bits working. We expect that benign defects are actually in the non-active regions of the circuits; then the fraction of defects that are benign should equal the

Map of Wafer 32881



Map of Good Bits

543 Total Die 451 Values 173.557 Mean 114.140 σ

Figure 17.

fraction of device area that is non-active. The experimental observations compare very favorably to this model (38% of defects are benign, and 40% of the area is non-active).

4.5 Advanced Technology and Test Circuits (A. G. Baca, R. J. Niescier)

The advanced technology objective is to provide demonstration circuits which achieve system performance equivalent to 400 MHz clock rates with 15-20 gate delays in the critical path. Yields of 3% will be shown to be achievable for 3-5 K gate complexity circuits. Power dissipation is to be comparable to that of the 200 MHz baseline technology circuits.

The current plan is shown in Figure 18. In order to accelerate the schedule, we processed the initial APT-1 lots (4) and APT-2 lots (1) with liftoff TiPtAu metallization. (The Al process was not available immediately after circuit design completions.) The interconnect yield was lower, but we achieved our objective of obtaining early feedback of the ring oscillator delays. Reliability studies for the Al metallization samples is commencing with approximately one month slip. It is anticipated that 500 Hrs of thermal aging (under bias) data will be available for the end of the year report.

The APT-1 and APT-2 masksets, which have been described previously, are the vehicles to prove-in the advanced technology. A total of 6 lots of APT-1 and 4 lots of APT-2 are being processed. Four of the APT-1 lots and one APT-2 lot have been completed. Wafer screen methodology developed for the baseline technology has been applied to the APT lots. Two of the APT-1 lots failed the wafer screen due to interconnect failures. Of the remaining two lots, three wafers are rated good by the PCM screen and three wafers are rated fair. These six wafers provided the working ring oscillator circuits. The APT-2 lot contained 2 wafers rated fair and three wafers rated poor. Testing has just commenced on the APT-2 lot.

FETs with 0.75μm gates exhibit greater intra-wafer variation than 1.0μm FETs of the baseline technology (approximately 90 vs. 25 mV standard deviation for the EFET). Inter-wafer variation is expected to be about the same in both technologies, but not enough wafers in the advanced technology have been processed to establish this.

APT-1 ring oscillators contain 38 sites for logic family comparisons of the improved version of SFFL, called low-power source follower logic (L-SFL), and DCFL. Thirty three of the sites have been shown to be functional. Two sites have layout errors. No failure cause has been determined for the remaining three nonfunctional sites. Unloaded ring oscillator delays have been compared for various 3-input NOR gates from APT-1 and PT-1 and are shown in Figure 19. The shrunken design rules provide a modest improvement in propagation delay times, and indicate that the 400 MHz specification can be reached. Sites with 200 and 500μm of wire loading, different fan outs, and space saving layout approaches are currently being analyzed.

An important milestone has been reached in demonstrating functional circuits with the 1.5μm design rules. These ring oscillators circuits provide the means to define and optimize the advanced technology.

4.6 Advanced Technology: Process Development (R. J. Shul, A.G. Baca)

Aluminum interconnects have been introduced into the SARGIC technology to reduce design rules and defect densities. Al is superior to the TiPtAu currently in use because subtractive patterning of the Al results in better definition of the metal lines and fewer shorts compared to the liftoff patterning of TiPtAu, especially with smaller design rules. In addition, sputtered Al provides better coverage into small via holes than evaporated TiPtAu and therefore fewer opens. Development has focused on reactive ion etch of Al, a diffusion barrier to prevent interaction of Al and Au based ohmic contacts, and prevention of corrosion of Al.

Advanced Technology Development: Current Plan

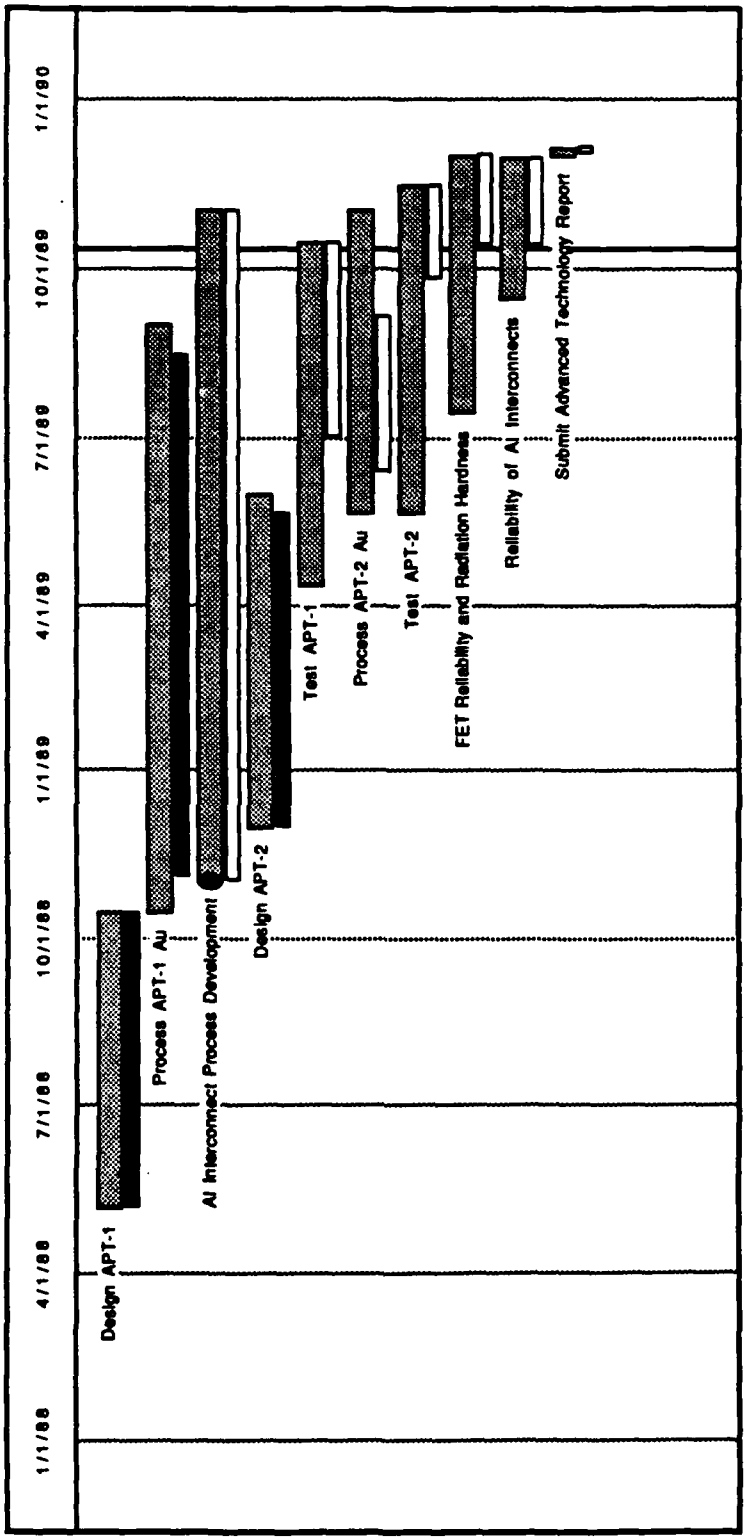


Figure 18.

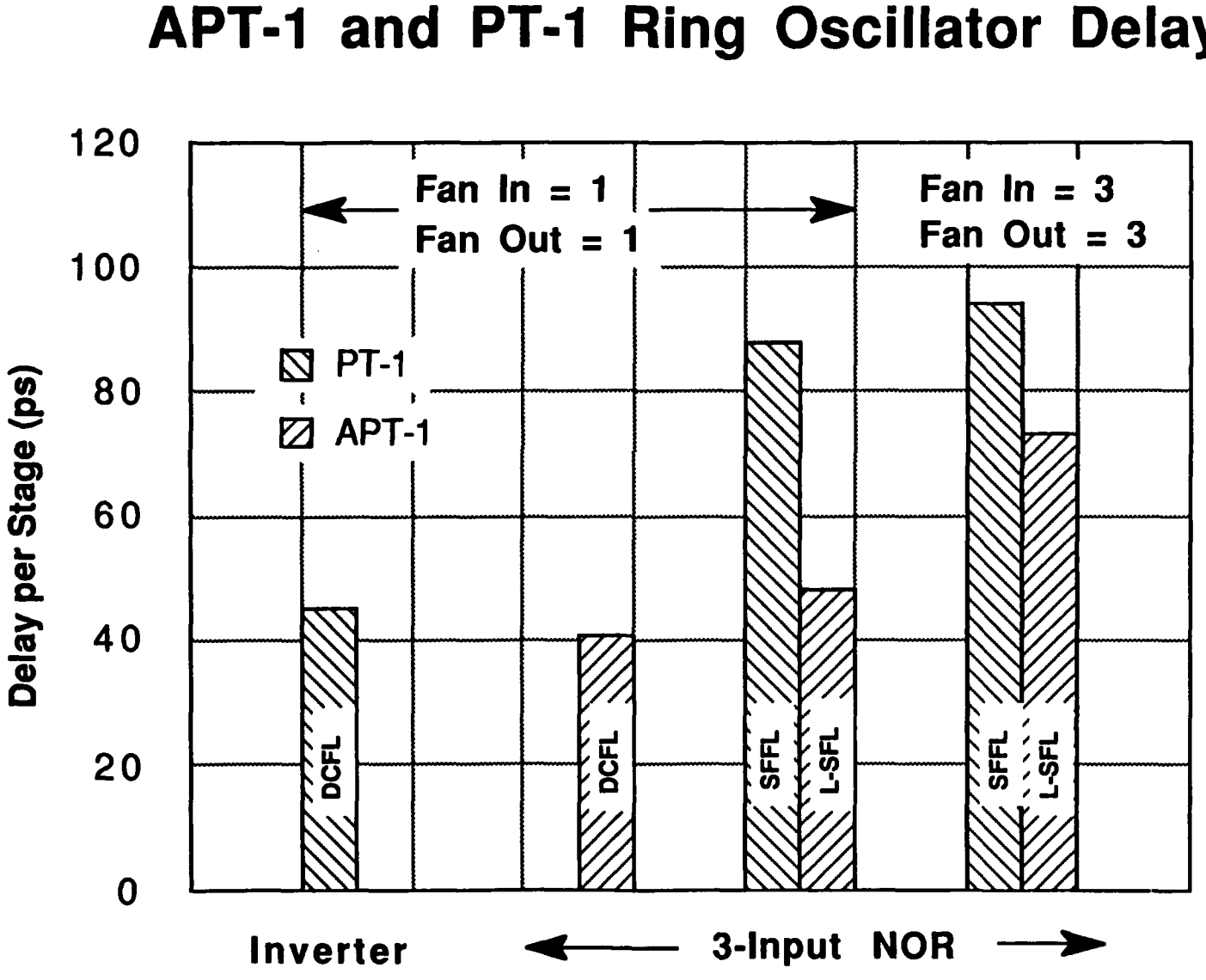

APT-1 and PT-1 Ring Oscillator Delays
120
100
80
60
40
20
0
Delay per Stage (ps)
Fan In = 1
Fan Out = 1
Fan In = 3
Fan Out = 3
PT-1
APT-1
DCFL
DCFL
SFFL
L-SFL
SFFL
L-SFL
Inverter
3-Input NOR

Figure 19.

A uniform, reproducible, anisotropic etch has been developed for Al in a chlorine based plasma. Al interconnects often corrode following a Cl etch due to the formation of a Cl containing reaction product, $AlCl_3$. When $AlCl_3$ is in the presence of H_20, $Al(OH)_3$ and HCl products form, promoting corrosion. A post-etch passivation consisting of a fluorine plasma and water rinse is used to prevent Al corrosion. F exchanges with Cl forming non volatile AlF_3. The water rinse is added to remove any remaining Cl. However, a water rinse makes Al susceptible to dislocations or "mouse bites," where Al sections are missing from patterned lines. This is prevented by adjusting the pH of the water so it is slightly acidic or basic.

Al stringers were identified in early work due to the concave profile of gate metal. Deposition of dielectric overgate metal results in a cusp or trench in which Al is deposited. Due to the anisotropic nature of the etch, the Al is extremely difficult to remove from the cusp. A sidewall for the gate has been developed to smooth out the dielectric profile and eliminate the Al stringers. A similar sidewall process is presently being integrated into bottom metal Al.

Deposition of Al directly over Au-based ohmic contacts may form highly resistive Al/Au intermetallics (purple plague). A conductive diffusion barrier, WSi, is therefore deposited between the Al and Au (see Figure 20). Preliminary thermal aging studies of the WSi diffusion barrier have shown no degradation in resistance for 250,000 vias in series.

The PT-Y maskset has been completed and used to evaluate the Al process. Via testers with 250,000 vias in series show approximately 96% yield on the initial lots processed. These results characterize the current capabilities of the 1.0μm via etch process in conjunction with the 1.5μm Al process. The initial TiPtAu lots using 2.0μm design rules show a 75% yield for testers with 181,500 vias in series.

In conclusion, the Al process is near completion and awaits the integration of the bottom metal sidewall process. Reliability studies for electromigration and the Al/Au barrier with bias and thermal aging is under way with results expected by the end of the 1989. Several lots of APT-1 and APT-2 are being processed with Al interconnects.

4.7 Package Choices, Fixturing, and Thermal Analysis (D. E. Miller, R. S. Moyer)

The most recent package/circuit assignment summary appears in Table 12. A detailed discussion follows.

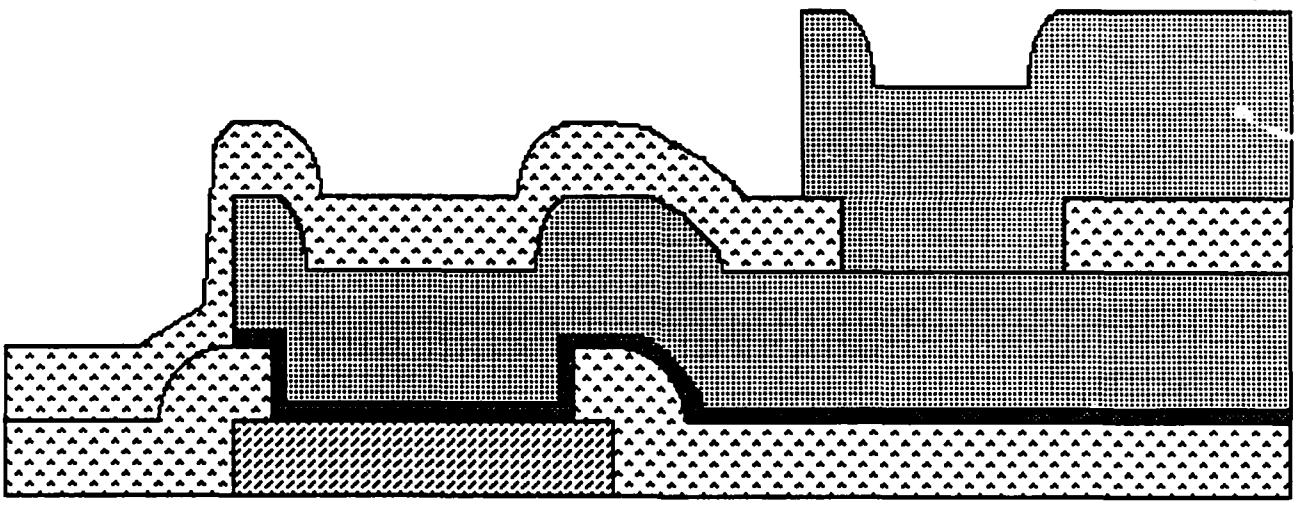
Assembly and Handling

PT-2M: TriQuint MLC-44 Package — We are continuing to assemble PT-2M circuits in the TriQuint MLC-44 package. Some are deliverable devices, but most are for reliability studies. The latter application requires a hermetic lid seal on the package. Tooling is being fabricated to perform this operation in a controlled ambient.

PT-2L, 1K Cell Array, 4K SRAM: Interamics 64/88 Package — PT-2L circuits have been assembled in this package. The 1K-Cell Array circuits will be packaged during the first week of October, 1989. A packaging plan for the 4K-SRAM has been generated for approval. All of these circuits are well matched to the package in die size and I/O location.

A difficulty with deformed package leads was encountered during PT-2L testing. The package leads are very fine pitch and easily deformed. Any amount of deformation results in misalignments between test fixture and package, and difficulty in maintaining good connections. A plastic carrier, developed in anticipation of a need for burn-in sockets, has

Diffusion Barrier (WSi) Used with Aluminum Interconnects



Aluminum

Barrier

SiON 4000 Å

Ohmic contact or Gate tab

Figure 20

DARPA PILOT LINE III
PACKAGE-CIRCUIT ASSIGNMENT SUMMARY

Package Cost @ 100 Quantity	Pitch Z_0	Signal Leads Total Leads	Cavity Size Max Die Size	High Speed Fixture Available	Burn-in Sockets Available	Circuit Reticle Date	Die Size	Signal Count Total I/O	Packages Required for RAD HARD Testing	Packages Required for REL. Testing
Tri-Quint PK-MLC-44-S $65	.050" 50Ω	24 44	.130" SQ .090" SQ	Yes TriQuint	Yes JEDEC	PT-1 11/87 PT-2M 10/88	.060" SQ .080" SQ	24 44 16 44	40	275 for 256 Bit SRAM
Interamics 64/88 $170	.020" 50Ω	64 88	.250" SQ .210" SQ	Yes In House	2/89 Azimuth Elect.	PT-2L 6/88 4K SRAM 9/89 1K Cell Array 4/89	.204" SQ .216" SQ .212" SQ	64 88 36 88 64 88	60	275 for 4K SRAM
TriQuint PK-MLC 196-S $180	.025" 50Ω	128 196	.430" SQ .390" SQ	Yes TriQuint	6/89 Yes	Transversal Filter Chip 9/89 Custom ALU 3/89 Standard Cell ALU 8/89 32 Bit Floating Point Multiplier 12/89	.360" SQ .292" SQ .292"SQ .360"x.380"	105 173 120 168 120 168 110 160	40	
NTK/256 pin $50	.020" 58-60Ω	224 256	.560"SQ .520"SQ	No	Yes Yamaichi	Cell Array Casino Test Chip 12/89	.462"SQ	172 236		

Table 12.

been ordered. The plastic carrier protects the leads during shipping and can be used to straighten package leads.

Custom ALU, Standard Cell ALU, Standard Cell Transversal Filter Chip, Custom Floating Point Multiplier: TriQuint MLC-196 — Four circuits are targeted for assembly in this package. The Custom ALU was the first to be assembled. Wire bonding is congested. The small die size relative to the package cavity results in long bond wires. The chip I/O design does not exactly match that of the package which results in some wires crossing over others. Some of this has been reduced by bonding chip VSS pads directly to the package floor.

Wire bonding for the Transversal Filter Chip and Floating Point Multiplier will be less of a problem because the dice are larger and I/O patterns for these chips are better matched to the package.

Cell Array Casino Test Chip: NTK 256 Package — Early in this program, we determined that the large die and high pin count of this circuit are beyond the capabilities existing in the industry, and no high speed packages have been developed for this application. Estimates from TriQuint and AT&T show that $50K and four months would be required to develop a package and test fixture. Considerable uncertainty exists as to the electrical and mechanical performance of such a test fixture.

Therefore, we will use the same package as we used for the standard cell Casino Test Chip. This 256 pin package was developed by AT&T for internal use. Low speed (~40 MHz) testing can be performed using a burn-in socket also developed by AT&T. Wire bonding and assembly are being examined for this circuit/package combination.

Mechanical Improvements to High Speed Test Fixtures

While electrical performance of the TriQuint high speed test fixtures meets this program's requirements, the mechanical performance could be improved. Inadequacies have been experienced during package testing. The difficulties are in loading the package into the test fixture and in maintaining contact between the package and fixture during multi-temperature testing. Improvements to the package clamping mechanisms are being made. The initial changes have provided improvement, and the effort is continuing.

Heat Transfer Analysis

A one dimensional heat transfer analysis has been applied to two packaged circuits, the 4K-SRAM and the Floating Point Multiplier. Thermal resistance, θ_{jc}, was calculated between the die surface and the package case. This heat transfer is conductive and is a function of power dissipation, chip area and material thermal properties. The calculated temperature difference from die surface to case, ΔT_{jc}, for the 4K-SRAM is 22°C. For the Floating Point Multiplier, ΔT_{jc} is 10°C. This represents only one component of heat transfer which influences junction temperature. Because of these significant temperature rises, packaged device testing is done with controlled package case temperatures.

5. RELIABILITY AND QUALITY

5.1 Radiation Hardness Testing (S. B. Witmer)

Transient ionizing dose measurements were made on standard and radiation hardened (rad hard) PT-2M SRAM testers. An upset threshold of about $1x10^{10}$rad(GaAs)/sec was obtained on the rad hard design and $5x10^{9}$rad(GaAs)/sec was obtained on the standard design (see Figure 21). The accessed row of the memory cells was more sensitive to upset than the unaccessed rows.

Initial SEU measurements were also made on standard and rad hard SRAM testers. Testing was performed at the Naval Research Laboratory (Washington, DC) using the pellitron accelerator, at AT&T using an ^{241}Am alpha source, and at NOSC (San Diego, CA) using the e-beam method. Similar to the transient dose results, increased sensitivity was also observed for the accessed row (see Figure 22). Additional SEU testing using the SRAM testers is planned for November using the Brookhaven heavy ion source.

The computer hardware and software for performing transient ionizing dose testing of the full-size, full-custom ALU circuit has been completed.

5.2 Reliability Testing (P. F. Thompson)

Reliability activities occurred in four areas this reporting period: thermal aging of aluminum vias, thermal aging of Ta_2N resistors, PT-2M HTOB (high temperature operating bias), and accelerated electromigration testing in support of the advanced technology.

Two via chain test wafers were aged 1000 hours at 200°C in air to determine the thermal stability of Via1 structures. Test wafers contained 15-20 structures, each consisting of 250,000 vias connecting ohmic metal to first level metal. Wafers used in this experiment contained the normal gold-based ohmic metal structure, with an additional 1000Å WSi layer deposited in situ with the ohmic structure. After deposition, lift off was performed on the ohmic-WSi structure. Then bottom metal (1000Å WSi, 8000Å Al) was deposited, patterned and etched. 4000Å of dielectric (SiON) was applied to one wafer, while the second wafer received no dielectric.

Median resistance versus time for the passivated and unpassivated wafers is shown in Figure 23. Both wafers behaved similarly, displaying resistance that decreased at a decreasing rate throughout the aging. The resistance values for both wafers show an exponential decay, plus a small linear decay. No thermally-induced failure mechanisms were apparent, and there was no measurable difference in the performance of the passivated and unpassivated wafer.

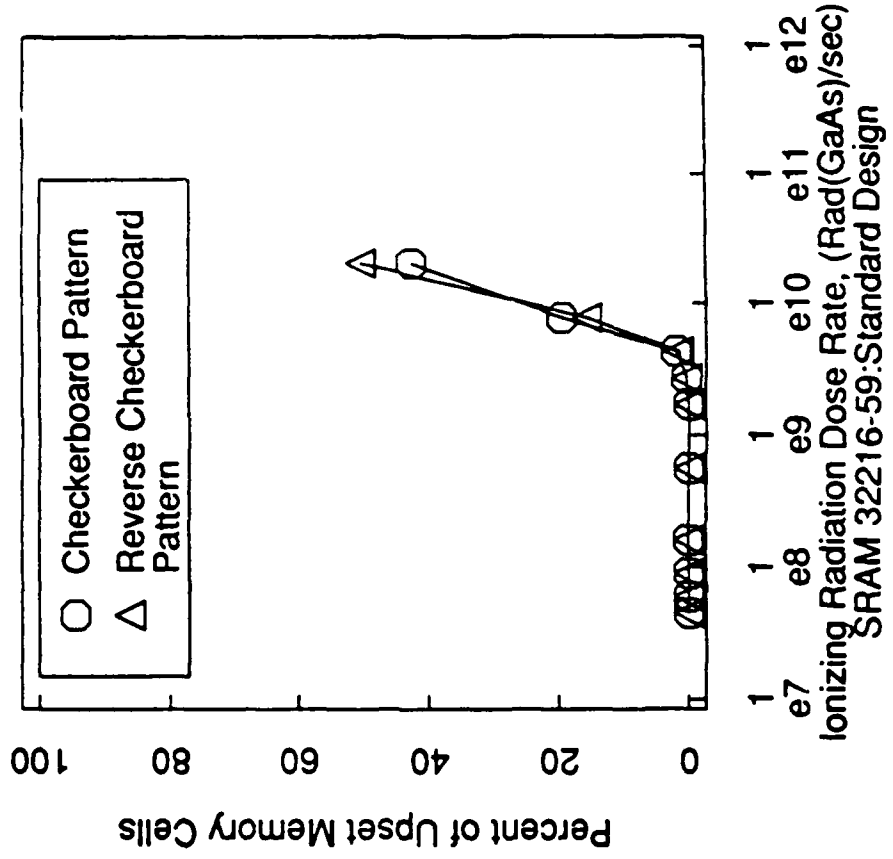
A 1000 hour thermal age study on Ta_2N resistor test structures is currently in progress. Seven wafers are being aged at temperatures from 135°C to 200°C. At the 500 hour test, all wafers showed no change in resistance, within the one percent accuracy of the test equipment. The study will be complete by October 12.

Preparations for PT-2M HTOB continued through this reporting period. All boards and fixtures are completed, and test software is written. System verification will be complete by October 12, prior to sample availability.

Preparations are also underway for accelerated electromigration testing of gold and aluminum metals and via structures. Preparation is scheduled to be completed by October 19.

5.3 Process Control Implementation Update (J. E. Brew, J. M. Mattei)

The Pilot Line III quality program continues to move forward as procedures for calculating Cp and Cpk (process capability) indices are implemented for parameters under statistical control. These indices are used to monitor the process capability with respect to the engineering or


Percent of Upset Memory Cells
0
20
40
60
80
100
Checkerboard Pattern
Reverse Checkerboard Pattern
1 e7 1 e8 1 e9 1 e10 1 e11 1 e12
Ionizing Radiation Dose Rate, (Rad(GaAs)/sec)
SRAM 32216-59:Standard Design

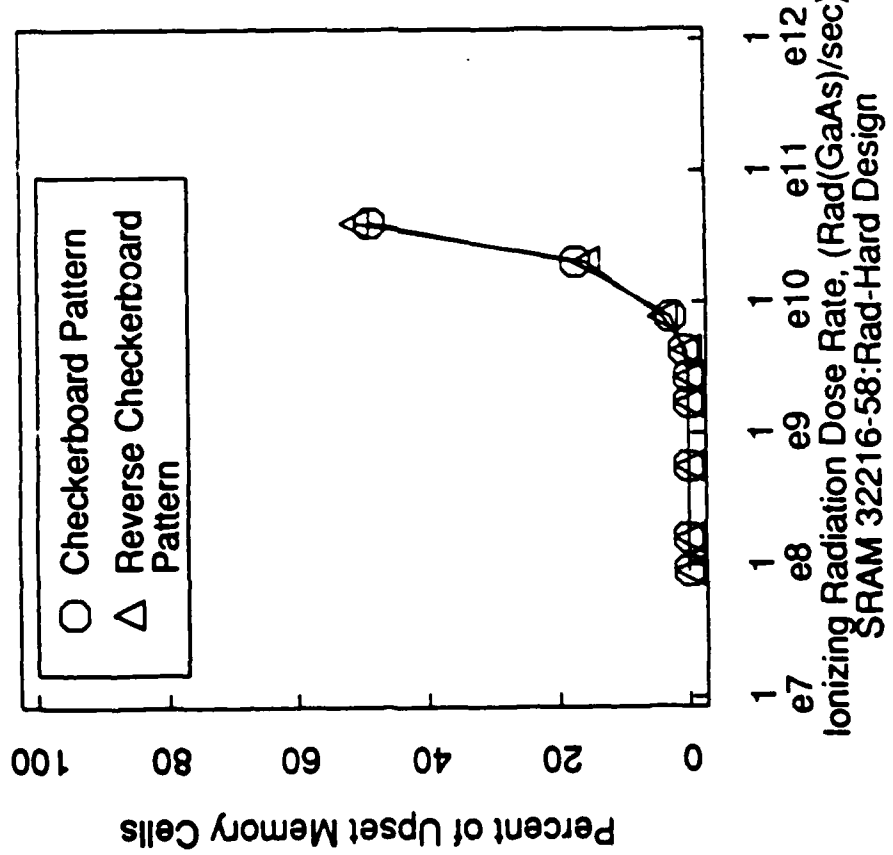
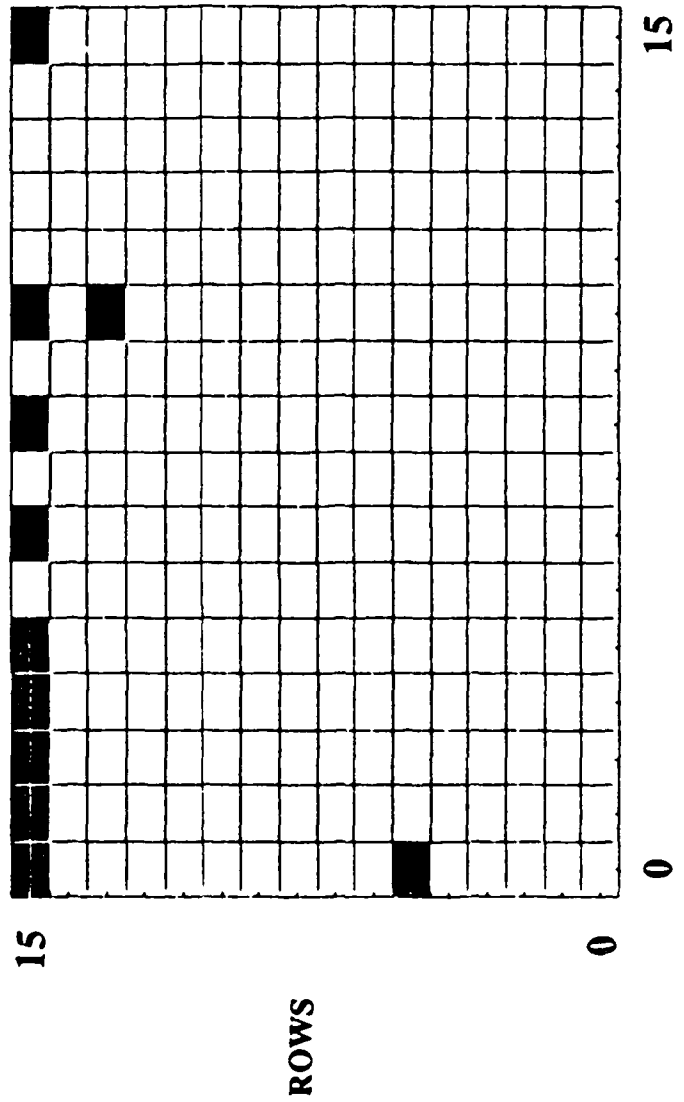

Percent of Upset Memory Cells
0
20
40
60
80
100
Checkerboard Pattern
Reverse Checkerboard Pattern
1 e7 1 e8 1 e9 1 e10 1 e11 1 e12
Ionizing Radiation Dose Rate, (Rad(GaAs)/sec)
SRAM 32216-58:Rad-Hard Design

Figure 21.

SEU Test Results on PT-2M SRAM: ^{241}Am Alpha Particles



Bit map of 256 bit PT2 SRAM (Rad. Hard Design) after 12 hr. of alpha irradiation ($\approx 1.6 \times 10^8$ particles/cm^2) from a ^{241}Am source. Row 15 is the accessed row and is more sensitive than the unaccessed rows.

Figure 22.

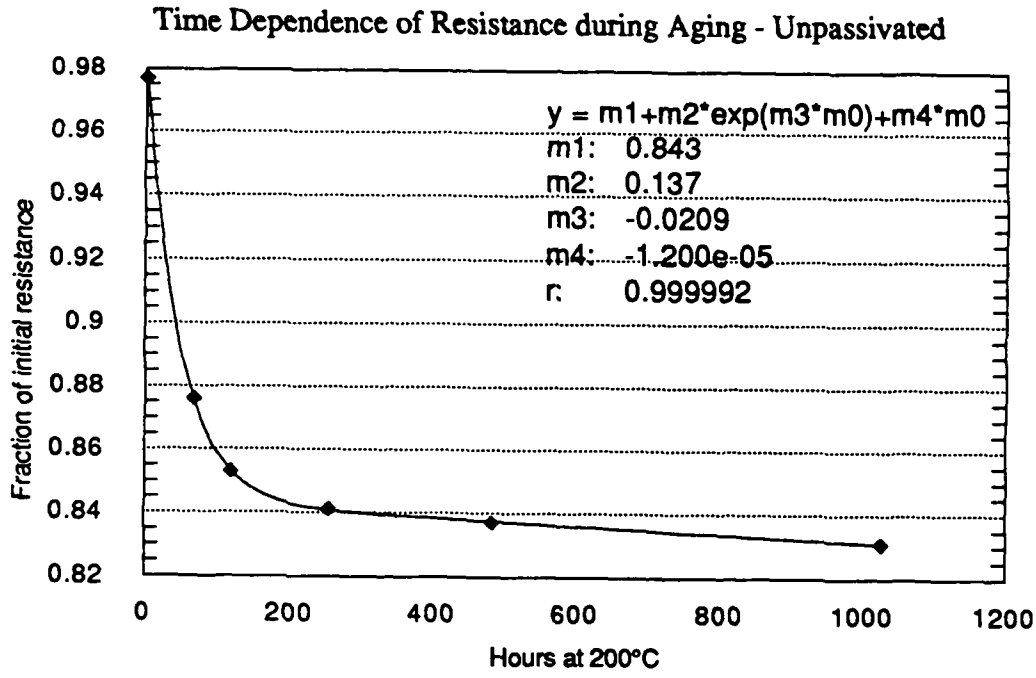


Figure 23a.

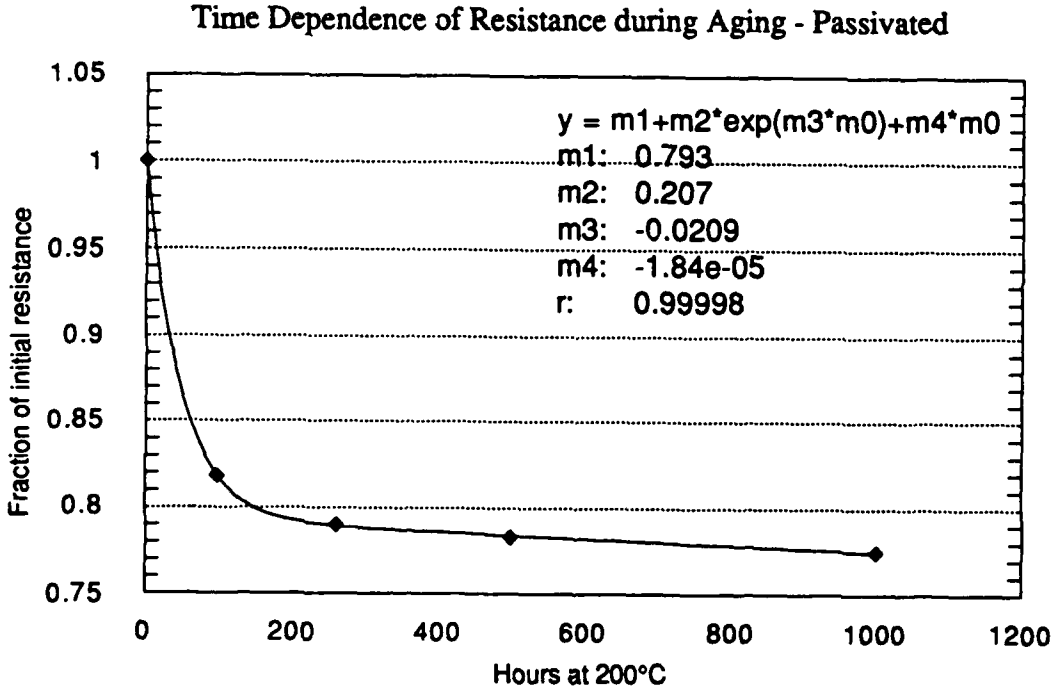


Figure 23b.

specification limits. Cp measures the range of the process variations compared to the range of the engineering or specification limits. Cpk is similar to Cp, but Cpk additionally measures how well the process is centered within the limits.

Efforts continue to get 100% of the control charts from engineering limits to statistical process control (SPC) limits. Currently, 44 control charts or 60% of the charts are under statistical process control. Table 13 illustrates the progress of the transition from engineering limits to statistical process control limits.

A reporting system for statistical control charts has been implemented. Weekly reports define the percent of control charts utilized, the total points plotted, the percent of control charts utilized that were in control, and the percent of points plotted that were in control. The attached graph illustrates the percent of points plotted on a weekly basis that were in control (see Figure 24).

GaAs WAFER FABRICATION AND DEVELOPMENT
STATISTICAL PROCESS CONTROL CHART STATUS
DARPA

AREA	TOTAL NO. OF CHARTS	SPC LIMITS	SHOP CONTROL CHARTS
MATERIALS (MBE)	19	14	14
PHOTORESIST	7	7	7
DIELECTRIC	8	7	7
METALLIZATION	10	7	7
WAFER PROBE	18	8	0
MEAS. STANDARDS	9	8	8
CLEANROOM	2	1	1
	73	52	44

STATISTICAL PROCESS CONTROL CHART PROGRESS

TIME FRAME	TOTAL NO. OF CHARTS	SPC LIMITS	SHOP CONTROL CHARTS
OCT.'88 - DEC.'88	56	46%	2%
JAN.'89 - APR.'89	68	60%	49%
MAY '89 - AUG.'89	67	73%	61%
SEPT '89-	73	71%	60%

Table 13

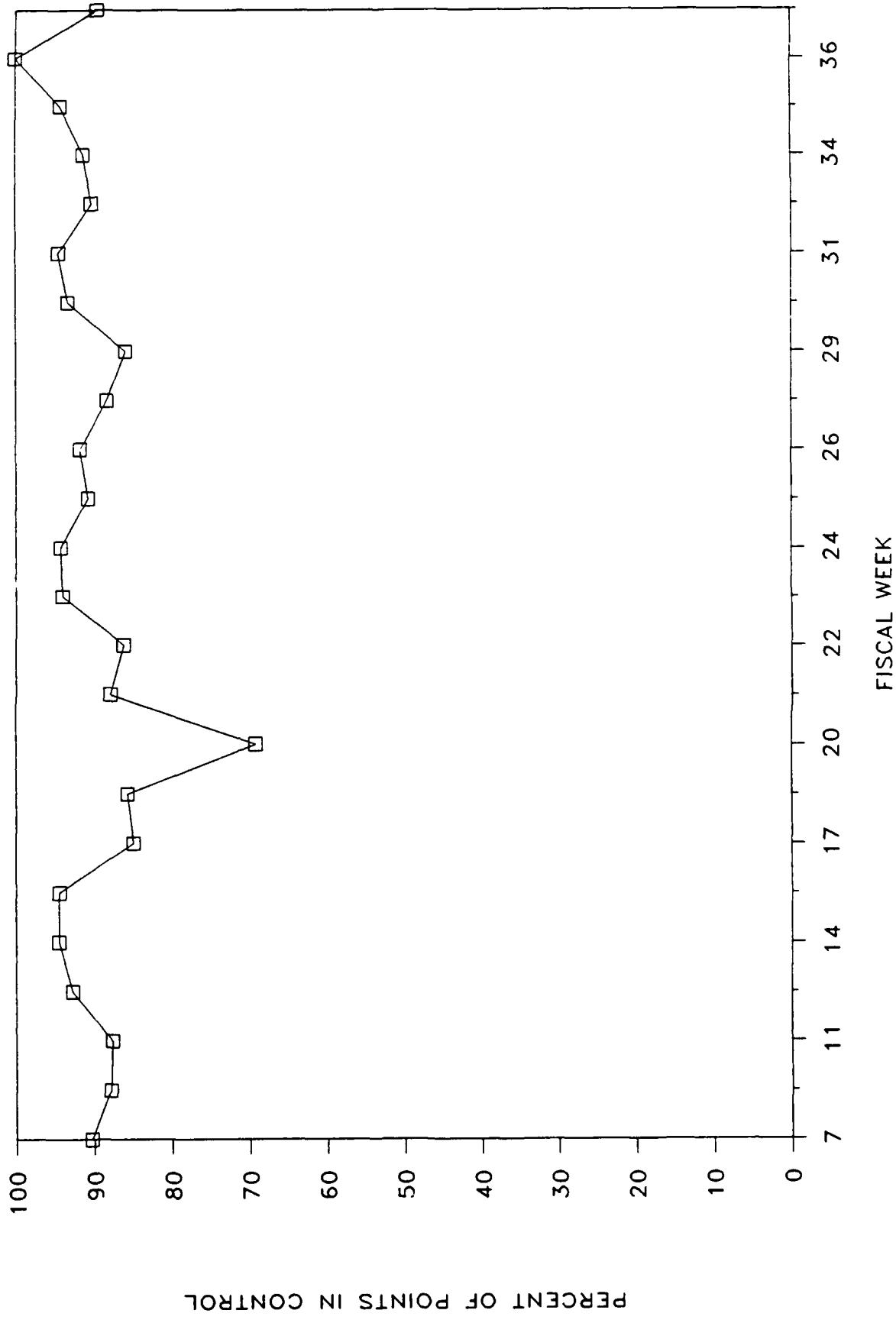

PERCENT OF POINTS IN CONTROL
100
90
80
70
60
50
40
30
20
10
0
7
11
14
17
20
22
24
26
29
31
34
36
FISCAL WEEK

Figure 24.