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THE GROWTH OF EPITAXIAL GaAs AND GaAlAs ON SILICON SUBSTRATES BY OMVPE

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CONTENTS

1. INTRODUCTION

1.1 This report covers the period December 1988 to February 1989.

1.2 The planned work for Quarter 10 was as follows:-

(1) Continue growth and assessment of GaAs/Si FET structures;

(2) Continue development of low temperature (~900°C) silicon substrate cleaning techniques,

(3) Carry out further growth on profiled silicon substrates.

(4) Defect reducing experiments using cyclic thermal anneal routines during growth,

(5) Study the effect of substrate orientation, on nucleation and initial stages of growth,

(6) TEM studies and assessment of defect reducing experiments, nucleation, and initial stages of growth;

(7) Design and fabrication of low complexity structures containing more than one device function.

However, following a progress meeting at the Naval Research Laboratories during January 1989, it was agreed with our sponsor, Dr H Lessof, that the program should be amended in the light of the world state-of-the-art in GaAs/Si. It was apparent that significant materials challenges still remained worldwide, and that unacceptable compromises in device performances would have to be made for the GaAs on Si approach to be pursued. As a result it was agreed that research on this programme should be aimed at investigating methods of improving materials characteristics. Clearly, a reliable laser on a silicon substrate would open up immense possibilities. The laser is the most demanding device to implement because of its sensitivity to dislocations, strain, uniformity, and planarity, etc. Therefore our

strategy will be to address the remaining material problems with the aim of implementing a III-V on silicon laser if material of sufficiently high quality can be prepared. The topics to be studied in the amended program have been agreed to be as follows:-

1. A satisfactory low temperature (<900^{0}C) Si cleaning technique is required. Investigation of the treatment of Si surfaces with hydrogen plasmas prior to GaAs growth will be pursued and the influence of surface treatment on the structural properties of the layers studied. The effects of the inclusion of AsH_3 and PH_3 in the H_2 flow will be investigated.

   Comparisons will also be made with growth of GaAs by OMVPE on Si surfaces prepared in an MBE chamber. The Si wafers will be prepared at the University of Wales College of Cardiff and coated with As in UHV for transportation to Plessey Caswell. Evaporation of the As in the OMVPE system prior to growth will then expose the MBE cleaned Si surfaces.

2. To date in this programme a number of methods have been employed to reduce the dislocation content of layers - these are (i) strained layer superlattices, (ii) cyclic annealing/growth procedures, and (iii) the use of profiled substrates. All have been found individually to reduce the imperfection content of layers. The effects of combining all three simultaneously in the same structure will be studied.

3. Selected area deposition using substrates masked with Si_3N_4 will be evaluated as a method of reducing the imperfect ... present in layers. TEM will be used to assess defect densities.

4. Optical microscopy has revealed that the Si substrate orientation influences the surface morphology of the layers, this topic will be investigated further, and the relationship between surface morphology and imperfection properties of the layers studied by optical and transmission electron microscopy.

5. Our theoretical calculations have shown that, in addition to interface strain fields, the shear modulus of a layer material plays an important role in its ability to turn over dislocations. In other words, a "stiffer" material is more likely to bend over a dislocation. GaAsP will be investigated as a material with appropriate properties.

6. In order to understand in more detail the origin of the imperfections present in the layers, nucleation of the initial layer and its influence on dislocation formation will be studied. "Initial" layers of different thickness will be deposited and the nucleation of the dislocations as neighbouring islands coalesce investigated by transmission electron microscopy. The influence of annealing on the formation of the imperfections will also be studied.

7. Compound and Orientation Dependent Epitaxy (CODE) is a technique which was discovered at Plessey Caswell. It allows InP and GaInAs to be deposited on etched InP substrates in such a way that InP is deposited conformally over mesas, whereas GaInAs is deposited only on (100) surfaces and not {111}. This allows buried layer structures to be prepared in one epitaxial process [1].

   We propose to combine CODE with growth on profiled substrates as a possible method of further reducing the dislocation content of layers.

1.3 Summary of Progress

(1) Growth of GaAs on Silicon FETs and GaAs FET Structures

Following discussions at the progress meeting in January, no FET structures were grown during this quarter, the emphasis being placed on material improvement.

(2) Growth of GaAs on Profiled Silicon Substrates

GaAs growths have now been carried out on the substrates referred to in quarter 9 which were processed to give linear features orientated in the [110], [1$\bar{1}$0], [010] and [100] directions. This material is now being assessed by TEM, and the results will be presented in future reports.

(3) Low Temperature Cleaning

Low temperature cleaning experiments have been continued using a hydrogen plasma and hydrogen/arsine mixtures.

(4) Selective Area Epitaxy

Photolithography and wet chemical etching has been used to prepare silicon nitride and silica masks on 3" diameter silicon substrates. The exposed substrate surfaces consist of a range of circular and rectangular features for assessment of growth behaviour on the mask material and in the window areas.

(5) Cyclic Thermal Annealing

Repetitive growth-anneal sequences during deposition of GaAs have resulted in a reduction of X-ray rocking curve widths, FWHM, from a previous best of 200 arc secs for unannealed material to a best value of 105 arc secs for annealed growth.

(6) Use of SLS in Conjunction with Cyclic Thermal Annealing

Strained layer superlattice containing structures have been grown on thermally annealed material, these structures are now being assessed by TEM.

(7) Transmission Electron Microscopy

In order to obtain a better understanding of the nucleation and early stages of growth of GaAs on silicon, recent TEM studies have been directed to

examination of the initial modes of growth for GaAs on silicon, and of the initial modes of growth of GaInAs in the strained layer systems GaInAs/GaAs and GaInAs/GaAs on silicon which are relevant to the growth of GaAs on silicon structures containing GaInAs/GaAs SLS dislocation filters.

2.0 MATERIALS GROWTH

2.1 Cyclic Thermal Annealing

A series of experiments was conducted in which the GaAs on silicon wafer was taken through a range of thermal annealing cycles during growth. The objective was to relieve strain periodically by annealing as the layer increased in thickness, and hence improve material quality [2].

After growth of the initialisation layer at 400^{0}C, a series of alternate anneal and grow routines were carried out. The temperature was held at 850^{0}C for 900 secs during the anneal, and 6000Å of GaAs were grown at 720^0 during each of the growth cycles. The basic annealing cycle is shown in Fig. 2.1.1(a) and the structure grown in Fig. 2.1.1(b).

Further experiments were carried out in which 2.6μm of GaAs were grown after the basic annealed growth. Fig. 2.1.2(a) and Fig. 2.1.2(b). In one case a pause, during which the wafer was allowed to cool to room temperature, was introduced between the annealing and overgrowth stages, Fig. 2.1.3.

The crystal quality of these structures was assessed by double crystal X-ray diffraction and the results are presented in Fig. 2.1.4 which shows X-ray rocking curve maps of the thermally annealed specimens, and for comparison, similar X-ray rocking curve mapping of unannealed FET first step material containing the "standard" $Ga_{0.9}In_{0.1}As$/GaAs SLS[3]. As can be seen in the diagram, the FWHM's of the diffraction peaks of the annealed material were generally lower than those obtained from the unannealed material, with a best value of 105 arc secs.

This improvement in crystal quality was encouraging, but plan view TEM revealed that the near surface defect density was $10^{8}cm^{-2}$.

Further experiments are now being undertaken to determine whether cyclic thermal annealing can be combined with SLS to give both improved crystallinity and reduced dislocation density.

2.2 TEM Studies

2.2.1 Introduction

During this period the emphasis, for the TEM investigations, has been placed on detailed studies of the early stages of growth for GaAs on Silicon and on the mode of growth for the GaInAs layers used in the Strained Layer Superlattice (SLS) dislocation filters. In order to achieve ideal configurations, for the generation and eventual removal of defects, we have found it necessary to study the modes of growth for the two heterosystems GaAs/Si and GaInAs/GaAs. This report presents our initial results and discussion.

Experimental

The wafers examined in this investigation are shown overleaf:

Sample	Structure	Tg
A	<50Å GaAlAs annealed at 950°C/Si	400
B	300Å GaAlAs unannealed/Si	400
C	300Å GaAlAs annealed at 950°C/Si	400
D	2000Å GaAs/2SLS + 3000Å spacer of GaAs/2000Å/300Å GaAlAs annealed at 950°C/Si	400/750
E	90Å GaAs/500Å GaAlAs/180Å $Ga_{.88}In_{.12}As$/GaAs.	650

All samples were grown by MOVPE. Growth conditions may be found in a previous report [4]. Transmission Electron Microscopy (TEM) was used as the principal tool of investigation. Selective area electron diffraction, Bright Field (BF), Dark Field (DF) and Weak Beam (WB) techniques were used for defect analysis. Observation of Moiré patterns has been used as a guide to local misorientation and strain relief. Specimens were examined in both (110) cross-section and (001) plan view at an accelerating voltage of 120 keV.

2.2.3 The initial growth of GaAs on Silicon

Figure 2.2.1 shows the (001) Plan view of Sample A. The islands of GaAs formed are small (typically <500Å), their density is approx. $1 \times 10^{10} cm^{-2}$. Moiré patterns generated during BF two beam imaging have shown terminating fringes indicative of an epilayer to substrate disregistery. WB microscopy has so far proved inconclusive in positively identifying the defects formed at the island to substrate interface.

The (001) Plan view of the annealed sample C is shown in Figures 2.2.1a and b. Figure 2.2.2a is a WB g(2g)220 micrograph. One set of pure edge dislocations, representing the disregistery between the epilayer and substrate due to the lattice mismatch is in contrast. Each edge dislocation is typically <1000Å in length. Both <110> orthogonal sets of misfit disloctions are apparent in the WB g(2g)400 micrograph of Figure 2.2.2b. The small contrast features are typical of those formed by a regular misfit dislocation array [5]. These features were not apparent in the unannealled Sample B. Contrast features attributable to dislocations did exist though no regular misfit grid had formed. We conclude that on annealing an ordered dislocation array has formed. The principal defects comprising this array are pure edge dislocations that have Burgers vectors $b = \frac{1}{2}[110]$ or $b = \frac{1}{2}[\bar{1}10]$ lying in the (001) plane of the interface. These dislocations always appear short in length being spaced, in a grid, approx. every 100Å. From the measured values of defect length and spacing we can calculate the expected threading dislocation density as 6.10^{11} cm^{-2}. This density will increase if secondary dislocations are produced during the coalescence of misoriented islands. Islands may be misoriented with respect to each other

due to asymmetries in defect densities in the two orthogonal <110> directions [6]. Dislocation nucleation will thus occur, as the islands coalesce, due to the disregistery between islands caused by the misorientation.

Figure 2.2.3a shows a [110] cross-section of sample C. All the defects in contrast are lying on {111} planes. Microtwins are also present but in lower densities. The film is only semi-continuous, as would be expected if an island nucleation mechanism was in operation. This could also be explained by surface contamination preventing lateral growth, however, analysis of the denuded areas revealed no evidence of contamination. Figure 2.2.3b shows the same sample tilted towards <111>. Moiré fringes, observed because of the tilt forcing the overlap of the Si and GaAs lattices, are clearly apparent. Figure 2.2.4 shows the [110] cross-section of Sample D. Again the sample has been tilted toward [111]. The crystalline quality of the initial growth appears good with no high density of inclined interfacial dislocations, stacking faults or microtwins.

2.2.4 The Mode of Growth of Strained GaInAs layers

Figure 2.2.6a shows a cross-section micrograph of sample E. The mismatch between epilayer and substrate, f = 0.85%. The upper $Ga_{.88}In_{.12}As$ interface is uneven. Figure 2.2.6b shows the (001) plan view of the sample. Dislocations form a misfit array approx. 8 x 10 μm in dimension. The Burgers vector of each dislocation is inclined to the interface plane such that $b = \frac{1}{2}[101]$, $\frac{1}{2}[011]$, $\frac{1}{2}[\bar{1}01]$ or $\frac{1}{2}[01\bar{1}]$. In this case the dislocations appear to have all been sourced from pre-existing substrate dislocations and all are 60° in nature.

2.2.5 Discussion

2.2.5.1 Gallium Arsenide on Silicon

The unannealed sample showed significantly greater crystallographic disorder than the annealed sample. This was determined by the direction and width of BF Moiré fringe images. The disorder could not be detected by electron

diffraction which showed similar single crystal patterns for both annealled and unannealled samples. The disorder is most simply interpreted as local area misorientation, displayed by changes in fringe direction, and local area strain relief, by changes in fringe width. Weak beam imaging was less useful for determining the nature of line defects in the unannealed sample than for the annealed. On annealing, short lengths of pure edge dislocation were generated. The BF Moiré patterns still displayed some areas of local misorientation but the patterns were distinctly more ordered. These observations coupled with that of the semi-continuous nature of the layer, and the observation of thinner films where discrete nuclei have been observed, agree with the observation that GaAs on Silicon grows by a 3-D mechanism. Our best model for the growth would appear to be the VW mechanism (figure 2.2.5a).

The mode of epitaxial growth can be principal in determining the type of defect that is formed when a mismatched epilayer is grown onto a crystallographically perfect substrate. For epitaxial systems we will have one of three basic thin film growth mechanisms [7] (figure 2.2.5). These may be modelled in terms of the free surface energies of the epilayer and substrate and the interfacial free energy between them. If the free surface energy of substrate A is γ_A of epilayer B is γ_B, and the interfacial free energy is γ_i, then the thermodynamical equilibrium condition for a monolayer island [8] (ie the Frank-Van der Merwe (FM) mechanism), for a layer of B on A is given by

$$\Delta\gamma_{BA} \equiv \gamma_b + \gamma_i - \gamma_A < 0 \qquad (1)$$

and requires that γ_i is negative. To achieve this growth mechanism there must be a small mismatch and a strong B-A bond. In the presence of mismatch between the epilayer and substrate then γ_i, which contains the components of elastic strain energy in the island and the misfit energy of interfacial disregistery, increases with island size. Beyond a critical size the conditions for the FM mechanism may be violated and a transition from a two dimensional (2D) mode to a three dimensional (3D) mode (ie the Volmer-Weber (VW) mechanism) may occur [9]. The surface free energy of (001) Gallium Arsenide, $\gamma_{GaAs} \sim 1.2\ Jm^{-2}$ [10], is smaller than that for silicon, $\gamma_{Si} \sim 2.1$

Jm^{-2} [11]. Considering these values in isolation we would expect monolayer by monolayer growth, however as island growth has been shown to occur we conclude that the interfacial free energy is sufficiently large for $\Delta\gamma_{GaAs-Si}$ to be positive and hence favour a 3D growth mode.

Pure edge dislocations cannot glide in from the surface in the way that 60° dislocations can. Cherns and Stowell [5] have proposed that for the epitaxial (f.c.c.) Pd on (001) Au growth system nucleation of a Shockley partial followed by the climb in of a Frank dislocation loop may lead to perfect edge dislocations being generated in the interface. Conversely, it is also possible for the Frank loop to dissociate i.e.

$$1/3[111] \rightarrow 1/2[110] + 1/6[\bar{1}\bar{1}2] \qquad (2)$$

where the Shockley partial generated escapes to a free surface leaving a $\frac{1}{2}\langle 110\rangle$ edge dislocation. For the reaction to be viable then a source of 6.10^{11} cm^{-2} stacking faults would be required. Stacking faults may form on the exposed faces of the growing islands. If this occurs then we can propose a mechanism by which interfacial misfit dislocations may be introduced.

The required densities of stacking faults are formed during the island nucleation and initial growth to coalescence which takes place at the low growth temperature of 400°C. Any asymmetric defect densities in islands will lead to a subtle misorientation of those islands and the possible secondary source of dislocations outlined earlier. During the anneal cycle (950°C) the reaction (2) occurs forming misfit dislocations within the interface, the principle driving force for this reaction is the more efficient relief of misfit by a $\frac{1}{2}\langle 110\rangle$ dislocation compared with a $1/3\langle 111\rangle$ partial dislocation.

Not all stacking faults are annealed out at this stage, hence our observation of the inclined defects remaining in sample C.

As growth proceeds at a higher temperature (750°C) then most of the remaining stacking faults eventually dissociate to form edge dislocations, hence the absence of them in sample D (Figure 2.3.4). This scenario is presented tentatively until more data is available. The observation of stacking faults

formed during island growth and of subtle Moiré fringe misalignment has been made previously [12].

2.2.5.2 Gallium Indium Arsenide Strained Layers

GaInAs layers are used solely in our SLS dislocation filters in GaAs on silicon, where the threading dislocation density is high 10^7-$10^8 cm^{-2}$ and local strain inhomogenities due to plastic relaxation can lead to interface wavyness.

Sample E was chosen because it contains a GaInAs strained layer grown on a gallium arsenide substrate where the dislocation density is low $10^3 cm^{-2}$ and most of the dislocations are restricted to the lower GaAs-GaInAs interface.

The wavy upper interface could not be correlated with the presence of misfit dislocations, hence in this sample we do not consider that the surface roughening is a consequence of strain inhomogenities due to local misfit relief. It is also unlikely that the principal cause is poor gas switching as these effects are not apparent in the AlGaAs to GaAs interface or in thinner samples demonstrated elsewhere [13]. Surface roughening, on the upper interface, of a strained layer has been reported previously [13,14] for this growth system. The observations lead us to suggest that we have a tendency toward Stranski-Krastanov growth, i.e. as the layer thickness increases there is a tendancy toward 3D growth, as denoted by the wavy upper interface. In a strained mismatch layer system this is coincident with an increasing mismatch stress energy as growth proceeds and the layer becomes thicker. The conventional model of a strained layer treats the substrate as an infinitely thick crystal upon which the epilayer pseudomorphically strains to fit. The mismatch strain acts as an 'in plane' strain at the epilayer to substrate interface with the epilayer tetragonally distorted in its vertical dimension. The implications of this are that the state of the growth front should remain unchanged as thickness increases, obviously if misfit dislocation generation occurs on a large scale then surface step formation and local stress inhomogenities will affect morphology. It is thought that these effects would have to be extensive to produce significantly deleterious effects. If the state of the growth front remains unchanged then it is

difficult to relate the onset of 3D growth with increasing elastic strain via increasing thickness.

The only factor changing with thickness should be the in-plane stress. We are suggesting that this is directly affecting the growth front (separated by over 100Å) during growth. Thus we are experiencing a component of it at the growth front, that directly affects the epilayer: adatom nucleation. We assume this effect to be small but may become significant with increasing thickness and mismatch. By assuming the presence of this component at the growth front, directly related to the changing elastic stress energy at the substrate to epilayer interface, we are able to construct a 3D growth scenario:

Growth starts in a monolayer by monolayer fashion. As growth proceeds there is an increasing tendency for adatoms to stick to part-formed monolayers rather than the surrounding matrix, the driving force for this is hypothesised as the increased strain relief enabled by lateral relaxation in the island, an opposite effect to that of increasing elastic stress. This relaxation effect has to be greater than that of the increasing energy due to contributions from the surfaces now formed at the island edges.

This mechanism requires that the substrate to epilayer relationship is constantly changing throughout growth, not necessarily through plastic deformation to relieve mismatch at the substrate to epilayer interface, but by interactions across the whole crystal that are purely transfers of the elastic stresses generated.

Conclusions

GaAs on silicon has been observed to grow by the formation of 3-D nuclei, i.e. by the Volmer-Weber mechanism. It may be hypothesised that if islands were larger and, as a consequence, the edge dislocations formed were longer then the number of 'threading' dislocation ends per unit length misfit dislocation would be reduced. To achieve this would require a decrease in the island density which could most easily be achieved by increased surface mobility of the adsorbed species facilitated by a higher growth temperature.

Historically, however, poorer morphologies result from higher growth temperature. At present we have no proof to suggest that the island dimensions limit the dislocation length, it may well be inextricably linked to the nature of their source. Clearly we also have to consider that the greater the degree of misorientation in the as deposited film the worse any secondary defect nucleation will be.

For the GaInAs on GaAs growth system we have hypothesised that under the conditions investigated to date a Stranski-Krastanov growth mechanism is exhibited for thicker epilayers. For strained layer superlattice filters we require the interfaces to be as sharp as possible. The lateral glide of dislocations at these filters is proportional to the magnitude of the in-plane stress at the strained layer filter interface. The magnitude of this stress will effectively be reduced if this interface is not abrupt, hence we would expect the filter efficiency to be reduced. It follows that as the most abrupt interfaces are achieved with thinner layers then the strained layer superlattice should consist of increased numbers of thinner GaInAs/GaAs periods where the same overall lattice mismatch may be achieved but avoiding the possible problem of incurring wavy interfaces. Structures containing up to a 100 periods of 100Å $Ga_{0.85}In_{0.15}As$/GaAs SLS layers were used in previously grown dislocation filter systems. These observations indicate that the use of multiple period SLS structures containing thinner GaInAs layers with thicknesses in the range 10-50Å, should be investigated as dislocation filters.

2.3 Low Temperature Silicon Surface Cleaning Experiments

Low temperature (~900°C) silicon surface cleaning experiments have been continued during this period. The apparatus and experimental details were described in quarterly report No. 9, September-November 1988, where successful substrate cleaning at temperatures in the range 900-950°C was reported.

Recent experiments have been carried out aimed at improving reproducibility and reducing contamination arising from interactions between the plasma and reactor walls.

The feasibility of low temperature thermal cleaning of silicon surfaces in hydrogen/arsine mixtures is also being explored. The results of these studies will be presented in quarter 11.

2.4 Growth on Profiled Substrates

Gallium arsenide has been deposited on silicon wafers containing linear features orientated in the [110], [1$\bar{1}$0], [010] and [100] directions. This material is now being assessed by TEM, and SEM.

2.5 Selective Area Growth

2000Å of silica, or 2000Å of Si_3N_4 were deposited on silicon substrates, and photolithography used to open up windows in the mask, with the geometries shown in Fig. 2.5.1. These consist of a series of different diameter circular features and a range of different sizes and orientations of rectangular features. This will enable the growth behaviour at the mask-substrate interface to be studied for a range of different mask geometries. Prior to growth the wafers will be cleaned by ozone ashing followed by very brief buffered HF dip. Etching trials on control specimens have shown that 2000Å of Si_3N_4 is removed in buffered HF in about 1½ minutes.

Substrates for selective area epitaxy have also been prepared by similar photolithography, and etching to leave areas separated by "V" section grooves, see Fig. 2.5.2. The idea here is to exploit CODE (Crystallographic orientation dependent epitaxy) to achieve selective area growth without the presence of any mask material on the substrate during growth.

The growth rate of GaAs on the {111} planes exposed in the "V" grooves is very low in comparison with growth on the planar (001) surface [14] which should result in isolated rectangular features separated by a grid of 'V' section grooves.

CODE growth is a technique pioneered at Caswell in growth of III-V alloys on InP substrates [1] hence it is anticipated that the technique could also be successfully employed for selective area epitaxy of InP/GaInAs on silicon.

Growth on these substrates will be carried out in quarter 11.

2.6 Reduction of Crystallographic Slip

Growth on three inch and two inch diameter substrates which have been cleaned in situ by heating at temperatures in excess of 1100°C for 20 minutes immediately prior to epitaxial deposition have generally shown considerable crystallographic slip due to thermal stress generated during wafer cleaning. These layers have been grown using a flat but recessed susceptor and it was considered that some of the thermal strain may have been generated by non uniform contact of the substrate with the susceptor. This effect has now been reduced in the case of 2 inch wafers by using susceptors equipped with a stepped recess which supports the substrate on a 3mm wide band around its edge and about 100μm above the substrate surface, Fig. 2.6.1. Substrates placed on this recessed susceptor, and subjected to the usual temperature cycle during the thermal clean at 1100°C have shown substantially less slip. Regions of slip extend inwards from the edge of the wafer and show variations in the number density of slip lines and distance propagated from the substrate edge.

Slip regions containing ~11 slip lines per mm extending 8-12mms from the 2" wafer edge were observed when the flat bottom recessed susceptor was used. Use of the modified stepped recess susceptor resulted in a reduction in the number of regions of slip, and of the slip line density to ~4 lines mm, and the slip regions extended for typically 2-5mms from the substrate edge.

3. CONCLUSIONS

(1) The narrowest X-ray linewidths for GaAs on Si observed to date, 105 arc secs, were obtained by cyclic thermal annealing during growth. However, layers contained 10^8 defects cm^{-2}.

(2) Crystallographic slip observed in wafers heated to 1100^{0}C in hydrogen has been significantly reduced by using stepped recess susceptors.

(3) A further batch of silicon substrates has been processed ready for selective area epitaxy.

(4) TEM studies of the nucleation and early stages of growth of GaAs on silicon confirm a 3-dimensional growth mode, and indicate a relationship between island size and the number of threading dislocations.

(5) TEM studies of GaInAs/GaAs SLS dislocation filters suggest that the SLS would divert dislocations more effectively if they contain increased numbers of thinner GaInAs/GaAs periods.

(6) A series of profiled substrates with differing surface geometries have been prepared for epitaxial deposition.

4. FUTURE PROGRAMME

(1) Continue development of low temperature (~900°C) silicon substrate cleaning techniques.

(2) Compare growth of GaAs on silicon surfaces prepared in an MBE chamber with growth on surfaces prepared in the atmospheric pressure MOVPE system.

(3) Study the effect of simultaneously combining SLS dislocation filters, cyclic thermal annealing, and the use of profiled substrates in the same growth run.

(4) Carry out further selective area epitaxy experiments using recently prepared substrates.

(5) Carry out further experiments on the effect of Si substrate orientation on layer nucleation, surface morphology, and electrical properties.

(6) Continue TEM investigations of initial layer nucleation.

(7) Investigate the application of compound and orientation dependent epitaxy (CODE) to selective area epitaxy of III-Vs on silicon.

(8) Investigate the growth of InP and GaInAs on planar and patterned substrates on silicon.

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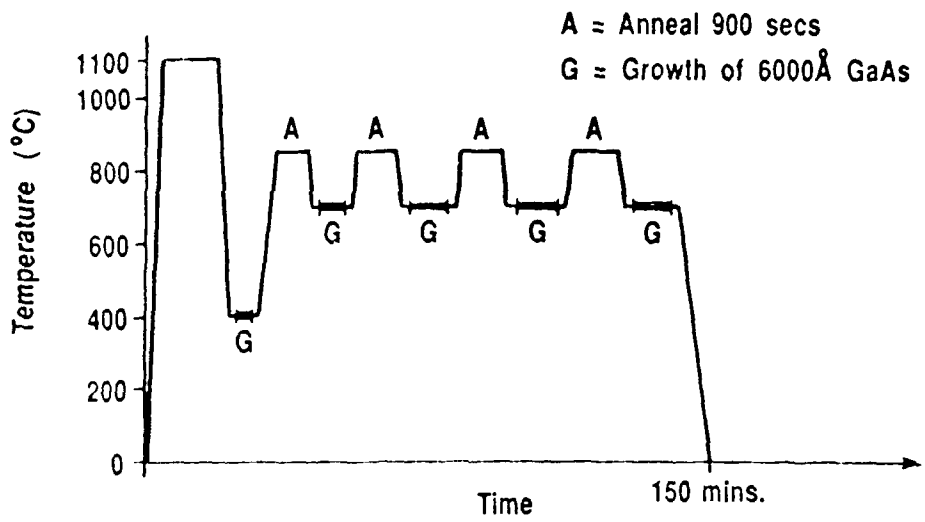


Fig. 2.1.1. (a) GROWTH-ANNEAL TEMPERATURE CYCLE

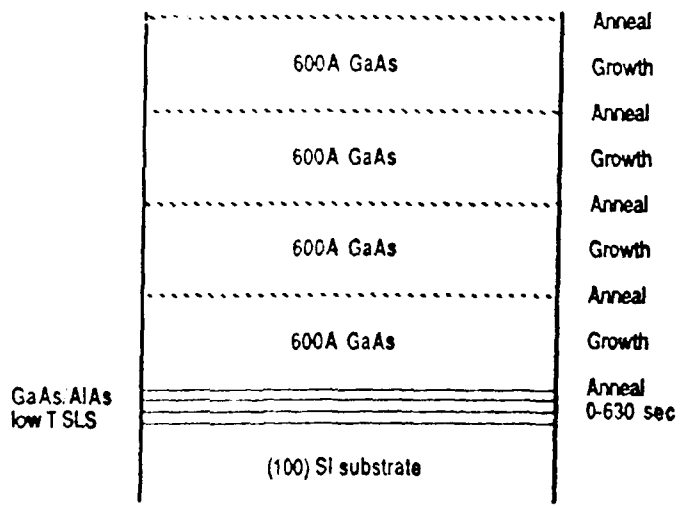


Fig. 2.1.1. (b) GROWTH-ANNEAL STRUCTURE

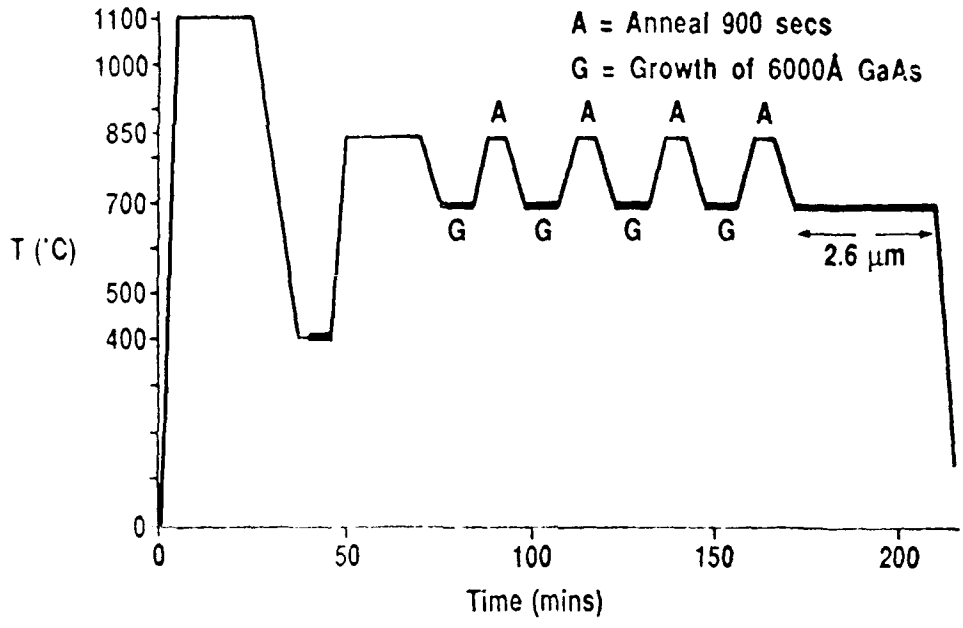


Fig. 2.1.2. (a) GROWTH-ANNEAL TEMPERATURE CYCLE WITH OVERGROWTH

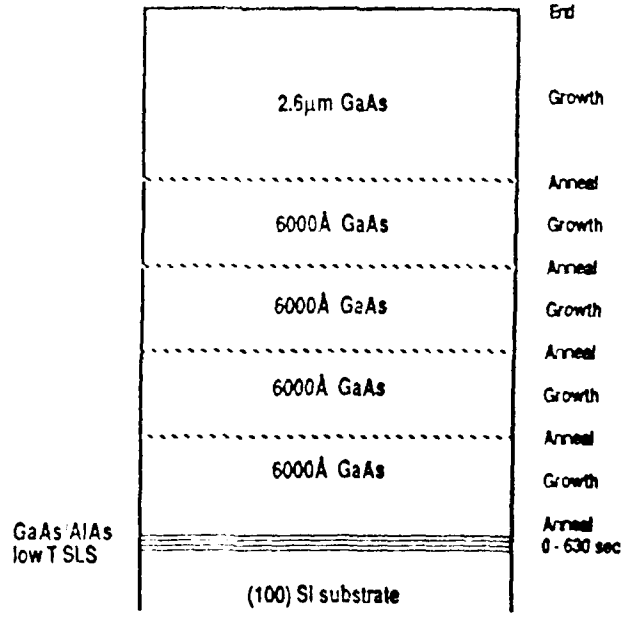


Fig. 2.1.2. (b) GROWTH-ANNEAL STRUCTURE WITH OVERGROWTH

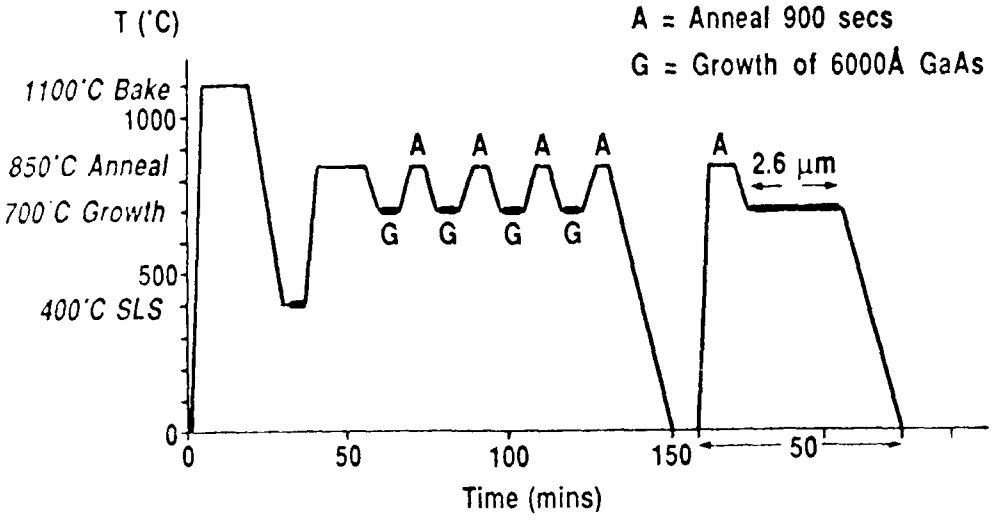
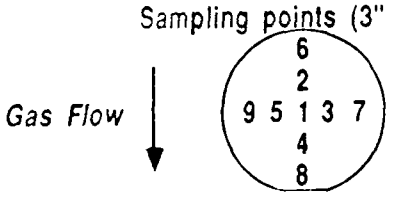


Fig. 2.1.3. GROWTH-ANNEAL TEMPERATURE CYCLE WITH PAUSE



Key

OA - 704. Growth/Anneal.
OA - 706. Growth/Anneal with Pause and Overgrowth.
OA - 709. Growth/Anneal with Overgrowth.

Double crystal XRD rocking curve FWHM (arc sec)

Run No	Experiment	1	2	3	4	5	6	7	8	9	Mean	S.D.
OA-375	Standard SLS	180	196	220	190	210	186	117	180	172	190	+/-16
OA-702	Standard SLS	253	268	230	225	244	263	230	240	250	245	+/-15
OA-704	Growth/TCA	167	153	210	187	187	163	182	177	182	179	+/-17
OA-706*	Growth/TCA	115	134	110	153	124	105	120	120	124	123	+/-14
OA-709	Growth/TCA	134	132	177	162	146	125	186	134	134	148	+/-22
OA-711	Growth/TCA/SLS	380	320	390	500	410	340	420	450	450	410	+/-60

**Significant cross hatching*

Fig. 2.1.4. X-RAY WORKING CURVE COMPARISON OF ANNEALED AND NON-ANNEALED GROWTH STRUCTURES

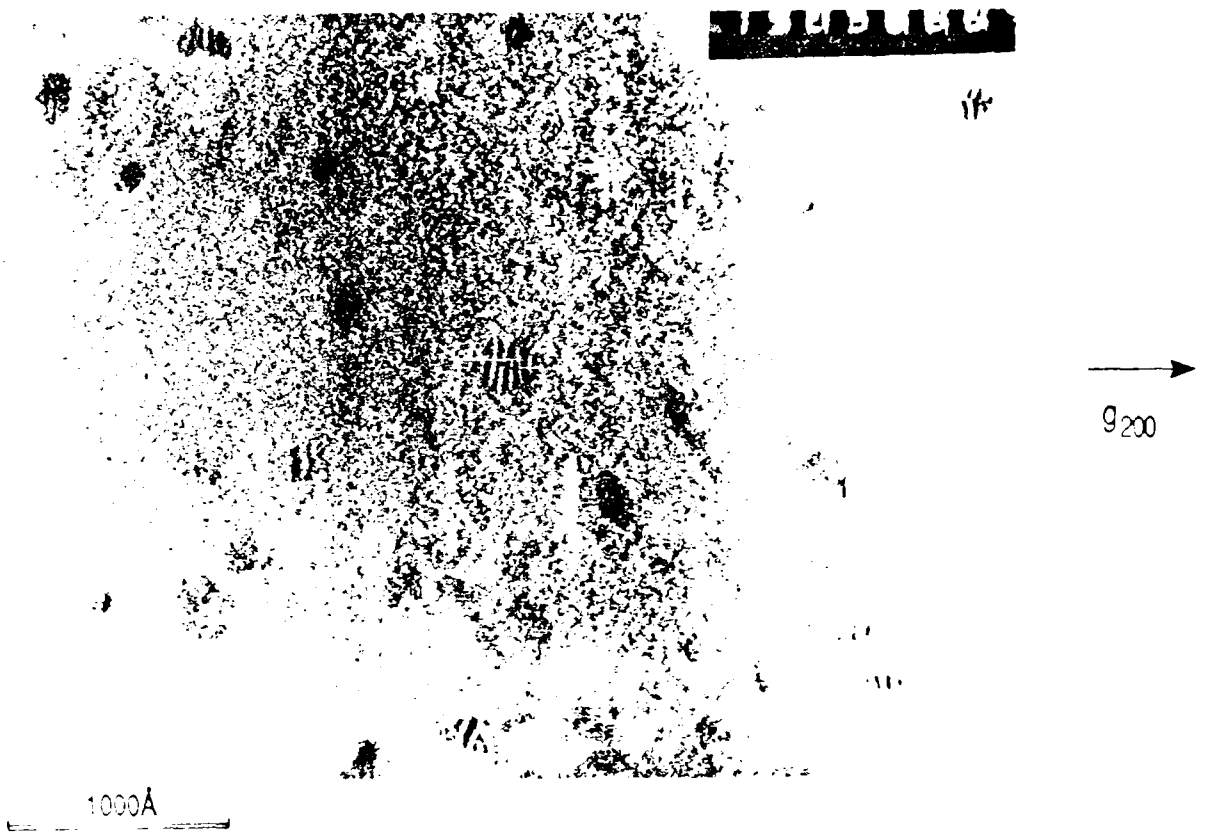


Fig. 2 2.1. SAMPLE A. ISLAND GROWTH

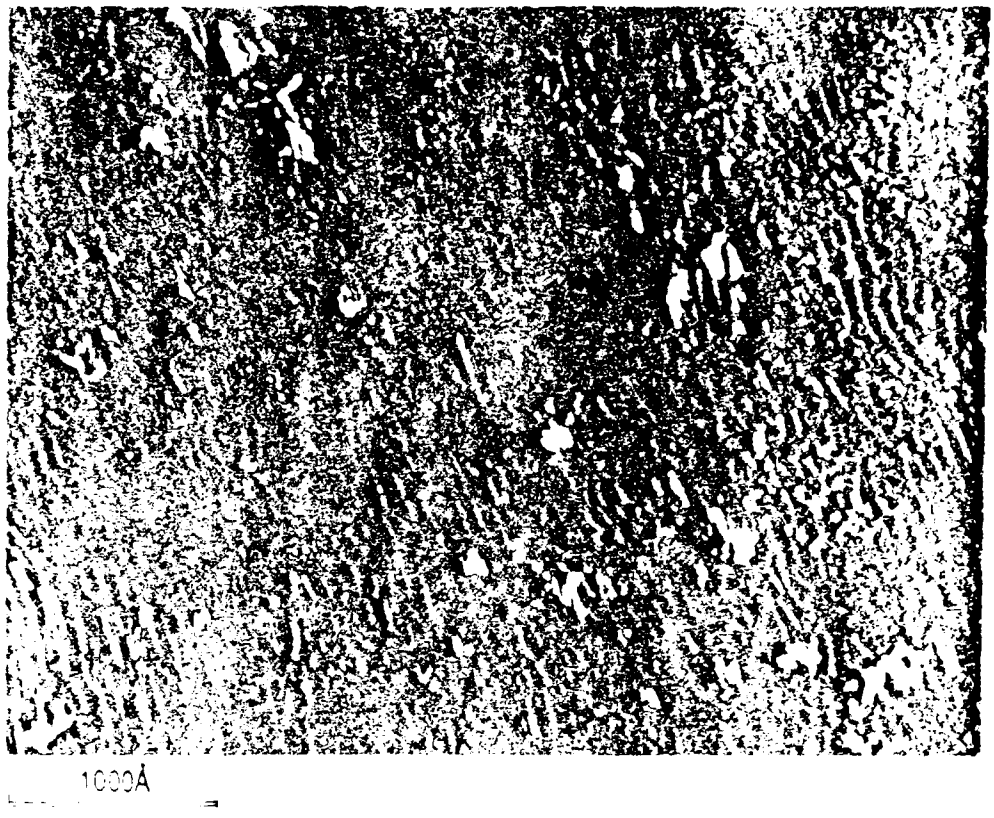


Fig 2.2.2 (a) SAMPLE C. 1 SET OF MISFIT DISLOCATIONS IN CONTRAST

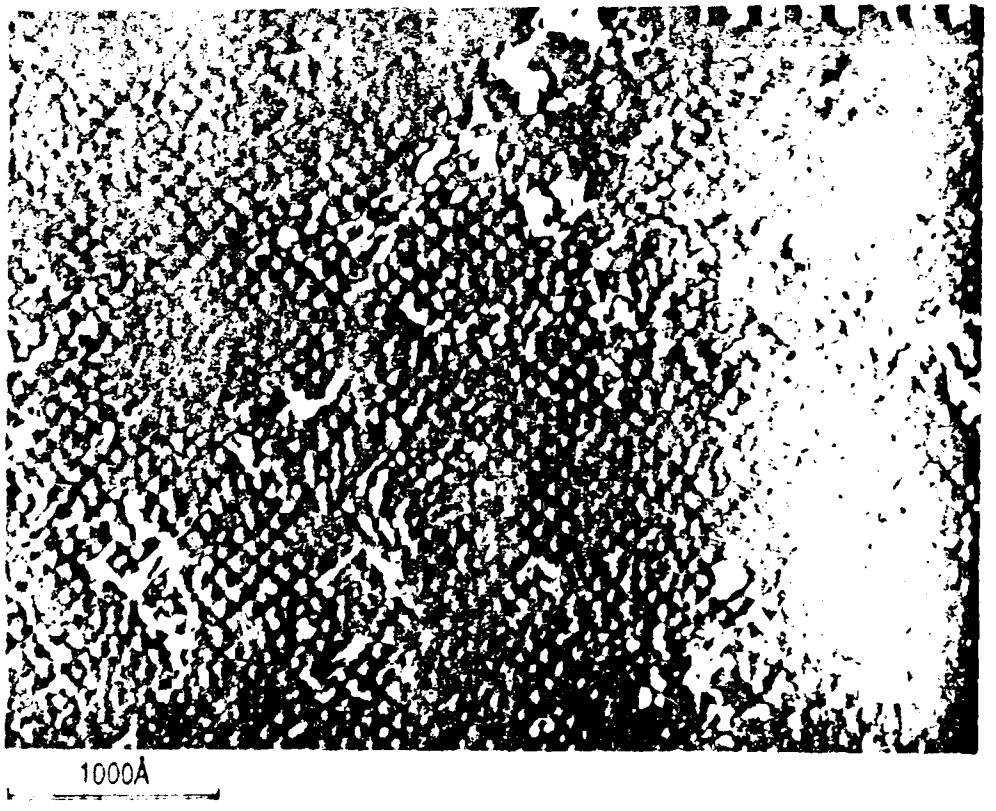


Fig 2.2.2. (b) SAMPLE C. BOTH SETS OF MISFIT DISLOCATIONS IN CONTRAST

Fig. 2.2.3. (a) SAMPLE C. [011] CROSS SECTION

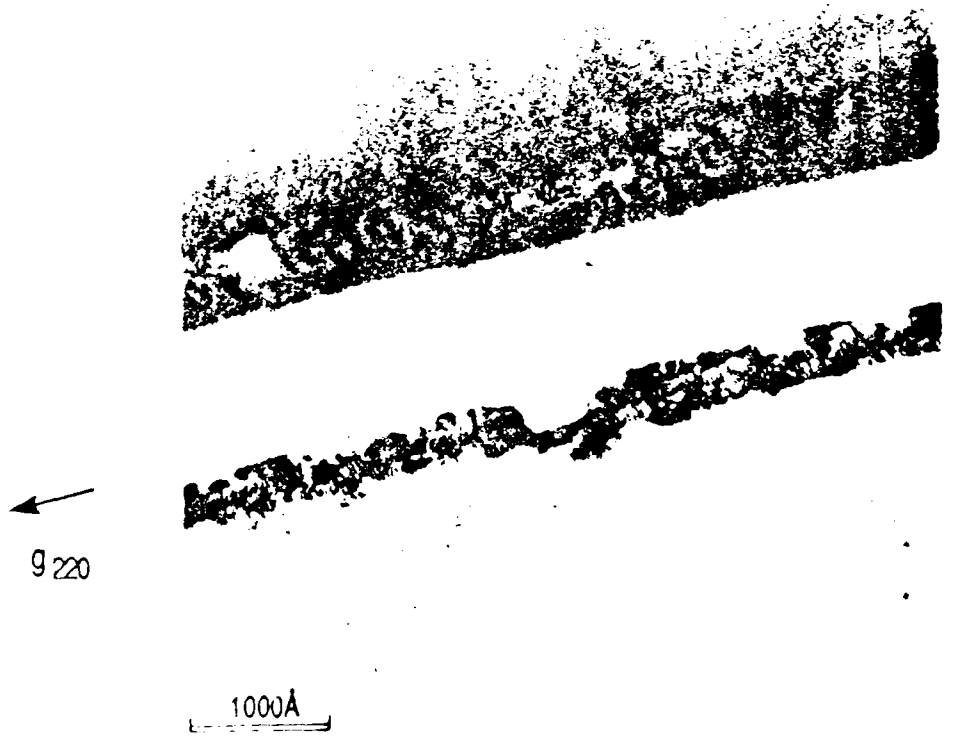
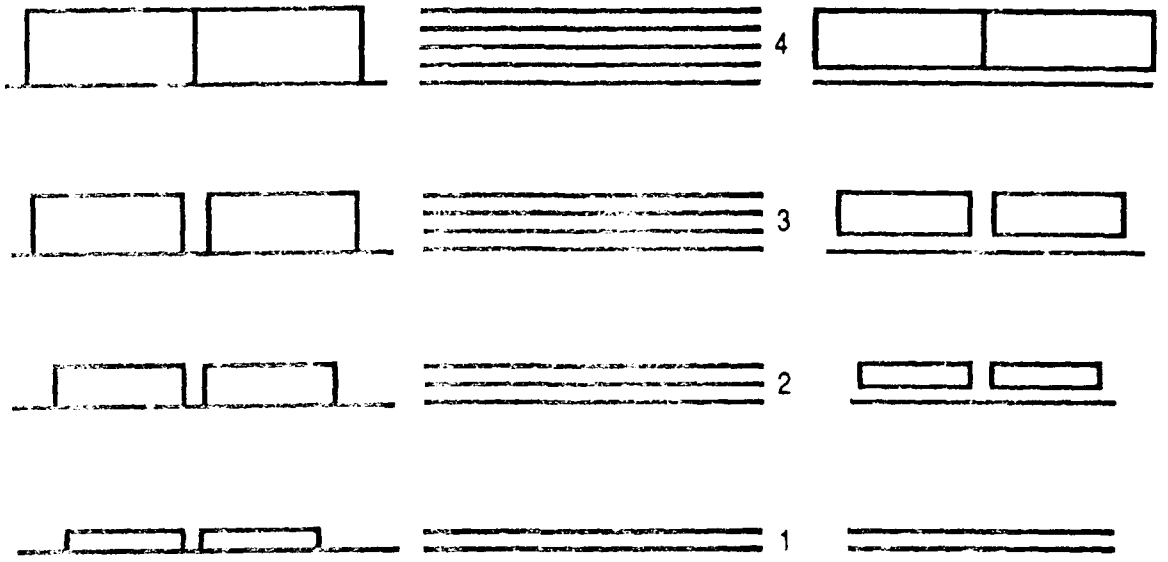


Fig. 2.2.3. (b) SAMPLE C. [011] CROSS SECTION TILTED TO [111]

Fig. 2.2.4. SAMPLE D. INTERFACE BETWEEN GaAs AND SILICON



a. Volmer-Weber b. Frank-Van der Merwe c. Stranski-Krastanov

Fig. 2.2.5. THE 3 BASIC THIN FILM GROWTH MECHANISMS

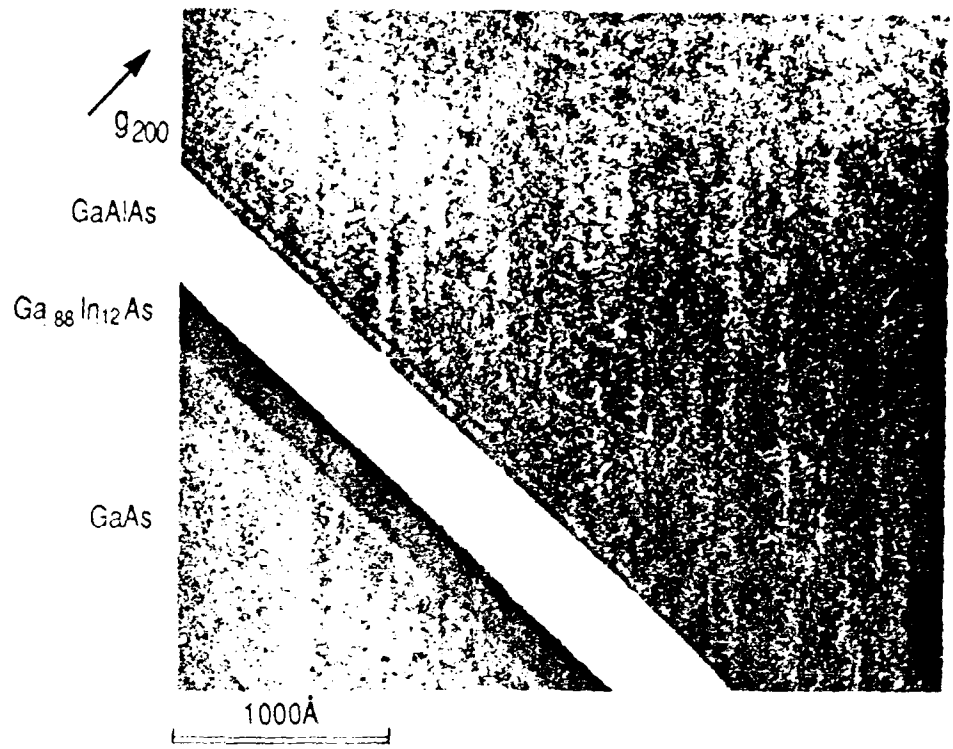


Fig. 2.2.6. (a) SAMPLE C. SINGLE STRAINED GaInAs LAYER

Fig. 2.2.6. (b) SAMPLE E. MISFIT DISLOCATIONS SOURCED FROM PRE-EXISTING SUBSTRATE DISLOCATIONS

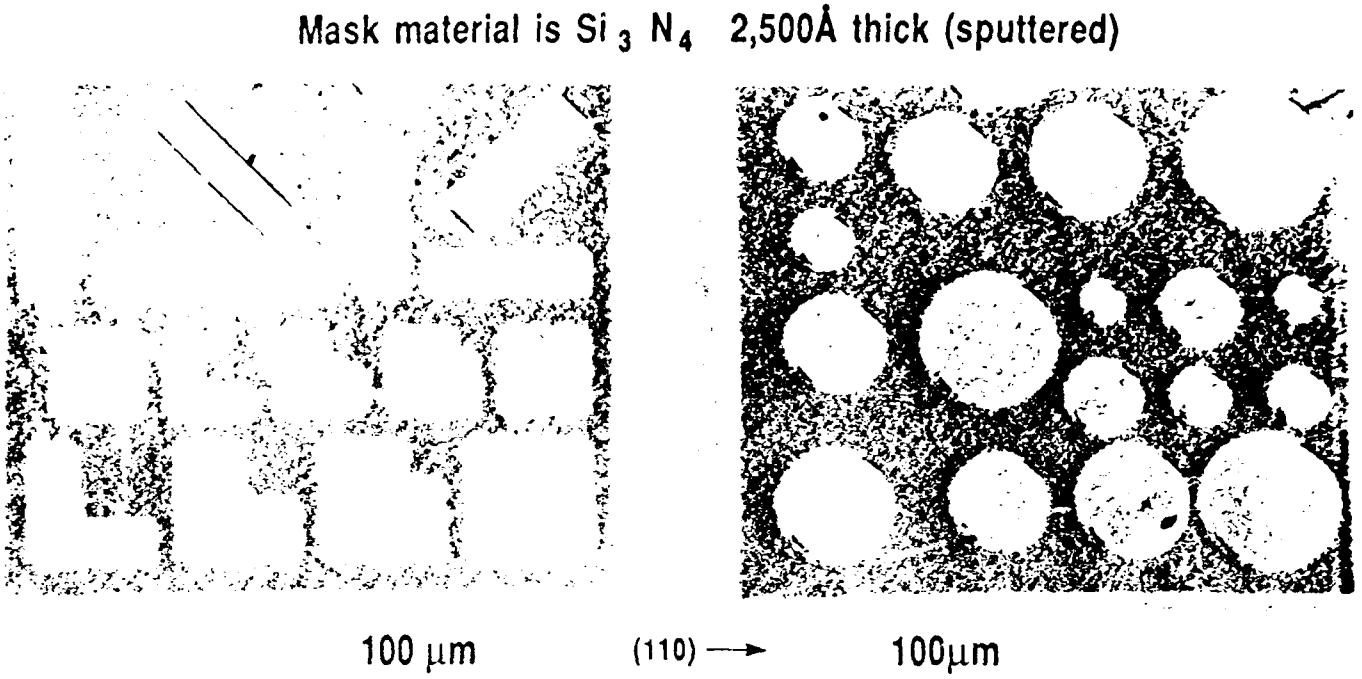


Fig. 2.5.1. SUBSTRATE PREPARED FOR SELECTIVE AREA EPITAXY

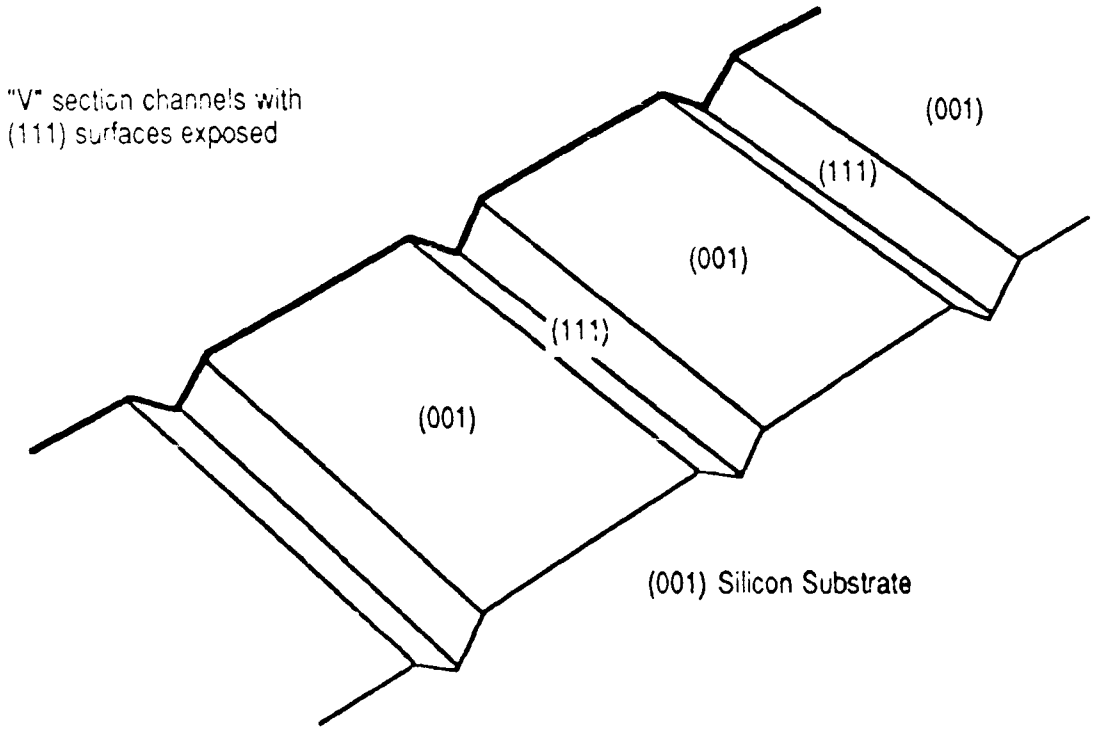


Fig. 2.5.2. "V" GROOVE SUBSTRATE FOR CODE GROWTH OF GaAs ON SILICON

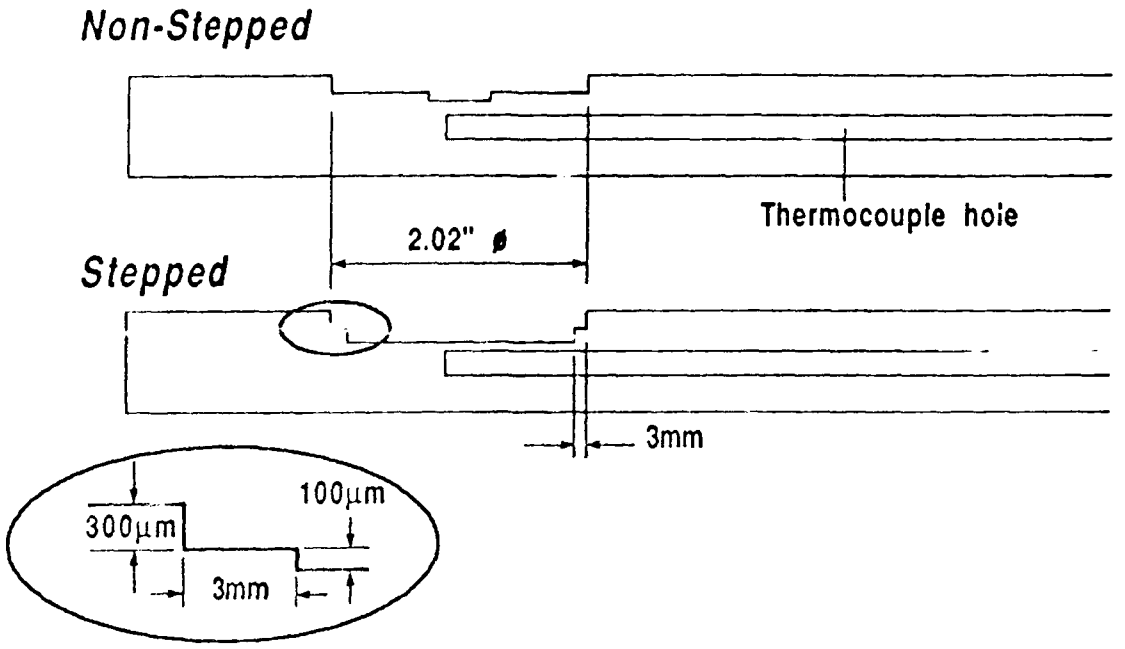


Fig. 2.6.1. SUSCEPTOR RECESSES