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VHSIC/VHSIC-LIKE RELIABILITY PREDICTION MODELING

IIT Research Institute

William K. Denson and Philip Brusius

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This report describes a study in which the objective was to develop a reliability prediction model for CMOS VHSIC and VHSIC-Like Devices. Since little field failure rate data is available on these devices, a physics of failure approach was taken in which each failure mechanism was modeled separately. The failure modes/mechanisms modeled were time-dependent dielectric breakdown, electromigration, contamination, hot carrier effects, package related mechanisms, electrical overstress, and a miscellaneous category. Each of the failure mechanisms modeled were derived from life test results, screening test results, test structure data, and theoretical considerations. Keywords: Complementary Metal Oxide Semiconductors; Very Large Scale Integrated Circuits;

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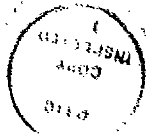

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EXECUTIVE SUMMARY

IIT Research Institute and Honeywell SSED have teamed to develop a reliability prediction model for VHSIC and VHSIC-Like CMOS devices with the intent that the model be suitable for inclusion into MIL-HDBK-217. Traditional methods of reliability prediction modeling have relied on the statistical analysis of empirical field failure rate data. Since no field data was available for this purpose, a reliability physics based modeling approach was used in conjunction with empirical data from life tests, environmental tests, and test structures.

Two separate models were developed; a detailed model and a short form model. The detailed model is based on the characteristics of specific failure modes, manufacturer specific information such as defect density and wearout performance, and key application data including temperature and operating time. The short form model is a condensed version of the detailed model and does not require manufacturer specific information but rather easily accessible information. The penalty in using the short model is its lower precision and accuracy relative to the detailed model.

In addition to the data supplied by Honeywell to this effort, a database was built containing life test, burn-in, and environmental test results from a variety of manufacturers. Much of the data contained in this database was used in the quantification of early life failure rates for various specific failure mechanisms. Therefore the detailed model predicting defect related early life failure rates will yield an industry wide representative failure rate. It was also determined in this study that it is these defect related mechanisms that drive the failure rate in the part's useful life. Intrinsic wearout mechanisms have also been modeled which will provide an approximate end of life time as a function of the parts design rules and its particular application.

There was also difficulty in predicting failure rates due to event driven, design related failure mechanisms such as electrostatic discharge (ESD) and CMOS latch-up. Event statistics are generally not available, and robustness varies greatly among products and manufacturers. This can lead to very unpredictable application problem often resolved by reliability engineers.

The detailed model has been validated with the life test data that was available on 1.0 and 1.2 micron processes from three separate manufacturing processes. It was also observed that there were relatively large variations in observed failure rates between manufacturers. The model partially accounts for these variations by including fabrication specific information such as defect density and wearout data.

Another difficulty was the large number of failures reported for which the failure mechanism was unknown, implying some level of uncertainty regarding the completions of the present models.

It is quite apparent from the results of this study that a total quality management approach presents demands which go beyond traditional statistical process control, which seeks stabilization of process outcomes, monitored in terms of measured quantities such as film thicknesses, lateral dimensions, and electrical parameters. Clearly, an additional important requirement exists for monitoring and reducing various process defect densities. This will help to reduce the number of products which contain the types of defects known to cause early life failures. However, achieving the highest attainable quality in an environment where defects are infrequent and randomly placed implies an obvious need for 100% product level electrical testing for time zero failures caused by defects, as well as 100% product level reliability screening for early life failure mechanisms influenced by defects.

This effort also attempted to utilize data from ongoing efforts such as the yield enhancement and generic qualification programs. It was unfortunately concluded that the level of standardization (between manufacturers) necessary for input to a reliability model has not yet been achieved. Therefore, data from these efforts are used as an input to the model in a more qualitative sense in which case a multiplication factor is applied modifying the failure rate.

In summary, it is recognized that there is no perfect reliability model covering all CMOS VLSI devices from a variety of manufacturers. Given this, the goal of the model is to strive for accuracy for most devices, manufacturers, and applications. It is the view of IITRI and Honeywell that the model meets its goals in that it is sensitive to the proper factors effecting reliability in the proper proportion.

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EVALUATION

The objective of this effort was to develop a reliability prediction model for fielded CMOS VHSIC and VHSIC-Like devices. Since little or no field reliability data was available, an approach was taken that used methods which deviated from the traditional statistical analysis of field failure rate data. The effort was successful in accomplishing this objective with the development of two models, a detailed model and a short form model, for predicting failure rates for VHSIC and VHSIC-Like CMOS microcircuits.

The detailed model is based on the characteristics of specific failure modes, manufacturer specific information such as defect density and wearout performance, and key application data including temperature and operating time. The short form model is a condensed version of the detailed model and does not require manufacturer specific information, but rather easily accessible information. The penalty in using the short model is its lower precision and accuracy relative to the detailed model.

The models account for both time dependent and defect-related failure mechanisms. A data base was built containing the life test, burn-in and environmental test results from a variety of manufacturers. Much of the data contained in this data base was used in the quantification of early life failure rates for various specific failure mechanisms. Therefore the detailed model, in predicting defect-related early life failure rates, will yield an industry wide representative failure rate. The use of actual defect densities, if properly measured, will result in predicted reliability values which are more precise and accurate than conventional regression type prediction models.

It was also determined in this study that it is these defect-related mechanisms that drive failure rate in the parts useful life. Wearout mechanisms have also been modeled which will provide an approximate end of lifetime as a function of the parts design rules and its particular application.

The model addresses three time-dependent mechanisms; electromigration, time-dependent dielectric breakdown, and hot carrier effects. The model has factors for chip area, defect density and/or minimum feature size so that changes in technology can readily be factored in. It has a correction factor to modify the model as VHSIC field experience becomes available and to modify the model for a particular fabrication process based on the availability of high quality life tests. The model can also utilize test pattern data from manufacturers in conjunction with the Yield Enhancement and Generic Qualification programs. There is a package factor which considers the number of package pins and includes the following package types: PIN Grid Arrays, Chip Carriers, and Dual-In-Line Packages. It also has factors for EOS/ESD and whether or not the device is on the QPL/QML.

The detailed model has been validated with the life test data that was available on 1.0 and 1.25 micron feature size devices from three separate manufacturing processes. The models will be proposed for inclusion in MIL-HDBK-217 "Reliability Prediction of Electronic Equipment."

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1.0 INTRODUCTION

The intent of this effort was to develop a reliability prediction model for fielded CMOS VHSIC and VHSIC-Like integrated circuits. Since no field reliability data on these circuit types was anticipated for development of these models, methods were used that deviated from the traditional statistical analysis of field failure rate performance of the device types being modeled.

Since integrated circuit technology is advancing at a pace more rapid than our ability to collect field data and build models accordingly, this program also represented an effort to develop reliability prediction model development methodologies which alleviate the need for extensive quantities of field experience.

It was also an intent of this study is to make maximum use of the voluminous amounts of work done and being done in the area of high density CMOS reliability assurance. Data was collected during this program from Honeywell and other semiconductor manufacturers willing to participate. This approach assured that the prediction models developed are not valid only for Honeywell devices, but rather models that are reflective of the entire VHSIC and VHSIC-Like CMOS industry.

The general failure rate model was developed using data of various manufacturers and therefore calculates an average expected failure rate. In reality, large variations in failure rates are observed between manufacturers. In most cases the root cause for this difference cannot be modeled in a general reliability prediction model. Attempts were made to address this difference by including factors such as defect density, however, there are still many very subtle factors which heavily influence reliability, many of which are not fully understood, much less quantifiable. It should be noted, however, that the model is applicable only for a relatively mature technology that consistently yields acceptable die from every completed wafer.

It is also noted that other factors may strongly influence reliability more broadly defined as trouble free application of products in real systems. Design related overstress, ESD and latch-up robustness fall into this category, and these may vary greatly among products and manufacturers. These are also event driven failure mechanisms, and failure rate prediction would require knowledge of event statistics as well as device robustness.

Additionally, although this is primarily a theoretical, bottom up approach to reliability model building, this study attempted to maximize the use of empirical data, on both specific failure mechanisms and the entire device. This represents a radical departure from traditional failure rate modeling methods since it offers the potential of using data on specific failure mechanisms (from test structures, life tests, etc.), whereas historical methods have required empirical data on the entire packaged part.

Also recognized in this effort is the need for various types of models filling the needs of specific users. For example, to fully utilize the knowledge base of large scale CMOS reliability, a model which uses detailed physical parameters of the circuits being fabricated is required. Additionally, the need is also recognized for a short, easy to use model, capable of rapidly providing reliability estimates. This effort addressed the needs of these two user types by providing both a detailed model and a short form model.

2.0 REPORT ORGANIZATION AND NOTATION

The remainder of this report is organized as follows:

- Section 3.0 presents the approach taken in this study to meet the stated objectives. It summarizes the methodology used to separate failure rate contributions from individual failure mechanisms and also how the early life and wearout failure rates were quantified. It also discusses the relationship of this effort to related efforts such as the yield enhancement and generic qualification programs.

- Section 4.0 discusses the database that was built for this effort, the manner in which data was collected, and profiles of the database regarding the type and complexities of devices the data was collected from.

- Section 5.0 is the main section of this report which presents the derivation of failure rate models for each failure mechanism that was modeled. Failure rate contributions were derived and summarized in this section for oxide, metal, hot carriers, contamination, package related failures, electrical overstress, and a miscellaneous category. Section 5.0 also presents a detailed discussion of the relationships between yield, defect density, die area, and device type, and presents the rationale used in this effort for making the model a function of the defect density/area product.

- Section 6.0 presents the complete detailed version of the model, inclusive of all failure rates modeled. Due to the relative complexity of the model, the calculations from it are tedious. Therefore, a computer program was written to facilitate calculations. In this computer program, the user simply enters the desired input variables and can then perform a prediction at a single instant in time or can choose the charting option that will calculate the failure rate as a function of time and plot the resulting values.

- Section 7.0 presents the derivation of each factor in the short form model along with a summarization of the complete short model.

- Section 8.0 discusses modeling considerations given to fault tolerant designs. Since there are too many design possibilities to adequately model fault tolerance with a single factor, there is no factor in the model, but rather guidelines are presented to model its effect based on a detailed knowledge of the device architecture and design. Examples of fault tolerant techniques and guidelines to model them are presented in this section.

- Section 9.0 presents a summary of the 1.0 and 1.2 micron data that was used in the model validation phase of this effort, and a summary of how the predicted values compared to the observed. It also discusses the variation in failure rates observed as a function of the manufacturing process and presents some data on the accuracy that can be expected from the prediction.

- Section 10.0 presents sample calculations for 18 separate combinations of input variables, and gives plots of predicted failure rate as a function of time.

- Section 11.0 discusses briefly how field data, when available, can be used to modify the model.

- Section 12.0 discusses conclusions and recommendations regarding this modeling effort.

NOTATION AND DEFINITIONS

A = Gate Oxide Area as Used in Section 5.1.2.3 and Total Die Area as Used Elsewhere

A_B = Constant in Black's Equation

AE_{ox} = Acceleration Due to the Electric Field

A_{GF} = Acceleration Factor Due to the Oxide Electric Field

A_{HC} = Magnitude of Hot Carrier Degradation

AHE = Avalanche Hot Electron

A_n = Oxide Area of Chip N

A_0 = Oxide Area of Chip 0 for which Reliability is to be Extracted from Data on Test Structure Oxide with on a A_s

A_r = Reference Die Area

A_T = Acceleration Due to Temperature

AT_{CON} = Temperature Acceleration Factor for Contamination Related Failures

AT_{HC} = Temperature Acceleration Factor for Hot Carrier Degradation

AT_{MET} = Temperature Acceleration for the Metal Failure Rate

AT_{MIS} = Temperature Acceleration Factor for Miscellaneous Failure

AT_{ox} = Temperature Acceleration Factor for the Oxide Failure Rate

$A_{TYPEMET}$ = A constant which accounts for the relative differences in metal lengths between various device types

$A_{TYPE_{ox}}$	=	A constant which accounts for the relative differences in oxide area densities between various device types
AV_{ox}	=	Oxide Electric field acceleration factor
C	=	Constant
CDIP	=	Ceramic DIP
CLCC	=	Ceramic Leadless Chip Carrier
CPGA	=	Ceramic Pin Grid Array
DC	=	Duty Cycle, % Operating Time
D_{EFF}	=	Effective Defect Density
DIP	=	Dual In Line Package
D_n	=	Oxide Defect Density of Chip 0 (Used only in Section 5.1.2.3)
D_o	=	Oxide Defect Density as used in Section 5.1.2.3, and Critical Defect Density for Feature Size X_o Elsewhere
D_{oOX}	=	Oxide Defect Density
D_{oMET}	=	Metal Defect Density
D_r	=	Reference Defect Density
D_s	=	Defect Density of a Test Structure
D(w)	=	Area Density with Weakness Factor Larger than w
E	=	Gate Oxide Breakdown Strength

Ea	=	Activation Energy, Per the Arrhenius Relationship (in Electron Volts, eV)
E_o	=	Normalizing Electric Field
EOS	=	Electrostatic Discharge
E_{ox}	=	Electric Field Strength in the Oxide (MV/cm)
E_{REF}	=	Reference Electric Field
ESD	=	Electrostatic Discharge
E_s	=	Actual Electric Field
FIT	=	Failure Unit (Failures/10^9 hours)
FO	=	Fallout Rate (Percentage)
FO_R	=	Reference Fallout Rate
f(t)	=	Time to Failure Probability Density Function
F(x)	=	Cumulative Probability Distribution as a Function of x
G	=	Process Specific Constant
h(t)	=	Hazard Rate
I_d	=	Drain Current
I_{SUB}	=	Substrate Current
J	=	Current Density
K	=	Boltzman's Constant = $8.65 \times 10^{-5} \left(\frac{eV}{^oK}\right)$

L_{DD} = Low Dose Drain

m = Exponent for I_{sub} Term in Hot Carrier Model

n = Exponent of Current Density for Black's Equation in Section 5.2 and Exponent for Hot Carried Degradation in Section 5.3

P = Power

PDIP = Plastic DIP

P(f) = Probability of Failure due to EOS or ESD

P(f/c) = Probability of Failure given Contact from an EOS/ESD Source

PGA = Pin Grid Array

PLCC = Plastic Leadless Chip Carrier

PPGA = Plastic Pin Grid Array

P(w) = Probability of containing at least one defect with weakness factor w

QML = Qualified Manufacturers List

$Q_N(t)$ = Cumulative Failure Density of Chip N

$Q_o(t)$ = Cumulative Failure Distribution for an Oxide with Defect Density D_n

$Q_s(t)$ = Cumulative Failure Density for a Test Structure

Q(t) = Cumulative Failure Density Function

R = Duty Ratio for Substrate Current

r = Duty Cycle

RH	=	Relative Humidity
RH_{EFF}	=	Effective Relative Humidity
R(t)	=	Reliability Function
S	=	Shape Parameter Used in the Stapper Yield Model
S_D	=	Single Drain
S_N	=	Constant
S_V	=	Standard Derivation
T	=	Temperature
t	=	Time
t_{BD}	=	Time to Breakdown
T_c	=	Case Temperature
TDDB	=	Time Dependent Dielectric Breakdown
T_J	=	Junction Temperature
T_o	=	Reference Temperature
t_0	=	Effective Screening Time
t_{50}	=	Time at which 50% of the Population Fails
t_{50REF}	=	Reference t_{50} Time
V_d	=	Drain Voltage

V_{GS}	=	Gate Source Voltage
V_{SD}	=	Source Drain Voltage
V_{TH}	=	ESD Failure Threshold Voltage
X_o	=	Reference Feature Size
X_s	=	Actual Feature Size
Y_N	=	Constant
β	=	Constant
ΔH	=	Activation Energy
θ_{JA}	=	Junction-Ambient Thermal Resistance
θ_{JC}	=	Junction-Case Thermal Resistance
λ	=	Failure Rate (in Failures per Million hours)
λ_b	=	Base Failure rate
λ_{BP}	=	Base Package Failure Rate
λ_c	=	EOS/ESD Contact Rate
λ_{CON}	=	Contamination Failure Rate
λ_{EOS}	=	Electrical Overstress Failure Rate
λ_{ESD}	=	Electrostatic Discharge Failure Rate
λ_{MET}	=	Metal Failure Rate

λ_{MIS} = Miscellaneous Failure Rate

λ_{ox} = Oxide Failure Rate

$\lambda_{ox}(t)$ = Time Dependent Oxide Failure Rate

λ_{PAC} = Package Failure Rate

λ_{p} = Predicted Failure Rate

λ_{PH} = Package Hermeticity Failure Rate

$\lambda(t)$ = Failure Rate as a Function of Time

Π_{c} = Field Data Correction Factor

Π_{CD} = Die Complexity Factor

Π_{E} = Environment Factor

Π_{MFG} = Manufacturing Process Correction Factor

Π_{PT} = Package Type Factor

Π_{Q} = Quality Level Factor

Π_{SP} = Package Screening Factor

σ_{PH} = Standard Deviation for Hermeticity Related Failure Mechanisms

σ_{HC} = Standard Deviation for the distribution of Hot Carrier Failures

σ_{MET} = Standard Deviation for the metallization electromigration failure distribution

σ_{ox}	=	Standard Deviation for the TDDB Failure Distribution
τ	=	Exponential Time Constant
τ_{HC}	=	Hot Carrier Lifetime

3.0 APPROACH

The approach taken in this effort was to analyze each failure mechanism independently and develop a separate failure rate expression for each. This approach assumes that each failure mechanism is independent of each other and one is not the result of the other. While in all cases this is not entirely true, it represents a justifiable approximation when considering the limited prediction accuracy expected from such a model. Figure 3-1 summarizes the methodology used in this study.

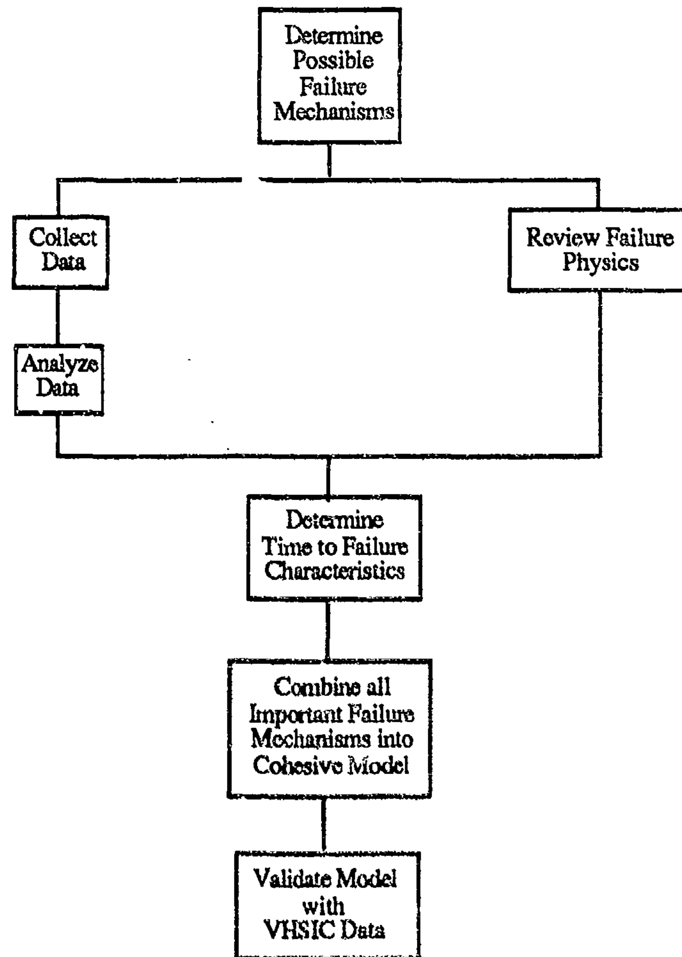


FIGURE 3-1:
MODEL DEVELOPMENT METHODOLOGY

The first step in this process was to identify as many potential failure mechanisms/modes as possible. These failure mechanisms are listed as follows:

Oxide Failures
Time Dependent Dielectric Breakdown
Metallization Failures
Electromigration
Hot Carriers
Corrosion
Ionic Contamination
Wire Bond Failures
Package Hermeticity Failures
Electrical Overstress (including ESD)
Die Bond Failures
Soft Errors
Latch Up

Next, each of these were studied to determine:

(1) Prevalence in causing failure of small feature size CMOS
(2) Time to failure characteristics
(3) How well they can be screened
(4) The factors and stresses which influence their failure characteristics

Since there are many more failure mechanisms possible than can effectively be quantified in a single model, it was the objective of this study to choose only those failure mechanisms that drive or dominate the failure rate and model them accordingly.

To accomplish this and to identify time to failure characteristics, a database was developed from screening and life test data of VHSIC-Like devices. The physics of failure characteristics of each mechanism were studied and both the fabrication variables and stresses that affect each mechanism were determined.

Next, a failure rate as a function of time was derived for each mechanism based either on empirical data from the database or based on theoretical considerations. These failure rates were then combined into a cohesive model.

The basic premise of the approach used in this effort was that die related failure mechanisms are predominantly accelerated by temperature, voltage and current and package related mechanisms are predominantly accelerated by environmental stresses (primarily temperature cycling).

Table 3-1 summarizes the number of observed failures contained in the database as a function of test type and failure class. This data supports the approach being taken of accelerating die related failure mechanisms with temperature and package related mechanisms with temperature cycling.

TABLE 3-1:
DATABASE PROFILE: NUMBER OF OBSERVED FAILURES

	Test Type		
Failure Class	Life Test	Temperature Cycling	Misc. Environmental
Oxide	274	7	0
Metal	62	3	6
Package	24	214	0
Assembly	21	0	0
Contamination	603	5	0
Unknown	789	54	4

Each known failure mechanism was analyzed, determining characteristics of infant mortality, wearout, random failures, or some combination thereof.

Each failure mechanism will therefore have either an early life (decreasing failure rate) term, a wearout failure rate term (based on the lognormal time to failure distribution), a time independent (event related) failure rate term, or a combination of the three. Table 3-2 summarizes each failure mechanism addressed in the detailed model and their associated failure rate term(s).

TABLE 3-2:
FAILURE MECHANISM CONTRIBUTION TERMS

Failure Mechanism	Short Term Decreasing λ	Long Term Wearout λ	Time Independent λ
Oxide	X	X	Note 1
Metal	X	X	
Hot Carriers		X	Note 1
Contamination	X		
Package		X (for non-hermetic only)	X
Electrical Overstress			X
Miscellaneous	X		X

Note 1: Very recent information suggests that ESD overstress can adversely affect both oxide wearout and hot carrier degradation rates. A time independent factor might be appropriate, depending on whether further work relates this effect to early life failures.

Each entry in this table represents an additive failure rate in the model and each of these failure rates are described separately in subsequent sections of this report.

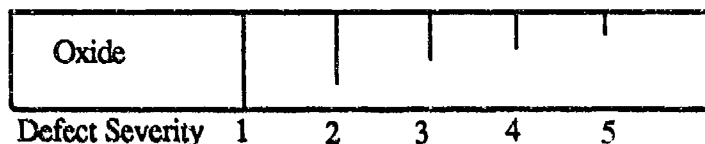
The short term decreasing failure rates for oxide, metal, contamination, and miscellaneous failure mechanisms are essentially defect related mechanisms that have the potential of being screened out. For these, the time to failure data in the database developed for this study was utilized to develop empirical failure rate relationships as a function of time.

The long term wearout failure rates are theoretically derived based on various sources including data reported in the literature, specialized test results, and test structure results. These are all based on the lognormal time to failure distribution and will predict an approximate time at which the end of life of that part is approaching. For a well designed part, the failure rate contribution from these mechanisms should be essentially zero in the useful life of the part, indicating that the failure rate is driven by the defect related mechanisms as well as the time independent, event related mechanisms.

The time independent mechanisms are those that are primarily event related, such as electrostatic discharge. The package failure rate is treated in our model as a time independent mechanism, however, there is a time dependent package related contribution in the miscellaneous term. The rationale for this is further discussed in subsequent sections of this report.

In failure mechanisms that exhibit both a short term failure rate and a wearout failure rate, the defect severity distribution plays an important role in the short and long term failure characteristics. This defect severity distributioı relates the severity of defects to its prevalence in occurring.

Figure 3-2 represents a hypothetical case illustrating an oxide with various defect severities (from Reference 8). This example relates these severities to the expected time of failure.



1. - Yield loss at wafer probe
2. - Burn-In Failure
3. - Failure during equipment checkout
4. - Failure during first year of operation
5. - Failure after 4 years of operation

FIGURE 3-2:
DEFECT SEVERITY EXAMPLE

In the contained model herein, 2, 3 and 4 are modeled with the short term failure rate contribution and 5 is modeled with the term for long term wearout. 1 is yield loss and is not explicitly addressed in the model.

This modeling approach has several advantages:

(1) By separating the failure rates due to each failure mechanism, the model can be more sensitive to stresses which affect each mechanism differently. For example, each mechanism typically will have a unique temperature activation energy, which can be modeled separately, instead of choosing an average activation energy which would result in an oversimplified approximation of the effect of temperature.

(2) It allows the user to quantitatively ascertain the benefit of screening temperature and duration. Since the predicted failure rate is a function of time, the user can model a typical failure rate improvement by trying various temperatures and durations.

(3) It gives a better representation of the behavior of the failure rate as a function of time and also provides a realistic estimate of how long the devices can be expected to last in fielded systems.

It would have been very advantageous to this effort if it were possible to identify and rank the significant failure modes and mechanisms. Unfortunately, the number of variables effecting the prevalence of each failure mode and mechanism is very high and therefore this ranking would only be valid for the device whose data was used in deriving the ranking. In other words, one CMOS process may have one particular failure mechanism prevalent, whereas another process may have different mechanisms prevalent. This is due to the many variables controlling the failure mode distribution. To attempt to quantify this variability, a survey was issued to various CMOS VLSI manufacturers in which they were asked to give percentages of failures they observe for each failure mechanism listed. This survey questionnaire is given in Appendix A. Table 3-3 summarizes the seven responses of this survey regarding the failure mode distributions, and indicates a wide variation in the prevalence of the observed failure mechanisms. These results illustrate the difficulty in deriving a model based on expert opinion.

TABLE 3-3:
FAILURE MECHANISMS DISTRIBUTIONS

Failure Mode/Mechanism	Survey Responses 1	2	3	4	5	6	7
Electromigration	-	-	-	-	-	13%	x
Dielectric Breakdown	x	50%	<.1%	98%	-	2%	x
Soft Errors	-	-	-	-	-	-	
Parametric Drift	x	-	.1%	-	-	38%	x
Hot Electrons	-	-	-	-	-	-·	
Latch Up	x	10%	.1%	-	x	-	x
Electrical Overstress	x	20%	2%	x	-		
Package Related	-	20%	<.1%	-	x	28%	x
Other	-	-	-	-	x	19%	x

x = Failure Mode occurs but no percentage given in survey response.

3.1 MODELING TIME TO FAILURE CHARACTERISTICS

It was originally intended to quantify a bimodal distribution for each failure mechanism. For example, Figure 3-3 illustrates the bimodal distribution.

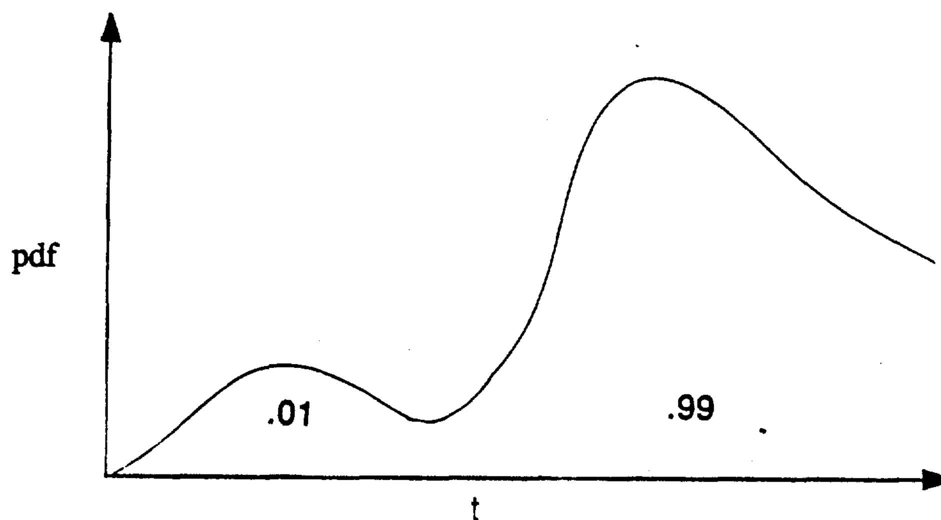


FIGURE 3-3:
BIMODAL DISTRIBUTION

Where the ratio of the area under each curve are derived from the data contained in the database developed for this effort. For example, if the database indicates that 1% of the population of devices fail in screening tests for a specific failure mechanism, then the area under the first curve will be 1% of the total.

In the case of ionic contamination, screening (or test) effectiveness is very high, and there are no wearout failures expected (i.e., all infant mortality failures), the time to failure distribution in Figure 3-4 will result in the case where 1% of the population fails in screening from contamination. Therefore, this is not the probability density function for the entire part but only for contamination.

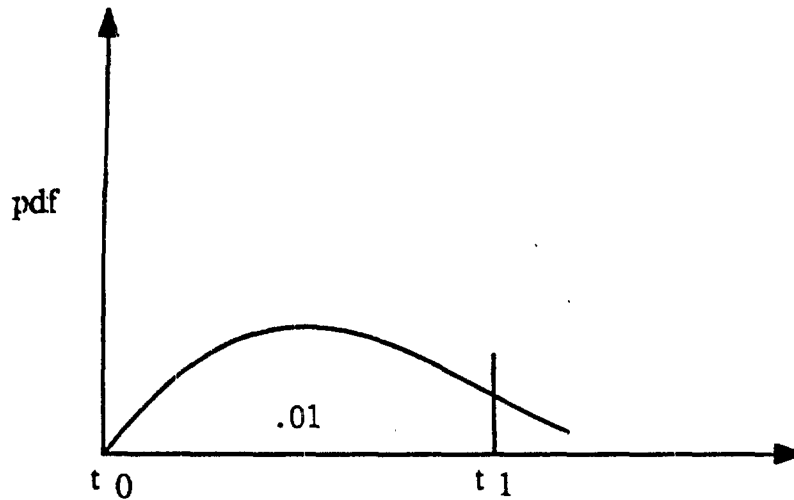


FIGURE 3-4:
FIRST MODE OF THE BIMODAL DISTRIBUTION

In Figure 3-4 the short term screening failures are expected but no wearout failures are expected due to the characteristics of contamination. If a device has been exposed to screens for an equivalent time of t_1, then the initial time of field operation would be t_1. If it has not been screened, then the initial time of field operation would begin at t_0 and 1% of the population (i.e., all contamination failures) would be expected to fail between t_0 and t_1 from contamination.

It became apparent that, while the wearout portion of the distribution could be fairly well defined, the early life defect related portion could not be modeled as an increasing and then decreasing distribution.

Also, although the time to failure characteristics were analyzed, all models were developed in a hazard rate format, instead of time to failure, to be more consistent with conventional reliability prediction methodologies, and to facilitate failure rate predictions.

3.1.1 Development Methodology

From the failure mechanisms observed in the database, there are very few observances of die failures occurring from the wearout failure mechanisms (electromigration, TDDB (time dependent dielectric breakdown), Hot Carriers, and moisture related failures in nonhermetic packages). For example, the vast majority of failures in an oxide are not time dependent dielectric breakdown, but rather other early life oxide failure mechanisms, possibly due to defects more severe than those that are manifested as TDDB failures.

To account for these failures, an exponential hazard rate model was chosen and fit to the observed failure rates (as a function of time) for each applicable failure mechanism. For example, the following basic model was used:

$$\lambda(t) = \lambda_b e^{-\tau t}$$

where:

λ_b is the base failure rate (constant)

τ is the time constant of the exponential

t is time

The time to failure data contained in the database was used to derive the observed failure rates, as a function of time and all were normalized to a 25°C temperature by multiplying the actual time by the acceleration due to temperature (A_T) (see Section 5.1.2-1). This acceleration was between the actual temperature and 25°C. The failure mechanisms for which early life failure rates were derived are; Metal, Oxide, Contamination, and a Miscellaneous category (containing various time dependent assembly and package related mechanisms). Since package related failure mechanisms accelerated by temperature cycling are modeled separately in the package factor, these factors are derived only from high temperature accelerated life test data.

Each observed failure was categorized into one of the following failure classes; oxide, metal, contamination and miscellaneous.

The following failure mechanisms/modes listed under each class summarize the observed failure cause (from life tests) contained in the database for each of these classes.

Oxide

Functional failure, threshold voltage shift
Input leakage failure, threshold voltage shift
Functional failure, gate oxide step defect
Access time out of spec, charge loss, oxide defect
Access time out of spec, charge loss, wearout
Nominal march, oxide damage
Nominal march, oxide damage
Page mode failure, oxide damage

Metal

Metal masking defect
Functional failure from aluminum corrosion
Functional failure from metal contact defect
Failure parameter from aluminum corrosion
Open metal trace
Open metal trace from aluminum corrosion
Functional metal failure from pattern shifting

Contamination

Parameter failure from contamination
Functional failure from contamination
Ionic leakage, bake recoverable
Ionic contamination
Bits failure, ionic contamination from assembly debris

Miscellaneous (Package, Assembly or Unknown)

Functional failures (unknown mechanism)
Pattern shifting
AC/functional
Masking defect
Column short to VSS
Parametric failure
Diffusion mask defect
Output leakage
Input leakage
Functional, trace, degradation
Input transistor short
Junction short
Pin leakage, bake recoverable
Open
Retention failure
Nominal march
Nominal march, poly defect
Nominal march, marginal room temp. AC
ICC stand by, out of spec, low resistor value
Wire bond failure

The methodology used to develop early life failure rates are as follows:

(1) The times of failure, for each failure mechanism were extracted from the database.

(2) These times were converted to an equivalent 25°C time based on the temperature acceleration factor for each particular failure observance.

(3) An equivalent total number of part hours (at 25°C) for the entire database was extracted for each failure mechanism observance (based on the individual mechanisms temperature acceleration factor) for small time intervals.

(4) A regression analysis was then performed on the failure rates calculated as a function of time, and fit to the following model:

$$\lambda(t) = \lambda_b e^{-t\tau}$$

$$\text{or } \ln \lambda(t) = \ln \lambda_b - t\tau$$

(5) Values of λ_b and τ were then determined.

Figure 3-5 illustrates a hypothetical application of this methodology. For this example, the following failure rates and time intervals were observed.

Time (10^6 hrs.)	λ
0 - .04	.015
.04 - 1.67	.0028

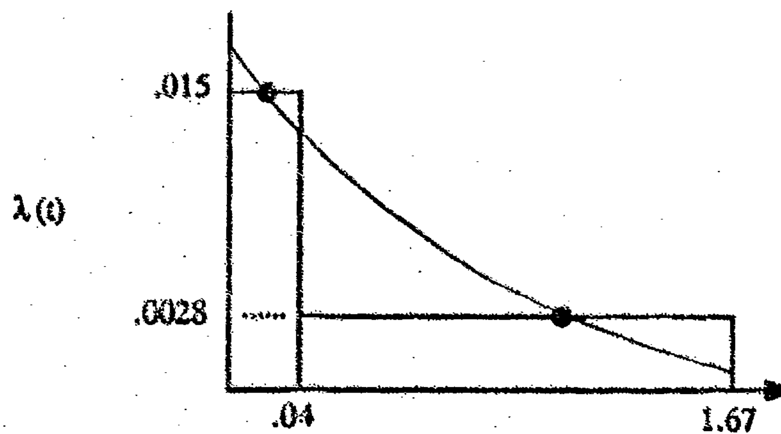


FIGURE 3-5:
HYPOTHETICAL FAILURE RATE AS A FUNCTION OF TIME

A simple regression solution was obtained using the mid point values of time in each interval, and by taking the natural logarithm transformation of the failure rate value. The following relationship was then obtained:

$$\lambda(t) = .011\, e^{-2.2\, t}$$

The next step was to insure that the cumulative failure rate (integral) was the same for the predicted and observed. This was accomplished by adjusting the τ value if required to meet this condition. The λ_b value was kept constant because there was a relatively high confidence in it since there was typically a large number of part hours and failures observed in that interval, thus yielding an accurate failure rate in the early time interval. Section 5.1.1 discusses the derivation of the actual oxide failure rate.

The screening test effectiveness has not explicitly been accounted for in the model since empirical test results were used to develop the early life failure rates (which are related to test effectiveness) based on screening and life test results. However, screening effectiveness was implicitly included in the model. It is logical to assume therefore that the test effectiveness for a particular test is approximately constant throughout the industry at the present state of the art and inherent in the model. It was attempted to derive test effectivenesses for various screens. This was abandoned due to the empirical approach taken and the fact that accurately deriving test effectivenesses is extremely difficult, and in many cases impossible.

3.1.1.1 Temperature Acceleration Factor

Since the early life failure rate is intended to model defect related failure mechanisms, a given constant percentage of the population is expected to fail in a certain time period under a certain set of circumstances. For example, if the temperature is raised by a level consistent with an acceleration factor of 10, the same percentage of parts should fail in 1/10th the time of the original temperature. That is:

$$\int_0^{t} \lambda(t)\, dt\ (25°C) = \int_0^{\frac{t}{A_T}} \lambda(t)\, dt\ (\text{at } T)$$

(A_T = acceleration due to temperature T)

and

$$\lambda(t) = \lambda_b A_T e^{-\tau A_T t}$$

where λ_b = base failure rate

3.1.1.2 Effects of Duty Cycle

The defect related mechanisms being modeled in the early life are those that occurred during operating life tests and therefore will typically only be accelerated to failure when the device is in operation. Since the models presented in this report are for operating conditions, they do not include duty cycle as an input. If the effect of duty cycle needs to be accounted for, it can be modeled in the same manner as temperature as follows:

$$\lambda(t) \; \alpha \; (DC) \lambda_b e^{-\tau DC t} \qquad (\alpha = \text{Proportional to})$$

(where (DC) = Duty Cycle)

$(0 \leq DC \leq 1)$

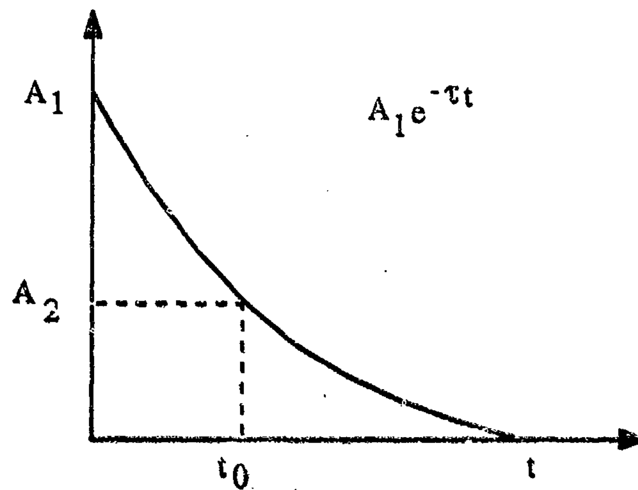
In this case the duty cycle is defined as the percentage of time the device is in its normal operating state. The one factor that does require duty cycle is the failure rate of plastic package types in which case an effective relative humidity has to be calculated as a function of duty cycle.

Therefore, summarizing the effect of both temperature and duty cycle yields:

$$\lambda(t) = \lambda_b A_T (DC) e^{-\tau DC A_T t}$$

3.1.1.3 Effects of Screening Time

If a device is burned in or subjected to a high temperature operating screen, one would expect a certain percentage of defective parts to fail. In this model, this effect is accounted for simply by adding an effective screening time (t_0) to the time variable (t). An example showing the effects of screening time is presented in Figure 3-6.



t_0 = Effective Screening time
= (Actual Screening time) A_T

$A_2 = A_1 e^{-\tau t_0}$

FIGURE 3-6:
HYPOTHETICAL EARLY LIFE FAILURE RATE

Therefore, the failure rate equation after an equivalent screening time t_0 becomes:

$$\lambda(t) = \lambda_b \, e^{-\tau t_0 A_T (DC)} \, e^{-\tau (DC) A_T t}$$

Note that the A_T may be different for screening and use environments. It should also be noted here that only life test results were used for development of these failure rates, and all environmental test results were used only for the package factor. There were, however, a few time dependent package related mechanisms occurring during life tests, and these are accounted for in the miscellaneous failure rate.

Therefore, using the method outlined herein, Table 3-4 summarizes the parameters derived for λ_b, τ, and activation energy (E_a). E_a is to be used for A_T for each failure mechanism.

TABLE 3-4:
EARLY LIFE FAILURE RATE PARAMETERS

Failure Mechanism	λ_b (F/10^6 hrs.)	$\tau\left(\frac{1}{\text{hrs.}}\right)$	$E_a\left(\frac{\text{eV}}{°\text{K}}\right)$
Metal	.00102	1.18	.55
Oxide	.0788	7.70	.30
Contamination	.000022	.0028	1.0
Miscellaneous	.010	2.2	.43

The derivation of each of these failure rates is given in subsequent sections of this report which discuss each failure mechanism separately.

Since approximately 58% of all failures were of unknown failure mechanisms (no failure analysis or inconclusive failure analysis) the parameters in Table 3-4 were derived by assuming that the unknown failure mechanisms had the same relative percentages between mechanisms as the known failure mechanism distribution. In this manner all failures were accounted for.

3.1.2 Modeling of Wearout Failure Mechanisms

All wearout failure mechanisms in this model have been modeled with a lognormal time to failure distribution. All wearout failure mechanisms modeled in this effort have empirically been shown by many researchers to follow the lognormal distribution. This distribution is given by:

$$f(t) = \frac{1}{\sqrt{2\pi}\, t\sigma} \exp\left[\frac{(\ln t - \ln t50)^2}{2\sigma^2}\right]$$

where t is time, t_{50} is the time at which 50% of the population fails, and σ is the standard deviation.

Since the prediction model is in the form of a hazard (h(t)) or failure rate, the hazard rate of the lognormal must be used. This is given by:

$$h(t) = \frac{f(t)}{R(t)}$$

Since R(t), the reliability function, involves an integral and becomes complex for the lognormal distribution, the hazard rate cannot be obtained in a closed form solution over all times.

Various statistical simulations were performed to determine if the lognormal distribution could be approximated with other simpler distributions. A pdf (probability density function) was obtained for the extreme value of the lognormal and this truncated distribution was then subjected to the Kolmogorov-Smirnov (or K-S) test to determine which, if any distribution fitted this data set. A constant failure rate (exponential pdf), Poisson, or normal distributions clearly did not fit the distribution.

If however, the reliability is relatively high (i.e., greater than .8), the probability density function itself represents a good approximation to the hazard rate, so that if the reliability is greater than .8, there is no more than 20% error in this approximation. The point at which the reliability is .8 for any given mechanism signals that the device population is reaching end of life, and the hazard rate will be dramatically increasing. Therefore, by defining the model to be valid only for those times where the reliability is greater than .8, the closed form probability density function can be used to approximate the hazard rate. Beyond this time, the model is not valid.

Since there are several variables affecting the failure rate of the wearout mechanisms, the end of life time has been defined to be that in which the time is equal to .5 t_{50} or when the failure rate for a single mechanism has reached .1 F/10^6 hrs., whichever is less. The failure rate predictions are therefore invalid beyond these times.

The Figures 3-7 through 3-12 illustrate the lognormal distribution's probability density function, cumulative distribution function, and hazard function for several combinations of means (t_{50}) and standard deviations (σ). The mean and sigma are given in the upper right hand corner of each graph.

One area of concern in the use of the lognormal distribution is its high sensitivity to variations in sigma. In all distributions defined thus far, a sigma of 1.0 is typical. Although it is evident that this value is fairly well accepted, slight deviations from it can significantly affect the model. To illustrate this, Table 3-5 shows the results of a few failure rate calculations at 10 years. This dependency can also be seen in Figure 3-12 which illustrates the hazard rate at the extreme value of a lognormal distribution with a mean life of 10^6 and a sigma which varies from .7 to 1.3.

TABLE 3-5:
HAZARD RATE AS A FUNCTION OF MEAN AND SIGMA

	Sigma				
t_{50}	.5	.9	1.0	1.1	1.5
10^6	$6.4x10^{-11}$	$1.3x10^{-7}$	$2.3x10^{7}$	$3.6x10^{-7}$	$8.1x10^{-7}$
$5x10^6$	$5.6x10^{-20}$	$2.1x10^{-10}$	$1.3x10^{-9}$	$4.8x10^{-9}$	$8.0x10^{-8}$
10^7	$2.9x10^{-25}$	$4.9x10^{-12}$	$6.1x10^{-11}$	$3.9x10^{-10}$	$2.1x10^{-8}$

From these numbers it can be seen that using a sigma of .9 or 1.1 for a projected t_{50} of 10^6 hours can mean the difference from 130 to 360 FITS (i.e., Failures/10^9 hours). For longer t_{50} the relative change may be 1 or 2 orders of magnitude although the actual failure rate values are much smaller. Large uncertainties in the sigma result in very large uncertainties of the failure rate.

While a sigma in the range of 1.0 is reasonable and consistent with theory, the range of sigma reported in published data vary widely. The ideal model would measure how aggressive a manufacturer's design rules and process controls were. For example, if every metal stripe carried the maximum current density and the process was marginal or had wide variations (i.e., step coverage varied from 10% to 60% with design rules specifying 30%), then there would be a considerable electromigration risk. Another design may have just a few stripes where the current density is maximum and never experience electromigration. While it may be possible to develop design analysis software tools which calculate current densities for every line and then sum them in

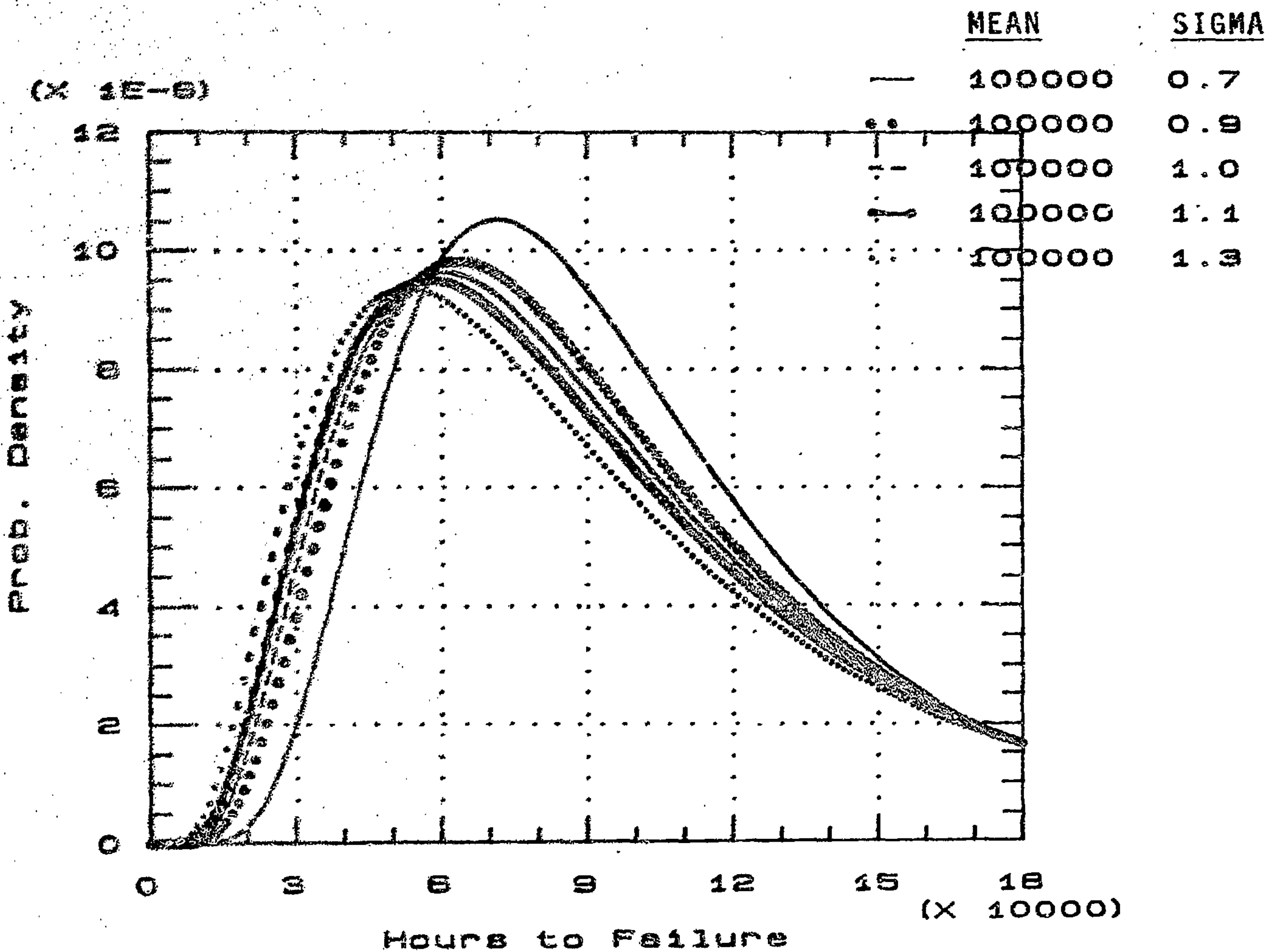


FIGURE 3-7: PROBABILITY DENSITY FUNCTION LOGNORMAL

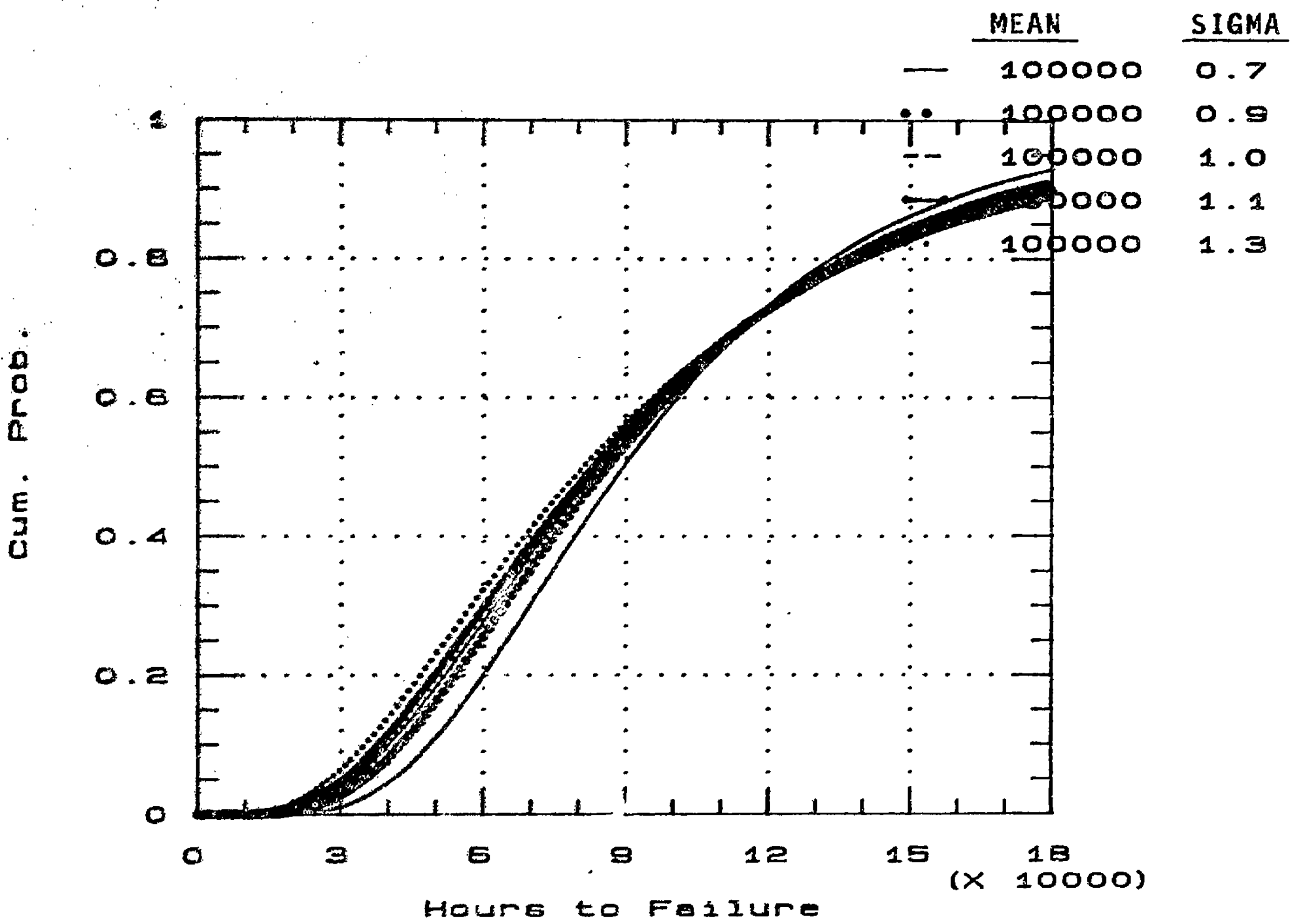


FIGURE 3-8: CUMULATIVE DISTRIBUTION FUNCTION LOGNORMAL

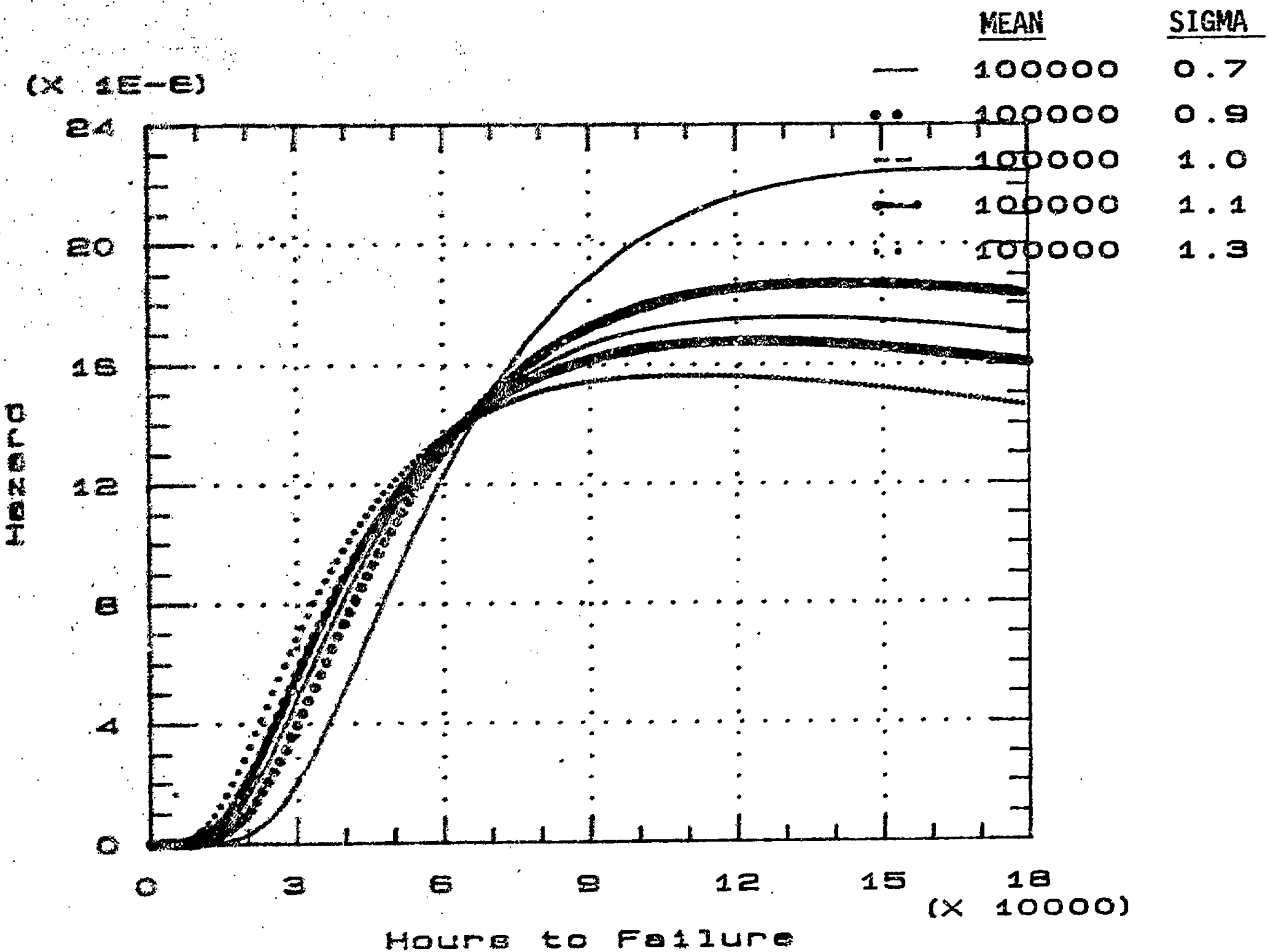


FIGURE 3-9: HAZARD FUNCTION LOGNORMAL

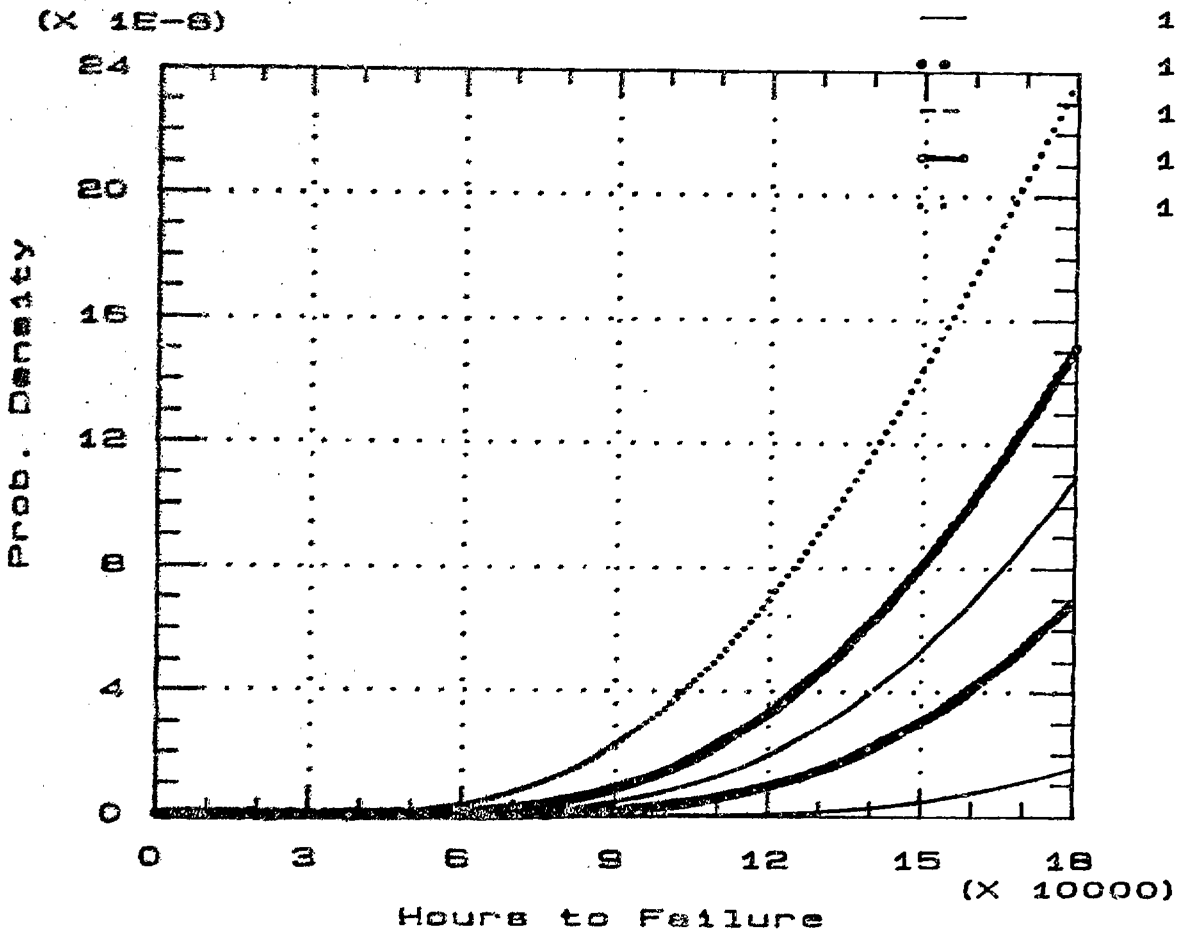


FIGURE 3-10: PROBABILITY DENSITY FUNCTION LOGNORMAL

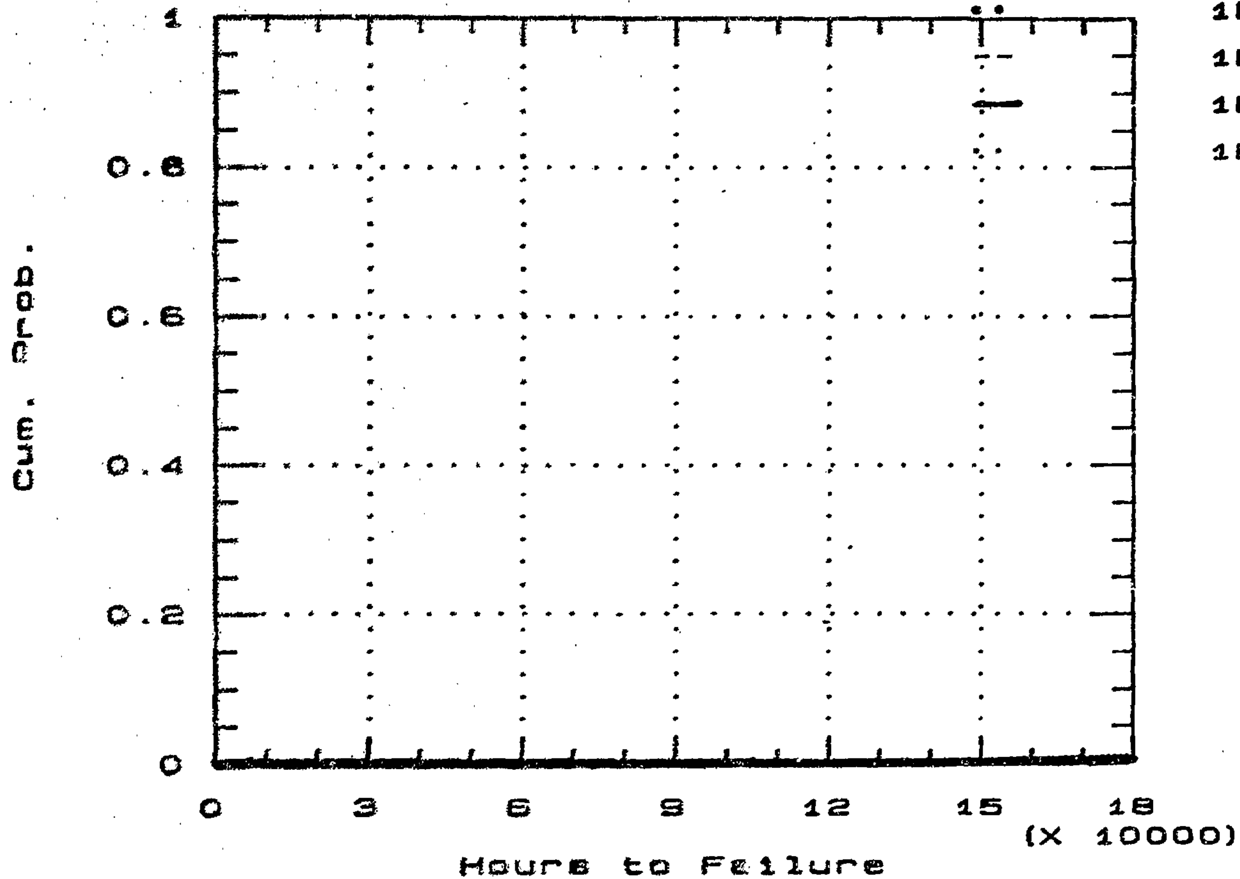


FIGURE 3-11: CUMULATIVE DISTRIBUTION FUNCTION LOGNORMAL

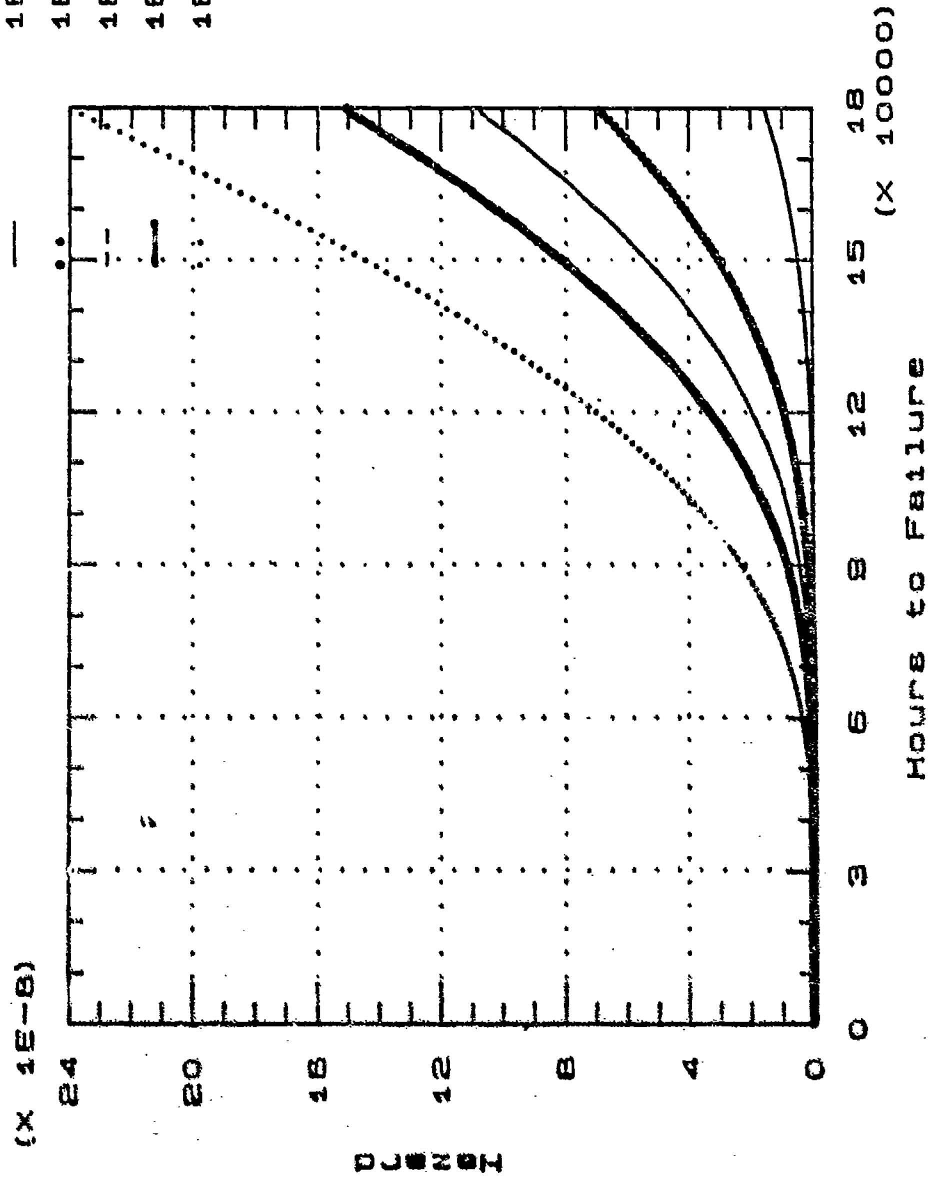


FIGURE 3-12: HAZARD FUNCTION LOGNORMAL

some manner, it is not likely that such information will ever be released publicly or to the DoD. Some manufacturers may also know that their step coverage and line width vary significantly, but such information is not likely to be released. Both of these factors make significant contributions to the sigma and make it very difficult to include in a general wearout prediction model. By using the default sigmas in the model, a typical failure rate for each mechanism can be obtained, with the understanding that there are wide variations.

The assumption in choosing an average sigma is that the random variations in the process and the statistical variations in measurement are accounted for in the sigma of the lognormal distributions (applicable for the wearout mechanisms only), since the distribution, mean and sigma were based on empirical data.

There was no data available which contradicts the use of the lognormal distribution, even at the extreme low end of the distribution which tends to be where its accuracy decreases. However, this is not a significant effect since the failure rate contribution of the lognormal distribution only becomes significant when the device is approaching its end of useful life, or its wearout period. Therefore, the wearout relationships will only provide an estimate for the end of life and very little information about the failure rate during the useful life of the device.

3.2 RELATIONSHIP TO THE GENERIC QUALIFICATION PROGRAM

This reliability prediction modeling effort, since it is for state of the art CMOS technology, should be coordinated with and related to other VHSIC/VHSIC-Like technology efforts such as yield enhancement and generic qualification.

Efforts were made to utilize data resulting from the Yield Enhancement and Generic Qualification efforts as input to the detailed model. Key elements of these programs that were of interest are the test structure testing performed on a regular basis. There are three elements to this testing:

(1) Parametric Monitor (PM) testing of individual transistors, diodes, and capacitors on every wafer. Undoubtedly there could also be a transistor with which to measure substrate current for the hot carriers t_{50} equation.

(2) Technology Characterization Vehicle (TCV) is used for periodic time dependent failure mechanisms for the same mechanisms used in prediction models. Thus, companies involved in Generic Qualification would have acceleration factors that might be used in their own models. It is also expected that fast wafer level tests will be developed and performed on every wafer run for electromigration, TDDB, and hot carriers.

(3) Standard Evaluation Circuits (SEC) are processed on a regular basis and regularly subjected to life tests. Perhaps, these could serve as the reference chip in the electromigration and TDDB equations.

In addition, the Generic Qualification program instills higher quality throughout the manufacturing process from design to assembly and shipment. Therefore, the short form model to be presented later has a quality factor associated with a manufacturer who can demonstrate this level of quality.

After investigating the potential use of these data sources, it was concluded that designing the model to include specific data from these sources would be very difficult, if not impossible due to the variability between manufacturers in the specific manners in which they obtain the data. For example, the SEC circuit provides much information useful for reliability studies but is not standardized between manufacturers. Therefore, it was concluded that the level of standardization necessary for input to a reliability model has not yet been achieved. In fact, in many cases it would be undesirable to have a very standardized method of determining reliability characteristics. This is due to the fact that there are many variables in the design and fabrication of a circuit and the best manner to test for their reliability characteristics is not always the same and may be unique for a particular process.

Since it is very important to make use of the data from these efforts, IITRI and Honeywell believe that an effective manner in which to accomplish this is to assign a base failure rate (for electromigration, time dependent dielectric breakdown, and hot carrier effects) as a function of a manufacturers ability to prove they have the failure mechanisms under control.

This approach has merit because well designed circuits typically exhibit very low failure rates for these mechanisms when used in typical applications. In fact, there has been very few instances of field failures reported due to these mechanisms. The database developed for this modeling effort supports this view since it also contains very few failures due to these mechanisms. These low failure rates are then reflected in the quality factor for those manufacturers on the QML (Qualified Manufacturers List) for the short form model and in the t_{50} expressions for the wearout mechanisms in the detailed model. This approach is consistent with the generic qualification effort which allows some flexibility in the methods used by the manufacturer in proving the adequacy of a design.

The detailed model accounts for the manufacturing process capabilities primarily in the defect density factor. Presumably, a manufacturer with good process controls such as those on a QML or QPL (Qualified Products List) will have a lower defect density than one without those controls in place. For this reason the differences between the QML or QPL status of a manufacturing process should inherently be accounted for in the defect density.

The short form model, however, cannot use defect density as an input since most users of the short form model will rarely have access to specific values. Therefore, a default defect density was derived. Additionally, the short form model includes a factor based on the QML or QPL status of the manufacturing process. This factor, discussed further in Section 7.1.4, was based on the observed variation in reliability between manufacturers, presuming that these differences are accounted for in the QML process.

Guidelines for one method of calculating the defect density for both oxide and metal are given in Appendix B. These are calculated separately indicating that if only the oxide defect density is known, it can be used and the default condition for metal defect density can be used.

4.0 DATA COLLECTION AND DATABASE DEVELOPED FOR THIS PROGRAM

4.1 DATABASE

A database was developed to hold and analyze the empirical data collected in this effort. This database has been developed for an IBM PC and contains provisions for entering the following information about the device itself, the stresses it was exposed to, and the results of those stresses:

<u>Device</u>

Part Number
Manufacturer
Part Description
Package Type
Number of Pins
Thermal Resistance
Technology
Gate Count
Feature Size
Die Dimensions
Metal Length
Metal Width
Number of Metal Layers
Metal Material
Gate Length
Oxide Thickness
Oxide Area
Metal Defect Density
Oxide Defect Density
Yield
ESD Susceptibility

<u>Stress</u>

Power Dissipation
Test Type
Junction Temperature
Current Density
Oxide Voltage
Test Conditions
Ambient Temperature

<u>Test Results</u>

Number Tested
Number Failed
Time to Failure
Failure Mechanism
Failure Mode

The type of test information collected was primarily operating life test, burn in, and various environmental tests. The failure causes, feature size, and die area of a profile of this database is given in the following sections. The detailed data contained in this database is given in Appendix D.

4.1.1 Failure Cause Profile

Since the objective of this modeling effort was to quantify the failure rate of each failure mechanism, knowing the cause of each observed failure was very important. The cause of failure was known for approximately half of all failures.

Table 4-1 illustrates the number of observed failures as a function of the failure cause (failure class) and test type. Each observed failure that had a reported associated failure cause (failure mode, mechanism, or cause) was classified into one of the failure classes listed in this table, thus facilitating failure rate modeling of each failure class.

One data source contributed a large number of failures for which the failure class was not entirely defined. Therefore, Table 4-2 summarizes the same information as Table 4-1 but excludes that data source. As explained in Section 3.0, the unknown data was assumed to have the same relative weightings as the known failures when performing the actual modeling. This modeling was accomplished by increasing the predicted failure rate of each of the known mechanisms by a given percentage. In this manner all failures are accounted for.

TABLE 4-1:
TOTAL NUMBER OF FAILURES OBSERVED AS A FUNCTION OF TEST TYPE AND FAIL CLASS

Failure Class	Life Test	Temperature Cycling	Environmental	Total
Unknown	789	54	4	847
Assembly	21	0	0	21
Package	24	214	0	238
Metal	62	3	6	71
Misc.	44	4	5	53
Oxide	274	7	0	281
Contamination	603	5	0	608
Wearout	7	0	0	7
Total	1824	287	15	2126

TABLE 4-2:
NUMBER OF FAILURES OBSERVED AS A FUNCTION
OF TEST TYPE AND FAIL CLASS EXCLUDING ONE
DATA SOURCE

Failure Class	Life Test	Temperature Cycling	Environmental	Total
Unknown	437	54	4	495
Assembly	21	0	0	21
Package	22	214	0	236
Metal	62	3	6	71
Misc.	44	4	5	53
Oxide	111	7	0	118
Contamination	48	5	0	53
Wearout	7	0	0	7
Total	752	287	15	1054

4.1.2 Feature Size Profile

The distribution of feature sizes present in the database (in those cases where it was known) is given in Figure 4-1. Although devices with feature sizes in the 3-5 micron area were beyond the scope of this study, they were included to make provisions in the database to identify trends as a function of feature size. A weighted (by number of tested devices) average of feature sizes in this database is 2.0 μm.

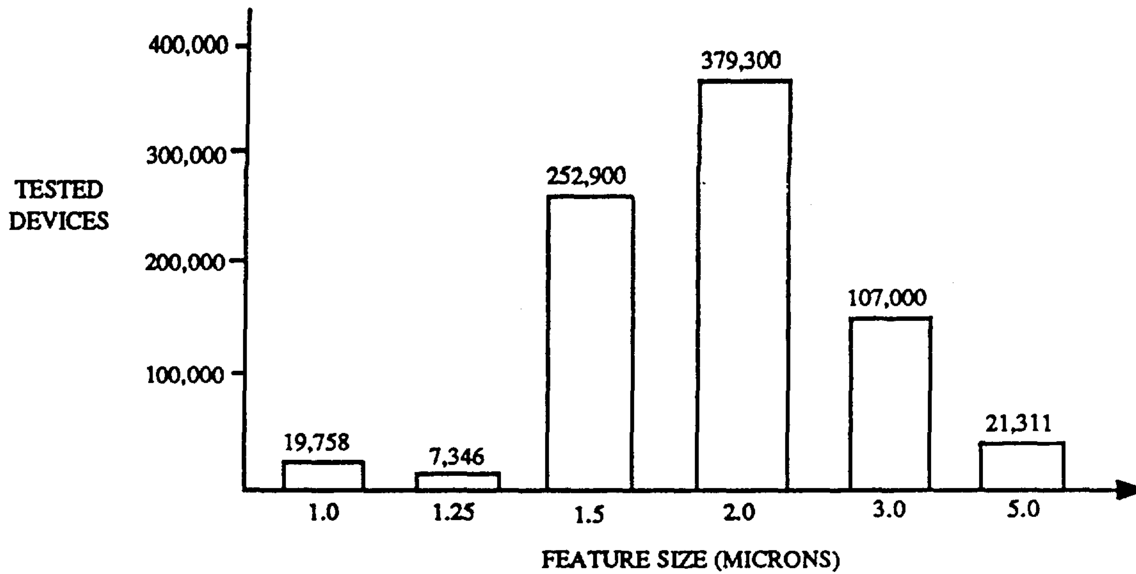


FIGURE 4-1:
FEATURE SIZE PROFILE

4.1.3 Die Area Profile

The distribution of die areas present in the database is given in Figure 4-2. The weighted die area by number of devices is .21 cm^2.

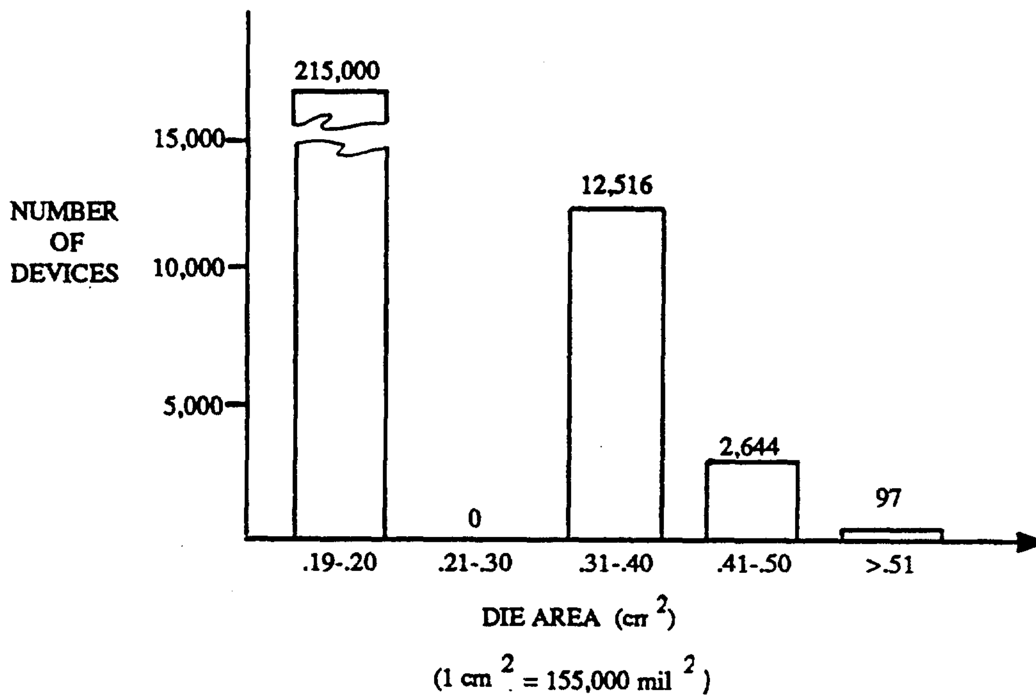


FIGURE 4-2:
DIE AREA PROFILE

5.0 FAILURE MECHANISM CHARACTERIZATION

5.1 OXIDE FAILURE RATE

5.1.1 Oxide Early Life Failures

The early life failure rate for oxide related failure mechanisms was developed using the methodology outlined in Section 3.0. Table 5-1 summarizes the data used in development of this factor. In this table, the accelerated time interval is the effective time interval (in 10^6 hrs.) at 25°C (using the oxide temperature acceleration factor with an activation energy of .3 eV). The accelerated part hours are the total effective observed oxide part hours at 25°C in each time interval, and the last column is the number of observed oxide failures occurring in each interval.

TABLE 5-1:
OXIDE FAILURE DATA

Equivalent Time Interval at 25°C (10^6 hrs.)	Accelerated Part Hours (10^6 hrs.)	Number of Failures
0-0.002344	644.832020	3
0.002345-0.008204	1601.110137	13
0.008205-0.016950	1648.146367	1
0.016951-0.024417	1372.043816	19
0.024418-0.048834	4309.957812	229
0.048835-0.049224	6.008332	2
0.049225-0.050446	15.044018	1
0.050447-0.138452	524.665804	2
0.138453-0.193123	35.612394	3

Selecting two discrete ranges for the regression solutions yields the following data in Table 5-2. These ranges were defined based on the quantity of data. For example, there was a large quantity of data from devices that were tested at an equivalent time of .048834, therefore 0-.048834 was one of the ranges chosen. It should be noted here that relatively large ranges of time had to be grouped into each of the two ranges because in many cases sources reported failures occurring within a time interval. For example, if the devices on test were tested only at 500 hours, the failures observed actually occurred prior to 500 hrs., although the exact time is not known.

TABLE 5-2:

OXIDE EARLY LIFE SUMMARIZED FAILURE RATE

Effective Range	Midpoint	Effective Part hrs. (10^6)	Number of Failures	Failure Rate (F/10^6 hrs.)
0-.048834	.024417	9576	265	.0277
.048835-.193123	.12098	582	8	.0137

Regressing on this data and adjusting the time constant to insure that the cumulative failure rates are equivalent for the predicted and observed cases yields:

$$\lambda_{ox}(t) = .0331\ e^{-7.7\ t}$$

Since failures of unknown causes represented 58% of the data, the failure rate derived here should be multiplied by 2.38 to compensate for the unknown failures. This assumes that the unknown failures have the same relative rate of occurrence between mechanisms as do the known failures. Since the cumulative failure rate is directly proportional to the constant (in this case .0331), this constant should be multiplied by 2.38, yielding the following hazard rate:

$$\lambda_{ox\ early\ life} = .0788\ e^{-7.7\ t}$$

Combining the effects of temperature and screening time yields:

$$\lambda_{ox\ early\ life} = .0788\ e^{-7.7\ t0}\ A_{T_{ox}}\ e^{-7.7\ A_{T_{ox}}\ t}$$

There are several factors that already affect the early life oxide failure rate that are not present in this expression. One such factor is the oxide electric field. To be able to include this factor the electric field would need to be known for all devices in the database, since it is an empirical relationship. Unfortunately, the electric field was rarely reported, making it impossible to include this effect. This early life oxide model therefore, as with the other early life failure rates, represents an industry wide average observed hazard rate.

The oxide wearout hazard rate however, has included the effects from factors such as electric field since it is a more theoretically based factor.

5.1.2 Oxide Wearout

Time dependent dielectric breakdown is considered an oxide wearout mechanism and has empirically been shown to follow the lognormal time to failure distribution. Since a lognormal distribution is uniquely defined with a mean (t_{50}) and standard deviation (σ), the intent of the effort to quantify the oxide wearout failure rate was to quantify the t_{50} and σ as a function of applicable stress and fabrication variables.

Although many researchers have studied time dependent dielectric breakdown thoroughly, the basic physics of failure is still not completely understood. This fact makes it difficult to derive a general t_{50} model valid for all manufacturing processes in all situations. As explained in Section 3.0 of this report, however, the wearout mechanisms only provides an indication of an approximate end of life time and contribute very little to the failure rate in the useful life of the device. Therefore, if a manufacturer can prove that the t_{50} for oxide wearout for his particular process is much greater than the life expectancy of a part, this factor can essentially be ignored in the failure rate calculation.

For these reasons, the failure rate for oxide wearout (TDDB) was derived as a function of temperature, electric field in the oxide, oxide area and defect density. These relationships were derived from empirical data from various researchers on oxide reliability. The following sections summarize the development of these factors.

5.1.2.1 Temperature Acceleration Factor

The basic temperature acceleration follows the Arrhenius relationship of the following form,

$$A_{T_{ox}} = \exp\left[\frac{-Ea}{K}\left(\frac{1}{T_J} - \frac{1}{T_0}\right)\right]$$

where $A_{T_{ox}}$ = Temperature Acceleration Factor for Oxide

T = Temperature (in degrees Kelvin)

T_0 = Reference Temperature = 298°K

K = Boltzman's Constant = 8.63×10^{-5} (ev/°K)

T_J = Average Junction Temperature (°C)

Ea = Activation Energy (eV)

Based on test results contained in the literature, the commonly accepted activation energy is .3 eV, which has also been experienced by Honeywell, and therefore is the nominal value to be used in this model. The temperature acceleration factor for TDDB is therefore the following:

$$A_{T_{ox}} = \exp\left[\frac{-.3}{K}\left(\frac{1}{T_J} - \frac{1}{298}\right)\right]$$

5.1.2.2 Electric Field Acceleration Factor

Crook (Reference 27) had originally derived a form for the acceleration factor due to the electric stress applied across an oxide. This form was:

$$A_{EF} \alpha \exp\left[\frac{E_{REF} - E_S}{E_0}\right]$$

where E_{REF} = Reference Electric Field = 3MV/cm

E_S = Actual Electric Field

E_0 = Normalizing Electric Field

Domangue (Reference 31) has conducted tests at various electric field stresses (3, 4, and 5 MV/cm) from which an acceleration factor can be obtained. Analysis of his data yields an E_0 = .1324 MV/cm and therefore an acceleration factor can be stated as follows:

$$A_{EF} = \exp\left[\frac{3 - E_S}{.1342}\right]$$

More recent work by Hu (Reference 39) on oxides closer to those types and thicknesses used in VHSIC circuits has shown that the time to breakdown is related to the electric field in the following manner:

$$t_{BD} \; \alpha \; e^{\frac{B+H}{E_{OX}}}$$

where B = 240 MV/cm

H = 80 MV/cm

It can be seen that this acceleration factor has enormous changes for reasonable changes in E_{OX}. For example, a 5 volt part that has 300 $\overset{\circ}{A}$ and 100 $\overset{\circ}{A}$ oxides (E_{OX} of 1.67 and 5 MV/cm respectively) would have acceleration factors differing by 56 orders of magnitude.

Hu had used a smaller number, 192, instead of 320 for comparing the 1% cumulative failure points as opposed to the 50% cumulative failure point, arguing that the value should be smaller for defect related breakdown than for near intrinsic breakdown. Since in this model, the 1% cumulative failure point is of much more interest than the 50% point, the constant of 192 will be used in this factor. Therefore, using an exponent of 192 and choosing the $A_{V_{OX}}$ term to agree with empirical data at high electric fields yields:

$$A_{V_{OX}} = e^{-192\left(\frac{1}{E_{OX}} - \frac{1}{2.5}\right)}$$

In addition to the electric field, various researchers have also observed a relationship between the acceleration factor and oxide thickness. Derivation of this factor (from Reference 26) based on empirical studies yields:

$$\text{Acceleration} \ \alpha \ 4.2 \log T_{OX} - 6.95$$

Therefore, the factor that could be used in the oxide model is therefore:

$$A_{Tox} = \exp\left[\frac{4.2 \log T_{OXR} - 6.95}{4.2 \log T_{OX} - 6.95}\right]$$

where T_{OXR} = Reference oxide thickness
T_{OX} = Actual oxide thickness

Since the variation in this factor is very small compared to the electric field acceleration factor, it was not included in the model since the uncertainties in the electric field factor are much larger than the oxide thickness factor itself.

Table 5-3 summarizes some of the acceleration factors found in the literature.

5.1.2.3 Die Area and Defect Density

This section discusses the relationship between die area, defect density, and yield. Although it is included in this section, the discussion of yield effects is not specific to oxide. In this model, there are separate defect densities for oxide and metal, although they use the same default value, which is a function of feature size.

Phillips (Reference 28) has suggested the use of extreme value statistics to derive the area/defect density relationship of gate oxides. In extreme value statistics, the hazard rate can be closely approximated by the exponential function. Thus,

$$h(x) = \frac{1}{1-F(x)} \frac{d\,F(x)}{dx}$$

TABLE 5-3:
ELECTRIC FIELD ACCELERATION FACTOR (A_{EF})
AND ACTIVATION ENERGY (E_a) IN LITERATURE

Reference	Material	T_{ox}(A)	Temp. (C)	A_{EF} (1/ (MV/CM))	E_a (eV)
29	Poly	> 400	25-160	10^7	.3-25
30	Al	450	85-250	$10^{1.5+.5}$	2.1
31	Poly	390	25-150	$10^{2.0}$	.36
32	Poly	400	-	$10^{1.7}$	.26
33	Poly	100-200	-	10^4	1.0
34	Poly	100-400	-	$10^{5.6}$	-
35	Poly	100	25-150	$10^{1.87}$-$10^{2.0}$	.3
36	Poly	200	20-250	$10^{2.5}$	.3
37	Poly	60-100	170-250	$10^{1.74}$-$10^{1.9}$	1.0-1.1
38	Poly	110	25-275	$10^{1.41}$	.23

From the data in Reference 28 and from extreme value statistics, for a gate oxide area A_1 with average breakdown E_1

$$h_1(E) = \exp\ (S_N(E\text{-}E_1)/S_V\text{-}Y_N)$$

and similarly for a gate oxide area A_2 with average breakdown E_2

$$h_2(E) = \exp\ (S_N(E\text{-}E_2/S_V\text{-}Y_N)$$

Thus;

$$h_1\ (E)/h_2\ (E) = \exp\ (S_N(E_2\text{-}E_1)/S_V)$$

It is noted the S_N and Y_N are constants that depend only on the sample size and that S_V is the standard deviation and the same for both distributions (A_1 and A_2).

It is also clear from the data presented, which is supported by the extreme value statistic theory, that

$$\ln(\text{-}\ln\ (1\text{-}F_1)) - \ln\ (\text{-}\ln(1\text{-}F_2)) = \ln(A_1/A_2)$$

and

$$S_N(E\text{-}E_1)/S_V - S_N\ (E\text{-}E_2)/S_V = \ln(A_1/A_2)$$

Thus;

$$S_N\ (E_2\text{-}E_1)/S_V = \ln(A_1/A_2)$$

and

$$h_1(E)/h_2(E) = \exp\ (\ln(A_1/A_2) = A_1/A_2$$

Thus, the ratio of the hazard rates is equal to the ratio of the gate oxide areas in extreme value statistics.

This factor indicates that if reliability data is available on a circuit such as a SEC, the hazard rate could be extrapolated to the entire chip by knowing the gate oxide areas. Or, if the average areas of the devices in the database is known, it can be used as the reference area.

The following discussion summarizes another analysis that was conducted to determine the relationship between both area/defect density and hazard rate.

If f(t) is the failure density function, then the cumulative failure density function is given by:

$$Q(t) = \int_0^t f(t)\, dt$$

Crook (Reference 27) used another expression for Q(t) which was said to be from Li and Maserjian (Reference 41), which was actually obtained from Price (Reference 42). Price derived the following expression in 1970 from Bose-Einstein statistics, stating that earlier models using Boltzman statistics were inaccurate;

$$Q_S(t) = 1/(1+1/A_S D_S)$$

A_S is the area, D_S is the defect density and $Q_S(t)$ is the cumulative failure density. Price derived this expression for integrated circuit yields. On the assumption that the effective defects are randomly distributed along two dimensions and are thus indistinguishable, Li and Maserjian found the equation applicable for the effective defect density for time dependent dielectric breakdown. Note that D or D_S is a function of time. In the discussion that follows the subscript s indicates that these values are for the stress test structure from which data is generated in the laboratory.

With the above formula it follows that for a second chip with area A_0 and the same defect density the cumulative failure density is given by:

$$Q_0(t) = 1/(1+(A_s/A_0)(1/Q_S(t)-1))$$

In a similar fashion it can be shown that for a third chip with the same area as the second chip A_0, but a different defect density a cumulative failure density function is given by:

$$Q_n(t) = 1/(1+(D_0/D_n)(1/Q_0(t)-1))$$

If the last two equations are combined, the resulting equation becomes

$$Q_n(t) = 1/(1+(D_0A_S/D_nA_0(1/Q_S(t)-1))$$

or

$$Q_n(t) = 1/(1+(D_SA_S/D_nA_n)(1/Q_S(t)-1))$$

From this expression it is clear that as the defect density and/or the gate oxide area gets large, the cumulative number of failures gets large.

Crook also showed that the hazard rate (the probability that a device will fail in the time (t+dt) if it has already survived until t) is found by differentiating Q(t) and amounts to

$$h_n(t) = 1/(1-Q_n(t))$$

From the above discussion a failure rate for time dependent dielectric breakdown of a given chip can be found if all of the following are known:

(1) the sigma and the t_{50} of the TDDB failures of a test structure with a known defect density and area;

(2) voltage and thermal acceleration factors if the test structure work was performed at accelerated conditions;

(3) the area and defect density of the given chip.

Unfortunately, the calculations involve the integral of a complicated function. To deal with this problem numerical integration was used to assess the effect of changing the area and defect density. It immediately became clear that for a small number of cumulative failures, the formulas could be greatly simplified. From the last cumulative failure density function expression above, if $Q_S (t)$ is small, then

$$Q_n (t) = 1/(D_S A_S/D_n A_n)\,(1/Q_S (t))$$
$$= D_n A_n Q_S(t)/D_S A_S$$

Thus, the cumulative failure density function is directly proportional to the defect density and the area of the chip. Since the cumulative failure density function is the integral of the failure density function, it follows that the failure density function is directly proportional to the area and defect density. For the first few failures the instantaneous failure rate is equal to the failure density function, and thus it is directly proportional to defect density and area. Thus, in the first approximation to double the chip area (or defect density) is to double the chip failure rate.

In the previous paragraphs some relationships were established between the cumulative failure probability Q_n, and the number of defects, D, and the chip area, A. These relationships were based on a model developed by Price (Reference 42) using Bose-Einstein statistics. A more general defect model was derived by Stapper (Reference 43). In this model the probability defect density function is related to the gamma distribution. For this model the yield is given by

$$Y = 1/(1+AD_0/S)^S$$

where A is the chip area, D_0 the average defect density, and S a shape parameter. This model assumes that the defects have a given distribution pattern across the wafer. In the limiting case where S approaches 0, the distribution is a delta function, meaning the defect density is constant and all defects are randomly distributed and independent. This condition leads to the Poisson yield estimate

$$Y = e^{-D_0 A}$$

Also it can be seen that when the S of the Stapper model is 1, the yield model reduces to

$$Y = 1/(1+AD_0)$$

which was described previously as the Price model, but actually used earlier by Seeds (Reference 44). In this case the defect density distribution is exponential. A comparison of these and two other yield models is shown in Figure 5-1. The Poisson model is the most pessimistic and the Seeds model is the most optimistic. The Stapper model can be adjusted by the shape parameter to cover the area in between. The following derivation is similar to that presented previously with the exception that the more general Stapper model is used.

The cumulative probability of failure plus the yield must add to 1. Thus

$$Q(t) = 1 - Y = 1 - 1/(1 + D_0 A/S)^S$$

If $Q_n(t)$ is the cumulative failure probability of a circuit with D_n average defects and A_n area, and $Q_0(t)$ is the cumulative failure probability of a different circuit with area A_n and the same average defects, then

$$D_n(t) = \frac{S}{A_n}\left[\frac{1}{[1-Q_n(t)]^{1/S}} - 1\right] = D_0(t) = \frac{S}{A_0}\left[\frac{1}{[1-Q_0(t)]^{1/S}} - 1\right]$$

If the above is solved for $Q_0(t)$ in terms of $Q_n(t)$ and the two areas, we get

$$Q_0(t) = 1 - \left[1 \Big/ \left[1 + \frac{A_0}{A_n}\left[\frac{1}{[1-Q_n(t)]^{1/S}} - 1\right]\right]\right]^S$$

In a similar fashion

$$Q_0(t) = 1 - \left[1 \Big/ \left[1 + \frac{A_0 D_0}{A_n D_n}\left[\frac{1}{[1-Q_n(t)]^{1/S}} - 1\right]\right]\right]^S$$

The above equation relates the cumulative failure probability of a given device to that of another device as a function of area and defects.

To help understand this relationship a number of graphs were generated. Figures 5-2, 5-3, and 5-4 show the effect of the shape factors for different A_0D_0/A_nD_n ratios. From these graphs it is clear that when the area defect factor is near unity (that is, the chips have approximately the same areas and defect distributions), the shape factor S has modest effects on the relative failure probability. When the area defect factor is large (that is, the Q_0 device has a much larger area

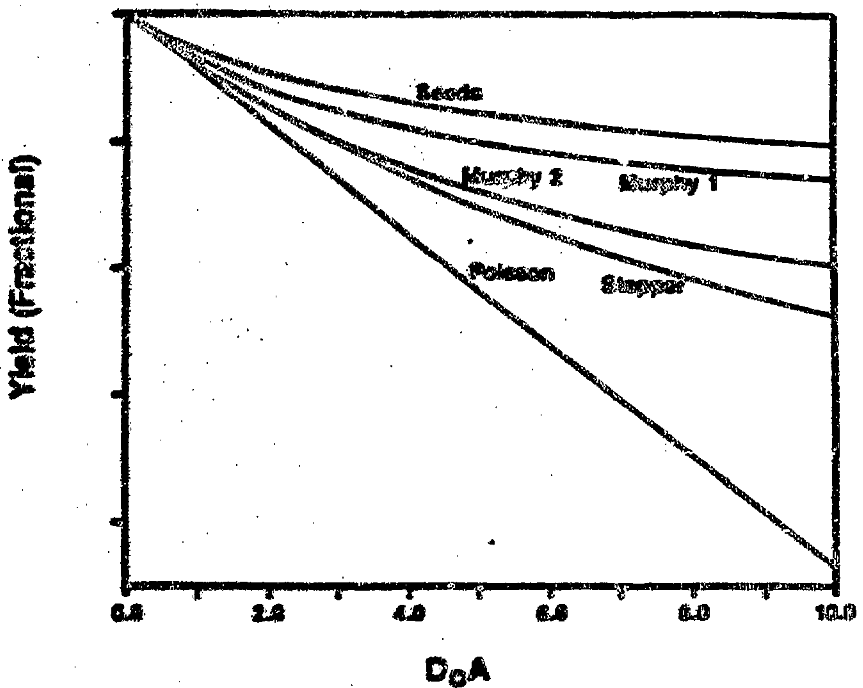


FIGURE 5-1: YIELD AS A FUNCTION OF DEFECTS AND AREA FOR DIFFERENT MODELS

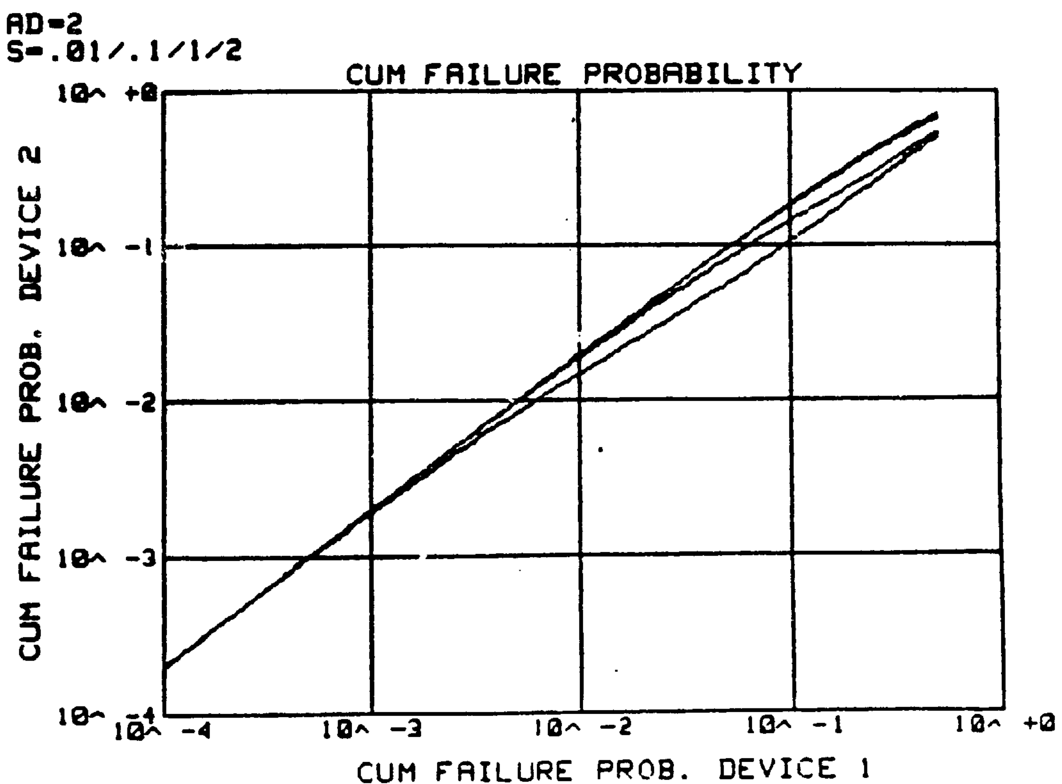


FIGURE 5-2: CUM FAILURE PROBABILITY FOR $A_oD_o/A_nD_n = 2$ AND S = .01, .1, 1, AND 2

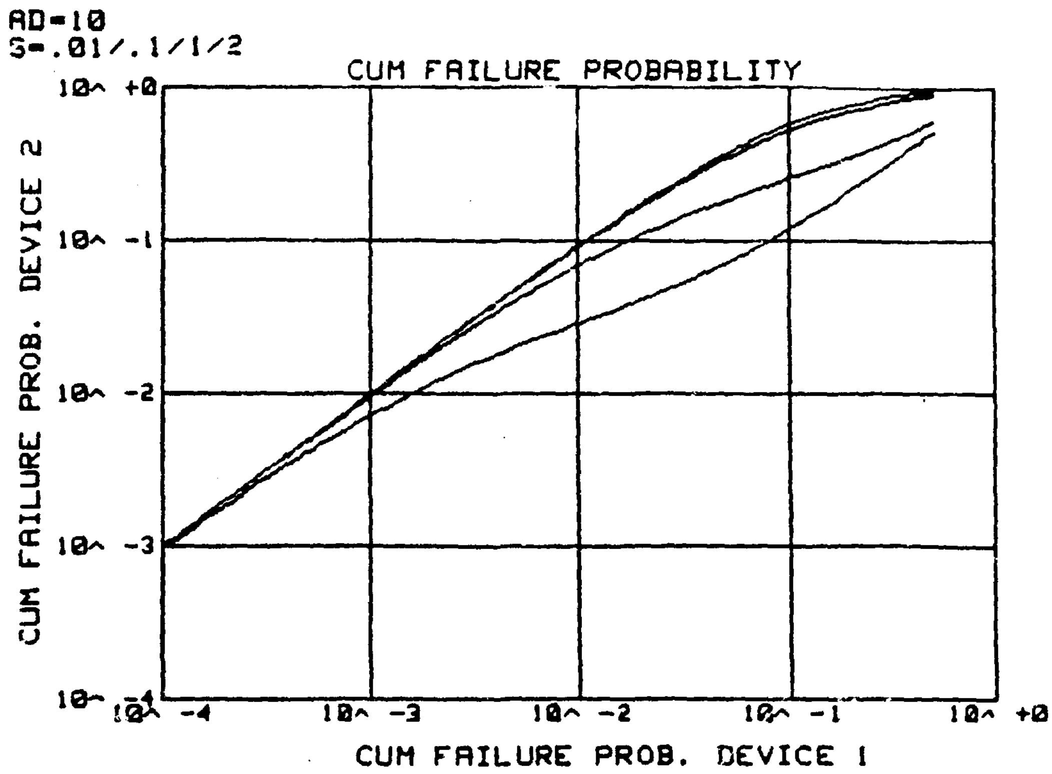


FIGURE 5-3: CUM FAILURE PROBABILITY FOR $A_oD_o/A_nD_n = 10$ AND S = .01, .1, 1, AND 2

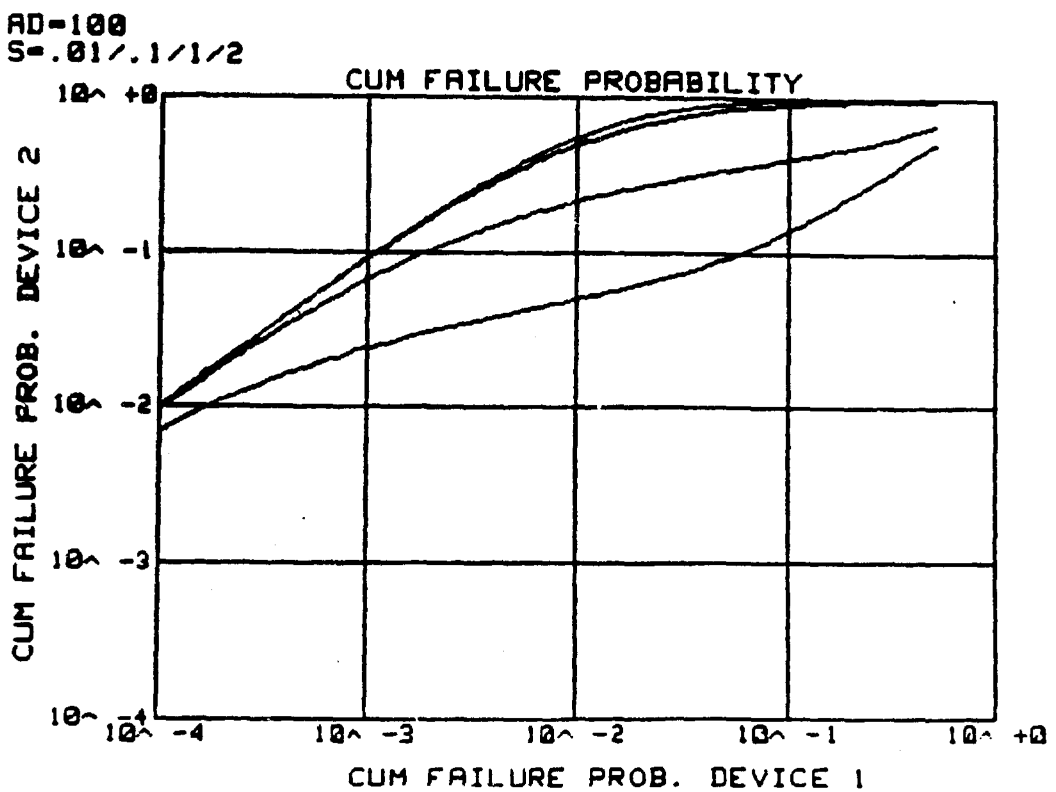


FIGURE 5-4: CUM FAILURE PROBABILITY FOR $A_oD_o/A_nD_n = 100$ AND S = .01, .1, 1, AND 2

and/or defect density), then the effect of the shape factor is more pronounced. Stapper indicated that IBM had seen S range from 0.1 to 2.2 depending upon the type of defect, however, it takes substantial quantities of data to establish an S value.

The model presented herein assumes that the areas and defect densities of the devices used to derive these factors (from the database) are similar to those that predictions will be performed on, and therefore that the direct relationship between area/defect density and hazard rate is valid.

Figure 5-5 demonstrates the effect of the area defect factor when S=1. This is the Seeds or Price model. From this graph it can be seen that for cumulative failure probabilities less than 10%, the cumulative failure probability of one device is equal to the defect area factor times the cumulative failure probability of the other device. This demonstrates graphically that for the S=1 model the cumulative failure probability (and thus, the failure rate) is directly proportional to the level of defects and the chip area. Intel (Reference 27) has also presented data to support this theory.

Figure 5-6 shows a slightly different area defect factor effect when S=.01 which is close to the Poisson defect distribution. In this instance the curves deviate from the asymptote at a slightly lower point. Again the cumulative failure probability is directly related to the area defect factor.

The above analysis seems to indicate that for the first few failures, which are the only ones of interest here, the probability of failure is directly proportional to the defect level and to the chip area. This analysis is based on yield theory and has been demonstrated to be consistent with the Phillips model (Reference 28) to be discussed later.

In the previous discussion a general model was presented to relate the cumulative TDDB failures for one device to that for another. The key factors were device area and number of defects. This reliability model was based on the Stapper yield model and includes a curve fitting or shape factor S. The following model analyzes how some published data fits that model.

In 1979 Intel published TDDB data for a number of different sized capacitors (Reference 27). This data showed the cumulative number of failures in a given period of time for populations of different sized capacitors. Figures 5-7 and 5-8 illustrates those data points plotted. The four lines represent four area/defect ratios consistent with Intel's data. The different capacitors they used were all from the same set of wafers so that the defect levels should have been consistent

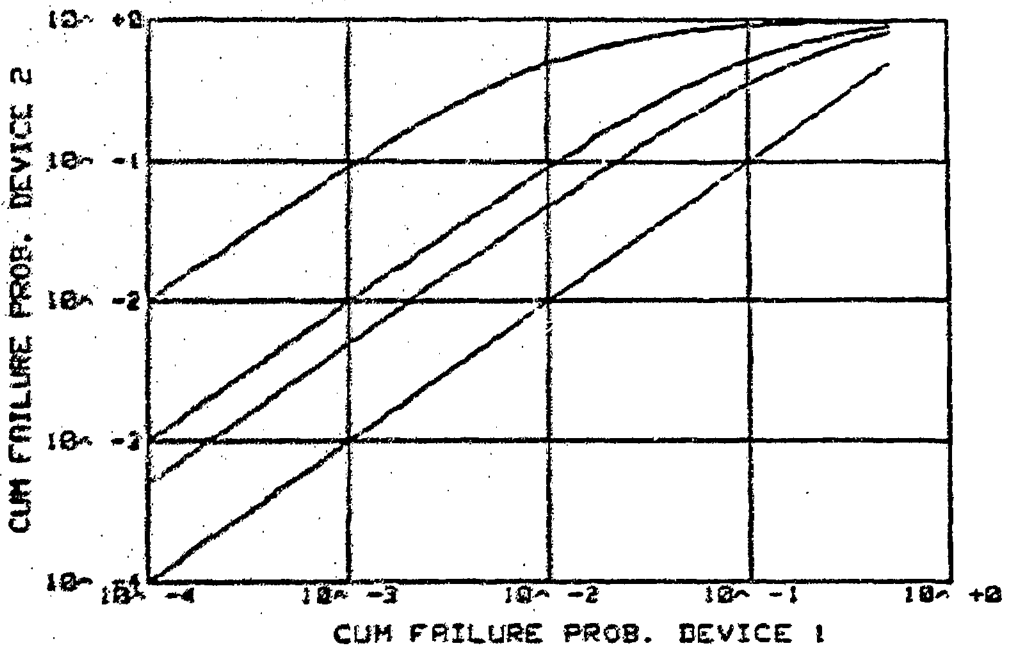


FIGURE 5-5: CUM FAILURE PROBABILITY FOR S = 1 AND AD = 1, 5, 10 AND 100

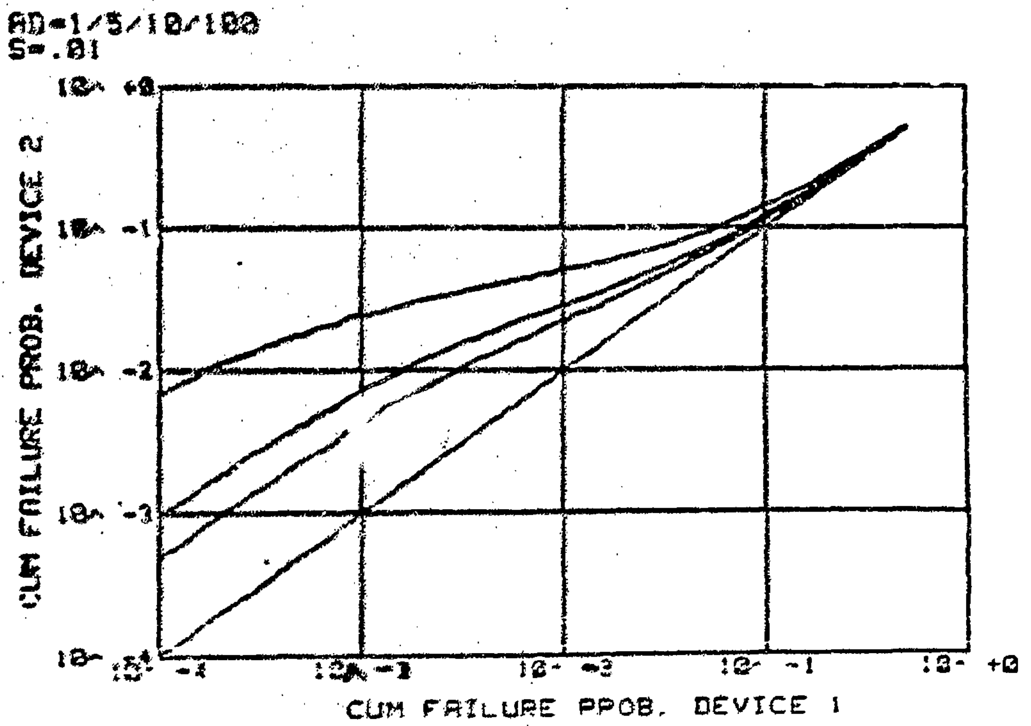


FIGURE 5-6: CUM FAILURE PROBABILITY FOR S = .01 AND AD = 1, 5, 10 AND 100

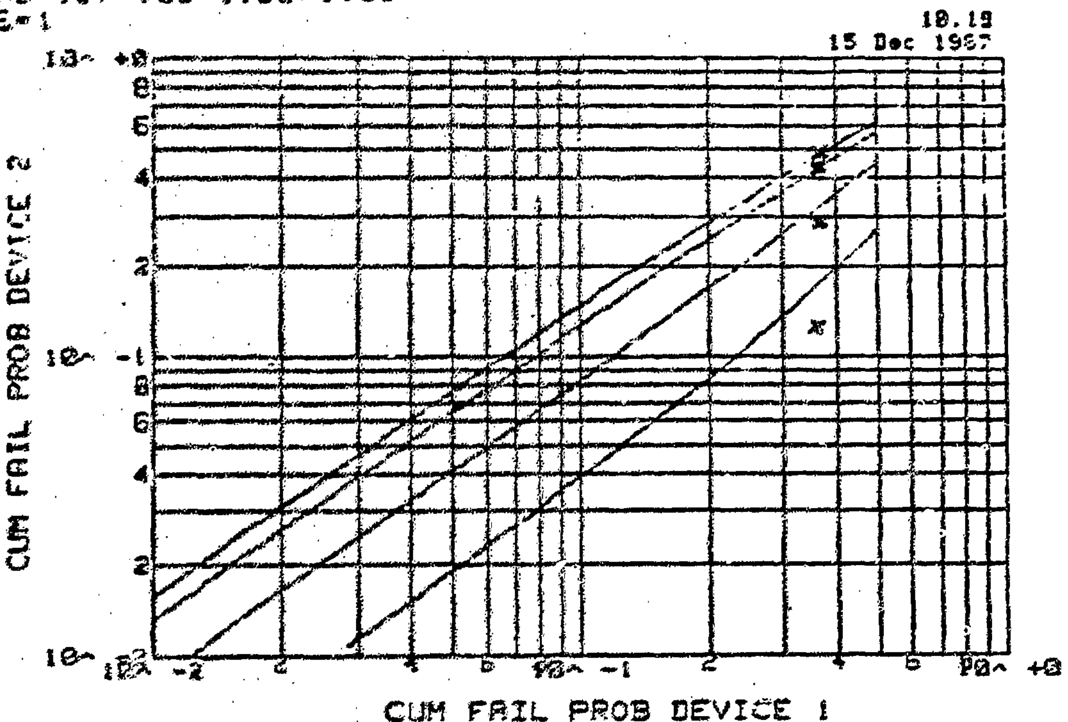


FIGURE 5-7: CUM FAILURE PROBABILITY

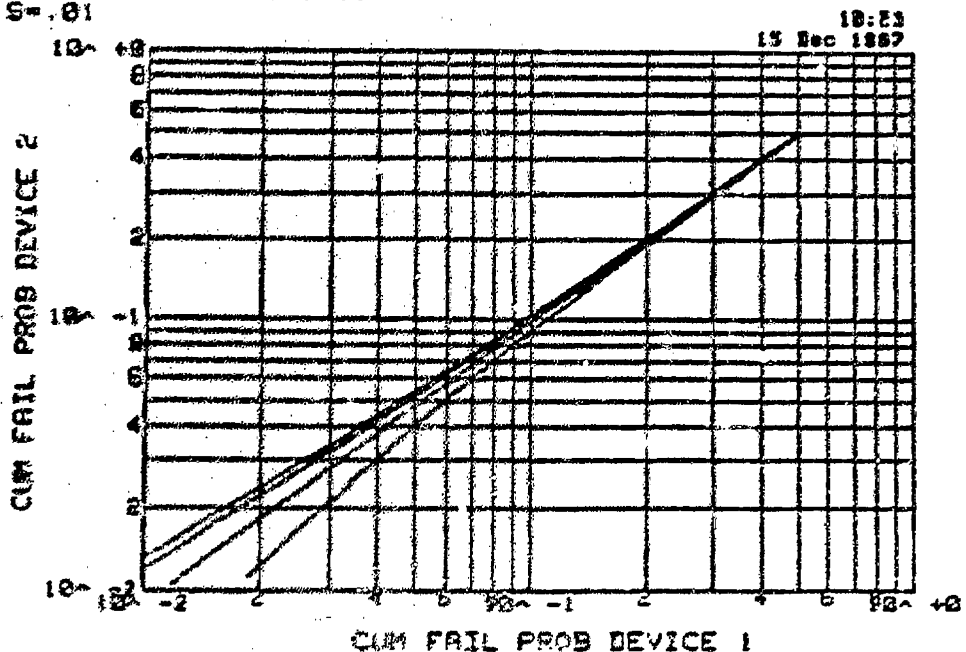


FIGURE 5-8: CUM FAILURE PROBABILITY

The data for S=1, representing the Seeds model, seems to show the right trend. Indeed, this was the model that Intel used. To try to have the model better fit the data, two approaches were tried. First, curves for different values of S (from .2 to 10) were generated. Second, part 1 in the graph was changed from first to middle to last data point. The results from that data are summarized in Table 5-4.

TABLE 5-4:
STAPPER MODEL WITH VARIOUS S VALUES

Device ($x10^6 \mu^2$)	Cum Fails (in $3x10^6$ sec.)	Part 1 Standard S = 1	Part 3 Standard S = 1	Part 5 Standard S =1	Part 3 Standard S = .3	Part 3 Standard S = 4
.7	12%	-	16%	16%	23%	15%
1.55	29%	24%	32%	31%	34%	32%
1.9	36%	27%	-	34%	-	-
2.5	46%	32%	43%	42%	42%	44%
3.0	44%	36%	48%	-	43%	51%

While in general it can be said that smaller values of S tend to close or narrow the range of the data points, reasonable values of S do not bring the lowest point down enough (Intel's 12% point) without significantly raising the data points for the larger areas. Because the Intel data is not perfect (the largest capacitor actually had fewer failures than the next largest one), it is not likely that any model will fit all the data points well. Thus, the S = 1 model seems like a reasonable one to start with, although there is not enough data to refine that parameter estimate at this time.

Lee (Reference 45) has also derived a model based upon the Poisson distribution function for randomly distributed defects. In this model the probability that a sample would contain at least one defect with "weakness factors" larger than the value w was given by;

$$P(w) = 1 - e^{-AD(w)}$$

where A is the oxide area and D(w) is the total area density with "weakness factor" larger than w. It was also empirically found that the time to breakdown was related to the weakness factor by;

$$t_{BD} = e^{\frac{G}{E_{OX}}}$$

where E_{OX} is the electric field in the gate oxide and G is a factor specific to each process. Thus, the above probability can be seen to indicate the cumulative fraction of parts that would fail at a particular time for a particular process under a specific gate bias. By analyzing TDDB data for six different capacitors from $2x10^{-2}cm^2$ to $5x10^5\ cm^2$ and the above equations, the authors derived an expression for D(w). They were thus able to predict the failure rate and TDDB curve for any oxide area and electric field for their oxides. This relationship is duplicated in Figure 5-9.

Of particular interest are the following:

(1) The relationship between reliability and stress, area, and defects may be modeled;

(2) The relationship appears to be consistent with the Poisson distribution function, whereas it was previously presented that Intel's data for reliability as a function of area and defects was consistent with the Seeds model and not the Poisson distribution.

(3) The defect measurement or "weakness factors" can be found indirectly from a lot of data but cannot be measured directly.

At the Wafer Reliability Workshop at Lake Tahoe, California in October of 1987, there was a consensus that two good models for time dependent dielectric breakdown existed and were supported by convincing data. One was the Berkeley model and the other model was described in a paper by Wolters and Zegers-Van Duynhoven of Phillips Research Laboratories (Reference 28) of which some aspects were previously discussed. This model is described below.

Perhaps the most unique aspect of the Phillips model is the use of extreme value probability instead of the conventional lognormal statistics. It is argued that using the lognormal distribution which is good in the region of the median is inconsistent with the weak link nature of dielectric breakdown - that is, the device will fail at some defect which acts as the weakest spot.

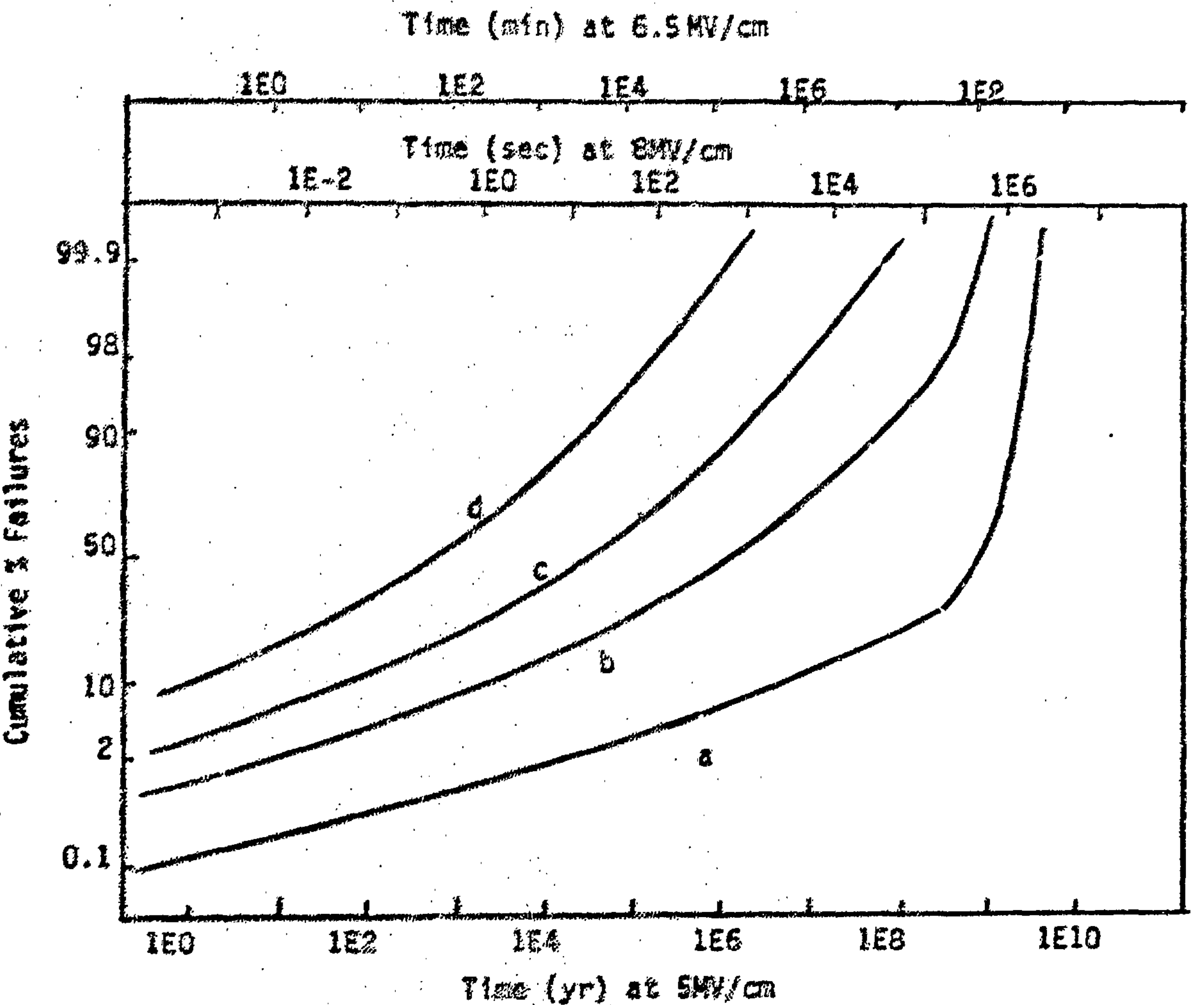


FIGURE 5-9:
THEORETICAL CURVES OF CUMULATIVE FRACTION OF FAILURE FOR DIFFERENT OXIDE AREAS (a) .001 cm^2, (b) .01 cm^2, (c) .03 cm^2, AND (d) .1 cm^2. FROM REFERENCE 1

Extreme value statistics are often used when the values of interest are the largest or smallest in the distribution. Mechanical fracture of materials or the electric breakdown of transformer oil (Reference 46) are typical weakest link processes. Gate oxide breakdown depends on intrinsic material properties as well as defects. Indeed, it is the 1%, or .01% failure point that is of more interest than the 50% point.

It is argued that the hazard rate at low values is approximated by an exponential function. This idea was proved by Gumbel (Reference 47) for various distributions including lognormal.

Thus,

$$\frac{1}{1-F(x)} \frac{d\,F(x)}{C\;dx} = \exp(x)$$

and

$$\ln(-\ln(1-F(x))) = \text{a linear function of } x$$

In the above equations F(x) is the cumulative probability of failure at x. x could be the breakdown electric field or the log of time to failure at a constant voltage.

A large distribution or amount of data is required to make the above equations work properly. The author had breakdown data on some 12000 capacitors and grouped them into 30 groups of 400 and made another distribution of the lowest value in each of the 30 groups. When plotted on extreme value probability paper, the grouped distribution resulted in a line parallel to the original distribution (Figure 5-10). Of interest was that the shift between the two curves was about ln (400) which happens to be the log of the ratio of the effective areas of the two groups of capacitors. Thus, the shift corresponds to the increase in probability of finding a defect among the group of 400. This shift is predicted by the "stability postulate" of extreme value statistics and should hold as long as the defects are distributed homogeneously (i.e., Poisson). When defects are clustered, the shift is less.

Since the factor ln (-ln(1-F)) scales accordingly to the factor $\ln(A_2/A_1)$, it follows that;

$$\ln(-\ln(1-F_2)) - \ln(-\ln(1-F_1)) = \ln(A_2/A_1)$$

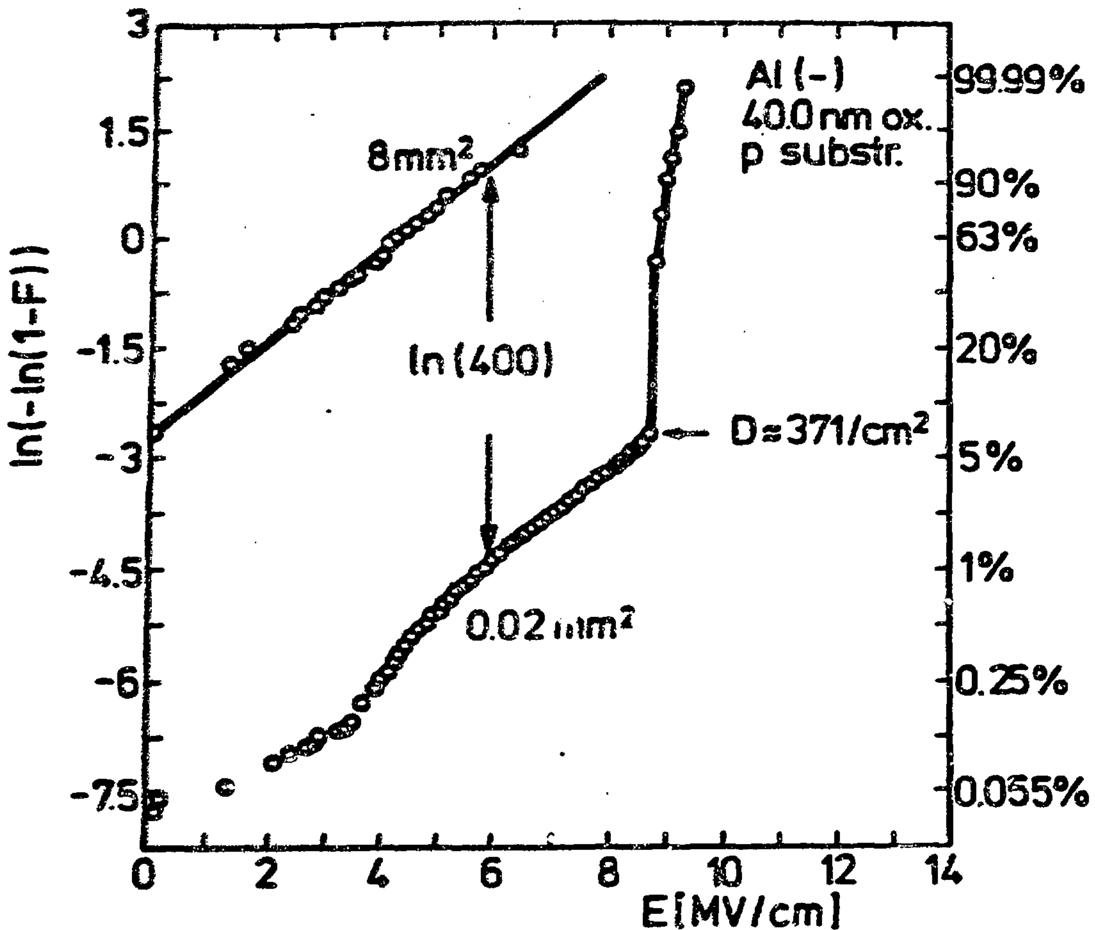


FIGURE 5-10:
BREAKDOWN DISTRIBUTION OF 12000 CAPACITORS (LOWER CURVE) AND THE SMALLEST VALUE OF EACH GROUP OF 400 (UPPER CURVE).

where F_1 and F_2 are the fractions of the parts that have failed with gate oxide areas A_1 and A_2 respectively. From the above it is easy to show that

$$F_2 = 1 - (1-F_1)^{A2/A1}$$

This type of equation, relating F_1 and F_2, was used earlier to make graphs based upon the Stapper model. Similar graphs are shown in Figure 5-11 and 5-12 with shaping parameter S = 1 and 5 respectively. It is seen that Figure 5-12 with S = 5 gives a remarkably good fit.

An expression was also derived from the extreme value statistics of the Phillips model to indicate that the ratio of failure (i.e., hazard) rates was equal to the ratio of gate oxide areas. Their data tended to support this relationship. Since this is a simple and easy to work with relationship, other published works were examined to find data to support or reject this model. While many researchers have presented various types of time-to-breakdown data for various conditions, few have moved the next step and presented failure rate data, especially failure rates for devices with different oxide areas. While failure rates can easily be calculated from t_{50} and sigma data, the frequent use of high sigmas (greater than 1) in this type of testing can result in failure rates that are extremely sensitive to modest changes in the data.

The researchers at Berkeley have calculated and published failure rate data for devices with different oxide areas (Reference 39). A representation of one of the published graphs is shown in Figure 5-13. From this graph it is easy to see that for reasonable product lifetimes (10 years or less), the failure rate of a chip with 10x the area of another chip, is 10x the failure rate of that chip (assuming similar defect densities). After some years of operation, the relationship would not be as good. Thus, their data and model agree reasonably well with the Phillips model.

The Berkeley failure rate/area relationship is based on the assumption that the defects are not uniformly distributed across the wafer - that is, a Gamma distribution function and the Stapper Yield model with S = .6. Extending the approach used in that report produced the graphs shown in Figures 5-14, 5-15 and 5-16.

Figure 5-14 demonstrates the cumulative failure probability of a chip when the cumulative failure probability of a smaller chip (20% of the oxide area) is known and the shaping factor S = .3, .6 and .9. This chart indicates that when the failure probability of the smaller chip is small, the failure probability of the larger chip will be 5x as much (the ratio of the oxide areas). The simple

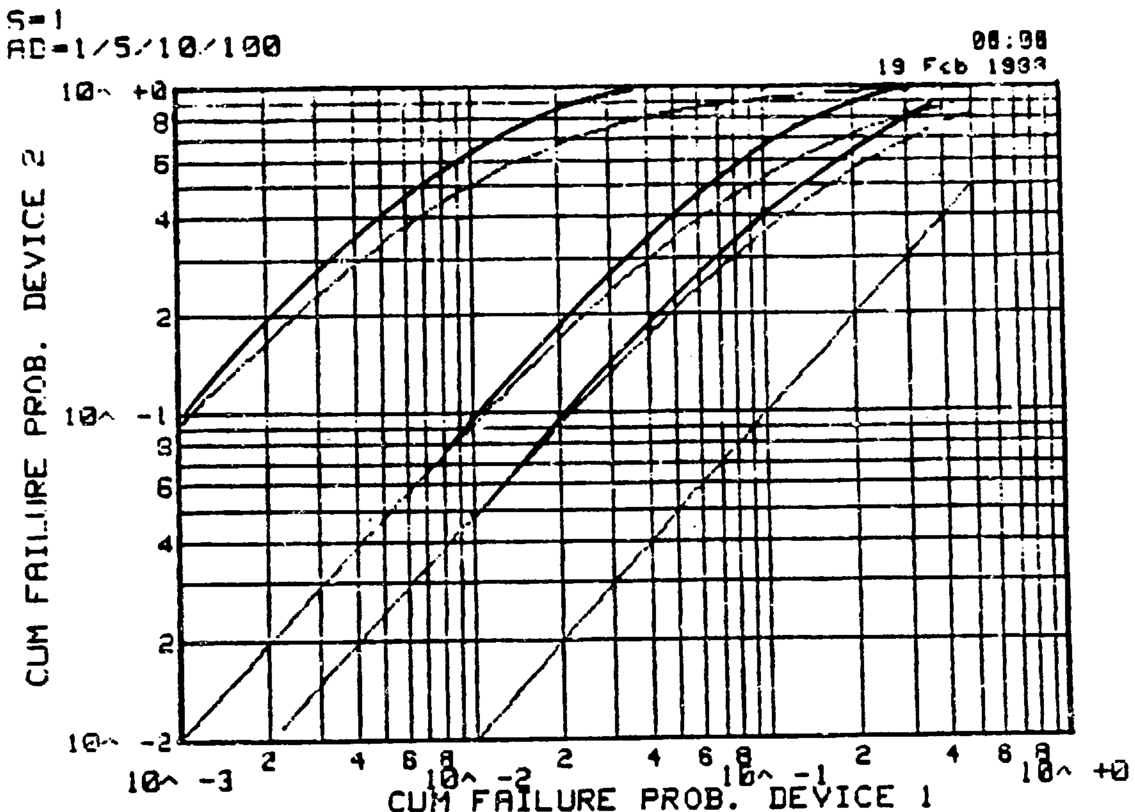


FIGURE 5-11:

CUMULATIVE FAILURE PROBABILITY OF 2 DEVICES WHOSE AREA X DEFECT DENSITY HAVE THE RATIO OF 1, 5, 10, AND 100 WITH THE SHAPING PARAMETER S=1.

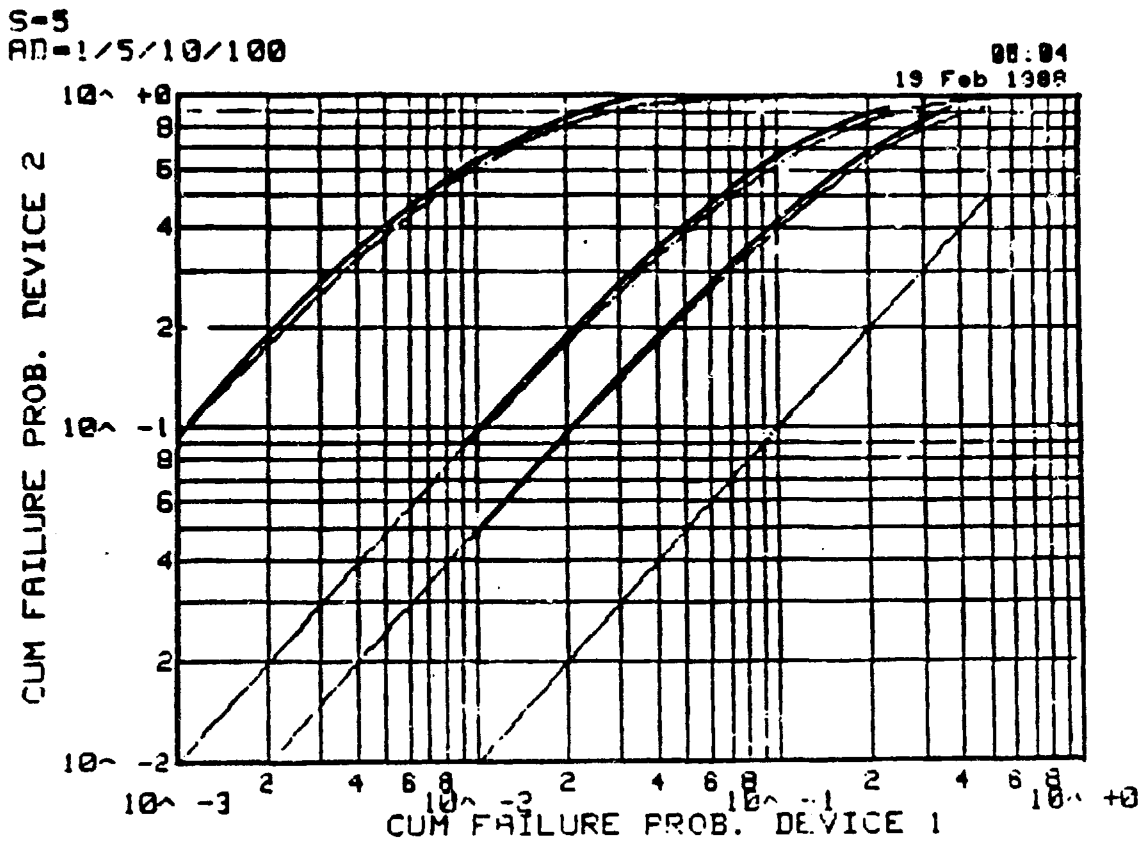


FIGURE 5-12:
CUMULATIVE FAILURE PROBABILITY OF 2 DEVICES WHOSE AREA X DEFECT DENSITY HAVE THE RATIO OF 1, 5, 10, AND 100 WITH THE SHAPING PARAMETER S=5.

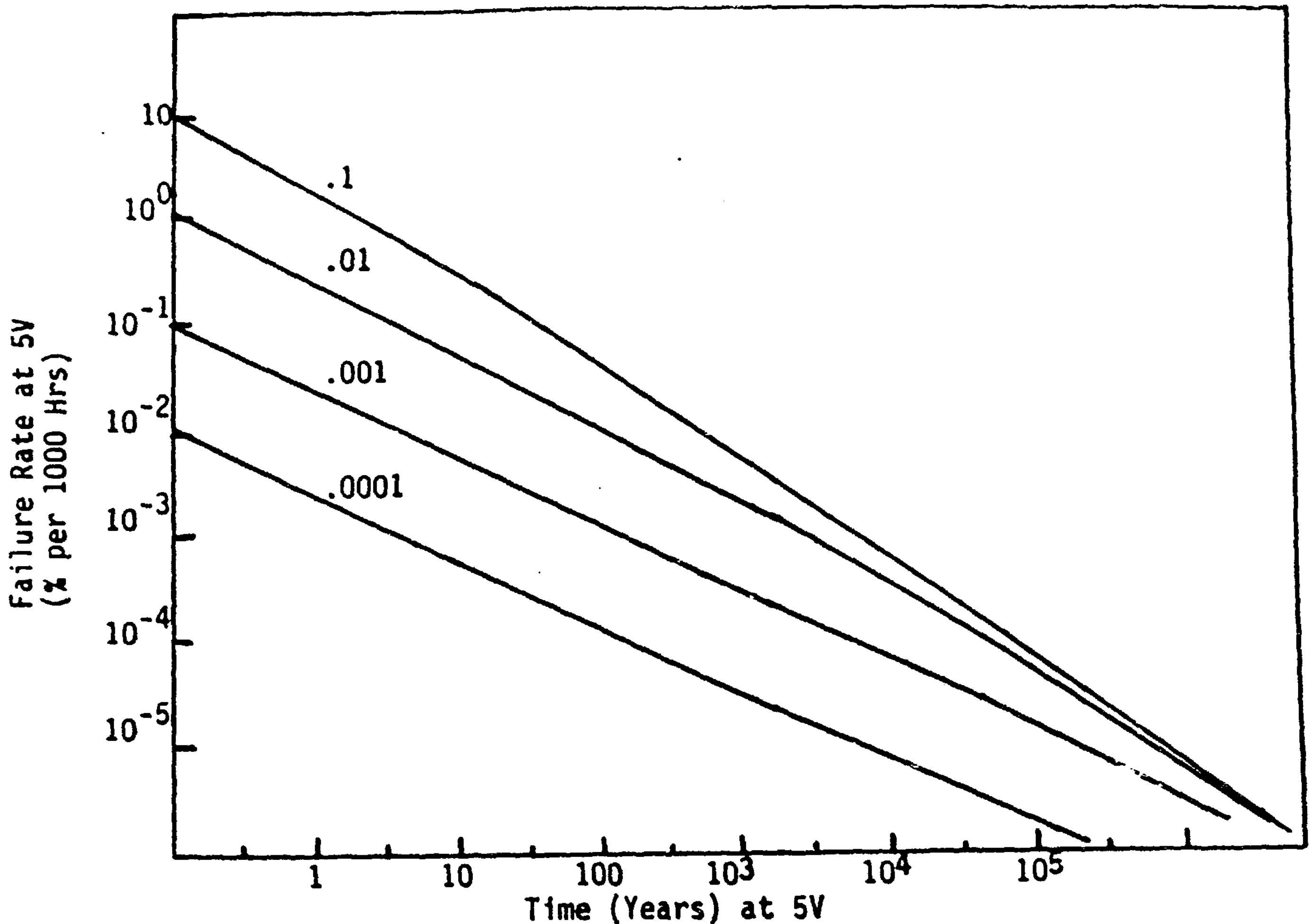


FIGURE 5-13:
THEORETICAL CURVES OF FAILURE RATE FOR DIFFERENT GATE OXIDE AREAS AT 5V OPERATION. TIME AXIS CHANGES AT DIFFERENT VOLTAGES

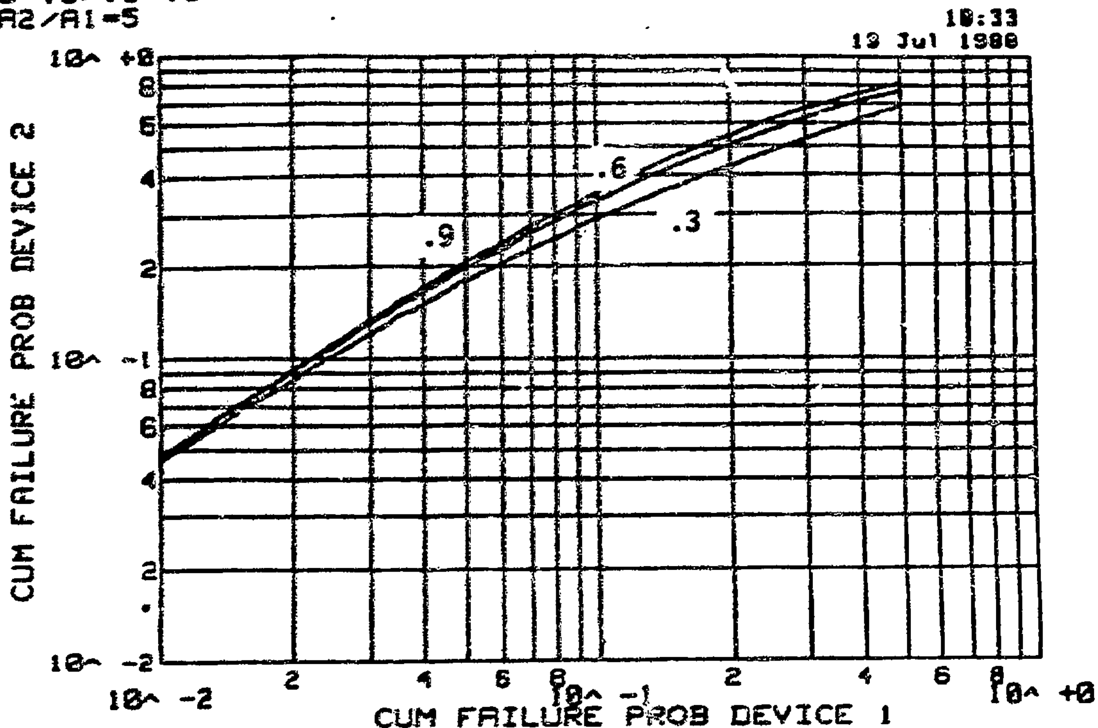


FIGURE 5-14:

CUMULATIVE TDDB FAILURE PROBABILITY FOR DEVICE WHEN CUMULATIVE TDDB FAILURE PROBABILITY OF ANOTHER DEVICE WITH 1/5 GATE OXIDE AREA AND SHAPING FACTOR S = .3, .6 AND .9

relationship does not hold as well when the failure probability of the smaller chip is more than 10%. Figure 5-15 shows a similar graph where the oxide area of the larger chip is 10x that of smaller one.

In a similar fashion Figure 5-16 demonstrates the case where the area ratio is 50. These charts suggest that if a large number of chips with more than one oxide area are life tested, then for the first few failures the number of failures for chips with different area will be proportional to the area of those chips (for the TDDB mechanism).

Since the exact value of the S factor to use is not clear, Figure 5-17 was generated to show the effect of different S values. It is clear that for larger S values, the area ratio model is a better approximation. However, for S = .01, approaching the Poisson case where S = 0, the model is valid only for smaller cumulative failure probabilities. Table 5-5 demonstrating some of these effects is shown below. In this table, the columns represent the cumulative failure probability, the chip area ratio, the S value, and the cumulative failure probabilities ratio, respectively. Ideally, the 2nd and 4th columns would be the same. It can also be seen from this data that the area ratio model is less consistent for larger area ratios.

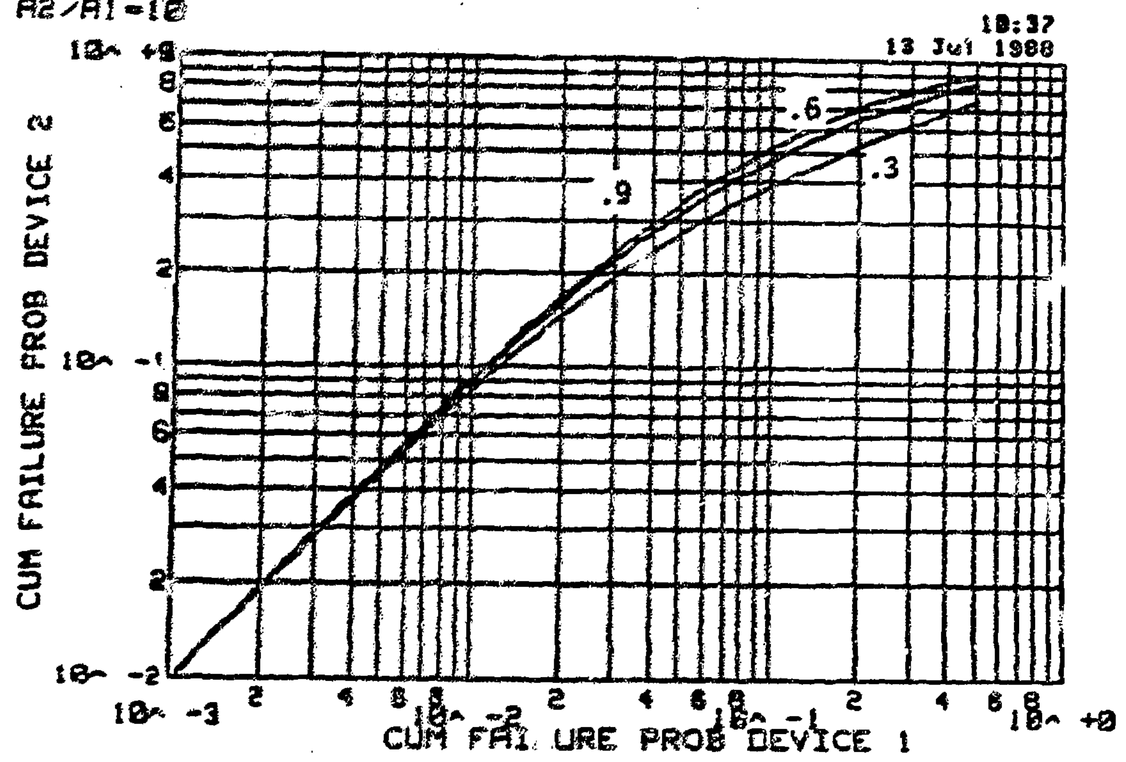


FIGURE 5-15:

CUMULATIVE TDDB FAILURE PROBABILITY FOR DEVICE WHEN CUMULATIVE TDDB FAILURE PROBABILITY OF ANOTHER DEVICE WITH 1/10 GATE OXIDE AREA AND SHAPING FACTOR S = .3, .6 AND .9

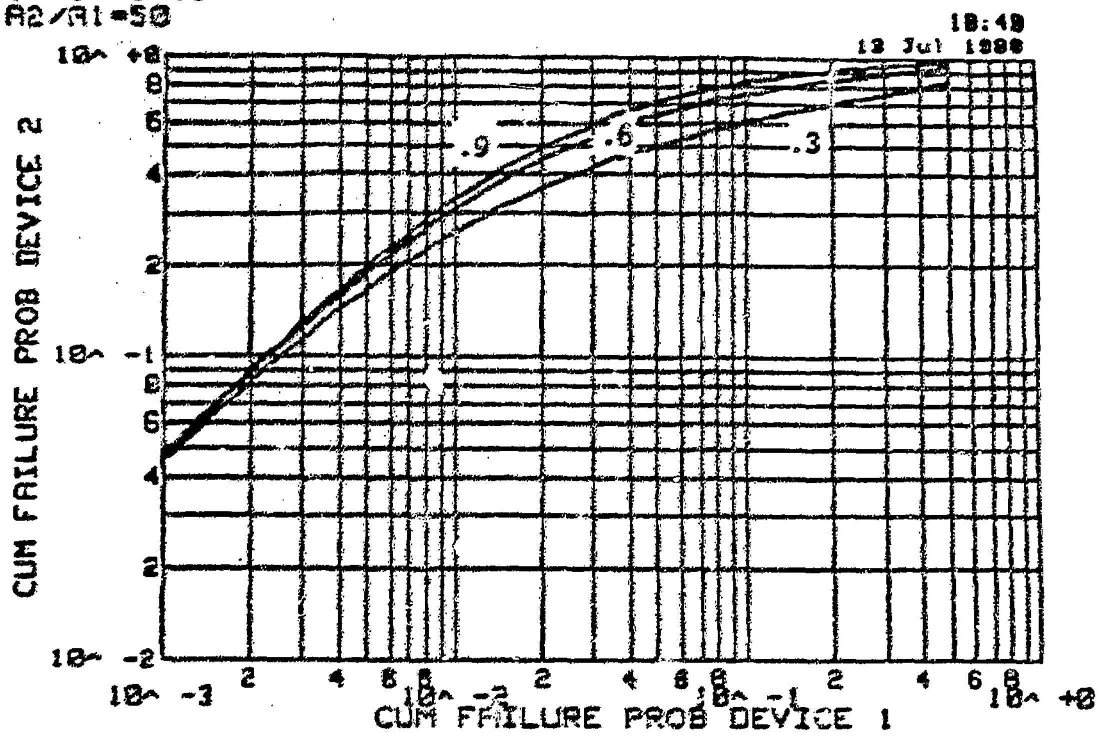


FIGURE 5-16:

CUMULATIVE TDDB FAILURE PROBABILITY FOR DEVICE WHEN CUMULATIVE TDDB FAILURE PROBABILITY OF ANOTHER DEVICE WITH 1/50 GATE OXIDE AREA AND SHAPING FACTOR S = .3, .6 AND .9

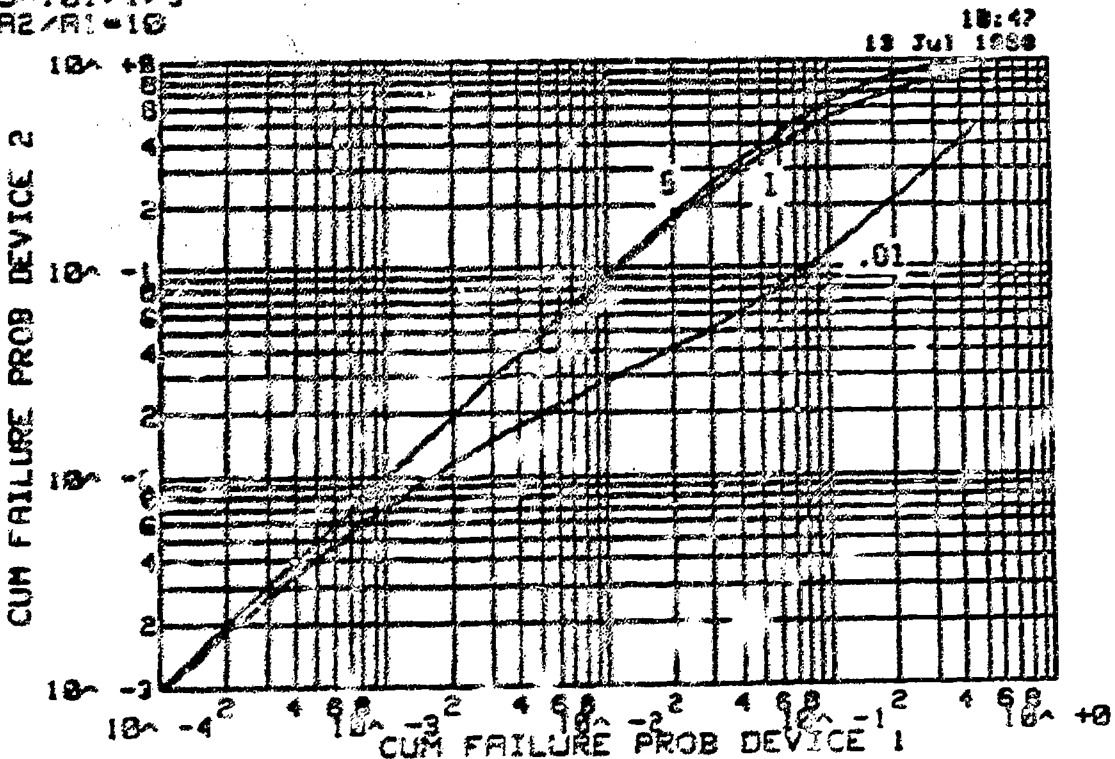


FIGURE 5-17:

CUMULATIVE TDDB FAILURE PROBABILITY FOR DEVICE WHEN CUMULATIVE TDDB FAILURE PROBABILITY OF ANOTHER DEVICE WITH 1/10 GATE OXIDE AREA AND SHAPING FACTOR S = .01, 1, 5

TABLE 5-5:
AREA, S VALUE, AND CUMULATIVE
% FAILURES COMPARISON

CFP_1	A_2/A_1	S	CFP_2/CFP_1
1%	5	.6	4.8
10%	5	.6	3.3
.1%	10	.6	10
1%	10	.6	9
10%	10	.6	4.6
10%	10	.01	1.2
10%	10	2	5.7
10%	10	5	6.2
.1%	50	.6	48
1%	50	.6	31
10%	50	.6	6.5

In summary the TDDB portion of the failure rate is modeled as directly proportional to the gate oxide area. For this model, a failure rate must be established for a "standard" or "reference" chip of known area. As stated previously, the average area of the die contained in the database of .21 cm^2 is to be used for this purpose.

5.1.2.3.1 Calculating Defect Densities

The previous discussions have analyzed the area/defect density/yield relationships and concluded that the oxide hazard rate is directly proportional to the die area and defect density (D). The most desirable means to calculate the actual value of defect density to be used in the hazard rate expression is to use defect measuring test structures of the actual fabrication process. One way to calculate this defect density is given in Appendix B.

It is not likely that defect density data can be obtained from manufacturers unless required by a certification program such as the Generic Qualification program. For this reason, it is imperative that a default condition be defined if actual defect densities cannot be determined. The following discussion summarizes this default value.

Reference 6 discusses the following effective defect density (D_{EFF}):

$$D_{EFF} = D_0\left(\frac{X_0}{X_S}\right)^2$$

where, D_0 is a critical defect density for a feature size of X_0
X_0 is a reference feature size
X_S is the actual feature size

This relationship is based on MIL-STD-209 which states that the defect density increases as the square of decreasing feature size.

Although there is some concern as to this assumption's validity, and various researchers have proposed their own defect density distributions, for the purposes of this model the MIL-STD-209 approach is the most widely recognized and will be used. Therefore, the default value of D/D_R will be $(X_0/X_S)^2$. Since the average feature size in the database from which the failure rate were derived was 2 micron, this value can be used for X_0. The default defect density is therefore $(2/X_S)^2$.

5.1.2.3.2 Effective Areas and Device Type Relationships

Since oxide area has been shown to be directly correlated with failure rate, devices exhibiting different packing densities will result in significant differences in reliability. Ideally, the actual gate oxide area would be [illegible] as an input into the reliability prediction model. It is impractical, however, to require that it be known since a relatively detailed design analysis of the chip must be done to determine it. To alleviate this need, a relative scaling factor was derived for various component types which is multiplied by the total die area, such that the only area input into the model is the total die area. Since the average die area of devices whose data was used to derive the model is .21 cm^2, the device type correction factors for metal and oxide to be presented in this section are normalized to typical oxide areas and metal lengths of a .21cm^2 chip.

To derive a relative scaling factor, of particular interest was the difference in physical features (i.e., metal area and gate oxide area) for different circuit types (gate array, RAM, custom chip). For this purpose the Yield Analysis Tool (YAT) was used to determine critical areas for the different chip types. The YAT is a software tool that quantitatively analyzes circuit features on integrated circuit devices. The YAT input is the layout database of the integrated circuit device and a table which describes the circuit features to be analyzed. The histograms output describe the distribution of features sizes, chip maps of the smallest features, total area of selected features, overlap edge length, and overlap area. This tool is generally used for yield projection and, with the appropriate wafer processing, the identification of yield inhibitors.

For the purpose of this analysis YAT data for four different CMOS chips was analyzed for metal 1 length (less than 3 microns wide), metal 2 length, p channel gate area, n channel gate area, and metal 1 space length (the total length of parallel first metal runner less than 3 microns apart). The results of that analysis are summarized in Table 5-6.

TABLE 5-6:
FEATURE DENSITY

Feature	Units	Custom Chip 1	Custom Chip 2	SRAM	Gate Array
Metal 1	cm/cm^2	390	619	289	698
Metal 2	cm/cm^2	291	317	400	668
P gate area	% of total chip	1.3	1.9	2.2	2.5
N gate area	% of total chip	1.2	1.8	2.6	2.6
Metal 1 space	cm/cm^2	511	618	743	600

It should be noted that the specific SRAM for which data was available was a 2Kx8 device of modest size (.24cm^2) that did not efficiently use the pad area and thus may have a more modest density. Also the gate array data includes unused gates.

To better understand some of the differences in Table 5-6, a more detailed analysis was performed on the metal 1 length and the n channel gate oxide area. This detailed data is shown in Tables 5-7 and 5-8 respectively.

TABLE 5-7:
METAL 1 COMPARISON

Feature	Units	Custom Chip 1	Custom Chip 2	SRAM	Gate Array
Total Length	cm	667	[illegible]	210*	914
Average Length	micron	12.8	13.7	4.3	7.4
%≤1.6 micron wide	%	48	56	13	0
%≤2.6 micron wide	%	53	67	29	74
Ave. Length 1.6 micron	micron	23	119	17	0
Ave. Length 2.6 micron	micron	12	3.7	11	30

*SRAM is 1/4 size of other chips.

TABLE 5-8:
N-CHANNEL GATE OXIDE COMPARISON

N Gate Oxide	Units	Custom Chip 1	Custom Chip 2	SRAM	Gate Array
Instances <10 microns^2	Number	1.5K	18K	49K*	17K
Instances 50-60 microns^2	Number	2.9K	3.7K	.91K*	37K
Average area	Microns^2	32	35	10	40
Total Instances	Number	36K	52K	54K*	63K
Total Area	cm^2	.0114	.018	.0053*	.025

*SRAM is 1/4 size of other chips.

This analysis shows that custom chips may not be as densely packaged as SRAMs and gate arrays. The gate array densities listed would generally be reduced by a factor that may approach the percent utilization number. If that were done then all chips would have comparable metal 1 length and the SRAM would have the densest gate oxide percentage and close metal 1 lines. The analysis indicates that the density is design dependent.

A presentation at the 1987 GOMAC conference by engineers from United Technologies Microelectronic Center (Reference 3) tried to correlate failure rate and design complexity. Using life test data from gate array variations, they looked for correlation to traditional measures of complexity such as number of inputs and outputs, die size, and number of transistor pairs, as well as new bench marks such as metal 1 area, metal 2 area, and coincident metal area. UTMC saw poor correlation between the number of I/O's to the normalized failure rate and fair correlation to the number of transistor pairs. They demonstrated good correlation (correlation coefficients of .96 to .99) for the failure rate versus metal 1 area, metal 2 area, and coincident metal area. They point out that the life tests were performed on early 3 micron technology parts where intermetal dielectric integrity was the predominant failure mechanism. They did not show the results of failure rate plots versus gate oxide area, number of vias, and number of contacts. Clearly, the correlation would be dependent on the type of failures observed. The data seemed to indicate that a part with much metal 1 would also have much metal 2, much coincident metal, and much gate oxide area, such that a considerable amount of data would be required to properly sort out the effects.

Since the data in the database (contained in Appendix D) is from a good cross-section of device types (logic, memory, gate arrays, etc.) the failure rate expressions developed are for an "average" device. Therefore, the area ratio A/Ar factor only has to be a relative number between the various device types. Table 5-9 summarizes the relative area factors for Custom/Logic devices and for Memory/Gate Array devices. The Custom/Logic average percent oxide area was obtained by averaging the sum of the P and N gate areas (in Table 5-6) for Custom Chips 1 and 2 (((1.3+1.2) + (1.9+1.8))/2=3.1). Similarly, the average oxide area for Memory/Gate Arrays is the average total (P and N) percent areas for the SRAM and Gate Array. A similar procedure was used to derive the average metal length. For example, the average metal length for Custom/Logic devices is; ((390+291) + (619+317))/2 = 808. The A_{TYPE} factors were then derived simply by normalizing the factor to 1 for an "average" device. That is; 4.95/3.10 = 1.23/.77.

TABLE 5-9:
RELATIVE OXIDE AREA AND METAL LENGTH
RATIOS FOR VARIOUS DEVICE TYPES

Device Type	Average Gate Oxide Area (% of Chip)	$A_{TYPE_{ox}}$	*Average Metal Length	$A_{TYPE_{MET}}$
Custom & Logic Devices	3.10	.77	808	.88
Memory Gate Arrays	4.95	1.23	1027	1.12

*Average linear length of first and second layer metal per chip area.

The area of the chip can then be modified with the $A_{TYPE_{ox}}$ for the oxide failure rate and the $A_{TYPE_{MET}}$ for the metal failure rate. These are dimensionless factors which indicate for oxide, that memories/gate arrays typically have 1.23/.77 = 1.59 times the oxide per area as do custom and gate arrays.

5.1.2.5 Oxide Wearout t_{50}

The primary oxide wearout stress related acceleration factor have been determined to be temperature and electric field. Therefore the t_{50} of the lognormal can be defined as:

$$t_{50} = \frac{t_{50_{REF}}}{A_{T_{ox}} A_{V_{ox}}}$$

To calculate $t_{50_{REF}}$, data in Table 5-10 was extracted from the literature.

TABLE 5-10:
DATA USED TO DERIVE t_{50} CONSTANT

Area (10^6 μm)	T_{ox} (Å)	Temp. (°K)	E_S (Mv/cm)	t50 (Observed Hrs.)
1.5	600	298	3	2.8×10^{7}
75	390	423	4	544
75	390	348	4	4,402
75	390	398	4	27,800
75	390	298	4	880,000
75	390	298	3	1.54×10^{9}
75	390	298	4	1.74×10^{6}
75	390	298	5	422

Since electric fields of 5 MV/cm are being used reliably in VHSIC/VHSIC-Like devices, it appears that this data is not representative of these class of devices. Therefore, to derive a t_{50REF}, empirical t_{50} data at high electric fields was used. This data, not presented here for proprietary reasons, was from high field accelerated tests performed on VHSIC-Like oxides. Calculating the $A_{V_{ox}}$ and $A_{T_{ox}}$ terms under the conditions of, that test and solving for t_{50REF} yields a value of 1.3×10^{22} (10^{6} hrs.). This yields the following t_{50} time for TDDB:

$$t_{50_{ox}} = \frac{1.3 \times 10^{22}}{A_{V_{ox}} A_{T_{ox}}}$$

Empirical data from the literature indicates that a sigma of 1 is appropriate for these distributions for oxide under normal operating conditions. However, various investigators have determined that the sigma is directly related to the MTF. (That is, as the MTF goes down, so does the sigma). Unfortunately, there is not enough quantitative data available to define an accurate sigma as a function of MTF. Therefore, unless an accurate sigma is known for a particular process, the value of 1 should be used.

Also, in the t_{50} equation to be used in the model, a (QML) factor is added to account for the improved reliability expected from the procedure taken by manufacturers that are on the Qualified Manufacturer List (QML). The rationale for chosing the .5 to 2 values for this factor are given in Section 7.1.4.

This factor is also used in this form in the t_{50} expressions for metal and Hot Carrier wearout failure rates.

5.1.3 Oxide Hazard Rate Summary

It has been shown that the oxide wearout hazard rate is directly proportioned to area and defect density. There is no reason to believe that both the early life and wearout terms will not be accelerated as a function of area/defect density. The form of the oxide failure rate is therefore:

$$\lambda_{ox} = \frac{A}{A_R}\frac{D_{0ox}}{D_R} A_{TYPE_{ox}} (\lambda_{Early\ Life} + \lambda_{Wearout})$$

where:

A_R = .21 cm^2, the reference chip area
D_R = 1 , the reference defect density

The entire detailed oxide hazard rate is then given as follows:

$$\lambda_{ox}\ (\text{in } F/10^6) = \frac{A\, A_{TYPE_{ox}}}{A_R}\left(\frac{D_{0_{ox}}}{D_R}\right)\left[(.0788\, e^{-7.7\, t_0})\,(A_{T_{ox}})\,(e^{-7.7\, A_{T_{ox}} t})\right.$$

$$\left. + \frac{.399}{(t+t_0)\sigma_{ox}} \exp\left(\frac{-.5}{\sigma_{ox}^2}\left(\ln(t+t_0) - \ln t_{50_{ox}}\right)^2\right)\right]$$

A = Total Chip Area

$A_{TYPE_{ox}}$ = .77 for Custom and Logic Devices

= 1.23 for Memories and Gate Arrays

A_R = .21 cm^2

$D_{0_{ox}}$ = Defect Density calculated by using the procedure of Appendix B (if unknown, use $\left(\frac{X_0}{X_S}\right)^2$ where X_0= 2 μm and X_S is the feature size of the device)

D_R = 1 defect/cm^2

t_0 = Effective Screening time

= (Actual Time of Test in 10^6 hrs.) * $A_{T_{ox}} A_{V_{ox}}$
(where $A_{T_{ox}}$ and $A_{V_{ox}}$ are the values during screening)

$A_{T_{ox}}$ = Temperature Acceleration Factor

$$= \exp\left[\frac{-.3}{8.63\times10^{-5}}\left(\frac{1}{T_J} - \frac{1}{298}\right)\right]$$

T_J = Average junction operating temperature

$= T_C + \theta_{JC} P$ (in °K)

$$A_{V_{ox}} = e^{-192\left(\frac{1}{E_{ox}} - \frac{1}{2.5}\right)}$$

E_{ox} = The maximum power supply voltage (V_{DD}) divided by the gate oxide thickness (in MV/cm)

$$t_{50_{ox}} = \frac{1.3 \times 10^{22}\ (QML)}{A_{T_{ox}} A_{V_{ox}}} \text{ (in } 10^6 \text{ hrs.)}$$

QML = 2 if on QML, .5 if not.

σ_{ox} = Sigma obtained from test data of oxide failures from the same or similar process. If not available, use a σ_{ox} value of 1.

t = Time (in 10^6 Hours)

5.2 METAL FAILURE RATE

5.2.1 Metal Early Life Failures

As in the case of oxide, the early life failure rate due to metal was derived using the methodology outlined in Section 3.0. Table 5-11 summarizes the data used in this derivation. Given in this table is the effective time interval (at 25°C), the total accelerated part hours using the temperature acceleration factor with an activation energy of .55 eV, and the total number of metal failures observed in the time interval.

TABLE 5-11:
METAL FAILURE DATA

Equivalent Time Interval at 25°C (10^6 hrs.)	Accelerated Part Hours (10^6 hrs.)	Number of Failures
0 - 0.059872	16468.541808	3
.059873 - 0.209553	40975.894310	6
.209554 - 0.623669	77953.612970	9
.623670 - 1.248337	111354.649173	36

Table 5-12 presents the summarized data used in the derivation of this factor.

TABLE 5-12:
METAL EARLY LIFE SUMMARIZED FAILURE DATA

Effective Range (10^6 hrs.)	Midpoint	Effective Part Hours (10^6)	Number of Failures	Failure Rate F/10^6
0 - .059872	.029936	16469	3	.000182
.059873 - .623669	.36177	118929	15	.000126

For the data in this table, the failure data in the range 0.623670 - 1.248337 was excluded since the 36 failures observed were detected only at a single time in that interval and the time of failure was not known. All that was known was that the 36 failures occurred less than 1.248337. This data therefore could not be used to identify failure rate dependency on time.

Deriving the metal factor with a simple regression solution of the above data and adjusting the T to match the observed cumulative failure rate yields:

$$\lambda_{MET}(t) = .00043\, e^{-1.18\, t}$$

Adjusting the constant .00043 to account for the unknown failures, and adding the accelerations due to temperature and screening yields the following metal failure rate:

$$\lambda_{MET\ Early\ Life} = .00102\, e^{-1.18\, t()}\, A_{TMET}\, e^{-1.18\, A_{TMET}\, t}$$

5.2.2 Metal Wearout

Electromigration is the predominant metal wearout failure mechanism and its probability density function is modeled with a lognormal time to failure distribution. The mean time to failure (t_{50}) is often given by Black's equation:

$$t_{50} = A_B J^{-n} \exp \frac{Ea}{KT}$$

To determine the value of A_B that should be used in this expression, the dataset in Table 5-13 was used.

TABLE 5-13:
SUMMARY OF OBSERVED PARAMETER VALUES FROM THE LITERATURE
(all Lognormal Distribution)

Conditions	J (A/cm^2)	n	Ea	t_{50} Hrs.	σ	Temp. (°C)	Reference
Al-Cu-Si Films	10^5 - 2 x 10^6	2	.5	- -	.2 - .5	150 - 250	52
Al - Ti - W Stripes							
w/thermal gradient	2.5 x 10^6	- -	- -	- -	.52	185	53
wo/thermal gradient	2.5 x 10^6	- -	- -	- -	.34	185	
Constant Current		2	.43		- -	125	54
	2 x 10^6			174	.79	150	55
				167	.73	150	
				465	1.1	150	
				126	.67	150	
				175	.80	150	
				120	.78	150	
				644	1.04	150	
				127	.84	150	
				175	.80	150	
				144	.77	150	
				567	1.12	150	
				126	.76	150	
- - - - -	- - - - -	- - -	.4	- -	- -	150-250	56
Al Si Alloy films	6.6 x 10^5	- - -	.54	- -	.23 - .65	< 230	57
Al - Cu - Si Films	1.6x10^6-2x10^6	2	.5		.2 - .5	195 - 250	58
Au - Cu - Alloys	2 x 10^6			1600	1.4	220	59
				819	.42	220	
				525	.70	220	
				354	.73	220	
				15	.40	220	
Al - Poly Si Metal			.9			150-220	60
Al - Si Films		- -	- -				61
leakage		2.3	.9± .1	- -	- -	- -	
open		2.3	.5	- -	- -	- -	
Al	2x10^6		.56 ± .04	- -		125-300	62
TiW/Al	10^6-4x10^6	2.06	.53	- -		- -	
Al/.5% Cu/1%Si	2x10^6	1.7	.55	- -	- -	125	63
	<10^5	1					64
	10^5 - 10^6	1.5	. . .				
	.45x10^6-2.88x10^6	2	- -				
	10^6 - 2x10^6	4.5	- -				
Small Grain	.55 - 2.65(10^6)		.48	- -	- -	180	65
Large Grain	.5 - .2 (10^6)	- -	.84	- -	- -	180	
Glassed Large Grain	.45 - .9(10^6)	- -	1.2	- -	- -	180	
Al	4x10^6	2	- -	- -	.56	125	66
Al	.333/.242 (10^6)	2	.511	1039	.7	191	25
	.283/.189	2	.525	2318	1	173	
	.268/.179	2	.529	2672	.8	175	

Based on this summary of information, representative values of n and the activation energy are 2 and .55 eV respectively. With this information the t_{50} expression becomes:

$$t_{50} = \frac{A_B \text{ (METAL TYPE)}}{J^2 A_{TMET}}$$

where:

$$A_{TMET} = \exp\left[\frac{-.55}{8.63\times10^{-5}} \left(\frac{1}{T_J} - \frac{1}{298}\right)\right]$$

A_B (METAL TYPE) = "Base" t_{50} as a function of the metal type used.

Using the data in Table 5-12, the constant A_B was derived for Aluminum metallization and turns out to be .39 million hours. For Al-Cu metal this constant was calculated to be 14.5 million hours, or 37.5 times the constant for aluminum. Therefore, the (METAL TYPE) factor is:

(METAL TYPE) = 1 for Aluminum
= 37.5 for Al-Cu

Towner et al, (Reference 12) concluded from empirical electromigration testing of aluminum conductor lines, that the mean time to failure (t_{50}) increases as the inverse square of the duty cycle of pulsed operation. That is:

$$t_{50} \text{ (pulsed DC)} = \frac{t_{50} \text{ (constant DC)}}{r^2}$$

where:

r = duty cycle

Since the t_{50} equation developed was based on constant current conditions, the actual duty cycle should be accounted for. Therefore, when calculating the current density (J) to be used in the $t_{50_{MET}}$ equation, the average absolute value should be used.

Also, investigated for the electromigration t_{50} model was the use of a testing effectiveness factor. Electromigration field failures are rarely reported and electromigration burn-in failures are even rarer, although they have been reported (Reference 67). It is generally thought that if the

screen or burn-in detects any electromigration failures, then there will be many more field failures soon. Without wafer level tests, it is difficult to conceive a screen that is effective for electromigration.

The use of an area/defect density factor was also investigated for metal wearout as it was in the oxide wearout case. Modeling electromigration is not as straight forward as in the oxide case. There have been a number of studies which found the electromigration lifetime related to the line length to some critical length which most likely is related to line width (References 48, 49, 50, 51). The idea here is that the failure of a line is dependent upon the existence of a worst case grain boundary situation, and that a line of a critical length has a high probability of having such a situation and therefore has a certain tendency to fail. A longer line's tendency to fail is not significantly greater. This critical length for near micron lines is probably in the order of 1000 microns (Reference 5). Since VLSI devices have meters of minimum width metal films, this approach suggests that the electromigration failure rate factor is essentially the same for all large chips with a particular metallization process using a particular set of design rules.

For this reason, the area/defect density factor will only accelerate the early life metal failure rate and not the electromigration case. The metal defect density to be used can be calculated as given in Appendix B.

5.2.3 Metal Failure Rate Summary

The model form of the metal failure rate is:

$$\lambda_{MET} = \frac{A}{A_R}\frac{D0_{MET}}{D_R} A_{TYPE_{MET}} (\lambda_{MET\ Early\ Life}) + \lambda_{MET\ Wearout}$$

The complete detailed metal failure rate is therefore given as follows.

$$\lambda_{MET} = \left[\frac{A}{A_R}\frac{D0_{MET}}{D_R} A_{TYPE_{MET}} (.00102\ e^{-1.18\ t_0}) (A_{T_{MET}}) (e^{-1.18\ A_{T_{MET}} t}) \right]$$

$$+ \left[\frac{.399}{(t+t_0)\sigma_{MET}} \exp\left(\frac{-.5}{\sigma_{MET}^2} \left(\ln(t+t_0) - \ln t_{50_{MET}} \right)^2 \right) \right]$$

A	=	Total Chip Area (in cm^2)
$A_{TYPE_{MET}}$	=	.88 for Custom and Logic Devices
	=	1.12 for Memory and Gate Arrays
A_R	=	.21 cm^2
$D0_{MET}$	=	Defect Density calculated using the method in Appendix B. (If unknown use $\left(\frac{X_0}{X_S}\right)^2$ where $X_0 = 2\ \mu m$ and X_S is the feature size of the device)
D_R	=	1 defect/cm^2

$A_{T_{MET}}$ = Temperature Acceleration Factor

$$= \exp\left[\frac{-.55}{8.63\text{x}10^{-5}}\left(\frac{1}{T_J} - \frac{1}{298}\right)\right]$$

$T_J = T_{case} + \theta_{JC} P$ (in ^oK)

t_0 = Effective Screening Time (in 10^6 hrs.)

= $A_{T_{MET}}$ (at Screening Temp.) * (Actual Screening Time (in 10^6 hrs))

(to Calculate t_0 use $A_{T_{MET}}$ based on the junction temp. during screening)

$$t_{50_{MET}} = (QML)\frac{.388 * (\text{Metal Type})}{J^2 A_{T_{MET}}} \quad \text{(in } 10^6 \text{ hrs.)}$$

(QML) = 2 if on QML, .5 if not.

Metal Type = 1 for Al

37.5 or Al-Cu

37.5 for Al-Si-Cu

J = The mean absolute value of Metal Current Density (in 10^6 Amps/cm^2)

σ_{MET} = sigma obtained from test data on electromigration failures from the same or a similar process. If this data is not available use $\sigma_{MET} = 1$.

t = time (in 10^6 hrs)

5.3 HOT CARRIER DEGRADATION

It is well known that hot carrier effects can degrade MOS transistors with short channel lengths. This degradation (Reference 68) can be expressed as:

$$\text{transistor parametric shift} = A_{HC}t^{n}$$

Where t is the stress time, and the power factor of time "n" changes according to hot carriers injection mechanisms (therefore varies according to the device structure) but generally falls in the range of .25 to .75 (Reference 68, 69). The constant term "A_{HC}" represents the magnitude of device degradation and is related to the drain voltage (Vd) by:

$$A_{HC} = \beta \exp(-\alpha/Vd)$$

Where "β" is some constant of proportionality. By plotting the log of the transistor parametric shift versus the log of time, the constant term "A_{HC}" and the power factor term "n" can both be determined. By plotting the log of A versus 1/Vd the value of "α" (slope) and "β" (y-intercept) can be determined at different drain voltages. The first equation above can then be rearranged:

$$t = (\text{transistor parametric shift}/A_{HC})^{1/n}$$

With known values of "A_{HC}" and "n" the time "t" for a given parametric shift can then be estimated.

Another method of predicting device lifetime used by other investigators is to monitor the device substrate current (I_{sub}). Device lifetime "τ_{HC}" has been shown to be related to the substrate current by the relationship:

$$\tau_{HC} = C^{*}(I_{sub})^{-m}$$

Where C is a constant dependent on parameters such as drain current, etc., and the power factor "m" fails in the range of 2.7 - 3.2 (Reference 68, 69). Since the substrate current is relatively easy to measure, it has the potential of being used as way of monitoring sensitivity to hot carrier effects on suitable test structures at the wafer level. The degradation due to hot carriers is also a strong function of temperature and frequency, which are related to I_{sub}. If I_{sub} can accurately be determined, the effects of temperature and frequency will inherently be accounted for.

Previous analysis has concentrated on measuring the shift in the threshold voltage when the transistor is in the linear or ohmic region (V_{DD} = 100mV), or a shift in the maximum drain current (V_{GS}, V_{DD} = 5v) with the source and drain connections reversed. In either case the transistors must be biased at maximum avalanche hot electron (AHE) stress condition (typically V_{GS} = 3.5v, V_{DS} = 6.4v) for a minimum of 8 hours to predict the transistor's sensitivity to hot carrier degradation. A recent study found that the above equation holds not only in static stress but also in dynamic stress. Where the device lifetime can be written by:

$$\tau\ \text{dynamic} = C\,(I_{sub,\,peak})^{-m}/R \quad \text{(Reference 71)}$$

Where $I_{sub,\,peak}$ is the peak value of pulsed substrate current and R is duty ratio for the substrate current pulse.

Also investigated was the possibility of using I_{sub} measured at the wafer level on a process monitor test structure as a means of predicting device lifetime due to a hot carrier degradation. A hot carrier test found the low dose drain (LDD) n-channel transistor was less sensitive to hot carrier effects when compared to a single drain (SD) transistor structure. The peak substrate current at V_{DD} = 5.5 volts was measured at room temperature on 20 LDD and 20 SD 10/1.0 n-channel transistors before the hot carrier test. The results were:

	I_{sub} (μA)	
	Mean	Std Dev.
LDD	3.54	0.19
SD	9.97	0.52

Thus there is a good possibility that substrate current measurements at the wafer level may provide a fast and reliable method to model hot carrier degradation.

A hot carrier degradation model of this type does not address a particular failure mode, and does have different impacts on memory chips and logic devices. This hot carrier model is intended to indicate how a transistor's parameters degraded. This model form is generally accepted, however, what is difficult is to judge is how that transistor degradation affects circuit performance for a memory, digital or analog application. While a manufacturer could model this, the results are not likely to be shared. The specific application of a transistor is most important. For example a pass transistor, where the current may go backwards from the drain to source, will be affected more than an on/off transistor in an inverter gate.

It is the judgement of the authors at this time that either a product has a hot electron problem or it does not. Thus, the model should be very sensitive to modest changes - i.e., the failure rate may move into the FIT range very quickly if some threshold is exceeded. Otherwise, the failure rate is in the fractional FIT range.

The possibility of using substrate current measurements at the wafer level to provide a fast and reliable method to model hot carrier degradation is intuitively appealing. Other researchers have also written of this goal and the discussion below involves some measurements that have been taken to investigate this matter.

The data in Table 5-14 shows I_{sub}, I_{dd} @ I_{sub}, and the gate voltage, all with V_{DD} = 5.5 volts at 3 temperatures. All six 10/1 transistors experienced the hot carrier test at 5.5 volts. Note that the Vg values at which I_{sub} occurs changes, indicating the hot carrier damage affects the maximum electric field in the channel. The 300/1.2 transistors were not stressed. For both transistors sites, the I_{sub}/I_{DD} ratio of the single drain (SD) device was approximately 2x higher at all temperatures. From the data we should be able to (1) correlate projected life times to room temperature I_{sub} data, and (2) determine the temperature dependence of I_{sub}.

As previously shown the device lifetime "τ" due to hot carrier degradation has been modeled as:

$$\tau = C^* I_{sub}^{-m}$$

Where C is a constant dependent mainly on the transistor's response to drain bias conditions, I_{sub} is the substrate current, and the power factor term "m" is equal to ϕ_{it}/ϕ_i, where ϕ_{it} is the critical energy to create an interface trap, and ϕ_i is the impact ionization energy. However, this model does not account for the dependence of substrate current generation on drain current, which can be modeled as (Reference 69):

$$I_{sub} = C^* I_d^* \exp(-\phi_i/q^* \lambda E_m)$$

Where C is a constant, I_d is the drain current, λ is the mean free path for electrons, and E_m is the maximum electric field in the channel. Therefore, a better expression for modeling device lifetime would be (Reference 72):

$$\tau = A/I_d^*(I_{sub}/I_d)^{-m}$$

TABLE-5-14:

I_{SUB} VS. TEMPERATURE

PART NUMBER	NMOS SIZE	ROOM TEMPERATURE DATA Idd (uA)	Isub (uA)	Vg	Isub/Idd	-5 C DATA Idd (uA)	Isub (uA)	Vg	Isub/Idd	-55 C DATA IDD (uA)	Isub (uA)	Vg	Isub/Idd
e3-6-2	10/1	780	5.6	3.37	7.18E-03	GATE LEAKAGE				GATE LEAKAGE			
e3-10-5	10/1	580	4.6	2.96	7.93E-03	610	5.4	2.97	8.85E-03	760	8.3	3.09	1.09E-02
e3-10-9	10/1	700	5.4	3.03	7.71E-03	770	6.3	3.13	8.18E-03	960	9.66	3.26	1.01E-02
e3-10-13	10/1	610	4.5	2.98	7.38E-03	640	5.47	2.98	8.55E-03	830	8.57	3.12	1.03E-02
LDD(AME;Vdd = 5.5v)				AVG = 7.55E-03				AVG = 8.53E-03				AVG = 1.04E-02	
e3-2-3	10/1	1310	21.9	3.94	1.67E-02	1530	25.2	4.13	1.65E-02	1650	36.6	4.01	2.22E-02
e3-2-8	10/1	1460	26.9	4.1	1.84E-02	1580	31.6	4.1	2.00E-02	1830	47.2	4.16	2.58E-02
e3-2-11	10/1	1690	28.7	4.18	1.70E-02	1790	34.3	4.19	1.92E-02	2140	52.3	4.27	2.44E-02
e3-2-12	10/1	1760	29.3	4.31	1.66E-02	1850	35.6	4.31	1.89E-02	2160	53.8	4.31	2.49E-02
SD(AME;Vdd = 5.5v)				AVG = 1.72E-02				AVG = 1.86E-02				AVG	2.43E-02
e3-6-2	300/1.2	GATE LEAKAGE				GATE LEAKAGE				GATE LEAKAGE			
e3-10-5	300/1.2	12140	91.4	2.67	7.55E-03	13410	108.1	2.72	8.06E-03	16740	169.3	2.8	1.01E-02
e3-10-9	300/1.2	11560	87.3	2.54	7.55E-03	12120	102.4	2.58	8.45E-03	14990	155.5	2.66	1.04E-02
e3-10-13	300/1.2	11140	87.7	2.58	7.87E-03	12530	106.1	2.62	8.47E-03	15490	166.2	2.68	1.07E-02
LDD				AVG = 7.66E-03				AVG = 8.33E-03				AVG = 1.04E-02	
e3-2-3	300/1.2	14090	235	2.60	1.67E-02	16010	275	2.74	1.72E-02	19190	403	2.76	2.10E-02
e3-2-8	300/1.2	13760	251	2.63	1.82E-02	15100	299	2.65	1.96E-02	19940	443	2.76	2.22E-02
e3-2-11	300/1.2	13550	241	2.63	1.78E-02	14465	282	2.63	1.95E-02	19770	422	2.73	2.13E-02
e3-2-12	300/1.2	13550	248	2.64	1.83E-02	14590	280	2.65	1.97E-02	19750	423	2.8	2.14E-02
SD				AVG = 1.78E-02				AVG = 1.90E-02				AVG = 2.15E-02	

In 1987 a hot carrier test was performed at Honeywell on discrete 10/1.0 and 10/1.2 um n-channel transistors with a L_{DD} drain structure, and 250Å gate oxide. The transistors were biased for maximum avalanche hot electron current with V_D = 6.0 and 7.5 volts at 77°K. Due to processing differences between test structures from 3 wafers, there were substantial differences in substrate current for same size transistors.

As mentioned previously, there is disagreement as to what should be the failure criteria for a discrete transistor. For the purpose of this test the lifetime was defined as a 10% decrease in the integral of I_d as V_{SD} is swept from 0 to 5.5 volts with V_{GS} = 5.5 volts. This criteria (which we call "area under the curve") was chosen since it monitors the transistor's response in both the linear and saturation regions of operation.

Figure 5-18 is a log normal plot of the cumulative failures versus time for 19 parts from the test. From this plot it is apparent the hot carrier failure mechanism follows a lognormal distribution, and the presence of a "sport" population is evident. The sigma for this test is approximately 1.1. Figure 5-19 is a plot of the log of τ times the drain current versus the log of ratio of I_{sub} divided by I_d. The power factor "m" is equal to 2.5, which is in good agreement with published values. The following listing summarizes published values for this exponent:

Author	Affiliation	Year	Power Factor	Reference
Takeda et al	Hitachi	1983	3.2 - 3.4	68
Hu et al	Cal Berkely	1985	2.9	69
Tzou et al	AMD	1985	2.7	73
Horiuchi et al	NEC	1986	2.5	71
Weber	Siemens	1986	2.9	8[illegible]
Krieger et al	VLSI	1988	2.9	84
Tran	AT&T	1987	2.9 - 3.2	85
Chen et al	AT&T	1987	3.1	86
Duvvury et al	T.I.	1987	2.8	87
Bellens et al	IMEC	1988	2.7	88
Weber	Siemans	1988	2.9	89

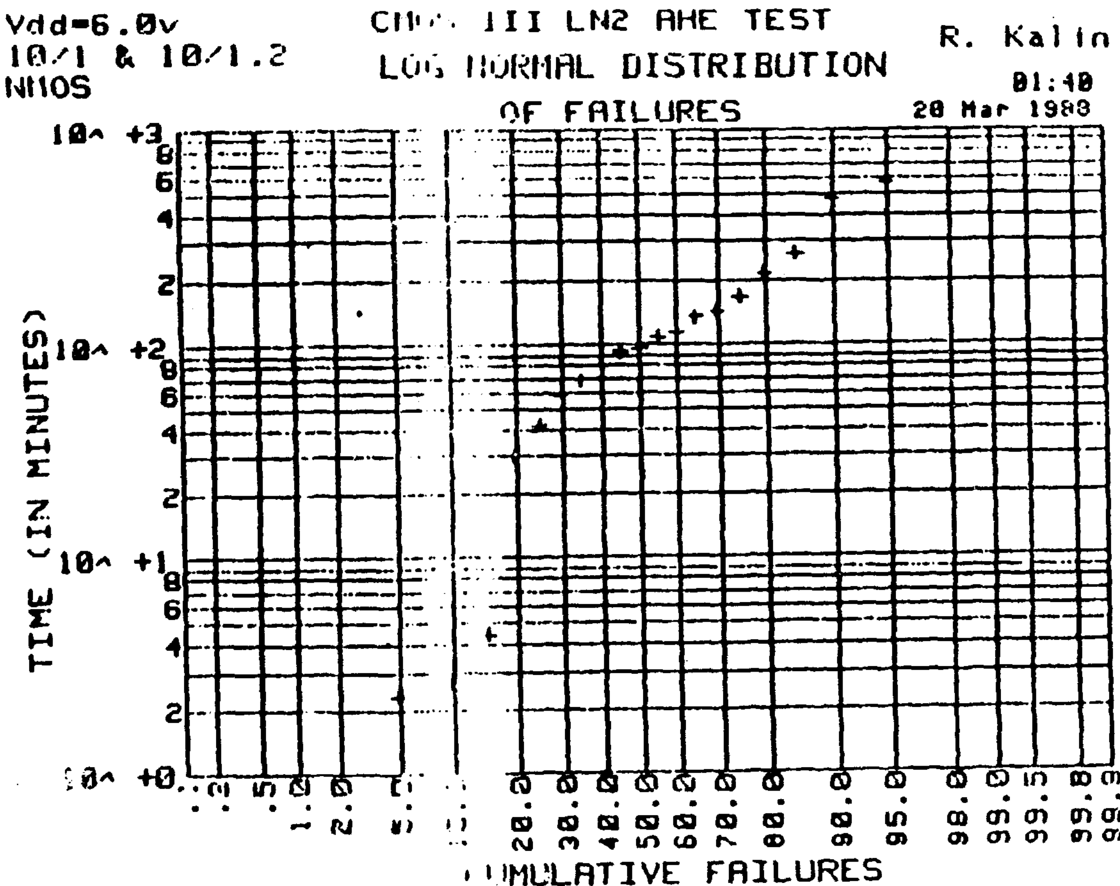


FIGURE 5-18:
LOGNORMAL PLOT OF FAILURES DUE TO HOT CARRIER DEGRADATION VS. TIME

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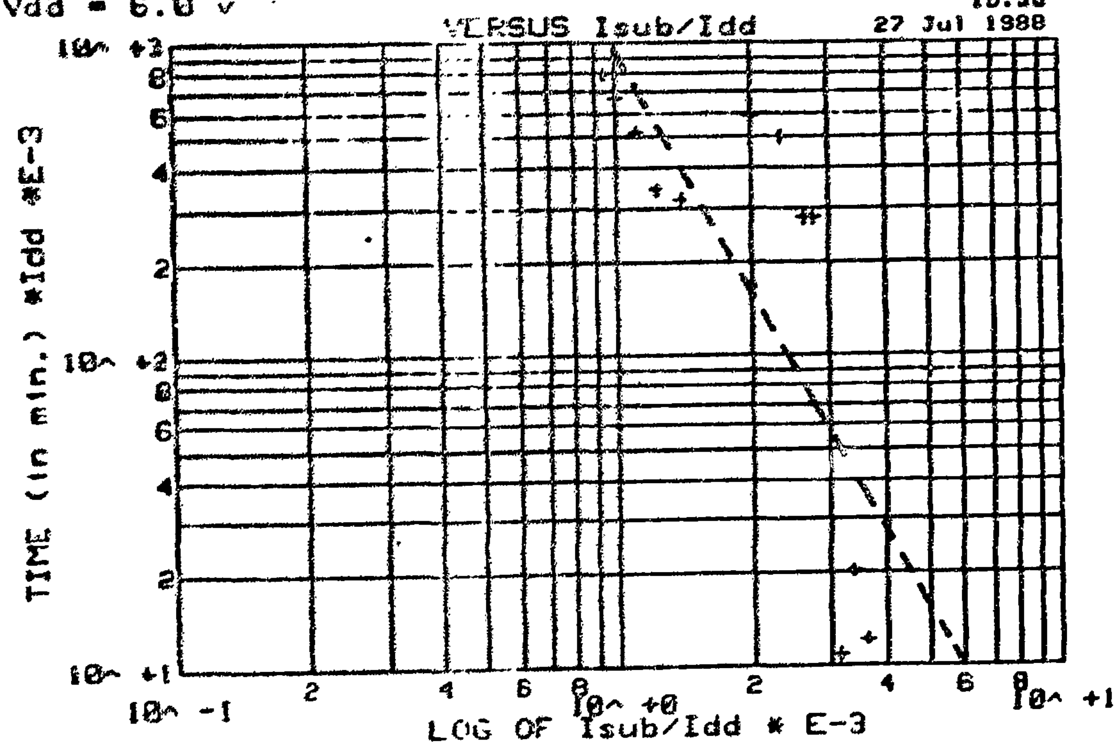


FIGURE 5-19:
PLOT OF LOG OF T $*I_d$ VS.
THE LOG OF I_{SUB}/I_d

Is is important to note that the model should account for temperature effects. One research effort (Reference 73) found that the constant term A in the previous equation changes with temperature according to the equation:

$$A_{HC} = A_0 \exp(-.039\ eV/kT)$$

Where k is Planck's constant. The drain current I_d and the substrate current I_{sub} also change at different rates as a functio[illegible] [illegible] temperature; in general, our data indicates I_{sub} increases more at lower temperatures than I_d. Using this methodology to predict lifetime, the data summarized below indicates the impact temperature has on device li[illegible]etime due to hot carrier degradation.

Parameter	77°K	298°K
constant term "A_{HC}"	$4x10^{-8}$	$3x10^{-6}$*
drain current I_d	3.11mA	2.20mA
substrate current I_{sub}	3.44µA	0.75µA
power factor term "m"	2.5	2.5*
lifetime	3.8 hours	8,000 hours

* = assumed or calculated values.

Based on this data, a t_{50} for the lognormal relationship can be defined as follows:

$$t_{50} = \frac{C}{A_{THC}\, I_d}\left(\frac{I_{sub}}{I_d}\right)^{-2.5}$$

Where C is a constant derived to match empirical data. Deriving C from the above data yields a value of $3.74x10^{-5}$.

If actual values of I_d and I_{sub} are not known, there must be provisions in the model for default values. Based on the measured values presented previously, the following default currents can be used for 10/1.2 (width/length in microns) N-channel transistors:

$$I_d = 3.5\, e^{-.0069\, T_J} \text{ (mA)}$$

$$I_{sub} = .0058\, e^{-.00157\, T_J} \text{ (mA)}$$

Hot carrier degradation is strictly a wearout mechanism and therefore should contain no contribution to the early life failure rate. Also, since this phenomena effects all transistors, it is not area or defect density dependent. Therefore, the final failure rate contribution from hot carriers is the following:

$$\lambda_{HC} = \frac{.399}{t\sigma_{HC}} \exp\left[\frac{-.5}{\sigma_{HC}^2}\left(\ln(t + t_o) - \ln t_{50_{HC}}\right)^2\right]$$

$$t_{50_{HC}} = \frac{3.74\times10^{-5}}{A_{T_{HC}} I_d}\left(\frac{I_{sub}}{I_d}\right)^{-2.5}$$

$$A_{T_{HC}} = \exp\left[\frac{.039}{8.63\times10^{-5}}\left(\frac{1}{T_J+273} - \frac{1}{298}\right)\right]$$

T_J = Average junction temperature
$= T_C + \theta_{JC} P$ (in °K)

I_{sub} = Drain Current at Operating Temperature. If unknown use
$I_{sub} = .0058\, e^{-.00157\, T_J}$ (mA)

I_d = Substrate Current at Operating Temperature. If unknown use
$I_d = 3.5\, e^{-.00689\, T_J}$ (mA)

σ_{HC} = sigma derived from test data, if not available use 1.1

t_0 = $A_{T_{HC}}$ (at Screening Temp.) • (Test Duration)

t = time (in 10^6 hrs.)

5.4 CONTAMINATION

Although the physics of failure characteristics of contamination and methods of control are fairly well understood, many failures due to contamination appeared in the data collected for this program. Due to this observance, a failure rate for contamination was derived and included in the model. Here, the contamination failure class is defined as any type of contamination, ionic or other.

The prevalence of contamination related failures tend to be highly dependent on the particular fabrication processes and thus the failure rate model contained herein is an industry wide representative value, and can vary widely from manufacturer to manufacturer. Contamination is strictly an early life mechanism and contains no wearout contribution. Like hot carriers, contamination failures are not area or defect density related and therefore do not have these terms in the failure rate equation. They are typically easily screened due to their high activation energy and temperature acceleration.

Table 5-15 summarizes the data used in the derivation of the contamination failure rate. In this table the first column is the equivalent time interval at 25°C obtained by multiplying the actual time by the acceleration due to temperature, using an activation energy of 1.0 eV. A value of 1.0 eV is widely accepted in the semiconductor industry. The second column is the equivalent number of total part hours in the interval using the same acceleration due to temperature, and the last column lists the number of failures in that time interval.

TABLE 5-15:

CONTAMINATION DATA

Equivalent Time Interval at 25°C (in 10^6 hrs.)	Accelerated Part Hours	Number of Failures
0 - 20.431619	5619901.501721	1
20.431620 - 71.510666	14006588.472287	1
71.510667 - 212.829365	27088162.036146	2
212.829366 - 228.845835	3064959.151818	2
228.845836 - 425.658727	35348454.984858	595
425.658728 - 2724.355183	20233992.578138	1
2724.255184 - 6994.508872	6635426.324593	1

Table 5-16 presents the summarized data used. The first five data points from Table 5-15 were combined for the first entry in Table 5-16 and the sixth and seventh were combined for the second in Table 5-16. Regressing on these two datapoints yields the following failure rate:

$$\lambda_{CON} = 9.36 \times 10^{-6} e^{-.0028\, t}$$

TABLE 5-16:

SUMMARIZED CONTAMINATION DATA

Time Interval (10^6 hrs.)	Midpoint	Part Hours (10^6 hrs.)	Number Failures	Failure Rate (F/10^6 hrs.)
0 - 425.658727	212.0	85,128,066	601	7.1×10^{-6}
425.658728 - 6994.508872	3709	26,869,418	2	7.4×10^{-8}

Accounting for the unknown failures and accelerations due to temperature, duty cycle and screening time, the data in Table 5-16 yields the following equation:

$$\lambda_{CON} = .000022\, e^{-.0028\, t_0\, A_{T_{CON}}}\, e^{-.0028\, A_{T_{CON}}\, t}$$

$A_{T_{CON}}$ = Temperature Acceleration Factor

$$= \exp\left[\frac{-1.0}{8.63 \times 10^{-5}}\left(\frac{1}{T_J + 273} - \frac{1}{298}\right)\right]$$

T_J = Junction temperature

$= T_C + \theta_{JC} P$ (in °K)

t_0 = Effective Screening Time

= $A_{T_{con}}$ (at screening junction temperature) * (actual screening time in 10^6 hrs.)

t = time (in 10^6 hrs.)

5.5 PACKAGE RELATED FAILURE RATE

To develop a model for package related failures (i.e., package, lead, die bond, interconnects, etc.) the assumption was made that environmental stresses (i.e., temperature cycling, thermal shock, vibration, mechanical shock) accelerate package related failure mechanisms to a much higher degree than die related failure mechanisms. Since these environmental stresses are event related, they can be modeled with an exponential time to failure distribution and therefore a constant failure rate can be derived. The data presented previously in the database profile supports this approach.

5.5.1 Screening Factor

Since there is no field experience data available, the approach used to develop field failure rates for VHSIC/VHSIC-Like package styles was to derive a failure rate for lower complexity package types for which field experience is available and multiply that failure rate by the ratio of fallout rates observed between VHSIC package types and MSI/LSI package types for which field experience is available.

Many package defects can be screened effectively and therefore a strong relationship between reliability and quality should be expected. The approach used in the package failure rate development was therefore to make this failure rate a function of quality (screening level) and environment. The premise of this factor is that the post screened percent defective in a given population is equal to the initial percent defective minus the percent fallout after the population is exposed to a screen (or screening sequence), and the field failure rate expected from a particular package style is directly proportional to the fallout rate observed for that package when exposed to environmental testing.

The following screening level categories and associated observed fallout percentage were used to derive the package factor (Reference 76).

None	0%
Burn-in	.36%
Environmental Series	1.37%
Burn-in/Environmental Series	1.66%

These are general categories and are representative of data from a variety of sources and test conditions. They are typically, but not limited to MIL-STD-883 tests. In this context Burn-in is normally a high temperature (125°C), short duration (160 hours) test designed to identify defective parts. Environmental tests are intended to be representative of various environmental screens such as; temperature cycling, shock/vibration, humidity, etc. As an example Quality Level B devices are subjected to both burn in and environmental tests.

These broad categories were chosen because fallout rate data for specific screens loses its statistical significance. Additionally, many tests are performed in a series, making it impossible to identify the fallout rate of each one.

Assuming that the test effectiveness for package related mechanisms is directly proportional to the fallout rate percentage for a particular test or series of tests, and that the test effectiveness for a burn-in with environmental series is in the 80-100% range (or approximately 90%), the test effectiveness along with a relative failure rate correction factor for package screening, are summarized in Table 5-17. This yields a 10:1 ratio in the expected package failure rate between Class B and D devices.

TABLE 5-17:
PACKAGE TEST EFFECTIVENESS AND SCREENING FACTOR

Screening Level	Class	Test Effectiveness	Π_{SP}
None	D	0	10
Burn-in	-	20	8
Environmental Series	-	72	2.8
Burn-in with Environmental Series	B	90	1

Once the test effectiveness has been derived, the package failure rate can be defined as follows:

$$\lambda_{package} = \lambda_{BP} \frac{FO}{FO_R} \Pi_{SP} \Pi_E$$

where:

λ_{BP} = base package failure rate
FO_R = reference fallout rate for MSI/LSI
FO = observed fallout rate for VHSIC/VHSIC like packages
Π_E = environmental factor
Π_{SP} = package screening factor

The 10:1 ratio of package failure rates is applicable for the environments where it would be expected that most of the defective parts would be accelerated to failure. In a benign environment, it would not be expected that defective parts would be accelerated to failure and therefore there would be less benefit to screening parts used in benign environments. However, without data to the contrary, and since the package failure rate is normalized to unscreened devices used in benign environments, a worst case failure rate ratio between quality levels for G_B is also 10:1, and treated as an independent factor from environment.

5.5.2 Environment Factor

λ_{BP} can now be derived from empirical field failure rate data and failure mode distributions (percent of failures due to the package). To accomplish this, Reliability Analysis Center data (Reference 75) on MSI/LSI devices was used to calculate an average IC failure rates for these combinations of screen class and environment. These failure rates are summarized in Table 5-18.

TABLE 5-18:
AVERAGE λ AS FUNCTION OF ENVIRONMENT

Screen Class	Environment	Failure Rate
Burn-in/Environment (B)	A_{IF}	.285
Burn-in/Environment (B)	A_{UF}	.441
None (D)	G_B	.372

These environments and screen classes were chosen since there existed good quality data in these categories and also to provide a good mix of vibration and temperature cycling stresses. The exact stresses in each environment can not be specifically identified and therefore the environments must be qualitatively defined as in the current MIL-HDBK-217 models.

Next, failure mode distributions were used to identify the percentage of failures due to package related failure mechanisms. For this the following data extracted from Reference 75 was used:

Device Category	% Package Hermetic	% Package Nonhermetic
Digital	60.9	47.2
Linear & Interface	19.9	23.7
Memory	5.3	20.3
VLSI	7.1	14.3

From this, it was determined that 25% of IC failures are typically due to the packages, indicating that the base failure rate would be 25% of the above listed numbers. These package failure rates are given in Table 5-19.

Using the package failure rates in Table 5-19 in conjunction with the quality factors (Π_{SP}) given in Table 5-17, the relative environmental factors for A_{IF}, A_{UF}, and G_B environments can be defined. This was accomplished by making the product of Π_{SP} and Π_E proportional to the package failure rate. These relative environment factors are presented in Table 5-20, normalizing G_B to one.

TABLE 5-19:
PACKAGE FAILURE RATE AS FUNCTION OF
ENVIRONMENT AND SCREEN CLASS

Environment	Class	Package Failure Rate
A_{IF}	B	.071
A_{UF}	B	.110
G_B	D	.093

These ratios betwen G_B, A_{IF}, and A_{UF} environments factors are relatively consistent with the environmental factors currently in MIL-HDBK-217E. Therefore, assuming the relative Π_E's between environments in 217E are valid, the values for all environments are defined in Section 5.5.8.

TABLE 5-20:
ENVIRONMENT FACTOR

Environment	Π_E
A_{IF}	8.15
A_{UF}	12.5
G_B	1

5.5.3 Package Type Factor (Π_{PT})

The values in Table 5-20 correspond to the lower complexity devices from which they were derived. They now can be modified to the higher complexity VHSIC/VHSIC-Like device packages via the fallout rate ratio $\frac{FO}{FO_R}$.

For a typical MIL-STD-883 Class B screening sequence for a DIP package, RAC data (Reference 76) indicates a typical fallout percent of 1.66% of which 25% of these failures are due to package related mechanisms. The reference fallout rate can therefore be defined as follows:

$$FO_R \text{ (package)} = (1.66\%)\ (.25) = .415\%$$

To modify these failure rates to VLSI/VHSIC, the package fallout rates in Table 5-21 were derived from the VHSIC/VHSIC-like database (Appendix D) for devices subjected to environmental testing consistent with a Class B screen. For example, .79 was derived by observing the percentage of nonhermetic chip carriers that failed from a combination of burn-in and environmental testing. The column labeled "total" is a weighted average and was derived by observing the total fallout rate (i.e., devices failed/devices tested) for both hermetic and plastic parts for each package type. Similarly, the row labeled "total" was obtained by calculating the total fallout rate for both hermetic and nonhermetic packages.

The fact that the FO_R listed above is very close to the total fallout rates in Table 5-21, although coincidental, indicates that there is good agreement between these two separate methods of obtaining fallout rate, and lends a degree of confidence in these results.

TABLE 5-21:
OBSERVED VHSIC/VHSIC-LIKE PACKAGE FALLOUT RATE

	Nonhermetic	Hermetic	Total
Chip Carriers	.79%	1.4%	1.03%
Pin Grid Array	.69%	.33%	.49%
DIP	.18%	.30%	.22%
Total	.41%	.61	

Since there is not a significant difference in the hermetic vs. nonhermetic fallout rates, there will be no distinction between these for the base failure rates although a failure rate term will be added for the nonhermetic effects of plastic packages. Using the totals for the three packages types for FO, the ratios can be defined as in Table 5-22, along with the package type factor (normalizing DIP's to a value of 1). For example, the FO/FO_R factor for DIP's is .22/.415 = .53.

TABLE 5-22:
PACKAGE TYPE FACTOR

Type	FO/FO_R	Π_{PT}
Chip Carriers	2.48	4.67
Pin Grid Array	1.18	2.23
DIP	.53	1

5.5.4 Package Base Failure Rate

The package failure rate can therefore be summarized as:

$$\lambda_{PAC} = \lambda_{BP} \Pi_E \Pi_{SP} \Pi_{PT}$$

where: Π_E = Environmental Factor
Π_{SP} = Package Screening Factor
Π_{PT} = Package Type Factor

Π_E

G_B	1.0
A_{IF}	8.15
A_{UF}	12.5

Π_{SP}

No Screening	10
Burn-In	8
Env. Series	2.8
Burn-In/Env. Series	1

Π_{PT}

DIP	1
PGA	2.23
Chip Carrier	4.68

Since the relative values of the environmental factor, screening factor, and package type factor have been previously derived, the base package failure rate was derived by setting the observed package failure rate equal to the predicted for a known case and solving for λ_{BP}. Since there is high confidence in the A_{IF}, Class B observed failure rates for DIPs were the ones used. This failure rate is .285, of which 25% is due to the package, yielding an observed failure rate of .071 $F/10^6$ hrs. Since the FO/FO_R factor for DIPs is .53 (Table 5-22), and the Π_{PT} factor was normalized to 1 for DIP's, the failure rate (λ_{PAC}) for DIP's is (.071) (.53) = .037 ($F/10^6$). The value of .53 is due to increased reliability of DIP packages from the time the observed field data was collected to the time the fallout rate data collected for this effort was obtained. Therefore,

$$.037 = \lambda_{BP}\Pi_E\Pi_{SP}\Pi_{PT}$$

$$\lambda_{BP} = \frac{.037}{\Pi_E\Pi_{SP}\Pi_{PT}} = \frac{.037}{(8.15)(1)(1)} = .0046$$

It has been shown in past studies that the package failure rate is also a function of package complexity, of which number of pins is one measure. From Reference 9 the following relationships were obtained for the package failure rate of DIPs up to 64 pins.

$$\lambda_{package} = \Pi_E \Pi_Q [.00044 + .00042 (\# \text{ pins})] \qquad \text{Hermetic DIPs}$$

$$\lambda_{package} = \Pi_E \Pi_Q [.0035 + .00009 (\# \text{ pins})] \qquad \text{Nonhermetic DIPs}$$

The data used to derive these numbers were predominantly from commercial quality devices in a ground benign application with $\Pi_E = .38$ and $\Pi_Q = 17.5$ (hermetic) and $\Pi_Q = 35$ (for nonhermetic).

Therefore, using these relationships to derive the $\lambda_{package}$ yields;

$$\lambda_{PAC} \text{ (Hermetic)} = .00293 + .00279 (\# \text{ Pins})$$

$$\lambda_{PAC} \text{ (Nonhermetic)} = .0465 + .00120 (\# \text{ Pins})$$

If these relationships are extrapolated to the pin counts of VHSIC type devices, the package failure rate and the number of pins would be directly proportional. That is, a 200 pin package would have twice the failure rate as a 100 pin package. This is not intuitively appealing since there are many package related failure mechanisms that are not complexity dependent. Failure mechanisms relating to the lead, lead/seal interface, and wire bonds can be considered complexity dependent since they are essentially independent of each other in a reliability sence. Conversely, the die bond is considered complexity independent since there is only one, which is independent of the lead/wire bond assembly. Data from Reference 75, which provides failure mode data on a wide variety of part types, indicates that this assumption is a reasonable approximation for a general use reliability model. To alleviate this situation in lieu of enough empirical data to precisely define this relationship, the assumption was made that the complexity dependent and complexity independent package failure rates are equal at the average complexity value in the VHSIC database (120 pins). Therefore, this yields the following base package failure rate to be used in this model is:

$$\lambda_{BP} = .0024 + 1.85 \times 10^{-5} (\# \text{ Pins})$$

5.5.5 Junction Temperature Calculation

In calculating the junction temperature, the average junction temperature should be used. The standard method of accomplishing this is adding the case temperature to the temperature rise due to power dissipation;

$$T_J = T_C + \theta_{JC} P$$

where:

T_C = Case Temperature

θ_{JC} = Junction-CaseThermal Resistance

P = Worst Case Actual Power

To calculate T_J, the actual θ_{JC} of the device being predicted should be used. If it is not known, however, the following alternate method using θ_{JA} can be used;

$$T_J = T_A + \theta_{JA} P$$

where θ_{JA} is the junction to ambient thermal resistance. Table 5-23 summarizes θ_{JA}'s values which were derived by various manufacturers and represent typical values. (Note: There are very wide variations in these values).

TABLE 5-23:

JUNCTION - AMBIENT THERMAL RESISTANCE VALUES

θ_{JA} (°C/W)

# PINS	PLCC	CLCC	PPGA	CPGA	CDIP	PDIP
24	92	42	-	-	50	50
28	65	40	-	-	50	50
40	65	40	-	-	43	43
44	61	40	-	-	42	42
48	58	38	-	-	38	38
52	56	38	-	-	38	38
64	50	37	-	-	30	30
68	46	36	90	36	-	-
84	44	35	81	34	-	-
120	39	34	81	34	-	-
124	39	34	75	31	-	-
144	37	33	68	30	-	-
180	36	31	57	29	-	-
200	36	30	50	29	-	-
200	36	30	48	29	-	

5.5.6 Effects of Nonhermetic Parts

Although there was not a significant difference in fallout rates observed between plastic encapsulated and hermetic devices, there is reason to believe that the long term failure rate for nonhermetic devices, under high humidity and high temperature conditions would be worse than hermetic packages due to moisture penetration and corrosion. To account for this effect the literature was reviewed for models relating failure rate and variables such as relative humidity, temperature and power dissipation. Numerous models have been proposed (References 15, 16, 17, 18, 19, 20 and 22), but the one used in this model to account for nonhermetic package types is given in Reference 10, where the effects of ambient relative humidity, temperature, and the effective chip humidity have been modeled.

The time to failure distribution for the corrosion associated with moisture is modeled with a lognormal distribution and, per Reference 10, has a mean life of:

$$t_{50} = A \cdot e^{\frac{\Delta H}{KT}} \; e^{\frac{296}{RH_{EFF}}}$$

where ΔH is the activation energy (.2 eV) and RH_{EFF} is the effective relative humidity.

If the duty cycle is not 1.00, the average effective RH_{EFF} must be used in the t_{50} equation. Calculating this average value as a function of the junction and ambient RH's yields:

$$RH_{EFF} = DC \; RH_{EFF}\,(op) + (1 - DC)\; RH_{EFF}\,(dor)$$

where;

DC	= duty cycle (% operating time)
RH	= relative humidity of the environment
RH_{EFF} (op)	= operating effective RH
RH_{EFF} (dor)	= dormant effective RH

$$RH_{EFF} = DC\,(RH)\, e^{5230\left(\frac{1}{T_{J1}} - \frac{1}{T_A}\right)} + (1 - DC)\, RH\, e^{\left(\frac{1}{T_{J2}} - \frac{1}{T_A}\right)}$$

T_A	= normalizing temperature
T_{J1}	= operating junction temperature
T_{J2}	= nonoperating junction temperature ($T_{J2} = T_A$)

$$RH_{EFF} = (DC)\,(RH)\, e^{5230\left(\frac{1}{T_J} - \frac{1}{T_A}\right)} + (1 - DC)\,(RH)$$

$$(T_J = T_A + \theta_{JA}\, P)$$

Normalizing the temperature factor to 25°C and calculating the A constant according to the t_{50} values from Reference 10, yields the following t_{50} expression of the lognormal distribution:

$$t_{50} = .000086\, e^{\frac{.2}{8.63\times10^{5}}\left(\frac{1}{T_A} - \frac{1}{298}\right)} e^{\frac{2.96}{RH_{EFF}}}$$

where t_{50} is in 10^6 hrs. and $(0 < RH_{EFF} < 1)$.

It is well understood that there are typically large differences between manufacturers (and even large variations within manufacturers) regarding the quality and reliability of the plastic encapsulate material. However, as with the other wearout mechanisms modeled, the lognormal expression provides an estimate of the time at which the failure rate can be expected to increase and the end of life may be approaching.

5.5.7 Verifying Package Failure Rates with Temperature Cycling Data

Since the data collected for this effort indicates that package related failures are primarily accelerated by temperature, an exercise was undertaken to correlate the package failure rate with the number of temperature cycles the device has been exposed to. Although the results from this exercise will not be used in the final model, it was useful to observe the degree of correlation which existed in the re[illegible]'s of these two methodologies.

To accomplish this, instead of time being the independent variable, the number of temperature cycles was used and the method of modeling the early life failure rate mechanisms outlined in Section 3.0 was used. Also, instead of temperature and duty cycle being the acceleration factors, the temperature cycling rate was used.

For example, if the failure rate as a function of time (given in Figure 5-20) is derived based on temperature cycling tests then, as in the early life time dependent mechanisms case (metal, oxide, etc.), where the time acceleration factor is given by the temperature acceleration factor (Arrhenius), the failure rate for package related failures will be a function of number of cycles instead of time. To accomplish this the temperature cycling rates in Figure 5-21 for the Bay of an A-7C aircraft (from Reference 4) were used along with the duty cycle data of Table 5-24 (also from Reference 4) to derive a typical cycling rate.

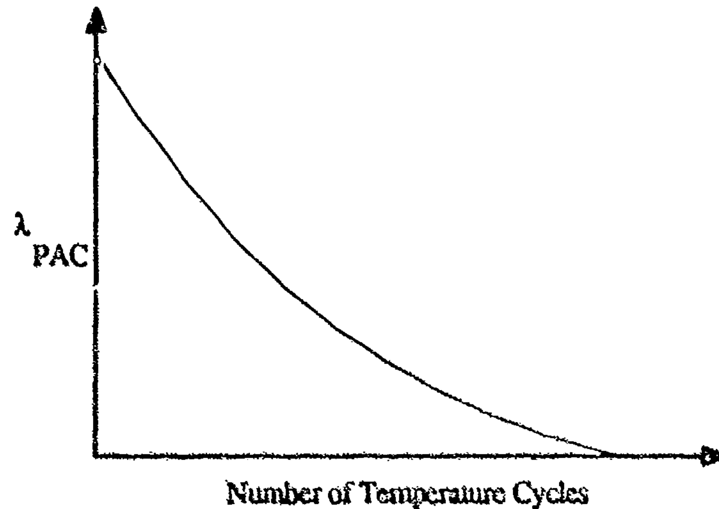


FIGURE 5-20:
HYPOTHETICAL FAILURE RATE AS A FUNCTION OF NUMBER OF CYCLES

TABLE 5-24:
AIRCRAFT UTILIZATION DATA

Aircraft Type	FHRS/ Sortie	Landings/ Month	Sorties Month	FHRS/ Month
A7D	1.53	14.95	14.97	22.91
YA7D	1.41	22.81	14.17	20.20
*A7	1.53	14.98	14.96	22.89
A10A	1.83	17.23	17.21	31.31
*A10	1.83	17.23	17.21	31.31
A37B	1.30	17.20	14.36	18.64
0A37B	1.36	19.63	8.91	11.74
*A37	1.30	17.78	13.28	17.28
B52G	6.79	12.72	4.66	31.64
B52H	7.29	10.89	4.32	31.11
*B52	7.00	7.73	2.60	20.50
FB111A	3.30	12.78	6.58	21.84
*FB111	3.30	12.78	6.58	21.84
C5A	4.96	36.43	11.44	56.61
*C5	4.96	36.43	11.44	56.61
C130A	2.23	32.04	12.27	27.31
C130B	2.28	39.58	15.22	34.52
C130D	1.85	27.79	14.83	26.94
C130E	2.34	51.80	21.89	51.09
C130H	2.54	52.59	24.33	61.06
*C130	2.44	42.25	17.45	42.44

*Indicates AN/ARN-118 RIW data.

TABLE 5-24:

AIRCRAFT UTILIZATION DATA (CONT'D)

Aircraft Type	FHRS/ Sortie	Landings/ Month	Sorties Month	FHRS/ Month
C141A	3.46	55.66	25.10	86.83
N0141A	2.48	20.92	6.61	16.59
Y0141B	1.60	18.17	9.00	14.18
*C141	3.46	54.28	24.34	84.05
KC135A	4.13	19.59	6.51	26.85
NKC135A	2.76	15.73	5.76	15.98
KC135Q	4.60	17.89	6.68	30.68
*C135	4.36	19.90	6.86	29.85
F4C	1.30	14.27	11.40	14.86
RF4C	1.53	17.27	13.43	20.64
F4D	1.30	16.76	13.44	19.54
F4E	1.29	17.50	15.14	19.54
F4G	1.33	15.04	14.68	19.40
*F4	1.34	16.66	13.76	18.48
F5E	0.97	25.60	25.50	24.59
*F5	0.98	28.34	25.02	24.49
F15A	1.30	15.05	15.00	19.54
F15B	1.36	31.15	17.36	23.63
F15C	1.42	15.91	15.54	21.90
F15D	1.40	13.41	12.85	17.73
*F15	1.32	17.31	15.45	20.45
F16A	1.26	15.28	14.74	18.6
	F16B	1.24	28.52	14.04
17.43				
*F16	1.26	20.95	14.46	18.20

TABLE 5-24:
AIRCRAFT UTILIZATION DATA (CONT'D)

Aircraft Type	FHRS/ Sortie	Landings/ Month	Sorties Month	FHRS/ Month
F111A	2.32	11.75	6.95	16.10
EF111A	3.21	9.25	9.25	28.68
F111D	2.24	11.97	8.07	18.07
F111E	2.49	8.08	7.27	17.88
F111F	2.49	8.28	7.27	18.13
*F111	2.36	10.13	7.37	17.48
T37B	1.27	84.72	23.97	30.51
*T37	1.27	84.72	23.97	30.51
T38A	1.22	77.48	22.87	28.00
*T38	1.21	73.84	22.89	27.57

*Indicates AN/ARN-118 RIW data.

This cycling rate data yielded of Figure 5-21 an approximate mission cycling rate of:

$$\frac{3 \text{ cycles}}{200 \text{ min.}} = .9 \frac{\text{cycles}}{\text{hr.}}$$

From the aircraft utilization data, a typical fighter will have a duty cycle of:

$$DC = \frac{20 \text{ flight hrs. per month}}{730 \text{ hrs. per month}}$$

$$DC = .027$$

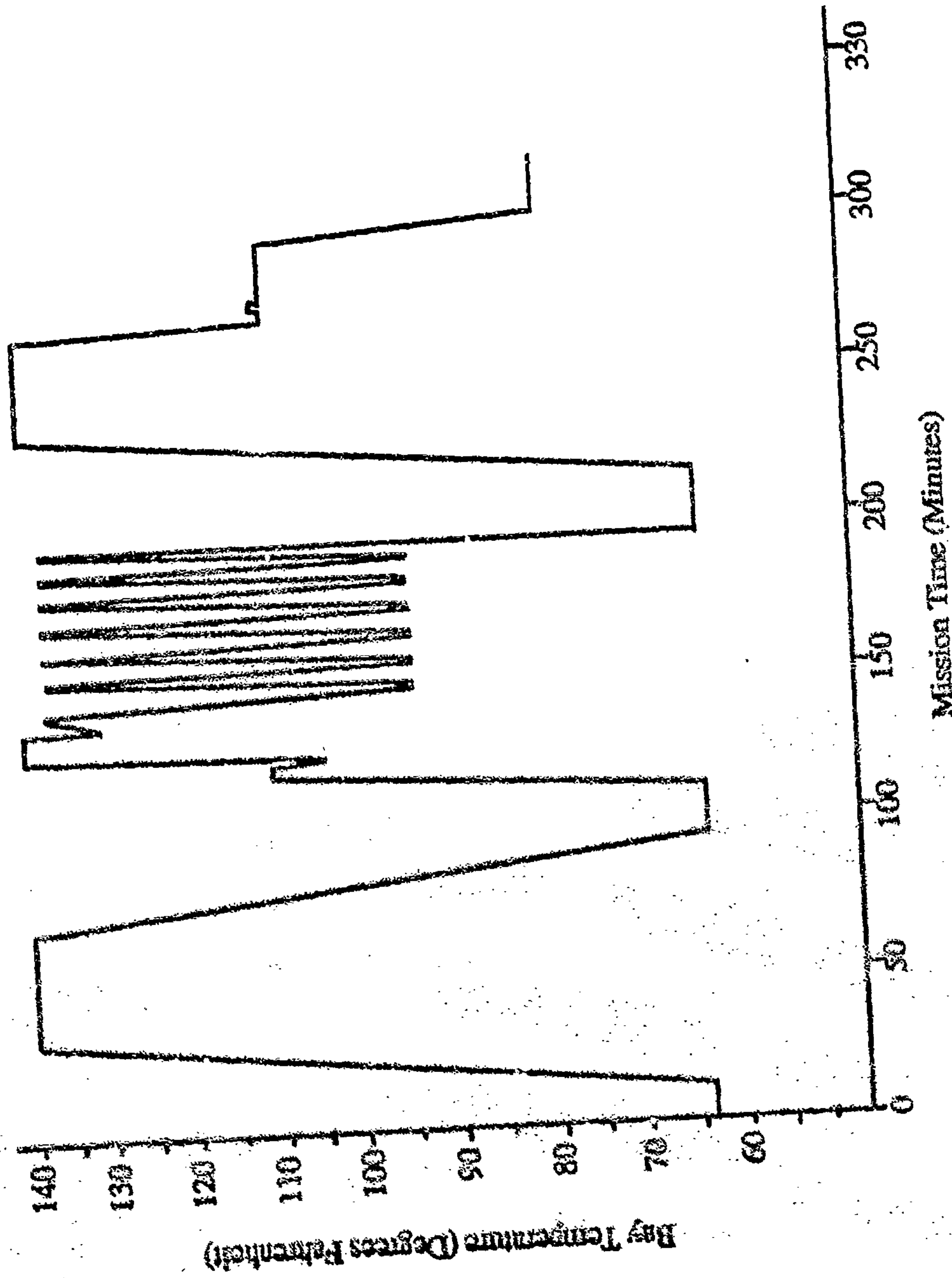


FIGURE 5-21: A-7D BAY TEMPERATURE
(HOT TEMPERATURE)

Next, a relationship was derived between the number of temperature cycles and failure rate. The same method used to develop the other early life failure rates was used (outlined in Section 3.0). Table 5-25 summarizes the data used. The first column lists the number of cycles interval at which the population of devices were tested for failure, the second column lists the total number of part cycles in that interval and the last column lists the number of observed failures in that interval. Table 5-26 summarizes the data used to derive this relationship.

TABLE 5-25:
PACKAGE DATA AS A FUNCTION
OF TEMPERATURE CYCLING

Cycles (10^6 Cycles)	Part Cycles	Number Failed
0 - 0.000100	0.762800	2
.000101 - 0.000300	1.451700	31
.000301 - 0.000500	1.379606	90
.000501 - 0.001000	3.190000	91

TABLE 5-26:
PACKAGE SUMMARY DATA

# Cycles Range (10^6 cycles)	Midpoint (10^6)	Part Cycles (10^6)	Failures	Failure Rate (F/10^6 Cycles)
0 - .000500	.000250	3.5941	123	34.2
.000500 - .001000	.000750	3.1900	91	28.2

Regressing on this data yields the following relationship:

$$\lambda\ (\#\ \text{cycles}) = 37\ e^{-365\ (\#\ \text{cycles})}$$

(where # cycles is in 10^6 cycles)

In the case of the package failure rate, a temperature acceleration factor is not applicable, rather it is the number of temperature cycles the device has been exposed to that is important. Therefore, the temperature acceleration factor can be replaced by a duty cycle which is the percentage of time the device is being cycled at a rate of .9 cyc./hr. As opposed to the other models for λ_{ox} λ_{MET}, etc., in this model the package failure rate is a worst case value that improves with a decreasing duty cycle. Although it is recognized that failures due to temperature cycling are primarily wearout related, the model was fit to data from a wide variety of devices, which tend to "smooth out" the failure rate function.

Adding the effects of screening and duty cycle, and converting number of cycles to time (using .9 cycles per hour) yields the following:

$$\lambda_{PAC} = 37 \left(\frac{F}{10^6 \text{ cyc.}}\right) .9 \left(\frac{\text{cyc.}}{\text{hr.}}\right) (DC)\, e^{.9\, t\, (DC)}\, e^{.365\, (\#\text{ cycles})}$$

where:

- F = Number of Failures
- $\frac{cyc}{hr.}$ = Cycles per hour
- DC = Duty Cycle

For a typical duty cycle factor of .027, the initial failure rate would be .90. This failure rate is somewhat pessimistic because the temperature extremes observed in the test data from which it was derived is greater than the actual temperature extremes associated with an uninhabited fighter environment. The lower failure rate yielded from the package factor presented previously were developed from actual field data, representative of a lower temperature extreme cycling situation. Decreasing the temperature extremes could easily decrease the failure rate by an order of magnitude. Also, the data used to derive this relationship is from a combination of DIPs, Pin Grid Arrays, and Chip Carriers, the mixture of which is inherently less reliable than the DIP data used previously. However, this exercise did provide an expected worst case failure rate which compares favorably with the package failure rate equation that will be used in this model.

5.5.8 Package Failure Rate Model Summary

A summary of the package failure rate is therefore given as follows and the values for these factors in the following tables.

$$\lambda_{PAC} = (.0024 + 1.85 \times 10^{-5} (\#Pins)) \pi_E \pi_{SP} \pi_{PT} + \lambda_{PH}$$

Application Environment Factors (Π_E)

Environment	Π_E	Environment	Π_E
G_E	.52	A_{IB}	6.8
G_{MS}	.88	A_{IA}	5.4
G_F	3.4	A_{IF}	8.1
G_M	5.7	A_{UC}	4.0
M_P	5.2	A_{UT}	5.4
N_{SB}	5.4	A_{UB}	10
N_S	5.4	A_{UA}	8.1
N_U	7.7	A_{UF}	12
N_H	8.0	S_{SF}	1.2
N_{UU}	8.6	M_{FF}	5.3
A_{RW}	12	M_{FA}	15
A_{IC}	3.4	M_L	17
A_{IT}	4.0	C_L	300

Package Screening Factor (Π_{SP})

Screen Level	Screen Class	Π_{SP}
No Screening	D	10
Burn-In	-	8.0
Environmental	-	2.8
Burn-In/Environmental	B	1.0

Package Type Factor (Π_{PT})

Package Type	π_{PT}
DIP	1.0
Pin Grid Array	2.2
Chip Carrier	4.7

λ_{PH} = Package Hermeticity Factor

λ_{PH} = 0 for Hermetic Packages

$$\lambda_{PH} = \frac{.399}{t\sigma_{PH}} \exp\left[\frac{-.5}{\sigma_{PH}^2}\left(\ln(t) + \ln(t_{50_{PH}})\right)^2\right] \text{ for nonhermetic packages}$$

$$t_{50_{PH}} = 86 \exp\left[\frac{\text{[illegible]}}{8.63\times10^{-5}}\left(\frac{1}{T_A} - \frac{1}{298}\right)\right] \exp\left[\frac{2.96}{RH_{EFF}}\right]$$

T_A = Ambient Temp.

$$RH_{EFF} = (DC)(RH)\, e^{5230\left(\frac{1}{T_J} - \frac{1}{T_A}\right)} + (1-DC)(RH)$$

(for example, for 50% Relative Humidity, use RH = .50)

5.6 ELECTRICAL OVERSTRESS FAILURE RATE

The occurrence of a catastrophic electrical overstress (EOS) event is an event related failure mechanism since it is the result of an externally supplied voltage or current. Since it is event related and not an inherent reliability failure mechanism, it is independent of time and dependent only on the probability of an EOS event, the magnitude of the overstressing voltage or current, and the susceptibility of the device to damage. It can therefore be modeled as a constant failure rate as a function of susceptibility level.

Although there are many types of EOS sources, each with their own characteristics, the best source of susceptibility information (and in most cases the only source) is the tests specified in MIL-STD-883, Method 3015. Although this is only one measure of the EOS susceptibility of a device, it is the most readily available and therefore will be used as an input into the model. The assumption in using this approach is that the EOS and ESD susceptibility levels are highly correlated.

Although it is also recognized that the electrical environment in which the device is deployed is a primary factor in the EOS failure rate, it cannot be used in the model since users of the model often have no control of the final environment and do not know the EOS characteristics of it. In some cases, the relative EOS severity between environments can be defined. For example, there appears to be more EOS failures from devices in avionics equipment, where power quality is always a concern. However, to quantify the magnitude of severity levels as a function of environment would be unduly complex and is beyond the scope of this study. Therefore the objective in deriving an EOS factor is that a "typical" EOS failure rate be derived only as a function of the ESD susceptibility of the device. By modeling the EOS failure rate in this manner, it is essentially being treated as an environmental stress.

The basic premise for this factor is the following relationship:

$$P(f) = P(f/c)P(c)$$

where:

P(f) is the probability of field failure due to Electrostatic Discharge or Electrical Overstress

P(f/c) is the probability of failure given that the device has been contacted by the EOS/ESD source

P(c) is the probability of contacting the device with the EOS/ESD source

To derive the probability of failure due to an EOS/ESD event, an EOS/ESD modal failure rate was developed by deriving a representative failure rate for integrated circuits (for a variety of device types and environments) and multiplying this failure rate by the percentage of failures observed to occur as a result of electrical overstress. These values were derived from the Reliability Analysis Center's data, which indicates that a total of 7948 failures were observed in a total of 16116 million part hours (yielding a failure rate of .493). Also from the RAC failure analysis database (Reference 75), 8.5 percent of all failures in the database were due to EOS/ESD, indicating that an EOS/ESD modal failure rate of .0419 ($F/10^6$). Therefore, under typical conditions in one year of operation, the probability of failure (P(f)) due to EOS/ESD is:

$$P(f) = 1 - e^{-\lambda_{ESD} t} = .000367$$

To derive a probability of failure given the device has been contacted with an EOS/ESD pulse P(f/c), data (from Reference 77) was used which identifies the failure voltage distribution for all microcircuits. This distribution is lognormal with a mean of approximately 2200 volts. The population from which this distribution was obtained and the population from which the EOS/ESD modal failure rate was calculated should be very similar since they are representative of a good cross-section of device types, technologies, and operational environments.

From data available in the literature (Reference 1) the voltage distributions given in Table 5-27 were defined for the stressing voltage as a function of the level of ESD protection in a given area (based on a normal distribution). The average listed in the table is the distribution used to represent the voltages present in the environment of the devices from which the EOS/ESD modal failure rate was derived.

TABLE 5-27:
ESD SOURCE VOLTAGE DISTRIBUTIONS

	ESD Protected	ESD Unprotected	Average
Mean	1175	8000	4600
Std. Deviation	375	1750	2000

It is reasonable to assume that the stress voltage distribution is not normally distributed as previously presumed (Reference 1) but rather lognormally or exponentially distributed. As illustrated in Figure 5-22, an exponential distribution is intuitively appealing since the probability of having a given voltage present in a particular situation increases with decreasing voltage.

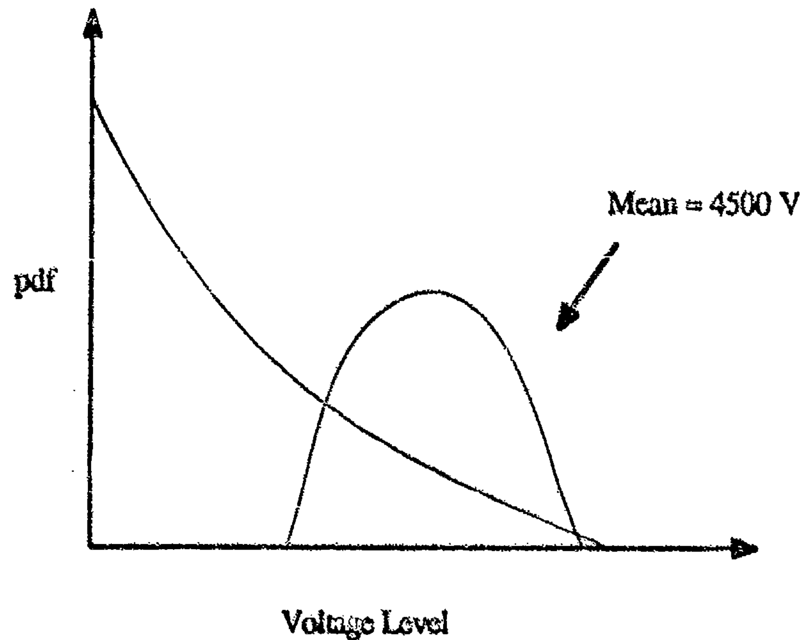


FIGURE 5-22:
STRESS VOLTAGE DISTRIBUTION

Assuming the exponential distribution and using the mean voltage for the normal of 4500 V and e[illegible]g this to the mean of an exponential ($\theta = \frac{1}{\lambda}$) yields a θ of .0002 and the following stress voltage disuribution:

$$\text{pdf } (V_{STRESS} = .0002\, e^{-.0002\, V}$$

Calculating the contact rate:

$$P(f/c)\, P(c) = P(f)$$

$$\text{for } t = .00876\ (\text{x}10^6 \text{ hrs.})$$

$$P(f) = 1 - e^{-\lambda_{EOS}\, t} = 1 - .999633 = .000367$$

(from empirical data $\lambda_{EOS} = .0419$ @ $t = .00876 \times 10^6$ hrs.)

$$P(f/c) = \frac{P(f)}{P(f/c)}$$

Assuming a mean threshold voltage of 2200 volts:

$$P(f/c) = 1 - \int_0^{2200\ V} .0002\, e^{-.0002\, V_{TH}}\, dV$$

$$= .644$$

where;

V_{TH} = ESD Voltage Threshold

$$\left(\text{in general } P(f/c) = 1 - \left[1 - e^{-.0002\, V_{TH}}\right] = -e^{-.0002\, V_{TH}}\right)$$

$$P(c) = \frac{P(f)}{P(f/c)} = \frac{.000367}{.644} = .00057$$

$$P(c) = 1 - e^{-\lambda_c\, t}$$

$$\lambda_c = \frac{-\ln(1-P(c))}{t} = .065 \frac{\text{contacts}}{10^6 \text{ hrs.}}$$

$$e^{-\lambda_{EOS} t} = \frac{1}{t} (-\ln (1 - P(f/c) (.00057))$$

$$P(f/c) = -e^{-.0002 V_{TH}}$$

Therefore,

$$\lambda_{EOS} = \frac{-\ln (1 - .00057 e^{-.0002 V_{TH}})}{.00876} (F/10^6 \text{ hrs.})$$

A graph relating λ_{EOS} to ESD susceptibility level is given in Figure 5-23.

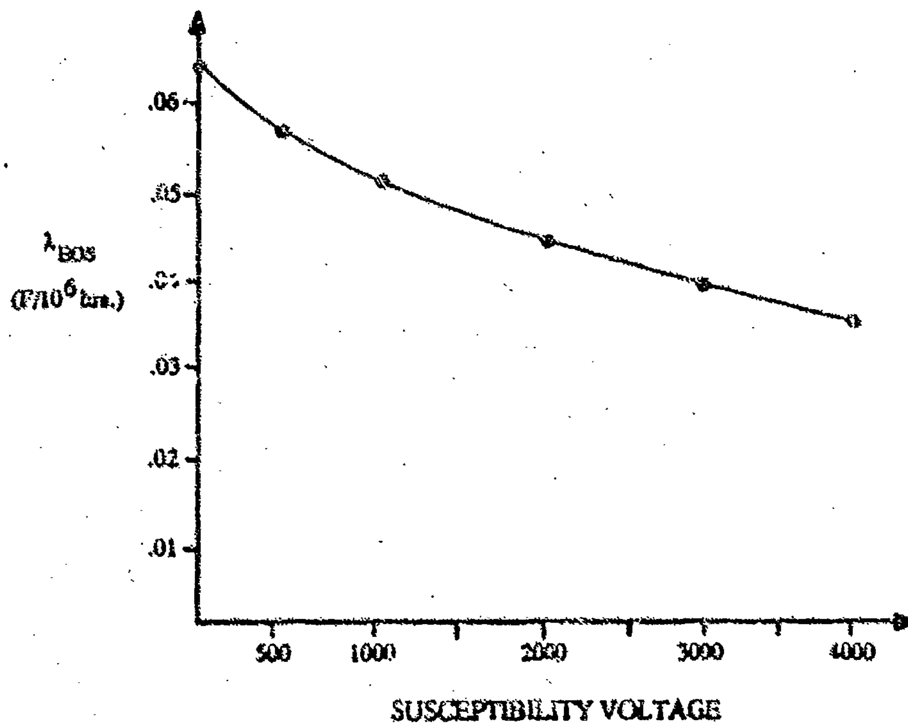


FIGURE 5-23: λ_{EOS} AS A FUNCTION OF SUSCEPTIBILITY

5.7 MISCELLANEOUS FAILURE RATE

A miscellaneous failure mechanism category was defined since there were various failure causes in the database which could not be categorized into one of the previously defined early life failure mechanisms. Rather than separating each of these miscellaneous mechanisms into a separate failure rate which would make the model more complex, they were summarized into one category which includes various failure mechanisms relating to the assembly and time dependent package failures causes. This miscellaneous failure rate is intended to be stricktly an emperical relationship used only to allow the predicted failure rates to be as close to the observed data as possible.

The package related failure rate derived previously was based only on failures induced by temperature cycling. There were a small percentage of package failures that occurred as a result of accelerated operational life testing. These failures, since they occurred during life tests are considered time dependent and are included in this miscellaneous category.

To derive this factor, the method (outlined in Section 3.0) used for the other early life failure rates was used. Since it was not a single mechanism being modeled an equivalent activation energy had to be derived. This was accomplished by weighting the acceleration due to temperature for each mechanism in accordance with the number of failures for that mechanism (Reference 7). Figure 5-24 illustrates this concept.

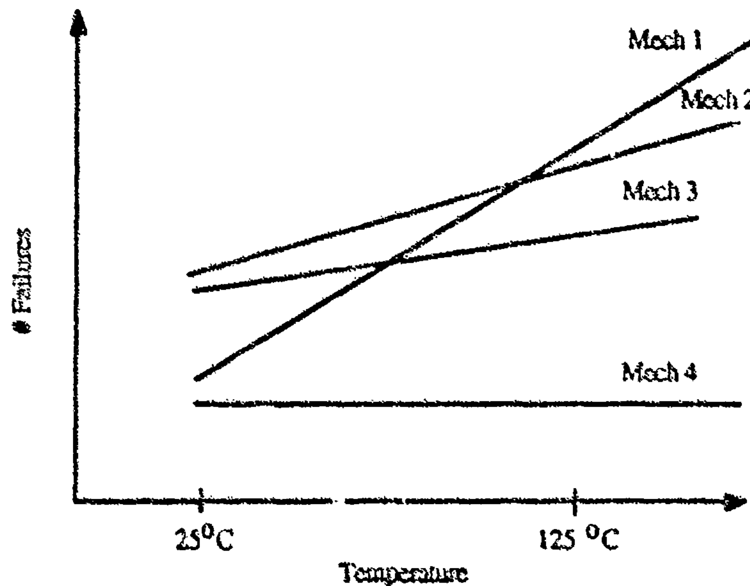


FIGURE 5-24: HYPOTHETICAL MIXTURE OF FAILURE RATES

Since the database contains primarily 125°C life test data, the number of failures at 25°C was projected for each failure mechanism based on the observed number of failures at 125°C. The equivalent activation energy was then calculated based on the weighted and combined individual accelerations. This activation energy was found to be .423 eV, and will be the one used to calculate the equivalent part hours for derivation of the miscellaneous early life failure rate. To derive this factor, the data in Table 5-28 was used. The summarized data used in derivation of this factor is given in Table 5-29:

TABLE 5-28:
FAILURE DATA FOR MISCELLANEOUS FAILURE RATE

Effective Time Interval (10^6 hrs.)	Effective Part Hours (10^6 hrs.)	Number of Failures
0 - 0.011543	3175.006037	2
.011544 - 0.020183	2372.378700	1
.020184 - 0.040402	5501.966794	42
.040403 - 0.066083	4944.568256	1
.066084 - 0.070642	868.808198	1
.070643 - 0.082514	2198.587890	2
.082515 - 0.112394	5498.847131	1
.112395 - 0.120244	1430.374353	6
.120245 - 0.210243	15242.040931	15
.210244 - 0.240488	5036.427332	4
.240489 - 0.242412	29.643048	5
.242413 - 0.355239	1255.910793	1
.355240 - 0.393352	458.155979	1
.393353 - 0.420487	271.892485	1
.420488 - 1.510862	200.857977	4

TABLE 5-29:
SUMMARIZED MISCELLANEOUS FAILURE DATA

Effective Time Interval (10^6 hrs.)	Midpoint (10^6)	Part Hours (10^6)	Number of Failures	Failure Rate (F/10^6 hrs.)
0 - .040402	.020201	11049	45	.00407
.040403 - 1.510862	.73520	37434	42	.00112

This data yielded the following relationship:

$$\lambda_{MIS} = .0042\ e^{-2.2\ t}$$

Accounting for unknown failures and adding the effects of acceleration due to temperature and screening yields:

$$\lambda_{MIS} = (.01\ e^{-2.2\ t_o})\ (A_{T_{MIS}})\ (e^{-2.2\ A_{T_{MIS}} t})$$

where $A_{T_{MIS}}$ = Temperature Acceleration Factor

$$= \exp\left[\frac{-.423}{8.63\text{x}10^{-5}}\left(\frac{1}{T_J} - \frac{1}{298}\right)\right]$$

t_o = Effective Screening Time

= $A_{T_{MIS}}$ (at Screening Temp.) * Actual Screening Time (in 10^6 hours)

t = time (in 10^6 hrs.)

6.0 DETAILED MODEL SUMMARY

This section summarizes the detailed model in its entirety. Table 6-1 summarizes the input parameters of the detailed model and their default values. The default values are either averages of the values contained in the database or "typical" values.

TABLE 6-1:
INPUT PARAMETERS

VARIABLE	UNITS	DEFAULT
Die Area	cm^2	.21 cm^2
Device Type		*
1) Custom and Logic		
2) Memory and Gate Array		
Defect Density	Def/cm^2	1
Feature Size	Micron	2
Power (Actual) (P)	Watt	*
Theta-JA (θ_{JA})	^oC/watt	(See Table 5-23)
Theta-JC (θ_{JA})	^oC	-
Ambient Temperature (T_A)	^oC	*
Screening Duration	10^6 hours	*
Screening Temperature	^oC	*
Screening Power Dissipated	watt	*
Current Density in Metal (J)	10^6 Å /cm^2	.5
Electric Field in Oxide (E_{ox})	MV/cm	2
Substrate Current (I_{sub})	mA	$.0058\ e^{-.00689\ T_J}$
Drain Current (I_d)	mA	$3.5\ e^{-.00157\ T_J}$
Proven Mfg. Process (on QML?)		*
1) yes		
2) No		
Sigma Oxide (σ_{ox})	-	1
Sigma Metal (σ_{MET})	-	.5
Sigma Hot Carriers (σ_{HC})	-	1.1
Package Type	-	*
Pin Count (NP)	-	*
Environmental Screens Applied		*

TABLE 6-1:
INPUT PARAMETERS (CONT'D)

VARIABLE	UNITS	DEFAULT
Application Environment		
1) None		
2) Burn-In		
3) Environmental		
4) Burn-In/Environmental		
ESD Susceptibility (V_{TH})	Volts	1000V
Duty Cycle (DC)	-	1
Correction Factor (π_c)		1

* Needed as an input to detailed model

VHSIC/VHSIC-LIKE FAILURE RATE MODEL

$$\lambda_P(t) = \left[\lambda_{OX}(t) + \lambda_{MET}(t) + \lambda_{HC}(t) + \lambda_{CON}(t) + \lambda_{PAC} + \lambda_{ESD} + \lambda_{MIS}(t)\right]\pi_C$$

$\lambda_P(t)$ = Predicted Failure Rate as a Function of Time

$\lambda_{OX}(t)$ = Oxide Failure Rate

$\lambda_{MET}(t)$ = Metallization Failure Rate

$\lambda_{HC}(t)$ = Hot Carrier Failure Rate

$\lambda_{CON}(t)$ = Contamination Failure Rate

λ_{PAC} = Package Failure Rate

λ_{ESD} = EOS/ESD Failure Rate

$\lambda_{MIS}(t)$ = Miscellaneous Failure Rate

π_C = Field Correction Factor = 1

The Field Correction Factor (π_C) is currently 1 but may change in the future when field failure rates become available.

The equations for each of the above failure mechanism failure rates are on the following pages.

OXIDE FAILURE RATE EQUATION

$$\lambda_{ox}\ (\text{in F}/10^6) = \frac{A\ A_{TYPE_{OX}}}{A_R}\left(\frac{D0_{ox}}{D_R}\right)\left[(.0788\, e^{-7.7\, t_0})\,(A_{T_{ox}})\,(e^{-7.7\, A_{T_{ox}} t}) + \frac{.399}{(t+t_0)\sigma_{ox}} \exp\left(\frac{-.5}{\sigma_{ox}^2}\left(\ln(t+t_0) - \ln t_{50_{ox}}\right)^2\right)\right]$$

A = Total Chip Area (in cm^2) (typical values for this area range approximately from .1 to $1 cm^2$)

$A_{TYPE_{OX}}$ = .77 for Custom and Logic Devices

= 1.23 for Memories and Gate Arrays

A_R = $.21\ cm^2$

$D0_{ox}$ = Defect Density (If unknown, use $\left(\frac{X_0}{X_s}\right)^2$ where $X_0 = 2\ \mu m$ and X_s is the feature size of the device)

D_R = 1 Defect/cm^2

t_0 = Effective Screening Time

= (Actual Time of Test (in 10^6 hrs.)) * ($A_{T_{ox}}$ (at junction screening temp.) (in °K))* ($A_{V_{ox}}$ (at screening voltage))

OXIDE FAILURE RATE EQUATION (CONTINUED)

A_{Tox} = Temperature Acceleration Factor

$$= \exp\left[\frac{-.3}{8.63\times10^{-5}}\left(\frac{1}{T_J} - \frac{1}{298}\right)\right]$$

where $T_J = T_C + \theta_{JC}P$ (in °K)

$$A_{Vox} = e^{-192\left(\frac{1}{E_{ox}} - \frac{1}{2.5}\right)}$$

E_{ox} = Maximum Power Supply Voltage V_{DD}, divided by the gate oxide thickness (in MV/cm)

$$t_{50ox} = \frac{1.3\times10^{22}\,(QML)}{AT_{ox}\,AV_{ox}} \quad \text{(in } 10^6 \text{ hrs.)}$$

(QML) = 2 if on QML, .5 if not.

σ_{ox} = Sigma obtained from test data of oxide failures from the same or similar process. If not available, use a σ_{ox} value of 1.

t = Time (in 10^6 Hours)

METAL FAILURE RATE EQUATION

$$\lambda_{MET} = \left[\frac{A\ A_{TYPE_{MET}}}{A_R}\frac{D_{0_{MET}}}{D_R}\ (.00102\ e^{-1.18\ t_0})(A_{T_{MET}})(e^{-1.18\ A_{T_{MET}} t})\right]$$

$$+\left[\frac{.399}{(t+t_0)\sigma_{MET}} \exp\left(\frac{-.5}{\sigma_{MET}^2}\left(\ln(t+t_0) - \ln t_{50_{MET}}\right)^2\right)\right]$$

A = Total Chip Area (in cm^2) (typical values for this area range approximately from .1 to 1 cm^2)

$A_{TYPE_{MET}}$ = .88 for Custom and Logic Devices

= 1.12 for Memory and Gate Arrays

A_R = .21 cm^2

$D_{0_{MET}}$ = Defect Density as Calculated in Appendix B (If unknown use $\left(\frac{X_0}{X_S}\right)^2$ where $X_0 = 2\ \mu m$ and X_S is the feature size of the device)

D_R = 1 Defect/cm^2

$A_{T_{MET}}$ = Temperature Acceleration Factor

$$= \exp\left[\frac{-.55}{8.63 \times 10^{-5}}\left(\frac{1}{T_J} - \frac{1}{298}\right)\right]$$

$T_J = T_{CASE} + \theta_{JC}P$ (in °K)

t_0 = Effective Screening Time (in 10^6 hrs.)

= $A_{T_{MET}}$ (at Screening Temp. (in °K)) * (Actual Screening Time (in 10^6 hrs)) (to Calculate t_0 use $A_{T_{MET}}$ based on the junction temperature during screening)

$$t_{50_{MET}} = (QML)\frac{.388 * (\text{Metal Type})}{J^2 A_{T_{MET}}} \quad (\text{in } 10^6 \text{ hrs.})$$

(QML) = 2 if on QML, .5 if not.

Metal Type = 1 for Al

37.5 for Al-Cu or for Al-Si-Cu

J = The mean absolute value of Metal Current Density (in 10^6 Amps/cm^2)

σ_{MET} = sigma obtained from test data on electromigration failures from the same or a similar process. If this data is not available use $\sigma_{MET} = 1$

t = time (in 10^6 hrs.)

HOT CARRIER FAILURE RATE EQUATION

$$\lambda_{HC} = \frac{.399}{t\sigma_{HC}} \exp\left[\frac{-.5}{\sigma_{HC}^2}\left(\ln(t + t_0) - \ln t_{50_{HC}}\right)^2\right]$$

$$t_{50_{HC}} = \frac{(QML)3.74\times10^{-5}}{A_{T_{HC}} I_d}\left(\frac{I_{sub}}{I_d}\right)^{-2.5}$$

(QML) = 2 if on QML, .5 if not

$$A_{T_{HC}} = \exp\left[\frac{.039}{8.63\times10^{-5}}\left(\frac{1}{T_J} - \frac{1}{298}\right)\right]$$

where $T_J = T_C + \theta_{JC}P$ (in °K)

I_d = Drain Current at Operating Temperature. If unknown use

$I_d = .0058\, e^{-.00157\, T_J}$ (in °K) (mA)

I_{sub} = Substrate Current at Operating Temperature. If unknown use

$I_{sub} = 3.5\, e^{-.00689\, T_J}$ (in °K) (mA)

σ_{HC} = sigma derived from test data, if not available use 1.1

t_0 = $A_{T_{HC}}$ (at Screening Temp.(in °K)) • (Test Duration in 10^6 hours)

t = time (in 10^6 hrs.)

CONTAMINATION FAILURE RATE EQUATION

$$\lambda_{CON} = .000022\, e^{-.0028\, t_0 A_{T_{CON}}}\, e^{-.0028\, A_{T_{CON}} t}$$

$A_{T_{CON}}$ = Temperature Acceleration Factor

$$= \exp\left[\frac{-1.0}{8.63\text{x}10^{-5}}\left(\frac{1}{T_J} - \frac{1}{298}\right)\right]$$

where $T_J = T_C + \theta_{JC}P$ (in °K)

t_0 = Effective Screening Time

= $A_{T_{con}}$ (at screening junction temperature (in °K)) * (actual screening time in 10^6 hrs.)

t = time (in 10^6 hrs.)

PACKAGE FAILURE RATE EQUATION

$$\lambda_{PAC} = (.0024 + 1.85 \times 10^{-5} (\#Pins)) \pi_E \pi_{SP} \pi_{PT} + \lambda_{PH}$$

Application Environment Factors (Π_E)

Environment	Π_E	Environment	Π_E
G_E	.52	A_{IB}	6.8
G_{MS}	.88	A_{IA}	5.4
G_F	3 4	A_{IF}	8.1
G_M	5.7	A_{UC}	4.0
M_P	5.2	A_{UT}	5.4
N_{SB}	5.4	A_{UB}	10
N_S	5.4	A_{UA}	8.1
N_U	7.7	A_{UF}	12
N_H	8.0	S_{SF}	1.2
N_{UU}	8.6	M_{FF}	5.3
A_{RW}	12	M_{FA}	15
A_{IC}	3.4	M_L	17
A_{IT}	4.0	C_L	300

Package Screening Factor (Π_{SP})

Screen	Quality Level*	Π_{SP}
No Screening	D	10
Burn-In	-	8.0
Environmental	-	2.8
Burn-In/Environmental	-	1.0

*Quality level as defined in Table 5.1.2.7-1 of MIL-HLBK-217.

PACKAGE (CONTINUED)

Package Type Factor (Π_{PT})

Package Type	Π_{PT}
DIP	1.0
Pin Grid Array	2.2
Chip Carrier	4.7

λ_{PH} = Package Hermeticity Factor

λ_{PH} = 0 for Hermetic Packages

$$\lambda_{PH} = \frac{.399}{t\sigma_{PH}} \exp\left[\frac{-.5}{\sigma_{PH}^2}\left(\ln(t) - \ln(t_{50_{PH}})\right)^2\right] \text{ for nonhermetic packages}$$

$$t_{50_{PH}} = 86 \exp\left[\frac{.2}{8.63\times10^{-5}}\left(\frac{1}{T_A} - \frac{1}{298}\right)\right] \exp\left[\frac{2.96}{RH_{EFF}}\right]$$

T_A = Ambient Temp. (in °K)

$$RH_{eff} = (DC)(RH)\, e^{5230\left(\frac{1}{T_J} - \frac{1}{T_A}\right)} + (1-DC)(RH)$$

where $T_J = T_C + \theta_{JC}P$ (in °K)

(for example, for 50% Relative Humidity, use RH = .50)

$\sigma_{PH} = .74$

t = time (in 10^6 hrs.)

EOS/ESD FAILURE RATE EQUATION

$$\lambda_{EOS} = \frac{-\ln(1 - .00057\, e^{-.0002\, V_{TH}})}{.00876}$$

V_{TH} = ESD Threshold of the device using a 100 pF, 1500 ohm discharge model

MISCELLANEOUS FAILURE RATE EQUATION

$$\lambda_{MIS} = (.01\, e^{-2.2\, t_o})\,(A_{T_{MIS}})\,(e^{-2.2\, A_{T_{MIS}}\, t})$$

$A_{T_{MIS}}$ = Temperature Acceleration Factor

$$= \exp\left[\frac{-.423}{8.63\text{x}10^{-5}}\left(\frac{1}{T_J} - \frac{1}{298}\right)\right]$$

where $T_J = T_C + \theta_{JC}P$ (in °K)

t_o = Effective Screening Time

= $A_{T_{MIS}}$ (at Screening Temp. (in °K)) * Actual Screening Time (in 10^6 hours)

t = time (in 10^6 hrs.)

7.0 SHORT FORM MODEL

7.1 DERIVATION METHODOLOGY

The detailed model presented previously is intended to model VHSIC CMOS failure rates as accurately as possible. As discussed in the introduction of this report, it is recognized that there is a need for a much simplified model, both in the data required for calculation and in the complexity of the calculations themselves.

To accomplish this, a short form model was derived from the detailed version. The following model form was chosen which has additive failure rates for die related failure mechanisms, package related failure mechanisms, and electrical overstress; each multiplied by the appropriate correction factors:

$$\lambda_P = \lambda_{BD}\pi_{MFG}\pi_T\pi_{SD}\pi_{CD} + \lambda_{BP}\pi_E\pi_{SP}\pi_{PT} + \lambda_{EOS}$$

where:

λ_{BD}	is the base failure rate for the die
π_{MFG}	is the correction factor based on the manufacturing process
π_T	is the die temperature factor
π_{SD}	is the die screening factor
π_{CD}	is the die complexity factor
λ_{BP}	is the package base failure rate
π_E	is the environment factor
π_{SP}	is the package screening factor
π_{PT}	is the package type factor
λ_{EOS}	is the failure rate due to electrical overstress

The derivation of each of these factors is summarized as follows.

7.1.1 Temperature Factor

To develop a temperature acceleration factor for the short form model, an average "equivalent" activation energy had to be derived, recognizing that a single activation energy is an approximation and only applicable for a single failure mechanism. To accomplish this, the detailed model was exercised for a variety of conditions and various temperatures and an average activation energy calculated from the resulting failure rate ratios at various temperatures. As with the individual failure mechanisms, the following temperature acceleration factor form was used:

$$\pi_T = e^{\frac{-Ea}{K}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)}$$

where:

- Ea is the equivalent activation energy
- K is the Boltman's Constant
- T_1 is the junction temperature
- T_2 is a reference temperature

Calculating an average Ea yielded a value of .33 eV. Therefore, normalizing the acceleration factor to 298 degrees Kelvin, the temperature acceleration factor becomes:

$$\pi_T = e^{\frac{-.33}{8.63 \times 10^{-5}}\left(\frac{1}{T_J} - \frac{1}{298}\right)}$$

7.1.2 Die Screening Factor

The overall effects of burn-in can also be determined from the detailed model by knowing the duration and the junction temperature of the burn-in. Since the detailed model has a decreasing failure rate for the defect related early life failure mechanisms, the effects of burn-in can easily be determined by exercising the model for various burn-in lengths and temperatures. The failure rate improvement after the burn-in can then be determined. The lengths and temperatures chosen were those of Class D, B and S (per MIL-HDBK-217) quality level devices. For these devices, the following relative burn in factors were derived (normalizing Class D (no burn-in) to 1.

TABLE 7-1:
DIE SCREENING FACTOR

Class	π_{SD}*
D	1
B	.94
S	.85

*QML parts will initially be exposed to Class B screening as a baseline. Further refinement of this factor will be made as data becomes available.

7.1.3 Die Complexity Factor

The die complexity factor in the detailed model was a function of die area and defect density. The area acceleration factor was (Area (in cm^2))/.21, and the default defect density value to be used in the short form model is:

$$D=\left(\frac{2}{X_S}\right)^2$$

where: X_S = feature size

The die complexity factor (Π_{CD}) is therefore,

$$\Pi_{CD}=\frac{A}{.21}\left(\frac{2}{X_S}\right)^2$$

where

A = Area in cm^2
X_S = Feature size in microns

which yields the relative complexity factors in Table 7-2, as a function of chip area and feature size.

TABLE 7-2:
DIE COMPLEXITY FACTOR

Feature Size (Microns)	Chip Area (cm^2) .1-2	.2-.4	.4-1.0	1.0-2	2-3
1.00	2.8	5.7	13	28	47
1.25	1.9	3.9	9.0	19	32
1.50	1.3	2.5	5.9	13	21
2.00	.71	1.4	3.3	7.1	12
2.50	.45	.92	2.1	4.6	7.6
3.00	.31	.63	1.5	3.1	5.2

However, since only the metal and oxide failure rates are accelerated with the feature size/die area factor, the factors in Table 7.1-2 must be decreased accordingly. From the life test data presented in Table 4-2 (excluding unknown, assembly and package failures), 64% of die failures are due to metal and oxide (173 failures out of 272) and therefore the actual π_C should be:

$$\pi_C = \left[\frac{A}{.21}\left(\frac{2}{X_S}\right)^2 (.64)\right] + .36$$

which yields the π_C values in Table 7-3.

TABLE 7-3:
SHORT FORM MODEL DIE COMPLEXITY FACTOR

Feature Size (Microns)	Chip Area (cm^2) .1-2	.2-.4	.4-1.0	1.0-2	2-3
1.00	2.1	4.0	8.7	18	30
1.25	1.6	2.8	6.1	12	21
1.50	1.2	2.0	4.1	8.7	14
2.00	.81	1.3	2.5	4.9	8.0
2.50	.65	.95	1.7	3.3	8.2
3.00	.56	.76	1.3	2.3	3.7

7.1.4 Manufacturing Process

Since the detailed model assumes that the differences in manufacturing processes are accounted for in the defect density term and since the short form model will always use the default condition for defect density, $\left(\frac{2}{X_2}\right)^2$, there must be a way to incorporate the effects of the level of control in a manufacturing process into the short form model. The rationale for including the effect of the manufacturing process is that companies on the Qualified Manufacturers List (QML) or the Qualified Products List (QPL) must have demonstrated to the qualifying activity that its technology has low failure rates for time dependent dielectric breakdown, electromigration and hot carrier degradation. Non QML manufacturing lines generally do not demonstrate these low failure rates in such a thorough manner to outside organizations.

To incorporate the effects of manufacturing process control, the 1.0 and 1.2 micron failure rate data was used and a defect density required to make the observed and predicted failure rates the same was calculated. The mean of these calculated defect densities was then taken for each manufacturer, and a 8.5:1 ratio was observed from the best to worst manufacturer. Therefore, assuming this range in defect densities based on the level of process control, the following categories can be defined along with their associated defect densities:

Manufacturing Process	D
QML or QPL	.33
Non QML or QPL	2.5

For the summarized model, these numbers must be scaled in accordance with the following, since only 64% of all die related failures are typically due to oxide or metal. Table 7-4 presents the final factors.

$$\pi_{MFG} = (.64)\, D + .36$$

TABLE 7-4:
π_{MFG} VALUES

Manufacturing Process	π_{MFG}
QML or QPL	.55
Non QML or QPL	2.0

7.1.5 Package Failure Rate

Since the detailed model package failure rate is not a function of time and it is relatively simple to use, it can essentially be used as is in the short form model. One part of the package failure rate model that was time dependent and cannot be used is the treatment of plastic packages. Since the short form model cannot be time dependent, another approach was be taken to account for long term reliability degradation due to nonhermetic effects. To accomplish this, the fallout rate of the various package types was modified by adding to them a typical fallout rate for plastic devices exposed to temperature/humidity tests. A typical fallout rate for this test is .4%.

In previous sections of this report, the fallout rates listed in Table 7-5 were presented as a function of package type:

TABLE 7-5:
PACKAGE TYPE FALLOUT RATES

Package Type	FO (%)
Chip Carrier	1.03
Pin Grid Array	.49
DIP	.22

Data in Table 5-21, which presents early life fallout rate differences between plastic and hermetic parts, can not be used to derive their relative failure rates since that data is representative of screen tests used to detect package defects. The Pi factor being developed for plastic packages here is intended to be representative of its expected long term reliability.

Therefore, to account for plastic encapsulation, .4 can be added to the fallout rates in Table 7-5 to account for long term nonhermetic reliability effects. Therefore, the fallout rates listed in table 7-6 were used. Based on these fallout rates, a π_{PT} can be derived in the same manner as in the detailed model and these values are summarized in Table 7-7.

TABLE 7-6:
FALLOUT RATE AS A FUNCTION OF PACKAGE HERMETICITY

Package Type	FO Rate	
	Hermetic	Nonhermetic
Chip Carrier	1.03	1.43
Pin Grid Array	.49	.89
DIP	.22	.62

TABLE 7-7:
SHORT FORM PACKAGE TYPE FACTOR

Package Type	π_{PT}	
	Hermetic	Nonhermetic
Chip Carrier	4.68	6.50
Pin Grid Array	2.23	4.05
DIP	1	2.82

A summary of the short form model package failure rate therefore is as follows:

λ_{BP} = Package Base Failure Rate

$= .0024 + (1.85 \times 10^{-5})$ (# Pins)

Application Environment Factors (Π_E)

Environment	Π_E	Environment	Π_E
G_E	.52	A_{IB}	6.8
G_{MS}	.88	A_{IA}	5.4
G_F	3.4	A_{IF}	8.1
G_M	5.7	A_{UC}	4.0
M_P	5.2	A_{UT}	5.4
N_{SB}	5.4	A_{UB}	10
N_S	5.4	A_{UA}	8.1
N_U	7.7	A_{UF}	12
N_H	8.0	S_{SF}	1.2
N_{UU}	8.6	M_{FF}	5.3
A_{RW}	12	M_{FA}	15
A_{IC}	3.4	M_L	17
A_{IT}	4.0	C_L	300

Package Screening Factor (Π_{SP})

Screen Level	Class	π_{SP}*
None	D	10
Burn-In	-	8.0
Environmental	-	2.8
Burn-In/Environmental	B	1.0

*QML Parts will initially be exposed to Class B screening as a baseline. Further refinement of this factor will be made as data becomes available.

Package Type Correction Factor (Π_{PT})

Package Type	Π_{PT} Hermetic	Π_{PT} Nonhermetic
DIP	1.0	2.8
Pin Grid Array	2.2	4.0
Chip Carrier	4.7	6.5

7.1.6 Die Base Failure Rate

To derive a die base failure rate λ_{BP} for the short form model, the following procedure was used:

(1) A prediction was performed with the detailed model for a variety of temperatures, screen durations, die areas, and feature sizes.

(2) The twenty year average failure rate was calculated for each of these combinations λ_p.

(3) A base failure rate was calculated for each combination to make the prediction failure rate in the short form model equal to the 20 year average predicted from the detailed model:

$$\lambda_{BD} = \frac{\lambda_p - \lambda_{PAC}}{\pi_{TYPE}\pi_T\pi_{SD}\pi_{CD}\pi_{MFG}}$$

(4) The geometric mean of these base failure rates was taken.

The data used in calculation of these base failure rates are summarized in Table 7-8 and yielded a λ_{BD} value of .025 F/10^6 hrs.

TABLE 7-8
DATA USED IN CALCULATING SHORT FORM DIE BASE FAILURE RATE

Part ID	Conditions: DIE: Temp. (°C)	Screen Level at 125°C (160 hrs. = Class B)	Die Complexity: Area cm2	Feat Size (micron)	Package: Type	# Pins	Screen Level	Env.	Detailed Model λp (20 Year (Average)	Summarized Model Factors: λPAC	π_{TYPE}	π_T	π_s	π_{CD}	λ_{BD}
												Ea 2.33			
1	25	None	.15	3	HERM PGA	120	Burn-In	Benign	.151	.081	1.19	1	1	.56	.103
2	25	None	.7	1.5					.457			1	1	4.1	.077
3	25	None	2.5	1.0					2.73			1	1	30	.074
4	25	160 hr.	.15	3					.130			1	.94	.56	.078
5	25	160 hr.	.7	1.5					.420			1	.94	4.1	.076
6	25	160 hr.	2.5	1.0					2.64			1	.94	30	.076
7	75	None	.15	3					.187			6.32	1	.56	.167
8	75	None	.7	1.5					.648			6.32	1	4.1	.018
9	75	None	2.5	1.0					4.07			6.32	1	30	.018
10	75	160 hr.	.15	3					.166			6.32	.94	.56	.021
11	75	160 hr.	.7	1.5					.615			6.32	.94	4.1	.018
12	75	160 hr.	2.5	1.0					3.95			6.32	.94	30	.018
13	125	None	.15	3					.274			25.1	1	.56	.011
14	125	None	.7	1.5					.85			25.1	1	4.1	.006
15	125	None	2.5	1.0					5.17			25.1	1	30	.006
16	125	160 hr.	.15	3					.251			25.1	.94	.56	.011
17	125	160 hr.	.7	1.5					.817			25.1	.94	4.1	.006
18	125	160 hr.	2.5	1.0					5.02			25.1	.94	30	.006
															Geometric Mean = .025

(P = 0 so that $T_A = T_J$)

$\pi_{MFG} = 1$

As described in the detailed model, the failure rate is a function of the device type and separates the failure rate due to oxide and metal. The A_{TYPE} correction factors for Metal and Oxide therefore should be weighted (in accordance with the number of failures expected for each) and combined. For custom and logic devices:

$$A_{TYPE} = .64\,(.77) + .36\,(.88) \qquad \begin{pmatrix} 64\%\ \text{oxide} \\ 36\%\ \text{metal} \end{pmatrix}$$
$$= .81$$

For memories and gate arrays:

$$A_{TYPE} = .64\,(1.23) + .36\,(1.12)$$
$$= 1.19$$

Since this A_{TYPE} factor only effects the oxide & metal failure rate the actual factor should be (since 64% of all failures are due to oxide or metal):

$$A_{TYPE_{ACTUAL}} = A_{TYPE}\,(.64) + .36$$

Therefore for custom and logic devices A_{TYPE} .88 and for memories and gate arrays, $A_{TYPE} = 1.12$.

Combining this device type correction factor with the base failure rate results in the following base failure rate as a function of device type:

Device Type	λ_{BD}
Custom and Logic	.02
Memories and Gate Array	.03

7.1.7 Short Form Model Summary

The complete short form model is presented on the following pages in a format intended to be replacement pages for MIL-HDBK-217.

The part operating predicted failure rate (λ_P) is:

$$\lambda_P = \lambda_{BD}\Pi_{MFG}\Pi_{SD}\Pi_{CD} + \lambda_{BP}\Pi_E\Pi_{SP}\Pi_{PT} + \lambda_{EOS}$$

where:

λ_P is the Device Predicted Failure Rate in F/10^6 Hours.

λ_{BD} is the Die Base Failure Rate:

For Logic and Custom Devices, $\lambda_{BD} = .02$
For Memories and Gate Arrays, $\lambda_{BD} = .03$

Π_{MFG} is the Manufacturing Process Correction Factor, Table 1.

Π_T is the Temperature Acceleration Factor, Table 2.

Π_{SD} is the Die Screening Correction Factor, Table 3.

Π_{CD} is the Die Complexity Corrective Factor, Table 4, based on the Area (in cm^2) and the Feature Size (in Microns) of the Die.

λ_{BP} is the Package Base Failure Rate:

$\lambda_{BD} = .0024 + (1.85 \times 10^{-5})$ (NP)
where NP = Number of Package Pins

Π_E is the Environment Factor, Table 5.

Π_{SP} is the Package Screening Factor, Table 6.

Π_{PT} is the Package Type Correction Factor, Table 7.

λ_{EOS} is the Failure Rate due to Electrical Overstress, Table 8, based on the Electrostatic Discharge Susceptibility of the Part, in Volts.

TABLE 1:
Π_{MFG}, MANUFACTURING PROCESS CORRECTION FACTOR

Manufacturing Process	Π_{MFG}
QML or QPL	.55
Non QML or Non QPL	2.0

TABLE 2:
TEMPERATURE ACCELERATION FACTOR (SEE NOTE BELOW)

T_J (°C)	Π_T	T_J (°C)	Π_T	T_J (°C)	Π_T	T_J (°C)	Π_T
25	1	51	2.80	77	6.73	103	14.32
27	1.09	53	3.01	79	7.16	105	15.12
29	1.18	55	3.23	81	7.61	110	17.25
31	1.29	57	3.47	83	8.09	120	22.24
33	1.40	59	3.72	85	8.59	125	25.13
35	1.52	61	3.99	87	9.11	135	31.81
37	1.63	63	4.27	89	9.67	145	39.80
39	1.78	65	4.56	91	10.24	150	44.35
41	1.92	67	4.88	93	10.85	155	49.29
43	2.08	69	5.21	95	11.48	165	60.44
45	2.24	71	5.56	97	12.15	175	73.44
47	2.42	73	5.93	99	12.84		
49	2.60	75	6.32	101	13.57		

Note: $\Pi_T = \exp\left[-3824\left(\frac{1}{T_J} - \frac{1}{298}\right)\right]$

where:

T_J is the worst case junction temperature (°K). T_J is estimated using the following expression:

$$T_J = T_C + \theta_{JC} P + 273$$

where:

T_C is case temperature (°C).

θ_{JC} is junction to case thermal resistance (°C)/watt) for a device soldered into a printed circuit board. If θ_{JC} is not available, use a value contained in a specification for the closest equivalent device or use the table on Page 5.1.2.7-5.

P is the worst case power realized in a system application. If the applied power is not available, use the maximum power dissipation from the device specification or from the specification for the closest equivalent device.

If T_C cannot be determined, use the following:

ENVIRO.	G_B	G_{MS}	G_F	G_M	M_P	N_{SB}	N_S	N_U	N_H	N_{UU}	A_{RW}	A_{IC}	A_{IT}	A_{IB}
T_C (°C)	35	36	45	50	40	45	45	80	45	25	60	60	60	60

ENVIRO.	A_{IA}	A_{IF}	A_{UC}	A_{UT}	A_{UB}	A_{UA}	A_{UF}	S_F	M_{FF}	M_{FA}	U_{SL}	M_L	C_L
T_C (°C)	60	60	95	95	95	95	95	45	60	50	40	60	45

TABLE 3:
Π_{SD}, DIE SCREENING CORRECTION FACTOR

Quality Level	Π_{SD}*
D	1.0
B	.94
S	.85

*QML parts will initially be exposed to Class B screening as a baseline. Further refinement of this factor will be made as data becomes available.

TABLE 4:
Π_{CD}, DIE COMPLEXITY CORRECTION FACTOR

Die Area (cm^2)					
Feature Size	.1-.2	.2-.4	.4-1.0	1.0-2.0	2.0-3.0
1.00 Micron	2.1	4.0	8.7	18	30
1.25	1.6	2.8	6.1	12	21
1.50	1.2	2.0	4.1	8.7	14
2.00	.81	1.3	2.5	4.9	8.0
2.50	.65	.95	1.7	3.3	5.2
3.00	.56	.76	1.3	2.3	3.7

TABLE 5:
Π_E, APPLICATION ENVIRONMENT FACTORS

ENVIRONMENT	Π_E	ENVIRONMENT	Π_E
G_B	.52	A_{IB}	6.8
G_{MS}	.88	A_{IA}	5.4
G_F	3.4	A_{IF}	8.1
G_M	5.7	A_{UC}	4.0
M_P	5.2	A_{UT}	5.4
N_{SB}	5.4	A_{UB}	10
N_S	5.4	A_{UA}	8.1
N_U	7.7	A_{UF}	12
N_H	8.0	S_F	1.2
N_{UU}	8.6	M_{FF}	5.3
A_{RW}	12	M_{FA}	15
A_{IC}	3.4	M_L	17
A_{IT}	4.0	C_L	300

TABLE 6:
Π_{SP}, PACKAGE SCREENING FACTOR

Quality Level	Π_{SP}*
D	10
B	1.0

*QML parts will initially be exposed to Class B screening as a baseline. Further refinement of this factor will be made as data becomes available.

TABLE 7:
Π_{PT}, PACKAGE TYPE CORRECTION FACTOR

Package Type	Π_{PT}	
	Hermetic	Nonhermetic
DIP	1.0	2.8
Pin Grid Array	2.2	4.0
Chip Carrier	4.7	6.5

TABLE 5.1.2.12-8:
λ_{EOS}, ELECTRICAL OVERSTRESS FAILURE RATE

V_{TH} (ESD Susceptibility (Volts))*	λ_{EOS}
0 - 1000	.057
1000 - 2000	.048
2000 - 4000	.040
4000 - 16000	.034
>16000	.025

*Voltage ranges which will cause the part to fail. If unknown, use 0-1000 volts.

8.0 FAULT TOLERANT RELIABILITY CONSIDERATIONS

8.1 INTRODUCTION

VHSIC and VHSIC-Like Chip designs often use system style architecture to handle a multitude of functions such as CPU, RAM, ROM and I/O. To model a system that contains a large quantity of VHSIC and VHSIC-Like chips, with a straight series reliability model, would be inaccurate if the chip design employs such fault tolerant mechanisms as redundancy and error detection and correction (EDAC).

To complete this VHSIC/VHSIC-Like reliability modelling effort, a wide variety of fault tolerant techniques used in chip designs were reviewed and general modelling techniques were derived to account for these redundancy effects. An attempt was made to account for redundancy techniques in the model by including a pi factor similar to the other factor used. This approach was abandoned however since it was determined that such a factor would be an oversimplification of the actual process. Therefore, to model these effects accurately, each individual design must be analyzed separately and modeled accordingly. The following discussion summarizes the techniques that can be used to model these effects. These techniques are based on the following, basic assumptions;

(1) The die substrate failure rate is directly proportional to the die area, (i.e., 25% of the area contributes 25% of the failure rate).

(2) All die failures are independent.

With these assumptions the modelling techniques are classified into two basic categories, redundancy and EDAC. Section 8.2 contains the redundancy models and Section 8.3 contains the EDAC model. Section 8.4 contains guidelines for the application of the models to VHSIC/VHSIC-Like designs.

8.2 THE RELIABILITY OF REDUNDANT DESIGNS

The reliability of VHSIC devices can be enhanced by the use of redundant circuit elements at critical locations within the chip. Redundancy involves the use of two or more signal paths throughout the system by the addition of parallel elements. It is noted that in general the addition of redundant circuit elements reduces the basic series reliability while at the same time increasing mission reliability.

Depending upon the specific application there are many approaches to redundancy. Redundancy is classified into two major classes; they are:

(1) Active Redundancy - External components are not required to perform the function of detection, decision and switching when an element or path within the chip fails.

(2) Standby Redundancy - External elements are required to detect, make a decision and switch to another element or path within the device as a replacement for a failed element or path.

An overview of the techniques modeled in this report is given in Figure 8-1.

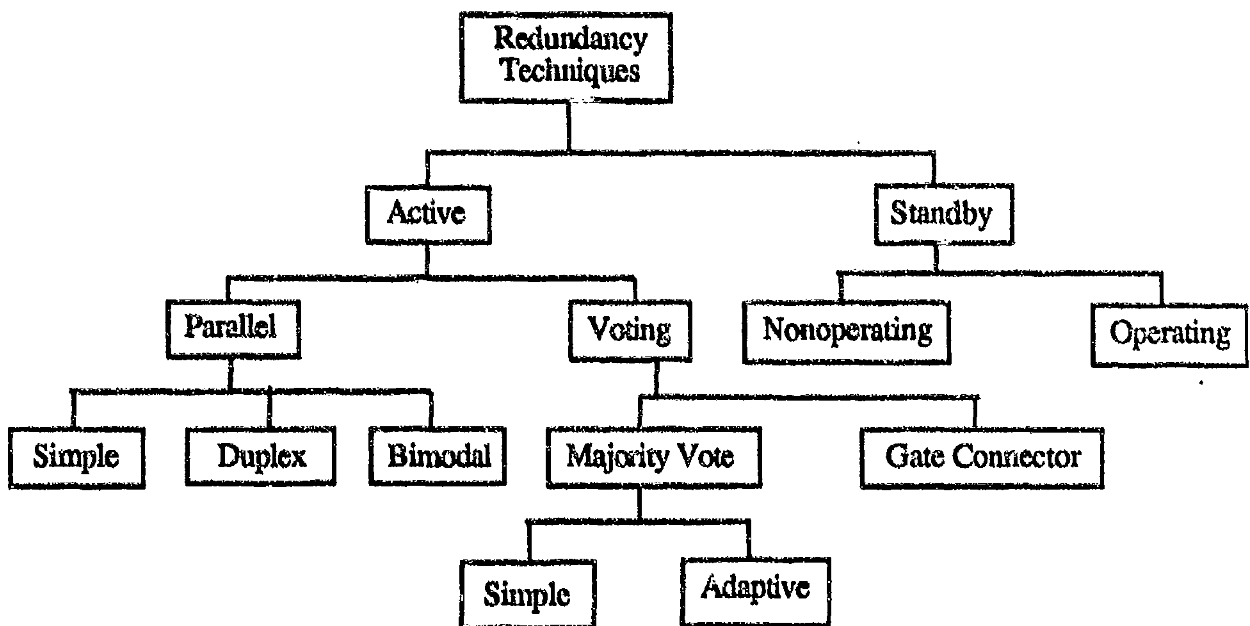


FIGURE 8-1:
REDUNDANCY TECHNIQUES

The following sections contain a short synopsis of each of the techniques mentioned in Figure 8-1. It is important to note that they use a simple probability, that is, the reliability is modeled in terms of the number of successful paths through the circuit subtracting out the successes that are counted more than once. For example, if there are two successful events that could occur (Path A and Path B) and they are independent, then the probability of successful operation is:

$$P(AUB) = P(A) + P(B) - P(A)P(B)$$

where:

P(AUB)	=	The probability of either Event A or Event B occurring
P(A)	=	The probability of Event A occurring
P(B)	=	The probability of Event B occurring

8.2.1 Simple Parallel Redundancy

Simple parallel redundancy (SPR) is one of the most widely used active redundancy techniques. If any functional element fails open then another identical path exists through the redundant elements. The concept is visualized in Figure 8-2.

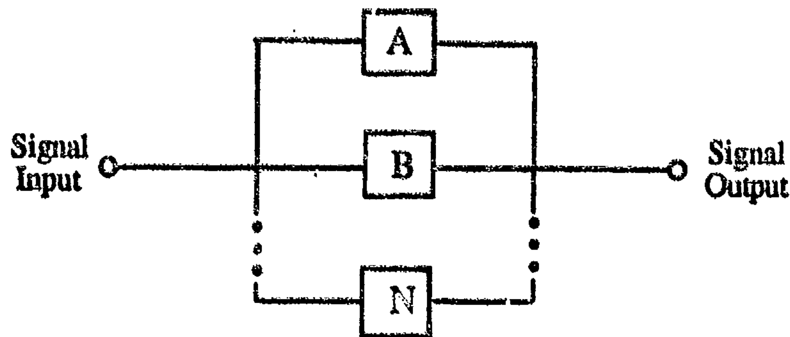


FIGURE 8-2:
SIMPLE PARALLEL REDUNDANCY

All elements are usually identical, but they may be different. The probability model for this case is:

$$R(t) = 1 - (1-e^{\lambda t})^{n}$$

where:

$R(t) \equiv$ Reliability at time t
$\lambda \equiv$ Failure rate of the corresponding chip area
$n \equiv$ Number of redundant elements

If the elements are different, then the reliability of each element must be calculated separately. The advantages of SPR are simplicity, a significant gain in reliability from nonredundant device design and its applicability to both analog and digital circuitry. The disadvantages are the issues of load sharing, problems with voltage sensitivity across redundant elements and electrical overstress propagation.

8.2.2 Duplex Parallel Redundancy

Duplex parallel redundancy (DPR) is used in redundant logic applications. It is primarily used in computer applications where redundant digital outputs are monitored by an error detection device such as a parity checker. If an error is detected the faulty output is disabled and the system function is never interrupted. Figure 8-3 is an illustration of a DPR application.

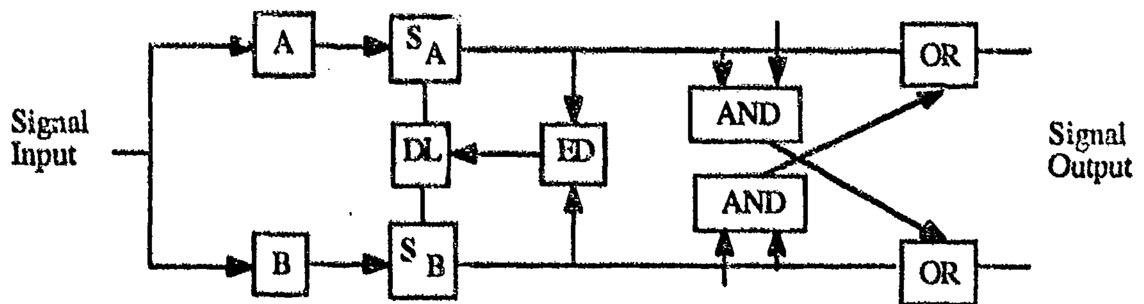


FIGURE 8-3:
DUPLEX REDUNDANCY

In Figure 8-3 Elements A and B represent redundant logic, S_A and S_B are the switches to disable the logic of A or B if they should be found faulty, ED is the error detection element and DL is the diagnostic logic element. If logic elements A and B are identical the reliability model would be as follows:

$$R(t) = P_{ED} P_{DL} (2 R_E R_S)^2 (2 R_{out} - R^2_{out})]$$

where:

$R(t)$ = Reliability at time t
P_{ED} = Probability of error detection
P_{DL} = Probability of the diagnostic logic
R_E = Reliability of the redundant logic (A, B)
R_S = Reliability of the identical switches, S_A and S_B
R_{out} = Reliability of the output circuitry
R_{out} = $P_{G01} + P_{G02} R_{GA} - P_{G01} P_{G02} R_{GA}$

where:

P_{G01} = Probability first input to OR gate gets through
P_{G02} = Probability second input to OR gate gets through
R_{GA} = Reliability of the and gate

The advantages of employing the DPR techniques are:

(1) Application to duplex, active redundant modes or separate elements.

(2) Will maintain system function up to n-1 failures.

(3) Protects against both open and short failure modes.

(4) Faulty units can be reported to the next higher level of assembly without disrupting operation.

The disadvantages of DPR are increased complexity due to additional detection and sensing circuitry, increased storage capability required for redundant data elements and additional diagnostic routines.

8.2.3 Bimodal Parallel Redundancy

Bimodel Parallel Redundancy (BPR) is an active redundancy technique that combines both series and parallel success paths. This technique prevents system level failures by protecting against shorts and opens. Direct shorts across the chip due to a single element shorting is provided by a redundant element in series. An open across the device is prevented by the parallel elements. Figure 8-4 and 8-5 contain the block diagrams for the two major types of BPR.

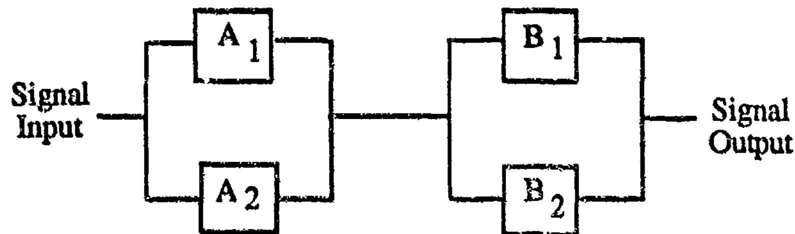


FIGURE 8-4:
BIMODAL PARALLEL/SERIES REDUNDANCY

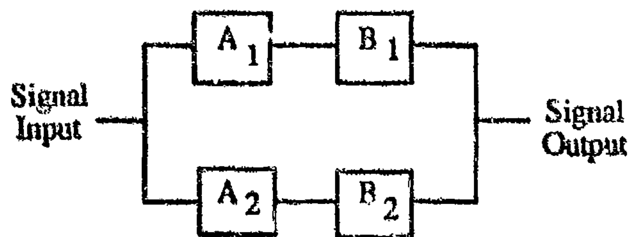


FIGURE 8-5:
BIMODAL SERIES/PARALLEL/REDUNDANCY

The parallel/series techniques is useful when the primary expected failure mode is open. The series/parallel technique is useful when the primary expected failure mode is short. The reliability calculation for the parallel/series case (assuming identical functional blocks) is:

$$R(t) = (2R_A - R_A^2)(2R_B - R_B^2)$$

where:

$R(t)$ ≡ Reliability at time t
R_A ≡ Reliability of the A Elements
R_B ≡ Reliability of the B Elements

The reliability calculation for the series/parallel case (assuming identical functional blocks) is:

$$R(t) = 2R_A R_B - (R_A R_B)^2$$

where:

$R(t)$ ≡ Reliability at time t
R_A ≡ Reliability of the A elements
R_B ≡ Reliability of the B elements

The major advantage of the BPR techniques that have been described is that it provides a significant gain in reliability at the chip level (and therefore system level) for short mission times. Another advantage is that it can provide greater protection against particular failure modes. Its major disadvantages are that it is difficult to design at the chip level and for long mission times it can actually be less reliable than a non redundant design.

8.2.4 Majority Voting Redundancy

Majority voting redundancy (MVR) can be implemented in two ways; the straight MVR technique and an enhanced adaptive majority logic technique. The idea behind the basic MVR is that decision logic can be built into the SPR model by inputting signals from the parallel elements to a voting element to compare each signal with the remaining signals. Valid decisions are made only if the number of useful elements exceeds the number of failed elements.

The adaptive majority logic technique uses the basic MVR, but utilizes a comparator and switching network to switch out or inhibit failed redundant elements. This enhancement reduces the possibility of a majority of bad elements determining the vote. Figure 8-6 and 8-7 contain the block diagrams for the two MVR techniques.

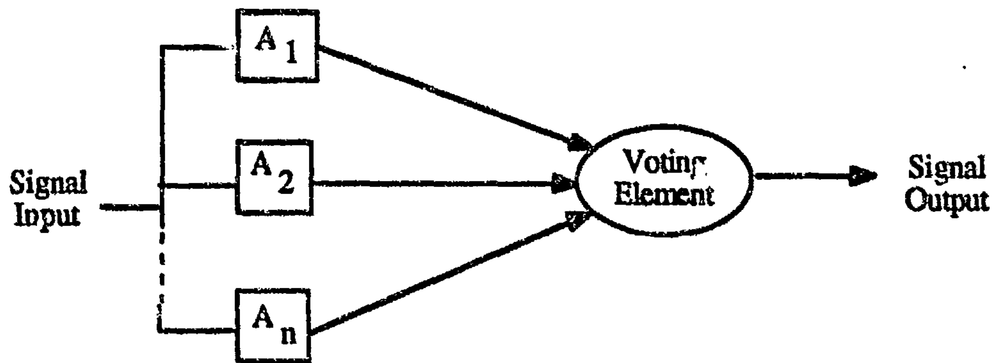


FIGURE 8-6:
MAJORITY VOTING REDUNDANCY

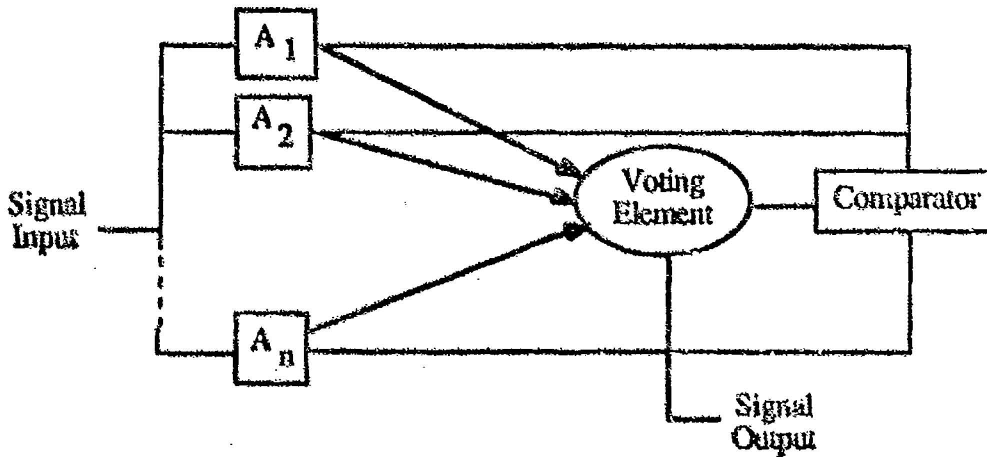


FIGURE 8-7:
MVR WITH ADAPTIVE ELEMENTS

The MVR reliability model assuming all redundant elements are identical is:

$$R(t) = \left[\sum_{i=0}^{n} \binom{2n+1}{i} (1-e^{\lambda_A t})^{i} e^{-\lambda_A t (2n+1-i)} \right] e^{-\lambda_{MVR} t}$$

where:

R(t)	≡	Reliability at time t
λ_A	≡	Failure rate of a single redundant elements
λ_{MVR}	≡	Failure rate of the voting element
n	≡	The number of redundant elements minus the minimum number of elements required

The model can be added to so that it can be applied to the adaptive MVR technique. The reliability of the comparator and sensing circuitry must be added as well. Since there are so many possible implementations of this technique the derivation of specific model is left to the user.

The advantages of using the MVR techniques are that it:

(1) Can be implemented to provide indication of faulty signals.

(2) Can provide significant gains in reliability for short missions.

The disadvantages are that to be effective it requires the voting element to have a much greater reliability than the redundant elements and that in some cases for long mission times it can produce a lower reliability.

8.2.5 Gate Connector Redundancy

Gate connector redundancy (GCR) is a voting type of redundancy similar to MVR. It is primarily used in digital circuitry where redundant elements require a vote, but not as significant a voting mechanism as those used in MVR. Outputs of the redundant elements are fed to switch-like gates which perform the voting function.

The gates contain no cells whose failure would caus redundant circuit elements to fail. Figure 8-8 contains the block diagram for the GCR technique.

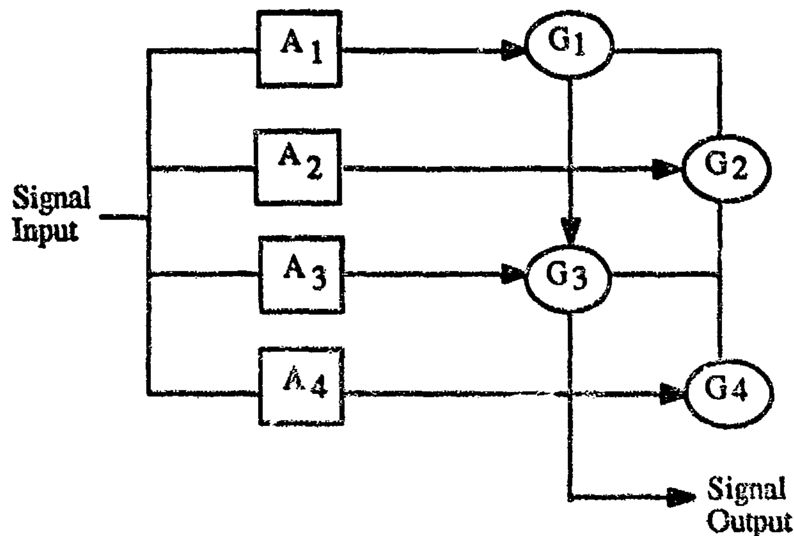


FIGURE 8-8:
GATE CONNECTOR REDUNDANCY

The reliability model for this technique is as follows:

$$R(t) = R_1R_2R_3R_4 + R_1R_2R_3Q_4 + R_1R_2Q_3R_4 + R_1Q_2R_3R_4 + Q_1R_2R_3R_4$$

where:

$R(t)$ = Reliability at time t

R_i = Reliability of path through A_i

$$R_1 = R_A R_G^2$$
$$Q_1 = 1\text{-}R_1 \quad (Q = \text{Unreliability})$$

R_2 = Reliability of path through A_2

$$R_2 = R_A R_G^3$$
$$Q_2 = 1\text{-}R_2$$

$R_3 \equiv$ Reliability of path through A_3

$$R_3 = R_A R_G$$
$$Q_3 = 1 - R_3$$

$R_4 \equiv$ Reliability of path through A_4

$$R_4 = R_A R_G^4$$
$$Q_4 = 1 - R_4$$

The gate connector technique is usually only used when the gates used to provide the voting function have extremely high reliabilities. The advantages and disadvantages of GCR are the same as MVR.

8.2.6 Standby Redundancy

Standby redundancy techniques include implementation for both operation and nonoperating modes. Standby techniques do not employ any load sharing. As soon as a faulty element is detected then another element is switched in its place. Operating standby redundancy (OSR) allows the redundant elements to remain active while nonoperating standby redundancy (NSR) allows the redundant elements to remain inactive. At the time of this writing only OSR techniques are employed as it is not possible to activate or power only portions of a monolithic substrate. OSR is illustrated in Figure 8-9.

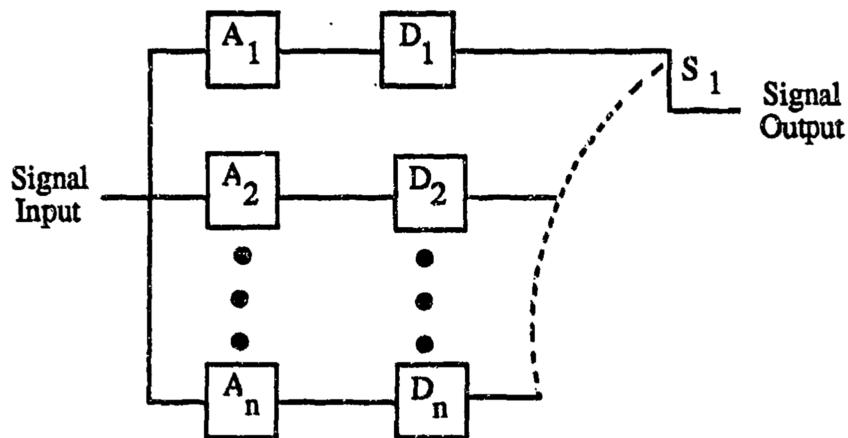


FIGURE 8-9:
OPERATING STANDBY REDUNDANCY

The A_i are the redundant elements, the D_i are the sensors which detect failures and S_1 is the switch. The reliability model for OSR is as follows:

$$R(t) = e^{-\lambda_A t}\left[\sum_{r=0}^{n-1}\frac{(\lambda_A t)^r}{r!}\right]$$

where:

$R(t)$ = Reliability at time t

λ_A = Failure rate of the active element and detector

n = Number of active elements

The advantages of OSR are that it is applicable to both analog and digital circuitry and it is effective in protecting against failure due to intermittent failure modes. Its disadvantages are the increased delay time due to sensing and switching functions, increased complexity and limitations on maximal reliability gains due to the failure modes of the sensing and switching devices.

8.3 ERROR DETECTION AND CORRECTION RELIABILITY MODELING

VHSIC and VHSIC-like devices sometimes utilize error detection and correction (EDAC) circuitry to improve the reliability of Random Access Memory (RAM). EDAC uses error correction codes (ECCs) such as the Hamming, Golay and Binary Coded Hexidecimal (BCH) to add redundancy to the stored data elements. When the data is written to a memory location a code value is calculated and stored with it. When the data is read the code is retrieved with it and the value of the code is regenerated. If the two values are not equal the entire stored word is used to generate a new (and hopefully) correct word. Though there are many types of ECCs this study considered only single error correction/double error detection (SEC/DEC) codes. This type of EDAC is implemented as shown in Figure 8-10.

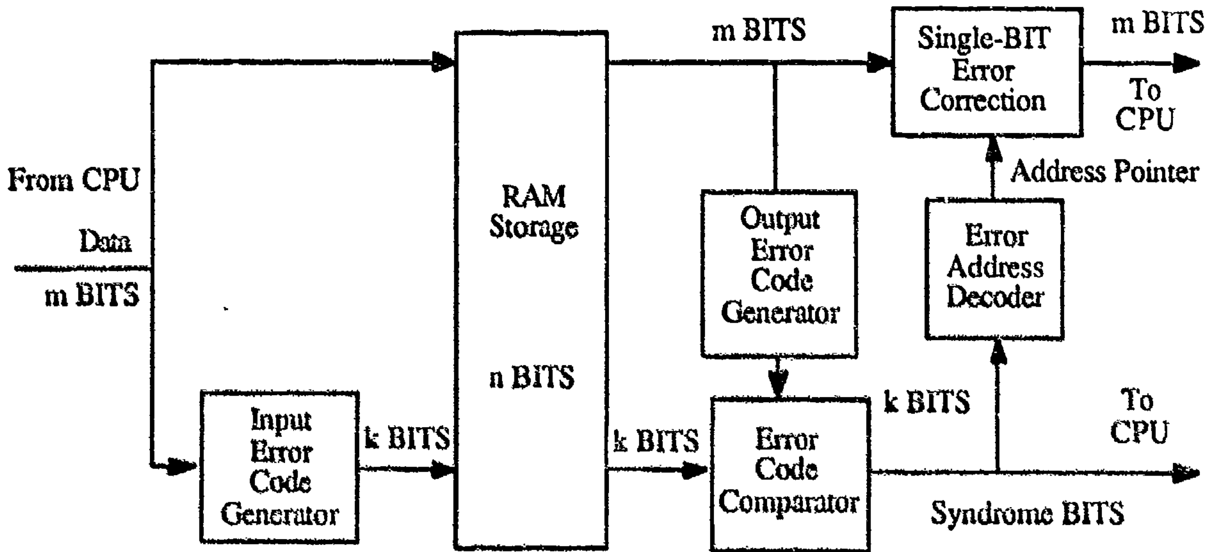


FIGURE 8-10:
EDAC BLOCK DIAGRAM

After reviewing a multitude of EDAC reliability assessment models it became apparent that as reported in "Large Scale Memory Error Detection and Correction Study," (Reference 79), the models can become quite complex. As reported in that study the Levine and Meyers EDAC model is an excellent approximation that is relatively easy to use. The model is presented as follows with one natural extension for chip level application.

$$R_{ECC}(t) \equiv (R_{RAM}{}^{m} + mR_{RAM}{}^{m-1}(1-R_{RAM}))R_{EDAC}$$

$R_{ECC}(t)$ ≡ Reliability of RAM at time t

R_{RAM} ≡ Reliability of the RAM as a function of the substrate failure rate:

$$R_{RAM} = \exp(1-\lambda_{RAM}\, t)$$

R_{EDAC} ≡ Reliability of the additional substrate used to implement EDAC:

$$R_{EDAC} = \exp(-\lambda_{EDAC}\, t)$$

m ≡ Total number of data bits, $m = n+k$, n = data, k = code

The failure rates for the RAM and EDAC functions are determined by the percentage of substrate area they occupy. If the RAM takes up 50% of the substrate then it experiences 50% of the substrate failure rate.

For multiple ECCs there are models that can be applied for which the reader is referenced to RADC-TR-87-92 for more detail.

8.4 SUBSTRATE LEVEL RELIABILITY MODELING GUIDELINES

The reliability models described in Sections 8.2 and 8.3 should be applied with guidelines put forth in this section. The system level techniques that are applied below the chip level have a major difference. Instead of summing piece-part failure rates, a percentage of the substrate failure rate is used. That percentage is equal to the percentage of substrate real-estate that each respective function occupies. Figure 8-11 illustrates this concept.

RAM 32%
CPU 30%
EDAC 8%
I/O 15%
ROM 15%

FIGURE 8-11:
SUBSTRATE REAL ESTATE PERCENTAGES

Given that the reliability of the RAM has been improved by the EDAC circuitry and that they together take 50% of the substrate area, the reliability of the RAM would be calculated using 50% of the predicted substrate failure rate.

In summary, the reliability modeling of VHSIC and VHSIC-like device follows the following sequence:

(1) Obtain all the required information on the device, its design and its application.

(2) Calculate the failure rate of the substrate and its packaging.

(3) Determine if the architecture of the device includes any redundancy or EDAC.

(4) If it does not, add the die, package, and EOS failure rates and the calculation is complete. If it does, proceed to step (5).

(5) Select the appropriate model for the type of redundancy employed.

(6) Calculate the percent of substrate that the redundancy implementation consumes.

(7) Calculate the reliability of the redundant items and the nonredundant items.

(8) Calculate the chip level reliability as follows:

$$R(t) = R_{RI}\, R_{NRI}\, R_{PKG}$$

where:

$R(t)$ = Reliability at time t
R_{RI} = Reliability of the redundant items
R_{NRI} = Reliability of the nonredundant items
R_{PKG} = Reliability of the package

The chip level reliability is viewed as illustrated in Figure 8-12.

FIGURE 8-12:
CHIP LEVEL RELIABILITY BLOCK DIAGRAM

If there is no redundancy employed 100% of the substrate failure rate is used to calculate the chip level reliability.

9.0 MODEL VALIDATION

All data collected in this (continued in Appendix D)effort was used in derivation of the model parameters. Although the majority of this data was not from 1.25 micron VHSIC technology, but rather 2.0 micron average, it was necessary to use it all to insure statistically sound parameters.

The methodology used therefore was to validate and refine the model based on the 1.0 and 1.25 micron data that was available. Table 9-1 summarizes the results of this validation effort. All data available for these devices was accelerated life test data taken at 125°C, 150°C or 200°C ambient temperatures.

Table 9-1 lists the number of actual part hours, the number of devices tested, the number of failures, the observed failure rate, the duration of the test, the predicted average (over the test duration) failure rate using the detailed model and the predicted/observed failure rate ratio. The predicted values were obtained by using a ground benign environment with a duty cycle of 1.00.

The mean and standard deviation of the log $\left(\frac{\lambda_P}{\lambda_O}\right)$ values yields -.056 and .43, respectively. Since the mean of the logged values is -.056, the actual mean of $\left(\frac{\lambda_P}{\lambda_O}\right)$ is .88, indicating that the model on the average is 12% optimistic. However, the zero failure data was not used in this analysis, which would tend to cause somewhat pessimistic observed failure rate values. The zero failure data accounted for 11.5 percent of the total observed part hours and therefore the observed failure rates should be approximately 11.5% lower than the values used in this analysis since only data with observed failures were used. It should also be noted here that a 12 percent deviation is very small compared to the natural failure rate variability.

TABLE 9-1:
MODEL VALIDATION DATA

Part Hours	# Tested	# Failed	λ Observed F/10^6 hrs.	Test Duration hrs.	λ_P	$\frac{\lambda_P}{\lambda_O}$
24,900	155	1	40	168	50.4	1.26
18,000	113	1	55	168	48.4	.88
17,000	107	2	117	168	43.9	.37
15,600	97	0	0-64	168	59.4	.37
21,100	132	0	0-47	168	37.9	.37
22,600	141	3	133	168	27.8	.21
20,100	126	1	50	168	10.0	.20
34,600	216	0	0-29	168	24.5	.20
18,000	112	1	56	168	11.0	.20
27,500	172	1	36	168	20.5	.57
32,500	203	0	31	168	21.0	.68
78,600	491	3	38	168	21.0	.55
25,100	157	0	0-40	168	13.6	.55
40,900	255	1	24	168	23.0	.96
54,000	54	4	74	1,000	81.9	1.11
2,660,000	54	11	4	168	19.8	4.95

TABLE 9-1:
MODEL VALIDATION DATA (CONT'D)

Part Hours	# Tested	# Failed	λ Observed F/10^6 hrs.	Test Duration hrs.	λ_P	$\frac{\lambda_P}{\lambda_O}$
39,312	234	3	76	168	37.4	.49
710,000	510	20	28	1,000	30.4	1.09
218,000	218	4	18	1,000	30.4	1.69
497,000	497	3	6	1,000	30.4	5.07
29,064	173	1	34	168	37.4	1.1
191,000	191	2	10	1,000	30.4	3.04
706,000	706	7	10	1,000	30.4	3.04
47,712	284	0	0-21	168	37.4	3.04
349,000	698	0	0-3	500	34.4	3.04
48,048	286	1	21	168	37.4	1.78
49,500	99	0	0-20	500	34.4	1.78
46,240	80	2	43	580	9.1	.21
182,090	315	0	0-5	580	9.1	.21
3,555	42	0	0-281	84	91.9	.21
1,232	18	0	0-812	68	98.4	.21
2,076	34	0	0-482	61	98.4	.21

The conclusion of this exercise is that the detailed model accurately predicts the failure rate as it stands and does not need to be modified.

There appears to be a relatively large variance in observed reliabilities between manufacturers but relatively little for a particular manufacturer. For example, Figures 9-1 and Figure 9-2 from (Reference 14) illustrate the variability that can be expected from a well controlled product line in which a variance of a factor of approximately two is observed. The data from the VHSIC database indicates that an order of magnitude variation is not untypical, especially between manufacturers. Several factors can account for this, particularly the fact that the actual defect densities were not known for this data, and probably varied significantly between manufacturers. This further illustrates the significance of defect density as an indicator of reliability.

Another exercise was undertaken in which it was assumed that the observed failure differences between manufacturers was attributable to differences in defect density. In this analysis a defect density was calculated for each failure rate which made the observed equal the predicted failure rate. A mean of these defect densities were then calculated for each manufacturer and ranged from .3 to 2.57 defects /cm^2. The failure rate prediction was then performed again with this "customized" defect density, and the log of the predicted/observed ratio was calculated. The standard deviation of these values was in this case .27 as opposed to .43 as in the case of the "uncustomized" defect densities.

A summary of the standard deviations of the ($\log \frac{\lambda_P}{\lambda_O}$) values for a typical regression model (Reference 78), the detailed model with D = 1, and the detailed model with customized defect density are given in Table 9-2.

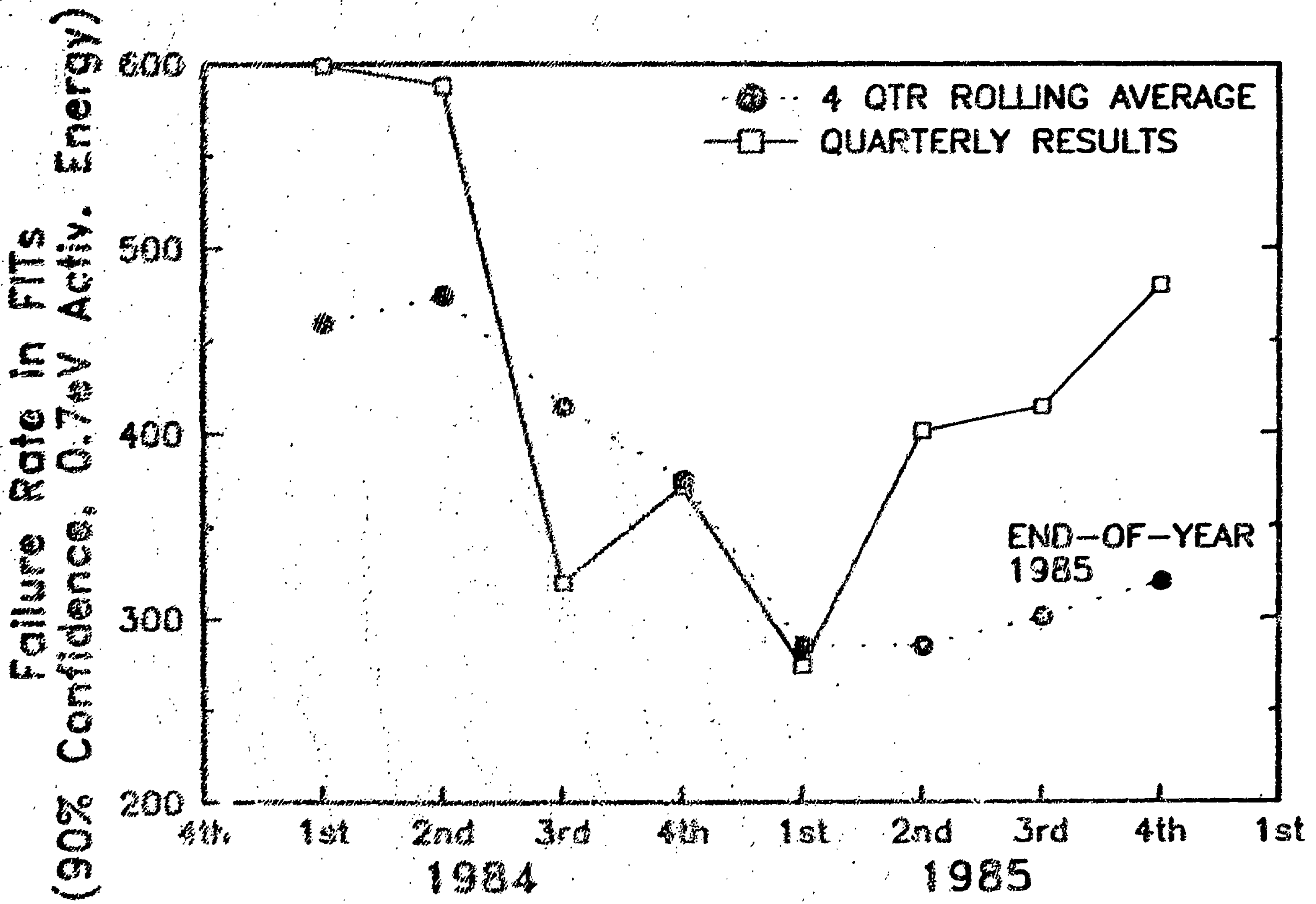


FIGURE 9-1:

MOTOROLA MICROPROCESSOR PRODUCT GROUP HIGH TEMPERATURE OPERATING LIFE 1984 - 1985 TOTALS

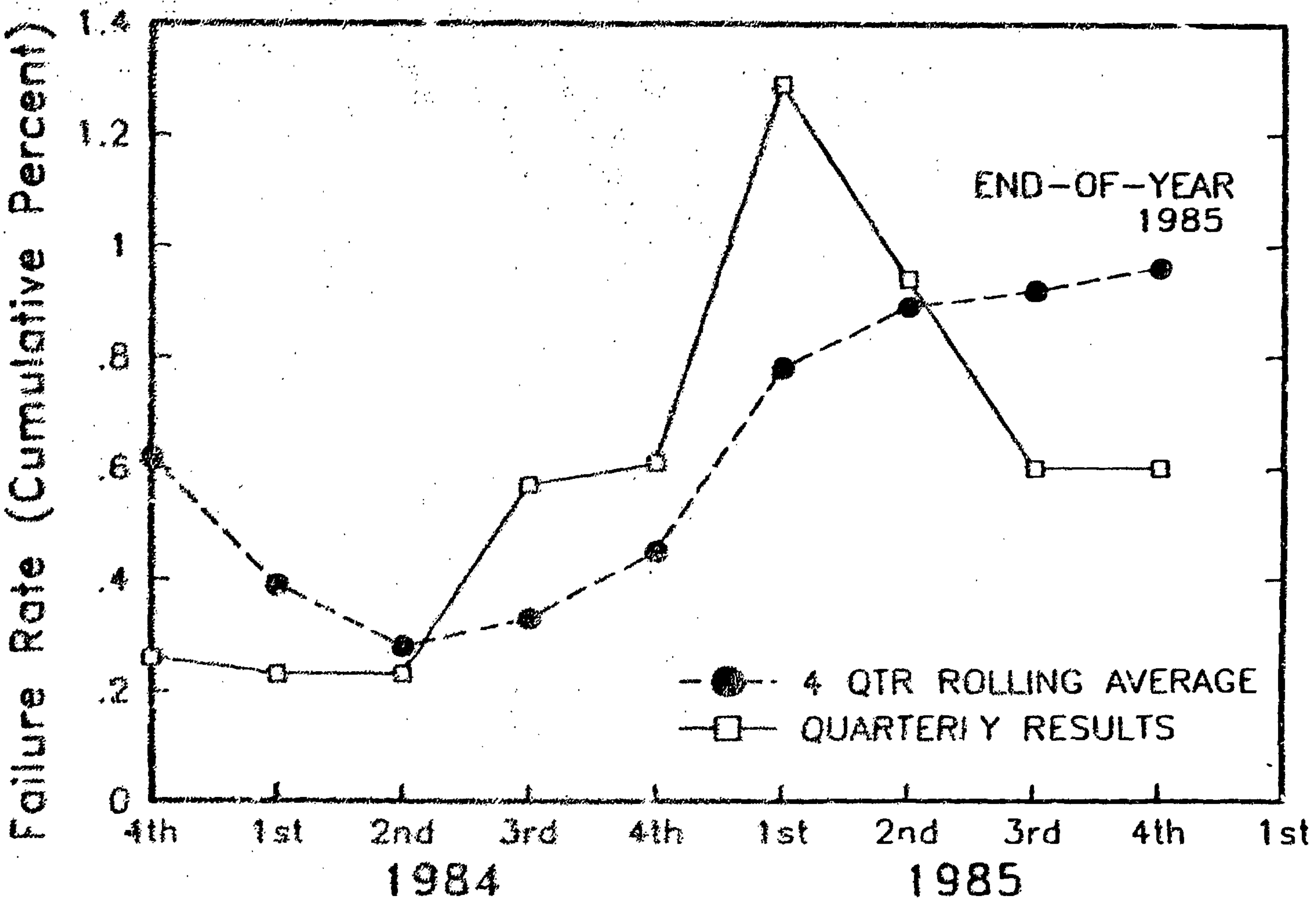


FIGURE 9-2:
MOTOROLA MICROPROCESSOR PRODUCT GROUP TEMPERATURE
CYCLE 1984 - 1985 TOTALS

TABLE 9-2:
STANDARD DEVIATION SUMMARY

Model Type	σ
Regression Model	.47
Detailed Model (D=1)	.43
Detailed Model (Custom D)	.27

An analysis like this was not performed on the short form model since it was intended only to be used for field failure rate predictions and extrapolating it to high temperature operating life conditions is questionable. It is believed however, that its precision should be comparable to a typical regression model, since these two model types have similar forms and complexities.

10.0 SAMPLE CALCULATIONS

This section of the report presents various sample calculations using the detailed model with various input variables. The failure rate graphs in this section were generated by a computer program that was written to perform predictions using the detailed model. The first illustration in each figure is the input screen in which the user specifies the input variables to be used. A description of each of these fields taken from the users manual to this program is given in Appendix C. The second illustrates the calculated failure rate as a function of time and plots these values. The dashed lines represent (from top to bottom) the highest predicted value, the mean predicted value and the lowest predicted value, all for a 20 year period. The first twelve years of operation only are plotted.

The input variables that were varied for these predictions were Die Area, Feature Size, Temperature, Duty Cycle, and Screening Duration. Table 10-1 summarizes the values of each of these variables for each example.

It can be seen in most of these failure rate plots that the failure rate is almost always continuously decreasing throughout the useful life of the device, and that it takes a very long time to reach the constant failure rate portion of the curve. This is specially true in benign, low temperature applications where many defects are not accelerated to failure in the early life of the device. Conversely, the model indicates in high temperature applications, that the failure rate is initially very high but decreases rapidly due to the fact that defects are being removed at a high rate.

It is also apparent in this model that die area and feature size heavily influence the predicted failure rate, as well as defect density.

TABLE 10-1:
EXAMPLE PREDICTIONS INPUT VARIABLES

Example Number	Die Area (cm^2)	Feature Size (Micron)	Duty Cycle	Ambient Temperature (°C)	Screening Duration (hrs.)
1	.10	1.25	.50	50	168
2	.50	1.25	.50	50	168
3	1.00	1.25	.50	50	168
4	.20	1.00	1.00	25	168
5	.20	1.00	.50	25	168
6	.20	1.00	1.00	25	168
7	.20	1.00	1.00	75	168
8	.20	1.00	1.00	125	168
9	.50	1.00	1.00	25	168
10	.50	1.00	1.00	75	168
11	.50	1.00	1.00	125	168
12	1.00	1.00	1.00	25	168
13	1.00	2.00	1.00	25	168
14	1.00	3.00	1.00	25	168
15	.50	3.00	1.00	25	168
16	.20	3.00	1.00	25	168
17	.20	3.00	1.00	25	500
18	.20	3.00	1.00	25	1000

EXAMPLE 1

VHSIC/VHSIC Like Model

Part Number | Desc | Mfr | Package | Pins
EXAMPLE1 | 1 | 2 | 3 | 22

Complexity & Unit | Dev Type | Die Area | Theta Ja

Feat Size | Defect Den | Mfg Pro | ESD | Met Type

Scrn | Duration | Temp | Pwr

Twp | Act Pwr | Curr Den | Elct Fld | Env | RHmd

Subst I | Drain I | Dty Cyc

σ Oxide | σ Metal | σ Hot Carr

Instant Time

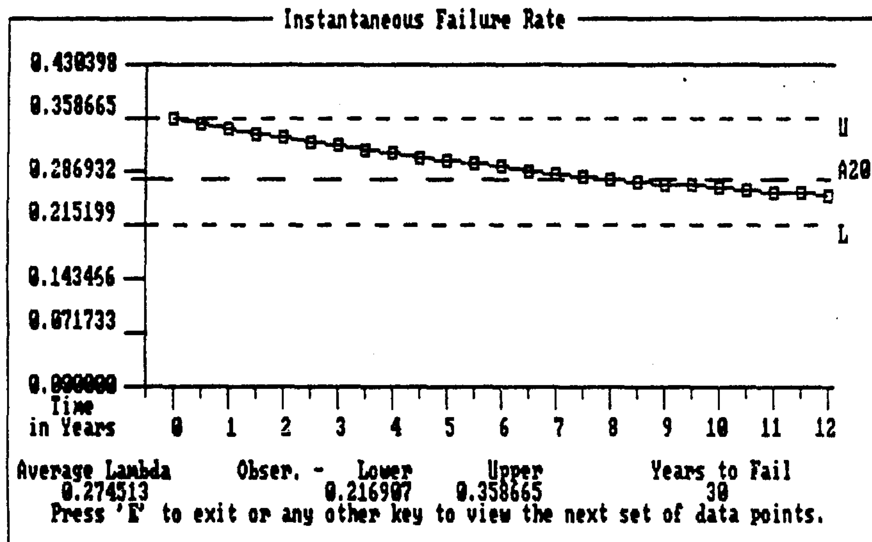
Instant Lambda

Factor	Value
Oxide	0.010785
TDDB	1.3218405347E-15
Metal	0.001522
EM	0.024540
Hot C	3.5837777503E-24
Cont	0.000260
Pack	0.113872
ESD	0.053286
Misc	0.012643
Time	0.262800
Lambda	0.216907

Average failure rate:

0.274513

Any key to view chart.



EXAMPLE 2

VHSIC/VHSIC Like Model

Part Number: EXAMPLE2 | Desc: 1 | Mfr: 2 | Package: 3 | Pins: 22

Complexity & Unit: 100 | 3 | Dev Type: 2 | Die Area: 2.5 | Theta Ja: 29

Feat Size: 1.25 | Defect Den: 9999 | Mfg Pro: 3 | ESD: 1 | Met Type: 2

Scrn: 2 | Duration: 168 | Temp: 125 | Pwr: .5

Tmp: 50 | Act Pwr: .25 | Curr Den: 1 | Elct Fld: 3 | Env: 1 | RHmd: 2.9

Subst I: 9999 | Drain I: 9999 | Dty Cyc: 2.5

σ Oxide: 1 | σ Metal: 1 | σ Hot Carr: 1

Instant Time

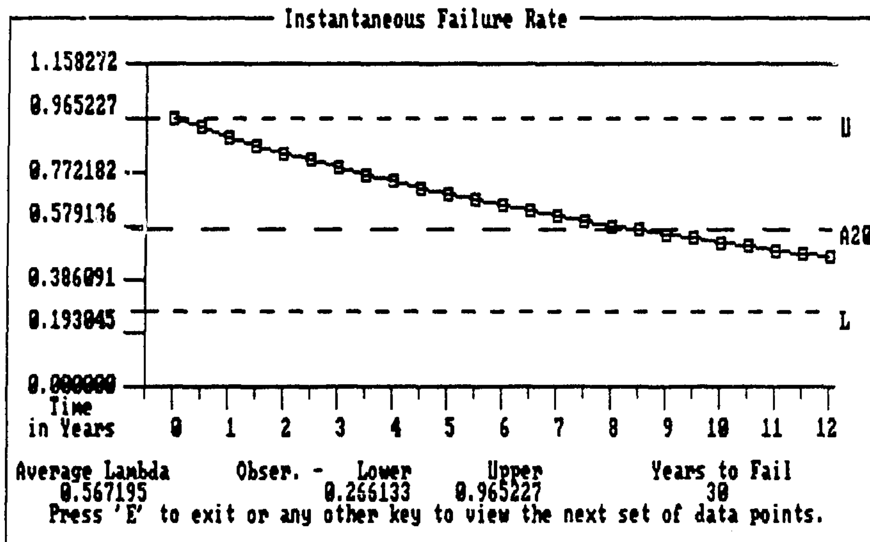
Instant Lambda

Factor	Value
Oxide	0.053924
TDDB	6.6092026733E-15
Metal	0.007610
EM	0.024540
Hot C	3.5837777503E-24
Cont	0.000260
Pack	0.113872
ESD	0.053286
Misc	0.012643
Time	0.262800
Lambda	0.266133

Average failure rate:

0.567195

Any key to view chart.



EXAMPLE 3

VHSIC/VHSIC Like Model

Part Number	Desc	Mfr	Package	Pins
EXAMPLE3	1	2	3	224

Complexity & Unit		Dev Type	Die Area	Theta Ja
1	U	2	1.	29.

Feat Size	Defect Den	Mfg Pro	ESD	Met Type
1.25	9999.	3	1	2

Scrn	Duration	Temp	Pwr
2	168	125	.5

Tmp	Act Pwr	Curr Den	Elct Fld	Env	RHmd
5	.25	1.	3.	1	3.9

Subst I	Drain I	Dty Cyc
9999.	9999.	.5

σ Oxide	σ Metal	σ Hot Carr
1.	1.	1.1

Instant Time

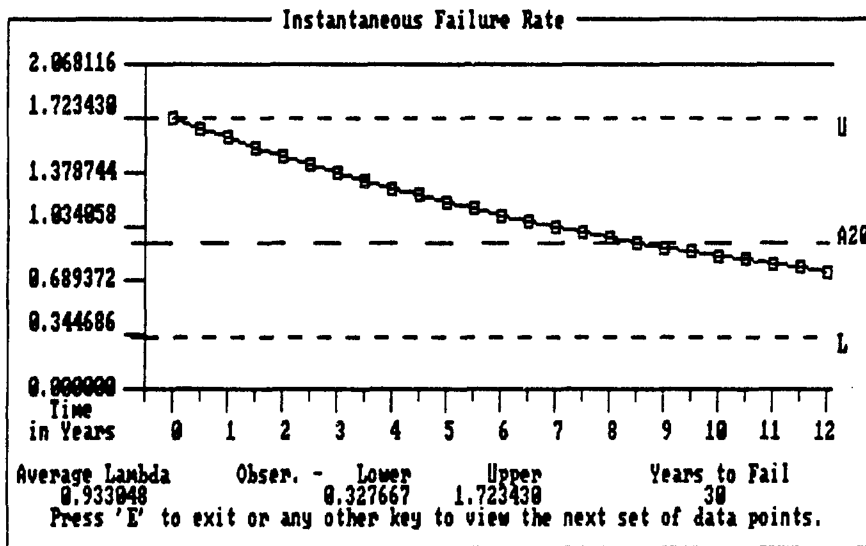
Instant Lambda

Factor	Value
Oxide	0.107847
TDDB	1.3218405347E-14
Metal	0.015220
EM	0.024540
Hot C	3.5837777503E-24
Cont	0.000260
Pack	0.113872
ESD	0.053286
Misc	0.012643
Time	0.262800
Lambda	0.327667

Average failure rate:

0.933048

Any key to view chart.



EXAMPLE 4

VHSIC/VHSIC Like Model

Part Number: EXAMPLE4 | Desc: 1 | Mfr: 2 | Package: 3 | Pins: 22

Complexity & Unit | Unit: 1 | Dev Type: 2 | Die Area | Theta Ja

Feat Size | Defect Den | Mfg Pro: 3 | ESD | Met Type: 2

Scrn: 2 | Duration | Temp: 125 | Pwr

Tmp: 25 | Act Pwr | Curr Den | Elct Fld | Env: 1 | RHmd

Subst I | Drain I | Dty Cyc

σ Oxide | σ Metal | σ Hot Carr

Instant Time

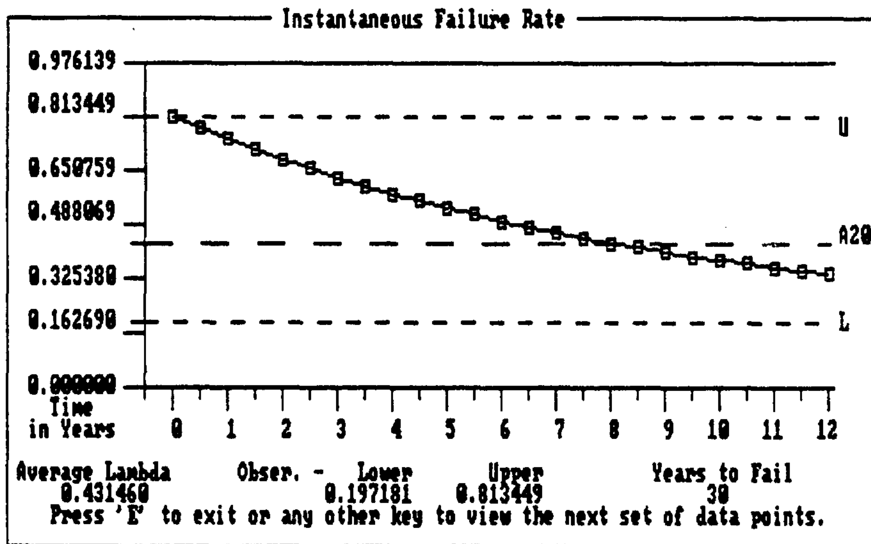
Instant Lambda

Factor	Value
Oxide	0.018971
TDDB	1.9441410446E-14
Metal	0.004718
EM	1.0851259788E-18
Hot C	8.4182293786E-21
Cont	0.000133
Pack	0.113872
ESD	0.053286
Misc	0.006201
Time	0.262800
Lambda	0.197181

Average failure rate:

0.431460

Any key to view chart.



EXAMPLE 5

VHSIC/VHSIC Like Model

Part Number EXAMPLE5 | Desc 1 | Mfr 2 | Package 3 | Pins

Complexity & Unit | Dev Type 2 | Die Area | Theta Ja

Feat Size | Defect Den | Mfg Pro 3 | ESD | Met Type 2

Scrn 2 | Duration 168 | Temp 125 | Pwr

Tmp 25 | Act Pwr | Curr Den | Elct Fld | Env 1 | RHmd

Subst I | Drain I | Dty Cyc

σ Oxide | σ Metal | σ Hot Carr

Instant Time

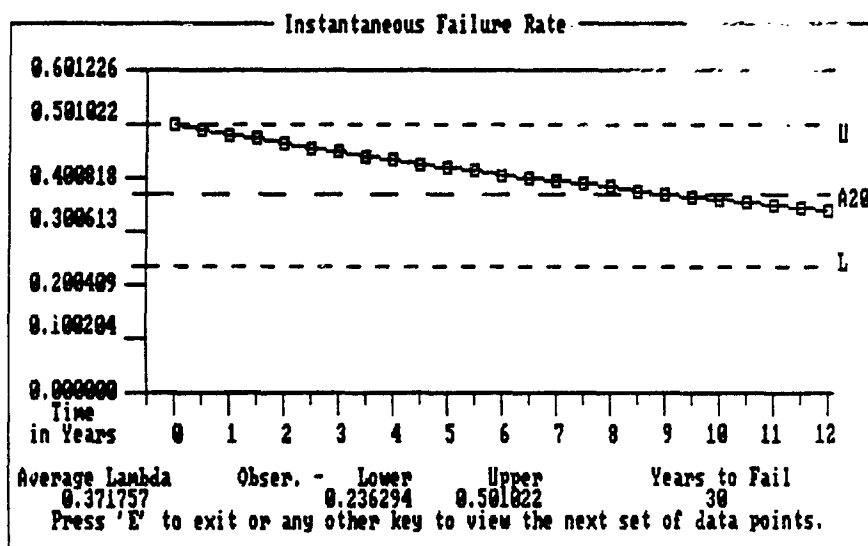
Instant Lambda

Factor	Value
Oxide	0.053956
TDDB	1.1888458255E-16
Metal	0.003584
EM	8.2267213373E-23
Hot C	3.1705479073E-23
Cont	0.000067
Pack	0.113872
ESD	0.053286
Misc	0.011529
Time	0.262800
Lambda	0.236294

Average failure rate:

0.371757

Any key to view chart.



EXAMPLE 6

VHSIC/VHSIC Like Model

Part Number | Desc | Mfr | Package | Pins

Complexity & Unit | Dev Type | Die Area | Theta Ja

Feat Size | Defect Den | Mfg Pro | ESD | Met Type

Scrn | Duration | Temp | Pwr

Tmp | Act Pwr | Curr Den | Elct Fld | Env | RHmd

Subst I | Drain I | Dty Cyc

σ Oxide | σ Metal | σ Hot Carr

Instant Time

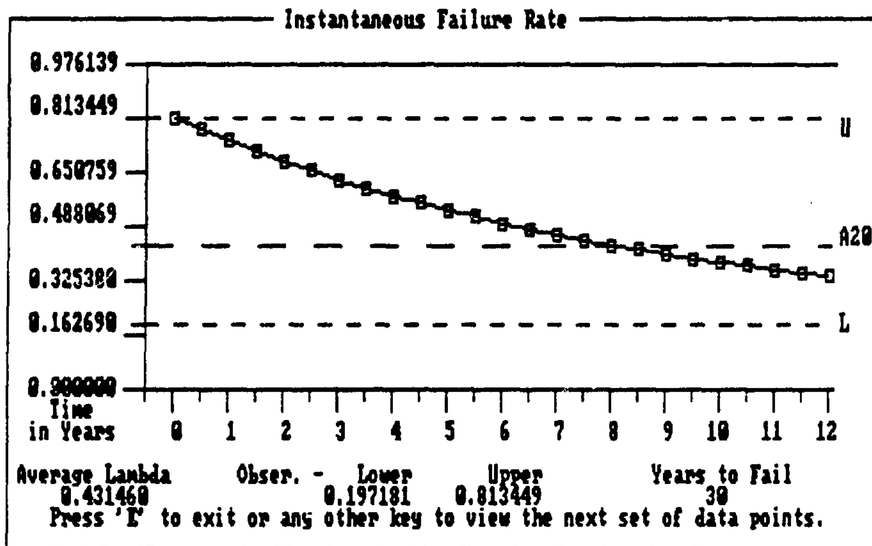
Instant Lambda

Factor	Value
Oxide	0.018971
TDDB	1.9441410446E-14
Metal	0.004718
EM	1.0851259788E-18
Hot C	8.4182293786E-21
Cont	0.000133
Pack	0.113872
ESD	0.053286
Misc	0.006201
Time	0.262800
Lambda	0.197181

Average failure rate:

0.431460

Any key to view chart.



EXAMPLE 7

VHSIC/VHSIC Like Model

Part Number EXAMPLE7 | Desc 1 | Mfr 2 | Package 3 | Pins 22

Complexity & Unit | Dev Type 2 | Die Area | Theta Ja

Feat Size | Defect Den 9999 | Mfg Pro 3 | ESD | Met Type 2

Scrn 2 | Duration 168 | Temp 125 | Pwr

Tmp 75 | Act Pwr | Curr Den | Elct Fld 3 | Env 1 | RHmd

Subst I 9999 | Drain I 9999 | Dty Cyc 1

r Oxide 1 | r Metal | r Hot Carr 1

Instant Time

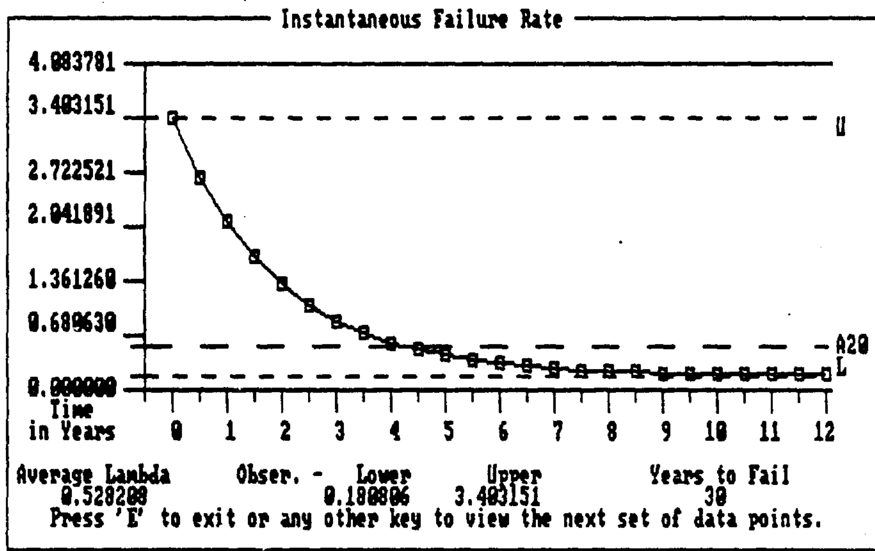
Instant Lambda

Factor	Value
Oxide	2.8230992648E-07
TDDB	1.7111589750E-09
Metal	1.6091920696E-07
EM	0.004214
Hot C	1.4914253023E-24
Cont	0.010565
Pack	0.113872
ESD	0.053286
Misc	0.000004
Time	0.262800
Lambda	0.181942

Average failure rate:

0.528208

Any key to view chart.



EXAMPLE 8

VHSIC/VHSIC Like Model

Part Number	Desc	Mfr	Package	Pins
EXAMPLE8	1	2	3	[illegible]

Complexity	& Unit	Dev Type	Die Area	Theta Ja
1	U	2	[illegible]	29.

Feat Size	Defect Den	Mfg Pro	ESD	Met Type
1.	9999.	3	[illegible]	2

Scrn	Duration	Temp	Pwr
2	168	125	[illegible]

Tmp	Act Pwr	Curr Den	Elct Fld	Env	RHmd
125	[illegible]	[illegible]	3.	1	[illegible]

Subst I	Drain I	Dty Cyc
9999.	9999.	1.

σ Oxide	σ Metal	σ Hot Carr
1.	[illegible]	1.

Instant Time [illegible]

Instant Lambda [illegible]

Factor	Value
Oxide	9.102120
TDDB	3.3744580197E-18
Metal	END OF LIFE
EM	END OF LIFE
Hot C	0.000000
Cont	1.046869
Pack	0.113872
ESD	0.053286
Misc	0.927430
Time	0.000001
Lambda	END OF LIFE

TOO FEW POINTS TO PLOT

Any key to continue.

EXAMPLE 9

VHSIC/VHSIC Like Model

Part Number EXAMPLE9 | Desc 1 | Mfr 2 | Package 3 | Pins 224

Complexity & Unit | Dev Type 2 | Die Area | Theta Ja 29

Feat Size | Defect Den 9999 | Mfg Pro 3 | ESD | Met Type 2

Scrn 2 | Duration 168 | Temp 125 | Pwr

Tmp 25 | Act Pwr | Curr Den | Elct Fld 3 | Env 1 | RHmd

Subst I 9999 | Drain I 9999 | Dty Cyc 1

σ Oxide | σ Metal | σ Hot Carr

Instant Time

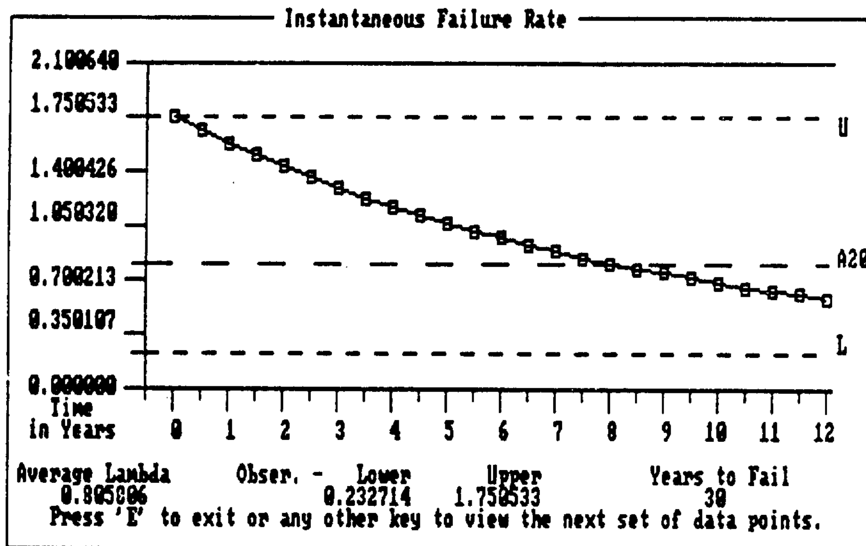
Instant Lambda

Factor	Value
Oxide	0.047426
TDDB	4.8603526115E-14
Metal	0.311795
EM	1.0851259788E-18
Hot C	8.4182293786E-21
Cont	0.000133
Pack	0.113872
ESD	0.053286
Misc	0.006201
Time	0.262800
Lambda	0.232714

Average failure rate:

0.805806

Any key to view chart.



EXAMPLE 10

VHSIC/VHSIC Like Model

Part Number · Desc · Mfr · Package · Pins

Complexity & Unit · Dev Type · Die Area · Theta Ja

Feat Size · Defect Den · Mfg Pro · ESD · Met Type

Scrn · Duration · Temp · Pwr

Tmp · Act Pwr · Curr Den · Elct Fld · Env · RHmd

Subst I · Drain I · Dty Cyc

σ Oxide · σ Metal · σ Hot Carr

Instant Time

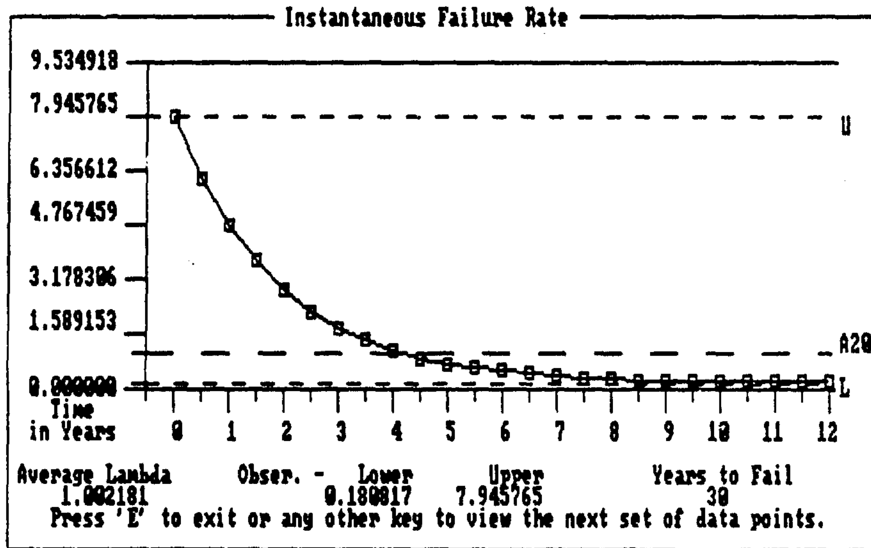
Instant Lambda

Factor	Value
Oxide	7.0577481621E-07
TDDB	4.2778974375E-09
Metal	4.0229801739E-07
EM	0.004214
Hot C	1.4914253023E-24
Cont	0.010565
Pack	0.113872
ESD	0.053286
Misc	0.000004
Time	0.262800
Lambda	0.181943

Average failure rate:

1.002181

Any key to view chart.



EXAMPLE 11

VHSIC/VHSIC Like Model

Part Number | Desc | Mfr | Package | Pins
EXAMPLE11 | 1 | 2 | 3 | 22

Complexity & Unit | Dev Type | Die Area | Theta Ja
[illegible] 1 | 2 | [illegible] | 29

Feat Size | Defect Den | Mfg Pro | ESD | Met Type
1 | 9999 | 3 | 1 | 2

Scrn | Duration | Temp | Pwr
2 | 168 | 125 | [illegible]

Tmp | Act Pwr | Curr Den | Elct Fld | Env | RHmd
125 | [illegible] | [illegible] | 3 | 1 | [illegible]

Subst I | Drain I | Dty Cyc
9999 | 9999 | 1

σ Oxide | σ Metal | σ Hot Carr
1 | [illegible] | 1

Instant Time
[illegible]

Instant Lambda
[illegible]

Factor	Value
Oxide	22.755301
TDDB	8.4361450493E-18
Metal	END OF LIFE
EM	END OF LIFE
Hot C	0.000000
Cont	1.046860
Pack	0.113872
ESD	0.053286
Misc	0.927430
Time	0.000001
Lambda	END OF LIFE

TOO FEW POINTS TO PLOT

Any key to continue.

EXAMPLE 12

VHSIC/VHSIC Like Model

Part Number: EXAMPLE12 | Desc: 1 | Mfr: 2 | Package: 3 | Pins: 22

Complexity & Unit | Dev Type: 2 | Die Area | Theta Ja

Feat Size | Defect Den: 9999 | Mfg Pro | ESD | Met Type: 2

Scrn: 2 | Duration: 168 | Temp: 125 | Pwr

Tmp: 25 | Act Pwr | Curr Den | Elct Fld | Env: 1 | RHmd

Subst I: 9999 | Drain I: 9999 | Dty Cyc

σ Oxide | σ Metal | σ Hot Carr

Instant Time

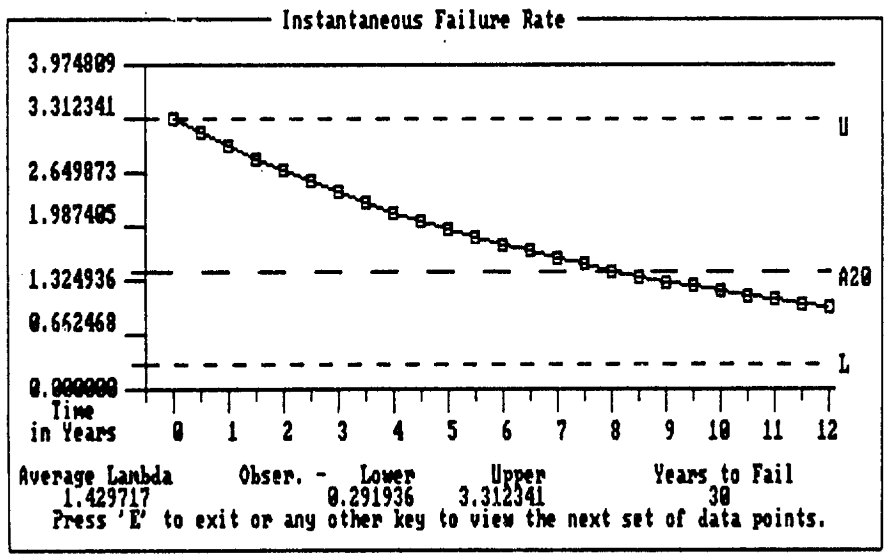
Instant Lambda

Factor	Value
Oxide	0.094853
TDDB	9.7207052230E-14
Metal	0.023591
EM	1.0851259788E-18
Hot C	8.4182293786E-21
Cont	0.000133
Pack	0.113872
ESD	0.053286
Misc	0.006201
Time	0.262800
Lambda	0.291936

Average failure rate:

1.429717

Any key to view chart.



EXAMPLE 13

VHSIC/VHSIC Like Model

Part Number	Desc	Mfr	Package	Pins
EXAMPLE13	1	2	3	22

Complexity	& Unit	Dev Type	Die Area	Theta Ja
1	1	2	1.	29.

Feat Size	Defect Den	Mfg Pro	ESD	Met Type
2.	9999.	3	1	2

Scrn	Duration	Temp	Pwr
2	168	125	.5

Tmp	Act Pwr	Curr Den	Elct Fld	Env	RHmd
25	.5	.5	3.	1	[illegible]

Subst I	Drain I	Dty Cyc
9999.	9999.	1.

σ Oxide	σ Metal	σ Hot Carr
1.	.5	1.1

Instant Time

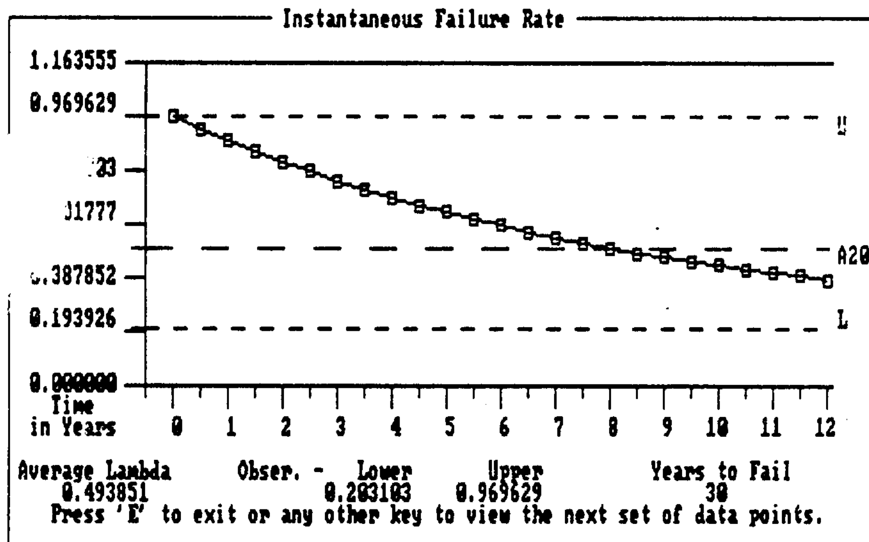
Instant Lambda

Factor	Value
Oxide	0.023713
TDDB	2.4301763057E-14
Metal	0.005898
EM	1.0851259788E-18
Hot C	8.4182293786E-21
Cont	0.000133
Pack	0.113872
ESD	0.053286
Misc	0.006201
Time	0.262800
Lambda	0.203103

Average failure rate:

0.493851

Any key to view chart.



EXAMPLE 14

VHSIC/VHSIC Like Model

Part Number	Desc	Mfr	Package	Pins
EXAMPLE14	1	2	3	[illegible]

Complexity & Unit		Dev Type	Die Area	Theta Ja
[illegible]	U	2	[illegible]	29.[illegible]

Feat Size	Defect Den	Mfg Pro	ESD	Met Type
3.[illegible]	9999.[illegible]	3	[illegible]	2

Scrn	Duration	Temp	Pwr
2	[illegible]168	125	[illegible]

Tmp	Act Pwr	Curr Den	Elct Fld	Env	RHmd
25	[illegible]	[illegible]	3.[illegible]	1	[illegible]

Subst I	Drain I	Dty Cyc
9999.[illegible]	9999.[illegible]	[illegible]

σ Oxide	σ Metal	σ Hot Carr
1.[illegible]	[illegible]	1.1[illegible]

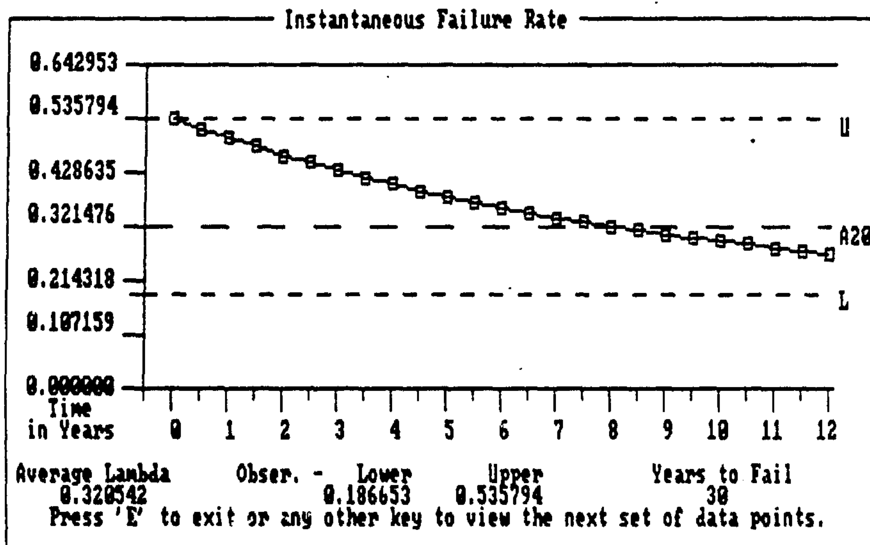
Instant Time
[illegible]

Instant Lambda
[illegible]

Factor	Value
Oxide	0.010539
TDDB	1.0800783581E-14
Metal	0.002621
EM	1.0851259788E-18
Hot C	8.4182293786E-21
Cont	0.000133
Pack	0.113872
ESD	0.053286
Misc	0.006201
Time	0.262800
Lambda	0.186653

Average failure rate:
0.320542

Any key to view chart.



EXAMPLE 15

VHSIC/VHSIC Like Model

Part Number	Desc	Mfr	Package	Pins
EXAMPLE15	1	2	3	[illegible]

Complexity & Unit		Dev Type	Die Area	Theta Ja
[illegible]	U	2	[illegible]	[illegible]

Feat Size	Defect Den	Mfg Pro	ESD	Met Type
[illegible]	[illegible]	3	[illegible]	2

Scrn	Duration	Temp	Pwr
2	[illegible]	125	[illegible]

Tmp	Act Pwr	Curr Den	Elct Fld	Env	RHmd
25	[illegible]	[illegible]	[illegible]	1	[illegible]

Subst I	Drain I	Dty Cyc
[illegible]	[illegible]	[illegible]

σ Oxide	σ Metal	σ Hot Carr
[illegible]	[illegible]	[illegible]

Instant Time

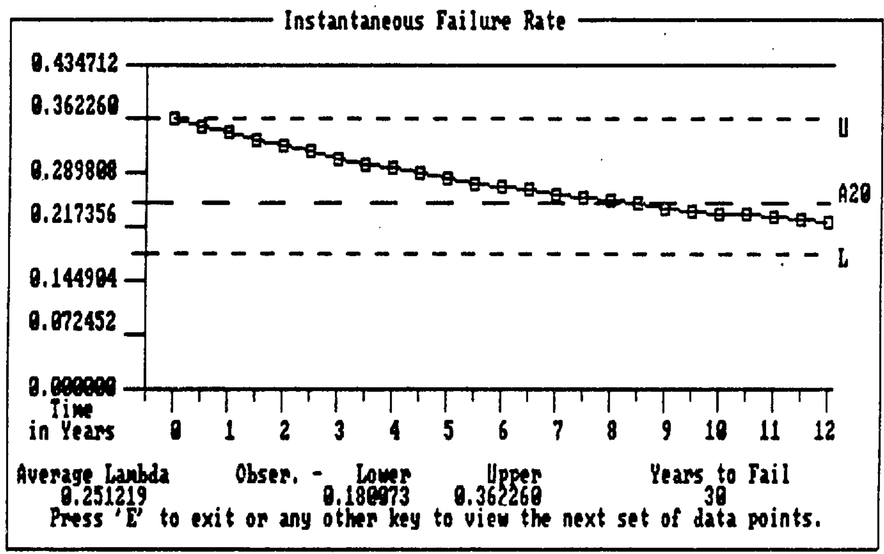
Instant Lambda

Factor	Value
Oxide	0.005270
TDDB	5.4003917905E-15
Metal	0.001311
EM	1.0851259788E-18
Hot C	8.4182293786E-21
Cont	0.000133
Pack	0.113872
ESD	0.053286
Misc	0.006201
Time	0.262800
Lambda	0.180073

Average failure rate:

0.251219

Any key to view chart.



EXAMPLE 16

VHSIC/VHSIC Like Model

Part Number: EXAMPLE16 | Desc: 1 | Mfr: 2 | Package: 3 | Pins: 224

Complexity & Unit: 1 | Dev Type: 2 | Die Area | Theta Ja: 29

Feat Size: 3 | Defect Den: 9999 | Mfg Pro: 3 | ESD: 1 | Met Type: 2

Scrn: 2 | Duration: 168 | Temp: 125 | Pwr

Tmp: 25 | Act Pwr | Curr Den | Elct Fld: 3 | Env: 1 | RHmd: 3.2

Subst I: 9999 | Drain I: 9999 | Dty Cyc: 1

σ Oxide: 1 | σ Metal | σ Hot Carr: 1

Instant Time

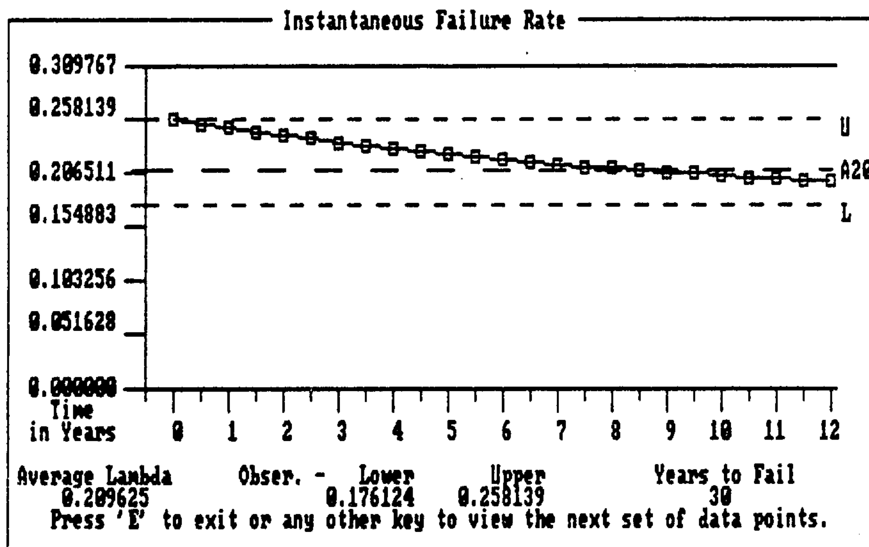
Instant Lambda

Factor	Value
Oxide	0.002108
TDDB	2.1601567162E-15
Metal	0.000524
EM	1.0851259788E-18
Hot C	8.4182293786E-21
Cont	0.000133
Pack	0.113872
ESD	0.053286
Misc	0.006201
Time	0.262800
Lambda	0.176124

Average failure rate:

0.209625

Any key to view chart.



EXAMPLE 17

VHSIC/VHSIC Like Model

Part Number	Desc	Mfr	Package	Pins
EXAMPLE17	1	2	3	[illegible]

Complexity & Unit		Dev Type	Die Area	Theta Ja
[illegible]	1	2	[illegible]	[illegible]

Feat Size	Defect Den	Mfg Pro	ESD	Met Type
[illegible]	[illegible]	3	[illegible]	2

Scrn	Duration	Temp	Pwr
2	[illegible]	125	[illegible]

Tmp	Act Pwr	Curr Den	Elct Fld	Env	RHmd
25	[illegible]	[illegible]	[illegible]	1	[illegible]

Subst I	Drain I	Dty Cyc
[illegible]	[illegible]	[illegible]

σ Oxide	σ Metal	σ Hot Carr
[illegible]	[illegible]	[illegible]

Instant Time [illegible]

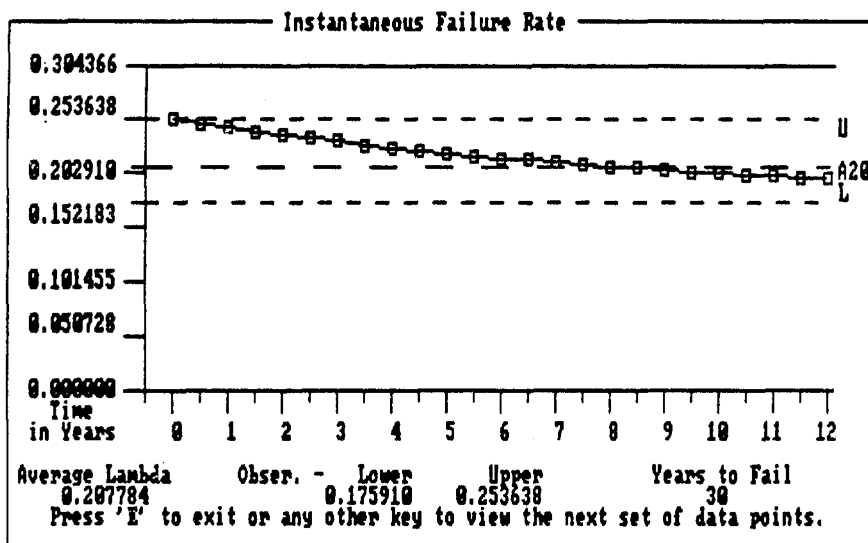
Instant Lambda [illegible]

Factor	Value
Oxide	0.001975
TDDB	2.7015794139E-15
Metal	0.000452
EM	2.5286245249E-16
Hot C	8.4726084007E-21
Cont	0.000133
Pack	0.113872
ESD	0.053286
Misc	0.006192
Time	0.262800
Lambda	0.175910

Average failure rate:

0.207784

Any key to view chart.



EXAMPLE 18

VHSIC/VHSIC Like Model

Part Number: EXAMPLE18
Desc: 1 Mfr: 2 Package: 3 Pins: 224

Complexity & Unit: 100000 U Dev Type: 2 Die Area: 0.20 Theta Ja: 20.00

Feat Size: 3.000 Defect Den: 9999.00 Mfg Pro: 0 ESD: 1000 Met Type: 2

Scrn: 2 Duration: 0.00000 Temp: 125 Pwr: 0.500

Tmp: 25 Act Pwr: 0.500 Curr Den: 0.50000 Elct Fld: 3.000 Env: 1 RHmd: 0.20

Subst I: 9999.000000 Drain I: 9999.000 Dty Cyc: 1.00

σ Oxide: 1.000 σ Metal: 0.500 σ Hot Carr: 1.00

Instant Time: 0.000000

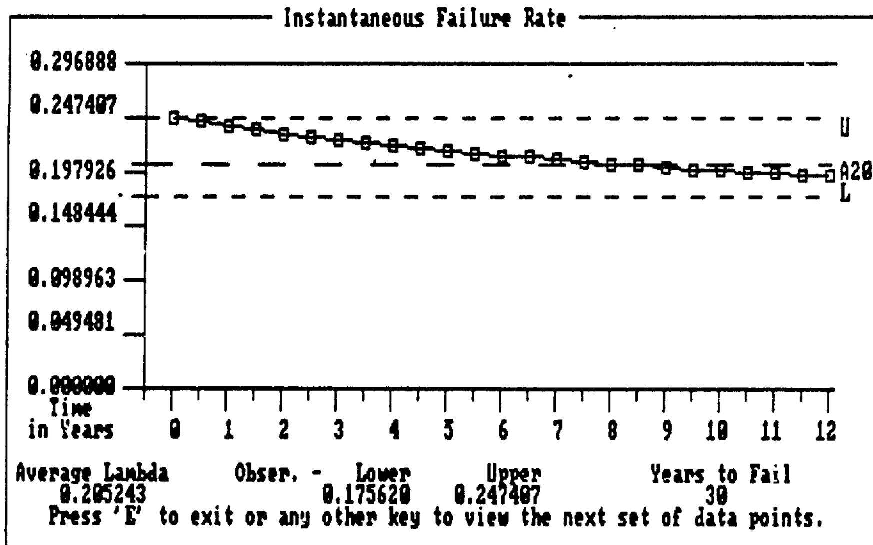
Instant Lambda: 0.000000

Factor	Value
Oxide	0.001790
TDDB	3.7296118073E-15
Metal	0.000362
EM	5.4890132761E-14
Hot C	8.5550729288E-21
Cont	0.000133
Pack	0.113872
ESD	0.053286
Misc	0.006177
Time	0.262800
Lambda	0.175620

Average failure rate:

0.205243

Any key to view chart.



11.0 MODIFICATIONS TO THE MODEL

The detailed model contained in this report is an industry wide representation of state-of-the-art VLSI/VHSIC CMOS reliability. It is recognized, however, that the best reliability predictions are accomplished based on empirical reliability data from a specific fabrication process. This empirical data is ideally field failure rate experience but can also be life test results.

As mentioned in the presentation of the detailed model, there is a correction factor π_C, which can be used to modify the model as more empirical data does become available. At the writing of this report, π_C is one (1) by definition since all data available was used in the derivation of the model and therefore on average, the observed data equals the predicted data.

The π_C factor can therefore be used for the following purposes:

(1) To modify the model as VHSIC field experience data becomes available.

(2) To modify the model for a particular fabrication process based on the availability of high quality life tests.

The second purpose above should only be used in the absence of defect density data when the default value $(X_0/X_S)^2$ is used. Additionally, either of these methods should only be used when there is statistically significant amounts of high quality data available.

The method of calculating π_C is a straightforward geometric mean of observed/predicted ratios:

$$\pi_C = \left[\prod_{i=1}^{n} \left(\frac{\lambda_O}{\lambda_P} \right) \right]^{\frac{1}{n}}$$

where: λ_O = observed failure rate

λ_P = predicted failure rate

n = number of failure rate observances

The predicted failure rate should be an average value over the time interval the observed data was taken. All other inputs should be as close to the actual values of the test as possible.

A manufacturer should also be given the opportunity to adjust the failure rates for the individual failure mechanisms in the event adequate data on specific failure mechanisms exists. This should be done only if there is a large quantity of failures which have been failure analyzed to determine the cause of failure. If this option is chosen, all failures must be accounted for and categorized into one of the mechanisms in the present model. To accomplish this, the methodology described previously in this report for modeling the early life oxide, metal, contamination, and miscellaneous failure mechanisms should be used.

12.0 CONCLUSIONS AND RECOMMENDATIONS

12.1 CONCLUSIONS

A reliability prediction model has been developed for CMOS VHSIC/VHSIC-Like devices from analysis and failure rate modeling of specific failure mechanisms. To quantify the failure rates of each of these mechanisms, a database was built which contains life test and environmental test results. Since this database was built from many manufacturers data, the failure rate predictions are industry wide representative values, and will vary from manufacturer to manufacturer. This effort concluded that the best way to account for these differences is to use actual defect densities. It is believed that the use of actual defect densities, if properly measured, will result in predicted reliability values which are more precise and accurate than conventional regression type prediction models.

Derived from the detailed model, a simpler "short form" model was developed with the understanding that systems engineers often need a quick reliability prediction tool with easily accessible input parameters.

This effort was the first in support of the MIL-HDBK-217 VLSI integrated circuit reliability prediction models that deviated from the traditional statistical analysis of field data. A combination of physics of failure information, life test results, screening results, and test structure data was used to achieve the study objectives. These objectives were not only to develop a reliability model for VHSIC/VHSIC-Like CMOS devices, but also to develop a methodology that, if successful, can be effectively used in a timely manner to develop reliability prediction models for emerging microcircuit technologies.

The authors believe that the detailed model presented in this report is generally more accurate and more sensitive to the fabrication and stress variables that truly effect device reliability. The tradeoff for this improvement is the complexity of the failure rate equations themselves, which if done by hand can be very time consuming. For this reason, it is desirable to computerize the prediction model, thus avoiding tedious calculations. The short for model developed, although easier to use, is expected to yield less precise predictions. Although less accurate than the detailed model, data has been presented indicating that the short form model precision is approximately equivalent to traditional regression analysis models.

12.2 RECOMMENDATIONS

IITRI/Honeywell recommends that the model contained herein (the detailed version, short form, or both) be incorporated into MIL-HDBK-217. The authors believe that this model currently represents the best available general purpose, small feature size CMOS device reliability prediction methodology. It is also recommended that users collect the data necessary for use of the detailed model, since it is more accurate than the short form model. Also, by exercising the detailed model with actual data, feedback can be obtained to determine if this modeling approach can be accurately extended to other technologies, and for future device types.

It is also recommended that more attention be given to collecting accurate field failure rate information for these device types as part of a government sponsored program. This data should then be submitted to a central repository of data such as the Reliability Analysis Center, so that it would be available for MIL-HDBK-217 model development efforts.

There are also many logical follow on studies to this effect which would enhance the knowledge base of VLSI/VHSIC reliability characterization. The most obvious possibly is to collect, when available, field failure rate and cause data and refine the model accordingly. In addition to field reliability data, life test and screening data should continue to be collected and analyzed so that a comprehensive database can be built.

Another very useful effort would be the extension of the methodology developed herein to bipolar VHSIC and VLSI technologies since much of the modeling done in this model could be applied to bipolar devices.

One goal of this effort was to relate failure rate prediction to efforts such as the Generic Qualification Program. Although a certain degree of success was attained toward this goal, it was ultimately concluded that there is currently a lack of standardization throughout the industry in quantifiable parameters that could be used in a reliability model. Since there are various standardization efforts underway in this area, the results of these efforts should be investigated for use as reliability indicators. Furthermore, a very useful related effort would be to define standard methodologies for the quantification of reliability characteristics.

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APPENDIX A:

SURVEY LETTER AND FORM

R

COMMITMENT TO EXCELLENCE

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Rome, New York 13440
315/336-2359

April 16, 1987

Mr. Jeff Katz
Director of Marketing ASIC Products
Intel Corporation
3065 Bowers Avenue
Mail Stop: SCI-5
Santa Cara, CA 95051

Dear Mr. Katz:

IIT Research Institute (IITRI) has recently initiated a study under contract to Rome Air Development Center (RADC Contract Number F30602-86-C-0261) to develop VHSIC and VHSIC-like CMOS reliability prediction models. Since meaningful amount., of empirical field reliability data are not expected to be available for use in model development, these prediction methodologies will be based primarily on information available during circuit fabrication such as test structures, yield, and screening information.

The intent of this study is to correlate this information with field reliability performance for each failure mechanism of interest and to combine these mechanisms into a useable prediction model form, ultimately for inclusion in MIL-HDBK-217, "Reliability Prediction of Electronic Equipment".

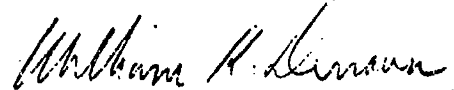
To achieve the goals of this program and to develop prediction models valuable to users, IITRI needs information on a wide variety of part types and fabrication lines. We are currently seeking data and information from organizations involved in VHSIC/VHSIC-like fabrication in the following areas; field failure rates, life test results, screening data, yield data, and test structures data. Any information your organization can provide in these areas will greatly assist us in achieving our goals.

Any information submitted to IITRI for use in this effort will be kept strictly proprietary, without traceability to data submittors.

We feel it will be very important to the electronics industry to have accurate reliability prediction models for VLSI and VHSIC devices, and that we can provide good models if cooperation is obtained from the semiconductor industry. Please fill out the attached survey form and send back to IITRI, at which time one of our representatives will call to further pursue these matters.

If there are any questions, please call Alex Recchio at (315) 336-2359. IITRI very much appreciates your cooperation in completing the enclosed survey and looks forward to your participation in this effort.

Sincerely,



William K. Denson
Project Engineer

Alex Recchio
Senior Data Specialist

WKD/AJR:jev

Attachment

VLSI/VHSIC RELIABILITY SURVEY

Name: ______________________________

Title: ______________________________

Organization: ______________________________

Division: ______________________________

Address: ______________________________

____

Phone Number: ______________________________

(1) Does your organization manufacture or use MOS VLSI or VHSIC circuits?

____

If so, please outline their characteristics

- Device type (Memory, Microprocessor, etc.)

  ____

- Feature size (Gate Length, Metal Width)

  ____

- Complexity (Approx. Number of Gates, Transistors)

  ____

- Packaging (Type, Number of Pins)

  ____

(2) Please check below the type(s) of data that your organization has on the above device(s):

_____ Field Failure Rates
_____ Life Test Results
_____ Screening Data (of any Type)
_____ Failure Analysis Data

If Failure Analysis Data is available, which failure mechanisms/modes are observed (along with relative percentages of occurrence)?

		Percentage
____	Electromigration	______
____	Dielectric Breakdown	______
____	Soft Errors	______
____	Parametric Drift	______
____	Hot Electrons	______
____	Latch Up	______
____	Electrical Overstress	______
____	Package Related	______

_____ Quality control monitor data (test structures, reliability evaluation monitors, etc.)

If yes, which types are available?

____

____

____

(3) Can the above data be made available to IITRI for this study?

____

(4) Could you please provide point-of-contact (if other than addressee)?

Name: ______________________________

Title: ______________________________

Phone: ______________________________

(5) Remarks:

____

____

____

____

APPENDIX B:

OXIDE AND METAL DEFECT DENSITY CALCULATIONS

As an option to using $(X_o/X_s)^2$ in the metal and oxide factors, defect density factors can be used as follows:

$$F_{met} = \left(\frac{D_{o\ met}}{D_{r\ met}}\right)$$

and

$$F_{ox} = \left(\frac{D_{o\ ox}}{D_{r\ ox}}\right)$$

where

$D_{o\ met}$ = The defect density measured with an interdigitated meander test structure as described in the metal defect monitor test method below.

$D_{r\ met}$ = $\frac{(-\ln 0.90)}{A\ f_{met}}$

F_{met} = 0.15, the fraction of actual minimum-pitch metal length out of the total minimum-pitch metal length possible on the chip.

$D_{o\ ox}$ = The defect density measured with a capacitor test structure as described in the gate oxide monitor test method below.

$D_{r\ ox}$ = $\frac{(-\ln 0.90)}{A\ f_{ox}}$

F_{ox} = 0.01, the fraction of actual gate oxide area to total area of the chip.

Metal Defect Monitor Test Method

It is assumed that the defects are random. First metal layer defect density, $D_{o\ met}$, is established with an interdigitated meander, shown in Figure 1. The meander is laid out with the minimum first metal line width and space dimensions allowed for the device in question. The minimum serpentine length should be:

$$L_{met} = \frac{f_{met} A_{max}}{2 P_{met}}$$

where A_{max} is the die area of the maximum size device to be manufactured in the same technology, and P_{met} is the minimum pitch allowed by the layout rules for the first metal layer. Data from a minimum of 50 randomly selected test structure sizes must be used.

Three types of test measurements are performed on these structures. First, for the contact test, two-probe resistance measurements are made between nodes 1 and 8, 2, 3, 4, 5, 6 and 7. Second, four-probe resistance measurements are made on the serpentine with current forced at nodes 2 and 7 in Figure 1, and voltage sensed at nodes 3 and 6. Third, for the bridging test, leakage between adjacent metal lines is measured by forcing a voltage at the node formed by connecting together nodes 1, 4, 5, and 8 in Figure 1 and measuring a leakage with a current meter connected between ground and the node formed by connecting together nodes 2, 3, 6 and 7 in Figure 1. The pass range for the two-probe resistance measurements is between 0.5x nominal calculated resistance and 1.5x nominal calculated resistance. The pass range for the serpentine measurement is between 0.5x nominal calculated serpentine resistance and 1.5x nominal resistance. The pass range for the leakage resistance between adjacent metal lines is between 10 times the nominal resistance of the serpentine and 1.0E18 ohms.

Yields are calculated in the following way. For contact yield,

$$Y_c = \frac{N_{cp}}{N_{cp} + N_{cf}}$$

where N_{cp} is the number of sites that pass the contact test, and N_{cf} is the number of sites that fail the contact test. If Y_c is less than 0.5 (50%) then the test must be performed again. For serpentine and bridging yield,

$$Y_{sb} = \frac{N_{sb\,p}}{N_{sb\,p} + N_{sb\,f}}$$

where of the sites that pass the contact test, N_{sbp} is the number of sites that pass the serpentine and the bridging tests, and N_{sbf} is the number of sites that fail either the serpentine or the bridging tests.

The defect density is calculated from the yield with the following equation:

$$D_{o\,met} = \frac{(-\ln Y_{sb})}{f_{met}\,A_{max}}$$

<u>Gate Oxide Defect Monitor Test Method</u>

It is assumed that the defects are random. Gate oxide defect density, $D_{o\,ox}$, is established with a capacitor test structure, shown in Figure 2. The gate oxide area should be:

$$A_{ox} = f_{ox}\,A_{max}$$

where A_{max} is the die area of the maximum size device to be manufactured in the same technology as the device in question. Data from a minimum of 50 randomly selected test structure sites must be used.

Two types of test measurements are performed on these structures. First, for the contact test, two-probe resistance measurements are made between nodes 1, 2, 3, 4, 5 and 6. Second, for the leakage test, leakage between gate and the n- or p- channel silicon is measured by forcing a voltage (V_{DD}) at the node formed by connecting together nodes 1, 2, 3 and 4 in Figure 2 and measuring a leakage with a current meter connected between ground and the node formed by connecting together nodes 5 and 6 in Figure 2. The pass range for the two-probe resistance measurements is between 0.5 X nominal calculated resistance and 1.5 x nominal calculated resistance. The pass range for the leakage resistance the gate and silicon is between 1.0E-10 ohms and 1.0E18 ohms.

Yields are calculated in the following way. For contact yield,

$$Y_C = \frac{N_{CP}}{N_{CP} + N_{CF}}$$

where N_{CP} is the number of sites that pass the contact test, and N_{CF} is the number of sites that fail the contact test. If Y_c is less than 0.5 (50%) then the test must be performed again. For oxide leakage yield,

$$Y_{Cap} = \frac{N_{Cap\ P}}{N_{Cap\ P} + N_{Cap\ F}}$$

where of the sites that pass the contact test, $N_{Cap\ P}$ is the number of sites that pass the leakage test, and $N_{Cap\ F}$ is the number of sites that fail the leakage tests.

The defect density is calculated from the yield with the following equation:

$$D_{0ox} = \frac{(-\ln Y_{Cap})}{f_{ox} A_{max}}$$

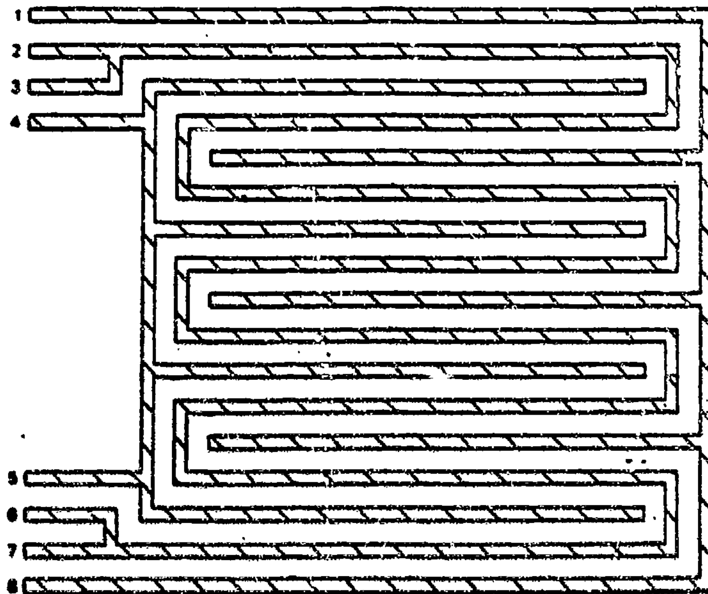


FIGURE 1:
INTERDIGITATED MEANDER

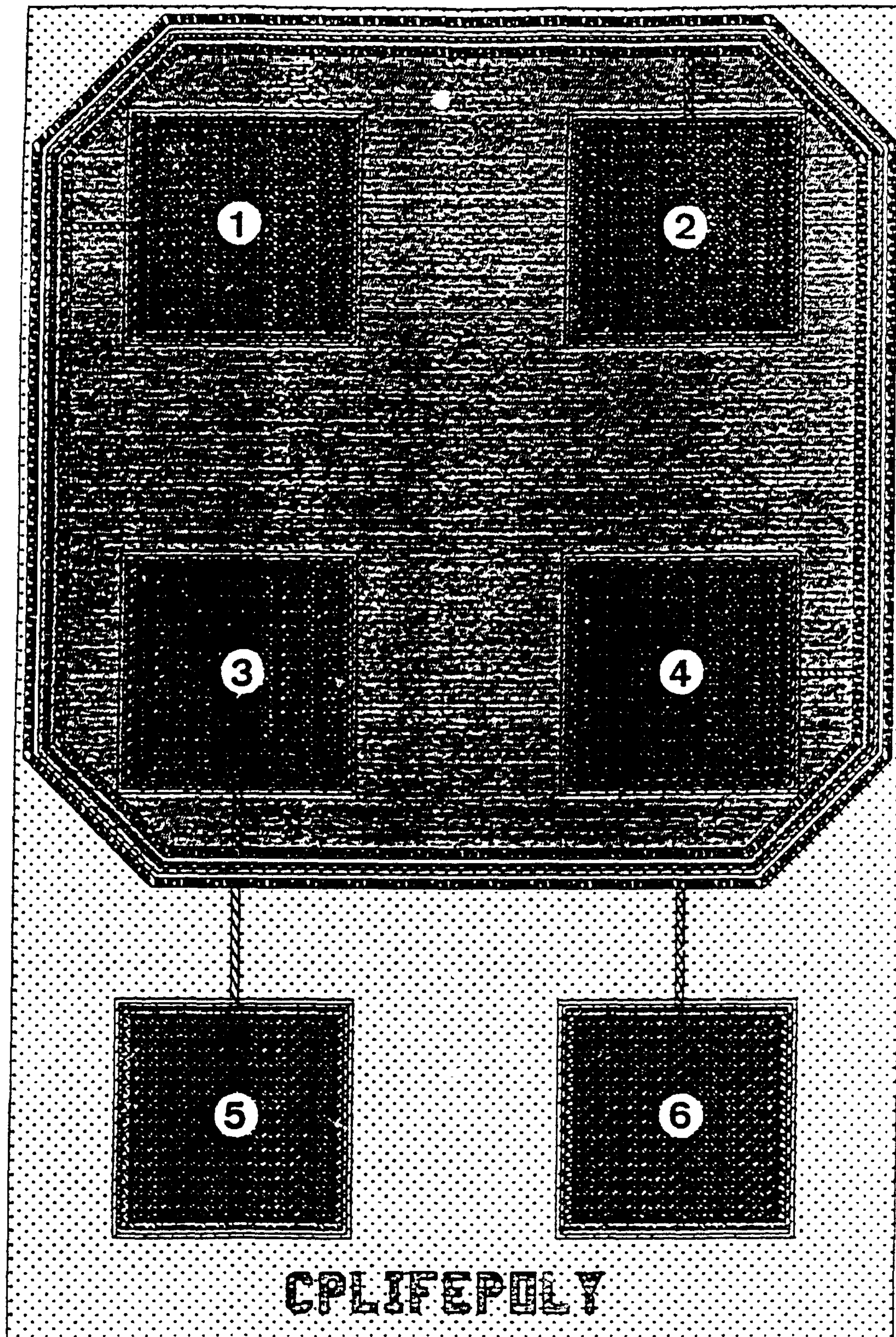


FIGURE 2:
CAPACITOR TEST STRUCTURE

APPENDIX C:
FIELD DESCRIPTIONS

- PART NUMBER is the part identification number of the current device. This field is not required for calculation of the part. This field is required for storage of parameters. There are no constraints on the contents of this field.

- PART DESCRIPTION is the generic part type of the current device. This field is not required for calculation of the part or storage of parameters. The contents of this field is selected from a look up list, to which new entries may be added.

- MANUFACTURER is the manufacturer of the current device. This field is not required for calculation of the part or storage of parameters. The contents of this field is selected from a look up list, to which new entries may be added.

- PACKAGE TYPE is the type of package enclosure of the current device. This field is required for calculation of the part and storage of parameters. The contents of this field is selected from the look up list, which may not be added to.

- NUMBER OF PINS is the total number of pins (including pins not internally connected) on the current device. This field is required for calculation of the part and storage of parameters. The contents of this field is entered directly and must be greater then zero.

- COMPLEXITY is the gate, bit or transistor count of the current device. The UNITS are "G" for gate, "B" for bit, and "T" for transistor. This field is not required for calculation of the part or storage of parameters. The contents of this field is entered directly.

- DEVICE TYPE is the basic family to which the current device belongs. This field is required for calculation of the part and storage of parameters. The contents of this field is selected from a look up list, which may not be added to.

- DIE AREA is the size, in square centimeters, of the die of the current device. This field is required for calculations of the part and storage of parameters. The contents of this field is entered directly. If the DIE AREA is unknown, use 99.00.

- THERMAL COEFFICIENT is the Junction to Ambient thermal resistance of the device. This field is required for calculation of the part and storage of parameters. The contents of this field is entered directly.

- FEATURE SIZE is the size, in microns, of the smallest feature of the device. For example, VHSIC Phase 1 is 1.25 microns. This field is required for calculation of the part and storage of parameters. The contents of this field is entered directly. If the FEATURE SIZE is unknown, use 99.000.

- DEFECT DENSITY is the number of critical defects per square centimeter. This field is required for calculation of the part and storage of parameters. The contents of this field is entered directly. If the actual DEFECT DENSITY for the feature size is unknown, use 9999.00.

- MANUFACTURING PROCESS identifies the device as being manufacturered in accordance with the Generic Qualification Program (QML) or listed on the M-38510 QPL. This field is required for calculation of the part and storage of parameters. The contents of this field is selected from a look up list, which may not be added to.

- ESD SUSCEPTIBILITY LEVEL is the worst case threshold voltage of the device relative to the 100pF, 1500 OHM Model in accordance with MIL-STD-883B, Method 3015. This field is required for calculation of the part and storage of parameters. The contents of this field is entered directly. If a RANGE of SUSCEPTIBILITY is known, use the MIDPOINT voltage of the RANGE. If unknown, use 99999.

- METAL TYPE is the metallization material used. This field is required for calculation of the part and storage of parameters. The contents of this field is selected from a look up list, which may be not added to.

- SCREEN TYPE is the amount of screening the device has been subjected to. This field is required for calculation of the part and storage of parameters. The contents of this field is selected from a look up list, which may not be added to.

- SCREEN DURATION is the length of the screen performed on the device in millions of hours. This field is required for calculation of the part and storage of parameters. The contents of this field is entered directly and must be greater then zero.

- SCREEN TEMPERATURE is the ambient temperature of the screen performed on the device, in degrees centigrade. This field is required for calculation of the part and storage of parameters. The contents of this field is entered directly and must be greater then zero.

- SCREEN POWER LEVEL is the power dissipated, in watts, by the device in the screen performed. This field is required for calculation of the part and storage of parameters. The contents of this field is entered directly and must be greater then zero.

- AMBIENT TEMPERATURE is the temperature which the device is exposed to, in degrees centigrade. This field is required for calculation of the part and storage of parameters. The contents of this field is entered directly and must be greater then zero.

- ACTUAL POWER LEVEL is the power dissipated by the device in its intended application, in watts. This field is required for calculation of the part and storage of parameters. The contents of this field is entered directly and must be greater then zero.

- CURRENT DENSITY is the average absolute value current density of the majority of metal runs, in 10E06 Amps/sq cm. This field is required for calculation of the part and storage of parameters. The contents of this field is entered directly and must be greater then zero.

- ELECTRIC FIELD is the average electric field value in the gate oxide, in megavolts/cm. This field is required for calculation of the part and storage of parameters. The contents of this field is entered directly and must be greater then zero.

- ENVIRONMENT is the application environment the device is operating in. This field is required for calculation of the part and storage of parameters. The contents of this field is selected from a look up list, which may not be added to.

- RELATIVE HUMIDITY is the average relative humidity expected in the device environment. This field is required for calculation of the part and storage of parameters for non-hermetic packages. The contents of this field is entered directly and must be greater then zero.

- SUBSTRATE CURRENT is the current, in milliamperes, the device substrate carries. This field is required for calculation of the part and storage of parameters. The contents of this field is entered directly and must be greater then zero. If unknown, enter 9999.000000.

- DRAIN CURRENT is the current, in milliamperes, the device drain carries. This field is required for calculation of the part and storage of parameters. The contents of this field is entered directly and must be greater then zero. If unknown, enter 9999.000000.

- DUTY CYCLE is the percentage of total time the device is operated. For example, 50% operation --> duty cycle = 0.50. This field is required for calculation of the part and storage of parameters. The contents of this field is entered directly and must be greater then zero.

- SIGMA OXIDE is dielectric breakdown failures observed from time to failure data on the oxide or similar oxide. This field is required for calculation of the part and storage of parameters. The contents of this field is entered directly and must be greater then zero. If unknown, use 9999.000.

- SIGMA METAL is the sigma for electro-migration failures observed from time to failure data on the metal, or similar metal, of the device. This field is required for calculation of the part and storage of parameters. The contents of this field is entered directly and must be greater then zero.

- SIGMA HOT CARRIER is the sigma for hot carriers failures observed from time to failure data on the same carrier, or similar devices. This field is required for calculation of the part and storage of parameters. The contents of this field is entered directly and must be greater then zero.

APPENDIX D:

DETAILED DATA

ROME AIR DEVELOPMENT CENTER
VHSIC/VHSIC-LIKE/MOS DATABASE

Device ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
1	MASK ROM	UNKNOWN	0	0.0	0.00	DYN HIGH TEMP LIFE	125	80	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	100	1000 NO UNIT	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	85	1000 HOURS	168 HOURS	1	AC/FUNCTION
										500 HOURS	1	OUTPUT LEAKAGE
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	105	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	1	METAL MASKING DEFECT
						DYN HIGH TEMP LIFE	125	108	1000 HOURS	168 HOURS	3	MASKING DEFECT
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	122	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	108	1000 NO UNIT	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	1	COLUMN SHORT TO VSS
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN

ROME AIR DEVELOPMENT CENTER
VHSIC/VHSIC-LIKE/MOS DATABASE

Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
1	MASK ROM	UNKNOWN	3	0.0	0.00	DYN HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	80	1000 NO UNIT	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	1	PARAMETRIC FAILURE, CONTAMINATION
						STAT HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	1	FUNCTIONAL FAILURE
										500 HOURS	1	PARAMETRIC FAILURE, CONTAMINATION
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	85	1000 HOURS	168 HOURS	2	OUTPUT LEAKAGE
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	105	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	108	1000 NO UNIT	168 NO UNIT	0	UNKNOWN
										500 NO UNIT	0	UNKNOWN
										1000 NO UNIT	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	88	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	110	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	3	INPUT LEAKAGE FAIL.
										500 HOURS	1	SHORT, ASSEMBLY ERROR
										1000 HOURS	0	UNKNOWN

ROME AIR DEVELOPMENT CENTER
VHSIC/VHSIC-LIKE/MOS DATABASE

Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
1	MASK ROM	UNKNOWN	0	0.0	0.00	STAT HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT BIAS TEMP HUMID	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	1	SHORT, MISHANDLED AT TEST
										1000 HOURS	4	FAILED PARAMETER, ALUMINUM CORROSION
										1000 HOURS	1	FAILED PARAMETER, ESD
						STAT BIAS TEMP HUMID	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	1	FAILED PARAMETER, ALUMINUM CORROSION
						STAT BIAS TEMP HUMID	125	114	1000 HOURS	168 HOURS	2	INPUT LEAKAGE FAIL., THRES. VOLT. SHIFT
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						TEMPERATURE CYCLE	125	100	500 NO UNIT	500 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	85	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	1	FUNCTIONAL FAILURE, CRATER UNDER BALL BD
										1000 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	102	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	0	UNKNOWN

ROME AIR DEVELOPMENT CENTER
VHSIC/VHSIC-LIKE/MOS DATABASE

Device (Cont'd)

ID#	Description	Package Type	Fea Pin	Dia Siz	Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
1	MASK ROM	UNKNOWN	0	0.0	0.00	PRESSURE POT	125	50	96 HOURS	96 HOURS	0	UNKNOWN
						PRESSURE POT	125	26	96 HOURS	96 HOURS	0	UNKNOWN
						TEMPERATURE CYCLE	125	26	300 CYCLES	300 CYCLES	0	UNKNOWN
2	MASK ROM	UNKNOWN	0	0.0	0.00	DYN HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	111	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	111	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	101	1000 NO UNIT	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	2	PARAMET. LIMIT FAIL., CONTAMINATION
										1000 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	111	100 NO UNIT	100 CYCLES	0	UNKNOWN
						THERMAL SHOCK	125	52	300 CYCLES	300 CYCLES	0	UNKNOWN
						THERMAL SHOCK	125	42	300 CYCLES	300 CYCLES	0	UNKNOWN
						THERMAL SHOCK	125	68	300 CYCLES	300 CYCLES	0	UNKNOWN
						THERMAL SHOCK	125	45	300 CYCLES	300 CYCLES	0	UNKNOWN

Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
2	MASK ROM	UNKNOWN	0	0.0	0.00	THERMAL SHOCK	125	50	300 CYCLES	300 CYCLES	0	UNKNOWN
						THERMAL SHOCK	125	50	300 CYCLES	300 CYCLES	0	UNKNOWN
3	MASK ROM	UNKNOWN	0	0.0	0.00	DYN HIGH TEMP LIFE	125	87	1000 HOURS	168 HOURS	4	FUNCTIONAL FAILURE, DIFFUSION MASK. DEF.
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	104	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	99	1000 NO UNIT	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	120	1000 HOURS	168 HOURS	1	PARAMETRIC FAILURE, CONTAMINATION
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	105	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	90	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	102	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	102	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN

ROME AIR DEVELOPMENT CENTER
VHSIC/VHSIC-LIKE/MOS DATABASE

Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
3	MASK ROM	[illegible]	0	0.0	0.00	DYN HIGH TEMP LIFE	125	102	1000 HOURS	1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	103	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	101	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	96	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	96	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	95	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	1	PARAMETRIC FAILURE, CONTAMINATION
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	102	1000 NO UNIT	168 NO UNIT	0	UNKNOWN
										500 NO UNIT	0	UNKNOWN
										1000 NO UNIT	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	105	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	1	FUNCTIONAL FAILURE, METAL MASKING DEFECT
						STAT HIGH TEMP LIFE	125	102	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	102	1000 HOURS	168 HOURS	0	UNKNOWN

ROME AIR DEVELOPMENT CENTER
VHSIC/VHSIC-LIKE/MOS DATABASE

Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
3	MASK ROM	UNKNOWN	0	0.0	0.00	STAT HIGH TEMP LIFE	125	102	1000 HOURS	500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	102	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	1	FAILED PARAMETER, METAL MASKING DEFECT
						STAT HIGH TEMP LIFE	125	103	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	1	FUNCTIONAL FAILURE, METAL MASKING DEFECT
						STAT HIGH TEMP LIFE	125	103	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	103	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	1	OPEN METAL TRACE, ALUMINUM CORROSION
						TEMPERATURE CYCLE	125	92	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	100	500 CYCLES	500 CYCLES	1	OPEN
						TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	120	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	1	LIFTED BALL BOND
						TEMPERATURE CYCLE	125	92	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	102	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	1	PARAMET. LIMIT FAIL., CONTAMINATION
						TEMPERATURE CYCLE	125	102	1000 CYCLES	500 CYCLES	1	OPEN, WIRE BREAK

Device (Cont'd)

ID	Description	Package Type	Max Die Pin	Max Die Siz	Max Die Area	Test Type	Amb Temp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
3	MASK ROM	UNKNOWN	0	0.0	0.00	TEMPERATURE CYCLE	125	102	1000 CYCLES	1000 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	105	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	88	1000 NO UNIT	500 CYCLES	0	UNKNOWN
										1000 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	103	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	1	OPEN, BALL BOND LIFT
7	UNKNOWN	UNKNOWN	0	0.0	0.00	DYN HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	1	WIRE SWEEP
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	1	AC/FUNCTION
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	63	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN

Device (Cont'd)

ID#	Description	Package Type	Fea Min	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
7	UNKNOWN	UNKNOWN	0	0.0	0.00	DYN HIGH TEMP LIFE	125	100	1000 NO UNIT	168 NO UNIT	0	UNKNOWN
										500 NO UNIT	0	UNKNOWN
										1000 NO UNIT	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	45	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	90	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	99	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	1	INPUT LEAKAGE FAIL., THRES. VOLT. SHIFT
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	96	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN

Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
7	UNKNOWN	UNKNOWN	0	0.0	0.00	DYN HIGH TEMP LIFE	125	100	1000 HOURS	500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	90	1000 HOURS	168 HOURS	1	INPUT LEAKAGE FAIL., THRES. VOLT. SHIFT
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	100	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	96	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT BIAS TEMP HUMID	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	1	OPEN METAL TRACE, ALUMINUM CORROSION
										1000 HOURS	9	OPEN METAL TRACE, ALUMINUM CORROSION
						DYN HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN

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Device (Cont'd)

ID#	Description	Package Type	Pin	Die Siz	Fam Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
7	UNKNOWN	UNKNOWN	0	0.0	0.00	DYN HIGH TEMP LIFE	125	100	1000 HOURS	1000 HOURS	0	UNKNOWN
						STAT BIAS TEMP HUMID	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	4	FUNCTIONAL FAILURE, METAL MASKING DEFECT
										500 HOURS	2	INPUT LEAKAGE FAIL., THRES. VOLT. SHIFT
										1000 HOURS	10	FUNCTIONAL FAILURE, METAL MASKING DEFECT
						STAT BIAS TEMP HUMID	125	100	1000 HOURS	168 HOURS	2	FAILED PARAMETER, ALUMINUM CORROSION
										500 HOURS	1	JUNCTION SHORT
										1000 HOURS	0	UNKNOWN
						STAT BIAS TEMP HUMID	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	4	FAILED PARAMETER, METAL MASKING DEFECT
						STAT BIAS TEMP HUMID	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	3	FAILED PARAMETER, METAL MASKING DEFECT
										500 HOURS	2	FAILED PARAMETER, ALUMINUM CORROSION
										1000 HOURS	0	UNKNOWN
						STAT BIAS TEMP HUMID	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	1	FUNCTIONAL FAILURE, METAL MASKING DEFECT
						STAT BIAS TEMP HUMID	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	1	INPUT LEAKAGE FAIL., THRES. VOLT. SHIFT
										1000 HOURS	1	INPUT LEAKAGE FAIL., THRES. VOLT. SHIFT
						STAT BIAS TEMP HUMID	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	3	INPUT LEAKAGE FAIL., THRES. VOLT. SHIFT
										1000 HOURS	2	INPUT LEAKAGE FAIL., THRES. VOLT. SHIFT
						STAT BIAS TEMP HUMID	125	95	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT BIAS TEMP HUMID	125	98	1000 HOURS	48 HOURS	1	INPUT LEAKAGE FAIL., THRES. VOLT. SHIFT
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN

Device (Cont'd)

IDN	Description	Package Type	Pin	Pkg Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
7	UNKNOWN	UNKNOWN	0	0.0	0.00	STAT BIAS TEMP HUMID	125	98	1000 HOURS	1000 HOURS	0	UNKNOWN
						STAT BIAS TEMP HUMID	125	100	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	1	PIN LEAKAGE, CHIPOUT UNDER BALL
						TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	1	OPEN, BOND LIFT AT FRAME
						TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	23	PIN LEAKAGE, CHIPOUT UNDER BALL
										1000 CYCLES	16	PIN LEAKAGE, CHIPOUT UNDER BALL
						TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	1	SHORT, WIRE SAG
										1000 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	104	1000 CYCLES	500 CYCLES	1	PIN LEAKAGE, CHIPOUT UNDER BALL
										500 CYCLES	1	FUNCTION,METAL, PATTERN SHIFTING
										1000 CYCLES	0	UNKNOWN
						TEMPER[illegible] CYCLE	125	100	1000 NO UNIT	500 CYCLES	9	PIN LEAKAGE, CHIPOUT UNDER BALL
										1000 CYCLES	5	PIN LEAKAGE, CHIPOUT UNDER BALL
						TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	5	PIN LEAKAGE, CHIPOUT UNDER BALL
										1000 CYCLES	33	PIN LEAKAGE, CHIPOUT UNDER BALL
						TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	22	PIN LEAKAGE, CHIPOUT UNDER BALL
										1000 CYCLES	14	PIN LEAKAGE, CHIPOUT UNDER BALL
						TEMPERATURE CYCLE	125	96	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	100	100 NO UNIT	100 CYCLES	0	UNKNOWN

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Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
7	UNKNOWN	UNKNOWN	0	0.0	0.00	PRESSURE POT	125	50	96 HOURS	96 HOURS	2	FUNCTIONAL FAILURE
						PRESSURE POT	125	50	96 HOURS	96 HOURS	2	FUNCTIONAL FAILURE, ALUMINUM CORROSION
						PRESSURE POT	125	50	96 HOURS	96 HOURS	1	FUNCTIONAL FAILURE, ALUMINUM CORROSION
						PRESSURE POT	125	50	96 HOURS	48 HOURS	0	UNKNOWN
										96 HOURS	0	UNKNOWN
						PRESSURE POT	125	50	96 HOURS	96 HOURS	0	UNKNOWN
										96 HOURS	1	FUNCTIONAL FAILURE, ALUMINUM CORROSION
										96 HOURS	1	FAILED PARAMETER, ESD
						PRESSURE POT	125	100	96 HOURS	48 HOURS	0	UNKNOWN
										96 HOURS	0	UNKNOWN
						PRESSURE POT	125	100	96 HOURS	48 HOURS	1	OPEN METAL TRACE, ALUMINUM CORROSION
										96 HOURS	0	UNKNOWN
						THERMAL SHOCK	125	50	300 CYCLES	300 CYCLES	5	INPUT LEAKAGE FAIL., THRES. VOLT. SHIFT
						THERMAL SHOCK	125	50	300 CYCLES	300 CYCLES	0	UNKNOWN
						THERMAL SHOCK	125	50	300 CYCLES	300 CYCLES	0	UNKNOWN
						THERMAL SHOCK	125	50	300 CYCLES	300 CYCLES	0	UNKNOWN
						THERMAL SHOCK	125	50	300 CYCLES	300 CYCLES	2	INPUT LEAKAGE FAIL., THRES. VOLT. SHIFT
						THERMAL SHOCK	125	100	300 CYCLES	300 CYCLES	0	UNKNOWN
9	UNKNOWN	UNKNOWN	0	0.0	0.00	DYN HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN

Device (Cont'd)

IDE	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
9	UNKNOWN	UNKNOWN	0	0.0	0.00	STAT HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	99	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT BIAS TEMP HUMID	125	102	1000 HOURS	102 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT BIAS TEMP HUMID	125	100	1000 NO UNIT	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	1	FUNCTIONAL FAILURE, METAL MASKING DEFECT
										1000 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	3	OPEN, HEEL BREAK
										1000 CYCLES	4	OPEN, BALL BOND LIFT
										1000 CYCLES	2	FAILED PARAMETER, PATTERN SHIFTING
										1000 CYCLES	1	FUNCTIONAL FAILURE, DIE CRACK
						THERMAL SHOCK	125	50	300 CYCLES	300 CYCLES	0	UNKNOWN
						THERMAL SHOCK	125	50	300 CYCLES	300 CYCLES	0	UNKNOWN
10	UNKNOWN	UNKNOWN	0	0.0	0.00	DYN HIGH TEMP LIFE	125	102	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN

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Device (Cont'd)

ID#	Description	Package Type	Pin	Pkg Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
10	UNKNOWN	UNKNOWN	0	0.0	0.00	DTM HIGH TEMP LIFE	125	100	1000 HOURS	500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DTM HIGH TEMP LIFE	125	98	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DTM HIGH TEMP LIFE	125	99	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	2	FUNCTIONAL FAILURE, THRES. VOLT. SHIFT
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DTM HIGH TEMP LIFE	125	99	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DTM HIGH TEMP LIFE	125	100	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DTM HIGH TEMP LIFE	125	100	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DTM HIGH TEMP LIFE	125	99	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DTM HIGH TEMP LIFE	125	100	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	1	INPUT LEAKAGE FAIL., THRES. VOLT. SHIFT
						DTM HIGH TEMP LIFE	125	99	1000 NO UNIT	48 HOURS	0	UNKNOWN

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Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
59	UNKNOWN	UNKNOWN	0	0.0	0.00	DYN HIGH TEMP LIFE	125	99	1000 NO UNIT	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	1	FUNC.,GATE,OXIDE STP, GATE OXIDE DEFECT
						STAT HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	100	1000 NO UNIT	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	99	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	100	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	95	1000 HOURS	48 HOURS	1	FUNCTIONAL FAILURE, CONTAMINATION
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	77	1000 NO UNIT	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT BIAS TEMP HUMID	125	100	1000 HOURS	168 HOURS	1	INPUT LEAKAGE FAIL., THRES. VOLT. SHIFT
										500 HOURS	0	UNKNOWN
										1000 HOURS	2	INPUT LEAKAGE FAIL., THRES. VOLT. SHIFT
										1000 HOURS	1	FAILED PARAMETER, ALUMINUM CORROSION
						STAT BIAS TEMP HUMID	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	1	INPUT LEAKAGE FAIL., THRES. VOLT. SHIFT

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Device (Cont'd)

IDE	Description	Package Type	Pin	Sig	Fac Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
10	UNKNOWN	UNKNOWN	0	0.0	0.00	STAT BIAS TEMP HUMID	125	100	1000 HOURS	1000 HOURS	0	UNKNOWN
						STAT BIAS TEMP HUMID	125	96	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	1	INPUT LEAKAGE FAIL., THRES. VOLT. SHIFT
										1000 HOURS	1	PIN LEAKAGE, CHIPOUT UNDER BALL
						STAT BIAS TEMP HUMID	125	90	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT BIAS TEMP HUMID	125	95	1000 NO UNIT	48 NO UNIT	0	UNKNOWN
										168 NO UNIT	0	UNKNOWN
										500 NO UNIT	1	INPUT LEAKAGE FAIL., THRES. VOLT. SHIFT
										1000 NO UNIT	0	UNKNOWN
						STAT BIAS TEMP HUMID	125	89	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	1	INPUT LEAKAGE FAIL., THRES. VOLT. SHIFT
										1000 HOURS	0	UNKNOWN
						STAT BIAS TEMP HUMID	125	100	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	1	INPUT LEAKAGE FAIL., THRES. VOLT. SHIFT
										1000 HOURS	0	UNKNOWN
						STAT BIAS TEMP HUMID	125	98	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	1	INPUT LEAKAGE FAIL., THRES. VOLT. SHIFT
						STAT BIAS TEMP HUMID	125	100	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT BIAS TEMP HUMID	125	100	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	1	INPUT LEAKAGE FAIL., THRES. VOLT. SHIFT

Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
10	UNKNOWN	UNKNOWN	0	0.0	0.00	STAT BIAS TEMP HUMID	125	98	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT BIAS TEMP HUMID	125	90	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	1	DIE CRACK, INADEQUATE SCRUBBING
						TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	96	1000 NO UNIT	500 CYCLES	0	UNKNOWN
										1000 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	1	PIN LEAKAGE, CHIPOUT UNDER BALL
						TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	100	1000 NO UNIT	500 CYCLES	0	UNKNOWN
										1000 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	96	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	0	UNKNOWN

Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
10	UNKNOWN	UNKNOWN	0	0.0	0.00	TEMPERATURE CYCLE	125	109	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	96	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	0	UNKNOWN
						PRESSURE POT	125	50	96 HOURS	96 HOURS	0	UNKNOWN
						PRESSURE POT	125	110	96 NO UNIT	48 HOURS	0	UNKNOWN
										96 HOURS	0	UNKNOWN
						PRESSURE POT	125	100	96 HOURS	48 HOURS	0	UNKNOWN
										96 HOURS	0	UNKNOWN
						PRESSURE POT	125	50	96 HOURS	48 HOURS	0	UNKNOWN
										96 HOURS	0	UNKNOWN
						PRESSURE POT	125	100	96 HOURS	48 HOURS	0	UNKNOWN
										96 HOURS	0	UNKNOWN
						PRESSURE POT	125	100	96 HOURS	48 HOURS	0	UNKNOWN
										96 HOURS	0	UNKNOWN
						PRESSURE POT	125	98	96 HOURS	48 HOURS	0	UNKNOWN
										96 HOURS	2	PIN LEAKAGE, BAKE RECOVERABLE
						PRESSURE POT	125	100	96 HOURS	48 HOURS	0	UNKNOWN
										96 HOURS	0	UNKNOWN
						PRESSURE POT	125	100	96 HOURS	48 HOURS	0	UNKNOWN
										96 HOURS	0	UNKNOWN
						PRESSURE POT	125	100	96 HOURS	48 HOURS	0	UNKNOWN
										96 HOURS	0	UNKNOWN
						PRESSURE POT	125	70	96 HOURS	48 HOURS	0	UNKNOWN
										96 HOURS	0	UNKNOWN
						PRESSURE POT	125	99	96 HOURS	48 HOURS	0	UNKNOWN

Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
10	UNKNOWN	UNKNOWN	0	0.0	0.00	PRESSURE POT	125	99	96 HOURS	96 HOURS	0	UNKNOWN
						PRESSURE POT	125	100	96 HOURS	48 HOURS	0	UNKNOWN
										96 HOURS	1	PIN LEAKAGE, BAKE RECOVERABLE
						TEMPERATURE CYCLE	125	50	300 CYCLES	300 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	110	300 CYCLES	300 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	100	300 CYCLES	300 CYCLES	1	PIN LEAKAGE, CHIPOUT UNDER BALL
						TEMPERATURE CYCLE	125	50	300 CYCLES	300 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	100	300 CYCLES	300 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	100	300 CYCLES	300 CYCLES	1	PIN LEAKAGE, CHIPOUT UNDER BALL
						TEMPERATURE CYCLE	125	100	300 CYCLES	300 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	100	300 CYCLES	300 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	98	300 CYCLES	300 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	100	300 CYCLES	300 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	70	300 CYCLES	300 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	100	300 CYCLES	300 CYCLES	0	UNKNOWN
11	UNKNOWN	UNKNOWN	0	0.0	0.00	TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	0	UNKNOWN
12	UNKNOWN	UNKNOWN	0	0.0	0.00	DYN HIGH TEMP LIFE	125	100	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	100	1000 HOURS	48 HOURS	0	UNKNOWN

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Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
12	UNKNOWN	UNKNOWN	0	0.0	0.00	DYN HIGH TEMP LIFE	125.	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	81	1000 HOURS	48 HOURS	1	FUNCTIONAL FAILURE, THRES. VOLT. SHIFT
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	100	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT BIAS TEMP HUMID	125	100	1000 NO UNIT	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT BIAS TEMP HUMID	125	97	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						TEMPERATURE CYCLE	125	87	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	0	UNKNOWN
						PRESSURE POT	125	100	96 HOURS	48 HOURS	0	UNKNOWN
										96 HOURS	0	UNKNOWN
13	UNKNOWN	UNKNOWN	0	0.0	0.00	DYN HIGH TEMP LIFE	125	100	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	100	1000 HOURS	48 HOURS	0	UNKNOWN

Device (Cont'd)

IDS	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
13	UNKNOWN	UNKNOWN	0	0.0	0.00	DYN HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	100	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	99	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	100	1000 NO UNIT	48 HOURS	0	UNKNOWN
										168 HOURS	1	FUNCTIONAL FAILURE, METAL MASKING DEFECT
										500 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	99	1000 HOURS	48 HOURS	1	SHORT,WIRE,WIRESAG, ASSEMBLY ERROR
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	1	FUNC.,TRACE,DEGRADE
						DYN HIGH TEMP LIFE	125	100	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	1	FUNCTIONAL FAILURE, ELECTROMIGRATION
						STAT HIGH TEMP LIFE	125	100	1000 HOURS	48 HOURS	3	FUNCTIONAL FAILURE, MET. CONTACT DEFECT

Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
13	UNKNOWN	UNKNOWN	0	0.0	0.00	STAT HIGH TEMP LIFE	125	100	1000 HOURS	48 HOURS	2	PARAMETRIC FAILURE
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	100	1000 NO UNIT	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	1	INPUT LEAKAGE FAIL., THRES. VOLT. SHIFT
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	100	48 NO UNIT	48 HOURS	1	INPUT LEAKAGE FAIL., THRES. VOLT. SHIFT
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	100	1000 HOURS	48 HOURS	1	SHORT,WIRE,WIRESAG, ASSEMBLY ERROR
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	100	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	1	AC/FUNCTION
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	100	1000 HOURS	48 HOURS	2	FUNCTIONAL FAILURE, ELECTROMIGRATION
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	1	INPUT LEAKAGE FAIL., THRES. VOLT. SHIFT
						STAT HIGH TEMP LIFE	125	99	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	1	FUNCTIONAL FAILURE, ELECTROMIGRATION
						STAT HIGH TEMP LIFE	125	100	1000 NO UNIT	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN

Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
13	UNKNOWN	UNKNOWN	0	0.0	0.00	STAT BIAS TEMP HUMID	125	99	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT BIAS TEMP HUMID	125	99	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	1	AC/FUNCTION
										500 HOURS	4	INPUT LEAKAGE FAIL., THRES. VOLT. SHIFT
										1000 HOURS	2	INPUT LEAKAGE FAIL., THRES. VOLT. SHIFT
						STAT BIAS TEMP HUMID	125	100	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	1	INPUT LEAKAGE FAIL., THRES. VOLT. SHIFT
										500 HOURS	0	FAILED PARAMETER, ALUMINUM CORROSION
										1000 HOURS	1	INPUT LEAKAGE FAIL., THRES. VOLT. SHIFT
						STAT BIAS TEMP HUMID	125	100	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	1	FUNCTIONAL FAILURE, ELECTROMIGRATION
						STAT BIAS TEMP HUMID	125	98	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	2	FAILED PARAMETER, ALUMINUM CORROSION
						STAT BIAS TEMP HUMID	125	89	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT BIAS TEMP HUMID	125	99	1000 NO UNIT	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT BIAS TEMP HUMID	125	100	1000 NO UNIT	48 NO UNIT	0	UNKNOWN
										168 NO UNIT	0	UNKNOWN

Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
13	UNKNOWN	UNKNOWN	0	0.0	0.00	STAT BIAS TEMP HUMID	125	100	1000 NO UNIT	500 NO UNIT	0	UNKNOWN
										1000 NO UNIT	0	UNKNOWN
						STAT BIAS TEMP HUMID	125	89	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	1	INPUT LEAKAGE FAIL., THRES. VOLT. SHIFT
										500 HOURS	1	INPUT LEAKAGE FAIL., THRES. VOLT. SHIFT
										1000 HOURS	1	INPUT LEAKAGE FAIL., THRES. VOLT. SHIFT
						STAT BIAS TEMP HUMID	125	99	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	1	FUNCTIONAL FAILURE, ELECTROMIGRATION
						STAT BIAS TEMP HUMID	125	100	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT BIAS TEMP HUMID	125	100	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	6	PIN LEAKAGE, CHIPOUT UNDER BALL
										1000 CYCLES	2	PIN LEAKAGE, CHIPOUT UNDER BALL
						TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	1	PIN LEAKAGE, CHIPOUT UNDER BALL
										1000 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	1	AC/FUNCTION
										1000 CYCLES	1	FUNCTIONAL FAILURE, METAL MASKING DEFECT
						TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	2	PIN LEAKAGE, CHIPOUT UNDER BALL
										1000 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	1	FUNCTIONAL FAILURE, THERMAL STRESS
						TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	0	UNKNOWN

Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
13	UNKNOWN	UNKNOWN	0	0.0	0.00	TEMPERATURE CYCLE	125	100	1000 CYCLES	1000 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	2	PIN LEAKAGE, CHIPOUT UNDER BALL
						TEMPERATURE CYCLE	125	96	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	96	1000 CYCLES	500 CYCLES	2	PIN LEAKAGE, CHIPOUT UNDER BALL
										1000 CYCLES	1	PIN LEAKAGE, CHIPOUT UNDER BALL
						TEMPERATURE CYCLE	125	96	1000 CYCLES	500 CYCLES	1	PIN LEAKAGE, CHIPOUT UNDER BALL
										1000 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	96	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	1	OPEN, CHIPOUT UNDER BALL
						PRESSURE POT	125	50	96 HOURS	48 HOURS	0	UNKNOWN
										96 HOURS	0	UNKNOWN
						PRESSURE POT	125	100	96 HOURS	48 HOURS	0	UNKNOWN
										96 HOURS	0	UNKNOWN
						PRESSURE POT	125	100	96 HOURS	48 HOURS	0	UNKNOWN
										96 HOURS	0	UNKNOWN
						PRESSURE POT	125	100	96 HOURS	48 HOURS	0	UNKNOWN
										96 HOURS	0	UNKNOWN
						PRESSURE POT	125	100	96 HOURS	48 HOURS	0	UNKNOWN
										96 HOURS	0	UNKNOWN
						PRESSURE POT	125	0	96 HOURS	48 HOURS	0	UNKNOWN

Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
13	UNKNOWN	UNKNOWN	0	0.0	0.00	PRESSURE POT	125	0	96 HOURS	96 HOURS	0	UNKNOWN
						PRESSURE POT	125	87	96 HOURS	48 HOURS	0	UNKNOWN
										96 HOURS	2	FUNCTIONAL FAILURE
						PRESSURE POT	125	100	96 HOURS	48 HOURS	0	UNKNOWN
										96 HOURS	1	PIN LEAKAGE, RECOVERD AFTER BAKE
						PRESSURE POT	125	100	96 HOURS	48 HOURS	0	UNKNOWN
										96 HOURS	0	UNKNOWN
						PRESSURE POT	125	100	96 HOURS	48 HOURS	1	OPEN METAL TRACE, ALUMINUM CORROSION
										96 HOURS	0	UNKNOWN
						PRESSURE POT	125	98	96 HOURS	48 HOURS	0	UNKNOWN
										96 HOURS	0	UNKNOWN
						PRESSURE POT	125	100	96 HOURS	48 HOURS	0	UNKNOWN
										96 HOURS	0	UNKNOWN
						PRESSURE POT	125	113	96 HOURS	48 HOURS	0	UNKNOWN
										96 HOURS	0	UNKNOWN
						THERMAL SHOCK	125	50	300 CYCLES	300 CYCLES	11	PIN LEAKAGE, CHIPOUT UNDER BALL
						THERMAL SHOCK	125	100	300 CYCLES	300 CYCLES	0	UNKNOWN
						THERMAL SHOCK	125	94	300 CYCLES	300 CYCLES	5	PIN LEAKAGE, CHIPOUT UNDER BALL
						THERMAL SHOCK	125	100	300 CYCLES	300 CYCLES	1	PIN LEAKAGE, CHIPOUT UNDER BALL
						THERMAL SHOCK	125	100	300 CYCLES	300 CYCLES	0	UNKNOWN
						THERMAL SHOCK	125	100	300 CYCLES	300 CYCLES	0	UNKNOWN
						THERMAL SHOCK	125	100	300 CYCLES	300 CYCLES	0	UNKNOWN
						THERMAL SHOCK	125	100	300 CYCLES	300 CYCLES	0	UNKNOWN
						THERMAL SHOCK	125	100	300 CYCLES	300 CYCLES	3	PIN LEAKAGE, CHIPOUT UNDER BALL

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Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
13	UNKNOWN	UNKNOWN	0	0.0	0.00	THERMAL SHOCK	125	100	300 CYCLES	300 CYCLES	0	UNKNOWN
						THERMAL SHOCK	125	100	300 CYCLES	300 CYCLES	1	PIN LEAKAGE, CHIPOUT UNDER BALL
						THERMAL SHOCK	125	100	300 CYCLES	300 CYCLES	0	UNKNOWN
						THERMAL SHOCK	125	93	300 NO UNIT	300 CYCLES	6	PIN LEAKAGE, CHIPOUT UNDER BALL
14	UNKNOWN	UNKNOWN	0	0.0	0.00	STAT HIGH TEMP LIFE	125	103	1000 NO UNIT	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
15	MASK ROM	UNKNOWN	0	0.0	0.00	DYN HIGH TEMP LIFE	125	101	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	101	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN

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Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
15	MASK ROM	UNKNOWN	0	0.0	0.00	STAT HIGH TEMP LIFE	125	100	1000 HOURS	500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	100	1000 NO UNIT	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						STAT HIGH TEMP LIFE	125	100	1000 HOURS	168 HOURS	1	FUNCTIONAL FAILURE, BOND PAD CORROSION
										500 HOURS	0	UNKNOWN
										1000 HOURS	1	INPUT TRANS. SHORT
						STAT BIAS TEMP HUMID	125	100	1000 HOURS	168 HOURS	1	FUNCTIONAL FAILURE, BOND PAD CORROSION
										500 HOURS	0	UNKNOWN
										1000 HOURS	1	INPUT TRANS. SHORT
						STAT BIAS TEMP HUMID	125	100	1000 HOURS	168 HOURS	2	FAILED PARAMETER, ALUMINUM CORROSION
										500 HOURS	2	FUNCTIONAL FAILURE, DIE CRACK,MAT'L,ASSM
										1000 HOURS	0	UNKNOWN
						TEMPERATURE CYCLE	125	102	1000 CYCLES	500 CYCLES	12	OPEN, BALL BOND LIFT
										1000 CYCLES	2	FUNCTIONAL FAILURE
						TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	0	UNKNOWN
										1000 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	1	FAILED PARAMETER, PATTERN SHIFTING
										1000 CYCLES	2	IONIC LEAKAGE, BAKE RECOVERABLE
						TEMPERATURE CYCLE	125	100	1000 CYCLES	500 CYCLES	1	PIN LEAKAGE, DIE CRACK
										1000 CYCLES	1	OPEN, BALL BOND LIFT
										1000 CYCLES	1	OPEN PARAMETER, DIE CRACK

Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
15	MASK ROM	UNKNOWN	0	0.0	0.00	TEMPERATURE CYCLE	125	100	100 CYCLES	100 CYCLES	2	FINE LEAK FAILURE, VOID IN SEAL
						TEMPERATURE CYCLE	125	100	100 CYCLES	100 CYCLES	0	UNKNOWN
						PRESSURE POT	125	50	96 HOURS	96 HOURS	0	UNKNOWN
						PRESSURE POT	125	50	96 HOURS	96 HOURS	0	UNKNOWN
						PRESSURE POT	125	50	96 HOURS	96 HOURS	0	UNKNOWN
						THERMAL SHOCK	125	50	300 CYCLES	300 CYCLES	1	OPEN, BALL BOND LIFT
						THERMAL SHOCK	125	50	300 CYCLES	300 CYCLES	0	UNKNOWN
16	MASK ROM	UNKNOWN	0	0.0	0.00	STAT BIAS TEMP HUMID	125	105	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	1	LEAKAGE, MOISTURE
17	MASK ROM	UNKNOWN	0	0.0	0.00	STAT BIAS TEMP HUMID	125	104	1000 NO UNIT	168 NO UNIT	1	OPEN METAL TRACE, ALUMINUM CORROSION
										500 NO UNIT	2	OPEN METAL TRACE, ALUMINUM CORROSION
										1000 NO UNIT	4	OPEN METAL TRACE
						PRESSURE POT	125	50	96 HOURS	96 HOURS	0	UNKNOWN
						PRESSURE POT	125	50	96 HOURS	96 HOURS	0	UNKNOWN
						TEMPERATURE CYCLE	125	50	300 CYCLES	300 CYCLES	1	OPEN, BALL BOND LIFT
18	EEPROM	CERAMIC DIP	24	5.0	0.00	DYN HIGH TEMP LIFE	125	159	168 HOURS	168 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	64	500 HOURS	500 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	64	1000 HOURS	1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	152	168 HOURS	168 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	93	2000 HOURS	500 HOURS	0	UNKNOWN

Device (Cont'd)

#	Description	Package Type	Pin	Fam Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
18	EEPROM	CERAMIC DIP	24	5.0	0.00	DTN HIGH TEMP LIFE	125	93	2000 HOURS	1000 HOURS	0	UNKNOWN
										2000 HOURS	1	IONIC CONTAMINATION
						DTN HIGH TEMP LIFE	125	75	2000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
										2000 HOURS	0	UNKNOWN
						DTN HIGH TEMP LIFE	125	328	168 HOURS	168 HOURS	0	UNKNOWN
						DTN HIGH TEMP LIFE	125	99	2000 HOURS	500 HOURS	0	UNKNOWN
										1000 HOURS	1	RETENTION FAILURE
										2000 HOURS	0	UNKNOWN
						DTN HIGH TEMP LIFE	125	387	168 HOURS	168 HOURS	1	IONIC CONTAMINATION
						DTN HIGH TEMP LIFE	125	126	1000 NO UNIT	500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DATA RETENTION BAKE	125	50	2000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
										2000 HOURS	0	UNKNOWN
						DATA RETENTION BAKE	125	24	2000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
										2000 HOURS	0	UNKNOWN
						DATA RETENTION BAKE	125	20	2000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
										2000 HOURS	0	UNKNOWN
						DATA RETENTION BAKE	125	55	2000 NO UNIT	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN

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Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
18	EEPROM	CERAMIC DIP	24	5.0	0.00	DATA RETENTION BAKE	125	55	2000 NO UNIT	500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
										2000 HOURS	0	UNKNOWN
						HIGH TEMP HIGH VOLT	125	25	2000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
										2000 HOURS	0	UNKNOWN
						HIGH TEMP HIGH VOLT	125	25	2000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
										2000 HOURS	0	UNKNOWN
						HIGH TEMP HIGH VOLT	125	51	2000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
										2000 HOURS	0	UNKNOWN
						HIGH TEMP HIGH VOLT	125	25	2000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
										2000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	84	0 NO UNIT	0 NO UNIT	0	UNKNOWN
										2000 HOURS	0	UNKNOWN
19	EEPROM	PLASTIC DIP	24	5.0	0.00	DYN HIGH TEMP LIFE	125	410	168 HOURS	168 HOURS	1	IONIC CONTAMINATION
						DYN HIGH TEMP LIFE	125	51	2000 HOURS	500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
										2000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	309	168 HOURS	168 HOURS	0	UNKNOWN

Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
19	EEPROM	PLASTIC DIP	24	5.0	0.00	DYN HIGH TEMP LIFE	125	76	2000 HOURS	500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
										2000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	214	168 HOURS	168 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	15	2000 HOURS	500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
										2000 HOURS	0	UNKNOWN
						DATA RETENTION BAKE	125	51	2000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
										2000 HOURS	0	UNKNOWN
						DATA RETENTION BAKE	125	25	2000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	1	RETENTION FAILURE
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
										2000 HOURS	0	UNKNOWN
						DATA RETENTION BAKE	125	76	2000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
										2000 HOURS	0	UNKNOWN
						HIGH TEMP HIGH VOLT	125	0	2000 NO UNIT	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
										2000 HOURS	0	UNKNOWN
						HIGH TEMP HIGH VOLT	125	15	48 HOURS	48 HOURS	0	UNKNOWN
						HIGH TEMP HIGH VOLT	125	14	168 HOURS	168 HOURS	0	UNKNOWN
						HIGH TEMP HIGH VOLT	125	13	2000 HOURS	500 HOURS	0	UNKNOWN

Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
19	EEPROM	PLASTIC DIP	24	5.0	0.00	HIGH TEMP HIGH VOLT	125	13	2000 HOURS	1000 HOURS	0	UNKNOWN
										2000 HOURS	2	OXIDE DEFECT
						TEMPERATURE CYCLE	125	57	1000 CYCLES	168 CYCLES	0	UNKNOWN
										500 CYCLES	0	UNKNOWN
										1000 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	59	1000 CYCLES	168 CYCLES	0	UNKNOWN
										500 CYCLES	0	UNKNOWN
										1000 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	30	1000 CYCLES	168 CYCLES	0	UNKNOWN
										500 CYCLES	0	UNKNOWN
										1000 CYCLES	0	UNKNOWN
						RELATIVE HUMIDITY	125	52	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						RELATIVE HUMIDITY	125	52	168 HOURS	168 HOURS	0	UNKNOWN
						RELATIVE HUMIDITY	125	51	500 HOURS	500 HOURS	0	UNKNOWN
						RELATIVE HUMIDITY	125	49	1000 HOURS	1000 HOURS	0	UNKNOWN
						RELATIVE HUMIDITY	125	15	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						RELATIVE HUMIDITY	125	52	500 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
						RELATIVE HUMIDITY	125	47	1000 HOURS	1000 HOURS	0	UNKNOWN
						RELATIVE HUMIDITY	125	52	168 HOURS	168 HOURS	0	UNKNOWN
						RELATIVE HUMIDITY	125	51	500 HOURS	500 HOURS	0	UNKNOWN
						RELATIVE HUMIDITY	125	47	1000 HOURS	1000 HOURS	0	UNKNOWN

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Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
19	EEPROM	PLASTIC DIP	24	5.0	0.00	RELATIVE HUMIDITY	125	15	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						AUTOCLAVE	125	40	240 HOURS	48 HOURS	0	UNKNOWN
										144 HOURS	0	UNKNOWN
										240 HOURS	0	UNKNOWN
						AUTOCLAVE	125	33	240 HOURS	48 HOURS	0	UNKNOWN
										144 HOURS	0	UNKNOWN
										240 HOURS	0	UNKNOWN
						AUTOCLAVE	125	20	144 HOURS	48 HOURS	0	UNKNOWN
										144 HOURS	0	UNKNOWN
						AUTOCLAVE	125	17	240 HOURS	240 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	52	100 CYCLES	100 CYCLES	0	UNKNOWN
										48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	1	OXIDE BREAKDOWN
										1000 HOURS	0	UNKNOWN
										2000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	51	1 CYCLES	48 HOURS	0	UNKNOWN
										1 CYCLES	1	PACKAGE
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
										2000 HOURS	0	UNKNOWN
20	EPROM	CERAMIC DIP	28	0.0	0.00	DYN HIGH TEMP LIFE	150	90	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	150	105	1000 HOURS	[illegible]8 HOURS	0	UNKNOWN
										[illegible]00 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN

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Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
20	EPROM	CERAMIC DIP	28	0.0	0.00	HIGH TEMP STORAGE	[illegible]	40	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						[illegible]. LOW TEMP. LIFE	-20	40	1000 NO UNIT	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
21	UVEPROM	CERAMIC DIP	24	1.2	0.00	DYN HIGH TEMP LIFE	150	86	2000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
										2000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	150	89	2000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	1	CHARGE LOSS, ACCESS TIME, OXIDE DEFECT
										1000 HOURS	0	UNKNOWN
										2000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	150	89	168 HOURS	168 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	150	88	1000 HOURS	500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	150	144	168 HOURS	168 HOURS	1	CHARGE LOSS, ACCESS TIME, OXIDE DEFECT
										500 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	150	144	500 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	150	240	168 HOURS	168 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	150	180	1000 HOURS	500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						HIGH TEMP STORAGE	200	77	1000 HOURS	168 HOURS	1	ICONIC CONT., BITS FAIL, ASSEMBLY DEBRIS
										500 HOURS	0	UNKNOWN
										1000 HOURS	1	CHARGE LOSS, ACCESS TIME, WEAROUT
						HIGH TEMP STORAGE	200	77	1000 HOURS	168 HOURS	0	UNKNOWN

Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Die Siz	Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
21	UVEPROM	CERAMIC DIP	24	1.2	0.00	HIGH TEMP STORAGE	200	77	1000 HOURS	500 HOURS	0	UNKNOWN
										1000 HOURS	2	CHARGE LOSS, ACCESS TIME, WEAROUT
						HIGH TEMP STORAGE	200	77	1000 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
22	EPROM	CERAMIC DIP	28	0.0	0.00	DYN HIGH TEMP LIFE	150	506	168 HOURS	168 HOURS	1	ASSM. DAMAGE, LEAKAGE, POOR BOND
						DYN HIGH TEMP LIFE	150	240	1000 HOURS	500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
23	EPROM	CERAMIC DIP	28	0.0	0.30	DYN HIGH TEMP LIFE	150	127	168 HOURS	168 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	150	103	1000 NO UNIT	500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
24	PLA	100 LCC (FLAT)	100	0.0	0.00	OPERATING LIFE TEST	125	5	1000 HOURS	1000 HOURS	0	UNKNOWN
25	PLA	CERAMIC PGA	120	0.0	0.00	OPERATING LIFE TEST	125	55	1000 HOURS	1000 HOURS	0	UNKNOWN
						OPERATING LIFE TEST	125	55	1000 HOURS	1000 HOURS	0	UNKNOWN
						OPERATING LIFE TEST	125	60	1000 HOURS	1000 HOURS	0	UNKNOWN
26	PLA	PLASTIC PGA	144	0.0	0.00	DYN HIGH TEMP LIFE	125	36	1000 HOURS	1000 HOURS	0	UNKNOWN
						HUMIDITY BIAS LIFE	125	24	1000 HOURS	1000 HOURS	0	UNKNOWN
						HUMIDITY BIAS LIFE	125	25	1000 HOURS	1000 HOURS	0	UNKNOWN
						PRESSURE POT	121	6	256 HOURS	256 HOURS	0	UNKNOWN
						PRESSURE POT	121	7	256 HOURS	256 HOURS	0	UNKNOWN

Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
26	PLA	PLASTIC PGA	144	0.0	0.00	PRESSURE POT	121	7	256 NO UNIT	256 HOURS	0	UNKNOWN
						PRESSURE POT	0	25	96 HOURS	96 HOURS	0	UNKNOWN
						PRESSURE POT	0	25	96 HOURS	96 HOURS	0	UNKNOWN
						TEMPERATURE CYCLE	0	25	500 CYCLES	500 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	0	25	500 CYCLES	500 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	0	21	1000 CYCLES	1000 CYCLES	0	UNKNOWN
27	PLA	CERAMIC LCC (FLAT)	64	0.0	0.00	OPERATING LIFE TEST	125	10	1000 HOURS	1000 HOURS	0	UNKNOWN
28	PLA	LEAD PLASTIC CC	84	0.0	0.00	PRESSURE POT	121	49	96 HOURS	96 HOURS	0	UNKNOWN
						PRESSURE POT	0	49	96 HOURS	96 HOURS	0	UNKNOWN
29	PLA	PLASTIC PGA	84	0.0	0.00	PRESSURE POT	121	25	168 HOURS	168 HOURS	0	UNKNOWN
30	PLA	PLASTIC PGA	100	0.0	0.00	PRESSURE POT	121	30	96 HOURS	96 HOURS	0	UNKNOWN
						TEMPERATURE CYCLE	0	25	140 CYCLES	140 CYCLES	0	UNKNOWN
31	PLA	LEAD PLASTIC CC	84	0.0	0.00	PRESSURE POT	121	96	96 HOURS	96 HOURS	0	UNKNOWN
						PRESSURE POT	121	16	96 HOURS	96 HOURS	0	UNKNOWN
						PRESSURE POT	121	9	96 HOURS	96 HOURS	0	UNKNOWN
						PRESSURE POT	121	25	96 HOURS	96 HOURS	0	UNKNOWN
						PRESSURE POT	0	25	48 HOURS	48 HOURS	0	UNKNOWN
						PRESSURE POT	0	24	48 HOURS	48 HOURS	0	UNKNOWN

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Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
34	PLA	LEAD PLASTIC CC	84	0.0	0.00	PRESSURE POT	0	25	48 HOURS	48 HOURS	0	UNKNOWN
35	PLA	CERAMIC PGA	180	0.0	0.00	TEMPERATURE CYCLE	0	10	100 CYCLES	100 CYCLES	0	UNKNOWN
						TEMP. CYC.,CONST ACC	0	10	10 CYCLES	10 CYCLES	0	UNKNOWN
37	PLA	CLCC (CUSTOM)	68	0.0	0.00	THERMAL MECH. STRESS	0	25	10 CYCLES	10 CYCLES	0	UNKNOWN
38	PLA	CERAMIC LCC (CUSTOM)	132	0.0	0.00	THERMAL MECH. STRESS	0	25	10 CYCLES	10 CYCLES	0	UNKNOWN
40	PLA	LEADED CHIP CARRIER	196	0.0	0.00	TEMP. CYC.,CONST ACC	0	25	10 CYCLES	10 CYCLES	0	UNKNOWN
41	PLA	CERAMIC PGA	84	0.0	0.00	TEMP. CYC.,CONST ACC	0	25	10 CYCLES	10 CYCLES	0	UNKNOWN
42	PLA	CERAMIC PGA	68	0.0	0.00	TEMP. CYC.,CONST ACC	0	15	10 CYCLES	10 CYCLES	0	UNKNOWN
43	PLA	LEAD SIDEBRAZE DIP	48	0.0	0.00	TEMP. CYC.,CONST ACC	0	25	10 CYCLES	10 CYCLES	0	UNKNOWN
						TEMP. CYC.,CONST ACC	0	25	10 CYCLES	10 CYCLES	0	UNKNOWN
						TEMP. CYC.,CONST ACC	0	25	10 CYCLES	10 CYCLES	0	UNKNOWN
						TEMP. CYC.,CONST ACC	0	43	10 CYCLES	10 CYCLES	0	UNKNOWN
44	PLA	CERAMIC LCC	148	0.0	0.00	OPERATING LIFE TEST	125	48	1000 HOURS	1000 HOURS	0	UNKNOWN
45	PLA	CERAMIC LCC	132	0.0	0.00	OPERATING LIFE TEST	125	37	1000 HOURS	1000 HOURS	0	UNKNOWN
46	PLA	CERAMIC PGA	180	0.0	0.00	OPERATING LIFE TEST	125	39	1000 HOURS	1000 HOURS	0	UNKNOWN

Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
46	PLA	CERAMIC PGA	180	0.0	0.00	OPERATING LIFE TEST	125	33	1000 HOURS	1000 HOURS	0	UNKNOWN
						OPERATING LIFE TEST	125	24	1000 HOURS	1000 HOURS	0	UNKNOWN
						OPERATING LIFE TEST	125	48	1000 HOURS	1000 HOURS	0	UNKNOWN
						TEMP. CYC.,CONST ACC	0	45	10 CYCLES	10 CYCLES	0	UNKNOWN
47	PLA	LEAD PLASTIC CC	68	0.0	0.00	PRESSURE POT	121	24	264 HOURS	264 HOURS	0	UNKNOWN
						PRESSURE POT	0	25	48 HOURS	48 HOURS	0	UNKNOWN
48	PLA	LEAD PLASTIC CC	68	0.0	0.00	PRESSURE POT	0	60	96 HOURS	96 HOURS	0	UNKNOWN
49	PLA	LEAD PLASTIC CC	132	0.0	0.00	PRESSURE POT	0	15	96 HOURS	96 HOURS	0	UNKNOWN
50	PLA	CERAMIC PGA	84	0.0	0.00	TEMPERATURE CYCLE	0	9	10 CYCLES	10 CYCLES	0	UNKNOWN
						TEMP. CYC.,CONST ACC	0	10	10 NO UNIT	10 CYCLES	0	UNKNOWN
51	UNKNOWN	CERAMIC PGA	211	0.0	48.50	BURN IN	125	155	168 HOURS	168 HOURS	1	UNKNOWN
52	UNKNOWN	CERAMIC PGA	218	0.0	43.30	BURN IN	125	113	168 HOURS	168 HOURS	1	UNKNOWN
53	UNKNOWN	CERAMIC PGA	219	0.0	42.30	BURN IN	125	107	168 HOURS	168 HOURS	2	UNKNOWN
54	UNKNOWN	CERAMIC PGA	178	0.0	50.50	BURN IN	125	97	168 HOURS	168 HOURS	0	UNKNOWN
55	UNKNOWN	CERAMIC PGA	149	0.0	46.20	BURN IN	125	132	168 HOURS	168 HOURS	0	UNKNOWN
56	UNKNOWN	CERAMIC PGA	220	0.0	40.30	BURN IN	125	141	168 HOURS	168 HOURS	3	UNKNOWN

Device ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
57	UNKNOWN	CERAMIC PGA	212	0.0	31.30	BURN IN	125	126	168 HOURS	168 HOURS	1	UNKNOWN
58	UNKNOWN	CERAMIC PGA	217	0.0	42.70	BURN IN	125	216	168 HOURS	168 HOURS	0	UNKNOWN
59	UNKNOWN	CERAMIC PGA	218	0.0	34.20	BURN IN	125	112	168 HOURS	168 HOURS	1	UNKNOWN
60	UNKNOWN	CERAMIC PGA	212	0.0	42.60	BURN IN	125	172	168 HOURS	168 HOURS	1	UNKNOWN
61	UNKNOWN	CERAMIC PGA	196	0.0	39.00	BURN IN	125	203	168 HOURS	168 HOURS	0	UNKNOWN
62	UNKNOWN	CERAMIC PGA	207	0.0	39.30	BURN IN	125	491	168 HOURS	168 HOURS	3	UNKNOWN
63	UNKNOWN	CERAMIC PGA	195	0.0	37.80	BURN IN	125	157	168 HOURS	168 HOURS	0	UNKNOWN
64	UNKNOWN	CERAMIC PGA	210	0.0	38.00	BURN IN	125	255	168 NO UNIT	168 HOURS	1	UNKNOWN
65	MICROPROCESSOR	PLASTIC DIP	64	0.0	0.00	DYN HIGH TEMP LIFE	125	629	930 HOURS	930 HOURS	5	UNKNOWN
66	MICROPROCESSOR	CERAMIC DIP	64	0.0	44.60	HIGH TEMP OPER.LIFE	125	659	999 HOURS	999 HOURS	3	UNKNOWN
						TEMPERATURE CYCLE	0	74	1000 CYCLES	100 CYCLES	0	UNKNOWN
										500 CYCLES	0	UNKNOWN
										1000 CYCLES	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	537	802 HOURS	802 HOURS	3	UNKNOWN
67	MICROPROCESSOR	CERAMIC LCC (FLAT)	68	0.0	44.60	HIGH TEMP OPER.LIFE	125	45	922 HOURS	922 HOURS	0	UNKNOWN
68	MICROPROCESSOR	CERAMIC DIP	64	0.0	44.60	HIGH TEMP OPER.LIFE	125	173	965 HOURS	965 HOURS	0	UNKNOWN

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Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
68	MICROPROCESSOR	CERAMIC DIP	64	0.0	44.60	DYN HIGH TEMP LIFE	125	120	994 NO UNIT	994 HOURS	1	UNKNOWN
69	SEMICUSTOM GATE ARRY	CERAMIC PGA	144	0.0	0.00	STAT HIGH TEMP LIFE	125	17	1000000 HOURS	1000 HOURS	0	UNKNOWN
70	SEMICUSTOM GATE ARRY	CERAMIC PGA	180	0.0	0.00	STAT HIGH TEMP LIFE	125	57	1000 HOURS	1000 HOURS	1	FUNCTIONAL FAILURE
						STAT HIGH TEMP LIFE	125	100	1000 HOURS	1000 HOURS	3	FUNCTIONAL FAILURE
71	STATIC RAM	UNKNOWN	0	0.0	0.00	BURN IN	125	4048	168 HOURS	168 HOURS	1	DESTROY DURING ANALY, NOMINAL MARCH
						DYN HIGH TEMP LIFE	125	300	1008 HOURS	1008 HOURS	0	UNKNOWN
						STAT BIAS TEMP HUMID	85	100	1008 HOURS	1008 HOURS	0	UNKNOWN
						TEMPERATURE CYCLE	0	200	500 CYCLES	500 CYCLES	0	UNKNOWN
						BURN IN	125	24394	168 HOURS	168 HOURS	10	UNKNOWN
						BURN IN	125	2400	168 HOURS	168 HOURS	0	UNKNOWN
						BURN IN	125	1995	168 HOURS	168 HOURS	2	UNKNOWN
						DYN HIGH TEMP LIFE	125	1409	840 HOURS	840 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	1980	840 HOURS	840 HOURS	0	UNKNOWN
						STAT BIAS TEMP HUMID	85	870	1008 HOURS	1008 HOURS	0	UNKNOWN
						TEMPERATURE CYCLE	0	660	500 CYCLES	500 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	0	2868	500 CYCLES	500 CYCLES	32	UNKNOWN
						TEMPERATURE CYCLE	0	1721	500 CYCLES	500 CYCLES	10	UNKNOWN
72	STATIC RAM	UNKNOWN	0	0.0	0.00	BURN IN	125	26097	168 HOURS	168 HOURS	44	UNKNOWN

Device (Cont'd) ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
72	STATIC RAM	UNKNOWN	0	0.0	0.00	BURN IN	125	2199	168 HOURS	168 HOURS	3	UNKNOWN
						BURN IN	125	1195	168 HOURS	168 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	199	1008 HOURS	1008 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	1800	840 HOURS	840 HOURS	1	UNKNOWN
						DYN HIGH TEMP LIFE	125	2292	840 HOURS	840 HOURS	6	UNKNOWN
						DYN HIGH TEMP LIFE	125	899	168 HOURS	168 HOURS	2	POLY DEFECT, NOMINAL MARCH
										168 HOURS	2	FOREIGN MATTER, NOMINAL MARCH
										168 HOURS	1	FOREIGN MATTER, MARCH
73	STATIC RAM	UNKNOWN	0	0.0	0.00	BURN IN	125	694	168 HOURS	168 HOURS	1	POLY DEFECT, NOMINAL MARCH
						BURN IN	125	3405	168 HOURS	168 HOURS	2	UNKNOWN
						DYN HIGH TEMP LIFE	125	200	1008 HOURS	1008 HOURS	1	POLY DEFECT, NOMINAL MARCH
						DYN HIGH TEMP LIFE	125	706	1008 HOURS	1008 HOURS	2	UNKNOWN
						TEMPERATURE CYCLE	0	100	500 CYCLES	500 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	0	552	500 CYCLES	500 CYCLES	1	UNKNOWN
74	STATIC RAM	UNKNOWN	0	0.0	0.00	BURN IN	125	972	168 HOURS	168 HOURS	2	FOREIGN MATTER, NOMINAL MARCH
						BURN IN	125	4192	168 HOURS	168 HOURS	3	UNKNOWN
						BURN IN	125	2937	168 HOURS	168 HOURS	9	UNKNOWN
						DYN HIGH TEMP LIFE	125	200	1008 HOURS	1008 HOURS	1	FOREIGN MATTER, NOMINAL MARCH
						DYN HIGH TEMP LIFE	125	1448	840 HOURS	840 HOURS	2	UNKNOWN
						DYN HIGH TEMP LIFE	125	1194	1666 HOURS	1666 HOURS	12	UNKNOWN

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Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Fail'ed	Failure Mode/Mechanism
74	STATIC RAM	UNKNOWN	0	0.0	0.00	STAT BIAS TEMP HUMID	85	98	1008 HOURS	1008 HOURS	0	UNKNOWN
						STAT BIAS TEMP HUMID	85	902	1008 HOURS	1008 HOURS	0	UNKNOWN
						STAT BIAS TEMP HUMID	85	421	1008 HOURS	1008 HOURS	0	UNKNOWN
						TEMPERATURE CYCLE	0	150	500 CYCLES	500 CYCLES	1	LIFTED BOND @ POST, CONTINUITY
										500 CYCLES	1	BROKEN WIRE BOND, CONTINUITY
						TEMPERATURE CYCLE	0	580	500 CYCLES	500 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	0	422	500 CYCLES	500 CYCLES	0	UNKNOWN
75	STATIC RAM	UNKNOWN	0	0.0	0.00	BURN IN	125	648	168 HOURS	168 HOURS	2	FOREIGN MATTER, NOMINAL MARCH
										168 HOURS	1	OXIDE DEFECT, NOMINAL MARCH
						BURN IN	125	2772	168 HOURS	168 HOURS	5	UNKNOWN
						BURN IN	125	2075	168 HOURS	168 HOURS	9	UNKNOWN
						DYN HIGH TEMP LIFE	125	299	1008 HOURS	1008 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	1213	840 HOURS	840 HOURS	[illegible]	UNKNOWN
						DYN HIGH TEMP LIFE	125	596	1686 HOURS	1686 HOURS	10	UNKNOWN
76	STATIC RAM	UNKNOWN	0	0.0	0.00	BURN IN	125	1291	168 HOURS	168 HOURS	4	POLY DEFECT, NOMINAL MARCH
										168 HOURS	2	FOREIGN MATTER, NOMINAL MARCH
						BURN IN	125	6468	168 HOURS	168 HOURS	22	UNKNOWN
						BURN IN	125	1478	168 HOURS	168 HOURS	7	UNKNOWN
						DYN HIGH TEMP LIFE	125	300	1008 HOURS	1008 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	1104	840 HOURS	840 HOURS	4	UNKNOWN
						DYN HIGH TEMP LIFE	125	301	840 HOURS	840 HOURS	3	UNKNOWN

Device ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
77	STATIC RAM	UNKNOWN	0	0.0	0.00	BURN IN	125	6482	168 HOURS	168 HOURS	1	LOW RESISTOR VALUE, ICC STAND-BY PARAM.
						DYN HIGH TEMP LIFE	125	399	1008 HOURS	1008 HOURS	0	UNKNOWN
						STAT BIAS TEMP HUMID	0	197	1008 HOURS	1008 HOURS	1	FOREIGN MATTER JUNCT, ICC STAND-BY PARAM.
										1008 HOURS	1	NOMINAL MARCH
						TEMPERATURE CYCLE	0	293	500 CYCLES	500 CYCLES	1	NOMINAL MARCH
78	STATIC RAM	UNKNOWN	0	0.0	0.00	BURN IN	125	6252	168 HOURS	168 HOURS	4	FOREIGN MATTER, NOMINAL MARCH
										168 HOURS	2	NOMINAL MARCH
						DYN HIGH TEMP LIFE	125	299	1008 HOURS	1008 HOURS	1	FOREIGN MATTER, NOMINAL MARCH
						STAT BIAS TEMP HUMID	85	200	1008 HOURS	1008 HOURS	2	LOW RESISTOR VALUE, ICC STAND-BY PARAM.
						TEMPERATURE CYCLE	0	299	500 CYCLES	500 CYCLES	0	UNKNOWN
79	DYNAMIC RAM	UNKNOWN	0	0.0	0.00	BURN IN	125	2995	168 HOURS	168 HOURS	1	POLY DEFECT, NOMINAL MARCH
										168 HOURS	1	MARGINAL ROOMTEMP AC, NOMINAL MARCH
						BURN IN	125	30936	168 HOURS	168 HOURS	43	UNKNOWN
						BURN IN	125	2701	168 HOURS	168 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	400	1008 HOURS	1008 HOURS	0	UNKNOWN
						DYN HIGH TEMP LIFE	125	1398	840 HOURS	840 HOURS	2	UNKNOWN
						STAT BIAS TEMP HUMID	85	150	1008 HOURS	1008 HOURS	0	UNKNOWN
						STAT BIAS TEMP HUMID	85	867	1008 HOURS	1008 HOURS	3	UNKNOWN
						TEMPERATURE CYCLE	0	150	500 CYCLES	500 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	0	1650	500 CYCLES	500 CYCLES	5	UNKNOWN
80	DYNAMIC RAM	UNKNOWN	0	1.3	0.00	BURN IN	125	4997	168 HOURS	168 HOURS	3	OXIDE DAMAGE, NOMINAL MARCH

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Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
80	DYNAMIC RAM	UNKNOWN	0	1.3	0.00	BURN IN	125	4997	168 HOURS	168 HOURS	2	OXIDE DAMAGE, PAGE MODE
						DYN HIGH TEMP LIFE	125	299	1008 HOURS	1005 HOURS	1	OXIDE DAMAGE, NOMINAL MARCH
						STAT BIAS TEMP HUMID	85	100	1008 HOURS	1008 HOURS	0	UNKNOWN
						TEMPERATURE CYCLE	0	150	500 CYCLES	500 CYCLES	0	UNKNOWN
81	UVEPROM	UNKNOWN	0	0.0	0.00	BURN IN	125	914	168 HOURS	168 HOURS	0	UNKNOWN
						BURN IN	125	3553	168 HOURS	168 HOURS	1	UNKNOWN
						DYN HIGH TEMP LIFE	125	200	1008 HOURS	1008 HOURS	1	CHARGE GAIN, NOMINAL MARCH
						DYN HIGH TEMP LIFE	125	1433	840 HOURS	840 HOURS	2	UNKNOWN
						HIGH TEMP STORAGE	150	191	1008 HOURS	1008 HOURS	0	UNKNOWN
						HIGH TEMP STORAGE	150	1526	1008 HOURS	1008 HOURS	3	UNKNOWN
						TEMPERATURE CYCLE	0	294	500 CYCLES	500 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	0	1100	500 CYCLES	500 CYCLES	2	UNKNOWN
82	VARIOUS	UNKNOWN	0	2.0	0.00	DYN HIGH TEMP LIFE	125	134000	1000 HOURS	1000 HOURS	53	OXIDE DEFECT
										1000 HOURS	36	UNKNOWN
										1000 HOURS	39	CONTAMINATION
83	VARIOUS	UNKNOWN	0	1.5	0.00	DYN HIGH TEMP LIFE	125	134000	1000 HOURS	1000 HOURS	53	OXIDE DEFECT
										1000 HOURS	36	UNKNOWN
										1000 HOURS	39	CONTAMINATION
						DYN HIGH TEMP LIFE	125	43200	100 CYCLES	100 CYCLES	1	HERMITICITY LEAKAGE
										1000 HOURS	16	OXIDE DEFECT
										1000 HOURS	15	UNKNOWN
										1000 HOURS	5	CONTAMINATION

Device ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
84	VARIOUS	UNKNOWN	0	1.5	0.00	DYN HIGH TEMP LIFE	125	43200	1000 NO UNIT	1000 HOURS	16	OXIDE DEFECT
										1000 HOURS	15	UNKNOWN
										1000 HOURS	5	CONTAMINATION
						DYN HIGH TEMP LIFE	125	32500	100 CYCLES	1000 HOURS	26	OXIDE DEFECT
										100 CYCLES	0	UNKNOWN
										1000 HOURS	27	UNKNOWN
										1000 HOURS	357	CONTAMINATION
85	EPROM	UNKNOWN	0	2.0	0.00	DYN HIGH TEMP LIFE	125	19200	0 NO UNIT	1000 HOURS	8	OXIDE DEFECT
										1000 HOURS	32	UNKNOWN
										1000 HOURS	1	CONTAMINATION
86	MICROPROCESSOR	UNKNOWN	0	3.0	0.00	DYN HIGH TEMP LIFE	125	107000	0 NO UNIT	1000 HOURS	21	OXIDE DEFECT
										1000 HOURS	15	UNKNOWN
										1000 HOURS	93	UNKNOWN
										1000 HOURS	93	CONTAMINATION
										1000 HOURS	1	PACKAGE
87	EPROM	UNKNOWN	0	2.0	19.72	DYN HIGH TEMP LIFE	125	215000	1000 HOURS	1000 HOURS	1	UNKNOWN
										1000 HOURS	19	OXIDE DEFECT
										1000 HOURS	2	UNKNOWN
										1000 HOURS	53	CONTAMINATION
										1000 HOURS	100	UNKNOWN
88	EPROM	UNKNOWN	0	2.0	38.10	DYN HIGH TEMP LIFE	125	11100	100 CYCLES	100 CYCLES	0	UNKNOWN
										1000 HOURS	4	OXIDE DEFECT
										1000 HOURS	16	UNKNOWN
										1000 HOURS	2	CONTAMINATION
89	STATIC RAM	CERAMIC DIP	18	1.0	0.00	OPERATING LIFE TEST	150	395	1000 NO UNIT	43 HOURS	3	LEAKAGE/SHORT
										168 HOURS	1	COLUMN FAILURE
										500 HOURS	0	UNKNOWN
										1000 HOURS	2	LEAKAGE/SHORT

ROME AIR DEVELOPMENT CENTER
VHSIC/VHSIC-LIKE/MOS DATABASE

Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Siz	Dfe Area	Test Type	Amb Temp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
89	STATIC RAM	CERAMIC DIP	18	1.0	0.00	OPERATING LIFE TEST	150	395	1000 NO UNIT	1000 HOURS	1	BITS FAIL
						HIGH TEMP OPER.LIFE	150	515	1000 HOURS	48 HOURS	5	BITS FAIL
										48 HOURS	1	COLUMN FAILURE
										48 HOURS	1	LEAKAGE/SHORT
										48 HOURS	1	BITS FAIL
										168 HOURS	2	BITS FAIL
										168 HOURS	1	OPEN
										500 HOURS	1	OPEN
										500 HOURS	1	MISHANDLED AT TEST
										1000 HOURS	0	UNKNOWN
						HIGH TEMP OPER.LIFE	150	234	16[illegible] HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	1	COLUMN FAILURE
										168 HOURS	1	LEAKAGE/SHORT
										168 HOURS	1	BITS FAIL
						BAKE	250	80	500 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	4	OPEN
										500 HOURS	14	LEAKAGE/SHORT
						HIGH TEMP, REV BIAS	[illegible]0	80	1000 HOURS	48 HOURS	5	BITS FAIL
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						TEMPERATURE CYCLE	125	40	500 CYCLES	200 CYCLES	0	UNKNOWN
										500 CYCLES	0	UNKNOWN
						HIGH TEMP OPER.LIFE	125	58	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	1	DROPSIE FAILURE
						HIGH TEMP OPER.LIFE	125	115	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						HIGH TEMP OPER.LIFE	125	45	1000 HOURS	48 HOURS	1	COLUMN FAILURE

Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
89	STATIC RAM	CERAMIC DIP	18	1.0	0.00	HIGH TEMP OPER.LIFE	125	45	1000 HOURS	48 HOURS	1	DROPSIE FAILURE
										168 HOURS	1	VOLT SENS SINGLE BIT
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						HIGH TEMP OPER.LIFE	125	395	1000 HOURS	48 HOURS	3	LEAKAGE/SHORT
										168 HOURS	1	COLUMN FAILURE
										500 HOURS	0	UNKNOWN
										1000 HOURS	1	VOLT SENS SINGLE BIT
										1000 HOURS	2	LEAKAGE/SHORT
						HIGH TEMP OPER.LIFE	125	298	1000 HOURS	48 HOURS	1	SINGLE BIT
										168 HOURS	0	UNKNOWN
										500 HOURS	1	VOLT SENS SINGLE BIT
										1000 HOURS	0	UNKNOWN
						HIGH TEMP OPER.LIFE	125	199	1000 HOURS	48 HOURS	1	SINGLE BIT
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						HIGH TEMP OPER.LIFE	125	173	168 HOURS	48 HOURS	1	COLUMN FAILURE
										168 HOURS	0	UNKNOWN
						BAKE	125	52	500 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	1	OPEN
						LOW TEMP OPER. LIFE	125	20	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						HTRB	125	50	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						TEMPERATURE CYCLE	125	50	500 CYCLES	200 CYCLES	0	UNKNOWN

ROME AIR DEVELOPMENT CENTER
VHSIC/VHSIC-LIKE/MOS DATABASE

Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
89	STATIC RAM	CERAMIC DIP	18	1.0	0.00	TEMPERATURE CYCLE	125	50	500 CYCLES	500 CYCLES	0	UNKNOWN
						HIGH TEMP OPER.LIFE	125	65	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						HIGH TEMP OPER.LIFE	125	88	1000 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	1	VOLT SENS SINGLE BIT
										1000 HOURS	0	UNKNOWN
						HIGH TEMP OPER.LIFE	125	38	1000 HOURS	48 HOURS	1	COLUMN FAILURE
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						HIGH TEMP OPER.LIFE	125	396	1000 HOURS	48 HOURS	1	VOLT SENS SINGLE BIT
										168 HOURS	1	COLUMN FAILURE
										500 HOURS	0	UNKNOWN
										1000 HOURS	0	UNKNOWN
						HIGH TEMP OPER.LIFE	125	310	1000 HOURS	48 HOURS	1	ROW
										48 HOURS	1	SINGLE BIT
										168 HOURS	0	UNKNOWN
										500 HOURS	1	OPEN
										1000 HOURS	1	VOLT SENS SINGLE BIT
						HIGH TEMP OPER.LIFE	125	284	168 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
						BAKE	125	110	500 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	2	OPEN
										500 HOURS	1	OPEN
						LOW TEMP OPER. LIFE	125	34	500 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
						HTRB	125	130	500 HOURS	48 HOURS	0	UNKNOWN

Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
89	STATIC RAM	CERAMIC DIP	18	1.0	0.00	HTRB	125	100	500 HOURS	168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
						TEMPERATURE CYCLE	125	40	500 CYCLES	200 CYCLES	0	UNKNOWN
										500 CYCLES	0	UNKNOWN
						HIGH TEMP OPER.LIFE	125	398	500 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
						HIGH TEMP OPER.LIFE	125	300	500 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
						HIGH TEMP OPER.LIFE	125	286	168 HOURS	48 HOURS	1	SINGLE BIT
										168 HOURS	0	UNKNOWN
						BAKE	125	100	500 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
						LOW TEMP OPER. LIFE	125	30	500 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
						HTRB	125	100	500 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	1	SINGLE BIT
										500 HOURS	0	UNKNOWN
						TEMPERATURE CYCLE	125	52	500 CYCLES	200 CYCLES	0	UNKNOWN
										500 CYCLES	0	UNKNOWN
						HIGH TEMP OPER.LIFE	125	99	500 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
										500 HOURS	0	UNKNOWN
						HIGH TEMP OPER.LIFE	125	235	48 HOURS	48 HOURS	17	UNKNOWN
						HIGH TEMP OPER.LIFE	125	2342	168 HOURS	168 HOURS	9	UNKNOWN

Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
89	STATIC RAM	CERAMIC DIP	18	1.0	0.00	HIGH TEMP OPER.LIFE	125	1037	500 HOURS	500 HOURS	6	UNKNOWN
						HIGH TEMP OPER.LIFE	125	2016	1000 HOURS	1000 HOURS	10	UNKNOWN
						HIGH TEMP OPER.LIFE	125	1240	2000 HOURS	2000 HOURS	2	UNKNOWN
						HIGH TEMP OPER.LIFE	125	1979	48 HOURS	48 HOURS	14	UNKNOWN
						HIGH TEMP OPER.LIFE	125	1965	168 HOURS	168 HOURS	4	UNKNOWN
						HIGH TEMP OPER.LIFE	125	625	500 HOURS	500 HOURS	6	UNKNOWN
						HIGH TEMP OPER.LIFE	125	1039	1000 HOURS	1000 HOURS	2	UNKNOWN
						HIGH TEMP OPER.LIFE	125	297	2000 HOURS	2000 HOURS	1	UNKNOWN
						BAKE	125	438	500 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	1	PURPLE PLAGUE
										500 HOURS	15	PURPLE PLAGUE
						LOW TEMP OPER. LIFE	125	171	168 HOURS	48 HOURS	0	UNKNOWN
										168 HOURS	0	UNKNOWN
						LOW TEMP OPER. LIFE	125	54	500 HOURS	500 HOURS	0	UNKNOWN
						LOW TEMP OPER. LIFE	125	74	1000 HOURS	1000 HOURS	0	UNKNOWN
						LOW TEMP OPER. LIFE	125	43	2000 HOURS	2000 HOURS	0	UNKNOWN
						HTRB	125	5	48 HOURS	48 HOURS	5	BAKE RECOVERABLE
						HTRB	125	101	168 HOURS	168 HOURS	1	UNKNOWN
						HTRB	125	322	500 HOURS	500 HOURS	0	UNKNOWN
						TEMPERATURE CYCLE	125	55	200 CYCLES	200 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	180	500 CYCLES	500 CYCLES	0	UNKNOWN
						TEMPERATURE CYCLE	125	1	1000 CYCLES	1000 CYCLES	0	UNKNOWN

Device (Cont'd)

ID#	Description	Package Type	Pin	Fea Siz	Die Area	Test Type	Amb Tmp	Number Tested	Test Duration	Test Time	Number Failed	Failure Mode/Mechanism
89	STATIC RAM	CERAMIC DIP	18	1.0	0.00	TEMPERATURE CYCLE	125	110	2000 NO UNIT	2000 CYCLES	0	UNKNOWN
90	RAM	UNKNOWN	0	1.2	0.00	HIGH TEMP OPER.LIFE	125	315	578 HOURS	578 HOURS	1	BAKE RECOVERABLE
										578 HOURS	1	SINGLE BIT
						HIGH TEMP OPER.LIFE	200	42	84 HOURS	84 HOURS	0	UNKNOWN
91	RAM	UNKNOWN	0	1.2	0.00	HIGH TEMP OPER.LIFE	125	80	578 HOURS	578 HOURS	0	UNKNOWN
92	RAM	UNKNOWN	0	1.2	38.10	HIGH TEMP OPER.LIFE	200	18	68 HOURS	68 HOURS	0	UNKNOWN
						HIGH TEMP OPER.LIFE	200	34	61 HOURS	61 HOURS	0	UNKNOWN
						HIGH TEMP OPER.LIFE	200	20	500 HOURS	52 HOURS	1	UNKNOWN
										191 HOURS	1	UNKNOWN

RADC plans and executes research, development, test and selected acquisition programs in support of Command, Control, Communications and Intelligence (C^3I) activities. Technical and engineering support within areas of competence is provided to ESD Program Offices (POs) and other ESD elements to perform effective acquisition of C^3I systems. The areas of technical competence include communications, command and control, battle management information processing, surveillance sensors, intelligence data collection and handling, solid state sciences, electromagnetics, and propagation, and electronic reliability/maintainability and compatibility.