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Field-Effect Spectroscopy of Interface States

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During the past year our research has been concerned principally with the synthesis by MBE of $In_xAl_{1-x}As/InP$ heterojunctions in strained layer structures (SLS). Some of the layers were grown with their lattice constants matched to that of their (100)-oriented InP substrates. Others were chosen deliberately to be in compression or in tension and with appropriate combinations of their fractional indium concentration, x , and thickness, d, were intended to be strained pseudomorphically or strain-relaxed by the generation and/or motion of misfit dislocations. Conventional as well as double crystal rocking curve X-ray diffraction of the (400)-reflection plane was used to determine the composition-dependent lattice constant and PL spectroscopic measurements at temperatures near 4K and 300K were used to determine the fundamental bandgap of the various layers. The pseudomorphic strain-dependent shifts of the fundamental bandgaps were determined using a linear interpolation between the InAs and AlAs elastic stiffness coefficients, hydrostatic pressure coefficients and shear deformation potentials. These calculations were shown in good agreement with experimental measurements. The calculated composition-dependent critical thickness for the onset of plastic deformation and total relaxation of the strain determined ~~from these~~ measurements is in better agreement with the energy balance model of People and Bean than with the mechanical equilibrium model of Matthews and Blakeslee.

We have also investigated the surface properties of $In_xAl_{1-x}As$ layers within the composition range $0.43 < x < 0.62$. We find, in agreement with the earlier investigations of others, that such undoped layers grown by MBE using a substrate temperature, T_s = 500C are semi-insulating (SI) while those grown at or above T_S = 580C are semiconducting.

By donor-doping our SI $In_xAl_{1-x}As$ layers with silicon during their MBE growth ~~we were able to~~ determine their Schottky barrier height, ϕ_{Bn}, using C-V and internal photoemission measurements. We find that $\phi_{Bn}(x)$ is anomalous rising rapidly as a function of x to ϕ_{Bn} = 1.2 eV, the barrier height of AlAs. We find that in contrast with the SI layers others grown at T_s = 580C, undoped are semiconducting, have normal charge carrier transport properties and their $\phi_{Bn} = 0.62 \pm 0.5$ eV within the same composition range as that used for the SI layers, lattice matched, in compression and in tension relative to their InP substrates.

The enclosed reprints provide further details of this work. Also enclosed are reprints of papers published in the Technical/Scientific literature of work supported, in part, by the Office of Naval Research in the course of this program.

James Roach, who has been supported under this and previous support provided by ONR while continuing his studies at UCSD was awarded the Ph.D. degree on August 7, 1987. A copy of his thesis "Parasitic Interaction between III-V Compound Field Effect Transistors was forwarded to the Office of Naval Research.

Properties of strained layer $In_xAl_{1-x}As$/InP heterostructures

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X-ray diffraction and photoluminescence measurements were made on $In_xAl_{1-x}As$ layers grown by molecular-beam epitaxy whose lattice constants are matched, in tension, or in compression, relative to their (100)-oriented InP substrates. Using a linear interpolation between the InAs and AlAs elastic stiffness coefficients, hydrostatic pressure coefficients, and shear deformation potentials, the strain-dependent fundamental band gaps were calculated and shown to be in good agreement with the experimentally measured data within the pseudomorphic limit. The calculated composition-dependent critical thickness for the onset of plastic deformation of these layers is shown to be in better agreement with the energy balance model of People and Bean than the mechanical equilibrium model of Matthews and Blakeslee.

I. INTRODUCTION

Interest has recently increased in the growth of strained-layer heterostructures. The application of lattice-mismatched layers offers a wider range of electronic properties and the tailoring of such materials can allow the fabrication of novel devices. An important parameter in the growth of acceptable strained layer material is that of a composition-dependent critical thickness. For thicknesses less than the critical thickness h_c the layer is considered to be pseudomorphic. The mismatch strain between layer and substrate produces an elastic deformation of the layer and the interface between substrate and layer remains coherent. For layer thicknesses greater than h_c, a plastic deformation introduces misfit dislocations providing a partial or full relaxation of the mismatch strain and the interface between layer and substrate is incoherent.

The determination of critical thickness with respect to lattice mismatch has led to the development of two theoretical models,[1,2] both of which have found experimental support despite differences between them up to two orders of magnitude. To explain these differences, Fritz *et al.*[3] have suggested the possible role of low- and high-resolution measurement techniques. Differences in resolution are assumed to explain the support reported for both theories. Dodson and Tsao[4] suggest a more elaborate theory based on dislocation dynamics and relaxation via plastic flow. They assume that the thermally activated glide velocity of a dislocation in a strain field is roughly proportional to the average local stress, and, that strain relief is proportional to the density of misfit dislocations such that the effective stress driving the dislocation is reduced in direct proportion to the misfit dislocation density. By using these assumptions they obtain good agreement between calculated values of h_c, and the experimentally measured data on Si_xGe_{1-x}/Si heterostructures made by Bean *et al.*[5] Experimental results have been obtained by Orders and Usher[6] for the $In_xGa_{1-x}As$/GaAs system using double crystal x-ray diffractometry which are also in good agreement with the People and Bean model. Lievin and Fonstad[7] have investigated the properties of pseudomorphic molecular-beam epitaxy (MBE) grown $In_xGa_{1-x}As$ and $In_xAl_{1-x}As$ layers by means of reflection high-energy electron diffraction (RHEED). They define a threshold thickness h_{th} such that growth of thicknesses below this value demonstrate two-dimensional growth. As h_{th} is exceeded, three-dimensional growth can occur, and surface roughening will commence, an effect which can degrade material characteristics. A second thickness h_c describes the critical thickness above which dislocations are generated in the layers. Lievin and Fonstad suggest that h_{th}, which agrees with the critical thickness model presented by Matthews and Blakeslee,[1] may be of more significance than h_c.

$In_xAl_{1-x}As$ is a material of considerable interest for its possible applications in heterojunction transistors and quantum well structures. Although most research on this large band gap III–V material has centered on the specific alloy $In_{0.52}Al_{0.48}As$, whose lattice constant matches that of InP and the high-electron mobility alloy $In_{0.53}Ga_{0.47}As$, the ability to apply strained layers of $In_xAl_{1-x}As$ makes investigation of the lattice mismatched properties of the material worthwhile. $In_xAl_{1-x}As$ has[8] a room-temperature direct-band-gap E_g, in the composition range $0.32 < x < 1$. Davies *et al.*[9] and Wakefield *et al.*[10] have examined MBE-grown $In_xAl_{1-x}As$ by using cathodoluminescence spectroscopy at 4 and 300 K to measure the composition dependence of E_g. By associating the cathodoluminescence emission peak with the fundamental band gap, they have obtained the relationship

$$E_g = 3.02 - 3.99x + 0.74x^2 \text{ eV} \quad (1)$$

valid in the restricted range $x = 0.46$–0.55 at 300 K. Composition of layers was determined from Auger profiling and double-crystal x-ray rocking curves. In addition they have reported that the undoped $In_xAl_{1-x}As$ is semi-insulating when grown at substrate temperatures < 520 °C and semiconducting when grown at temperatures > 580 °C. This semi-insulating characteristic of InAlAs has been observed by others for similar growth temperatures and has been attributed to the presence of a high density of lattice defects. Chika *et al.*[11] and Turco *et al.*[12] have observed a considerable change in the indium incorporation rates during the growth of InAlAs for varying substrate temperatures. Using transmission electron microscopy (TEM), RHEED oscillations,

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x-ray diffraction, photoluminescence (PL), and excitation spectroscopy, Praseuth *et al.*[13] have examined the effects of substrate temperature as well as variations in the source flux ratio on the growth. They have observed that the indium sticking coefficient is related only to substrate temperature and not the arsenic partial pressure. Furthermore, TEM studies have shown the presence of quasiperiodic fluctuations in composition for certain growth conditions and substrate orientations, indicating the possibility of spinodal decomposition. Despite good linewidths from PL spectra, the TEM studies showed poor crystalline quality, establishing no correlation between optical and crystalline qualities in this material.

We have measured the perpendicular lattice constant of the epitaxial layers with respect to their InP substrates by x-ray diffractometry. In addition, PL measurements of the identical samples were used to provide information of the change of the fundamental band gap with composition. Using the information obtained from these two experimental procedures, the relaxation of the InAlAs from a pseudomorphic state to a relaxed state was observed and compared to the two principal models of critical thickness determination.

II. EXPERIMENT

$In_xAl_{1-x}As$ layers were grown on (100)-oriented Fe-doped semi-insulating InP substrates and S or Sn-doped *n*-type ($n = 2\times10^{17}$ cm^{-3}) InP substrates by a Varian Gen 1.5 MBE machine. The InP substrates were chemically cleaned before introduction to the MBE reactor. Prior to growth the substrates were subject to surface oxide removal by heating them to ~510 °C in an As flux. The arsenic stabilized surfaces were observed by means of RHEED, and then lowered or raised to their final substrate growth temperature of 500 or 580 °C. The layers were 0.5–0.6 μm thick with some additional layers up to 1.2 μm thick. All InAlAs layers were Si-doped to concentrations of $1\text{–}8\times10^{17}$ cm^{-3} as determined from Hall and capacitance versus voltage measurements.

The lattice mismatch between each layer and its substrate was measured by x-ray diffraction techniques using the (400) reflection plane to determine the perpendicular lattice constants. Photoluminescence spectroscopy was used directly to determine the fundamental band-gap parameters of the various layers at temperatures near 4 and 300 K.

III. RESULTS AND DISCUSSION

The lattice mismatch is defined as the difference between the unstrained lattice constant of the $In_xAl_{1-x}As$ layer and that of the InP substrate. Assigning the lattice parameter a_0 to the InP substrate, and a to the unstrained $In_xAl_{1-x}As$ layer, an additional lattice parameter a_p can be assigned to the lattice constant of the strained $In_xAl_{1-x}As$ layer along the plane in the growth direction if a simple tetragonally distorted model for the elastic deformation of the layer is used. This model, shown in Fig. 1, in both tension and compression, assumes a coherent heterojunction interface. Lattice mismatch is defined by

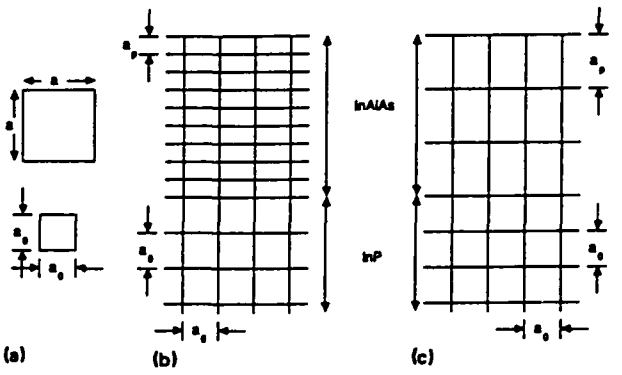

FIG. 1. Schematic representation of (a) unstrained lattice (for $a > a_0$), and tetragonally deformed lattices for (b) biaxial tension, and (c) biaxial compression.

$$\text{lattice mismatch} = \left(\frac{a-a_0}{a_0}\right) = \frac{C_{11}}{C_{11}+2C_{12}}\left(\frac{a_p-a_0}{a_0}\right), \tag{2}$$

where C_{11}, C_{12} are elastic stiffness coefficients of $In_xAl_{1-x}As$. The elastic stiffness coefficients were determined from a linear interpolation between the corresponding values of InAs and AlAs,

$$C_{11}(x) = 12.02 - 3.691x, \tag{3}$$

$$C_{12}(x) = 5.70 - 1.174x. \tag{4}$$

If the $In_xAl_{1-x}As$ layers are to be considered pseudomorphic, that is tetragonally distorted, then their in-plane lattice constant will match that of the InP substrate, given as a_0. The x-ray diffraction measurements will provide the perpendicular lattice constant a_p of the deformed layer. By manipulating Eq. (2), it is possible to calculate the lattice constant for the same layer in an undistorted state, where the

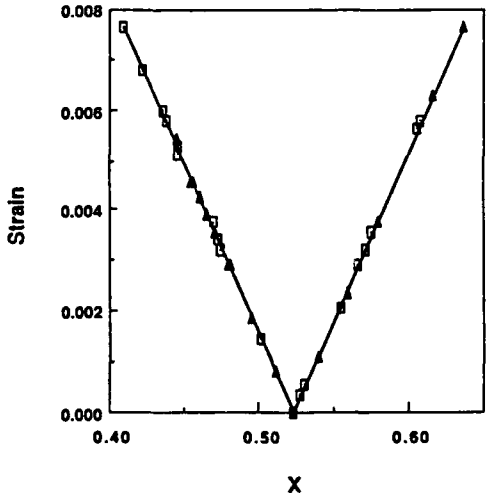

FIG. 2. Strain between $In_xAl_{1-x}As$ and InP as a function of composition x. All samples are assumed to be pseudomorphic. The composition x is calculated using the corrected unstrained $In_xAl_{1-x}As$ lattice constant. (□) Show samples grown at a substrate temperature of 500 °C, and (▲) a substrate temperature of 580 °C.

perpendicular and in-plane lattice constants are equal. This lattice constant is given in Eq. (2) as the value a, the unstrained $In_xAl_{1-x}As$ lattice constant. Once a is determined, it is then possible to calculate the composition of the unstrained $In_xAl_{1-x}As$ by assuming the applicability of Vegard's law. For $In_xAl_{1-x}As$, the lattice constant a is related to the fractional In content x by the equation

$$a = 0.3979x + 5.6605. \tag{5}$$

Figure 2 shows the dependence of $\Delta a/a_0$ on the fractional indium content x, having assumed all samples to be pseudomorphic, and demonstrates a qualitatively similar plot to that found for $In_yGa_{1-y}As$.[14]

Once the unstrained composition is calculated, it is possible to determine its fundamental energy band gap. Following Casey and Panish,[15] the relation between the In mole fraction and the unstrained E_g, in the direct band-gap region is

$$E_g = 3.07 - 3.408x - 0.698x^2. \tag{6}$$

The presence of an elastic strain will also have an effect on the energy band gap of the material. These strain induced band gap shifts can affect E_g for biaxial compression as well as that of tension. Asai and Oe[16] have calculated the energy difference between the conduction and valence band at the $k = 0$ transition to first order. Figure 3 shows the shift in the valence bands and conduction band arrangement about $k = 0$ for a zinc-blende-type crystal in both compression and tension. The change in the energy difference between conduction and valance bands are

$$\Delta E_0(1) = \left[-2b_1\left(\frac{C_{11}-C_{12}}{C_{11}}\right) + b_2\left(\frac{C_{11}+2C_{12}}{C_{11}}\right)\right]\beta, \tag{7}$$

$$\Delta E_0(2) = \left[-2b_1\left(\frac{C_{11}-C_{12}}{C_{11}}\right) - b_2\left(\frac{C_{11}+2C_{12}}{C_{11}}\right)\right]\beta, \tag{8}$$

where b_1 is the hydrostatic deformation potential, b_2 is the shear deformation potential, and the strain β is the same as the lattice mismatch of Eq. (2). The numerical values used in the calculations are presented in Table I.

TABLE I. List of the elastic stiffness coefficients C_{11} and C_{12}, the hydrostatic pressure coefficient $\partial E_g/\partial P$, the hydrostatic deformation potential b_1, and the shear deformation potential b_2, for InAs and AlAs. The hydrostatic deformation potential is related to the hydrostatic pressure coefficient by the relationship $b_1 = -1/3(C_{11}+2C_{12})(\partial E/\partial P)$.

Parameter	InAs[a]	AlAs[b]
C_{11} ($\times 10^{11}$ dyn/cm^2)	8.329	12.02
C_{12} ($\times 10^{11}$ dyn/cm^2)	4.526	5.70
$\frac{\partial E}{\partial P}$ ($\times 10^{-11}$ eV/dyn cm^{-2})	1.000	1.020
b_1 (eV)	−5.79	−7.96
b_2 (eV)	−1.8	−1.5

[a]S. Adachi, J. Appl. Phys. 53, 8775 (1982).
[b]S. Adachi, J. Appl. Phys. 58, R1 (1985).

Figure 4 shows the calculated band gap as determined from the x-ray measurements versus the fundamental band gap considered to coincide with the photoluminescence peak intensity. The figure displays two calculated band gaps for each sample: the strain-corrected $E_g(x)$ data using Eqs. (2)–(8) and the uncorrected $E_g(x)$ data which neglects the application of tetragonal distortion or strain-induced band gap shifts. A straight line of slope one is plotted to help identify the fitting quality of the calculated $E_g(x)$ with the measured PL data.

From Fig. 4, for samples in both biaxial compression ($x > 0.52$) and in biaxial tension ($x < 0.52$), the strain corrected $E_g(x)$ is in fair agreement with the measured values of E_g. However, for $x > 0.6$, the application for strain correction is no longer applicable. Instead, the x-ray-determined perpendicular lattice constant is sufficient for providing a calculated E_g that is in accord with the measured value. This suggests that these samples are no longer pseudomorphic; they may have relaxed to a state such that the perpendicular lattice constant represents the unstrained lattice constant of the layer. Further work is needed to examine the abruptness of this transition from pseudomorphic to a relaxed state.

Figure 5 is a plot of the critical thickness versus composition. The same samples examined in Fig. 4 are plotted here.

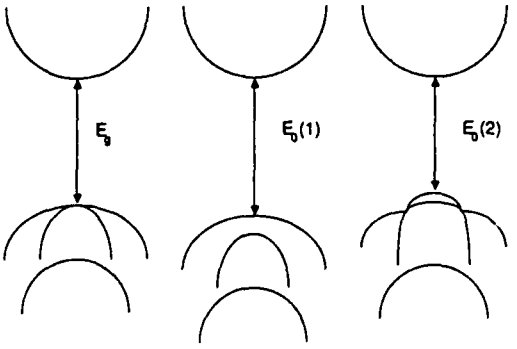

FIG. 3. The valence bands and lowest conduction bands of zinc-blende-type crystals near $k = 0$ for (a) unstrained, (b) under biaxial compressive stress, and (c) under biaxial tensile stress.

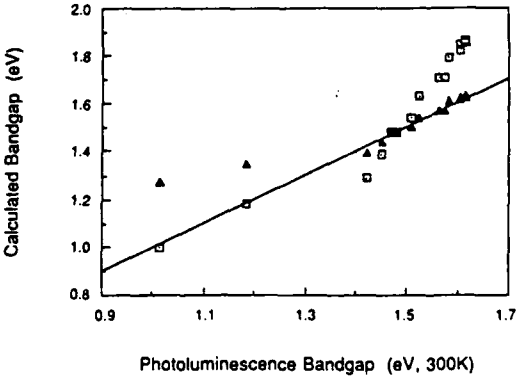

FIG. 4. The calculated fundamental band gap, determined from strain-corrected (▲) and uncorrected (□) x-ray data, as a function of the measured band gap as determined from photoluminescence measurements.

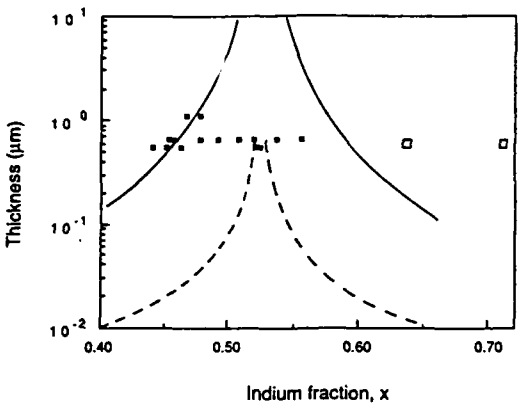

FIG. 5. Critical thickness h_c after the Matthews and Blakeslee model (—) and the People and Bean model (—) as a function of composition x for $In_xAl_{1-x}As/InP$ heterostructures. Data of Fig. 4 are plotted using (■) for pseudomorphic layers and (□) for samples assumed to have undergone relaxation.

Compositions are determined from the x-ray diffraction data with the corrected lattice constants used for those samples appearing pseudomorphic and the uncorrected (or perpendicular) lattice constant for the two samples assumed to have undergone strain relaxation. Also shown are the calculated $h_c(x)$ for two theoretical models. The solid line, is that of People and Bean's energy balance model,[2]

$$h_c = \frac{[1 - V(x)]_b}{[1 + V(x)]32\pi f(x)^2} \ln\left(\frac{h_c}{b}\right). \quad (9)$$

This model is based on the equivalence of the layer strain energy and the energy required to nucleate a dislocation. The dashed line, is the model of Matthews and Blakeslee's mechanical equilibrium model,[1]

$$h_c = \frac{b}{[1 + V(x)]4\pi f(x)} \left[\ln\left(\frac{h_c}{b}\right) + 1\right]. \quad (10)$$

This model is based on the assumption that the onset of the generation of misfit dislocations at the interface is determined by the absence of mechanical equilibrium for threading dislocations. In both models, V is the Poisson's ratio, given as $C_{11}/(C_{11} + C_{12})$, f the lattice mismatch, and b, the Burgers vector, described as the lattice constant of the layer divided by $\sqrt{2}$. The Poisson's ratio and the lattice mismatch are functions of composition. From Fig. 5, the transition region, and therefore critical thickness, shows a much closer agreement to the People and Bean model than the Matthew and Blakeslee model.

IV. SUMMARY

Our x-ray diffraction and photoluminescence measurements indicate a better agreement with the People and Bean energy balance model than the Matthews and Blakeslee mechanical equilibrium model for predicting the composition dependent critical thickness. Fritz and co-workers[3,17] have suggested the possibility of limited resolution in experimentally measuring h_c. They have shown that photoluminescence measurements may be more than two orders of magnitude more sensitive to dislocations than x-ray diffraction and using a scaling factor have been able to fit the Matthews and Blakeslee model to $In_xGa_{1-x}As/GaAs$ and Si_xGe_{1-x}/Si data obtained from relatively low-resolution x-ray diffraction measurements. Yet Praseuth *et al.*[13] have found no clear correlation between crystal perfection and PL linewidth. We consider our PL data to represent essentially low resolution measurements. Assuming Dodson and Tsao's theory[4] of dislocation dynamics and relaxation via plastic flow, a slow initial relaxation combined with the self-limiting increase in dislocation density may also account for our experimental measurements on strained layer $In_xAl_{1-x}As/InP$ heterostructures.

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Schottky barrier height of $In_xAl_{1-x}As$ epitaxial and strained layers

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The Schottky barrier height of *n*-type semiconducting and semi-insulating $In_xAl_{1-x}As$ grown by molecular beam epitaxy has been determined on the lattice-matched composition, $x = 0.523$, in tension and in compression relative to their (110) oriented InP substrates. For the semiconducting material in the composition range $0.43 < x < 0.62$, the barrier height is $\phi_{bn} = 0.62 \pm 0.05$ eV while the anomalous rise and saturation of ϕ_{bn} at 1.2 eV of the semi-insulating material, within the same composition range, is attributed to the presence of AlAs clusters within an $In_xAl_{1-x}As$ matrix.

The ternary alloy III-V compound semiconductor $In_xAl_{1-x}As$ has a direct band gap for $x > 0.32$, its lattice constant matches that of InP for $x = 0.523$, where its fundamental band gap, at room temperature, $E_g = 1.46$ eV. Its conduction and valence band edge discontinuities with respect to an InP heterojunction are 0.52 and 0.40 eV, respectively. It is also lattice matched to the smaller band gap, $E_g = 0.75$ eV, high electron mobility, ternary alloy, $In_{0.53}Ga_{0.47}As$. These properties make it a potentially useful material for a variety of discrete and integrated circuit high-frequency, optoelectronic and microwave device applications which include quantum well and superlattice structures.

Ohno *et al.*[1] have demonstrated the advantages of using $In_{0.52}Al_{0.48}As$ as a buffer layer between a semi-insulating (SI) InP substrate and an $In_{0.53}Ga_{0.47}As$ epitaxial layer in field-effect transistors (FETs). Because $In_{0.53}Ga_{0.47}As$ has a low Schottky barrier height, $\phi_{bn} = 0.2$ eV, a thin superposed layer of $In_{0.52}Ga_{0.48}As$ can also be used to enhance its effective surface barrier height.

Hsieh *et al.*[2] determined by means of internal photoemission measurements that *n*-type $In_{0.52}Al_{0.48}As$ grown by molecular beam epitaxy (MBE) with a substrate temperature of 580 °C has a barrier height $\phi_{bn} = 0.64$ eV. Lin *et al.*[3] have measured by means of capacitance versus voltage (*C-V*) and internal photoemission the composition dependence of metal-semiconductor surface barrier heights of Si-doped $In_xAl_{1-x}As$ layers with compositions in the range $0.42 < x < 0.55$, grown by MBE at a substrate temperature of 500 °C, and found that, at room temperature, $\phi_{bn} = 2.46 - 3.16x$; for the lattice-matched composition they found $\phi_{bn} = 0.85$ eV in fair agreement with that measured by Ohno *et al.*[1] These layers, if undoped, are semi-insulating with properties similar to those made by Wakefield *et al.*[4] and by Davies *et al.*[5] who found that undoped $In_xAl_{1-x}As$ layers grown by MBE are semi-insulating (SI) if grown at a substrate temperature $T_s < 520$ °C while for $T_s > 560$ °C they have semiconducting properties, with *n* typically of the order $10^{16}/cm^3$.

Additional evidence[6-8] has become available which shows that lattice-matched $In_{0.52}Al_{0.48}As$ layers grown at high T_s behave as conventional semiconducting materials while those grown at low T_s are semi-insulating. We have investigated and compared the composition dependence of the surface properties of the semiconducting layers with those of SI layers, lattice matched as well as strained in compression and in tension relative to their InP substrates.

$In_xAl_{1-x}As$ layers were grown on (100) oriented, Fe-doped, semi-insulating, InP substrates and S- or Sn-doped *n*-type ($n = 2\times10^{17}$ cm^{-3}) InP substrates by MBE. Before initiating epitaxial growth, the substrates were heated to $T_s = 510$ °C in As_4 flux in order to remove their surface oxides and to create an As-stabilized surface[9]; thereafter, T_s was lowered or raised to its specific substrate growth temperature of 500 or 580 °C. The fractional In content of the layers was adjusted by changing the Al flux while maintaining a constant In flux with the substrate temperature held at either 500 or 580 °C. The V/III flux ratio was 2–2.5 for samples grown at 500 °C and 6.4–6.6 for samples grown at 580 °C.

The lattice mismatch of each layer with respect to its InP substrate was measured by conventional as well as double-crystal x-ray diffraction using the (400) reflection plane for the determination of its perpendicular lattice constant. Specimens of the same composition and doping grown at a higher temperature have a narrower full width at half maximum (FWHM) x-ray diffraction profile than those grown at a lower substrate temperature. All specimens were found to have specular surfaces without any identifiable morphological defects. The photoluminescence (PL) spectral response was also measured on these layers at 10, 77, and 300 K with the energy of the PL peak considered to be the fundamental band gap. The layers grown at 500 °C were found to have a PL linewidth up to three times greater than that of the specimens grown at 580 °C. Undoped samples grown at 500 °C have a very weak PL intensity compared to that of layers grown at 580 °C. Furthermore, the electron density of undoped layers grown at 500 °C is, at room temperature, between 10^{13} and 10^{14} cm^{-3}, while that of layers grown at 580 °C is between 10^{15} and 10^{16} cm^{-3} as determined by means of Hall measurements. To minimize effects associated with the InAlAs/InP heterojunction, most of the layers were doped deliberately with Si providing electron densities in the range between 1×10^{17} and 2×10^{18} cm^{-3}.

Most of the samples grown on *n*-InP substrates were lightly etched in buffered HF or H_3PO_4:H_2O_2:H_2O just prior to the thermal evaporation of Au or Al Schottky barrier contacts which were defined by photolithographic and lift-

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off techniques. In a few instances Al was evaporated on the epilayers *in situ* and used subsequently for Schottky barrier diodes. Transverse and planar Au-Schottky barrier diodes as well as planar and transverse mercury probe contacts made directly to the epilayer surfaces were used for 1 MHz C-V measurements. The extrapolated $1/C^2$ vs V curves were used to determine the electron concentrations and ϕ_{bn}, neglecting image force lowering. Internal photoemission spectroscopic measurements made on selected specimens confirm ϕ_{bn} determined from the C vs V data to within 0.1 eV.

Figure 1 shows ϕ_{bn} plotted against x, the fractional indium concentration of the layers. Also shown are the measured ϕ_{bn} values of Ohno[1] and Hsieh.[2] The composition was determined by assuming the applicability of Vegard's law with an appropriate correction for the lattice constant dependence on strain present between the InP substrate and the epilayer.[10] Clearly, there is a distinct difference between samples grown at 500 °C, whose barrier heights have a strong compositional dependence, and those grown at 580 °C, whose ϕ_{bn} is essentially independent of composition. We consider the latter to represent the barrier height of homogeneous semiconducting $In_xAl_{1-x}As$. The composition dependence of the Schottky barrier height of the normally undoped SI layers is considered to be anomalous. Because their $\phi_{bn}(x)$ saturates at 1.2 eV, the barrier height of AlAs, we attribute the anomally to the presence of AlAs clusters of variable density embedded in an $In_xAl_{1-x}As$ matrix whose density increases with increasing aluminum concentration. Best[11] found a similar $\phi_{bn}(x)$ dependence in $Al_xGa_{1-x}As$; for small values of x the barrier increased with increasing mole fraction of AlAs saturating at $\phi_{bn} \sim 1.2$ eV.

Chika *et al.*[12] have shown that over an extended range from $T_s \sim 500$ °C to $T_s \sim 570$ °C the growth rate of $In_xAl_{1-x}As$ is constant while for $T_s > 570$ °C the growth rate decreases rapidly reaching approximately half its value for $T_s = 580$ °C, ostensibly due to re-evaporation of In. We assume that the incorporation of AlAs clusters is a function not only of the Al concentration but also of the growth rate: that the density of such cluster decreases as the growth rate decreases.

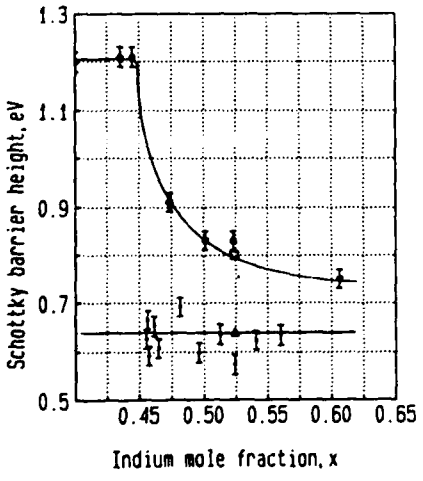

FIG. 1. Barrier height of $In_xAl_{1-x}As$ epitaxial layers lattice matched, strained in compression and in tension relative to their InP substrates. Those grown at $T_s = 500$ °C have an anomalous composition-dependent barrier height; layers grown at $T_s = 580$ °C have a barrier height of 0.62±0.05 eV in the same composition range. Also shown are the earlier measurements of Ref. 1 (open square) and Ref. 2 (open triangle).

The large differences in the In—As and Al—As bond energies and the low temperatures at which growth takes place suggest that nonrandom alloy clustering might be expected in MBE-grown $In_xAl_{1-x}As$. Thermodynamic criteria suggest that ternary III-V compound alloys with large differences in their binary lattice parameters may have miscibility gaps and are subject to spinodal decomposition.[13]

Transmission electron microscopy (TEM), x-ray diffraction, photoluminescence (PL), and excitation spectroscopy have been used by Praseuth *et al.*[14] to investigate the crystalline and optical properties of MBE-grown $In_xAl_{1-x}As$ layers lattice matched to InP. They found by means of TEM that growth on (4×2) reconstructed surfaces leads to quasiperiodic compositional fluctuations of the order of ~15 m, which suggest a spinodal decomposition, of the alloy produced, perhaps by the large surface mobility of the aluminum atoms. Hong *et al.*[15,16] have investigated the charge transport properties of Si-doped $In_xAl_{1-x}As$ layers lattice matched to InP, grown with $T_s = 500$ °C, and found an anomalous increase in μ with increasing temperature in the range between 400 and 600 K. Following the theoretical work of Marsh[17] on clustering in $In_{0.53}Ga_{0.47}As$, they calculated the temperature dependence of alloy scattering by assuming a cluster diameter of 7 nm and a 5% modulation in alloy composition and obtained good agreement with the experimentally measured anomally of μ vs T.

Deep level electron traps with large capture cross sections, with densities of the order $10^{15}/cm^2$ and activation energies of 0.56 and 0.60 eV have been found by Hong *et al.*[18] on the lattice-matched material, grown with $480\ °C < T_s < 520\ °C$ using deep level transient spectroscopic analysis. These data are consistent with the measurements of Whitney *et al.*,[19] who analyzed the nonexponential capacitance transient decay of MBE-grown $In_{0.52}Al_{0.48}As$, with $T_s = 530$ °C, and found that the highest density electron traps had activation energies of 0.58 and 0.61 eV. Following the arguments of Zur *et al.*,[20] such trap densities are sufficient to pin the surface Fermi level of the semiconducting material.

A model which might be more relevant in our case, although applied thus far only to Si and GaAs, is that of Munch,[21,22] who considered that charge transfer between adatoms and adsorbate-induced surface states as well as defect-related states is responsible for the equilibrium position of the surface Fermi level and hence for the barrier height.

An alternative view is that proposed by Freeouf and Woodall[23] who considered that the effective Schottky barrier height might depend on the weighted average of the work functions of one or more interface phases present between a metal and semiconductor. Instead of the metal work function an effective work function ϕ_{eff} is introduced in the Schottky equation such that $\phi_{bn} = \phi_{eff} - \chi$, where χ is the electron affinity of the semiconductor. In a similar

manner a random distribution of AlAs microclusters whose size and density are a function of x might determine the effective work function of the interfacial region: ϕ_{eff} increasing with decreasing x reaching, asymptotically, $\phi_{bn} = 1.2$ eV, the barrier height of AlAs.

In summary, we find that $In_xAl_{1-x}As$ grown by MBE at a substrate temperature of 580 °C is semiconducting and has, within the composition range $435 < x < 0.620$ a barrier height $\phi_{bn} = 0.6210 \pm 0.05$ eV while undoped $In_xAl_{1-x}As$, grown at 500 °C, is semi-insulating, and has a barrier height which increases anomalously with increasing Al concentration. Its saturation at 1.2 eV (the barrier height of AlAs) is attributed to the presence of AlAs clusters within the $In_xAl_{1-x}As$ matrix.

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Automatic shutter control for molecular-beam epitaxial reactors

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A simple, flexible, and relatively inexpensive microcomputer-controlled shutter system intended, principally, for use with molecular-beam epitaxial reactors is described. Eight pneumatic shutters, each one controlling the molecular-beam emission of a corresponding effusion cell, can be operated in any combination simultaneously or sequentially. Such a system has been built and is being used to grow heterojunction and superlattice structures of binary and ternary III-V alloys.

Molecular-beam epitaxy (MBE) is one of the more important techniques available for the synthesis of III-V heterojunctions, quantum wells, and superlattice structures. The composition and thickness of the epitaxial layers are made by opening and closing various combinations of electrically actuated and pneumatically operated shutters which control the emission of molecular or atomic fluxes derived from corresponding Knudsen effusion cell furnaces. Manual operation and switching of these shutters is feasible but it is not an acceptable option, in particular, if growth of multilayer heterojunctions or superlattices of variable thicknesses and compositions is required. Although MBE synthesis may involve simultaneous manipulation of a number of growth control parameters, the availability of a simple computer-controlled shutter system with a predetermined and easily modified program can relieve the operator of a major share of the burden involved in such synthesis. This note describes the implementation of such a system.

A microcomputer is programmed to select the primary address, dwell time, and control intervals of the switching combinations required to operate the MBE shutters. We have chosen an Apple Macintosh Plus microcomputer because of its low cost, simple interface access, wide range of commercially available software for data base management, and its potential use for other applications when not performing the control functions required for these purposes. In our case the MBE reactor is a Varian Gen-II equipped with eight Knudsen effusion cells. A minimum number of electronic circuits need to be constructed in order to provide an appropriate interface between the shutters and the microcomputer.

A block diagram of the MBE computer-controlled shutter system is shown in Fig. 1. The Macintosh Plus has a serial RS-232-C I/O interface. This is interfaced to a programmable scanner by means of an IOtech Corp. Mac488A bus controller, which converts the RS-232-C signal into an IEEE-488 signal for the scanner input. The programmable scanner, a KEITHLEY 705 (Keithley Instruments, Inc.), allows the selection of any one or any combination of eight pole switches that will operate the corresponding eight effusion cell furnace shutters. The scanner simply reads in the required data and writes the corresponding shutter information to an 8-bit output port.

The scanner output port is connected to an electronic solid-state relay system designed and built to Electronic Industries Association (EIA) standards using an RS-422-A specification. Details of the relay system are shown in Fig. 2. The logic of the TTL voltage level output from the programmable scanner is inverted by a Schmitt trigger-type inverter (SN74LS14) to a low-active TTL voltage level for fail-safe operation. In this case, if the RS-422-A cable is accidentally disconnected the shutter control system defaults to an all shutter closed state. The EIA standard RS-422-A balanced voltage digital interface is introduced to allow use of only a +5-V voltage supply to power both the drivers (AM26LS31) and the receivers (AM26LS33). Additionally, this type of interface has shown excellent characteristics with respect to cable length and noise control. The balanced

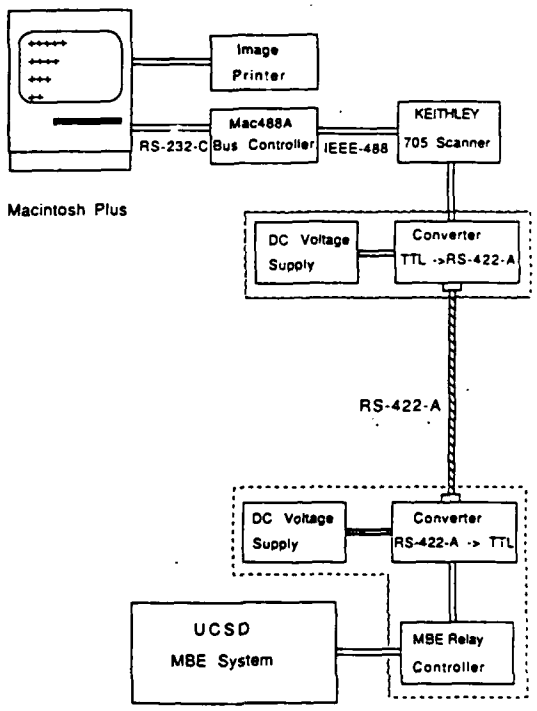

FIG. 1. Block diagram of MBE microcomputer-controlled shutter system.

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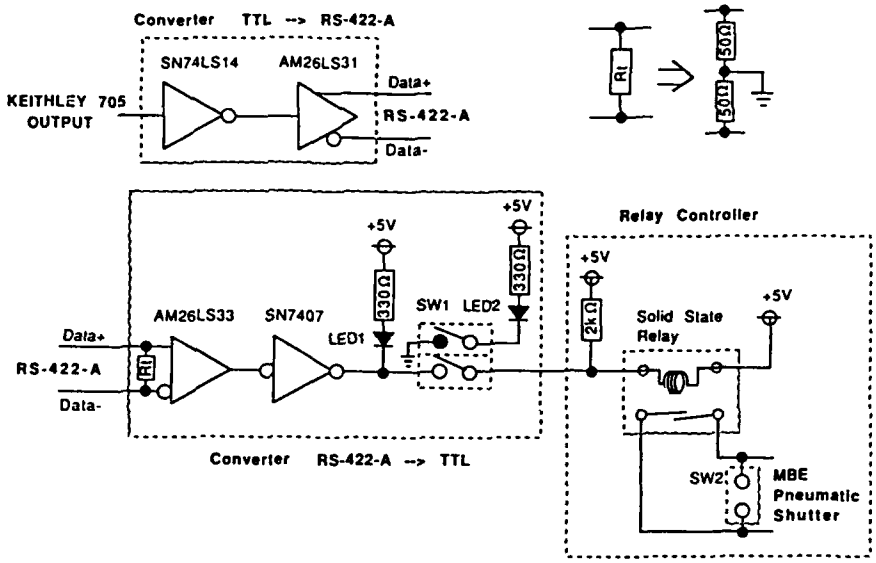

FIG. 2. Details of the interface circuit between the programmable scanner and the MBE system.

signal out of the driver is thus converted to TTL voltage levels by the receiver. A buffer (SN7407) is used to drive an indicator LED and the dc control input of a Gordos GA-8-4B02 relay when switch SW1 is closed. By use of the double-pole switch (SW1), the control line of the solid-state relay may be connected or disconnected, thus placing the shutter in or out of computer control. The dc input-controlled solid-state relays then shunt the ac shutter control line (118VAC:60 μA) of the corresponding pneumatic shutter of the MBE reactor. Since the relay is connected in parallel with the existing manual switches (SW2) on the MBE console, the shutters may be opened manually while in computer-controlled mode, or may be operated manually when the computer control is removed.

The microcomputer programming is very simple and easily written in the standard BASIC computer language. A fairly short program allows control of and communication to the programmable scanner. The Mac488A interprets simple high-level commands sent from the Macintosh Plus serial port and performs the IEEE-488 bus control and hand shaking. The first program step is to open a file for the serial I/O port. The interface parameters (baud-rate, parity, data-bits, and stop-bits) are specified in this code. A few lines of codes are required to satisfy the IEEE-488 protocol and initialize the scanner. A sample program is shown in Fig. 3. A simple routine can test and ensure complete operation of all shutters before the run actually takes place. Programming times allow shutter operations in as little as 1 s to as long as necessary with as many variations as possible. In addition, data can be printed out and stored to a floppy diskette for record keeping or analysis.

Although a specific microcomputer is described here, a different type perhaps with a parallel interface might be equally satisfactory and would allow direct access to the scanner. It might even be possible to eliminate the programmable scanner by substituting hardware which allows direct access to the microcomputer I/O board and feeds the output to independent buffers to drive the relays. This would further reduce the cost of the shutter control system. The use of a commercially available microcomputer allows easy programmability with the additional advantage of having it serve as a desktop facility for other uses when not driving the shutter control system.

```
BASIC Text:                                  Comments:

10  LET SHUTTER = 16                         'Prepare the data to open
                                             'shutter#5.
20  OPEN "COM1:9600,N,8,2" AS 1              'Open communications
                                             'between Mac Plus and
                                             'Mac 488A using 9600 bps, no
                                             'parity, 8 bits, 2 stop-bits.
30  SCANNER$ = "O" + OCT$(SHUTTER) + "X"     'Formats the data for the
                                             'programmable scanner in
                                             'octal code using a header "O"
                                             'and footer "X"
40  PRINT #1,"REMOTE 17"                     'Address device 17 to listen.
                                             'Device 17 is assigned to the
                                             'programmable scanner.
50  PRINT #1,"CLEAR 17"                      'Return device 17 to the
                                             'power-up default condition.
60  PRINT #1,"OUTPUT 17; "SCANNER$""         'Open shutter# 5.
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FIG. 3. An example program for opening the communication between the Macintosh Plus and the programmable scanner. This program executes the opening of one pneumatic shutter.

Simple, inexpensive double ac Hall measurement system for routine semiconductor characterization

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A simple, comparatively inexpensive Hall-effect measurement apparatus is described in which the magnetic field and sample current are sine waves at different frequencies. The current for the electromagnet is obtained directly from the 60-Hz power line, providing magnetic fields $\simeq$0.1 T(rms). The sample current frequency is 200 Hz and the Hall voltage is detected at the sum frequency, 260 Hz, by a lock-in amplifier. Such double ac Hall measurements eliminate most thermoelectric and thermomagnetic errors associated with dc measurements. The same apparatus can be used to measure the sample resistivity at 200 Hz. Hall voltages as small as 10 μV were measured.

Hall measurements made on semiconductor bulk and thin layers typically employ dc currents and static magnetic fields. Significant advantages can be obtained over such dc measurements if the magnetic field and the current to the Hall sample are sinusoidal functions of different frequencies.[1-10] The Hall sample acts as a linear mixer of the current I (at frequency f_I) and magnetic field B (at frequency f_B) through the vector cross product $\mathbf{I}\times\mathbf{B}$ of the Hall voltage, which has a component at the sum $f_+ = f_I + f_B$ and difference $f_- = f_I - f_B$ frequencies. Either component may be selected by means of a lock-in amplifier (LIA), and the rms Hall voltage V_H at f_+ or f_- is given by $V_H = R_H IB/d\sqrt{2}$, where I and B are the rms magnitude of the current to the sample and of the magnetic field, respectively, d is the sample thickness, and R_H is the magnitude of the Hall coefficient. Lock-in detection increases noise rejection over dc measurements and thus increases the sensitivity of the measurement. Furthermore, the multiple commutations of current and magnetic field polarities necessary to eliminate thermoelectric and thermomagnetic errors (e.g., Righi–Leduc, Ettingshausen–Nernst) and misalignment voltages which appear in dc measurements[11,12] are not required with the double ac method.[8,13]

Most double ac systems described in the literature have rather complex features such as special sample holders or magnets,[2,6,8,9] a special sample geometry,[10] or relatively complicated electronic circuitry.[1,3,7-9] We describe here a simple double ac Hall-effect measurement system made primarily of inexpensive, easily obtainable, integrated circuits and components. Sample resistivity using Van der Pauw's method[11,12] can be measured with the same system. This is convenient for low magnetic field semiconductor material characterization.

A block diagram of the double ac Hall measurement system is shown in Fig. 1. The portions enclosed by the dashed lines reside on the circuit board. The 60-Hz 115-V ac power line supplies the current for the electromagnet giving $f_B = 60$ Hz. Power applied to the magnet coils is controlled

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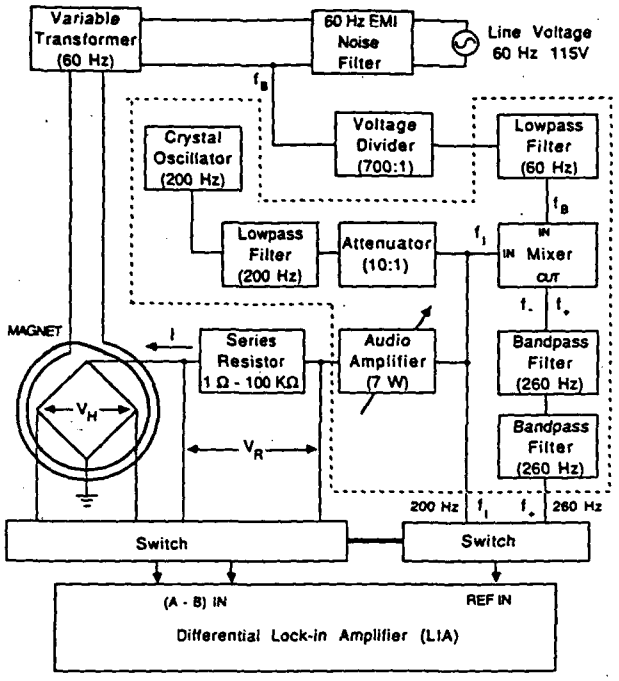

FIG. 1. Block diagram of the double ac Hall system.

by a variable transformer (60-Hz, 25-A rating). The 60-Hz EMI noise filter eliminates high-frequency interference and spikes in the line voltage. The 60-Hz signal is split to a 700:1 voltage divider and passed through a 60-Hz low-pass filter to the mixer input.

The sample current at frequency $f_I = 200$ Hz is generated as a 5-V TTL square wave by a thermally stable, voltage-programmable crystal oscillator (Statek PXO-1000). This signal is sent to the mixer after conversion from square to sine wave by a 200-Hz low-pass filter and amplitude reduction by a 10:1 attenuator. The 200-Hz signal is split at the input of the mixer to an audio amplifier chip and to a switch for use as the reference signal during current and resistivity measurements. The audio amplifier chip (National Semiconductor LM383AT) boosts the current level to the Hall sample (maximum of 100-mA rms at 5-V rms).

The 60 and 200-Hz inputs to the mixer provide $f_+ = 260$ Hz and $f_- = 140$ Hz. For detection of the Hall voltage, the 260-Hz sum frequency was chosen for the LIA reference signal to ease filtering requirements. The output of the mixer, a Motorola MC1494L four quadrant multiplier configured as a balanced modulator,[14] is applied to two 260-Hz, moderate Q, bandpass filters.

The LIA inputs are connected differentially and may be switched to read either the Hall voltage V_H or the voltage drop V_R across the series resistor, the latter being used to determine the magnitude of the sample current I. The current is controlled by R and by a 1-kΩ helipot which controls the gain of the audio amplifier chip. The crystal oscillator operates from a 5-V dc power supply, while the remainder of the chips are powered by a $\pm$ 15 V, 1-A supply. Figure 2 shows the circuit diagram of the portion enclosed in dashed lines in Fig. 1.

The two magnet coils each consist of three windings connected in parallel, with $\simeq$150 turns/winding of 18-AWG copper magnet wire on fiberglass forms of rectangular cross section, 1 in. wide by $\simeq$2.5 in. high by 3 in. long. These are mounted on facing E-shaped cores of high permeability

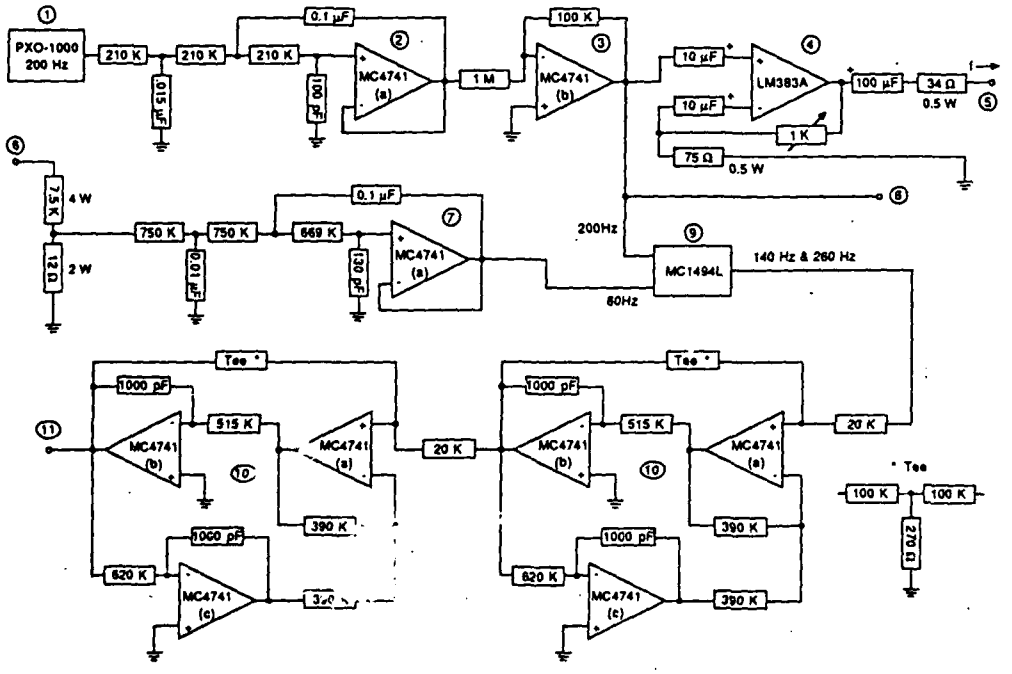

FIG. 2. Circuit for generating sample current and LIA reference signal: (1) crystal oscillator (200 Hz); (2) low-pass filter (200 Hz); (3) attenuator (10:1); (4) audio amplifier chip; (5) 200-Hz current output to sample (through switchable series resistor not shown); (6) 115-V, 60-Hz input to voltage divider (700:1); (7) low pass (60 Hz); (8) tap for 200-Hz reference signal; (9) mixer; (10) bandpass (260 Hz); (11) 260-Hz reference for LIA.

iron–silicon laminations (Thomas & Skinner, Inc.) with a 2-cm-wide airgap in the center of the facing E's. The high currents available directly from the ac power line provide adjustable magnetic fields up to 0.1 T(rms) in the gap.

With the sample in the magnet gap, Hall measurements are made by adjusting the current-gain potentiometer, *LIA* sensitivity controls, and R until significant LIA meter deflection is observed. The LIA phase controls are then set to give maximum meter deflection. The resulting reading is the rms Hall voltage V_H. The sensitivity limit is a few microvolts. The measurement error, determined with a precision Hall generator (F. W. Bell No. BH701), is less than 10% for $V_H = 10\,\mu$V at $B = 0.05$ T(rms). A switch reconnects the LIA across R and switches the LIA reference signal from 260 to 200 Hz. The LIA phase controls are again adjusted for maximum meter deflection giving V_R, which divided by R yields the rms sample current I.

A switch (not shown in figures) is used to commutate the current-supply leads and voltage-sensing leads from the Hall measurement configuration to that required for Van der Pauw resistivity measurements, and is also used to select the 200-Hz reference signal for the LIA. The sample is removed from the magnetic field, and the currents and voltages necessary for the evaluation of the sample resistivity are measured.[11,12]

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A New Semiconductor Device—The Gate-Controlled Photodiode: Device Concept and Experimental Results

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Abstract—**A new semiconductor device—the gate-controlled photodiode (GCPD)—has been presented. Basically, the GCPD is a photodetector whose external quantum efficiency can be modulated by an applied gate voltage. In its linear region, the GCPD is a multiplier of the incident light intensity and gate voltage. Its potential applications include optical matrix multiplication, matrix inversion, etc. This device has been demonstrated experimentally in Si substrate. 10 ns response time and a nonlinearity of less than 3 percent with 30 dB range of light intensity and within 23 dB range of gate voltage have been obtained thus far.**

I. Introduction

RECENTLY a new semiconductor device, the gate-controlled photodiode (GCPD), has been conceived and developed [1], which can be incorporated in a two-dimensional (2-D) GCPD array where it may fulfill the combined function of an electrically addressed 2-D spatial light modulator (SLM) and a photodetector array. Potential applications are for optical signal processing and computing, such as optical matrix multiplication and matrix inversion.

Fig. 1 illustrates schematically the GCPD. It consists of a p–n diode with its depletion region interconnected with the depletion region under a MOS gate. This gate is made of transparent material (e.g., poly-Si), while the p–n junction diode is covered by a metal electrode. If optical radiation at a wavelength shorter than the absorption edge of the semiconductor material is incident on the device, then photocurrent will be generated in the depletion region under the MOS gate. The function of the p–n junction diode is to collect the photocurrent. If the absorption length of the optical radiation in such a semiconductor is larger than the depletion depth X_d, as shown in Fig. 1, only the electron–hole pairs generated within the depletion region are converted into a photocurrent. The electron–hole pairs generated outside the depletion region will recombine; they do not contribute significantly to the photocurrent except by diffusion. Hence, for a substrate with short diffusion length, the photocurrent generated under the MOS gate is proportional approximately to the depletion depth X_d. For a MOS structure biased below its inversion threshold, the depletion depth X_d is controlled by the gate voltage V_G. Very few carriers are generated in the depletion region of the p–n junction diode because the radiation is blocked by the metal electrode. Thus, for reasonably long gates, the photocurrent I_{ph} is proportional, approximately, to the product of the light intensity I_0 and the depletion depth X_d which, in turn, is a function of V_G.

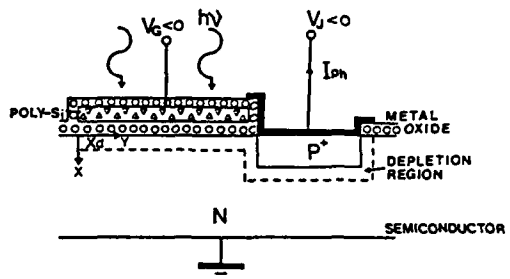

Fig. 1. A schematic diagram of the gate-controlled photodiode (GCPD).

It is assumed that in the depletion region along the direction parallel to the semiconductor–oxide interface, there are drift and thermal diffusion of the charge carriers. This is different from conventional photodiodes in which drift is the dominant transport mechanism. Diffusion is slow, and it may limit the speed of response of the device. In order to increase the drift velocity, a special device structure using a stepped-oxide-thickness gate has been investigated experimentally in order to increase the transverse electric field.

In Section II, the device physics of GCPD are described. Section III is concerned with the experimental device structure and its fabrication, and experimental results are reported in Section IV. The potential applications are discussed briefly in Section V.

II. The Device Physics

The basic physical structure of the GCPD is shown in Fig. 1. Although samples with p-type substrates have also been fabricated, we discuss here primarily devices fabri-

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cated on n-type substrates. The behavior of p-substrate devices is considered to be analogous to the n-substrate devices.

A. Dark Current

Let the p–n junction diode be reverse biased at V_J, while the gate voltage is negatively biased at V_G. In the absence of optical radiation, carriers are thermally generated in the semiconductor. The thermally generated electron–hole pairs in both the gate depletion region and the p–n junction depletion region constitute the dark current. According to the theoretical arguments of Grove and Fitzgerald, the total dark current I_D in a GCPD consists of three components: 1) the current generated in the p–n junction depletion region, 2) the current generated in the gate depletion region, and 3) the current generated in the surface layer of the gate depletion region [2]. Let the depletion depth under the MOS gate of a GCPD have a uniform value X_d; then the dark current I_D may be expressed as

$$I_D = qUV_{JD} + qUA_s\left(X_d + \frac{U_s}{U}\right) \tag{1}$$

where q is the electron charge, U is the bulk generation rate, U_s is the surface generation rate, V_{JD} is the volume of the p–n junction depletion region, and A_s is the surface area of the gate depletion region.

An estimate of the ratio U_s/U can be made on the basis of the Shockley–Read–Hall theory [3] of recombination–generation processes. For single-level recombination–generation centers with energy level $E_t = E_{st} = E_i$ where E_i is the intrinsic Fermi level or for uniformly distributed recombination–generation centers within the forbidden gap, one obtains a simple result [2]:

$$U_s/U = S_0T_0$$

where S_0 is the surface recombination velocity of a depleted surface and T_0 is the carrier lifetime within the depletion region. Typical values of S_0 on thermally oxidized silicon surfaces are on the order of 1–10 cm/s. Typical values of t_0 are on the order of 1–10 μs [5]. Thus, typical values of S_0T_0 are on the order of 10^{-2}–1 μm.

B. The Photocurrent

When a laser beam with power P_L illuminates the gate area A_s of the GCPD, the photogeneration rate in the semiconductor under the gate is given by [4]

$$G(x) = \eta\frac{\phi_0}{d}e^{-(x/d)} \tag{2}$$

where d is the absorption length, η is the quantum efficiency, and ϕ_0 is the incident photon flux per unit area, given by $\phi_0 = P_L(1-\gamma)/A_s \cdot h\nu$ where γ is the total fractional optical radiation loss of the structure due to the absorption and the reflection of the poly-Si gate and the oxide and the reflection of the Si. The photocurrent contributed by the gate depletion region is given by

$$I_{ph,G} = q\int_{V_{GD}} G\,dv = qA_s\int_0^{X_d} G(x)\,dx.$$

The carriers generated within a diffusion length outside the depletion region may also contribute to the photocurrent. If they are all taken into account, we obtain [4]

$$I_{ph,G} = \eta q\phi_0\left[1 - \frac{\exp(-X_d/d)}{1 + L_p/d}\right]A_s \tag{3}$$

where L_p is the hole diffusion length.

Under the assumption that the absorption in the depletion region is uniform, i.e., $X_d \ll d$ and for most cases $L_p \ll d$, then (3) becomes

$$I_{ph,G} = \eta q\frac{\phi_0}{d}\cdot(A_sX_d). \tag{4}$$

From (2), for $X_d \ll d$, $G \cong G_0 = \eta(\phi_0/d)$. Thus, (4) may be rewritten as

$$I_{ph,G} = qG_0(A_sX_d). \tag{5}$$

For thermal generation, the surface layer of a depletion region is considered to have a much higher generation rate than that of the bulk due to a much higher density of recombination–generation centers at the surface layer. For optical generation, the role of surface recombination–generation centers is considered of no significance. Our experimental results also indicate that, for photoexcitation with photon energy slightly larger than the bandgap of the semiconductor, the surface generation process is not important. Then, the total photocurrent I_{ph} in the GCPD may be expressed by (5), i.e., $I_{ph} = I_{ph,G}$. Note that the photogeneration rate in the p–n junction depletion region is negligible because the incident light is blocked by the metal electrode.

C. The External Quantum Efficiency

It is usually convenient to measure experimentally the responsivity, which is defined here as the ratio of the photocurrent to the optical power [4] and the external quantum efficiency η_e.

$$R = I_{ph}/P_L = \frac{\eta q}{h\nu}\cdot\frac{X_d}{d} \tag{6}$$

and

$$\eta_e = \frac{X_d\eta}{d} \tag{7}$$

where we have neglected the total loss coefficients.

D. The Depletion Depth X_d

The relationship between X_d and V_G depends on factors such as doping profile, oxide thickness, and space charges in the oxide layer; these may be due to ionic contamination or electrically active lattice defects, interface states, etc. Under the depletion approximation and for a uniformly doped substrate, one obtains [6]

$$X_d = \frac{\epsilon_s\epsilon_0}{C_0}\left[\left(1 + \frac{2|V_G - V_{FB}|C_0^2}{qN_D\epsilon_s\epsilon_0}\right)^{1/2} - 1\right],$$
$$\text{for } V_G \le 0 \text{ and } |V_{FB}| \le |V_G| \le |V_T| \tag{8}$$

where N_D is the donor concentration, ϵ_s is the dielectric constant of silicon, ϵ_0 is the permittivity of free space, V_T is the inversion threshold voltage, V_{FB} is the flat-band voltage, and C_0 is the capacitance per unit area of the oxide layer.

$$C_0 = \frac{\epsilon_{ox}\epsilon_0}{X_0} \tag{9}$$

where X_0 is the oxide layer thickness and ϵ_{ox} is the dielectric constant of SiO_2.

When $V_G = V_T$, X_d will reach its maximum value $X_{d,\max}$. In the GCPD, there is a p–n junction interconnected with the MOS structure. Thus, nonequilibrium MOS theory [2] should be used to estimate this value in order to take into account the effect of the p–n junction on the MOS structure. A good approximation of $X_{d,\max}$ for the short-gate GCPD is given by [2]

$$X_{d,\max} = \left(\frac{2\epsilon_s\epsilon_0|V_J + 2\phi_F|}{qN_D}\right)^{1/2} \tag{10}$$

where V_J is the junction voltage of the p–n junction diode and $\phi_F = (E_i - E_F)/q$. E_F is the Fermi level of the semiconductor and E_i is the intrinsic level. Thus, the dynamic range of V_G depends on V_J.

Equation (8) derived for no illumination is expected still to be valid when the density of the photogenerated carriers is much smaller than N_D [7].

E. Transport Mechanisms

In the depletion region under the gate, when electron–hole pairs are generated by optical radiation, the electric field separates them, and the electrons and holes drift in opposite directions. In a GCPD with n-type substrate and biased negatively, all photogenerated electrons may drift toward the grounded substrate to contribute to the photocurrent measured in the external circuit. The hole transport mechanism, however, is more complicated. In the gate depletion region, photogenerated holes transfer in the transverse direction parallel to the semiconductor–oxide interface toward the p–n junction. Only those holes which reach the p–n junction contribute to the photocurrent. In a MOS structure not connected to a p–n junction diode, there is only a longitudinal electric field in the direction normal to the semiconductor–oxide interface. In the GCPD, the transverse electric field generally is weak except for the region near the p–n junction. Hence, diffusion plays an important role in hole transport.

Suppose the transverse electric field E_y is zero everywhere under the gate oxide except at $y \cong L$. In that case, the gradient of the hole concentration along the y direction is small at $y \cong 0$. At $y = L$, there is a strong E_y that produces a large drift velocity; thus, the hole concentration is low. Transport of holes along the y direction can then be modeled by the solution of the diffusion equation subject to the following boundary conditions: zero hole gradient at $y = 0$ and zero hole concentration at $y = L$. Such a solution had been obtained by Carnes *et al.* [8].

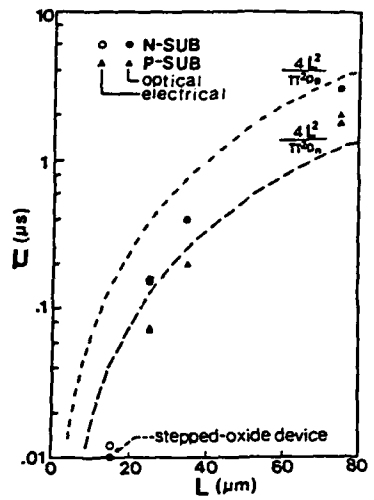

Fig. 2. Response time τ versus gate length L for both n- and p-type substrates. Here, $D_n = 18.3\ cm^2 \cdot s^{-1}$ and $D_p = 6.5\ cm^2 \cdot s^{-1}$.

From this solution, one may obtain the total number of holes remaining at time t, $N_{tot}(t)$, in the depletion region under the gate oxide as [8]

$$N_{tot}(t) = \frac{8}{\pi^2} N_{tot}(o) \exp\left(-\frac{t}{\tau_d}\right) \tag{11}$$

where $\tau_d = 4L^2/\pi^2 D_p$, D_p is the hole diffusion constant. Equation (11) implies that the decay of the photogenerated holes in the depletion region under the gate due to diffusion alone is exponential in time with decay constant τ_d. The calculated τ_d versus gate length L, for both the n and p substrate, are shown as dashed curves in Fig. 2.

In reality, the drift also plays a role in hole transport in the GCPD. In the cases of short-gate devices or stepped-gate oxide devices, the drift mechanism will dominate. The value of $4L^2/\pi^2 D_p$ is only the upper limit of the response time in a GCPD. An investigation on transport mechanisms based on solving 2-D Poisson's equation and continuity equations will be reported elsewhere.

III. Device Structure and Fabrication

GCPD's with poly-Si gates have been fabricated on both n- and p-type silicon substrates. Fig. 3 shows the structure of the GCPD as actually implemented. Fig. 4 shows a top-view photomicrograph of a GCPD sample with 75 μm gate length. The experimental GCPD incorporates the major features of the structure shown in Fig. 1 with some modifications. One modification is the use of an n^-/n^+ epitaxial substrate; another modification is the use of an n^+-doped ring. The objective of the modifications is to minimize series resistance. The 150 μm thick n^+ substrate is phosphorus-doped with doping concentration $N_D = 1 \times 10^{19}\ cm^{-3}$ (0.006 $\Omega \cdot$ cm resistivity), while the 15 μm thick n^--epitaxial layer has $N_D = 4 \times 10^{14}\ cm^{-3}$ (11–12 $\Omega \cdot$ cm resistivity). These epitaxial wafers are ⟨100⟩ oriented. Gate lengths are 75, 35, 25, and 15 μm.

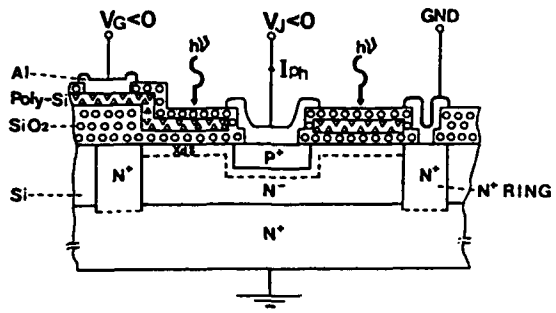

Fig. 3. Cross section of the gate-controlled photodiode (GCPD) with poly-Si gate. n^- on n^+ epitaxial structure and n^+ ring are used to reduce the series resistance.

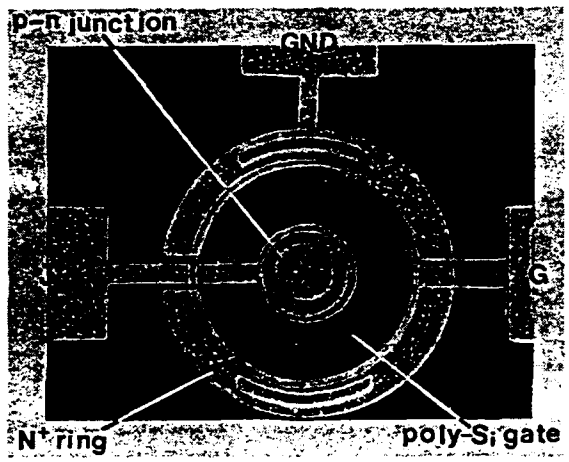

Fig. 4. A 200× microphotograph of a GCPD sample (gate length L = 75 μm).

The fabrication procedure started with the cleaning of silicon wafers. A 1 μm thick field oxide was thermally grown by the wet oxidation process at 1050°C and then selectively etched in buffered HF to define the n^+-ring area. After the n^+ ring was formed by phosphorus diffusion, a gate oxide of 1000 Å was then grown in dry O_2 at 1100°C on the gate area. Then the 5000 Å thick poly-Si was deposited at 625°C by LPCVD. The poly-Si gate was patterned by photolithography and plasma etching. Boron diffusion was carried out simultaneously for both the p^+ region of the p–n junction diode and the poly-Si gate—this is a so-called "self-alignment diffusion process." After high-temperature annealing in Ar at 1000°C for 30 min, the contact windows were opened and the Al electrodes were formed. Then, the samples were annealed in forming gas (10 percent hydrogen and 90 percent nitrogen) at 450°C for 30 min.

After the above process, the density of the fixed oxide charge was determined to be about 3×10^{10} cm^{-2}, and the interface state density was determined to be less than 2.5×10^{10} cm^{-2} from the C–V measurements. The flat-band voltages V_{FB} were determined to be −0.3 to −0.5 V.

IV. Experimental Measurements

A. The Experimental Evaluation Setup

The experimental setup is illustrated in Fig. 5. A CW semiconductor laser with 0.84 μm wavelength is used as the light source. Its maximum output power is 5.5 mW and its response time is 1 ns. The relationship between electrical current input and optical output of the semiconductor laser was calibrated accurately. The gate voltage V_G of the GCPD, defined as the voltage between the gate and the substrate, was supplied by either a dc source or a pulse generator. The photocurrent I_{ph} is measured through a sampling resistor R_0.

B. Responsivity and Photocurrent

If we neglect the surface photogeneration current and the diffusion of the carriers into the depletion region from the substrate, the responsivity R and the photocurrent I_{ph} of the GCPD are given by (6) and (5). The dependence of X_d on V_G is given by (8). Combining (8) with I_{ph}, we obtain the dependence of I_{ph} on both P_L and V_G:

$$I_{ph} = \frac{\eta q}{h\nu} \cdot \frac{P_L}{d} \cdot \frac{\epsilon_s \epsilon_0}{C_0} \left[\left(1 + \frac{2|V_G - V_{FB}|C_0^2}{qN_D\epsilon_s\epsilon_0} \right)^{1/2} - 1 \right], \quad \text{for } |V_{FB}| \le |V_G| < |V_T|. \tag{12}$$

The computed curves of I_{ph} versus P_L, V_G as a parameter are shown in Figs. 6 and 7. Equation (12) is valid for substrates with uniform doping profile when the effect of the p^+ region on the depletion region under the gate can be neglected. Fig. 6 also shows the experimental data for the 75 μm gate-length GCPD. For $V_G \le -2$ V, the data agree with (12) well. In Fig. 7, for the 25 μm gate-length sample, the experimental data deviates from (12) for $V_G > -10$ V. This deviation is attributed, in part, to the effect of the p^+ region on the depletion region under the gate. In the case of shorter gate length, one-dimension approximation is no longer valid, and two-dimension analysis must be used.

Fig. 8 shows the calculated and the measured responsivity R versus V_G for 75, 35, and 25 μm gate-length samples, respectively. Note that the measured responsivity is not zero at zero gate voltage for all the samples. When $V_G = 0$, there is no depletion layer under the gate. Probably the zero-gate-voltage photocurrent $I_{ph,0}$ is due to the carriers generated near the p–n junction within a hole-diffusion length range as illustrated in the inset in Fig. 9. In order to verify this explanation, let the gate width be unity; then we have

$$I_{ph,0} = qG_0 \cdot L_p(X_j + w)$$

where L_p is the hole diffusion length, X_j is the junction depth, and w is the depletion depth of the p–n junction. Assuming uniform absorption, we obtain

$$G_0 = \eta \frac{\phi_0}{d} = \frac{\eta}{d} \frac{P_L}{A_s \cdot h\nu}.$$

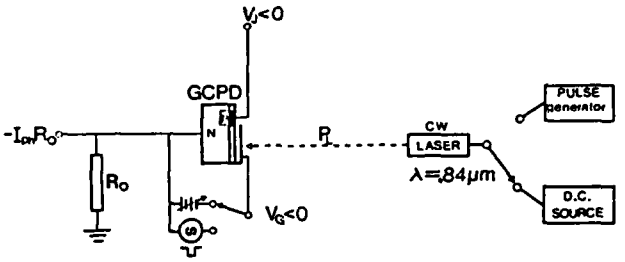

Fig. 5. A schematic diagram of the experimental setup.

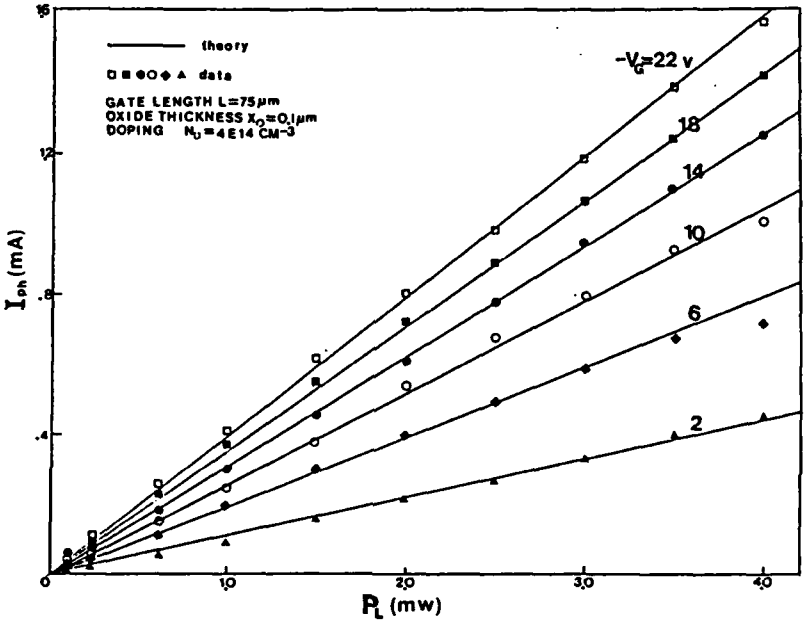

Fig. 6. Photocurrent I_{ph} versus optical power P_L, V_G as a parameter, for 75 μm gate length GCPD.

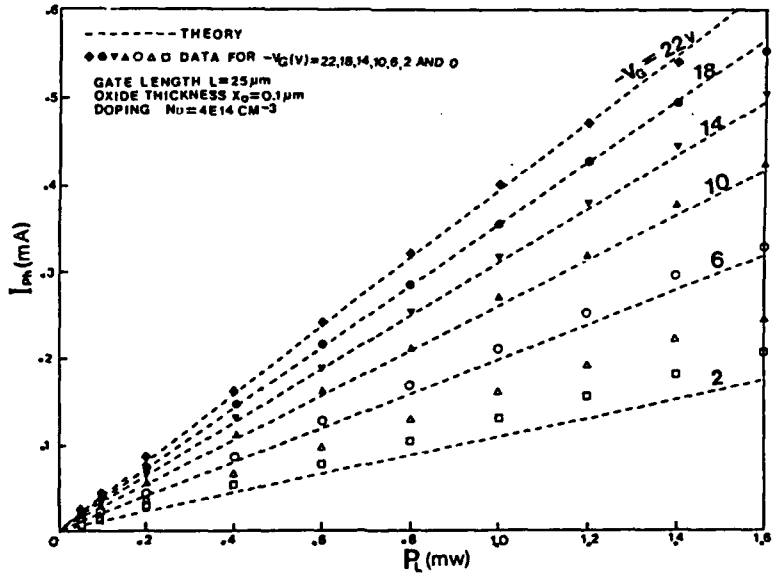

Fig. 7. Photocurrent I_{ph} versus optical power P_L, V_G as a parameter, for 25 μm gate length GCPD.

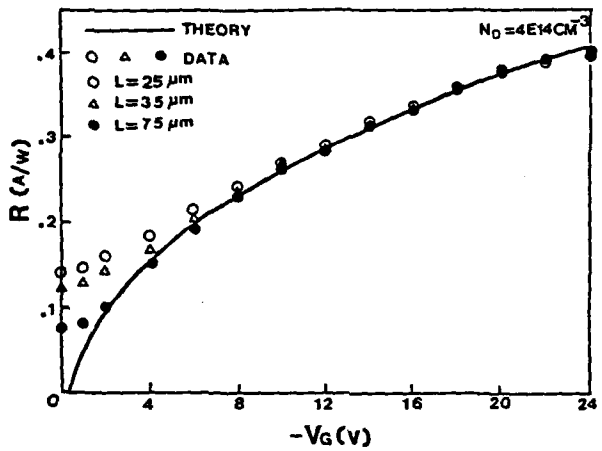

Fig. 8. Responsivity R versus gate voltage V_G for different gate length GCPD's.

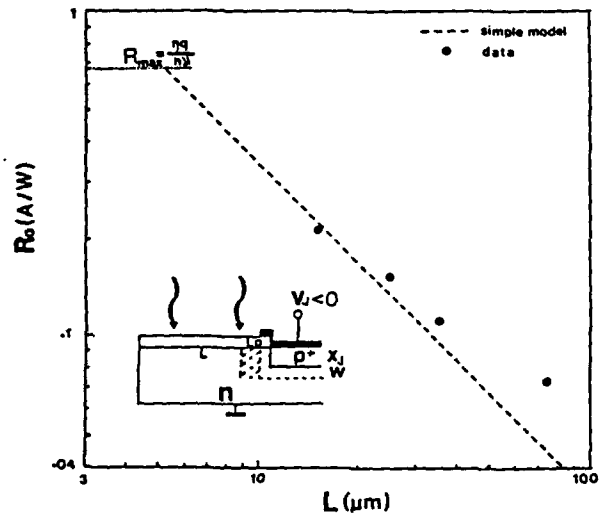

Fig. 9. Comparison of the experimental data of R_0 to the the calculated curve based on the simple model shown in the insert.

Here, $A_s = L$. Thus,

$$I_{ph,0} = \frac{\eta q}{h\nu} \cdot \frac{L_p(X_j + w)}{L \cdot d} \cdot P_L$$

and

$$R_0 = \frac{I_{ph,0}}{P_L} = \frac{\eta q}{h\nu} \cdot \frac{L_p(X_j + w)}{L \cdot d}. \qquad (14)$$

Taking $L_p = 5\ \mu m$, $X_j + w = 12\ \mu m$, we obtain the curve of R_0 versus L, shown in Fig. 9. The experimental data, plotted as solid circles, are in agreement with the theoretical curve.

Fig. 10 shows a plot of I_{ph} versus V_G, with P_L as a parameter, for $L = 25\ \mu m$. The linearity of the experimental data, for both I_{ph} versus P_L and I_{ph} versus V_G, has been determined based on the data. Using the method of least squares, we find straight lines which are able to fit the

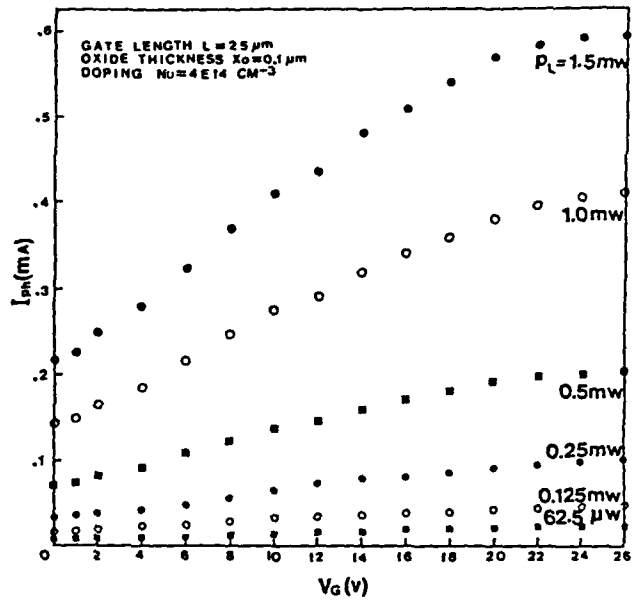

Fig. 10. Photocurrent I_{ph} versus gate voltage V_G, optical power P_L as a parameter. Gate length $L = 25\ \mu m$.

experimental data best, and then calculate the deviations of the experimental data from these lines. For 15 and 25 μm gate-length samples, within the ranges of the light intensity I_0 from 2 to 2000 mW/cm^2, and V_G from 0.1 to 20 V, the mean relative deviation is less than 3 percent for both the relationships of I_{ph} versus P_L and I_{ph} versus V_G. For 35 and 75 μm gate-length samples, the mean relative deviations are 3.8 and 5.5 percent, respectively.

In the case of thermally generated carriers, when the surface is depleted, recombination-generation centers at the oxide-silicon interface provide yet another contribution to the total generation current. There is a sharp jump in the total thermally generated current versus gate voltage characteristics [5]. However, no such leap in the I_{ph} versus V_G characteristics has been observed for the $\lambda = 0.84\ \mu m$ light incident on the Si GCPD (see Fig. 10).

C. Response Time

Both optical and electrical response times of GCPD samples were measured. Here, following [9], the rise time is defined as the time within which the electrical output of the GCPD (i.e., $-I_{ph}R_0$ in Fig. 5) reaches the $e - 1/e$ ($= 0.63$) of its maximum value for an optical or electrical square pulse input, while the decay time is defined as the time after which the output of the GCPD decays to the $1/e$ ($= 0.37$) from its maximum value. In our experiment, the decay time is equal to the rise time approximately.

Fig. 2 shows the experimental data of optical response time (solid circles and triangles) for GCPD devices with different gate lengths on both n- and p-type substrates. Obviously, the response time depends on the minority carrier mobility and the gate length. For longer gate de-

vices, the experimental data are closer to the calculated time-constant curves based on diffusion.

Generally speaking, the transverse electric field is weak in a GCPD, as discussed previously. From the result of diffusion analysis given in (11), we expect τ_d to be proportional to L^2. This result is confirmed experimentally for devices with $L > 20$ μm as shown in Fig. 2. In order to increase the transverse electric field, devices with stepped gate oxide have been made. Experimentally measured τ of a stepped gate oxide device is shown in Fig. 2 with $L = 15$ μm. The gate oxide has three steps, 400, 2200, and 4000 Å thick. The measured time response is 10 ns. If $L = 7.5$ μm is used, and if the device is made on a p substrate, taking advantage of the higher mobility of the electrons, 1 ns time response may be achievable.

Fig. 2 also shows the experimental data of the electrical response time (hollow circles and triangles). In this case, the optical power is kept constant while the gate voltage is in the form of electrical square pulses. Significant differences between electrical response and optical response may be observed only for 15 μm gate length samples. This difference is attributed to the additional RC time constant which is used to establish the depletion region. This RC time constant should be added to the carrier transit time. Hence, the response time of the electrical pulse is greater than that of the optical pulse. In the GCPD's with n^--n^+ or p^--p^+ epitaxial substrates, the RC time constants are on the order of several ns. For GCPD devices with optical response times greater than a 100 ns, this difference cannot be observed.

D. Dynamic Range

The dynamic range of V_G of a GCPD will be limited by the saturation of R at large negative gate voltage at the upper end and by the nonzero R at V_G near zero at the lower end.

In the depletion approximation, the maximum value of the depletion depth X_d is given by [2]

$$C_{d,max} = \left(\frac{2\epsilon_s \epsilon_0 |V_J + 2\phi_F|}{qN_D} \right)^{1/2}.$$

The gate voltage at which X_d reaches this value is defined as the inversion voltage V_T. The starting point of depletion under the gate oxide is at $V_G = V_{FB}$. Hence, (12) is valid only within the range of V_G given by

$$|V_{FB}| \leq |V_G| \leq |V_T|$$

where V_T is a function of V_J. In principle, this range may be defined as the ultimate limit of the dynamic range of V_G.

For the upper limit, as V_G reaches V_T, V_G can no longer control X_d. R will be saturated at $V_G = V_T$. The calculated curves of R versus V_G, using V_J as a parameter, and the experimental measurements are shown in Fig. 11. Basically, the experimental data agree with the above prediction. However, it is apparent that the experimentally measured R continues to increase at gate voltages which are more negative than the calculated V_T. For example, for the 25 μm gate-length sample, the calculated V_T is -22.5 V for $V_J = -20$ V, but R is absolutely independent of V_G only for $V_G \lesssim -40$ V.

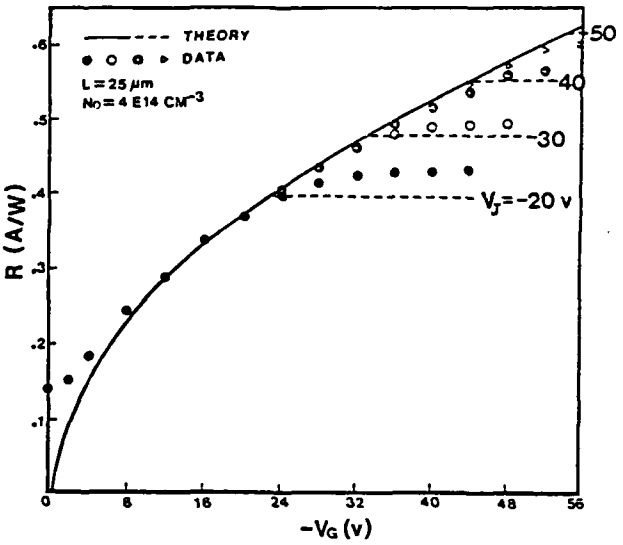

Fig. 11. Responsivity R versus gate voltage V_G for different junction voltages.

On the other hand, for the lower limit, the flat-band voltage V_{FB} has been determined to be -0.3 to -0.5 V by C-V measurement. Usually, X_d is considered to be zero at $V_G = V_{FB}$. However, we have observed a photocurrent at $V_G = 0$, as discussed in Section IV-B.

V. Potential Applications

Within the range of V_G where X_d is approximately linearly dependent on V_G, the GCPD is, in effect, a multiplier of P_L and V_G. Thus, an optical matrix–vector multiplier based on a GCPD array may be obtained [1]. Furthermore, such a 2-D GCPD array may serve as a building block for other optical processors, such as a matrix inverter.

A 2-D GCPD array may be used for matrix–vector multiplication as follows. Consider the 2-D array shown in Fig. 12, which consists of $N \times N$ GCPD's. At each row, the p^+ doped regions of adjacent GCPD's are interconnected to each other via a p^+ collector bar. We may consider the N GCPD's in a row as one total unit with N separate gates which are controlled by N gate voltages $V_{G,j}$. The output photocurrent of this total unit is proportional to $\Sigma_{j=1}^{N} P_{L,j} V_{G,j}$ where $P_{L,j}$ is the optical power incident on the jth GCPD. There are thin gate-oxide layers over each gate region and thick-oxide layers between adjacent gates in different rows. At each column, the same poly-Si gate strip is deposited over both the thin oxides and the thick oxides. The same voltage $V_{G,j}$ is applied to the poly-Si gate strip. $V_{G,j}$ induces depletion layers that have the same thickness under all the gates in the same jth column. The thick-oxide layers are thick enough so that there are essentially no depletion layers formed under

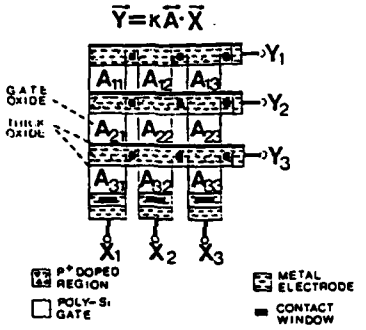

Fig. 12. A top view of the proposed GCPD matrix-vector multiplier.

the thick-oxide layers in the normal operating range of the gate voltage. Let A_{ij} be the optical intensity incident on the GCPD at the ith row and the jth column and let X_j be the gate voltage applied to the jth column. Let Yi be the total photocurrent in the ith row. If $\overleftrightarrow{A}$ is the 2-D optical input, $\vec{X}$ is the input vector, represented by the gate voltages, then $\vec{Y}$ is the product vector, i.e.,

$$\vec{Y} = \overleftrightarrow{KA} \cdot \vec{X}$$

where K is a constant of proportionality. Thus, the GCPD array is capable of performing the basic matrix-vector multiplication operations. This multiplication operation is performed with the response time τ of a single GCPD.

A major feature of a GCPD matrix processor is its high parallelism. In such a processor, the signal detection, multiplication, and addition are carried out simultaneously. The interconnection of the various GCPD's for obtaining the summation of photocurrents in a row and applying the identical V_G to all the devices in the same column is extremely simple. Thus, a large array can be fabricated in a fairly simple manner. These two features might allow operations to be carried out with high speed on large matrices.

The GCPD array might also be used as nonmatrix processors, such as a generalized crossbar switching network.

VI. Conclusion

A new semiconductor device, the gate-controlled photodiode, has been experimentally demonstrated. In this device, the gate voltage V_G controls the depletion depth X_d and modulates the photocurrent. Thus, in the linear region, its photocurrent is proportional to the product of the gate voltage and the light intensity. Based on the depletion approximation and a one-dimensional model, a simple device model has been presented. The experimental data agree with the theoretical predicted performance based on this simple model.

By choosing the proper doping concentration and lifetime of the carriers in the substrate and the oxide thickness, GCPD samples with 10 ns response time and nonlinearity of less than 3 percent within 30 dB range of light intensity and within 23 dB range of gate voltage have been obtained. The response speed, the linearity, and the dynamic range may be improved in the future by further optimizing the design of the GCPD. For example, the nonuniform doping profile may be utilized to improve the linearity of the dependence of I_{ph} on V_G. On the other hand, it is also possible to design a GCPD structure that has more enhanced nonlinear characteristics.

A 2-D GCPD array may be used in some applications such as matrix inversion to serve the function of the 2-D SLM and the photodetector array. It has a higher speed than that of presently available 2-D SLM's. It may play an active role in optical signal processing and computing.

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A-HETEROJUNCTION AND DIELECTRICALLY INSULATED GATE InP FIELD EFFECT TRANSISTORS*

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Experimental data are presented on d.c. drain current instabilities in depletion mode insulated gate InP field effect transistors (D-MISFETs). d.c. drain current decay with time exhibited by InP MISFETs represents impediment to their use. New data presented here suggest that the models proposed to account for this instability may have to be revised. The construction and properties of a different type of device employing semi-insulating $In_xAl_{1-x}As$ as the gate insulator is described. It is shown that such heterojunction insulated gate field effect transistors have none of the d.c. instabilities associated with MISFETs and that they provide good prospects for applications which require high frequency and high power performance.

1. INTRODUCTION

Major advantages of III–V compound semiconductors are their electron mobilities and peak electron velocities which, in many binary and ternary alloys, are considerably larger than those of silicon[1]. Substantial scientific and technological efforts have been applied to the development of III–V compound semiconductor technologies similar to that of silicon metal/oxide/semiconductor technology. Silicon's native oxide, SiO_2, behaves as a near-ideal dielectric material, making it eminently suitable as a gate insulator in field effect transistors, and provides an advantage not available for III–V compounds investigated thus far. Instead, synthetic insulators deposited or plasma anodized have been and are continuing to be developed for these compounds. The quality of the resultant insulator–semiconductor interfaces is determined primarily from measurements made on two-terminal capacitors and three-terminal metal/insulator/semiconductor field effect transistors (MISFETs)[2–4].

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Relatively early in the search for gate insulators compatible with GaAs MISFETs, it became apparent that there are serious problems associated with Fermi level pinning near the midgap at insulator–GaAs interfaces. High interface state densities prevent Fermi level displacement over more than 0.4 eV within the lower half of the fundamental band gap and prevent either accumulation or inversion in such structures. In contrast, the equilibrium surface Fermi level of InP in the absence of an externally applied gate voltage is in the vicinity of its conduction band. Its interface density is about one order in magnitude smaller near midgap than that of GaAs and its Fermi level can be displaced over most of its band gap. With suitable synthetic gate insulators, accumulation as well as inversion can be achieved with InP metal/insulator/semiconductor structures[5].

In recent years, substantial progress worldwide has been achieved in the evolution of discrete[6,7] and integrated circuits[8–10] using depletion (D), accumulation (A) and inversion (I) mode InP MISFETs. A-MISFETs have been made by taking advantage of the specific properties of semi-insulating (SI) InP which allows accumulation of its surface by a positive applied gate voltage. With source and drain contacts produced by ion implantation of donors into SI InP substrates, and with synthetic gate insulating layers such as SiO_2 or In_3PO_4 deposited on it by vapor phase transport, simple electrode metalization procedures can then be employed to make MISFETs which are well suited for digital as well as analog monolithic circuit integration.

However, a serious problem encountered with both A- and I-MISFETs is the d.c. stability of their transistor parameters[11]. It is manifested as a monotonic decrease in channel current with time while d.c. potentials are applied between the source and drain electrodes, and between the gate and source electrodes. Methods to circumvent or at least minimize this problem have been attempted and, as yet, there is no fully documented or reproducible evidence that the d.c. instability can be considered negligible for most purposes. This failure points to an incomplete understanding of the origin of this problem. A number of mechanisms have been proposed[12–17], most identifying electron trapping into localized electron energy levels as a key element, with differences in the proposed location of the traps and the capture–emission processes.

To learn more about the nature of these d.c. instabilities associated with InP MISFETs, we investigated the properties of a D-MISFET. We expected to find much smaller instabilities in such structures because the InP channel is separated from its insulator interface by a depletion region. Instead we found fairly substantial instabilities, comparable in most respects with those observed on A-MISFETs and I-MISFETs. These observations are described in the following section.

To explore alternatives intended to provide d.c. stable field effect transistors with insulated gate characteristics, we also investigated the feasibility of heterojunction-based InP MISFET-like structures and describe them in the following sections. We find that such devices are d.c. stable and that they may have some significant advantages compared with those made heretofore, based on synthetic dielectric gate insulators.

2. DEPLETION MODE MISFETS

D-MISFETs were made of InP epitaxial layers grown by low pressure organometallic chemical vapor deposition on SI InP (100)-oriented substrates. These epilayers, nominally 0.5 μm thick, were not doped; they have electron densities of the order of 10^{16} cm^{-3} and typical mobilities of 3×10^3 cm^2 V^{-1} s^{-1}. Transistor fabrication began with etching isolation mesas using a 10% solution of iodic acid. Next, ohmic contacts for the source and drain were formed by the vacuum deposition of AuGe–Ni, which were then alloyed at 375 °C in forming gas for 15 min. Thereafter, an indirect plasma-assisted vapor transport process was used to deposit SiO_2 as the gate insulator at a substrate temperature of 300 °C and an aluminum gate was then vacuum deposited on it. The transistor configuration is shown in Fig. 1. It consists of a split gate, a source-to-drain spacing of 8 μm, a gate length of 6 μm and a width of 250 μm.

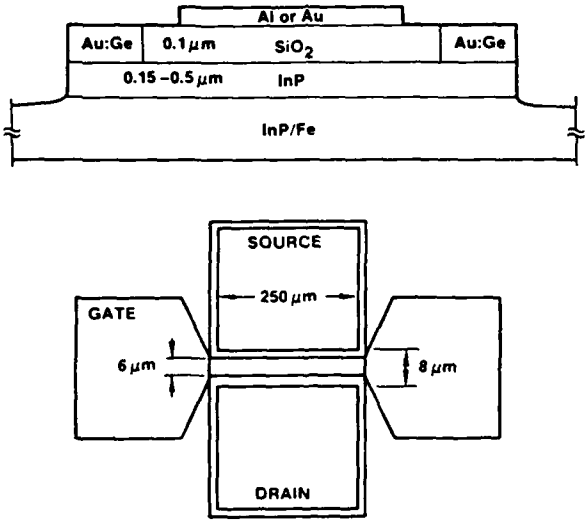

Fig. 1. Cross-section and top view of InP D-MISFETs investigated in this work.

Preliminary indications of instabilities associated with such D-MISFETs were obtained from observations made on a Tektronix-type 576 curve tracer; the transistor current *vs.* voltage (I–V) characteristics decayed with time as shown in Fig. 2. Measurements made of the drain current d.c. bias voltages applied to the drain and to the gate revealed a logarithmic channel current decay with time such as that shown in Fig. 3. Some drift of the drain current was found to exist even after an elapsed period of 36 h with constantly applied bias potentials.

Furthermore, we found an additional type of instability not reported previously. Following its d.c. drain current decay, the D-MISFETs appear to recover only partially to their original drain current values after a period in which the transistor is stored without any potentials applied to it. Figure 4 shows a

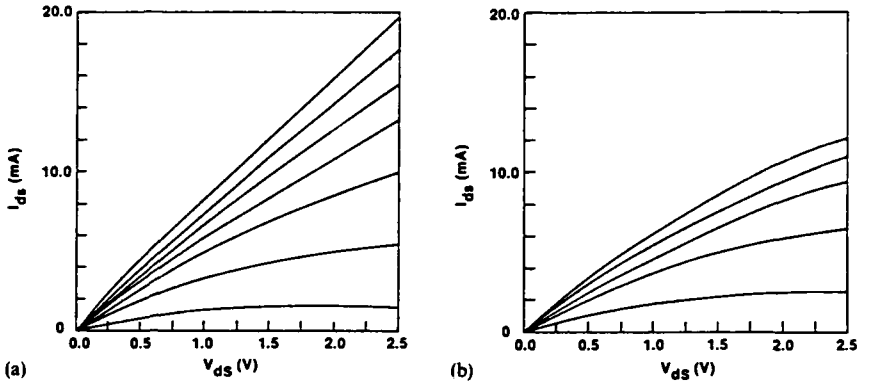

Fig. 2. Drain current decay with time of a representative InP D-MISFET observed on a Tektronix 576 curve tracer; gate voltage steps are 2 V increments: (a) initial characteristics; (b) results 1 h later; the MISFET was cycled continuously on the curve tracer during this interval.

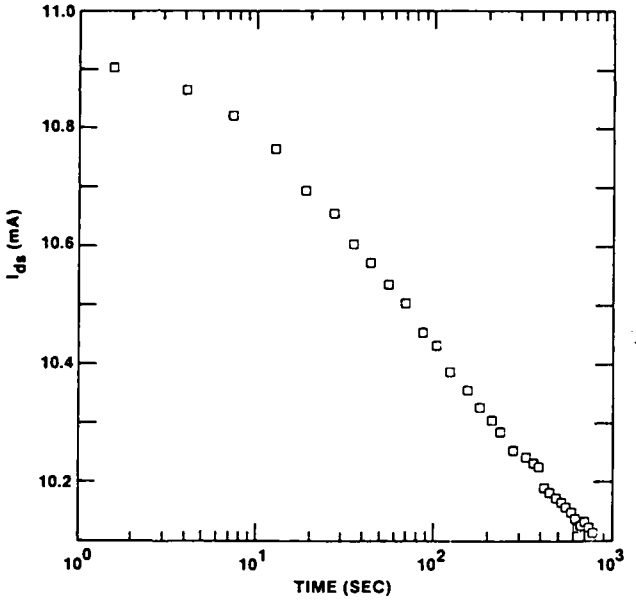

Fig. 3. Channel current *vs.* time for a D-MISFET with gate bias magnitude one-quarter of that needed to pinch off the channel. The change in drain current within 10 min is about 7%.

representative example of such an incomplete recovery with resumption of the logarithmic drain current decay after a wait of 24 h between measurements. It suggests a charge storage mechanism and a memory effect similar to that observed on metal nitride/oxide silicon structures. Attempts to accelerate the recovery of drain current in D-MISFETs by application of a positive rather than a negative gate voltage, thermal or optical incident radiation have not been successful thus far. We

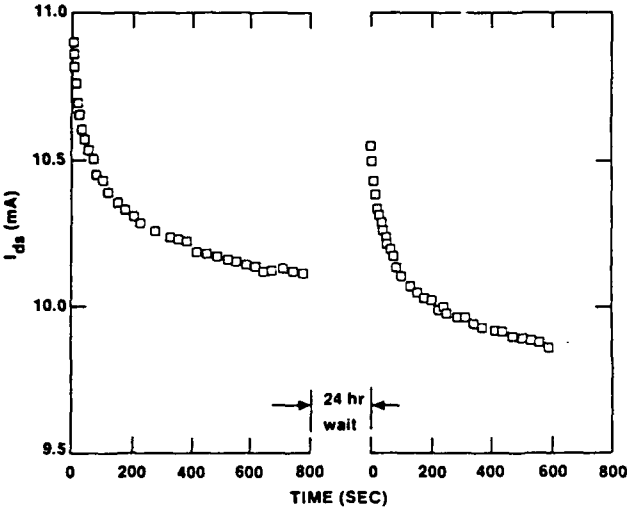

Fig. 4. Repeated measurements made on an InP D-MISFET; drain current *vs.* time with 24 h interval between measurements in which no potentials were applied to the MISFET shows incomplete recovery of the transistor drain current to its original value.

obtained, in fact, similar results with A-MISFET and conclude that these effects may be generic in character.

These observations indicate that the drain current decay mechanism might be more complex than the models proposed thus far. It is particularly surprising that the drain current decays irrespective of the polarity of the applied gate voltage. The cause for the decay might be injection of electrons from either the metal gate electrode or the InP channel into the insulator where they are trapped. The resultant time-dependent stored charge in the gate capacitance would reduce the effective surface potential acting on the MISFET channel.

In any case, the properties of the insulator and of the insulator–InP interface are crucial for optimizing MISFET characteristics. Although substantial improvements, including a reduction in the d.c. instability, have been obtained by post-annealing treatment and densification of the insulator[18] or by the use of phosphorus[19,20] or arsenic[21] during its vapor phase deposition, no completely satisfactory solution has emerged. We considered and describe here a different approach, in which the gate insulator and channel comprise a highly asymmetric heterojunction but retain many of the specific characteristics of MISFETs.

3. HETEROJUNCTION-INSULATED GATE FIELD EFFECT TRANSISTORS

Prototype depletion mode heterojunction-insulated gate field effect transistors (HIGFET) were made by replacing gate insulating layers of InP MISFETs with $In_xAl_{1-x}As$ layers grown at this time by modular beam epitaxy, on n-type epitaxial InP layers, 0.1–0.5 μm thick, which had been previously grown by organometallic chemical vapor deposition on SI InP (100)-oriented substrates. $In_{0.43}Al_{0.57}As$

layers grown at nominal substrate temperatures of 500 °C are essentially semi-insulating and, for thicknesses of less than 0.1 μm, are fully depleted of charge carriers. HIGFET fabrication using these epilayers started with etching a mesa isolation pattern using 1 H_3PO_4: 1 H_2O_2: 38 H_2O, which etches $In_xAl_{1-x}As$ at a rate of 0.1 μm min^{-1} and 1 HCl: 1 CH_3COOH which etches InP. The location of source and drain pads was etched with the same phosphoric acid etch and corresponding electrodes made of eutectic AuGe–Ni were alloyed to the InP channel. Gate electrodes were made by optical photolithographic processing of a vacuum-deposited aluminum layer on the $In_{0.43}Al_{0.57}As$ gate insulator. The device geometry is the same as that used to make the D-MISFETs.

Among the advantages of $In_{0.43}Al_{0.57}As$ used as a quasi-insulator for the transistor gate are its high Schottky barrier (about 1.2 eV) and low gate leakage current (less than 0.1 μA for a reverse gate bias of −4 V), such as that required to pinch off the channel of the D-HIGFET. Low frequency characteristics of a representative HIGFET are shown in Fig. 5. The extrinsic transconductance g_m of such prototype devices with their relatively large dimensions and low electron density of the InP channel (4×10^{16} cm^{-3}) is somewhat low ($g_m = 20$ mS mm^{-1}). We estimate that, by reducing the gate length to 1 μm and increasing the electron density in the channel to 10^{17} cm^{-3}, the transconductance of such devices may reach $g_m > 150$ mS mm^{-1}.

The d.c. stability of HIGFETs was measured by applying d.c. gate and drain

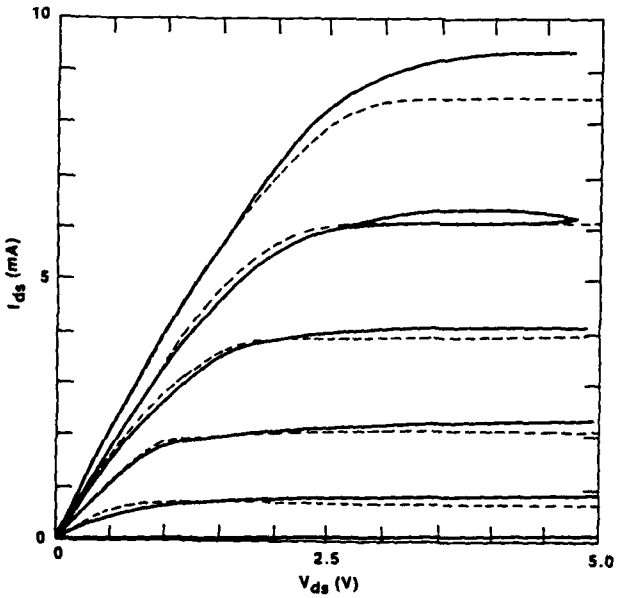

Fig. 5. *I–V* characteristics of a HIGFET: ---, calculated curves using Hill's model. Bulk parameters were used for the InP ($d = 0.18$ μm, $N_d = 4.5 \times 10^{16}$ cm^{-3}, $\mu = 3 \times 10^3$ cm^{-2} V^{-1} s^{-1}, $v_{sat} = 2.5 \times 10^7$ cm s^{-1}) and $In_{0.43}Al_{0.57}As$ ($\varepsilon = 12.5$); the series resistance is about 180 Ω and the interface state density is about 4×10^{11} cm^{-2} eV^{-1}.

potentials while monitoring the drain current as a function of time. Figure 6 shows the results of some of these measurements and, from these data, as well as from other similar measurements made over much longer time periods, we conclude that the D-MISFET instabilities described in the previous section are absent in such HIGFETs.

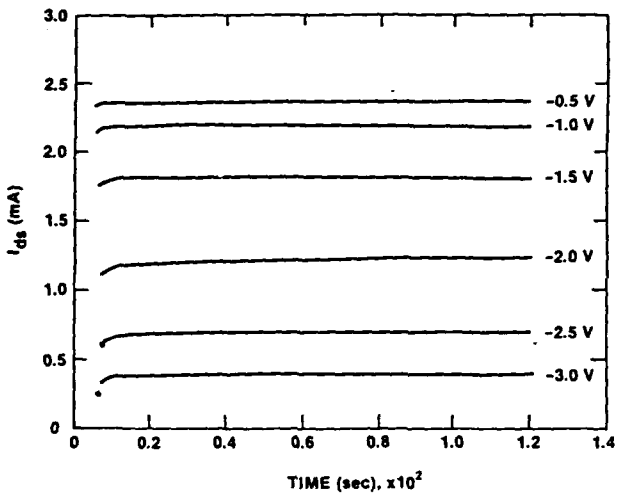

Fig. 6. Channel current *vs.* time of a HIGFET during first 2 min after d.c. potentials were applied to it. Measurements for longer time periods indicate continued d.c. stable operation.

It remains to be seen whether the same performance advantages can be obtained on the enhancement mode HIGFET and whether the expected increase in g_m by downscaling its geometry and increasing its active channel doping will lead to an increase in their gain–bandwidth product.

4. DISCUSSION

Among the issues which require further consideration are the similarities and differences between MISFETs and HIGFETs. We have found it possible to apply a model, such as Hill's, developed explicitly for MISFETs[22], to analyze and fit low frequency data as shown by the overlaid broken lines on the transistor characteristics in Fig. 5. Implicit in the use of this model is the assumption that the HIGFET gate capacitance can be represented in terms of a conventional insulator, whose composition-dependent dielectric constant is linearly interpolated between those of InAs and AlAs.

Measurements made on two-terminal $In_{0.43}Al_{0.57}As$–InP capacitors, which will be reported elsewhere[23], indicate that, to first order, the InP epilayer is slightly depleted; for $V_g = 0$ V, its equilibrium surface potential is $V_s = -0.05$ eV. The $In_{0.43}Al_{0.57}As$ layer is completely depleted and a negative interface state density between them is of the order of $10^{11}\,cm^{-2}\,eV^{-1}$. The conduction band edge

discontinuity is unknown but might be slightly larger than that of the lattice matched heterojunction whose conduction band discontinuity is reported to be $\Delta E_c = 0.52$ eV. The high aluminum content of the $In_xAl_{1-x}As$ layer, whose lattice constant is mismatched relative to InP, creates a large tensile strain which is not accommodated by a pseudomorphic elastic deformation; lattice defects are created at the interface which relieve the local stress; etching the 0.1 μm layer which appears to contain no surface morphological defects confirms their presence within approximately 400 Å of the interface. Their role and connection with interface trapping centers has not been determined as yet. Preliminary evidence suggests that, although interfacial defects can be reduced by reducing the aluminum concentration in the $In_xAl_{1-x}As$ layers while approaching the lattice matched composition, this is obtained at the expense of the Schottky barrier height and the gate leakage current.

High frequency and possibly high power HIGFETs might be obtained using $In_xAl_{1-x}As$–InP heterojunctions by a judicious choice of the material parameters. The higher thermal conductivity of InP and the considerably higher threshold field for electron transfer from the conduction band minimum to its upper valley compared with GaAs, the larger ΔE_c of this system compared with GaAs–$Ga_xAl_{1-x}As$, makes such heterojunctions of particular interest for sub-micrometer-size field effect transistors and integrated circuit applications.

5. CONCLUSIONS

The mechanism or mechanisms involved with channel current drift in InP MISFETs appear to be either suppressed or eliminated in InP HIGFETs. Such devices may have high frequency and microwave and power handling properties comparable with or superior to those employing synthetic dielectric layers. If the same method of synthesis were used for depositing the InP channel, as well as the gate quasi-insulator, then a number of processing steps currently used in the fabrication of such transistors would be eliminated. Although adequate for many applications, a more reliable and consistent method of synthesis of high quality $In_xAl_{1-x}As$ layers grown on InP, with a lower interface state density than the 10^{11} cm^{-2} eV^{-1} obtainable at this time, is considered desirable.

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$In_xAl_{1-x}As/InP$ Heterojunction Insulated Gate Field Effect Transistors (HIGFET's)

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$In_xAl_{1-x}As/InP$ Heterojunction Insulated Gate Field Effect Transistors (HIGFET's)

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Abstract—**Stability problems in conventional InP metal-insulator-semiconductor field effect transistors (MISFET's) have been overcome in InP heterojunction insulated gate FET's (HIGFET's) by replacing the insulator with $In_xAl_{1-x}As$. We report on the fabrication and low-frequency operation of the HIGFET with a composition of $x = 0.43$. Transistor characteristics have been successfully modeled by an analytical MISFET model which indicate a low interfacial state density ($\cong 10^{11}/cm^2$) and near flat-band condition.**

THE transconductance g_m and the gain-bandwidth product f_t of field effect transistors (FET's) are strong functions of the electric field-dependent velocity $v(E)$ of the charge carriers. In the linear v versus E region, the mobility of InP is smaller than that of GaAs. However, as shown in Table I [1], the conduction-band intervalley gap Γ–L of InP is greater than that of GaAs; InP has a higher peak velocity and a correspondingly higher threshold for electron transfer from the center of the Brillouin zone to the subsidiary L minima and it also has a higher thermal conductivity than GaAs. Although the low surface barrier height of n-type InP makes this material unsuitable for metal–semiconductor FET's (MESFET's), its favorable surface and bulk properties provide the basis for metal–insulator-semiconductor FET's (MISFET's). If the surface chemical preparation of InP prior to growth of a compatible gate insulator is under adequate control, then its fast surface state density can be reduced to the order of $10^{11}/cm^2$-eV and the Fermi level can be displaced by an applied gate voltage V_g over most of the fundamental bandgap E_g. However, such gate insulators and their dielectric–InP interfaces are far from ideal. Fast surface and interface states reduce g_m and f_T and may introduce a frequency dispersion of MISFET parameters; slow states and interfacial tunneling of charge carriers produce low-frequency hysteresis and drift of the drain current [2]. These detrimental effects must be eliminated if InP MISFET's are to compete successfully with GaAs-based discrete and integrated circuit devices.

We describe here an InP heterojunction insulated gate FET (HIGFET) which circumvents many of these problems by substituting the gate insulator with an undoped depleted

TABLE I
COMPARISON OF SOME InP AND GaAs MATERIAL PARAMETERS

	PARAMETER	InP	GaAs
1	Γ–L valley separation	0.54 eV	0.33 eV
2	Impact ionization threshold	2.10 eV	1.70 eV
3	Threshold field for intervalley electron transfer	11 kV/cm	3.6 kV/cm
4	Peak electron velocity	2.7×10^7 cm/s	2×10^7 cm/s
5	Thermal conductivity (300K)	0.83 W/cm-K	0.52 W/cm-K
6	Drift mobility (300K, $n=1\times10^{17}/cm^3$)	3×10^3 cm^2/V-s	5×10^3 cm^2/V-s
7	Fundamental bandgap (300K)	1.34 eV	1.42 eV

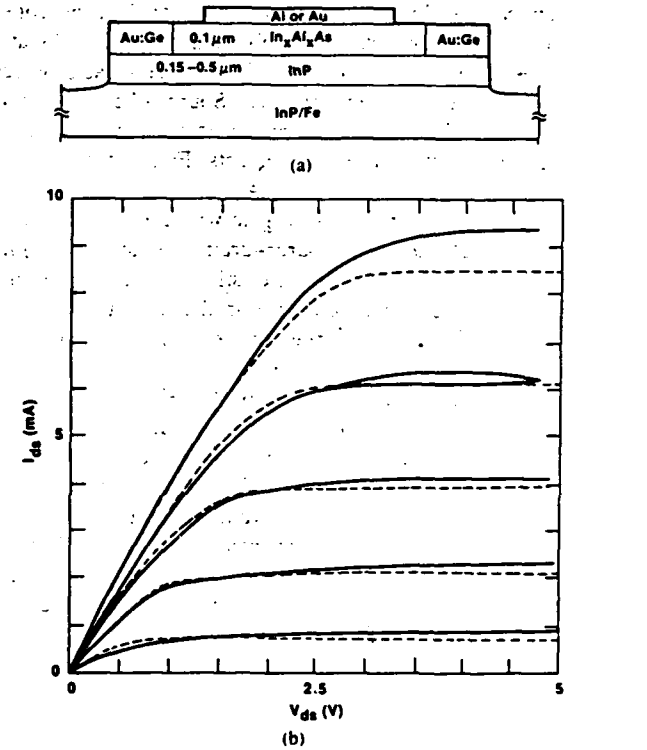

Fig. 1. (a) Cross section of heterojunction insulated gate transistor. (b) Low-frequency transistor characteristics of a prototype depletion-mode HIGFET. Solid lines represent experimental data; dashed lines represent calculations following Hill's model [5]. Parameters used were: InP thickness of 0.18 μm; electron density = $4.5 \times 10^{16}/cm^3$; $v_{sat} = 1.5 \times 10^7$ cm/s; $\mu = 3000$ cm^2 V·s; In_xAl_{1-x}. As thickness of 0.1 μm; interface density of $4 \times 10^{11}/cm^2$; surface potential = −0.05 eV; series source and drain resistance both = 90 Ω.

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$In_xAl_{1-x}As$ layer grown by molecular beam epitaxy (MBE). We have chosen $x = 0.43$ because this ternary alloy has a large barrier height $\phi_b = 1.2$ eV and a fundamental bandgap $E_g(300\text{ K}) = 1.62$ eV, while the lattice matched alloy $x = 0.52$ has $\phi_b = 0.8$ eV and $E_g(300) = 1.46$ eV [3].

Prototype HIGFET's with typical transistor-like characteristics, such as that shown in Fig. 1, exhibit negligible dc channel current drift as shown in Fig. 2, in contrast with many conventional MISFET's which have a logarithmic time-dependent dc drain current drift and decay to 50 percent and more of their initial value within 10 min [2]. Preliminary investigations suggest that the dc drain current is stable for periods on the order of hours. Such investigations are still underway.

HIGFET's were made by growing 0.1–1-μm thick epitaxial InP layers with typical electron densities between 2 and $5.10^{16}/cm^3$ on (100)-oriented semi-insulating InP substrates using low-pressure metal organic chemical vapor phase deposition. The InP epilayers were cleaned with organic solvents and lightly etched to remove native oxide before loading into a modified Varian Gen II MBE System. Residual surface oxide was removed by a standard *in-situ* heating prior to the growth of undoped $In_xAl_{1-x}As$, essentially semi-insulating, 0.1 to 0.2 μm thick. Transistor mesas were formed by chemically etching with 1 phosphoric acid :1 hydrogen peroxide :38 H_2O which selectively etches $In_xAl_{1-x}As$ at a rate of $\sim$1000 A/min [4] and 1 HCl:1 acetic acid which selectively etches InP very rapidly. Source–drain windows were opened with the same phosphoric acid etch to expose the InP and AuGe eutectic used for contacts. Finally the gate was defined and metallized with Al or Au.

The device geometry is a split gate with a gate length of 6 μm, width of 282 μm, and source–drain separation of 8 μm. Low-frequency transistor characteristics are shown in Fig. 1(b); the extrinsic transconductance in the saturated region is 20 mS/mm. With ∓ 10 V applied between the gate and source the leakage current is less the 1 μA.

The one-dimensional MISFET model of Hill [5], which is a two-piece approximation adapted from models developed by Pucel *et al.* [6] and Lile [7], was used in conjunction with the parameters given in the caption of Fig. 1(b) to fit qualitatively the experimental data. Estimated value of total series resistance is 180 Ω from which an intrinsic $g_m = 31.5$ mS/mm is calculated. We have ignored to first order the conduction-band offsets between InP and $In_{0.43}Al_{0.57}As$; the composition dependence of the band offsets of $In_xAl_{1-x}As$ are not known as yet except for the composition of $x = 0.52$ whose lattice constant matches that of InP and which has a staggered band-edge discontinuity with a 0.52-eV conduction-band offset and a 0.40 eV valence-band offset [8]. We assume that in our case the InP surface is nearly at flat band; relatively few misfit dislocations generate interfacial charge, however, its magnitude is not considered sufficient to pin the surface Fermi level.

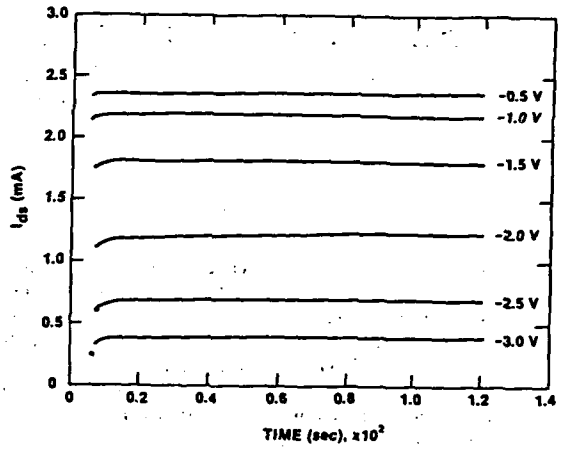

Fig. 2. DC drain current versus time for various gate voltages from 0 to -2.5 V in -0.5-V steps. Source–drain voltage is 0.5 V.

Acknowledgment

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Sidegating in GaAs Current Limiters

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Sidegating in GaAs Current Limiters

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Abstract—**Potentials of several volts or less applied to the sidegate contact of an ion-implanted GaAs current limiter cause a decrease in the channel current, in both the linear and saturated modes of operation. Larger sidegate potentials have the opposite effect due to the addition of a large substrate leakage current, and cause an apparent shift in the impact-ionization threshold of the channel current.**

I. INTRODUCTION

THE PARASITIC interactions between field-effect transistors (FET's) made on semi-insulating (SI) GaAs substrates are of considerable interest. At present they limit the maximum integrated circuit density attainable on this material. The development of a GaAs VLSI technology, promising for high-speed and microwave applications, rests heavily on understanding and eliminating these unwanted interactions. Device interaction in circuits has been simulated experimentally by applying a potential to an injecting "sidegate" contact on a SI GaAs substrate and observing its effect on the operating parameters of a nearby FET made on the same substrate. This sidegate potential has been found to modulate the drain current in the FET, even to the extent of causing pinchoff. It has been proposed that an electron space-charge-limited current flowing in the substrate between the sidegate and the FET alters the potential at the n-type to SI junction formed at the FET channel–substrate interface; this changes the junction depletion width, changing the FET channel cross section and modulating the FET current. This effect is intimately related to the compensation mechanism, involving deep levels, of the SI material [1]–[3].

We have investigated sidegating on a simpler structure, that of the GaAs current limiter, which may be thought of as an "ungated FET" [14]. The current limiter (also called saturated resistor) is used as an active load in logic inverters [5], [6]. It is a two-terminal device made by ion implantation into silicon nitride-capped undoped SI GaAs (Fig. 1). Having no gate eliminates some complications in the investigation of sidegating, such as the effects of gate-voltage and gate-leakage current. The channel, 1 to 2 μm long by 1.5 to 2.5 μm wide, is implanted with a donor concentration on the order of $10^{17}/cm^3$ to a depth of ~ 0.2 μm; the ohmic contacts to the channel, as well as the sidegate contact (not shown) are n^+-implanted to a depth of ~ 0.3 μm and have a AuGe metallization. The sidegate is separated from the channel by ~ 100 μm of SI material. The "back junction" in the figure represents the junction formed at the n-channel to SI substrate interface. The modulation of this junction by the sidegate potential is presumed to produce sidegating in a manner similar to that observed on GaAs depletion-mode metal-semiconductor FET's (DMESFET's).

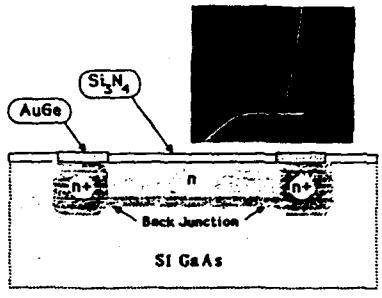

Fig. 1. Cross-sectional view of ion-implanted current limiter structure. Insert is quasi-static current–voltage characteristic of current limiter with 1-μm-long channel for sidegate potential $V_{SG} = 0$ V. Horizontal axis is channel voltage V_{CH} (0.5 V/div.), vertical is channel current I_{CH} (200 μA/div.).

Most measurements were performed on a Tektronix 576 curve tracer in the dc mode. The current-limiter channel voltage V_{CH} was swept manually at a slow rate, and a dc sidegate bias V_{SG} was provided by a separate dc power supply (both V_{CH} and V_{SG} are referenced to ground). Thus, the entire current-limiter current–voltage trace could be obtained quasi-statically for any sidegate bias. For some measurements, the curve tracer was replaced by a dc voltage source, and the channel current I_{CH} monitored through a small series resistor. Temperature dependent measurements were made using a CTI Cryogenics helium refrigeration system. As an aid in characterizing high-field effects, light emission measurements for wavelengths from 6000 to ~ 9300 Å were obtained with a SPEX 1870 0.5-m spectrometer and a RCA 4832 photomultiplier.

The insert in Fig. 1 shows the quasi-static curve-tracer current–voltage curve for a 1-μm current limiter with $V_{SG} = 0$ V. This shows a linear relationship, corresponding to a constant electron mobility region, for $V_{CH} < 1$ V; as V_{CH} is increased, I_{CH} saturates, here at a value of ~ 400 μA. The current saturation occurs when the electric field in the channel becomes large enough to begin velocity saturation of the channel electrons, beyond about 3 kV/

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cm in GaAs [7], [8]. The velocity, and hence I_{CH}, then become essentially independent of V_{CH}. For a 1-μm channel length, one might ideally expect this to occur at $V_{CH} \approx 0.3$ V. Realistically, however, substantial contact resistances, impurity scattering, and other factors may greatly increase the voltage required for saturation, especially in short-channel devices. For higher V_{CH}, 3.7 V in this case, there is a negative resistance (NR) and an abrupt rise in I_{CH}. Such high-field breakdown characteristics are commonly observed on GaAs DMESFET's and are attributed to impact ionization in, or in the vicinity of the channel [9], [10].

II. Results and Discussion

If a negative potential V_{SG} is applied to the sidegate contact, then the channel current has two distinct regions: 1) for V_{SG} several volts or less, I_{CH} decreases noticeably, both in the linear and saturated regimes, compared to its value at $V_{SG} = 0$ V; 2) larger values of V_{SG} cause an increase in the measured I_{CH}, and an apparent shift of the impact-ionization threshold to lower V_{CH}.

The first of these is illustrated in Fig. 2, for voltages less than the negative resistance (NR) threshold, where I_{CH} is plotted versus V_{SG} for (a) $V_{CH} = 100$ mV (linear region) and (b) $V_{CH} = 2$ V (saturated region). The total decrease in I_{CH} in Fig. 2(a) is 15 percent. This may be due to the negative sidegate potential reverse biasing the channel–substrate junction, thereby reducing the channel cross section, such as proposed for GaAs DMESFET's. If V_{CH} is increased, the effect of sidegating is diminished. For instance, in Fig. 2(b) for $V_{CH} = 2$ V (in saturation), the decrease in I_{CH} is less than 5 percent. As V_{CH} approaches the impact-ionization threshold, V_{SG} no longer causes a decrease in I_{CH}. We believe this effect is similar to that observed by Mottet and Le Mouellic on DMESFET's [11], and by Tsironis on both DMESFET's and ungated structures [12], [13]. They found that, even prior to breakdown, the decrease in channel (drain) current caused by the negative sidegate potential was eliminated at high drain-source voltages. Mottet and Le Mouellic attributed this to (prebreakdown) impact ionization in the channel. Tsironis, who did a detailed analysis of "prebreakdown" phenomena, found this compensation of sidegating to be due to an excess current flow caused by low-level impact ionization in the channel-substrate space-charge region and microplasma formation near the drain (positive) contact. This would lead, at higher channel voltages, to the observed breakdown of the device as the microplasmas merged to form large regions sustaining impact ionization. Ideally then, if the current limiter or FET were used only near the impact-ionization threshold, one might eliminate the effect of sidegating. Unfortunately, this is not a very useful mode of operation; the carrier multiplication process associated with this region substantially increases the noise power generated in the device [13].

An alternate explanation for this apparent compensation of sidegating at large channel voltages is given by

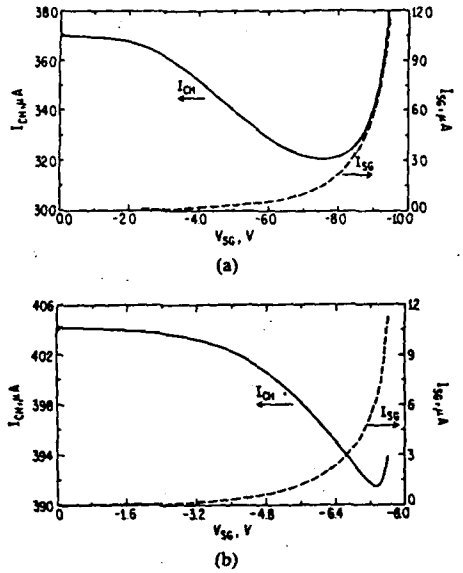

Fig. 2. I_{CH} (solid) and substrate current I_{SG} (dashed) versus V_{SG} for (a) $V_{CH} = 100$ mV (linear region); (b) $V_{CH} = 2$ V (saturated region).

Goronkin and Vaitkus for DMESFET's [14]. They propose that impact ionization of trapped carriers (as opposed to impact ionization of the lattice) eventually leads to the collapse of the channel–substrate space-charge region, a resultant expansion of the channel cross section and an increase in drain (channel) current. It is possible that this mechanism is also applicable to current limiters. It seems unlikely, however, that impact ionization of trapped charge carriers, by itself, can account for the negative resistance (NR) observed in our devices; there are not enough deep levels (traps) in the material to sustain the large currents observed after breakdown. In addition, impact ionization of carriers from traps is unlikely to cause near band-edge light emission such as described subsequently and shown in Fig. 5.

Fig. 3(a) shows the decrease in I_{CH} with V_{SG} as a function of temperature from ~220 to 330 K, for $V_{CH} = 2$ V. It was found that the fractional change in I_{CH} varied only slightly, (e.g., by less than a factor of 2 at $V_{SG} = -5$ V) over this temperature range. The substrate current I_{SG} on the other hand, increased by roughly three orders of magnitude over the same temperature range (Fig. 3(b)). Similar results are evident in the work of Lee and Chang on depletion MESFET's [15]. This indicates that sidegating, as measured by the change in I_{CH}, is essentially independent of the magnitude of the substrate current and suggests that sidegating is not strongly affected by the free carrier concentration in the substrate. The increase in I_{CH} (at any V_{SG}) observed as the temperature is lowered may be attributed, in part, to an increase in the electron saturation velocity v_s. According to the temperature dependence of v_s as measured by Houston and Evans [16], however, the increase in v_s is not by itself sufficient to account for the increase in I_{CH}.

Referring again to Fig. 2, further increasing V_{SG} causes

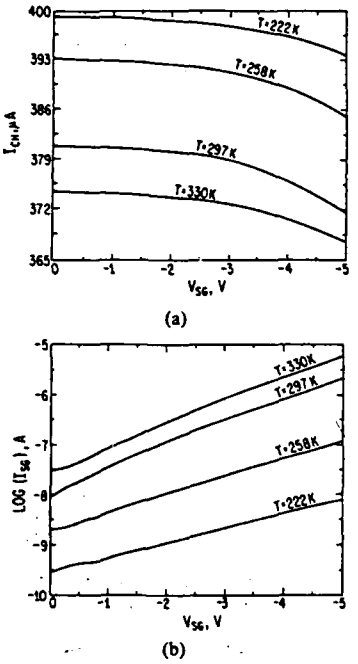

Fig. 3. Effects of temperature on sidegating characteristics: (a) I_{CH} versus V_{SG}; (b) I_{SG} versus V_{SG}. V_{CH} = 2 V. There is nonzero current in (b) at V_{SG} = 0 V since $V_{CH} - V_{SG}$ = 2 V there.

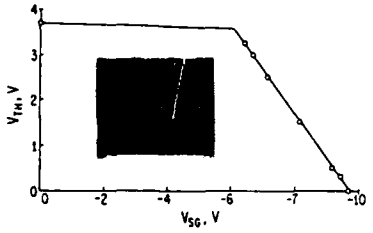

Fig. 4. Apparent impact-ionization threshold V_{TH} versus V_{SG}. Insert is I_{SG} versus V_{SG} for V_{CH} = 0 V. Horizontal scale is −1 V/div., vertical is 1 mA/div.

I_{CH} to level out, then to increase sharply near the NR threshold. The dashed curves in Fig. 2(a) and (b) shows that a sharp rise in the substrate leakage current I_{SG} flowing between the sidegate and the current limiter accompanies the sharp rise in I_{CH}, and the change in I_{CH} is equal to the change in I_{SG}.

Fig. 4 shows that the threshold channel voltage V_{TH}, the apparent impact ionization (NR) threshold in the measured I_{CH}, decreases linearly with V_{SG} when V_{SG} exceeds, in this case, about −6 V, with a slope of −1. This implies that the impact-ionization threshold occurs at a constant potential difference between sidegate and current limiter (just under 10 V here) provided that V_{SG} is greater than a specific threshold value.

This dependence of the apparent impact-ionization threshold V_{TH} on V_{SG}, has been found to result from the substrate leakage current I_{SG}. The decrease in V_{TH} with V_{SG} begins once the potential difference between the current limiter and the sidegate, $V_{CH} - V_{SG} \approx 10$ V for this example. A closer examination shows that I_{SG} also exhibits a NR, and becomes quite large (insert in Fig. 4) if $V_{CH} - V_{SG}$ exceeds ~10 V. One then sees the superposition of the I_{SG} characteristic, with its NR, on I_{CH}. Thus, for large V_{SG}, impact ionization in the channel is preceded by a NR in the substrate and the threshold for channel impact ionization is never reached. In Fig. 4 one actually sees then, the change in channel voltage required to satisfy the condition $V_{CH} - V_{SG} \approx 10$ V, which causes the NR and turn-on of I_{SG}, not a decrease in the threshold for impact ionization in the channel, as it first appears.

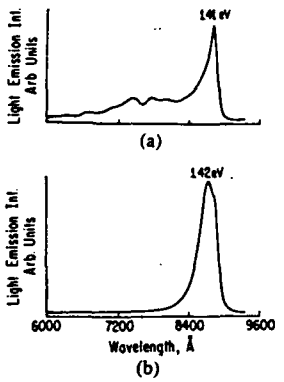

Fig. 5. Light emission spectra: (a) at channel impact-ionization threshold; (b) at substrate breakdown threshold. (Signal "humps" in (a) at wavelengths less than the peak are background.)

Interestingly, when we checked for the white light emission others have observed, both at the impact ionization threshold of the channel [10], [13], [18] ($V_{CH} - V_{SG} < 10$ V, $V_{CH} = 3.7$ V), and at the breakdown (NR) threshold of the substrate current [17], [18] ($V_{CH} - V_{SG} \approx 10$ V, $V_{CH} < 3.7$ V), we observed instead emission in a fairly narrow wavelength region centered about the GaAs bandgap (1.42 eV), as seen in Fig. 5(a) and (b), respectively. We assume that a MESFET emits white light because most of the holes generated by impact ionization in its channel are removed through its gate circuit; this prevents direct radiative band-edge emission such as is produced by a current limiter that might be considered as an ungated MESFET. An "excess" gate current measured in the impact-ionization regime of MESFET's has been attributed to holes [11].

The results of this work show that the effect of sidegating on the GaAs current limiters is very similar to that observed on DMESFET's, as long as the sidegate potentials are not large enough to cause breakdown in the substrate.

Acknowledgment

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NARROW BANDGAP SEMICONDUCTOR DEVICES

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ABSTRACT

A review of past and current research on electronic devices based on the modulation of the surface potential of depletion, accumulation or inversion layers of bulk or thin film elemental or compound semiconductors whose fundamental bandgaps, $E_g < 1$ eV, reveals that the characteristics of the semiconductor-gate insulator interfaces determine, to a large extent, their charge carrier transport properties; in the case of metal-insulator-semiconductor (MIS) structures the energy levels, density and capture cross-sections of interface states as well as the type, density and spatial distribution of traps within the insulator affect their DC drain current stability, their transconductance and their gain-bandwidth products. At this time, semiconductor-quasi-insulator-semiconductor heterostructures have superior properties compared to MIS structures and most of the MIS-related problems are also absent in modulation-doped two-dimensional electron gas heterojunction structures.

INTRODUCTION

A field-effect transistor (FET) is a three-terminal device which depends on the electrostatic modulation of the current, I_{DS}, which flows between its source and drain electrodes. Control of the source-drain conductance is implemented by the gate voltage, V_g, applied to a control gate situated above and in between the source and drain electrodes of the FET shown, in Fig. 1. Such transistors are usually made by means of photolithographic, etching and liftoff procedures. They employ semiconducting layers deposited or grown on insulating or semi-insulating (SI) substrates by vacuum deposition, chemical vapor phase deposition (CVD), organometallic vapor phase epitaxy (OMVPE), molecular beam epitaxy (MBE) or by direct ion implantation into available SI substrates. The source and drain contacts might be alloyed, diffused or ion implanted ohmic contacts or junctions. The low surface barrier height, ψ_B, of narrow bandgap semiconductors prevents the use of metal Schottky barrier gate electrodes. A great deal of effort has been expended in attempting to circumvent this problem by the use of p-n junction or heterojunction gates or by the use of dielectrically insulated gate structures. Figure

2 shows typical low frequency characteristics of FET and represents the dependence of I_{DS} on the applied source-drain voltage, V_{DS}, with V_g as a fixed independent parameter. It shows that I_{DS} is essentially linear in V_{DS} for low values of V_{DS} and reaches a saturated value, I_{DSS}, in large V_{DS}. An FET which has a quiescent $I_{DS}(V_g = 0) = 0$ is an enhancement mode transistor in contrast with a normally conducting FET which can be

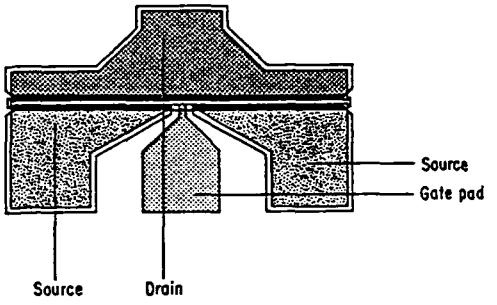

Figure 1. Configuration of a split source FET.

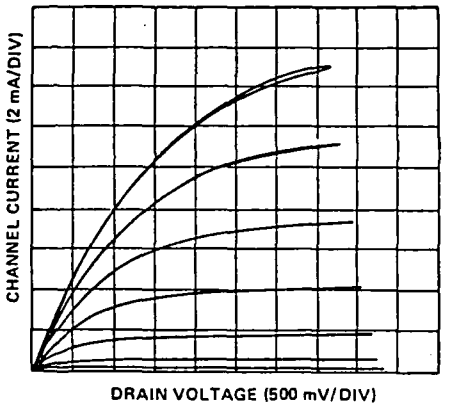

Figure 2. Typical low frequency FET characteristics, horizontal axis is applied source-drain voltage, vertical axis is drain current with gate voltage as a parameter.

modulated in depletion. From data such as that shown in Fig. 2 the transconductance, $g_m = (\partial I_{DS}/\partial V_g)$ can be obtained from both the saturated and linear $I_{DS}(V_{DS})$ regimes. A figure-of-merit of such transistors is their current gain cutoff frequency, f_T, where the output current is equal to the input current, and is also defined as the gain-bandwidth product,

$$f_T = g_m \cdot (2\pi C_{gs})^{-1} \qquad (1)$$

where C_{gs} is the gate to source capacitance. It is related to the transit time, τ_t, by $f_T = (2\pi\tau_t)^{-1}$. The electron transit time is nearly independent of I_{DS} or V_g over a substantial portion of the range in

which $g_m(I_{DS})$ and $C_{gs}(I_{DS})$ have essentially the same slopes. An additional figure-of-merit is the frequency at which the transistor output power is equal to the input power; this is the maximum frequency of oscillation, where g_i and g_D are, respectively, the input and output

$$f_{max} = (f_T/2) \cdot (g_i/g_D)^{1/2} \qquad (2)$$

conductance of the FET. In order to reduce τ_t the gate length, l_g, of the FET, its low electric field mobility, μ_0 and the intervalley gap, $\Delta\Gamma L$, between the conduction band minimum and the next higher conduction band valley are primary considerations. For a large f_T, μ_0 and $\Delta\Gamma L$ should be as large as possible and l_g as small as possible. Two-dimensional computer simulations of conventional FET reveal that g_m increases only slowly with decreasing l_g while $g_D = (\partial I_{DS}/\partial V_{DS})$ also increases. The limit for the useful reduction of l_g is when it is approximately equal to the channel thickness, d. To keep $(l_g/d) > 1.5$, a value chosen as the lower limit, the channel thickness must be reduced as well as the gate length. However, to keep I_{DS} within reasonable bounds the electron density must also be increased. Such an increase, produced by increasing the donor density implies an increase in impurity scattering with a corresponding reduction in μ_0 as well as the possibility of interband tunneling or barrier breakdown. Additional constraints are imposed on the source-drain channel length. To first order, the portion of the channel not covered by the gate represents a series resistance, R_s, which reduces g_m so that

$$g_m = g_m(1 + g_m R_s)^{-1} \qquad (3)$$

The source and drain resistances also depend on their contact and spreading resistances; elaborate metallurgical methods and self-aligned techniques are used to minimize these and to make the fraction of the channel not covered by the gate negligible. A less useful but often quoted FET figure-of-merit is the field-effect mobility, μ_{fe}, derived by fitting $I_{DS}(V_g)$ vs V_{DS} low frequency measurements to the gradual channel approximation model.

Thin Film Transistors

Among the earliest applications considered for InSb thin films was their use in thin film transistors (TFT). Such a device consists of an InSb polycrystalline film vacuum-deposited on a glass substrate and shaped in the form of a narrow channel between ohmic source and drain electrodes. The channel conductivity is modulated by a potential applied to a metal gate which is insulated from the channel by an intermediate dielectric layer. Frantz[1] made such a TFT using flash-evaporated InSb with an electron density, $n = 3.7\times10^{17}/cm^3$ and mobility $\mu = 560 cm^2/V\text{-}s$. He obtained conductivity modulation at room temperature in both depletion and enhancement but did not obtain saturation of the drain current nor did he obtain channel pinchoff. Subsequently Luo and Epstein[2] used a similar procedure to construct coplanar TFT with InSb layers 0.03 to 0.05 μm in thickness, electron density $n = 5\times10^{17} cm^3$ and mobility $\mu = 250\ cm^2/V\text{-}s$. Gate insulators were 0.04 μm thick vacuum-deposited SiO_x layers. Vacuum-deposited In or Sb was used for source and drain electrodes and Al as the gate elec-

trode. At room temperature the I_{DS} vs V_{DS} characteristics of these TFT were essentially the same as those obtained by Frantz; at 77°K they found the expected saturation of I_{DS} and channel pinchoff as a function of V_g. For l_g = 25 μm they obtained a maximum g_m = 6 mS.

Lile and Anderson[3] have investigated the properties of structurally inverted InSb TFT. The surface of an aluminum gate vacuum-deposited on its glass substrate was anodized to a thickness of ~ 0.015 μm thus providing the gate insulating layer upon which 0.2 to 0.3 μm thick InSb was vacuum-deposited through an aperture mask. They demonstrated that source and drain series resistance reduce g_m and, although they obtained a well defined I_{DSS}, their g_m < 1 mS was attributed primarily to the low μ_0 ~ 300 cm^2/V-s. Van Calster[4] investigated the properties of dual gate InSb TFT with 0.15 μm thick SiO_x gate insulators and tried various thermal annealing procedures to improve the mobility of vacuum-deposited InSb layers. The latter is a function of thickness and is, typically, only 10^3 cm^2/V-s for a thickness, d = 0.1 μm, decreasing sharply with d. Due to the strong degeneracy of the electron gas he observed transistor action down to liquid helium temperatures.

In contrast with the InSb TFT are the results obtained by Brody and Kunig[5] on InAs TFT. By controlling the As/In vapor flux ratio they deposited, in vacuum, InAs films on glass and sapphire substrates with Hall mobilities of $3x10^3$ cm^2/V-s for d < 0.1 μm and $8x10^3$ cm^2/V-s for d > 0.3 μm while the electron densities were in the range between 10^{17} and $2x10^{18}$ cm^3. A coplanar TFT with a channel length of 100 μm and width of 1400 μm employing a 0.1 μm InAs layer and a 0.15 μm thick SiO_x gate insulator was found to have a g_m = 10 mS and a f_T = 8 MHz. In view of the degeneracy of the electron distribution such a TFT is essentially temperature independent. However, they found the DC characteristics to be unstable and attributed this to charge redistribution in the insulator.

Vacuum-deposited PbS layers have been used for TFT.[3,6] Evaluation of their properties is complicated by inter- and intragrain variations in stoichiometry and by the presence of oxides of both Pb and Te. Near intrinsic conductivity was required in order to observe conductivity modulation thus introducing a strong temperature dependence of the TFT characteristics. Effective electron mobilities were found to be low; of the order of 300 cm^2/V-s and g_m < 1 mS.

Metal-Insulator-Semiconductor Field-Effect Transistors

Metal-insulator-semiconductor field-effect transistors (MISFET) represent, in most respects, a more advanced stage of device evolution than TFT. MISFET employ single crystal semiconductors usually for inversion mode transistors. Their parameters are, therefore, not dependent on the size and distribution of grains or the electrical properties of intergrain barriers of polycrystalline layers nor are they subject to charge carrier scattering at the channel-substrate heterointerface as are TFTs because the substrate is isolated from the inversion layer by a depletion region. The source and drain contacts have a conductivity opposite to that of the substrate; they are, therefore, isolated from each other unless the gate voltage exceeds a threshold, V_{th}, sufficient to establish a conducting inversion layer channel between them. Figure 3 illustrates, schematically, the structure of such a device.

InSb MISFET

In order to investigate the oscillatory magnetoconductivity and negative photo-conductivity of quantized electrons in the surface inversion layer of InSb Katayama et al[7,8] made n-channel MISFETs of p = $10^{14}/cm^3$ single crystal InSb. Gate insulating layers were made by the deposition of SiO_2 using chemical vapor phase disproportionation of $(C_2H_2O)_4Si$. Vacuum-deposited Al was used as the gate; source and drain electrodes were made by Rh plating and In-Sn alloy was used to attach leads to them. The MISFET were found to have electron mobilities in excess of 10^4 $cm^2/V\text{-}s$ at 4°K. They were used to evaluate the Shubnikov-de Haas oscillations obtained as a function of the applied transverse magnetic induction and their dependence on V_g. They observed a negative photoconductivity attributed to resonant absorption between surface quantum levels in the spectral range between 13 and 28 μm and suggested that optically-induced electronic transitions between sub-bands might provide the basis for a gate voltage-tunable photosensor. Shappir et al[9] have demonstrated the feasibility of p-channel inversion-mode MISFET operating at 77°K. For this purpose they used Te-doped InSb, N_D = $8.5\times10^{14}/cm^3$, in which Cd was diffused to form the source and drain contacts and 0.1 μm thick SiO_x was deposited, at 215°C, to form the gate

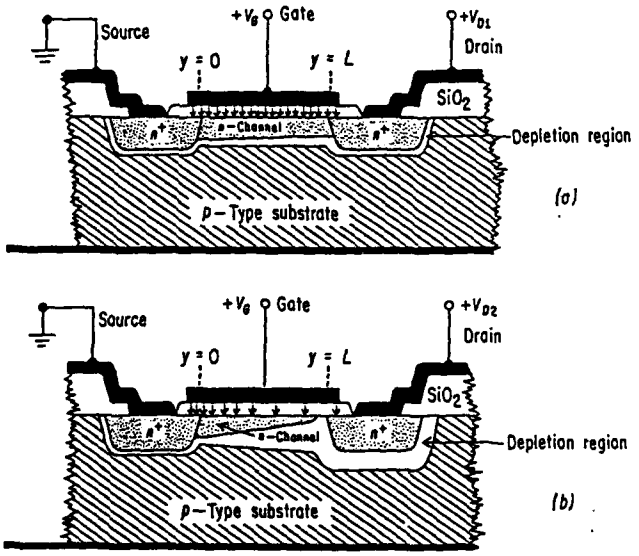

Figure 3. Cross-section of inversion-mode MISFET; a) applied gate voltage is above threshold for channel conduction; b) with gate voltage greater than channel pinchoff value.

insulating layer. The MISFET were made by means of photolithographic techniques with a width to length ratio, w/l = 13.7; the source and drain contacts were made by vacuum-deposition of Cr-Au alloy layers.

From the MISFET characteristics they calculated an effective hole mobility, μ_p = 330 cm^2/V-s. Experimentally observed hysteresis in I_{DS} vs V_{DS} was attributed to modulation of the positive charge in the oxide; with the application of a negative V_g tunneling of electrons was considered to take place from the oxide, where they are trapped, into the semiconductor; when V_g is removed the electrons tunnel back into the traps driven by the electric field associated with the positive oxide charges. Below V_{th} they found an early breakdown of the drain junction attributed to V_g-dependent tunneling of electrons from the valence band of the drain p-region into the n-type inversion layer formed under that portion of the gate which overlaps the reverse biased drain region.

Fujisada[10] described a p-channel inversion-mode MISFET made by selective Be ion implantation into Te-doped n = $6x10^{14}/cm^3$ InSb with low temperature activation of the implanted species for the source and drain contacts. He used a composite gate insulator made of a ~ 0.03 μm thick anodic oxide grown on the InSb surface by wet anodization procedures on which a 0.36 μm thick Al_2O_3 is vacuum-deposited. Such a composite insulator allows the surface potential to be modulated from accumulation through flatband and depletion into inversion with an interface state density, at midgap, of ~ $3\text{-}4x10^{11}/cm^2$-eV and a slight flatband shift of ~ 0.03 V. However it cannot be operated effectively in saturation because of the large increase in drain-substrate current with V_{ds}; furthermore, the DC value of its I_{DS} is unstable and it has a V_{ds} and V_g dependence of its V_{th}. Wei et al[11] have obtained good results with a direct deposition of SiO_x on InSb for linear and two-dimensional charge injection devices as well as MISFET. The gate insulator, ~ 0.1 μm thick, was produced by the pyrolitic reaction of oxygen and silane in ratio of $1:10^3$ in N_2 carrier gas at ~ 200°C. Photolithographic techniques were used to form p-channel, planar, circular gate MISFET, with the source and drain electrodes made by Be^+ ion implantation, through the insulator, with a fluence of ~ $5x10^{14}/cm^2$ and with post-implantation anneal performed in Argon at ~ 200°C. Transient capacitance measurements performed at 78°K on such reverse biased p-n junctions indicated two deep levels: E_c - 0.05 eV and E_c - 0.11 eV. The interface state density was found to have a minimum of $5x10^{10}/cm^2$-eV in the upper half of the bandgap increasing to $5x10^{11}/cm^2$-eV in the lower half of the bandgap. The flatband voltage shift < 0.2 eV. The channel hole mobility, derived from the MISFET characteristics, was ~ 310 cm^2/V-s. Ohashi et al[12] have made n-channel inversion-mode MISFET of molecular beam epitaxially-grown p-type 2 to $5x10^{17}/cm^3$ InSb on GaAs substrates with 0.08 μm thick SiO_2 for gate insulators. The gate length was varied from 3 to 100 μm and the properties of such MISFET, at room temperature, were evaluated and compared to theoretical expectations. The calculated μ_{fe} as a function of the epilayer thickness, is between $1.5x10^3$ and $4x10^3$ cm^2/V-s, considerably smaller than the bulk Hall mobility and I_{DS} did not saturate as a function of V_{DS}; g_m = 6 mS/mm and did not increase with decreasing l_g as expected from elementary theory. The interface state density measured at 77°K was 2 to $6x10^{12}/cm^2$-eV at midgap; however, no account was taken of its effect on g_m. The low μ_{fe} of the inversion layer was attributed to interfacial scattering between the gate insulator and the epilayer surface.

Tunneling in a gate-controlled junction diode made of InSb was

investigated by Margalit et al[13] at 77°K. The n-inversion layer at the surface of the p-diffused region is controlled by the surface potential which is a function of the gate voltage applied to the metal gate on the ~ 0.2 μm thick SiO_2 gate insulating layer. For tunneling to occur in the reverse biased junction the bottom edge of the conduction band at the surface must overlap the bulk valence band edge and the p acceptor density in the bulk must be large enough so that the depletion layer width is sufficiently thin to provide an appreciable tunneling probability. For tunneling in the forward biased junction an additional requirement is imposed: for $V_g = 0$ the Fermi level, E_F, must cross below the valence band edge in the bulk and above the inverted surface conduction band edge. In either case in order to obtain modulation of the surface potential and hence of the tunneling current, the surface state and interface state density at the dielectric-semiconductor interface must be small.

Fujisada and Sasase[14] and subsequently Fujisada and Kawada[15] have also investigated the properties of InSb gate-controlled p-n junction diodes. Gate insulators were either ~ 34 nm thick anodized oxide (MOS) or composite ~ 50 nm thick anodic oxide with a superposed ~ 0.18 μm thick Al_2O_3 layer (MAOS structures). Reverse biased current vs voltage measurements made at 77°K on both MOS and MAOS diodes indicated that this current is essentially independent of V_g and that it increased gradually with voltage up to ~ the value of V_g. Thereafter it depends strongly on V_g. An exponential increase in current is obtained when the junction voltage exceeds V_g; the current increases one order of magnitude for every 0.3 V for the MAOS device and it increases by the same amount for 0.07 V applied to the MOS device.

InAs MISFET

InAs has properties advantageous for MISFET applications because of its low effective electron mass and relatively high energies of its satellite conduction band minima. However, its fundamental bandgap which is only 0.38 eV at 77°K restricts the maximum V_{DS} because of ionization-induced breakdown of the channel. The surface of n-type InAs is normally accumulated and that of p-type InAs is normally inverted. Baglee et al[16] have investigated inversion layer charge transport in InAs at 77°K using a gated Van der Pauw clover-leaf-type structure. Acceptor doped, $p = 2.5 \times 10^{17}/cm^3$, (111B)-oriented InAs was used as the substrate and gate insulators, nominally 0.1 μm thick, were made either by wet anodization in various electrolytes or by the sputter deposition of SiO_x in vacuum. Al was used as the gate electrode and In was used for the contacts. Gated Hall measurements were made by pulsing the source-drain current in order to avoid Joule heating. Figure 4a shows the surface electron density, n_s, as a function of V_g. Evidently the specimen anodized in KOH has a lower $n_s(V_g)$ than the others employing different gate insulators. However its peak mobility, shown in Fig. 4b, is higher although its dielectric breakdown strength is lower and its leakage current is higher than those of the other insulators. The decrease in the Hall mobility with increasing n_s in Fig. 4b has been interpreted by Moore and Ferry[17] as scattering from Coulombic centers localized at the semiconductor-oxide interface while at higher n_s surface roughness is considered to be the dominant mobility limiting mechanism. For the data in Fig. 4b a Coulombic scattering density of $1.3 \times 10^{11}/cm^2$ and an rms surface roughness of 1.5 nm was used to match

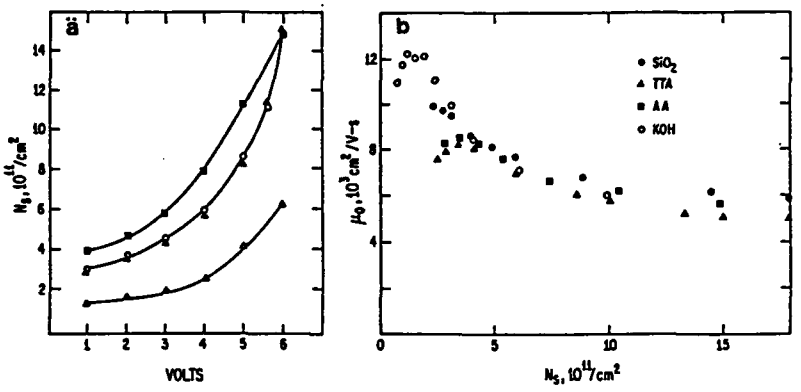

Figure 4. a) Gated surface galvanomagnetic properties of InAs at 77°K; surface electron density as a function of gate voltage and various gate insulators (after Baglee et al, ref. 16); b) Mobility of surface charge carriers of InAs at 77°K as a function of surface electron density and type of gate insulator; ● , sputtered SiO_2; ▲ , anodized in tartaric acid solution; ■ , anodized in arsenic acid; o, anodized in KOH (after Baglee et al, ref. 16).

the KOH oxide data; it is in good agreement with fixed charge in the oxide calculated from C-V measurements in terms of the measured shift of the onset of inversion which yielded $N_{fix} = 9x10^{10}/cm^2$. Similar results were also obtained for the other oxides. However, there is a discrepancy between the theoretically calculated density of scattering centers for the SiO_x gate insulator and that determined from C-V data; the latter, $N_{fix} = 2x10^{12}/cm^2$ ought to produce an effective mobility of 5600 $cm^2/V-s$ instead of the value measured experimentally, 9800 $cm^2/V-s$. A possible reason for the discrepancy might be some form of, as yet undetermined, screening of the Coulomb potential in the oxide accompanied perhaps by an extended spatial distribution of the fixed charge. Figure 5 shows the good fit between the theoretically calculated and experimentally measured inversion channel mobilities determined by Moore and Ferry[17] and includes the data obtained by Kawaguchi[18] using a mylar film gate insulator. Reich and Ferry[19] have made a two-dimensional computer simulation of a narrow, $l_g = 0.25$ μm InAs Schottky barrier gate FET operating at 77°K. Using a finite difference two-dimensional numerical analysis to solve the $I(V_g, V_{DS})$ characteristics in the linear and velocity saturation regimes, they came to the conclusion that such devices might provide performance competitive with superconductive Josephson junction devices.

Borrello et al[20] have investigated the interaction between the InAs depletion regions formed by surface states and impurity diffusion. Mead and Spitzer[21] found from C-V measurements made on p-InAs at 77°K that the hole barrier is 0.47 eV while $E_g = 0.44$ eV. This implies that the Fermi level is ~ 0.03 eV above the conduction band edge indicating degenerate inversion. The surface depletion region is dependent on the carrier concentration through the Debye screening length and the surface

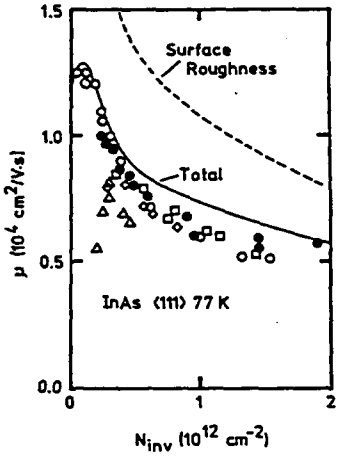

Figure 5. Dependence of measured and theoretically calculated inversion channel mobility of InAs as a function of its electron density and type of gate insulator: □ , anodized in arsenic acid; o, anodized in KOH; ◇ , anodized in tartaric acid; ● , sputter deposited SiO_2; △ , mylar sheet (after Moore and Ferry, ref. 17).

depleted layer can be made to merge with a bulk depleted layer formed by impurity diffusion. This was done by Cd diffusion into *n*-type InAs forming a p-n junction in which the Cd concentration at the surface is between 10^{18} and $10^{19}/cm^3$ dropping to ~ $10^{17}cm^3$ at a depth of 2 μm and declining thereafter with a complementary error function profile. A metal contact is deposited on the etched junction surface. In the band diagram of Fig. 6, w is the diffusion depth less the barrier width. If a sufficient amount of doped material is removed by etching, then the position of zero electric field is altered from w to a plane which permits an externally applied potential to influence the entire structure. Eventually, the valence band edge is several kT from the Fermi level and the hole concentration in the potential well is no longer determined by the impurity concentration. The hole lifetime can influence directly, via the barrier height, the electron current produced by an external potential applied to such a junction.

Mercury Cadmium Telluride Gate-controlled Diodes

Kolodny and Kidron[22] have investigated the properties of gate-controlled ion-implanted p-n junctions of mercury cadmium telluride. For this purpose they used p-type $Hg_{0.71}Cd_{0.29}Te$ wafers with hole densities of 1 to $5x10^{16}/cm^3$ and μ_0 ~ 250 $cm^2/V-s$ at 77°K. Ion implantation of B, Al, P, and Ar was performed at room temperature with fluences of 10^{13} to $10^{15}/cm^2$ and energies of 10^2 to $3x10^2$ keV. After post-implantation annealing in vacuum up to 140°C the junction depth was, typically, < 1 μm . Gate-controlled diodes were made with vacuum-deposited indium gate electrodes overlapping the edge of the mesa diodes and insulated by ~ 0.5 μm thick ZnS or by an anodic oxide of HgCdTe, as

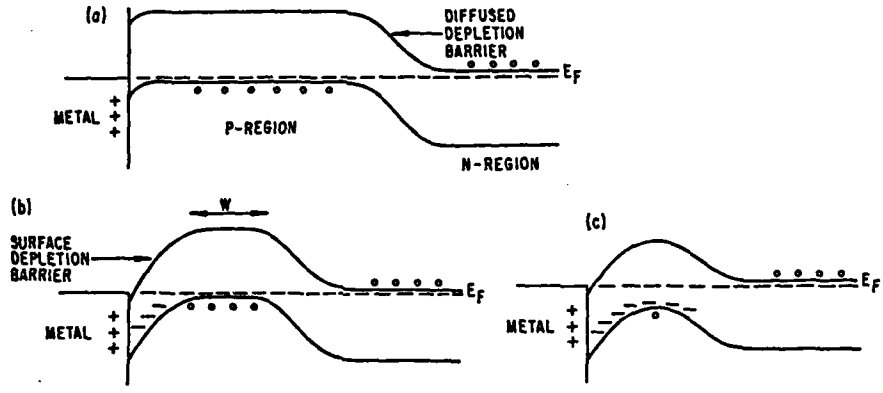

Figure 6. Surface and diffusion potential barrier interactions in InAs; a) energy band diagram following diffusion of Cd into n-type InAs; b) reducing thickness of p-type surface layer by etching, w, is diffusion depth less surface barrier width; c) further reduction of surface layer with valence band edge several kT from Fermi level (after Borrello et al, ref. 20).

shown schematically in Fig. 7. If V_g is more negative than the flatband voltage, V_{fb}, then the surface on the p-side of the junction is accumulated and that on the n-side is inverted. The interface charge was

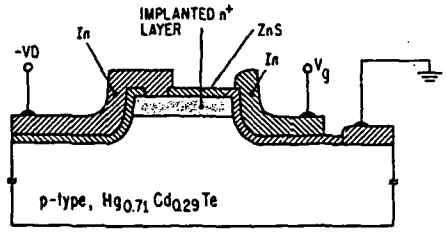

Figure 7. Schematic cross-section of HgCdTe gate-controlled junction diode (after Kolodny and Kidron, ref. 22).

determined to be negative - $3x10^{11}/cm^2$. Figure 8 shows the characteristic properties of such a device attributed to reverse and forward tunneling currents with the forward injection currents large enough to mask the differential negative resistance. For $V_G > V_{fb}$ an n-type surface inversion layer forms on the p-side of the junctions. In reverse bias the large leakage currents saturate. This saturation current, through the inversion layer, is attributed to reverse and forward tunneling currents with the forward injection currents large enough to mask the differential negative resistance. For $V_g > V_{fb}$ an n-type surface inversion layer forms on the p-side of the junction. In

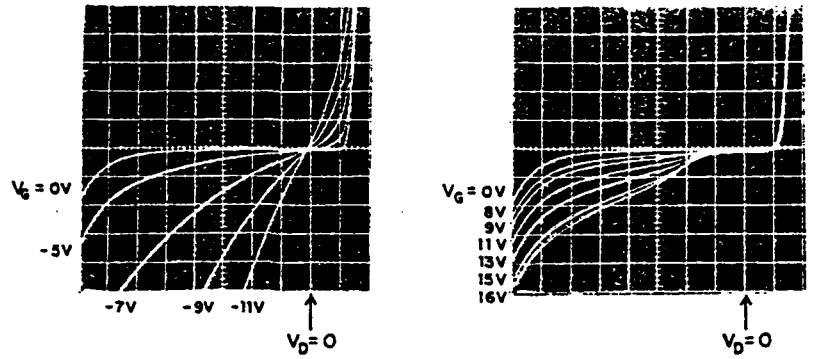

Figure 8. Current vs voltage of gate-controlled junction diode at 77 K. Left: $V_g < V_{fb}$ (p-side accumulated; Right: $V_g > V_{fb}$ (p-side inverted) [after Kolodny and Kidron, ref. 22].

reverse bias the large leakage currents saturate. This saturation current, through the inversion layer, is attributed to channel pinchoff in a manner similar to that of silicon gate-controlled diodes. The dielectric properties of the oxides of HgCdTe grown by wet anodization were investigated by Bertagnolli[23] using KOH-ethylene solutions. Such oxides grown at room temperature have a fixed positive charge $\sim 10^{12}/cm^2$, a 0.1 V hysteresis attributed to slow surface states $\sim 10^{11}/cm^2$, and a low frequency dispersion of its dielectric properties. No such dispersion is found in the higher quality oxides grown at 50°C. These exhibit a fixed charge $\sim 1.4 \times 10^{12}/cm^2$, a smaller hysteresis, $\sim 5 \times 10^{10}/cm^2$, a fast surface state density $\sim 10^{12}/cm^2$-eV and a high surface recombination velocity. Oxides grown at 75°C, on the other hand, were found to have a pinned surface Fermi level.

Germanium MISFET

Germanium has a room temperature electron mobility $\mu_n = 3900\ cm^2/V\text{-}s$ and a hole mobility $\mu_p = 1800\ cm^2/V\text{-}s$ compared to silicon with the same impurity concentration, $\mu_n = 1400\ cm^2/V\text{-}s$ and $\mu_p = 450\ cm^2/V\text{-}s$ and is, therefore, of particular interest for use in integrated circuits employing complementary n-channel and p-channel MISFET. However, the native oxides of Ge are volatile at the oxidation temperature, they are usually composed of suboxides rather than GeO_2 and their interface charge densities are considerably greater than $10^{12}/cm^2$. Rzhanov and Neizvestny[24] found that Ge MISFET with composite SiO_2-Si_3N_4 gate insulators have more favorable electrical properties. The room temperature μ_{fe} dependence on n_s of such MISFET is qualitatively similar to that of Si MOSFET; it rises from $\sim 750\ cm^2/V\text{-}s$ at 300°K to $\sim 10^3\ cm^2/V\text{-}s$ at 140°K decreasing thereafter with a further decrease in temperature. Further investigations on Ge n-channel inversion-mode MISFET have been made by Rosenberg[25]. He used (100)-oriented p-doped Ge with gate insulators made by the thermal reaction at ~ 700°C of Ge with nitrogen to form ~ 0.01 μm thick Ge_3N_4 layers. These were found to have a breakdown strength in excess of 5×10^6 V/cm and an interface density of

less than $2\times10^{11}/cm^2$. Source and drain electrodes were made by the ion implantation of As and vacuum deposited Aℓ was used for metallization of the gate, source and drain. Such a prototype MISFET had a $\mu_{fe} = 1.9\times10^3$ $cm^2/V\text{-}s$ although its drain resistance was high and it had large junction leakage currents.

Ternary III-V Alloy MISFET

The ternary alloy $In_{0.53}Ga_{0.47}As$ with a fundamental room temperature bandgap of 0.75 eV, $\mu_0 = 8\times10^3$ $cm^2/V\text{-}s$ for $n = 10^{17}/cm^3$ is well suited for a variety of FET applications and it can be grown in the form of epitaxial layers on SI InP substrates. Wieder et al[26] have shown that such layers with a hole density, $p = 2\times10^{17}/cm^3$ can be used to make inversion mode MISFET with source and drain electrodes of alloyed 20:80 Sn-Au and gate insulating layers made of 0.1 μm thick SiO_2 grown by the low temperature plasma assisted pyrolisis of silane in the presence of NO_3. Subsequently, Liao et al[27] described such an inversion-mode MISFET with a Si_3N_4 gate insulator with a $g_m = 3$ mS/mm. Considerably better results were obtained by Ishii et al[28] with enhancement-mode MISFET employing a composite gate insulator of ~ 0.01 μm thick anodic oxides of $In_{0.53}Ga_{0.47}As$ and ~ 0.1 μm of superposed $Aℓ_2O_3$. The thickness of the $In_{0.53}Ga_{0.47}As$ layer was chosen so that, for $V_g = 0$, it is totally depleted and a positive V_g is required for channel conduction. For $l_g = 10$ μm and a surface state density $\sim8\times10^{11}/cm^2\text{-}eV$ near mid-gap they obtained a $g_m = 17$ mS/mm. They also found that, in analogy to InSb MISFET, these have a DC drain current drift which has a logarithmic time dependence attributed to tunneling of charge carriers into traps in the gate insulator. Kaumans et al[29] investigated the nature of the semiconductor-dielectric interface of $In_{0.53}Ga_{0.47}As$ and SiO_2 using various post-deposition thermal annealing cycles and made non-optimized n-channel inversion-mode MISFET with a $\mu_{fe} < 100$ $cm^2/V\text{-}s$. Considerably better results were obtained by Gardner et al[30,31] using low temperature chemical vapor phase-deposited SiO_2 annealed for 16 hours at 300°C prior to gate metallization and annealed again for 15 min. following deposition of the gate metal. Their n-channel inversion-mode MISFET had l_g of 1.5 to 3 μm and width of 150 μm. They obtained $\mu_{fe} = 2.5\times10^3$ to 4.6×10^3 $cm^2/V\text{-}s$. Such devices also exhibited a significant DC drain current drift with I_{DS} decaying to ~ 50% of their initial value in ~ 100 s. However, similar self-aligned structures with ion-implanted source and drain electrodes, $l_g = 1$ μm; width of 140 μm, gate insulator thickness of 0.9 μm, interface state density < $10^{11}/cm^2\text{-}eV$ and a fixed oxide charge density ~ $4\times10^{10}/cm^2$ had a $g_m = 43$ to 64 mS/mm and the drain current instability was reduced to ~ 2% of its original value. More recently[32], by minimizing the gate overlap parasitic capacitance and by using a gate length of 1 μm they obtained a $g_m = 107$ mS/mm corresponding to an electron velocity of 2.5×10^7 cm/s. Depletion-mode MISFET of similar configuration made of n-type $In_{0.53}Ga_{0.47}As$ were found to have[33] an estimated $f_T = 20$ GHz, surface state densities in the range between 2.5×10^{12} in accumulation to $2\times10^{10}/cm^2\text{-}eV$ in inversion and a minimum noise figure of 3.4 dB with 9.4 dB associated gain at 4 GHz.

Gate-controlled galvanomagnetic measurements have been made on transistor-like five-terminal MISFET structures by Mullin and Wieder[34] using 0.25 μm thick $In_{0.53}Ga_{0.47}As$ epilayers grown on semi-insulating InP substrates with 0.1 μm thick Al_2O_3 gate insulators. Hall effect and resistivity measurements were made on such structures as a function of the applied gate voltage and the data were used to derive the density of surface states and their position within the bandgap. They found that while the surface Fermi level of virgin structures is pinned ~ 2 eV below the conduction band even mild thermal annealing at 120°C for 16 h reduces the density of interface states from ~ $5x10^{12}/cm^2$-eV to $2x10^{11}/cm^2$-eV at midgap and allows the surface potential to be displaced over most of the fundamental bandgap. Wieder et al[35] also demonstrated an enhancement-type MISFET based on surface accumulation of nearly semi-insulating $In_{0.53}Ga_{0.47}As$ which has its residual donors compensated by deep level Fe^- acceptors. A non-optimized structure with an 8 μm long gate 240 μm in width with either SiO_2 or Al_2O_3, 0.12 μm thick gate insulators and Al gate electrodes had a field-effect mobility of 793 cm^2/V-s. O'Connor et al[36] used a 10 to 25 nm thick silicon nitride gate insulator, made by reacting ammonia with silane at 300°C, for an $In_{0.53}Ga_{0.47}As$ MISFET, defined as an insulator-assisted Schottky gate FET. Such as device with a gate l_g = 1.2 μm, width of 250 μm, gate capacitance, ~ 4.2 pF had a g_m = 130 mS/mm and a current of ~ $2x10^{-3}$ A/cm^2 for 10 V reverse bias. Subsequently Cheng et al[37] described a similar device with a 5 to 12 nm thick electron beam-evaporated SiO_2 gate insulator and a self-aligned recessed gate structure; they obtained a g_m = 150 mS/mm, a v_s = $2.4x10^7$ cm/s and an estimated f_T = 15 GHz.

$In_{0.53}Ga_{0.47}As$ Homojunction Field-Effect Transistors

The feasibility of p-n homojunction gate field-effect transistor (JFET) was demonstrated by Leheny et al[38] using ~ 1 μm thick liquid phase epitaxially-grown, n = $2x10^{16}/cm^3$, $In_{0.53}Ga_{0.47}As$. A 20 μm long 1 mm wide gate was made by Zn diffusion through a silicon nitride mask at 750°C for 70 s in a $ZnAs_2$ atmosphere. The resultant metallurgical junction at a depth of 0.5 μm required V_g = - 4 V for channel pinchoff and had a g_m = 1 mS/mm. A homojunction quasi-Schottky barrier gate diode employing a depleted, thin p^+-layer to reduce the gate leakage current while eliminating the problems associated with a hetero-interface gate was described by Chen et al[39]. Using MBE an n^+ $In_{0.53}Ga_{0.47}As$ layer, 0.5 μm thickness, was first grown on an(100)-oriented n^+ InP substrate followed by a 3 μm thick, Sn-doped, n = $10^{17}/cm^3$ layer and thereafter by an 8 nm Be-doped, p = $8x10^{18}/cm^3$ layer. The effective barrier height rose from ~ 0.27 eV to 0.47 eV. The properties of JFET made by MBE were also investigated by Chang et al[40]. They deposited first a buffer layer of high resistivity $In_{0.52}Ga_{0.48}As$ on (100)-oriented semi-insulating InP followed by a relatively thin transition layer of $In_{0.53}Ga_{0.25}Al_{0.22}As$; thereafter, the undoped n-type channel, 0.7 μm in thickness, n = $2x10^{16}/cm^3$ was deposited followed by an 0.8 μm thick Mn-doped, p = $10^{18}/cm^3$ gate layer. For l_g = 2 μm they obtained a g_m = 50 mS/mm and found that in the narrow gate devices there is an inflection point in the I_{DS} vs V_{DS} curves accompanied by a sharp rise in I_{DS} attributed to an unfavorable channel length to depth ratio. High

frequency JFETs were made by Chai et al[41] using MBE-grown n-type $In_{0.53}Ga_{0.47}As$ layers deposited directly, without any intermediate buffer layer, on SI InP substrates. The junction gate was made by Be ion implantation with a fluence of $10^{14}/cm^2$ at 30 keV followed by annealing at 675°C for 20 min. in flowing hydrogen with an activation ~ 20%. The g_m = 86 mS/mm was considerably smaller than that expected of the measured μ_0 = 5.5 to 6.5x10^3 cm^2/V-s and the l_g < 1 μm. Further investigations revealed that μ_0 decreases at the channel-substrate interface to ~ 10^3 cm^2/V-s; this as well as a corresponding reduction in v_s, might be responsible for the smaller than expected g_m. Nevertheless, these JFETs with a 250 μm wide gate were found to have, at channel pinchoff, a source-drain breakdown strength ~ 20 V; they also had a 5.2 dB gain at 11 GHz with a power added efficiency of 14 %. Schmitt and Heime[42] have suggested that some of the problems encountered with ion-implanted ternary alloy JFETs might be due to the long range diffusion tails which follow high temperature annealing of the implanted acceptors compensating the donors in the channel and reducing the electron mobility. However, Selders et al[43] demonstrated that SiO_2-capped $In_{0.53}Ga_{0.47}As$ subjected to rapid thermal annealing of ion-implanted Be (800°C for 0.5 s) can produce JFETs with g_m = 130 mS/mm and an f_T = 15 GHz. Schmitt and Heime[42] have made ternary alloy JFETs by diffusing Zn at 600°C for 10 min. which had been earlier deposited from a "spin-on" solution. With the metal gate as a mask, photo-lithographic and etching techniques were used to fashion junction gates 1.2 μm in length and 300 μm in width to produce devices with g_m = 100 mS/mm, v_s = 2.3x10^7 cm/s and f_{max} = 30 GHz.

A self-aligned JFET grown by MBE deposited on SI or n^+ InP was described by Cheng et al[44]; it was intended to make such transistors compatible with optoelectronic devices integrated on the same substrate. The vertical junction structure consists of an 0.05 μm thick p^+ = 2x10^{19}/cm^3 cap layer, a 0.4 to 0.5 μm thick, n = 10^{17}/cm^3 channel and a Be-doped p^+ = 5x10^{18}/cm^3, 0.4 to 0.8 μm thick confinement layer all of $In_{0.53}Ga_{0.47}As$. Cr-Au gate metal patterns were photolithographically defined and self-aligned techniques were used to make the Au-Ge source and drain electrodes. A preferential, crystallographically selective etching solution was used to produce an undercut gate ~ 1 μm in length, 100 to 320 μm in width. Such devices have been made to operate in both depletion and enhancement. In depletion typical g_m = 90 mS/mm while in enhancement g_m = 60 to 70 mS/mm. An alternative means of channel isolation was also employed[45] by replacing the SI InP layer with a 1 μm thick undoped $In_{0.52}Al_{0.48}As$ layer grown by metal organic vapor-phase epitaxy (MOVPE) with no significant improvement in performance.

MOVPE was also used by Wake et al[46] for making JFET. They found, however, that considerable outdiffusion of the p dopant can occur during growth and this decreases the mobility and saturated velocity of the electrons in the channel as well as reducing its free electron density due to compensation of its donors. Cadmium is an acceptor and has a lower diffusion coefficient than Zn in InP; by using Cd in the buffer layer in concentration equal to or smaller than that of the channel they obtained high quality junctions. These were used with a preferential etching solution and self-aligned techniques to make JFETs with l_g = 1.5 μm, width of 270 μm and g_m = 210 mS/mm; the gate to source capacitance C_{gs} = 0.5 pF for V_g = 0, the calculated v_s = 2.7x10^7 cm/s,

close to the estimated theoretical maximum and the calculated f_T = 18.5 GHz.

Heterojunction Field-Effect Transistors

Among the reasons for the current research emphasis on ternary alloy hetero-junction gate field-effect transistors (HJFET), in particular, two-dimensional gas (2DEG) modulation doped transistors, is their potentially superior high speed and low noise characteristics in comparison with other FET. Initially, $In_{0.52}Al_{0.48}As$ with a fundamental bandgap, E_g = 1.46 eV, whose lattice constant matches that of InP, was intended, primarily, as a heterojunction gate for raising the effective barrier height of $In_{0.53}Ga_{0.47}As$ while avoiding problems associated with interfacial misfit dislocations. It was also considered to be an adequate buffer layer between the active channel and its SI InP substrate. Ohno et al[47] have made such a depletion-mode HJFET using MBE to grow, sequentially, on a (100)-oriented InP substrate a 0.1 μm $In_{0.52}Al_{0.48}As$ buffer layer, a 0.125 μm $In_{0.53}Ga_{0.47}As$ layer with a superposed barrier-enhancing 0.06 μm thick $In_{0.52}Al_{0.48}As$ layer followed by an Al gate. Photolithographic techniques and a phosphoric acid/hydrogen peroxide etch were used to make devices with AuGe source and drain electrodes, 2.75 μm gate length, 3.5 μm source-gate separation, and 10 μm source drain separation. They obtained a saturated g_m = 57 mS/mm, an apparent barrier height of 0.80 eV and a gate leakage current, for a reverse bias of 8 V, of 416nA/μm^2. A similar double heterostructure depletion mode HJFET was made, using MBE, by Barnard et al[48]. With a gate 0.6 μm in length, 0.65 μm wide and source-drain spacing of 2.9 μm they obtained, in the depletion-mode, a g_m = 135 mS/mm. The gate leakage current was less than 62 nA/μm^2 for V_g < 3 V rising to 310 nA/μm^2 for V_g = 4 V. In the enhancement-mode these devices had a small g_m (attributed to negatively charged interface states at the channel-buffer interface) which decreased with increasing positive bias.

In modulation-doped field-effect transistors (MODFET) very high charge carrier mobilities are obtained by separating, spatially, the conduction electrons in the channel layer from their ionized donor impurities which are present in an adjacent, larger bandgap layer. The carriers are confined in a 2DEG quantum well by the inter-facial band edge discontinuities between these layers.

The structure and configuration of a MODFET are subject to the following criteria which determine the thickness and doping of each layer:

(a) The $In_{0.52}Al_{0.48}As$ cap layer need be n-doped to ~ $10^{17}/cm^3$; it should be thin enough so that it is nearly depleted by band bending from both its metal Schottky barrier and its heterojunction interface with the $In_{0.53}Ga_{0.47}As$ channel.

(b) The $In_{0.53}Ga_{0.47}As$ layer containing the 2DEG usually has a background n-type electron density of $5x10^{15}$ to $2x10^{16}/cm^3$ when grown by MBE. The 2DEG is confined in an accumulation region at the heterojunction interface. It is desirable for the layer thickness to be small enough, typically, 0.1 to 0.2 μm, so that this background charge concentration represents less than 10% of the ~ $10^{12}/cm^2$ surface charge density in the 2DEG well.

(c) An undoped, essentially, SI $In_{0.52}Al_{0.48}As$ buffer layer should, preferably, isolate metallurgically the $In_{0.53}Ga_{0.47}As$ layer from possible outdiffusion of impurities or propagation of defects from the InP substrate.

Electrical and galvanomagnetic measurements made on MBE-grown modulation-doped $In_{0.53}Ga_{0.47}As$-$In_{0.52}Al_{0.48}As$ structures by Cheng et al[49] exhibited electron mobility enhancement by a factor of 2 at 300°K and a factor of 6 at 77°K in comparison with n-type $In_{0.53}Ga_{0.47}As$ with the same electron concentration. Chen et al[50] have described the construction and performance of a MODFET employing such a hetero-structure; $In_{0.53}Ga_{0.47}As$ 1.5 μm thick with $n = 2\times10^{15}/cm^3$ was first grown by MBE on SI (100)-oriented InP followed by an 9 nm undoped spacer layer of $In_{0.52}Al_{0.48}As$ and then by an 0.15 μm Si-doped $n = 10^{17}/cm^3$ layer of the same alloy. The MODFET was made with a gate $l_g = 5.2$ μm, 340 μm in width and a source-drain separation of 10.4 μm. Source and drain contacts were made by sequential deposition of 20 nm Ge, 0.1 μm Au-Ge, 20 nm Pt and 20 nm Au which were alloyed at 450°C for 1 min. The enhanced μ_0 was credited for the measured $g_m = 31$ mS/mm at 300°K and 69 mS/mm at 77°K with the g_m fairly constant for $V_g < 2$ V; an abrupt decrease of g_m for $V_g > 2$V was attributed to the initiation of parasitic charge transport in the $In_{0.52}Al_{0.48}As$ layer. Chen et al[51] proposed a theoretical model for the dependence of g_m on V_g whose principal features are shown, schematically, in Fig. 9. If $0 > V_g > V_{FB}$ then g_m is independent of V_g and the band diagram of Fig. 9a is applicable; the flatband voltage, V_{FB}, is defined as the gate voltage required to quench the 2DEG, as shown in Fig. 9b; in this case the MODFET conducting channel is not completely pinched off due to the presence of background carriers and g_m is to some extent a function of V_g. Figure 9c shows that as V_g exceeds V_{FB} the depletion edge extends into the undoped $In_{0.53}Ga_{0.47}As$ layer and g_m becomes a strong function of V_g.

Pearsall et al[52] have made recessed gate depletion-mode MODFET with $l_g = 1.2$ μm, 125 to 250 μm in width and source-drain spacing of 8 μm. At 300°K they obtained a $g_m = 90$ mS/mm and at 77°K a $g_m = 200$ mS/mm. Their measurements suggested that a substantial fraction of the channel current is carried not in the 2DEG but in the rest of the $In_{0.53}Ga_{0.47}As$ layer and that this occurs as a consequence of real space transfer of moderately "hot" electrons out of the 2DEG potential well. It has been suggested by Chan et al[53] that an $In_{0.53}Ga_{0.47}As$/InP-based inverted modulation-doped structure might have a higher v_s than one with a normal configuration, one in which the InP layer is on top of the $In_{0.53}Ga_{0.47}As$ channel while in an inverted structure it is below the channel. They found that in the inverted structure I_{DSS} is consistent with the low field electron concentration and the bulk v_s, while in a normal structure I_{DSS}, is significantly smaller than expected and might be attributed to real space transfer of electrons into the InP layer. Seo et al[54] have used MBE to make an inverted $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ HJFET in which the active channel is a single quantum well of $In_{0.53}Ga_{0.47}As$ 10 to 40 nm in thickness. Using a recessed gate configuration they obtained with a 1.8 μm long and 60 μm wide gate a $g_m = 130$ mS/mm and a gate leakage current of 3 μA for V_g

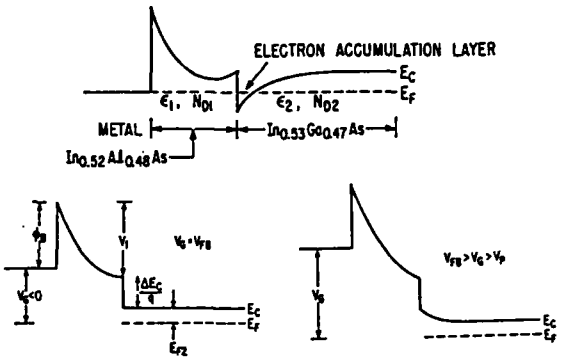

Figure 9. Band diagram of $In_{0.53}Ga_{0.47}As$ MODFET as a function of applied gate voltage: E_1, N_{D1} and E_2 N_{D2} are the respective fundamental bandgaps and donor doping densities of $In_{0.52}Al_{0.48}As$ and $In_{0.53}Ga_{0.47}As$ with $N_{D1} >> N_{D2}$; a) with two-dimensional quantum well; b) at flatband; c) beyond flatband, depletion layer extends into $In_{0.53}Ga_{0.47}As$ (after Chen et al, ref. 51).

= -3 V. However, just as for the other MODFET, they found a strong dependence of g_m on V_g affected by real space charge transfer.

OVERVIEW

The low barrier height of narrow bandgap semiconductors which prevents their use for Schottky barrier gate FET has led to the search for alternatives. If compatible gate insulators with interfacial properties similar to those of the Si-SiO_2 system were available then insulated gate depletion and inversion-mode transistors analogous to MOSFETS might be feasible. Such devices might use the high electron mobility and saturated velocity of the narrow gap semiconductors while retaining the configurational simplicity of MOSFET. However, insulators presently available are far from ideal; only fragmentary information is available on insulator-semiconductor interfaces. MISFET as well as two-terminal MIS structures employing narrow gap semiconductors exhibit hysteresis and a logarithmic time dependent drift of their DC characteristics. This drift, attributed to tunneling of electrons from a semiconductor surface into traps located in the insulator within ~ 4 nm of its interface, is also present in Si-SiO_2 structures (it is smaller by two orders of magnitude in comparison with that of III-V semiconductors). Furthermore, electron scattering from charged interfacial centers as well as roughness scattering limit the surface channel mobility of MISFETs to less than 20% of their Hall mobilities. Fast and slow surface states also interpreted as spatial fluctuations in surface potential affect adversely the g_m and f_T of MISFETs. They depend on empirically-based semiconductor surface preparation, prior to deposition of the insulator, on the parameters of the deposition process itself, on the fundamental properties of the native oxides as well as on those of the synthetic dielectric layers.

Homojunction FET circumvent some of the problems associated with MISFETs. However, the gate voltage swing in forward bias must not exceed the built in contact potential difference between the ion-implanted or diffused p^+ gate and the n channel. Leakage currents limit the maximum applicable reverse gate bias and the relatively large junction capacitance of such structures reduce their f_T. Nevertheless, excellent results have been obtained with $In_{0.53}Ga_{0.47}As$ enhancement and depletion-mode JFET and a depleted p-doped layer under the metal gate of an MESFET has been used to raise its effective surface barrier height.

A MODFET is, in some respects, the analog of a MISFET with the insulator replaced by a doped but depleted large bandgap semiconducting layer adjacent to an undoped narrow bandgap 2DEG channel. Modulation doping implies that in such a heterostructure charge carriers are transferred from the large gap into the narrow bandgap channel where they are confined by the band offsets between them and are not subject to impurity scattering. Preliminary results obtained with $In_{0.53}Ga_{0.47}As$/ $In_{0.52}Al_{0.48}As$ MODFETs appear promising although at his stage of their development their performance is limited in part by the residual impurity concentration of $In_{0.53}Ga_{0.47}As$ and, if the gate voltage is large enough, by real space transfer out of the 2DEG well.

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Composition dependence of Au/$In_xAl_{1-x}As$ Schottky barrier heights

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The surface barrier heights ϕ_{bn} and room-temperature band gaps E_g of Si-doped $In_xAl_{1-x}As$ layers grown by molecular beam epitaxy on *n*-type (100) oriented InP substrates have been determined as a function of composition with capacitance versus voltage, internal photoemission, photoluminescence, and double-crystal x-ray rocking curve measurements for $0.45 < x < 0.55$. The results indicate that E_g and ϕ_{bn} are linear functions of x; they also suggest that ϕ_{bn} (0.78) = 0 and, for $x > 0.78$, *n*-type surfaces might be accumulated and *p*-type surfaces are likely to be inverted.

$In_xAl_{1-x}As$ is a material of considerable interest for applications that include heterojunction field-effect transistors (HJFET's) and quantum well structures. Research on this ternary alloy system has been centered on $In_{0.52}Al_{0.48}As$ whose lattice constant a matches that of InP as well as that of the low effective mass, high electron mobility alloy $In_{0.53}Ga_{0.47}As$. One of the first applications, demonstrated by Ohno *et al.*,[1] employed $In_{0.52}Al_{0.48}As$ in an HJFET structure as both a buffer layer between the $In_{0.53}Ga_{0.47}As$ channel and its InP substrate, and as the means for enhancing the surface barrier height of the $In_{0.53}Ga_{0.47}As$ channel ($\phi_{bn} = 0.2$ eV). A capacitance-voltage (*C-V*) measured Schottky barrier height of 0.80 eV was obtained by Ohno *et al.*[1] for *in situ* deposited Al/$In_{0.52}Al_{0.48}As$ contacts while Hsieh *et al.*,[2] using internal photoemission, found $\phi_{bn} = 0.64$ eV with Au contacts ostensibly for the same composition. More recently GaAs, which is lattice mismatched relative to $In_{0.53}Ga_{0.47}As$ by 3.7% was used[3,4] to raise the ϕ_{bn} of an $In_{0.53}Ga_{0.47}As$-based HJFET. Transmission electron microscopy studies[5] have shown that the resultant strain was accommodated by dislocations confined to within $\approx$40 nm of the heterojunction interface and somewhat improved HJFET performance has been obtained with thicker (100 nm) GaAs enhancement layers.

No detailed investigations have been made, however, of the dependence of the HJFET criteria on the composition of $In_xAl_{1-x}As$, its ϕ_{bn}, and its interfacial charges produced by misfit dislocations. Little is known about this alloy system, which has a direct room-temperature fundamental band gap E_g in the range of $0.32 < x < 1$ (Ref. 6), except for $E_g(x)$ between $0.46 < x < 0.56$ as investigated by Wakefield *et al.*[7] and Davies *et al.*[8] Since it has been suggested[9] that, to first order, the threshold voltage V_T of enhancement-mode HJFET depends on ϕ_{bn} in accordance with

$$V_T = \phi_{bn} - \Delta E_c , \qquad (1)$$

where ΔE_c is the heterojunction conduction band edge discontinuity, we have measured the composition dependence of ϕ_{bn} and E_g over the same range of x as Davies *et al.*[8] and report our preliminary results.

Experimental investigations were made on 0.5–0.6 μm thick $In_xAl_{1-x}As$ specimens grown by molecular beam epitaxy (MBE) at UCSD on (100) oriented, S- or Sn-doped ($n = 2\times10^{17}$ cm^{-3}) InP substrates. Following As stabilization of the InP surfaces, the fractional In content was varied by changing the Al flux while maintaining a constant In flux with the substrate temperature held at 500 °C. In order to keep the depletion region well within the $In_xAl_{1-x}As$, the layers were donor doped with Si. The lattice mismatch of the layers relative to their InP substrates, $\Delta a/a_0$, was measured by double-crystal x-ray diffractometry and their fractional In content x was calculated from these measurements by the use of Vegard's law with corrections for the tetragonal distortion[10] that compensates the interfacial strain. Figure 1 shows the dependence of $\Delta a/a_0$ on x determined in this manner and is qualitatively similar to that of $In_yGa_{1-y}As$,[11] in the vicinity of $y = 0.53$, relative to InP. Photoluminescence measurements, made at room temperature, were used to de-

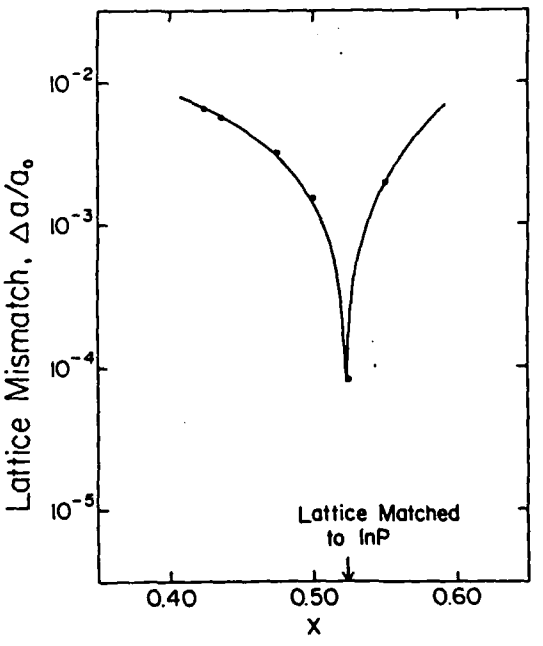

FIG. 1. Lattice mismatch $\Delta a/a_0$ between $In_xAl_{1-x}As$ and InP as a function of x.

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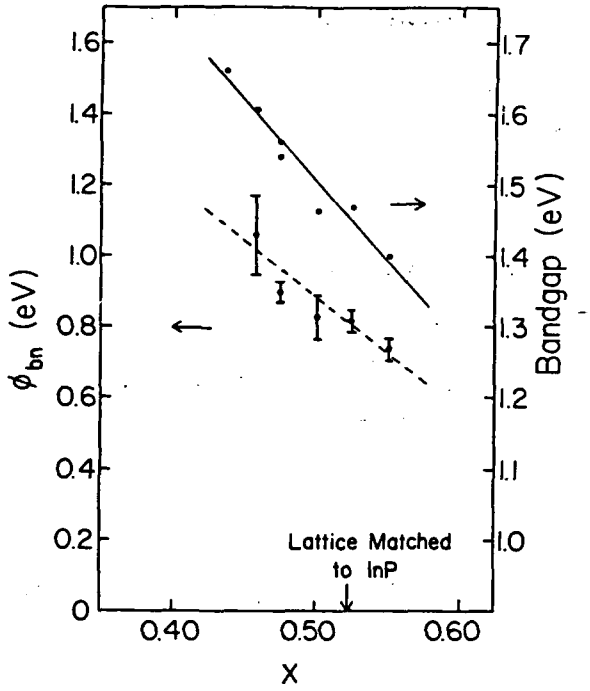

FIG. 2. Room-temperature band gaps and Au/n-$In_xAl_{1-x}As$ Schottky barrier heights as a function of x. Solid line is obtained from Ref 8 and dashed line represents Eq. (3).

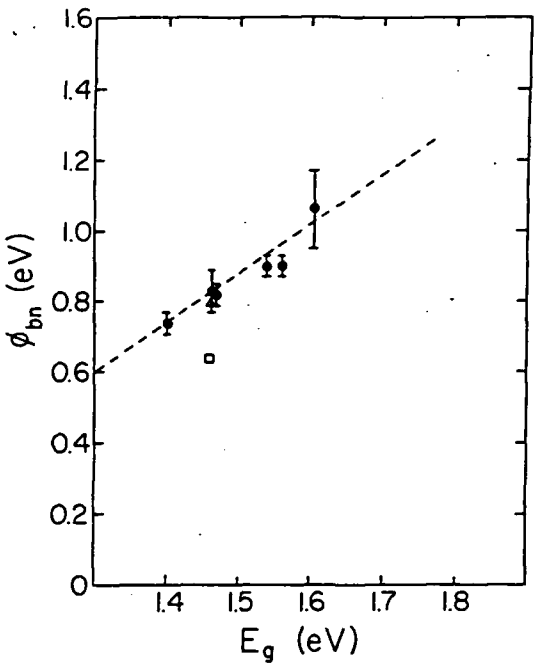

FIG. 3. Dependence of metal/n-$In_xAl_{1-x}As$ Schottky barrier height on band gap. (●) our data; (△) $Al/In_{0.52}Al_{0.48}As$ from Ref. 1; (□) $Au/In_{0.52}Al_{0.48}As$ from Ref. 2; dashed line represents Eq. (2).

termine E_g as a function of x; it is shown in Fig. 2 to be in good agreement with those of Davies *et al.*[8] made over the range of $0.46 < x < 0.56$.

After lightly etching the $In_xAl_{1-x}As$ surfaces in buffered HF and H_3PO_4:H_2O_2:H_2O solutions, circular Au Schottky barrier contacts were vacuum deposited and defined by liftoff technique. Their InP substrates were then mounted onto copper blocks with indium solder. C-V measurements, performed at room temperature on at least 10 diodes of each specimen, yielded electron densities between 1 and 2×10^{18} cm^{-3}; this implies that the Fermi level is within 1 kT of the conduction-band edge if the density of states electron effective mass is assumed to be $m^*/m_0 = 0.15$. The extrapolated values of ϕ_{bn} from $1/C^2$ vs V curves, neglecting image force lowering, are also plotted in Fig. 2. In order to ascertain that the band-edge discontinuities do not introduce any errors in the evaluation of ϕ_{bn}, additional C-V data were obtained from planar Schottky barrier diodes as well as transverse and planar mercury probe contacts made directly to the epilayers. Internal photoemission spectroscopic measurements (IPS) were also made on selected specimens and confirmed the C-V data within 0.1 eV.[12] This good agreement between the various types of C-V and IPS measurements suggests that the misfit dislocations at the interface do not play a significant role in determining ϕ_{bn}. Nomarski interference microscopy of etched layers indicates that they are confined to the immediate vicinity of the interface.

Figure 3 shows that ϕ_{bn} is a linear function of E_g having the form

$$\phi_{bn} = 1.38E_g - 1.20 \qquad (2)$$

and, in view of the linear dependence of E_g on x from Fig. 2, we obtain

$$\phi_{bn} = 2.46 - 3.16x\,, \qquad (3)$$

provided that $x > 0.42$. Lorenz and Onton[6] have suggested that the transition from direct to indirect band gap occurs at $x = 0.32$ with $E_g = 2.06$ eV; for $x = 0.32$, a value of $E_g = 1.92$ eV is extrapolated from $E_g(x)$ in Fig. 2. In terms of Eqs. (2) and (3), ϕ_{bn} (0.32) = 1.45 eV at the transition point and presumably decreases with decreasing x to that of AlAs,[13] $\phi_{bn} = 1.2$ eV. Clearly, the ternary alloy in $In_xAl_{1-x}As$ does not follow the common anion rule[14] and the corresponding $\phi_{bn}(x)$ is, in many respects, qualitatively similar to that of $Ga_xAl_{1-x}As$ measured by Best.[15] Furthermore, Eq. (2) suggests that $\phi_{bn} = 0$ for $x = 0.78$ and, for $x > 0.78$, it is to be expected that the surface of $In_xAl_{1-x}As$ might be accumulated in analogy to the properties of $In_yGa_{1-y}As$ for $y > 0.725$ (Ref. 16). In addition, this would suggest that the surfaces of p-type $In_xAl_{1-x}As$, for $x > 0.78$, may be inverted if the equilibrium surface Fermi level is determined by surface states which fix its position within the band gap.

In conclusion, the Schottky barrier height of Au on n-$In_xAl_{1-x}As$ has been measured as a function of composition for $0.45 < x < 0.55$, where ϕ_{bn} increases linearly with decreasing indium content. For $x < 0.45$, the barrier height is assumed to peak at 1.45 eV at the direct-indirect band gap transition and then to decrease to 1.2 eV for $x = 0$. C-V and IPS measurements from this study suggest that the interfacial misfit dislocations do not play a significant role in determining ϕ_{bn}.

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SCHOTTKY-BARRIER HEIGHT OF $In_{0.43}Al_{0.57}As$

Indexing term: Semiconductor devices and materials

The Schottky-barrier height of *n*-type $In_{0.43}Al_{0.57}As$ grown by molecular-beam epitaxy on (100)-oriented *n*-type InP substrates measured by capacitance/voltage and internal photoemission measurements is $\phi_{Bn} = 1.2 \pm 0.1$ eV, comparable to that of AlAs and substantially larger than that of $In_{0.52}Al_{0.48}As$.

Relatively little is known about the synthesis and properties[1-3] of the ternary III-V semiconducting alloys $In_xAl_{1-x}As$ except for $In_{0.52}Al_{0.48}As$, whose lattice constant matches that of InP and therefore can be grown[4,5] in the form of epitaxial layers on *n*-doped, *p*-doped or semi-insulating (SI) substrates. The lattice constant of this alloy also matches that of the high-electron-mobility ternary alloy $In_{0.53}Ga_{0.47}As$ employed for a variety of electronic and electro-optic devices.[6-10] Barnard *et al.*[4] and Ohno *et al.*,[5] using molecular-beam epitaxy (MBE), have grown $In_{0.52}Al_{0.48}As$ as a buffer for $In_{0.53}Ga_{0.47}As$ and as an intermediate layer between it and a superposed metal electrode to increase the effective barrier height between them.

The composition of liquid-phase epitaxially grown $In_xAl_{1-x}As$ lattice-matched to InP was determined by Nakajima *et al.*[3] using Cu Kα X-ray diffraction to evaluate the lattice constants with the InP (400) reflection peak as a standard and deriving the fractional In concentration by means of Vegard's law. The corresponding room-temperature fundamental bandgap, $E_g(300\text{ K}) = 1.42$ eV, was then related to the photoluminescence emission peak (PL). Davies *et al.*[1,2] investigated the composition dependence of the fundamental bandgap of $In_xAl_{1-x}As$ for $0.46 \leq x \leq 0.56$ using double-crystal X-ray rocking curves to determine the lattice constants, allowing for the tetragonal distortion of the epilayers to calculate x and to relate it to E_g obtained from PL data measured at 4 K and 300 K. Exact lattice-matching to InP was obtained for $x = 0.523$ with $E_g(4\text{ K}) = 1.508$ and

$$E_g(300\text{ K}) = 1.450 + 2.29(0.523 - x) \quad (1)$$

Ohno *et al.*[11] have investigated the synthesis and properties of *n*-type $In_{0.52}Al_{0.48}As$ lattice-matched to InP, and from *C/V* measurements derived a barrier height $\psi_{Bn} = 0.80$ eV. In the course of establishing the proper epitaxial growth parameters which would produce, on our MBE machine, the same alloy, we have also grown some layers of the compound $In_{0.43}Al_{0.57}As$ whose lattice constant is mismatched with respect to its (100)-oriented Si- or Sn-doped, $n = 2 \times 10^{17}/\text{cm}^3$, InP substrates. This was done after arsenic stabilisation[12] of the InP surfaces, as determined by means of high-energy electron diffraction, while the substrates were held at a temperature of 500°C. X-ray double-crystal rocking curves using the (400) reflection of Cu Kα radiation were employed to determine the lattice constant; then, by assuming that the elastic stiffness coefficients are the same as those of $In_xGa_{1-x}As$, a correction was made for tetragonal distortion in calculating the composition of the epilayers.[13,14] We found an Al content of 0.575, i.e. $x = 0.425$, approximately 19% smaller than the In fraction of the lattice-matched composition of eqn. 1. Although the surfaces of the epilayers, whose thickness $0.5 < d < 2.0$ μm, appeared specular with Nomarski interference, microscopy etching revealed numerous misfit dislocations within a few nanometres of their InP interfaces. The electron concentration, obtained from Hall measurements at room temperature, is $n = 2.45 \times 10^{17}/\text{cm}^2$, and the mobility, $\mu = 145\ \text{cm}^2/\text{V s}$, is comparable to that of $Ga_xAl_{1-x}As$ with the same electron density. The density of states effective mass of these alloys is not known. If it is assumed to be $(m_n^*/m_0) \simeq 0.2$, then the Fermi level is within $2kT$ of the conduction band edge. The room-temperature PL shows a peak at 1.62 eV. In view of the relatively heavy doping and the uncertainties involved in the correction for the tetragonal distortion, this extrapolated from eqn. 1 for $x = 0.425$.

Schottky-barrier diodes were made of epilayers grown on the *n*-doped InP substrates. Their surfaces were lightly etched in a buffered HF solution to remove their native surface oxides. Au or Al circular electrodes were then vacuum-deposited and their substrates were mounted either on TO-5 headers or copper blocks. To circumvent any effects attributable to the $In_{0.42}Al_{0.58}As$/InP heterojunction interface, planar Schottky diodes were also made of the same epilayers with the same metal electrodes.

Current/voltage (*I/V*) measurements, such as that shown in the inset of Fig. 1, are qualitatively similar to those obtained on lattice-matched alloy Schottky-barrier diodes.[15] However, their ideality factor is too large for reliable barrier-height measurements. Capacitance/reverse-bias voltage (*C/V*) data obtained on both transverse and planar configuration Schottky diodes gave results similar to that shown in Fig. 1; the extrapolated value, considering the Fermi level to be within $2kT$ of the conduction band, is the barrier height ϕ_{Bn}. These measurements were augmented by *C/V* data obtained

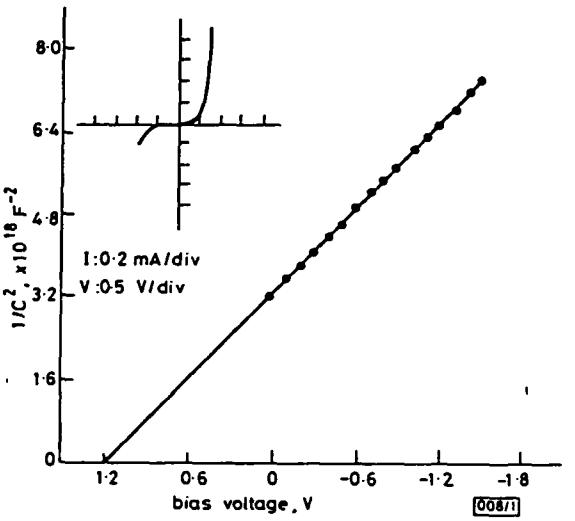

Fig. 1 *$1/C^2$ against applied reverse-bias voltage for an Al/$InAl_{0.43}As_{0.57}$ Schottky diode at room temperature*

The electron concentration calculated from the slope of this curve is $5 \times 10^{17}\ \text{cm}^{-3}$, in reasonable agreement with $n = 3 \times 10^{17}\ \text{cm}^{-3}$ obtained from Hall measurements; the inset shows a typical room-temperature *I/V* characteristic of such a diode

with both transverse and planar mercury probe contacts made directly to the epilayers. We find $\phi_{Bn} = 1.2 \pm 0.1$ eV, irrespective of the nature of the metallic contact, type of contact or device configuration.

We have also determined ϕ_{Bn} from internal photoemission data obtained on these Schottky diodes, assuming that this alloy has a direct gap. Fig. 2 shows that the extrapolated square root of the normalised photoresponse as a function of the incident energy $\phi_{Bn} = 1.2$ eV, in good agreement with the *C/V* data. In contrast, Ohno *et al.*[16] found from *C/V* measurements made on $In_{0.52}Al_{0.48}As$ that $\phi_{Bn} = 0.80$ eV, while Hsieh *et al.*,[15] using internal photoemission, ostensibly on the same alloy, found $\phi_{Bn} = 0.64$ eV and from *I/V* measurements $\phi_{Bn} = 0.53$ eV. We have also made *C/V* measurements on similar *n*-doped Schottky-barrier diodes of the lattice-matched alloy $In_{0.523}Al_{0.477}As$ grown on our MBE machine. Its composition was determined from double-crystal X-ray rocking curves in the above-described manner, and the barrier height was found to be $\psi_{Bn} = 0.81$ eV, in excellent agreement with the results of Ohno *et al.*[11,16] Evidently the Schottky-barrier height of our $In_{0.43}Al_{0.57}As$ layers is the same as that of AlAs[17] and about twice that of $In_{0.52}Al_{0.48}As$. Further work is under way on the other, non-lattice-matched, $In_xAl_{1-x}As$ alloys. However, it is not clear, as yet, whether ϕ_{Bn} has a systematic dependence on composition similar,[18,19] perhaps,

Electro-optical properties of III-V compound semiconductors for spatial light modulation applications

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Abstract

Electroabsorption and electrorefraction properties of bulk and multiple quantum well structures made from III-V compound semiconductor materials are discussed in this paper. The large electroabsorption that has already been observed is suitable for spatial light modulation. The potential advantages for using these structures for spatial light modulation include high speed of response and monolithic integration with detectors and electronic devices on the same chip. Variations of the electro-optical properties such as absorption wavelength, birefringence, nonlinearity and speed of response as a function of structural composition and thicknesses may offer opportunities for creative bandgap engineering that can be used eventually to tailor the material properties to suit specific device requirements

1. Introduction

Lasers, detectors and high-speed transistors have already been realized in III-V compound semiconductors based on GaAs and InP substrates. Heterojunction, quantum well and superlattice III-V compound semiconductor structures have demonstrated unique electronic and optical properties such as high mobility in modulation doped materials, large nonlinear optical coefficients and sharp tunable exciton lines at room temperature. Thus, if there is a materials technology that can become the basis for advancing the future of high-speed optical/electronic technology with far reaching consequences in optical computing, signal processing and communication, similar to that of silicon in microelectronics, then it is likely to be that of the III-V compound binary semiconductors and related ternary and quaternary alloys.

The spatial light modulator (SLM) is a key component for optical computing and signal processing. Two-dimensional spatial light modulator arrays with a large number of pixels which will require low switching energy, have a low threshold, that can be used in cascades (including three-terminal operation, same input and output wavelength), can perform a variety of logic function, will have high speed, good sensitivity and large dynamic range are urgently needed. In this paper, we shall examine some of the electro-optical properties of III-V compound semiconductors which may be used for spatial light modulation applications.

Consider a SLM array which consists of a large 2-dimensional array of unit cells. For an optically addressed SLM, an optical signal carrying a given piece of information is detected and is transformed into an electrical signal in each unit cell. Operations such as thresholding may be performed. An efficient light modulator will then modulate the transmission (or reflection) of a second incident optical beam according to the processed electrical signal. Alternatively, the processed electrical signal can be supplied electronically (such as through a CCD array) without the first optical beam. In either case, since sensitive and efficient detectors have already been demonstrated in III-V compound semiconductors, the key issue is how to make an efficient optical input/output switch (or a modulator) which will have high speed while requiring low power for switching (or modulation). Thereafter, the issues to be met, include, among others, the integration of the detector, the switch and other electronic devices in a unit cell.

For any input/output switch (or modulator) in a unit cell of an SLM, the processed electrical signal is applied to the electrodes that are fabricated on the surface by planar fabrication techniques. The separation of the electrodes is typically of the order of 10 μm so that there is good resolution for the array. Regardless of the electrode geometry, a small unit cell implies that the penetration of the electric field in the direction normal to the surface is small. Thus significant depth of modulation must be achieved for the normally incident radiation within only a few micrometers distance of propagation. Since the conventional linear electro-optical coefficient of all the III-V compound semiconductors is small ($r \sim 10^{-12}$ M/V), it is not possible to obtain a significant phase shift of optical radiation within a few micrometers of distance of propagation. Thus electro-absorption and electrorefraction become the principal mechanism through which efficient modulation can be realized in III-V compound semiconductors.

2. Electro-absorption and electro-refraction in bulk III-V compound semiconductors

Consider first a direct bandgap III-V compound semiconductor such as GaAs or InP. There is an abrupt increase in the absorption of optical radiation if its wavelength is less than a critical value called the absorption edge. The critical wavelength is equal to the bandgap energy, E_g, times the velocity of light, C, divided by the Planck's constant, h. At longer wavelength the absorption is nearly negligible. However, the position of this absorption edge (i.e., E_g) can be shifted to a longer wavelength and broadened by the

application of an electric field in accordance with the Franz-Keldysh effect[1]. If laser radiation of a wavelength slightly longer than the absorption edge is transmitted through a semiconductor sample, then its attenuation will be increased by the applied electric field because of the consequent shift and the broadening of the absorption edge, defined as electro-absorption (EA). From basic principles in solid-state physics, we know that there is also a change of refractive index associated with any absorption line or absorption edge. Thus, associated with EA, there is always a change in refractive index produced by the applied electric field at optical wavelengths near the absorption edge, called electro-refraction (ER). EA in GaAs has been measured many years ago by Stillman et al[2] and it has been used to make electro-optic modulators[3]. ER in GaAs and InP has been reported recently by Van Eck et al[4]. Electro-optical modulation in InGaAsP/InP diodes has been reported by Bach et al[5]. Figures 1 and 2 show the EA and the ER effect obtained at the University of California, San Diego (UCSD) in InP and in GaAs. Clearly, a large change of absorption coefficient $\Delta\alpha$ on the order of tens of cm^{-1} and a large change of index Δn on the order of 10^{-3} can be obtained. An EA modulator with extinction ratio of 20 dB at 6 V has been demonstrated in strip loaded InGaAsP planar waveguide 720 μm long by Noda et al[6]. Nevertheless, when the propagation distance, L, is only a few μm, $\Delta\alpha L$ is only of the order of 0.05 and $k\Delta nL$ is of the order of 0.01 radians. Thus EA and ER in the bulk materials are not large enough to produce an effective modulation depth within a single pass. The modulation effect for a given $\Delta\alpha$ or Δn can be enhanced by means of Fabry-Perot resonance (i.e., multiple pass modulation). For example, Figure 3 shows the calculated transmittivity of $In_{0.53}Ga_{0.47}As$ sample illustrated on the top part of the figure at the 1.75 μm wavelength range with doping concentration of 5×10^{15} cm^{-1} in the n InGaAs layer and $R_1 = R_2 = 0.9$. Nevertheless the required switching voltage (i.e., switching energy) is not as low as we would like.

3. Electro-absorption and electro-refraction in quantum well structures and exciton

A Multiple Quantum-Well (MQW) structure is made up of alternating layers of two materials with different bandgaps. The electrons and holes in such a structure are confined to the material with the smaller bandgap whose thickness is comparable to a DeBroglie wavelength (~ 50A to 150 A) and constitutes a quantum well. The material with the larger bandgap is called the barrier. One result of the carrier confinement within the quantum well is an optical absorption spectrum at room temperature which differs from that of the absorption edge in the same bulk material in two aspects. (1) The absorption edge of an MQW structure occurs at a wavelength corresponding to the transition between quantized energy levels in the well; (2) there is a much sharper and stronger excitonic absorption line near the absorption edge which can be shifted by an applied electric field[7]. Since the exciton absorption line is much sharper than the absorption edge of the bulk material, the $\Delta\alpha$ and the Δn produced by EA and by ER can be expected to be much larger than that of the $\Delta\alpha$ and the Δn obtained in bulk materials.

EA has already been observed in $Al_yGa_{1-y}As$/GaAs MQW structure grown by molecular beam epitaxy (MBE) method on GaAs substrate[7,8]. Recent results indicate that $\Delta\alpha$ as large as 1500 cm^{-1} have been obtained with 100 psec response time[9]. In this structure the $Al_yGa_{1-y}As$ layers are lattice-matched to GaAs. GaAs is the well and $Al_yGa_{1-y}As$, which has a larger E_g than GaAs, is the barrier. Thus the wavelength of the exciton absorption peak is shorter than the absorption edge of the GaAs substrates. While guided wave modulators have been demonstrated with 100 psec speed of response in such a structure[10], modulators for SLM applications with normally incident radiation would experience absorption from the GaAs substrate unless the substrate is removed. Goodhue at al[11] in the MIT Lincoln Laboratory has reported 60% depth of modulation in a CCD-addressed SLM using 60 layers of $Al_yGa_{1-y}As$/GaAs MQW with the GaAs substrate removed by selective etching. Figure 4 shows the optical transmission versus wavelength and bias of their sample.

EA has also been reported in a MQW PIN diode structure with 60 layers of $In_{0.53}Ga_{0.47}As$ wells (thickness ~ 75A) and $In_{0.52}Al_{0.48}As$ barriers (thickness ~ 75A) grown by MBE on and lattice-matched to (100) InP substrate by Wakita et al[12]. In this structure, $In_{0.53}Ga_{0.47}As$, the well material, has a fundamental bandgap of 0.75 eV at room temperature, while $In_{0.52}Al_{0.48}As$, the barrier material, has a fundamental bandgap of 1.46 eV at room temperature. Thus the exciton absorption lies in the 1.4 to 1.5 μm wavelength range depending on the thickness of the well. Figure 5 shows the transmission light intensity spectra of this diode as a function of reverse bias.

At UCSD, we have fabricated MQW structures of $In_xGa_{1-x}As$/GaAs grown by MBE on GaAs substrates with $x \leq 0.2$. In this case the $In_xGa_{1-x}As$ is the well, and GaAs is the barrier. $In_xGa_{1-x}As$ is not lattice-matched to the GaAs substrate. Cross sectional transmission electron microscopy of such a sample have shown no dislocation in the $In_xGa_{1-x}As$ layers and their barriers. In other words, it is possible within certain limits to vary the composition and the thickness of the well while keeping the lattice constant parallel to the MQW interface fixed at the value of the substrate. Such an MQW structure is called a strained layer structure (SLS). Since the E_g of the well is smaller than that of GaAs, exciton absorption occurs at a wavelength longer than the absorption edge of the GaAs. There is no need for removing the GaAs substrate for the normally incident radiation in SLM applications. Figure 6 shows the measured intensity transmission and

absorption coefficient as a function of wavelength at various bias voltages for an undoped MQW structure that consists of 10 layers of $In_{0.13}Ga_{0.87}As$ wells (100A thick) and GaAs barriers (150A thick), sandwiched between a 3000A GaAs buffer layer and a 3000A n^+ cap layer of GaAs, on a p^+ GaAs substrate. At 2 V, corresponding approximately to an electric field of 36 KV/cm in quantum wells, the maximum change of transmission is 0.064 at 0.950 μm wavelength. Such a rate of modulation, on a per-well basis, is comparable to that reported for $Al_yGa_{1-y}As$/GaAs MQW structures.

In summary, EA in all three quantum well structures has $\Delta\alpha$ more than one order of magnitude larger than those in the bulk. Assuming that $\Delta\alpha = 2{,}000\ cm^{-1}$ and a propagation distance L of 3 μm, $\exp[-\Delta\alpha L] = 0.55$. Thus effective EA intensity modulation for SLM can be obtained in $Al_yGa_{1-y}As$/GaAs MQW, in $In_xGa_{1-x}As$/GaAs MQW or in $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ MQW. No ER data is available yet.

4. Comparison of the properties of the MQW structures for SLM applications

Although EA and ER occur in all three MQW structures, the optical and electronic properties of these structures are not the same.

$In_{0.53}Ga_{0.47}As$ has an effective mass nearly a factor of two smaller than that of GaAs. Its mobility values reach up to 9500 cm^2/V-sec in high purity materials. Potential applications of $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ MQW and superlattice structures include a variety of FETs, modulation-doped two-dimensional electron gas devices and phototransistors with response in excess of 1 GHz. Thus in the long range, this MQW structure could yield SLM's with an extremely high speed of response. This is the potential advantage of this material system. The principal disadvantages of this structure for SLM application are (1) its long wavelength of operation and (2) the use of InP as substrates. The distance of propagation required for obtaining a given depth of modulation is larger at the longer wavelength. Silicon detectors cannot be used at the long infrared wavelengths, while good avalanche photodiodes and high-speed phototransistors are still in a development stage. Commercially available InP substrates are more expensive and not as high in crystallographic perfection as GaAs substrates.

The $Al_yGa_{1-y}As$/GaAs system and the $In_xGa_{1-x}As$/GaAs for $x \leq 0.25$ system are in some respects similar to each other in that they both use GaAs as substrate and both operate in the near infrared wavelength where silicon detectors are quite sensitive. Because of these two factors, they are more likely to be used for SLM applications in the immediate future. However, the $In_xGa_{1-x}As$/GaAs system is a strained layer structure whose long term stability is not yet known. The $Al_yGa_{1-y}As$/GaAs system needs to have its GaAs substrate etched away, resulting into a weak physical structure[11]. There are deep level centers associated with Al which may affect the ultimate speed of SLM[13]. On the other hand, the range of wavelength available from GaAs diode lasers is suitable for EA modulation using the $Al_yGa_{1-y}As$/GaAs system, while radiation from a dye laser is needed for EA modulation using the $In_xGa_{1-x}As$/GaAs system. The $Al_yGa_{1-y}As$/GaAs system is at this time the most commonly investigated quantum well structure. Conversely much is still unknown about the properties of the strain layer structures (SLS). However, the SLS may also offer new opportunities such as tuning of the bandgap E_g and creating artificial birefringence and nonlinearity by strain.

5. Conclusions

Although much is still unknown about the fundamental properties of the MQW structures, the known properties of these structures have already demonstrated their attractiveness in SLM applications. The tunability of the exciton absorption wavelength with respect to well thickness[14], the difference in exciton absorption with respect to TE and TM polarization of light in a waveguide[12], the difference in EA with respect to the orientation of the modulation electric field[7], the possibility of using ternary or quaternary compounds for changing the well (or the barrier) composition[15], the use of strain to tune the bandgap or to create artificial birefringence and nonlinearity in SLS, the use of bandgap discontinuity for creating local electric field and charge distribution and the potential for integrating these monolithically with detectors, phototransistors and other electronic devices are all opportunities for creative "bandgap engineering" that can be used eventually to tailor the material properties to suit specific device requirements.

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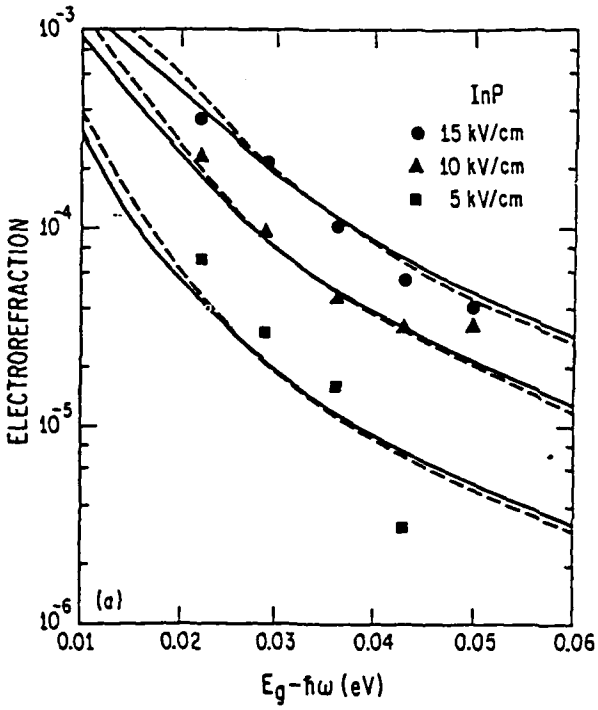

Figure 1A. Electrorefraction in InP. The vertical scale is the change of the refractive index Δn. The curves represent theoretical predictions for the three electric field strength. The points represent experimental data for the same three electric field strength. The solid curves are based on the theory of D.E. Aspnes and N. Bottka, in Semiconductors and Semimetals, edited by R.K. Willardson and Albert C. Beer (Acad. Press, NY, 1972) Vol. 9, pp. 457-543. The dashed curves are based on the corrected theory of H.D. Rees in Solid State Communication, 5, 365(1967).

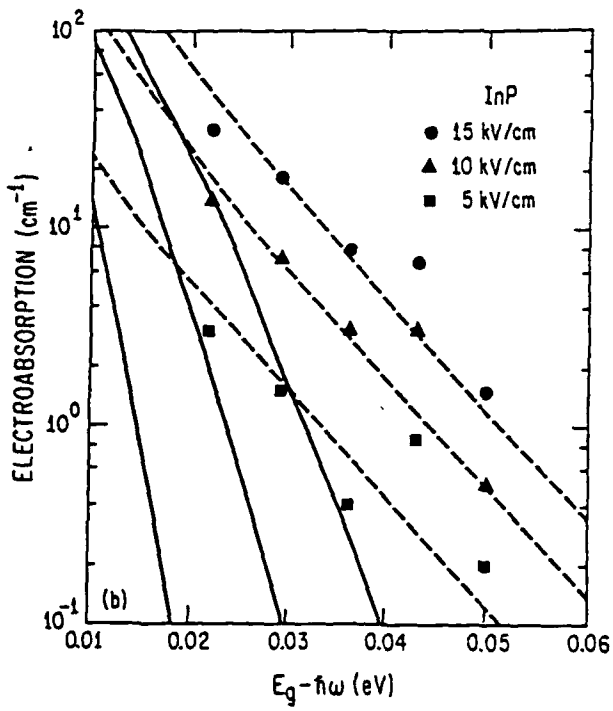

Figure 1B. Electroabsorption in InP. The vertical scale is the absorption coefficient. The curves represent theoretical predictions for the three electric field strength. The points represent experimental data for the same three electric field strength. The solid curves are based on the theory of D.E. Aspnes and N. Bottka. The dashed curves are based on the corrected theory of H.D. Rees.

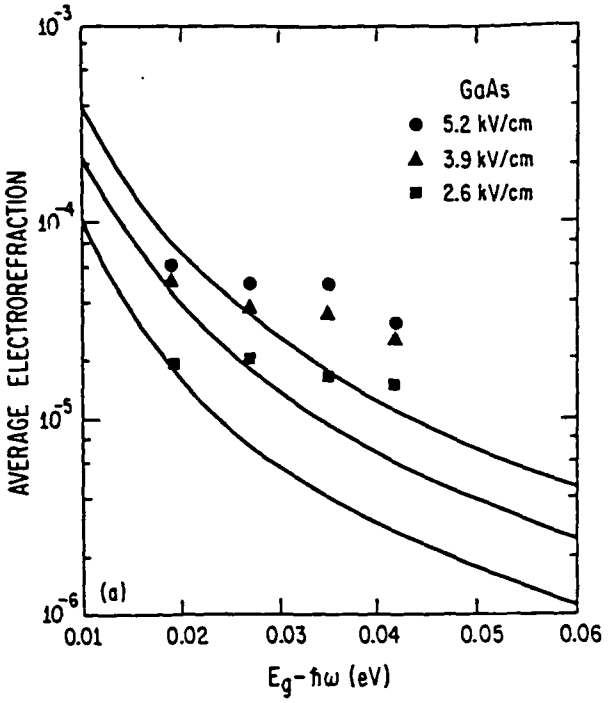

Figure 2A. Electrorefraction in GaAs. The vertical scale is the change of refractive index Δn. The points represent experimental data for three different average electric fields. The curves represent theoretical predictions for the same electric field based on the theory of D.E. Aspnes and N. Bottka. In the GaAs sample the electric field is apparently non-uniform.

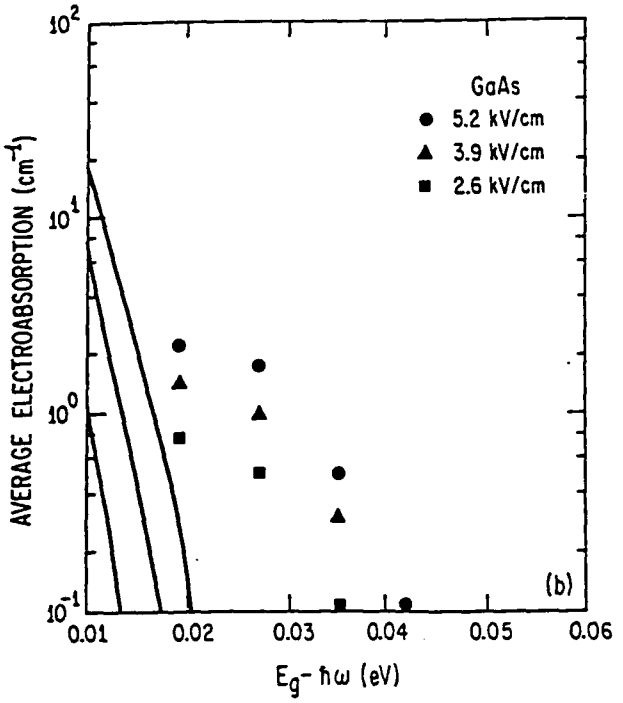

Figure 2B. Electroabsorption in GaAs. The vertical scale is the absorption coefficient. The points represent experimental data for three different average electric fields. The curves represent theoretical predictions for the same electric field based on the theory of D.E. Aspnes and N. Bottka.

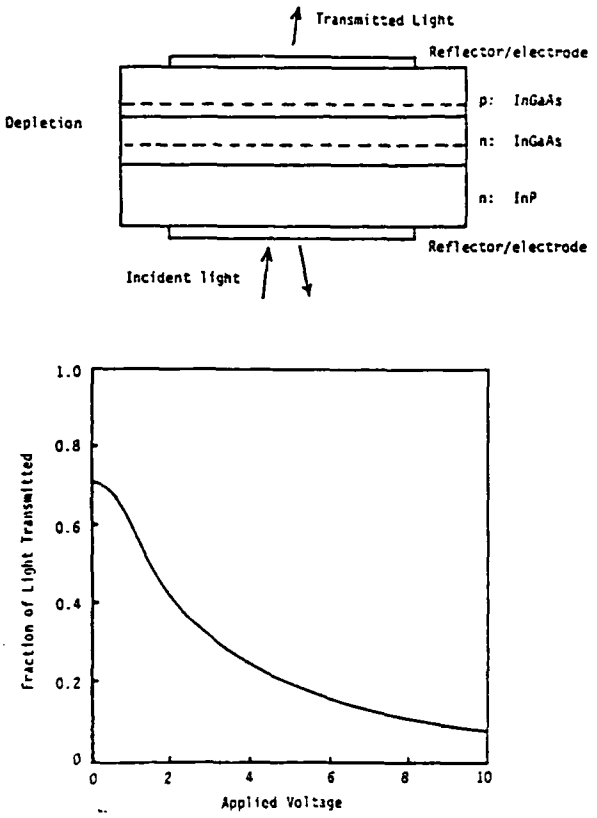

Figure 3. Transmittivity of $In_{0.53}Ga_{0.47}As$ Fabry-Perot Resonator at 1.75 μm wavelength. $N_D = 5 \times 10^{16}$ cm^{-3}; $R_1 = R_2 = 0.9$; maximum depletion depth = 0.54 μm; and maximum electric field = 375 KV/cm.

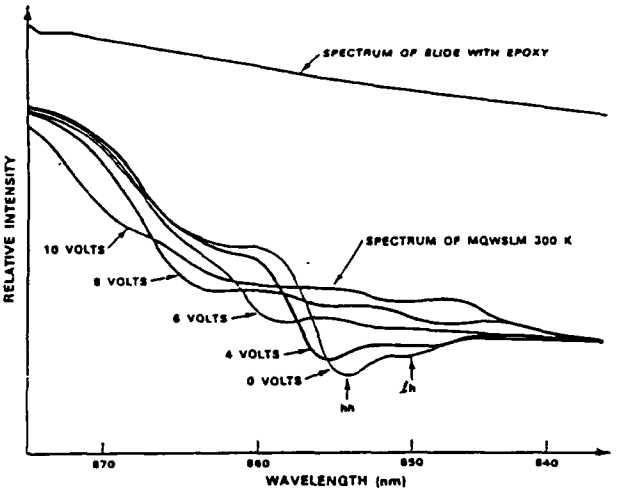

Figure 4. Optical transmission versus wavelength and bias of a GaAℓAs/GaAs MQW SLM structure which has been mounted with epoxy to a glass slide after the GaAs substrate is etched away. The absorption peaks labeled hh and ℓh are due to electron-heavy-hole and electron-light-hole excitons. This figure is reproduced from reference.

Franz–Keldysh electrorefraction and electroabsorption in bulk InP and GaAs

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Franz–Keldysh electrorefraction and electroabsorption were measured for semi-insulating InP and GaAs at several electric fields and several wavelengths near the absorption edge. For InP, the experimental results are described well by an effective mass approximation theory with a correction that accounts for the exponential absorption tail. It is shown that, at least in InP, Franz–Keldysh electrorefraction is under some conditions much stronger than the Pockels effect.

For the fabrication of electro-optic modulators, III-V semiconductors offer several advantages, such as low dielectric constant for high microwave phase velocity, and the possibility of monolithic integration of modulators with lasers, detectors, and electronic devices. A disadvantage of these materials is their relatively small Pockels coefficient. In this letter we report measurements of the Franz–Keldysh electrorefraction effect, which can be much stronger than the Pockels effect under some conditions, e.g., for optical wavelengths within several tens of nanometers of the absorption edge.

The Franz–Keldysh effect[1] is an electric field-induced change of the complex dielectric constant of a direct band-gap semiconductor, occurring at optical energies close to the band-gap energy. The Franz–Keldysh effect has two parts, electroabsorption (EA) and electrorefraction (ER), which are respectively changes of the absorption coefficient and refractive index due to an applied electric field. Franz–Keldysh electroabsorption has previously been measured[2] and used to make electro-optic modulators,[3] but only limited measurements of electrorefraction have been reported.[4] Here we report measurements of ER and EA at several electric fields and at several optical wavelengths near the absorption edge.

The materials used in this work were InP and GaAs. Semi-insulating wafers were used so that a large electric field could be applied across the entire wafer thickness. The InP sample was 100 μm thick and the GaAs sample 440 μm thick. Each sample was polished on both sides, and transparent electrodes of indium tin oxide were deposited on both sides so that light could propagate in the direction parallel to the electric field. The light source was an optical parametric oscillator driven by a pulsed dye laser. For EA measurements, transmission through the sample was measured both with and without the applied voltage. For ER measurements, the sample was placed in one arm of a Mach–Zehnder interferometer, and an attenuator was placed in the other arm to balance the absorption in the sample. As a voltage pulse was applied to the sample, the position of the interference fringe pattern was monitored with a photodetector. The photodetector current was amplified and sampled by an analog-to-digital converter and the result was averaged digitally. This measurement apparatus had a phase sensitivity of 10 mrad. From the change of fringe position the change of refractive index was calculated. All measurements were made at room temperature. To eliminate thermal changes of the refractive index and absorption coefficient, the voltage was applied to the sample in short pulses. To eliminate the effect of photogenerated carriers, the energy density of the incident light pulse was kept below about 10^{-7} J/cm^2.

The experimental data for InP are shown in Fig. 1. The electric field is assumed to be uniform throughout the sample. The solid curves represent the calculated Franz–Keldysh ER and EA according to an effective mass approximation (EMA) theory found in the literature.[1,2] The dashed curves represent a correction due to the exponential absorption tail,[5] which has the measured functional form $\alpha = 2500\ \mathrm{cm}^{-1} \times \exp[(\hbar\omega - E_g)/8.0\ \mathrm{meV}]$ for our sample. For ER there is good agreement between the EMA theory and experiment, and the correction due to the absorption tail is relatively small. For EA the experimental data are orders of magnitude greater than the EMA theory. The corrected theory, however, fits the experimental data very well, except for the anomalous bump at $\hbar\omega = E_g - 0.043$ eV.

In our GaAs samples the current is a very nonlinear function of voltage; it also varies with time. This suggests that the electric field is both nonuniform and unstable. This is consistent with previous reports of current nonlinearity[6] and instability[7] in bulk semi-insulating GaAs. It is possible to measure the phase change and transmission change due to a voltage applied to the sample, but since the electric field is nonuniform we cannot deduce from this measurement the change of refractive index and absorption coefficient caused by a particular local electric field. We can only measure the average change of refractive index and average change of absorption coefficient, which are plotted in Fig. 2 as a function of wavelength for several different values of the calculated average electric field. Neither the average EA data nor the average ER data follow the form of the theory, but the discrepancy is much greater for EA. This is to be expected since according to the EMA theory EA is much more nonlinear as a function of electric field than ER and is therefore likely to be much more sensitive to nonuniformity of the electric field.

For the purpose of comparing Franz–Keldysh ER with the Pockels effect, we use the figure of merit $\Delta n/E$, the change of refractive index divided by the applied electric field. For the Pockels effect in InP, this ratio has the value[8] $\Delta n/E = 1/2\, n^3 r_{41} = 26 \times 10^{-12}$ m/V. The maximum value that we have measured is $\Delta n/E = 240 \times 10^{-12}$ m/V. For the widely used electro-optic material $LiNbO_3$, the value is[9]

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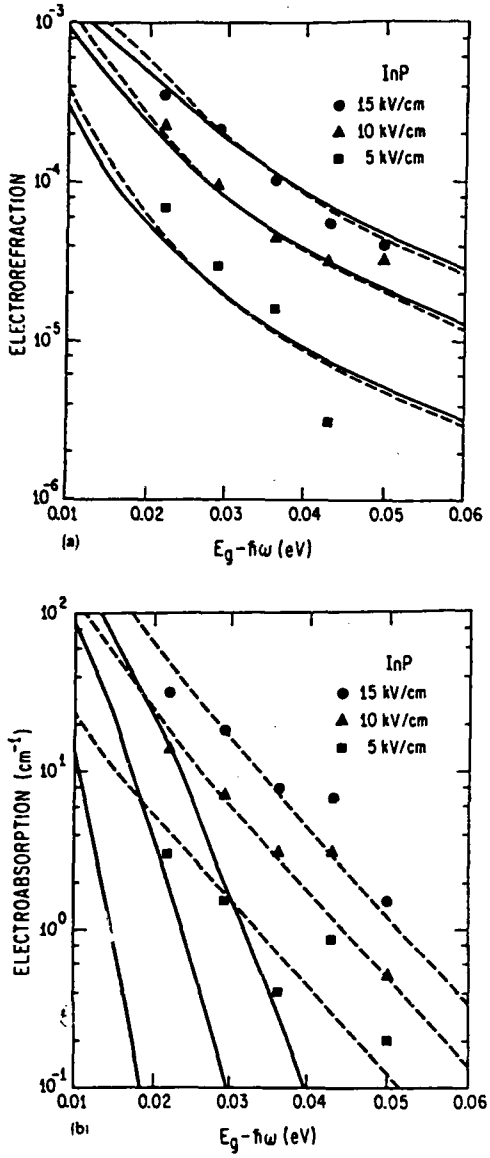

FIG. 1. (a) Electrorefraction and (b) electroabsorption in InP. The points represent experimental data for three different electric fields. The curves represent theoretical predictions for the same three electric fields. The solid curves represent the EMA theory (Ref. 1) and the dashed curves represent the corrected theory (Ref. 5).

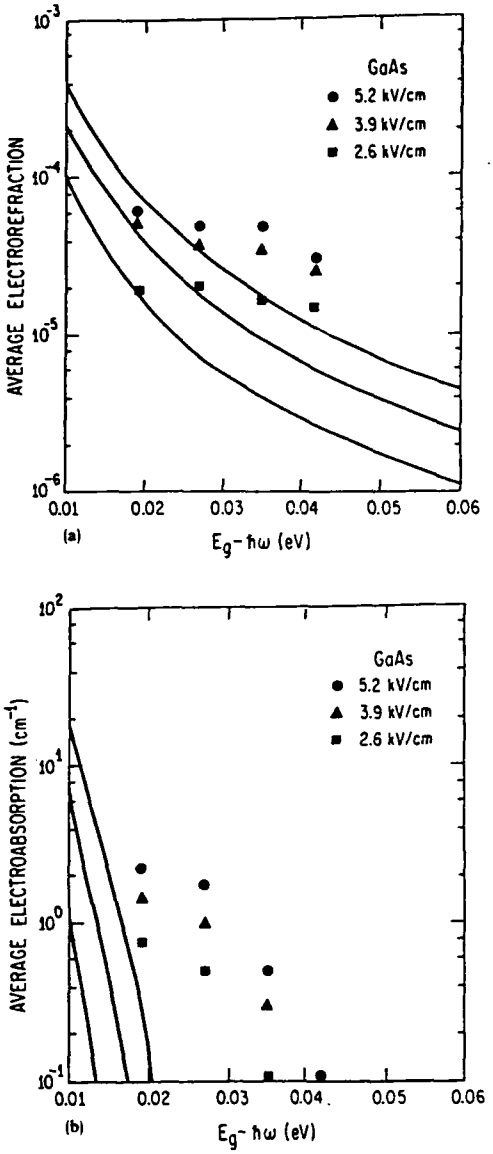

FIG. 2. (a) Average electrorefraction and (b) average electroabsorption in GaAs. The points represent experimental data for three different average electric fields. The curves represent predictions of the EMA theory (Ref. 1) for the same three electric fields. In the GaAs sample the electric field and thus the electrorefraction and electroabsorption are apparently nonuniform, so we can compute only the average along the optical path of these quantities.

$\Delta n/E = 1/2\ n_e^3 r_{33} = 164\times10^{-12}$ m/V. Thus the Franz–Keldysh electrorefraction effect can offer electro-optic modulation an order of magnitude greater than the Pockels effect in the same material, and even greater than the Pockels effect in $LiNbO_3$. Much larger electric fields can be achieved in the depletion layer of reverse-biased p-n junctions than in the semi-insulating materials used in this work; thus much larger $\Delta n/E$ can probably be achieved than reported here. If multiple quantum well structures are used, then the sharp exciton lines might provide even greater Δn.

For many device applications of electrorefraction, such as phase modulators, absorption and electroabsorption are undesirable side effects. A measure of the utility of electrorefraction is the ratio $\Delta n/k$, where n and k are the real and imaginary parts of the refractive index respectively, and the absorption coefficient α is equal to $4\pi k/\lambda$. For a useful phase modulator $\Delta n/k \gg 1$ is desired. The exponential absorption tail is fairly strong in Fe-doped semi-insulating InP,[10] with the result that $\Delta n/k < 1$, within the range of wavelength and electric field of our measurement. This suggests that semi-insulating InP is not useful for electro-optic phase modulation within this range of wavelength and electric field. Perhaps undoped InP would be more useful because of its weaker absorption tail.[10] The theory suggests that a large $\Delta n/k$ ratio can be realized by using larger electric fields and operating at wavelengths farther from the absorption edge.

Novel devices might be implemented which would make use of both ER and EA. For example, a waveguide intensity modulator could utilize both attenuation due to EA and mode extinction due to ER. A second example is a semiconductor Fabry–Perot étalon tuned to a transmission peak when no electric field is applied. An electric field would cause transmission to drop in the vicinity of the peak and simultaneously detune the etalon, causing an even greater drop in transmission.

In summary, electrorefraction and electroabsorption have been measured in InP and compared with the Franz–Keldysh theory. The EMA theory is in good agreement with the electrorefraction data. For electroabsorption the EMA theory is inadequate, but a theory that accounts for the exponential absorption tail is in good agreement with the data. For GaAs the electrorefraction and electroabsorption data cannot be inferred from the measurement because of the nonuniformity of the electric field in the sample. The results of the InP measurement show that Franz–Keldysh electrorefraction may provide a good alternative to the Pockels effect for some applications.

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Electrical properties and applications of $In_xAl_{1-x}As/InP$

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Prototype depletion mode heterojunction-insulated gate field-effect transistors using $In_{0.43}Al_{0.57}As$ as a quasigate insulator were fabricated and their low-frequency properties were evaluated. Typical extrinsic transconductances of $g_m = 20$ mS/mm were obtained for devices with gate length of 6 μm which exhibited no direct current (dc) drain current instabilities. A qualitative fit to a metal–insulator field-effect transistor (MISFET) model was obtained using the material parameters of the InP and $In_{0.43}Al_{0.57}As$ epilayers and assuming that this quasi-insulator could be represented as a conventional insulator. The equilibrium surface potential has been determined to be -0.05 eV. Capacitance–voltage (C–V) and conductance-frequency measurements made on similar heterojunction capacitors show that the maximum interface state density is in the low $10^{11}/cm^2$ eV range and confirm the slight depletion of the InP surface.

I. INTRODUCTION

The search for high-speed field-effect transistors intended for both digital and analog integrated circuit applications has led to the evolution of heterostructure-insulated gate field-effect transistors (HIGFETs) employing an undoped, depleted semiconductor layer as a quasi-insulator.[1–4] Such heterojunction transistors have been made of GaAs as well as $In_xGa_{1-x}As$. It appears that lattice matching between the quasi-insulator and the active channel is not an absolute requirement and in some cases a lattice-mismatched semiconductor used as a gate insulator may even be advantageous.[5–7] InP has some specific advantages for transistor applications which are listed in Table I.[8,9]

Previously, research on InP FETs has been concerned primarily with insulated gate FETs (MISFETs) employing homo- and heteromorphic gate insulating layers and with investigations of the density and distribution of surface and interface states present at various insulator/InP interfaces.[10] These interface states are thought to give rise to a number of problems detrimental to device performance, including the well-documented direct current (dc) device instability in which the channel current decays substantially with time.[11]

TABLE I. Comparison of some material parameters for InP, GaAs, and $In_{0.53}Al_{0.47}As$.

Parameters	InP	GaAs	$In_{0.53}Al_{0.47}As$
Energy gap (300 K) (eV)	1.34	1.42	0.75
Γ–L separation (eV)	0.61	0.33	0.61
Impact ionization threshold (eV)	2.10	1.7	
Threshold field for electron transfer (kV/cm)	11	3.6	3–4
Peak electron velocity (cm/s)	2.7×10^7	2.0×10^7	3.5×10^7
Thermal conductivity (300 K) (W/cm/K)	0.83	0.52	0.66
Drift mobility (300 K, $N_d = 10^{17}/cm^2$) (cm^2/V s)	2800	4600	9000
Static dielectric constant	12.38	13.13	13.82

A completely satisfactory gate insulator has not yet been found and the research for appropriate FET device configuration and fabrication techniques is still underway.

For this work, semi-insulating $In_xAl_{1-x}As$ has been used for the quasi-insulator. It has a relatively high surface barrier height, and a fundamental band gap which depends on the mole fraction x of indium present in the ternary alloy. The surface Schottky barrier has been reported by Lin *et al.*[12] to increase linearly with composition from $\phi_b \approx 0.8$ eV at the lattice-matched composition, $x = 0.52$, to $\phi_b \approx 1.2$ eV for $x = 0.43$, as presented in Table II. It is presumed that a high Schottky barrier might reduce the gate leakage current at the expense of lattice matching between $In_xAl_{1-x}As$ and InP.

II. TRANSISTOR FABRICATION AND PROPERTIES

InP epitaxial layers with thicknesses of 0.1 to 0.5 μm were grown by low pressure organometallic chemical vapor deposition (OMCVD) on semi-insulating (100)-oriented InP substrates. These undoped layers had good morphology and were n-type with electron concentrations on the order of $10^{16}/cm^3$ as determined by Hall measurements. The samples were etched using 1 HF: 1 HCl: 4 H_2O + 5 drops of H_2O_2 per 12 ml of solution to remove their native oxides prior to loading the samples into a modified Varian Gen II molecular–beam epitaxy (MBE) system. Residual oxides were removed by *in situ* heating followed by the growth of undoped

TABLE II. Some material properties of $In_xAl_{1-x}As$ grown by MBE at 500 °C.

Indium mole fraction of $In_xAl_{1-x}As$,	Schottky barrier height (eV)	Band gap (eV)	Lattice mismatch between InAlAs and InP ($\Delta a/a_0$)
0.52	0.80	1.45	7.98×10^{-5}
0.49	0.88	1.51	2.0×10^{-3}
0.46	1.05	1.58	3.98×10^{-3}
0.43	1.20	1.66	6.31×10^{-3}

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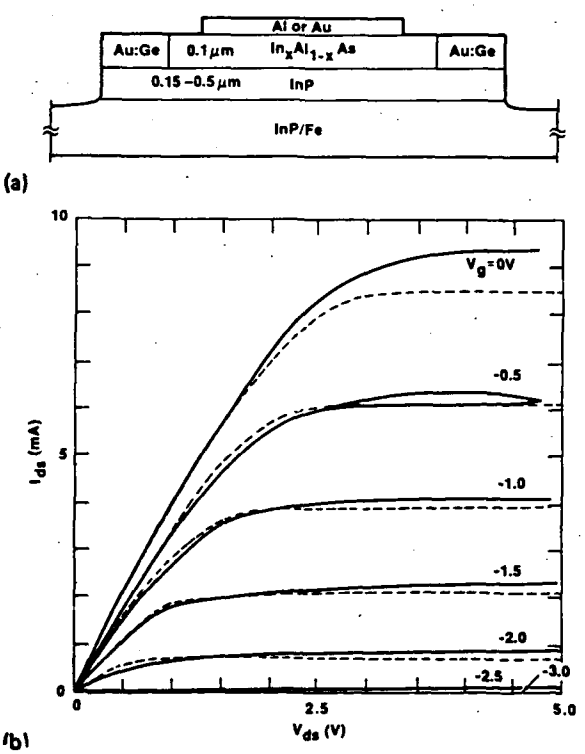
$In_{0.43}Al_{0.57}As$, nominally 0.1 μm in thickness, at a substrate temperature of 500 °C.

The transistor fabrication began with mesa isolation using 1 H_3PO_4: 1 H_2O_2: 38 H_2O which preferentially etches $In_xAl_{1-x}As$ at a rate of 1000 Å/min[13] and 1 HCl: 1 CH_3COOH to etch InP; source-drain pads were etched with the same phosphoric acid etch, metallized with AuGe eutectic and annealed in a reducing atmosphere at 375 °C for 15 min. Gate contacts were made by evaporating aluminum or gold electrodes. The device cross section is shown in Fig. 1(a).

Transistor characteristics of a representative depletion-mode HIGFET measured on a curve tracer are presented in Fig. 1(b) and they show good saturation and pinchoff of the drain currents. The threshold voltage is calculated to be -3.5 V. The reverse gate leakage current is <0.1 μA for gate biases up to -4 V. A positive gate voltage applied to the gate produces an enhancement of the drain current, consequently the transistor is not fully on at zero gate voltage.

The extrinsic transconductance of this prototype device, with the relatively large dimensions of 6-μm gate length, 250-μm gate width, and 8-μm source-drain spacing, InP doping density of $N_d = \sim 4\times10^{16}/cm^3$ and mobility, $\mu = 3000\ cm^2/V\ s$, is $g_m \sim = 20$ mS/mm. Work still underway leads us to believe that a reduction in gate length to 1 μm and an increase in N_d to the order of $N_d = 10^{17}/cm^3$ will yield values for $g_m > 150$ mS/mm.



. 1. (a) Schematic cross section of the $In_xAl_{1-x}As$/InP heterojunction ısulated gate transistor; (b) Solid line represents measured characteristics of $In_{0.43}Al_{0.57}As$/InP HIGFET obtained at 60 Hz. Dashed lines represent calculated values using Hill's model as discussed in the text. Parameters used: $In_{0.43}Al_{0.57}As$ with $\epsilon = 12.5$, $d = 0.1$ μm; InP with $N_d = 4.5\times10^{16}/cm^3$, $\mu = 3000\ cm^2/V\ s$, $v_{sat} = 1.5\times10^7$ cm/s, $D = 0.18$ μm, and band bending at zero gate bias of -0.05 eV; an interface state density at the $In_{0.43}Al_{0.57}As$/InP of $4\times10^{11}/cm^2$ eV and series source and drain resistances of 90 Ω each.

In order to determine if HIGFETs exhibit the same dc drain current instabilities as InP MISFETs, measurements were made by applying dc gate and source-drain voltages while monitoring the output drain current as a function of time. Figure 2 shows some results with the transistor sampled in both the linear and saturated regions. Based on this data, as well as from other preliminary measurements made over much longer time periods, the HIGFETs are considered to be free of major dc instabilities. These results compare favorably to the best data reported thus far on InP MISFETs.[14,15]

To qualitatively fit the HIGFET transistor characteristics, a model by Hill[16] has been used which was originally developed for MISFETs from the combined models of Pucel *et al.*[17] and Lile.[18] It is based on a two piece linear approximation of the velocity-field curve and it takes into account the presence of interface states, a "built-in" surface potential, and parasitic series source and drain resistances. Implicit in the use of this model is the assumption that the $In_xAl_{1-x}As$ insulating layer has the properties of a conventional insulator with a capacitance per unit area being given by $C_i = \epsilon/d_i$, where ϵ, is the composition dependent dielectric constant corresponding to a linear interpolation between the values of ϵ_{InAs} and ϵ_{AlAs}, and d_i is the layer thickness.

The best fit of this model to the experimental data is shown by the dashed curves in Fig. 1(b), where it was assumed that the surface InP is depleted at zero gate bias with a band bending of -0.05 eV, that the field-effect electron mobility is 3000 $cm^2/V\ s$ (the same as the Hall mobility), that an interface state density of $4\times10^{11}/cm^2$ eV is present at the quasi-insulator InP interface and that a series resistance of 180 Ω represents the region of the active channel which is not covered by the gate. In order to justify these assumed values, the properties of two-terminal heterojunction capacitors, made of the same materials, have been investigated. The preliminary investigations are described in the following section.

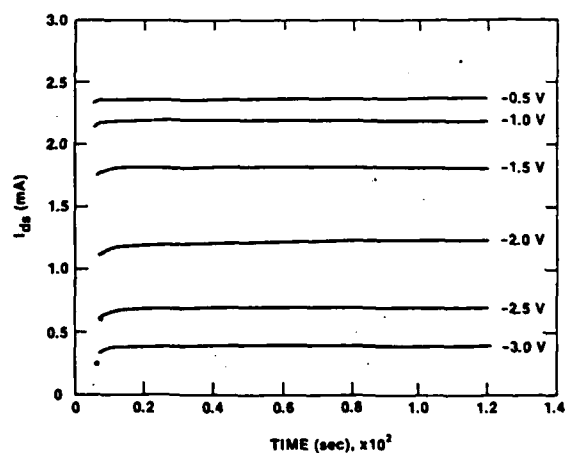


FIG. 2. Drain current vs time of HIGFET shown in Fig. 1(b) for a fixed $V_{ds} = 0.5$ V and $V_g = -0.5$ steps. For $V_g > -2$ V the transistor is in the linear region and for $V_g < -2$ V it is in the saturated region.

III. STRUCTURE AND PROPERTIES OF $In_xAl_{1-x}As$/InP HETEROJUNCTION (HJ) CAPACITORS

Heterojunction capacitors were made of $In_xAl_{1-x}As$/InP epitaxial layers similar to those used for the HIGFET but grown on sulfur-doped InP substrates with carrier concentrations $>10^{18}/cm^3$. The $In_xAl_{1-x}As$ layers were 0.1 μm thick with indium mole fractions of $x = 0.52, 0.49, 0.46$, and 0.43. Metal contacts were made to these structures by the vacuum deposition of aluminum electrodes with a circular area of 2.2×10^{-3} cm^2 or by using a mercury probe with contact area estimated to be 3.17×10^{-3} cm^2. Capacitance measurements were made at room temperature using an HP 4277A LCZ meter with frequencies between 10 kHz and 1 MHz, and gate bias sweep rates <0.1 V/s.

Figure 3 shows the capacitance dependence on gate voltage for HJ capacitors having $In_xAl_{1-x}As$ layers with $x = 0.42$ and $x = 0.57$. The calculated equivalent parallel plate capacitances of these samples are $C_i = 248$ and 242 pF, respectively. It is to be expected that the measured capacitance of HJ capacitors should approach their insulator capacitances when the surface becomes strongly accumulated. For small positive voltages the measured capacitance does increase, however, before it reaches the calculated values of C_i, large gate currents are drawn. We are interpreting the measured capacitance as a series combination of the capacitance of the totally depleted quasi-insulating $In_xAl_{1-x}As$ layer (C_i) and the capacitance of the depleted region extending into the InP. Therefore, the apparent saturation of the measured capacitance near zero gate bias suggests that interfacial states are being charged and are partially screening further depletion in the InP.

Using models developed principally for silicon MOS capacitors,[19] the ideal high frequency C–V curve was calculated for these HJ capacitors. Comparing point by point the theoretical and experimental C–V curves, it was possible to determine the explicit dependence of band bending, V_s, at the InP surface on the applied gate bias, V_g, as shown in Fig. 4(a).

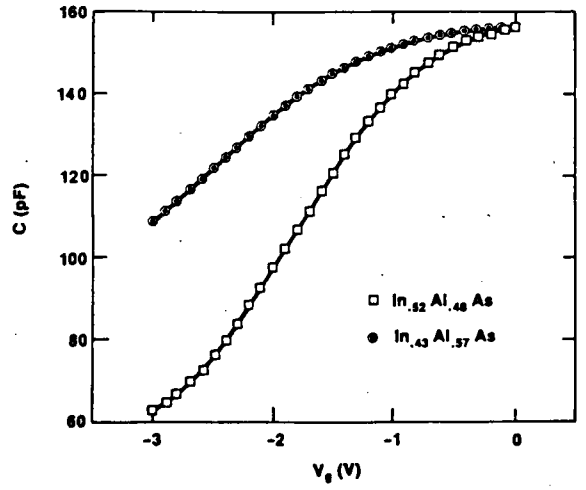


FIG. 3. C–V measurements made at a frequency of 1 MHz on HJ capacitors with $In_xAl_{1-x}As$ layers of $x = 0.52$ and 0.43, thickness $= 0.1\,\mu$m, and area of 2.2×10^{-3} cm^2.

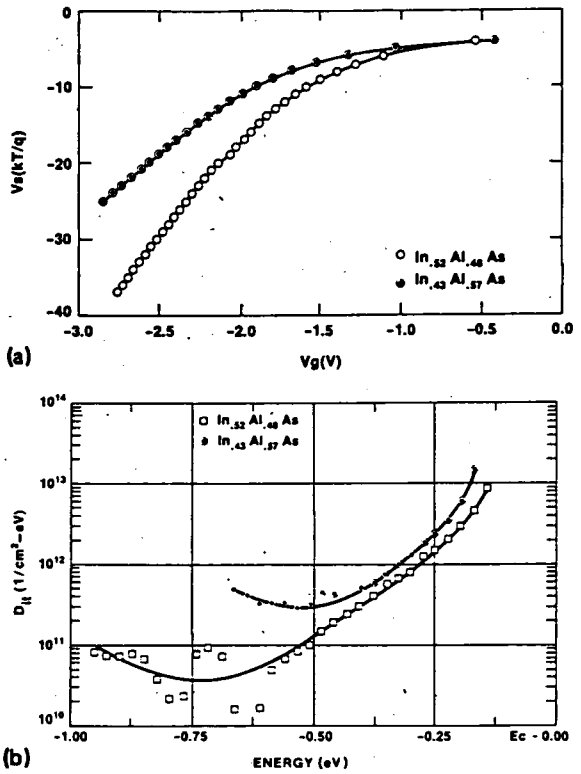


FIG. 4. (a) Calculated band-bending vs applied gate voltage from C–V data shown in Fig. 3 from data taken at room temperature. (b) Calculated density of interface states vs energy using Terman analysis.

The band bending at zero gate voltage, V_{SO}, is calculated to be $\sim$0.13 eV for these samples. V_{SO} did not appear to be a function of the composition of the $In_xAl_{1-x}As$ quasi-insulator. However the amount of applied gate bias necessary to bend the bands is dependent on x; it takes a larger applied gate voltage to move the surface potential an equivalent amount for compositions further from lattice matching. The interface state density, D_{it}, distribution in energy was extracted from the band-bending dependence on applied gate voltage using Terman analysis[19] by means of

$$D_{it} = (1/q)\left\{C_i\left[\left(\frac{\partial V_s}{\partial V_g}\right)^{-1} - 1\right] - C_s\right\}, \qquad (1)$$

where q is the electronic charge, C_i is the insulator capacitance of $In_xAl_{1-x}As$, V_s is the band bending, and C_s is the space charge capacitance of the InP layer. It is evident that the D_{it} versus energy in the band gap shown in Fig. 4(b) has the characteristic "U" shape and is similar qualitatively to D_{it} profiles reported for InP MIS capacitors[20]; it increases towards the band edges within the InP fundamental energy gap and decreases to a minimum of $<10^{11}/cm^2$ eV near midgap for the lattice-matched composition. The minimum value reported for InP MIS capacitors is $\sim10^{11}/cm^2$ eV near midgap.[21]

The density of interface state distribution in the band gap was also calculated from conductance versus frequency measurements. The model used for the calculations assumes a distribution of single-level interface traps that has a Gaus-

sian spatial distribution of band bending fluctuations.[19] To begin the analysis, the parallel conductance of the interface states was calculated from the measured data:

$$\langle G_p \rangle/\omega = (\omega C_i^2 G_m)/[G_m^2 + \omega^2 (C_i + C_m)^2], \qquad (2)$$

where G_p is the parallel conductance, C_i is the insulator capacitance of the $In_xAl_{1-x}As$, G_m is the measured conductance, ω is the measuring frequency, and C_m is the measured capacitance. The resulting plot of $\langle G_p \rangle/\omega$ vs ω contains a peak which represents the frequency at which the capacitor exhibits a maximum energy loss whose amplitude is used to calculate the interface state density. An example of one such plot is shown in Fig. 5(a). The measurement was repeated for different applied gate biases to calculate the interface state density as a function of band bending and the results are shown in Fig. 5(b). The minimum of D_{it} is in the low 10^{11}/cm^2 eV range, in good qualitative agreement with the Terman analysis of the C–V data as well as the transistor analysis. However, the distribution of the interface state density appears to be essentially independent of energy within the InP bandgap in contrast to the Terman analysis.

The lattice-mismatched quasi-insulator composition of $In_{0.43}Al_{0.57}As$ was chosen for the prototype depletion-mode

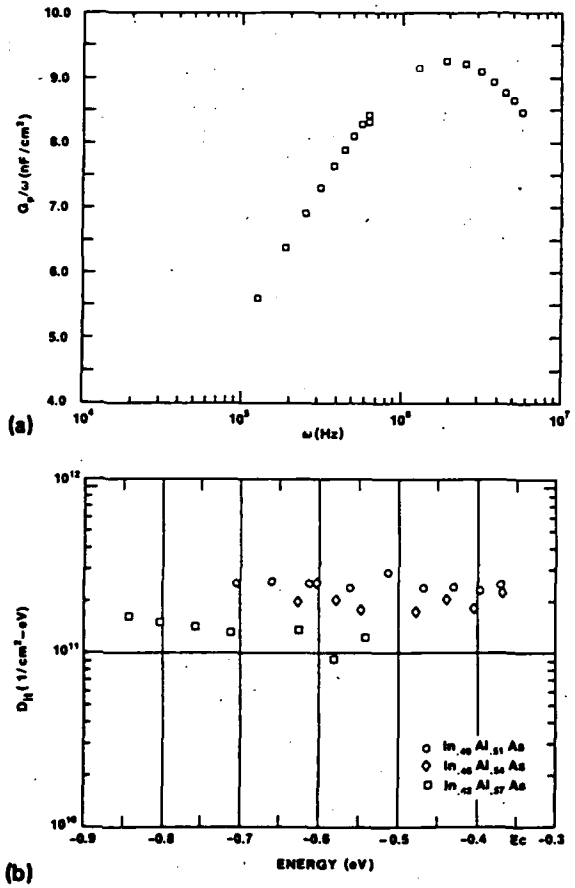


FIG. 5. (a) Equivalent parallel conductance data for an $In_{0.49}Al_{0.51}As$/InP HJ capacitor with $V_g = -0.3$ V. The $In_{0.49}Al_{0.51}As$ layer thickness is 0.1 μm and capacitor area is 3.17×10^{-3} cm^2; (b) Density of interface states vs energy calculated from parallel conductance vs frequency measurements made on HJ capacitors with $In_xAl_{1-x}As$ layers of $x = 0.49$, 0.46, and 0.43, thickness = 0.1 μm and area of 3.17×10^{-3} cm^2.

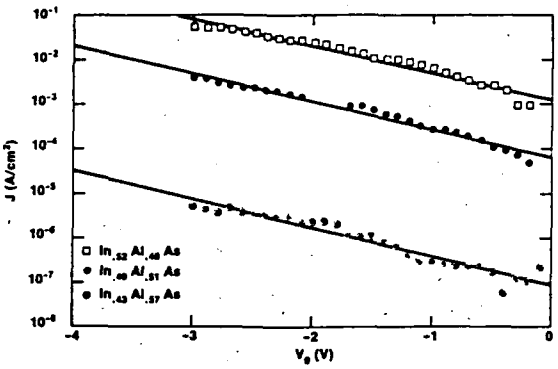


FIG. 6. Current density vs gate voltage through HJ capacitors with $In_xAl_{1-x}As$ layers of $x = 0.52$, 0.49, and 0.43, thickness = 0.1 μm, and area of 2.2×10^{-3} cm^2.

HIGFETs because of its large surface Schottky barrier height which was expected to reduce the gate leakage curent. Measurement of current density, J, as a function of gate voltage through the various HJ capacitors shown in Fig. 6 verify this expectation; they show an increase for decreasing aluminum mole fraction. The slope of the $\log(J)$ versus gate voltage is independent of composition but the current density increases by four orders of magnitude from $x = 0.43$ to $x = 0.52$.

IV. DISCUSSION

An equilibrium heterojunction band diagram applicable to the $In_xAl_{1-x}As$/InP heterostructure is suggested in Fig. 7 for the lattice-matched composition, whose conduction band edge discontinuity was determined by Caine *et al.*[22] to be 0.52 eV. The Schottky barrier in the $In_{0.52}Al_{0.48}As$ surface is taken to be 0.8 eV, and the surface potential of the InP is -0.1 eV which makes the potential drop across the totally depleted quasi-insulating $In_{0.52}Al_{0.48}As$ layer ~ -0.1 eV. It is assumed that, qualitatively, the same type of band

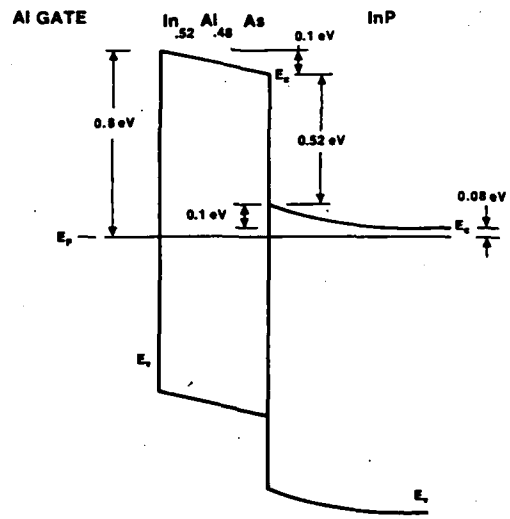


FIG. 7. Energy band diagram for the Al/$In_{0.52}Al_{0.48}As$/InP heterostructure.

diagram is applicable to heterostructures with lattice-mismatched $In_xAl_{1-x}As$ using higher Al mole fractions and correspondingly larger band gaps and barrier heights.

The origin of the Schottky barrier at the metal-$In_xAl_{1-x}As$ surface is attributed to Fermi level pinning by a high density of surface acceptor states. A negative sheet charge is assumed to be present at the $In_xAl_{1-x}As$/InP interface. At equilibrium, the negatively charged acceptor centers at the metal–$In_xAl_{1-x}As$ interface as well as this sheet charge, balance the positive space charge in the depleted InP layer and in the quasi-insulator.

Although the interfacial state density is increased slightly by using compositions of nonlattice-matched $In_xAl_{1-x}As$ to InP, the current density through the heterostructure is reduced considerably. The $In_xAl_{1-x}As$ compositions with a higher aluminum mole fraction do not provide an advantage in this respect.

V. SUMMARY

InP HIGFETs were made with lattice-mismatched $In_xAl_{1-x}As$ as a quasi-insulating gate layer and the properties of such devices were evaluated in terms of a MISFET model. Two-terminal heterojunction capacitor measurements validate the assumption that the *n*-type InP surface at equilibrium is slightly depleted in the immediate vicinity of the conduction band edge. The density of fast interface states determined from *C–V* measurements is in the high $10^{10}/cm^2$ eV range at midgap. These results are qualitatively confirmed by conductance measurement which suggest interface states that are energy independent and have typical values in the low $10^{11}/cm^2$ eV range.

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