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FOREIGN TECHNOLOGY DIVISION

PULSE CIRCUITS OF RADAR STATIONS

by

V.G. Grigor'yants

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EDITED TRANSLATION

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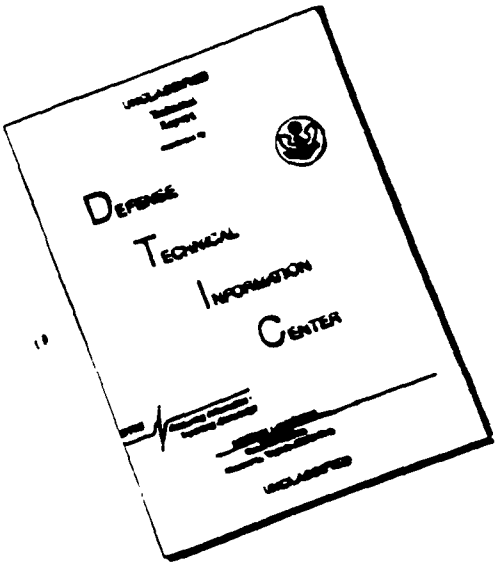

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О о	*О о*	O, o	Ю ю	*Ю ю*	Yu, yu
П п	*П п*	P, p	Я я	*Я я*	Ya, ya

*ye initially, after vowels, and after ъ, ь; e elsewhere.
When written as ё in Russian, transliterate as yё or ё.

RUSSIAN AND ENGLISH TRIGONOMETRIC FUNCTIONS

Russian	English	Russian	English	Russian	English
sin	sin	sh	sinh	arc sh	$\sinh^{-1}$
cos	cos	ch	cosh	arc ch	$\cosh^{-1}$
tg	tan	th	tanh	arc th	$\tanh^{-1}$
ctg	cot	cth	coth	arc cth	$\coth^{-1}$
sec	sec	sch	sech	arc sch	sech^{-1}
cosec	csc	csch	csch	arc csch	csch^{-1}

Russian	English
rot	curl
lg	log

GRAPHICS DISCLAIMER

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FOREWORD /3

This book basically is intended for engineering and technical personnel who maintain radar equipment in troop units. Its goal is to aid the reader to refine physical processes in pulse devices and to master reading of radar station pulse circuits. Understanding of physical processes in pulse devices and ability to analyze, to read, any radar station pulse circuit is required for proper equipment maintenance, effective preventive measures, and rapid detection and correction of malfunctions.

Certain typical pulse signal transformations always will occur in radar station pulse circuits. In turn, these transformations are made with the aid of a limited number of standard elementary circuits -- "building blocks," from which the basic circuits in any pulse device are synthesized. The main content of this book is devoted to study of such elementary circuits and their interaction. Basic information on the role and place of pulse circuits in radar, on pulse signal characteristics and parameters, on standard pulse transformations, and on pulse circuit types introduce this material. A series of elementary items, which may be useful to some readers as they work with this book, is found in the attachments.

A. V. Kuznetsov wrote a portion of the material at the author's request (Chapter III, §6; Chapter V, §4; Chapter VI, §6 and 7; Chapter VII; Chapter IX, §7).

This is not the usual textbook for a course on pulse technology (there are

Translator's note: demultiplication should be division.

sufficient of these, widely recognized, available to support higher and secondary military educational institution programs). First, only those devices that have found wide use in extant radar equipment are examined in the book. Second, it will not contain information on calculation and design of pulse circuits. Main attention has been placed on a description of the physical principles of their operation, characteristic features and properties, adjustments, practical use variations, and the influence of typical malfunctions. Several problems /4 mainly of theoretical interest have been omitted. Third, the book is intended in the main for independent work on the part of the reader, which reflects the main form of instruction for engineering and technical personnel in troop units and a basic element of the instructional process in educational institutions. That fact stipulated some of the book's special structural features.

Questions (problems) in the form of exercises are provided in order to vitalize the material and to increase effectiveness in material assimilation as the reader progresses. Answers to these problems require comprehension, critical analysis, and sometimes even some development ("invention") of the material in the basic text. No questions or problems that can be answered simply by reading the text or through mechanical working of formulas are provided in order not to create the illusion of material assimilation.

Responding to the questions requires the reader to formulate answers, which encourages the maximum degree of profound assimilation of the material. The multiple-choice method of questioning is not used virtually at all in this book because of the inherent drawbacks of this approach.

We recommend that answers be provided in written form. This teaches an individual to formulate answers precisely and plays the role of "physical activity" reinforcing the student's mental activity.

The answers to the questions, with the required explanations, are provided in Chapter X for self-correction. They are to be referred to only after the reader has written (or honestly tried to write) his own answer. It is assumed that the reader will conduct himself in just this manner because, since he decided to use this book, he is interested in profound assimilation of the material and understands that his ability independently to find the correct answers in this sense is the best criterion.

Working with exercises is very desireable. Therefore, some supplementary information is included in the associated explanations, generalizations are provided, and highlights underscored, with some problems examined from a different point of view. Some of the exercises are designed also to prepare the reader for subsequent material.

PROCEDURE FOR INDEPENDENT USE OF THE BOOK (Appeal to the Reader)

As you prepare to begin work, have a notebook handy. It is useful to outline the material to the extent you deem advisible. However, when encountering the next question (problem) in the text, formulate your answer and, without fail, /5 write it down in the notebook (sketch the requisite characteristics, graphs, curves, and circuits). If the question is difficult, go through the appropriate material again, then again attempt to provide an answer.

Check it against the correct response only after you have entered your answer in the notebook. The answer will be found on the page indicated at the end of each exercise. You also will find the necessary explanation there.

PROCEDURE FOR USING THE BOOK IN AN AUDITORIUM UNDER A TEACHER'S SUPERVISION (Recommendation for the Teacher)

Effective use of the book in an auditorium under the supervision of a teacher and the latter's participation are possible if the following two conditions are fulfilled: a group of workable size (20-25 students) and the availability of sufficient copies of the book. Individual paragraphs of the book (besides the introduction to each chapter) or the description of some circuits can be omitted, with the requisite changes made to the number and content of the exercises depending on specific goals and study conditions. Approximately 60-80 training hours are required for full coverage of the book's material.

Each student must have a text and notebook at the lessons. Chapter X, containing the answers to the exercise, should be covered over in the books beforehand. Introductory lectures on each topic, which are assigned to the most-experienced teachers and which can be delivered to a batch of students (class), must precede individual work with the book. The content and number of such lectures are determined

in each invidual case, depending on the training and nature of the student contingent and the specifics of the educational institution. The overall task for the introductory lectures is to prepare the students for independent work with the book from a methodological and psychological point of view. Some of the lectures must be given at the conclusion of a particular class for illumination of questions not covered in the book.

As they work independently, students voluntarily outline the material in their notebooks and can approach the teacher with any questions (for example, on places they don't understand or which are not explained in the book, in connection with associations or proposals that occur, and so on). However, reaching an exercise in the text, the student must precisely and intelligently write his formulated answer (draw the requisite characteristics, graphs, curves, circuits) and provide them to the teacher for a critique. The teacher examines the answer and, depending on the degree of its correctness and completeness, provides assistance to the /6 degree to which this is necessary for a particular student (approval, basis of the error, indication of its causes, follow-up question, brief explanation, and so on).* Experience shows that it requires an average of 1 minute per question for the teacher's critique. The student is told to continue reading the book only after approval is obtained for an answer.

The teacher maintains only one record during the sessions, a record of independent work in the group. This record comprises a list of the group with vertical columns corresponding to lesson numbers. Correct answers are denoted by a plus sign (+) and incorrect, or unsubstantiated, answers denoted by a minus sign (-) (we use red and blue grades). Since, in the final analysis, a correct answer is required for each problem, a "plus" must be the final notation in each square. A large number of "minuses" in any vertical column indicates the requirement for additional explanation of this problem. It is evident that such a system completely and clearly reflects the situation in a group at any particular moment, as well as the rate and quality of each student's work.

Students who complete the study of a given section ahead of time, with approval

*In some cases, the teacher may recommend that the student read the appropriate explanation in Chapter X. Therefore, the teacher must have two or three "unexpurgated" copies of the book.

on all responses, may be released from further mandatory attendance at lectures on this section, while those obviously falling behind must be called in for mandatory addtional consultations. It is advisible to allow exams (quizzes) to be taken ahead of time.

There is no reason for students to be reluctant to present the teacher answers that may turn out to be incorrect, but, on the contrary, they should be interested in frequent contacts with the teacher for the qualified continual monitoring of the effectiveness of their work. Therefore, the critique the teacher provides on answers must be constructive and be designed only to aid the student, to approve and vitalize their mental activities in the desired direction.

In particular, it is necessary (and the students must be absolutely convinced of this) that an evaluation given by a teacher on a comprehensive exam or quiz in no way depend on the plus-minus ratio. Where required, the use of minuses can be eliminated if the psychological barrier on the part of the students to the grading system is not overcome. Mutual efforts on the part of the students during the process only facilitate learning and should not be prohibited. Possible isolated attempts of dishonest mechanical copying of a comrade's answers without the work being done are evident to the teacher and rapidly eliminated.

The teacher's efforts must insure timely examination of all answers that /7 are turned in to him, which may require intense efforts on his part during the lessons. However, given establishment of the conditions described above, a favorable atmosphere for creative enthusiasm is established rapidly in the auditorium for studying the material, which will result in increased effectiveness.

The approach recommended above for independent work with the book also is applicable for studying the material in the auditorium. In this variant, the students, working on the material, approach the teacher with questions only at their own initiative. The teacher's activities during the lessons are eased since he, in essence, is released from ongoing monitoring and controlling assimilation of the material. Instead, he can give periodic (three to five per semester) graded check quizzes on individual sections (themes). These can be automated. This approach to monitoring makes it possible, with a delay equating to the interval between quizzes, to evaluate the results of independent work by the students and to rank them accordingly.

CHAPTER I /8

GENERAL INFORMATION ON PULSE SIGNALS AND DEVICES IN RADAR

§ 1. CONCEPT OF PULSE RADAR. PULSE SIGNAL PARAMETERS

The majority of radar stations (RLS) employed at present in troop units operate in the pulse mode, i. e. emitting electromagnetic energy into space and receiving it from an object in individual brief portions -- pulses. Here, pulses emitted (outgoing and interrogation) and received from an object (echo or return) turn out to be separated in time. Thanks to this, the pulse radar method makes it possible most simply to determine the range to an object from the delay time of a pulse received from an object relative to the emitted pulse, and to have a single antenna at the RLS used alternately for transmission and reception. In addition, the discontinuous structure of pulse signals makes it possible to use their time selection (differentiation of pulses by the time of their formation) and, for this reason, improve radar system capabilities: to divide signals in time from different objects, to code signals by time parameters, to create multichannel lines with channel time division, and so on.

What are radar pulse signals? The brief deviation of voltage or current from the set value is referred to as an electric pulse. The term "brief" must

be understood in the sense that pulse duration is less than or equal to the duration of transient processes arising in electric circuits when they operate.*

There are two types of pulses, which are distinguished by the nature of the change of voltage or current during the action of the pulse -- video pulses and radio [r-f] pulses.

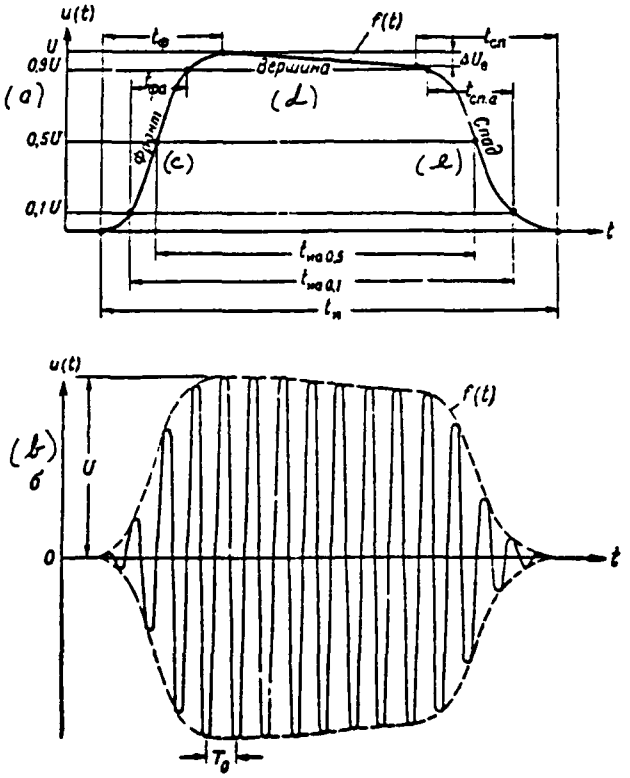

Figure I.1. Voltage Video Pulse (a) and Radio Pulse (b). (c) -- porch; (d) -- tilt; (e) -- droop.

A brief increase or decrease in constant voltage or current is called /9 a video pulse (Figure I.1a). In the first case, a positive video pulse results, while a pulse of negative polarity occurs in the other.

*We will point out that processes arising when the electrical balance in a circuit is disrupted are called transient processes.

A packet of high-frequency harmonic oscillations is called an r-f pulse (Figure I.1b). The frequency of these oscillations is called the basic frequency or carrier frequency $f_0 = \frac{1}{T_0}$, where T_0 is the period of the harmonic oscillations. It is evident that it is senseless to talk about the polarity of an r-f pulse, obtained from pulse modulation of video pulses by a microwave oscillator. Reverse transformation, obtaining video pulses from r-f pulses, is accomplished by /10 r-f pulse detection (separation from the envelope).

If there are no special reservations, in future we will examine voltage video pulses.

The parameters of a single pulse are its amplitude (maximum value) U, form f(t), pulse duration t_u, pulse rise time t_ϕ, pulse decay time t_{cn}, and tilt dissipation ΔU_n (Figure I.1a).

The envelope of a real pulse has a smooth nature due to the nature of the transient processes in electrical circuits. This complicates strict (single sign) determination of t_u, t_ϕ, t_{cn} intervals. Therefore, values t_u, t_ϕ, t_{cn} in practice are measured at specific previously-agreed upon levels relative to pulse amplitude and are referred to as active times.

As depicted in Figure I.1a, active time t_{un} for a pulse with amplitude U usually is computed at level 0.5U, active pulse rise time $t_{\phi n}$ usually is determined as the time interval between the moments the envelope acquires values 0.1U and 0.9U at the pulse's leading edge. Analogously, active pulse decay time t_{cn} is determined at pulse decay.

Mathematically, a video pulse may be written in the form

$$u(t)_n = Uf(t). \qquad (I.1)$$

where f(t) — time function describing the form of the pulse ($f(t) \leqslant 1$ since, when f(t) = 1, f(t) = U — the pulse reaches the amplitude value).

The form of real pulses usually is approximated by several simple functions

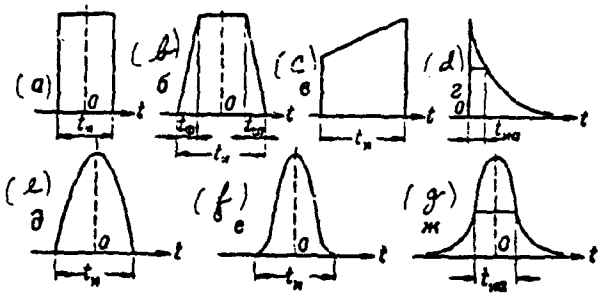

Figure I.2. Square (a), Trapezoidal (b, c), Exponential (d), Cosine (e), Square-Cosine (f), and Gaussian (g) Pulses.

of f(t). Pulses of the most-characteristic forms examined in radar are depicted in Figure I.2.

From the energy point of view, a single pulse is characterized by its /11 energy $W_и$ and pulse power $P_и$, understood to mean power average for the pulse's time of activity $P_и = \frac{W_и}{\tau_и}$.

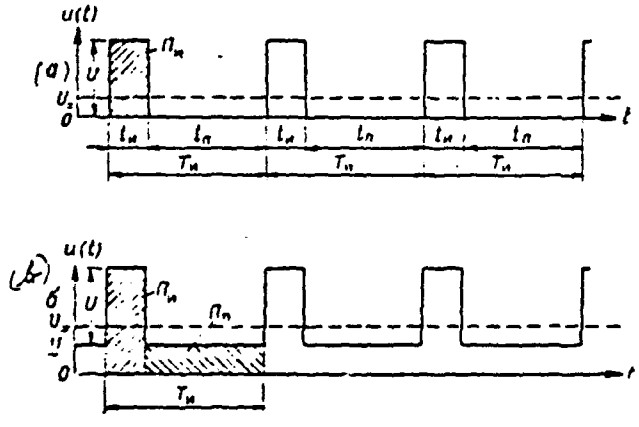

Figure I.3. Periodic Square Pulse Trains (Q = 4).

Periodic pulse trains (Figure I.3), trains of periodically-repeating r-f

and video pulses of a given form and amplitude, are used in radar. Additionally, the parameters of such signals are:

-- resting time between pulses $t_п$;

— pulse repetition period $T_и = t_и + t_п$;

— pulse repetition rate (number of pulse per second $F_и = \frac{1}{T_и}$;

— pulse duty ratio $Q = \frac{T_и}{t_и}$;

— pulse ratio $\lambda = \frac{1}{Q} = \frac{t_и}{T_и}$;

As a rule, pulse duration is much less than resting time $t_и \ll t_п$. Consequently, the greater $t_и \ll T_и$ and $Q \gg 1$. The latter inequality expresses the basic time ratio in pulse radar.

Mathematically, a periodic video pulse train may be written in the form

$$u(t)_и = Uf(t - nT_и), \qquad (I.2)$$

where n = 0, 1, 2, 3,. . . /12

Like any periodic function*, a periodic voltage video pulse train may be presented in the form of the sum of two components, direct and alternating $u(t)_и = U_- + u_-$. Direct component U_- is the average value of the signal for pulse repetition period $T_и$. Alternating component u_- determines only the form of the pulses, while the average value of the alternating component for the period equals zero.

The direct component may be found graphically as the height of a square with base $T_и$, whose area equals area $П$, limited by the voltage curve for period $T_и$.

*Naturally, a real pulse signal is not a strictly periodic function. First, all its parameters to a certain degree change over time and, second, it has a beginning and an end, corresponding to the equipment cutting in and out, i. e., its periodicity is not infinite (for any n). Therefore, the more precisely the signal is described by expression (I.2), the more stable its parameters and the greater the number of pulse repetition periods it observes.

Area $П$ conveniently is determined as the algebraic sum of the areas enclosed by the voltage curve for the pulse activity time and resting time: $П = П_и + П_п$, therefore

$$U_= = \frac{П}{T_и} = \frac{П_и}{T_и} + \frac{П_п}{T_и}.$$

For the pulses depicted in Figure I.3a, voltage is missing during resting times ($П_п = 0$) , and, considering the square form of the pulses, $П_и = Ut_и$. Thus,

$$U_= = \frac{П_и}{T_и} = U\frac{t_и}{T_и} = \frac{U}{Q}. \qquad (I.3)$$

For those depicted in Figure I.3b, which have the same form and amplitude but are designated with a nonzero initial level $\underline{U}$ (value of voltages during resting times), $П_и = (U + \underline{U})t_и$ and $П_п = \underline{U}t_п$

$$U_= = \frac{U}{Q} + \underline{U} \qquad (I.4)$$

— the direct component changes by the value of the initial level (considering its sign).

Mathematically, the area enclosed by the curve of the function are expressed by the specific integrals of this function accepted in the appropriate limits. Therefore, for any pulse form, one may write

$$U_= = \frac{1}{T_и}\int_0^{T_и} u(t)_и\,dt = \frac{1}{T_и}\left[\int_0^{t_и} u(t)_и\,dt + \int_{t_и}^{T_и} u(t)_и\,dt\right]. \qquad (I.5)$$

It follows from the ratios presented that the direct component will depend /13 on pulse amplitude, form, polarity, repetition period, and initial level.

Comprehension of the physical processes in pulse devices in many cases is facilitated when representing pulse signals by their frequency spectra -- the aggregate of harmonic components of different frequencies (see Attachment 1).

Spectral representation of pulse signals will lie at the basis of the frequency method of line circuit analysis (see Attachment 7).

From the power point of view, a periodic pulse signal is characterized, along with pulse power $P_и$, also by average power $P_{ср}$ -- power averaged during the pulse repetition period. Since pulse energy equals $W_и = P_и t_и$, and, from determination $P_{ср} = \frac{W_и}{T_и}$, then

$$P_и = P_{ср}\frac{T_и}{t_и} = P_{ср}Q, \qquad (I.6)$$

i. e., pulse power will exceed average power by factor Q. Ratio (I.6) is the basic energy ratio for pulse radar.

§ 2. PULSE RADAR STATION COMPOSITION AND OPERATING PRINCIPLE

The following are pulse radar station basic elements (Figure I.4): synchronizer, transmitter, receiver, transceiving antenna (A), antenna control system, antenna switch (AP), high-frequency energy transmission lines (LP), feeders or wave guides*, displays, automatic range and angular coordinate target tracking systems, and energy source.

The synchronizer sets the station's operating rhythm and insures that all its units operate in strict time agreement. It generates short video sync pulses with repetition period $T_и$ (Figure I.5a). These pulses are supplied to the transmitter, displays, and automatic target range tracking system**.

The transmitter creates powerful outgoing r-f pulses and will comprise a driver (sometimes omitted), modulator, and microwave oscillator. Sync pulses reach this driver, where they are amplified to the level required to control the modulator's operation. Powerful modulating video pulses are generated in the /15

*Antenna, antenna switch, and high-frequency energy transmission lines comprise the station's antenna-feeder or antenna-wave guide system.

**The synchronizer also generates the supplemental video pulse trains required for the operation of various RLS elements and devices connected thereto.

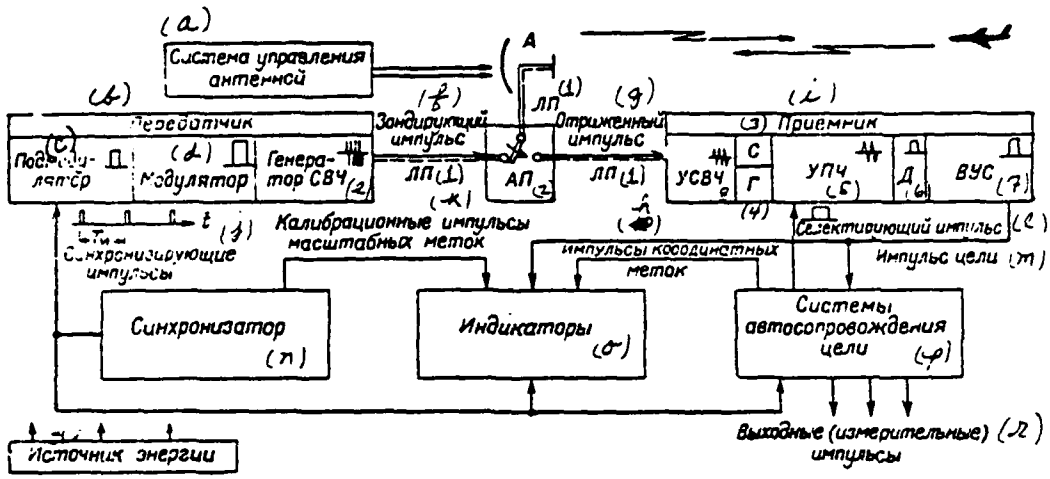

Figure I.4. Pulse Radar Station Simplified Structural Diagram. (a) -- Antenna control system; (b) — Transmitter; (c) -- Driver; (d) -- Modulator; (e) Microwave oscillator; (f) — Outgoing pulse; (g) — Echo pulse; (h) -- Collimating mark pulses; (i) — Receiver; (j) — Sync pulses; (k) -- Scale mark calibration pulses; (l) — Gate pulse; (m) — Target pulse; (n) -- Synchronizer; (o) — Displays; (p) -- Automatic target tracking systems; (q) -- Energy source; (r) — Output (measuring) pulses; (1) -- LP; (2) -- AP; (3) — S [Mixer]; (4) -- G [Hetrodyne]; (5) -- UPCh [Intermediate Frequency Amplifier]; (6) — D [Detector]; (7) — VUS [Video Amplifier]; (8) — USVCh [Microwave Amplifier].

the modulator (Figure I.5b) and modulate the microwave oscillator, which generates outgoing pulses (Figure I.5c).

Outgoing pulse repetition period $T_и$ is provided by the synchronizer, their power $P_и$, form, and duration $t_и$ by the parameters of both the modulator and the microwave oscillator, and carrier frequency f_0 by the microwave oscillator.

Outgoing r-f pulses are fed from transmitter output along transmission lines via the antenna [transmit-receive -- T-R] switch to the antenna and radiated by it into space. Echo r-f pulses (Figure I.5d) return to the RLS during resting times between outgoing pulses*, are received by this antenna, and are supplied

*In accordance with Figure I.5d, two echo pulses arise for each outgoing pulse repetition period. This corresponds to a case where two targets A and B, with different ranges r_A and r_B, are within the RLS coverage zone.

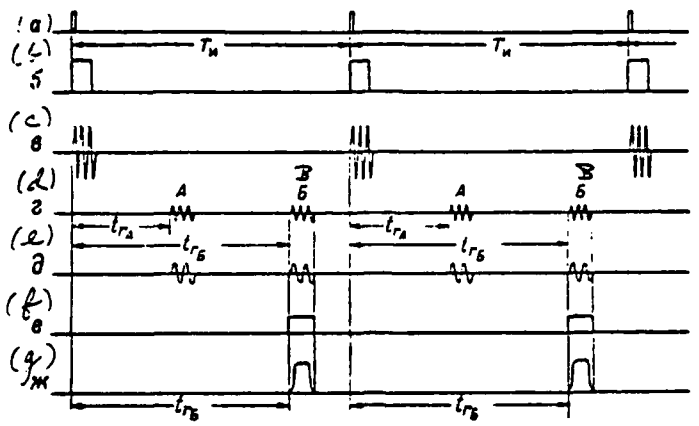

Figure I.5. For Target Signal Formation and Conversion: (a) — Sync pulses; (b) — Modulating video pulses; (c) — Outgoing r-f pulses; (d) — Echo r-f pulses; (e) — Intermediate frequency r-f pulses; (f) — Gate pulses; (g) — Target pulses at receiver output.

to the receiver input via the antenna switch along the transmission lines.

The antenna is for radiation and reception of high-frequency electromagnetic energy. RLS use directional antennas, which radiate and receive electromagnetic energy in narrow spatial beams. This creates the capability of determining target bearing, its angular coordinates.

The antenna control system remotely controls antenna rotation in azimuth /16 and angle of site and is a conventional system of electromechanical servos.

The T-R switch, affected by outgoing pulses, automatically connects the antenna to the transmitter output and disconnects it from the receiver. During the resting time between outgoing pulses, it connects the antenna to the receiver input, disconnecting it from the transmitter.

The receiver amplifies r-f pulses received by the antenna and converts them to video pulses. A superhetrodyne receiver usually is used and it will comprise an input device (VU), microwave oscillator (USVCh), hetrodyne (G), mixer (S), intermediate frequency [IF] amplifier (UPCh), detector (D), and video amplifier (VUS).

An input device (preselector) provides the receiver's carrier frequency selectivity. The USVCh will serve for preliminary amplification of r-f pulses on the carrier frequency (mainly for the purpose of reducing the receiver's noise factor). R-f pulses are supplied from the USVCh output to the mixer. Also supplied to the mixer is a constant harmonic voltage generated by the hetrodyne, a low-power automatic harmonic oscillator. The hetrodyne's voltage frequency is $f_r < f_0$. IF (varied) r-f pulses $f_{пр} = f_0 - f_c$ (Figure I.5e) are separated at mixer output. Basic r-f pulse amplification will occur on an intermediate frequency in the UPCh, which also determines the receiver's overall frequency-selectivity properties.

Temporary selection of target range signals may occur in the UPCh.* Video gate pulses (Figure I.5g), which open the stage only long enough for the passage of pulses from the target selected for tracking (Target B in Figure I.5), are supplied for this purpose to one normally-closed UPCh stage. Gate pulses are generated in the automatic range tracking system, where the requisite time for their delay relative to outgoing pulses is provided automatically.

Amplified and gated IF r-f pulses are supplied from the UPCh output to the detector input, where separation of the r-f pulse envelope will occur. Target video pulses appear at the detector output and then are amplified additionally in the video amplifier to the level necessary for RLS terminal devices to operate (Figure I.5g).

The displays are designed for observation of the aerial situation, target search and selection, visual determination of its coordinates, and preparation for automatic tracking. Displays in operating principle are pulse oscillographs with linear or two-dimensional sweeps. Time-base linear sweeps synchronized /17 by a sync pulse with the repetition frequency of the outgoing pulse are created for range measurement.

These sweeps are obtained with the aid of sawtooth voltages or currents acting upon the tube's deflection yoke. Intensifier pulses, which enable the tube only during the forward motion of the sweep (the operating linear portion of the sweep's sawtooth voltage or current) or, on the other hand, quench pulses for the retrace

*Also based on angular coordinates in some cases.

of the sweep, which disable the tube during the retrace, are supplied to the cathode ray tube's [CRT] control electrode (or cathode) to eliminate ambiguities in target blip positions on the screen. Range sweep displacement, in accordance with the law of antenna rotation or the scanning (rocking) of its radiation pattern, will occur for measurement of angular coordinates. Target video pulses are fed from the receiver output either to the CRT deflection yoke or to its control electrode (cathode). In the former case, target blips are received in the form of electron beam excursions (amplitude signal display) and, in the latter, in the form of bright marks (brightness signal display). The amplitude display is used when linear sweeps are used, and the brightness display when two-dimensional sweeps are used. Coordinates are determined either from graphic scales or (more accurately) from electronic scales. The latter are created with the aid of scale mark calibration pulses. These pulses are generated in the synchronizer with repetition frequency $F_м$ corresponding to the value of the scale marks.

Automatic tracking systems are intended for automatic measurement of present position data. These systems operate as closed automatic control systems -- servos. The measurement method selected for a given coordinate determines system design.

Measurement of range (slant range) to the target r always will be accomplished from lag time t_r of the echo pulse relative to the outgoing pulse (Figure I.5). This time for an RLS with a passive response, i. e., operating from pulses reflected from the target, is linked with range by the simple ratio

$$r = \frac{C}{2} t_r \qquad (I.7)$$

where $C = 3 \times 10^8$ meters per second, the velocity of radio wave propagation.

An electronic servo automatically measuring lag time t_r is used for automatic range tracking. The idea of this system's operation is explained in Figure I.6. Sync pulses (I.6a) and target video pulses (I.6b) are fed to the system input. A pair of strobe (tracking) pulses (Figure I.6c) one after the other, as well as an output (measuring) pulse coinciding with the axis of symmetry of the /18 strobe pulse pair (Figure I.6d), are generated in the system for each repetition period.

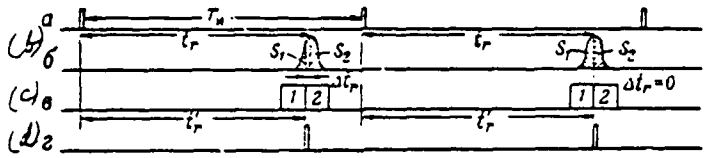

Figure I.6. For the Automatic Range Tracking Principle: (a) -- Sync pulses; (b) -- Target video pulses; (c) -- Strobe pulses; (d) -- Output (measuring) pulses.

The target pulse's axis of symmetry in each repetition period lags relative to the sync pulse by a time proportional, in accordance with (I.7), to the true range to the target,* while the strobe pulse pair's axis of symmetery lags by time t_r', proportional to the range value measured and issued by the system. The strobe pulse delay by time t_r' is supplied by the system's constant delay circuit, which controls the moment the strobe pulse generator is triggered.

The automatic tracking principle will comprise automatic tracking of target pulses by the strobe pulse pairs (and by the measuring pulses as well). During this tracking process, difference $\Delta t_r = t_r - t_r'$, which is the automatic tracking time error, strives towards zero, i. e., $t_r' \to t_r$ -- the range value supplied by the system will strive towards true range. Target pulse tracking by strobe pulses will occur due to the action of the voltage of error signal $u_{co} \sim \Delta t_r$, generated by a time discriminator, the system's sensing element. This discriminator will comprise a two-channel coincidence circuit and a difference circuit. The former generates two pulse voltages, whose amplitudes are proportional to areas of coincidence S_1 and S_2 of each strobe pulse with the target pulse (Figure I.6b). Comparison of these voltages will occur in the latter and a voltage proportional to difference $S_1 - S_2$, i. e., to tracking time error $\Delta t_r \sim S_1 - S_2$, is generated, while the polarity of this voltage corresponds to the error sign. The difference circuit's output voltage also is error signal voltage since it will contain information on the tracking magnitude and error sign. This voltage also is /19 controlled by the variable delay circuit, which displaces the strobe pulses (measures

*With a constant error equal to half the target pulse duration (Figure I.5).

time t_r') in the direction of error Δt_r reduction, i. e., immediately following the target pulses*.

Initiation of target tracking (target lock-on) requires a certain rough strobe pulse-target pulse coincidence, if only that voltage $u_{co.}$ appears at the discriminator output. Under influence of this voltage, the strobe pulses will begin to displace in the requisite direction. This coincidence will occur either automatically due to periodic displacement of the strobe pulses within the limits of period T_* of the so-called search circuit or visually with the aid of a display. In the latter case, an electronic range mark reflecting the position of the strobe pulses is created, along with the target blips, on the display. The pulses for receipt of this mark are generated simultaneously with the strobe pulses in the automatic tracking system. Controlling the constant delay circuit manually, the electronic range mark (and, consequently, the strobe pulses) must coincide with the target pulse in order for the automatic tracking system to lock on the target.

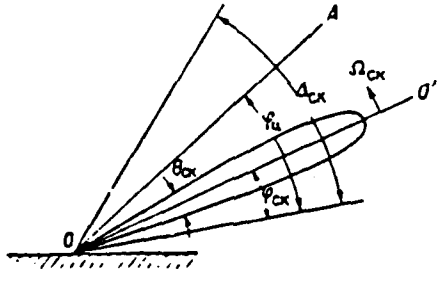

Figure I.7. For Periodic Sector Scan With a Fan Beam.

Gate pulses supplied to the receiver also are generated along with the strobe pulses (Figure I.5f).

Automatic angular coordinate tracking can be accomplished through automatic guidance of the antenna's geometric axis to the target. A servo (contained in the antenna control system), which reacts to a deviatior of the antenna's axis

*The difference circuit's output voltage is detected beforehand and is integrated to create the requisite tracking system dynamic properties.

from the target bearing and automatically corrects this deviation by turning the antenna, is used for this purpose.

Some RLS employ a periodic fan beam sector scan. Here, angular coordinate determination is accomplished in the tipping plane by measurement of time intervals, i. e., the identical methods used to determine range. This scanning system for the vertical plane is explained in Figure I.7, where $\Delta_{ск}$ -- scan sector, $\theta_{ск}$ -- fan beam angle in the scan plane (the beam will flatten in this plane, but is broad in the mutually-perpendicular plane), OO' -- beam axis (bearing of maximum radiation and reception), OA -- bearing to the target. Scanning will occur /20 in accordance with the sawtooth law: a beam displaces with constant rate $\Omega_{ск}$ from the lower (initial) edge of sector $\Delta_{ск}$ к to the upper edge (forward motion of the beam), then returns rapidly (beam retrace). Target signals will arise during the scan process only during target paint time $t_{обл}$, i. e., during the time the target is located within the boundaries of beam angle $\theta_{ск}$. Beam angle $\theta_{ск}$ and scan rate $\Omega_{ск}$ are selected so that a series (packet) of echo pulses $t_{обл} \gg T_и$ will arrive during that time from the target.

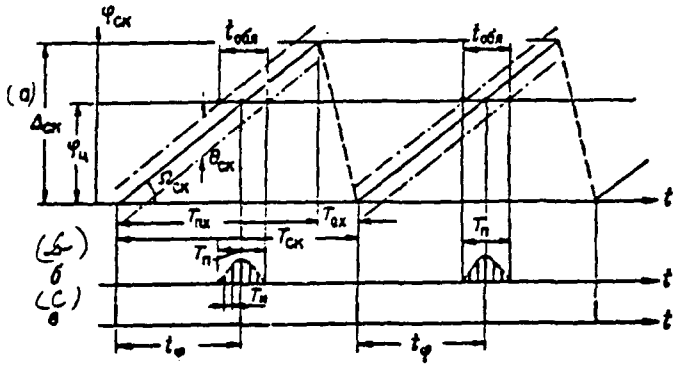

Figure I.8. For Angular Coordinate Measurement During Periodic Sector Scan. (a) — Beam scan law; (b) — Target pulses at receiver output; (c) — Angular reference pulses.

The mechanism for forming the packets and obtaining information about target angular coordinate $\varphi_ц$ is explained in Figure I.8. The sawtooth law of beam scanning over time is depicted in Figure I.8a. The solid sloping lines depict the law

of angle change $\varphi_{сн}$ between the lower edge of sector $\Delta_{сн}$ and the beam axis during the time of its forward motion $T_{пг}$, while the parallel dotted lines with periods show displacement of the upper and lower edges of the beam for this time. The dotted line indicates the beam's retrace since, during retrace time $T_{ох}$, the RLS transmitter is blanked (shut off) to avoid ambiguity in target coordinate determination. Packets of target video pulses arising during time $t_{об.п}$ at the receiver output and, consequently, having duration $T_п = t_{об.п}$, are depicted in Figure I.8b. The form of the envelope of each packet is determined by the radiation diagram in the scanning plane, while the center of the packet (its amplitude) arises exactly at the moment the beam's axis coincides with the bearing to the target, i. e., when $\varphi_{сн} = \varphi_ц$. Therefore, given a constant scan rate, /21 the coordinate of the target, computed from the lower edge of the scan sector, turns out each time to be proportional to time interval $t_ц$ between the moment of initiation of the beam's forward motion and the center of the packet:

$$\varphi_ц = \Omega_{сн} t_ц. \qquad (I.8)$$

Angular reference pulses (Figure I.8c), which coincide with the beginnings of the beam's forward motion, will serve to fix the moments of the initiation of the counting of intervals $t_ц$.*

An electronic servo analogous to the automatic range tracking system and the system automatically measuring intervals $t_ц$ may be used for automatic angular coordinate tracking in this case. The strobe pulse pairs in such a system are generated with frequency scanning and, under the influence of error signal voltage, track the pulse packet centers.** Angular gate pulses, which are supplied to the receiver and provide an additional target signal time selection based on angular coordinate by means of opening the UPCh only during the time of passage of the pulse packet from the selected target, may be generated simultaneously with the strobe pulse pairs.

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*Reference pulses, as well as those blanking the transmitter, are generated with frequency scanning by an additional angular synchronizer, which controls the scan mechanism, at the station.

**Angular strobe pulse duration must be compatible with packet duration $T_п$.

EXERCISE I.1

a) Prove formula (I.7). Derive the formula for range determination when using an RLS with active response.

b) To avoid range ambiguity, an echo pulse must be received before the next outgoing pulse is radiated (see Figure I.5). From this condition, what is the maximum RLS range if period $T_п$ = 600 μsec?

c) There are three targets at r_1 = 73, r_2 = 85, and r_3 = 100 kilometers in the sector of coverage of an RLS with passive response. What must be the delay time of the gate pulses (relative to the outgoing pulses) in order that only the pulses from the second target pass to the receiver output? How is gate pulse duration determined ?

d) The least distance between two targets with identical angular coordinates r_{min} at which individual measurement to each target is still possible, is referred to as RLS range resolution. How is value r_{min} determined when measuring range from the display and from the automatic tracking system (see Figure I.6)?

e) What must the repetition frequency of calibrating pulses equal to create 5-kilometer electronic scale range marks on the display?

f) Periodic sector coverage will take place (Figures I.7 and I.8). Determine the number of pulses in a packet of scanning sector $\alpha_с$ = 30°, scanning frequency $F_с$ = 20 Hz, beam retrace time $T_{об}$ = 10 ms, beam angle $\theta_л$ = 2°, and pulse repetition frequency $F_п$ = 2.5 kHz. What will target angular coordinate $\varphi_ц$ equal if interval $t_з$ = 32 usec? (Page 443)

§ 3. STANDARD SIGNAL CONVERTERS IN RADAR STATION PULSE DEVICES. REVIEW OF ELEMENTARY PULSE CIRCUITS

It follows from examination of a pulse radar station's structural diagram that both video and r-f pulses operate in its circuits. The following will comprise the r-f pulse activity sphere, which is referred to as the radar station's RF section: microwave oscillator, antenna-wave guide system, and the receiver HF stages up to the detector, inclusive. The following will comprise the video pulse

activity sphere, which is referred to as the radar station's a.f. section: transmitter synchronizer, driver, and modulator, receiver video amplifier, displays, and automatic tracking systems. These RLS units are pulse devices in the sense that they almost entirely will comprise circuits for receipt, formation, and change of video pulse parameters and their trains.*

The following are standard signal conversions in pulse devices: pulse generation, pulse shortening (differentiation) and stretching (integration), pulse expansion with retention of their form, pulse amplification (increasing the amplitude), pulse inversion (changing the polarity), holding or changing the initial level of pulses (level of voltage during resting times), pulse clipping ("shearing" the peak), pulse time delay, pulse frequency repetition division, formation of sawtooth (linearly-changing) voltages or currents.

The concept of these conversions is explained in Figure I.9, in which example diagrams depict several basic voltages in an RLS synchronizer and range display.

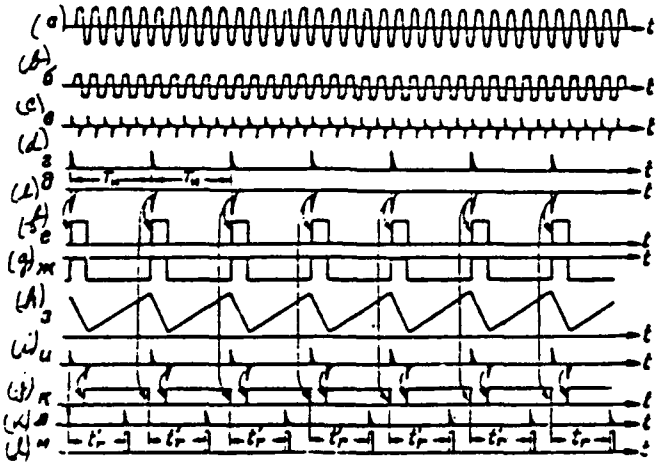

Figure I.9. Several Standard Signal Conversions in Pulse Devices.

*Several other RLS devices such as the receiver automatic amplification regulation system, a.f. noise-suppression system, and so on also are pulse devices.

Diagram a depicts a harmonic voltage generated in the synchronizer by a master sine wave self-excited oscillator. Diagram b depicts periodic voltage of almost trapezoidal form obtained by upper and lower clipping of voltage a. Diagram c depicts short bipolar pulses of exponential form obtained by differentiation of voltage b; the repetition frequency of resultant pulses of one (positive, for example) polarity equals the frequency of the initial harmonic voltage. Diagram d depicts pulses obtained after repetition frequency division of the positive pulses in diagram c into a whole number once; the repetition period of these pulses supplies station outgoing pulse repetition period $T_п$. Diagram e depicts synchronizer output pulses obtained through amplification and inversion of the d pulses. Diagram f depicts square pulses formed in a display by expansion of the e pulses; the duration of these pulses supplies the duration of display sweep retrace. Diagram g depicts square pulses obtained through displacement of /23 the pulse f initial level (a change in the direct component). Diagram h depicts sweep sawtooth voltage obtained with the aid of the g pulses. Diagram i depicts pulses obtained as a result of pulse f differentiation. Diagram j depicts sweep forward motion intensifier pulses; the duration of these pulses corresponds to the intervals between negative i and e pulses. Diagram k depicts pulses delayed by time t_r' relative to the e pulses. These pulses determine the position of the electronic range mark. Delay time t_r' corresponds to the range to the target and is supplied by the operator with the aid of control voltage $u_{упр} \sim t_r'$ (we assume that there is no automatic range tracking system). Diagram l depicts the range mark pulses formed from the k pulses.

Standard signal conversions are made by elementary pulse circuits of the following basic types.

1) Linear R-C, R-L, and R-L-C corrective networks, including:

— pulse modulator capacitance and inductive corrective networks;

— an R-C and an R-L integrator for pulse stretching, voltage pulsation filtration, and a number of other purposes; /24

-- a differentiating R-C network and R-L network for pulse shortening;

— transient R-C networks and pulse transformers for undistorted transmission of the pulse voltage alternating component and isolation (separation) of stages or networks based on the direct component;

— shock-excitation tuned circuits mainly used for shaping a series of pulses with a stable repetition frequency;

-- artificial lines used to bring the pulse delay over time to a fixed time, as well as for shaping of pulses of a strictly-determined duration.

2) Video pulse amplifiers. Pulse amplification often is accompanied by a change in tneir polarity. In this event, amplifiers are referred to as amplifier-inverters. If pulse polarity is retained during amplification, the amplifiers are referred to as repeaters.

3) Level holds (dc restorers), which insure the change and clamping of the pulse initial level.

4) Limiters, used to restrict the magnitude of pulse voltage, either on one side (unilateral limiters) or simultaneously from both sides (bilateral limiters).

5) Square-wave generators. Pulse generators can operate in both a free-running and monostable mode. In the former, the generator independently generates a periodic train of video pulses, all of whose parameters determined by the generator's own circuitry. In the latter case, the generator is controlled (enabled) by short external pulses and generates pulses of long duration, determined either by the parameters of the generator's own circuitry or by the intervals between two external pulses.

6) Pulse repetition frequency dividers, which are pulse generators generating pulses less frequently by a whole number than the external pulses with the initial repetition frequency supplied to them.

7) Sawtooth voltage or current generators, which, like pulse generators, can operate either in the free-running mode or be controlled by external pulses. The complexity of these generators' circuitry depends on the sawtooth voltage (current) linearity requirements.

8) Pulse variable time delay circuitry. These circuits are enabled by external pulses and are sawtooth voltage generators with forward motion duration (linear sector) regulated depending on control voltage magnitude, at the end of which /25 output (delay) pulses are generated.

In addition, a series of circuits used for simple functional pulse conversion are used widely in pulse devices. They include:

-- coincidence circuits measuring the time of coincidence (mutual overlap) of two pulses;

-- difference circuits comparing the amplitude of two pulses;

— level comparison circuits fixing the moments of equality of two voltages;

— pulse counters.

EXERCISE I.2

From the aforementioned elementary pulse circuits, compile a functional diagram of a synchronizer and range display corresponding to the curves depicted in Figure I.9. (Page 444)

CHAPTER II

/26

R-C, R-L, AND R-L-C CORRECTIVE NETWORKS

§ 1. TRANSIENT PROCESSES IN R-C AND R-L NETWORKS

1. Charge and Discharge of a Capacitor Across a Resistance

We will examine the circuit shown in Figure II.1. We will assume that, at moment in time t' = 0, initial voltage at the capacitor is absent ($u_c(0) = 0$) and switch K will be thrown to position 1. From this moment, charging of the capacitor will begin from constant voltage source E. Charge current i, will pass across circuit +E, switch K, capacitor C, resistance* R, -E. In accordance with Kirchoff's seond law, for this circuit the following condition must be met

$$E = u_R + u_C. \qquad \text{(II.1)}$$

Since $u_R = iR$, $i = C\frac{du_C}{dt}$, this condition is written in the form of differential equation

$$E = RC\frac{du_C}{dt} + u_C \qquad \text{(II.1a)}$$

*The term "resistance" is used throughout this book. It would be more precise to use the term "resistor" in those instances where the discussion involves an element of an electrical circuit, rather than a property.

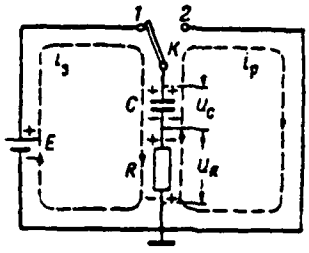

Figure II.1. Capacitor Charge and Discharge Circuit Across a Resistance.

whose solution is expression

$$u_C = E\left(1 - e^{-\frac{t}{\tau}}\right), \qquad \text{(II.2)}$$

where $\tau = RC$ -- circuit time constant (see ratios XI.9 and XI.12).

Differentiating (II.2), we will get the expression for the discharge current

$$i_3 = C\frac{du_C}{dt} = \frac{E}{R}e^{-\frac{t}{\tau}} = I_3 e^{-\frac{t}{\tau}}, \qquad \text{(II.3)}$$

consequently, voltage to resistances R equals /27

$$u_R = i_3 R = Ee^{-\frac{t}{\tau}}. \qquad \text{(II.4)}$$

The curves for functions (II.2), (II.3), and (II.4) are constructed in Figure II 2a and are exponential curves (see Attachment 3, Figure 6).

We will explain the results obtained.

At moment t' = 0, voltage u_C remains equal to zero, since voltage jumps in a capacitor physically are impossible (see Attachment 2). But, when $u_C = 0$ in accordance with (II.1), source voltage turns out to be applied fully to resistance R. Therefore, at the initial moment, voltage u_R, and, consequently, current i_3 as well, are maximum and correspondingly equal $u_R(0) = E$, $i_3(0) = I_3 = \frac{E}{R}$.

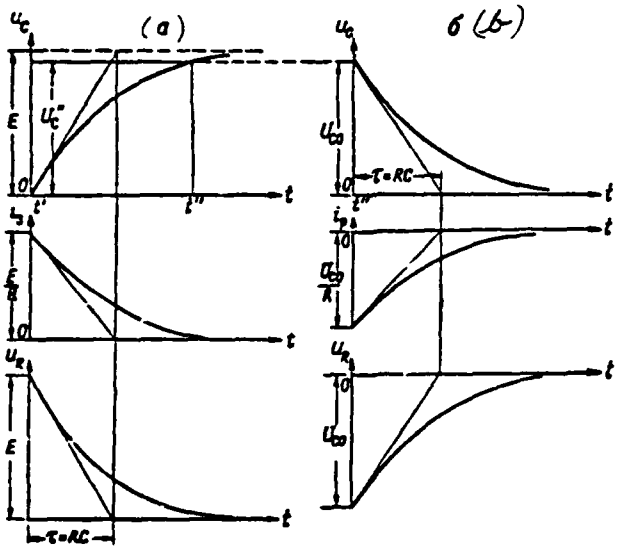

Figure II.2. Voltage and Current Curves in an R-C Network. (a) -- As the capacitor is charging; (b) — As the capacitor is discharging.

Further, as current i_1 flows due to accumulation of charges on the capacitor's plate, voltage u_c gradually increases. The rate of increase of this voltage is proportional to the capacitor charge voltage magnitude at a given moment in time:

$$\frac{du_c}{dt} = \frac{i_c}{C} = \frac{i_1}{C}. \qquad \text{(II.5)}$$

But, $i_1 = \frac{u_R}{R}$ or, considering (II.1) /28

$$i_1 = \frac{E - u_c}{R}. \qquad \text{(II.6)}$$

This ratio reflects the fact that, in the capacitor charge circuit, voltage u_C turns out to be connected in opposition to source voltage E, i. e., it counteracts the latter. Therefore, to increase voltage u_C, current i_1, and, consequently, voltage u_R as well, diminish. But, dimunition of current magnitude will lead, in accordance with (II.5) to a decrease in the rate of voltage u_C increase. This, in accordance with (II.6), in turn will retard the decrease in current i_1 and

voltage u_R . Thus, the increase in voltage u_C and decrease in current i_1 and voltage u_R will occur at a continually-decreasing rate.

Since voltage in the capacitor due to its charge increases ever more slowly, it reaches set value $u_C = E$ only when $t = \infty$ (it is evident that the capacitor is unable to charge itself to a greater voltage). Here, $E - u_C = 0$, $i_1(\infty) = 0$, $u_R(\infty) = 0$.

Now, we will assume that, up to certain moment in time t", capacitor C succeeded in charging itself to voltage $U''_C = U_{C_0} (U_{C_0} < E$ and, at that moment, switch K (Figure II.1) will change to position 2. For the sake of simplicity, we will take moment t" as the initial moment (t" = 0). At that moment, external voltage source E disconnects and capacitor C plates are connected together across resistance R, resulting in the capacitor starting to discharge across the resistance. Discharge current i_0 passes through the circuit: capacitor C "plus" plate, switch K, resistance R, capacitor "minus" plate. In accordance with Kirchhoff's second law, the following condition must be met for this circuit

$$u_C + u_R = 0, \qquad \text{(II.7)}$$

where $u_R = i_p R$; $i_p = i_C = C \frac{du_C}{dt}$.

Therefore, the circuit's differential equation will be written $u - RC \frac{du_C}{dt} = 0$, and its solution will be

$$u_C = U_{C_0} e^{-\frac{t}{\tau}}, \qquad \text{(II.8)}$$

where $\tau = RC$ — circuit time constant.*

Differentiating (II.8), we will get for discharge current

$$i_p = C \frac{du_C}{dt} = -\frac{U_{C_0}}{R} e^{-\frac{t}{\tau}} = -I_p e^{-\frac{t}{\tau}}. \qquad \text{(II.9)}$$

*See ratios (XI.9, XI.11).

Consequently, voltage at resistance R equals /29

$$u_R = i_p R = -U_{C0} e^{-\frac{t}{\tau}} \qquad \text{(II.10)}$$

The minus sign in expressions (II.9) and (II.10) indicates that current direction in the circuit and, therefore, voltage u_R polarity during capacitor discharge, are opposed to those created during its charge. The curves of exponential functions (II.8), (II.9), and (II.10) are depicted in Figure II.2b and can be explained in the following manner.

At the initial moment in time $(t''=0) u_C = U_{C0}$ while discharge current and voltage u_R are maximum: $I_p = -\frac{U_{C0}}{R}$; $U_R = -U_{C0}$. Due to capacitor discharge, voltage u_C gradually decreases at a rate proportional to the current magnitude: $i_p : \frac{du_C}{dt} = \frac{i_p}{C}$. But, based on (II.7)

$$i_p = -\frac{u_C}{R}.$$

Therefore, a voltage u_C decrease elicits a decrease in current i_p and voltage u_R decrease. A current i_p magnitude decrease will lead to a decrease in the voltage u_C decrease rate, which in turn retards the decrease in the current i_p and voltage u_R magnitude. Here, at any moment in time, based on (II.7), equality $u_R = -u_C$ is fulfilled. The discharge process concludes where $t = \infty$ when $u_C = 0$ (capacitor completely discharged), therefore $i_p(\infty) = 0$; $u_R(\infty) = 0$.

The duration of the transient processes in an R-C network, in accordance with (XI.15), can be accepted in practice as equalling

$$t_{\text{откр}} \approx 3\tau, \qquad \text{(II.11)}$$

where $\tau = RC$.

EXERCISE II.1

Draw the curves of voltage u_C, current i_p , and voltage u_R from Figure II.2a. Construct on these graphs curves u_C , i_p , and u_R if source voltage

$\tilde{C}$ decreases by a factor of 2; capacitance C increases by factor of 2; resistance R decreases by a factor of 2. (Page 444)

2. Charge and Discharge of an Inductance Across a Resistance

We will examine the circuit shown in Figure II.3. We assume that, at moment t' = 0, current in the inductance is absent $i_L(0)=0$ and switch K will be placed in position 1. At that moment, discharge of inductance L begins from constant voltage source E by current $i_1=i_L$ across circuit: +E, switch K, inductance L, resistance R, -E.

In accordance with Kirchhoff's second law, for this circuit

$$E = u_R + u_L. \tag{II.12}$$

Substituting $u_R=iR$, $u_L=L\frac{di_L}{dt}$, in this equality, we get the circuit's differential equation in the form /30

$$E = i_1R + L\frac{di_1}{dt}, \tag{II.12a}$$

and its solution

$$i_1 = \frac{E}{R}\left(1-e^{-\frac{t}{\tau}}\right) = I_1\left(1-e^{-\frac{t}{\tau}}\right), \tag{II.13}$$

where $\tau=\frac{L}{R}$ -- circuit's time constant;

$I_1=\frac{E}{R}$ -- discharge current amplitude.

Voltage u_R changes proportionally to the current:

$$u_R = i_1R = E\left(1-e^{-\frac{t}{\tau}}\right), \tag{II.14}$$

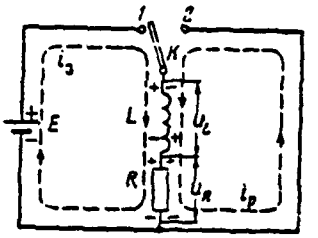

Figure II.3. Inductance Charge and Discharge Circuit Across a Resistance.

while voltage in the inductance equals

$$u_L = L\frac{di_1}{dt} = Ee^{-\frac{t}{\tau}}. \qquad \text{(II.15)}$$

The curves of exponential functions (II.13), (II.14), and (II.15) are constructed in Figure II.4a and can be explained in the following manner.

Using equality (II.12) and the expressions for voltages $u_L = L\frac{di_1}{dt}$ and $u_R = i_1 R$, we will get

$$\frac{di_1}{dt} = \frac{u_L}{L} = \frac{E - i_1 R}{L}. \qquad \text{(II.16)}$$

Since current jumps physically are impossible in an inductance (see Attachment 2), at moment $t' = 0$, $i_1(0) = 0$, $u_R(0) = 0$ and the source voltage turn out to be applied completely to the inductance $u_L(0) = E$. Self-induction electromotive /31 force [emf] $e_L = -u_L = -L\frac{di_1}{dt}$, which at moment t' is maximum $(e_L(0) = -E)$ *, opposes an increase in current.

*We will recall that, in accordance with the Lenz rule, given any change in current passing across an inductance, self-induction emf arises in it opposing this change; this emf is balanced by voltage $u_L = -e_L$.

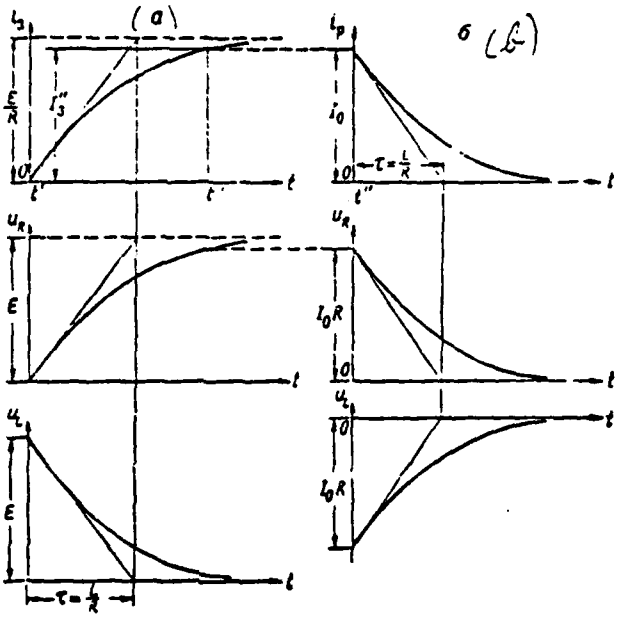

Figure II.4. Curves of Current and Voltage in an R-C Network. (a) — During Inductance Charge; (b) — During Inductance Discharge.

Here, current growth rate $\left(\frac{di_1}{dt}\right)_{t=0} = \frac{E}{L}$ also is maximum. Then, due to the current i_1 increase, the rate of its increase and voltage U_L decrease in accordance with (II.16). Simultaneously, the rise in voltage u_L and the voltage $u_R = i_1 R$ rate of decrease are slowed. In the constraint where $t \to \infty$, the current increase ceases and it reaches amplitude magnitude $I_1 = \frac{E}{R}$. Here, $u_R(\infty) = E, u_L(\infty) = 0$ — the source voltage is balanced completely by the voltage drop in the resistance. /32

We will assume now that, at moment t" following achievement by current i_1 of a certain value $I_3'' = I_0 \left(I_0 < \frac{E}{R}\right)$, switch K will transfer to position 2. Since the external voltage source here is disconnected, while the R-L network is short-circuited, discharge of the inductance begins.

We now for simplicity will accept the moment of discharge initiation as initial moment t" = 0.

This condition must be fulfilled during the discharge process

$$u_R + u_L = 0, \tag{II.17}$$

from whence the network's differential equation will be written $i_p R + L\frac{di_L}{dt} = 0$, while its solution will be

$$i_p = I_0 e^{-\frac{t}{\tau}}, \tag{II.18}$$

where $\tau = \frac{L}{R}$ — circuit time constant.

Based on an analogous law, voltage u_R also will change:

$$u_R = i_p R = I_0 R e^{-\frac{t}{\tau}}. \tag{II.19}$$

The voltage in the inductance equals

$$u_L = L\frac{di_p}{dt} = -I_0 R e^{-\frac{t}{\tau}}, \tag{II.20}$$

i. e., and as follows from (II.17), $u_L = -u_R$.

The curves of exponential functions (II.18), (II.19), and (II.20) are presented in Figure II.4b and can be explained in the following manner. Self-induction emf $e_L = -u_L$, arising due to energy stored in a magnetic field, opposes a decrease in current $i_0 = i_L$ during the discharge process. Here, since self-induction emf changes its polarity (derivative $\frac{di_L}{dt}$ during a current decrease will become negative), the sign of voltage u_L also changes. At initial moment $i_p = I_0$ (current jumps are impossible in an inductance), $u_R = I_0 R$ and $u_L = -I_0 R$, i. e., self-induction emf, and, consequently, current decrease rate, are maximum. A subsequent current decrease in connection with gradual consumption of the stored electromagnetic energy (with its conversion into thermal energy in resistance R) will lead to a decrease in the magnitude of voltages $u_R = -u_L$, i. e., to a decrease in self-induction emf and current decrease rate. Under the constraint where $t \to \infty$ $\frac{di_L}{dt} \to 0$, $u_L(\infty) = -u_R(\infty) = 0$, $i_p(\infty) \to 0$.

The duration of the transient processes in an R-L network as usual can /33 in practice be accepted in accordance with (XI.15) as

$$t_{перех} \approx 3\tau, \tag{II.21}$$

where $\tau = \frac{L}{R}$.

EXERCISE II.2

Draw the curves of current i_L and voltages u_R and u_L from Figure II.4b. Construct on these graphs the curves for i_L , u_R , and u_L , if resistance R is increased by a factor of 2. Explain the results obtained. (Page 446)

3. Principles of Pulse Modulator Operation

The modulator at a pulse RLS is part of the transmitter and shapes powerful modulating video pulses (see Figure I.4). These pulses usually are used as microwave oscillator plate voltage (this type of pulse modulation is referred to as plate pulse modulation).

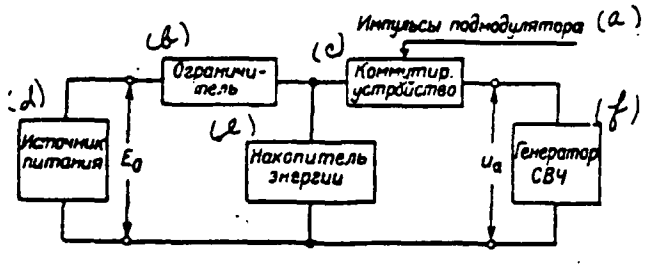

Figure II.5. Pulse Modulator Structural Diagram. (a) — Driver pulses; (b) — Limiter; (c) — Commutating device; (d) — Feed source; (e) -- Energy integrator; (f) -- Microwave oscillator.

A simplified structural diagram of a pulse modulator is presented in Figure II.5 and includes three basic elements: energy integrator, power limiter, and commutating device, which controls the driver video pulses. The overall principle of modulator operation is as follows. The commutating device disconnects the energy integrator from the microwave oscillator during resting times between pulses.

The oscillator does not operate here since it lacks plate voltage ($u_a = 0$). At that moment, the energy integrator is charged from the feed source across the limiter. The latter constrains the power consumed from the source to the magnitude nominal for that source. However, since charge time, given a large pulse duty ratio $Q = \frac{T}{\tau_u}$, occupies an overwhelming portion of the pulse repetition period, sufficient energy is stored in the integrator.

The commutating device connects the microwave oscillator to the integrator for a time equal to pulse duration τ_u. The integrator rapidly discharges to /34 the microwave oscillator (there is no power limiter in the discharge circuit), supplying it the energy accumulated during the resting time. This energy also is converted by the microwave oscillator into a powerful outgoing r-f pulse.

Thus, modulator operation is based on the transient processes of energy integrator charge and discharge. These transient processes must flow in a manner that meets the following conditions:

— amplitude of the modulating video pulse U_a at a given feed source voltage E_0 must be as great as possible;

— the form of the modulating video pulses must be as close to square as possible;

— energy losses in the charge and discharge circuit must be minimal, i. e., modulator efficiency must be as high as possible.

A resistance or inductance is used as power limiter in the integrator charge circuit. Modulator tubes usually play the role of commutating device. A high-voltage transmitter rectifier is the feed source. A capacitor or inductance (choke) may be used as the energy integrator, the modulator's basic element.*

A simplified circuit for a modulator with a capacitive energy integrator is depicted in Figure II.6a. In this circuit, R_0 — limiting resistance, C_n — reservoir capacitor, the commutating device is depicted in the form of switch K with internal resistance R_v, R_r — internal resistance of the microwave generator

*An artificial long line also may be used as energy integrator.

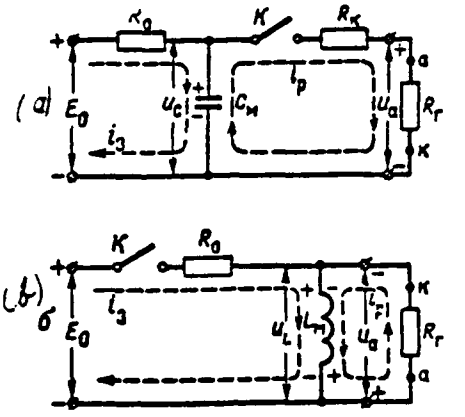

Figure II.6. Modulator Simplified Circuits: (a) — With capacitive energy integrator; (b) — With inductive energy integrator.

in its operating mode (point a corresponds to plate, while point k to the generator's cathode).

Switch K will be open during resting times between pulses and capacitor will charge from the constant voltage E_0 source; switch K closes during a /35 pulse and capacitor $C_м$ will discharge to the microwave generator.

Modulator operation is explained by the curves in Figure II.7. When the modulator is connected to the feed source, capacitor $C_м$ must charge completely. Here, voltage u_c increases by exponent (II.2) from zero to value $U_{c\,max}$ with constant charge circuit time $\tau_1 = R_3 C_м$, while charge current drops by exponent (II.3) with the identical time constant from maximum value $I_{3\,max} = \frac{E_0}{R_3}$ to zero.

The capacitor will discharge to the oscillator with time constant $\tau_2 = (R_р - R_г) C_м$ when switch K closes. Voltage u_c drops during the discharge process by exponent (II.8) from value $U_{c\,max}$ with time constant τ_2; based on the same law (II.9) discharge current $i_р$ drops with a jump arising at the moment the switch closes. This current's

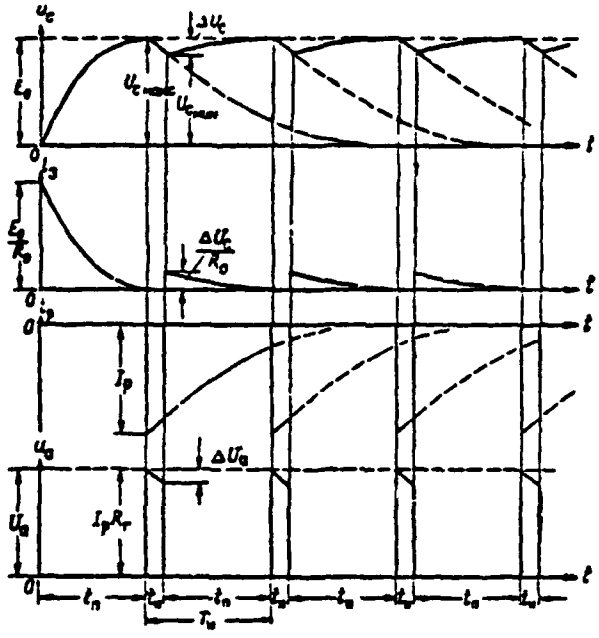

Figure II.7. Curves of Currents and Voltages in a Modulator with a Capacitive Energy Integrator.

amplitude equals $I_p = \frac{E_c - U_{c\,min}}{R_a + R_r}$. A pulse of plate voltage $u_a = i_p R_r$ with amplitude /36 $U_a = I_p R_r = \frac{U_{c\,max}}{R_a + R_r} R_r = \frac{U_{c\,max}}{1 + R_a/R_r}$ arises when discharge current flows in the oscillator. In order for this amplitude to be as great as possible, two things are required. First, essentially full charge of the capacitor must be insured during resting times between pulses. Second, the commutating device must have low internal resistance. Consequently, the following ratios must be provided: $t_n \ll t_n$ (here, $U_{c\,max} \approx E_c$) and $R_a \ll R_r$ (here, $U_a \approx U_{c\,max}$).

By the end of the pulse, voltage in the capacitor decreases to value $U_{c\,min}$, i. e., to magnitude $\Delta U_c = U_{c\,max} - U_{c\,min}$. Accordingly, current i_p decreases during the pulse and plate voltage decreases to magnitude $\Delta U_a \approx \Delta U_c$ (peak of the shaped pulse).

A simplified circuit for a modulator with an inductive energy integrator is depicted in Figure II.6b. In this circuit, R_0 — limiting resistance, which includes the internal resistance of the commutating device, switch K, within it,

K, $L_н$ -- accumulating choke, $R_г$ — microwave oscillator internal resistance in its operating mode. Switch K closes during resting times between pulses and the choke is charged from the voltage E_0 source; switch K opens during the time of the pulse, resulting in discharge of the choke to the microwave oscillator.

A special feature of the circuit with an inductive energy integrator is the capability of using a low-voltage feed source since, given appropriate selection of circuit parameters, the amplitude of the plate voltage U_a pulses may exceed source voltage E_0 greatly.

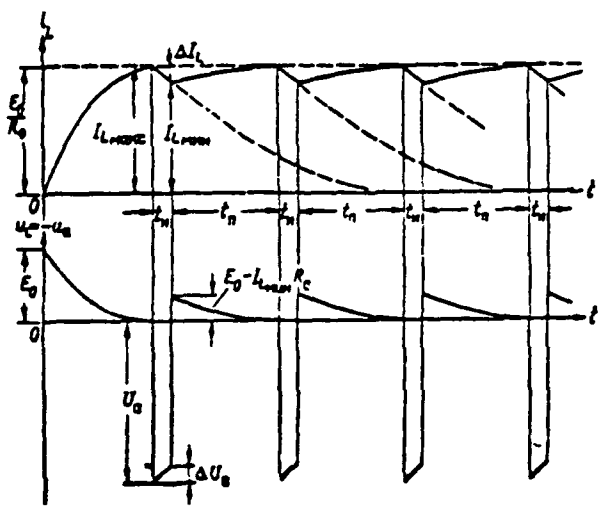

Figure II.8. Curves of the Current and Voltage in a Modulator with an Inductive Energy Integrator.

The curves in Figure II.8 explain the operation of the modulator. Choke $L_н$ will be charged completely when the modulator is connected to the feed source and switch K closes. Here, charge current $i_з = i_L$ increases from zero to maximum value $I_L = \frac{E_0}{R_г}$ by exponent (II.13) with charge circuit time constant $\tau_1 = \frac{L_н}{R_г}$. Voltage $u_L = -u_a$ at the first moment is maximum and equals E_0, but then decreases by law (II.15) with the identical time constant. Since in the charge process

plate voltage u_a is applied as a "minus" to the oscillator plate (point a in Figure II.6b), it does not operate (its internal resistance equals infinity). Therefore, connection of the oscillator to the choke does not exert any influence in the charge process.

The choke begins to discharge to the oscillator the moment switch K opens. Here, current i_L begins to decrease by law (II.18) from value I_L with time constant $\tau_2 = \frac{L_2}{R_2}$. Voltage u_L changes its polarity in connection with a change in the sign of derivative $\frac{di_L}{dt}$ and, with a jump, reaches an amplitude value that is equal /37 to $-U_L = U_a = I_L R_r = E_0 \frac{R_r}{R_0}$. Further, voltages u_L and u_a decrease in connection with the current i_L decrease in magnitude with identical time constant τ_2. Therefore, its peak decreases to magnitude $\Delta U_a = \Delta I_L R_r$ during the time of the pulse. A modulator shortcoming is its low efficiency, which results from passage of large current $i_1 \approx I_L$ (given low ΔI_L) across resistance R_0 during the entire resting time.

EXERCISE II.3

a) Stemming from the law of energy retention, find the ratio between the transmitter's pulse and average power.

b) How should the parameters of a modulator with a capacitive integrator be selected to reduce the decrease in pulse peak (see Figure II.7)? How will this impact upon modulator efficiency and pulse energy?

c) What ratios must be established with an inductive integrator to shape pulses with amplitude $U_a = E_0$ and slight peak decrease ΔU_a? At what pulse duty ratio can these ratios be established? (Page 447)

§ 2. BASIC R-C AND R-L NETWORK TYPES /38

1. Action of a Square Pulse on an R-C Network. Basic R-C Network Types

Figure II.9 presents a depiction of an R-C network and the curves of voltages u_c and u_R when affected by a square pulse with amplitude U and duration t_u at

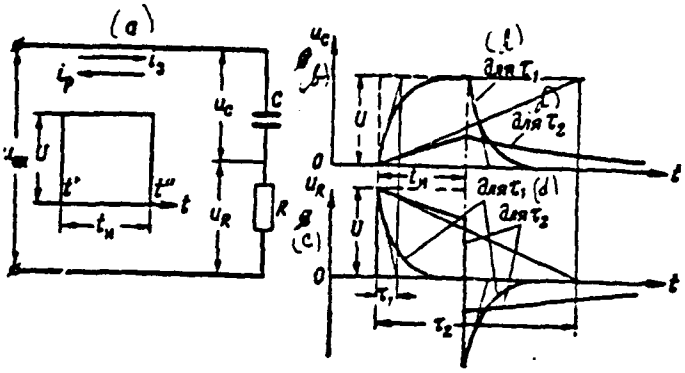

Figure II.9. Effect of a Square Pulse on an R-C Network. (d) — For.

its input. These curves are constructed for two values of network time constant $\tau = RC$: $\tau_1 < t_и$ and $\tau_2 > t_и$ are easily obtained from Figures II.1 and II.2 if one considers that the pulse porch acts at moment t' (switch K in Figure II.1 will transfer to position 1), with its droop at moment $t'' = t' + t_и$ (switch K will transfer to position 2). Actually, given the effect of the pulse porch acted upon by voltage $u_{вх} = U$, capacitor C begins to charge, which is equivalent (in Figure II.1) to charge C from the constant voltage $E = U$ source. Under the effect of the pulse droop $u_{вх} = 0$, capacitor C begins to be completely charged across the input voltage source; if you take the source resistance as being zero, then this is equivalent (in Figure II.1) to an R-C network short circuit.

Thus, the curves in Figure II.9 may be obtained by coincidence of moment t" for the curves in Figures II.2a and II.2b.

If you accept voltage from capacitor C $u_{вых} = u_C$ as circuit output voltage, then the circuit diagram is depicted in accordance with Figure II.11a. In accordance with Figure II.9b, a pulse with a stretched exponential porch and droop is obtained at the output of such a network. The duration of this pulse will be greater and its amplitude lesser the greater the network's time constant.

Assuming in network equation (II.1a) $E = u_{вх}$, $u_C = u_{вых}$, $RC = \tau$ for random input voltage and capacitor output, we will get

$$\tau \frac{du_{вых}}{dt} + u_{вых} = u_{вх}. \qquad (II.22)$$

Given

$$\tau \frac{du_{вых}}{dt} \gg u_{вых} \qquad \text{(II.23)}$$

from equation (II.22) follows

$$\tau \frac{du_{вых}}{dt} \approx u_{вх}$$

or

$$u_{вых} \approx \frac{1}{\tau} \int u_{вх}\, dt \qquad \text{(II.23a)}$$

—output voltage is proportional to the integral from the input voltage. Therefore, an R-C network with a capacitor output (Figure II.11a) is called an integrator.

Given

$$\tau \frac{du_{вых}}{dt} \ll u_{вых} \qquad \text{(II.24)}$$

from equation (II.22) follows

$$u_{вых} \approx u_{вх} \qquad \text{(II.24a)}$$

Condition (II.23) is characterized by a fast, and condition (II.24) by a slow, function $u_{вых}(t)$. Consequently, the network integrates fast functions, high-frequency pulse spectrum harmonics in particular, better than it does slow functions, low-frequency pulse spectrum harmonics in particular. Integration in accordance with (II.23) for given signal form $u_{вх}$ will occur more precisely the greater the time constant τ. However, as follows from (II.23a), output voltage magnitude decreases as τ increases. Consequently, the more precise the integration effect, the less it is.* Therefore, an amplitude condition of approximate integration

*For this reason, an R-C integrator almost always is used in practice, not for mathematical integration of input voltages, but for other purposes involving approximate integrating action of the network (see Chapter II, § 3).

is

$$t_{вых} \ll t_и \qquad \text{(II.25)}$$

Considering that voltage $u_{вых} = u_C$ under the effect of the input signal's porch increases gradually, the following approximate integration time condition /40 corresponds to inequality (II.25)

$$t \ll \tau \qquad \text{(II.26)}$$

where t -- duration of the integration process.

In particular, the following is a condition for approximate integration of a pulse of duration $t_и$

$$t_и \ll \tau \qquad \text{(II.26a)}$$

This is confirmed by the curves in Figure II.9b, from which it follows that only when $\tau = \tau_2 > t_и$ will approximate integration of a square pulse occur during the time it is active.

If voltage $u_{вых} = u_R$ with resistance R is used as network output voltage, then the network diagram is depicted in accordance with Figure II.11b. Two shortened exponential pulses of varied polarity arise at the moment of application of the input pulse's porch and droop given $\tau = \tau_1 < t_и$ at the output of such a network in accordance with Figure II.9c. But, given $\tau = \tau_2 > t_и$, there appears an almost square pulse of identical duration $t_и$ with a peak decreasing according to the exponential law and with an exponential "tail" of opposite polarity.

Assuming $E = u_{вх}$, $RC = \tau$ for random input voltage in network equation (II.1a) and considering that $u_C = u_{вх} - u_R$ according to Kirchhoff's second law and, for this instance, $u_R = u_{вых}$, we will get

$$\frac{du_{вых}}{dt} + \frac{1}{\tau} u_{вых} = \frac{du_{вх}}{dt}. \qquad \text{(II.27)}$$

Given

$$\frac{du_{вх}}{dt} \ll \frac{1}{\tau} u_{вых} \qquad (II.28)$$

from equation (II.27) follows

$$u_{вых} \approx \tau \frac{du_{вх}}{dt} \qquad (II.28a)$$

— output voltage is proportional to the input voltage derivative. Therefore, an R-C network with a resistive output, given a sufficiently-low τ value (see below) is called a differentiating circuit.

Given

$$\frac{du_{вых}}{dt} \gg \frac{1}{\tau} u_{вых} \qquad (II.29)$$

from equation (II.27) follows

$$u_{вых} \approx u_{вх} \qquad (II.29a)$$

Condition (II.28) characterizes a slow, while condition (II.29) a fast, function $u_{вх}(t)$. Consequently, the network differentiates slow functions, low-frequency pulse spectrum harmonics in particular, better than it does fast functions, /41 high-frequency pulse spectrum harmonics in particular. In accordance with (II.28), differentiation for the given form of signal $u_{вх}$ will occur more precisely the smaller time constant τ is. However, as follows from (II.28a), the output voltage magnitude decreases with a decrease in τ. Consequently, the more precise the differentiation effect, the smaller it is.* Therefore, the condition of approximate differentiation based on the ratio of the magnitudes of voltages $u_{вх}$ and $u_{вых}$ may be written in the form

$$u_{вых} \ll u_{вх} \qquad (II.30)$$

*For this reason, a differentiating R-C network is used in practice, not for mathematical input voltage differentiation, but only for pulse shortening (see Chapter II, § 4).

Considering that voltage $u_{вых} = u_R$ decays gradually under the effect of the input signal's porch, the following approximate differentiation time condition corresponds to inequality (II.30)

$$t \gg \tau \tag{II.31}$$

where t -- duration of the differentiation process.

In particular, a condition of approximate differentiation of a pulse with duration $t_и$ is

$$t_и \gg \tau \tag{II.31a}$$

This is confirmed by the curves in Figure II.9c, from which it follows that only when $\tau = \tau_1 < t_и$ does approximate differentiation of a square pulse occur.

Given

$$t_и \ll \tau \tag{II.32}$$

equality (II.29) is accomplished and $u_{вых} \approx u_{вх}$, i. e., this network supplies an output pulse almost without distortion, which is confirmed by the curve in Figure II.9c for $\tau = \tau_2 > t_и$. Here, constant voltage is not transmitted across the network thanks to presence of capacitor C. Therefore, the R-C network depicted in Figure II.11b, when condition (II.32) is met, is called a transient or isolating network and is used for transmission of pulse signal alternating components from the output of one stage to the input of another and separation of these stages based on the direct component.

2. Action of a Square Pulse on an R-L Network. Basic R-L Network Types

An R-L network and the curves of voltages u_L and u_R under the effect of a square pulse with amplitude U and duration $t_и$ on its input are depicted in Figure II.10. These curves also are constructed for two values of network time constant $\tau = \tau_1 < t_и$ and $\tau = \tau_2 > t_и$. They are obtained easily from Figures /42 II.3 and II.4 if one considers that the pulse porch acts at moment t', its droop

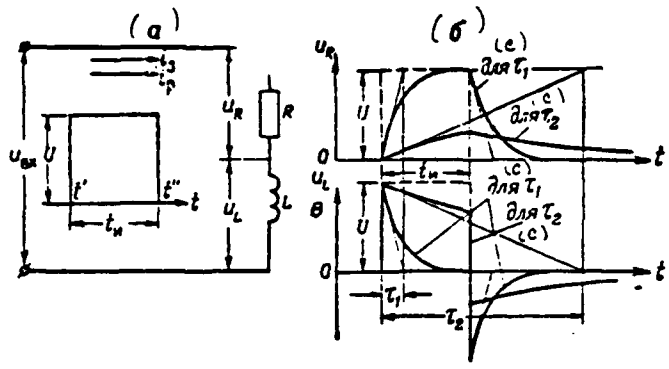

Figure II.10. Effect of a Square Pulse on an R-L Network. (c) — For.

at moment $t''=t'-t_и$, and pulse amplitude U = E and, if one disregards input pulse source resistance (given these conditions, it is sufficient only to match moment t" in Figures II.4a and II.4b).

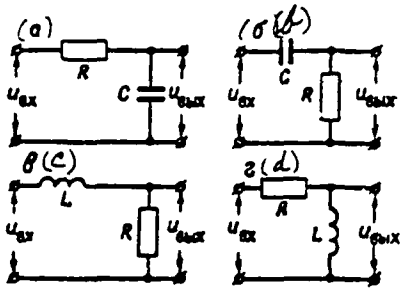

Figure II.11. Basic Types of the Simplest Networks: (a) — R-C integrator; (b) — Differentiating or transient R-C network; (c) — R-L integrator; (d) — Differentiating R-L network.

The network diagram is depicted in accordance with Figure II.11a if voltage $u_{вых}=u_R$ with resistance R is used at the R-L network output voltage. The curves of the network's output voltage (Figure II.10b) in this instance correspond to the curves of voltage $u_{вых}=u_C$ for an R-C network (Figure II.9b). Therefore, based on an analogy with the R-C network depicted in Figure II.11a, this R-L network is an integrator, while the condition for approximate integration of a pulse with

duration τ_n , just as for an R-C integrator, in accordance with (II.26a) (see the curves in Figure II.10b), is

$$t_u \ll \tau.$$

The network diagram is depicted in accordance with Figure II.11c if voltage $u_{вых} = u_L$ with inductance L is used as R-L network output voltage. The /43 curves of the network's output voltage (Figure II.10в) in this case correspond to the curves of voltage $u_{вых} = u_R$ for an R-C network (Figure II.9c). Therefore, by analogy with the R-C network depicted in Figure II.11b, this R-L network is a differentiating circuit, while the condition for approximate differentiation of a pulse with duration t_u , just as for a differentiating R-C network, in accordance with (II.31a) (see the curves in Figure II.10c), is

$$t_u \gg \tau.$$

In both cases, R-L network properties may be explained by analysis of equation (II.12a) and are analogous to the properties of corresponding R-C networks.

EXERCISES II.4

a) Point out the R-C integrators in Figures II.14, II.16, III.18, and IX.4.

b) Compute the time constant of the R-C network depicted in Figure II.11b and determine the purpose of this network if C = 300 pF and R = 10 kΩ.

c) Why can't the R-L network depicted in Figure II.11d be used as a transient network? (Page 447)

§ 3. PRACTICAL USE OF R-C INTEGRATORS

1. Obtaining a Linearly-Changing Voltage

The only use for an R-C integrator (Figure II.11a), when its integrating properties are used in the mathematical sense, is to obtain voltages that change linearly over time.

One must precisely integrate constant voltage $u_{вх} = E = \text{const}$ to obtain a linearly-changing voltage:

$$u_{вых} = \frac{1}{\tau}\int_0^t E\,dt = \frac{E}{\tau}t. \qquad (II.33)$$

Actually, the output voltage of an R-C integrator changes in connection with the charge of a capacitor by the law of exponents (II.2) $u_{вых} = u_C = E\left(1 - e^{-\frac{t}{\tau}}\right)$, i. e., it is distinguished from a linearly-changing voltage (II.33) by magnitude $= E\frac{t - \tau\left(1 - e^{-\frac{t}{\tau}}\right)}{\tau}$, which is an integration error and increases as time passes.

Ratio (II.26) is a condition for approximate integration: $t \ll \tau$; here, based on (XI.16)

$$u_{вых} \approx \frac{E}{\tau}t. \qquad (II.33a)$$

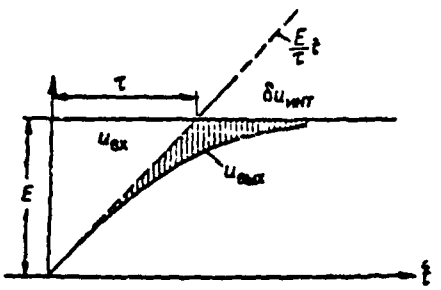

Figure II.12. Use of an R-C Integrator to Obtain Linearly-Changing Voltage.

This is explained in Figure II.12, from which it is evident that only /44 the initial sector of the output voltage may be used as linearly-changing voltage, while the linearity of this sector is better, the shorter it is compared to the circuit's time constant. But here, the output voltage's maximum magnitude decreases:

$$U_{вых} \ll E.$$

2. Stretching Pulse Porches

The form of the pulse arising at the output of an R-C integrator when a square pulse is supplied to its input is depicted in Figure I. .3 (also see Figure II.9b).

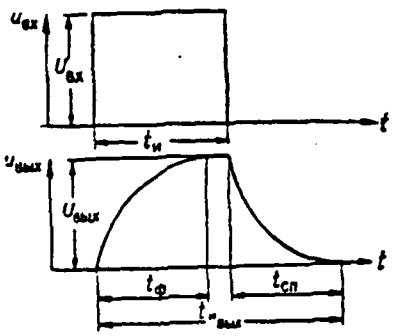

Figure II.13. Stretching an R-C Integrator's Pulse.

Capacitor C will be charged across resistance R during the action of an input pulse for the time of its duration $t_и$, while complete discharge of the capacitor across this resistance will occur after termination of the input pulse. Therefore, in accordance with (II.2) and (II.8), the output pulse's porch is described by expression

$$u_ф = U_{вх}\left(1 - e^{-\frac{t}{\tau}}\right), \tag{II.34}$$

while its droop is expressed

$$u_{сп} = U_{вых}\, e^{-\frac{t-t_и}{\tau}}, \tag{II.35}$$

where $\tau = RC$ — circuit time constant; /45

$U_{вх}$ — input pulse amplitude;

$$U_{вых} = U_{вх}\left(1 - e^{-\frac{t_и}{\tau}}\right) \qquad (II.36)$$

-- output pulse amplitude.

Thus, stretching of both the output pulse's porch and droop will occur. Output pulse duration always exceeds that of the input pulse ($t_{и\,вых} > t_и$) due to the stretching of the former's droop. Therefore, an R-C integrator operating in the mode described usually is called a stretching circuit.

EXERCISE II.5

a) To what are porch and droop duration, as well as complete pulse duration at R-C integrator output, equal?

b) Draw the curves of R-C integrator output voltage when affected at its output by a square pulse with amplitude $U_{вх}$ and duration $t_и = 4$ usec if circuit parameters are R = 1 kΩ, C = 1,000 pF; r = 20 kΩ, C = 200 pF; R = 2 kΩ, C = 0.006 uF. (Page 448)

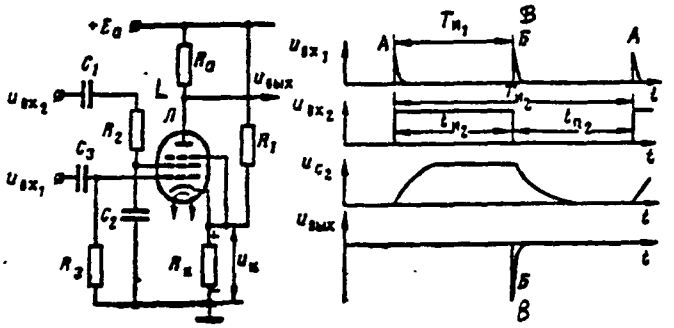

Figure II.14. Variant for Using an R-C Integrator in a Coincidence Circuit.

A variant for using the stretching properties of an R-C integrator in a coincidence circuit is depicted in Figure II.14. The network comprises pentode L, which, in initial state, is blanked along the first and second grids by positive bias u_c supplied to the cathode from divider R_1, R_2. Therefore, the pentode opens for plate current only when there is simultaneous action (coincidence) of positive pulses in the pentode's first and second grids. The amplitude of pulses $u_{вх1}$ and $u_{вх2}$ must be sufficient for reliable opening of the pentode along the corresponding grids. A negative pulse of output (plate) voltage is created in the resistance of anode load R_a while the pentode is open. Short positive input pulses $u_{вх1}$ with repetition period $T_{п1}$ are supplied across transient /46 circuit C_3R_3 to the pentode's first grid. Positive square pulses $u_{вх2}$, whose duration is $t_{и2} = T_{п1}$ and repetition period is $T_{п2}$, are supplied across isolating capacitor C_1 and integrator (stretching circuit) R_2C_2 to the pentode's second grid. The job of the integrator is to separate only those pulses $u_{вх1}$, which coincide with the droop of pulses $u_{вх2}$ (pulse B in Figure II.14).

If there is no R-C integrator, then pulse $u_{вх2}$ would act upon the pentode's second grid without distortions. Here, first, false tripping of the circuit would be possible from A pulses coinciding with the pulse $u_{вх2}$ porch, and, second, proper tripping of the circuit by B pulses would become unreliable. Thanks to the action of the R-C integrator, the porch and drop of the pulse of its output voltage $u_{вых2}$ are stretched. Stretching ("tilting") the porch of this pulse rules out the circuit being tripped by A pulses, while stretching of the pulse's droop insures reliable circuit tripping by a B pulse.

EXERCISE II.6

Formulate the requirements for the magnitude of the time constant for integrator $\tau = R_2C_2$, fulfillment of which is required for normal operation of the coincidence circuit under examination. (Page 449)

3. Obtaining a Time Delay

R-C integrators often are used to create a time delay at the moment pulse trigger circuits or electronic relays are tripped. The following is the general operating principle of such devices. A starting signal in the form of a pulse

or of a change of pulse of positive polarity with a steep porch is supplied to the R-C integrator's input. This network's output voltage picked off the capacitor is supplied to the control grid of starting triode $u_g = u_c$. This triode in the initial state is blanked by negative bias $U_{g0} < E_{g0}$, where $E_{g0} < 0$ — is triode cut-off voltage. Under the influence of the starting signal, voltage at network output (in the triode grid) begins to increase gradually and reaches cut-off voltage E_{g0} only during the passage of a slight amount of time after the effect of the starting signal's porch. Therefore, the moment the triode opens, i. e., tripping of the trigger circuit, is delayed accordingly relative to the starting signal's porch. Delay time $t_з$ will depend on the magnitude of the initial negative voltage in grid U_{g0}, cut-off voltage E_{g0}, and the rate of voltage increase in the capacitor, i. e., on the amplitude of the starting signal and the integrator's time constant.

Provision of sufficiently-high time delay stability requires that the voltage in the tube's grid at the moment threshold cut-off voltage is exceeded increase with a sufficiently-high rate. Therefore, network parameters usually are /47 selected so that the time delay obtained will correspond to the initial sector of the exponent of the R-C integrator's output voltage.

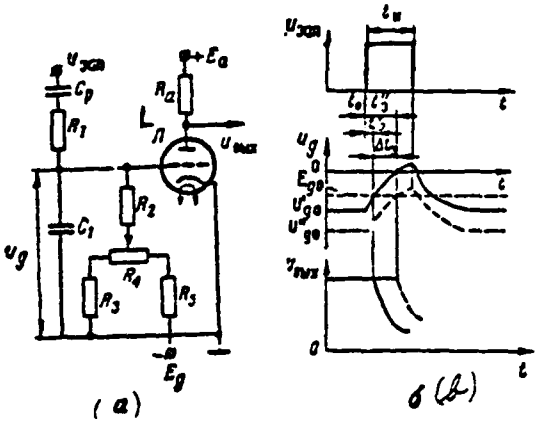

Figure II.15. Trigger Circuit Starting Delay.

One possible trigger circuit starting delay circuit and curves of voltages explaining the obtaining of the delay are depicted in Figure II.15. Starting triode L in initial state is blanked by negative voltage U_{g0}, picked off divider

R_5, R_4, R_3. The magnitude of this voltage may be changed with the aid of potentiometer R_4. A positive square-wave trigger pulse across isolating capacitor C_n is supplied to the input of integrator R_1, C_1 and stretched by it. Therefore, the moment the triode unblocks is delayed relative to the moment of action of the trigger pulse t_0 porch by time $t_з$. A negative change of pulse of its plate voltage $u_a = u_{вых}$, by which the trigger circuit also is tilted (see Chapter VI, § 2), arises the moment the triode unblocks.

Changing the intitial negative voltage in the grid, it is possible within slight limits $\Delta t_з$ also to change the delay time: where $|U'_{g0}| > |U''_{g0}|$ $t'_з > t''_з$. A time delay on the order of units or fractions of microseconds is obtained by using similar circuits.

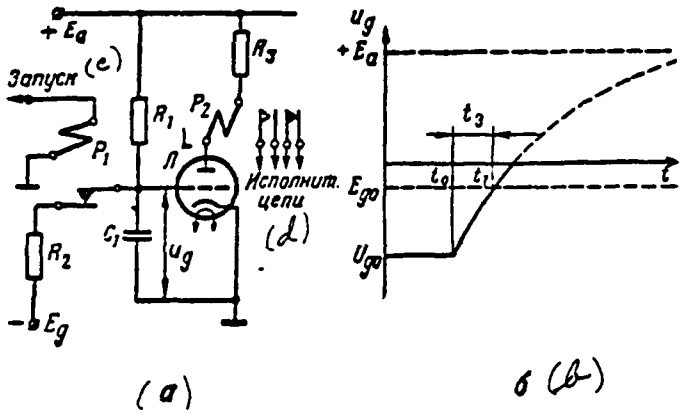

Figure II.16. Electronic Relay Tripping Time Lag. (c) — Start; (d) — Actuator circuits.

A circuit for an electronic relay with fixed time lag $t_з = \text{const}$. is depicted in Figure II.16. The circuit is assembled on triode L and includes voltage divider R_1, R_2, command relay P_1, integrator R_1, C_1, and actuator relay P_2.

The relay P_1 winding is deenergized in the intitial state. The normally-closed contacts of this relay form divider circuit R_1, R_2, from which is picked off constant negative voltage blanking the triode $U'_{g0} < E_{г0}$. Up until this voltage, /48 capacitor C_1 is charged: C_1 [illegible] $t_з$. The command to start the circuit is supplied

at moment t_o in the form of voltage feeding relay P_1. When this relay trips, its contacts open and the divider circuit is interrupted. Recharging of capacitor C_1 along circuit $+E_a$, resistance R_1, capacitor C_1, $-E_a$ (chassis ground) begins from that moment. During the recharging process, voltage in the capacitor increases from initial value $U_{c0}<0$, striving towards value $E_a>0$ by the law of exponents, which, in accordance with (XI.10), may be written in the form

$$u_C = u_g = U_{g0} + (E_a - U_{g0})\left(1 - e^{-\frac{t}{\tau}}\right). \quad (II.37)$$

where $\tau = R_1 C_1$ — recharging circuit time constant.

At moment t_1, when this voltage reaches cut-off voltage, triod L opens, its plate current will pass through the winding of relay P_2, and the latter trips, switching the actuator circuits with its contacts. The voltage rising further in the grid is limited at the zero level due to the tube's grid current, for which sufficiently-large resistance : $R_1 \gg r_{g1}$ is selected (see § V.3).

Lag time $t_3 = t_1 - t_0$ obtained in this manner may reach several seconds.

EXERCISE II.7

a) What limits maximum delay time in the Figure II.15 circuit? What limits the selection of the integrator's time constant?

b) Compute the time lag obtained in the Figure II.16 circuit if /49 E_a = +300 V, E_g = -300 V, R_1 = 2 MΩ, R_2 = 200 kΩ, C_1 = 2 uF, E_{go} = -8 V.

What malfunction will cause the circuit tc trip without a time lag? (Page 449)

4. Conversion of Pulse-Duration Modulation to Pulse-Amplitude Modulation

In the event pulses of varied duration are supplied to the input of an R-C integrator, pulses with an amplitude proportional to the duration of the input

*We accept that $X(\infty) = E_a$, $X(0) = U_{c0}$ in expression (XI.10).

pulses may be obtained at the network's output:

$$U_{вых} \sim t_{и\,вх}. \qquad (II.38)$$

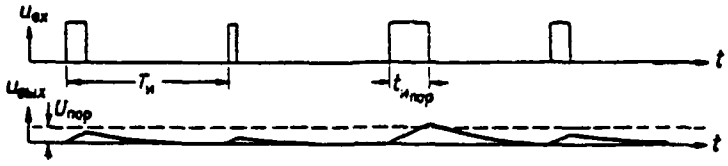

Figure II.17. Conversion of Pulse-Duration Modulation to Pulse-Amplitude Modulation.

This idea behind such conversion is explained in Figure II.17.

An analogous principle may be employed for selection (extraction) of pulses by duration. To do so, R-C integrator output voltage is supplied to the input of the trigger circuit or pulse limiter from below with threshold voltage $U_{пор}$ (dotted line in Figure II.17. Then, pulses will arise at device output only in the event that the pulses at the R-C integrator output exceed value $U_{пор}$, i. e., pulse duration at network input exceeds the assigned duration $t_и \geqslant t_{и\,пор}$.

EXERCISE II.8

How must the R-C integrator time constant be selected in order to fulfill relationship (II.38)? (Page 450)

5. Smoothing Filters

R-C integrators often are used as filters which smooth stray pulsations of constant or slowly-changing voltages. We will determine the frequency characteristics of an R-C integrator in order to explain its filtering properties (see Attachment 6).

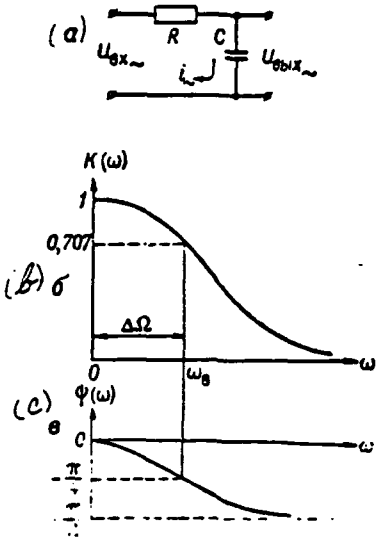

Figure II.18. R-C Integrator Frequency Characteristics.

Using the method of complex amplitude, for R-C network circuitry (see Figure II.18a) we will get

$$\dot{U}_{вых} = \frac{1}{j\omega C}\dot{I} = \frac{\dot{U}_{вх}}{R + \frac{1}{j\omega C}} \cdot \frac{1}{j\omega C},$$

from whence, in accordance with (XI.20), the network's complex frequency characteristic equals /50

$$\dot{K}(\omega) = \frac{\dot{U}(\omega)_{вых}}{\dot{U}_{вх}} = \frac{1}{1 - j\omega CR} = \frac{1}{1 + \omega^2 C^2 R^2} - j\frac{\omega CR}{1 + \omega^2 C^2 R^2}.$$

Hence, based on (XI.23), we will get the expression for the network's AChKh [amplitude characteristic] and FChKh [phase characteristic] in the form

*For separation of the real and imaginary part $\dot{K}(\omega)$, the numerator and the denominator of expression $\frac{1}{1 - j\omega CR}$ are multiplied by expression $(1 + j\omega CR)$, complexly conjugated with the denominator.

$$K(\omega) = \frac{1}{\sqrt{1+\omega^2 C^2 R^2}} = \frac{1}{\sqrt{1+\omega^2\tau^2}};$$
$$\varphi(\omega) = -\operatorname{arc\,tg}\,\omega CR = -\operatorname{arc\,tg}\,\omega\tau. \qquad \text{(II.39)}$$

These characteristics are constructed accordingly in Figure II.18b, c and show that, when harmonic voltage passes across this network, a decrease in its amplitude and a delay in its phase will occur, while both effects manifest themselves the more strongly, the higher the frequency of the harmonic voltage (given $\omega\to\infty K(\omega)\to 0\ \varphi(\omega)\to -\frac{\pi}{2}$). Since low-frequency harmonics (given $\omega\to 0 K(\omega)\to 1\quad \varphi(\omega)\to 0$) will pass across the network in the best manner, it is a low-frequency filter $\omega<\omega_в$. The network's bandwidth $\Delta\Omega$ will fall between frequency $\omega=0$ and upper frequency limit $\omega_в$, which, in accordance with determination of the bandwidth, will be found from condition $K(\omega_в)=\frac{1}{\sqrt{2}}$.

Using the first (II.39) expression for the networks AChKh, we will get

$$\frac{1}{\sqrt{1+\omega_в^2\tau^2}} = \frac{1}{\sqrt{2}},$$

from whence

$$\omega_в\tau = 1 \qquad \text{(II.39a)}$$

If pulses whose spectrum lies completely outside the limits of its bandwidth are active at the network's input, then these pulses will be suppressed at /51 the network's output, i. e., pulse voltage smoothing will occur. The smoothing action of an R-C integrator is explained in Figure II.19.

Since the frequency of the first (lowest-frequency) harmonic of the pulse spectrum equals pulse repetition frequency $\Omega_1=\Omega_и$, then the frequency smoothing condition is

$$\Omega_и \gg \omega_в = \frac{1}{\tau} \text{ или } \tau \gg \frac{1}{\Omega_и} \qquad \text{(II.40)}$$

This condition must be met in all cases where R-C integrators are used as smoothing filters.

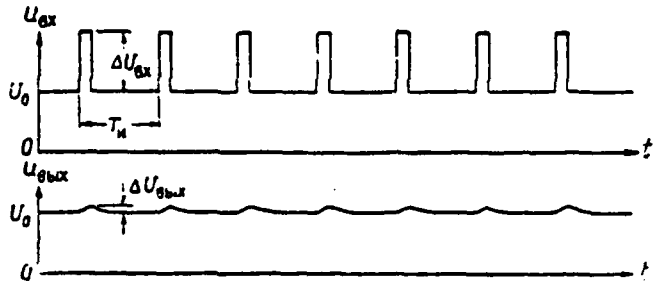

Figure II.19. Voltage Smoothing (Filtration) by an R-C Integrator.

EXERCISE II.9

Explain from physical representations the form of an R-C integrator's AChKh and FChKh (Figure II.18). (Page 450)

6. Influence of Parasitic Parameters

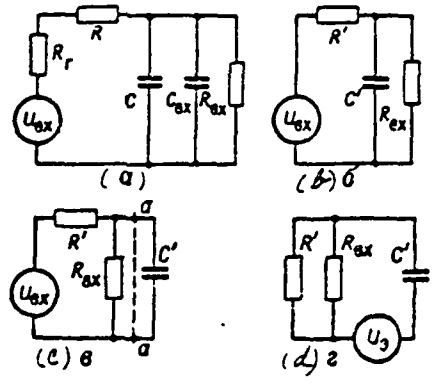

Figure II.20. For Determination of the Influence of Parasitic Parameters on an R-C Integrator.

We will examine the influence of input signal source internal resistance $R_г$, input capacitance $C_{вх}$, and resistance $R_{вх}$ of the next stage (load) on an R-C

integrator. An equivalent circuit for the network considering these parameters is depicted in Figure II.20a. This circuit immediately will lead to the Figure II.20b circuit, where [illegible]. Resistance R' and capacitance C' form an integrator with time constant [illegible]. Thus, source internal resistance and the load input capacitance only improve the network's integrating properties. In the event of necessity, their influence may be considered by the corresponding decrease in R and C. We will redraw the circuit in Figure II.20b in the form shown in Figure II.20c for consideration of the influence of resistance [illegible] and we will use the theorem concerning an equivalent oscillator relative to points aa (see Attachment 5). Then we will get the circuit in Figure II.20d, /52 where, in accordance with (XI.19),

$$u_1 = u_{вх} \frac{R_{вх}}{R + R_{вх}} < u_{вх} \qquad (II.41)$$

while the time constant of the resultant network equals

$$\tau_1 = \frac{R R_{вх}}{R + R_{вх}} C = R_1 C < \tau \qquad (II.41a)$$

Consequently, the influence of resistance $R_{вх}$ manifests itself in the decrease of both network output voltage and its time constant. It is evident from ratios obtained that, given the assigned magnitude $R_{вх}$, it is advisible to use $R' > R_{вх}$, since this only reduces the network's output voltage, essentially without increasing the equivalent time constant, i. e., without increasing integration precision. This consideration limits the maximum value of resistance R.

§ 4. PRACTICAL USE OF DIFFERENTIATING R-C NETWORKS

1. Pulse Shortening (Peaking)

A circuit for a differentiating R-C network was depicted in Figure II.11b. The main use of differentiating circuits is for shortening (peaking) pulses for shaping short-duration pulses for triggering, cut-off, and synchronization of pulse generators and for other purposes. Therefore, differentiating R-C networks also are called choppers. The chopping action of an R-C network is explained /53 in Figure II.21 (see also the curve for voltage u_R in Figure II.9c where

$\tau = \tau_1 < t_{и}$). Due to the action of the porch of a square input pulse (Figure II.21a), in accordance with (II.3), an exponential pulse of capacitor charge current with amplitude $I = \frac{U_{вх}}{R}$ (see Figure II.21b) arises in the network, while the voltage in the capacitor increases by the law of exponents (Figure II.21c). When condition (II.31a) $\tau \ll t_{и}$ is met, the charge of the capacitor essentially ceases long before the termination of the input pulse. Here, $t_1 = 0$, $u_C = U_{вх}$.

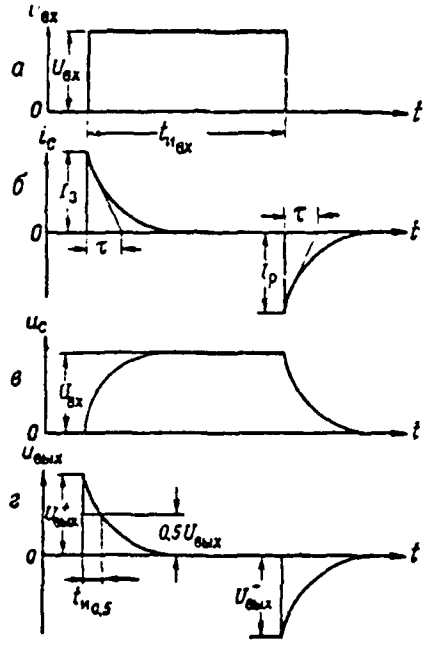

Figure II.21. R-C Chopper Action.

An exponential pulse of capacitor discharge current of opposite direction with amplitude $I_р = I_з = I = \frac{U_{вх}}{R}$ arises in the network in accordance with (II.9) during the action of the input pulse's droop, while the voltage in the capacitor decays by the law of exponents to zero. The network's output voltage is picked off resistance R and equals $u_{вых} = u_{вх} - u_C = i_C R$. Therefore, two short exponential voltage pulses of opposite polarity with identical amplitude $U^{+}_{вых} = U^{-}_{вых} = IR = U_{вх}$

(Figure II.21d) arise at the network's output at the moments of action of the input pulse's porch and droop.

It should be underscored that voltage jumps corresponding to the input pulse's porch and droop always are transmitted completely to the network's output (see Attachment 2). Duration of the output pulses is determined by the network's time constant and coupled to it in the following manner. Since an exponential pulse is described by the expression $u_{вых} = U_{вых} e^{-\frac{t}{\tau}}$, then, determining its active duration $t_{и}$ at level $aU_{вых}$ $(a<1)$, we will get $aU_{вых} = U_{вых} e^{-\frac{t_{и}}{\tau}}$, from whence /54

$$t_{и} = \tau \ln \frac{1}{a}. \qquad (II.42)$$

Using the normal method of computing the active duration of a pulse at level $0.5\,U_{вых}$ (see Figure II.21d), we will get

$$t_{и\,0,5} = \tau \ln 2 \approx 0{,}7\tau. \qquad (II.42a)$$

EXERCISE II.10

Redraw from Figure II.21 the curve of the output voltage of an R-C chopper and indicate how this voltage will change if:

a) the network's time constant is decreased by a factor of 2;
b) if the network's time constant is increased by a factor of 2.
c) if the input pulse's duration is increased by a factor of 2. (Page 451)

2. Influence of the Finite Duration of an Input Pulse's Porch

Above, we examined passage of a square pulse with vertical porches across an R-C chopper. Now we will examine how the finite duration of an input pulse's porch influences the amplitude and shape of this network's output voltage.

For simplicity we will accept that the voltage in the pulse's porch increases by linear law $u_{в} = bt$, where $b = \frac{du_{в}}{dt} = \frac{U_{вх}}{t_{ф}}$ — is pulse steepness, after which it

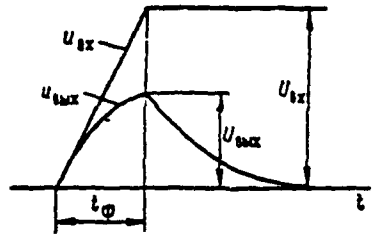

Figure II.22. Influence of the Finite Duration of an Input Pulse's Porch.

will become constant (Figure II.22). We will find the law of change of network output voltage given action of a linear porch with the aid of the Duhamel integral for the network's transient characteristic (see Attachment 8). Assuming in expression (II.14) that $t \geqslant 0$ $E = \sigma(t) = 1$, we will get the network's transient characterisitic (XI.25) in the form $h(t) = e^{-\frac{t}{\tau}}$ and, in accordance with (II.26), we get

$$u_{вых.ф} = \int_0^t be^{-\frac{t-t'}{\tau}} dt' = b\tau\left(1 - e^{-\frac{t}{\tau}}\right). \qquad \text{(II.43)}$$

Hence, the increase rate, i. e., steepness of the output voltage's /55 porch, equals

$$\frac{du_{вых.ф}}{dt} = be^{-\frac{t}{\tau}}. \qquad \text{(II.43a)}$$

At the termination of the porch's action, in accordance with (II.43), output voltage reaches amplitude value

$$U'_{вых} = b\tau\left(1 - e^{-\frac{t_ф}{\tau}}\right) = U'_{вх}\frac{\tau}{t_ф}\left(1 - e^{-\frac{t_ф}{\tau}}\right). \qquad \text{(II.44)}$$

After this, capacitor charge continues, but already under the effect of constant input voltage, in connection with which output voltage decays by the law of exponents

$$u_{вых.сп} = U'_{вых}e^{-\frac{t-t_ф}{\tau}}.$$

It follows from ratio (II.44) that, due to the finite duration of the input pulse's porch, output pulse amplitude decreases in ratio

$$\frac{U_{вых}}{U_{вх}} = \frac{\tau}{t_p}\left(1 - e^{-\frac{t_p}{\tau}}\right). \qquad \text{(II.44a)}$$

This expression will strive towards 1 where $\frac{t_p}{\tau} \to 0$ and decrease given increase $\frac{t_p}{\tau}$, striving towards zero where $\frac{t_p}{\tau} \to \infty$.

The duration of the output pulse increases to the magnitude of the input pulse's porch:

$$t_{и\,вых} \approx t_и + 3\tau. \qquad \text{(II.45)}$$

Ratios (II.43a), (II.44a), (II.45) make it possible to form the following conclusions. Given any differentiating circuit finite time constant, the influence of the finite duration of the input pulse's porch manifests itself in a decrease in the steepness of the input pulse's porch and amplitude (in comparison with the steepness of the input pulse's porch and amplitude) and an increase in the output pulse's duration. The steepness of the output pulse's porch and amplitude increase during an increase in the network's time constant. However, here, output pulse duration increases due to stretching of its droop.

EXERCISE II.11

a) Draw the curves of a differentiating R-C network's input and output voltages given the action on its input of changes of voltage with a vertical and sloping linear porch of identical amplitude, if $\tau = t_и$, $\tau = 2t_и$, $\tau = 0{,}5t_и$.

b) Formulate the condition of pulse porch differentiation. (Page 451)

3. Influence of Parasitic Parameters /56

We will examine the influence on a differentiating R-C network of the internal resistance of the input signal source (of the output resistance of the previous

stage) $R_{\text{г}}$, input capacitance $C_{\text{вх}}$, and resistance $R_{\text{вх}}$ of the next stage (load). An equivalent circuit for the network taking these parameters into account is depicted in Figure II.23a.

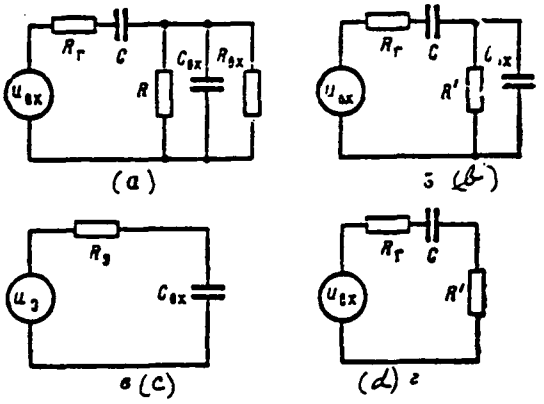

Figure II.23. For Consideration of the Influence of Parasitic Parameters on a Differentiating R-C Network.

Strict analysis of this circuit's properties is sufficiently complex and is not part of our task. However, even its purely qualitative examination permits the following conclusions to be drawn. Resistance $R_{\text{вх}}$ is connected in parallel with resistance R and, therefore, only decreases the network's output resistance, i. e., its time constant. Consequently, this resistance only improves the network's chopping action. Resistance $R_{\text{г}}$, due to the change of voltage forming in it, decreases the network's transfer ratio, i. e., output voltage amplitude. In addition, this resistance increases the network's time constant, which will lead to stretching of the output pulse due to its droop. Capacitance $C_{\text{вх}}$ rules out voltage jumps at network output, i. e., the output voltage's porch is stretched. Thus, it is evident that the influence of parasitic parameters manifests itself in the decrease in output pulse amplitude and additional stretching of its porch and droop. We will examine this problem in greater detail, having assumed that a pulse or a change of voltage with a vertical porch is acting upon the network's input.

The Figure II.23a circuit easily will lead to the Figure II.23b circuit, /57 where $R' = \frac{RR_i}{R - R_i} < R$. We will assume that $C \gg C_{ex}$. Then, it is possible in the first approximation to disregard the influence of capacitor C for rapid changes in output voltage during shaping of its porch, i. e., for the high-frequency harmonics of the output voltage's spectrum. Actually, during pulse shaping time, voltage in this capacitor increases only slightly and, therefore, has almost no influence on output voltage. It is possible to consider from the spectral point of view that, for high-frequency harmonics, capacitor C is only very slight resistance, which need not be considered. In this event, the Figure II.23b circuit, with the aid of the theorem on an equivalent oscillator, will lead to the Figure II.23c circuit, where $R_3 = \frac{R_i R}{R_i - R}$, $U_3 = U_{ex} \frac{R'}{R - R_i}$. This circuit is an R-C integrator and shows that the output pulse's porch is stretched in conjunction with the process of charging parasitic capacitance C_{ex} with time constant $\tau_{ex} = R_3 C_{ex}$. Therefore, porch duration will comprise $t_{p.max} \approx 3 R_3 C_{ex}$. Moreover, since $U_3 < U_{ex}$, output voltage amplitude will decrease.

On the other hand, for slow changes in output voltage during action of the pulse peak or change, i. e., for low-frequency harmonics of the input voltage spectrum, it is possible to disregard the influence of capacitance C_{ex}, since its resistance will be great (current branching to this capacitance $i_{C_{ex}} = C \frac{du_{ex}}{dt}$ is slight). Then, the Figure II.23b circuit will lead to the Figure II.23d differentiating circuit. This circuit's time constant equals $\tau_{ex} = C(R_i + R') > \tau_{ex}$, will lead to stretching of the output pulse's droop: $t_{cn.max} \approx 3C(R_i + R')$. In addition, due to the change of voltage to resistance R_i , output voltage will decrease by a factor of $\frac{R' + R_i}{R'}$. The actual shape of the output pulse is shown in Figure II.24 (dotted line 1 depicts the shape of the output pulse without consideration for the influence of parasitic parameters, while dotted line 2 depicts the /58 shape of the output pulse without consideration for the influence of capacitance C_{ex}). Usually, $C \geq (4 \div 5) C_{ex}$ is chosen, with the output pulse's porch here being still sufficiently short in comparison with its overall duration, which is determined by the decay time. However, the extraordinary increase in C for a decrease in the influence of C_{ex} is unadvisible since, with the assigned output pulse duration, this would require a decrease in resistance $R(\tau = R'C)$. But,

the latter would lead to a decrease in network output voltage due to the influence of resistance R_2 . Moreover, given $R<R_2$, output pulse duration still will depend insufficiently on resistance R(R').

4. Voltage Divider High-Frequency Compensation

The voltage divider R_1, R_2 circuit with transfer ratio $K=\frac{u_{вых}}{u_{вх}}=\frac{R_2}{R_1+R_2}$ is depicted in Figure II.25a. When pulse voltage is transmitted across this divider, load input capacitance $C_{вх}$ (of the next stage) exerts material influence. Since this capacitance shunts the divider's output and its resistance decreases as frequency rises, it elicits high-frequency distortions in the shape of the transmitted pulse -- stretching of its porches. Actually, using the theorem on an equivalent oscillator relative to points aa, we will switch to the integrator circuit in Figure II.25b, where $R_э=\frac{R_1R_2}{R_1+R_2}$. Thus, the shape of the output pulse's porch will be determined by the charge of capacitor C with time constant

$$\tau_э=R_эC_{вх}.$$

Compensating capacitance $C_к$ (Figure II.25c) is connected in parallel to resistance R_1 for divider compensation in the high-frequency realm. This capacitance, shunting resistance R_1 on high frequencies, imparts differentiating properties to the network: the divider's transfer ratio increases for these frequencies (АЧХ roll-off increases in the high-frequency area).* Selection of capacitance $C_к$ magnitude will occur based on the following considerations. The influence of capacitances $C_{вх}$ and $C_к\left(\frac{1}{\omega C_{вх}}\gg R_2,\ \frac{1}{\omega C_к}\gg R_1\right)$ may be disregarded at low frequencies and the divider's transfer ratio equals $K_к=\frac{R_2}{R_1+R_2}$. On the other hand, one may disregard the influence of resistances R_1 and R_2 $\left(\frac{1}{\omega C_{вх}}\ll R_2,\ \frac{1}{\omega C_к}\ll R_1\right)$ at high frequencies. Here, the result is capacitive voltage divider $C_к$, $C_{вх}$ and transfer ratio $K_к=\frac{C_к}{C_к+C_{вх}}$. /59

*Since the steepness of the pulse's porch at divider output increases here, capacitance $C_к$ often is referred to as an accelerating capacitance.

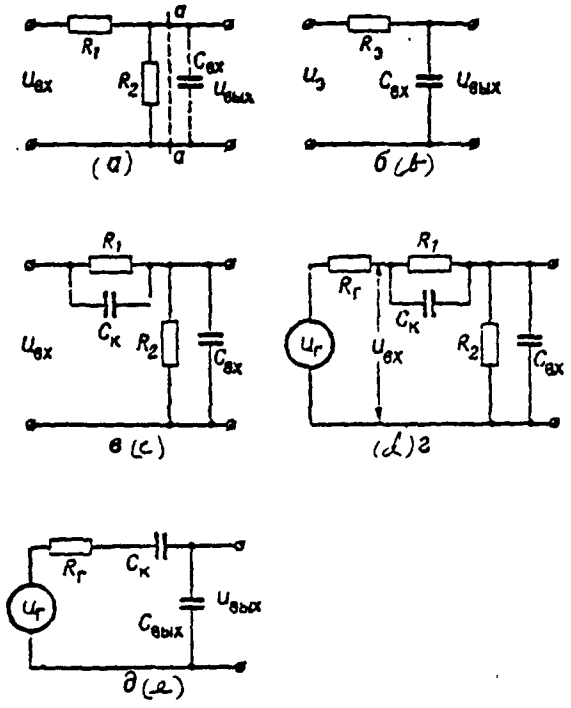

Figure II.25. For Voltage Divider Compensation.

It is evident that equality $K_u = K_0 = \text{const}$ (see XI.24) must be a condition for undistorted pulse transfer, i. e.,

$$\frac{R_2}{R_1 + R_2} = \frac{C_к}{C_к + C_{вх}},$$

hence

$$C_{вх}R_2 = C_кR_1. \qquad (II.46)$$

A divider with compensating capacitance $C_к$ is called a compensating divider when condition (II.46) is met. Such a divider transmits, without distortion, the shape of the $u_{вх}$ pulses acting at its input. However, the shape of these pulses $u_{вх}$ compared to that of oscillator pulses $u_г$ is distorted due to the /60 influence of the internal resistance $R_г$ of the pulse generator. Distorted $u_{вх}$ pulses are transferred to the divider output already without additional distortions when condition (II.46)

is met. Thus, pulse distortions are unavoidable even at the output of the compensated divider. We will turn to the circuit shown in Figure II.25d, where oscillator internal resistance $R_{\text{вн}}$ has been considered, in order to examine this problem.

Disregarding, as usual, the influence of resistances R_1 and R_2 at high frequencies, we will get the circuit shown in Figure II.25e. Given the effect of the pulse $u_{\text{г}}$ porch, capacitance $C_{\text{вых}}$ in this circuit will be charged with time constant

$$\tau_{\text{к}} = R_{\text{г}} C_{\text{э}}$$

where

$$C_{\text{э}} = \frac{C_{\text{к}} C_{\text{вых}}}{C_{\text{к}} + C_{\text{вых}}}.$$

But, if the compensating capacitance was absent, then charging of capacitance $C_{\text{вых}}$ would occur with time constant $\tau = R_{\text{г}} C_{\text{вых}} > \tau_{\text{к}}$ $(C_{\text{вых}} > C_{\text{э}})$. Therefore, connection of compensating capacitance $C_{\text{к}}$ in this case as well will lead to a reduction in the output voltage's porch.

Connection of compensating (accelerating) capacitances is used in triggers, phantastrons, and other pulse circuits, when there is a requirement to compensate for the influence of parasitic capacitances connected to voltage divider output.

EXERCISE II.12

Obtain ratio (II.46) using the expression for the complex frequency characteristic of the network depicted in Figure II.25c. (Page 452)

§ 5. TRANSIENT R-C NETWORKS

1. Role of Transient R-C Networks. Linear and Nonlinear Transient R-C Networks

Radar station pulse devices may comprise many tube stages of varied purpose connected together in a specific sequence. Stage connection, transfer of pulse voltage from the output of one stage to the input of another, as a rule will occur

across transient R-C networks. A transient R-C network insures minimum shape distortion, i. e., of the alternating component of the transmitted pulse voltage and isolation (separation) of stages by direct component. Separation of stages by the direct component is required so that the second stage's operating mode in direct current may be supplied regardless of the direct component of the first stage's output voltage. The circuit for a transient R-C network was depicted in Figure II.11b (it does not differ from a differentiating R-C network) /61 while, in accordance with (II.32), ratio $\tau \gg t_и$ must be met for a transient R-C network.

The processes of charging and discharging capacitor C will occur alternately in the R-C network when pulse voltage is transferred across it. Capacitor charging will occur with time constant $\tau_з = CR_з$, where $R_з$ — resistance in the charging circuit, while discharge will occur with time constant $\tau_р = CR_р$, where $R_р$ — resistance in the discharging circuit.

If resistances in the capacitor charging and discharging circuits equal each other ($R_з = R_р = R$) and, consequently, the time constants of the charging and discharging circuits are equal ($\tau_з = \tau_р = \tau$), then the transient R-C network is referred to as linear. If the resistances in the capacitor charging and discharging circuits are not equal ($R_з \neq R_р$) and, consequently, the charging and discharging time constants are unequal ($\tau_з \neq \tau_р$), then the network is referred to as nonlinear.

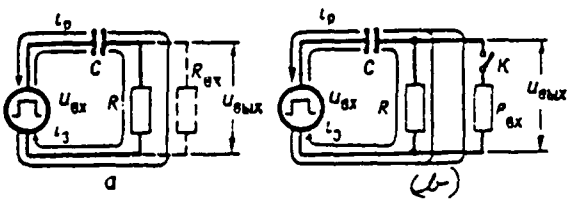

Figure II.26. Linear (a) and Nonlinear (b) Transient R-C Networks.

The ratio of resistances $R_з$ and $R_р$ usually is determined by the properties of the stage's input resistance $R_{вх}$, connected to network output (Figure II.26).

If resistance $R_{вх}$ is not changed as the network operates, then $R_з = R_р = \frac{RR_{вх}}{R - R_{вх}}$ and the network is linear (Figure II.26a).

If resistance $R_{вх}$ for charging current has one value ($R_{вх.з}$), while that for discharging current has another ($R_{вх.р}$), then $R_з = R_р$ and the network is nonlinear (Figure II.26b). For example, if $R_{вх.з} \gg R$ (switch K will be open), while $R_{вх.р} \ll R$ (switch K will be closed), then

$$R_з = \frac{R_{вх.з}R}{R_{вх.з} + R} \approx R,$$

while

$$R_р = \frac{R_{вх.р}R}{R_{вх.р} + R} \approx R_{вх.р}. \qquad (II.47)$$

EXERCISE II.13

a) Point out transient R-C networks in Figures III.18, III.29, VI.5, and VI.10.

b) Draw the curves of the current and voltage in the capacitor and of the output voltage of a transient R-C network given the effect on its input of a change in pulse (step) of constant voltage with amplitude U_0. (Page 453)

2. Passage of a Single Pulse Across a Transient R-C Network

We will assume that a single square pulse is active at the input of a linear transient R-C network. The curves of voltages u_C and $u_{вых} = u_R$ for this example were examined in Figure II.9 (example $\tau = \tau_2 > t_и$) and are repeated separately in Figure II.27. At the initial moment in time (t = 0), $u_{вх} = U_{вх}$, $u_C = 0$ and $u_{вых} = U_{вых.нач} = U_{вх}$, the input pulse's porch will be reproduced completely at the network's output. Further, while the pulse ($u_{вх} = U_{вх} = \text{const}$) is active, capacitor C charging will occur and voltage u_C gradually increases: $u_C = U_{вх}\left(1 - e^{-\frac{t}{\tau}}\right)$. Since $u_{вых} = u_{вх} - u_C$, in accordance with Kirchhoff's second law, then voltage $u_{вых}$ here decreases by the same law of exponents and, at the end of the pulse (where $t = t_и$), will comprise $U_{вых.кон} = U_{вх} - U_{C кон}$, where $U_{C кон} = U_{вх}\left(1 - e^{-\frac{t_и}{\tau}}\right)$ — maximum voltage to which the capacitor was charged. When $\tau \gg t_и$, capacitor C is charged /63 slightly for time $t_и$. Therefore, $U_{C кон} \ll U_{вх}$ and $U_{вых.нач} \approx U_{вых.кон} = U_{вх}$.

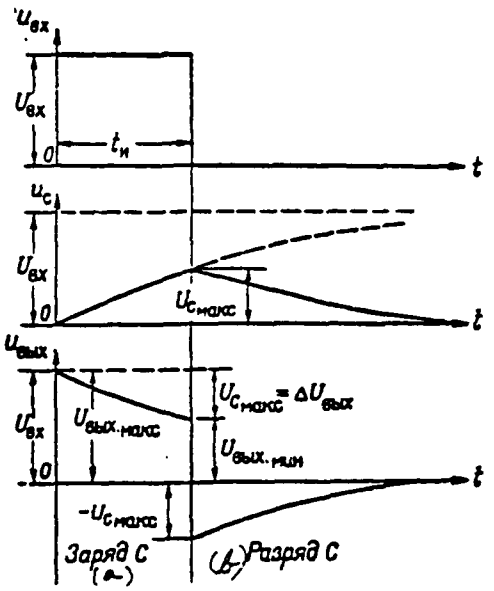

Figure II.27. Passage of a Single Pulse Across a Linear Transient R-C Network. (a) -- C Charge; (b) -- C Discharge.

At moment $t = t_и$, the pulse's droop is reproduced completely at the network's output, output voltage with a jump decreases to value $-U_{C\,макс}$. Actually, when $u_{вх} = 0$, $u_C = U_{C\,макс}$, we will get $u_{вых} = -U_{C\,макс}$. Further, complete discharge of the capacitor with identical time constant τ will occur. During the discharge process, $u_{вых} = -u_C$ (where $t \geqslant t_и$, $u_{вх} = 0$) and voltage $u_{вых}$, remaining negative, decays to zero by the law

$$u_{вых} = -U_{C\,макс} e^{-\frac{t - t_и}{\tau}}.$$

Thus, a single pulse is transmitted across a linear transient R-C network with, in principle, unavoidable distortions, which show up in the exponential decay of the output pulse's peak to magnitude $\Delta U_{вых} = U_{C\,макс}$ and appearance after its termination of an exponential "tail" of negative polarity output voltage with amplitude $-U_{C\,макс}$. Quantitatively, these distortions are evaluated by the factor

$$m = \frac{U_{вых.макс} - U_{вых.мин}}{U_{вых.макс}} = 1 - \frac{U_{вых.мин}}{U_{вых.макс}} \qquad (II.48)$$

Since $u_{вых} = U_{вых.макс} e^{-\frac{t}{\tau}}$, as capacitor C charges, then $U_{вых.мин} = U_{вых.макс} e^{-\frac{t_и}{\tau}}$ and

$$m = 1 - e^{-\frac{t_и}{\tau}}. \qquad (II.48a)$$

hence it is evident that magnitude m will be less, i. e., the closer the input pulse's shape is to being square, the greater the network's time constant τ. Actually, when τ increases, the charge will occur more slowly. Therefore, during time $t_и$, the capacitor succeeds in charging itself to the lesser value $U_{C\,макс}$, resulting in the decay of the pulse's peak, as well as the negative spike amplitude, decrease as well. However, here, if the network is linear, the output voltage's tail elongates in the area $t > t_и$, since capacitor C charging also slows.

If one supplies assumed value $m_{доп}$ and requires that pulse distortions not exceed the assumed values ($m \leq m_{доп}$), then, after taking the logs of (II.48a), we will get

$$\tau \geqslant \frac{t_и}{\ln \frac{1}{1 - m_{доп}}}. \qquad (II.49)$$

This formula makes it possible to compute the requisite magnitude of the transient network's time constant from known duration of the input pulse and assigned value $m_{доп}$. For example, if $m_{доп} = 0.1$ ($U_{вых.мин} = 0.9\ U_{вых.макс}$), then $\tau \geqslant 10.5\ t_и$.

We will examine how the ratio of resistances $R_з$ and $R_т$ influences /64 the shape of the pulse at network output.

During charging, the capacitor acquires quantity of electricity $q_з = \int_{0}^{t_и} i_з\, dt$, where $i_з$ — charging current, while, upon termination of the output pulse, given a complete charge, the capacitor must lose the identical quantity of electricity

$$q_р = \int_{t_и}^{\infty} i_р\, dt = q_з$$

where $i_р$ — discharging current.

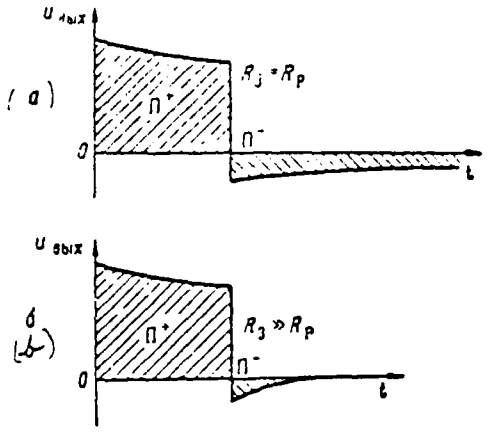

Figure II.28. Ratio of Areas Constrained by Curve $u_{вых}$:
(a) — For a linear R-C network; (b) — For a nonlinear R-C network.

But, according to Ohm's law

$$i_з = \frac{u^+_{вых}}{R_з}, \quad i_р = \frac{u^-_{вых}}{R_р},$$

where $u^+_{вых}$ and $u^-_{вых}$ — positive and negative output voltages arising during the charge and discharge of capacitor C, respectively. Therefore,

$$\frac{1}{R_з}\int_0^{t_и} u^+_{вых}\,dt = \frac{1}{R_р}\int_{t_и}^{\infty} u^-_{вых}\,dt.$$

The integral on the left side of this equality graphically equals the /65 positive area $П^+$ limited by the output voltage curve for the time the pulse is active, while the integral on the right side equals the negative area $П^-$ limited by the output voltage curve after input pulse termination. Therefore, the latter expression may be written

$$\frac{П^+}{R_з} = \frac{П^-}{R_р} \qquad \text{or} \qquad \frac{П^+}{П^-} = \frac{R_з}{R_р}. \tag{II.50}$$

It follows from this that if a transient R-C network is linear ($R_1 = R_2$), then the positive and negative areas limited by the output voltage curve must be equal, i. e., $П^- = П^-$ (Figure II.28a). If it is nonlinear ($R_1 \neq R_2$), then the equality of the areas is disrupted. For example, if $R_1 \gg R_2$, then $П^- \gg П^-$ (Figure II.28b). In this event, capacitor C rapidly discharges after termination of the input pulse due to the slight R_2 magnitude, which also will lead to a reduction of the duration of the voltages negative "tail."

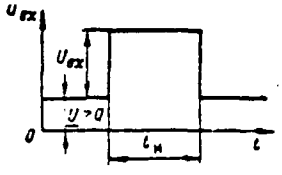

Figure II.29. For Exercise II.14.

EXERCISE II.14

a) Draw curves of voltages u_c and $u_{вых}$ if a pulse with positive initial level $U>0$ (Figure II.29) is active at the input of a linear transient network.

b) Draw the shape of the output voltage of a transient R-C network acted upon by square pulse with $U=0$, if $R_1 \ll R_2$, but $\tau_1 = \tau_2 = CR_1 \gg t_и$. (Page 453)

3. Passage of a Pulse Train Across a Transient R-C Network. Direct Component Loss. Dynamic Bias

We will examine initially passage of a pulse train across a linear transient R-C network. We will assume that a periodic train of square pulses is active at the input of such a network, beginning at moment t = 0 (Figure II.30a). Let mandatory condition (II.32) $\tau \gg t_и$ be met in this network, but the resting time between pulses be insufficient for complete capacitor discharge $t_п < 3\tau$. Then, capacitor C, insufficiently charged during a regular pulse, does not succeed in discharging completely during the resting time. Therefore, during passage of a certain number of the first pulses in the train, positive voltage increment

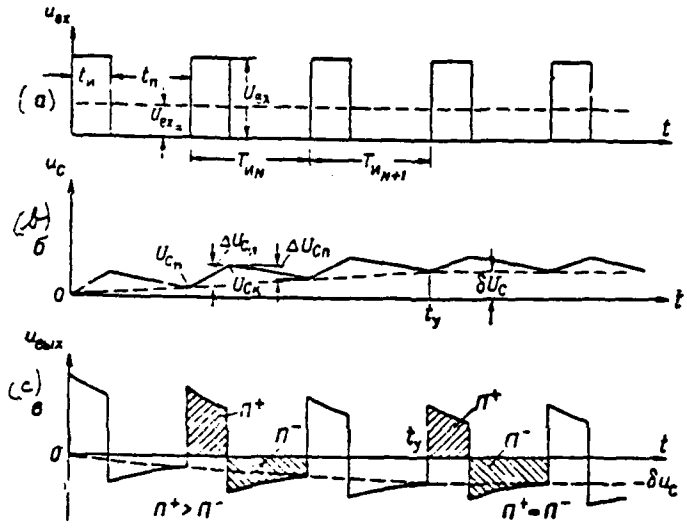

Figure II.30. Passage of a Pulse Train Across a Linear Transient R-C Network.

in the capacitor for the time each pulse ΔU_{Cn} will exceed in magnitude the negative increment of this voltage for the resting time following the pulse ΔU_{Cn} : /66

$$\Delta U_{Cn} > |\Delta U_{Cn}|. \tag{II.51}$$

As a result, as depicted in Figure II.30b, at the beginning of each subsequent pulse, excess voltage $U_{Cn}>0$, will exist in the capacitor. When inequality (II.51) is met as a result of the accumulation of charges in the capacitor, this voltage gradually will increase from pulse to pulse (with a rise in the number of period N), i. e., $U_{Cn}^{N+1} > U_{Cn}^{N}$. Simultaneously, voltage in the capacitor will increase at termination of each succesive pulse $(U_{Cn}^{N+1} > U_{Cn}^{N})$.

Since the charge of the capacitor during the time the pulse is active will occur under the effect of voltage $U_{ex} - U_{Cn}$, while its discharge during resting time will occur from initial voltage U_{Cn} , then based on (XI.10), voltage increments ΔU_{Cn} and ΔU_{Cn}, respectively, equal

$$\Delta U_{C\text{п}} = U^{N}_{C\text{п}} - U^{N}_{C\text{н}} = (U_{\text{вх}} - U^{N}_{C\text{н}})\left(1 - e^{-\frac{t_{\text{и}}}{\tau}}\right); \qquad /67$$

$$\Delta U_{C\text{н}} = U^{N+1}_{C\text{н}} - U^{N}_{C\text{п}} = -U^{N}_{C\text{п}}\left(1 - e^{-\frac{t_{\text{п}}}{\tau}}\right). \qquad \text{(II.52)}$$

Since $U^{N}_{C\text{н}}$ and $U^{N}_{C\text{п}}$ rise as time passes, then positive increments $\Delta U_{C\text{п}}$ gradually decrease, while negative increments $\Delta U_{C\text{н}}$ increase in magnitude. As a result, the rise in residual voltage $U_{C\text{п}}$ gradually slows down. After a certain amount of time $t = t_{\text{у}}$, dynamic equilibrium is established in the capacitor: the amount of electricity accumulated in it during the time of charge $t_{\text{и}}$ and the amount of electricity lost during the time of discharge $t_{\text{п}}$ will become equal $q_{\text{з}} = q_{\text{п}}$. The following equality begins to exist from this moment

$$\Delta U_{C\text{п}} = |\Delta U_{C\text{н}}|, \qquad \text{(II.52a)}$$

while the residual voltage achieves the set value

$$U_{C\text{п}} = \delta U_{C}.$$

The law of change for the network's output voltage is depicted in Figure II.30c. Based on Kirchhoff's second law, $u_{\text{вых}} = u_{\text{вх}} - u_{C}$. As is evident from the curve, due to the increase in residual voltage in the capacitor $U_{C\text{п}}$, the initial

*For simplicity, the moment of the beginning of the charge (initiation of the pulse) is accepted as the initial moment of time t = 0 in the first (II.52) expression, while the beginning of discharge (end of the pulse) is accepted in the second expression.

level of output pulses $\underline{U}_{вых}$ (dotted curve) displaces "downwards" $\underline{U}_{вых} = -U_{Cн}$ and, when $t \geqslant t_и$, it becomes equal to

$$\underline{U}_{вых} = -\delta U_C \qquad \text{(II.52b)}$$

We will find the set value $\underline{U}_{вых.уст}$, stemming from the ratio of areas $П+$ and $П-$ in Figure II.30c. Ratio (II.50) must be met in the set mode and is $(R_i = R_p)$ $П+ = П-$ for a linear network. Disregarding the distorted shapes of the pulses, in accordance with Figure II.30c, in range $t \geqslant t_и$ we will get

$$П+ = (U_{вх} - |\underline{U}_{вых}|)\, t_и, \quad П- = |\underline{U}_{вых}|\, t_п \qquad \text{(II.53)}$$

or, comparing these areas and considering expression (I.3)

$$\underline{U}_{вых} = -\delta U_C = -U_{вх}\frac{\tau}{T_и} = -\frac{U_{вх}}{Q} = -U_{вх\sim} \qquad \text{(II.54)}$$

Thus, when a periodic train of pulses acts upon a linear transient R-C network in the set mode, its capacitor discharges to the value of the input signal's direct component, while the initial level of the output signal displaces to the magnitude of the alternating component with an opposite sign. Here,

$$u_{вых} = u_{вх} + \underline{U}_{вых} = u_{вх\sim} + U_{вх=} - U_{вх=} = u_{вх\sim};\ U_{вых=} = 0 \qquad \text{(II.54a)}$$

— only the alternating component will be reproduced at network output and, /68 consequently, a loss of the input signal's direct component will occur.

We now will move to a nonlinear transient R-C network $(R_з \neq R_р)$.

Disregarding, as usual, pulse shape distortions at network input and using equality (II.53), we will find that, in the set mode based on (II.50), the following condition must be met $\frac{(U_{вх} - |\underline{U}_{вых}|)\, t_и}{|\underline{U}_{вых}|\, t_п} = \frac{R_з}{R_р}$,

hence
$$\underline{U}_{вых} = -\delta U_C = -U_{вх}\frac{t_и R_р}{R_з t_п + R_р t_и} = -U_{вх}\frac{1}{\frac{R_з}{R_р}\frac{t_п}{t_и} + 1}. \qquad \text{(II.55)}$$

*For simplicity in the first expression (II.52) we use the moment of charge initiation (pulse initiation) as the initial moment of time t = 0, and in the second expression - the discharge initiation (pulse end).

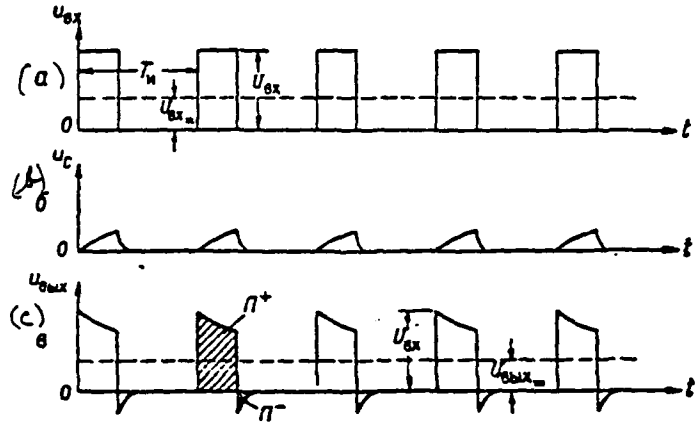

Figure II.31. Passage of a Pulse Train Across a Nonlinear Transient R-C Network Where $R_1 \gg R_2$.

It follows from this expression that, depending on the magnitude of ratio $\frac{R_1}{R_2}$, the ouptput voltage's initial level may change (consequently, as opposed to a linear network, it will not depend on the direct component of input voltage $U_{вх=}$).

Actually, if, for example, $R_1 \gg R_2$, then $\frac{R_1}{R_2} \gg 1$. Consequently, $\Pi^+ \gg \Pi^-$ and, in accordance with (II.55), $U_{вых}=0$. The curves of voltages $u_{вх}$, u_C and $u_{вых}$ for this case are depicted in Figure II.31. Here, capacitor C, slightly charged during the time of pulse $t_и$, then rapidly discharges /69 during resting times as a result of the low magnitude of resistance R_2 . Therefore, at the beginning of the action of each successive pulse, there is no residual voltage in the capacitor (Figure II.31b). Since $u_{вых}=u_{вх}-u_C$, then each pulse at network output begins from the zero level (Figure II.31c). In other words, when $R_1 \gg R_2$, the output voltage's minimum value is fixed at the zero level $U_{вых}=0$. Since $U_{вх}=0$ also (see Figure II.31a), then output voltage essentially

does not differ from input voltage and their direct components are equal ($U_{вых=} = U_{вх=}$) . We will recall that the direct component at the output of a linear network always equalled zero, regardless of the value $U_{вх=}$.

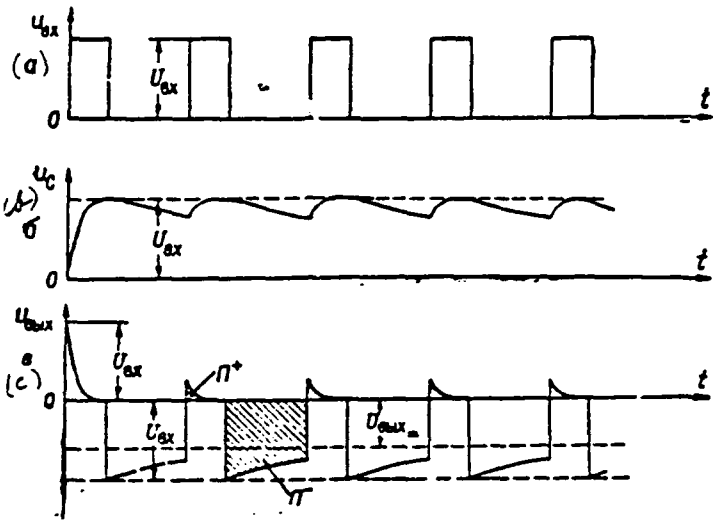

Figure II.32. Passage of a Pulse Train Across a Nonlinear Transient R-C Network Where $R_з \ll R_р$.

If, on the other hand, $R_з \ll R_р$, then $\frac{R_з}{R_р} \ll 1$. Consequently, $П^+ \ll П^-$ and, in accordance with (II.55) $\underline{U}_{вых} \approx -U_{вх}$. Voltage curves corresponding to this event are depicted in Figure II.32. Here, as a result of the low magnitude of resistance $R_з$, capacitor C rapidily is charged during the action of the pulses to their amplitude value $U_{вх}$, while it discharges slightly during rest times. Here, the direct component of the output voltage, in accordance with formula (I.4), is negative and equals

$$U_{вых=} = \frac{U_{вх}}{Q} + \underline{U}_{вых} = \frac{U_{вх}}{Q} - U_{вх} < 0.$$

In this event, the maximum value of the output voltage is fixed at the /70 zero level $U_{вых}=0$.

It is evident that, selecting the resistance $R_з$ and $R_р$ ratio, it is possible to change the output voltage's initial level and direct component within the $U_{вх}$ range.

It should be underscored that, for a nonlinear network as well, the input voltage's direct component as usual will not pass across an isolating capacitor. The direct component of output voltage $U_{вых=}$ is created independently of $U_{вх=}$ by virtue of the networks nonlinear properties.

So, a loss of the input voltage's direct component and bias in the initial level of output voltage will occur generally due to the influence of isolating capacitor C during transmission of a pulse train across a transient R-C circuit. The sign and magnitude of this bias, in accordance with formula (II.55), will depend both on network properties (resistances $R_з$ and $R_р$) and on the input voltage parameters (pulse polarity, amplitude, and duty ratio).

Voltage from a transient R-C network output usually is supplied to the tube stage input. The initial mode of this stage is determined by the initial position of the tube's operating point in its characteristic and is created by bias voltage to the tube's control grid. Additional bias of the output voltage's initial level to magnitude $-\delta U_c$, stipulated by the influence of the transient R-C network, changes the position of the operating point and is referred to as dynamic bias or operating point creep. Usually, the latter is undesireable and is eliminated by using so-called level holds connected to the transient R-C network output (see Chapter IV). In some cases, on the other hand, dynamic bias is used specially in pulse circuits, to replace external negative bias source E_g , for example.

EXERCISE II.15

a) How does a change in initial level, i. e., in the direct component of the input voltage (displacement of the "вх" curve along the "vertical"), influence the output voltage of a linear and a nonlinear R-C network?

b) Cutting off a tube during resting times between pulses requires supplying negative bias $E_g < E_{гр}$, where $E_{гр}$ — tube negative cut-off voltage, to its control grid. What input pulse and transient R-C network parameters will make it possible

to insure tube cut-off due to dynamic bias? Examine the cases of a linear and a nonlinear R-C network separately. (Page 454)

§ 6. SHOCK EXCITATION CIRCUIT

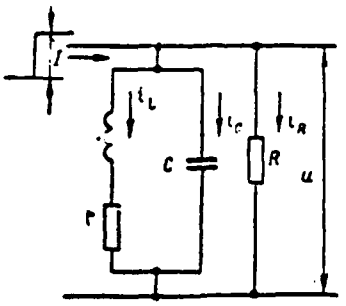

Figure II.33. Parallel Shock Excitation Circuit.

A tuned circuit excited by a change of current or voltage often is used during pulse shaping. This type of circuit is called a shock excitation circuit. A diagram of a circuit excited by a change of current I is presented in Figure II.33. This circuit will comprise inductance L and capacitance C connected to two /71 parallel branches (such a circuit is called parallel); r designates the resistance of an inductor; R designates a resistance shunting the circuit and it may comprise current generator internal resistance, load resistance, or resistance specially connected to create an aperiodic mode (see below). Current and voltage oscillations, stipulated by the periodic exchange of energy between the inductance and the resistance, arise in the circuit when it is excited. The frequency of the oscillations is determined only by the circuit's parameters and, therefore, is distinguished by high stability. Due to presence of resistances r and R, a portion of the energy retained in the circuit's reactive elements, is converted to heat during exchange. Therefore, the amplitude of the excited oscillations unavoidably decreases over time and. in the final analysis, the oscillations cease (such oscillations are referred to as damped oscillations). Energy losses and, consequently, oscillation damping, are greater, the greater the resistance r and the less the resistance R.

In accordance with Kirchhoff's first and second laws, after the action of the change of current, for the circuit we may write

$$I = i_L + i_C + i_R = i_L + C\frac{du}{dt} + \frac{u}{r};\quad u = L\frac{di_L}{dt} + i_L r.$$

Substituting value i_L from the first equation in the second and considering that usually $R \gg r$, after simple conversions we will get the circuit's differential equation:

$$\frac{d^2u}{dt^2} + 2\alpha\frac{du}{dt} + \omega_0^2 u = \omega_0^2 I r_*$$

where $\omega_0 = \frac{1}{\sqrt{LC}}$;

$\alpha = \frac{r + \frac{L}{R}}{2L}$ — damping factor.

Considering the initial condition (at the moment the action of the change takes place $t=0;\ i_L=0;\ u=0;\ i_R=0;\ i_C=I$) and assuming $\alpha<\omega_0$, we will get the solution of the differential equation in the form /72

$$u = \frac{I}{\omega_c C} e^{-\alpha t}\sin(\omega_c t - \varphi) + IR_* \qquad (II.56)$$

where $R_* = \frac{Rr}{R+r}$;

$\omega_c = \sqrt{\omega_0^2 - \alpha^2}$ — frequency of the free oscillations in the circuit;

φ — initial phase shift.

A curve of the damped oscillations in the circuit, constructed in accordance with (II.56), is depicted in Figure II.34.

For determination of the polarity of the first half-cycle of voltage in the circuit, one should consider that, since current jumps are impossible in the branch with the inductance, then, at the initial moment, current $I = i_C$. Therefore,

*Since the circuit contains two reactive elements (capacitance and inductance), a differential equation of the second order results.

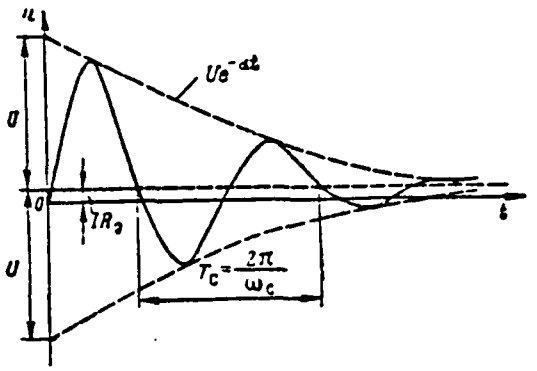

Figure II.34. Damped Voltage Oscillations in the Circuit.

the polarity of the first half-cycle coincides with the polarity of the voltage at the capacitor as it is charged by current I.

If $\alpha \ll \omega_0$ (slight damping), then $\omega_c \approx \omega_0$. Therefore, the amplitude of the voltage in the capacitor equals

$$U_C = U = \frac{I}{\omega_c C} \approx \frac{I}{\omega_0 C} = I\rho,$$

where $\rho = \sqrt{\frac{L}{C}}$ — characteristic resistance of the circuit.

The oscillation mode of a shock excitation circuit may be used for shaping short calibrated pulses occurring with stable period $T_n = T_c$. Oscillating voltage arising in the circuit is amplified for this purpose, subjected to bilateral limiting, and differentiated. One possible use of the circuit in blocking oscillator circuitry also is described in Chapter VII.

The circuit will convert to an aperiodic mode when condition $\alpha > \omega_0$ is /73 met (great damping) due to large energy losses in the resistances: only one "splash" of voltage, whose polarity is identical to that of the first half-cycle in the oscillating mode, will arise in it.

The circuit is shunted specially by slight resistance R to create the aperiodic

mode. Here, one may disregard the influence of inherent losses in the circuit (in resistance r) and consider that $\alpha \approx \frac{\omega^2 L}{2R}$. Then condition $\alpha > \omega_0$ may be written in the form

$$\frac{\omega^2 L}{2R} > \frac{1}{\sqrt{LC}},$$

hence $R < \frac{1}{2}\sqrt{\frac{L}{C}}$.

Therefore, a condition of critical damping in the circuit, during which the oscillating process already does not arise, is

$$R = \frac{1}{2}\sqrt{\frac{L}{C}}. \tag{II.57}$$

If there is no shunt resistance ($R = \infty$), then $\alpha = \frac{r}{2L}$ (damping is determined only by losses in resistance r). In this event, resistance r needs to be increased to obtain the aperiodic mode. From equality $\alpha = \omega_0$, i. e., $\frac{r}{2L} = \frac{1}{\sqrt{LC}}$, we will get the condition of critical damping in the form

$$r = 2\sqrt{\frac{L}{C}}. \tag{II.58}$$

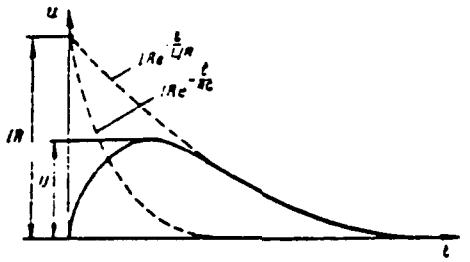

Figure II.35. Aperiodic Voltage "Splash" in the Circuit.

In a case where $\alpha \gg \omega_0$ (strongly-aperiodic mode), the solution of the circuit's differential equation is written in the form

$$u \approx IR\left(e^{-\frac{t}{L/R}} - e^{-\frac{t}{RC}}\right). \tag{II.59}$$

i. e., it is the difference of two exponents, the time constants of which, due to the fact that R is slight, usually is linked with inequality $\frac{L}{R} > RC$. The curve of the aperiodic voltage in the circuit (Figure II.35) is constructed in accordance with (II.59). The duration of the voltage splash received is determined by time constant $\frac{L}{R}$ and approximately equals $\tau_и \approx 3\frac{L}{R}$. Consequently, when R increases, duration $\tau_и$ decreases.

The aperiodic mode may be used for further shaping of the square pulse /74 obtained from the "splash."

Shock excitation of the circuit may be accomplished not only during a positive change of current, but also during a spasmodic decrease in current from magnitude I to zero. Here, the processes in the circuit in principle do not differ from those examined, since the current changing in accordance with law $i = \begin{cases} I & \text{at } t < 0 \\ 0 & \text{at } t \geq 0 \end{cases}$ may be represented by the sum of direct current I and negative change $i = \begin{cases} 0 & \text{at } t < 0 \\ -I & \text{at } t \geq 0 \end{cases}$. Therefore, the shape of the voltage in the circuit will differ from that presented in Figure II.34 only in polarity and in the absence of a constant drop in voltage IR, where $t > 0$ (the last member in expression II.56).

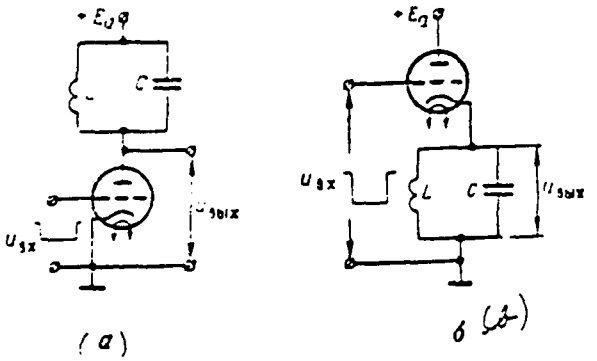

Figure II.36. Methods of Shock Excitation Circuit Connection.

Typical diagrams for connection of the circuit to a triode plate and cathode circuit are shown in Figure II.36. In both diagrams, the triode is operating in the switched mode and will serve for creation of changes in current exciting the circuit. Negative square pulses blocking the triode are supplied to the triode grid for this purpose. Damping oscillations in the circuit are excited twice, during the action of the input pulse's porch (blocking the triode) with a negative change of plate current and during the action of its droop (opening the triode) by a positive change of plate current. However, in the second diagram with the circuit connected to the cathode circuit, when the triode opens, the circuit effectively is shunted by the slight output resistance of the stage with cathode load ($R_{вых} \approx \frac{1}{S}$)*. Here, the mode in the circuit turns out to aperiodic, i. e., damping oscillations arise only during the action of porch $u_{вх}$. In addition, increased amplitude of the negative input pulse is required in this circuit /75 since, during the action of a negative half-cycle of voltage in the loop, the cathode potential decreases and the danger of the triode opening arises. Thus, the amplitude of the negative input pulse must satisfy condition

$$U_{вх} > U_{вых\,max} + |E_{вх}|, \tag{II.60}$$

where $U_{вых\,max}$ — amplitude of the first negative half-cycle $u_{вых}$.

EXERCISE II.16

Draw the curves of voltage $u_{вх}$ and $u_{вых}$ for the circuits depicted in Figure II.36, assuming that oscillations in the circuit arising during the action of porch $u_{вх}$ are damped completely by the time pulse action terminates (during time $t_{вх}$).

(Page 455)

§ 7. PULSE TRANSFORMER

A pulse transformer (IT) is for transformation of pulse voltages and is used mainly for the following purposes:

— changing pulse amplitude or polarity;

*See formula (III.71).

— agreement of resistances (for example, of a load with a feeder's characteristic impedance);

-- couplings between stages or circuits with their isolation by the direct component.

An IT will comprise a primary (input) and secondary (output) winding placed on a common ferromagnetic core. In several instances, an IT may comprise two to three secondary windings where there is a requirement for several output voltages.

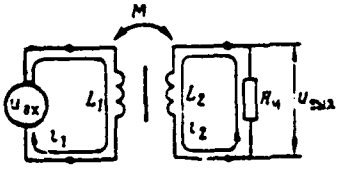

Figure II.37. Pulse Transformer Circuit.

A pulse transformer circuit is depicted in Figure II.37 and does not differ from the circuit of a standard transformer that transforms commercial frequency /76 alternating voltages. In principle, the processes in a pulse and a standard transformer also do not differ and are described by known equations:

$$u_{вх} = L_1 \frac{di_1}{dt} - M \frac{di_2}{dt}; \quad u_{вых} = -L_2 \frac{di_2}{dt} - M \frac{di_1}{dt}. \qquad (II.61)$$

where, in accordance with Figure II.37, L_1 -- inductance, while i_1 -- current of the primary winding; L_2 -- inductance, while i_2 -- current of the secondary winding; M — mutual inductance; $u_{вых} = -i_2 R_н$.

The main specific requirement levied on an IT is minimal distortions in the shape of the transmitted pulses. Considering the spectral composition of pulse systems, this means that an IT must be broadband.

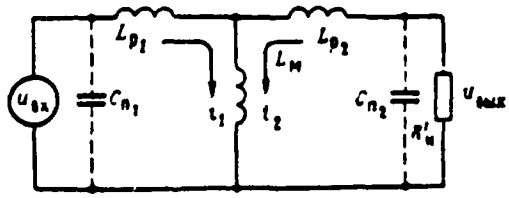

Figure II.38. Simplified IT Equivalent Circuit.

The transformer's core primarily must not be saturated in order to reduce these distortions.* Magnetization flux $\Phi_м$, permeating both windings, and leakage flux $\Phi_{р1}$ and $\Phi_{р2}$, each of which coupled with only one of the windings, arise in the core as the IT operates. Therefore, an equivalent IT circuit may take the form depicted in Figure II.38, where $L_м$ -- magnetization inductance; $L_{р1}$ and $L_{р2}$ -- primary and secondary winding leakage induction, $C_{р1}$ and $C_{р2}$ -- primary and secondary winding parasitic (inter-turn) capacitances.** It follows from examination of this circuit's frequency properties that magnetization inductance stipulates pulse shape low-frequency distortions, i. e., reduction of its peak. These distortions are less, the greater the inductance $L_м$, i. e., the greater the flux $\Phi_м$, and, consequently, the core's magnetic permeability. Leakage inductances stipulate the pulse shape's high-frequency distortions, /77 i. e., stretching of its porches, and must be as slight as possible. Therefore, one will strive for a coupling coefficient close to 1 in an IT:

$$K = \frac{M}{\sqrt{L_1 L_2}} = 1 \qquad \text{(II.62)}$$

High-frequency distortions also are created due to influence of parasitic capacitances $C_{п1}$ and $C_{п2}$, which shunt the IT input and output. Moreover, parasitic capacitances, along with winding inductances, form oscillating circuits, which receive shock excitation from the input pulse's porch and droop. As a result,

*This also provides the basis for conditional assignment of IT to the class of linear circuits.

**Resistances of active losses in each of the windings and in the core and an inter-winding capacitance are not considered in the circuit for simplicity.

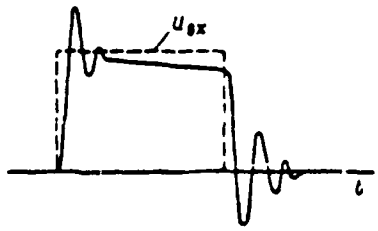

Figure II.39. IT Output Pulse Shape.

parasitic damping oscillations arise as the porch and droop act upon the IT output. The normal shape of an IT output pulse is depicted in Figure II.39.

The (II.61) equations for the Figure II.38 circuit may be written

$$u_{в1} = W_1 \frac{d\Phi_м}{dt} + L_{р1} \frac{di_1}{dt}; \quad u_{вых} = W_2 \frac{d\Phi_м}{dt} + L_{р2} \frac{di_2}{dt}. \tag{II.63}$$

where W_1 and W_2 — number of primary and secondary winding turns.

Hence, it follows that, if there are no leakage inductances $(L_{р1} = L_{р2} = 0)$, then

$$u_{вых} = \frac{W_2}{W_1} u_{в1} = n u_{вх}, \tag{II.63a}$$

where $n = \frac{W_2}{W_1} = \sqrt{\frac{L_2}{L_1}}$ — transformation ratio.

The power the transformer requires from the source equals $p_1 = u_{в1} i_1$, while the power in the load equals $p_2 = u_{вых} i_2$. If one disregards losses of energy in the IT, then $p_1 = p_2$.

$$n = \frac{u_{вых}}{u_{в1}} = \frac{i_1}{i_2}. \tag{II.64}$$

It is convenient to use IT equivalent circuits in which the parameters of the secondary network are converted to the primary (or, vice versa, the parameters of the primary network to the second). In the first instance, if you do not

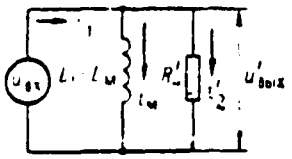

Figure II.40. Simplified Equivalent IT Circuit When Parameters of the Secondary Network are Converted to those of the First Network.

consider leakage inductance and parasitic capacitances, an equivalent IT circuit like the one depicted in Figure II.40 may be used, where $L_м = L_1$ -- magnetization inductance; $i_м$ -- magnetization current creating flux $\Phi_м$; $R'_н$, i'_2, $u'_{вых}$ -- load resistance, secondary network current, and secondary network voltage reduced /78 to the primary network, respectively. The values of the reduced magnitudes will be found from the following considerations.

If there is no load resistance $R_н$ (IT running at no load), then $i_2 = 0$ and all the current of the primary winding would create magnetization flux $i_м = i_1$. When resistance $R_н$ is present, current i_2 creates a degaussing field, whose action is equivalent to a decrease in magnetization current passing across inductance L_1, to slight magnitude i'_2:

$$i_м = i_1 - i'_2 \tag{II.65}$$

This decreased magnetization current also creates magnetic flux inducing reduced output voltage:

$$u'_{вых} = L_1 \frac{di_м}{dt}. \tag{II.66}$$

Based on (II.64), looking upon current i'_2 as current arising in the primary winding as a result of the passage of current i_2 in the secondary winding, we will get

$$i'_2 = ni_2. \tag{II.67}$$

Since current i'_2 appears due to the influence of the load, then, in the equivalent circuit, it flows across reduced load resistance R'_2.

Further, in accordance with Figure II.40, we get $R'_н = \frac{u_{вх}}{i_2} = \frac{u_{вх}}{ni_2}$. But, since $u_{вх} = \frac{u_{вых}}{n}$, while $\frac{u_{вых}}{i_2} = R_н$, then

$$R'_н = \frac{u_{вых}}{i_2 n^2} = \frac{R_н}{n^2}. \qquad (II.68)$$

Finally,

$$u_{вых} = i_2 R_н = ni_2 \frac{R_н}{n^2} = \frac{u_{вх}}{n} = u_{вх}. \qquad (II.69)$$

IT structure must provide minimal leakage inductance and parasitic capacitance values, a maximum magnetization inductance value, and slight losses of energy in windings and the core (to eddy currents) even for the high-frequency components of the pulse spectrum. For this purpose, IT windings have an insignificant number of turns placed one atop the other, while the IT core is wound with fine ribbon steel with a high permeability value and has a relatively-large cross-section while being short. High-quality pot-type magnetic cores are widely used. /79
The steep porches of the currents passing through the IT windings induce high-voltage pulse voltages in its windings $\left(u_L = L\frac{di}{dt}\right)$. This generates the requirement for better IT winding insulation. Nonetheless, the most characteristic IT shortcoming is the insulation's electrical breakdown.

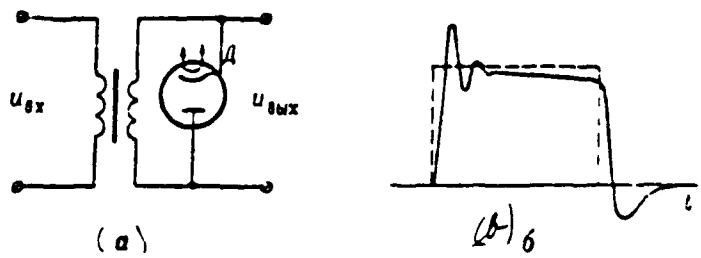

Figure II.41. Damping Diode Connection Circuit and Action.

IT windings sometimes are shunted by resistances, which damp parasitic oscilla. ing circuits and convert them to the aperiodic mode, in order to eliminate output voltage oscillations (Figure II.39). However, here, in accordance with Figure II.35, output pulse droop is stretched. In some cases, the first

positive half-wave of oscillation following the pulse trailing edge is especially undesireable. This half-wave can act upon the next stage just as the basic pulse does (for example, causing a repeat false triggering of the starting circuit). Suppression of this half-wave usually is provided by a special damping diode connected as shown in Figure II.41a. This diode is opened only by the action of negative output voltage. Therefore, while the pulse is active, it remains blocked, i. e., it exerts no influence on pulse shape and, in particular, does not stretch its trailing edge. The diode opens due to the action of the first negative half-wave. Here, since the conducting diode's internal resistance is slight, damping significantly greater than critical will be introduced into the circuit and further oscillations cease (Figure II.41b).

EXERCISE II.17

Explain why, in spite of the presence of inductivities of windings L_1 and L_2, rapid (almost instantaneous) changes in currents i_1 and i_2 are possible in an IT when there is a change of pulse porch and droop. (Page 456)

CHAPTER III /80

PULSE AMPLIFIERS

§ 1. GENERAL INFORMATION ON PULSE AMPLIFIERS

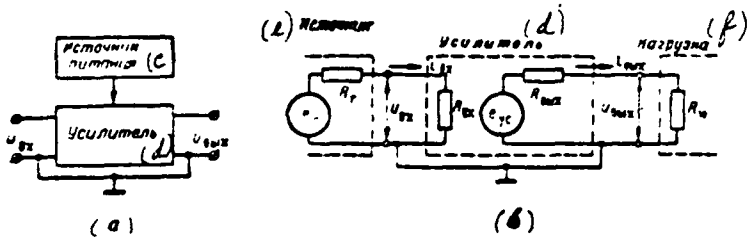

Figure III.1. Amplifier as a Two-Port (a) and Basic Amplifier Structure (b); (c) -- Feed source; (d) -- Amplifier; (e) -- Source; (f) -- Load.

Pulse amplifiers are used in the receiver video amplifier and in other radar station pulse devices when there is a requirement to increase video pulse amplitude without shape distortion. In addition, pulse amplifiers organically are included in such other pulse circuits as certain limiters, pulse generators, sawtooth generators, equation comparison circuits, and so forth. Amplifiers are assembled from electron tubes or transistors. In the most common form, an amplifier can be a two-port having two input and two output terminals with an external supply source connected to them (Figure III.1a). Amplifier input and output, as a rule,

have one common point connected to the circuit's chassis ("grounded"). Control of supply source energy will occur under the influence of a low-power input signal, which thereby creates the output signal. Electron tubes or transistors here play the role of control elements -- valves, regulating the flow of source energy over time based on the law of input signal change. Thus, from a power point of view, signal amplification is stipulated by source energy consumption.

Voltages and currents in an amplifier generally also have direct and /31 alternating components. Direct components determine the mode when input voltage equals zero. Alternating components determine the amplifier's "a-c" operating mode. This very mode characterizes the passage of pulse signals across the amplifier. Therefore, for analyis of pulse amplifier operation, we will use their structural and equivalent circuits only for alternating components. The element determining the amplifier's "a-c" operation are not depicted in these circuits, all d-c sources being replaced by a short circuit, in particular.

An amplifier structural diagram is presented in Figure III.1b, in which the input signal source is represented by emf generator $e_г$ with internal resistance $R_г$ loaded to amplifier input resistance $R_{вх}$, while the amplifier itself from the output -- in the form of emf generator $e_{ус}$ with internal output resistance $R_{вых}$ loaded to load resistance $R_н$ *.

Amplifier input resistance $R_{вх}$ is understood to mean its internal resistance measured from the input terminals, while output resistance $R_{вых}$ is understood to mean its internal resistance measured from the output terminals, i. e., resistance which the external load "encounters."

Figure III.1b amplifier input and output circuits conditionally are depicted as isolated. Coupling between them is reflected by ratio

$$e_{ус} = K^* u_{вх},$$

where K* -- amplifier voltage gain without considering the effect of load resistance.

*Any of the emf generators may be represented also in the form of a current generator (see Attachment 4); here, other amplifier structural diagrams result. In addition, generally speaking, all resistances in Figure III.1b may be complex.

Amplifiers are categorized as voltage, current, and power, depending on the ratio of the parameters in their input and output circuits.

If this condition is satisfied

$$R_{вх} \gg R_г, \quad R_н \gg R_{вых}. \tag{III.1}$$

then inout and output current are insignificant (the output signal source and the amplifier itself operate virtually in a no-load mode), while input and output voltages are maximum:

$$u_{вх} = i_{вх} R_{вх} = e_г \frac{R_{вх}}{R_{вх} + R_г} \approx e_г; \quad u_{вых} = e_{ус} \frac{R_н}{R_н + R_{вых}} \approx e_{ус} \tag{III.1a}$$

In this event, the amplifier's determinant property is voltage amplification and its basic parameter is voltage gain, understood to mean the ratio of the output voltage increment to the input voltage increment that caused it: /82

$$K_u = K = \frac{\Delta u_{вых}}{\Delta u_{вх}}. \tag{III.2}$$

The (III.1) ratios are satisfied usually for electron tube amplifiers, which also will fall in the category of voltage amplifiers.

If this condition is satisfied

$$R_{вх} \ll R_г; \quad R_н \ll R_{вых}. \tag{III.3}$$

then input and output voltage are insignificant (input signal source and the amplifier itself operate virtually in a short-circuit mode), while input and output voltage are maximum:

$$i_{вх} = \frac{e_г}{R_{вх} + R_г} \approx \frac{e_г}{R_г}; \quad i_{вых} = \frac{e_{ус}}{R_{вых} + R_н} \approx \frac{e_{ус}}{R_{вых}}. \tag{III.3a}$$

In this event, the amplifier's determinant property is current amplification and its basic parameter is current gain

$$K_i = \frac{\Delta i_{вых}}{\Delta i_{вх}}. \tag{III.4}$$

Ratio (III.3) usually is satisfied for transistor amplifiers, which therefore fall in the current amplifier category.

If conditions whereby the generator agrees with load (see Attachment 4) are met for the source of the input voltage and of the amplifier itself

$$R_{вх} = R_г; \quad R_н = R_{вых}, \tag{III.5}$$

then input signal power consumed at amplifier input and output signal power supplied to load are maximum and the amplifier is a power amplifier.

In practice, amplifier division into three categories will be less strict. For example, the term current amplifier is given to a voltage amplifier based on operating conditions at input with a current output ($R_г \gg R_{вх}$; $R_н \ll R_{вых}$). The term power amplifier is applied to a voltage amplifier based on operating conditions at input with power output ($R_{вх} \gg R_г$, $R_{вых} = R_н$), and so forth. One also should keep in mind that power amplification of a signal must occur in any amplifier, even when agreement conditions (III.5) are not satisfied.

Pulse amplifier special features are linked with the requirement to obtain minimum distortion of amplified pulse shapes. Electron tube and transistor amplifiers have nonlinear volt-ampere characteristics. The amplifier operating mode is selected so that essentially only the linear sectors of these characteristics are used when an input signal is active in order to decrease nonlinear distortions. This also provides a basis for representing the amplifier by equivalent circuits /83 justified for linear devices.

Amplifier bandwidth must be as large as possible (see Attachment 7) to decrease linear (frequency) distortions. Therefore, resistances are used as the pulse amplifier load and, moreover, special frequency compensation measures are used to compensate for the influence of stray and coupling capacitances.

§ 2. ELECTRON-TUBE AMPLIFIER OPERATING PRINCIPLE

1. Electron-Tube Static Characteristics and Parameters

Tube device output voltages are picked off load resistances connected to the tube's plate current network. Tube characteristics and parameters, not considering the influence of load resistances, i. e., describing the properties of the tubes themselves, are referred to as static.

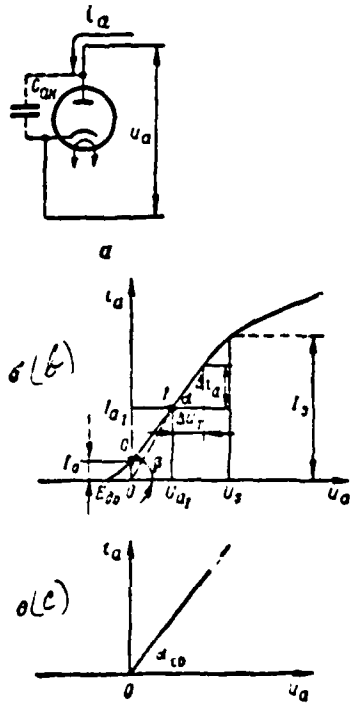

Figure III.2. Diode (a), Its Actual (b), and Idealized (c) Plate Characteristics.

A diode, having only two electrodes -- a cathode and an anode (Figure III.2a) -- is the simplest electron tube. The properties of a diode as a nonlinear resistance are described completely by the diode's static plate characteristic (Figure III.2b), by the relationship of its plate current to plate voltage:

$$i_a = \varphi(u_a). \qquad \text{(III.6)}$$

In this characteristic, $E_{зап}$ — diode cut-off voltage, U' — saturation voltage, I — saturation current. When $u_a>0$ (plate potential exceeds cathode potential), a plate accelerating electrical field exists in the diode, under the influence of which electrons emitted by the cathode displace to the anode. In area $0<u_a<U'$ (area of spatial charge existence) relationship (III.6) essentially is linear. When $u_a=0$, slight initial current I_0 (on the order of tenths of /84 a milliampere) exists in the diode since several of the fastest electrons emitted by the cathode are supplied to the plate and there is no accelerating field. Therefore, complete cessation of plate current (diode cut-off) will occur given a certain negative plate voltage $u_a=E_{зап}$, which, for the majority of diodes, is -0.25 to -0.75 V. In the range $E_{зап}<u_a<0$, the plate characteristic is nonlinear, which is stipulated by the random distribution of initial electron speeds. In practice, the nonlinearity of the diode's plate characteristic and values $E_{зап}$ and I_0 are disregarded and the idealized plate characteristic (Figure III.2c) is used.

Thus, the diode's main property is its unilateral conductivity. A diode has no amplification properties due to the absence of a grid. Therefore, diodes are used for nonlinear conversions of pulse signals not linked with their amplification in such devices as detectors, level holds, and amplitude limiters. We will examine a diode's basic parameters.

The ratio of the plate current increment to the plate voltage increment it caused is called the diode's transconductance:

$$S=\frac{\Delta I_a}{\Delta u_a}\left[\frac{мА}{в}\right]. \qquad (III.7)$$

Graphically, transconductance is determined to be the tangent of the slope of the characteristic at a given point to the X-axis ($S=\operatorname{tg}\alpha$) (see Figure III.2b).

The diode's internal resistance to alternating current is the ratio of the plate voltage increment to the plate current increment it caused:

$$R_д=\frac{\Delta u_a}{\Delta I_a}=\frac{1}{S}\ [ом]. \qquad (III.8)$$

Values S and R_i are constant for the characteristic's linear sector, S decreases in the lower and upper nonlinear sectors, while R_i increases.

A diode's internal resistance to direct current is the ratio of plate voltage to plate current:

$$R_{oo} = \frac{u_a}{i_a} \text{ [ом]} \tag{III.9}$$

A diode's internal resistances to alternating and direct current generally do not equal each other. Thus, for point 1 in the linear sector $R_0 = CT_\beta$, but $R_{oo} = \frac{U_a}{I_a} = CT_\alpha$, since $\beta > \alpha$, then $R_{oo} < R_0$. Values R_0 and R_{oo} coincide for the diode's idealized characteristic.

The less a conducting diode's internal resistance (forward resistance) and the greater a blocked diode's internal resistance (back resistance), the /85 more nearly are its electrical valve-like actions expressed. The internal resistance of most diodes used in pulse technology to alternating current for the linear sector of the characteristic will range from 100--1,000 ohms, while the back resistance will be hundreds of megohms.

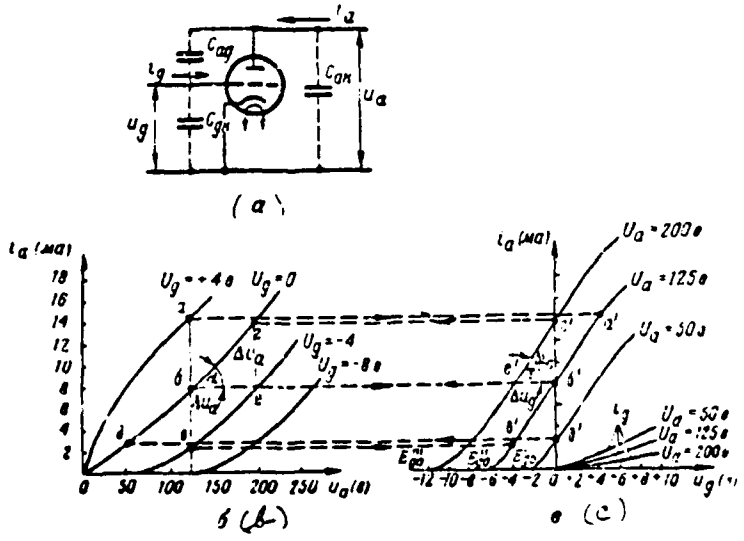

Figure III.3. Triode (a), Its Plate (b), and Its Transfer and Grid Characteristics (c).

A diode's stray interelectron capacitance C_{a} (in Figure III.2a it conditionally is connected by the dotted line outside the tubes bulb) may have significance as diodes operate in pulse circuits. This capacitiance is referred to as a transfer capacitance and usually comprises about 5 pF.

The simplest amplifier tube is a triode, which has three electrodes -- anode, cathode, and control grid (Figure III.3a).

Triode plate current is a function of two variables -- plate and grid voltages:

$$i_a = \varphi(u_a, u_g). \tag{III.10}$$

Therefore, a triode's basic properties are described by relationships of two forms:

$$i_a = \varphi(u_a) \quad \text{where} \quad U_g = \text{const}; \tag{III.11}$$

$$i_a = \varphi(u_g) \quad \text{where} \quad U_a = \text{const}. \tag{III.12}$$

Relationships (III.11) for various fixed values U_g are referred to as /86 static plate characteristics (Figure III.3b), while relationships (III.12) for various fixed values U_a are referred to as static transfer characteristics (Figure III.3c).

Negative voltage E_{g0} in transfer characteristics where current i_a ceases is referred to as cut-off voltage or triode cut-off. Cut-off voltage for higher U_a values increases in magnitude (transfer characteristics displace "to the left") since a greater grid brake field is required to neutralize the plate accelerating field. Plate and transfer characteristics in different coordinate systems reflect the identical (III.10) relationship. Therefore, they are coupled organically: transfer characteristics may be plotted from the family of plate characteristics and, on the other hand, plate characteristics may be plotted from the family of transfer characteristics (see dotted-line plots in Figure III.3b, c).

Given $u_g > 0$, grid current i_g, passing from the grid to the cathode arises

in the triode, along with plate current, due to electrons which are intercepted by the control grid. Relationship

$$i_g = \varphi(u_g) \qquad \text{where} \qquad U_a = \text{const} \qquad \text{(III.13)}$$

are referred to as grid characteristics (grid current characteristics). They are plotted on the same curve with the transfer characteristics (Figure III.3c) and demonstrate that the conducting properties of the triode's grid--cathode path are analogous to the diode, for which the triode's grid plays the role of plate.

We will examine a triode's basic static parameters.

Transconductance of a triode static transfer characteristic (abbreviated simply as transconductance) is the term used for the ratio of the plate current increment to the voltage on the grid that caused it, given constant plate voltage:

$$S = \frac{\Delta i_a}{\Delta u_g} \text{ [ma/v]} \qquad \text{where} \qquad U_a = \text{const.} \qquad \text{(III.14)}$$

Transconductance characterizes the efficiency of the grid's control activity and demonstrates by how many milliamperes triode plate current changes when grid voltage changes 1 volt. Value S equals the tangent of the triode transfer characteristic slope for a given value U_a at a given point to the X-axis (see triangle $6'2'e'$ in Figure III.3c, where $S = \text{tg}\gamma$). $S = 2 \div 5$ mA/V in the linear sector of the characteristics for the majority of triodes.

Triode gain μ is the term describing the ratio of the increments of plate and grid voltages, each of which that, acting independently, would cause an identical change in plate current:

$$\mu = \frac{\Delta u_a}{\Delta u_g} \qquad \text{where} \qquad \Delta i_a = \text{const.} \qquad \text{(III.15)}$$

The concept of this parameter may be explained in the following manner. /87 Since the grid will be closer to the cathode than the anode, a change in voltage u_a affects plate current magnitude greater by a factor of μ than such a change in voltage u_g. In other words, obtaining a given change in plate current requires that the plate voltage increment be greater by a factor of μ than the grid voltage

increment. Value μ may be determined both from the family of plate and from the family of transfer characteristics. Thus, for example, examining triangle $6ee$ in Figure III.3b, we see that a change in plate current by magnitude $\Delta i_a = ee$ requires either that, given $U_g = 0$, plate voltage be changed by magnitude $\Delta u_a = 6e = 75$ V, or, given $u_a = 200$ V, changing grid voltage by magnitude $\Delta U_g = 4$ V. Examining triangle $6'e'e'$ in Figure III.3c, we see that obtaining an identical change in plate current $\Delta i_a = e'6' = ee$ requires either, given $U_g = -200$ V, changing grid voltage by magnitude $\Delta u_g = e'6' = 4$ V, or, given $u_g = 0$, changing plate voltage by magnitude $\Delta U_a = 75$ V. In both instances, we will get $\mu = \frac{\Delta u_a}{\Delta u_g} = \frac{75}{4} \approx 19$.

It is possible also to determine gain from approximate formula

$$\mu = -\frac{U_a}{E_{g0}}, \tag{III.16}$$

where E_{g0} -- triode cut-off voltage corresponding to given value U_a.

Values μ for triodes usually comprise several tens of unities.

The ratio of the increment of plate voltage to the plate current increment it caused, given constant grid voltage, is referred to as a triode's internal resistance to alternating current R_i:

$$R_i = \frac{\Delta u_a}{\Delta i_a} \ [\text{ом}] \qquad \text{where} \qquad U_g = \text{const} \tag{III.17}$$

The physical concept of this parameter is identical to that for a diode. Value R_i will be found from the triode's plate characteristic for given value U_g (see, for example, triangle $6ee$ in Figure III.3b, where $R_i = \frac{\Delta u_a}{\Delta i_a} = \operatorname{ctg} \alpha$). The magnitude of resistance R_i for triodes usually comprises unities or tens of kilohms.

A triode's internal resistance to alternating current R_{i0} is, as for a diode, the ratio of plate voltage to plate current:

$$R_{i0} = \frac{u_a}{i_a}. \tag{III.18}$$

Value R_{i0} is determined from the triode's plate characteristic and may be changed within broad limits, both during a change in plate voltage (as a /88 result of the nonlinearity of the characteristics) and especially during a change in grid voltage.

Using expressions (III.14), (III.17), and (III.15), we will get

$$SR_i = \mu. \qquad \text{(III.19)}$$

Ratio (III.19) is referred to as the triode's basic or internal equation.

There are three interelectrode capacitances in a triode, conditionally depicted in Figure III.3a inside the tube's bulb. Grid--cathode capacitance C_{ck} is called input capacitance, plate--cathode capacitance C_{ak} output capacitance, and plate--grid capacitance C_{ag} is called triode transfer capacitance. Interelectrode capacitance values in triodes usually comprise unities of picofarads.

EXERCISE III.1

a) Prove ratio (III.16).

b) Determine and compare triode resistances to alternating and direct current as points a, b, c in Figure III.3b.

c) Explain the relative position of the grid current characteristics for various values i_a in Figure III.3c. (Page 456)

A triode shortcoming is significant (2--15 pF) transfer capacitance C_{ag}, which stipulates the stray capacitive coupling between input and output circuits for the high-frequency components of the pulse spectrum.

A five-electrode amplifier tube, a pentode, which, along with control grid g_1, has screen grid g_2 and suppressor grid g_3 (Figure III.4), to a significant degree is free from this shortcoming. Screen grid g_2 functions as an electrostatic screen between the plate and control grid g_1. Grid g_2 "grounds itself" for the alternating component across bypass capacitor C_{c2} to eliminate the capacitive

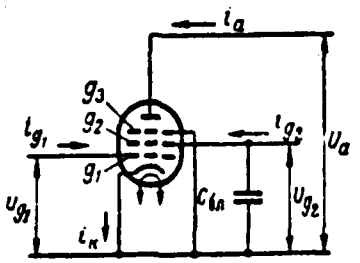

Figure III.4. Pentode.

coupling between these electrodes, while constant positive voltage $U_{g2}(U_{g2}\approx 0.5\,U_a)$ is supplied to grid g_2 to create an accelerating field between it and the cathode. Since $U_{g_1}>0$, some electrons displacing to the anode must be intercepted by the screen grid and current i_{g_2} arises in it.

Suppressor grid g_3 usually is connected to the cathode. Therefore, an accelerating field directed at grid g_3 exists in the plate--grid g_3 path, even given slight plate voltage $u_a>0$. This field constrains the onset of the dynatron effect -- secondary electrons dislodged from the plate dropping onto grid g_2 -- and returns them to the plate.

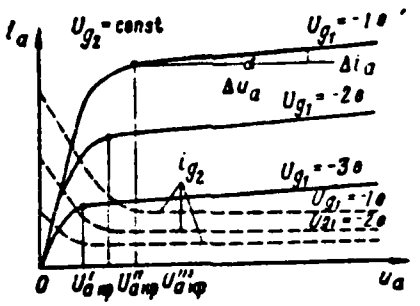

Figure III.5. Pentode Static Plate Characteristics.

The family of the pentode's static plate characteristics $i_a=\varphi(u_a)$ /89 where $U_{g2}=\text{const}$ and of various fixed values U_{g1} is depicted in Figure III.5. Ratios $i_{g_2}=\varphi(u_a)$ given identical conditions are depicted by the dotted line. Each plate characteristic has a sloping nonlinear sector in area $u_a<U_{a\,кр}$ and

an almost horizontal linear sector in area $u_a > U_{a\,kp}$, where $U_{a\,kp}$ — plate voltage critical value corresponding to the boundary between these sectors. This plate characteristic form is explained as follows. Since $U_{g2} = U_{g3} = 0$, then a strong brake field directed at grid g_3 forms in the path between grids g_3 and g_2.

This field is weakened by plate accelerating field, which penetrates partially across the grid g_3 turns. Given slight plate voltages $u_a < U_{a\,kp}$, a brake field, which delays electrons flying across grid g_2 with insufficiently-high speeds, prevails in the aforementioned path and returns them to this grid. Here, current i_{g2} increases due to the decrease in current i_a. Therefore, this pentode operating mode is referred to as the return mode. In this mode, due to the increase in voltage u_a because of the growing action of the plate's field, fewer and fewer electrons which flew to grid g_2 are returned in its field between grids g_3 and g_2, while remaining electrons drop onto the plate. Therefore, current i_a increases due to the current i_{g2} decrease. Given sufficiently-large plate voltages $u_a > U_{a\,kp}$, the brake field between grids g_3 and g_2 is compensated for by plate accelerating field to the extent that already all electrons that migrated to grid g_2 drop onto the plate. Here, current i_{g2} is created only because of the electrons en route to plate directly intercepted by grid g_2. This pentode operating mode is referred to as the intercept mode. In this mode, the number of electrons intercepted by grid g_2 is determined (for given value U_{g1}) mainly by voltage U_{g2} and virtually will not depend on voltage u_a since plate accelerating field essentially operates only beyond grid g_2 and thanks to the presence of grid g_3 in weakened form. Therefore, currents i_a and i_{g2} in area $u_a > U_{a\,kp}$ virtually will not depend on voltage u_a: $i_a \approx \text{const}$; $i_{g2} \approx \text{const}$. For the majority of pentodes, $U_{a\,kp} = 30-60$ V.

Basic pentode parameters are determined by the identical ratios (III.14--III.19) as were those for a triode. However, since the presence of a screen (as well as a suppressor) grid weakens the influence of the pentode's plate voltage on plate current magnitude, pentode internal resistance to alternating current /90 is great and usually will fall in the $R_i = 0.1-1$ MΩ range. Pentode S transconductance may reach 10 mA/V and more due to screen grid accelerating field. The increase in R_i and S values, in accordance with (III.19), will lead to an increase in pentode gain μ to several thousand unities. In addition, thanks to the screening action of grid g_2 (and g_3 as well), the pentode's transfer capacitance C_{ag1} decreases to thousandths of pF.

Pentode operation in plate characteristic horizontal sectors usually is insured since it is in these very sectors that pentode internal resistance to alternating current is constant and great: $R_i = \frac{\Delta u_a}{\Delta i_a} = \infty \operatorname{ctg} \alpha$. In addition, the very weak relationship of plate current to plate voltage in this area stipulated wide use of pentodes as current-stabilizing one-ports (see Chapter IX, § 3).

Since all currents in a pentode are created due to cathode emission current, then pentode full cathode current generally (where $u_a>0$, $u_{g2}>0$, $u_{g1}>0$) equals

$$i_k = i_a + i_{g2} + i_{g1} \; (i_{g1} \ll i_{g2}). \tag{III.20}$$

Current i_k magnitude and, consequently, that of all its components, will depend materially on control grid voltage (the relative position of the characteristics for various U_{g1} values in Figure III.5 explains this). Given $U_{g1} < E_{g1}$, the pentode is blocked at the control grid (cathode current) and all currents in it cease.*

Given fixed voltage $U_{g1} > E_{g01}$, current $i_k \approx \text{const}$, while the ratio between its components i_a and i_{g2} will depend on the suppressor grid's potential. Therefore, in several circuits, suppressor grid g_3 is disconnected from the cathode and is used as a second control grid, supplying negative signal u_{g3} to it.

The controlling influence of grid g_3 is explained in Figure III.6, /91 where relationship $i_a = \varphi(u_{g3})$ and $i_{g2} = \varphi(u_{g3})$ curves, where U_a = const for two fixed U_{g1} values, are presented.

These relationships are explained in the following manner: where $u_{g3}=0$ and $U_a > U_{a\,min}$ (intercept mode), $i_a \gg i_{g2}$. In area $u_{g3}>0$, current i_a increases slightly since its increase where $i_k = \text{const}$ is possible only due to the i_{g2} decrease, which is small. When voltage u_{g3} decreases, the braking action of the field between grids g_3 and g_2 increases, resulting in an increase in current i_{g2}, while current i_a decreases (the pentode transfers to the return mode). Given a slight sufficiently-high negative voltage $u_{g3} = E_{g03}$ value, the braking field between grids

*Only current i_{g1} and $i_k = i_a + i_{g2}$ cease when $E_{g01} < U_{g1} \leq 0$.

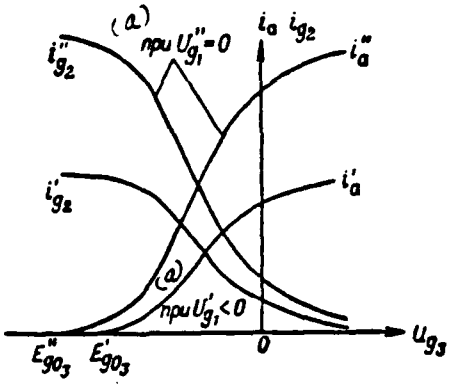

Figure III.6. Ratio of Currents I_a and I_{g2} to Voltage U_{g3} (Transitron Effect in a Pentode). (a) -- Where.

g_3 and g_2 intensifies to such an extent that not a single electron can overcome it and reach the plate. Here, current i_{g2} will become maximum $i_{a2}=i_k$, while plate current disappears. Voltage E_{go3} is referred to as pentode suppressor grid (plate current) cut-off voltage. A further reduction in voltage u_{g3} already will not lead to a change in current i_{g2} since cathode current essentially will not depend on the grid g_3 potential.

Redistribution of pentode cathode current between plate and screen grid due to the voltage change in the suppressor grid is referred to as the transitron effect. Presence of the characteristics' falling sector $i_{a2}=\varphi(u_{g3})$ makes it possible to use the transitron effect in a pentode to obtain spasmodic transitions in certain sawtooth generator circuits (see Chapter IX, § 5).

EXERCISE III.2

a) Under what conditions may screen grid current in a pentode equal zero?

b) Negative voltage u_{g3} is supplied to a suppressor grid when the latter is used as a control grid. How does that impact upon elimination of the dynatron effect?

c) Explain the relative position of the characteristics in Figure III.6 for various fixed values of U_{g1}. (Page 457)

2. Fundamental Ratios in an Electron-Tube Amplifier

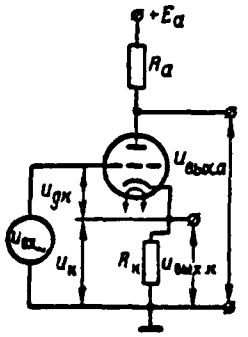

Figure III.7. Generalized Basic Circuit for a Triode Amplifier with Plate and Cathode Loads.

A generalized basic triode amplifier circuit is depicted in Figure III.7. The alternating component of input voltage $u_{вх}$ influences the control grid, eliciting a change in tube control voltage u_{gk} and current i_a. An increase in voltage $u_{вх}$ means a change in voltage u_{gk} and current i_a as well, while a decrease in voltage $u_{вх}$ means a decrease in voltage u_{gk} and current i_a. Thus, plate current always changes in phase with the stage's input voltage. Plate voltage E_a source, plate load resistance R_a, and cathode load R_k are connected to the plate current circuit. Stage output voltages u_a and u_k are picked off these resistances.*

Output voltage via plate output differs from source E_a voltage in the magnitude of the voltage drop across resistance R_a:

$$u_a = E_a - u_{R_a} = E_a - i_a R_a, \tag{III.21}$$

while this voltage's alternating component equals

$$u_{a\sim} = -i_{a\sim} R_a. \tag{III.21a}$$

Therefore, if current i_a increases, then voltage u_a decreases. On the other hand,

*Resistances R_a and R_k are tube load resistances. They should not be confused with amplifier external load resistance $R_н$ (see Figure III.1b). Therefore, in future they are designated $R_н^{\cdot}$ (see Figure III.8).

if current i_a decreases, then voltage u_a increases. Thus, stage plate voltage always changes out of phase with plate current and, consequently, with input voltage.

Output voltage via the cathode output equals the voltage drop at resistance R_k :

$$u_k = i_a R_k \tag{III.22}$$

i. e., it charges always in phase with plate current and, consequently, with input voltage.

Since the control grid is connected across the input voltage source to the low end of resistance R_k, voltage u_k turns out to be applied out of phase to the tube grid--cathode path, i. e., acts backwards on circuit input. Actually, in accordance with Kirchhoff's second law, for the input network circuit we have

$$u_{вх-} = u_{gk} + u_k \text{ or } u_{gk} = u_{вх-} - u_k \tag{III.23}$$

i. e., the tube's control voltage u_{gk} decreases by magnitude u_k. Consequently, thanks to connection of resistance R_k, the stage turns out be be enveloped by negative voltage feedback. Negative feedback action may be explained in the following manner.

A rise in voltage $u_{вх}$ will lead to a rise in voltage u_{gk}, which elicits a rise in current i_a and voltage u_k. But, the increase in cathode potential relative to the circuit chassis is equivalent to a decrease in grid potential relative to the cathode, i. e., voltage u_{gk}, and, therefore, retards an /93 increase in current i_a and voltage u_k. On the other hand, given a voltage $u_{вх}$ decrease, a voltage u_k decrease will occur, which is equivalent to an increase in voltage u_{gk} and retards the decrease in current i_a and voltage u_k. It is possible symbolically to write the action of the negative feedback, given an increase or decrease in voltage $u_{вх}$ by magnitude $=\Delta u_{вх}$, in the form

$$+\Delta u_{вх} \rightarrow \underline{\uparrow \Delta u_{gk} \rightarrow \uparrow \Delta i_a \rightarrow \uparrow \Delta u_k} \rightarrow -\Delta u_{вх} \rightarrow \underline{\downarrow \Delta u_{gk} \rightarrow \downarrow \Delta i_a \rightarrow \downarrow \Delta u_k} \tag{III.24}$$

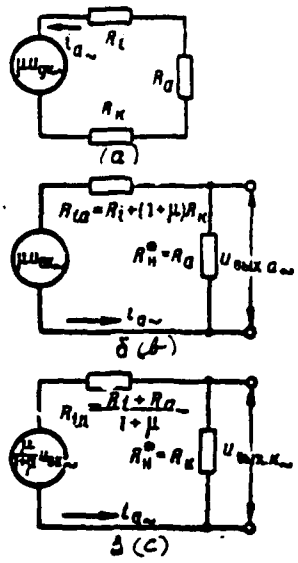

Figure III.8. Equivalent Circuits of an Amplifier with Plate and Cathode Loads.

Considering determination of static gain K (III.15), the tube on the plate circuit side may be represented in the form of emf generator $e_{\sim} = \mu u_{g\sim}$ with internal resistance to alternating current R_i (III.17). Since both load resistances R_a and $R_к$ are connected in series with resistance R_i to the plate current circuit, we will get the equivalent amplifier circuit (based on the alternating component) depicted in Figure III.8a.

In accordance with this circuit

$$i_{a\sim} = \frac{\mu u_{g\sim}}{R_i + R_a + R_к}. \qquad \text{(III.25)}$$

Substituting based on (III.23) $u_{g\sim} = u_{вх\sim} - i_{a\sim} R_к$ into this expression and solving the resultant equation for current $i_{a\sim}$, we will get

$$i_{a\sim} = \frac{\mu u_{вх\sim}}{R_i + R_a + (1+\mu) R_к} \qquad \text{(III.26)}$$

If stage output voltage is picked off plate load resistance ($u_{вых\sim} = u_{a\sim} = -i_{a\sim} R_a$), then, based on (III.26), the equivalent amplifier circuit may

be depicted in accordance with Figure III.8b, where

$$R_{i\sim} = R_i + (1+\mu)R_k \qquad \text{(III.27)}$$

--amplifier internal resistance to alternating current. Therefore, plate output stage (III.2) gain equals

$$K_a = \frac{u_{вых\sim}}{u_{вх\sim}} = \frac{u_{a\sim}}{u_{вх\sim}} = -\frac{I_{a\sim}R_a}{u_{вх\sim}} = -\frac{\mu R_a}{R_i + R_a + (1+\mu)R_k}, * \qquad \text{(III.28)}$$

while its output resistance (resistance the output terminals) /94

$$R_{вых\,a} = \frac{R_i R_a}{R_a + R_{i\sim}} = \frac{R_a[R_i + (1+\mu)R_k]}{R_a + R_i + (1+\mu)R_k} \qquad \text{(III.29)}$$

If output voltage is picked off cathode load resistance $u_{вых\sim} = u_{k\sim} = I_{\sim}R_k$, then, having divided the numerator and denominator of expression (III.26) by $1 + \mu$, we will get

$$I_{a\sim} = \frac{\frac{\mu}{1+\mu}u_{вх}}{\frac{R_i + R_a}{1+\mu} + R_k} \qquad \text{(III.30)}$$

and the amplifier's equivalent circuit may be represented in accordance with III.8c, where

$$R_{ik} = \frac{R_i + R_a}{1+\mu} \qquad \text{(III.31)}$$

— amplifier internal resistance to alternating current. Therefore, cathode output stage (III.2) gain equals

$$K_k = \frac{u_{вых\sim}}{u_{вх\sim}} = \frac{u_{k\sim}}{u_{вх\sim}} = \frac{I_{a\sim}R_k}{u_{вх\sim}} = \frac{\frac{\mu}{1+\mu}R_k}{\frac{R_i - R_a}{1+\mu} + R_k} = \frac{\mu R_k}{R_i + R_a + (1+\mu)R_k}, \qquad \text{(III.32)}$$

*The "-" sign in this expression reflects the phase opposition of grid and plate voltage changes.

while its output resistance

$$R_{\text{вых}\,k} = \frac{R_k R_{i\,k}}{R_k - R_{i\,k}} = \frac{R_k (R_i + R_a)}{R_i + R_a + (1+\mu) R_k}. \qquad \text{(III.33)}$$

Analysis of ratios (III.28), (III.29), (III.32), and (III.33) allow the following conclusions to be made:

-- in magnitude, gain K_a may be significantly greater than unity, i. e., $|K_a| \gg 1$, if $R_a \gg R_k$, $\mu \gg 1$, however always $|K_a| < \mu$;

— in principle, gain K_k may not be greater than unity $K_k < 1$ and close to unity if $R_k \gg R_a$, $\mu \gg 1$;

— inequality $R_{вых\,a} > R_{вых\,k}$ always is satisfied for output resistances; consequently, voltage from the plate output should be supplied to a high-resistance load, while that from the cathode output is supplied to a low-resistance load.

Cathode output stage properties result from negative feedback action. Actually, we will write ratio (III.23) for voltage increments in the form

$$\Delta u_{вых} = \Delta u_{вх} - \Delta u_{с} = \Delta u_{вх}\left(1 - \frac{\Delta u_k}{\Delta u_{вх}}\right) = \Delta u_{вх}(1 - K_k). \qquad \text{(III.34)}$$

Tube control voltage increment Δu_{gk} is the reason for appearance of the /95 output signal -- increment Δu_k. Increments $\Delta u_{вх}$, Δu_{gk}, Δu_k have the identical sign so increment Δu_{gk} arises only if $\Delta u_k < \Delta u_{вх}$, i. e., $K_k < 1$.

In addition, when internal load resistance R_k (see Figure III.1b) is connected to resistance $R_н$, voltage decrease u_k is compensated for by negative feedback action by a current i_a increase. Consequently, output voltage u_k will depend slightly on resistance $R_н$, which also explains the slight amount of output resistance $R_{вых\,k}$.

We will note also that any current i_a stray changes (for instance, due to source voltage E_a oscillations, tube parameter changes over time, tube replacements, and so on) are compensated for, in accordance with (III.24), due to negative feedback action. Therefore, often an amplifier has only a plate output, while resistance R_k

is connected only for stabilization of the d-c stage's operating mode.* However, presence of resistance $R_к$, in accordance with (III.28), always will lead to a decrease in gain K_a.

Analyzing tube operation in an amplifier involves use of the transconductance of its dynamic transfer characteristic $S_д$ ratios of plate current increment to tube control voltage increment Δu_{c1} it caused Δi_a, given presence of load resistances. Using expressions (III.25) and (III.19), we will get

$$S_д = \frac{\Delta i_a}{\Delta u_{c1}} = \frac{u}{R_i + R_a + R_к} = S\frac{1}{1 + \frac{R_a}{R_i} + \frac{R_к}{R_i}} < S, \qquad \text{(III.35)}$$

where S — transconductance of the static transfer characteristic (III.14).

The general expressions obtained above for gains, output resistances, and tube dynamic characteristic transconductance make it possible, as particular cases, to determine the parameters of two basic pulse amplifier types -- amplifiers with a plate load only ($R_к$=0) and amplifiers with a cathode load only (R_a = 0).

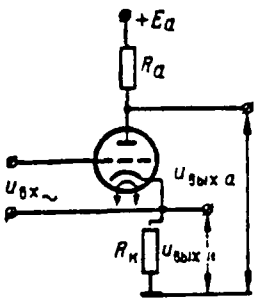

Figure III.9. Amplifier with Plate and Cathode Loads Without Feedback.

In several practical circuits, in two-stage pulse generators in particular, amplifier input voltage from plate and cathode loads is supplied, not between grid and chassis as shown in Figure III.7, but between grid and cathode according

*And also for expansion of the stage's dynamic range and decrease in pulse linear distortions (see below).

to the Figure III.9 circuit. In this case, as is easy to demonstrate, plate and cathode output gains, respectively, obtained equal /96

$$K_a = -\frac{\mu R_a}{R_i + R_a + R_k}; \qquad \text{(III.36)}$$

$$K_k = \frac{\mu R_k}{R_i + R_a + R_k}. \qquad \text{(III.37)}$$

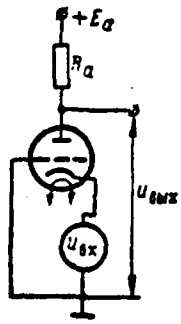

Figure III.10. Amplifier with Grounded Grid.

We will get the (III.10) circuit if the input voltage grid terminal in the Figure III.9 circuit is connected to the chassis and $R_k = \infty$ is accepted. This is referred to as grounded-grid circuit or, more precisely, a common-grid circuit, since the grid terminal is common for input and output voltages. We will encounter such a circuit when we analyze the operation of a two-stage pulse generator. Therefore, we will examine its basic properties briefly.

Since the source of voltage $u_{вх}$ in such a circuit is connected to the cathode network, tube full plate current will pass across it and its output resistance must be slight. Therefore, a cathode follower (see below) is used usually as the voltage $u_{вх}$ source. One may disregard negative voltage feedback action, given the slight source output resistance.

Voltage $u_{вх}$ changes the potential of the cathode, given fixed grid potential, which is equivalent to a change in voltage between grid and cathode. Voltage u_{gk} decreases when cathode potential increases and vice versa. Therefore, $u_{gk\sim} = -u_{вх\sim}$ and the tube may be represented by emf generator $e_i = \mu u_{gk\sim} = -\mu u_{вх\sim}$.

for consideration of the tube's controlling action. However, plate current in this circuit changes, not only due to a change in voltage in the grid, but /97 also directly due to a change in cathode potential, even if the grid had been connected briefly with the cathode. From this point of view, the plate current circuit is a voltage divider comprising series-connected resistances R_a and R_i, to which emf $e_2 = -u_{ex\sim}$ is applied. Therefore, for the plate current alternating component, we will get

$$i_{a\sim} = \frac{e_2}{R_i + R_a} = -\frac{(\mu + 1)u_{ex}}{R_i + R_a} \qquad \text{(III.38)}$$

and grounded-grid stage gain equals

$$K_{sc} = \frac{u_{vyx\sim}}{u_{ex\sim}} = -\frac{i_{a\sim}R_a}{u_{ex\sim}} = \frac{(\mu + 1)R_a}{R_i + R_a} \qquad \text{(III.39)}$$

Stage input resistance is determined as:

$$R_{ex.sc} = \frac{u_{ex\sim}}{i_{ex\sim}} = \frac{u_{ex\sim}}{i_{a\sim}} = \frac{R_i + R_a}{\mu + 1}. \qquad \text{(III.40)}$$

i. e., slightly, while output resistance is determined from formula (III.29), where R_i should be understood to mean voltage u_{ex} source internal (output) resistance.

EXERCISE III.3

a) Point out the polarity of the pulses at the outputs of the circuits depicted in Figures III.7, III.9, and III.10 when they are supplied a positive input pulse. At which inputs of these circuits and for which load resistance values may the pulse amplitude exceed that of the input pulse?

b) Prove ratios (III.36) and (III.37). (Page 457)

§ 3. PLATE-LOAD ELECTRON-TUBE AMPLIFIERS

1. Amplifier Operating Principle

Plate-load amplifiers provide the greatest voltage gain and are the most-widely distributed pulse amplifiers. Basic (simplest) circuits for such triode (a) and

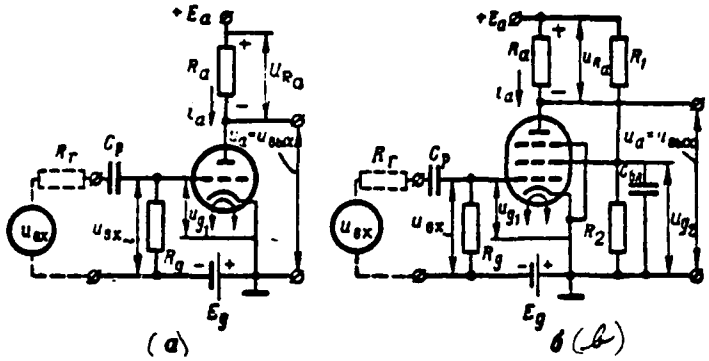

Figure III.11. Basic Plate-Load Amplifier Circuits.

pentode (b) amplifiers are depicted in Figure III.11. Load resistance R_a is connected to the tube's plate network in both circuits. Input voltage is supplied to the control grid across transfer network $C_p R_r$, which passes only the alternating component of this voltage. Negative bias voltage E_g also is applied to the grid. Therefore, the voltage between the control grid and cathode equals

$$u_{gk} = u_{g1} = u_{ax\sim} + E_g \ (E_g < 0). \qquad \text{(III.41)}$$

Bias voltage E_g determines the tube's "d-c" operating mode. Its magnitude is selected so that, given the action of voltage $u_{ax\sim}$, tube operation will occur in the linear sectors in the negative area of the plate characteristics $u_{g1} < 0$ /98 when control grid current $i_{g1} = 0$ (see Figure III.3c). Current i_{g1} is undesireable since the stage's input resistance decreases, power expended in the tube input network increases, and, in addition, it will lead to onset of additional nonlinear distortions of voltage u_{g1} (relative to voltage u_{ax})*. However, even when $u_{g1} < 0$, several electrons "settle" in the control grid, charging it negatively and constraining plate current. Resistance R_g, which is referred tc as leakage resistance ($R_g = 0.1 \div 2$ MΩ) is connected to the circuit to "drain off" these electrons.

*These distortions arise due to voltage drop in resistance R_r of the previous stage as the alternating component of current i_{g1} flows across it.

In accordance with (III.21), stage output voltage equals $u_a = E_a - i_a R_a$.

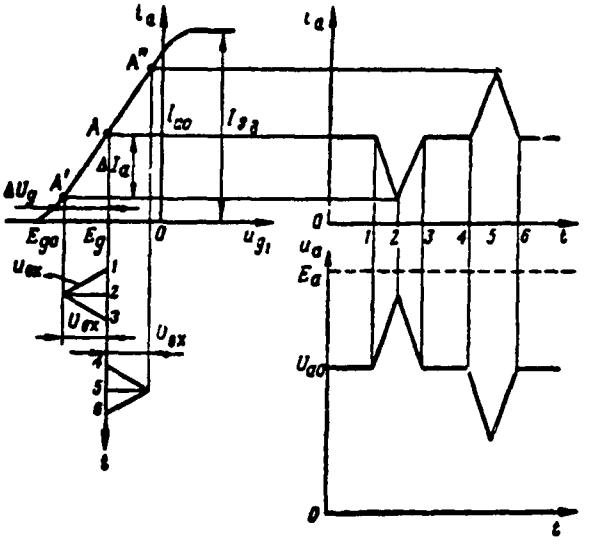

Figure III.12. For Explanation of Plate-Load Amplifier Operation.

The amplifier pentode circuit has additional elements forming the screen grid feed network: voltage divider R_1, R_2, with the aid of which voltage U_{g2} is supplied, and bypass capacitor C_{6a} across which the current i_{g2} alternating component is closed. Amplifier operation is explained in Figure III.12, where voltage $u_{g1\sim} = u_{ex\sim}$ for clarity is accepted as being in the form of bipolar triangular pulses and voltage u_{g1} coupling with current i_a is depicted by the dynamic transfer characteristic (see below). In this characteristic, E_{go} -- tube cut-off voltage, I_{s_a} — maximum possible (considering the influence of the load) plate current, referred to as dynamic saturation current.

In the initial mode where $u_{ex} = 0$, $u_{g1} = E_g = \text{const}$ and $i_a = I_{ao}$. Current /99 I_{ao} is referred to as initial, or quiescent, current, while point A in the characteristic, corresponding to the E_g and I_{ao} values, is called the operating point. Plate current $U_{ao} = E_a - I_{ao}R_a$ initial level corresponds to current I_{ao}.

A negative pulse of current i_a and a positive pulse of voltage u_a arise during

the action of a negative input pulse; the opposite occurs when the input pulse is positive. There are no pulse shape distortions at amplifier output because all operating values of voltage u_{g1} will fall within the linear sector of the characteristic A'A" and, therefore, plate current changes in proportion to input voltage changes. Operating point A was selected in the center of the characteristic's linear sector (input voltage changes symmetrically to both sides) by means of bias voltage E_g selection for this purpose, while input pulse amplitude is sufficiently small. Nonlinear distortions would result if the operating point is chosen incorrectly or if the input pulses in the stage have extraordinary amplitude.

EXERCISE III.4

a) Reproduce the curves depicted in Figure III.12, having left the dynamic transfer characteristic and bias voltage E_g unchanged and having increased input pulse amplitude by a factor of 2. What will maximum and minimum amplifier plate voltage values equal in this event?

b) How should voltage E_g change in order to insure amplification, /100
without nonlinear distortions, only of the positive or only of the negative pulses of maximum amplitude?

c) How can you obtain only the alternating component of plate voltage $u_{a\sim} = -i_{a\sim}R_a$ at the stage output? (Page 458)

2. Dynamic Characteristics

Static plate (III.11) and transfer (III.12) characteristics reflect the properties of a tube itself. However, in the dynamic mode, given presence of plate load resistance R_a, in accordance with (III.21), plate voltage itself is a function of plate current $u_a = E_a - i_a R_a$ due to the voltage drop across this resistance. Therefore, operation of a tube in an amplifier is determined by dynamic plate and transfer characteristics, which, along with tube properties, also reflect the influence of the load.

The characteristic, simultaneously considering relationships (III.11) and

(III.21) for given values E_a and R_a, is referred to as the dynamic or plate load characteristic:

$$i_a = \varphi_1(u_a) = \varphi(E_a - i_a R_a) \quad \text{where} \quad E_a = \text{const}, \; R_a = \text{const} \tag{III.42}$$

This characteristic will be plotted from the family of static plate characteristics and is the combination of the points of their intersection on the relationship (III.21) curve. It is convenient to present (III.21) in the following form to find the latter

$$i_a = \frac{E_a}{R_a} - \frac{1}{R_a} u_a \tag{III.43}$$

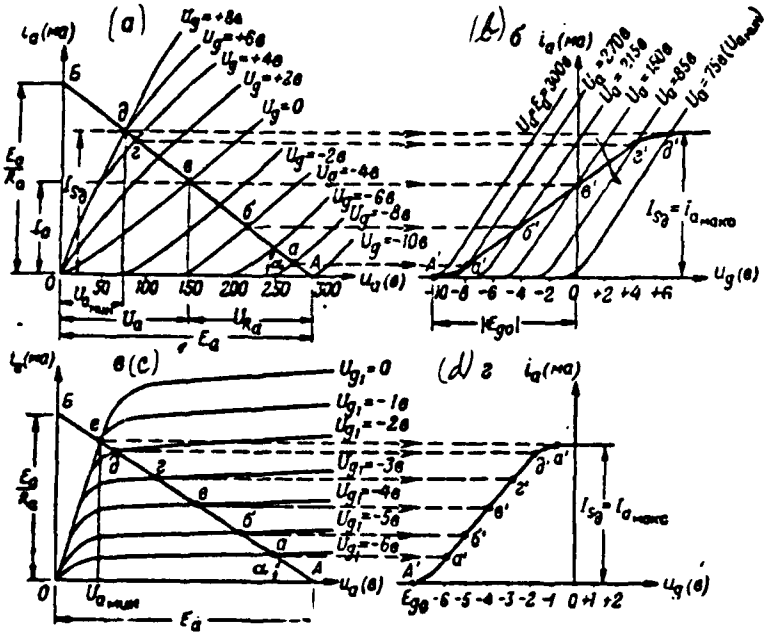

Figure III.13. Dynamic Characteristics of a Triode (a, b) and Pentode (c, d) Plate-Load Amplifier.

Ratio (III.43) is the load line equation. The plot of a triode dynamic plate characteristic is depicted in Figure III.13a. Load line AB intercepts, at the coordinate axes, portions equalling, on the basis of (III.43), $0A = E_a$

(given $i_a=0$, $u_a=E_a$, and $0\delta=\frac{E_a}{R_a}$ (where $u_a=0$, $i_a=\frac{E_a}{R_a}$)). This line's slope to the X-axis equals

$$\alpha=\operatorname{arc\,tg}\frac{0\delta}{0A}=\operatorname{arc\,tg}\frac{1}{R_a}, \qquad \text{(III.44)}$$

i. e., will depend only on the magnitude of resistance R_a.

Point A corresponds to tube cut-off. Given an increase in grid u_g voltage, current i_a increases only to value $I_{s\partial}$, at which time plate voltage is minimal $u_a=U_{a\min}$. Values $I_{s\partial}$ and $U_{a\min}$ are determined by extreme upper point ∂ of load line intersection with static plate characteristics (for even greater voltages U_g, these characteristics flow along with the load line and intersect it at the same point ∂). The tube's operating mode in which plate current is maximum and plate voltage is minimal is referred to as dynamic tube saturation /101 while current $I_{s\partial}$ is referred to as dynamic saturation current.

Dynamic saturation will occur because, given a decrease (due to an increase in current i_a) of plate voltage to value $U_{a\min}$, plate accelerating field will become so weak that a further increase in voltage U_g will lead only to redistribution of tube cathode current among electrodes: an ever-greater share of electrons is intercepted by grid (current i_g increases); plate current remains essentially constant and equals the $I_{s\partial}$ value.

Since values i_a and u_a, corresponding to portion $\delta\partial$, physically are unreal, the dynamic plate characteristic is the combination of the points lying in portion $A\partial$. This characteristic makes it possible, for given values E_a and R_a, to determine the magnitude of current i_a and voltages u_a and $u_{Ra} = i_aR_a$ for any voltage U_g. Thus, for example, in accordance with Figure III.13a, point α corresponds in the dynamic characteristic to voltage $U_g = 0$. Projecting this point to the /102 X-axis, we will get values U_a and U_{Ra} and, projecting it to the Y-axis, value I_a.

The characteristic, simultaneously considering relationships (III.12) and (III.21), is referred to as the dynamic transfer characteristic:

$$i_a=\varphi_\partial(u_g, u_a) \qquad \text{where} \quad E_a=\text{const}, R_a=\text{const} \qquad \text{(III.45)}$$

This characteristic will be plotted from the family of static transfer characteristics considering relationship (III.21). Its plot for a triode is explained in Figure III.13b. When the tube is closed ($u_g \leqslant E_g$), current $i_a = 0$ and, in accordance with (III.21), $u_a = E_a$. Therefore, the initial point of static characteristic (III.45) coincides with the initial point of the static characteristic for $u_a = E_a$ (point A'). This point also determines tube real cut-off voltage E_{g0}. An increase in voltage u_g results in onset of and increase in plate current. However, in accordance with (III.21), plate voltage simultaneously decreases. Therefore, for each large current i_a value, the point of the dynamic characteristic will fall already in another (located "to the right") static characteristic for a lower u_a value satisfying ratio (III.21) (points a'. $б'$. $в'$. $г'$). Thus, dynamic characteristic (III.45) always intersects the family of static characteristics (III.12) and, therefore, has lesser transconductance. The transconductance of the dynamic characteristic's linear sector is determined from expression (III.35) if $R_k = 0$ is placed in the latter:

$$S_д = \frac{\Delta i_a}{\Delta u_g} = \frac{S}{R_i + R_a} = S\frac{R_i}{R_i + R_a}. \qquad \text{(III.46)}$$

By virtue of the increase in voltage u_g, plate current increases only to value $Is_д$, which corresponds to the static characteristic for $u_a = U_{i\,min}$ (point $д'$). Here, the tube transfers to the dynamic saturation mode, which is reflected by the dynamic characteristic's horizontal sector. Just as was the case for the static characteristics, dynamic plate and transfer characteristics organically are coupled together. Therefore, it is simpler to plot the dynamic transfer characteristic from the dynamic plate characteristic, without using the family of static transfer characteristics. To accomplish this, it is sufficient to determine i_a and U_g values corresponding to each point A. а. б. в. г. д. е in Figure III.13a and to transfer these points to the coordinate system [i_a, u_g]. Then, we will get points A'. б'. в'. г'. д'. е' in Figure III.13b through which the dynamic transfer characteristic will pass.

A pentode's dynamic plate characteristic is depicted in Figure III.13c, while its dynamic transfer characteristic (these characteristics assume U_{g2} = const) is plotted from it in Figure III.13d using the aforementioned method. The basic difference between the dynamic characteristics of a pentode and a triode /103 are that, for the former, dynamic saturation occurs at lower (usually still given

negative) values u_{g1}. This is explained by the influence of the screen grid's field facilitating redistribution of cathode current between it and the plate at low plate v ltages.

Dynamic saturation of a tube in an amplifier arises during the action of positive pulses of extraordinarily-high amplitude. In this event, the idea of amplifier overload is brought up. A result of an overload is the onset of pulse nonlinear distortions (see Exercise III.4). On the other hand, in some circuits, special use is made of dynamic saturation, such as in limiters with upper plate current cut-off (see Chapter V, § 3).

EXERCISE III.5

a) What are dynamic plate and transfer characteristics like when $R_a = 0$?

b) Redraw the pentode dynamic characteristics from Figure III.13c, d and point out how they will change if resistance R_a is increased by a factor of 2.

(Page 459)

3. Amplifier Equivalent Circuits and Parameters

Assuming that $R_i \approx 0$ in (III.25), we will get

$$i_{a\sim} = \frac{\mu u_{g\sim}}{R_i - R_a}. \qquad \text{(III.47)}$$

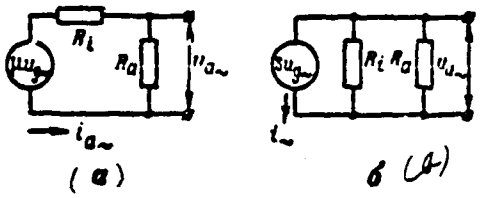

Figure III.14. Plate-Load Amplifier Equivalent Circuits.

The equivalent amplifier circuit based on the alternating component presented

in Figure III.14a, where the tube is represented in the form of emf generator μu_g with internal resistance R_i loaded across resistance R_a, corresponds to this expression.

Using ratios (III.21a), (III.47), and (III.19), for the plate voltage alternating component we will get

$$u_{a\sim} = -i_{a\sim}R_a = -\frac{\mu}{R_i}u_{g\sim}\frac{R_aR_i}{R_a+R_i} = -Su_{g\sim}\frac{R_aR_i}{R_a+R_i} \qquad \text{(III.48)}$$

Another equivalent amplifier circuit presented in Figure III.14b, where the tube is represented in the form of current generator $i_{a\sim} = Su_{g\sim}$ operating across resistances R_a and R_i connected in parallel, corresponds to this expression. The Figure III.14b circuit also may be obtained directly through conversion of the Figure III.14a circuit based on ratio (XI.17).

Assuming that $R_i = 0$ in expressions (III.28) and (III.29), for a plate-load amplifier we will get

$$K = -\frac{\mu R_a}{R_i + R_a}; \qquad \text{(III.49)}$$

$$R_{вых} = \frac{R_iR_a}{R_i + R_a}. \qquad \text{(III.50)}$$

Using expressions (III.46) and (III.50), also for gain we will get /104

$$K = -S_gR_a \quad \text{or} \quad K = -SR_{вых}. \qquad \text{(III.51)}$$

All these ratios may also be obtained directly from examination of the equivalent circuits in Figure III.14.

Relationship (III.49) is explained by curve $|K| = \varphi\left(\frac{R_a}{R_i}\right)$ in Figure III.15. It follows from this curve that gain increases with an increase in resistance R_a within the constraint (where $R_a \to \infty$) to tube static gain μ. However, an increase in resistance R_a will lead to a rise in the voltage drop across it, not only due to the alternating, but also because of the direct, component of the plate current, i. e., to a decrease in the direct component of plate voltage U_a. As a result, given too high R_a values, the tube's operating point falls in

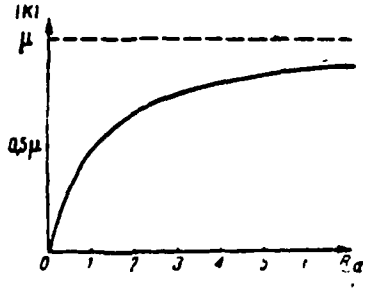

Figure III.15. For Selection of Plate Load Resistance.

the area of dynamic saturation, which brings with it a drop in amplification due to a decrease in the transconductance of the dynamic transfer characteristic (in its upper "bend") and onset of nonlinear distortions even of weak signals (see Exercise III.4). Reestablishment of the stage's normal operation in this event requires an extraordinary increase in source voltage E_a. Moreover, as will be demonstrated, resistance R_a must be decreased for a reduction in output pulse rise and decay time. Therefore, as a rule, in pulse amplifiers (especially for pentodes) the following inequality is satisfied

$$R_a \ll R_i. \tag{III.52}$$

Here, in accordance with (III.50) and (III.51) /105

$$R_{вых} \approx R_a \overset{анод}{\underset{\text{л}}{\text{g}}} |K| \approx SR_a \ll \mu^*. \tag{III.53}$$

Amplifier input resistance equals the equivalent resistance between the tube's grid and cathode

$$R_{вх} = R_{gk} = \frac{R_c r_{gk}}{R_c + r_{gk}}. \tag{III.54}$$

*Only for a triode, if the main requirement levied on the amplifier is obtaining maximum gain; $R_a = (3 \div 5) R_i$; here, $K = (0.7 \div 0.8)\mu$.

where R_g -- leakage resistance

r_{gk} -- control grid--cathode path resistance.

If the amplifier, as usual, operates without grid currents ($u_{g1}<0$), then $r_{gk} \gg R_g$ and

$$R_{вх} \approx R_g \qquad \text{(III.54a)}$$

Given the presence of control grid current ($u_{g1}>0$)

$$R_{вх} \approx r_{gk} \qquad \text{(III.54b)}$$

Amplifier input capacitance $C_{вх}$ determines the capacitive component of the input current arising due to the presence of interelectrode capacitances C_{gk} and C_{ag}. For capacitance $C_{вх}$ location, we will assume that input voltage changes by a harmonic law and we will switch to the method of complex amplitudes.

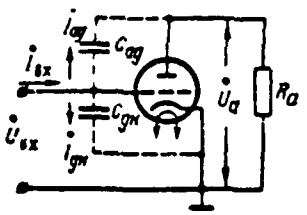

Figure III.16. For Amplifier Input Capacitance Determination.

If one disregards the influence of reactive elements in the plate network, then it is possible to represent the amplifier circuit from the alternating component considering capacitances C_{gk} and C_{ag} in accordance with Figure III.16. It follows from this circuit that the amplifier's capacitive input current equals

$$I_{вх} = I_{gk} + I_{ag}$$

Since voltage $U_{вх}$ is applied to capacitance C_{gk} and voltage $U_{вх} - U_a$ to capacitance

C_{ag}, then

$$I_{gk} = j\omega C_{gk} U_{вх};\ I_{ag} = j\omega C_{ag}(U_{вх} - U_a)$$

and the amplifier's input conductivity equals

$$Y_{вх} = \frac{I_{вх}}{U_{вх}} = j\omega\left[C_{gk} + C_{ag}\left(1 - \frac{U_a}{U_{вх}}\right)\right] = j\omega\left[C_{gk} + C_{ag}(1 - K)\right] =$$
$$= j\omega\left[C_{gk} + C_{ag}(1 + |K|)\right] = j\omega C_{вх},$$

where $K = \frac{U_a}{U_{вх}} = -\frac{U_a}{U_{вх}}$ — complex gain. Consequently, the amplifier's /106 desired input capacitance equals

$$C_{вх} = C_{gk} + C_{ag}(1 + |K|). \qquad \text{(III.55)}$$

Thus, where $K \gg 1$, value $C_{вх}$ significantly may exceed the sum of capacitances C_{gk} and C_{ag} and reach hundreds of picofarads. This is explained physically by the fact that voltage exceeding input voltage by a factor of $1 + K$ turns out to be applied to capacitance C_{ag}: $U_{вх} - U_a = U_{вх} - KU_{вх} = U_{вх}(1 + K)$. This will lead to an increase in current I_{ag}, which is equivalent to an increase in capacitance C_{ag} by a factor of $1 + K$.

Amplifier output capacitance is determined by interelectrode capacitance C_{ak}: $C_{вых} = C_{ak}$.

Actually, an amplifier's input and output capacitances also include a circuit capacitance $C_м$, which usually comprises several picofarads. Taking this capacitance into account

$$C_{вх} = C_м + C_{gk} + C_{ag}(1 + |K|);\ C_{вых} = C_м + C_{ak} \qquad \text{(III.56)}$$

Analysis of linear pulse distortions will take place with the aid of the equivalent amplifier circuit based on the alternating component depicted in Figure III.17a, analogous to the Figure III.14a equivalent circuit, but it additionally

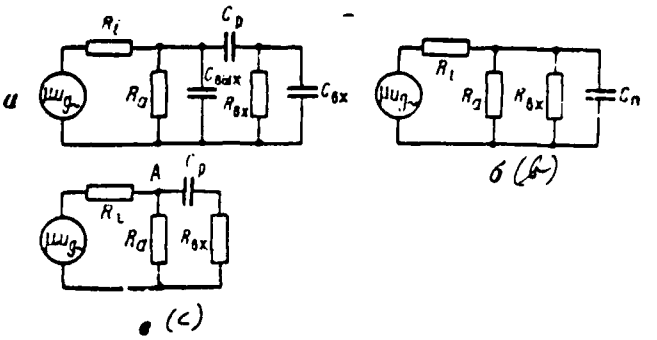

Figure III.17. For Analysis of Linear Pulse Distortions at Plate-Load Amplifier Input.

considers the influence of output capacitance $C_{вых}$ connected to the plate of isolating capacitor C_p, input capacitance $C_{вх}$ of the next stage, and its input resistance $R_{вх}$.

One may disregard the influence of capacitor C_p in the area of the pulse spectrum's high frequencies since its resistance $\frac{1}{\omega C_p}$ is close to zero. Therefore, the equivalent amplifier circuit will lead to the circuit depicted in Figure III.17b, where $C_п = C_{вх} + C_{вых}$ — total stray capacitance. It is evident from that circuit that, due to the influence of capacitance $C_п$, which shunts amplifier output, its ACHKh acquires a "roll-off" in the high-frequency area.* Pulse shape high-frequency distortions, which manifest themselves in the stretching of their porch and droop, arise due to this since the rate of output voltage change is constrained by the rate of capacitance $C_п$ charge (discharge). If $R_i \gg R_д$, $R_{вх} \gg R_д$, then one may disregard the influence of resistances R_i and $R_{вх}$ and consider that the capacitance $C_п$ charge (discharge) time constant equals $\tau_п \approx C_п R_д$, hence pulse rise (decay) time at amplifier output will equal

$$t_{ф(сд)} \approx 3 C_п R_д \qquad \text{(III.57)}$$

The advisibility of decreasing resistance $R_д$ in pulse amplifiers, in accordance with (III.52), also follows from this.

*Amplifier ACHKh form is similar to that depicted in Figure 9 (page 529).

On the other hand, one may disregard the influence of resistances $C_{вх}$ /107 and $C_{вых}$ in the low-frequency area since their resistances are high: $\frac{1}{\omega C_{вх}} \gg R_г$, $\frac{1}{\omega C_{вых}} \gg R_{вых}$. Therefore, the amplifier equivalent circuit will lead to the circuit in Figure III.17c. It follows from this that, due to the influence of isolating capacitor $C_р$, amplifier ACHKh acquires a "roll-off" in the low-frequency area. As a result, low-frequency distortions arise, which manifest themselves in the droop of the pulse. The magnitude of this droop is determined from formula (II.48a) for transient network $C_р R_{вх}$.

In the medium-frequency area, when capacitive reactance $\frac{1}{\omega C_р}$ is sufficiently slight, while capacitive reactances $\frac{1}{\omega C_{вх}}$ and $\frac{1}{\omega C_{вых}}$ are sufficiently great, one may disregard the influence of all capacitances in the Figure III.17a circuit. Also disregarding in this circuit the influence of resistance $R_{вх}$ (where $R_{вх} \gg R_а$), we will return to the Figure III.14a circuit, whence it follows that ratios (III.49) and (III.51) determine the stage's gain at medium frequencies.

EXERCISE III.6

a) Which tube, triode or pentode, should be used in an amplifier to obtain:
-- greatest gain;
-- minimum linear pulse distortions?

b) What will amplifier output voltage and gain equal if:
-- as a result of the "combustion" of resistance $R_а$, its magnitude increases to infinity ($R_а = \infty$) ;
-- resistance $R_а$ shorts out due to a short circuit in assembly ($R_а = 0$) ?

c) Multistage pulse amplifiers comprising several plate-load amplifying stages connected in series across transient R-C networks are used to obtain great pulse amplification. What will be the polarity of the pulses at the output of a three-stage amplifier if pulses of negative polarity are supplied to its input?

(Page 460)

4. Amplifier Fundamental Circuit Arrangement /108

A standard schematic diagram of a pentode plate-load amplifier is presented in Figure III.18.

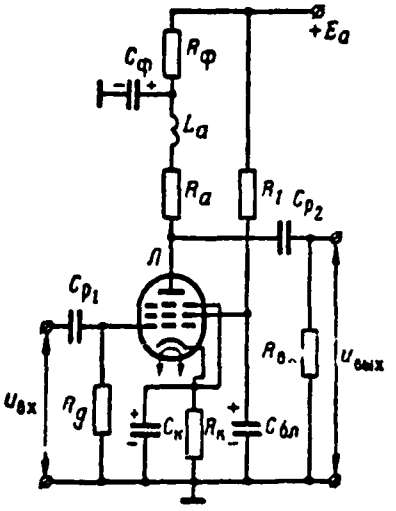

Figure III.18. Pentode Plate-Load Amplifier Schematic Diagram.

In this circuit, R_g -- leakage resistance, R_a -- plate load resistance, $R_{вх}$ -- input resistance of the next stage, C_{p1} and C_{p2} -- interstage capacitors, R_1 -- damping resistance, while $C_{бл}$ -- bypass capacitor in the screen grid's feed network, $C_к R_к$ -- self-bias cell, $C_ф R_ф$ -- plate decoupling filter, L_a -- compensating inductance.

The screen grid supply network presented here differs from the Figure III.11b circuit in that resistance R_2 is absent. Here, constant voltage across grid g_2 is determined only by source E_a voltage and the voltage drop across resistance R_1 due to passage across it of the direct component of current i_{g2}:

$$U_{g2} = E_a - I_{g2}R_1 \qquad \text{(III.58)}$$

(current i_{g2} alternating component, as usual, is closed across capacitor $C_{бл}$).

Self-bias cell $C_k R_k$ will create direct negative grid bias E_g. Bias is obtained due to the flow of the plate current's direct component (as well as of current i_{g2}) across resistance R_k and equals

$$E_g = -U_k = -(I_a + I_{g2}) R_k \qquad \text{(III.59)}$$

The alternating component of currents i_a and i_{g2} close across capacitor C_k, for which its capacitance must be sufficiently great. This is not the sole method of obtaining bias. In many circuits, it is obtained with the aid of a voltage divider fed from an external source (self-bias). Use of dynamic bias obtained across capacitor C_1 of the input transient R-C network when input pulses pass across it also is possible (see Chapter II, § 5). In this case, negative bias may be obtained only given positive input pulse polarity.

Plate decoupling filter $C_\phi R_\phi$ will smooth plate supply voltage pulsations. /109 Oscillations of this voltage will occur both due to fluctuations in the output voltage of the supply source rectifier, and due to the influence of the operation of the stage itself on the rectifier. The latter reason may lead to an undesireable mutual influence of several stages across a common plate supply source.

Decoupling the stage from the supply source will occur in the following manner. When the stage operates in the pulse mode, its plate current in the pulse may reach a significant magnitude (on the order of ampere unities), resulting in a drop in rectifier output voltage if special measures are not taken.

Resistance R_ϕ selected is much greater than the stage's internal resistance, corresponding to a "bump" of plate current $R_\phi \gg R_i$, in order to constrain the current consumed from the rectifier. Capacitor C_ϕ plays the role of an autonomous plate supply source: when the tube is blanked ($i_a = 0$), it charges across resistance R_ϕ to voltage E_a, while, during the time of a pulse, it discharges across plate load resistance R_a and the tube ($i_a = i_C$). The capacitor discharge time constant must be sufficiently great so that, during pulse time t_u, voltage in it will decrease slightly. On the other hand, during resting time t_n, the capacitor essentially must be completely recharged to initial voltage E_a.

All these requirements will be met if

$$\tau_{разр} = C_ф (R_a + R_{i.l}) \gg t_и; \quad \tau_{зар} = C_ф R_ф \leqslant \frac{t_п}{3}. \qquad (III.60)$$

Filter parameter selection also will occur on the basis of these ratios. Usually, when considering the filter, the permissable degree of plate voltage pulsation in percents is $\frac{\Delta U_a}{E_a}$ 100%, where $\Delta U_a = E_a - U_{a\,мин}$ — is the magnitude of the plate voltage reduction during the time of the pulse (resulting from capacitor $C_ф$ discharge). This makes it possible to specify the first (III.60) inequality for capacitance $C_ф$ selection.

It is evident that networks $R C_{ан}$, $R_к C_к$ and $R_ф C_ф$ are smoothing R-C low-frequency filters (see Chapter II, § 3). Therefore, their parameters unconditionally must satisfy ratio (II.40). The purpose of inductance L_a will be examined below.

EXERCISE III.7

a) What will be the consequences of the failure of capacitor $C_к$ in the self-bias cell?

b) What type bias, autonomous, self, or dynamic, may insure tube cut-off?

c) Determine the requisite capacitance of the plate filter's capacitor $C_ф$ if, given $t_и = 1$ μsec, plate voltage pulsation magnitude $\frac{\Delta U_a}{E_a}$ must not exceed 5% and the stage's internal resistance during pulse action equals $R_{i\,0} = 5$ kΩ, $R_a = 5$ kΩ. /110

d) Compute the parameters of plate filter $C_ф$ and $R_ф$, if $t_и = 1$ usec, $T = 2(3)$ usec, $E_a = 150$ V, plate current peak value in a pulse $I_a = 0.75$ A, while plate voltage pulsation magnitude $\frac{\Delta U_a}{E_a}$ must not exceed 5%.* (Page 460)

*The conditions in this problem correspond to the operating mode of a triode blocking oscillator (see Chapter VII).

5. Frequency Compensation Elements

Simple High-Frequency Parallel Compensation Circuit. An equivalent amplifier circuit in the high-frequency area was depicted in Figure III.17b. As a result of the influence of stray capacitance C_a, which shunts the amplifier output, its AChKh in this area has a "bump", which will lead to stretching of the output pulse porch and droop. Compensating inductance L_a (see Figure III.18) is connected in series with resistance R_a to the tube plate network for AChKh compensation in the high-frequency area. Given the presence of this inductance, representing the tube as a current generator in accordance with Figure III.14b and disregarding the influence of resistances R_i and $R_{вх}$ ($R_i \gg R_a$, $R_{вх} \gg R_a$), we will get the equivalent amplifier circuit depicted in Figure III.19a.

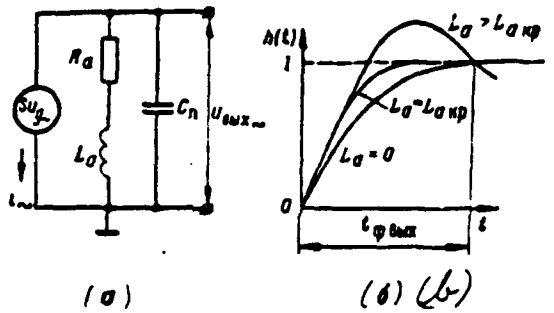

Figure III.19. For High-Frequency Compensation with Inductance $L_a (R_i \gg R_a)$.

Inductance L_a is connected in parallel with capacitance C_n. Therefore, such compensation also is referred to as parallel. The action of inductance L_a is explained simply from the frequency point of view. Capacitive reactance $\frac{1}{\omega C_n}$ decreases with an increase in frequency. But, here, inductive reactance ωL_a also increases. Consequently, given a decrease in the resistance of one parallel branch, the resistance of the other parallel branch increases. As a result, the equivalent resistance of the branches between circuit output terminal remains approximately constant.

Analysis of the transient processes in the circuit provides an analogous /111 result. Actually, given the action of current drop I, inductance L_a retards the

rise in current in its branch, i. e., it increases the current of the capacitive branch with C_a ($i = i_L + i_C$). Since capacitance C_a is charged by greater current, the rate of output voltage growth $\frac{du_{вых}}{dt} = \frac{du_C}{dt} = \frac{i_C}{C}$ increases. Here, the initial rate of pulse porch growth remains identical to that without inductance L_a since, in the first moment in any case, all current will pass across capacitance C_a. $I_C(0) = I$.

Rise time is reduced when inductance L_a increases since a greater (close to the initial) value of charging current C_a is maintained longer. However, it should be taken into account that inductance L_a, resistance R_a, and capacitance C_a form a parallel oscillatory circuit. An oscillatory process arises in this circuit given an extraordinarily-large L_a value, resulting in stray oscillations being applied to the output pulse (see Chapter II, § 6). Its aperiodic mode must be insured to avoid a shock excitation circuit. Therefore, inductance L_a usually is selected from circuit critical damping condition (II.58):

$R_{a\,кр} = 2 \sqrt{\frac{L_a}{C_a}}$, hence

$$L_{a\,кр} = 0{,}25 R_a^2 C_a. \qquad \text{(III.61)}$$

An example of pulse porch at amplifier output, given square pulse action on the input at moment t = 0 for various L_a values, is depicted in Figure III.19b.

Low-Frequency Compensation Using a Plate Filter. An amplifier equivalent circuit in the low-frequency area was depicted in Figure III.17c. As a result of the influence of interstage capacitor C_p, the amplifier AChKh has a "bump" in this area, which will lead to a reduction in pulse tilt based on the law of exponents (see Figure II.27). This reduction may be eliminated if one insures an increase, based on the same law, in plate potential (point A in Figure III.17c), i. e., of the voltage at transient network input. The idea of low-frequency compensation also concludes here in this case.

Compensation will occur with the aid of plate filter $R_ф$, $C_ф$, which is connected to the circuit just as is plate decoupling and and which does not differ externally at all from it (see Figure III.18).

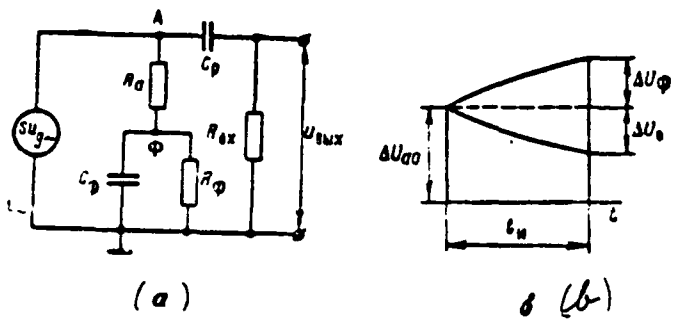

Figure III.20. For Low-Frequency Compensation with a Plate Filter.

Given presence of a filter, representing the tube as a current generator in accordance with Figure III.14b and disregarding the influence of resistance R_i ($R_i \gg R_a$), we will get the amplifier equivalent circuit depicted in Figure III.20a. We will use this circuit to explain the filter's action.

Capacitance $C_ф$ represents zero resistance for the pulse porch (current i jump at moment t = 0). Therefore, point $ф$ potential remains equal to zero, while plate potential (point A) increases with a jump to identical magnitude ΔU_{a0}, that would occur also without the filter. The charge of capacitor $C_ф$ with /112 time constant $\tau_ф = R_ф C_ф$ will occur following this. During the charging process, the potential of point $ф$, and, consequently, of point A as well, increases by the law of exponents.

We will assume that the filter is absent and we will consider that transient network output voltage diminishes as linear law ($\tau_п = R_{вх} C_р \gg t_и$). Then, at the end of the pulse, this voltage will decrease by magnitude $\Delta U_0 \approx U_{вх} \frac{t_и}{\tau_п}$, where $U_{вх}$ — pulse amplitude at transient network input (in the amplifier plate network).

Point A potential would rise by magnitude $\Delta U_{a\infty} = iR_ф = \frac{U_{вх}}{R_i} R_ф$ during the time of the full charge of capacitor $C_ф$ if the filter is present. Therefore, expression $\Delta u_a = \Delta U_{a\infty} \left(1 - e^{-\frac{t}{\tau_ф}}\right)$ describes the law of growth of this potential from initial jump ΔU_{a0}.

We will assume that condition $\tau_ф = C_ф R_ф \gg t_и$ is met, i. e., point A potential

during the time the pulse is active increases also as linear law

$$\Delta u_1 \approx \Delta U_{вых} \frac{t}{\tau_ф} = U_{вх} \frac{R_ф}{R_ф + R_ф} \frac{t}{\tau_ф} .$$

Then, at the end of the pulse, this voltage rises by magnitude

$$\Delta U_{вых} = U_{вх} \frac{R_ф}{R_ф + R_ф} \frac{t_и}{\tau_ф} = U_{вх} \frac{t_и}{C_ф R_ф} .$$

Equating values $\Delta U_{вых}$ and $\Delta U_{вых}$ (in accordance with Figure III.20b), we will get the condition for precise compensation in the form

$$\frac{t_и}{\tau_ф} = \frac{t_и}{C_ф R_ф} \qquad \text{or} \qquad C_ф R_{вх} = C_ф R_ф \tag{III.62}$$

from whence the requisite value of filter $C_ф$ capacitance is determined. The magnitude of filter resistance $R_ф$ is selected from condition $\tau_ф = C_ф R_ф \geq t_и$. However, an extraordinary increase of this resistance is undesireable since, just like an increase in resistance R_a, it will lead to a decrease in plate voltage across the tube and requires an increase in source voltage E_a. Usually, $R_ф \leq (3 \div 5) R_ф$.

§ 4. CATHODE-LOAD ELECTRON-TUBE AMPLIFIERS (CATHODE FOLLOWERS)

1. Cathode Follower Operating Principle

A cathode follower has high input resistance and slight input capacitance, slight output resistance, gain close to unity (less than unity), and follows input pulse polarity. Linear and nonlinear distortions of pulses transmitted across a cathode follower are insignificant, while the amplitude of the transmitted pulses may be coincident with supply source voltage E_a. Moreover, a cathode follower circuit is distinguished by its simplicity and stable operation. All this stipulated wide use of cathode followers in RLS pulse devices as impedance-matching stages and in many other instances when high input and low output circuit resistance are required.

A basic triode cathode follower circuit is depicted in Figure III.21. All specified cathode follower properties are explained by the action of negative

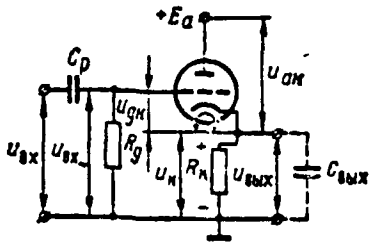

Figure III.21. Cathode Follower Basic Circuit.

voltage feedback arising thanks to connection of cathode-load resistance $R_к$ (see Chapter III, § 3). In accordance with (III.23), for a cathode follower we have

$$u_{gк} = u_{вх~} - u_к.$$

The feedback in a cathode follower acts not only by means of the alternating component, but also by means of the direct component. Actually, if $u_{вх~} = 0$, then plate quiescent current I_{a0} will pass across the tube creating constant voltage drop $U_{к0} = I_{a0}R_к$, applied with a "minus" to the control grid, across resistance $R_к$. This voltage acts as negative bias voltage

$$U_{gк0} \approx -U_{к0} = -I_{a0}R_к. \qquad \text{(III.63)}$$

In accordance with Kirchhoff's second law, we have $E_a = u_{aк} + u_{вых}$, for the input (plate) network or, considering (III.22)

$$u_{aк} = E_a - i_a R_к. \qquad \text{(III.64)}$$

In accordance with (III.23), (III.63), and (III.64), the curves of the /114 voltages in a cathode follower given the action of bipolar triangular pulses at its input are depicted in Figure III.22. The selected amplitude of these pulses is sufficiently low and the position of the operating point such that voltage $u_{gк}$ changes in the area $0 > u_{gк} > E_{g0}$, i. e., essentially, there are no nonlinear distortions.

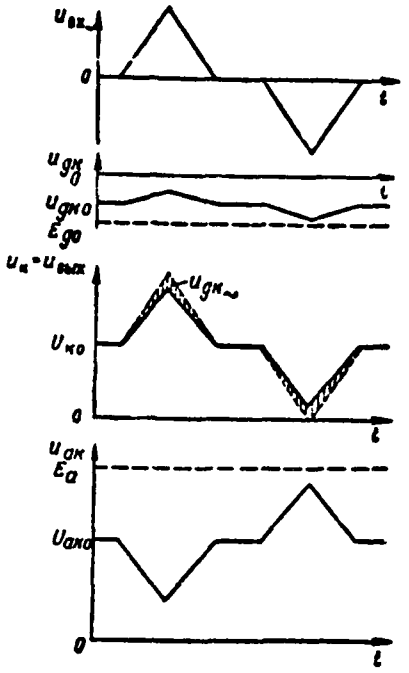

Figure III.22. Curves of Voltages in a Cathode Follower.

EXERCISE III.8

a) What polarity may voltage u have (relative to the chassis)?

b) An increase in resistance $R_к$ will lead to a rise in the magnitude of voltage $u_{вых} = -U_{к0} = -I_{к0}R_к$ when $u_{вх} = 0$. Is tube cut-off possible here?

c) How does shunting resistance $R_к$ with capacitor $C_к$ influence circuit operation? (Page 461)

2. Graphical Analysis of Cathode Follower Operation

Processes in a cathode follower may be explained clearly using a graphical approach. The influence of load impedance $R_к$ on cathode follower plate voltage $u_{ак}$ is determined by ratio (III.64), which is similar to ratio (III.21) for a /115 plate-load amplifier. Therefore, cathode follower dynamic characteristics are

plotted just as are those of a plate-load amplifier (see Chapter III, § 3) given replacement in load line equation (III.43) of resistance R_a by R_k .

Assuming in (III.35) that $R_a = 0$, for the transconductance of the cathode follower's dynamic transfer characteristic we will get

$$S_{\text{дин}} = S\frac{R_i}{R_k + R_i} \qquad \text{(III.65)}$$

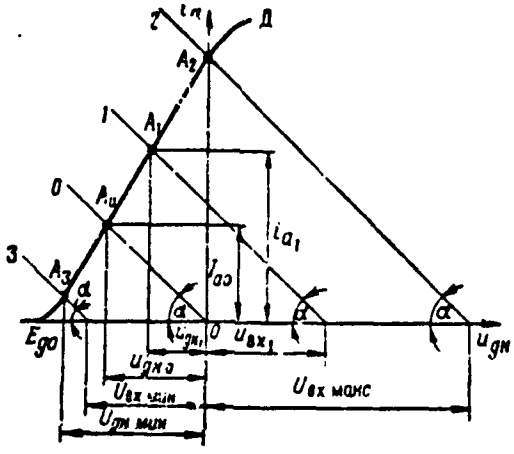

Figure III.23. Graphical Explanation of Cathode Follower Processes.

This characteristic is plotted in Figure III.23 (curve II) and reflects relationship $i_a = \varphi_2(u_{gk}, u_{ak})$. But, due to negative feedback action, voltage u_{gk} itself in a cathode follower is a function of current i_a:

$u_{gk} = u_{вх\sim} - i_a R_k$. In order to plot this function in the same diagram, we will represent it in the form

$$i_a = \frac{u_{вх\sim}}{R_k} - \frac{u_{gk}}{R_k} \qquad \text{(III.66)}$$

Ratio (III.66) for given instantaneous value $u_{вх}$ is the equation of the line referred to as the feedback line. In accordance with (III.66), the coupling line intersects on the X-axis (where $i_a = 0$) portion $u_{gk} = u_{вх\sim}$ and slopes to this axis by angle

$$\alpha = \operatorname{arc\,tg}\frac{1}{R_k}. \qquad \text{(III.67)}$$

The feedback line for another value $u_{вх}$ displaces accordingly along the /116 horizontal, and the angle of slope remains fixed. The family of feedback lines for various voltage $u_{вх}$ values, which is accepted as the parameter, given magnitude $R_к = \text{const}$, is depicted in Figure III.23 by lines 0, 1, 2, 3. The point at which the dynamic characteristic intersects the feedback line for a given value $u_{вх}$ determines voltage u_{gA} and current i_a in the circuit (points A_0, A_1, A_2, A_3). So, for $u_{вх}=u_{вх1}$, feedback line 1 intersects the dynamic characteristic at point A_1 with coordinates u_{gA1}, i_{a1}. Other points of the lines physically have no concept.

Operating point A_c lying on the feedback line for $u_{вх}=0$ (line 0) determines stage d-c operating mode. This is referred to as the bias line. Initial bias U_{c0} and quiescent current I_{a0} determine operating point position. The feedback line displaces to the right for positive $u_{вх}$ values and to the left for negative values relative to bias line 0. Line 2 is plotted for value $u_{вх}=U_{вх.макс}$, where point A_2 ($u_{gA}=0$) reflects circuit state. Further increase in voltage $u_{вх}$ will shift the reflected point to area $u_{gA}>0$, i. e., will lead to appearance of current i_g and resulting decrease in state input resistance, as well as to onset of nonlinear distortions due to a dynamic characteristic upper bend.

Line 3 is plotted for value $u_{вх}=U_{вх.мин}$, where point A_3 ($u_{gA}=U_{gA.мин}$) reflects circuit state. Further decrease in voltage $u_{вх}$ will lead to onset of nonlinear distortions due to a dynamic characteristic lower bend, while, where $u_{вх}<E_{g0}$, to tube blanking. Therefore, value $U_{вх.макс}$ constrains positive pulse maximum amplitude, while value $U_{вх.мин}$ constrains negative pulse maximum amplitude at stage output. Comparing in Figure III.23 the magnitude of values $U_{вх.макс}$ and $U_{вх.мин}$, we see that this circuit is more amenable to positive pulse transfer.

The graphical construction presented makes it possible to use given resistance $R_к$ magnitude to determine stage operating point and dynamic range (values $U_{вх.макс}$ and $U_{вх.мин}$) or, vice versa, to select resistance $R_к$ magnitude for the desired operating point position. However, one must consider that a change in $R_к$ magnitude means a change not only in feedback line slope, but, in accordance with (III.65), a change in dynamic characteristic transconductance as well.

EXERCISE III.9

a) How and how much does the dynamic range (maximum input voltage change)

differ for stages with only a plate and with only a cathode load, given the identical degree of nonlinear distortions? For which stage will nonlinear distortions be less, given identical voltage ... change constraints?

b) Complile plots that are analogous to those in Figure III.23, but /117 for a higher resistance ... magnitude. How will an increase in resistance R_k impact upon stage operation? What constrains the maximum amplitude of this resistance?

(Page 461)

3. Cathode Follower Parameters

Assuming in (III.32) and (III.33) that $R_a = 0$, for cathode follower gain and output resistance we will get

$$K_{u0} = \frac{\mu R_k}{R_i + (1+\mu) R_k}, \qquad \text{(III.68)}$$

$$R_{вых.\,0} = \frac{R_i R_k}{R_i + (1+\mu) R_k} \qquad \text{(III.69)}$$

Since $\mu \gg 1$, for triodes and especially for pentodes, considering (III.19), these formulas may be written in approximate form

$$K_{u0} \approx \frac{\mu R_k}{R_i + \mu R_k} = \frac{1}{1 - \frac{1}{SR_k}}; \quad R_{вых.\,0} \approx \frac{R_i R_k}{R_i + \mu R_k} = \frac{1}{S} \frac{1}{1 - \frac{1}{SR_k}} \qquad \text{(III.70)}$$

Given $SR_k \gg 1$, we will get even simpler expressions

$$K_{u0} \approx 1; \quad R_{вых.\,0} \approx \frac{1}{S} \qquad \text{(III.71)}$$

It follows from the resultant ratios that cathode follower gain $K_{u0} < 1$ also is closer to unity (more precisely to value $\frac{\mu}{1+\mu}$), the greater tube transconductance S and resistance R_k. However, resistance R_k increase will lead to quiescent current I_{a0} decrease and bring stage operating point close to a dynamic transfer characteristic lower bend (see Exercise III.9). Therefore, depending on stage operating conditions, resistance R on the order of several hundred ohms, unities, or even tens of kilohms is selected. Here, for example, even given a relatively-low

transconductance value S ≈ 3 Ma/V (6N1P, 6N5P, 6H7C) triodes) and low resistance [illegible] KΩ, in accordance with (III.70), we will get [illegible].

Cathode follower output resistance [illegible] and, given an increase in transconductance S and resistance [illegible], also approaches ratio [illegible] (more precisely, magnitude [illegible]). Since, for most tubes, transconductance S equals several mA/V, output resistance comprises only several hundred ohms.

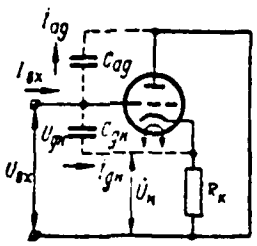

Figure III.24. For Determination of Follower Input Capacitance.

Cathode follower input resistance, given absence of grid currents, /118 in accordance with (III.54) equals $R_{вх} \approx R_к$. We will use the method of complex amplitudes to find the cathode follower's input capacitance and we will turn to its circuit for alternating components presented in Figure III.24. In accordance with this circuit, input capacitive current $I_{вх}$ is stipulated by the presence of interelectrode capacitances $C_{gк}$ and C_{ag} and equals

$$I_{вх} = I_{gк} + I_{ag}$$

Since voltage $U_{gк} = U_{вх} - U_к$ is applied to capacitance $C_{gк}$ and voltage $U_{вх}$ to capacitance C_{ag}, then

$$I_{gк} = j\omega C_{gк}(U_{вх} - U_к); \quad I_{ag} = j\omega C_{ag} U_{вх}$$

and stage input conductance equals

$$Y_{ex} = \frac{I_{ex}}{U_{ex}} = j\omega\left[C_{gk}\left(1 - \frac{U_k}{U_{ex}}\right) + C_{ag}\right] =$$
$$= j\omega\left[C_{gk}(1 - K_{cn}) + C_{ag}\right] = j\omega C_{ex},$$

then input capacitance equals

$$C_{ex.cn} = C_{gk}(1 - K_{cn}) - C_{ag} \approx C_{ag} \qquad \text{(III.72)}$$

since $|1 - K_{cn}| \ll 1$. Comparing the resultant expression with (III.55) we see that cathode follower input capacitance is less by a factor of tens than that for a plate-load amplifier due to negative feedback action.

High-frequency pulse distortions stipulated by the influence of circuit input and output capacitances are unavoidable at cathode follower output, just as was the case for a plate-load amplifier. Since follower capacitance C_{ag} is slight, capacitance $C_{вых}$ shown by the dotted line in Figure III.21 is of main significance. This capacitance equals $C_{вых} = C_{ak} + C_{kн} + C_м + C_н$, where C_{ak} -- tube plate--cathode capacitance*, $C_{kн}$ -- capacitance between cathode and filament, $C_м$ -- circuit /119 capacitance, and $C_н$ -- load capacitance.

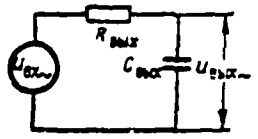

Figure III.25. For Calculation of Follower Output Capacitance Influence.

Accepting on the basis of (III.71) that $K_{cn} \approx 1$, $R_{вых.cn} = \frac{1}{S}$, we will assume the cathode follower's equivalent circuit for high frequencies in accordance with Figure III.25. It is evident from that figure that the time constant for the

*Capacitance C_{ak} for the alternating component is connected in parallel across resistance R_i (and, therefore, is included in $C_{вых}$ as a component) since the tube plate for the alternating component is connected to "ground" across a capacitor bypassing the supply source.

follower output network equals

$$\tau_{вых} = C_{вых} R_{вых.эп} \qquad \text{(III.73)}$$

and is slight due to the insignificance of resistance $R_{вых.эп}$. Therefore, steep pulse porches are transmitted with insignificant distortions across the cathode follower. Thus, when $C_{вых}$=40 pF, $R_{вых.эп}$=250 ohms, we will get $\tau_{вых}$=0,01 usec, while pulse rise (decay) time at output will comprise $t_{ф(сп)} \approx 3\tau_{вых}$=0,03usec. However, that will be the case only given sufficiently-low pulse amplitude. It is possible that grid current may appear or the tube cut off and, as a result, there may be additional stretching of the porches if there are great amplitudes and steep pulse porches caused by capacitance $C_{вых}$, which retards a change in cathode potential. This is explained by the curves in Figure III.26 using transmission of a positve square pulse as the example.

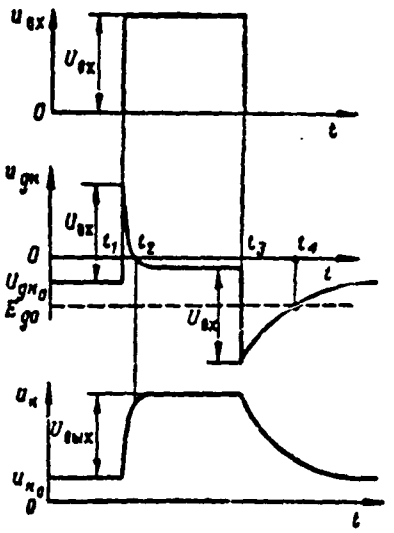

Figure III.26. Transmission of a Pulse of Great Amplitude.

We will examine these curves, having ratio $u_{gк} = u_{вх} - u_к$ in mind. At moment t_1, cathode potential does not change ($u_к = U_{к0}$) and the pulse porch turns out to be applied wholly to the grid--cathode sector due to the presence of capacitance $C_{вых}$. Therefore, voltage $u_к$ with a jump increases by magnitude $U_{вх}$. If $u_{gк} >$, then grid voltage will become positive and grid current i_g appears.

Further, because of capacitance $C_{вых}$ charge, voltage $u_к$ increases while voltage $u_{вых}$ drops according to the same law. Until moment t_2, until $u_{вых} \geq 0$, the /120 charge of capacitance $C_{вых}$ will occur with currents i_a and i_g, while, later, only by current i_a. Here, during interval $t_2 - t_1$, porch steepness decreases for two reasons: first, due to the increase of resistance $R_{вых.кр}$ and, second, due to the decrease in pulse amplitude affecting the grid stipulated by the voltage drop across the pulse source input resistance (of the previous stage) as current i_g flows across it. Then milking of capacitance $C_{вых}$ will occur with time constant $\tau_{вых}$.

At moment t_3, cathode potential does not change ($u_к = U_{к.макс} = U_а - U_{см.з}$) and, therefore, voltage $u_{вых}$ with a jump drops by the magnitude of pulse droop $U_{вх}$. If $U_{а.мин} = -U_{к.макс} < E_а$ here, then the tube is cut off. But, given a blanked tube, the feedback circuit turns out to be disrupted. Therefore, in interval $t_4 - t_3$, until $u_{вых} \leq E_а$, capacitance $C_{вых}$ discharge will occur across resistance $R_к$ with time constant $\tau_{разр} = C_{вых} R_к \gg \tau_{вых} (R_к \gg R_{вых.кр})$. Then milking of capacitance $C_{вых}$ will occur with time constant $\tau_{вых}$. Thus, the output pulse's droop is stretched to a significantly-greater degree than its porch is.

We will note in conclusion that use of a pentode rather than a triode in a cathode follower, due to the large value of transconductance S at the identical $R_к$ value, provides great gain and less output resistance, while, due to lesser capacitance $C_{вх}$, it is possible to improve the shape of the output pulses.

EXERCISE III.10

a) Draw a cathode follower equivalent circuit in which the tube is represented in the form of a current generator.

b) In accordance with Figure III.26, at moment t_4, a decrease will occur in the time constant of capacitance $C_{вых}$ discharge in connection with unblanking of the tube. Why is there no break at that moment in the $u_{вых}$ and $u_к$ curves?

(Page 462)

4. Cathode Follower Circuit Variants

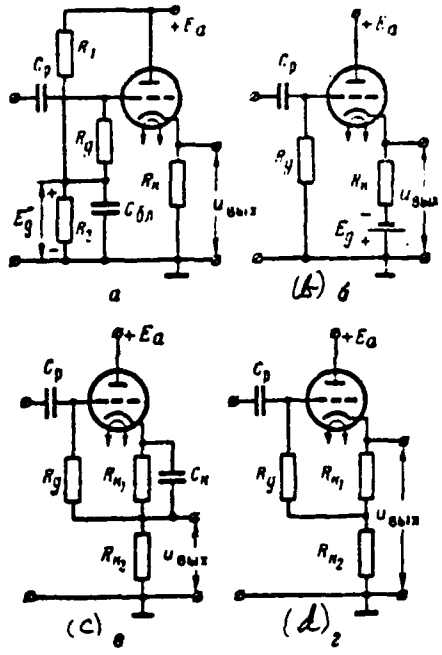

Figure III.27. Cathode Follower Circuit Variants.

Several practical cathode follower circuit variants are depicted in Figure III.27. These circuits differ from the basic circuit (III.21) by the presence of and the methods of supplying additional bias voltage, which make it possible to change the position of the stage's operating point. In the Figure III.27a circuit, positive bias voltage E_g from resistance R_2 of divider R_1, R_2 is supplied to grid. Capacitor $C_{k.}$ bypasses resistance R_2 by means of the alternating component. Bias voltage $E_g>0$ shifts the operating point based on the dynamic transfer characteristic "upwards," which makes it possible to increase the maximum amplitude of positive-polarity input pulses without decreasing resistance $R_{.}$, i. e., stage gain.

Negative bias voltage is introduced into the cathode network in Figure III.27b, which is equivalent to supplying positive bias to grid. Therefore, this circuit operates just like the previous one. However, voltage $E_g<0$ decreases the output voltage direct component, which will become equal to $U_{вых.т} = U_{вых} - E_g = I_{a0}R_k - E_g$.

Self-bias network $R_{k1}C_k$ is used in the Figure III.27c circuit. Negative grid bias is obtained due to the voltage drop only across resistance R_{k1} equalling

$$U_{g0} = -U_{k1} = -I_{a0}R_{k1}$$

The voltage drop due to passage of the plate current's direct component across resistance R_{k1} does not impact upon the position of the operating point thanks to capacitor C_p isolating the grid from the chassis ("ground") where the direct component is concerned. When input voltage is active, the output voltage alternating component, stipulating negative feedback action and gain magnitude, arises only across resistance R_{k2}. Usually, $R_{k2} > R_{k1}$. Here, the position of the operating point is determined by resistance R_{k1} and can be selected in the middle of the dynamic characteristic linear sector, while stage gain and dynamic range are determined only by resistance R_{k2} and can be made sufficiently large. The Figure III.27d circuit operates analogously. Here, the position of the operating point is provided also by resistance R_k but, since it is not isolated by a capacitor, the alternating component of feedback voltage (and of output voltage), given the action of the input signal, is picked off from the sum of resistances $R_{k1}+R_{k2}$.

EXERCISE III.11

Explain graphically how to determine the position of the operating point and dynamic range for the circuits presented in Figure III.27. Write the expressions for the gain of these circuits. (Page 463)

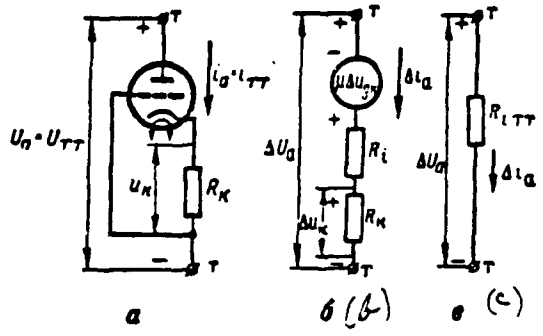

Figure III.28. Cathode-Load Stage as a Current-Stabilizing One-Port.

A cathode-load stage assembled like a cathode follower circuit often is /122 used to stabilize current i_a passing across it. Here, it should be looked upon as a current-stabilizing "TT" one-port, whose circuitry is depicted in Figure III.28a. In this instance, the stage, in essence, is not a cathode follower (the input voltage in it is not supplied, while the output voltage is not picked off), but given voltage u_a changes, current i_a stabilization is insured due to negative feedback action identical to that in a cathode follower (III.24). Actually, if, for example, voltage u_a is decreased, then current i_a must also decrease but here, voltage u_k drops and, consequently, grid voltage $u_{gk}=-u_k$ increases. But, this constrains a decrease in current i_a.

We will represent the tube in the form of emf generator μu_{gk} with internal resistance R_i for quantitative evaluation of the stage's current-stabilizing action. Then we will get the equivalent circuit of a one-port for the increments of current and voltages depicted in Figure III.28b. In accordance with this circuit, considering that, given $u_{a1}=0$, $\Delta u_{gk}=-\Delta u_k=-\Delta i_a R_k$, we will get

$$\Delta i_a=\frac{\Delta u_a-\mu\Delta u_{gk}}{R_i+R_k}=\frac{\Delta u_a+\mu\Delta i_a R_k}{R_i+R_k} \quad \text{или} \quad \Delta i_a=\frac{\Delta u_a}{R_i+(1+\mu)R_k}.$$

The latter expression makes it possible to represent the one-port by the Figure III.28c equivalent circuit, where

$$R_{i\sim}=\frac{\Delta u_a}{\Delta i_a}=R_i+(1+\mu)R_k \tag{III.74}$$

-- one-port internal resistance to alternating current.

Thus, negative feedback increases stage internal resistance to alternating /123 current by magnitude μR_k . This explains the stage's current-stabilizing action.

§ 5. PHASE INVERTER. DIFFERENCE CIRCUIT

If load impendances equal to each other $R_{a1}=R_{a2}=R_a$ are placed in an amplifier with plate and cathode loads (Figure III.7), then, based on (III.28) and (III.32), we will get

$$K_{u1}=K_{u2}=\frac{\mu R_a}{R_i+(1+\mu)R_k}<1 \tag{III.75}$$

-- stage gains at plate and cathode outputs are identical in magnitude and less than unity. Since, in this instance, stage output voltages u_a and u_k are equal in magnitude but opposite in phase, such an amplifier is referred to as a phase inverter.

When a pulse of given polarity is supplied to phase inverter input, a pulse of different polarity, but of identical amplitude, will appear at its outputs: $U_{вых\,a} = U_{вых\,k}$. Assuming in (III.75) that $\mu \gg 1$, we will get

$|K_a| = K_k = \frac{1}{1 + \frac{1}{SR_н}}$, from whence it follows that, given $SR_н \gg 1$

$$|K_a| = K_k \approx 1 \qquad \text{(III.75a)}$$

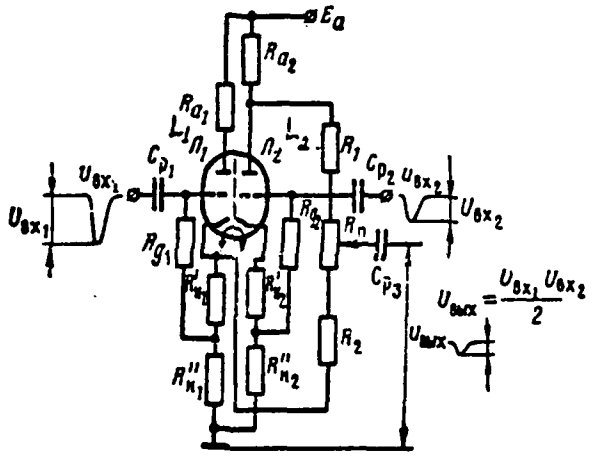

Figure III.29. Difference Circuit.

We will examine one characteristic use of phase inverters using the difference circuit depicted in simplified form in Figure III.29. This circuit makes it possible to obtain voltage proportional to the half-difference of two input voltages:

$$U_{вых} = K \frac{U_{вх1} - U_{вх2}}{2}, \qquad \text{(III.76)}$$

and is used widely as a comparator in automatic tracking system discriminators (see Chapter I, § 2).

The circuit will comprise two identical triode phase inverters L_1 and L_2 with equal plate and cathode loads:

$$R_{a1} = R_{a2} = R_{a1} = R_{a2};\quad R'_{k1} = R'_{k2};\quad R''_{k1} = R''_{k2} \qquad \text{(III.76a)}$$

The first stage has a plate and the second a cathode output, while voltage divider $R_1 R_a R_2$ is connected between these outputs. Input pulse voltages -- both of negative polarity with amplitudes $U_{вх1}$ and $U_{вх2}$, are supplied to the triode grids across coupling capacitors C_{p1} and C_{p2}. Output pulse voltage with amplitude $U_{вых}$ is picked off the contact arm of potentiometer R_a across coupling capacitor C_{p3}. The contact arm is set beforehand in a position whereby, given voltage equality $u_{вх1} = u_{вх2}$ independent of their magnitude, there would be no /124 output signal $u_{вых} = 0$. Possible differences in stage parameters are compensated for in this manner, i. e., balancing of the circuit will occur. Leakage resistances R_{g1} and R_{g2} are connected only to a portion of stage loads R'_{k1} and R'_{k2} in order to decrease the magnitude of triode initial negative grid bias. This insures amplification of negative input pulses in the linear sectors of the triodes' dynamic transfer characteristics (see Figure III.27d and Exercise III.11).

EXERCISE III.12

Compile an equivalent circuit for a difference circuit, representing both stages in the form of emf generators $e_1 = u_{вых1}$ and $e_2 = u_{вых2}$. Using this circuit, prove ratio (III.76). (Page 464)

§ 6. TRANSISTOR AMPLIFIERS

1. Transistor Amplifier General Characteristics

At the present time, amplifiers assembled on transistors are used widely for amplification of pulse signals and harmonic oscillations. Transistors replace electron tubes in these amplifiers. However, no complete analogy exists between electron-tube circuits and transistor circuits since the latter have several special features.

Thus, for example, input current in the entire range of frequencies exists

in a transistor. Input current in electron tubes is stipulated by the presence of interelectrode capacitances and appears only at relatively-high frequencies. /125 Presence of input current in transistors will lead to losses in input signal power. Moreover, the magnitude of triode amplifier input resistance has a lower value than that in tube amplifiers. This requires that special measures be taken for amplifier stage agreement.

Couplings exist in transistors between input and output in the entire range of frequencies, while, in tubes, stray feedback across plate--grid capacitance begins to mainfest itself only at relatively-high frequencies. Consequently, if we replaced a tube with a one-port in the video frequency area, then a transistor during analysis will have to be replaced by a two-port.

The dependency of transistor characteristics and parameters on temperature is an important transistor distinguishing feature. The determinant turns out to be collector junction temperature, which, in low-power transistors, essentially will depend on environmental temperature and, in powerful transistors operating in terminal stages, will depend on power dissipated in the junction as well as on heat abstraction conditions in it. At present, industrially-produced germanium transistors can operate in a temperature range of -60 to +100° C, while silicon transistors operate in the -60 to +200° C range.

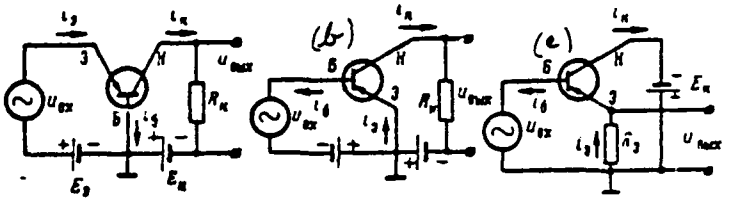

Figure III.30. Transistor Connection in an Amplifier Circuit: (a) -- Common-base circuit; (b) -- Common-emitter circuit; (c) -- Common-collector circuit.

A transistor may be connected to an amplifier circuit in three different ways, depending on which electrode is common for the input and output network. Thus, there are three types of circuits (Figure III.30):

-- common-base (OB) circuit;

-- common-emitter (OE) circuit;

— common-collector (OK) circuit.

In a common-base circuit, emitter current is input current, while collector current is output current. Current gain in a common-base transistor circuit is determined as

$$\alpha = \frac{\Delta I_к}{\Delta I_э}\Big|_{U_б = \text{const}} \qquad \text{(III.77)}$$

and always is less than unity.

The magnitude of current gain α, determined as the ratio of the increments /126 of collector current and emitter current, essentially does not differ from the magnitude determined by the ratio of the direct components of currents, i. e.,

$$\alpha = \frac{I_к}{I_э}\Big|_{U_б = \text{const}} \qquad \text{(III.78)}$$

A magnitude of voltage gain in a common-base circuit significantly greater than unity may be obtained. In actuality, a change in emitter current will occur under the influence of alternating voltage $u_{вх}$

$$\Delta I_э = \frac{\Delta U_{вх}}{R_{вх}},$$

where $R_{вх}$ — input resistance of the circuit for alternating current. This resistance is slight since forward bias voltage $E_э$ is applied to the emitter junction.

A change in emitter current will lead to a change in collector current, resulting in a change occurring in voltage across resistance $R_н$

$$\Delta U_{вых} = \Delta I_к R_н.$$

Voltage gain may be determined as

$$K_u = \frac{\Delta U_{вых}}{\Delta U_{вх}} = \frac{\Delta I_к R_н}{\Delta I_э R_{вх}} = \alpha \frac{R_н}{R_{вх}}. \qquad \text{(III.79)}$$

It is possible to obtain magnitude $R_к \gg R_{вх}$, considering that $\alpha \approx 1$, if ratio $K_u \gg 1$ is provided.

It is not difficult to demonstrate that power gain also will occur in an OB circuit. Power gain K_p can be computed approximately using formula

$$K_p = \frac{P_{вых}}{P_{вх}} = \frac{\Delta I_к \Delta U'_{вых}}{\Delta I_э \Delta U_{вх}} \approx \alpha^2 \frac{R_к}{R_{вх}}. \qquad \text{(III.80)}$$

Thus, stage voltage and power gain in a transistor approximately equal the ratio of load resistance to input network resistance. It is for this very reason that semiconductor triodes got the name transistor, i. e., transformers of resistance.*

Base current $I_б$ is input current and collector current $I_к$ is output current when a transistor is connected as a common-emitter circuit. Hence, current gain for this circuit may be determined as

$$\beta = \frac{\Delta I_к}{\Delta I_б}\Big|_{U_к = \text{const}}. \qquad \text{(III.81)}$$

Considering that $\Delta I_б = (\Delta I_э - \Delta I_к) \ll \Delta I_э$, magnitude $\beta \gg 1$. /127

It is easy to establish the coupling between current gains in a common-base and in a common-emitter circuit.

Actually:

$$\beta = \frac{\Delta I_к}{\Delta I_б}\Big|_{U_к = \text{const}}, \quad \alpha = \frac{\Delta I_к}{\Delta I_э}\Big|_{U_к = \text{const}},$$

while $\Delta I_б = \Delta I_э - \Delta I_к$, hence

$$\beta = \frac{\Delta I_к}{\Delta I_э - \Delta I_к} = \frac{\frac{\Delta I_к}{\Delta I_э}}{1 - \frac{\Delta I_к}{\Delta I_э}} = \frac{\alpha}{1 - \alpha}. \qquad \text{(III.82)}$$

*The word "transistor" stems from the English words "transformer of resistance."

Base current is the input current and emitter current is the output current in a common-collector transistor circuit. Hence, current gain

$$\beta_к = \frac{\Delta I_э}{\Delta I_б}\Big|_{U_к = \text{const}}$$

Considering that current ratio $\Delta I_э = \Delta I_б + \Delta I_к$ is fixed for any type of transistor connection, we get

$$\beta_к = \frac{\Delta I_э}{\Delta I_б} = \frac{\Delta I_к + \Delta I_б}{\Delta I_б} = \beta + 1 \qquad \text{(III.83)}$$

2. Equivalent Transistor Circuits

Three basic methods are used at the present time to study transistor amplifiers: the linear two-port, the physical equivalent circuit method, and the graphical method. The latter two found greatest use in engineering practice.

The equivalent circuit method is used most often for computation of amplifiers operating a small signal, i. e., when the structure and parameters of the equivalent circuit remain fixed and are independent of signal level. Here, an equivalent circuit is an electrical model in which physical processes occurring in a transistor are reflected.

The graphical method is founded on use of transistor input and output static characteristics. The beauty of this method is its clarity and the ability to use it for a small and for a large signal. However, use of static characteristics is restricted to the d-c mode and the low-frequency area. Therefore, the graphical method is used in practice mainly for selection of operating point and analysis of key transistor properties. Such amplifier indicators as current gain K_i, voltage gain K_u, input resistance $R_{вх}$, and output resistance $R_{вых}$ are considered using equivalent circuits.

One of the clearest equivalent circuits obtained on the basis of physical representations of transistor operation is a T-circuit (Figure III.31). The parameters of this circuit are transistor internal resistances. A current or voltage generator connected to the input network reflects transistor amplification properties.

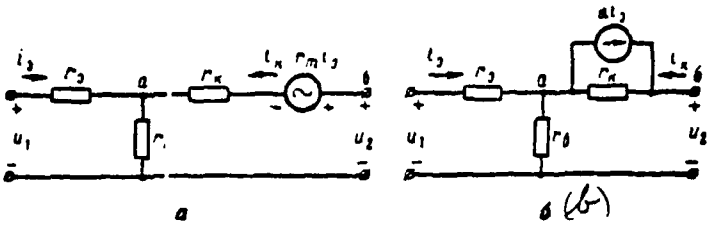

Figure III.31. Equivalent Circuit for a Transistor in a Common-Base Circuit: (a) — With equivalent voltage generator; (b) -- With a current generator.

Two T-shaped equivalent circuit variants for a common-base transistor circuit are presented in Figure III.31: with voltage generator $r_m i_э$ (Figure III.31a) and with current generator $\alpha i_э$ (Figure III.31b). This circuit's parameters are:

$r_э$ -- forward-bias emitter junction resistance;

$r_к$ — reversed-bias collector junction resistance;

$r_б$ — base layer resistance;

r_m — equivalent generator resistance;

α — current gain for a common-base circuit.

Magnitudes of internal resistances in modern transistors will fall in the ranges:

$r_э$ -- several dozen ohms;

$r_к$ — from several hundred kilohms to unities of megohms;

$r_б$ — several hundred ohms.

Magnitude α is determined by transistor materials and production technology. In industrially-produced transistors, $\alpha \approx 0.95 \div 0.995$.

Equivalent generator resistance r_m sometimes is eliminated from a circuit, replacing resistance $ar_к$ equal to it. Actually, equating the voltages of corresponding sectors ab in Figure III.31a and III.31b equivalent circuits, we get

$$i_к r_к - r_э i_э = (i_к - \alpha i_э) r_к,$$

hence

$$r_m = \alpha r_к.$$

In the circuit examined, transistor amplification properties are considered /129 by introduction of equivalent generator , analogous to generator in the tube equivalent circuit.

The polarity of this generator's voltage considers the circumstance that collector current must coincide in phase with emitter current (current direction is indicated in Figure III.31 by arrows).

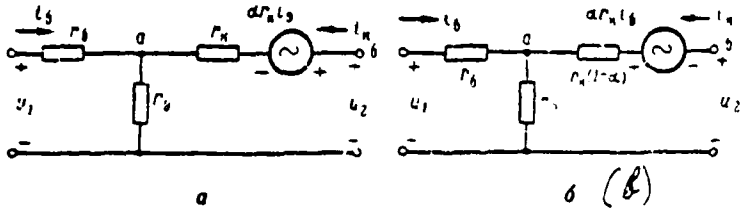

Figure III.32. Equivalent Circuit for a Transistor in a Common-Emitter Circuit.

An equivalent circuit for a transistor in a common-emitter circuit is depicted in Figure III.32. The Figure III.32a circuit usually is converted so that the emf generator is reflected by input current, base current in this instance. We will examine the sector of the collector network between points a and b. One may write for this sector

$$u_{ab} = i_к r_к - \alpha r_к i_э \qquad \text{(III.84)}$$

Considering that in a transistor, we will rewrite expression (III.84 in the following form:

$$u_{ab} = i_к r_к - i_б \alpha r_к - i_э \alpha r_к = r_к (1 - \alpha) i_к - \alpha r_к i_э \qquad \text{(III.85)}$$

The Figure III.32a equivalent circuit may be converted to the form shown in Figure III.32b based on the resultant expression. As follows from formula (III.85), the polarity of equivalent generator is opposite of that of generator . This speaks to the fact that collector current and base current are opposite.

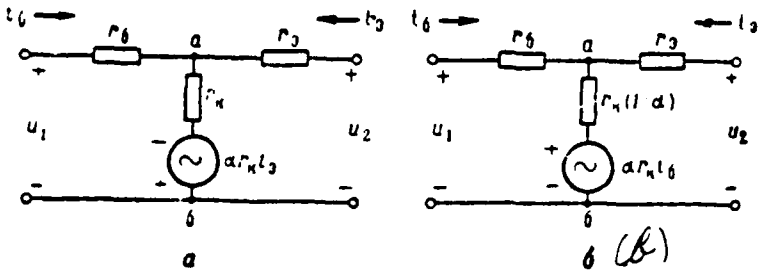

Figure III.33. Equivalent Circuit for a Transistor in a Common-Collector Circuit.

An equivalent circuit for a transitor in a common-collector circuit is depicted in Figure III.33. Here, in the Figure III.33b circuit, just as in the previous case, the equivalent genrator's emf is expressed as input current $i_б$.

The equivalent circuits examined may be used only at low frequencies, where transistor reactivity need not be considered. Moreover, modulation of the width of the base due to a change in collector voltage is not considered in these circuits. Reactive elements in a transistor need to be considered when frequencies increase. Junction capacitances primarily are among such elements.

Emitter and collector junctions are areas with a space charge and, from /130 this point of view, may be characterized by charge capacitances $C_э$ and $C_к$, respectively. Charge capacitance magnitudes are determined by pn junction geometric dimensions and the properties of the material from which they are manufactured, and also will depend on external voltage applied to the junction. A change in external voltage will lead to a change in the width of the spatial charge area: the area of the space charge expands with an increase in reverse voltage and the charge capacitance decreases; shrinkage of the space charges will occur with an increase in forward voltage and capacitance increases. Since the emitter junction displaces in a forward direction, while the collector junction does so in a reversed direction, emitter junction charge capacitance $C_э$ turns out to be much greater than collector junction capacitance $C_к$. Emitter junction capacitances comprise magnitudes on the order of hundreds of picofarads, while collector junction capacitances comprise magnitudes from unity to several tens of picofarads. However, one may disregard emitter junction capacitance influence since it is shunted by very slight resistance $r_э$. On the other hand, collector capacitance plays a

significant role since it is connected in parallel to resistance r_{κ} of great magnitude. For example, given a 5 pF collector junction capacitance and resistance MΩ, the capacitive and active components of collector resistance will be approximately equal at a frequency of 30 kHz. Consequently, collector capacitance exerts material influence on amplifier frequency characteristics.

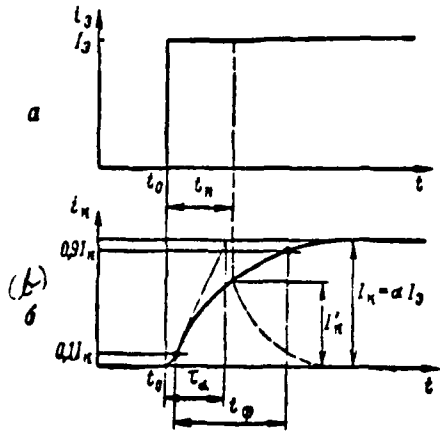

Figure III.34. Collector Current Transient Characteristic.

Diffusion processes in transistors exert significant influence on amplifier frequency properties. A phenomenon similar to the finite rate of electron transit in an electron tube is observed at high frequencies. A drop in gain α will occur with a rise in frequency. Diffused motion of carriers near the base is the main cause of the decrease in gain. They will move randomly, with varied thermal /131 rates and along varied trajectories. This will lead to the fact that, given emitter current jump-in by magnitude $I_э$ (Figure III.34a), there will be no corresponding collector current jump-in. Collector current pulse porch (or change) will turn out to be stretched (Figure III.34b). If the duration of the current's input pulse coincides with collector current-rise time, then the transient process will not succed in terminating and the amplitude of output current $I_к$ will turn out to be less than set value $I_к = \alpha I_э$.

Collector current pulse amplitude will drop when input pulse duration decreases. An analogous picture will be observed given the action of a periodic pulse or sine signal. Thus, the variety of the average rate of carriers diffusing near the base will lead to a decrease in collector current amplitude with a rise in

signal frequency. Fixed emitter current amplitude is equivalent to a drop in the factor α magnitude.

Along with the transistor phenomenon noted, a lag exists in collector current change relative to emitter current change. Lag time will depend on carrier mobility and base thickness. The period of oscillations and diffusion time will become coincident with a rise in signal frequency and the phase shift between the input and output signal will grow. It is evident that transistors made of the same material but having a thinner base will provide less lag and less dispersion of carrier rates, i. e., they will be of a higher frequency.

On the basis of what has been said, it is possible to consider that gain α in a common-base circuit, determined as the ratio of collector current to emitter current, will depend on frequency and may be characterized by modulus $|\alpha|$ and phase φ_2.

One may use the collector current transient characteristic (Figure III.34b) for approximate evaluation of frequency dependence of α , which, without considering lag, may be approximated with satisfactory precision by exponent /132

$$i_к(t) = I_к\left(1 - e^{-\frac{t}{\tau_к}}\right).$$

Here, $\tau_к$ — time constant characterizing the rate of collector current build-up and depending on the mobility of nonbasic carriers near the base and on the latter's thickness.

Considering that $i_к = \alpha I$, one may consider the collector current value in the set mode as equalling $I_к = \alpha_0 I$, (α_0 -- current gain value at low frequency). Consequently,

$$i_к(t) = I_к\alpha_0\left(1 - e^{-\frac{t}{\tau_к}}\right).$$

Since current I, after connection retains a constant value, then current gain is a function of time

$$\alpha(t) = \alpha_0\left(1 - e^{-\frac{t}{\tau_к}}\right). \qquad \text{(III.86)}$$

This form of gain α transient characteristic is analogous to that of an R-C integrator (see expression II.2). Therefore, based on an analogy with the frequency dependence of R-C network gain $\left(K(j\omega)=\frac{1}{1+j\omega RC}\right)$, current gain frequency dependence may be written as

$$\alpha(j\omega)=\frac{\alpha_0}{1+j\omega\tau_\alpha}. \tag{III.87}$$

In this event

$$\left.\begin{aligned}\alpha(\omega)&=\frac{\alpha_0}{\sqrt{1+(\omega\tau_\alpha)^2}},\\ \varphi_\alpha&=\operatorname{arctg}\omega\tau_\alpha\end{aligned}\right| \tag{III.88}$$

The frequency at which modulus α decreases by a factor of $\sqrt{2}$ relative to its low-frequency value is referred to as current gain threshold frequency

$$\omega_\alpha=\frac{1}{\tau_\alpha}=2\pi f_\alpha \tag{III.89}$$

Threshold frequency f_α will fall within limits ranging from tens of kilohertz to hundreds of megahertz, depending on transistor type. It should be noted that the utility of the (III.88) formulas is restricted to frequencies . . . .

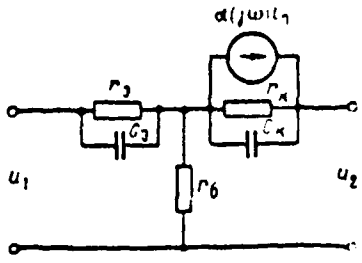

Figure III.35. Equivalent Circuit for a Transistor in a Common-Base Circuit Considering Capacitances.

An equivalent circuit for a transistor in a common-base circuit, considering junction capacitances and frequency dependence of gain . . , is depicted in Figure III.35.

Current gain in a common-emitter circuit (see expression III.82) equals /133

$$\beta(j\omega) = \frac{\alpha(j\omega)}{1-\alpha(j\omega)} \qquad \text{(III.90)}$$

Substituting value $\alpha(j\omega)$ from (III.87) in the above expression, after simple conversions we will get

$$\beta(j\omega) = \frac{\beta_0}{1+j\omega\tau_\beta}, \qquad \text{(III.91)}$$

where $\beta_0 = \frac{\alpha_0}{1-\alpha_0}$, $\tau_\beta = \frac{\tau_\alpha}{1-\alpha_0} = \frac{1}{\omega_\alpha}\cdot\frac{1}{1-\alpha_0}$.

Hence, the gain threshold frequency in a common-emitter circuit

$$f_\beta = \frac{1}{2\pi\tau_\beta} = f_\alpha(1-\alpha_0). \qquad \text{(III.92)}$$

Consequently, $f_\alpha \gg f_\beta$, i. e., a common-base circuit is more broadband than a common-emitter circuit is.

Thus, a transistor gain drop in the high-frequency area mainly will depend on a change in gain and on the magnitude of collector capacitance $C_к$. The first or second factor, or both simultaneously, may play the main role, depending on circuit parameters and transistor type.

3. Determination of Transistor Amplifier Basic Indicators

We will examine the operation of transistor amplifiers in the linear amplification mode given slight signals. In this case, the operating point is selected in that area of the volt-ampere characteristics where they may be considered linear. In this event, transistor equivalent circuits may be used to determine basic amplifier indicators: current and voltage gain and input and output resistance. We will consider that transistor parameters are purely active, i. e., the transistor is operating in the low-frequency area. Influence of the reactive elements of external networks and of the transistor itself will be examined specifically using pulse video amplifier circuits as our example.

Common-Base Circuit. This circuit is analogous to an amplifier with a common

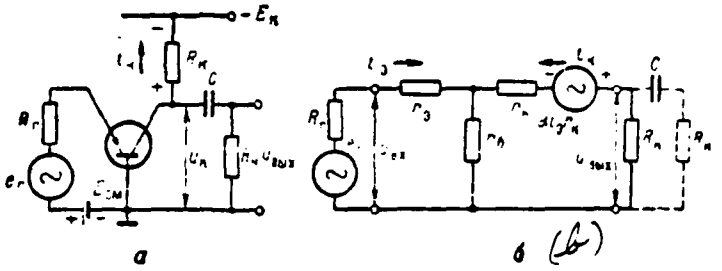

Figure III.36. Common-Base Amplifier:
(a) — Simplified circuit; (b) -- Equivalent circuit.

grid. A simplified amplifier circuit is depicted in Figure III.36a, while /134 its equivalent circuit for alternating components is shown in Figure III.36b. In this circuit, source $E_к$ is the amplifier supply source, while source $E_{см}$ is emitter junction forward bias and, thus, determines operating point. Opposite supply polarity must be used when npn transistors are used. Resistance $R_н$ connected to the collector network is the amplifier's load.

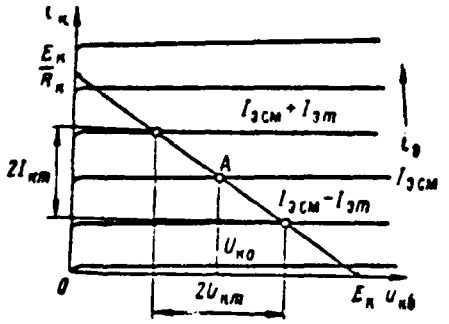

Figure III.37. For Determination of a Transistor's Common Operating Point in an OB Circuit.

One can explain operating point selection using the family of OB circuit collector characteristics and load line (Figure III.37). It is evident from Figure III.36a that the load line equation, just as was the case in tube amplifiers, may be written in the form

$$u_к = E_к - i_к R_к.$$

Providing with the aid of source $E_{см}$ initial current value $i_э = I_{эсм}$, we get operating point A at load line intersection with the corresponding collector current characteristic. Here, current $I_к$, almost equal to the emitter current magnitude, flows across the collector network. Collector current creates voltage drop $U_{R_к} = I_к R_к$ across resistance $R_к$. Consequently, in the initial mode, constant currents flow across the transistor networks, while constant voltage $U_{к0}$ exists in the collector (Figure III.38).

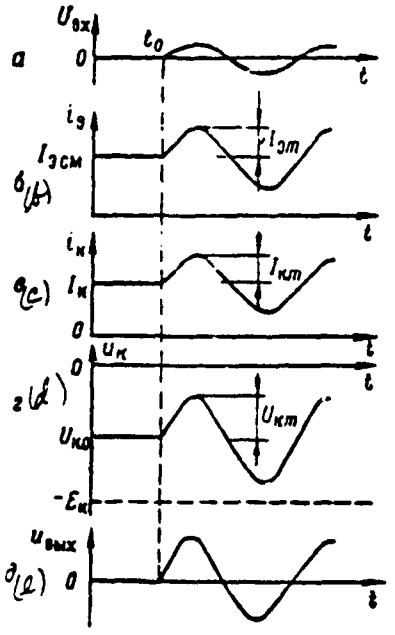

Figure III.38. Voltage Curves in a Common-Base Transistor Amplifier.

Let sinusoidal voltage $e_г = U_m \sin \omega t$ be supplied from moment t_1 to the /135 amplifier input. The height of the potential barrier of the emitter pn-junction will change due to the action of the input signal, which will elicit a corresponding change in emitter current and collector current.

Given positive input signal half-waves, emitter current will increase, while it will decrease given negative half-waves. Consequently, emitter and collector current alternating components with amplitudes $I_{эm}$ and $I_{кm}$ appear in the transistor.

Since an increase in collector voltage corresponds to an increase in collector current, the output voltage isolated from the direct component by capacitor C will be in phase with the input voltage (Figure III.38e).

We will not consider the influences of coupling capacitor C and external load $R_н$ when determining basic amplifier indicators, assuming that capacitive reactance X_C is very slight, while resistance $R_н$ is considerably greater than resistance $R_к$. In this event, a Kirchhoff equation for the input and output network may be written from the Figure III.36b equivalent circuit in the following form:

$$\begin{aligned} u_{вх} &= (r_э + r_б) i_э + r_э i_к; \\ 0 &= (r_э + r_к) i_э - (r_к - r_э + R_н) i_к. \end{aligned} \qquad \text{(III.93)}$$

Circuit input resistance may be determined as

$$R_{вх} = \frac{u_{вх}}{i_{вх}}. \qquad \text{(III.94)}$$

In our case, *emitter current* $i_э$ *is input current.*

Solving the second system (III.93) equation for current $i_к$, we will get

$$i_к = -\frac{r_э + r_к}{r_б + r_к + R_н} \cdot i_э. \qquad \text{(III.95)}$$

Then, eliminating current $i_к$ from the system's first equation, we will get /136

$$u_{вх} = (r_э - r_б) - r_э \frac{r_б + r_к}{r_б + r_к + R_н} i_э. \qquad \text{(III.96)}$$

Hence, input resistance

$$R_{вх} = \frac{u_{вх}}{i_э} = r_э - r_б - r_э \frac{r_б + r_к}{r_б + r_к + R_н} \qquad \text{(III.97)}$$

We will compile the output network circuit for determination of output

resistance magnitude, having expressed current i_1 by input network parameters. In accordance with the Figure III.36b circuit, we have

$$u_{вх} = e_г - i_г R_г - (r_г + r_б)\, i_б - r_б i_к$$

Hence

$$i_б = \frac{e_г - r_б i_к}{r_г + r_б + R_г}. \qquad \text{(III.98)}$$

Having substituted the current $i_б$ value (III.98) into the second (III.93) system equation and making simple conversions, we will get

$$e_г \left(\frac{r_б - \beta r_к}{R_г + r_г + r_б} \right) + \left(r_к + r_э - r_б \frac{r_э - \beta r_к}{R_г + r_г + r_б} \right) i_к + i_к R_к = 0. \qquad \text{(III.99)}$$

Introducing designations

$$e_{г.экв} = e_г \frac{r_б + \beta r_к}{R_г + r_г + r_б} \qquad \text{and} \qquad R_{э.б} = r_к + r_э - r_б \frac{r_б + \beta r_к}{R_г + r_г + r_б},$$

expression (III.99) may be rewritten in the following form:

$$e_{г.экв} = -(i_к R_{э.б} + i_к R_к). \qquad \text{(III.100)}$$

The minus sign speaks to the fact that, given input signal positive polarity, output current $i_к$ will have a direction opposite to that we accepted for the equivalent circuit. It is possible, in accordance with the resultant formula, to represent the amplifier's output network in the form of the Figure III.39 equivalent circuit. In that circuit, resistance $R_э$ is transistor output resistance

$$R_э = R_{э.б} = r_к + r_э - r_б \frac{r_б + \beta r_к}{R_г + r_г + r_б}. \qquad \text{(III.101)}$$

Current gain $K_I = \frac{i_к}{i_г}$ may be found directly from the second system (III.93) equation

$$K_I = \frac{i_к}{i_г} = -\frac{\beta r_б}{r_к + r_э + R_к}. \qquad \text{(III.102)}$$

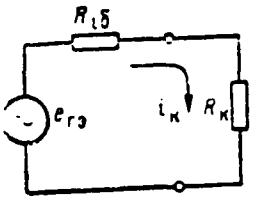

Figure III.39. Equivalent diagram of output network of amplifier

An important qualitative amplifier indicator is voltage gain, the ratio /137 of voltage $u_{вых}$ to signal source emf $e_г$:

$$K_u = \frac{u_{вых}}{e_г}. \qquad \text{(III.103)}$$

Considering that $u_{вых} = -i_к R_к$, while $e_г = (r_э - r_б - R_г) i_э + r_б i_к$, one may write

$$K_{u0} = \frac{-i_к R_к}{i_э r_э + r_б i_э + R_г i_э + r_б i_к} = \frac{-\frac{i_к}{i_э} R_к}{r_э + r_б + R_г + r_б \frac{i_к}{i_э}}.$$

Hence, considering that $K_i = \frac{i_к}{i_э}$ (see expression III.102), finally we get

$$K_{u0} = \frac{R_к (r_б + \alpha r_к)}{(R_г + r_э + r_б)(r_к + r_б + R_к) - r_б (r_б + \alpha r_к)} \qquad \text{(III.104)}$$

It is evident from the resultant expression that gain K_u will depend on signal source internal resistance $R_г$.

EXERCISE III.13

How is the relationship of voltage gain to signal source resistance $R_г$ physically explained? (Page 465)

The following inequalities usually are satisfied in transistor amplifiers:

$$r_к \gg r_б;\ r_б \gg r_э;\ r_к (1 - \alpha) > R_к.$$

Thus, for example, $r_к = 0.7$ MΩ, $r_б = 200$ ohms, $r_э = 20$ ohms, and $\alpha = 0.95$ for a P15 transistor.

Therefore, discarding the small terms in expressions (III.97), (III.101), (III.102), and (III.104), we will get simplified formulas suitable for practical calculations:

$$R_{вх.э} \approx r_э - r_б (1 - \alpha); \qquad \text{(III.105)}$$

$$R_{вых.э} \approx r_к \frac{R_г - r_э + r_б (1 - \alpha)}{R_г - r_э - r_б}; \qquad \text{(III.106)}$$

$$K_u \approx \quad (III.107)$$

$$K_i \approx \quad (III.108)$$

It is evident from analysis of the resultant formulas that a common-base transistor amplifier possesses very slight input and large output resistances. Circuit voltage gain is much greater than unity ($K_u \gg 1$), while current gain is less than unity ($K_i < 1$). Signal amplification in the circuit will occur without a change in its phase. /138

The requirement for comparators in multistage amplifiers is a serious shortcoming of common-base circuits. However, the capability to obtain high gain at relatively-slight load resistances insures a decrease in frequency distortions.

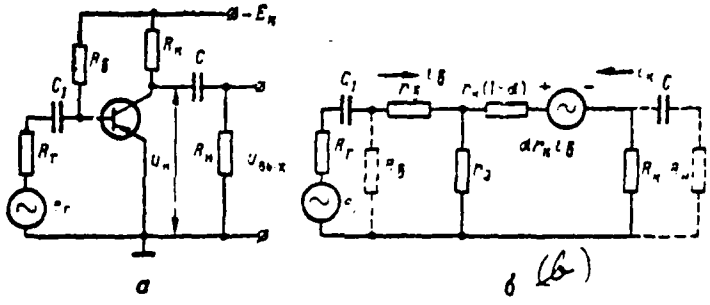

Figure III.40. Common-Emitter Amplifier:
(a) -- Simplified circuit; (b) -- Equivalent circuit.

Common-Emitter Circuit. A circuit for a common-emitter stage and its equivalent circuit for alternating components is depicted in Figure III.40. In its properties, this circuit is analogous to a common-cathode amplifier circuit.

Source $E_к$ in this circuit is used to supply the transistor and to impart /139 initial bias. The output signal is picked off resistance $R_н$ and is transmitted across isolating circuit $C_р$ to the next stage.

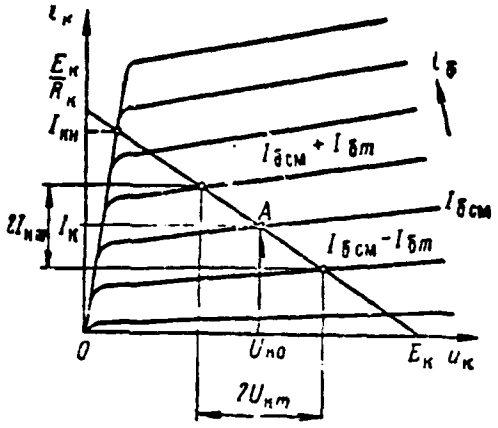

Figure III.41. For Determination of an OE Transistor Operating Point.

The amplifier's initial mode is determined by magnitudes $R_б$, $R_к$, $E_к$. OE circuit collector characteristics with load line plotted are depicted in Figure III.41. Operating point position is determined by the intersection of this line with the static characteristic corresponding to bias current $I_{б.см}$. The magnitude of this current may be determined as

$$I_{б.см} = \frac{E_к}{R_б},$$

since resistance $R_б$ magnitude usually is selected as much greater than resistance passing across the emitter--base sector.

Emitter junction potential barrier height changes when alternating sine voltage is supplied to input, which elicits a change in base and collector current. A positive half-wave of input voltage (Figure III.42a) decreases base current (Figure III.42b) and, consquently, collector current as well (Figure III.42c). Therefore, negative collector voltage increases (Figure III.42d) and output voltage turns out to be opposite in phase to input voltage.

Just as was the case for the common-base circuit, we will disregard the influence of coupling capacitors C_1 and C and the shunting action of resistances

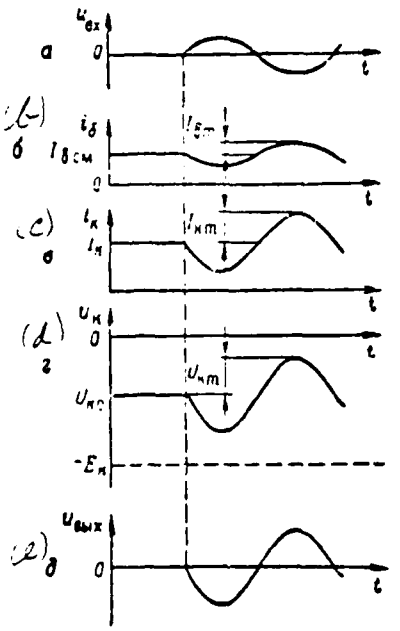

Figure III.42. Common-Emitter Transistor Amplifier Voltage Curves.

and when determining basic indicators, assuming that conditions are satisfied.

The system of Kirchhoff's equations for this case will be written as:

$$\dots \qquad \text{(III.109)}$$

We will use these equations to find all stage parameters, similar to /140 what was done for the common-base amplifier.

The reader is tasked independently to find all common-emitter circuit indicators.

Input resistance

$$R_{вх} = \frac{u_{вх}}{i_б} = r_б + r_э \frac{r_к + R_н}{r_к + R_н + r_э + R_э}. \qquad \text{(III.110)}$$

Output resistance

$$R_{вых.э} = r_к(1-\alpha) - r_э \frac{R_г + r_э + r_к}{R_г + r_э + r_б}. \qquad \text{(III.111)}$$

Current gain

$$K_{i\beta} = \frac{i_к}{i_б} = \frac{r_к - r_э}{r_э(1-\alpha) + R_к + r_б}. \qquad \text{(III.112)}$$

Voltage gain

$$K_{u\beta} = \frac{U_{вых}}{e} = \frac{R_к\,r_б - r_к r_э}{r_г r_э + R_г r_б + R_г R_к + r_э R_к + r_к(1-\alpha) - r_э r_б - r_к r_б}. \qquad \text{(III.113)}$$

Considering inequalities $r_к(1-\alpha) \gg R_к$ and $r_к(1-\alpha) \gg r_б$, which essentially always are satisfied, and keeping in mind that $\beta = \frac{\alpha}{1-\alpha}$, the above formulas are simplified considerably:

$$R_{вых.э} \approx r_б + \frac{r_э}{1-\alpha}. \qquad \text{(III.114)}$$

$$R_{вых.э} \approx r_к \frac{r_г + (R_г + r_э)(1-\alpha)}{r_э + r_б + R_г}; \qquad \text{(III.115)}$$

$$K_{i\beta} \approx \beta; \qquad \text{(III.116)}$$

$$K_{u\beta} \approx -\frac{\beta R_к}{r_э + R_г + r_б(1-\alpha)} \qquad \text{(III.117)}$$

The resultant mathematical ratios demonstrate that, given a common-emitter transistor circuit, input resistance turns out to be greater and output resistance less than in the common-base circuit. Small resistance sometimes is connected to the emitter network to increase input resistance. However, stage gain decreases somewhat here.

EXERCISE III.14

How does one explain the fact that the magnitude of the input resistance in a common-emitter circuit is greater than that in a common-base circuit? Why

does connection of a resistance to the emitter network increase input resistance magnitude? (Page 465)

Current gain in a common-emitter circuit is significantly greater than unity, while voltage gain is approximately equal to that in a common-base circuit. Signal power amplification in this circuit is much greater than in a common-base /141 circuit, thanks to the high factor β value. Inversion of the amplified signal will occur in the circuit. The common-emitter circuit examined has found very wide use in low-frequency and video amplifiers.

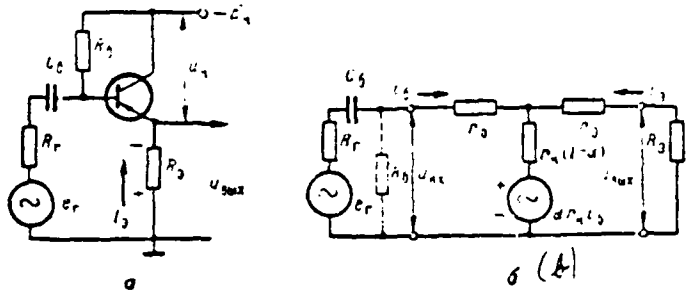

Figure III.43. Common-Collector Amplifier:
(a) -- Simplified circuit; (b) -- Equivalent circuit.

Common-Collector Circuit (Emitter Follower). A schematic diagram of a common-collector stage and its equivalent circuit for the alternating component are depicted in Figure III.43a, b. In its properties, this circuit is analogous to a cathode follower and usually is referred to as an emitter follower.

The amplifier's initial mode is determined by magnitudes of resistances R_1, R_2 and source voltage E_1. The operating point's position, just as was the case examined above, may be determined from the family of static output characteristics and load line. The load characteristic's equation $i_к = f(u_к)$ may be obtained from the expression $E_1 = I_к R_2 + u_к$, considering that $i_э \approx i_к$. Given factor α sufficiently close to unity, the load characteristic's approximate equation has the form

$$E_1 \approx I_к R_2 - u_к \qquad \text{(III.118}$$

Since the voltage drop in the base-emitter sector is slight, then bias current may be determined from expression

$$I_{\text{б. см}} \approx \frac{E_к - I_э R_э}{R_б}$$

Considering $I_э = (\beta + 1) I_б$ (see III.83), we have

$$I_{\text{б. см}} = \frac{E_к}{R_б (\beta + 1) + R_э} \qquad \text{(III.119)}$$

Potential barrier height in this circuit will rise when positive voltage is supplied to input, base and emitter current decrease, while emitter /142 voltage increases (it will become less negative). Thus, the phase of the amplified signal in an emitter follower circuit does not change.

A system of Kirchhoff equations for the Figure III.43b equivalent circuit input and output network may be written in the following form:

$$\left.\begin{aligned} u_{вх} &= (r_б + r_э) i_б + r_э (1 - \alpha) i_э, \\ U &= r_э i_б + [r_к - r_э (1 - \alpha) + R_э] i_э. \end{aligned}\right\} \qquad \text{(III.120)}$$

We will find all the stage's parameters from these equations.

Input resistance

$$R_{вх.э} = \frac{u_{вх}}{i_б} = r_б + r_э \frac{R_э + r_к}{R_э + r_к + r_э (1 - \alpha)}. \qquad \text{(III.121)}$$

Output resistance

$$R_{вых.э} = r_к + r_э \frac{(R_б + r_б)(1 - \alpha)}{R_б + r_б + r_э}. \qquad \text{(III.122)}$$

Current gain

$$K_{i.э} = \frac{i_к}{i_б} = \frac{r_э}{R_э + r_к - r_э (1 - \alpha)}. \qquad \text{(III.123)}$$

Voltage gain

$$K_{u\kappa} = \frac{i_{вых}}{e_г} = \frac{R_1 r_к}{(R_г - r_A - r_к)(R_э + r_э) + r_к (R_г + r_0)(1 - \alpha)} \qquad \text{(III.124)}$$

If the inequalities normally found in transistor circuits are satisfied,

$$r_к \gg r_0 + R_г; \quad r_к (1 - \alpha) \gg R_э; \quad R_э \gg r_э,$$

then the resultant ratios have a simpler form:

$$R_{вх.к} = R_{вх.эп} \approx \frac{R_э}{1 - \alpha} = R_э (\beta + 1); \qquad \text{(III.125)}$$

$$R_{вых.к} = R_{вых.эп} \approx r_э + (R_г + r_0)(1 - \alpha); \qquad \text{(III.126)}$$

$$K_{ik} = K_{iэп} \approx \beta + 1; \qquad \text{(III.127)}$$

$$K_{uк} = K_{эп} \approx \frac{R_1}{R_э + (R_г + r_0)(1 - \alpha)} = \frac{(\beta + 1) R_1}{(\beta + 1) R_э + (R_г + r_0)}. \qquad \text{(III.128)}$$

Thus, input resistance is great in an emitter follower circuit, while output resistance is slight. Current amplification is approximately the same as that in a common-emitter circuit, voltage amplification is less than unity, and output voltage is in phase with input voltage.

The enumerated properties are in full accord with those of a cathode /143 follower and, therefore, this circuit found very wide use as buffer and output stages.

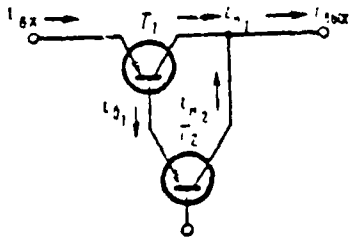

Figure III.44. Composite Transistor.

The necessity often arises in transistor technology to match pulse generators with a very-high resistance output (on the order of hundreds of kilohms and even unities of megohms) with a low-resistance load. In this event, special requirements are levied on the transistor from the maximum α (or β) point of view. Composite transistors, as shown in Figure III.44, often are used to obtain gain α approximating unity. If transistor T_1 and T_2 current gain equals α_1 and α_2, respectively, then the entire circuit's current gain z_2 equals

$$z_2 = z_1 + z_2 - z_1 z_2. \qquad \text{(III.129)}$$

EXERCISE III.15

Prove ratio (III.129) using Figure III.44. (Page 465)

If α_1 and α_2 are close to unity, then current gain β has a value on the order of hundreds and even thousands of unities in a common-emitter transistor circuit. Having a resistance R_1 magnitude on the order of unities of kilohms, input resistance magnitudes on the order of tens of megohms are possible.

EXERCISE III.16

What will emitter follower input resistance equal if two composite transistors with gains $z_1 = z_2 = 0.98$ and resistance $R_1 = 1$ kΩ are used in the follower? (Page 465)

4. Pulse Video Amplifier Circuits

Common-emitter and common-collector circuits have found greatest use in transistor pulse video amplifiers. The common-base circuit is used comparatively rarely since it has low input resistance (on the order of tens of ohms) and requires special matching stages.

The common-emitter stage depicted in Figure III.40a may be used to amplify video pulses. If the amplitude of the amplfied pulses is slight and the operating point does not depart linear sectors of the transistor volt-ampere characteristic, then amplification of the pulse signals does not differ from the amplification /144 of harmonic oscillations examined above. Representation of the pulse in the form

of the sum of harmonic oscillations may be used to determine the distortions of the pulse shapes if the transistor frequency characteristics are known. Along with transistor reactive parameters influencing mainly high-frequency distortions, reactive elements of external networks, such as interstage capacitors, matching transformers, self-bias networks, and the like, play a substantial role.

We will examine video amplifier frequency properties using the Figure III.40a circuit as our example since this type circuit has had widest distribution.

An equivalent circuit for a common- ·itter stage, considering the influence of collector ($C_к$) and emitter ($C_э$) junction capacitances by means of their direct connection to the equivalent circuit can be used for analysis of video amplifier frequency properties. In addition, one also must consider the frequency dependence of gain $\alpha(j\omega)$ or $\beta(j\omega)$.

However, junction capacitances play a decisive role when using high-frequency transistors with a large frequency limit magnitude (for example, P403 transistors with frequency $f_\alpha = 120$ MHz).

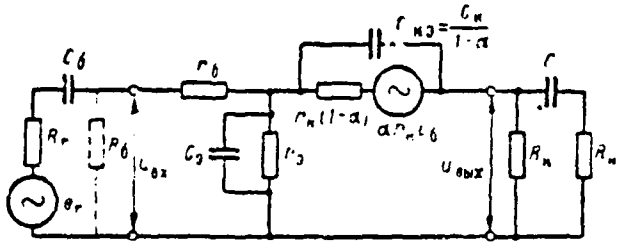

Figure III.45. Common-Emitter Video Amplifier Equivalent Circuit.

An OE amplifier equivalent circuit considering junction resistances is depicted in Figure III.45. The converted capacitance of collector junction $C_{к\omega}$ formally may be determined from the equivalent circuit (III.40b) by replacement of collector junction resistance $r_к(1-\alpha)$ by complex *impedance*

$$z_к = \frac{r_к}{1 + j\omega r_к C_к}(1-\alpha), \qquad \text{(III.130)}$$

determined by parallel connection of resistance $r_к$ and capacitance $C_к$ (see Figure

III.35). Having divided and multiplied the second term in the (III.130) /145
denominator by magnitude $(1-z)$, one may write

$$z_{\text{вх}} = \frac{r_{\text{б}}(1-z)}{1-\frac{1}{1-z}r_{\text{б}}(1-z)} = \frac{r_{\text{б}}(1-z)}{1+jC_{\text{вх}}r_{\text{б}}(1-z)}, \qquad \text{(III.131)}$$

where

$$C_{\text{вх}} = \frac{C_{\text{к}}}{1-z} = C_{\text{к}}(\beta+1). \qquad \text{(III.132)}$$

It is convenient to analyze circuit frequency properties for the middle-, low-, and high-frequency areas.

The capacitances of interstage capacitors $C_{\text{р}}$ and C, as well as transistor high-frequency properties, are not considered in the medium-frequency area. Selected resistance $R_{\text{к}}$ magnitude is considerably greater than stage input resistance. Therefore, it need not be considered during analysis. Ratios (III.110), (III.111), (III.112), and (III.113) may be used to compute basic amplifier indicators. However, one must consider that load resistance $R_{\text{н}}$ shunts resistance $R_{\text{к}}$. The subsequent amplifying stage, whose input resistance is relatively small, usually is amplifier load. Therefore, a magnitude determined by parallel connection of resistances $R_{\text{к}}$ and $R_{\text{н}}$ should be substituted in ratios (III.110) and (III.113) or (III.117) in place of $R_{\text{к}}$:

$$R'_{\text{к}} = \frac{R_{\text{к}}R_{\text{н}}}{R_{\text{к}}+R_{\text{н}}} \qquad \text{(III.133)}$$

If the subsequent stage is assembled into an identical circuit, then load resistance $R_{\text{н}} = R_{\text{вх}}$, and may be determined from formula (III.110) or (III.114).

Presence of coupling capacitor C in the low-frequency area decreases the current across the load and, consequently, stipulates frequency characteristic roll-off in this area, i. e., distortion of amplified pulse tilt. Capacitor $C_{\text{р}}$, whose presence decreases input current, affects the amplifier characteristic in an identical manner. Conditions $C \gg \frac{t_{\text{и}}}{R_{\text{н}}}$ и $C_{\text{р}} \gg$ need to be satisfied for undistorted transmission of pulse tilt. Since input resistance magnitudes in transistor amplifiers are slight, then coupling capacitor capacitance value often

reaches several microfarads, and sometimes even tens of microfarads. This capacitance does not increase transistor amplifier weight and overall dimensions since supply voltage does not exceed several tens of volts and, therefore, small components may be used.

The influence of coupling capacitors, whose resistance is insignificant, may be disregarded in the high-frequency area. We will consider only collector junction capacitance $C_{кв}$. It should be stated that emitter junction capacitance /146 $C_э$ also impacts upon amplifier frequency properties. The fact of the matter is that capacitance $C_э$, shunting junction resistance at high frequencies, will lead to input signal redistribution. An increase in frequency means an increase in the share of the signal impinging on base distributed resistance $r_б$ and the useful share of signal across the emitter junction decreases. As a result, amplification falls off. One strives to decrease the magnitude of resistance $r_б$ in high-frequency transistors for this reason.

But, since the impact of collector junction resistance $C_{кв}$ begins to manifest itself at lower frequencies, capacitance $C_э$ then usually is not considered.

The circuit's complex gain in the high-frequency area may be determined by substitution of complex magnitude $z_э$ from (III.130) in expression (III.113) to replace resistance $r_э$ and magnitude $R'_к$ (III.133) to replace resistance $R_к$. Before doing so, we will simplify expression (III.113), considering that inequality $r_б(1-\alpha) \gg r_э$ always is justified:

$$K'_{ов} = \frac{\alpha R'_к}{r_э + (r_б + R_г)\left(\frac{R'_к}{r_к} + 1 - \alpha\right)}. \qquad \text{(III.134)}$$

Following the appropriate substitutions in formula (III.134), we get

$$K'_{ов}(j\omega) = \frac{\alpha R'_к}{r_э + r_б + R_г\left[\frac{R'_к(r_к j\omega C_к + 1)}{r_к(1-\alpha)} + 1 - \alpha\right]} =$$

$$= \frac{\alpha R'_к}{r_э + \frac{(r_к + R_г)R_к}{r_к(1-\alpha)} + (r_б + R_г)(1-\alpha) + \frac{R_к(r_б + R_г)j\omega C_к}{1-\alpha}}. \qquad \text{(III.135)}$$

Collector load resistance in pulse amplifiers usually is minimal. Therefore,

inequality $r_к(1-a) \gg R_г$ is satisfied. In this case, expression (III.135) may be simplified and, considering (III.117), rewritten in the following form:

$$K_{ад}(j\omega) = \frac{aR_к'}{r_э + (r_б + R_г)(1-a)} \cdot \frac{1}{1 + \frac{R_к(r_б + R_г)C_{кэ}j\omega}{r_э + (r_б + R_г)(1-a)}} = \frac{K_{ад}}{1 + j\omega\tau_{эд}'}, \quad \text{(III.136)}$$

where

$$\tau_{эд}' = \frac{C_{кэ}(R_г + r_б)}{a} K_{ад}. \quad \text{(III.137)}$$

Hence, the gain modulus is /147

$$K_{ад}(\omega) = \frac{K_{ад}}{\sqrt{1 + \omega^2\tau_{эд}'^2}}. \quad \text{(III.138)}$$

Thus, time constant $\tau_{эд}'$ determines upper frequency limit $\omega_{в.д} \approx \frac{1}{\tau_{эд}'}$, and, consequently, amplified pulse rise time.

We will simplify expression (III.137) somewhat:

$$\tau_{эд}' = \frac{C_{кэ}(R_г + r_б)}{a} \cdot K_{ад} = \frac{C_к(R' + r_б) \cdot R_к'}{r_э[1 - a + (R_г + r_б)(1-a)]} \approx \frac{C_к R_к'(R_г + r_б)}{r_э(1-a)} \quad \text{(III.139)}$$

It is evident from this that $\tau_{эд}'$ must be decreased by decreasing resistance $R_г$ and transistors with a slight derivative $C_к r_б$ value used in order to expand the bandwidth in the high-frequency area, i. e., to reduce the porches. We will note that derivative $C_к r_б$ is a very important transistor high-frequency parameter and, along with other parameters, will occur in reference books. Significant decrease in resistance $R_к$ cannot be used to expand bandwidth since a fall-off of stage amplification occurs here.

Stage amplification properties to a strong degree will depend on the magnitude of threshold frequency $f_т$ when low-frequency transistors are used. We will assume that load resistance $R_к'$ is small and, therefore, the influence of capacitance $C_к$,

may be disregarded. Then, the amplifier frequency characteristic in the high-frequency area may be determined from expression (III.117) by substitution of complex value $z(j\omega)$ from (III.87):

$$K_{u\Phi}^{*}(j\omega) = \frac{\frac{z_0}{1+j\omega\tau_0} R_{\Phi}}{r_0 + (R_{\Phi} + r_{\Phi})\left(1 - \frac{z_0}{1+j\omega\tau_0}\right)} = \frac{K_{u\Phi}}{1+j\omega\tau_{0\Phi}}. \qquad \text{(III.140)}$$

where

$$K_{u\Phi} = \frac{z_0 R_{\Phi}}{r_0 + (R_{\Phi} + r_{\Phi})(1 - z_0)},$$

$$\tau_{0\Phi} = \tau_0 \frac{r_0 + (r_0 + R_{\Phi})}{r_0 + (R_{\Phi} + r_{\Phi})(1 - z_0)}. \qquad \text{(III.141)}$$

Since inequality $(r_0 + R_{\Phi}) \gg r_0$ always is satisfied, then

$$\tau_{0\Phi} = \frac{\tau_0}{1 - z_0} = \tau_{\beta} = \frac{1}{2\pi f_{\beta}}. \qquad \text{(III.142)}$$

It is evident from this that, given slight load resistances, the upper /148 frequency limit will depend only on transistor type and completely determines amplified pulse rise time.

Transient processes determining rise time flow during the period of 4--5 time constants. Pulse rise time is accepted as computed between levels 0.1--0.9 of the output voltage (or current) amplitude value. Here, rise time equals

$$t_{\phi} = 2.2\tau_{0\Phi}. \qquad \text{(III.143)}$$

EXERCISE III.17

There is a requirement to select a transistor to amplify a pulse of duration $t_{\Phi} = 0$ usec with permissible rise time $t_{\phi} \leq 0.1 t_{\Phi}$:

P14 -- f_{α} = 1.0 MHz; α = 0.95;
P15 -- f_{α} = 2.0 MHz; α = 0.95;
P168 -- f_{α} = 1.0 MHz; α = 0.98
P103 -- f_{α} = 1.0 MHZ; α = 0.9. (Page 465)

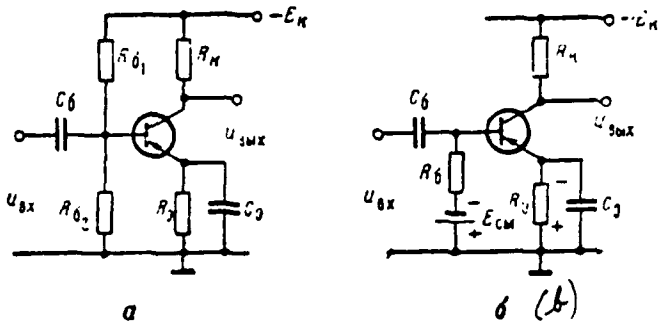

Figure III.46. Video Amplifier with Negative Current Feedback: (a) — Operating circuit; (b) -- Reduced circuit.

It was pointed out above that a common-emitter circuit has a lower frequency limit value compared to a common-base circuit and, consequently, the amplified pulse does not have a good a porch shape. However, this circuit shortcoming may be eliminated by using a compensating R-C network R_1C, connected as depicted in Figure III.46a.

If only one resistance $R_э$ is connected to the transistor emitter network, then this will lead to manifestation of negative current feedback and, thus, to an increase in input resistance and a decrease in stage gain. Connection of capacitor $C_э$ in parallel to resistance $R_э$ will lead to a decrease in the degree of feedback with a rise in frequency. Input resistance will decrease with an increase /149 in input pulse porch steepness and will increase the influx of carriers near the base. Consequently, influx to the collector will increase as well. This will lead to a reduction in pulse rise time. In frequency language, this is designated an increase in gain at high frequencies and frequency characteristic equalization.

Appropriate selection of $R_э$ magnitude makes it possible to decrease pulse rise time to a value close to that of the rise time in a common-base circuit. However, a decrease in stage gain in the low- and medium-frequency area will occur and will lead to a requirement for more stages to obtain assigned signal amplitude at output.

Nonetheless, the video amplifier circuit with emitter resistance $R_э$ (Figure

III.46a) will find wider use than will the Figure III.40a circuit since it has better initial mode temperature stability.

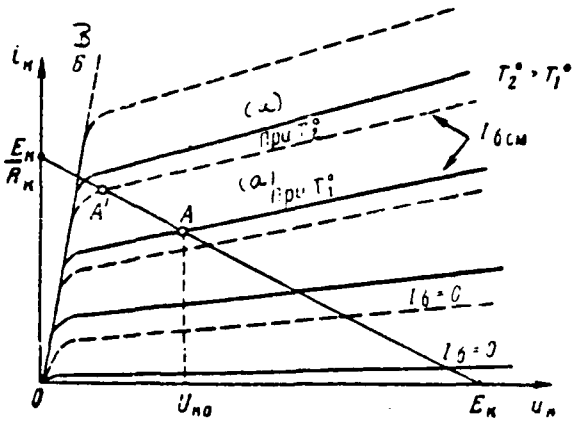

Figure III.47. Change in Operating Point Position Given Increased Temperature: (a) -- Where.

We will examine this question in somewhat more detail. Bias in the Figure III.40a circuit is fixed since $I_{б.см} = \frac{E_б}{R_б}$. Collector characteristics displace to the area of higher collector current values when temperature increases (Figure III.47). Here, bias current $I_{б.см}$ remains constant and the operating point (point A) shifts along the load line and may reach the critical mode line (0б), where a transistor loses amplification properties.

EXERCISE III.18 /150

$R_к = 1.2$ kΩ, $R_б = 160$ kΩ, and $E_к = -12$ V in the Figure III.40a amplifier circuit. Using collector characteristics (see Attachment 9), determine:

a) maximum positive output pulse amplitude at normal temperature;

b) pulse amplitude change when temperature changes. (Page 465)

Temperature stability in the Figure III.46a video amplifier circuit is achieved by a change in bias current with a change in temperature. We will use the theorem of the equivalent generator to convert the Figure III.46a input network in order

to demonstrate this. Equivalent circuit parameters (Figure III.46b) are:

$$\left.\begin{aligned} E_{\text{см}} &= \frac{E_к}{R_{б1}+R_{б2}}\cdot R_{б2}, \\ R_б &= \frac{R_{б1}\cdot R_{б2}}{R_{б1}+R_{б2}}. \end{aligned}\right| \qquad \text{(III.144)}$$

Considering that usually $R_б \gg r_б$ and $R_э \gg r_э$, bias current may be determined from formula

$$I_{б.\text{см}} = \frac{E_{\text{см}} - I_э R_э}{R_б}. \qquad \text{(III.145)}$$

Collector current, and, consequently, emitter current $I_э$, increases when the temperature increases. The voltage drop across resistance $R_э$ will rise, thanks to which base current $I_{б.\text{см}}$ decreases, by means of which operating point stabilization is achieved.

In other words, presence of resistance $R_б$ creates negative d-c feedback, which stabilizes the initial mode.

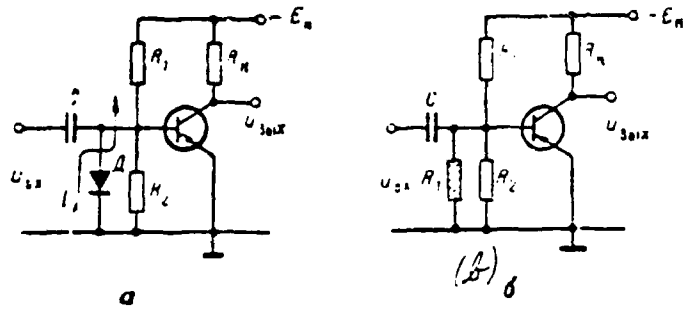

Figure III.48. Temperature - compensated Amplifier Circuit:
(a) -- With diode; (b) -- With effective thermal resistance.

Temperature compensation through use of nonlinear resistances such as thermistors and semiconductor diodes connected in the return (inverse) direction are used widely to stabilize transistor operating point. A temperature-compensated video amplifier circuit is depicted in Figure III.43. In the first instance, /151 a diode and, in the second, a thermistor is used as nonlinear resistance. The

principle of compensation means that bias in the base network changes when the environmental temperature changes. Thus, for example, collector current must increase, given an increase in temperature and given fixed bias. However, diode I_0 back current increases when the temperature rises (Figure III.48a) and bias voltage decreases. Therefore, collector network current essentially remains unchanged. High results may be obtained in transistor mode temperature stabilization if identical transistor and compensating element thermal inertness is insured.

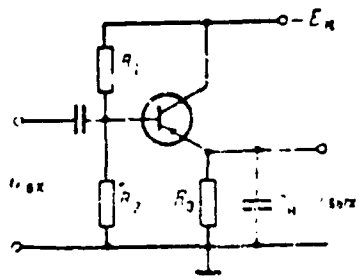

Figure III.49. Emitter Follower Circuit.

Common-Emitter Stage (Emitter Follower) A standard circuit for a common-collector stage, referred to as an "emitter follower," is depicted in Figure III.49. As pointed out above, an emitter follower is characterized by high input and low output resistance, making it possible to use it successfully as a decoupling and matching stage and as a power amplifier. High amplification stability and extreme circuit simplicity may be added to the list of advantages.

An emitter follower's transfer constant, determined in accordance with (III.128), is close to unity, even given relatively-large load resistance $R_н$ values. The magnitude of resistance $R_э$ in emitter followers intended for pulse transfer usually does not exceed units of kilohms. In this event, the stage's upper frequency limit will not depend on junction capacitances and is determined essentially by transistor amplification frequency limit.*

We will substitute the complex value of gain $\dot{K}_{н}$ from (III.91) in the

*This assumption is justified when using low-frequency transistors (type P16, P21, P30, P42, and others, for example).

emitter follower transfer constant (III.128) formula to determine stage upper frequency limit:

$$K_{\text{эп}}(j\omega) = \frac{\beta(j\omega) R_{\text{э}}}{\beta(j\omega) R_{\text{э}} + (R_{\text{г}} + r_{\text{б}})} = \frac{\beta_0 R_{\text{э}}}{\beta_0 R_{\text{э}} + (R_{\text{г}} + r_{\text{б}})(1 + j\omega\tau_\beta)}$$
$$= \frac{\beta_0 R_{\text{э}}}{\beta_0 R_{\text{э}} + (R_{\text{г}} + r_{\text{б}})} \cdot \frac{1}{1 + \frac{j\omega\tau_\beta (R_{\text{г}} + r_{\text{б}})}{\beta_0 R_{\text{э}} + (R_{\text{г}} + r_{\text{б}})}} = \frac{K_{\text{эп}}}{1 + j\omega\tau_{\text{эп}}}, \qquad \text{(III.146)}$$

where /152

$$\tau_{\text{эп}} = \tau_\beta \frac{R_{\text{э}} + r}{\beta_0 R_{\text{э}} + (R_{\text{г}} + r_{\text{б}})} \qquad \text{(III.147)}$$

Output pulse rise time computed at amplitude value levels 0.1--0.9 equals

$$t_{\text{ф}} = 2{,}2\tau_\beta \frac{R_{\text{г}} + r_{\text{б}}}{\beta_0 R_{\text{э}} + R_{\text{г}} + r_{\text{б}}} \approx 2{,}2\tau_\beta \frac{R_{\text{г}}}{\beta_0 R_{\text{э}} + R_{\text{г}}}. \qquad \text{(III.148)}$$

If signal source internal resistance is slight, then rise time $t_{\text{ф}} \approx 2{,}2\tau_\beta$ obtained is almost identical to that in a common-base circuit.

Rise time when high-frequency transistors are used is determined not by transistor frequency limit, but by base network time constant $(R_{\text{г}}+r_{\text{б}})C_{\text{к}}$ formed by signal source resistance $R_{\text{г}}$, base resistance $r_{\text{б}}$, and transistor collector resistance $C_{\text{к}}$.

In conclusion, we will note one other special feature of an emitter follower operating a capactive load (capacitance $C_{\text{н}}$ is denoted by the dotted line in Figure III.49). An oscillating mode of output voltage determination is possible in this case. B. N. Fayzulayev examined this problem in detail in [18], so we will dwell only on the physical aspect of this phenomenon.

The capacitance shunts load resistance $R_{\text{н}}$ during pulse porch transfer, given a capacitive load, resulting in an additional charge being introduced to the transistor base. Emitter follower output curren. comprises resistive and capacitive components. Capacitive current must cease by the end of the transmitted porch, while the base charge must be determined only by the load's resistive component. However, the base charge is unable to change instantaneously. Therefore, current exceeding the established value will flow across the transistor. Capacitance

$C_н$ continues to be charged as a result. Voltage with an opposite sign /153
will be applied to the emitter-base junction when voltage at output exceeds the set value and base current will change direction. Dispersal of excessive charge and decrease in current across the transistor occur as a result. Voltage at output takes on the set value following several over-oscillations.

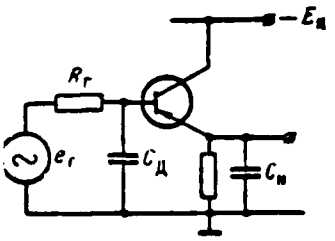

Figure III.50. Capacitance $C_д$ Connection for Oscillation Damping.

Damping capacitor $C_д$ of slight capacitance is connected at emitter follower input in those cases when the oscillatory mode is undesireable (Figure III.50). This decreases transistor input current magnitude, thereby constraining the onset of an excess base charge. However, this has a deleterious effect on pulse porch steepness.

CHAPTER IV /154

CLAMP CIRCUITS

§ 1. CLAMP CIRCUIT PURPOSE, CLASSIFICATION, AND OPERATING PRINCIPLE

It was demonstrated in Chapter II, § 5 that, when a pulse train flows across a transient R-C network, its output voltage initial level changes due to influence of coupling capacitor C. In accordance with (II.54), it changes in a linear R-C network by the input voltage d-c component magnitude (a d-c component loss occurs). In accordance with (III.55), it changes in a nonlinear R-C network by a magnitude depending on pulse $U_{вх}$ amplitude and ratios $\frac{t_и}{t_н}$ and $\frac{R_i}{R_p}$. It is evident that this level change will depend also on pulse shape and polarity.

If transient R-C network output voltage reaches electron-tube circuit input, the change in initial voltage level will elicit tube operating point "drift" (displacement) in its transfer characteristic. Operating point drift may impact significantly on processes in the circuit and, in some instances, completely disrupt its operation.

If dynamic bias caused by transient network influence is fixed, then it would be simple to compensate for it by means of additional fixed opposite polarity bias supplied to circuit input from an external source. But, as we saw, dynamic bias will depend on parameters of the pulses supplied to transient R-C network

input. These parameters may be changed as pulse circuits operate, first of all, specially. For example, forward sweep sawtooth voltage and intensifier pulse duration change with a jump during a staged scale change in the range display; sawtooth sweep voltage amplitude and polarity change periodically during a type P-display; and so forth. Secondly, random pulse parameter changes always occur due to unavoidable instability in circuit operation, influence of parasitic parameters and interference, and so forth. Sometimes, just by virtue of its nature, pulse voltage is characterized by a random structure (for example, radar receiver signal at output).

Consequently, the intitial level of voltage at transient R-C network //155 output always is subjected to changes and, therefore, the method of dynamic bias compensation by means of a fixed bias source is not applicable. Therefore, special devices providing a fixed and predetermined initial output voltage level, given any pulse parameter changes at network input and at any moment in time, are connected at transient R-C network output. These devices are called clamps. Thus, clamps are tasked to stabilize the initial mode of circuits connected to transient R-C network output.

Since it is possible to clamp either output voltage lower level $\underline{U}_{вых}$ or its upper level $\overline{U}_{вых}$, while, in each instance, this level may equal zero, be positive, or be negative, then six standard clamp circuits exist:

-- zero lower clamp $(\underline{U}_{вых}=0)$;
-- positive lower clamp $(\underline{U}_{вых}>0)$;
-- negative lower clamp $(\underline{U}_{вых}<0)$;
-- zero upper clamp $(\overline{U}_{вых}=0)$;
-- positive upper clamp $(\overline{U}_{вых}>0)$;
-- negative upper clamp $(\overline{U}_{вых}<0)$.

These circuits' output voltages, given the influence of positive pulses at transient network input, are depicted in Figure IV.1.

If, as a result of clamp operation, output voltage initial level turns /156 out to equal input voltage initial level $\underline{U}_{вых}=\underline{U}_{вх}$ or $\overline{U}_{вых}=\overline{U}_{вх}$, then the clamp is referred to as a level restorer. In particular, when $\underline{U}_{вых}=\underline{U}_{вх}=0$ or $\overline{U}_{вых}=\overline{U}_{вх}=0$, the clamp is referred to as a zero level restorer or zero restorer.

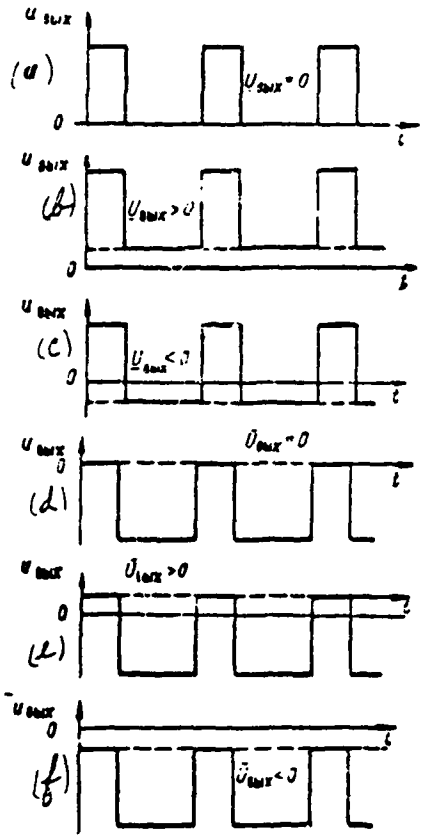

Figure IV.1. Clamp Output Voltages: (a) -- Zero lower clamp; (b) -- Positive lower clamp; (c) -- Negative lower clamp; (d) -- Zero upper clamp; (e) -- Positive upper clamp; (f) -- Negative upper clamp.

Since where there is equality of identical initial levels fixed voltage components $u_{вых}$ and $u_{вх}$ also turn out be equal ($U_{вых=} = U_{вх=}$), then a level restorer often is referred to also as a fixed component restorer.

Bilateral synchronous clamp circuits, used if input voltage polarity may be changed during the operating process, are a special type.

Clamp action is based on use of nonlinear R-C network properties. The diode clamp circuit, a structural diagram of which is depicted in Figure IV.2, is used most widely. The clamp comprises diode D and fixed bias source E. In principle, the diode is a required clamp nonlinear element and is connected in parallel to

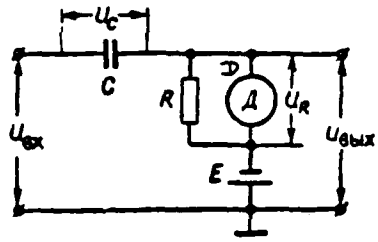

Figure IV.2. Clamp Circuit Structural Diagram.

transient network output resistance R. Thanks to unilateral conductivity, the latter converts it basically into a nonlinear clamp.

Actually, current may pass across the diode in one direction only (from plate to cathode), while diode internal resistance $R_д$ is slight in the conducting state. Therefore, depending on diode connection method, it will shunt resistance R either during the charging process or during the discharging process, here decreasing total network resistance to magnitude

$$\frac{RR_д}{R+R_д} \approx R_д \ll R. \qquad (IV.1)$$

As a result, resistances in the capacitor charging network $R_з$ and discharging network $R_р$ will become radically different: either $R_з = R_д \ll R_р = R$ or, vice versa, $R_р = R_д \ll R_з = R$. Here, the voltage u_R maximum or minimum value is clamped at the zero level (see Figure II.30 and II.31).

The second clamp circuit element — fixed bias source E — is connected in series with parallel-connected resistance R and the diode so that voltage /157 at clamp output equals

$$u_{вых} = u_R + E. \qquad (IV.2)$$

This bias determines the required (differing from zero) initial level value and, consequently, output voltage d-c component. Bias voltage E does not affect diode operation and input voltage a-c component passage.

Thus, with the help of the diode, the upper or lower (depending on diode connection method) initial voltage level u_R is clamped at zero, while bias E increases or decreases (depending on E polarity) the output voltage initial level to the requisite magnitude. Here, the clamped output voltage initial level will not depend on input voltage parameters and is determined by the clamp circuit itself.

In particular cases (given zero level clamping), bias E may be absent.

§ 2. ZERO LOWER CLAMPS

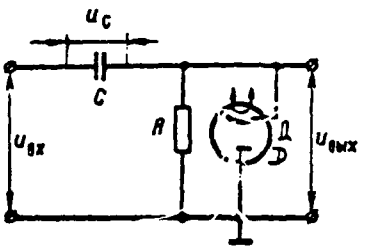

Figure IV.3. Zero Lower Clamp Circuit.

A zero lower clamp circuit is depicted in Figure IV.3. We will examine its operation as positive pulses with initial level $U_{вх}=0$ are supplied to input. The curves of circuit voltages for this instance are depicted in Figure IV.4.

Capacitor C is charged during pulse action when $u_{вх}=U_{вх}$. Since here voltage $u_{вых}=u_{вх}-u_c>0$ and is applied with a "plus" to diode cathode and with a "minus" to diode plate, the diode is blanked and charging current i_1 will pass across resistance $R_1=R$. Charging network time constant equals $\tau_1=CR$, while inequality (II.32) $\tau_1 \gg t_и$ must be satisfied in order to have minimum a-c component distortion.

Capacitor C discharges during resting times when $u_{вх}=0$. The diode opens since here voltage $u_{вых}=-u_c<0$ and is applied with a "plus" to plate and a "minus" to cathode. Therefore, in accordance with (IV.1), $R_p \approx R_1$ and discharging current i_p mainly passes across the diode. Discharging network time constant $\tau_p=CR_1$. Consequently, a significantly nonlinear network was the result when $R_1 \gg R_p$ and

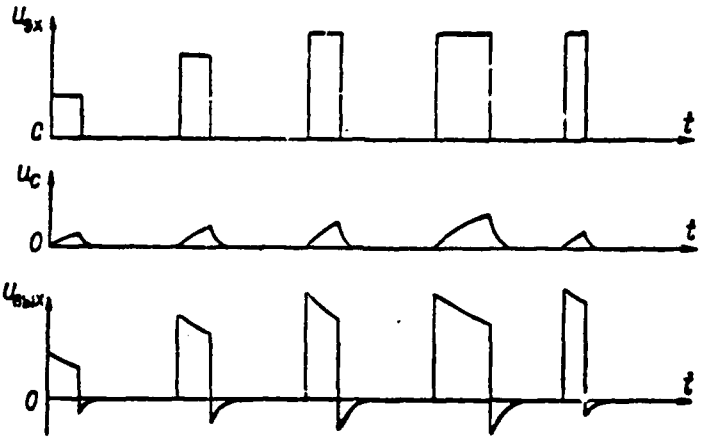

Figure IV.4. Voltage Curves for a Zero Lower Clamp Given a Change in Input Pulse Amplitude and Duration from $\underline{U}_{вх}=0$.

$\tau_и \gg \tau_р$. In accordance with Figure II.31, voltages in such a network change ($\Pi^+ \gg \Pi^-$).

Here, if $\tau_р \ll \tau_и$, then capacitor C essentially succeeds in discharging /159 completely during resting times. Therefore, at the end of the resting time $u_{вых}=0$, i. e., the output voltage lower initial level is clamped at zero: $\underline{U}_{вых}=0$.

Since the input voltage lower initial level in the examined instance also equals zero, the clamp circuit operates in the zero lower clamp restorer mode, i. e., as a d-c component restorer: $\underline{U}_{вых}=\underline{U}_{вх}=0$; $U_{вых-}=U_{вх-}$.

It is important to note that, if only $\tau_р \ll t_{ч.ср}$, then, as depicted in Figure IV.4, clamping occurs also when input signal parameters change ($U_{вх}$, $t_и$, $t_п$) .

We now will assume that negative pulses are supplied to circuit input ($u_{вх} < 0$). Voltage curves for this instance are depicted in Figure IV.5.

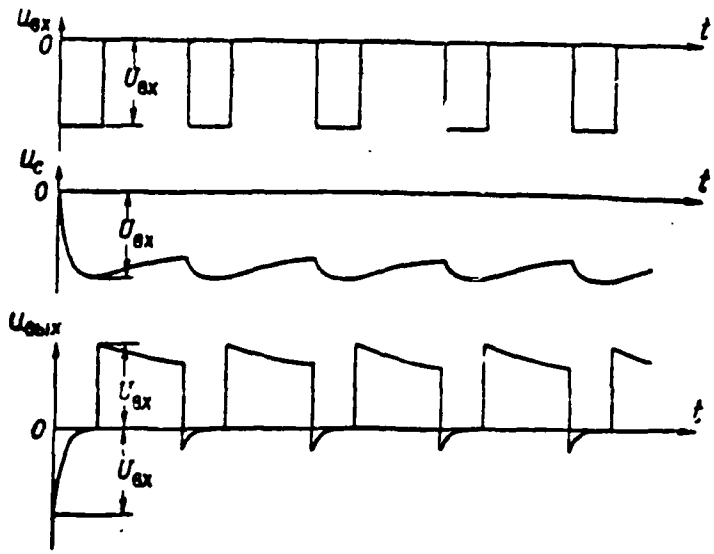

Figure IV.5. Voltage Curves for a Zero Lower Clamp During Negative Pulse Action When $U_{вх}=0$.

Now, on the other hand, during pulse action where $u_{вх}=-U_{вх}$, capacitor C charges across a diode with slight time constant $\tau_з=CR_з \ll t_и$. Therefore, during time $t_и$, capacitor C charging essentially ceases, while voltage in it at the end of the pulse reaches value $U_{C\,мин}=-U_{вх}$, while output voltage reverts to zero: $u_{вых}=u_{вх}-u_C=U_{вх}-U_{вх}=0$.

During resting times, $u_{вх}=0$ and the capacitor discharges across large resistance R with time constant $\tau_р=CR \gg t_п$. Therefore, capacitor voltage during resting time changes slightly, while, since at the onset of resting time where $u_{вх}=0$, $u_{вых}=-U_{C\,мин}=U_{вх}$. Then, output voltage decreases slightly compared to its maximum value. Consequently, as usual, output voltage lower initial level $U_{вых}=0$ is clamped at zero.

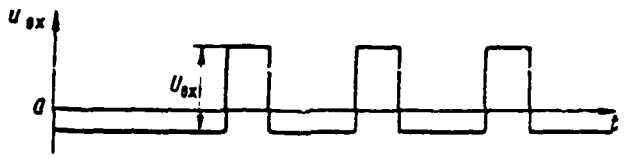

Figure IV.6. For Exercise IV.1.

EXERCISE IV.1

Plot the curves of voltages u_C and $u_{вых}$ for a zero lower clamp if voltage depicted in Figure IV.6 ($U_{вх}<0$) is supplied to its input. (Page 466)

§ 3. ZERO UPPER CLAMPS

A zero upper clamp circuit is depicted in Figure IV.7. It differs from the zero lower clamp circuit only in the method of diode connection.

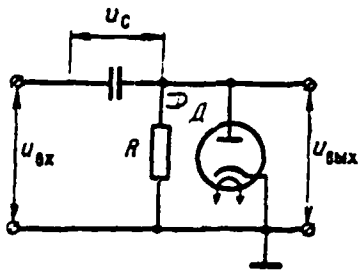

Figure IV.7. Zero Upper Clamp Circuit.

We will assume that positive voltage pulses ($u_{вх}\geqslant 0$) are supplied to /160 circuit input. Capacitor C is charged during pulse $u_{вх}=U_{вх}$ action. Since voltage $u_{вых}=u_{вх}-u_C>0$ also is supplied as a "plus" to plate and as a "minus" to cathode, charging occurs across the diode ($R_-=R_i\ll R$) with slight time constant $\tau_з=CR_i$.

During rest times, $u_{вх}=0$ and capacitor C discharges. Since here voltage $u_{вых}=-u_C<0$ also is applied as a "minus" to plate and as a "plus" to cathode,

the diode is blanked and capacitor C discharges across resistance $R_1 = R$ with large time constant $\tau_1 = CR$.

Consequently, a basically nonlinear network resulted where $R_p \gg R$; $\tau_p \gg \tau_1$. Voltages for such a network in the circuit change in accordance with Figure II.32 ($U^- < U^+$) . If $\tau_1 \ll t_и$ here, then capacitor C succeeds essentially in charging completely during pulse action time, while voltage $u_{вых} = 0$ by the moment the pulse ceases; as a result, output voltage upper initial level turns out to equal zero: $\overline{U}_{вых} = 0$.

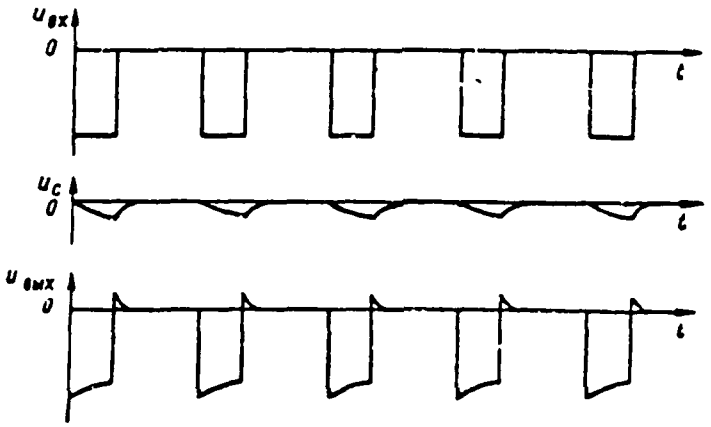

Figure IV.8. Zero Upper Clamp Voltage Curves During Negative Pulse Action Where $\overline{U}_{вх} = 0$.

We will assume that negative voltage pulses ($u_{вх} < 0$) are supplied to circuit input. Voltage curves in the circuit for this example are depicted in Figure IV.8.

During pulse action when $u_{вх} = -U_{вх}$, the capacitor charges, while /161 the diode turns out to be blanked for charging current: $R_1 = R$; $\tau_1 = CR \gg t_и$. Therefore, during time $t_и$, capacitor C succeeds in charging slightly and $u_{вых} = u_{вх} - u_C \approx -U_{вх}$.

During resting time, $u_{вх} = 0$ and the capacitor rapidly discharges across the diode with slight time constant $\tau_1 = CR_д$. If $\tau_p \ll t_п$, then, during resting

time, capacitor C discharges completely and, when the subsequent pulse becomes active, voltage $u_{вых}=0$.

Consequently, output voltage $u_{вых}\leq 0$, i. e., as usual, its upper level $U_{в.у}=0$ is clamped at zero.

Since in this case $\bar{U}_{вых}=\bar{U}_{вх}=0$ and, thus, $U_{вых-}=U_{вх-}$ as well, the clamp then operates in the zero upper-restorer mode, i. e., as a d-c component restorer.

EXERCISE IV.2

Plot the curves of voltages u_c and $u_{вых}$ for a zero upper clamp if the voltage depicted in Figure IV.6 is supplied to its input. (Page 466)

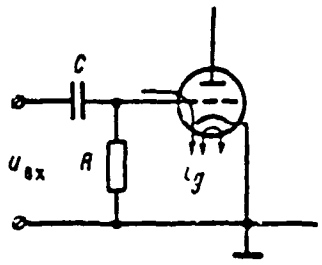

Figure IV.9. Use of the Triode Grid--Cathode Path For Zero Upper Clamping.

A zero upper clamp in which the electrical valve-like actions of a triode grid--cathode path are used instead of a diode, often are used in practical circuits (Figure IV.9).

Such a circuit is used when positive pulses are supplied to triode input and makes it possible to insure triode cut-off during resting times. The circuit operates in the following manner. The triode is open while the positive pulse is active and rapid capacitor C charge occurs across slight grid--cathode path resistance ($r_{gk}\ll R$) by grid current i_g. The capacitor discharges slowly during resting times across large transient network resistance R (grid--cathode path resistance is infinitely great for discharging current). Here, negative voltage

$u_{вых} \approx -U_{вх}$ arises at resistance R and the triode may be closed by this voltage (conditions for triode cut-off with dynamic bias were examined in Exercise II.15).

§ 4. NON-ZERO CLAMPS

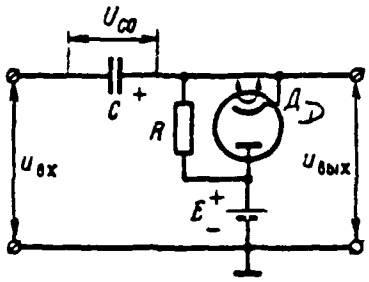

Figure IV.10. Positive Lower Clamp Circuit.

We will examine the Figure IV.10 circuit. It differs from a zero lower clamp circuit (Figure IV.3) only by the presence of fixed bias source $E>0$* . Source E is connected in accordance with Figure IV.2 (in series to parallel- /162 connected resistance R and a diode) and $u_{вых}=U_R+E$ in accordance with (IV.2).

If $u_{вх}=0$, then, under the influence of bias source E, capacitor C charges across the diode, voltage source $u_{вх}$ internal resistance, and bias E to constant voltage $U_{C0}=-E$. Here, $u_{вых}=-U_{C0}=E=\text{const}$.

It is important to note that, due to source E, no bias is supplied to the diode (bias source E "minus" is isolated by the capacitor from diode cathode). Therefore, given input voltage action, the diode operates just as it does without bias source E.

Capacitor C voltage changes additionally when input pulses $u_{вх}$ are supplied (component $u_{C\sim}$ appears) depending on pulse $u_{вх}$ and ratio $R_з$ and $R_р$ parameters (in order that this ratio, as usual, is determined by resistances R and $R_д$, source E internal resistance must be as low as possible). Here, resultant capacitor

*Bias source E polarity is determined relative to "ground."

voltage equals $u_C = U_{C0} + u_{C\sim}$, where $U_{C0} = -E$, while voltage $u_R = u_{вх} - u_C - E = u_{вх} - u_{C\sim}$, i. e., it changes exactly as in a circuit with analogous diode connection, but without bias source E (zero lower clamp circuit).

Since $u_{вых} = u_R - E$, the curve of the voltage at output of this circuit displaces "upwards" to magnitude E. Thus, it is a positive lower clamp /163 circuit: $U_{вых} = E > 0$.

It is evident that the output voltage of any clamp circuit with a bias source also will differ from the output voltage of a clamp circuit with analogous diode connection, but without bias source E (zero clamp), only by displacement "upwards" or "downwards" (depending on E polarity) by magnitude E.

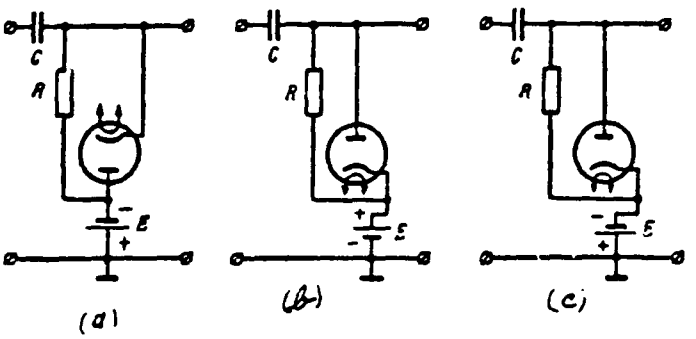

Figure IV.11. Non-Zero Clamps.

EXERCISE IV.3

a) Draw the curves of voltages $u_{вх}$, u_C, $u_{вых}$ for the Figure IV.10 circuit given negative square pulse action.

b) Determine the Figure IV.11 clamp circuit type. (Page 466)

§ 5. D-C COMPONENT RESTORATION

A clamp is a d-c component restorer if d-c voltage components at transient network output and clamp output turn out to be equal $U_{вх=} = U_{вых=}$.

The d-c component restoration mode is not simply reproduction of the input voltage d-c component at clamp output. Actually, d-c component $U_{вх=}$ is not passed by isolating capacitor C to network output. Value $U_{вых=}$ for a given a-c component $u_{вых}$ will depend on output voltage initial level. But, this level is determined only by the diode connection method and bias E in the clamp circuit itself and will not depend on input voltage parameters (this is the whole idea behind using clamps). Consequently, d-c component restoration requires that output voltage initial level, independent of the clamp circuit, coincide with input voltage initial level. We will assume, in order to explain this concept, that a positive lower clamp restores the d-c component $U_{вых=} = U_{вх=}$, but, during the operating process, from certain moment in time t_1, input voltage initial level began to change (Figure IV.12). Since $U_{вых} = \text{const}$ for a given clamp circuit, the restoration mode is disrupted here: $U_{вых} \neq U_{вх}$; $U_{вых=} \neq U_{вх=}$.

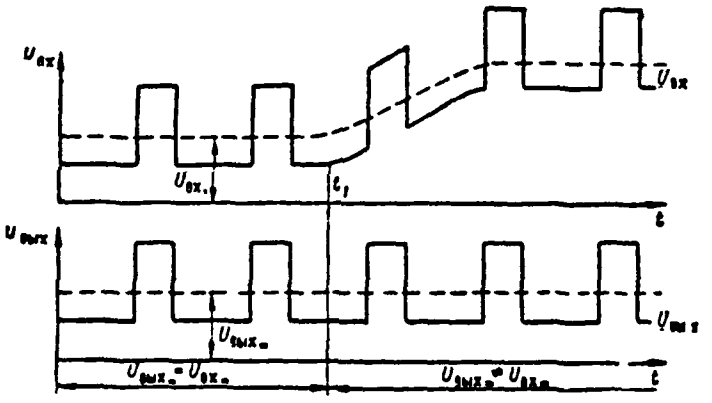

Figure IV.12. Disruption of the D-C Component Restoration Mode When Input Voltage Initial Level Changes.

Thus, d-c component restoration using clamps is possible only given input voltage initial level constancy.

EXERCISE IV.4

A cathode-ray tube [CRT] with an electrostatic deflection system is used in a horizontal range A-display and signal amplitude display. A simplified circuit for supply of positive intensifier pulses $u_{имп.с}$ to CRT control electrode, /164

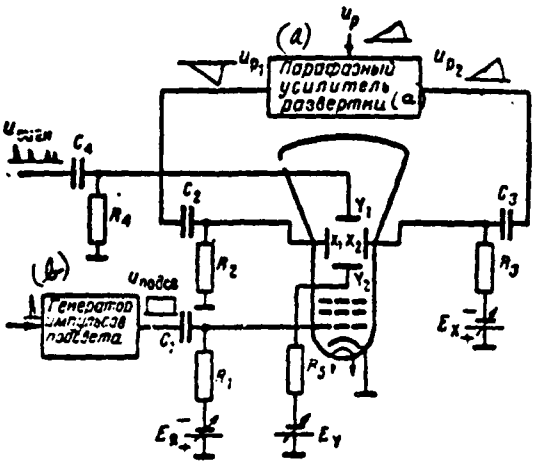

Figure IV.13. For Exercise IV.4.
(a) — Paraphase sweep amplifier; (b) — Intensifier pulse generator.

paraphase sweep voltage u_{p1} and u_{p2} to horizontal deflection plates X_1 and X_2, and positive target video pulses $u_{c.имп}$ to vertical deflection plates Y_1 and Y_2 is depicted in Figure IV.13. Explain what consequences may result from influence of transient networks R_1C_1, R_2C_2, R_3C_3, and R_4C_4. Draw this circuit and connect to it clamp circuits which eliminate transient network influence. (Page 466)

§ 6. BIDIRECTIONAL (SYNCHRONOUS) CLAMPING /165

Regardless of input voltage polarity, voltage at diode clamp output always changes only in one direction from the clamped level: downwards if upper level $\overline{U}_{зам}$ is clamped and upwards if lower level $\underline{U}_{зам}$ is clamped. This is referred to as unidirectional clamping and is achieved thanks to undirectional diode conductivity.

Input voltage polarity in some devices may be changed during operation. Slight initial level $\overline{\underline{U}}_{зам}$ then requires clamping, from which output voltage must change to one direction or the other, depending on input voltage polarity. This is referred to as bidirectional clamping.

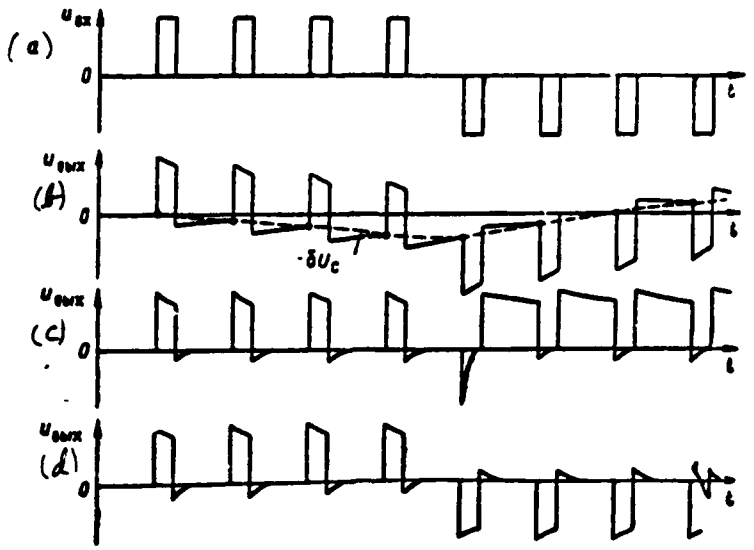

Figure IV.14. Input Pulses of Alternating Polarity (a) and Voltage at Linear Transient Network Output (b), Zero Lower Clamp (c), and Bidirectional Zero Clamp (d).

The difference between unidirectional and bidirectional clamping is explained in Figure IV.14.

Square input pulses, whose polarity was changed during operation from positive to negative ($U_{вх}$, and U_m are fixed magnitudes), are depicted in Figure IV.14a.

If this voltage is transferred across a linear transient network, then, due to positive pulse action, charges of one sign will be accumulated in the /166 capacitor, while charges of the other sign will be accumulated due to negative pulse action. Therefore, the sign of "drift" voltage δU_c will change (Figure IV.14b).

Given unidirectional zero lower clamping $U_{вых}=0$, output voltage changes only upwards from this level, regardless of input pulse polarity (Figure IV.14c). Given bidirectional zero clamping $U_{вых}=0$, zero lower clamping results from positive pulse action, while zero upper clamping results from negative pulse action (Figure IV.14d).

Just as in unidirectional clamping, bidirectional clamping may occur not only at zero, but also at the positive or negative level.

Capacitor C must discharge rapidly in some direction upon cessation of the input pulse during bidirectional clamping, depending on the capacitor C voltage sign. If the discharge constant for any discharge current direction $\tau_p \ll t_и$, the discharge essentially ceases during resting time and, at onset of the subsequent pulse, $u_{вых} = \underline{U}_{вых} = 0$. Therefore, a bidirectional clamp comprises two unidirectional clamps, one which accomplishes lower clamping and the other which accomplishes upper clamping at the identical level.

The charging circuit time constant must be great $\tau_з \gg t_и$ so that pulse shape distortions are minimal. Since charging current may flow in one direction or the other depending on pulse polarity, both clamps must be blanked simultaneously when pulses are active. Strobe pulses generated by a special circuit blank clamp tubes at this time. Strobe pulse amplitude must be such that tubes are blanked during maximum input voltage magnitude $U_{вх}$, while their duration must equal output pulse duration $t_и$. Bidirectional clamps sometimes are called synchronous since strobe pulses must act in synchronization with input voltage pulses.

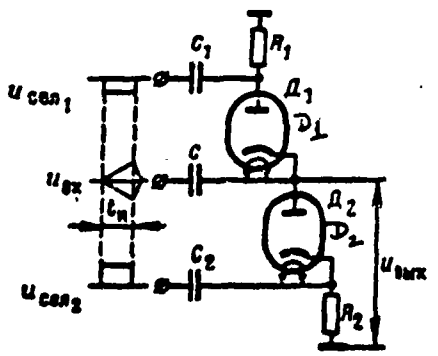

Figure IV.15. Bidirectional Diode Clamp.

We will examine a synchronous (bidirectional) clamp assembled from two /167 diode clamps (Figure IV.15). Diode D_1 accomplishes zero lower clamping, while diode D_2 accomplishes zero upper clamping.

Both diodes are blanked synchronously by strobe pulses of varying polarity, but of identical amplitude and duration, while input pulses are active. Diode D_1 is blanked by negative pulse $u_{ce.1}$ supplied to its plate across transient network R_1C_1. Diode D_2 is blanked by positive pulse $u_{ce.2}$ supplied to its cathode across transient network R_2C_2. Strobe pulse $U_{ce.1} = U_{ce.2}$ amplitude must be greater than $U_{вх}$ in order that diodes cut off reliably. Here, for any input voltage pulse polarity, capacitor C charges across the high input resistance of the subsequent stage with large time constant $\tau_з \gg t_и$. During resting times, both diodes are open and, depending on the residual voltage sign, capacitor C rapidly discharges across network R_1D_1 or R_2D_2 (resistances R_1 and R_2 must not be large). Zero initial level $U_{вых} = 0$ is clamped as a result.

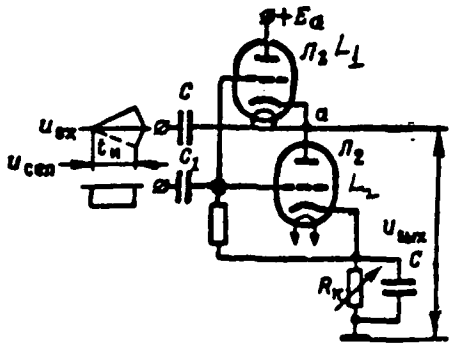

Figure IV.16. Bidirectional Triode Clamp.

A synchronous (bidirectional) clamp assembled on two triodes is depicted in Figure IV.16. Triode L_1 accomplishes lower clamping, while L_2 accomplishes upper clamping.

Tubes L_1 and L_2 and resistance $R_к$ form a voltage divider across which current i_0 flows. Here, output voltage $\underline{U}_{вых}$ clamping level is determined by potential of point a relative to "ground."

Value $\underline{U}_{вых}$ changes slightly if tube L_1 or L_2 internal resistance changes (for example, when they are replaced or E_a changes). Actually, L_1 in the initial mode may be looked upon as a cathode follower, with L_2 serving as its cathode load. Therefore, a change in L_1 or L_2 internal resistance is compensated for by a corresponding change in L_1 grid bias. As a result, the voltage drop across L_2 and voltage $\underline{U}_{вых}$ approximately are constant.

The requisite $\underline{U}_{вых}$ value is established by variable resistance $R_к$, making it possible to change current i_0.

Negative strobe pulses $u_{стр}$ supplied to tube grid simultaneously cut /168 off both tubes while input pulses are active. Therefore, charging circuit time constant $\tau_з \gg t_и$ is great at any input pulse polarity. Both tubes are open during resting times and, depending on polarity of the voltage to which capacitor C is charged over time $t_и$, it will discharge rapidly, either across tube L_2 and resistance $R_к$ or across tube L_1 and plate voltage source.

Voltage $u_{вх}$ initial level change does not depend on clamping level $\underline{U}_{вых}$, just as was the case for unidirectional clamp circuits.

CHAPTER V /169

LIMITERS

§ 1. GENERAL INFORMATION ON LIMITERS

Devices intended to constrain voltage magnitude at a certain level are referred to as limiters. Limiter output voltage follows the input voltage shape only until $u_{вх}$ reaches a certain predetermined level, after which $u_{вых}$ remains constant.

Clipping threshold (of output voltage) $u_{вых}$ is the term applied to the input voltage value, which, when achieved, still does not influence $E_н$ magnitude, i. e., a constraint is reached. The constant output voltage level maintained upon input voltage attainment of clipping threshold $E_с$ is referred to as clipping level (of output voltage) U_0*.

There are three basic limiter types -- upper, lower, and clipper-limiter. Limiter action, given these limiter types and varied $E_с$ and U_0 values, is explained

*The terms clipping threshold and level often are used interchangeably relative both to input and to output voltage. Here, each time one must stipulate which specific voltage this term refers to. The definitions we use for these terms, first, avoid the necessity for such stipulations, and, second, are more correct in essence (threshold -- input signal critical value, level -- output signal fixed value).

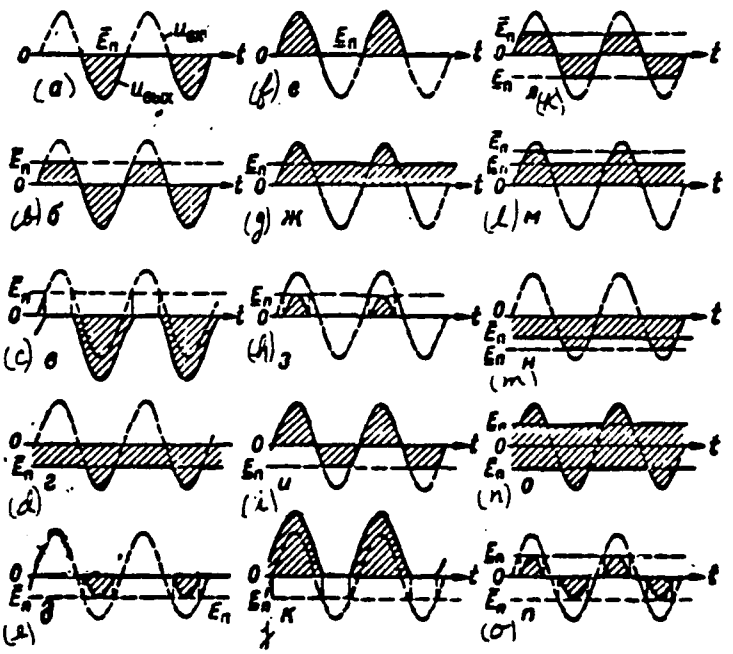

Figure V.1. Limiter Action (dashed line depicts $u_{вх}$, solid line depicts $u_{вых}$).

Upper Limiting: (a) [illegible] (b) [illegible] (c) [illegible]

(d) [illegible] (e) [illegible]

Lower Limiting: (f) [illegible] (g) [illegible] (h) [illegible]

(i) [illegible] (j) [illegible]

Bidirectional "External" Limiting: (k) [illegible]

(l) [illegible] (m) [illegible]

Bidirectional "Internal" Limiting: (n) [illegible]

(o) [illegible]

in Figure V.1 using sine-wave input voltage limiting as our example. In Figure V.1 and in future, we will designate upper and lower clipping threshold as $\bar{E}_п$ and $\underline{E}_п$, and upper and lower clipping levels as $\bar{U}_0$ and $\underline{U}_0$.

The input voltage portion lying below clipping threshold $u_{вх} < \bar{E}_п$, when $u_{вх} \geqslant \bar{E}_п$, is reproduced at output during upper limiting and then $u_{вых} = U_0 = \text{const}$ (Figure V.1a—e).

The input voltage portion lying above clipping threshold $u_{вх} > E_н$, when $u_{вх} \leqslant \underline{E}_н$, is reproduced at output during lower limiting and then $u_{вых} = U_0 = \text{const}$ (Figure V.1f--j).

Both upper limiting with threshold $\bar{E}_н$ and lower limiting with threshold /170 $\underline{E}_н$ occurs during bidirectional limiting (Figure V.1k--o). If $\bar{E}_н > \underline{E}_н$ here, then the input voltage portion trapped between clipping thresholds $\bar{E}_н > u_{вх} > \underline{E}_н$ is reproduced at output. Limiting in this instance may be referred to as "external" (Figure V.1k--m). If $\bar{E}_н < \underline{E}_н$, the input voltage portion lying above the upper and below the lower clipping threshold is reproduced at output. In this instance, limiting may be referred to as "internal" (Figure V.1n--o).

In each instance, the clipping threshold value may be zero (Figure /171 V.1a, f), positive (Figure V.1b, c, g, h), or negative (Figure V.1d, e, i, j). Both thresholds $\bar{E}_н$ and $\underline{E}_н$ may have different (Figure V.1k, n, o) and identical (Figure V.1l, m) polarity, but always $\bar{E}_н \neq \underline{E}_н$.

Clipping level U_0 value may be determined either by clipping threshold ($U_0 = E_н$ in Figure V.1a, b, e--g, i, k--n) or independently supplied ($U_0 = 0$ where $E_н = 0$ in Figure V.1c, d, h, j, o).

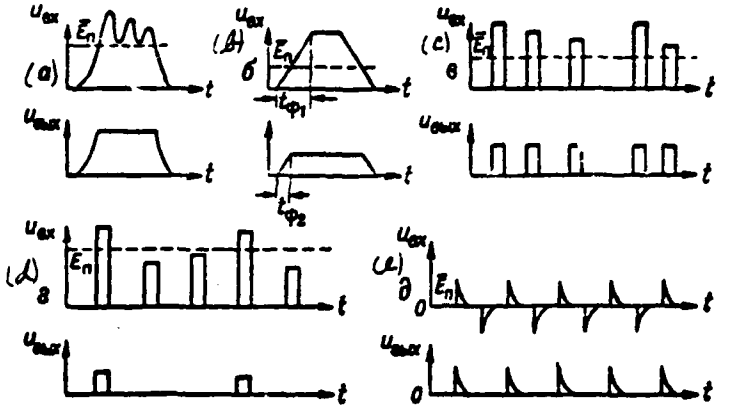

Figure V.2. Basic Limiter Uses: (a) -- Shaping a flat pulse tilt; (b) -- Reduction in pulse rise time; (c) -- Obtaining constant pulse amplitude; (d) -- Amplitude oulse selection; (e) -- Polarity pulse selection.

Limiters are used for the following purposes in RLS pulse devices:

-- for shaping a flat pulse tilt (Figure V.1a), in particular for obtaining pulses of almost trapezoidal shape from sinusoidal voltage (Figure V.1k);

-- for pulse rise time reduction (Figure V.2b);

-- for pulse amplitude stabilization -- obtaining pulses of strictly-constant amplitude from pulses of varied amplitude (Figure V.2c);

-- for amplitude pulse selection (Figure V.2d);

-- for polarity pulse selection (V.2e).

Two operating modes varying in principle always may be identified in any limiter:

-- transfer mode, when input voltage without distortions is reproduced at limiter output (no limiting occurs); here, $u_{вых} = K u_{вх}$, where /172 $K = \frac{\Delta u_{вых}}{\Delta u_{вх}} = \text{const} \neq 0$ -- limiter derivative gain outside the limiting area; if $K > 1$, then, in the transfer mode, the limiter amplifies input voltage, i. e., it operates as an amplifier-limiter;

-- limiting mode, when output voltage constantly $u_{вых} = U_0 = \text{const}$ and will not depend on value $u_{вх}$; since $\Delta u_{вых} = 0$ here, then derivative gain in the limiting area $K' = 0$; the more precise the latter equality, the more strict the limiting.

Thus, ideal limiter value K must change with a jump from a certain infinite value to zero when input voltage reaches the clipping threshold. This signifies that the limiter characteristic -- the curve of relationship $u_{вых} = \varphi(u_{вх})$ -- must materially be nonlinear and be represented by a broken line having a sloping sector corresponding to the transfer mode ($K = \text{const} \neq 0$) and a horizontal sector corresponding to the limiting mode ($K' = 0$).

Characteristics of three limiter types are depicted in Figure V.3 as /173 examples, as is their action in accordance with Figure V.1b, i, k).

EXERCISE V.1

a) How must unidirectional limiters be changed for a change in clipping threshold $E_з$ and for a change in clipping level U_0?

b) Plot limiter characteristics causing the limiting in accordance with Figure V.1a, e, g, o). (Page 468)

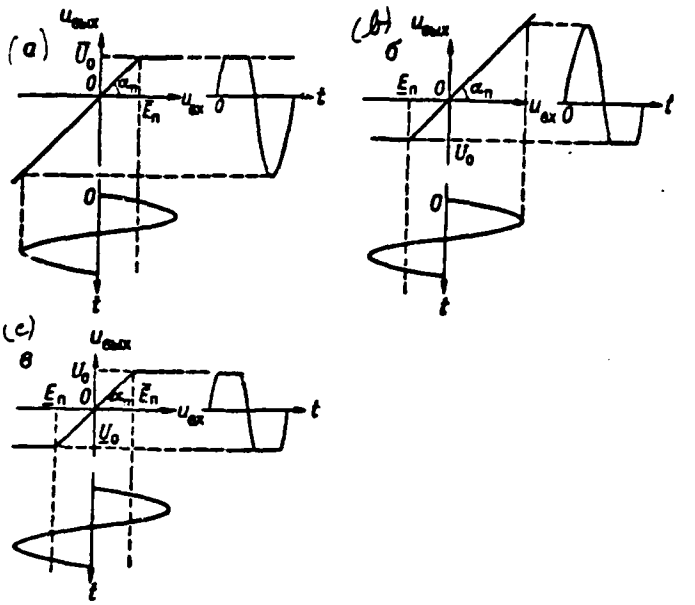

Figure V.3. Limiter Characteristics and Action: (a) — Upper where $\bar{E}_n - \bar{U}_0 > 0$; (b) — Lower where $\underline{E}_n - \underline{U}_0 < 0$; (c) — "External" Clipper-Limiter where $\bar{E}_n - \bar{U}_0 > 0$; $\underline{E}_n - \underline{U}_0 < 0$.

A limiter must include a nonlinear element, which radically changes its resistance when input voltage attains clipping threshold E_n in order to obtain a broken characteristic. Tube or semiconductor diodes and triodes, as well as multigrid tubes (pentodes), are used in this capacity.

Nonlinear elements are categorized by type, method of connection, and operating mode:

-- series diode limiters;
— parallel diode limiters;
— grid limiters;
-- plate limiters with plate current lower cut-off;
-- plate limiters with plate current upper cut-off;
— transistor limiters.

§ 2. DIODE LIMITERS

1. General Notes

The operating principle of diode limiters (just as that of clamp circuits) is founded on the electrical valve-like actions of a diode -- to pass current in one direction only, from plate to cathode. Tube and semiconductor diode circuits and operating principle do not differ and, therefore, will be examined together. We will recall that direct resistance R_d (open diode resistance in the area $u_a>0$) for most tube diodes comprises 100--1,000 ohms, while back resistance R'_d (closed diode resistance in the area $u_a<0$) comprises hundreds of megohms; $R_d = 1 \div 500$ ohms and $R'_d = 0.1 \div 10$ megohms for semiconductor diodes.

An idealized diode characteristic is similar to upper or lower limiter characteristics (Figure V.3a, b) since it has one break. Therefore, only unidirectional limiting is possible with one diode. Limiting type (upper or lower) will depend on direction of diode connection. The limiter characteristic (break point) needs to be displaced along the horizontal ($u_{вх}$ axis) or vertical /174 ($u_{вых}$ axis), respectively, to obtain non-zero clipping thresholds and levels. Outside bias sources E are introduced into the limiter circuit for this purpose.

A clipper-limiter characteristic (V.3c) must have two breaks, requiring mandatory use of two diodes connected in opposition. Here, one diode provides upper limiting, while the other provides lower limiting.

Thus, a diode limiter circuit includes a diode (or two diodes), resistance for requisite voltage drops, and outside bias sources supplying clipping threshold and level values.

There are two types of limiters, depending on the method of diode connection relative to load impedance (limiter output terminals):

-- if the diode is connected in series with load impedance, then it is called a series diode limiter;

-- if the diode is connected in parallel to load impedance (i. e., to limiter output network), then it is called a parallel diode limiter.

Since diodes do not have amplifying properties, then $K<1$ for diode limiters. Therefore, diode limiter output voltage amplitude always is less than input voltage amplitude, while, in principle, $u_{вых}$ porch steepness may not exceed that of $u_{вх}$.

2. Series Diode Limiters

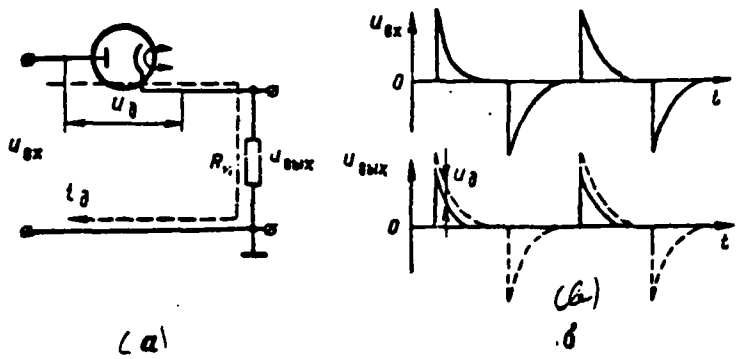

Figure V.4. Lower Series Diode Limiter Circuit and Voltage Curves For Zero Clipping Threshold and Level ($E_н=U_0=0$).

The simplest series diode limiter circuit is depicted in Figure V.4. Limiter output voltage equals voltage drop across load impedance $R_н$ arising due to diode current passage:

$$u_{вых} = u_{R_н} = i_д R_н, \tag{V.1}$$

i. e., it arises only when the diode will conduct.

The circuit operates in the following manner.

Transfer mode. The diode opens when $u_{вх}>0$ and voltage at limiter output will equal

$$u_{вых} = i_д R_н = \frac{u_{вх}}{R_д + R_н} R_н = \frac{u_{вх}}{1 + \frac{R_д}{R_н}}. \tag{V.1a}$$

Value $u_{вых}$ obtained is less than value $u_{вх}$ by the magnitude of the voltage drop across the open diode $u_д = i_д R_д$ (according to Kirchhoff's second law $u_{вых} = u_{вх} - u_д$).

A decrease in magnitude $u_д$ requires use of diodes with slight internal resistance $R_д$ and reduction of current in the limiter network $i_д = \frac{u_{вх}}{R_д + R_н}$, i. e., an increase in load impedance $R_н$. Therefore, the following inequality must be satisfied /175 in series diode limiters

$$R_н \gg R_д. \tag{V.2}$$

Here, limiter gain in the transfer mode approaches its maximum value

$$K = \frac{1}{1 + \frac{R_д}{R_н}} \approx 1 \quad \text{and} \quad u_{вых} \approx u_{вх}.$$

Limiting mode. The diode is closed when $u_{вх} < 0$, current $i_д = 0$, and there is no voltage at circuit output $u_{вых} = 0$.

The action of this limiter when bipolar exponential pulses are supplied to its input is depicted in Figure V.4b, while its action when sinusoidal voltage is supplied (without considering $u_д$) is depicted in Figure V.1f. Thus, the limiter will place a lower bound on input voltage with zero clipping threshold and level: $\underline{E}_п = 0, \underline{U}_о = 0$.

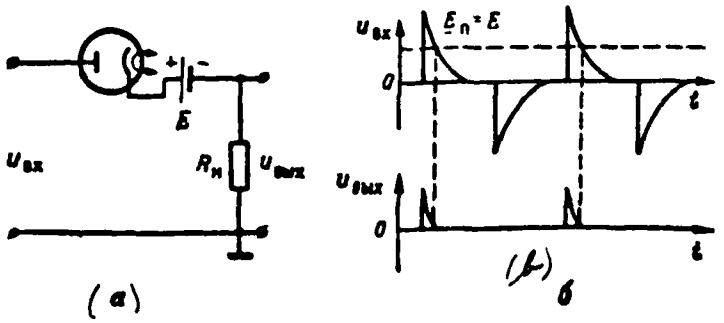

Figure V.5. Lower Series Diode Limiter Circuit and Voltage Curves For Positive Clipping Threshold and Zero Clipping Level ($\underline{E}_п > 0$; $\underline{U}_о = 0$) .

Fixed bias source E must be introduced into the limiter in such a way that it not enter the output network in order to obtain the non-zero clipping threshold, but, as usual, the zero clipping level. We will use the circuit depicted in Figure V.5a as our example. Resultant emf in this circuit will equal the algebraic sum of $u_{вх}$ and E, which will displace the limiter characteristic along the horizontal. We will examine how this will change limiter operation.

Transfer mode. Bias constrains diode opening for source E polarity connection depicted in Figure V.5a. Therefore, the diode will conduct only when $u_{вх}>E$ /176 and, if $R_н \gg R_д$, then we will get

$$u_{вых} = u_{Rн} = i_д R_н = \frac{u_{вх} - E}{R_н + R_д} R_н = \frac{u_{вх} - E}{1 + \frac{R_д}{R_н}} \approx u_{вх} - E > 0,$$

output voltage, remaining positive, will decrease by the magnitude of the bias.

Limiting mode. The diode will be closed when $u_{вх}<E$ and, as was the case in the previous circuit, $u_{вых}=0$. Consequently, lower limiting will occur with positive clipping threshold and zero clipping level: $E_н=E>0$, $U_з=0$. Limiter action when bipolar exponential pulses are supplied to its input is depicted in Figure V.5b, while it action when sinusoidal voltage is supplied is depicted in Figure V.1h.

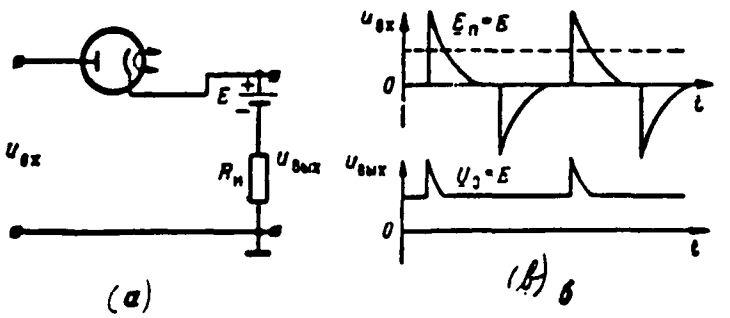

Figure V.6. Lower Series Diode Limiter Circuit and Voltage Curves For Positive Clipping Threshold and Level ($E_п=U_з>0$) .

Now, without changing source E polarity, we will transfer it to the limiter

output circuit. Then we will get the circuit depicted in Figure V.6a. As opposed to the previous circuit, output voltage will equal

$$u_{вых} = u_{R_н} - E. \qquad (V.3)$$

Therefore, the limiter characteristic will displace by magnitude E along the vertical. This, then, is the special feature of circuit operation.

Transfer mode. Since bias E, as usual, constrains diode opening, it will open, just as in the previous circuit, only when $u_{вх} > E$. Considering that bias E is positive relative to "ground," output voltage will turn out to equal (given $R_н \gg R_i$)

$$u_{вых} = u_{R_н} - E = \frac{u_{вх} - E}{R_i + R_н} R_н - E \approx u_{вх} - E + E = u_{вх}.$$

Limiting mode. The diode will be closed when $u_{вх} < E$ and $u_{вых} = U_о = E$. Consequently, as usual, in this case lower limiting will occur with positive clipping threshold, but now not with zero, but with positive clipping level $E_у = U_о = E > 0$. Limiter action when bipolar exponential pulses are supplied to its input is depicted in Figure V.6b, while it action when sinusoidal voltage is supplied is depicted in Figure V.1g.

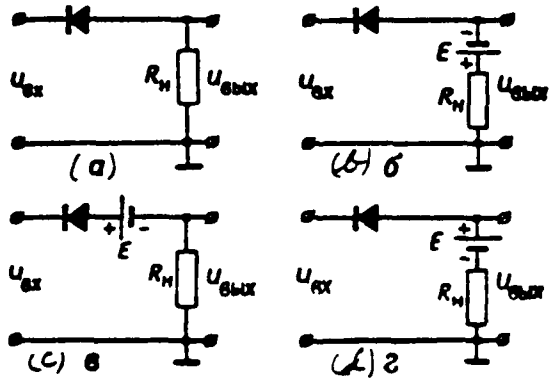

Figure V.7. Series Diode Limiter Circuits.

It is necessary to reverse bias source polarity (to connect it with a "minus" to diode cathode) to obtain a negative clipping threshold in the Figure V.5a and

V.6a circuits. This simultaneously will provide a clipping level sign change /178 for the Figure V.6a circuit. Limiter action in these cases will correspond to Figure V.1j and V.1i when sinusoidal input voltage is supplied to their input.

A change in diode connection direction suffices in order to obtain upper rather than lower limiting.

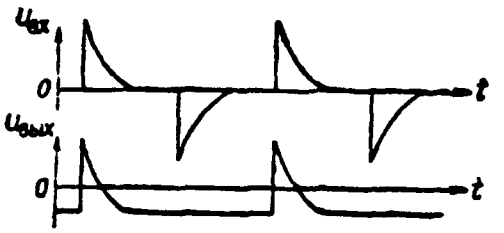

Figure V.8. For Exercise V.2b.

EXERCISE V.2

a) Characterize limiters depicted in Figure V.7. Point out for each circuit limiter type (upper, lower) and the E_0 and U_0 values. Find in Figure V.1 the curves which correspond to circuit operation.

b) Compile a series diode limiter circuit whose action would correspond to Figure V.8 when bipolar exponential pulses are supplied to its input. (Page 468)

As pointed out above, bidirectional limiting requires that a circuit comprise two unidirectional opposed limiters with $\bar{E}_n \neq \underline{E}_n$. One such circuit is depicted in Figure V.9a and comprises two series-connected diode limiters. The action of each limiter in the circuit was examined previously. If $R_2 \gg R_1$, then, in the first approximation, it was possible to look upon the action of both limiters independently and to consider that the first limiter sets a lower bound with negative threshold and level $\underline{E}_1 = \underline{U}_1 = -E_1$, while the second sets an upper bound with positive threshold and level $\bar{E}_n = \bar{U}_n = E_2$. Bidirectional "external" /179 limiting will occur as a result (see Figure V.1k).

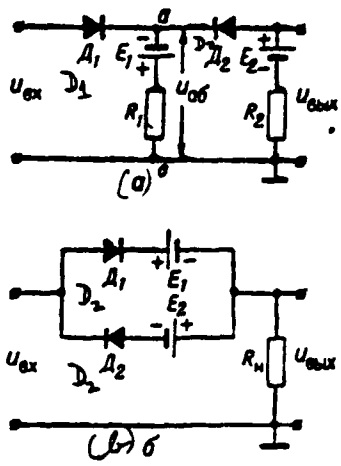

Figure V.9. Series Diode Clipper-Limiter.

If inequality $R_2 \gg R_1$ is not satisfied, it should be considered that current passing across diode D_2 influences the first limiter clipping threshold $E_п$. Actually, when diode D_1 is closed, diode D_2 is open by bias sources E_1 and E_2 operating in agreement. Therefore, the difference in potentials between points $а.\ б(u_{об})$ will be determined not only by bias E_1, but also by voltage drop across resistance R_1 when diode D_2 current i_{02} passes across it:

$$u'_{об} = u'_{R_1} - E_1 = i_{02}R_1 - E_1 = \frac{E_1 + E_2}{R_1 + R_2}R_1 - E_1 = \frac{E_2R_1 - E_1R_2}{R_1 + R_2}$$

$$(R_{д1} \ll R_1;\ \ R_{д2} \ll R_2).$$

Diode D_1 will open when $u_{вх} - u_{об} > 0$, i. e., $u_{вх} > u'_{об}$. Consequently, first limiter clipping threshold and level will equal

$$\underline{E}_п = \underline{U}'_0 = \frac{E_2R_1 - E_1R_2}{R_1 + R_2}.$$

Second limiter clipping threshold and level, as usual, will be determined by bias E_2:

$$\bar{E}_п = \bar{U}_0 = E_2.$$

Another clipper-limiter circuit comprising two parallel-connected series diode limiters with common load is depicted in Figure V.9b.

EXERCISE V.3

Analyze Figure V.9b circuit operation. Point out clipping threshold and level values and, in Figure V.1, find the curves corresponding to the operation of this circuit. (Page 470)

3. Parallel Diode Limiters

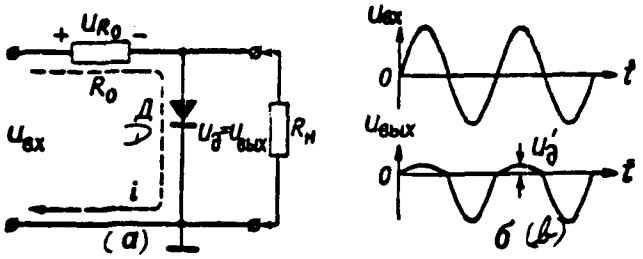

Figure V.10. Circuit and Voltage Curves for an Upper Parallel Diode Limiter With Zero Clipping Threshold and Level ($\bar{E}_п = 0$; $\bar{U}_з = 0$).

The simplest parallel diode limiter circuit is depicted in Figure V.10a. In addition to diode D, it includes limiting resistance R_0 having, as was pointed out earlier, principal significance. Limiter output voltage is formed across load impedance $R_н$ connected in parallel to the diode and, in accordance with Kirchhoff's second law, equalling

$$u_{вых} = u_д = u_{вх} - u_{R_0} = u_{вх} - iR_0 \qquad (V.4)$$

where $u_{R_0} = iR_0$ — voltage drop across resistance R_0.

Transfer mode. When $u_{вх} < 0$, the diode is closed and output voltage turns /180 out to be applied to series-connected resistance R_0 and $R_н$. Therefore,

$$u_{вых} = u_{вх} - u_{R_0} = u_{вх} - \frac{u_{вх}}{R_0 + R_н} R_0 = u_{вх} - \frac{u_{вх}}{1 + \frac{R_н}{R_0}} < u_{вх}. \qquad (V.5)$$

Value $u_{вых}$ is less than value $u_{вх}$ by the magnitude of voltage drop across

resistance R_0. In order to increase $u_{вых}$ (to decrease u_{R_0}), there is a requirement that

$$R_н \gg R_д \tag{V.6}$$

Then the limiter transfer constant in the transfer mode approximates its maximum value

$$K = \frac{1}{1 + \frac{R_д}{R_н}} \approx 1 \qquad \text{and} \qquad u_{вых} \approx u_{вх}$$

Limiting mode. Where $u_{вх} > 0$, the diode is open and its resistance $R_д$ is slight. Therefore, one may disregard shunting influence of resistance $R_н$ ($R_д \ll R_н$) and consider that input voltage is applied to series-connected resistances $R_д$ and R_0. Consequently,

$$u_{вых} = u_{вх} - u_{R_0} = u_{вх} - \frac{u_{вх}}{R_д + R_0} R_0 = u_{вх} - \frac{u_{вх}}{1 + \frac{R_д}{R_0}}. \tag{V.7}$$

In order to decrease $u_{вых}$ (to increase $u_{R_д}$), there is a requirement that

$$R_0 \gg R_д \tag{V.8}$$

Here, almost the entire voltage drop will occur across resistance R_0 and $u_{вых} \approx 0$.

Combining inequalities (V.6) and (V.8), we get the condition for resistance R_0 selection:

$$R_д \ll R_0 \ll R_н \tag{V.9}$$

It should be underscored that, since conducting diode internal resistance /181 is slight and may not equal zero, a certain input voltage portion equalling voltage drop $u_д$ across the open diode mandatorily will be reproduced at output during the limiting mode. Therefore, in principle, a parallel diode limiter may not provide strict limiting.

This circuit action is depicted in Figure V.10b where sinusoidal voltage is supplied to its input. In this case, upper limiting (not strict!) with zero clipping threshold and level will occur

$$\overline{E}_n = \overline{U}_0 = 0.$$

Bias source E also is introduced into the parallel diode limiter circuit to obtain non-zero clipping thresholds and levels; diode connection direction must be changed to accomplish the opposite type of limiting.

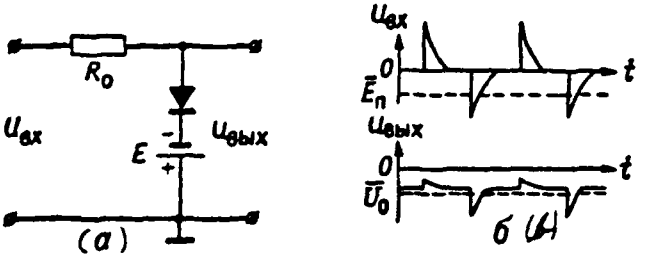

Figure V.11. Upper Parallel Diode Limiter Circuit and Voltage Curves With Negative Clipping Threshold and Level $(\overline{E}_n = \overline{U}_0 < 0)$.

We will use the circuit depicted in Figure V.11a as our example.

Transfer mode. Since bias E constrains diode cut-off, it closes only where $u_{вх} + E < 0$, i. e., where $u_{вх} < -E$. But, given a closed diode, the bias source does not influence output voltage magnitude (it is cut out) and $u_{вых} \approx u_{вх}$ (if $R_н \gg R_0$).

Limiting mode. Where $u_{вх} + E > 0$, i. e., $u_{вх} > -E$, the diode is open and

$$u_{вых} = u_{вх} - u_{R_0} = u_{вх} - \frac{u_{вх} + E}{R_0 + R_д} R_0 = \frac{u_{вх}}{1 + \frac{R_д}{R_0}} - \frac{E}{1 + \frac{R_д}{R_0}} \approx -E$$

(if $R_0 \gg R_д$).

Thus, upper limiting with negative and equal clipping threshold and level: $\overline{E}_n = -E$; $\overline{U}_0 = -E$ (due to open diode infinite resistance, clipping level is reduced /182

somewhat in absolute magnitude and limiting will not be strict). The action of this limiter when bipolar exponential pulses are supplied to its input is depicted in Figure V.11b.

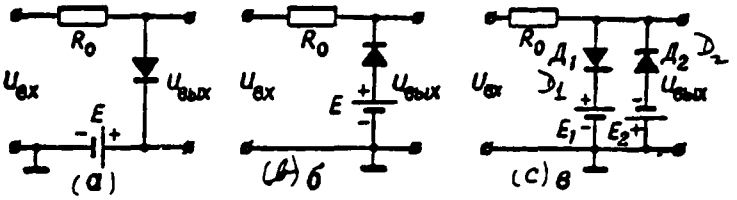

Figure V.12. Parallel Diode Limiter Circuits.

EXERCISE V.4

Analyze the operation and provide the characteristic of the limiters depicted in Figure V.12: for each, point out limiting type (upper, lower), clipping threshold and level values, and find the Figure V.1 curves corresponding to circuit operation. For simplicity, assume here that $R_д = \infty$; $R_д = 0$. (Page 470)

Parallel diode limiter and clamp circuits are similar to each other in the manner in which diodes are connected. This similarity sometimes leads to errors in determination of diode purpose when reading pulse circuits. In fact, limiter and clamp circuits and purposes are different. Voltage a-c component distortion (pulse amplitude reduction) will occur during limiting, while the voltage d-c component lost during passage across a transient R-C network changes (or is reestablished) in a clamp, while the a-c component (pulse amplitude, in particular) remains unchanged.

Parallel and series diode limiters also must be differentiated since their circuits, operating principle, and basic properties differ.

EXERCISE V.5

а) Draw two circuits, an upper parallel diode limiter where $E_д = U_0 = E > 0$ connected to transient R-C network output and a positive upper clamp where

$\overline{U}_{вых}=E>0$ connected to transient R-C network output. Point out two principal differences in these circuits.

b) Copy and fill in Table 1.

c) Draw a series and a parallel diode limiter circuit considering internal resistances of input voltage generator $R_г$ and bias source $R_и$ connected to the limiter output network. How do these resistances impact upon limiter operation?

(Page 471)

Table 1

Comparison Criteria	Diode Limiter Type	
	Series	Parallel
Circuit Characteristic Features		
When Will Limiting Occur (When is Diode Open, Closed)		
Limiting Quality (Strict, Not Strict)		
Basic Ratios in the Circuit and What They Provide (Improvement in the Transfer, Limiting Mode)		

4. Influence of Stray Capacitances

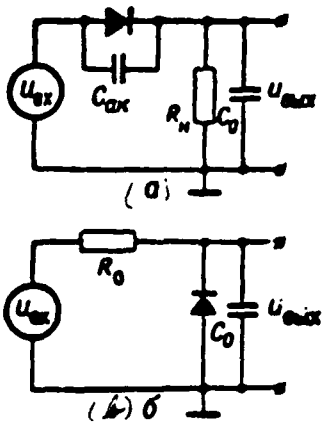

Figure V.13. For Calculation of Stray Capacitance Impact on Diode Limiter Operation

Stray circuit capacitances -- diode transfer capacitance $C_{дх}$, circuit capacitance $C_м$, and subsequent stage (load) input capacitance $C_{вх}$ -- may turn out to impact significantly when voltages with steep porches impact upon limiter operation. A series (a) and a parallel (b) upper limiter circuit with zero clipping threshold, considering stray capacitances, are depicted in Figure V.13.

$C_0 = C_м + C_{вх}$ for the first circuit, while $C_0 = C_{дх} + C_м + C_{вх}$ for the second circuit. We will assume that identical positive square-wave pulses, beginning with negative level $U_{вх} = -U''$ with amplitude $U_{вх} = U' + U''$, are acting upon the inputs of both circuits (Figure V.14a).

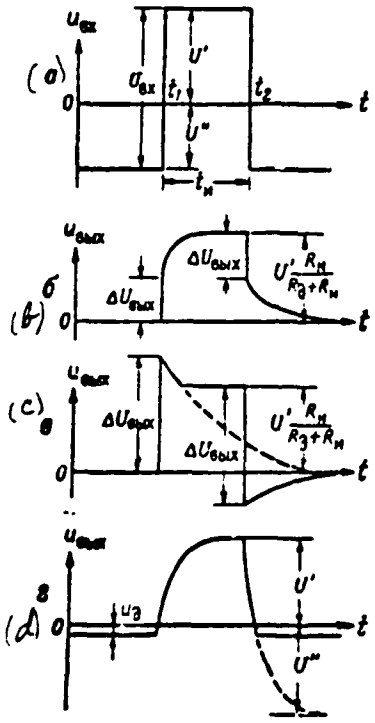

Figure V.14. Stray Capacitance Impact on Diode Limiter Operation: (a) — Input voltage; (b) and (c) — Series limiter output voltage; (d) — Parallel limiter output voltage.

Initially, we will examine stray capacitance impact on a series limiter. At moments t_1 and t_2, instantaneous voltage drops with amplitude $U_{вх}$ act upon circuit input. At these moments, one may disregard currents across the diode and resistance $R_н$ compared with currents in capacitances $C_{дх}$ and C_0 shunting

them. Consequently, voltage jumps $\Delta U_{вых}$, the magnitude of which will be determined by instantaneous charges across the arms of capacitive divider $C_{дк}$, C_0: /184 C_0: $\Delta U'_{вых} = U'_{вх}\frac{C_{ак}}{C_{дк}+C_к}$, will be transferred to circuit output. Depending on ratios U' and U" and $C_{дк}$, C_0, jump $\Delta U'_{вых}$ magnitude may be less or more than the magnitude of the positive portion of input voltage U' reproduced at output. The output voltage shape when $\Delta U_{вых}<U'$ is depicted in Figure V.14b, while that when $\Delta U_{вых}>U'$ is depicted in Figure V.14c.

In the first instance, at moment t_1 diode plate potential rises with a jump to value U', while cathode potential rises to magnitude $\Delta U_{вых}<U'$. Therefore, the diode turns out to be open and, following the jump across it, capacitance C_0 overcharge will occur to magnitude $U_{вых} = U'\frac{R_н}{R_н+R_д}$. Here, voltage $u_{вых}$ rises by an exponent with time constant $\tau_1 = \frac{R_д R_н}{R_д+R_н}(C_0+C_{ак}) \approx R_д(C_0+C_{ак})$. At moment t_2, diode plate potential decays with a jump by magnitude $U_{вх}$ and takes on value -U", while cathode potential decays by magnitude $\Delta U_{вых}<U'<U_{вх}$, the diode cuts off, and capacitance C_0 discharges across resistance $R_н$. Here, voltage $u_{вых}$ decays by an exponent with time constant $\tau_2 = R_н(C_0+C_{ак})$.

Since $R_н \gg R_д$, then $\tau_2 \gg \tau_1$ and, output pulse decay, the decay time of which will comprise $t_{сп} \approx 3\tau_2 = 3R_н(C_0+C_{ак})$, is stretched to the maximum degree. Therefore, if decay time is given, then condition $R_н < \frac{t_{сп}}{3(C_0+C_{ак})}$ puts an upper bound on load impedance magnitude, which satisfies condition (V.2), which places a lower bound on magnitude $R_н$.

In the second case, plate potential rises with a jump at moment t_1 to magnitude U', while cathode potential rises to magnitude $\Delta U_{вых}>U'$. Therefore, the diode turns out to be closed and, following the jump, capacitance C_0 will discharge across resistance $R_н$. Here, voltage . . decays by an exponent with time constant $\tau_1 = R_н(C_0+C_{ак})$ to magnitude $U''\frac{R_н}{R_д+R_н}$, when the diode opens. At moment t_2, /185 diode plate potential decays with a jump by magnitude $U_{вх}$, while cathode potential decays by magnitude $\Delta U_{вых}<U'_{вх}$ and the diode closes. Since $\Delta U'_{вых}>U''$, then negative voltage arises at output. This voltage disappears by an exponent with time constant $\tau_2 = R_н(C_0+C_{ак})$ in connection with capacitance C_0 discharge across resistance $R_н$.

Diodes with slight capacitance $C_{дд}$ (here, magnitude of $\Delta U_{вых} = U_{вх} \frac{C_{дд}}{C_0 + C_{дд}}$ jumps

decreases) must be used in this case to decrease resultant stray "spikes" $u_{вых}$.

We will shift to the parallel limiter circuit whose output voltage shape is depicted in Figure V.14d. At moment t_1, the diode is cut off and integrator R_0, C_0 is formed due to action of positive drop $U_{вх}$. Therefore, voltage $u_{вых} = u_{C_0}$ will rise by an exponent with time constant $\tau = R_0 C_0$ from level $u_д \approx 0$ to value U'. At moment t_2, capacitance recharging will begin across resistance R_0 (the diode is closed) due to action of negative drop $U_{вх}$. Voltage $u_{вых}$ will begin to decrease by an exponent with the same time constant $\tau = R_0 C_0$, but at a high rate, since it will strive towards value -U". However, when $u_{вых} = 0$, the diode opens, capacitance C_0 will turn out to be shorted by slight resistance $R_д$, voltage across it will take on value $u_д$, and it will not change further. Therefore, rise time exceeds decay time and equals $t_ф \approx 3\tau = 3R_0 C_0$. If value $t_ф$ is given, then condition $R_0 \leqslant \frac{t_ф}{3(C_{дд} + C_м + C_{вх})}$, which satisfies condition (V.8), will place a bound on resistance R_0 magnitude.

EXERCISE V.6

What diode limiter type and what conditions make it possible to reduce the influence of stray capacitances to a minimum? (Page 472)

5. Computing Actual Diode Characteristics. Diode Limiter Compensated Circuits

Differences between actual and ideal diode characteristics manifest themselves when voltages slight in magnitude are limited (see Figure III.2b).

The influence of a diode actual characteristic (Figure V.15a) on operation of a series diode lower limiter without outside bias sources when bipolar square pulses are clipped (Figure V.15b) is depicted in Figure V.15. "Premature" diode opening when $u_{вх} = E_{ф} < 0$ will lead to a change in clipping threshold and level (we will get $\underline{E}_з = E_ф < 0$, $\underline{U}_0 = I_0 R_д$) instead of $\underline{E}_з = \underline{U}_0 = 0$), while initial characteristic sector nonlinearity causes nonlinear $u_{вых}$ distortions near the clipping level /186 (Figure V.15c). Conditional bias source $E_{ск}$ applied with a "minus" to cathode,

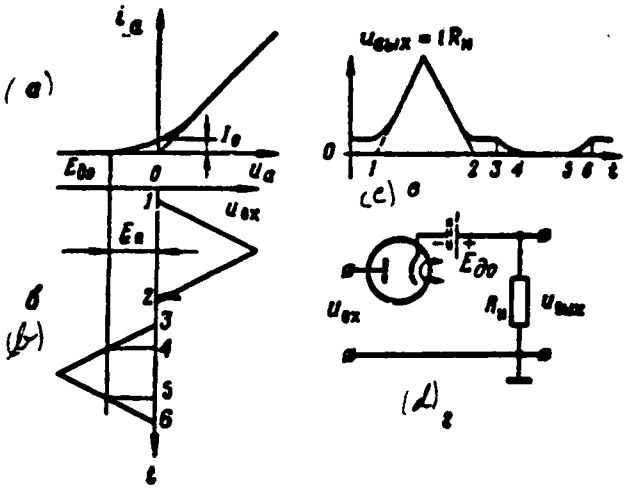

Figure V.15. For Computation of Tube Diode Characteristics.

should be introduced into the limiter circuit for computation of actual diode cut-off voltage (Figure V.15d).

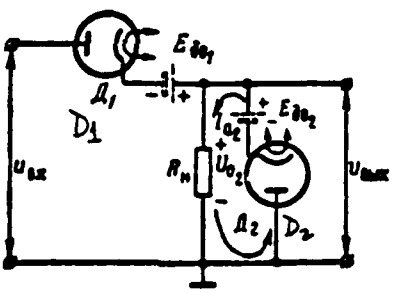

Figure V.16. Compensated Series Diode Limiter Circuit.

It has been established that a 10% filament voltage change biases the actual diode characteristic approximately 0.1 V "along the horizontal." Characteristics also may be biased approximately ± 0.25 V "along the horizontal" due to diode parameter spread and diode aging. All these instabilities equate to corresponding "bias" $E_{\partial 0}$ magnitude changes in Figure V.15d and, consequently, will lead to stray clipping threshold and level changes. A second, compensating, diode connected so that, given clipped diode zero drift, compensated diode zero drift will act in the opposite

direction, is introduced into the limiter circuit to combat these phenomena. A series diode lower limiter with zero clipping threshold compensated in this /187 manner is depicted in Figure V.16. The clipping threshold does not change during simultaneous and identical zero drift in both diodes (a change in fictitious voltages $E_{\phi 01}$ and $E_{\phi 02}$) since, as long as clipper diode D_1 is closed, compensating diode D_2 initial current creates voltage drop $U_{D2} = E_{\phi 02}$ across resistance $R_н$ equal to and acting in opposition to "bias" $E_{см1}$. The second half of the tube -- a dual diode, the first half of which is a clipper diode (this also explains the approximate equality of clipper and compensating diode zero drifts) — essentially is used as a compensating diode. However, clipping threshold stability increases only by a factor of 5—10 due to incomplete diode D_1 and D_2 identity. Compensated diode limiter circuits with non-zero clipping thresholds operating on the identical principle are depicted in Figure V.17.

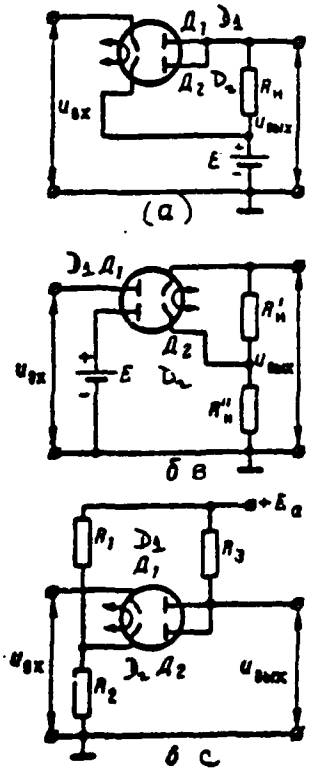

Figure V.17. Compensated Diode Limiter Circuits.

EXERCISE V.7

Analyze the operation of the Figure V.17 circuits. Indicate limiter type in each and explain the compensating diode action. (Page 472)

It should be kept in mind when semiconductor diodes are used that their parameters will depend on temperature to a great degree. Thus, germanium diodes operate stably at temperatures below 75° C, while silicon diodes operate stably at temperatures below 100--150° C. At higher temperatures, the back resistance of these circuits rapidly decays and limiter operation is disrupted.

6. Influence of a Transient R-C Network Connected at Limiter Input

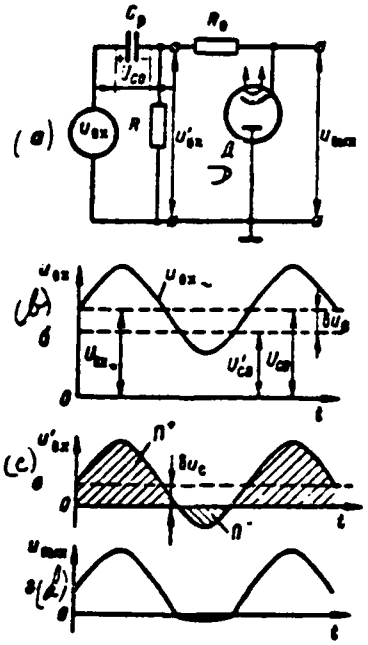

Figure V.18. Clipping Threshold Bias Due To Isolating Capacitor Influence.

Accumulation of charges in the isolating capacitor (see Chapter II, § 5) significantly may distort limiter operation if voltage at limiter input passes /188 across a transient R-C network in order to isolate d-c and a-c components. We

will explain this using a parallel diode lower limiter with zero clipping threshold and level as our example (Figure V.18a). We will assume that isolating capacitor C_p under input voltage action was charged in the steady-state mode to voltage U_{C0}. Then, it is evident that this voltage will act as additional (dynamic) bias $E=-U_{C0}$ applied to the diode, which will lead to a change in clipping threshold (but not level!). Input voltage and circuit parameters determine voltage U_{C0} polarity and magnitude.

We will assume that voltage $u_{вх}$, having positive d-c component $U_{вх=}$ and sinusoidal a-c component $u_{вх\sim}$: $u_{вх}=U_{вх=}-u_{вх\sim}$ is supplied to circuit input (Figure V.18b). We propose to use the limiter to place a lower bound on the a-c component with $E_{п}=U_{д}=0$. If capacitor C_p in the steady-state mode is charged to voltage $U_{C0}=U_{вх=}$ (as will occur in a linear transient R-C network), then d-c component action would be compensated for fully, only the a-c component ($u_{вх}=u_{вх}-U_{C0}=U_{вх=}+u_{вх\sim}-U_{вх=}=u_{вх\sim}$) would be applied to limiter input, and the problem would be solved. But, due to limiter influence, the transient network becomes nonlinear. Actually, under the action of positive half-wave component $u_{вх\sim}$, capacitor C_p additionally will be charged across resistance R (diode closed) and, during action of the negative half-wave, it will discharge across two parallel branches: resistance R, resistance $R_д$, and diode. Resultant network discharge resistance $R_р=\frac{RR_д}{R+R_д}$ is less than charging network resistance $R_з=R$ (we assume for simplicity that $R_д=0$, $R_г=0$). Therefore, the steady-state voltage value across the capacitor will decrease by certain magnitude δu_C: $U_{C0}=U_{вх=}-\delta u_C$ (Figure V.18b) and voltage at limiter output rises by that amount: /189
$u_{вх}=u_{вх}-U_{C0}=u_{вх\sim}+\delta u_C$ (Figure V.18c).

We will recall that value δu_C is determined from condition (II.50) for nonlinear transient R-C network output voltage in the steady-state mode

$$\frac{\Pi^+}{\Pi^-}=\frac{R_з}{R_р}.$$

As a result, a-c component $u_{вх\sim}$ will have a lower bound, not at zero, but at negative clipping threshold value $E_д=-\delta u_C$ (a portion of negative half-waves $u_{вх\sim}$ will be reproduced at limiter output). Output voltage clipping level will remain zero since $u_{вых}=u_д\approx 0$ when the diode is open (Figure V.18d).

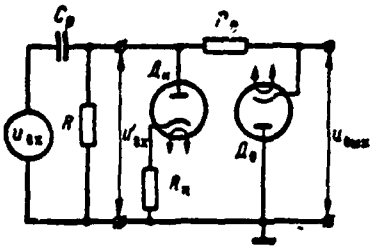

Figure V.19. Method of Equalizing Isolating Capacitor Charge and Discharge $(R_н = R_0)$.

It is sufficient in this instance to make the resistance in capacitor $C_р$ charging and discharging networks identical (i.e., due to limiter influence, to convert the transient R-C network from nonlinear to linear) in order to avoid a clipping threshold change. A circuit in which compensating diode $Д_н$ with resistance $R_н = R_0$ is connected in parallel to limiter input to provide equality $R_1 = R_р$ is depicted in Figure V.19. Diode $Д_н$ opens when $u'_{вх} > 0$ (in the transfer mode, when the limiter diode is closed), creating an additional branch for capacitor $C_р$ charging current across resistance $R_н$. As a result, we will get $R_р = \frac{RR_н}{R + R_н} = R_р = \frac{RR_0}{R + R_0}$, $\Delta u_C = 0 (П_+ = П_-)$, $u'_{вх} = u_{вх-}$, and sinusoidal voltage will be limited with the given zero threshold. However, this method of eliminating isolating capacitor influence only may be used if voltage $u_{вх}$ at limiter input (R-C network output) can be changed symmetrically relative to the zero level (i. e., does not have an d-c component). If pulse voltage having a d-c component that does not equal zero will be subject to limiting, then isolating capacitor influence may be eliminated using a more standard device -- a clamp circuit connected at transient R-C network output (see Chapter IV).

EXERCISE V.8

Pulse voltage picked off multivibrator plate load (Figure V.20b), where $E < U_{вх}$, is supplied to a limiter circuit with a transient R-C network /190 (Figure V.20a). Draw the circuit output voltage curve in the steady-state mode considering capacitor $C_р$ influence. Select the clamp type whose connection eliminates the transient network influence. Redraw the Figure V.20a circuit, having included the clamp circuit selected in it and draw the output voltage curve. (Page 473)

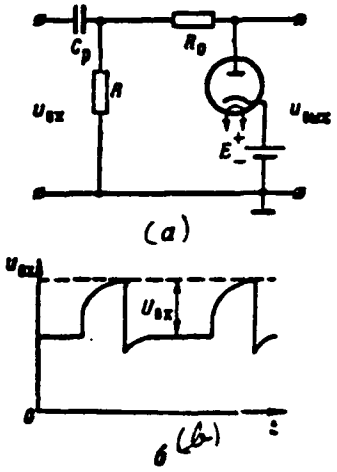

Figure V.20. For Exercise V.8.

Load impedance $R_н$ may serve as transient R-C network resistance R when parallel diode limiters are used. This is ruled cut for series diode limiters since the diode current a-c component in them is closed across generator $u_{вх}$ and installation of an isolating capacitor breaks this network. Actually, if capacitor $C_р$ in a series limiter circuit is connected to diode plate, then it will charge across the diode to maximum voltage, following which capacitor discharge will turn out to be impossible (the diode is closed to discharging current) and current will not pass across limiter load $R_н$. If capacitor $C_р$ is connected to diode cathode, then it cannot charge itself. Therefore, cathode potential will increase to value $U_{вх}$ and the diode cannot open. In both cases, a series diode limiter will not operate.

§ 3. MULTIELECTRODE-TUBE LIMITERS

1. General Notes

Derivative gain in the transfer mode is $K>1$ for multielectrode tube limiters as opposed to diode limiters, i. e., input voltage amplification occurs along with limiting. This makes it possible, first, to obtain output voltage amplitude, in spite of its limiting, greater than input amplitude and, second,

and especially significant, to increase output voltage porch steepness by a factor of K compared to input voltage porch steepness. Clipping amplifier output voltage is picked off the plate load. Therefore, clipping amplifiers invert input voltage phase.

Multielectrode tube limiting may be obtained due to appearance of control grid current (grid limiters), due to dynamic transfer characteristic lower knee (plate current lower cutoff limiting), and due to the upper knee of this /191 characteristic (plate current lower cutoff limiting).

2. Grid Limiters

Control grid current i_g flowing across the grid--cathode path from grid to cathode arises if triode control grid potential exceeds cathode potential ($u_{gk}>0$). The relationship between grid current and voltage u_{gk} is analogous to the diode characteristic (see Figure III.2 and III.3). Therefore, one may look upon the grid--cathode path as a diode which opens when $u_{gk}>0$ (the triode grid is this diode's plate, while the triode cathode is its cathode).

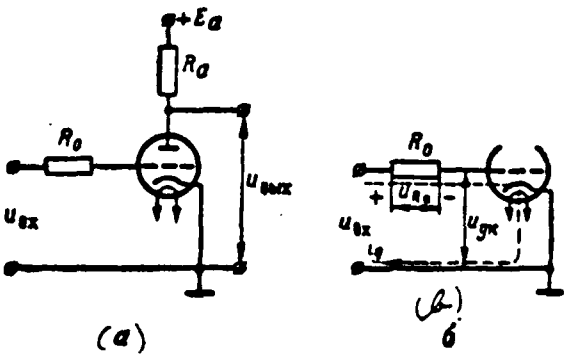

Figure V.21. Grid Limiter Circuit.

The simplest triode grid limiter circuit is depicted in Figure V.21. Presence of limiting resistance R_0 connected in series from the control grid to the tube input network is a characteristic feature of this circuit. The grid limiting process also occurs in this same network, shown separately in Figure V.21b. Actually,

a grid limiter input network circuit does not differ from a parallel diode upper limiter with zero clipping threshold and level (see Figure V.10). Limiting resistance R_0, in accordance with ratio (V.6), must be selected from condition $R_0 \gg r_{gk}$, where r_{gk} -- grid--cathode conducting path resistance. Resistance r_{gk} for most triodes comprises a magnitude of approximately 1 k Ω. Therefore, limiting resistance R_0 is selected usually in a range of 100 k Ω to 1--2 M Ω. The Figure V.21b diode limiter output voltage is voltage u_{gk} acting between triode grid /192 and cathode:

$$u_{gk} = u_{вх} - u_{R_0},$$

where

$$u_{R_0} = i_g R_0.$$

This voltage is amplified and inverted in the tube plate network. Thus, one may look upon a grid limiter as a combination parallel diode upper limiter and a plate-load amplifier.

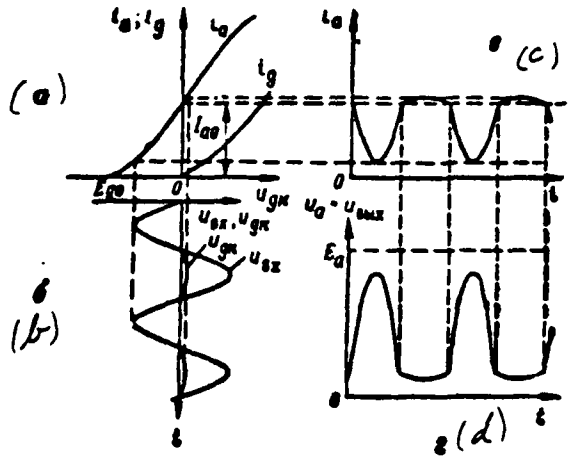

Figure V.22. Grid Limiter Operating Principle.

Grid limiter operation, given sinusoidal voltage limiting, is explained in Figure V.22. When negative half-cycles $u_{вх}$ $u_{gk} < 0$ are active, $i_g = 0$ ("diode" closed) and $u_{gk} = u_{вх}$ since $u_{R_0} = i_g R_0 = 0$. Grid current (Figure V.22a) appears

when positive half-cycles $u_{вх}$ are active and $u_{gk} \approx 0$ since almost the entire voltage drop in the input network occurs across resistance $R_0 \gg r_{gk}$. Therefore, positive half-cycles "are clipped" at the zero level (Figure V.22b). Triode plate current changes in accordance with the voltage u_{gk} law if voltage u_{gk} clipped in this manner changes within the bounds of the transfer characteristic linear sector, while maximum plate current value corresponds to value $u_{gk} \approx 0$ and equals I_{ao} (Figure V.22c). Limiter output voltage $u_{вых} = u_a = E_a - i_a R_a$ changes out of phase with u_{gk} (Figure V.22d). As a result, input voltage has an upper bound with clipping threshold $E_g \approx 0$, while output voltage has a lower bound with clipping level

$$\underline{U}_a = E_a - I_{ao} R_a. \qquad (V.10)$$

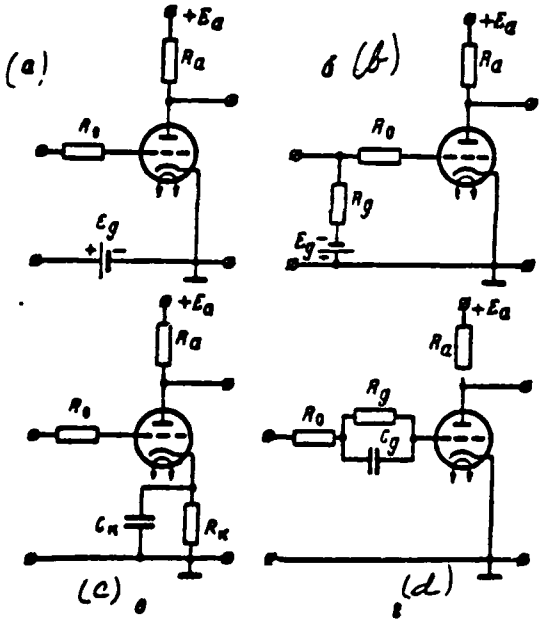

Figure V.23. Circuits For Grid Limiters With Non-Zero Clipping Thresholds.

Outside bias source E_g is introduced into the input network to change /193 the clipping threshold (Figure V.23a, b). Self-bias may be used for the same purpose (Figure V.23.c, d). In any case, however, expression (V.10) determines output voltage clipping level.

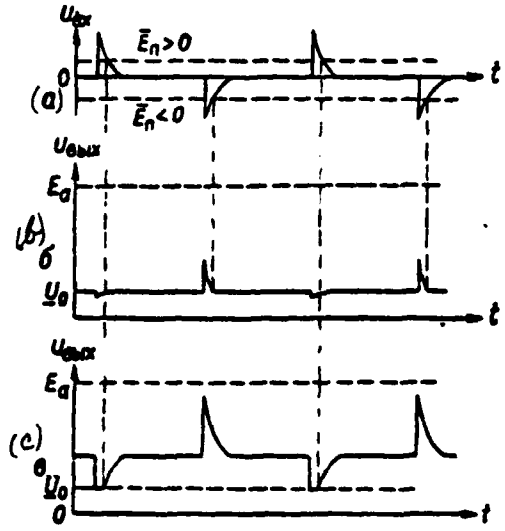

Figure V.24. For Exercise V.9.

EXERCISE V.9

a) Bipolar exponential pulses (Figure V.24a) are supplied to Figure V.23 circuit inputs. Indicate, for each circuit, clipping threshold $E_з$ sign and select the output voltage curve corresponding to it (Figure V.24b, c).

b) Attempt to compile a grid limiter circuit in which output voltage would have a lower bound (output—upper). (Page 474)

The impact of circuit stray input and output capacitances manifests itself when pulses with steep porches are supplied to grid limiter input. Circuit input capacitance $C_{вх}$ acts just like capacitance C_0 in a parallel diode limiter (see Figures V.13b and V.14d), i. e., along with resistance R_0, it forms an integrator leading to porch stretching (mainly) and voltage $u_{вых}$ fall-off. However, the influence of grid limiter input capacitance manifests itself more strongly since the /194 selected resistance R_0 significantly is greater than in a parallel diode limiter (triode resistance $r_{вых}$ is greater than open diode resistance $R_д$). Circuit output capacitance $C_{вых}$ operates just as in a pulse amplifier (see Chapter III, § 2) and will lead to additional porch stretching and output voltage fall-off. Resistance

R_0 and R_a permissible values must be bounded in order to decrease the influence of stray capacitances.

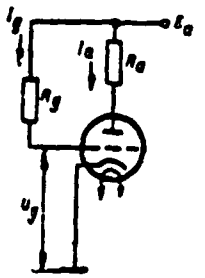

Figure V.25. Positive-Grid Circuit.

Grid clipping also occurs in those instances when the grid is connected across large resistance $R_g \gg r_{g0}$ to bus $+E_a$ (Figure V.25). Such circuits are referred to as positive-grid circuits and are used widely in pulse generators and saw-tooth generators. $U_{gk}>0$ when a grid is connected in this manner and grid current $I_g = \frac{E_a}{R_g + r_{g0}}$. flows across resistance R_g and the grid--cathode path.

Here

$$U_{g0} = E_a - I_g R_g = E_a - \frac{E_a R_g}{R_g + r_{g0}} = E_a - \frac{E_a}{1 + \frac{r_{g0}}{R_g}} \approx 0 \qquad (V.11)$$

-- grid potential which has an upper clamp essentially at the cathode potential /195 level. Thus, for example, we will get $U_{g0} = 250 - \frac{250 \cdot 10^6}{10^6 + 1.5 \cdot 10^3} \approx 0.37$ V when $r_{g0} = 1.5$ kΩ, R_g = 1 MΩ, E_a = 250 V.

We will note in conclusion that grid limiting also occurs when limiting resistance R_0 as such is absent, but output resistance of the previous stage (of the voltage u_{ex} generator) R_i is coincident with resistance r_{g0}, thus itself playing the limiting resistance role. Therefore, if grid limiting is undesireable, and, as the stage operates, voltage $u_{gk}>0$, then resistance R_i must be as small as

possible. In this event, it is advisible, for example, to use a cathode follower as the previous stage.

3. Plate Limiters With Plate Current Lower Cutoff

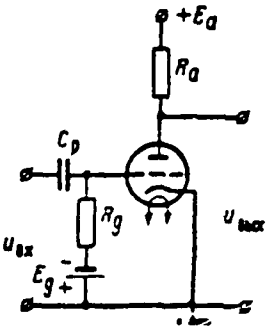

Figure V.26. Plate Limiter With Plate Current Lower Cutoff.

A triode is cut off ($i_a = 0$) if voltage applied to its control grid becomes less than cutoff voltage $u_c < E_c$. Here, plate voltage $u_a = E_a - i_a R_a$ rises to the source voltage E_a value, which it cannot exceed. This phenomenon also is used for plate current lower cutoff plate limiting. This limiter circuit is depicted in Figure V.26. It differs from a standard triode resistance amplifier only in operating mode: if input voltage in the amplifier must change within the constraints of the transfer characteristic linear sector, then the negative input voltage portion in this limiter must fall within the tube cutoff area.

Limiter action when sinusoidal voltage is supplied to input is explained in Figure V.27. A lower bound is placed on input voltage due to plate current lower cutoff, while an upper bound is placed on the output voltage. The magnitude of negative bias voltage E_g^* selected determines the clipping threshold value and the latter equals $E_a = E_{a0} - E_g$.

*Bias voltage E_g always will be applied as a "minus" to grid since, otherwise, the input voltage positive portion will cause grid current and will be subjected to grid clipping.

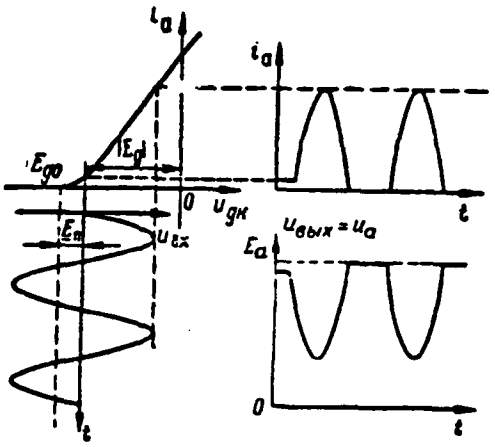

Figure V.27. Action of a Limiter with Plate Current Lower Cutoff.

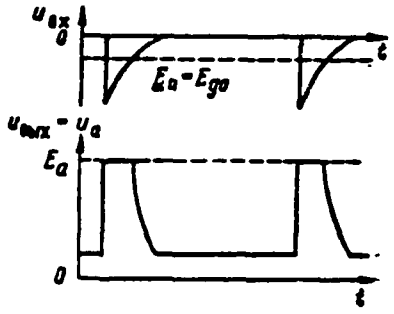

Figure V.28. Positive Pulse Clipping Due to Plate Current Lower Cutoff Where $E_g = 0$.

If there is a requirement to clip pulses of negative polarity, then bias E_g may be absent, while grid potential may be clamped at the cathode potential level ($U_{go} = 0$) due to grid current (see Figure V.25). Voltage curves for /196 this limiter type are depicted in Figure V.28.

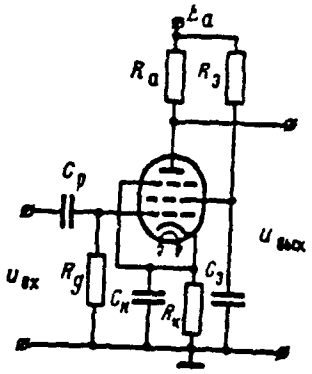

Figure V. 29. Limiter with Upper Cutoff of Anode Current

It should be underscored that, in any event, output voltage clipping level $U_0=E_0$ given plate current lower cutoff limiting. Tubes with sharp plate current cutoff are used in this limiter type to increase limiting precision.

EXERCISE V.10

Bipolar exponential pulses (Figure V.24a) are supplied to Figure V.26 circuit inputs. Determine clipping threshold and draw output voltage curves for three cases: $E_0<E_{00}$; $E_0=E_{00}$; $E_0>E_{00}$ if there only is plate current lower cutoff limiting.

(Page 474)

4. Plate Limiters With Plate Current Upper Cutoff

Plate current upper cutoff occurs due to tube dynamic saturation. The essence of this phenomenon was examined in Chapter III, § 2 and boils down to the fact that plate current increases when there is a voltage rise in the control grid, /197 while plate voltage drops to specific limits $I_{a\,max}=i_{s\,a}$, $U_{a\,min}$. As a result, the tube dynamic transfer characteristic acquires an upper bend, which also is used for limiting.

Triode dynamic saturation occurs when voltage u_{g1} values are positive (see Figure III.13b). But, when $u_{g1}=0$, control grid current, causing grid limiting, appears in the triode. Thus, this current always appears before plate limiting begins. Therefore, use of triodes for limiting with plate current upper cutoff only is possible in those rare instances when an input voltage generator has slight output resistance $R_i \ll r_{g1}$ (here, grid limiting essentially has no impact). Pentode dynamic saturation, thanks to screen grid action, still occurs given negative voltages u_{g1} (see Figure III.13d), i. e., precedes grid limiting. Therefore, most limiters with plate current upper cutoff comprise pentodes.

This limiter circuit is depicted in Figure V.29 and is analogous to a standard plate pentode limiter. However, as opposed to a limiter, its operating mode is selected so that a radical upper bend is obtained in the dynamic transfer characteristic in the $u_{g1}<0$ area. Large plate load impedance and increased screen grid voltage are used for this purpose, which facilitates cathode current redistribution between plate and this grid, which results in plate limiting beginning prior to grid limiting, while its precision increases.

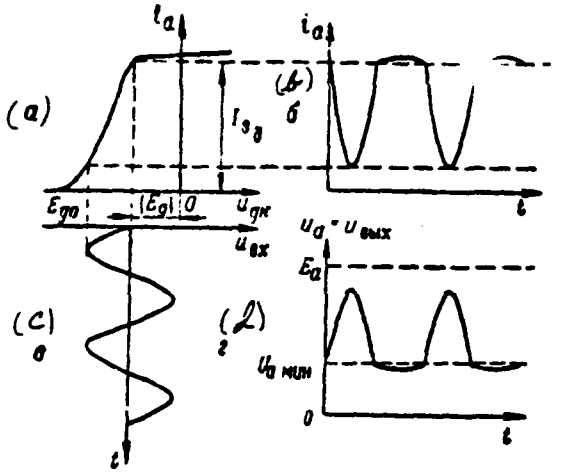

Figure V.30. Action of a Limiter With Plate Current Upper Cutoff.

Curves explaining circuit operation are depicted in Figure V.30. An upper bound is placed on input voltage ($E_g \bar{E}_s = 0$ for the negative bias E_g magnitude selected for Figure V.30), while a lower bound is placed on output voltage at level $\underline{U}_0 = U_{a\,min}$, due to plate current upper cutoff.

EXERCISE V.11

Redraw the output voltage curve for a limiter with plate current upper cutoff (Figure V.30d) and indicate how this voltage will change when magnitude E_g decreases and when resistance R_a increases. (Page 474)

5. Multielectrode-Tube Clipper-Limiters

Above, we saw that three limiting types were possible using multielectrode tubes:

— grid limiting (upper bound placed on input voltage and a lower bound on output voltage);

-- plate current lower cutoff limiting (lower bound placed on input voltage, upper bound on output voltage);

-- plate current upper cutoff limiting (upper bound placed on input voltage, lower bound on output voltage).

Combining these types of limiting in pairs so that both an upper and a lower bound would be placed on input voltage, we get the following types of clipper-limiters: if an upper bound is placed on input voltage due to grid currents and a lower bound due tc plate current lower cutoff, then this is referred to as a transfer clipper-limiter; if an upper bound is placed on input voltage due to plate current upper cutoff and a lower bound due to plate current lower cutoff, then this is referred to as a plate clipper-limiter.*

Transfer clipper-limiter. The transfer clipper-limiter circuit does not differ from the grid limiter circuit (see Figure V.21a, V23). However, the input voltage range change must cover the tube transfer characteristic "spread" /199 in order to provide both manifestation of grid currents (given u_{ex} maximums) and tube cut-off (given u_{ex} minimums). The values of both clipping thresholds $\overline{E}_{\text{o}}$ and $\underline{E}_{\text{o}}$ simultaneously may change, selecting the negative bias E_g magnitude. Bias magnitude must equal $E_g = \frac{E_{g1}}{2}$ to obtain symmetrical input voltage limiting. Operation of this limiter is explained in Figure V.31. The lower bound placed on output voltage (due to grid currents) is not as precise as upper bound $u_{a\max}$ (due to tube cut-off).

Plate clipper-limiter. This limiter circuit does not differ from the plate limiter circuit with plate current upper cutoff, i. e., a standard amplifying stage (see Figure V.29). However, the output voltage change range must from both sides cover the sloping sector of the tube dynamic transfer charac'eristic in order to provide both tube dynamic saturation (given u_{ex} maximums) and its cut-off (given u_{ex} minimums).

Operation of this limiter is explained in Figure V.32. The upper bound placed

*The third grid limiting combination and limiting due to plate current upper cutoff physically are impossible since both phenomena place an upper bound on input voltage.

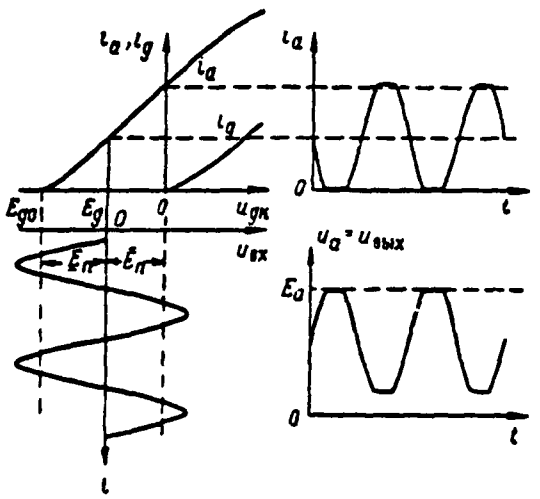

Figure V.31. Transfer Clipper-Limiter Action.

on output voltage (at level $U_0 = U_{a\,min}$) here also is not as precise as the upper bound (at level $U_0 = E_a$). As was the case in the previous circuit, the values of both clipping thresholds simultaneously may be regulated by magnitude E_g /200 selection. Reduced plate supply voltage E_a (to several tens of volts) often is used in the circuits under examination to decrease the input voltage change constraints required to obtain bidirectional limiting, as well as to "notch" a narrower band from the input signal. This facilitates both tube cut-off and its transition to the dynamic saturation area. As a result, the transfer characteristic "spread" corresponding to the transfer mode, i. e., the upper and lower clipping thresholds converge, is decreased.

Cathode-coupled clipper-limiter. As noted above, separate regulation of clipping thresholds $\bar{E}_п$ and $\underline{E}_п$ is hindered when transfer and plate clipper-limiters are used and different upper and lower limiting precision is obtained. The Figure V.33 cathode-coupled clipper-limiter does not have these shortcomings. It /201 will comprise two stages: a cathode follower (triode L_1) and a common-grid amplifier (triode L_2). Both cathodes are coupled across common cathode load impedance $R_к$.

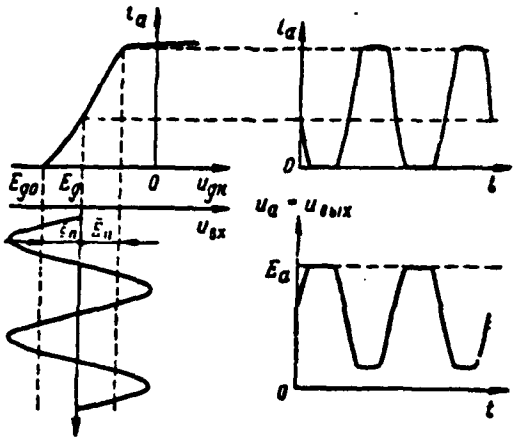

Figure V.32. Plate Clipper-Limiter Action.

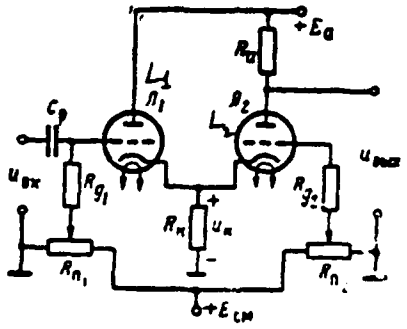

Figure V.33. Cathode-Coupled Clipper-Limiter.

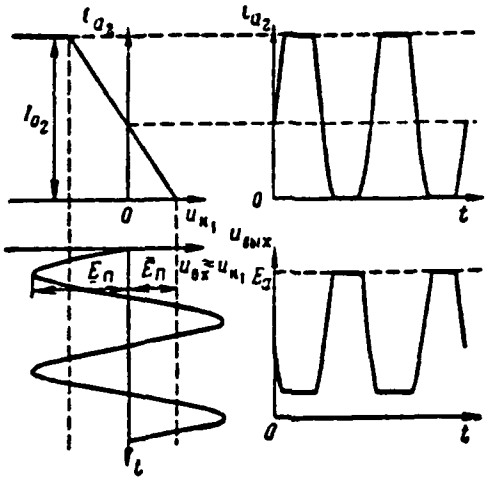

Figure V.34. Cathode-Coupled Clipper-Limiter Action.

Limiter operating principle is explained in Figure V.34 and will comprise the following. The transfer mode is insured when both triodes are open. Here, triode L_1 plate current creates voltage drop u_{k1} (cathode follower output voltage) across resistance R_k applied as a "minus" to triode L_2 grid, i. e., decreasing its plate current i_{a2}. Since voltage u_{k1} changes in phase with input voltage, voltage u_{gk2} changes opposite in phase with voltage u_{k1}, while voltage $u_{g2} = u_{вых}$

changes opposite in phase with voltage $u_{вх2}$, then limiter output voltage in the transfer mode changes in phase with the input voltage.

When voltage $u_{вх}$ decreases to value $\underline{E}_{вх}$ at which triode L_1 cuts off ($i_{a1}=0$), triode L_2 plate current will become maximum and equal quiescent current I_{a02}, while its plate voltage will become minimal. This insures that a lower bound is placed on input and output voltages. When voltage $u_{вх}$ rises to value $\overline{E}_{вх}$ at which triode L_2 cuts off due to a voltage $u_{вх1}$ increase, its plate voltage will become maximum. This places an upper bound on input and output voltages. Thus, a lower bound is placed on input voltage due to triode L_1 plate current lower cutoff, while an upper bound results from triode L_2 plate current lower /202 cutoff. This insures that an identically-precise upper and lower bound is placed on output voltage. Resultant output voltage clipping levels also are equal: $\underline{U}_0 = U_{a2\,max} = E_a - i_{a02}R_a$, $\overline{U}_0 = U_{a2\,min} = E_a$. $\underline{U}_0$ clipping thresholds and clipping level are set by potentiometers $R_{п1}$ and $R_{п2}$, which regulate bias voltages at the triode grids.

A sufficiently-large resistance $R_к$ (5--10 k Ω) is selected to prevent grid current manifestations, given positive $u_{вх}$ values, which insures deep negative feedback. Since a voltage $u_к$ drop here may reach several tens of volts, bias voltages picked off the potentiometers are positive.

Since the first circuit stage is a cathode follower, circuit input resistance is great, while input resistance is slight. The second stage common grid constrains signal "leakage" across triode L_2 transient capacitance $C_{ак}$ when L_2 is closed.

§ 4. TRANSISTORS IN LIMITER AND SWITCH CIRCUITS

1. Transistor Limiters

Transistor use as limiters is based on the nonlinearity of transistor dynamic characteristics. The common-emitter transistor stage is the most-widespread circuit (Figure V.35). It does not differ in appearance from a transistor amplifier (see Figure III.40, for example). However, operating modes differ significantly. A transistor in an amplifier operates in the large signal mode and its operating point leaves the characteristic's linear area boundaries, to the saturation area

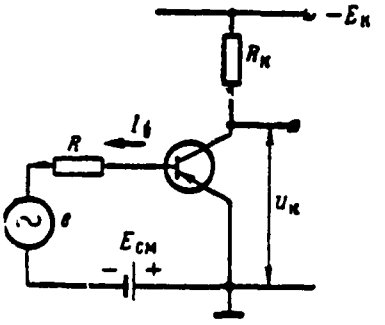

Figure V.35. Common-Emitter Circuit Transistor Limiter.

on the one hand and to the cutoff area on the other. An upper bound is placed on output voltage (for pnp transistors) due to collector current saturation, while a lower bound is placed due to transistor cut-off. The saturation and the cutoff areas are used simultaneously to obtain signal clipping-limiting, selecting /203 the operating point in the initial state somewhere in the middle of the active area.

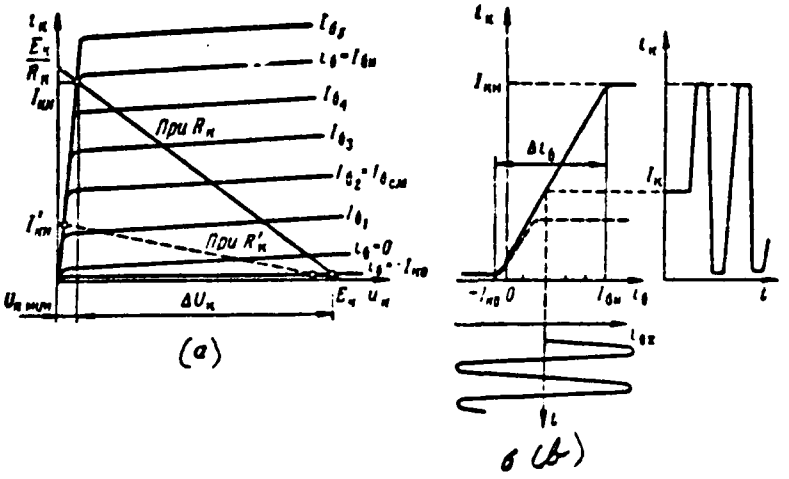

Figure V.36. Plotting an OE Transistor Load Line (a) and Dynamic Characteristic (b).

Practical determination of clipping thresholds may be accomplished using dynamic characteristic $i_к = f(i_б)$. For this purpose, the load line will be plotted

initially in the static collector characteristic family, then the dynamic characteristic will be plotted based on the points where it intersects the static characteristic. The dynamic characteristic plot is illustrated in Figure V.36. Threshold clipping levels determine this characteristic's breakpoints.

Base current $i_б = I_{бв}$ magnitude determines output voltage upper clipping threshold at which collector current reaches saturation $(i_к = I_{кн})$. The following relationship may be used to express transistor saturation condition:

$$i_б \geqslant I_{бв} = \frac{I_{кн}}{\beta_{ср}}, \tag{V.12}$$

where $\beta_{ср}$ — average current gain value for a given transistor.

Collector voltage in the saturation area equals $U_{к.нас}$, while collector current equals

$$I_{нас} = \frac{E_к - U_{к.нас}}{R_к} \approx \frac{E_к}{R_к}. \tag{V.13}$$

The magnitude of return base current $i_б = -I_{к0}$ at which uncontrolled /204 current $I_{к0}$ flows in the collector network determines lower clipping threshold. In the cutoff area, collector voltage equals

$$U_к = E_к - I_{к0}R_к. \tag{V.14}$$

To obtain bidirectional limiting, the current drop across the input network must equal the following magnitude

$$\Delta i_б > I_{бв} + I_{к0} \approx I_{бв}.$$

Here, the voltage drop across the collector equals

$$\Delta U_к = E_к - I_{к.н}R_к - U_{к.нас}. \tag{V.15}$$

Since values $I_{к.н}R_к$ and $U_{к.нас}$ in sum do not exceed 0.2—0.3 V (where the

resistance $R_н$ magnitude is on the order of tens of kilohms), then essentially it is possible to consider

$$\Delta U_к \approx E_к.$$

Collector current drop magnitude equals

$$\Delta I_к = I_{к.н} - I_{к0} \approx I_{к.н}.$$

Thus, a transistor in a limiter circuit possesses good switching properties.

There also is a requirement to note that signal limiting can occur when the input voltage drop has a relatively-low magnitude. This may be on the order of several tens of fractions of volts for germanium transistors and on the order of 1--2 volts for silicon transistors. However, one should remember that a transistor is controlled not by voltage, but by current, whose magnitude will depend on the magnitude of transistor input resistance and signal source internal resistance. Therefore, large input signal amplitudes essentially are required.

Resistance R (included here also is signal source internal resistance), whose magnitude is greater than transistor input resistance in the conducting state, is connected to the base network so that transistor influence on input current is slight. In this event, one may assume that signal source emf magnitude determines input current, i. e., $i_{б.н} = \frac{e}{R}$.

EXERCISE V.12

Is there an analogy between resistance R and resistance connected to a grid limiter network? (Page 475)

Limiter operating quality will depend on selection of load impedance $R_н$ magnitude. Actually, resistance $R_н$ needs to be increased to increase limiter sensitivity to the input signal. The dotted line in Figure V.36 represents the load line where $R'_н > R_н$ and the corresponding dynamic characteristic. In /205 this event, lower input current drop $\Delta i_б$ is required for bidirectional limiting. However, circuit temperature stability deteriorates when resistance $R_н$ magnitude

is great. Current $I_{к0}$ increases sharply at increased temperature. Since saturation current $I_{кн}$ magnitude, determined by external element parameters, specifically by resistance $R_к$ and source voltage $E_к$, remains unchanged, then collector current drop $\Delta U_к = I_{кн} - I_{к0}$ decreases. Consequently, the voltage drop across the limiter output also decreases. The following condition must be satisfied for normal limiter operation across a broad range of temperatures

$$I_{кн} \geqslant 10 I_{к0\ макс}. \qquad (V.16)$$

EXERCISE V.13

a) Select resistance $R_к$ for limiter operation in a temperature range up to +65° C if $E_к = -15$ V, $I_{к0\ макс} = 60$ uA.

b) Does resistance $R_к$ magnitude impact upon output signal amplitude when the temperature is fixed? (Page 475)

Resistance $R_к$ magnitude in practical limiter circuits is selected within a range of several tens of kilohms.

2. Transient Processes in a Transistor Switch Circuit

Transistor operation in the switching mode is used not only for signal amplitude limiting. The switching mode is used in many transistor pulse devices, such as switches, trigger circuits, multivibrators, and the like.

Good transistor switching properties make it possible to obtain shaped pulse amplitudes close to supply source voltage, which advantageously differentiates transistors from electron tubes.

Switching processes will depend little on stray and transistor junction capacitance magnitudes since usually the load impedances across which a charge (discharge) of these capactiances occurs is slight, on the order of unities of kilohms. However, the switching process in a transistor switch to a large degree will depend on the lag properties of the transistor itself coupled with the infinite rate of carrier diffusion and clean-out delay during deep saturation.

Switching time will depend on transistor type and on how it is connected in the circuit. This determines collector current pulse rise and decay time and, consequently, maximum possible switching frequency as well.

We will examine transient processes in a common-emitter transistor switch, whose circuit is identical to the limiter circuit depicted in Figure V.35.

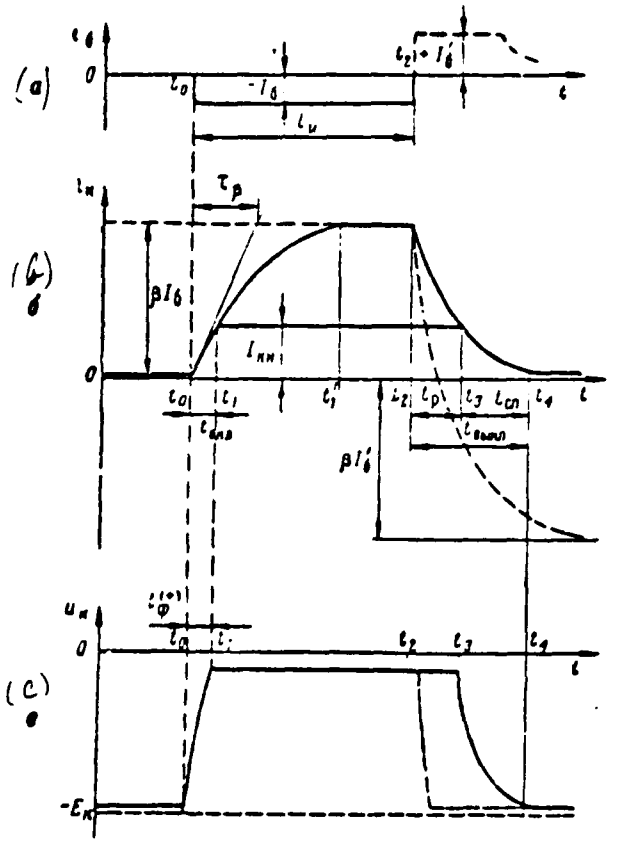

Figure V.37. Transient Processes in a Common-Emitter Transistor Switch (Dotted Line Depicts Process With Tripping Current Present).

In the initial state, let the transistor be cut off due to positive bias /206 source $E_{см}$ connected between the base and the emitter. At moment in time $t = t_0$ negative current drop $\Delta i_б = I_б > I_{бн}$ is supplied to the transistor base (Figure V.37a). The transistor unblanks in accordance with a law well-approximated by an exponent

(see Chapter III, § 6):

$$i_к(t) = \beta I_б\left(1 - e^{-\frac{t}{\tau_\beta}}\right), \qquad (V.17)$$

where $\tau_\beta = \frac{1}{2\pi f_\beta}$ -- collector current-rise time constant in a common-emitter /207 transistor circuit.

Collector current at moment in time $t = t_1$ reaches saturation and is clamped at this level (Figure V.37b). On time $t_{вкл} = t_1 - t_0$ may be obtained from expression (V.17) if one considers that, when $t = t_0$, $i_к \approx 0$, while, if $t = t_1$, $i_к = I_{кн}$:

$$I_{кн} = \beta I_б\left(1 - e^{-\frac{t_{вкл}}{\tau_\beta}}\right).$$

Hence, for rise time $t_\phi^{(+)}$ we get a positive collector voltage drop (Figure V.37c)

$$t_\phi^{(+)} = t_{вкл} = \tau_\beta \ln \frac{\beta I_б}{\beta I_б - I_{кн}} \qquad (V.18)$$

Usually, base current $I_б$ will strive towards an increase to accelerate the switching process. Then, it turns out that $\beta I_б \gg I_{кн}$ and formula (V.18) is simplified

$$t_\phi^{(+)} = t_{вкл} \approx \tau_\beta \frac{I_{кн}}{\beta I_б}. \qquad (V.19)$$

EXERCISE V.14

Demonstrate that the on time approximate value may be obtained directly from Figure V37b. (Page 475)

It follows from formulas (V.18) and (V.19) that transient process acceleration in a common-base transistor switch may be achieved by means of a large degree of saturation, which requires an increase in base current drop. We will note that a current $I_{кн}$ decrease for such purposes is undesireable due to deterioration in circuit temperature stability. However, the transistor deep saturation mode has its drawbacks. It is a case where collector current during deep saturation

does not decrease immediately after cessation of the current pulse in the base network (time moment $t = t_2$ in Figure V.37), but following slight time delay t_p.

Excessive carriers are cleaned out of the collector junction during this period of time and this process occurs until the concentration of minor carriers in the base at the collector junction reaches equilibrium value. After that the transistor turns out to be in the active area and collector current dimunition begins.

Collector current will fall to the initial value in accordance with an exponential law

$$i_к(t) = I_{кн} e^{-\frac{t}{\tau}}, \tag{V.20}$$

and, therefore, fall time is

$$t_{сп} = (3 \div 5)\tau. \tag{V.21}$$

Dispersal and fall time may be reduced significantly if, during cutoff, base current with a jump decreases from negative value $I_б$ to positive value $I'_б$. This is explained by acceleration of the dispersal of the charge accumulated in the base under the influence of a strong blanking signal. The transient process occurring as tripping current $I'_б$ is supplied is depicted by the dotted line in Figure V.37. It is evident from the figure that lag time t_p and fall time $t_{сп}$ may be reduced significantly by increasing the tripping current. Given great current $I'_б$ magnitude, the approximate turn-off time value $t_{выкл} = t_p + t_{сп}$ may be determined directly from Figure V.37

$$t_{выкл} = \tau \frac{I_б}{I_б + I'_б}. \tag{V.22}$$

Duration of collector voltage negative drop correspondingly may be determined from the formula

$$t'_з = t_{сп} = \tau \frac{I_{кн}}{2I'_б}. \tag{V.23}$$

Collector current decrease τ' in expressions (V.22) and (V.23) differs from τ_3 since, during a certain time period, the collector junction will be under the influence of forward voltage relative to the base and will act like an emitter. One may consider that $\tau' \approx \tau_3$ for qualitative evaluations.

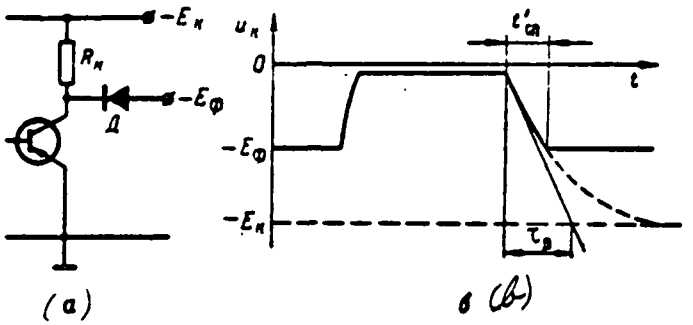

Figure V.38. Diode Clamp Method of On Time Reduction.

Transistor turn-off time may be reduced if collector voltage diode clamping is used (Figure V.38a). The absolute value of the magnitude of clamped voltage /209 source $E_ф$ is less than that of voltage $E_к$. Therefore, the process of switch initial state reestablishment ceases at level $u_к = E_ф$. It is evident from Figure V.38b that fall time may be determined in the following way:

$$t'_{сп} = \tau_э \ln \frac{E_к}{E_к - E_ф}. \qquad (V.24)$$

One cannot say that this method of decreasing turn-off time is completely satisfactory due to the decrease in voltage drops across the transistor collector. In addition, this method will not lead to a reduction in lag time.

One effective way to increase switch response speed is use of an R-C network at transitor input (Figure V.39a). Relatively-high actuating current arises in

*Time constant $\tau = (1 \div 1)\tau_э$ [6] depending on transistor type and design.

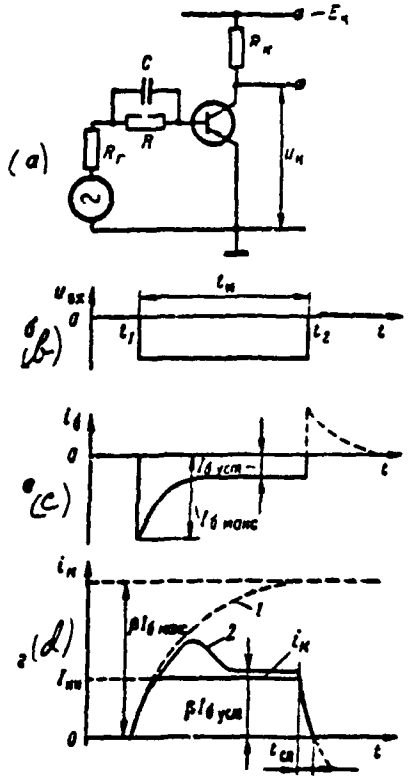

Figure V.39. Use of a Boosting R-C Network in a Transistor Switch.

this circuit when a negative voltage pulse (Figure V.39b) is supplied to the input circuit

$$I_{б.макс} = \frac{U_б}{R_г + r_{бэ}},$$

where $U_б$ -- input pulse amplitude;

$r_{бэ}$ -- base--emitter conducting sector resistance.

This current, charging capacitor C, decreases to the assigned value

$I_{б.уст} = \frac{U_п}{R_т + r_{бэ} + R} \approx \frac{U_п}{R}$, since usually $R \gg (R_т + r_{бэ})$. Resistance R magnitude is selected so that the degree of transistor saturation is insignificant and is suffices only for compensation of circuit element parameter variation.

Base current curves are depicted in Figure V.39c, while collector current curves are depicted in Figure V.39d. They explain the physical processes in the circuit. Here, curve 1 reflects the character of the change in ficticious collector current $i_к = \beta i_б$, which would arise when input d-c $i_б = I_{б\ нас}$, placing the transistor in the deep saturation mode, is present. However, input current decreases by virtue of capacitor C charge and ficticious collector current must change in accordance with curve 2. In fact, collector current is clamped at level $i_к = I_{кн}$ and rise time turns out to be insignificant. If circuit parameters are selected so that magnitude $\beta I_{б\ уст}$ slightly exceeds $I_{кн}$, then this rules out delay in transistor exit from the saturation state.

EXERCISE V.15

How is switch response speed linked with R-C time constant magnitude? (Page 475)

A large spike of base back current, which provides slight turn-off time, arises at the moment the switching pulse ceases.

CHAPTER VI /211

TWO-STAGE SQUARE-WAVE GENERATORS (MULTIVIBRATORS)

§ 1. GENERAL INFORMATION ON TWO-STAGE SQUARE-WAVE GENERATORS

1. Generator Construction Principle. Self-Excitation Conditions

Two-stage square-wave generators (flip-flops, multivibrators) are used widely in RLS pulse devices to obtain gate, blanking, and strobe pulses, display intensifier (flyback suppression) pulses, pulses controlling sawtooth generator operation, pulse repetition frequency division, pulse time delays, and so forth.

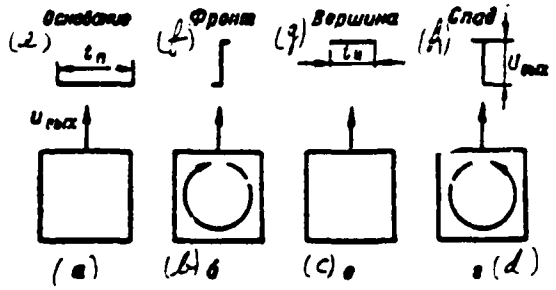

Figure VI.1. Four Square-Wave Pulse Generator Operating Stages: (a) -- First equilibrium state; (b) -- First reversal; (c) -- Second equilibrium state; (d) -- Second reversal; (e) -- Base; (f) -- Porch; (g) -- Tilt; (h) -- Droop.

Square pulses have an infinite frequency spectrum (see Attachment 1). So, from the frequency point of view, square-wave pulse generators simultaneously must produce harmonic oscillations in a broad (theoretically infinite) /212 frequency band.* One may divide the complete operating cycle of any square-wave pulse generator into four stages, conditionally and separately depicted in Figure VI.1. In two stages (Figure VI.1a, c) corresponding to pulse base and tilt shaping, generator output voltage must be constant, but must differ by a magnitude equal to pulse amplitude. Output voltage constancy is insured in the circuit's equilibrium state electrically. Therefore, the generator must have two different equilibrium states, while the duration of one determines resting time duration $t_п$ and the other pulse duration $t_и$. In the two other states (Figure VI.1b, d) corresponding to pulse porch and droop shaping, generator output voltage in the ideal case must change instantaneously -- rise or fall with a jump. A spasmodic circuit change from one equilibrium state to another due to action of internal forces is referred to as circuit reversal. Reversal occurs when a state of unstable equilibrium arises in a circuit, when any, even a slight, random change in the circuit's electrical mode will lead to an avalanche-like process resulting in the circuit changing to a new equilibrium state.**

An avalanche-like process develops in the event that any initial change of current or potential at a given point in a circuit is maintained and amplified due to processes arising within the circuit itself. This is the essence of the so-called self-excitation condition. It is evident that satisfaction of the self-excitation condition means that any electrical changes in a circuit must act in a closed loop: the output signal (the result of input signal action) must give way backwards to circuit input, maintaining and amplifying the input signal (the cause of the appearance of the output signal). Thus, a closed positive feedback loop must act twice in a generator, at the moment the pulse porch and droop are shaped. This loop must be open when the circuit is in equilibrium states.

The overall self-excitation condition is subdivided into a phase and amplitude

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*Therefore, they are called multivibrators -- multiple-frequency oscillation generators.

**An avalanche-like process is one that develops in a circuit on the avalanche principle -- with rising (theoretically to infinity) speed -- due to the action of internal forces.

self-excitation condition. The former means that an output signal supplied in reverse to circuit input must act in the same direction as does the input signal. This signifies that the resultant phase shift between output and input signals as the closed feedback loop is bypassed must equal (or be shorter than) 2π : /213

$$\varphi_{\Sigma} = \varphi_{вых} - \varphi_{вх} = 2\pi. \qquad \text{(VI.1)}$$

Feedback will be positive when this condition is met.

Amplitude self-excitation condition means that the output signal must exceed the input signal in magnitude (the result is to exceed the cause). This signifies that resultant gain in the positive feedback loop must be greater than unity

$$K_{\Sigma} = \frac{\Delta u_{вых}}{\Delta u_{вх}} > 1 \qquad \text{(VI.1a)}$$

This condition insures an uninterrupted rise in the conversion rate, i. e., its avalanche-like nature.

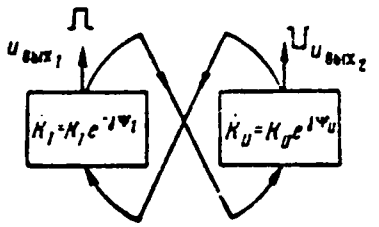


Figure VI.2. Multivibrator Schematic Diagram.

Two tube or semiconductor triode amplifying stages connected in a closed loop so that each stage's output voltage is supplied to the output of the other stage are used to satisfy conditions (VI.1) and (VI.1a) in the generators examined in this chapter. Therefore, the schematic diagram depicted in Figure VI.2 may represent such a generator in overall form (the positive feedback loop for equilibrium states is open).

For a two-stage generator, conditions (VI.1) and (VI.1a), respectively, are written in the form

$$\varphi_{\Sigma} = \varphi_{I} + \varphi_{II} = 2\pi; \tag{VI.2}$$

$$K_{\Sigma} = K_{I}K_{II} > 1, \tag{VI.2a}$$

where φ_{I} and φ_{II} — phase shifts;
K_{I} and K_{II} — gain moduli for each stage.

Phase self-excitation condition (VI.1) will be satisfied if each stage changes voltage phase 180°, i. e., is a phase inverter $\varphi_{I} = \pi$; $\varphi_{II} = \pi$.

As is known, the frequency band in which self-excitation conditions are satisfied must be as broad as possible to increase the reversal rate, i. e., pulse porch and droop steepness. From this point of view, presence of frequency-selection elements -- inductances and capacitances -- in the circuit is undesirable. Therefore, both stages in generator tube circuits are assembled as pulse amplifiers from resistances with plate load (see Chapter III, § 2). Output (plate) /214 voltage from each such amplifier changes opposite in phase to input (grid) voltage, which explains satisfaction of condition (VI.2), while its gain is greater than unity, which explains satisfaction of conditon (VI.2a).

All two-stage pulse generator circuits are categorized as symmetrical (when the circuits and all parameters of both amplifying stages are identical) and asymmetrical (when the circuits and amplifying stage parameters are different). Coupling of the plate (output) of one stage with grid (input) of another is referred to as plate-grid coupling. Two identical plate-grid couplings are mandatory in symmetrical circuits. Only one plate-grid coupling often is used in asymmetrical circuits. In this event, the other is replaced by a coupling of cathode networks created with the aid of cathode load impedance R_{k} common to both stages. Since the input of each amplifying stage is coupled to the output of the other and each stage is a phase inverter, then their input (and, consequently, their output) voltages change opposite in phase: if the input voltage of one stage rises with a jump, then the other drops with a jump. Jump magnitude is constrained by the nonlinearity of tube (or transistor) characteristics. The tube whose input voltage

drops cuts off, while its output (plate) voltage will become maximum. Blanking of this tube breaks the positive feedback network, i. e., disrupts satisfaction of self-excitation conditions, resulting in the next equilibrium state appearing in the circuit. A voltage rise at second tube input usually is clamped at the zero level due to its grid current. Therefore, this tube's output voltage is clamped in the equilibrium state at the minimum level. Thus, output voltage horizontal sectors are clamped in circuit equilibrium states due to plate-grid limiting (see Chapter V, § 3).

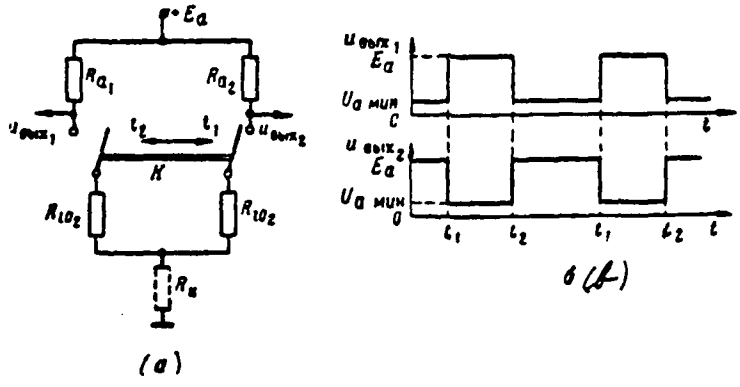


Figure VI.3. Multivibrator as a Double-Arm Nonlinear Voltage Divider (a) and Its Output Voltage Curves (b).

It is clear from what has been stated that the first tube always is unblanked and the second always blanked in the generator's first equilibrium state, while the opposite is true in the other state. This provides the foundation, from the output voltage shaping point of view, to represent the two-stage square-wave generator by a common equivalent circuit in Figure VI.3a in the form of a double-arm nonlinear voltage divider with commutator switch K. In this circuit, R_{a_1}, R_{a_2} -- plate load impedances, R_{i_1} and R_{i_2} -- tube internal d-c resistance, while the dotted line depicts common cathode load impedance $R_к$ (it is absent in circuits with two plate-grid couplings). The extreme left and right switch K positions correspond to the two stages of circuit equilibrium state. The jumps in the circuit (reversal stages) are equivalent to switch throw-over from one extreme position to /215 the other. The curves of the circuit's two output voltages picked off the stage plate loads and changing opposite in phase at the moment of switch throw-over is thrown are depicted in Figure VI.3b.

2. Basic Generator Types and Operating Modes

There can be three two-stage pulse generator operating modes depending on the nature of the causes of spasmodic conversions, i. e., on the method of throwing switch K in Figure VI.3. The three basic types are:

-- multivibrators with stages of stable equilibrium, usually referred to as flip-flops;

-- multivibrators with one state of stable equilibrium, usually referred to as monostable multivibrators;

-- free-running multivibrators without a single state of stable equilibrium.

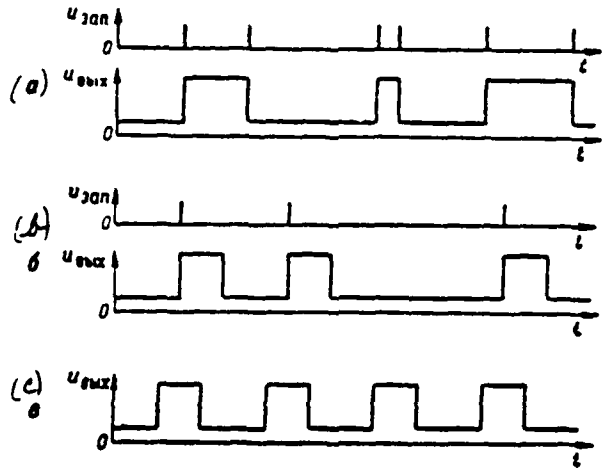


Figure VI.4. For Explanation of Flip-Flop (a), Monostable Multivibrator (b) and Free-Running Multivibrator (c) Operation.

Both equilibrium states are stable in flip-flops. Each may in and of itself continue as long as it desires and is disrupted only by an external stimulus. Consequently, each circuit reversal (switch throw-over) occurs only due to external trigger pulse action. Here, the duration of the developed pulses and their repetition frequency are determined exclusively by the time intervals between trigger pulses (Figure VI.4a). Therefore, there is no control in a flip-flop circuit.

Only one equilibrium state is stable in monostable multivibrators and it may be disrupted only by an external stimulus. Internal circuit processes determine

how long the circuit remains in the second equilibrium state. Therefore, /216
the second equilibrium state is temporarily stable (quasistable). Consequently, trigger pulses are required here for a circuit reversal only in one direction -- circuit reversal from a state of stable equilibrium to a state of temporarily-stable equilibrium. A circuit reversal in the opposite direction occurs spontaneously. Here, trigger pulse intervals provide only the generated pulse repetition period, with the parameters of the circuit itself determining the duration of these pulses (Figure VI.4b). Therefore, there usually is generated pulse duration control in a monostable multivibrator circuit. The circuit requires a timing (time-setting) element (energy accumulator), which also determines how long the circuit remains in the temporarily-stable state after triggering, in order for it to return spontaneously to the initial state of stable equilibrium. A timing capacitor connected to one plate-grid coupling plays this role.

Both equilibrium states in free-running multivibrators are temporarily-stable. Consequently, both circuit reversals (both switch K throw-overs) occur spontaneously and do not require trigger pulse stimuli. The circuit timing element -- a capacitor -- determines how long the circuit remains in each temporarily-stable state. Therefore, the circuit has two timing capacitors connected to both plate-grid /217 couplings. The parameters of the circuit itself determine all parameters of the pulses generated in the free-running mode. The circuit generates a periodic pulse train if circuit parameters remain unchanged during operation (Figure VI.4c). A free-running multivibrator circuit controls generated pulse repetition period and duration.

Presence of timing (as well as stray) capacitances always impacts unfavorably on generated pulse shape. Therefore, flip-flops develop pulses that most-closely approximate square pulses, while free-running multivibrators provide the greatest pulse shape distortions.

3. Principles of External Generator Triggering

Action of external trigger pulses, which cause a circuit reversal, is required for flip-flop and monostable multivibrator operation. In principle, there is a requirement here either to unblank a blanked tube with a pulse of positive polarity (an unblanked tube is blanked here) or to blank an unblanked tube with a pulse

of negative polarity (a blanked tube is unblanked here). In any event, an active avalanche-like reversal process arises only in the time interval when both tubes are unblanked since a positive feedback loop exists only at this time. Consequently, a circuit reversal caused by positive feedback action means that a blanked tube must be unblanked by a trigger pulse before the unblanked tube is blanked.*

Since it is mandatory that one tube is unblanked prior to triggering, then there always is the chance to use it as an amplifier, a trigger pulse inverter. Therefore, it is more advantageous to trigger with a negative pulse supplied to unblanked tube grid. In this case, an amplified positive pulse, which is transmitted across the plate-grid coupling to blanked tube grid, arises in the unbanked tube plate network. It is evident that an amplified positive pulse unblanks a blanked tube even in the event that negative trigger pulse amplitude at unblanked tube grid is insufficient to blank it. Active circuit reversal will ensue as a result. Thus, flip-flop and monostable multivibrator sensitivity to negative trigger pulses is greater by a factor of K than to a positive pulse. Consequently, negative trigger pulse amplitude may be correspondingly less than that of positive pulses. Actually, prior to triggering, voltage at unblanked tube grid equalled $U_{g\,max} \approx 0$ (resulting from grid limiting) and voltage at blanked tube grid equalled /218 $U_{g\,max} < E_{g2}$, then the amplitude of negative trigger pulse $U'_{зап}$ required to unblank a blanked tube across an unblanked tube must be selected from condition

$$U'_{зап} > \left| \frac{U'_{g\,max} - E_{g2}}{K} \right|, \qquad \text{(VI.3)}$$

where K -- stage gain in an unblanked tube considering plate-grid coupling transfer constant;

E_{g2} -- blanked tube cutoff voltage.

The amplitude of the positive trigger pulse required for direct unblanking of a blanked tube must be selected from condition

$$U'_{зап} > |U_{g\,max} - E_{g2}|. \qquad \text{(VI.3a)}$$

*In practice, there are cases where an unblanked tube is blanked initially during triggering due to stray capacitance influence. Here, a passive circuit reversal occurs when the positive feedback loop does not close (see below).

Along with a decrease in trigger pulse amplitude, negative pulse triggering also has several other advantages, which will be discussed below.

Negative trigger pulses must act in sequence during flip-flop triggering, first to the grid of one, then to the grid of the other tube (insuring flip-flop reversal first in one, then in the other direction), while, during monostable multivibrator triggering, to the grid of the same tube unblanked in a state of stable equilibrium (the circuit spontaneously returns to this state).

The role of trigger pulses in flip-flops and monostable multivibrators (just as is the case in other trigger devices) boils down only to the initial external stimulus on the circuit leading to initiation of an avalanche-like reversal process. This process itself already develops spontaneously and independent of this stimulus as self-excitation conditions are satisfied. This makes it possible, first, to use very short trigger pulses for triggering and, second, to trigger across special trigger tubes (diodes, triodes). A trigger tube transmits to a circuit only that portion of a trigger pulse porch whose action suffices for stimulation of an avalanche-like process (for unblanking a blanked tube). After this, it closes immediately, cutting the trigger pulse source out of the generator circuit and thereby eliminating their harmful mutual influence.

§ 2. MULTIVIBRATORS WITH TWO STABLE EQUILIBRIUM STATES (FLIP-FLOPS)

1. Flip-Flops With Two Plate-Grid Couplings (Symmetrical Flip-Flops)

A flip-flop circuit with two plate-grid couplings and external bias source E_g is depicted in Figure VI.5a. Voltage curves for characteristic circuit /219 points without consideration for the influence of stray capacitances are depicted by dotted lines in Figure VI.5b.

Two identical triode amplifying stages L_1 and L_2 with plate loads R_{a1} and R_{a2} form the flip-flop circuit. Each triode plate is connected with the other triode's grid across dividers R_1, R_{g2} and R_2, R_{g1} to create a closed positive

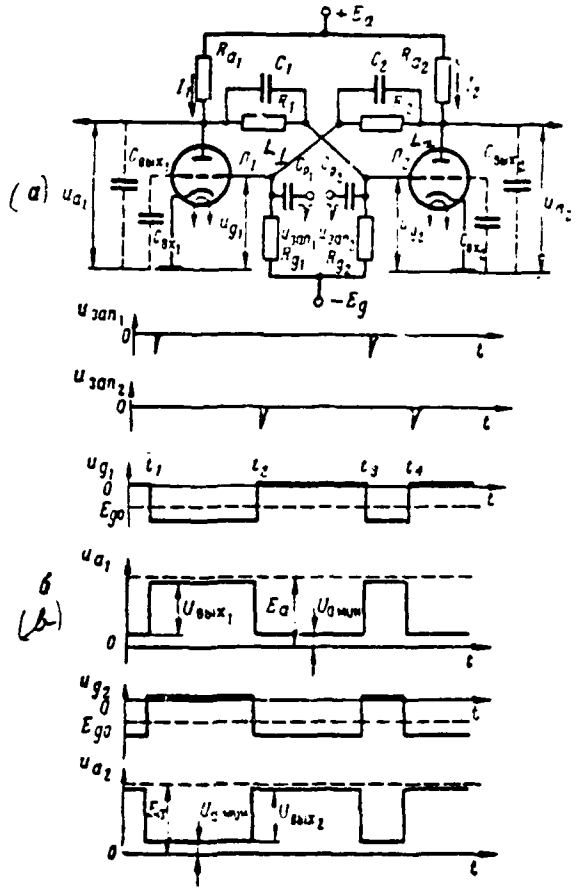


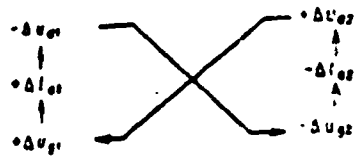
Figure VI.5. Flip-Flop With Two Plate-Grid Couplings and External Bias Source.

feedback loop. Resistances R_{g_1} and R_{g_2} are connected to negative bias source E_g^* to create requisite distribution of "d-c" potentials (tube blanking /220 capability). Accelerating capacitors C_1, C_2 used for high-frequency divider compensation making a decrease in the influence of tube stray input capacitances possible (see Chapter II, § 4), are connected in parallel to resistances R_1 and R_2. As a result, the flip-flop reversal rate increases. Capacitors C_1 and C_2

*Such coupling of one tube plate with the other tube grid often is referred to as potentiometric coupling.

in principle may be absent. Negative trigger pulses $u_{вх1}$ and $u_{вх2}$ are supplied alternately to triode grids across coupling capacitors $C_{р1}$, $C_{р2}$ (we will examine trigger circuits across trigger tubes below). Circuit output voltages are picked off plates: $u_{вых1}=u_{а1}$, $u_{вых2}=u_{а2}$. The parameters of both circuit halves ("arms") are absolutely identical. Therefore, this is referred to as a symmetrical flip-flop.

We will assume that, after the circuit is cut in, it will be in an equilibrium state where both triodes are open, their plate currents are identical $i_{а1}=i_{а2}$, while grid currents are absent $(u_{g1}=u_{g2}<0)$. This is a state of unstable equilibrium. Actually, due to postive feedback loop action in which amplitude self-excitation condition (VI.2a) is satisfied, any random current or voltage change (fluctuation) in one circuit arm will lead to onset of an avalanche-like process. We will assume, for example, that triode $Л_1$ plate current rose by magnitude $\Delta i_{а1}$. Then voltages $u_{а1}$ and u_{g2} will decrease, which will lead to a current $i_{а2}$ decrease, i. e., to a rise in voltages $u_{а2}$ and u_{g1} and, consequently, to a further and even greater increase in current $i_{а1}$ and so on. The resultant avalanche-like process symbolically may be depicted in the form



(VI.4)

It is evident that an identical process will arise during a random decrease in current $i_{а2}$ or voltages u_{g2}, $u_{а1}$, as well as during a rise in voltages u_{g1}, $u_{а2}$. The avalanche-like process will evolve in the opposite direction during a fluctuating change in any of these magnitudes with the opposite sign. In this case, this process will terminate in a circuit reversal to a state of stable equilibrium, where, as a result of tube nonlinear characteristics, the positive feedback loop will be disrupted (or gain K_2 in this loop will become less than unity). This will occur either during blanking of that triode whose grid voltage decreased /221 with a jump, or when an upper bound is placed on the other triode's rising grid voltage due to its grid current. Flip-flop circuits usually are constructed so that both phenomena occur.

Thus, immediately after being cut in, the circuit converts with a jump to one of two possible states of stable equilibrium, while, in the first, triode L_1 is blanked and its plate voltage is maximum ($u_{a1} = U_{a\,max}$) and triode L_2 is unblanked and its plate voltage is minimal ($u_{a2} = U_{a\,min}$); the opposite is true in the second state. Each circuit reversal -- its conversion from one state of stable equilibrium to the other -- occurs only due to trigger pulse stimulus (see Figure VI.4a). Triode plate voltages change with a jump in opposite directions during reversal to an identical magnitude equal to output pulse amplitude:

$U_{вых1} = U_{вых2} = U_{a\,max} - U_{a\,min}$.

We will examine basic considerations concerning circuit parameter selection.

Resistances R_{a1}, R_{a2} are selected using the same considerations used in pulse amplifiers and usually comprise tens or unities of kilohms (see Chapter III, § 2).

Divider resistances R and R_g selected must be large enough to weaken divider shunting action to amplifying stages. In order that a divider connected to an unblanked tube plate essentially does not decrease its load impedance $R_н$ (i. e., stage gain), this condition must be satisfied

$$R + R_g \gg R_a. \tag{VI.5}$$

Here

$$R_н = \frac{R_a(R + R_g)}{R_a + R + R_g} = \frac{R_a}{1 + \frac{R_a}{R + R_g}} \approx R_a. \tag{VI.6}$$

Unblanked tube grid current flows across the divider connected to blanked tube plate. As a result, blanked tube plate potential drops by magnitude $I_g R_1$. Since the unblanked tube grid--cathode path shunts divider output when grid current is present ($r_{g0} \ll R_g$), then equivalent resistance between unblanked tube grid and cathode will equal

$$R_{g0} = \frac{R_g r_{g0}}{R_g + r_{g0}} \approx r_{g0}. \tag{VI.7}$$

Therefore, blanked tube plate voltage turns out to equal

$$U_{a\,макс} = E_a - I_g R_a = E_a - \frac{E_a R_a}{R_a + R + R_g} \approx E_a - \frac{E_a R_a}{R_a + R + r_{ga}},$$

or, since $r_{ga} \ll R + R_a$, /222

$$U_{a\,макс} \approx E_a - \frac{E_a R_a}{R_a + R} = E_a \cdot \frac{1}{1 + \frac{R_a}{R}}. \qquad \text{(VI.8)}$$

In order that this voltage differ slightly from source voltage

$$U_{a\,макс} \approx E_a, \qquad \text{(VI.8a)}$$

this condition must be satisfied

$$R \gg R_a. \qquad \text{(VI.9)}$$

In accordance with conditions (VI.5) and (VI.9), resistances R and R_g on the order of hundreds of kilohms are selected.

Each divider transfer constant equals

$$K_д = \frac{\Delta u_{g1}}{\Delta u_{a2}} \approx \frac{\Delta u_{g1}}{\Delta u_{a1}} = \frac{R_g}{R + R_g} < 1. \qquad \text{(VI.10)}$$

Divider parameters and negative bias E_g magnitude are selected so that, when voltage $U_{a\,мин}$ is supplied to divider input from unblanked tube plate, the other tube will be blanked by divider output voltage $U_{g\,мин}$; when voltage $U_{a\,макс}$ is supplied to divider input from blanked tube plate, the other tube will be unblanked under the influence of divider output voltage $U_{g\,макс}$. If the tube connected to divider output is removed, then its minimum (for $U_{a\,мин}$) and maximum (for $U_{a\,макс}$) output voltages, in accordance with Kirchhoff's second law, considering (VI.5) and VI.10) will equal:

$$\left.\begin{aligned} U_{g\,мин} &= \frac{U_{a\,мин} + E_g}{R + R_g} R_g - E_g = (U_{a\,мин} + E_g) K_д - E_g; \\ U_{g\,макс} &= \frac{U_{a\,макс} + E_g}{R_a + R + R_g} R_g - E_g \approx (U_{a\,макс} + E_g) K_д - E_g. \end{aligned}\right| \qquad \text{(VI.11)}$$

One may accept that $U_{g\,мин} = 2E_{go}$ for reliable tube blanking; voltage $U'_{g\,макс}$ must be greater than zero for reliable tube unblanking and stabilization of its output voltage $U_{a\,мин}$. Then, grid current will arise in it when the tube is installed and, since $R \gg r_{gc}$, its input voltage will be clamped almost at the zero level $U'_{g\,макс} = 0$ (see Chapter V, § 3).

One may accept roughly that $U'_{g\,макс} = E_{g'} > 0$*. Considering these constraints, ratios (VI.11) will be written in the form

$$\left.\begin{aligned}(U_{a\,мин} + E_g)K_1 - E_g &= 2E_{go};\\ (U_{a\,макс} + E_g)K_1 - E_g &= |E_{go}|.\end{aligned}\right\} \qquad \text{(VI.11a)}$$

Subtracting the first equality from the second, we will get $(U_{a\,макс} - U_{a\,мин})K_1 = 3E_{go}$ /223

hence

$$K_1 = \frac{3|E_{go}|}{U_{a\,макс} - U_{a\,мин}} = \frac{3|E_{go}|}{U_{вых}}. \qquad \text{(VI.12)}$$

where $U_{вых} = U_{a\,макс} - U_{a\,мин}$ -- output pulse amplitude; value $U_{a\,макс}$ is determined in accordance with (VI.8), while value $U_{a\,мин}$ will be found from the load line intersection point for selected resistance R_a with the static plate characteristic for grid voltage $U'_{g\,макс} = 0$ (see Figure III.13a, for example).

Ratio (VI.12 makes it possible from values $U_{вых}$ and E_{go} to compute requisite magnitude K_1 and then, based on (VI.10), to refine resistance R and R_g magnitudes.

Negative bias E_g magnitude is determined from the second (VI.11a) equality:

$$E_g = \frac{K_1 U_{a\,макс} - |E_{go}|}{1 - K_1} \qquad \text{(VI.13)}$$

Since stage gains in a symmetrical circuit are identical $K_I = K_{II} = K$, then

*Conditions $U_{g\,мин} = 2E_{go}$, $U'_{g\,макс} = E_{go}$ do not consider the possibility of optimum circuit parameter selection from the point of view of circuit stability and speed.

amplitude self-excitation condition (VI.2a) may be written in the form

$$K_1 = K^2 > 1 \qquad \text{or} \qquad K > 1 \tag{VI.14}$$

Expressing arm gain based on (III.49), considering ratios (VI.6) and (VI.10), we will get

$$|K| = \frac{\mu R_a}{R_i + R_a} \cdot \frac{R_g}{R + R_g} \approx \frac{\mu R_a}{R_i + R_a} \cdot K_1 > 1 \tag{VI.14a}$$

This condition is satisfied automatically if divider transfer constant is selected in accordance with (VI.12). Actually, since always $K_1 < 1$, then it follows from (VI.12) that output pulse amplitude must satisfy inequality $U_{out} > 3E_g$, satisfaction of which is insured through selection of sufficiently-large plate load R_a resistances. If this inequality is satisfied, then we will get $K > 1$ since a change in voltage at stage input (at triode grid) by magnitude E_g means that voltage at stage output (divider connected to its plate) must change by a magnitude of at least $3E_g$.

EXERCISE VI.1

a) How will triode L_2 plate voltage change if triode L_1 loses emission (filament burns out) at the moment: when triode L_2 was unblanked; when triode L_2 was blanked? How will circuit state change when the bad triode is replaced (under voltage) by a good one?

b) We will assume that triode L_1 is unblanked in initial flip-flop state, triode L_2 is blanked, conditions (VI.12a) are satisfied, and the circuit is triggered by a real trigger pulse with finite porch steepness. We will disregard for the time being the influence of circuit stray capacitances and we will consider that the reversal process itself occurs instantaneously. Under these conditions, draw grid voltage and curves for two cases: if the trigger pulse /224 is supplied to triode L_2 grid; if it is supplied to triode L_1 grid.

For each instance, determine what the trigger pulse polarity and minimum

amplitude must be. In what instance will flip-flop reversal begin earlier? In what instance will an active (avalanche-like) flip-flop reversal occur?

(Page 475)

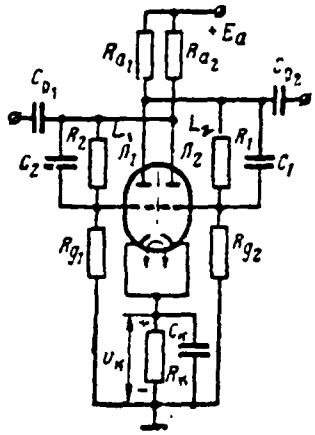


Figure VI.6. Flip-Flop With Two Plate-Grid Couplings and Self-Bias

The external negative bias source in a symmetrical flip-flop may be eliminated if self-bias, obtained with the aid of cathode load impedance $R_к$ common for both stages, is used. A symmetrical flip-flop circuit with two plate-grid couplings and self-bias is depicted in Figure VI.6. Current of one (unblanked) triode in each state of stable equilibrium flows across resistance $R_к$. Since flip-flop arm parameters are identical, then $I_{a1}=I_{a2}=I_a$ and constant voltage drop $U_к=I_aR_к$ applied with a "minus" to the grids is created across resistance $R_к$. Temporary pulsations of this voltage arise only at the moments of circuit reversal and are smoothed by capacitor $C_к$. A capacitance on the order of 0.001--0.01 uF is selected for this capacitor, depending on the duration of the transient processes in the circuit. This circuit does not differ from the previous one where operating principle is concerned. If one accepts, as usual, that $U_{g\,max}=2E_{g0}$, $U_{g\,max}=|E_{g0}|$, then, instead of ratios (VI.11a), one should write

$$U_{a\,max}K_2-U_к=2E_{g0};$$
$$U_{a\,max}K_1-U_к=|E_{g0}|.$$

hence divider gain, as usual, will be expressed by ratio (VI.12)

$$K_д = \frac{3|E_{g0}|}{U_{a\,макс} - U_{a\,мин}},$$

while self-bias magnitude equals

$$U_д = K_д U_{a\,макс} - |E_{g0}|. \qquad (VI.15)$$

i. e., less than the magnitude of external bias determined by expression (VI.13). This is explained by the fact that smaller currents (voltage $U_д$, as opposed /225 to voltage E_g, is not applied to the dividers) flows across the dividers in both states of stable equilibrium when external bias source E_g and the same values for R_a, R, and R_g are absent. As a result, voltage drops across resistances R_g applied with a "plus" to triode grids and, consequently, the negative bias magnitude required to create plate-grid limiting, decrease accordingly. Resultant output pulse amplitude $U_{вых} = U_{a\,макс} - U_{д\,мин}$ is somewhat less than in the previous circuit.

It is demonstrated in Figure VI.6 that trigger pulses are supplied across coupling capacitors $C_{св1}$, $C_{св2}$, not to grids (as in Figure VI.5) but to triode plates. Here, a pulse supplied to given triode plate is transmitted from this plate across the appropriate divider to the other triode grid and the triggering mechanism is not altered. As will be demonstrated below, triggering to plates is more preferable than triggering to grids, given that trigger tubes are used.

EXERCISE VI.2.

a) Explain why self-bias flip-flop output pulse amplitude at identical E_a, R_a, R, and R_g values is less then for a flip-flop with an external bias source. How will a change in resistance R_a (that does not disrupt circuit self-excitation conditions) impact upon pulse amplitude?

b) How will capacitor C_1 breakdown impact upon Figure VI.6 circuit operation?

c) What is the polarity of the pulses supplied when plates are triggered

and to what triodes (unblanked, blanked) are they supplied? What must the minimum amplitude of these pulses be? (Page 477)

2. Flip-Flop Resolving Time. Influence of Stray, Coupling, and Accelerating Capacitances

Flip-flop voltage curves depicted in Figure VI.5b are idealized since stray circuit capacitance influences are not taken into account. These capacitances were depicted in Figure VI.5a by a dotted line and, in the main, are the input and output capacitances of each tube.* Presence of stray capacitances precludes instantaneous (spasmodic) grid and plate voltage changes, i. e., stretches flip-flop triggering and reversal processes and distorts the shape of its output voltages. Therefore, flip-flop conversion from one state of stable equilibrium to another occupies a certain finite time interval, as a result of which flip-flop speed and its resolving capability are reduced.

The least time interval between adjacent trigger pulses during which assured flip-flop operation still occurs from each pulse is referred to as flip-flop /226 resolving capability or resolving time $t_{разр}$.

Resolving time determines the greatest frequency of assured flip-flop operation (if trigger pulses act in the form of a periodic train) $F_{ср.\,макс} = \frac{1}{t_{разр}}$ and the least pulse duration, which may be developed by the flip-flop $t_{и.\,мин} = t_{разр}$. Therefore, the tendency in high-speed electronic devices, computers for example, is to use flip-flops with the highest possible resolving capability, i. e., with the least resolving time.

One may represent resolving time in the form of the sum of three time intervals -- trigger time, reversal time, and recovery time:

$$t_{разр} = \Delta t_{упр} + \Delta t_{опр} + \Delta t_{в}. \qquad \text{(VI.16)}$$

*Capacitance $C_{э}$ also comprises a circuit capacitance, while capacitance $C_{выс}$ also comprises a circuit and a load capacitance connected to flip-flop plate (input capacitance of the next stage).

Trigger time $\Delta t_{зад}$ is understood to mean the time the flip-flop is acted upon by the trigger pulse to the reversal threshold, i. e., the interval from the onset of the trigger pulse action until the onset of positive feedback loop action.

Reversal time $\Delta t_{пер}$ is understood to mean the duration of the avalanche-like process of converting the flip-flop from one state of stable equilibrium to the other, i. e., the time the positive feedback loop is active.

Recovery time $\Delta t_в$ is understood to mean the duration of the transient processes arising following reversal, i. e., after the positive feedback loop closes. We will examine what each of these intervals depends on.

We will assume that triode L_1 in the initial state in the Figure VI.5a circuit is unblanked, while triode L_2 is blanked, and that flip-flop triggering occurs by a negative square pulse supplied to triode L_1 grid. We will accept that trigger pulse amplitude $E_{г}^{(-)} > U_{зап}^{(-)} > \left|\frac{U_{g\,max} - E_{g0}}{K}\right|$ in accordance with (VI.3), i. e., not sufficient for direct triode L_1 blanking, but sufficient for triode L_2 unblanking. This insures that the positive feedback loop closes, i. e., an active reversal characteristic (see Exercise VI.1b). Flip-flop voltage curves under these conditions are depicted in Figure VI.7. The dotted line indicates absence of accelerating capacitors C_1, C_2, while the solid lines indicate when these capacitors are present.

Triggering time. Initially, we will assume that accelerating capacitors are absent. Under the influence of trigger pulse vertical porch (Figure VI.7a), voltage u_{g1} due to the influence of input capacitance $C_{вх1}$ will drop only gradually (Figure VI.7b) due to charging of this capacitance from the trigger pulse generator across coupling capacitor $C_{р1}$. An equivalent circuit for capacitance $C_{вх1}$ charging network is depicted in Figure VI.8a, where $R_г$ -- trigger pulse generator /228 output resistance and, since triode L_1 is unblanked, then $C_{вх}$ should be understood as dynamic input capacitance equalling $C_{вх\,д} = C_{вх} + C_{ас}(1 + K)$ in accordance with (III.55). Disregarding in this circuit large resistance $R_{с1}$ (it is connected

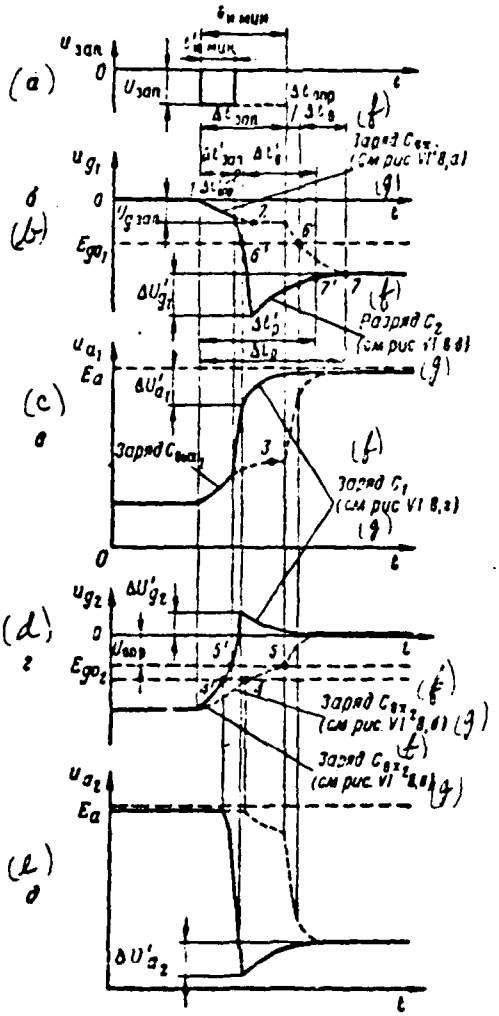


Figure VI.7. Flip-Flop Voltage Curves Considering Influence of Stray and Accelerating Capacitances. (f) -- Charge; (g) -- See Figure

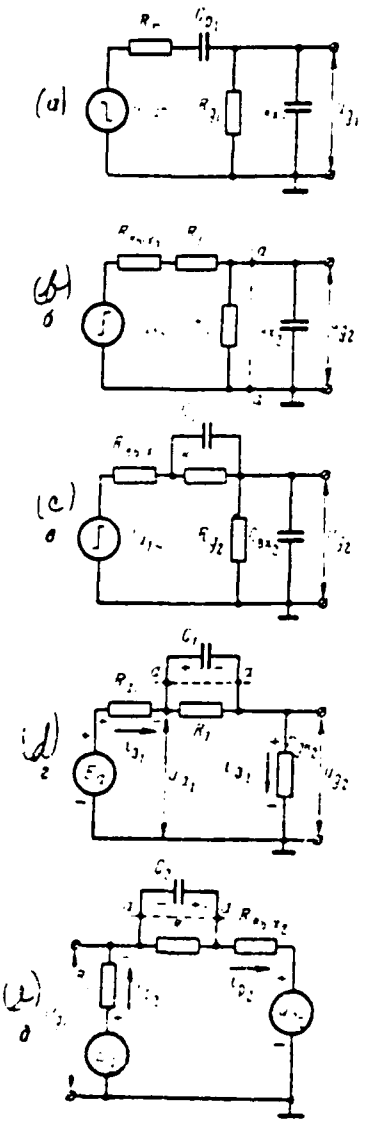


Figure VI.8. Equivalent Flip-Flop Stray and Accelerating Capacitance Charging (Discharging) Circuits.

in parallel with capacitance $C_{вых}$ and $R_{gl} \gg R_i$)*, for the time constant of the examined circuit we will get

$$\tau_{зар.\,вх1} \approx R_i \frac{C_{вх1} C_{p1}}{C_{вх1} + C_{p1}}. \qquad \text{(VI.17)}$$

During time $\Delta t \approx 3\tau_{зар.\,вх1}$ (time interval between points 1 and 2 in Figure VI.7b), voltage u_{g1} will reach steady-state value $U_{g\,зап}$ determined by the capacitance divider $C_{p1}, C_{вх1}$ arm relationship:

$$U_{g\,зап} = -U_{зап} \frac{C_{...}}{C_{p1} + C_{вх1}} = -U_{зап} \frac{1}{1 + \frac{C_{вх1}}{C_{p1}}} \qquad \text{(VI.18)}$$

(we are assuming that, during this time, the circuit still will not be brought to the reversal threshold).

Since triode L_1 operates in the amplifying mode, then, due to the voltage u_{g1} decrease, its plate voltage u_{a1} rises but reaches the steady-state value somewhat later (point 3 in Figure VI.7c) due to the additional influence of output /229 capacitance $C_{вых1}$. This capacitance is charged across the amplifying stage output resistance, which, in accordance with (III.50), equals

$$R_{вых1} = \frac{R_i R_{...}}{R_{...} - R_{...}},$$

i. e., with time constant

$$\tau_{зар\,вых1} = R_{вых1} C_{вых1}. \qquad \text{(VI.19)}$$

As a result of additional integrating action of capacitance $C_{вых1}$, voltage u_{a1} during a decrease in voltage u_{g1} by an exponent rises already not by the law

*Here and below, for approximate time constant location, just as before, we will disregard network elements exerting minor influence on pulse porch flow, i. e., of spectrum high-frequency components.

of exponents -- the rate of rise of this voltage at first increases, and then decreases. The voltage u_{a1} rise is transmitted across divider R_1, R_{g2} to triode $-_2$ grid. However, the voltage u_{g2} increase additionally will be constrained due to influence of input capacitance $C_{вх2}$. An equivalent charging circuit for this capacitance, if accelerating capacitor C_1 is absent, is depicted in Figure VI.8b. Employing the equivalent generator theorem relative to points aa, for the capacitance $C_{вх2}$ charging time constant we will get:

$$\tau_{зар.вх2} = \frac{(R_{вых1} + R)R_{g2}}{R_{вых1} + R + R_{g2}} C_{вх2} \approx \frac{RR_{g2}}{R + R_{g2}} C_{вх2}. \qquad (VI.20)$$

Equating expressions (VI.20) and (VI.19), we see that, since $\frac{RR_{g2}}{R + R_{g2}} \gg R_{вых1}$ ($R_1 \gg R_a$; $R_{g2} \gg R_a$; $R_1 > R_{вых1}$) , and, in addition, the triode input capacitance is greater than its output capacitance $C_{вх1} > C_{вых1}$, then $\tau_{зар.вх2} \gg \tau_{зар.вых1}$. Therefore, voltage u_{g2} will rise significantly more slowly compared to voltage u_{a1} (Figure VI.7d). Here, the law of voltage u_{g2} rise differs even more from the law of exponents than does the law of voltage u_{a1} rise as a result of capacitance $C_{вх2}$ additional integrating influence. At the moment when voltage u_{g2} reaches cutoff voltage (point 4 in Figure VI.7d), triode L_2 will unblank. However, satisfaction of self-excitation condition (VI.2a) means that voltage u_{g2} actually must somewhat convert cutoff voltage so that the triode operating point will leave the transfer characteristic sector with sufficiently-large transconductance. Therefore, the avalanche-like reversal process will begin even later -- when voltage u_{g2} reaches a certain threshold value $U_{отр} > E_{g2}$ (point 5 in Figure VI.7d).

We will note that, in the interval between points 4 and 5, when triode L_2 is unblanked, dynamic input capacitance $C_{вх2}$ already [illegible] be considered in expression (VI.20). Therefore, the rate of voltage u_{g2} rise in this interval will become even less.

Thus, trigger time $\Delta t_{зад}$ is determined by the interval between points 1 and 5 and is significant due to influence of capacitances $C_{вх}$, $C_{вых1}$, and mainly due

* $R_{вых1} \ll R_1$.

to the large capacitance $C_{вх2}$ charging time constant (initially static, then /230 dynamic). It is evident that, if the trigger pulse ceases before the positive feedback loop begins to operate, then there will be no circuit reversal. Therefore, the minimum required trigger pulse duration must satisfy condition [illegible] (Figure VI.7a).

A slight triggering time decrease may be achieved through increasing the steepness of the voltage u_{g1} porch while the trigger pulse is active. In accordance with (VI.17), a trigger pulse generator with slight output resistance R should be used for this purpose. However, this will lead to stretching the reversal process since slight resistance $R_г$ will shunt the positive feedback loop in the triode $Л_1$ grid--cathode path.

The capacitance of coupling capacitors needs to be decreased to 20--50 pF in order to reduce this harmful trigger pulse generator influence on the flip-flop (as well as the reverse influence of flip-flop unblanked triode slight resistance r_i when grid current to the generator is present). However, here flip-flop input networks for trigger pulses are converted into differentiators which, in turn, will lead to the following. First, the duration of a differentiated (chopped) trigger pulse in the unblanked triode grid already may turn out to be insufficient for flip-flop reversal. Second, as a trigger pulse of sufficiently-great duration $t_и > \Delta t_{триг}$ is differentiated, there is the danger of flip-flop misoperation by a pulse of opposite polarity arising at input network output during differentiation of the trigger pulse droop. In addition, a decrease in capacitance $C_в$, in accordance with (VI.18), will lead to a reduction in capacitance divider $C_{вх}$, $C_{вх1}$ transfer constant and, consequently, in the amplitude of that pulse at this divider's output (at triode $Л_1$ grid). Therefore, a trigger pulse generator must generate pulses of appropriately-great amplitude.*

We now will examine how connection of accelerating capacitors will impact upon triggering time. Presence of accelerating capacitor C_1 essentially does not impact upon the porch steepness of voltages u_{g1}, u_{c1}. However, the rate of voltage u_{g2} rise now increases significantly. Actually, when capacitor C_1 is

*Based on the reasons given, use of trigger tubes (see below) is the most effective way to decrease the mutual influence of the trigger pulse generator and flip-flop.

present, the equivalent circuit for the capacitance $C_{ак2}$ charging network may be depicted in accordance with Figure VI.8c. Disregarding the influence of large resistances R_1 and R_{g2} (they are connected in parallel to capacitances C_1 and [illegible] , we will get for this network's time constant

$$\tau_{зар\ ак2} \approx R_{вых1} \frac{C_1 C_{ак2}}{C_1 + C_{ак2}} \qquad (VI.21)$$

Equating expressions (VI.21) and (VI.20), we see that, since $R_{вых1} \ll \frac{R_a R_g}{R_a + R_{g2}}$, while $\frac{C_1 C_{ак2}}{C_1 + C_{ак2}} < C_{ак2}$, then $\tau_{зар\ ак2} \ll \tau_{зар.ак}$.

Therefore, when accelerating capacitors are present, the interval between points 1 and 5' already determine triggering time, i. e., it is reduced greatly: $\Delta t_{зап} \ll \Delta t_{зап}$. The minimum trigger pulse duration required for triggering is reduced accordingly $t_{и\ мин} \ll t_{и\ мин}$ (Figure VI.7a). In addition, capacitor C_1 in conjunction with capacitance $C_{ак2}$ for the voltage u_{a1} porch (change) forms a capacitance divider with transfer constant

$$K_C = \frac{C_1}{C_1 + C_{ак2}} = \frac{1}{1 + \frac{C_{ак2}}{C_1}} \qquad (VI.22)$$

Therefore, selecting a sufficiently-large capacitor C_1 capacitance ($C_1 \gg C_{ак2}$) , it is possible to increase the amplitude of the change of voltage transmitted across the divider from triode L_1 plate, making it possible to decrease trigger pulse amplitude accordingly.

The accelerating capacitor role increases even more when plates are triggered (based on the Figure VI.6 circuit). Actually, in this event, second divider R_2, R_{g1} across which a trigger pulse is transmitted to this grid from the blanked triode L_2 plate additionally will influence the amplitude and steepness of the pulse porch at triode L_1 grid. A capacitance divider comprising three series-connected capacitances C_{p1}, C_2, $C_{вх1}$ is formed for the trigger pulse when capacitor C_2 is present. An increase in this divider's transfer constant requires an increase in both the capacitance of coupling capacitor C_{p1} and that of accelerating capacitor C_2.

Reversal time. The positive feedback loop goes into action at moment t_5

(without accelerating capacitors) or t_5' (when they are present). Therefore, the rate of grid and plate voltage change rises sharply. A bound is placed on this rate for voltages u_{a1} and u_{a2} by the capacitance $C_{выт1}$ charge across resistance $R_{выт1}$ and the discharge of capacitance $C_{выт2}$ across resistance $R_{выт2}$, respectively ($R_{выт1}$ and $R_{выт2}$ -- amplifier output resistances which unblank simultaneously at the reversal stage). A bound is placed on the rate of voltage u_{g1} and u_{g2} change by the recharge of capacitances $C_{вх1}$ and $C_{вх2}$, respectively.

This recharge occurs in accordance with (VI.20) across large equivalent resistances $\frac{R R_{g2}}{R + R_{g2}}$ (for $C_{вх2}$) and $\frac{R_1 R_{g1}}{R_1 + R_{g1}}$ (for $C_{вх1}$) when accelerating capacitors are absent; when they are present, in accordance with (VI.21), it occurs across slight resistances $R_{выт1}$ and $R_{выт2}$, i. e., significantly faster. Therefore, all changes of potential in the circuit occur at high speed. When voltage /232 u_{g1}, decreasing, reaches cutoff voltage E_{go1} (points 6 or 6' in Figure VI.7b), triode L_1 blanks, the positive feedback loop is disrupted, and the avalanche-like process ceases.*

Consequently, reversal time equals the interval between points 5 and 6 without accelerating capacitors and the interval between points 5' and 6' when these capacitors are present, while $\Delta t'_{опр} < \Delta t_{опр}$. All other conditions being equal, reversal speed is greater, the greater the resulting gain in the feedback loop. Therefore, reversal time, just like triggering time, decreases when the capacitance of accelerating capacitors increases (here, the transfer constant of the capacitance dividers across which plate voltage changes is transmitted to grids) and when triodes with large transfer characteristic transconductance are used (here, triode gains increase).

Recovery time. After the feedback loop closes, grid and plate potentials continue to change to their fixed values, but already significantly more slowly -- at the rate of the passive processes of charging (discharging) of the corresponding capacitances.

*More precisely, this occurs somewhat earlier, when voltage u_{g1} converges with cutoff voltage to the extent that triode L_1 transconductance already will be insufficient to satisfy the self-exitation condition.

If no accelerating capacitors are present, then, since triode L_1 is blanked already, the voltage u_{a1} rise, which occurs at the rate of capacitance $C_{вых1}$ charge across resistance R_{a1} to value $U_{a1\ макс} \approx E_a$, is the source of further changes of potentials in the circuit. Remaining voltages accordingly change more slowly, while the last to reach its steady-state level is voltage u_{g1} (point 7 in Figure VI.7b). This also determines recovery time $\Delta t_в$.

When accelerating capacitors are present, recovery time rises due to their recharging. Actually, in the initial state, capacitor C_1, connected to unblanked triode L_1 plate, was charged to voltage

$$U_{C1\ нач} = U_{a1\ нач} - U_{g1\ нач}, \tag{VI.23}$$

while capacitor C_2, connected to blanked triode L_2 plate, was charged to voltage

$$U_{C2\ макс} = U_{a2\ макс} - U_{g1\ макс} \approx E_a > U_{C1\ нач}. \tag{VI.24}$$

We will assume that, during triggering and reversal time, voltages u_{c1} and u_{c2} essentially do not change (capacitances C_1 and C_2 are sufficiently large) and now we will disregard the influence of stray capacitances. Following reversal, capacitor C_1 must be charged to voltage $U_{C1\ макс} \approx E_a$, while capacitor C_2 must be discharged to voltage $U_{C2\ нач} = U_{a2\ нач} - U_{g1\ нач}$.

The capacitor C_1 charging network equivalent circuit is depicted in /233 Figure VI.8d. In this circuit, r_{g2} -- slight resistance of triode L_2 grid--cathode path when its grid current is present. A branch comprising resistance R_{g2} and bias source E_g parallel to this resistance is not shown (one may disregard the influence of this branch since $r_{g2} \ll R_{g2}$). Using the theorem of the equivalent generator relative to points aa, considering that $r_{g2} \ll R_1$, $R_{a1} \ll R_1$, for this network's time constant we will get:

$$\tau_{вых1} = \frac{(R_{a1} + r_{g2})\,R_1}{R_{a1} + r_{g2} + R_1} C_1 \approx R_{a1} C_1. \tag{VI.25}$$

Charging current i_{a1}, flowing across resistances R_{a1} and r_{g2}, reduces triode L_1 plate potential and increases triode L_2 grid potential. This current is maximum

at the first moment and then drops by an exponent with time constant $\tau_{зар1}$. Therefore, during reversal time, voltage u_{a1} does not reach fixed value $U_{a\,макс}$ by magnitude $\Delta U'_{a1} = I_{зар1} R_{a1}$ and, during the recovery process, rises to this value by an exponent with time constant $\tau_{зар1}$ (Figure VI.7c). Voltage u_{g2} initially with a jump will exceed the zero level by magnitude $\Delta U'_{g2} = I_{зар2} r_{g2}$, and then will decrease do this level by an exponent with the same time constant (Figure VI.7d). Since triode L_2 is unblanked, then a negative exponential excursion of its plate voltage with amplitude $\Delta U'_{a2} = K \Delta U'_{g2}$ corresponds to a voltage u_{g2} positive exponential excursion (Figure VI.7e).

The equivalent circuit for the capacitor C_2 discharging network is depicted in Figure VI.8e. Using the theorem of the equivalent generator relative to points aa, considering that $R_{вых2} \ll R_{g1}$, for this network's time constant we will get:

$$\tau_{разр2} = \frac{R_2 (R_{g1} + R_{вых2})}{R_2 + R_{g1} + R_{вых2}} C_2 \approx \frac{R_2 R_{g1}}{R_2 + R_{g1}} C_2. \qquad \text{(VI.26)}$$

Discharging current i_{p2} flowing across resistance R_{g1}, reduces triode L_1 grid potential. Therefore, immediately following completion of a reversal, voltage u_{g1} turns out to be lower than its fixed value $U_{g1\,мин}$ by magnitude $\Delta U'_{g1} = I_{p2} R_{g1}$, and then rises to this value by an exponent with time constant $\tau_{разр2}$.

Equating expressions (VI.25) and (VI.26), we will get $\tau_{разр2} > \tau_{зар1} \left(\frac{R_2 R_{g1}}{R_2 + R_{g1}} \gg R_{a1} \right)$. Therefore, voltage u_{g1} will attain its fixed value later than do voltages u_{a1}, u_{g2}, and u_{a2} (point 7' in Figure VI.7b).

Recovery time equals the interval between points 6' and 7' /234

$$\Delta t'_в \approx 3\tau_{разр2} = 3 \frac{R_2 R_{g1}}{R_2 + R_{g1}} C_2 \qquad \text{(VI.27)}$$

During time $\Delta t'_в$, flip-flop sensitivity to trigger pulses decreases. Actually, the stimulus of the subsequent pulse must lead to triode L_1 unblanking. However, if this pulse leads to the fact that capacitor C_2 discharge will cease, i. e., when voltage u_{g1} is less than its fixed value $U'_{g1\,мин}$, then the amplitude of this pulse may turn out to be insufficient. Therefore, the danger arises of a "lapse" of this (and, therefore, of the subsequent) trigger pulse.

Thus, inclusion of accelerating capacitors permits a decrease in triggering time and, consequently, use of shorter trigger pulses, a reduction in trigger pulse amplitude (especially when triggering plates), and reduced reversal time, i. e., to increase the steepness of the output voltages during this time.* But, on the other hand, this will lead to a rise in recovery time, a reduction in flip-flop sensitivity following reversal, and appearance of additional distortions in output voltage shape. Stretching the porch of the positive change in plate voltage blanking the tube is the most significant of these distortions (Figure VI.7c). In accordance with (VI.25), the duration of this porch turns out to equal

$$t_{\text{п}}^{(+)} \approx 3\tau_{\text{зап1}} = 3R_{a1}C_1. \qquad \text{(VI.28)}$$

Based on the reasons given, the capacitance of the accelerating capacitors is selected from compromise considerations -- either from the condition of complete divider frequency compensation (III.46) $CR = C_{\text{вх.л}}R_g$, which, when resistances R and R_g are approximately equal, will provide $C \approx C_{\text{вх.л}}$ or several times greater $C \approx (1 \div 3)C_{\text{вх.л}}$. Since triode input dynamic capacitance usually will fall within the limits $C_{\text{вх.л}} = 25 \div 50$ pF, then C = 25 ÷ 150 pF.

An increase in flip-flop resolving capability calls for use of triodes with slight interelectrode capacitances and great transfer transconductance (6N6P and 6N15P triodes, for instance), as well as a decrease in resistances R_a, R, and R_g, which will lead to a decrease in the recharge time of all stray and accelerating capacitances.** A resistance R_a decrease also will lead to a decrease in tube dynamic input capacitances, which correspondingly makes it possible to decrease /235 accelerating capacitors and thereby reduce recovery time. Connection of load to tube plate across an output cathode follower is employed to reduce flip-flop output capacitances and the capability of operating a low-impedance load. These measures are employed to reduce resolving time by approximately 1 usec, i. e., to obtain a frequency of assured flip-flop operations up to 1 MHz. A further

*In addition, as will be demonstrated below, accelerating capacitors increase flip-flop symmetrical triggering reliability.

**First, when resistances R_a, R, and R_g are reduced, the magnitude of the grid and plate changes of voltage decrease, which may lead to disruption of flip-flop d-c operating mode stability. Second, power dispersed in the unblanked tube grid rises. Both reasons place a lower bound on the magnitude of these resistances.

increase if flip-flop speed is achieved by introduction of high-frequency compensation to plate networks (see Chapter III, § 3) connected to the feedback network at cathode follower divider output (this makes it possible to decrease accelerating capacitances up to 5--20 pF), by a decrease in the magnitude of grid and plate voltage changes by using clamping (limiting) diodes, and by replacing triodes with pentodes. These methods permit an increase in the frequency of assured flip-flop operation to about 15 MHz.

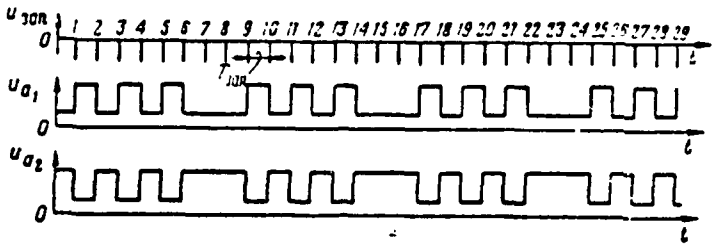


Figure VI.9. Flip-Flop Irregular Operation With Periodic Pulse "Lapses."

EXERCISE VI.3

a) As was noted, due to the requirement to decrease the capacitances of coupling capacitors, there is a danger of flip-flop misoperations due to trigger pulse differentiation in input networks. When is this danger the least, when positive pulses are used for triggering or when negative pulses are used?

b) How does an increase in coupling capacitor capacitance impact upon flip-flop operation?

c) Explain the reason for onset of periodic trigger pulse "lapses" arising each time following a series of flip-flop operations in accordance with Figure VI.9. (Page 477)

3. Symmetrical Flip-Flop Trigger Circuits

A flip-flop trigger circuit must insure:

-- reliable flip-flop reversal by means of pulses (or changes) of the smallest possible amplitude;

-- minimum triggering time, i. e., trigger pulse duration;

-- absence of misoperations; /236

-- least possible influence of trigger pulse generator output networks on the flip-flop and flip-flop input networks on the trigger pulse generator.

As we already have seen, satisfaction of the first three requirements best is insured during negative pulse triggering. Triggering occurs across trigger tubes, used to insure trigger pulse generator cut off from the flip-flop immediately following the beginning of reversal to decrease mutual flip-flop--trigger pulse generator influence. In addition, thanks to its electrical valve-like action, trigger tubes eliminate false flip-flop triggering by opposite-polarity pulses. Flip-flop triggering may be asymmetrical (individual) and symmetrical (common or counting).

In asymmetrical triggering, the flip-flop has two individual trigger pulse inputs, with pulses reversing the flip-flop in one direction supplied to each input. This triggering is employed usually when the flip-flop is used as a pulse stretcher, i. e., for shaping pulses whose duration must equal the intervals between two adjacent trigger pulses, each of which generated by an individual generator.

In symmetrical triggering, the flip-flop has one common input for trigger pulses, with each trigger pulse versing the circuit independent of the state which the circuit is in prior to pulse arrival. Such triggering usually is employed when the flip-flop is used for division of the repetition frequency or counting pulses generated by one generator in the form of a periodic train.

Initially, we will examine an asymmetrical triggering circuit. Asymmetrical triggering without triggering tubes may occur across coupling capacitors either to grids as in the Figure VI.5 circuit, or to plates as in the Figure VI.6 circuit. As we already know (see Exercises VI.1, 2), in the first example, the flip-flop is triggered each time by a negative pulse acting upon the unblanked triode grid. In the second case, this is done by a negative pulse acting upon a blanked triode plate. Plate triggering requires greater trigger pulse amplitude and it is advisible to increase the capacitance of accelerating capacitors.

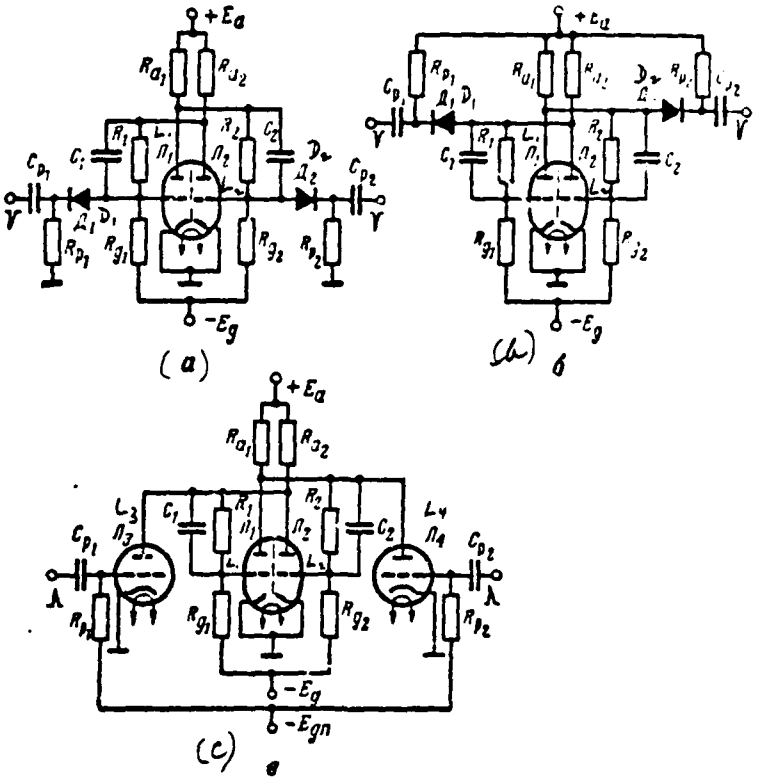


Figure V.10. Standard Circuits for Asymmetrical Triggering of Flip-Flops Across Trigger Tubes.

Standard circuits for asymmetrical triggering across trigger tubes are depicted in Figure VI.10. In Figure VI.10a, negative trigger pulses are supplied to triode grids across isolating circuits C_{p1}, R_{p1}; C_{p2}, R_{p2} and trigger diodes D_1 and D_2. Both diodes are connected so that only negative pulses may pass, thus eliminating the possibility of false triggering by positive pulses.

Let us assume that triode L_1 is unblanked, while triode L_2 is blanked. Since unblanked triode grid voltage is maximum and somewhat higher than zero, then /237 diode D_1 is unblanked (this diode's current facilitates left grid voltage clamping at level $U_{g1\,max} \approx 0$). Diode D_2 is blanked since its plate potential equals

$U_{a\,min}<0$, i. e., less than cathode potential. The circuit may be reversed from this state only by a negative pulse supplied to diode D_1 and across it to triode L_1 grid. Triode L_2 unblanks during triggering, triode L_1 grid voltage drops, and diode D_1 will blank, cutting the corresponding trigger pulse generator out of triode L_1 grid. Diode cutoff will occur at the moment when its plate voltage equates to cathode voltage. This moment will arrive before the trigger pulse porch ceases since, after reversal begins, triode L_1 grid voltage decreases /238 faster than the trigger pulse porch does (see Figure X.29). Diode D_2 unblanks when triode L_2 grid voltage, rising, reaches the zero level, connecting the second trigger pulse generator to this grid. Subsequent flip-flop reversal is possible only by a negative pulse supplied by this generator to diode D_2.

Coupling capacitors C_{p1}, C_{p2} rapidly charge to voltages applied with a "plus" to diode cathodes as negative trigger pulse porches flow across the diodes. These capacitors must discharge completely during resting times. Otherwise, diode cathode potentials will increase gradually due to dynamic bias, which constrains trigger pulse flow. Therefore, isolating network C_pR_p time constants must be sufficiently slight. One drawback of this triggering circuit type is that blanked diode back resistance shunts large blanked arm divider resistance R_g. If this back resistance is not sufficient, initial distribution of potentials in the circuit is disrupted. As a result, circuit operating reliability and stability will deteriorate.

Negative trigger pulses in Figure VI.10b are supplied across diodes D_1, D_2 to flip-flop tube plates. Since the cathodes of both diodes are connected to bus $+E_a$, while potentials of these plates (triode plates) are less than E_a, then both diodes are blanked in the initial state. As was the case in the previous circuit, the diodes do not permit positive trigger pulses to flow to the flip-flop circuit.

We will assume again that triode L_1 is unblanked in the initial state, while triode L_2 is blanked. Then diode D_1 is close to unblanking ($u_{a1} \approx E_a$) and a negative pulse supplied to its cathode will be transmitted to the blanked triode plates and then on to unblanked triode grid, causing a circuit reversal. Diode D_2 is blanked by large reverse voltage ($u_{a2}=U_{a\,min}$) and does not pass a trigger pulse since its amplitude usually is less than difference $E_a - U_{a\,min}$.

Thus, flip-flop triggering occurs each time across that diode connected to the blanked triode. After onset of the reversal, diode D_1 immediately is blanked due to rapid triode L_2 plate voltage decrease. The trigger pulse generator is cut off here more rapidly and more precisely than in the previous circuit since the magnitude and steepness of flip-flop negative plate voltage changes are much greater than the negative grid voltage changes. This is the basic advantage of such a triggering circuit. In addition, as opposed to the previous circuit, diode D_2 during reversal only approximates the unblanking threshold, but will remain blanked. Therefore, the second trigger pulse generator is not connected to the flip-flop circuit and does not retard its reversal.

However, as already noted above, triggering to plates requires greater trigger pulse amplitudes than does triggering to grids. Also, great reverse voltage /239 $E_a - U_{a\,min}$ turns out to be applied to the diode connected to the unblanked triode, creating the danger of semiconductor diode breakdown.

A circuit for asymmetrical flip-flop triggering across trigger triodes L_3, L_4 is depicted in Figure VI.10c. Negative bias E_{gr} is supplied to the grids of these triodes. It selected magnitude is sufficiently great for reliable triode blanking even given maximum possible plate voltage E_a. Therefore, both triodes are blanked prior to triggering and eliminate negative trigger pulse action on the flip-flop.

We again will assume that flip-flop triode L_1 is unblanked, while triode L_2 is blanked. Then, a positive trigger pulse must be supplied to triode L_3 grid to trigger the flip-flop. Triode L_3 unblanks while this pulse is active, its current will flow across plate load impedance R_{a2} common with blanked triode L_2, and an amplified negative pulse transmitted to an unblanked triode L_1 grid will arise in the triode L_3 and L_2 plate. Triode L_3 blanks again before the trigger pulse porch ceases if the rate of triode L_2 plate voltage decrease during the reversal process exceeds trigger pulse porch steepness. This is explained in Figure VI.11, where curves of grid and plate voltages, as well as the law of triode L_3 cutoff voltage level change (dotted line in Figure VI.11a) during the triggering process, are depicted. For clarity, reversal rate is accepted as infinitely large.

A trigger pulse begins to act at moment t_1 and unblanks triode L_3 at moment

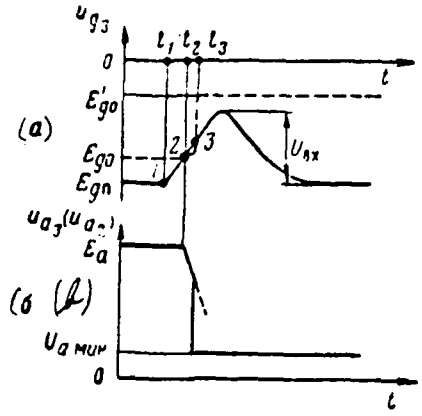


Figure VI.11. Trigger Triode L_3 Action in the Figure VI.10c Circuit.

t_2, when grid voltage compares with the cutoff voltage E_{go} level for maximum plate voltage $U_{a\,макс} \approx E_a$. Further, voltage u_{a3} begins to decrease and, at moment t_3 when triode L_2 unblanks, flip-flop reversal occurs. Here, voltage $u_{a3} = u_{a2}$ with a jump decreases to value $u_{a\,min}$ (Figure VI.11b). However, the lower negative cutoff voltage magnitude must correspond to the lower plate voltage. Therefore, cutoff voltage rises with a jump at the moment of reversal to level $E'_{g0} > E_{gn}$ (this level will fall above value $u_{g3\,макс} = E_{gn} + U_{вх}$, if $U_{вх} < E'_{g0} - E_{gn}$). But, since voltage u_{g3} continues to rise at a lower rate determined only by trigger pulse /240 purch steepness, then, at moment t_3, this voltage again compares with cutoff voltage (point 3) and triode L_3 again is blanked. Thus, trigger tubes unblank alternately only during short time intervals (in Figure VI.11a, in the interval between points 2 and 3), while all the rest of the time they are blanked and reliably cut trigger pulse generators off from the flip-flop. In addition, as a result of the amplifying action of these triodes, trigger pulse amplitude may be significantly decreased compared with the previous trigger circuits.

EXERCISE VI.4

a) How does the influence of blanked diode D_2 back resistance impact upon

distribution of potentials in the Figure VI.10a circuit?

b) What will happen if triode L_4 in the Figure VI.10c circuit malfunctions (loss of emission)? (Page 478)

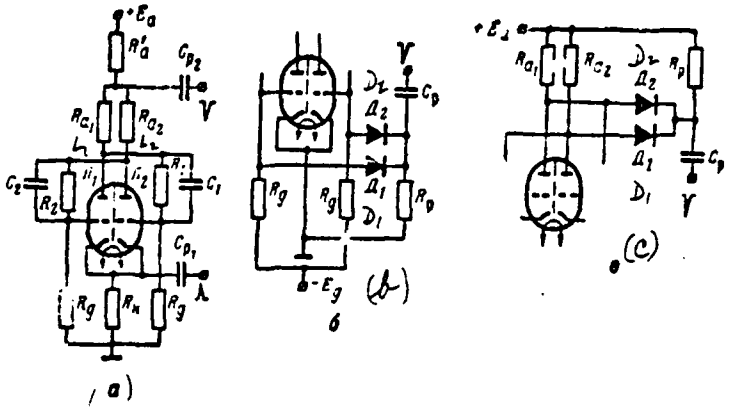


Figure VI.12. Standard Flip-Flop Symmetrical Trigger Circuits.

Standard symmetrical (counting) trigger circuits are depicted in Figure VI.12. Two methods of symmetrical triggering without trigger tubes are depicted in Figure VI.12a.

The first method involves supplying positive trigger pulses across coupling capacitor C_{p1} to flip-flop common cathode load impedance $R_{...}$. Each trigger pulse increases overall cathode potential, i. e., acts simultaneously on both grids like a negative pulse (capacitor $C_{...}$ shunting resistance $R_{...}$ in this case must be absent or it would delay the increase in cathode potential while the trigger pulse is active). Flip-flop reversal occurs from each trigger pulse, which /241 is amplified by the unblanked triode and transmitted from its plate to blanked triode grid. In this triggering method, the trigger pulse generator turns out to loaded at all times to flip-flop cathode network slight input resistance (on the order of 1/S) and, therefore, must be powerful enough. In addition, the trigger

pulse is transmitted to unblanked triode grid across large resistance R_g, which forms an integrator with this triode input resistance. As a result, the trigger pulse porch at grid is stretched, while its amplitude decreases.

The second method involves supplying negative trigger pulses across coupling capacitor C_{c2} to additional common plate resistance R'_a. This method will lead to a decrease in flip-flop output pulse amplitude (plate voltage changes). Actually, since current from one of the triodes always flows across common resistance R'_a, blanked triode plate voltage significantly will be less than value E_a.

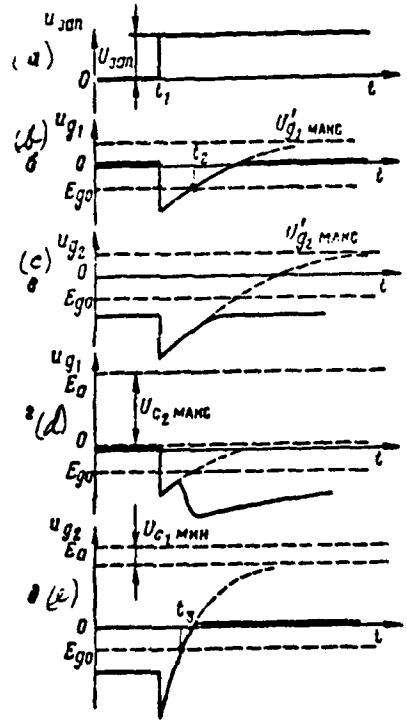


Figure VI.13. For Explanation of Processes During Symmetrical Triggering Without Trigger Tubes.

Symmetrical triggering without trigger tubes always is less reliable than asymmetrical triggering. It is a case where each negative trigger pulse in symmetrical triggering acts not only on unblanked triode grid, but simultaneously also directly on blanked triode grid, hindering its unblanking. If trigger pulse

amplitude here is insufficient, then the circuit will remain in the previous state, i. e., no triggering occurs. If trigger pulse amplitude is sufficient for blanking an unblanked triode, then both triodes will turn out to be blanked while the porch of this pulse is active. Then, triggering only may occur when accelerating capacitors of great capacitance are present. In order to demonstrate this, we will /242 assume that triode L_1 in the Figure VI.12a circuit prior to triggering was unblanked, triode L_2 was blanked, and a positive trigger drop with vertical porch was applied to coupling capacitor C_{p1} at moment t_1 (Figure VI.13a). Drop magnitude is $U_{зап} > E_{g2}$.

For simplicity, we will not consider the influence of circuit stray capacitances.

We will assume initially that accelerating capacitors are absent. Then, grid voltages will change in accordance with Figure VI.13b, c. The drop porch will flow across a coupling capacitor and with a jump increase cathode potential, i. e., reduce both grid voltages to an identical magnitude equalling $U_{зап}$. Therefore, immediately following the action of the drop, just as prior to it, triode L_1 grid voltage remains more positive then triode L_2 grid voltage. Further, in connection with coupling capacitor charging, both grid voltages will rise by an exponent with identical isolating network time constant $\tau_p = C_{p1}R_k$. Here, since both triodes turned out to be blanked, both grid voltages will strive towards identical maximum level $U_{g1\,макс} = U_{g2\,макс}$, determined in accordance with (VI.11). However, since voltage u_{g1} began to rise from a higher value, it is the first at moment t_2 to reach cutoff voltage. Therefore, triode L_1 unblanked until trigger drop action unblanks again, while triode L_2 will remain blanked, i. e., no circuit reversal occurs.

Now we will assume that there are accelerating capacitors in the circuit. Then, prior to triggering capacitor C_2 connected to blanked triode L_2 plate will be charged in accordance with (VI.24) to voltage $U_{C2\,макс} \approx E_a$, while capacitor C_1 in accordance with (VI.23) charges to voltage $U_{C1\,мин} = U_{a1\,мин} - U_{g2\,мин} < U_{C2\,макс}$. We will assume that during triggering and reversal time, these voltages essentially did not change $U_{C1} \approx \text{const}$, $U_{C2} \approx \text{const}$. In this event, grid voltages will change in accordance with Figure VI.13d, e. At moment t_1, just as before, both grid voltages with a jump will drop by trigger drop magnitude $U_{зап}$, and then further will begin to rise with the isolating network time constant. However, the levels to which these voltages will strive now will turn out to be different: voltage

u_{g1} will strive towards level $E_a - U_{a2\,max} \approx 0$, while voltage u_{g2} will strive toward level $E_a - U_{a1\,min} > 0$. Therefore, voltage u_{g2} will rise at a high rate and will reach cutoff voltage first at moment t_3. As a result, previously- blanked triode L_2 unblanks, i. e., circuit reversal will occur.

The capacitance of the accelerating capacitors is increased to 200--500 pF to increase the reliability of symmetrical triggering without trigger tubes. However, as was demonstrated above, this will lead to deterioration in flip-flop resolving capability due to the rise in recovery time. It should be noted that, even in this case, flip-flop triggering occurs with a large delay, avoiding /243 the active reversal stage. Actually, after blanking of both triodes at moment t_1. only one of them (L_2) unblanks at moment t_3. The other remains blanked and the positive feedback loop does not close. Therefore, only passive, "sluggish," flip-flop reversal occurs at a rate determined only by the coupling capacitor recharge rate.

It is not difficult to see that the examined nature of the triggering processes in essence will not change if a square pulse of identical polarity acts on a flip-flop instead of trigger drop. Actually, the decay of this pulse with a jump will increase both grid voltages. However, the blanked triode does not unblank since a negative pulse amplified by the unblanked triode will act simultaneously on its grid.

A circuit for symmetrical triggering with negative pulses to flip-flop grids across trigger diodes D_1, D_2 is depicted in Figure VI.12b (this circuit comes from the Figure VI.10a asymmetrical trigger circuit through connection of trigger diode cathodes). We will assume that triode L_1 is unblanked prior to triggering, while triode L_2 is blanked. Then, diode D_1 is unblanked (its plate potential equals $U_{a1\,max}$ and is slightly more than zero), while diode D_2 is blanked (its plate potential equals $U_{a2\,min} < 0$). Triggering is accomplished across unblanked diode D_1, which immediately transmits a trigger pulse to unblanked triode L_1 grid. During the reversal process, diode D_1 will blank due to a decrease in its plate voltage to value $U_{a1\,min}$. Diode D_2 unblanks, preparing the trigger circuit with the next trigger pulse.

This trigger circuit's shortcoming is that, in spite of the presence of two diodes, a negative trigger pulse still acts upon both flip-flop grids simultaneously,

which, as demonstrated above, reduces triggering reliability. In order to demonstrate this, we will assume that trigger pulse amplitude is less than value $U'_{a2\,min}$, i. e., insufficient for direct unblanking of blanked diode D_2 due to reduction of its cathode potential by the trigger pulse. But, diode D_2 plate potential will rise simultaneously with the reduction in its cathode potential (in connection with an increase in triode L_1 plate potential). Diode D_2 unblanks when these potentials are equal and the trigger pulse constraining triode L_2 unblanking also will pass. Flip-flop accelerating capacitances must be sufficiently great, just as in symmetrical triggering without diodes, in order for the circuit to reverse all the same.

A symmetrical trigger circuit using negative pulses across trigger diodes to flip-flop plate networks is distinguished for significantly-greater reliability. This circuit is depicted in VI.12c (it comes from the Figure VI.10b circuit by connecting diode cathodes). Here, diode cathode potential in the initial state equals E_a, while their plate potential always is less than E_a. Consequently, /244 both diodes are blanked. We will assume again that triode L_1 is unblanked, and triode L_2 is blanked. Then, diode L_1 will be close to the unblanking threshold and a negative trigger pulse will flow across it to blanked triode L_2 plate, then on to unblanked triode L_1 grid. Diode D_2 is blanked by large back voltage $E_a - U'_{a\,min}$ and, since the trigger pulse amplitude is significantly less than this magnitude, then it may not unblank. Thus, the trigger pulse acts directly only on the unblanked triode grid. As a result, the blanked triode unblanks and, as was the case in symmetrical triggering, an active (avalanche-like) circuit reversal occurs. Here, triode L_2 plate voltage decreases with a jump, resulting in diode D_1 again blanking immediately following onset of reversal, cutting the trigger pulse generator out. Diode D_2 remains blanked, only approximating the unblanking threshold upon reversal cessation. This also favorably impacts upon the reversal rate since, right up to its cessation, the harmful influence of the trigger pulse generator on the flip-flop is eliminated. The subsequent trigger pulse will trigger the flip-flop across diode D_2 and so on.

The shortcomings of this trigger circuit include (just as was the case for asymmetrical circuits triggering plates across trigger diodes) the requirement for a slight increase in trigger pulse amplitude and the possibility of breakdown of semiconductor diodes with large reverse voltage. Symmetrical circuit triggering across trigger triodes is the most reliable.

EXERCISE VI.5

a) What will breakdown of Figure VI.12c circuit diode D_2 lead to?

b) Draw a flip-flop symmetrical trigger circuit across trigger triodes and explain its operation. (Page 479)

4. Cathode-Coupling Flip-Flop

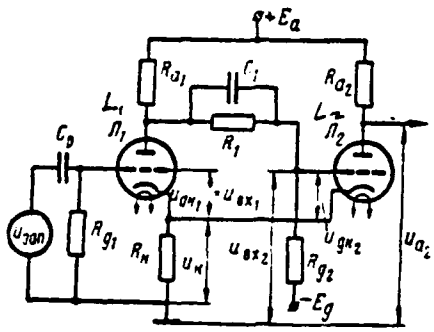


Figure VI.14. Cathode-Coupling Flip-Flop.

A cathode-coupling flip-flop circuit is depicted in Figure VI.14. This is an asymmetrical circuit. It differs from symmetrical flip-flop circuits in that one plate-grid coupling (from L_2 plate to L_1 grid) is absent and is replaced /245 by a cathode coupling formed with the aid of cathode load impedance $R_к$ common for both triodes.

The circuit has two states of stable equilibrium, just like any flip-flop.

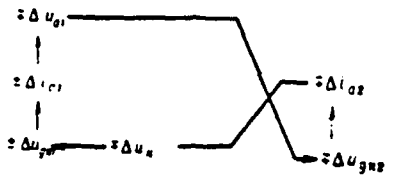
Triode L_2 is blanked, just as in a symmetrical circuit, by divider R_1, R_{g2} output voltage when triode L_1 is unblanked. Resistance R_{g2} is connected to negative bias source E_g to create distribution of potentials required here. Triode L_1 is blanked when triode L_2 is unblanked due to the voltage $U_к$ drop created across resistance $R_к$ by triode L_2 current and is applied with a "minus" to triode L_1 grid:

$$U_{g\kappa 1} = -U_{a2} = -I_{a2}R_k < E_{g_1} \qquad \text{(VI.29)}$$

Unblanked triode current flows across resistance R_k in any state of stable equilibrium, resulting in the fact that negative current feedback is created for this triode (the voltage u_k drop always is applied with a "minus" also to unblanked triode grid). This negative feedback stabilizes the flip-flop d-c operating mode.

Negative feedback is not active during the reversal stage when both triodes are unblanked and resistance R_k enters the positive feedback loop, causing an avalanche-like changeover process. This is explained by the fact that currents of both triodes $i_k = i_{a1} - i_{a2}$, which, just like grid potentials, change in opposite directions, simultaneously flow across resistance R_k during reversal. Here, triode L_1 operates like an amplifier with plate output (its input voltage is supplied from resistance R_k and applied directly between grid and cathode $u_{g\kappa 1} = -u_k$), while triode L_2 operates like a cathode follower (its input voltage is picked off divider output and applied between grid and "ground," while output voltage for internal processes in the circuit is picked off resistance R_k). Examining the triode L_2 input network, we may write for an increment of voltages during reversal (i. e., not considering fixed bias E_g) $\Delta u_{gx2} = \Delta u_{g\kappa 2} - \Delta u_k$, or, since $\Delta u_{gx2} = -K_1 \Delta u_{g\kappa 1}$, where K_1 -- arm on triode L_1 gain and $\Delta u_k = -\Delta u_{g\kappa 1}$, then $\Delta u_{g\kappa 2} = -\Delta u_{g\kappa 1}(K_1 - 1)$. Since $K_1 > 1$, then for increment magnitudes, we will get $\Delta u_{g\kappa 2} \gg \Delta u_{g\kappa 1}$ and, consequently, during the reversal process $\Delta i_{a2} \gg \Delta i_{a1}$. Therefore, voltage u_k changes in the same direction as does cathode follower current i_{a2}, i. e., opposite in phase to current i_{a1}, maintaining its change. Thus, if current i_{a1} rises, then voltage u_k, i. e., triode L_1 cathode potential, decreases, which is equivalent to a rise in this triode's grid potential $(u_{g\kappa 1} = -u_k)$, and will lead to a further increase in its plate current.

Symbolically, positive feedback loop action during reversal to both /246 sides may be depicted in the form



(VI.30)

Self-excitation condition (VI.2a) as usual must be satisfied for the avalanche-like process to arise. First arm gain is determined, just as was the case for the grounded-grid stage (see Figure III.10) with output across the divider and, based on (III.39), equals

$$K_1 = \frac{\Delta u_{a1}}{\Delta u_k} K_1' = \frac{(\mu_1 + 1) R_{a1}}{R_{i1} + R_{a1}} K_1', \tag{VI.31}$$

where K_1' -- divider transfer constant considering the influence of accelerating capacitor C_1 and stray capacitance $C_{вх2}$.

Second arm gain is determined, just as was the case for the stage with plate and cathode loads and with cathode output, loaded to grounded-grid stage input resistance ($R_н = R_{вх.з.с}$):

$$K_{II} = \frac{K_н \cdot R_{вх.з.с}}{R_{вых.к} + R_{вх.з.с}}, \tag{VI.32}$$

where values $K_н$ and $R_{вых.к}$ are computed from formulas (III.32 and III.33) for the triode L_2 stage, while $R_{вх.з.с}$ is computed from formula (III.40) for the triode L_1 stage.

Divider resistances as usual are selected in accordance with conditions (VI.5) and (VI.9). Accelerating capacitor C_1 plays an identical role and is selected from the identical considerations as was the case for symmetrical circuits.

We will accept, just as before, for blanked triode L_1 or L_2 $U_{сз.мин} = 2E_с$ (reliable blanking condition), while for unblanked triode L_2 $U_{сз.мин} = E_с > 0$ (grid

limiting condition). Then, we may write the following ratios for circuit parameter selection:

$$U_{a1} = I_{a1}R_a = 2,5E_{g1} \qquad \text{(VI.33)}$$

-- triode L_1 reliable blanking condition with triode L_2 current:

$$(U_{a1\,max} + E_{g1})K_1 - E_{g1} - U_{g1} = E_{g1} > 0 \qquad \text{(VI.33a)}$$

-- grid limiting condition in triode L_2 given blanked triode L_1 analogous to the second (VI.11a) condition;

$$U_{a1\,max} K_2 - E_{g2} - U_{g2} = E_{g2} \qquad \text{(VI.33b)}$$

(where $U_{a1\,max} = E_a - I_{a1}R_{a1}$, $U_{g1} = I_{a1}R_k$) /247

-- triode L_2 reliable blanking condition given unblanked triode L_1 analogous to the first (VI.11a) condition.*

Currents I_{a1} and I_{a2} in these ratios will be found from tube dynamic characteristics plotted considering plate and cathode resistances for each stage (see formula III.35).

From (VI.33a) considering (VI.33), we will get the requisite negative bias magnitude:

$$E_{g1} = \frac{K_1 E_a - 3|E_{g1}|}{1 - K_1}. \qquad \text{(VI.34)}$$

*It is mandatory that triode L_1 be unblanked when triode L_2 is blanked. Actually, its grid potential decreases only due to negative feedback by magnitude . The voltage may not blank triode L_1 since, if that were to occur, then $I_{a1} = 0$, , i. e., the reason for its blanking would disappear. (This concept often is formulated in the following way: "a tube may not blank itself with its own plate current"). Therefore, there is no special condition for triode L_1 unblanking when triode L_2 is blanked, in accordance with ratios (VI.33), (VI.33a), and (VI.33b).

It is most convenient to pick cathode-coupling flip-flop output voltage off resistance R_{a2}*. Here, connection of load essentially does not affect reversal rate since the triode L_2 plate network is not included in the positive feedback loop (VI.30).

Triggering a cathode-coupling flip-flop with negative pulses supplied alternately to unblanked tube grids is not advantageous since unblanked triode L_2 will operate like a trigger pulse cathode follower, only decreasing its amplitude. Symmetrical triggering to grids with single-polarity pulses (symmetrical triggering to plates completely is impossible due to absence of one plate-grid coupling) may not be used for this very reason. Therefore, triggering usually occurs with pulses u_{sig} of alternating polarity supplied to triode L_1 grid (of the amplifier with plate output). If triode L_1 is blanked, circuit reversal occurs from the first positive pulse, unblanking triode L_1; if triode L_1 is unblanked, then circuit reversal occurs from the first negative pulse, unblanking triode L_2 (across triode L_1).

Flip-flop voltage curves for this type of triggering are depicted in Figure VI.15. Voltage u_a (Figure VI.15d), which changes during reversal in phase with voltage u_{a1}, i. e., opposite in phase with voltage u_{a2}, also may be used as output voltage.

This triggering method sometimes is used to count the number of pulse polarity changes. In this event, the flip-flop is reversed only with the first pulse of the new polarity and does not react to subsequent pulses, until their polarity changes (these pulses are depicted by the dotted line in Figure VI.15a).

EXERCISE VI.6 /248

a) It follows from copmparison of ratios (VI.34) and (VI.13) that a cathode-coupling flip-flop requires a lesser negative bias E_g magnitude. How do you explain this?

*Resistance R_{a2} is included in the circuit for just that reason.

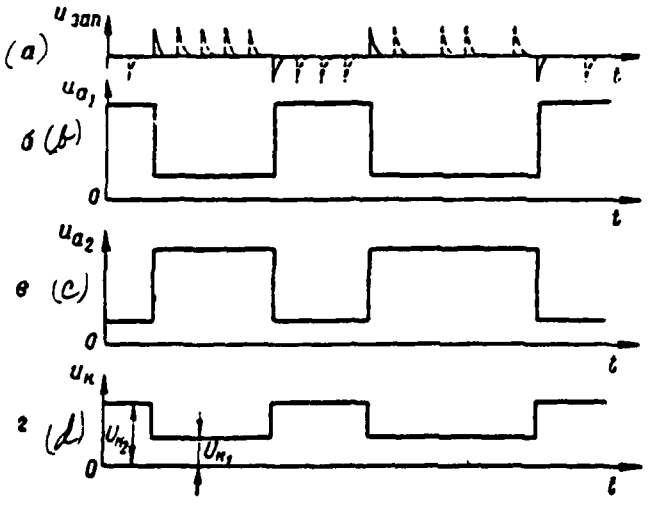


Figure VI.15. Cathode-Coupling Flip-Flop Voltage Curves When Triggered By Alternate-Polarity Pulses.

b) Prove the validity of the voltage u_a curves depicted in Figure VI.15d.

(Page 479)

A cathode-coupling flip-flop may be used also for shaping square pulses from output voltage of random form supplied here in the form of "continuous triggering" voltage $u_{зап}$ to triode L_1 grid.

Flip-flop operation in the square pulse shaping mode in the case of sinusoidal input voltage is explained in Figure VI.16. When voltage $u_{зап}$ rises, the circuit reverses when this voltage reaches the threshold value at which triode L_1 unblanks: $U_{зап} = U_{a2} - E_{см}$ (point 1 in Figure VI.16). When voltage $u_{зап}$ decreases, the circuit reverses when this voltage reaches the threshold value at which triode L_2 unblanks: $U_{зап} \approx$ (point 2 in Figure VI.16). Output voltage u_a rises with a jump to magnitude E_a at the moment triode L_1 unblanks since triode L_2 blanks and decreases with a jump to magnitude $I_{a1} R_a$.

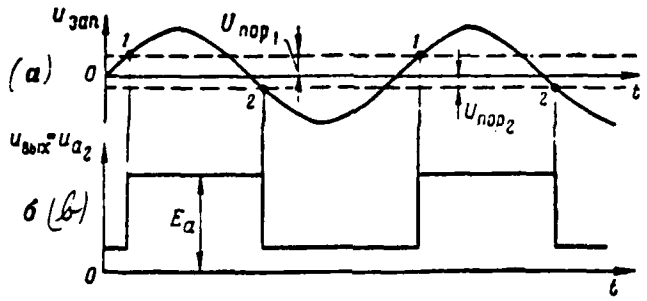


Figure VI.16. Cathode-Coupling Flip-Flop Voltage Curves in the Shaping Mode ("Continuous Triggering").

at the moment triode L_2 unblanks. This voltage does not change during the /249 intervals between reversal moments.

EXERCISE VI.7

a) Redraw the Figure VI.16 voltage curves and add voltage u_{a1} and u_{c} curves to them.

(b) Why is a cathode-coupling flip-flop rather than a symmetrical flip-flop used for shaping square pulses from random-shape continuous voltage? (Page 480)

§ 3. MONOSTABLE MULTIVIBRATORS

1. Cathode-Coupling Monostable Multivibrator

A cathode-coupling monostable multivibrator circuit is depicted in Figure VI.17. This circuit differs from a cathode-coupling flip-flop circuit (Figure VI.14) primarily by the type of coupling between triode L_1 plate and triode L_2 grid. This coupling in the flip-flop was potentiometric and accomplished across divider R_1, R_2 for both d-c (in stable equilibrium states) and for a-c (in reversal stages); accelerating capacitor C_1 here played a supplementary role. This coupling in a mulitvibrator is accomplished across network C_1R_{g2}, i. e., it is a capacitance coupling and therefore acts only on a-c; here, capacitor C_1 in principle is /250 a mandatory circuit element. In addition, there is no outside negative bias source E_g in a multivibrator.

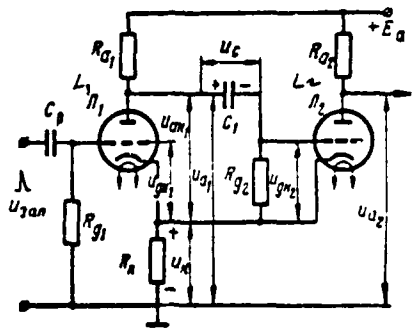


Figure VI.17. Cathode-Coupling Monostable Multivibrator.

These two circuit differences will lead to the fact that only one equilibrium state in a monostable multivibrator remains stable, i.e., it may last as long as is convenient: when triode L_2 is unblanked, triode L_1, just as in a cathode-coupling flip-flop, is maintained in the blanked state due to the voltage drop across common cathode resistance R_k due to flow of triode L_2 current across it. The other equilibrium state when triode L_1 is unblanked and triode L_2 is blanked may not be stable since, due to capacitor C_1 disruption of the d-c plate-grid coupling and absence of bias source E_g, the fixed cause for triode L_2 blanking when triode L_1 unblanks is eliminated (fixed divider output voltage $U_{g2min} < E_{g2}$ where $u_{g1} = U_{g1min}$ is the cause in a cathode-coupling flip-flop).

As can be seen from the circuit, triode L_2 may be blanked only by capacitor C_1 discharging current across unblanked triode L_1 and resistance R_{g2} since only this current creates a voltage u_{g2} drop applied with a "minus" across resistance R_{g2} to triode L_2 grid. But, capacitor discharging current may exist only for a limited time. Therefore, the second equilibrium state is quasistable (temporarily stable), while capacitor C_1, whose discharge rate determines how long the circuit remains in this state, is called the timing capacitor.

Circuit parameters usually satisfy inequalities:

$$R_{g2} \gg R_{a1} > R_{a2} > R_k; \; R_{g2} \gg R_{i01},$$

where R_{i01} -- unblanked triode L_1 internal d-c resistance.

Thus, prior to triggering, a monostable multivibrator will be in the single possible state of stable equilibrium (triode L_2 unblanked, triode L_2 blanked). It reverses due to trigger pulse stimulus -- it converts with a jump to a state of quasistable equilibrium, after a period of time reverting from this state with a jump, but now spontaneously, stimulated by internal forces.

The identical positive feedback loop (III.39) found in a cathode-coupling flip-flop is active in the circuit during the reversal stages. As usual, self-excitation condition (VI.2a) must be satisfied in order for the reversal processes to have an avalanche-like nature: $K_I K_{II} > 1$.

First stage gain is determined, as was the case in the cathode-coupling flip-flop, from formula (IV.73) for a grounded-grid amplifier and, considering that changes in voltage u_{a1} in a multivibrator are transmitted completely across capacitor C_1 to triode L_2 grid, equals

$$K_I = \frac{\Delta u_{a1}}{\Delta u_g} = \frac{\Delta u_{g2}}{\Delta u_g} = \frac{(\mu_1 + 1) R_{a1}}{R_{i1} + R_{a1}}. \tag{VI.35}$$

Second stage output voltage, as opposed to a cathode-coupling flip-flop, /251 is applied, not between grid and "ground," but between grid and triode L_2 cathode. Therefore, its gain is determined, as was the case for the stage with plate and cathode loads and cathode output without feedback (see Figure III.9) loaded to input resistance of the grounded-grid stage:

$$K_{II} = \frac{K_1 R_{вх\,2\,с}}{R_{вых.к} + R_{вх\,2\,с}}. \tag{VI.36}$$

where K_1 is computed from formula (III.37), $R_{вх\,2\,с} = R_{вх}$ -- from formula (III.40), and $R_{вых.к} = \frac{R_i + R_{i1} R_к}{R_{i1} + R_{i1} - R_к}$.

Voltage curves for a cathode-coupling monostable multivibrator without considering stray capacitances is depicted in Figure VI.18. We will examine the

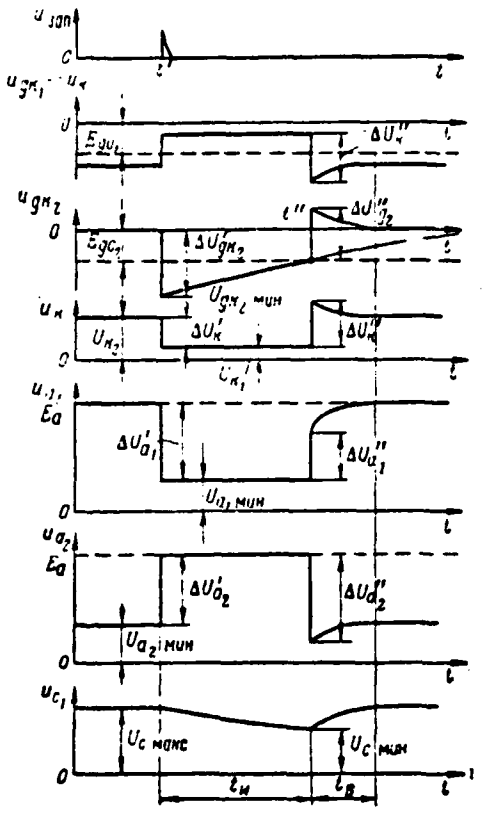


Figure VI.18. Cathode-Coupling Monostable Multivibrator Voltage Curves.

circuit operating cycle. Here, we will keep in mind that, in accordance with Kirchhoff's second law,

$$u_{a1} = u_{C_1} - u_{gk2} - u_k$$

or

$$u_{C_1} = u_{a1} - (u_{gk2} + u_k). \tag{VI.37}$$

Initial state $(t < t')$. In the initial stable state, there are no transient processes in the circuit. Therefore, capacitor C_1 current and voltage drop $u_{gk2} = i_{C_1} R_{gk2}$ equal zero and triode L_2 is unblanked. This triode's plate current,

flowing across resistance R_k, creates a voltage change in it applied with a "minus" to triode L_1 grid. Here, condition (VI.29) must be satisfied: $U_{gk1} = -U_{k2} = -I_{a2}R_k < E_{g01}$, i. e., triode L_1 is blanked. Unblanked triode L_2 plate voltage is minimal and equals $U_{a2\,мин} = E_a - I_{a2}R_{a2}$, that of blanked triode L_1 is maximum and equals $U_{a1\,макс} = E_a$, while capacitor C_1 is charged to a voltage, in accordance with (VI.37), equalling

$$U_{C\,макс} = U_{a1\,макс} - U_{g02} - U_{k2} = E_a - U_{k2} \qquad \text{(VI.38)}$$

and applied with a "plus" to triode L_1 plate. The circuit "awaits" the arrival of the trigger pulse in this state as long as necesary.

Triggering and reversal. A positive trigger pulse is supplied at moment t' across transient network $C_p R_{g1}$ to triode L_1 grid. Its amplitude must be sufficient to unblank triode L_1: $U_{имп} > U_{k2} - E_{g01}$. Positive feedback loop (VI.30) closes when triode L_1 current appears and an avalanche-like circuit reversal occurs. As a result, triode L_1 unblanks completely, while triode L_2 is blanked reliably. Here, voltages u_{a1}, u_k, u_{g2} with a jump decrease, respectively, to values $U_{a1\,мин} = E_a - I_{a1}R_{a1}$, $u_k = U_{k1} = I_{a1}R_k < U_{k2}$ (see Exercise VI.6) and $U_{g2\,мин}$, while voltages u_{a2} and u_{g1} with a jump increase, respectively, to values $U_{a2\,макс} = E_a$ and $U_{g1\,макс} = -U_{k1}$.

Voltage $U_{g2\,мин}$ may be found from the following simple circumstances. At the moment of reversal, a negative voltage step, equalling the difference of the negative steps of voltages u_{a1} and u_k, is transmitted completely across capacitor C_1 to triode L_2 grid. Since $u_{g2} = 0$ prior to triggering, then /252

$$U_{g2\,мин} = -\Delta U_{g2} = -\Delta U_{a1} = -\Delta U_{a1} - (-\Delta U_k)$$

or, since

$$\Delta U_{a1} = I_{a1}R_{a1},\ \Delta U_k = U_{k2} - U_{k1} = (I_{a2} - I_{a1})R_k,$$

then

$$U_{g2\,мин} = -I_{a1}R_{a1} + (I_{a2} - I_{a1})R_k. \qquad \text{(VI.39)}$$

The following condition must be satisfied for triode L_2 blanking /253

$$U'_{g2,\min} < E_{g2}. \tag{VI.39a}$$

which is insured due to sufficiently-high resistance $R_{a1} \gg R_k$ magnitude.

Quasistable state $(t' < t < t'')$. Capacitor C_1 discharge begins across unblanked triode L_1 and resistance R_{g2}, as well as across resistance R_{a1}, source E_a internal resistance, and resistances R_k and R_{g2} in connection with the triode L_1 plate voltage decrease at the moment of reversal. Thus, equivalent resistance in the discharging network will equal $R_{э.разр} = R_{g2} + \frac{R_{i1}(R_{a1}+R_k)}{R_{i1}+R_{a1}+R_k}$ or, since $R_{i1} \ll R_{a1}$, then $R_{э.разр} \approx R_{g2}$. Capacitor i_p discharging current decreases in accordance with the law of exponents $i_p = I_p e^{-\frac{t}{\tau_{разр}}}$, where I_p -- initial (amplitude) value of this current, considering the opposite action of voltages u_{C1} and $u_{ak1} = u_{a1} - u_k$ and ratio (VI.37), equalling

$$I_p = \frac{U'_{C\max} - U'_{ak1}}{R_{э.разр}} \approx \frac{E_a - U'_{g2} - E_2 + I_{a1}R_1 + U'_{k1}}{R_{э.разр}} \approx \approx \frac{I_{a1}R_{a1} - (I_{a2} - I_{a1})R_k}{R_{g2}}, \tag{VI.40}$$

while

$$\tau_{разр} \approx C_1 R_{э.разр} \approx C_1 R_{g2}. \tag{VI.41}$$

The voltage drop across resistance R_{g2} applied with a "minus" to triode L_2 grid changes in accordance with the same law:

$$u_{g2} = -i_p R_{g2} = -I_p R_{g2} e^{-\frac{t}{\tau_{разр}}} = U'_{g2,\min} e^{-\frac{t}{\tau_{разр}}}, \tag{VI.42}$$

where value $U'_{g2,\min} = -I_p R_{g2}$ already was determined beforehand by ratio (VI.39) and now also may be obtained directly by considering (VI.40).

During the capacitor C_1 discharge process, the voltage in it gradually decreases, striving towards infinity to value $U'_{C\infty} = U'_{ak1} = U'_{a1,\min} - U'_{k1}$, while voltage

u_{a2} increases gradually, striving towards the zero level (where $i_p=0$ $u_{a2}=0$). However, as long as this voltage remains less than cutoff voltage $u_{a2} < E_{go2}$, triode L_2 remains blanked ($u_{a2} = E_a$), while triode L_1 remains unblanked. Since $R_{g2} \gg R_{a1}$, then $i_{a1} \ll I_{a1}$ and the influence of current i_{a1} on voltage u_{a1} is immaterial. Therefore, $u_{a1} \approx U_{a1\,max} = \text{const}$.

Counter reversal. At moment t" when voltage u_{g2}, rising, equates to cutoff voltage E_{go2}, triode L_2 unblanks, again closing positive feedback loop (VI.30) and an avalanche-like circuit reversal in the opposite direction occurs. Here, triode L_2 unblanks completely, triode L_1 is blanked by voltage $u_{a1}=i_{a1}R_a$ drop, voltages u_{a1}, u_{g2} and u_a increase with a jump, while voltages u_{g1} and /254 u_{a2} decrease. At moment t", capacitor C_1 turns out to be discharged to a voltage in accordance with (VI.37) equalling

$$U_{c1\,min} = U_{a2} - U_{g2} = E_a - I_{a1}R_{a1} - I_{a1}R_a + E_{go2}. \qquad \text{(VI.43)}$$

At that moment, in connection with the increase in voltage u_{a1}, capacitor C_1 begins to charge through network: $+E_a$, resistance R_{a1}, capacitor C_1, equivalent resistance $\Delta I_a R_{g1}$ between triode grid and cathode, resistance R_a, $-E_a$ (chassis).

Capacitor C_1 charging current reduces triode L_1 plate potential by magnitude $\Delta I_a R_{a1}$, increases cathode potential by magnitude $I_a R_a$, and increases triode L_2 grid potential relative to cathode by magnitude $I_a R_{g2}$. Equivalent resistance R_{g2} in the final derivative may be replaced by grid--cathode path resistance r_{g2} since, where $u_{g2}>0$, grid current occurs in triode L_2, i. e., $r_{g2} \ll R_{g2}$ and

$$R_{g2} = \frac{r_{g2}R_{g2}}{r_{g2} + R_{g2}} \approx r_{g2}^{*}. \qquad \text{(VI.44)}$$

Since charging current at moment t" equals its maximum value I_{a1}, then the magnitudes of positive voltage steps u_{a1}, u_a, u_{g2}, respectively, equal

*Consequently, capacitor C_1 charging occurs with triode L_2 grid current, i. e., .

$$\Delta U''_1 = I_1 R_{a1} - I_2 R_{a2};\quad \Delta U''_R = (I_{a2} - I_{a1}) R_k + I_2 R_k;$$
$$\Delta U''_{gk2} = I_2 r_{gk2} - |E_{g0}|, \tag{VI.45}$$

where, considering (VI.43)

$$I_2 = \frac{E_a - U'_{C\,max} - U''_{k2}}{R_{a2} + r_{gk2} + R_k} = \frac{I_{a1}R_{a1} - (I_{a2} - I_{a1}) R_k - |E_{g0}|}{R_{a2} + r_{gk2} + R_k}. \tag{VI.46}$$

Negative voltage u_{gk1} step equals $\Delta U''_{gk1} = -\Delta U''_k$, while negative voltage u_{a2} step obtained is greater than at moment t', since voltage u_{gk2} will exceed the zero level by magnitude $I_2 r_{gk2}$.

Recovery ($t > t'$). Capacitor C_1 charging current, having arisen at moment t", decreases by the law of exponents

$$i_1 = I e^{-\frac{t}{\tau_{1ap}}},$$

where

$$\tau_{1ap} = C_1 (R_{a1} + r_{gk2} - R_k) \approx C_1 R_{a1} \tag{VI.47}$$

-- charging network time constant ($R_k + r_{gk2} \ll R_{a1}$).

Therefore, voltages [illegible] and [illegible] gradually rise after circuit counter reversal, while voltages u_{gk2} and [illegible] decay to their initial values with time constant [illegible]. The duration of capacitor C_1 charging determines circuit /255 recovery time (without considering stray capacitances) and essentially equals

$$t_в \approx 3\tau_{1ap} = 3C_1 R_{a1} \tag{VI.48}$$

Thus, pulses of negative polarity are shaped at triode L_1 plate and resistance R, while those of positive polarity are shaped at L_2 plate after triggering.

The best pulse shape results at triode L_2 plate since a coupling capacitor is not connected to this plate. In addition, this triode's plate network, just as was the case in a cathode-coupling flip-flop, is not included in the positive feedback loop and, consequently, connection of load here essentially will not impact upon the reversal rate. Therefore, circuit output voltage usually is picked off triode L_2 plate.

Output pulse duration equals the length of time the circuit remains in the quasistable state. This is determined to be the time in which negative voltage u_{g2} rises (decreases in absolute value) from value $U_{g2,max}$ to value E_{go2} during which triode L_2 unblanks. Equating $u_{g2}=E_{go2}$, $t=t_u$ in ratio (VI.42), we will write

$$E_{go2}=U_{g2,max}e^{-\frac{t_u}{\tau_{pas2}}}.$$

Taking the logarithm of this expression, we will get $t_u=\tau_{pas2}\ln\frac{U_{g2,max}}{E_{go2}}$, whereby, in accordance with (VI.39) and (VI.41)

$$t_u=C_1R_{g2}\ln\frac{I_{a1}R_{a1}-(I_{a2}-I_{a1})R_g}{|E_{go2}|}. \qquad \text{(VI.49)}$$

Essentially, resistance R_{g2} usually controls pulse duration.

EXERCISE VI.8

a) What will be the result of non-satisfaction of condition (VI.39a) $U_{g2,max}<E_{go2}$?

b) What will be the result of triggering a cathode-coupling monostable multivibrator with pulses having repetition period T_{rep} satisfying inequality $t_u<T_{rep}<t_u+\tau_0$? Draw the curves of voltages u_{a1}, u_{g1}, u_{g2} and u_{a1} for two or three repetition periods T_{rep}.

c) What will be the result of non-satisfaction of condition (VI.29) $U_{a2}=I_{a2}R_a>E_{c2}$ if $U_{a2}=E_{go1}$?

Draw the curves of voltages u_{g1} and u_{g2} in the circuit for this instance.

(Page 480)

2. Cathode-Coupling Retarding-Field Monostable Multivibrator

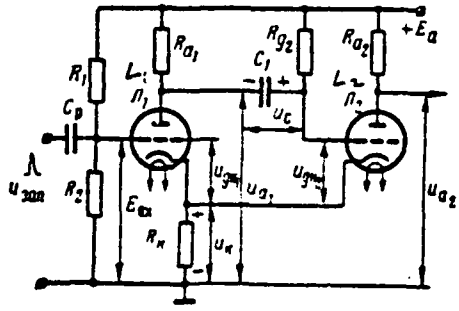


Figure VI.19. Cathode-Coupling Retarding-Field Monostable Multivibrator.

A cathode-coupling retarding-field monostable multivibrator circuit is depicted in Figure VI.19. This circuit differs from the cathode-coupling monostable multivibrator examined above (Figure VI.17) since triode L_2 grid is connected across large resistance R_{g2} to plate voltage $+E_a$ source bus rather than to cathode. Therefore, it is referred to as a circuit "with a positive grid."* In addition, voltage divider R_1, R_2, from which constant bias voltage E_{ex} positive relative to "ground" is supplied to triode L_1 grid, is present in the circuit under examination. However, this second difference is not considered a principal one, since the identical divider may be connected to the Figure VI.17 circuit as well.

A cathode-coupling retarding-field monostable multivibrator in principle operates just like a cathode-coupling "zero"-grid monostable multivibrator so the voltage curves in its characteristic points are similar to the Figure VI.18 curves.

Positive bias E_{ex} magnitude is selected from condition

*It would be more precise to say with positive bias in grid. From the Figure VI.17 circuit point of view, it may be referred to as a cathode-coupling "zero"-grid monostable multivibrator.

$$E_{вх} < U'_{к1} = I_{а1} R_к, \qquad (VI.50)$$

during satisfaction of which voltage between unblanked triode L_1 grid and cathode remains negative $(U_{гк1} = E_{вх} - U_{к1} < 0)$, i. e., insures that it operates without grid currents.* We will examine the special features of circuit operation stipulated by the presence of triode L_2 positive grid.

Triode L_2 must be unblanked in the initial stable state, when no transient processes occur in the circuit, since the potential of its grid connected to the $+E_a$ bus exceeds cathode potential. But, grid current I_{g2} flows here through network $+E_a$, resistance R_{g2}, grid--cathode path, resistance $R_к$, and chassis $(-E_a)$. Resistance R_{g2} is on the order of 1 megohm, i. e., $R_{g2} \gg r_{гк2}$. Therefore, almost the entire voltage drop caused by current I_{g2} in this network occurs across resistance R_{g2} and triode L_2 positive grid potential relative to cathode essentially turns out to equal zero $(U'_{гк2} \approx 0)$.**

In other words, triode L_2 in the initial state operates in the grid limiting mode (see Chapter V, § 3). Triode L_1, in spite of positive bias $E_{вх}$ applied /257 to its grid from the divider, must be blanked, just as was the case in the previous circuit, due to the voltage drop across resistance $R_к$:

$$U'_{к2} = (I_{а2} + I_{г2}) R_к \approx I_{а2} R_к \; (I_{г2} \ll I_{а2})$$

For this, circuit parameters are selected so that, in accordance with condition (VI.50) and instead of condition (VI.29), the following condition will be satisfied

$$U'_{к2} - E_{вх} > |E_{гк1}|. \qquad (VI.51)$$

Since $u_{а1} = E_а$, while $U'_{гк2} \approx 0$, then capacitor C_1 as usual is charged to maximum

*Therefore, in spite of the presence of divider R_1, R_2, only the triode L_2 grid is referred to as "positive."

**Voltage $U_{гк2}$ comprises several tenths of a volt when magnitude $E_а$ = 200 ÷ 300 V.

value equal, in accordance with (VI.38), $U_{C\,макс} = E_a - U_{k2}$ and applied with a "plus" to triode L_1 plate.

Triggering and reversal occur exactly as was the case in a cathode-coupling monostable multivibrator. As a result, triode L_1 unblanks and triode L_2 blanks. Triode L_2 grid voltage decreases with a jump to a value, in accordance with (VI.39) and (VI.39a), as usual equalling

$$U_{g2\,мин} = -I_{a1}R_{a1} + (I_{a2} - I_{a1})R_k < E_{g2}. \qquad \text{(VI.51a)}$$

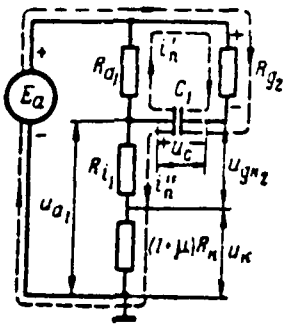


Figure VI.20. Capacitor C_1 Recharging Network.

The nature of processes in the quasistable state, compared with the previous circuit, changes only due to connection of triode L_2 grid, i. e., the "right" capacitor C_1 plate, to the $+E_a$ bus. Capacitor C_1 connected in that manner after triggering will strive already not to discharge, but to recharge itself to voltage of opposite polarity. The capacitor C_1 recharging circuit is depicted separately in Figure VI.20. Recharging current i_n flows from the "plus" capacitor plate to its "minus" plate along two parallel branches, i. e., it branches into two currents i_n' and i_n''. Current i_n' flows across resistances R_{a1} and R_{g2}, while current i_n'' flows across unblanked triode L_1, resistance R_k, plate voltage source E_a, and resistance E_{g2}. Full recharging current flows across resistance R_{g2} and creates a voltage $i_n'R_{g2}$ drop in it applied as a "minus" to triode L_2 grid. Triode L_2 also is maintained in a blanked state due to this voltage drop.

The capacitor during the recharge process will strive to recharge itself to voltage $U_{C_\infty} = -(E_a - U_{a_1 \text{ нас}}) = -(E_a - E_a + I_{a1} R_{a1}) = -I_{a1} R_{a1} < 0$, while voltage u_{gk2} will strive to rise to positive value

$$U_{gk2\infty} = E_a - U_{k1} = E_a - I_{a1} R_k > 0. \qquad \text{(VI.52)}$$

However, when this voltage, rising, equates to cutoff voltage /258 E_{go2}, triode L_2 unblanks and the circuit returns to the initial state. The processes of counter reversal and subsequent circuit recovery occur in a manner identical to that for a cathode-coupling monostable multivibrator.

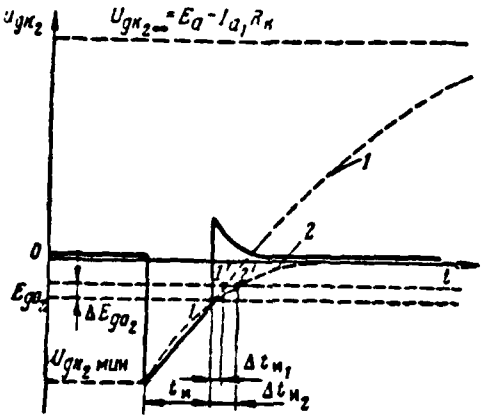


Figure VI.21. Triode L_2 Grid Voltage Law of Change.

The curve of voltage u_{gk2} for a complete retarding-field monostable multivibrator operating cycle is depicted by the solid line in Figure VI.21. The law of change for this voltage in the quasistable state is the initial sector of an exponential curve caused by the capacitor C_1 recharge process (dotted curve 1). The law of change for voltage u_{gk2} in a circuit with a "zero" grid stipulated by the capacitor C_1 discharge process is there as well for comparison (dotted line 2). Here, values $U_{gk2\,min}$ and t_u are accepted as being equal in both cases for the purposes of clarity. Recharge exponential curve 1 intersects level E_{go2} at a larger angle than does discharge exponential curve 2. As a result of this, pulse duration t_u shaped by the retarding-field circuit, will change to a lesser degree than in a zero-grid circuit as a result of this, given changes in supply voltages or tube parameters. Actually, for example, if triode L_2 cutoff voltage decreases by magnitude ΔE_{go2},

as depicted in Figure VI.21, then a retarding-field circuit counter reversal will occur at the moment determined by point 1'. This will occur in a "zero"-grid circuit at the moment determined by point 2'. The pulse duration increment in the first instance will be significantly less than in the second: $\Delta t_{u1} < \Delta t_{u2}$. Thus, a retarding-field circuit has increased pulse duration stability and this is its main advantage.

Another advantage of the retarding-field circuit is the essentially /259 linear relationship of pulse duration t_u to bias voltage E_{gx}. We will introduce a formula for pulse duration initially in order to demonstrate this.

In accordance with (XI.10), the law of voltage u_{g2} change corresponding to recharge exponential curve 1 in Figure VI.21 may be written

(VI.53)

where τ_{rep} -- capacitor C_1 recharge time constant. This time constant will be found easily from examination of the Figure VI.20 recharging network. Recharging current flows across resistance R_{g2} and two parallel branches -- resistance R_{a1} and triode L_1 with resistance R_i. The second branch is a current-stabilizing one-port with negative feedback, whose resistance in accordance with (III.74) equals $R_{i1} - (1+\mu_1)R_k$. Therefore $\tau_{rep} = C_1 \left\{ R_{g2} + \frac{R_{a1}[R_{i1} + (1+\mu_1)R_k]}{R_{a1} + R_{i1} + (1+\mu_1)R_k} \right\}$, or, considering that $R_{g2} \gg R_{a1} > \frac{R_{a1}[R_{i1} + (1+\mu_1)R_k]}{R_{a1} + R_{i1} + (1+\mu_1)R_k}$,

$$\tau_{rep} \approx C_1 R_{g2} \qquad \text{(VI.54)}$$

To find pulse duration, one must use $t = t_u$ in expression (VI.53), while $u_{g2} = E_{g02}$. Then we will get

$$E_{g02} = (U_{g2\,нач} - U_{g2\,\infty}) e^{-\frac{t_u}{\tau_{rep}}} + U_{g2\,\infty}$$

or

$$e^{\frac{t_u}{\tau_{rep}}} = \frac{U_{g2\,\infty} - U_{g2\,нач}}{U_{g2\,\infty} - E_{g02}}.$$

As is evident from Figure VI.21, only the initial linear sector of recharge exponential curve 1 corresponds to the quasistable state. But, given that the condition whereby the exponential curve initial sector is used ($t_и \ll \tau_{пер}$ or $\frac{t_и}{\tau_{пер}} \ll 1$), the latter equality may be rewritten as

$$1 + \frac{t_и}{\tau_{пер}} = \frac{U_{gk2\infty} - U_{gk2\,мин}}{U_{gk2\infty} - E_{go2}},*$$

hence

$$t_и = \tau_{пер} \frac{E_{go2} - U_{gk2\,мин}}{U_{gk2\infty} - E_{go2}}.$$

Substituting expressions for $U_{gk2\,мин}$ from (VI.39), $U_{gk2\infty}$ from (VI.52), and $\tau_{пер}$ from (VI.54) in the latter equality, we will get /260

$$t_и = C_1 R_{g2} \frac{I_{a1}(R_{a1} + R_k) - I_{a2}R_k + E_{go2}}{E_a - I_{a1}R_k - E_{go2}}.$$

Considering that $E_a \gg |I_{a1}R_k + E_{go}|$ ($E_a \gg I_{a1}R_k$; $E_a \gg |E_{go}|$ and terms $I_{a1}R_k$ and E_{go} have different signs) in the denominator of this expression, finally we will get

$$t_и \approx C_1 R_{g2} \frac{I_{a1}(R_{a1} + R_k) - I_{a2}R_k + E_{go2}}{E_a}. \qquad \text{(VI.55)}$$

Consequently, pulse duration $t_и$ linearly will depend on current I_{a1} flowing across triode L_1 in the quasistable state. But, the magnitude of this current in turn linearly will depend on the magnitude of bias E_{gz}. This is explained in Figure VI.22, where current I_{a1} values ($I''_{a1} > I'_{a1} > I_{a1}$) are found from the triode dynamic characteristic and feedback line for three values E_{gz} ($E''_{gz} > E'_{gz} > E_{gz}$). It goes without saying that this linear relationship will take place during E_{gz} changes only within those limits in which the operating point remains in the dynamic characteristic linear sector. Thus, when the aforementioned condition is satisfied, pulse duration $t_и$ linearly will depend on bias E_{gz} magnitude.

*When $x \ll 1$ $e^x \approx 1 + x$.

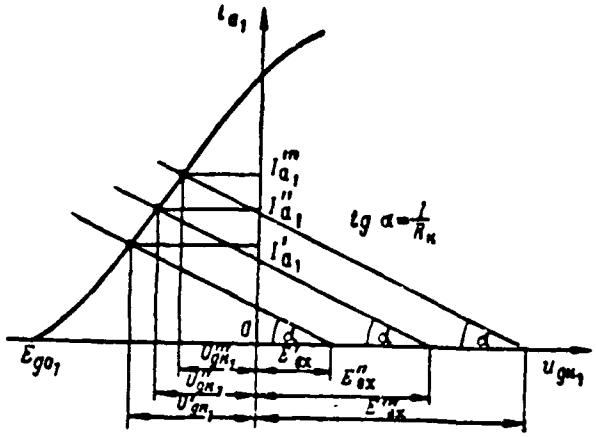


Figure VI.22. For Explanation of Current I_{a1} Linear Relationship to Bias E_{ex} Magnitude.

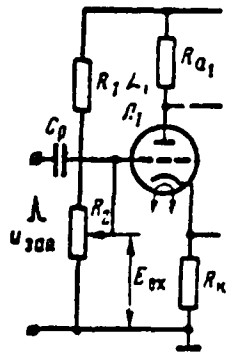


Figure VI.23. Magnitude E_{ex} Control in a Cathode-Coupling Retarding-Field Monostable Multivibrator.

Therefore, a cathode-coupling retarding-field monostable multivibrator may be used for pulse duration linear modulation with voltage $E_{вх}$, i. e., as a linear pulse stretcher. Voltage $E_{вх}$ in this instance is controlled using the circuit depicted in Figure VI.23 (pulse duration linearly will depend on the magnitude of R_2 contact arm displacement) or is supplied by the previous (control) stage.

EXERCISE VI.9

a) Draw voltage $u_{вых}$ curves for three voltage $E_{вх}$ values corresponding to Figure VI.22 and use these curves to explain the relationship of pulse duration $\tau_и$ to voltage $E_{вх}$ magnitude.

b) Can pulse duratation be controlled by voltage $E_{вх}$ (see Figure VI.23) in a cathode-coupling "zero"-grid monostable multivibrator?

c) Indicate possible methods of converting a cathode-coupling retarding-field monostable multivibrator to the free-running mode. (Page 482)

3. Monostable Multivibrator Triggering and Forced Cutoff

The simplest circuits for triggering monostable multivibrators with positive pulses were depicted in Figures VI.17 and VI.19. In practice, triggering of monostable multivibrators, as was the case with flip-flops, usually occurs across trigger tubes with negative pulses using a normally-unblanked triode.

A typical circuit for triggering a monostable multivibrator across trigger diode D is depicted in Figure VI.24a, while one in which triggering occurs across trigger triode $Л_3$ is depicted in Figure VI.24b. The circuits depict cathode-coupling retarding-field monostable multivibrators assembled on dual triodes, while the dotted line depicts cutoff networks, which will be examined below. In the first circuit, a trigger pulse of negative polarity is supplied across transient network $C_р R_з$ to diode D cathode. In the second circuit, a trigger pulse of positive polarity is supplied across transient network $C_р R_з$ to grid of triode $Л_3$, normally blanked by negative bias E_g. Both circuits are analogous to the corresponding flip-flop asymmetrical trigger circuits to plates (Figure VI.10b, c) with the single difference that only that part of the flip-flop trigger circuit connected

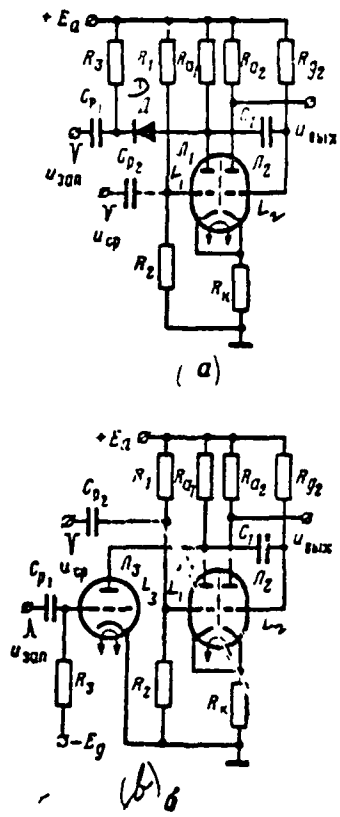


Figure VI.24. Typical Circuits for Monostable Multivibrator Triggering and Forced Cutoff.

to plate of normally-blanked triode L_1 is used to trigger a multivibrator. In both cases, as the trigger pulse acts upon this plate, a temporary negative pulse arises due to trigger tube current. This pulse is transmitted across capacitor C_1 to grid of normally-unblanked triode L_2, reducing its plate current. Here, /262 the voltage drop across resistance $R_к$ ($u_к = i_{a2}R_к$), i. e., triode L_1 cathode potential, decreases. As a result, triode L_1 unblanks, which also causes a circuit reversal. During the reversal process and still prior to its conclusion, diode D or triode L_3 blank in connection with a rapid reduction in triode L_1 plate and are cut out from the trigger pulse generator multivibrator.

As is already known, monostable multivibrator counter reversal to the initial

stable state occurs spontaneously when negative grid voltage of triode L_2 unblanked in the quasistable state, rising, reaches cutoff voltage. Here, the moment of counter reversal and, consequently, duration of the pulse shaped by the multivibrator, will depend on circuit parameters and supply voltage magnitudes, which may change during the operating process. Therefore, in some instances, stability of the shaped pulse duration turns out to be insufficient even when a retarding-field circuit optimum for this situation is used.

Synchronization of the moment of counter reversal by an external pulse, which will arrive after a certain period of time following the trigger pulse and which causes forced circuit counter reversal, is brought about in order to have strict shaped pulse duration stabilization. Forced counter reversal is referred to as multivibrator forced cutoff (or simply cutoff) and the external pulse causing this reversal is referred to as a cutoff pulse. It is evident that a cutoff pulse must act mandatorily on a circuit somewhat before it spontaneously returns to the initial state, i. e., the moment of forced counter reversal must precede the moment of natural circuit counter reversal. Here, forced shaped pulse /263 duration $t_{и3}$ will be determined exclusively by the time interval between trigger pulse and cutoff pulse and will be correspondingly less than the real duration of pulse $t_{и0}$, generated without forced cutoff $(t_{и3} < t_{и0})$.

Cutoff pulses usually are of negative polarity and, as depicted in Figure VI.24a, b, are supplied across transient capacitor $C_{р2}$ to grid of triode L_1 unblanked after triggering. An amplified positive pulse arises in this triode plate network due to cutoff pulse action and is transmitted across coupling capacitor C_1 to grid of triode L_2 blanked in the quasistable state. Triode L_2 unblanks if this pulse is of sufficient amplitude and a forced reversal of the circuit to the stable state occurs.

The forced cutoff mechanism is explained in Figure VI.25, where it is accepted for simplicity that, following triggering that occurred at moment t_1, voltage $u_{а.к2}$ rises by a linear law. Without a forced cutoff, the circuit would revert to the initial state at moment t_5, having shaped a pulse with duration $t_{и0}$. Under the stimulus of the cutoff pulse, the circuit returns to the stable state earlier (at moment t_3), shaping a pulse of duration $t_{и3}$. Here, minimum cutoff

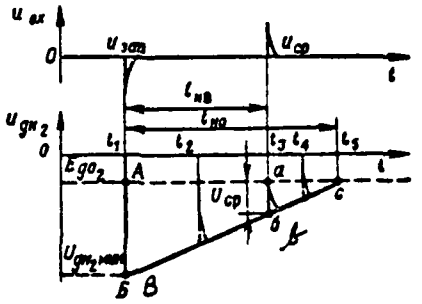


Figure VI.25. Monostable Multivibrator Forced Cutoff.

pulse amplitude $U_{ср.\ мин}$ must insure an increase in voltage u_{g_2} under the stimulus of this pulse to the level of cutoff voltage E_{go2}.

If a cutoff pulse of identical amplitude arrived even earlier (at moment t_2), when voltage u_{g_2} still had not risen sufficiently, then triode L_2 would remain blanked, i. e., no forced circuit reversal would occur. If, on the other hand, the cutoff pulse arrived later (at moment t_4), then its amplitude may be decreased accordingly but, since voltage u_{g_2} by this moment already has almost reached cutoff voltage, forced cutoff reliability would be reduced (given a slight stray rise in cutoff voltage magnitude, the circuit may reverse spontaneously).

One may obtain the expression linking requisite cutoff pulse amplitude $U_{ср}$ at triode L_2 grid with the given pulse duration and circuit parameters /264 easily by using Figure VI.25. Actually, due to the similarity of triangles ABC and $a\delta C$, we have

$$\frac{U_{g_2\ мин} - E_{go2}}{t_{и0}} = \frac{U_{ср.\ мин}}{t_{и0} - t_{и1}},$$

hence

$$U_{ср.\ мин} = \frac{t_{и0} - t_{и1}}{t_{и0}} (U_{g_2\ мин} - E_{go2})$$

or

$$U_{cp} > \left(1 - \frac{t_{w0}}{t_{w1}}\right)(U_{g2\,max} - E_{g2}). \qquad \text{(VI.56)}$$

Usually, a ratio $\frac{t_{w0}}{t_{w1}}$ on the order of $0.5 \div 0.7$ is selected.

EXERCISE VI.10

Under what conditions should you use a forced-cutoff monostable multivibrator rather than an asymmetrically-triggered flip-flop to shape pulses of a given duration? (Page 483)

§ 4. MULTIVIBRATORS IN THE FREE-RUNNING MODE

1. Basic Multivibrator Circuit

Examining the cathode-coupling monostable multivibrator circuits, we saw that any of them may transfer to the free-running mode if the condition for blanking triode L_1 in the stable state is disrupted by triode L_2 plate current (see Exercise VI.8c, VI.9c). Here, however, the processes of charging and discharging (for circuits with a retarding field -- recharging) of one and the same capacitor C_1, which flow with materially different time constants $\tau_{pasp} \gg \tau_{sap}$ will determine how long the circuit remains both in one and then in the other quasistable state. This will constrain the range of possible values for generated pulse duty ratio.

Therefore, a multivibrator with two plate-grid couplings usually is used for operations in the free-running mode. A circuit for such a multivibrator is depicted in Figure VI.26 and is referred to as a basic multivibrator circuit. If all the parameters of its arms are identical, i. e., identical tubes and $R_{a1} = R_{a2}$, $C_1 = C_2$, $R_{g1} = R_{g2}$, then it is referred to as a symmetrical circuit.

We will compare the basic multivibrator circuit with a symmetrical flip-flop circuit (Figure VI.15a). In the flip-flop, the plate coupling of each triode with the grid of the other triode is accomplished across voltage dividers R_1, R_{g2} and R_2, R_{g1}, i. e., both for the d-c and a-c component. This coupling in

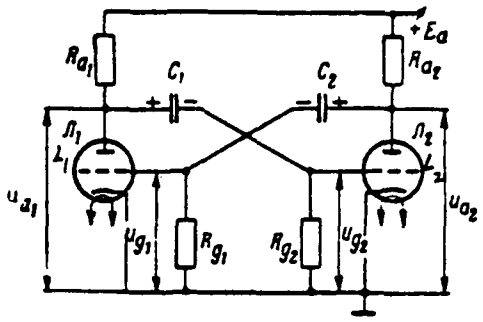


Figure VI.26. Multivibrator With Two Plate-Grid Couplings in the Free-Running Mode (Basic Circuit).

the multivibrator is accomplished across R-C networks C_1R_{g2} and C_2R_{g1}, i. e., only for the a-c component. In addition, an outside negative bias E_g source is absent in the multivibrator. Therefore, first, in a multivibrator as opposed to the flip-flop, plate voltage jumps across capacitors C_1 and C_2 are transmitted completely to grids:*

$$\mp \Delta U_{a1} = \mp \Delta U_{g2}, \quad \mp \Delta U_{a2} = \mp \Delta U_{g1}, \tag{VI.57}$$

and, second, and especially important, there are no reasons for fixed triode blanking.

The latter circumstance leads to the fact that both flip-flop stable equilibrium states are replaced in the multivibrator by temporary stable (quasistable) states.

Actually, the voltage drop across resistance R_g applied with a "minus" to triode grid, i. e., arising during the flow through it of current in the "from below upwards" direction may be the only reason for blanking of any triode in a basic multivibrator circuit. But, only the discharging current connecting the coupling capacitor across the other (unblanked) triode to the grid of this triode may play the role of such current. Since capacitor discharging current decays over time by the law of exponents, then each triode may be blanked only for a limited time from the moment the other triode unblanks (the given capacitor will begin to discharge).

*Capacitor C_1 and C_2 voltages do not succeed in changing at time of reversal.

Thus, the rate of capacitor C_1 discharge will determine how long the circuit remains in one quasistable state (triode L_1 unblanked, triode L_2 blanked), while the rate of capacitor C_2 discharge will determine how long it remains in the second state (triode L_1 blanked, triode L_2 unblanked). Therefore, both capacitors are circuit timing (time-supplying) elements. That state in which both triodes are unblanked, for both a multivibrator and flip-flop, is a state of unstable equilibrium from which the circuit will convert with a jump to one of the quasistable states when self-excitation conditions are satisfied. The action of the positive feedback loop when triodes are unblanked is analogous to a flip-flop and corresponds to the symbolic rendition (VI.4). The self-excitation conditions undergo somewhat of a change in connection with the change in plate-grid coupling type.

First off, capacitors C_1 and C_2 connected to these couplings in series /266 cause additional voltage phase shifts during their transmission from the plate of one triode to the grid of the other, resulting in the possibility of disruption of the phase self-excitation condition (VI.2) (we will recall that requisite phase shifts in the circuit are insured by the difference in phase of each triode's plate and grid voltages).

It is evident that capacitors C_1 and C_2 will exert the greatest influence on passage of the low-frequency harmonics of the spectrum of pulses generated by the circuit. Considering the spectral content of a periodic video pulse train (see Attachment 1), it is necessary that additional phase shifts be slight, even for the spectrum's first harmonic, whose frequency equals pulse repetition frequency $\Omega_1 = 2\pi F_n = \frac{2\pi}{T_n}$. It follows from this that the phase self-excitation condition will lead to the requirement

$$\Omega_1 \gg \frac{1}{\tau_g} \qquad \text{or} \qquad \tau_g \gg \frac{T_n}{2\pi}, \tag{VI.58}$$

where τ_g -- least of the grid network time constants equalling C_1R_{g2} or C_2R_{g1}.

In other words, it is necessary that these networks be transient rather than differentiating for all pulse spectrum harmonics, including the first harmonic.

Now we will switch to the amplitude self-excitation condition (VI.2a). The

circuit under examination includes two amplifying stages with plate loads, each of which during a reversal (for rapid u_a changes) is shunted across the coupling capacitor connected to it by resistance R_{gk} between the other tube's grid and cathode (by the input resistance of the other stage). Therefore, based upon (III.49) and considering ratio (VI.57), we will get

$$|K_1| = \frac{\mu_1}{R_{a1} + R_{i1}} \cdot \frac{R_{a1}R_{gk2}}{R_{a1} + R_{gk2}}; \quad |K_{II}| = \frac{\mu_2}{R_{a2} + R_{i2}} \cdot \frac{R_{a2}R_{gk1}}{R_{a2} + R_{gk1}},$$

where the second multiplier in each expression is stage load equivalent impedance.

It should be considered in each of these formulas that, due to the result of the electrical valve-like properties of each tube's grid--cathode path, its resistance R_{gk} and, consequently, the other tube's gain as the circuit operates, radically change in magnitude. Actually, when the circuit reverses in one direction (L_1 unblanks, L_2 blanks), voltage u_{gk1} rises with a jump and will become positive, while voltage u_{gk2} decreases and will become negative; the reverse is true when the circuit reverses in the other direction. But, when $u_{gk}>0$, grid current appears in the tube and, as a result of slight grid--cathode conducting path resistance $r_{gk} \ll R_g$, we get $R_{gk} \approx r_{gk}$. When $u_{gk}<0$, tube grid current is absent and $R_{gk}=R_g$. Therefore, for circuit reversal in one direction (L_1 unblanks, L_2 blanks), self-excitation condition (VI.2a) must be written in the form /267

$$\left(\frac{\mu_1}{R_{a1} + R_{i1}} \cdot \frac{R_{a1}R_{g2}}{R_{a1} + R_{g2}}\right)\left(\frac{\mu_2}{R_{a2} + R_{i2}} \cdot \frac{R_{a2}r_{gk1}}{R_{a2} + r_{gk1}}\right) > 1. \qquad \text{(VI.59)}$$

But, since $R_g \gg R_a$, $r_{gk} \ll R_a$, then the expressions for stage load equivalent impedances are simplified, i. e., $\frac{R_{a1}R_{g2}}{R_{a1} + R_{g2}} \approx R_{a1}$; $\frac{R_{a2}r_{gk1}}{R_{a2} + r_{gk1}} \approx r_{gk1}$. Also considering that ratio (VI.59) must be supplemented by the analogous ratio for circuit reversal in the opposite direction, finally we will get

$$\frac{\mu_1 R_{a1}}{R_{a1} + R_{i1}} \cdot \frac{\mu_2 r_{gk1}}{R_{a2} + R_{i2}} > 1; \quad \frac{\mu_2 r_{gk2}}{R_{a1} + R_{i1}} \cdot \frac{\mu_1 R_{a2}}{R_{a2} + R_{i2}} > 1 \qquad \text{(VI.60)}$$

or, for a symmetrical circuit ($\mu_1 = \mu_2 = \mu$; $R_{a1} = R_{a2} = R_a$; $R_{i1} = R_{i2} = R_i$; $r_{g01} = r_{g02} = r_{g0}$)

$$\left(\frac{\mu}{R_a + R_i}\right)^2 R_a r_{g0} > 1. \qquad \text{(VI.60a)}$$

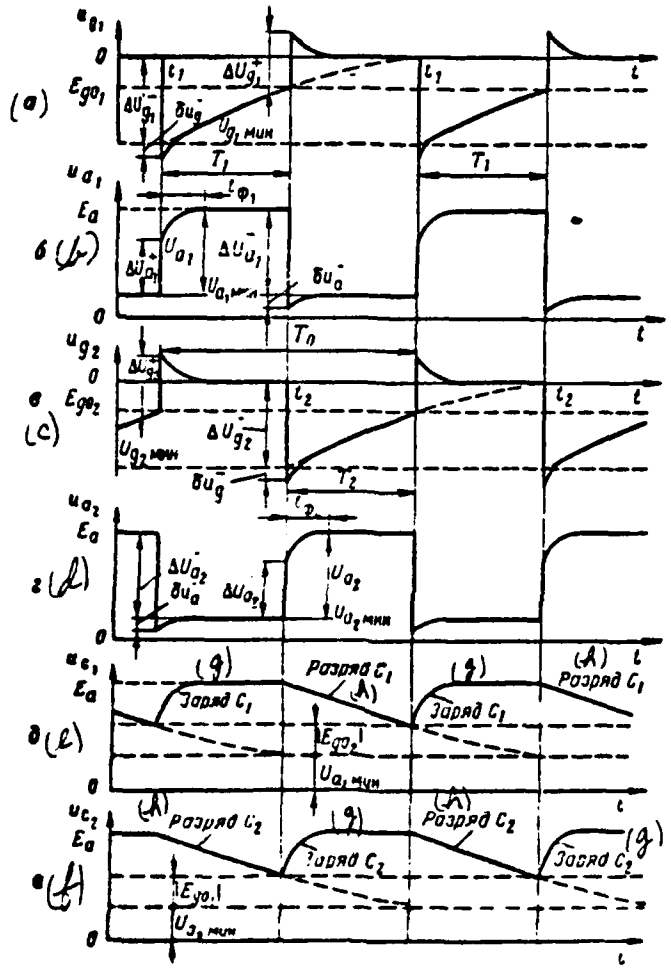


Figure VI.27. Voltage Curves in a Symmetrical Basic Multivibrator Circuit. (g) — Charge; (h) — Discharge.

Voltage curves in multivibrator characteristic points without considering stray capacitances for a symmetrical circuit are depicted in Figure VI.27. We

will examine circuit operation, beginning with moment t_1 when, as a result of positive feedback loop action, triode L_1 blanked and triode L_2 unblanked.

At that moment, triode L_1 plate current rises with a jump, in connection with which capacitor C_1 begins to charge. Meanwhile, triode L_2 plate voltage decreases with a jump, in connection with which capacitor C_2 begins to discharge.

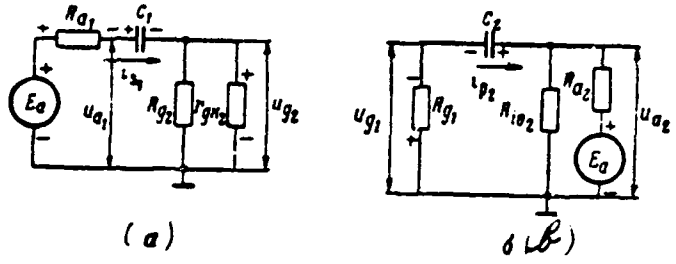


Figure VI.28. Equivalent Circuits for Capacitor C_1 Charge (a) and Capacitor C_2 Discharge (b).

Equivalent circuits for capacitor C_1 charge and C_2 discharge are depicted in Figure VI.28. Capacitor C_1 charging current $i_{з1}$ flows through network $+E_a$, resistance R_{a1}, capacitor C_1, parallel-connected resistances R_{g2} and r_{gk2} (equivalent resistance R_{gk2}), chassis ($-E_a$). Capacitor C_2 discharging current i_{p2} flows through network capacitor C_2 ("plus" plate), parallel-connected resistances R_{io2} (triode L_2 internal d-c resistance) and R_{a2}, resistance R_{g1}, capacitor C_2 ("minus" plate).

If you disregard capacitor C_1 charge, then the voltage u_{a2} negative step transmitted at moment t_1 across capacitor C_2 to triode L_1 grid will equal (see Figure VI.27a, d)

$$-\Delta U_{a2} = -\Delta U_{g1} = -I_{a2}R_{a2} = -I_{p2}R_{g1}, \qquad \text{(VI.61)}$$

where I_{a2} -- triode L_2 plate current magnitude when $u_{g2} = 0$;
I_{p2} -- capacitor C_2 discharging current amplitude.

Here, voltage u_{a2} will decrease to value

$$U_{a2\,мин} = E_a - I_{a2}R_{a2}. \tag{VI.62}$$

while voltage u_{g1} will decrease to value $U_{g1\,мин}$, which must insure reliable /269 triode L_1 blanking:

$$U_{g1\,мин} = -\Delta U_{g1} = -I_{a2}R_{a2} < E_{go1} \tag{VI.63}$$

Voltage u_{a1} must rise with a jump by magnitude $I_{a1}R_{a1}$, where I_{a1} -- triode L_1 plate current magnitude when $u_{g1} = 0$, and reach value $U_{a1\,макс} = E_a$.

However, in accordance with VI.28a, capacitor C_1 charging current, flowing across resistance R_{a1}, decreases triode L_1 plate potential. Therefore, the voltage u_{a1} positive step transmitted across capacitor C_1 to triode L_2 grid decreases and turns out to equal only (see Figure VI.27b, c)

$$+\Delta U_{a1} = +\Delta U_{g2} = (I_{a1} - I_{s1})R_{a1} = I_{s1}r_{gk2} + |E_{go2}|. \tag{VI.64}$$

where I_{s1} -- capacitor C_1 discharging current amplitude.

The last expression in (VI.64) is explained by the fact that step ΔU_{g2} begins with negative level E_{go2} (we will recall that the circuit reversal examined results from unblanking of previously-blanked triode L_2) and, due to current i_{s1}, triode L_2 grid potential must exceed the zero level (cathode potential) by magnitude $I_{s1}R_{gk2}$, where $R_{gk2} \approx r_{gk2}$ ($r_{go2} \ll R_{g2}$)*:

Thus, voltage u_{g2} rises with a jump to value

$$U_{g2\,макс} = I_{s1}r_{gk2} > 0. \tag{VI.65}$$

Due to this fact, unblanked triode L_2 plate current slightly will exceed magnitude I_{a2} corresponding to fixed value $u_{g2} = 0$, resulting in voltages u_{a2} and u_{g2} additionally dropping by magnitude $\delta u_a = \delta u_g$ (Figure VI.27a, d).

*When $u_{g2} > 0$, capacitor C_1 charges in triode L_2 main grid current $(i_{s1} = i_{g2})$.

Triode L_1 blanking breaks the positive feedback loop and the circuit converts to the quasistable state. Capacitor C_1 charging and C_2 discharging processes, /270 which began at the moment of reversal, continue in this state. The capacitor C_2 discharging process is the most important since it is exactly because of current i_{p2} that triode L_1 is maintained in the blanked state, while triode L_2 is unblanked. Actually, during the capacitor discharging process, the voltage in it will strive to decrease to value $U_{c2\,min}$ (Figure VI.27f), current i_{p2} will strive to decrease to zero, while negative voltage $u_{g1} = -i_{p2}R_{g1}$ will strive to rise to voltage $U_{g1} = 0$ (Figure VI.27a) with time constant τ_{pasp2}, which will be found easily from Figure VI.28b:

$$\tau_{pasp2} = C_2\left(R_{g1} + \frac{R_{c2}R_{a2}}{R_{c2} + R_{a2}}\right) \approx C_2R_{g1}. \qquad \text{(VI.66)}$$

since $R_{g1} \gg \frac{R_{c2}R_{a2}}{R_{c2} + R_{a2}}$.

However, as long as voltage u_{g1} remains less than cutoff voltage E_{go1}, triode L_1 remains blanked. The capacitor C_1 charging process occurs with time constant τ_{zap1}, which will be found from Figure VI.28a and, since $r_{gk2} \ll R_{g2}$ and $r_{gk2} \ll R_{a1}$, equals

$$\tau_{zap1} = C_1\left(R_{a1} + \frac{R_{g2}r_{gk2}}{R_{g2} + r_{gk2}}\right) \approx C_1(R_{a1} + r_{gk2}) \approx C_1R_{a1}. \qquad \text{(VI.67)}$$

Equating expressions (VI.67) and (VI.66), we see that, since $R_{a1} \ll R_{g1}$, then $\tau_{zap1} \ll \tau_{pasp2}$ and, consequently, capacitor C_1 charging succeeds in ceasing completely during the time the circuit remains in the quasistable state. Here, capacitor C_1 voltage rises by the law of exponents to value E_a (Figure VI.27e), current i_{a1} decays to zero in accordance with the same law, voltage u_{a1} rises to value $U_{a1\,max} = E_a$ (Figure VI.27b), voltage u_{g2} decreases to value $U_{g2} = 0$ (Figure VI.27c), in which connection voltage u_{a2} rises to value $U_{a2\,max}$ (Figure VI.27d). At moment t_2 when voltage u_{g1}, rising, equates to cutoff voltage E_{go1}, triode L_1 unblanks, the positive feedback loop again closes, and circuit reversal occurs in the opposite direction. Here, voltages u_{a1} and u_{g2} decrease with a jump, resulting in the fact that triode L_2 blanks, while voltages u_{g1} and u_{a2} rise with a jump. The

identical circumstances that came into play in the first reversal determine the magnitude of these steps.

The circuit will convert to the second quasistable state following reversal, during which occurs the process of capacitor C_2 charging due to the voltage u_{a2} positive step and capacitor C_1 discharging caused by the voltage u_{a1} negative step.

Equivalent capacitor C_1 charging and C_2 discharging circuits correspond to the circuits depicted in Figure VI.28a, b if all indices in these circuits are replaced by their opposites. Therefore, capacitor C_1 discharge occurs with /271 time constant

$$\tau_{разр1} \approx C_1 R_{g2}, \tag{VI.68}$$

while capacitor C_1 charge occurs with time constant

$$\tau_{зар2} \approx C_2 R_{a2} \tag{VI.69}$$

The determinant here is capacitor C_1 discharging since triode L_2 is maintained in the blanked state due to current i_{g1}. During this capacitor's discharging process, the voltage in it will strive to decrease to value $U_{a2\,мин}$, while negative voltage u_{g2} will strive to rise to zero.

Since $\tau_{зар2} \ll \tau_{разр1}$ ($R_{a2} \ll R_{g2}$), then the process of charging capacitor C_2 to voltage E_a while the circuit remains in the second quasistable state succeeds in ceasing completely. As a result of this, a gradual (exponential) rise in voltage u_{a2} to value $U_{a2\,макс} = E_a$, following the corresponding spasmodic changes occurs, voltage u_{g1} decreases to zero, and voltage u_{a1} increases to value $U_{a1\,мин} = E_a - I_{a1} R_{a1}$.

At moment $t_3(t_1)$, when voltage u_{g2}, rising, equates to cutoff voltage E_{go2}, the next circuit reversal occurs: triode L_2 unblanks with a jump, while triode L_1 blanks. Further, the processes repeat themselves.

Thus, antiphase periodic pulse trains of almost square shape (Figure VI.27b, d)

are shaped in triode plates. The complete cycle of circuit operation (pulse repetition period) equals

$$T_0 = T_1 + T_2^*, \tag{VI.70}$$

where T_1 -- cycle portion equalling the amount of time the circuit remains in one quasistable state (duration of the positive pulse at triode L_1 plate);

T_2 -- cycle portion equalling the amount of time the circuit remains in the second quasistable state (duration of the positive pulse at triode L_2 plate).

Capacitor C_1 and C_2 discharging processes determine intervals T_1 and T_2 and will be found as follows. During time $t = T_1$ ($t_1 < t < t_2$), negative voltage u_{g1} rises from value $U'_{g1\,max}$ to value E_{go1} based on the law $u_{g1} = U'_{g1\,max} e^{-\frac{t}{\tau_{разр1}}}$. Assuming $u_{g1} = E_{go1}$ where $t = T_1$, we will get $E_{go1} = U'_{g1\,max} e^{-\frac{T_1}{\tau_{разр1}}}$, from whence, after taking the logarithm and considering expressions (VI.63) and (VI.66)

$$T_1 = \tau_{разр2} \ln \frac{U'_{g\,max}}{E_{go2}} = C_2 R_{g1} \ln \frac{I_{a1} R_{a1}}{|E_{go1}|}. \tag{VI.71}$$

From analogous discussions for interval T_2, we will get /272

$$T_2 = \tau_{разр1} \ln \frac{U'_{g1\,max}}{E_{go1}} = C_1 R_{g2} \ln \frac{I_{a2} R_{a2}}{|E_{go2}|}. \tag{VI.72}$$

As demonstrated in Figure VI.27, $T_1 = T_2$ for a symmetrical circuit.

Plate voltage pulse amplitudes obtained accordingly equal

$$U'_{a1} = E_a - U_{a1\,min} = I_{a1} R_{a1};\ U'_{a2} = E_a - U_{a2\,min} = I_{a2} R_{a2} \tag{VI.73}$$

*We disregard the time of circuit reversal in both directions.

Considering (VI.67) and (VI.69), duration of the positive exponential porches of pulses caused by capacitor C_1 and C_2 charging processes equals

$$t_{p1} \approx 3\tau_{зар1} = 3C_1R_{a1}; \quad t_{p2} \approx 3\tau_{зар2} = 3C_2R_{a2}. \qquad \text{(VI.74)}$$

These ratios constrain multivibrator minimum pulse duration.

The Figure VI.27 curves are plotted without considering the input and output capacitances of each stage. The influence of these stray capacitances, just as was the case in a flip-flop, will rule out instantaneous circuit reversals, resulting in the fact that spasmodic voltage changes occur at a finite rate and will lead to additional stretching of generated pulse porch and droop.

Circuit parameters are selected from the following basic considerations. Plate load impedances R_{a1} and R_{a2} are selected in accordance with (VI.73) from the condition that requisite pulse amplitude be obtained; their magnitude usually will fall within the bounds of 3--10 kilohms. Coupling capacitor capacitance to obtain a slight pulse rise time in accordance with (VI.74) must be as low as possible, but significantly exceed circuit stray capacitances, and usually are selected on the order of one or several hundred picofarads. Resistances R_{g1} and R_{g2} to obtain self-excitation conditions (VI.58) and (VI.60) and pulse shape approximating a square pulse (satisfaction of ratios $\tau_{разр1} \gg \tau_{зар2}$ and $\tau_{разр2} \gg \tau_{зар1}$) must be significantly greater than plate load impedances $R_{g1} \gg R_{a2}$, $R_{g2} \gg R_{a1}$ and are established, depending on given pulse duration, on the order of tens or hundreds of kilohms.

The repetition frequency of the pulses generated by the circuit $F_п = \frac{1}{T_п} = \frac{1}{T + T_1}$ may range from unities of Hertz to hundreds of kilohertz. Pulse duration T_1 and T_2 control in accordance with (VI.71) and (VI.72) occurs either by a change in resistances R_{g1} and R_{g2} (smoothly) or by switching the coupling capacitors (discretely).

Asymmetrical circuits with unequal discharge time constants ($\tau_{разр1} \neq \tau_{разр2}$) /273 must be used to obtain pulses with unequal intervals ($T_1 \neq T_2$). Usually, a varied resistance R_{g1} and R_{g2} or (to obtain great circuit asymmetry) or capacitor C_1 and C_2 capacitances insures this. We will examine what is used to constrain the

maximum possible duty ratio value of pulses picked off, for example, triode L_1 plate: $Q_1 = \frac{T_1 + T_2}{T_1}$. There is a requirement that C_2 capacitance in expression (VI.71) be less than C_1 capacitance in expression (VI.72) to the maximum extent possible in order that pulse duration $t_u = T_1$ is less than resting time duration $t_n = T_2$ to the maximum possible extent. However, when $C_2 \ll C_1$, capacitor C_1 charging time constant will coincide with the capacitor C_2 discharging time constant. As a result, capacitor C_1 will not succeed in discharging during intervals T_1 and circuit operation will be disrupted. Therefore, the duty ratio of pulses generated by a multivibrator, even if their shape is immaterial, rarely exceeds the value 100.

EXERCISE VI.11

a) Draw the curves of voltages u_{g1}, u_{g2}, and u_{a2} for an asymmetrical basic multivibrator circuit if $R_{g1} = 2R_{g2}$ and remaining arm parameters are identical.

b) How is it possible to convert a basic multivibrator circuit to the monostable mode? Draw such a circuit when it is triggered by negative pulses and draw the curves of voltages $u_{...}$, u_{g1}, and u_{g2}. What will determine duration of the pulse this circuit generates? (Page 483)

2. Improved Variants of the Basic Multivibrator Circuit

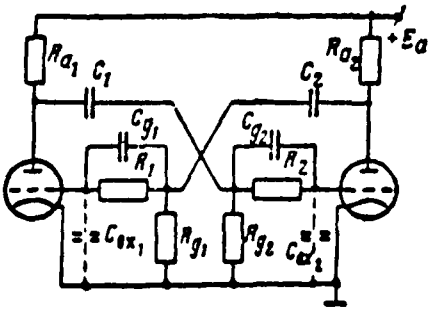


Figure VI.29. Multivibrator With Improved Pulse Shape.

The shape of plate voltage pulses in the basic multivibrator circuit is distorted mainly due to stretching of the leading edge caused by coupling capacitor charging

processes. The circuit depicted in Figure VI.29 may be used to improve this leading edge. Basic circuit structure and operating principle remain unchanged. Additional resistances R_1 and R_2 are connected to the capacitor C_1 and C_2 charging network and, therefore, decrease the amplitude of charging currents $I_{з1}$ and $I_{з2}$ picked off tube plate potentials after tube blanking. As a result of this, the magnitude of plate voltage positive steps rises (VI.64): $+\Delta U_{a1}=(I_{a1}-I_{з1})R_{a1}$ and $+\Delta U_{a2}=(I_{a2}-I_{з2})R_{a2}$. Resistances R_1 and R_2 on the order of 100 kilohms /274 are selected in order to obtain a noticeable effect. However, here a gradual rise in plate voltages after steps to values $U_{a\,макс}=-E_a$ occurs very slowly due to the significant increase in charging time constants $\tau_{зар1}$ and $\tau_{зар2}$. Therefore, a sloped pulse tilt results. In addition, resistances R_1 and R_2, along with circuit input capacitances $C_{вх1}$ and $C_{вх2}$ form an integrator constraining rapid voltage u_{g1} and u_{g2} changes at the moment of reversal. As a result, reversal processes are stretched out and voltage step transconductance decreases. Acclerating capacitors C_{g1} and C_{g2} of slight capacitance (20--30 pF) shunt resistances R_1 and R_2 in order to reduce the deleterious influence of the input capacitances. These capacitors act just like they did in the flip-flop. The shape of the plate voltage pulse for the circuit being examined is depicted in Figure VI.30 (pulse shape for the conventional basic circuit is depicted by the dotted line in this figure).

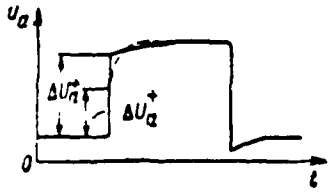


Figure VI.30. Figure VI.29 Circuit Pulse Shape.

The load connected to the plate of one (or both) triodes may impact materially on a multivibrator's free-running frequency. The pentode multivibrator circuit depicted in Figure VI.31 may be used to reduce the impact of load. Pentode screen grid networks play the role of multivibrator plate networks in this circuit. Output voltages are picked off pentode plates. Since capacitive coupling between pentode plates and screen grids is very slight due to presence of suppressor grids, the impact of load on circuit operation essentially is eliminated.

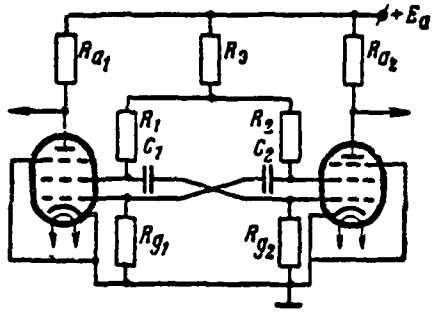


Figure VI.31. Pentode Multivibrator.

The repetition frequency of the pulses the basic circuit generates may change significantly when tubes are replaced and when there are supply voltage oscillations and stray parameter changes. This is caused by the slight transconductance of a blanked tube grid voltage rise when they intersect cutoff voltage levels. The retarding-field multivibrator circuit depicted in Figure VI.32 often is used to increase free-running frequency stability. Processes of capacitor C_1 and /275 C_2 recharge to voltages $E_a - U_{a\,min}$ occur in this circuit instead of the processes of their discharge to voltages $U_{a\,min}$. As a result, just as was the case in the retarding-field monostable multivibrator (see Figure VI.21), the rate of blanked tube grid voltage rise and, consequently, stability of the moments of their reversal, i. e., of both circuit reversals, rise significantly. In the main, the physics of circuit operation do not change.

EXERCISE VI.12

Prove the formulas for the duration of pulses T_1 and T_2 generated by the Figure VI.32 retarding-field multivibrator. (Page 485)

§ 5. LEVEL COMPARISON CIRCUIT (AMPLITUDE COMPARATOR)

A level comparison circuit provides precise registration of the moment of equality of two input voltages. A steep change (step) of circuit output voltage is generated at that moment. Usually, this change then is differentiated, resulting in a short comparison pulse, which also will serve as a marker for the moment of input voltage equality. One of the voltages compared by the circuit, as a

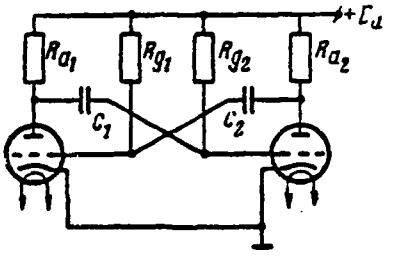


Figure VI.32. Retarding-Field Multivibrator.

rule, changes in accordance with a standard periodic law, has constant parameters, and is referred to as a reference pulse. The other is a slowly-changing ("constant") voltage and is referred to as control voltage since it controls comparison pulse position on the time axis.

Comparison circuit operating principle is explained in Figure VI.33, in which are depicted its structural diagram and voltage curves for two typical reference voltages, sinusoidal and sawtooth (linearly-changing).

The first comparison circuit variant (Figure VI.33b) may be used:

-- for conversion of sinusoidal reference voltage into square voltage pulses $u_{имп}$ whose duty ratio changes depending on voltage $u_{упр}$ magnitude;

-- to obtain, with the aid of sinusoidal calibration pulse voltage $u_{ср}$, whose repetition period rigidly is synchronized with period $T_{оп}$;

-- for precise determination of sinusoidal voltage phase by measuring /276 time intervals between comparison pulses and reference pulses supplying a zero phase reference.

In the latter two instances, control voltage is made equal to zero to eliminate the influence of sinusoidal voltage amplitude on comparison pulse position.

The second comparison circuit variant (Figure VI.33c) is used to obtain /277 a temporary comparison pulse time delay relative to the moments that a forward stroke of a sawtooth reference voltage begins. If this voltage during a forward stroke changes in accordance with a linear law, then the pulse delay also linearly will depend on control voltage magnitude. Actually, in accordance with Figure

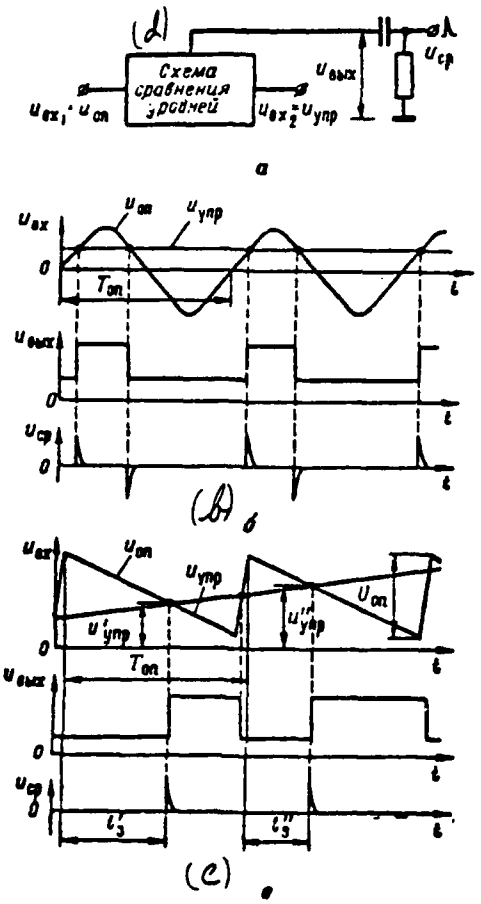


Figure VI.33. For Explanation of the Level Comparison Circuit Operating Principle. (d) -- Level comparison circuit.

VI.33c, disregarding the slight duration of voltage $u_{оп}$ return stroke, for the values of voltage $u_{упр}$ falling within the bounds $U_{оп.мин} < u_{упр} < U_{оп.мак}$, we will get:

$$t_з = T_{оп} - K(u_{упр} - U_{оп.мин}) \text{ и т.п. } \Delta t_з = -K\Delta u_{упр}. \qquad \text{(VI.75)}$$

where $K = \frac{T_{пл}}{T_{пл}} = \text{const}$.

Here, the delay interval in each period $T_{пл}$ corresponds to that voltage $u_{упр}$ value achieved at the moment of its equality with voltage $u_{оп}$ (voltage $u'_{упр}$ corresponds to delay t'_1, while voltage $u''_{упр}$ corresponds to delay t''_1, and so on).

Thus, a comparison circuit is used to obtain pulse-position modulation [PPM] -- conversion of information reflected by voltage $u_{упр}$ magnitude into comparison pulse phase (time position).

Generally speaking, it is possible to compare voltages using any nonlinear device whose volt-ampere characteristic has a sharp break. Thus, for example, limiter transition from the transfer to the clipping mode (or vice versa) occurs at the moment of equality of random-shape input voltage and constant reference voltage -- clipping threshold $E_{о}$ (see Chapter V). The difference between level comparison circuits and similar devices is that their output voltage will not depend on input voltage shape and changes with a jump only at the moment of equality of the latter.

A level comparison circuit must have two inputs. Since input voltages may change relative to each other as slowly as they please, then obtaining a precise change of voltage $u_{вых}$ at the moment of their equality is possible only due to onset of an avalanche-like process in the circuit. But, this requires that the positive feedback loop in the circuit close and the amplitude self-excitation condition be satisfied at the moment of transition. The circuit must be maintained by an input voltage in one of two states of stable equilibrium during the remaining time, depending on which of them is greater. For these reasons, level comparision circuits are assembled as two-stage square-wave generators operating in the control voltage external control mode.

One variety of such multivibrator-type circuits is depicted in Figure VI.34. It is similar to a cathode-coupling monostable multivibrator (see Figure VI.17), but has two inputs: sawtooth (linearly-dropping) reference voltage $u_{вх1} = u_{оп}$ /278

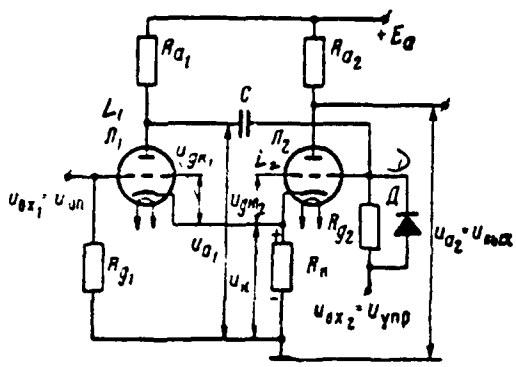


Figure VI.34. Multivibrator-Type Level Comparison Circuit.

is supplied to triode L_1 grid, while slowly-changing control voltage $u_{вх2} = u_{упр}$ is supplied to triode L_2 grid. Both voltages are positive.

In addition, large resistance $R_к$ and R_{g2} magnitude is characteristic of the circuit. We will explain below the requirement for this, as well as the role additional diode D plays. The overall circuit operating principle comprises the following.

Selected cathode load impedance $R_к$ is much greater than plate load impedances $R_к \gg R_{a1}$, $R_к \gg R_{a2}$. Therefore, both stages turn out to be enveloped by penetrating negative feedback and operate like cathode followers.

Since cathode follower gain is close to unity when $R_к$ magnitude is great, voltage $u_к$, which is created due to the unblanked tube current i_a flow across resistance $R_к$, approximates this tube's input voltage, i. e., $u_к = u_{вх} - u_{gk} \approx u_{вх}$. But, this voltage opposite in phase (with a "minus") turns out to be applied to the other tube grid. Therefore, at any given moment, that triode whose input voltage is higher unblanks and the other triode turns out to be blanked due to voltage $u_к$. If, for instance, $u_{оп} > u_{упр}$, then triode L_1 unblanks, $u_к = u_{вх1} = u_{оп}$, $u_{gk2} = u_{вх2} - u_{к2} \approx u_{упр} - u_{оп} < 0$ and triode L_2 is blanked. When $u_{оп} < u_{упр}$, on the other hand, triode L_2 is unblanked, while triode L_1 is blanked since $u_{gk1} = u_{оп} - u_{к2} \approx u_{оп} - u_{упр} < 0$. A positive feedback loop (VI.30), identical to the one in the cathode-coupling multivibrator, is active at the moments of

voltage $u_{упр}$ and $u_{оп}$ equality and circuit reversal occurs (negative feedback at moments of reversal, just as was the case in cathode-coupling multivibrators, is not active). It is important to note that capacitor C connecting triode L_1 plate with triode L_2 grid is required only to create a positive feedback loop but, in opposition to multivibrator circuits, is not a timing element. Actually, only an external cause -- the time interval during which one input voltage is greater than the other -- determines how long the circuit remains in each of the two fixed states.

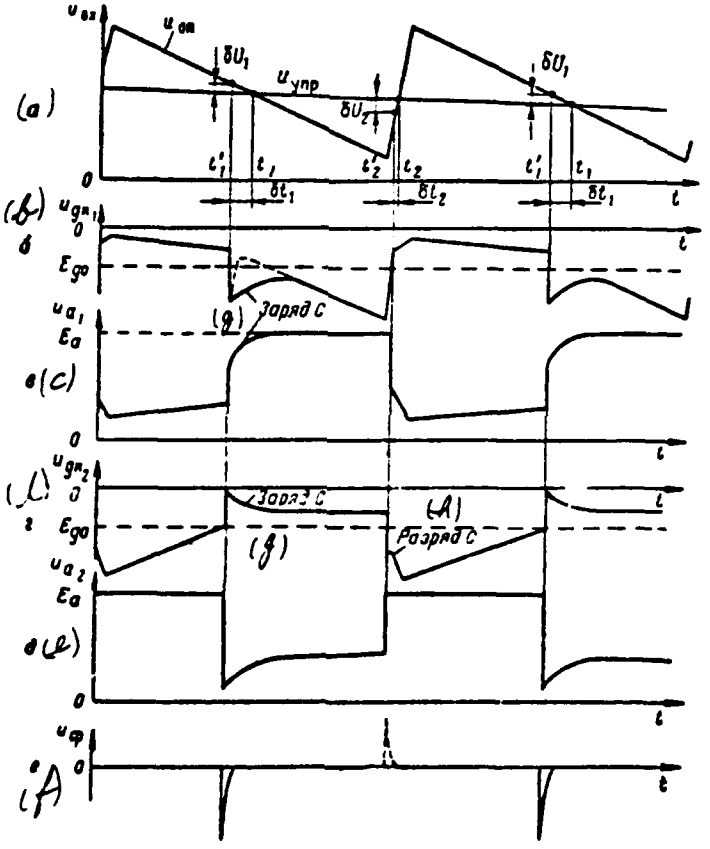


Figure VI.35. Voltage Curves in a Level Comparison Circuit.
(g) -- Charge; (h) -- Discharge.

Voltage curves in the circuit are depicted in Figure VI.35. The form of these curves is explained in the following manner.

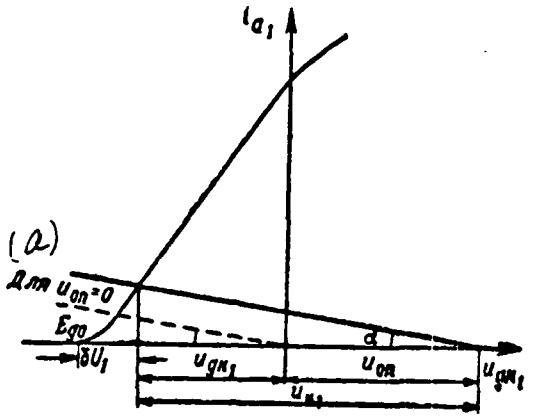


Figure VI.36. Graphic Explanation of Triode L_1 Operating Mode.
(a) -- For.

Triode L_1 is unblanked at the beginning of a forward stroke of a sawtooth voltage, as long as inequality $u_{on} > u_{ynp}$ $(t < t_1)$ is satisfied. We may examine its mode with the aid of Figure VI.36 where the dynamic plate-grid characteristic /280 (considering resistances R_k and R_{a1}) and the feedback line for a given instantaneous voltage u_{on} value are plotted: $i_{a1} = \frac{u_{on} - u_{g1}}{R_k}$ *. This line's point of intersection with the dynamic characteristic determines voltage u_{g1} and equals

$$u_{g1} = u_{on} - u_{k1} = E_{g0} + \delta U_1.$$

Load line slope, in accordance with (III.67) equalling $\alpha = \operatorname{arctg} \frac{1}{R_k}$, is slight due to the great resistance R_k magnitude. Therefore, voltage u_{g1} turns out negative for all values of u_{on} (the stage operates with grid currents), but

*This plot is analogous to that used for graphical analysis of cathode follower operation (see Figure III.23, Exercise III.9).

is greater than cutoff voltage E_{g0} since $u_{on}>0$. Voltage u_{gk1} decreases slightly due to the decrease of voltage u_{on} in accordance with the linear law, while voltage u_{a1} rises. In accordance with the same law and essentially with the same rate of change as that of voltage u_{on} , the voltage drop

$$u_{a1} = u_{on} - u_{gk1} = u_{on} - E_{g0} - \delta U_1.$$

Triode L_2 grid voltage equals

$$u_{gk2} = u_{ynp} - u_{k1} = u_{ynp} - u_{on} + E_{g0} + \delta U_1 \qquad \text{(VI.76)}$$

and rises according to the same law since $u_{ynp} \approx \text{const}$. Here, as follows from (VI.76), since $u_{on} > u_{ynp} + \delta U_1$, $u_{gk2} < E_{g0}$, i. e., triode L_2 is blanked*, and /281 its plate voltage is maximum $U_{a2} = E_a$.

Equality of voltages $u_{on} = u_{ynp}$ arrives at moment t_1. However, in accordance with (VI.76), voltage u_{gk2} rises to cutoff voltage somewhat earlier, at moment t_1', when reference voltage decreases to a magnitude exceeding voltage u_{ynp} by value δU_1: $u_{gk2} = E_{g0}$ where $u_{on} = u_{ynp} + \delta U_1$. At that moment, triode L_2 unblanks and the positive feedback network begins to operate: appearance of current i_{a2} increases voltage drop u_k , i. e., decreases voltage u_{gk1} and current i_{a1}, voltage u_{a1} rises, its increment is transmitted across coupling capacitor C to triode L_2 grid, causing a further current i_{a2} increase, and so on. Continuing voltage u_{on} decrease facilitates this process. As a result, an avalanche-like circuit reversal occurs at moment t_1': triode L_1 is blanked, while triode L_2 is unblanked.** Here, voltages u_{gk1} and u_{a2} decrease with a jump, while voltages u_{gk2} and u_{a1} rise with a jump. Voltage u_{gk2} when triode L_2 is unblanked remains negative due to the large resistance R_k magnitude (triode L_2, just like triode L_1, operates without grid currents).

It is clear from what has been said that voltage comparison occurs with time error $\delta t_1 = t_1 - t_1'$, which depends on voltage δU_1 magnitude. Resistance R_k must be increased in order to decrease this error, as is evident from Figure VI.36.

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*We assume that triode cutoff voltages are identical: $E_{go1} = E_{go2} = E_{go}$.

**Strictly speaking, circuit reversal will occur somewhat later, when voltage u_{gk2} exceeds cutoff voltage by a certain magnitude.

Capacitor C begins to charge along the network $+E_a$, resistance R_{a1}, capacitor C, resistance R_{g2}, voltage u_{ynp} source output resistance, chassis $(-E_a)$ in connection with the voltage u_{a1} increase at the moment of reversal. Charging current i_3, flowing across resistance R_{g2}, increases triode L_2 grid potential, which facilitates circuit reversal. Since this current, because of capacitor C charging, decays by the law of exponents, an exponential voltage u_{gk2} "bump" arises at triode L_2 grid, creating an identical current i_{a2} and voltage $u_{k2}=i_{a2}R_k$ "bump." But, since its grid voltage when triode L_1 is blanked equals $u_{gk1}=u_{on}-u_{k2}$, then an exponential voltage "bump" of opposite (negative) polarity arises in its grid.

If the capacitor C charge occurs too rapidly following a reversal, then the negative voltage u_{gk1} "bump" would cease until dropping voltage u_{on} becomes less than voltage u_{ynp} to the extent insuring reliable triode L_1 blanking (see the Figure VI.35b dotted line). Here, a random positive fluctuation of voltage u_{on} (or negative fluctuation of voltage u_{ynp}) arising immediately after moment t_1', may cause /282 a circuit counter misoperation. After this, the circuit again would reverse in the requisite direction in connection with the continuing reference voltage decrease. A sufficiently-large resistance R_{g2} is selected (on the order of a megohm) in order to extend the capacitor C charging process, i. e., the duration of the negative voltage u_{gk1} "bump," for a time during which voltage u_{on} will become significantly less than voltage u_{ynp} in order to eliminate the possibility of circuit misoperations. This guarantees a reliable single circuit reversal at moment t_1'.

Triode L_2 remains unblanked and triode L_1 blanked following a reversal until inequality $u_{on}<u_{ynp}$ $(t_1<t<t_2)$ is satisfied. During this entire time, current i_{a2} flows across resistance R_k and voltage $u_k=u_{k2}=i_{a2}R_k$ changes in phase with this current. Triode L_2 grid voltage, remaining negative, equals

$$u_{gk2}=u_{ynp}-u_{k2}>E_{g0}$$

and essentially is constant, eliminating the area of transient process immediately following reversal since voltage $u_{ynp}=\text{const}$. Voltage u_{a2} changes opposite in phase with voltage u_{gk2}. Triode L_1 grid voltage equals

$$u_{gk1}=u_{on}-u_{k2}<E_{g0}$$

and, since $u_{a2} \approx \text{const}$, changes in a manner almost identical to the voltage change. Here, voltage u_{a1} is maximum u_{on}.

Equality $u_{on} = u_{ynp}$ arrives at moment t_2 during the reference voltage return stroke. However, just as was the case for a forward circuit reversal, its counter reversal occurs somewhat earlier, at moment t_2', when equality $u_{on} + \delta U_2 = u_{ynp}$ is satisfied. Time error $\delta t_2 = t_2' - t_2$ is slight ($\delta t_2 \ll \delta t_1$) and has no significance due to the high rate of voltage u_{on} rise during the return stroke since a circuit counter reversal is not used further.

Triode L_1 is unblanked during a counter reversal and capacitor C discharges across this triode, resistance R_a, voltage u_{ynp} source output resistance, and resistance R_{g2}. Capacitor discharging current creates a negative voltage u_{ga2} "bump." It is desireable to clip this "bump" since, on the one hand, the danger of circuit misoperations during a counter reversal does not arise in connection with the great rate of voltage u_{on} rise and, on the other hand, there is a need to insure rapid circuit recovery prior to initiation of the subsequent forward stroke of this voltage (to prepare the circuit for the subsequent forward reversal). Therefore, diode D shunts resistance R_{g2} for capacitor C discharging current. This sharply decreases the capacitor discharge time constant, i. e., reduces /283 the recovery time of triode L_2 grid normal potential.

Circuit output voltage is picked off triode L_2 plate and then is differentiated (see Figure VI.33a). Comparison pulses of negative polarity, whose position (with error δt_1) corresponds to the moments of voltage u_{on} and u_{ynp} equality during each voltage u_{on} forward stroke (Figure VI.35f), are the result. Positive pulses obtained at differentiator output at moment t_2' are not used (depicted by the dotted line in Figure VI.35f).

As already indicated, it is advantageous to increase resistance R_a to decrease comparison error δt_1. Large resistance R_a also facilitates tube plate current stabilization, i. e., insures voltage u_{a2} drop amplitude constancy and, consequently, that of comparison pulses, given varied voltage u_{ynp} levels. Therefore, a resistance R_a on the order of unities of megohms is selected. However, here, resultant voltage u_{a2} drop amplitude is slight due to the tube plate current decrease and satisfaction of the amplitude self-excitation condition is hindered due to the

decrease in dynamic plate-grid characteristic transconductance. Resistance R_k often is connected to the cathode bias E_k ($E_k \approx E_c$) source negative terminal rather than to the circuit chassis to increase tube plate current and dynamic characteristic transconductance. Connection of a current-stabilizing triode or pentode with negative current feedback to the tube cathode network rather than resistance R_k is a more efficient approach (see Chapter III, § 4).

EXERCISE VI.13

a) In what instances and how does a diode D malfunction impact upon the operation of a level comparison circuit (Figure VI.34)?

b) How should the Figure VI.34 circuit be changed if sawtooth reference voltage is rising linearly (during the time of a forward stroke), rather than dropping linearly? (Page 485)

§ 6. TRANSISTOR FLIP-FLOPS

1. External Bias Source Flip-Flop

Transistor flip-flops are analogous to corresponding tube flip-flops and are two-stage amplifiers with a closed positive feedback loop. Transistors are assembled in a common-emitter [OE] circuit in amplifying stages. Here, such OE circuit advantages, compared to a common-base [OB] circuit, as large input resistances and sufficiently-high current and voltage amplification are employed in this transistor circuit arrangement. In addition, inversion of the amplifying signal occurs in an OE circuit and is required to satisfy self-excitation phase /284 conditions during the regenerative process.

The keying mode of operation, i. e., one transistor is in a state of saturation, while the other is in a blanked state, is used in the transistor flip-flop static mode. Providing blanking and saturation modes with a slight reserve, it is possible to obtain good circuit and pulse amplitude stability during a temperature change or when transistors are replaced. In addition, a high supply source utilization factor is insured in the keying mode.

One keying mode drawback is that the saturation mode will lead to a reduction in operating speed due to dispersal delay and a decrease in triggering sensitivity.

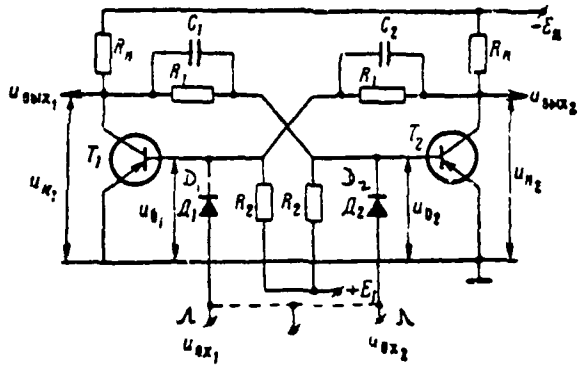

Figure VI.37. External Bias Source Transistor Flip-Flop.

The external bias source symmetrical flip-flop circuit depicted in Figure VI.37 in layout is analogous to an electron tube circuit. We will analyze this circuit for two states, the static mode and the switching process under trigger pulse action.

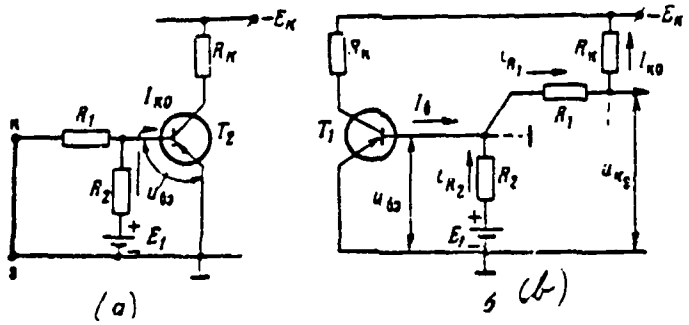

Figure VI.38. For Analysis of the Flip-Flop Static Mode.

Static mode. In the static mode, one transistor is blanked, while the other is unblanked and in the saturation mode. We will assume that transistor T_1 is unblanked, while transistor T_2 is blanked. The condition of transistor T_2 blanking may be determined from the equivalent circuit depicted in Figure VI.38a. Here,

saturated transistor T_1 is replaced by a short-circuited conductor (points K and Э in Figure VI.38a) since the potential of its collector approximates zero. Positive bias source E_1, whose voltage magnitude must exceed the voltage drop across resistance R_2 due to current $I_{к0}$ flow insures transistor T_2 blanking.

It is evident from the circuit (VI.38a) that /285

$$u_{бэ} = \frac{R_1}{R_1 + R_2}(E_1 - I_{к0}R_2). \qquad \text{(VI.77)}$$

Since inequality $u_{бэ}>0$ determines the blanking condition, one may write

$$R_2 < \frac{E_1}{I_{к0}}. \qquad \text{(VI.78)}$$

The maximum value of collector junction back current $I_{к0\,макс}$ (given the upper temperature value) must be substituted in inequality (VI.78) for reliable blanking in the temperature interval. It then is possible to transfer from inequality (VI.78) to equality

$$R_2 = \frac{E_1}{I_{к0\,макс}}. \qquad \text{(VI.79)}$$

The transistor T_1 saturation condition is written in the form

$$I_б \geqslant \frac{I_{кн}}{\beta} = \frac{E_к}{\beta R_к}.$$

Considering unblanked transistor T_1 voltage $u_{бэ}$ in the saturation mode as equalling zero, it is possible to find the expression for this transistor's base current in accordance with the Figure VI.38b equivalent circuit:

$$I_б = i_{R1} - i_{R2} = \frac{E_к - I_{к0}R_к}{R_1 + R_к} - \frac{E_1}{R_2} \approx \frac{E_к}{R_1 + R_к} - \frac{E_1}{R}, \qquad \text{(VI.80)}$$

since ratio $I_{к0}R_к \ll E_к$ usually is provided by the $R_к$ magnitude selected. Considering expression (VI.80), the saturation condition may be written in the form

$$I_б = \frac{E_к}{R_1 + R_к} - \frac{E_1}{R_2} \geqslant \frac{E_к}{\beta R_к}. \qquad \text{(VI.81)}$$

Hence /286

$$R_1 < \left(\frac{\beta}{1+\beta\frac{ER_к}{E_к R_1}} - 1\right) R_к. \qquad \text{(VI.82)}$$

Variation β is great in manufactured transistors since value α usually is controlled during manufacture. Even a slight α deviation from the assigned value will lead to a material difference in β magnitudes. Thus, for example, transistors in which $\alpha_1 = 0.98$ and $\alpha_2 = 0.99$ will have $\beta_1 \approx 50$ and $\beta_2 \approx 100$. Therefore, there is a requirement to insure satisfaction of inequality (VI.82) for an unfavorable value $\beta = \beta_{мин}$. It then is possible to transfer from inequality (VI.82) to equality

$$R_1 = \left(\frac{\beta_{мин}}{1+\beta_{мин}\frac{ER_к}{E_к R_1}} - 1\right) R_к \qquad \text{(VI.83)}$$

or, considering (VI.79)

$$R_1 = \left(\frac{\beta_{мин}}{1+\beta_{мин}\frac{I_{к1\,макс}}{I_{кн}}} - 1\right) R_к. \qquad \text{(VI.84)}$$

Ratios (VI.79) and (VI.84) make it possible to compute divider R_1, R_2 so that, for given supply sources $E_к$ and E_1 and resistance $R_к$, the flip-flop circuit will have a state of stable equilibrium with sufficient reserve. These ratios are introduced for cases where transistor T_1 is unblanked, while transistor T_2 is blanked. By virtue of circuit symmetry, these same ratios are also the conditions for the circuit's second stable state.

The difference in collector potentials in the blanked $U_{к\,макс}$ and in the unblanked $U_{к\,мин}$ states determines output pulse amplitude. It is evident from Figure VI.38b that $U'_{к\,макс} = \frac{(E_к - I_{к0}R_к)R_1}{R_1 + R_к}$. In the unblanked state $U_{к\,мин} \approx 0$. Thus, output pulse amplitude equals

$$U'_к = (E_к - I_{к0}R_к)\frac{R_1}{R_1 + R_к}. \qquad \text{(VI.85)}$$

EXERCISE VI.14

How does magnitude β impact upon pulse amplitude, given assigned circuit temperature stability? (Page 486)

Transient processes. Just as was the case for electron tube flip-flops, the individual method of trigger pulse supply or symmetrical ("counting") triggering, in which pulses of identical polarity are supplied across trigger diodes D_1 and D_2 to the input of both transistors, may be used to trigger transistor flip-flops. A counting trigger network is depicted by the dotted line in Figure VI.37.

The circuit is triggered in the majority of cases by pulses of positive /287 polarity (negative-polarity pulses for npn transistors), which act upon an unblanked and saturated transistor and make it possible to speed up carrier clean-out in the collector junction region.

Let a positive pulse be supplied to the base of unblanked transistor T_1. The process of excess carrier clean-out at the transistor T_1 collector junction begins due to positive voltage action and, after a certain time t_1 (Figure VI.39), the operating point will turn out to be in the active region. Collector current i_{k1} will begin to decrease from that moment on. Consequently, negative voltage u_{k1} will rise. Negative increments $-\Delta u_{k1}$ are transmitted across capacitor C_1 to transistor T_2 base, decreasing positive bias. Base voltage u_{b2} at moment t_2 will equal zero and transistor T_2 will unblank. Appearance of current i_{k2} /288 causes transistor T_2 collector voltage to increase. This, in turn, will lead to a transistor T_1 base voltage increase, causing its further blanking. As a result, the positive feedback network turns out to be closed and a regenerative process occurs in the circuit if the self-excitation condition is satisfied. The regenerative process condition may be expressed by inequality

$$\frac{\beta R_k}{R + R_k} > 1. \qquad \text{(VI.86)}$$

which is satisfied automatically if the flip-flop is computed correctly in the static mode.

Reversal time t_{rev} determined by transistor inertness equals τ_1 in the first

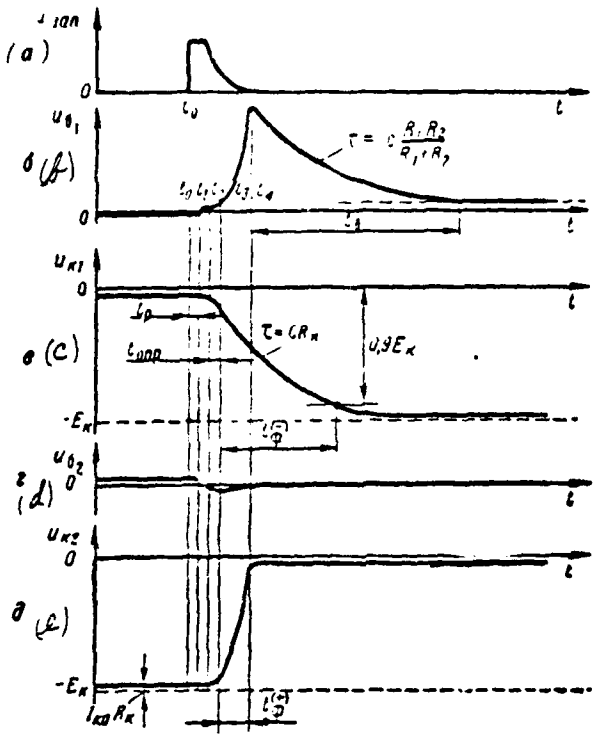

Figure VI.39. Transient Processes in a Flip-Flop.

approximation. The influence of transistor collector capacitances $C_к$ on the process rate is insignificant since charging of these capacitances occurs across relatively-slight resistances $R_к$.

Collector voltages and capacitor C_1 and C_2 voltages change slightly during the time of the regenerative process. The process of circuit recovery in the new stable state, when transistor T_2 is unblanked and transistor T_1 is blanked, begins from moment t_3. Here, capacitor C_1 is charged by base current $i_{б2}$ through the network $+E_к$, T_2 emitter-base, C_1, $R_к$, $-E_к$.

We will note that, given slight time $t_{опр}$ and sufficiently-large capacitor C_1 and C_2 capacitance magnitude, current $\Delta i_{б2}$ changes will equal collector current $\Delta i_{к1}$ changes and, accordingly, $\Delta i_{б1} = \Delta i_{к2}$. At moment t_3 when the regenerative

process ceases, transistor T_2 base current will have magnitude

$$i_{б2}(t_з) = I_{бm} \simeq \frac{E_к - |U_{б0}|}{R_к} \approx I_{кн}, \qquad \text{(VI.87)}$$

since unblanked transistor base voltage $U_{б2} \approx 0$. Further, base current decreases by the law of exponents

$$i_б(t) = I_{бm} e^{-\frac{t}{\tau_{зар}}}. \qquad \text{(VI.88)}$$

Disregarding the shunting action of resistances R_1 and R_2 ($R_1 \gg R_к$ и $R_2 \gg r_{эб}$), the capacitor C_1 charging time constant equals $\tau_{зар} = C_1 R_к$.

A rapid increase in transistor T_2 collector voltage occurs as a result of the flow of relatively-large base current $I_{бm}$ and positive porch $t_ф^+$ is shaped (Figure VI.39e). If current $i_{б2}$ does not change and remains equal to $I_{бm}$, then porch shaping will occur as in the usual switch (Figure VI.37c) and porch duration $t_ф^{(+)}$, in accordance with (V.19), may be determined:

$$t_ф^{(+)} = \tau_з \frac{I_{кн}}{\beta I_{бm}} \approx \tau_к. \qquad \text{(VI.89)}$$

In fact, base current decreases and, therefore, porch duration is /289 stretched somewhat, while saturation will occur somewhat later than when base current is constant.

Transistor T_1 collector voltage equals capacitor C_1 voltage since $U_{б2} \approx 0$.

Therefore, the law of voltage $u_{к1}$ change has an exponential relationship

$$u_{к1}(t) = E_к - (E_к - U_{б0}) e^{-\frac{t}{\tau_{зар}}}, \qquad \text{(VI.90)}$$

where $U_{б0}$ -- unblanked transistor base voltage.

Determining porch duration $t_\phi^{(-)}$ (Figure VI.39c) when voltage u_{K1} achieves level $0.9E_K$, we will get

$$t_\phi^{(-)} = \tau_{разр} \ln \frac{E_K - |U_{\omega}|}{0.1E_K}.$$

Since usually $|U_{\omega}| \ll E_K$, then

$$t_\phi^{(-)} \simeq C_1 R_K \ln 10 \approx 2.3 C_1 R_K. \qquad \text{(VI.91)}$$

Following reversal, capacitor C_2 discharges along two parallel networks: across resistance R_2 and unblanked transistor T_2 and across resistance R_1. Disregarding the slight unblanked transistor resistance, it is possible to express the discharging time constant by formula

$$\tau_{разр} = C_2 \frac{R_1 R_2}{R_1 + R_2}. \qquad \text{(VI.92)}$$

Since usually $\frac{R_1 R_2}{R_1 + R_2} > R_K$, while $C_1 = C_2$, then capacitance discharge determines flip-flop recovery time and has magnitude

$$t_в = (3 \div 5) C \frac{R_1 R_2}{R_1 + R_2}. \qquad \text{(VI.93)}$$

It is desirable to decrease capacitance magnitude for given resistance magnitudes in order to decrease recovery time and reduce porch $t_\phi^{(-)}$. However, unblanking transistor (transistor T_2 in our case) input current magnitude is clipped when capacitance magnitude is slight due to large resistance R_1. This will lead to porch $t_\phi^{(-)}$ deterioration. The reasons for such a phenomenon were examined in Chapter V, § 4. Thus, contradictory requirements are levied on accelerating capacitance magnitude. Optimal capacitance value is determined by formula

$$C = \frac{0.3}{f_в R_в}.$$

Transistors with the greatest frequency limit (such as P411 and P416 /290 transistors, for example) need to be used to reduce transient process time and to increase flip-flop speed. Also, the degree of saturation must be reduced where possible. An increase in trigger current amplitude is useful to decrease clean-out

time if circuit operating conditions require that a saturation mode with sufficient reserve be provided.

It also is possible to reduce transient processes if collector voltage diode clamping is used, as was demonstrated in Chapter V, § 4 (Figure V.38).

Low-frequency transistors like the P15, P16B, P26B, P26B, P30, P42, and so forth provide a switching frequency on the order of hundreds of hertz. High-frequency transistors like the P403, P410, P411, and P416 make it possible to increase switching frequency to several hundred megahertz [13].

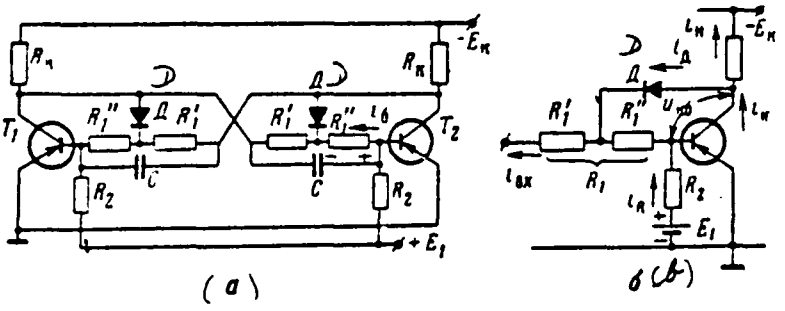

Figure VI.40. Unsaturated Flip-Flop Circuit (a) and Simplified Circuit for One Arm (b).

Unsaturated flip-flop circuits often are used instead of the circuits examined, called a saturated flip-flop circuit. The unsaturated mode makes it possible to eliminate the flip-flop reversal delay due to carrier clean-out. Introduction of nonlinear negative feedback into the circuit is a widespread method of averting unblanked transistor saturation. An unsaturated flip-flop circuit and a simplified circuit for one arm are depicted in Figure VI.40a, b, respectively. Here, nonlinear negative feedback between collector and base is accomplished by diode D, which closes the feedback when the transistor operating point approaches the saturation region and opens it the moment the transistor blanks. A small portion of common resistance R_1, designated R_1'', is connected in series with it to provide the requisite level of diode unblanking. As long as collector-base path voltage $U_{бк}$ is greater than the voltage drop across resistance R_1'', due to divider i_R and base $i_б$ currents, diode D is blanked and negative feedback is inactive. Therefore, base /291

current $i_б$ will rise with a rise in input current $i_{вх} = i_К - i_б$ and, consequently, collector current $i_К = \beta i_б$ rises also. Diode D unblanks, preventing transistor saturation, when output current reaches that value at which voltage $U_{R_К}$ will equal the voltage drop across resistance R_1''. Here, a further input current increase will lead mainly to an increase in the component of collector current flowing across the diode, while load current $i_н$ will remain essentially unchanged. Collector current is clamped close to the saturation boundary.

EXERCISE VI.15

How will pulse $U_{вх}$ rise and decay time change when capacitances C_1 and C_2 change? (Page 486)

2. Automatic Bias Flip-Flop

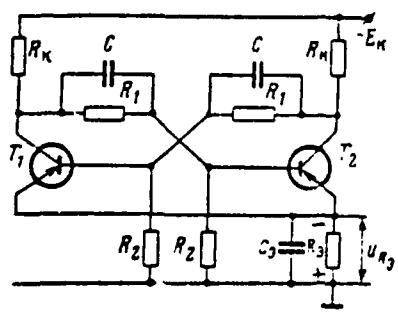

Figure VI.41. Automatic Bias Flip-Flop.

An automatic bias flip-flop circuit is depicted in Figure VI.41. Bias in this circuit is created by the voltage drop across resistance $R_э$ as unblanked transistor emitter current flows. The unblanking condition of the other transistor is identical to that of an external bias source flip-flop circuit. Consequently, it is possible to determine resistance R_2 from formula

$$R_2 = \frac{U_{R_э}}{I_{к0\ макс}} \qquad (VI.94)$$

Resistance R_3 magnitude is selected from the condition of one transistor's reliable blanking while the other is in the unblanked state, on the one hand, and providing maximum output pulse amplitude on the other. It is advisible to select the greatest possible resistance R_3 magnitude for reliable blanking. But, when a transistor is in the unblanked and saturated state, its collector voltage differs from zero and is approximately equal to voltage U_{R_3}. This will lead to a decrease in the voltage drop across the collector when the examined transistor is blanked. A resistance R_3 magnitude on the order of $(0.1 \div 0.2) R_к$ usually is selected.

EXERCISE VI.16 /292

Prove an approximate formula for determination of voltage U_{R_3} using circuit parameters, considering that the unblanked transistor is saturated. (Page 486)

Output voltage amplitude equals

$$U_м \simeq E_к \frac{R_1}{R_1 + R_к} \cdot \frac{R_к}{R_к + R_3}. \qquad \text{(VI.95)}$$

Amplitude here turns out to be 10--15% less compared with an external bias flip-flop.

Capacitor C_3 capacitance magnitude is selected from the condition of resistance R_3 shunting during the reversal process, i. e., a-c component shunting. Here, condition $R_3C_3 \geqslant t_{об}$ must be satisfied, where $t_{об}$ -- reversal process duration.

Main drawbacks of this flip-flop include more components and less output pulse amplitude, given identical supply source $E_к$, compared with the previously-examined circuit. However, negative d-c feedback, which stabilizes the operating point in case the transistor unsaturated mode is used, is created in an automatic bias flip-flop due to resistance R_3. In turn, the unsaturated mode makes it possible to rule out delay due to clean-out, i. e., to increase speed.

3. Emitter-Coupling Flip-Flop

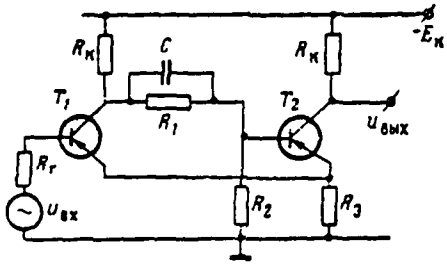

Figure VI.42. Emitter-Coupling Flip-Flop.

The emitter-coupling flip-flop circuit depicted in Figure VI.42 is another flip-flop circuit variant. A special feature of this flip-flop is that resistances and a boosting capacitance do not couple the transistor T_2 collector to the transistor T_1 base. Therefore, a much better output pulse shape results. The emitter- coupling flip-flop is used widely as a converter of sinusoidal voltage (or of any random-shape voltage) into square pulses and also may be used as a pulse-height discriminator. In this case, a regenerative process occurs when input voltage attains the tripping threshold and the pulse obtained as a result of transistor T_2 collector /293 voltage drop differentiation becomes the information on the assigned input signal level.

Pulses of alternating polarity must be used when triggering a flip-flop with pulses supplied to the transistor T_1 base.

The amplitude of the pulses at the transistor t_2 collector essentially equals

$$U_м \approx E_к \left(1 - \frac{R_э}{R_э + R_к}\right). \qquad \text{(VI.96)}$$

§ 7. TRANSISTOR MULTIVIBRATORS

1. Transistor Multivibrator in the Free-Running Mode

Transistor multivibrators in design are analogous to tube circuits. Electrical

processes flowing in these circuits as a pulse tilt is shaped also are analogous to those in tube circuits and are linked with timing capacitance recharge. The only difference here is that the blanked transistor exerts shunting action on the recharging circuit and, most importantly, a relationship exists between shunting activity and temperature. In particular, input network shunting of recharging R-C network blanked transistors in multivibrators will lead to a change in pulse duration or resting time with a temperature change. Processes linked with porch and droop shaping differ materially from those in tube circuits. This is exolained by transistor inertness due to the finite rate of diffusion of carriers and clean-out delays examined above. Stray and junction capacitances play a lesser role than transistor inertness since their recharging occurs across relatively-slight collector network resistances.

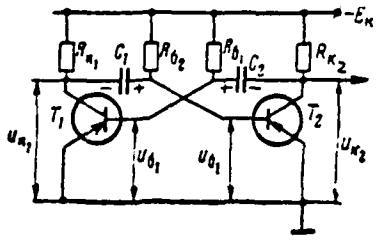

Figure VI.43. Transistor Mulitivibrator Circuit.

The circuit for a multivibrator operating in the free-running mode is depicted in Figure VI.43 and is analogous to a retarding-field multivibrator. In this case, coupling network resistances are connected to supply source $E_к$ negative terminal. As a result of this type of connection, capacitor C_1 and C_2 resistances $R_{к1}$ and $R_{к2}$ will have a tendency to recharge when transistors T_1 and T_2 /294 are in the unblanked state. It is advisible to connect the aforementioned resistances to source positive terminal since base voltage when the capacitor discharges will strive towards zero, while transistor unblanking occurs when the voltage between base and emitter is close to zero, i. e., the moment of reversal will be unstable.

Time diagrams explaining circuit operation are depicted in Figure VI.44. Here, we accept as our zero time reference random moment in time when transistor T_2 is unblanked and is saturated, while transistor T_1 is blanked by capacitor

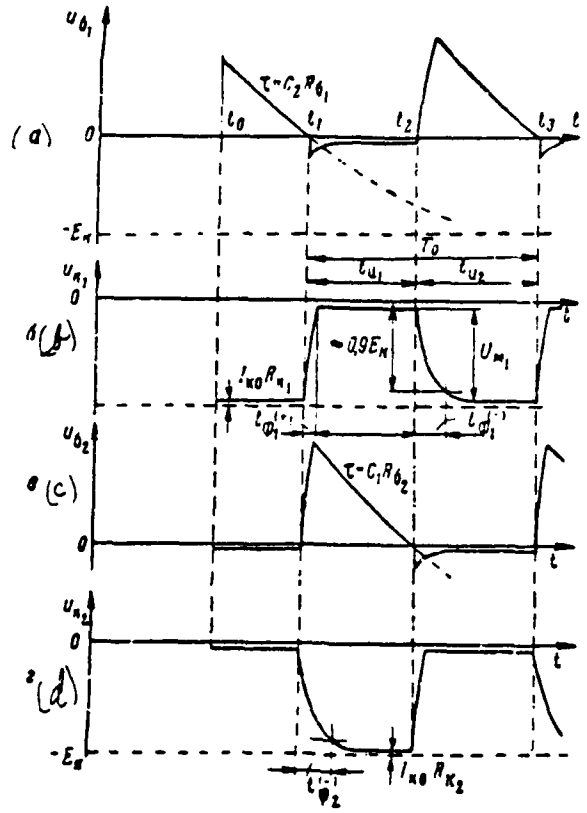

Figure VI.44. Time Diagrams Illustrating Multivibrator Operation.

C_2 positive voltage. In actuality, saturated transistor T_2 represents a /295 short circuit, resulting in capacitor C_2 being connected between transistor T_1 base and emitter. Capacitor C_2 discharges across unblanked transistor T_2, resistance $R_{к1}$, and supply source $E_к$. If you disregard unblanked transistor internal resistance and blanked transistor shunting action, then the recharging network time constant will turn out to equal

$$\tau_{разр} = R_{к1} C_2 \qquad \text{(VI.97)}$$

Circuit reversal will occur at certain moment t_1 when transistor T_1 base voltage reaches a level approximately equal to zero ($u_{б1} \approx U_{C2} \approx 0$) and the transistor will unblank. Appearance of collector current $i_{к1}$ will lead to an increase in

collector voltage $u_{к1}$ (its negative potential decreases), which causes capacitance C_1 discharge. The main portion of collector current $i_{к1}$ initially will flow across capacitor C_1 and across transistor T_2 input resistance. The excess discharge in the T_2 base disperses as a result and transistor T_2 leaves the saturation mode. Collector current $i_{к2}$ begins to decrease and transistor T_2 collector voltage begins to drop. In this connection, capacitor C_2 discharging current increases and, consequently, transistor T_1 base current increases. Thus, from this moment on, the positive feedback network turns out to be closed and a regenerative process, which concludes with the blanking of transistor T_2, occurs in the circuit. Just as was the case in the flip-flop, transistor collector and base voltages do not reach the steady-state value immediately. Positive porch $t_{\phi 1}^{(+)}$ shaping in the transistor T_1 collector is similar to porch $t_{\psi}^{(+)}$ shaping in a flip-flop (Figure VI.39e).

There is no rise in voltage $u_{к1}$ prior to transistor T_2 blanking due to load shunting $R_{к1}$ by slight resistance $r_{б2}$ (across capacitor C_1). Transistor T_1 collector voltage will begin to increase intensively only from the moment transistor T_1 is blanked. Given sufficiently-great capacitor C_2 capacitance, the voltage in it during regeneration essentially will not suceed in changing and therefore $\Delta i_{б1} = \Delta i_{к2} \approx \frac{E_к}{R_{к2}} = I_{кн2}$. Then, capacitor C_2 begins to charge through network

$+E_к$, $r_{эб1}$, C_2, $R_{к2}$, $-E_к$.

Charging time constant $\tau_{зар} \approx C_2 R_к$ usually is greater than time constant τ_1. Therefore, porch shaping occurs just as was the case for a conventional switch, given essentially unchanged turn-on current $i_{б1} = I_{кн2}$. Consequently, it is possible to determine rise time $t_{\phi 1}^{(+)}$ from (V.19), i. e.

$$t_{\phi 1}^{(+)} = \tau_3 \frac{I_{кн1}}{\beta I_{кн2}} \approx \tau_3 \frac{\frac{E_к}{R_{к1}}}{\beta \frac{E_к}{R_{к2}}} = \tau_3 \frac{R_{к2}}{\beta R_{к1}}. \qquad \text{(VI.98)}$$

Negative rise (decay) time $t_{\psi 2}^{(-)}$ in the transistor T_2 collector is linked with restoration of the charge in capacitor C_2 and is computed in the standard way: /296

$$t_{\phi 2}^{(-)} = 2{,}3 C_2 R_{к2}. \qquad \text{(VI.99)}$$

During time interval t_1--t_2, transistor T_1 is maintained in the blanked state due to capacitor C_1 voltage. A new multivibrator reversal occurs when voltage $u_{б1}$ reaches zero (moment t_2). Rise times $t_{ф1}$ and $t_{ф2}$ are determined from formulas (VI.98) and (VI.99), in which resistance and capacitor indices must be changed.

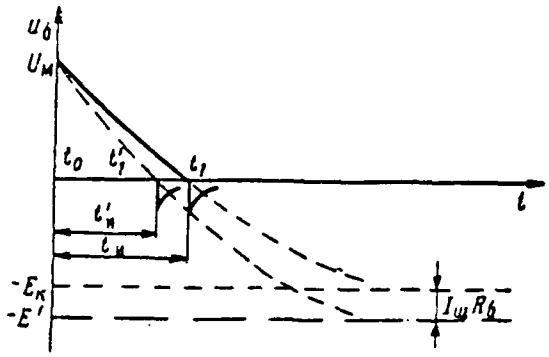

Figure VI.45. For Determination of Shaped Pulse Duration.

We will use Figure VI.45, which depicts the nature of the change in transistor base blanking voltage between two reversal moments t_0 and $t_1 = t_м$, for approximate determination of generated pulse duration $t_м$ and repetition period T.

The following designations are used here:

$U_м$ -- blanked transistor initial base voltage;

E -- voltage level to which the exponential curve will strive;

$t_м$ -- pulse duration determined by time of blanked transistor state.

Base voltage during the time interval being examined changes by the law of exponents:

$$u_б = -E + (U_м + E)e^{-\frac{t}{\tau}}, \qquad \text{(VI.100)}$$

where τ -- timing capacitance recharge time constant.

In accordance with (VI.100), pulse duration where $u_б \approx 0$ is determined /297

$$t_и = \tau \ln\left(1 + \frac{U_и}{E}\right). \qquad \text{(VI.101)}$$

The time constant in the multivibrator circuit being examined is determined from (VI.97) if you do not consider the shunting action of the blanked transistor, while the voltage level to which the exponential curve will strive equals $E_к$. Considering that $U_и = U_{C\,макс} \approx E_к$*, we get the pulse duration formula

$$t_и = \tau \ln 2 \approx 0{,}7\tau = 0{,}7R_б C. \qquad \text{(VI.102)}$$

Pulse repetition frequency in a symmetrical multivibrator equals

$$T_0 = 2t_и = 1{,}4R_б C, \qquad \text{(VI.103)}$$

and, in an asymmetrical multivibrator

$$T_0 = 0{,}7(R_{б1}C_2 + R_{б2}C_1). \qquad \text{(VI.104)}$$

These formulas are approximate and may have an error factor of 10% or more. And, they are not viable at all for increased temperatures. One must consider blanked transistor shunting by the input network in order to obtain more precise formulas.

We will examine the shunting action of the blanked transistor base network when the emitter-base junction characteristic approximates the theoretical, i.e., it corresponds to a blanked pn-junction characteristic. We will consider that shunting current $I_ш$ is constant in the entire pn-junction volt-ampere sector.

In this event, the blanked transistor input network is equivalent to an ideal current generator and the recharging network circuit will look like that depicted in Figure VI.46a. It is possible to reduce this circuit to one with an /298

*Such an assumption is justified given relatively large capacitance magnitudes (C_1 and C_2 exceeding 500--1,000 pF), when the charged capacitor does not succeed in discharging significantly while both transistors are in the unblanked state.

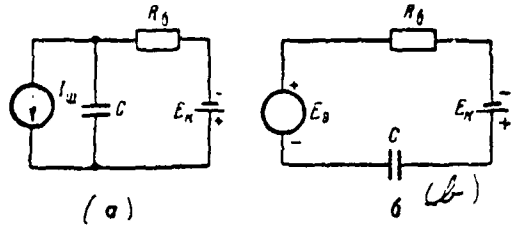

Figure VI.46. Capacitor Recharge Equivalent Circuit:
(a) -- With a current generator; (b) -- With a voltage generator.

equivalent generator $E_ш = I_ш R_0$ (Figure VI.46b). It follows from this that shunting will lead to a voltage increase in the recharging network to value

$$E' = E_к + I_ш R_0. \tag{VI.105}$$

This facilitates more rapid capacitor C recharge and pulse duration reduction. The exponential curve corresponding to the case under examination is depicted by the line of long dashes in Figure VI.45. Pulse duration considering shunting will equal

$$t'_и = R_0 C \ln\left(1 + \frac{U'_ш}{E_к + I_ш R_0}\right) \tag{VI.106}$$

Since $U'_ш \approx E_к$ in a multivibrator, then expression (VI.106) may be rewritten in the form

$$t'_и = R_0 C \ln\left(1 + \frac{1}{1 + \frac{R_0}{R_ш}}\right), \tag{VI.107}$$

where $R_ш = \frac{E_к}{I_ш}$ -- shunting resistance.

Ratio $\frac{R_0}{R_ш}$ sometimes is referred to in the literature [13] as the multiplying factor of a shunt. When the temperature increases, shunt current magnitude will rise, the multiplying factor of the shunt increases, and generated pulse duration decreases. It is clear that it is desirable to select resistance R_0 of the lowest

possible magnitude compared with $R_{вх}$ magnitude in order to decrease the shunting action in the circuit.

Resistance $R_{вх}$ magnitude in P13--P116 type germanium transistors at a temperature of +65° C will fall in the range of 0.3--0.8 megohms ($E_к = 10 \div 30$ V). Under identical conditions, resistance magnitude for P101--P1103 silicon transistors is $R_{вх} = (8 \div 70)$ megohms, while that of a P104 transistor is about 100 megohms.

EXERCISE VI.17

What constrains the threshold of a resistance $R_к$ decrease? (Page 486)

EXERCISE VI.18

The following is given for a symmetrical multivibrator: $R_{б1} = R_{б2} = 100$ kilohms; $C_1 = C_2 = 10{,}000$ pF; $E_к = 30$ V. Determine pulse duration $t_и$ relative change when temperature changes from +20 to +65° C if the following transistors are used in the circuit:

P14 ($I_{кб}$ = 10 uA at +20° C and $I_{кб}$ = 60 uA at +65° C);

P106 ($I_{кб}$ = 1.0 uA at +20° and $I_{кб}$ = 6.0 uA at +65° C).

Form a conclusion about the applicability of formulas (VI.102) and (VI.107) based on obtained results. (Page 486)

2. Monostable Transistor Multivibrators /299

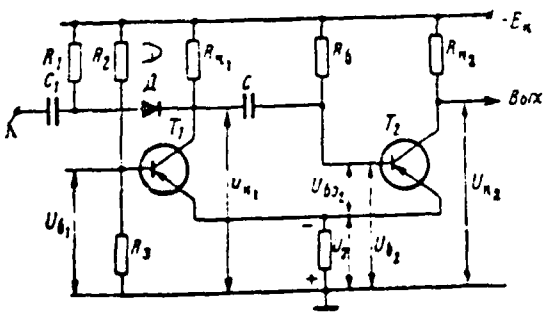

Figure VI.47. Emitter-Coupling Monostable Multivibrator.

The emitter-coupling monostable multivibrator (Figure VI.47) is the most-widespread trigger circuit variant. This circuit is analogous to a "positive"-grid and cathode-coupling tube multivibrator (Figure VI.19).

We will examine the somewhat-simplified operation of this circuit, considering that the processes of clean-out and regeneration are of negligible duration, and there is an instantaneous change of currents and voltages during reversal. We will evaluate rise time and factors impacting on their duration at the end of this section.

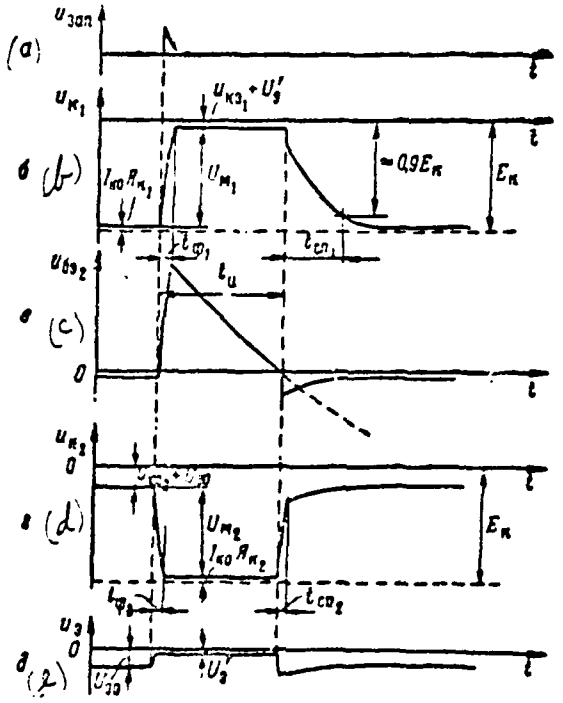

Figure VI.48. Time Diagrams Illustrating Monostable Multivibrator Operation.

Curves illustrating circuit operation are depicted in Figure VI.48.

Transistor T_2 is unblanked in the initial stable state due to negative voltage $E_к$ supplied to its base across resistance $R_б$. The transistor T_2 saturation mode is used for reliable operation. In this case, the voltage drop between

transistor T_2 electrodes is slight (transistor T_2 "is shrunk" to the point) and this transistor's currents are determined by ratios:

$$I_{к2} \approx \frac{E_к}{R_{к2} + R_э} \qquad \text{and} \qquad I_{б2} \approx \frac{E_к}{R_б + R_э}$$

The transistor T_2 condition, written in overall form $i_б \geqslant I_{бн} = \frac{I_{кн}}{\beta}$, may be expressed by circuit parameters

$$(R_{к2} + R_э)\beta \geqslant R_б + R_э. \tag{VI.108}$$

Considering that always $R_б \gg R_э$, expression (VI.108) has the form

$$(R_{к2} + R_э)\beta \geqslant R_б. \tag{VI.109}$$

Transistor T_2 emitter current creates a voltage drop across resistance /300 $R_э$

$$U'_{э0} = I_{э2}R_э = \frac{E_к R_э}{\frac{R_{к2}R_б}{R_{к2} + R_б} + R_э} \approx \frac{E_к R_э}{R_{к2} + R_э}, \tag{VI.110}$$

which is blanking current for transistor T_1.

Negative unblanking voltage from divider R_2, R_3 is supplied to transistor T_1 base.* The voltage divider must be computed so that transistor T_1 is blanked in the initial state, i. e., $|U'_{б1}| < |U'_{э0}|$. The following simple ratio expresses base potential

$$U'_{б1} = E_к \frac{R_3}{R_2 + R_3}, \tag{VI.111}$$

in which the voltage drop across divider resistances due to blanked transistor /301 T_1 current $I_{к}$. is not considered since a low-resistance (on the order of unities of kilohms) divider R_2--R_3 is selected for temperature stability.

It is possible to write the condition of transistor T_1 blanking in the initial state using circuit element magnitudes from ratios (VI.110) and (VI.111)

*We will examine the purpose of this divider below.

$$\frac{R_2}{R_3} > \frac{R_{k2}}{R_6}. \qquad \text{(VI.112)}$$

Capacitor C in the initial state is charged to voltage
$U_{C1} = E_a - U_{k0} - I_{k0}R_{k1} \approx E_a - U_{k0}$.

Both negative pulses supplied to the blanked transistor base network and positive pulses supplied to the unblanked transistor base network may trigger the circuit. Positive-polarity pulses may trigger the circuit being examined across trigger diode D. Diode D in the initial state is blanked since voltage $-E_a$ acts at its plate and $(-E_a + I_{k1}R_{k1})$ acts at its cathode.

Transistor T_1 collector potential increases upon trigger pulse arrival and this increase is transmitted across capacitor C to the unblanked transistor T_2 base. As a result, excessive carriers at the base are cleaned out and transistor T_2 converts to the active region. Current across transistor T_2 decreases, the voltage drop across resistance R_{k1} also decreases, and transistor T_1 unblanks. Onset of current i_{k1} will lead to an increase in potential u_{k1}. The rise of transistor T_1 collector voltage is transmitted across capacitor C to the transistor T_2 base, blanking it. The positive feedback network turns out to be closed and a reversal occurs in the circuit, as a result of which transistor T_2 blanks, while transistor T_1 unblanks.

Since transistor T_1 collector potential rises following reversal, then trigger diode D blanks, thus cutting the trigger network out of the multivibrator circuit.

It is desirable in the quasistable state reached to provide a transistor T_1 saturation region for the following reasons. First, a more rapid rise in collector voltage occurs when there is sufficiently-great input current i_{61} required to convert the transistor to saturation $(i_{61} > I_{6k1})$, i. e., pulse rise time is reduced. Second, when transistor T_1 is saturated, it is possible to obtain maximum pulse amplitude essentially independent of the transistor itself. Third, and finally, transistor T_1 does not impact upon capacitor C recharging current magnitude and, consequently, pulse duration will depend only on circuit parameters (without consideration of blanked transistor T_2 shunting).

The following inequality must be satisfied with sufficient reserve in /302 order for transistor T_1 to unblank and moreover for its saturation

$$|U_{61}| > |U_3'|. \tag{VI.113}$$

Here U_{61} -- base potential, while U_3' -- transistor T_1 emitter potential after reversal.

Since divider R_2, R_3 current significantly exceeds unblanked transistor T_1 base current, then the potential of its base changes slightly (one may consider that $U_{61} \approx U_{61}$) and is determined in accordance with (VI.111).

The following evident inequality must be satisfied in the transistor T_1 saturation region

$$U_3' = I_3 R_3 \geqslant I_{61\text{н}} R_3 = \frac{I_{k\text{н}1} R_3}{\beta}. \tag{VI.114}$$

i. e., emitter current rises after saturation due to base current where collector current $I_{k\text{н}1}$ is unchanged. It is possible to determine the latter's magnitude from formula

$$I_{k\text{н}1} = \frac{E_к - I_3 R_3 - u_{к\text{н}1}}{R_{к1}} \simeq \frac{E_к - I_{61} R_3}{R_{к1}}. \tag{VI.115}$$

Substituting (VI.115) in (VI.114) and making simple transforms, we get

$$U_3' = I_{61} R_3 \geqslant \frac{E_к R_3}{R_3 + R_{к1}} \tag{VI.116}$$

Hence, the transistor T_1 saturation condition in the quasistable state, in accordance with (VI.113), may be expressed by circuit parameters

$$\frac{R_3}{R_3} < \frac{\beta R_к}{R_3}. \tag{VI.117}$$

Equating expressions (VI.112) and (VI.117) and assuming $\alpha \approx 1$, it is possible to note requirements for a ratio of collector resistance magnitudes at which the

requirements for transistor T_1 blanking in the circuit's initial state and saturation in the quasistable state simultaneously are satisfied, i. e.,

$$R_{к1} > R_{к2}. \qquad \text{(VI.118)}$$

This is clear also from physical considerations: transistor T_2 current, dependent upon $R_{к2}$ magnitude, creates a voltage drop across resistance $R_к$, which is blanking for transistor T_1; in addition to this, transistor T_1 current must not create a large voltage drop across resistance $R_э$ in order not to hinder saturation of this transistor, i. e., $I_{б1} < I_{к2}$. In practice, the following usually is selected

$$R_{к1} = (1{,}5 \div 2) R_{к2}.$$

We will note that, as opposed to a tube multivibrator, it is impossible /303 in this circuit to eliminate resistance R_2 since, here, negative bias required for transistor T_1 unblanking will not be supplied to its base.

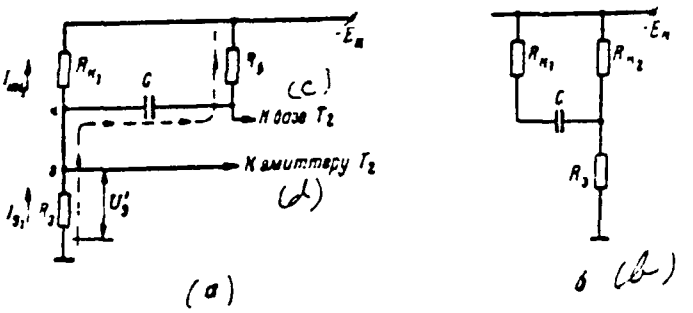

Figure VI.49. Equivalent Capacitor Recharging Circuit.
(c) — To T_2 base; (d) -- To T_2 emitter.

Capacitor C recharges after circuit reversal along network $-E_к, R_к$, transistor T_1, C, $R_э, -E_к$. A capacitor C equivalent recharging circuit is depicted in Figure VI.49a. The shunting influence of blanked transistor T_2 is not considered in this circuit.

In accordance with this circuit, the voltage to which the capacitor will strive to recharge equals

$$U'_{C\,max} = -(E_к - U'_{э}) = \frac{E_к R_{к1}}{R_э + R_{к1}}. \qquad \text{(VI.119)}$$

There is a minus sign in expression (VI.119) since, when the process is completed (if transistor T_2 is removed imaginarily), capacitor voltage polarity will change in comparison to its initial polarity. Concequently, considering initial voltage U'_{C0}, the law of voltage change may be written in the form

$$u_C = -U'_{C\,max} + (U'_{C0} + U'_{C\,max})\, e^{-\frac{t}{\tau_{разр}}} \qquad \text{(VI.120)}$$

where $\tau_{разр} = C\left(R_э + \frac{R_э R_{к1}}{R_э + R_{к1}}\right) \approx CR_э$ -- capacitor recharge time constant.

Transistor T_2 will unblank at the moment when capacitor C voltage reaches the zero level $u_C = 0$. This assertion is justified since unblanked and saturated transistor T_1 will be "shrunk" to a point and it is possible to assume that $u_{к2} = u_C$. Hence, pulse duration along the base, without considering the porch, may be obtained by substitution of values U_{C0} and U_C in formula (VI.120), /304 assuming $t = t_и$:

$$t_и = \tau_{разр} \ln\left(1 + \frac{U'_{C0}}{U'_{C\,max}}\right) =$$
$$= \tau_{разр} \ln \frac{R_{к1}(R_э - R_{э2}) + R_{э2}(R_э + R_{к1})}{R_{к1}(R_э + R_{э2})}. \qquad \text{(VI.121)}$$

The impact of shunting on output pulse parameters is considered precisely in the same manner as was the case in the multivibrator circuit.

Amplitudes of the shaped pulses are determined from formulas:

$$U'_{м1} = E_к - I_{к0} R_{к1} - U_{ост1} - U'_{э} \approx E_к - U'_{э}. \qquad \text{(VI.122)}$$

$$U'_{м2} = E_к - I_{к0} R_{к2} - U_{ост2} - U_м \approx E_к - U_м. \qquad \text{(VI.123)}$$

Emitter current $i_{э2}$ appears following transistor T_2 unblanking and transistor emitter potential decreases. This will lead to an increase in voltage between transistor T_1 base and emitter and, consequently, to a decrease in current $i_{к1}$ and voltage $u_{к1}$. The collector voltage reduction is transmitted across capacitor C to the transistor T_2 base, causing its current $i_{б2}$ to increase. A second avalanche-like process arises in the circuit and this process concludes with transistor T_1 blanking. The small voltage drop across the transistor T_1 collector at the moment of the second reversal explains the presence of resistance $R_э$ (Figure VI.48b).

Next, reestablishment of the circuit's initial state occurs. During this period, capacitor C charges along the network $+E_к$, R_1, T_2 emitter-base path, C, $R_{к1}$, $-E_к$. The capacitor charge time constant may be found from the equivalent circuit (Figure VI.49b):

$$\tau_{зар} = C\left(R_{к1} + \frac{R_{к2}R_э}{R_{к2} + R_э}\right). \qquad \text{(VI.124)}$$

Recovery process duration

$$t_в = (3 \div 5)\tau_{зар} = (3 \div 5)C\left(R_{к1} + \frac{R_{к2}R_э}{R_{к2} + R_э}\right). \qquad \text{(VI.125)}$$

EXERCISE VI.19

a) What is the best way to control pulse duration in an emitter-coupling multivibrator?

b) Is it possible to change pulse duration by changing divider R_2, R_3 resistances, as is the case in a tube multivibrator circuit? (Page 487)

Rise time. Pulse $u_{к2}$ shaped in the transistor T_2 collector usually is used as an output pulse. This pulse has a good porch and droop shape. Pulse /305 rise time will depend on the magnitude of the triggering signal and has magnitude $t_{ф2} \approx \tau_1$ given great input current $i_{б2}$. A high input current magnitude may be obtained either due to trigger pulse source or due to transistor T_1 collector current (see Chapter VI, § 6), which at the reversal stage, will assist in transistor T_2 blanking. Decay time $t_{сп2}$ may be obtained from expression (V.23), in which

$I_{кн} = I_{кн2}$ and $I_б = I_{б2}$ must be placed. As pointed out above, at the reversal stage, transistor T_2 base current is equal in magnitude to transistor T_1 collector current, i. e.,

$$I_{б2} = I_{кн1} \approx \frac{E_к}{R_{к1} + R_э} \qquad \text{(VI.126)}$$

Collector current $I_{кн2}$ may be determined from the formula

$$I_{кн2} \approx \frac{E_к}{R_э + R_{к2}}. \qquad \text{(VI.127)}$$

Therefore, decay time equals

$$t_{сф2} = \tau_э \frac{I_{кн}}{\beta I_б} = \tau_э \frac{R_{к1} + R_э}{\beta (R_{к2} - R_{э1})}. \qquad \text{(VI.128)}$$

Decay time may range from several tenths to unities of microseconds when low-frequency P16, P42, P103, and P104 transistors are used. Rise time can be reduced to hundredths of microseconds when high-frequency P403, P410, P416, and other such transistors are used.

A positive-polarity pulse has a relatively-good porch shape and an elongated droop. Rise time will depend on transistor T_1 operating region, i. e., on current $I_{б1}$ and current $I_{кн1}$ magnitude. A rise time reduction to magnitude $t_{ф1} \approx \tau_э$ requires an increase in base current $I_{б1}$ magnitude during the regeneration process by shunting resistance R_1 with a capacitor of relatively-great capacitance (to several thousand pF). Pulse rise time will depend on the capacitor C charging time constant and has magnitude $t_{ф1} \approx 2.3 \tau_{зар}$.

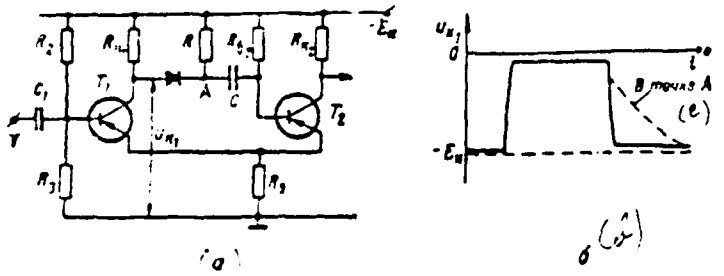

Figure VI.50. Cutoff-Diode Monostable Multivibrator:
(a) -- Circuit; (b) -- Time diagrams; (c) -- At point A.

A cutoff diode employed in the manner depicted in Figure VI.50a is used widely to make a fundamental improvement in pulse u_{K1} droop. At the moment pulse shaping ceases, diode D blanks due to the drop in transistor T_1 collector potential, cutting capacitor C out of the collector network. Here, a steep edge arises in the collector (Figure VI.50b), while capacitor C charges across resistance R. Circuit recovery time $t_{восст} = (3 \div 5)(R + R_{K1} \| R_{K2})C$ is somewhat greater than in the Figure VI.47 trigger circuit with identical parameters. Diode D is unblanked in the initial state and R_{K1} and R parallel connection determines transistor T_1 collector load /306 magnitude. Resistances R_{K1} and R selected usually are identical and equal double the R_{K1} magnitude in the Figure VI.47 circuit.

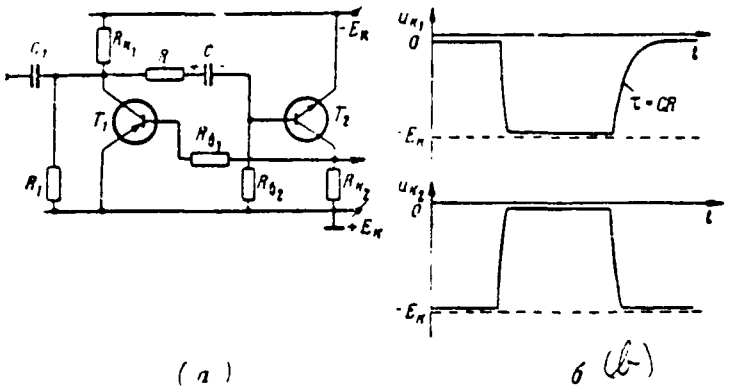

Figure VI.51. Diverse-Conductivity Monostable Transistor Multivibrator: (a) -- Circuit; (b) — Time diagrams.

A diverse-conductivity monostable transistor multivibrator circuit (VI.51) is finding wide practical use. The comparatively-low recovery time is its main advantage.

We will examine the physical process in this multivibrator circuit. Transistor T_2 (rpn-type) is unblanked in the initial state since voltage positive relative to the emitter is supplied to its base. Its saturated state is insured by selection of resistance R_{K1} and $R_{б1}$ magnitudes

$$R_{K1} \geq \beta R_{б1} \qquad \text{(VI.129)}$$

Since the voltage drop across the transistor T_2 collector-emitter path /307 is slight, then negative voltage close in magnitude to source voltage $E_к$ is applied to the transistor T_1 base across resistance $R_{б1}$. Consequently, transistor T_1 (pnp-type) also is unblanked and saturated if the following condition is satisfied

$$R_{б1} \leqslant \beta_1 R_{к1}. \qquad \text{(VI.130)}$$

There is slight negative voltage in the transistor T_1 collector. Therefore, the capacitor is charged to a voltage almost equal to $E_к$. Voltage polarity is depicted in Figure VI.51a).

Capacitor C begins to discharge and excess charge clean-out occurs in the transistor T_2 base when a trigger pulse of negative polarity is supplied. As soon as the transistor T_2 operating point turns out to be in the active region, the potential of its collector begins to increase, causing an increase in transistor T_1 base potential. Transistor T_1 blanking is accompanied by a decrease in its collector potential. The positive feedback network turns out to be closed and an avalanche-like process occurs in the circuit, leading to the blanking of both transistors.

Previously-charged capacitor C begins to recharge across resistances $R_{к2}$, R, $R_{к1}$, striving to recharge itself to voltage $-E_к$. Here, current i_C creates a voltage drop of negative polarity (relative to the common point) across resistance $R_{к2}$, as a result of which transistor T_2 is maintained in the blanked state. Its collector voltage has a slight negative magnitude (Figure VI.51b) and, thus, transistor T_1 also is blanked. Since usually $R_{к2} \gg (R_{к1} - R)$, transistor T_2 unblanks at the moment that capacitor voltage achieves the zero level.

Transistor T_2 collector potential begins to decrease when it unblanks, causing transistor T_1 unblanking. An avalanche-like process arises again in the circuit, with the result that the circuit returns to the initial state. After this, the capacitor begins to charge through the network $+E_к$, transistor T_1, R, C, transistor T_2 base-emitter path, $-E_к$. Resistance R is connected to constrain the capacitor charging current magnitude, which does not exceed the maximum-permissible magnitude

of current across the transistors. Resistance magnitude usually will fall within the bounds of several hundred ohms. Circuit recovery time

$$t_{в.в} = (3 - 5)RC. \qquad \text{(VI.131)}$$

since unblanked transistor T_1 resistance and resistance $R_{к2}$ are much less than R.

The flow of sufficiently-large base current $I_{б2}$ will lead to forced establishment of transistor T_2 collector voltage, i. e., rise time $t_{ф}$ turns out to be slight. /308

Pulse duration in this circuit may be determined just as it was in a multivibrator (see VI.101):

$$t_и = C(R_{б2} - R_{к1} + R)\ln\left(1 + \frac{U_м}{E_к}\right) \approx 0{,}7CR_{б2}. \qquad \text{(VI.132)}$$

since $R_{б2} \gg (R_к + R)$.

This multivibrator may shape pulses with a very high duty ratio.

Maximum duty ratio may be determined from the expression

$$Q = 1 - \frac{t_и}{T_{в.max}} = 1 + \frac{0{,}7R_{к1}}{(3 - 5)R} \qquad \text{(VI.133)}$$

EXERCISE VI.20

Determine the maximum pulse duty ratio in a multivibrator (Figure VI.51) when $R_{к1}$ = 100 kilohms, R = 200 ohms. (Page 488)

CHAPTER VII /309

BLOCKING OSCILLATORS

§ 1. BLOCKING OSCILLATOR GENERAL CHARACTERISTICS

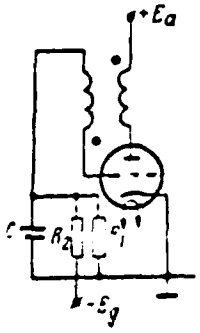

Figure VII.1. Simplified Blocking Oscillator Circuit.

A blocking oscillator is a relaxation oscillator which generates short-time-duration pulses and is a single-stage amplifier with transformer feedback (Figure VII.1). Varied methods of pulse transformer winding connection are used to satisfy phase self-excitation conditions, i. e., to create positive feedback. Thus, for example, transformer windings, which accomplish the coupling between plate and

grid networks, are connected in opposition to each other in a electron tube inverting amplifier circuit.* Thus, a transformer, just like a tube, inverts the signal and the resultant phase shift turns out to equal 2π, meaning that a regenerative process is possible when amplitude self-excitation conditions are satisfied in the circuit. Presence of only one amplifying element (of an electron tube or transistor) is a very valuable blocking oscillator property. The following should be added to the list of other blocking oscillator advantages.

A blocking oscillator makes it possible to shape essentially square pulses with a duration ranging from unities of nanoseconds to several tens of microseconds, with a broad range of change in their repetition frequency.

The power of the shaped pulses, given high duty ratio $\left(Q=\frac{T_0}{t_u}\geqslant 1000\right)$, turns out to be very high even when low-power amplifying tubes or transistors are used. This is explained by the fact that it is possible to obtain currents /310 greatly exceeding currents permissible during a continuous operating mode in tubes and transistors due to a pulse emission or injection, given large control signals. Restoration of emissivity then occurs during resting time.

For this reason, a blocking oscillator has very low internal resistance as a pulse is being shaped and may operate a low-resistance load.

Pulses of varied polarity may be obtained from pulse transformer windings. The amplitude of these pulses may exceed supply source voltage.

A blocking oscillator circuit is simple in design and will comprise few radio components. The pulse transformer is the only element of complex design. However, recently ferrite ring cores were introduced and transformer production technology has become less complex.

The following are among the most significant blocking oscillator shortcomings. First, presence in the circuit of such accumulators of energy as transformer

*Black dots are used in Figure VII.1 to designate opposed connection of the origin of the plate and grid windings.

inductance and stray capacitance will lead to onset of oscillations, which, in some cases, is extremely undesirable and requires special measures to eliminate them or to decrease amplitude. Second, a blocking oscillator places a heavy load on the supply source as a pulse is being shaped (very high current flows across a tube or transistor) and, when a low-power source is used, the voltage in it drops. This may impact negatively on the operation of other circuits connected to the same source. Therefore, decoupling filters always will be installed in the supply network to prevent source overload.

A blocking oscillator, like other relaxation oscillators, may operate in a monostable, free-running, and synchronization mode. All these modes will find use in various radio-technical devices. Specific blocking oscillator uses include employment as generators of modulating and sync pulses in radar stations. Blocking oscillators are used in television equipment to shape sawtooth voltages and currents. They are used in electronic computers as low-resistance switching circuits, pulse counters, and so forth.

It should be noted that analysis of the operation and determination of the quantitative ratios determining blocking oscillator parameters are complicated to a significant degree by the circumstance that, in general, two varied energy accumulators must be considered: transformer stray and timing capacitance and inductance. In addition, operation of the circuit amplifying element occurs in the region where the volt-ampere characteristic is nonlinear to a great degree, where satisfactory piecewise-linear approximation is impossible. Therefore, /311 a graphical-analytical method using tube or transistor pulse dynamic characteristics is used to analyze the processes in a blocking oscillator. A detailed examination of graphical-analytical methods of evaluating blocking oscillators has been made in the literature [2, 3, 8].

§ 2. ELECTRON-TUBE BLOCKING OSCILLATOR PHYSICAL PROCESSES

1. Monostable Blocking Oscillator Basic and Equivalent Circuits

We will examine physical processes in a blocking oscillator using a free-running circuit as our example (Figure VII.2a). Here, the blocking oscillator is assembled on tube L_2, while tube L_1 will serve as trigger pulse amplifier. Both tubes are

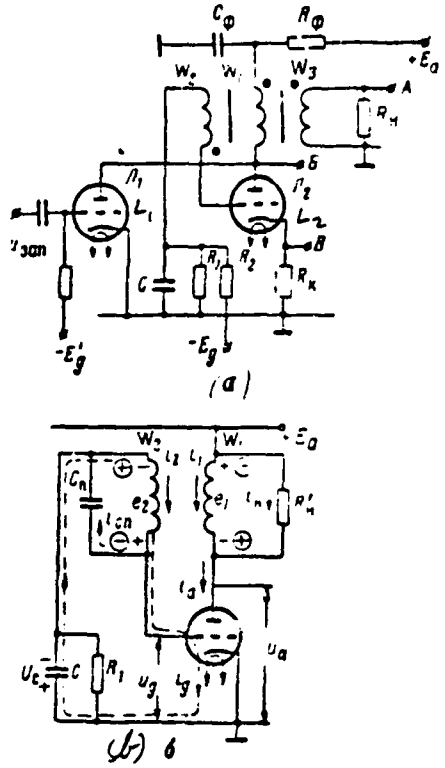

Figure VII.2. Free-Running Blocking Oscillator Schematic Diagram (a) and Its Equivalent Circuit (b).

blanked in the initial state. Tube L_2 is blanked due to the voltage drop across the divider in resistances R_1, R_2 from negative bias source E_g. As was the case in monostable multivibrators, divider parameters are selected in such a way that condition $|U_{c.}| \geq 1.5\ E_g$ is satisfied for reliable tube blanking. Capacitor C connected to the grid network is charged to this voltage. Connection of windings w_1 and w_2 in opposition provides positive feedback between plate and grid networks. Load winding w_3 connection may be random depending on required output pulse /312 polarity. The presence of a load winding is not required in principle. For instance, low-resistance resistor $R_н$ (on the order of several tens of ohms) may be connected to the cathode network to obtain positive-polarity pulses. The influence of this resistance usually is not considered when analyzing blocking oscillator operation because it is so slight.

Resistance R_b and capacitor C_b form a circuit and plate feed source E_a decoupling filter.

Transformer winding stray and tube electrode capacitances must be considered along with the aforementioned elements since they impact materially on shaped pulse rise and decay time.

One may disregard pulse transformer winding leakage inductance sincedesign measures reduce them to a minimum; i. e., "tight" coupling is used, in which the coupling coefficient between windings

$$k = \frac{M}{\sqrt{L_1 L_2}} \approx 1,$$

where L_1 -- plate winding inductance;
L_2 -- grid winding inductance;
M -- mutual inductance.

In future, we will examine only transformer plate and grid windings for simplicity in blocking oscillator operational analysis. It is possible to convert resistance $R_н$ into plate or grid network in order to evaluate the impact of this resistance, connected to the third winding. Let us assume, for example, that the resistance is converted into the plate network and, in accordance with (II.68), equals

$$R'_н = R_н n^2,$$

where $n = \frac{w_2}{w_1}$ -- transformation ratio between load and plate windings.

We will assume in our examination of the physical processes in the blocking generator that total equivalent capacitance has been brought to the transformer grid winding. In this event, the simplified blocking oscillator circuit may be depicted as shown in Figure VII.2b. Circuit operation may be divided into three stages: triggering and pulse porch shaping, tilt shaping, and pulse droop shaping.

2. Pulse Porch Triggering and Shaping

A positive-polarity trigger pulse is supplied to trigger tube L_1 grid, whose load is pulse transformer winding w_1. If trigger pulse porch steepness is sufficiently great, then a negative-polarity pulse is induced in the tube L_2 plate network. This negative-polarity pulse in turn is transformed to the grid /313 network in the form of a positive-polarity pulse.* Tube L_2 unblanks and plate current i_a flowing across resistance R_n and transformer winding w_1 arises in the plate network. Having designated these current components as i_n and i_1, it is possible to write $i_a = i_1 - i_n$.

The flow of current i_1 in the primary winding causes onset of self-induction e_1 emf, whose polarity is depicted in Figure VII.2b by the uncircled signs. Mutual induction emf e_2 arises in the grid network due to coupling among windings, increasing tube L_2 grid voltage. This will lead to a further plate current rise and, consequently, also to a current i_1 rise. Thus, the positive feedback network turns out to be closed and an avalanche-like current and voltage change in the circuit is possible if the amplitude self-excitation condition is satisfied. The avalanche-like current and voltage change in a blocking oscillator circuit has been referred to as the blocking process. A forward blocking process will lead to a rapid rise in grid voltage, a growth in plate and grid current, and a voltage drop across the tube plate. Cessation of the blocking process is linked with a decrease in grid current rate of change, given large positive grid voltages.

It should be considered that, as a result of blocking process rapidity, capacitor C voltage and energy of the transformer magnetic field do not succeed in changing. A change in magnetic field energy is linked with a change in magnetizing current I. This current, for example, brought to the transformer plate winding, may be determined in the following way. Onset of current i_1 in plate winding w_1 is accompanied by a change in magnetic flux and appearance of grid winding w_2 voltage. Current i_2, which arises in the grid winding as a result of the presence of e_2 emf, is directed so that it opposes a magnetic flux change, i. e., it decreases

*This is not the only method of triggering this type circuit. For example, it is possible to trigger the circuit with positive-polarity pulses supplied directly to the tube L_2 grid network across a low-capacitance coupling capacitor.

the magnitude of total ampere-turns. The resultant magnetic flux magnitude is proportional to the magnetizing ampere-turns:

$$Iw_1 = i_1 w_1 - i_2 w_2. \tag{VII.1}$$

Having divided both parts of equality (VII.1) by w_1, we will get

$$I = i_1 - \frac{i_2}{n}, \tag{VII.2}$$

where $n = \frac{w_2}{w_1}$ — transformation ratio between grid and plate windings.

In accordance with current direction depicted in Figure VII.2b, it is evident for a forward blocking process that

$$i_1 = i_a - i_g \tag{VII.3}$$

and

$$i_2 = i_{cn} + i_c. \tag{VII.4}$$

Substituting these values for currents i_1 and i_2 in expression (VII.2), for magnetizing current we finally will get

$$I = i_g - \left(i_g + \frac{i_g}{n} + \frac{i_{cn}}{n}\right) \tag{VII.5}$$

It is evident from the formula obtained that magnetizing action by the rising plate current is compensated for by the demagnetizing action of the simultaneously-rising remaining currents i_g, i_{cn}, i_g . Therefore, magnetic field energy $W_L = L_1 \frac{I^2}{2}$ during the course of the entire blocking process essentially remains equal to zero since there are no currents in transformer windings prior to triggering.

We will examine the development of a forward blocking process in more detail. The condition for onset of an avalanche may be written in the following form:

$$Kq > 1, \tag{VII.6}$$

K -- stage gain;

$q = \frac{1}{n} = \frac{w_2}{w_1}$ -- voltage transfer constant from plate to grid.

Grid and load winding resistances must be brought to the plate network to determine stage gain. Here, one must consider that, initially, grid voltage is negative and grid current is absent. Therefore, load resistance connected to the grid winding is very great and one may disregard grid network shunting action. As was demonstrated above, load resistance brought to the plate network has magnitude

$$R'_н = R_н n^2$$

Consequently, one may write the expression for stage gain as

$$K = \frac{\mu R'_н}{R_i + R_н} = S \frac{R_i}{R_i + R_н} R'_н = S_д R'_н. \qquad \text{(VII.7)}$$

where $S_д$ -- dynamic slope of the plate-grid characteristic.

Hence, the condition for onset of a forward blocking process is determined by the ratio

$$\frac{S_д R'_н}{n} > 1 \qquad \text{(VII.8)}$$

or /315

$$S_д > \frac{n}{R_н}. \qquad \text{(VII.8a)}$$

The latter inequality demonstrates that onset of the blocking process requires that tube dynamic slope at a minimum exceed the load characteristic slope by a factor of n. Consequently, trigger pulse amplitude must be such that the operating point during triggering shifts to the region of sufficiently-large tube plate-grid characteristic slope values where condition (VII.8a) is satisfied.

Since grid current is absent at the onset of a forward blocking process when $u_g < 0$, then current i_2 arising under the stimulus of e_2 emf closes across stray capacitance $C_н$, charging it. Grid current appears when voltage u_g achieves the zero level and part of current i_2 flows across the tube grid-cathode path.

A rise in grid current occurs due to a further voltage u_g increase, while grid-cathode path dynamic resistance R_{gk} drops. In this event, grid network shunting action rises and the condition for blocking process existence must be written with consideration for resistance $R'_{gk} = R_{gk}n^2$ brought to the plate network.

Thus,

$$\frac{S_\partial R_\text{э}}{n} > 1 \qquad \text{(VII.9)}$$

Here

$$R_\text{э} = \frac{R'_\text{н} R'_{gk}}{R'_\text{н} + R'_{gk}}.$$

Condition $R'_\text{н} > R'_{gk}$ usually is satisfied in practice, given positive grid voltages. In this case, inequality (VII.8) may be rewritten in the form

$$\frac{S_\partial R'_{gk}}{n} = S_\partial R_{gk} n > 1. \qquad \text{(VII.10)}$$

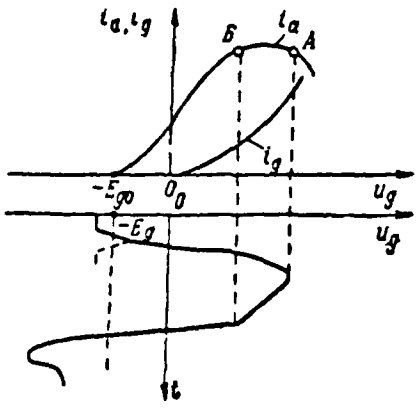

Figure VII.3. Illustration of the Change in Plate and Grid Currents During the Pulse Shaping Process.

Condition (VII.10) for existence of a forward blocking process ceases to be

satisfied in the region of large positive grid voltage values due to the rise in grid current characteristic slope and decrease in the plate current characteristic slope (Figure VII.3). The latter is explained by the fact that transformer winding voltages will rise when grid voltage rises, while tube plate voltage $u_a = E_a - e_1$ drops. Therefore, electrons are redistributed between plate and grid and plate current decreases.

Value $S_0 R_{ekv}$ will become equal to unity at a certain moment in time and the condition for existence of a forward blocking process ceases to be satisfied. Consequently, the rate of voltage rise in the circuit stops increasing. /316 Nonetheless, pulse porch shaping continues and the voltages and currents in the circuit continue to rise. Physically, this is explained by circuit inertness caused by the presence of shunting stray capacitances.

In actuality, current i_{C_0}, which branches into equivalent stray capacitance C_0, rose during the avalanche-like change in e_2 emf.

Voltage in the transformer grid winding and current across stray capacitance C_0 connected to this winding are coupled by known relationship

$$i_{C_0} = C_0 \frac{de_2}{dt}$$

It is evident thereby that current i_{C_0} reaches its maximum value at the moment the condition for an avalanche-like change of voltages ceases being satisfied and the rate of e_2 emf rise stops increasing. The presence of inductance in the grid network does not allow this current to disappear instantaneously. Consequently, this current will begin to decrease. But, the self-induction emf arising here in the grid network will strive to maintain decreasing current i_{C_0}. Therefore, the rise in transformer winding voltages continues, even though the rate of their rise begins to drop, i. e., the reversal process will be delayed. The rise in transformer winding voltages will cease when current i_{C_0} equals zero and, with this, the reversal process ceases.

The tube operating point turns out to be in the region of significant grid current slope and very slight (or even negative) plate current slope (Figure VII.3). Here, magnitude [illegible] and avalanche-like voltage and current changes are impossible.

3. Pulse Tilt Shaping

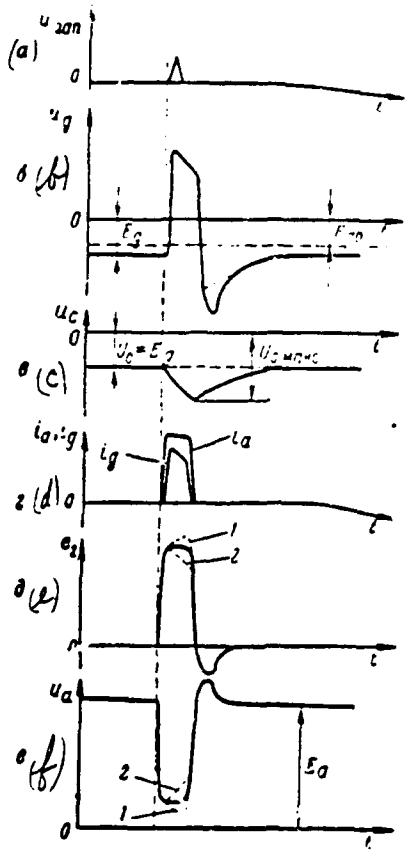

Figure VII.4. Monostable Blocking Oscillator Voltage and Current Curves.

Capacitor C voltage (Figure VII.4c) and transformer magnetizing current I essentially did not change during rapid porch shaping. Relatively-slow /317 processes linked with the rise in transformer magnetizing current I and capacitor C charging begin to occur following the reversal in the blocking oscillator circuit. It is possible during this period to disregard the influence of the stray capacitance since current i_{c_a} is infinitesimally small during the relatively-slow changes in potential. One also may overlook the influence of plate current on ongoing processes during the intitial stage of pulse tilt shaping since the plate

characteristic slope is slight. The grid characteristic slope is great and, therefore, grid current changes determine circuit state.

Grid current will charge capacitor C since voltage e_2 is positive relative to tube grid. Tube grid voltage $u_g = e_2 - u_C$ decreases due to capacitor charging, which in turn will lead to a grid current decrease. In this event, the grid current decrease causes appearance of self-induction emf in the transformer grid winding. Mutual induction emf arises in the plate network due to winding coupling. The signs of these emf are retained, just as was the case during a forward blocking process (the uncircled emf signs in Figure VII.2) in accordance with the law of electromagnetic induction. Transformer winding voltages change relatively slowly as a result. Magnetizing current I rises during this period mainly due to the grid current decrease coupled with a grid voltage decrease.

It should be noted that tilt shape may vary depending on the magnitude /318 of capacitor C capacitance. Capacitor C charges rapidly and grid current will decay rapidly, given sufficiently-slight capacitanc (several hundred pF). In this event, a sharp grid current decrease will elicit appearance of relatively-large self-induction emf and its magnitude may exceed that of e_2 emf extant at the moment of pulse porch cessation. A rise in grid winding voltage will lead to a slight decrease in tube plate voltage (dotted curve 1 in Figures VII.4e and VII.4f).

The capacitor voltage rise is insignificant if capacitance C is sufficiently great (several tens of thousands of pF) and e_2 emf will decrease with a decrease in grid voltage, i. e., the pulse tilt will slope (curve 2 in Figures VII.4e and VII.4f).

Finally, a decay in voltage u_g may compensate for a voltage u_C rise for a given capacitance C value, while voltages e_2 and u_a will remain approximately constant. This event is of the greatest practical interest since it makes it possible to shape an almost square pulse.

Due to the voltage decrease, the operating point gradually returns to the region where the plate characteristic slope takes on an ever greater value and,

at certain point 5 (Figure VII.3), reaches a magnitude at which the condition for existence of a blocking process again is satisfied.*

The pulse tilt shaping stage ends here. It should be noted that the duration of this process and, therefore, that of the shaped pulse, will depend on the capacitor charge rate, determined by the $R_{..}C$ time constant. Therefore, it is possible within certain limits to control output pulse duration by changing capacitor C capacitance.

4. Pulse Droop Shaping and Circuit Return to Initial State

An avalanche-like process leading to tube blanking arises again in the circuit as soon as the operating point turns out to be in the characteristic region where slope S_1 is sufficiently great and inequality (VII.10) begins to be satisfied.

In actuality, a voltage u_g reduction due to capacitor C charging begins to cause a noticeable plate current decrease. This leads to appearance of self-induction emf in the plate network, which strives to maintain the decreasing plate current (the polarity of this emf is depicted by the circled signs in Figure VII.2b). Mutual induction emf arising here in the grid network leads to a decrease in resulting winding w_2 voltage. Now, voltage u_g drops, not only due to capacitor C charging, /319 but mainly due to the voltage decrease in the transformer secondary winding. This in turn leads to a further, sharper, plate current decrease. Stray capacitance C_n begins to discharge during this process and a further rise in magnetizing current I occurs due to the flow of current i_{Cn} across transformer windings.

The developing avalanche-like process (the so-called reverse blocking process) leads to rapid tube blanking. The capacitor turns out to be charged to a certain voltage $U_{c\,макс}$ after tube blanking (Figure VII.4c). Magnitizing current also has a maximum value $I_{макс}$. Relatively slow processes linked with capacitor C discharge across divider resistance and with a magnetizing current decrease now begin in the circuit. Equivalent transformer parameters determine the nature of the magnetizing current decay and may occur in an aperiodic or oscillating manner.

*Strictly speaking, a reverse blocking process flows along other dynamic characteristics since another voltage acts in the tube grid due to capacitor C charging. However, the nature of the reversal processes here is unchanged.

The nature of the magnetizing current decrease is aperiodic if transformer windings are shunted by sufficiently-low resistances and ceases in the initial period of capacitor C discharge, as depicted in Figure VII.4b.

The quality of the loop formed by transformer inductance and stray capacitance, given a low-resistance load, turns out to be great and a oscillatory process with initial current $I_{маис}$ arises in the circuit.

The aperiodic nature of magnetizing current change usually is required since tube unblanking may occur during the oscillatory mode during positive grid voltage half-waves. In this case, the blocking oscillator will operate in the free-running mode and will shape distorted sinusoidal oscillations. In this connection, given a high-resistance load, a shunting resistance or damping diode must be connected in parallel with the transformer.

Capacitor C voltage will equal $U_{C0}=E_a$ following cessation of the transient processes and the blocking oscillator returns to the intital state.

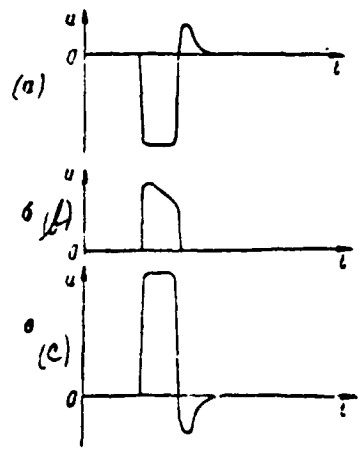

Figure VII.5. Pulse Shape at Different Blocking Oscillator Outputs.

EXERCISE VII.1

Oscillograms of pulses at different blocking oscillator outputs are depicted in Figure VII 5 (see Figure VII.2a). Determine the output point to which each of the indicated oscillograms corresponds. Explain the difference in these oscillograms. (Page 488)

§ 3. BLOCKING OSCILLATOR ELECTRON-TUBE CIRCUIT VARIANTS

1. Free-Running Blocking Oscillator

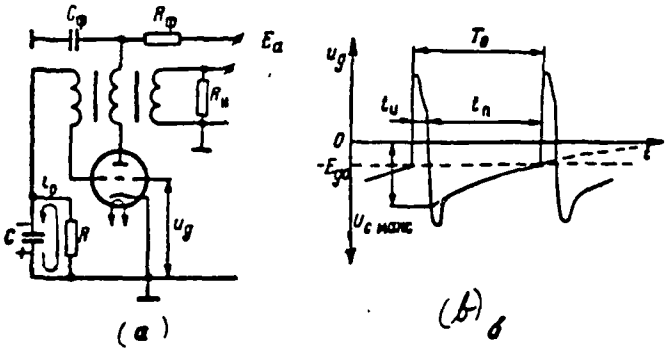

Figure VII.6. Free-Running Blocking Oscillator:
(a) -- Schematic diagram; (b) -- Grid voltage curve.

Negative bias source E_g and resistance R_2 must be eliminated in order for the Figure VII.1 blocking oscillator circuit to operate in the free-running mode. In this case, the blocking oscillator will take the form depicted in Figure VII.6a, in which the tube is blanked due to capacitor C charging during the pulse shaping process. The physical processes involved with pulse shaping do not differ in any way from corresponding processes in a monostable blocking oscillator.

The capacitor turns out to be charged to certain voltage $U_{C\,max}$, which exceeds blanking voltage (E_{go}) in absolute magnitude, following pulse cessation. The polarity of this voltage is depicted in Figure VII.6a. Further, the capacitor begins to discharge by the law of exponents $u_C(t) = U_{C\,max} e^{-\frac{t}{RC}}$.

Tube grid voltage $u_g = -u_c$ increases due to capacitor discharge until unblanking voltage $-E_{go}$ is achieved. The tube unblanks and a reversal similar to that described above occurs in the circuit.

Resting time duration t_n (see Figure VII.6b), during which the tube /321 is blanked, may be found from the expression

$$u_g(t) = -u_c(t) = -U_{c\,max} e^{-\frac{t}{RC}},$$

in which one must assume $u_g = -E_{go}$ when $t = t_n$:

$$u_g(t_n) = -U_{c\,max} e^{-\frac{t_n}{RC}} = -E_{go}.$$

Taking the logarithm of the latter inequality, we will get

$$t_n = RC \ln \frac{U_{c\,max}}{E_{go}} = 2{,}3\,RC \lg \frac{U_{c\,max}}{E_{go}}. \qquad \text{(VII.11)}$$

Expression (VII.11) may be used to determine pulse repetition period $T_0 = t_n + t_u \approx t_n$ since a blocking oscillator usually operates in a high duty ratio mode.

Repetition period T_0 is a very unstable magnitude since the slope of the exponential curve is very low at the point of blocking oscillator reversal. Large T_0 changes cause insignificant unblanking voltage E_{go} changes occurring due to the change in supply voltages or when tubes are replaced.

A retarding-field circuit is used to increase the stability of the repetition frequency of pulses the blocking oscillator generates (Figure VII.7a). Capacitor C in this circuit discharges along network $+E_a$, R, C, $-E_a$. Capacitor voltage here will strive to the $+E_a$ level (Figure VII.7b) rather than to the zero level, as was the case in the blocking oscillator circuit (Figure VII.6a), i. e., there is a tendency towards capacitor C recharge. Consequently, the exponential curve will be shorter and will intersect the line at a large angle and voltage /322 E_{go} instability will elicit a lesser T_0 change.

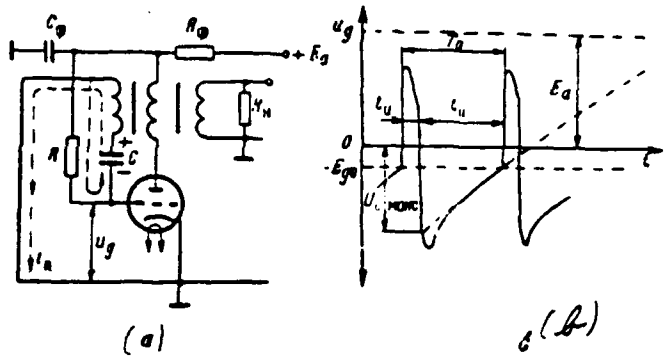

Figure VII.7. Retarding-Field Blocking Oscillator:
(a) -- Schematic diagram; (b) -- Grid voltage curve.

Pulse repetition period T_0 may be determined, considering that the capacitor begins to discharge from level $E_a + |U_{C\,макс}|$, but succeeds in discharging only to magnitude $E_a + |E_{g0}|$ (see Figure VII.7bC. Therefore

$$T_0 \approx 2.3 RC \lg \frac{E_a + |U_{C\,макс}|}{E_a + |E_{g0}|}. \qquad \text{(VII.12)}$$

It should be noted that the magnitude of resistance R in a blocking oscillator is selected in the range of several hundred kilohms to several tens of kilohms, at least. This is required in order to decrease the component of grid current flowing from the plate supply source. In turn, this measure is stipulated by the fact that tube grid current rises sharply at the moment of pulse generation due to large positive transformer secondary winding voltages and the power dispersed by the grid rises. The heat mode of the grid, rather than of the plate, in some cases determines the maximum power the tube supplies. Thus, for example, $P_{a\,доп}$ = 2.75 W, while $P_{g\,доп}$ = 0.2 W for a 6N8S tube, with plate and grid currents during the pulse comparable.

Resistance R within a range of several kilohms and connected directly to tube plate is selected in those cases when there is a requirement for a very high pulse repetition frequency (on the order of several tens of kilohertz), given a relatively-low duty ratio. In this event, the grid current component flowing across resistance R decreases since tube plate voltage drops as the pulse is shaped. However, pulse porch and droop deteriorate in such a circuit.

EXERCISE VII.2

A retarding-field blocking oscillator is used in a modulator to shape square pulses with duration $t_и$ = 3 usec and repetition frequencies F_1 = 1 kHz and F_2 = 10 kHz. Which element can be used to change the repetition frequency? Why? (Page 488)

2. Blocking Oscillator with a Grid Network Circuit

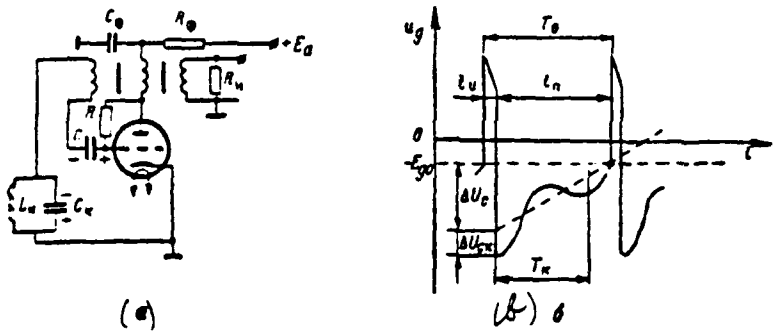

Figure VII.8. Blocking Oscillator with a Grid Network Tuned Circuit: (a) -- Schematic diagram; (b) -- Grid voltage curve.

A resonant circuit included in the grid network (Figure VII.8a) or in the cathode network is used in a blocking oscillator to improve pulse repetition frequency stability. The period of inherent oscillations $T_к = 2\pi\sqrt{L_к C_к}$ selected in such a circuit is significantly greater than the duration of the shaped pulse. In this case, inductive impedance $L_к$ is great for rapidly-changing grid current. Therefore, it may be disregarded while the pulse is being shaped. Circuit capacitance $C_к$, along with capacitance C, forms resultant capacitance $C_0 = \frac{CC_к}{C + C_к}$, which plays exactly the same role as does capacitance C in Figure VII.6a. Grid /323 current charges both capacitors while the pulse is being shaped and, since the following is selected

$$C_к = (5 \div 10)\,C, \tag{VII.13}$$

then the voltage increment is $\Delta U_{C_к} < \Delta U_C$ at the end of the pulse. The blocking

oscillator tube is blanked immediately after the pulse is shaped and shock excitation of the free oscillations in the resonant circuit results. These oscillations are accumulated with exponential capacitor C voltage, resulting in the sum (Figure VII.8b) $u_g \approx -(u_C + u_H)$ determining the grid voltage. Selecting the ratio between free-running period T_0 and period T_H using a distinct method, one may conclude that grid voltage approached unblanking level E_{go} sufficiently-steeply and pulse repetition period instability decreased sharply.

EXERCISE VII.3

Determine which T_0 and T_H ratios (Figure VII.8b) insure an increase in resting time stability if ratio (VII.13) is satisfied. (Page 488)

3. Blocking Oscillator with a Grid Network Delay Line

As pointed out above, tube parameters and the magnitude of the capacitor capacitance in the grid network determine the duration of pulses shaped by a blocking oscillator. The blocking oscillator circuits examined do not insure high shaped pulse duration when tube operating mode changes, a tube wears out, or a tube is replaced. Meanwhile, pulse duration may change by 50% or more.

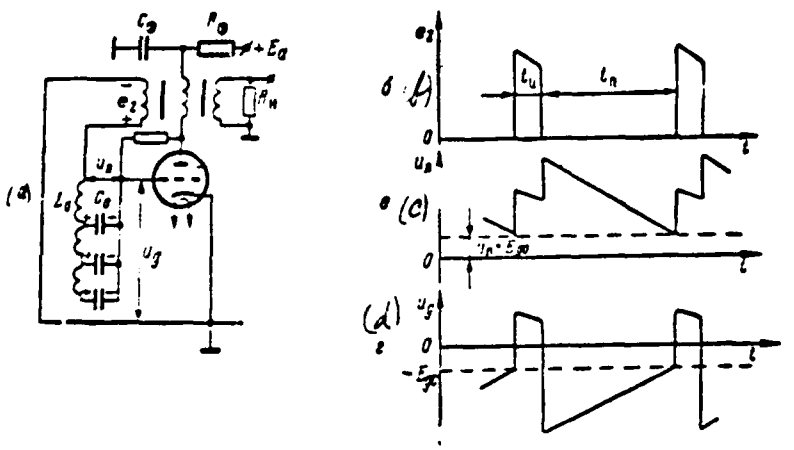

Figure VII.9. Blocking Oscillator with a Grid Network Delay Line: (a) -- Schematic diagram; (b) -- Voltage curves.

Pulse duration stability may be increased considerably if the capacitor in the grid network is replaced by an artificial delay line opened at the end (Figure VII.9a). This line's characteristic impedance is $\rho_л \approx R_{gk}$ (R_{gk} -- average value of the resistance of the grid-cathode path of a tube operating in the pulse mode where $u_g > 0$).

The voltage drop arising across the transformer grid winding during the forward blocking process will be divided between resistance R_{gk} and line input resistance $R_{вх}$. Since the line input resistance for an incident wave equals its characteristic impedance ($R_{вх} = \rho_л$), voltages at line input and tube grid equal:

$$u_л = \frac{e_2 - |E_g|}{R_{вх} + R_{gk}} \cdot R_{вх}; \qquad \text{(VII.14)}$$

$$u_g = \frac{e_2 - |E_g|}{R_{вх} + R_{gk}} \cdot R_{gk}. \qquad \text{(VII.15)}$$

The voltage active in the tube grid transfers the operating point to the region where $S \cdot R_{gk} n < 1$ and the avalanche ceases.

When the incident wave reaches the open end of the line, its reflection with the identical sign will occur. The reflected wave returns to line input terminals after time interval

$$t = 2t_л = 2n\sqrt{L_0 C_0}.$$

where n -- number of elementary links; /325

L_0 -- inductance of one link;

C_0 -- capacitance of one link.

Voltage at line input at that moment rises sharply. Since $u_g - u_л = e_2 \approx \text{const}$, grid voltage drops sharply, the operating point shifts to the region of significant plate current slope, which leads to a counter reversal.

Consequently, shaped pulse duration will not depend upon tube operating mode and is determined by the magnitude of the delay, i. e.,

$$t_и = 2n\sqrt{L_0 C_0} \qquad \text{(VII.16)}$$

Next, the line discharges (VII.9c) across resistance R. Recoveries of line inductance L_0 do not exert an essential impact on the slow process and they can be disregarded, assuming that capacitance $C = nC_0$ will be found in the grid network.

It should be noted in conclusion that the pulse transformer used in the Figure VII.9a circuit must be calculated for duration $t > 2t_1$ in order that magnetizing current does not saturate the core while the pulse is being shaped.

§ 4. TRANSISTOR BLOCKING OSCILLATOR

Transistor blocking oscillators in operating principle differ little from corresponding tube circuits and are relaxation oscillators with one amplifying element, where positive feedback is accomplished with the aid of a pulse transformer. Various methods of connecting the transformer secondary winding make it possible to use both a common-emitter and a common-base tranformer circuit. In addition, there are several ways of connecting the timing capacitance.

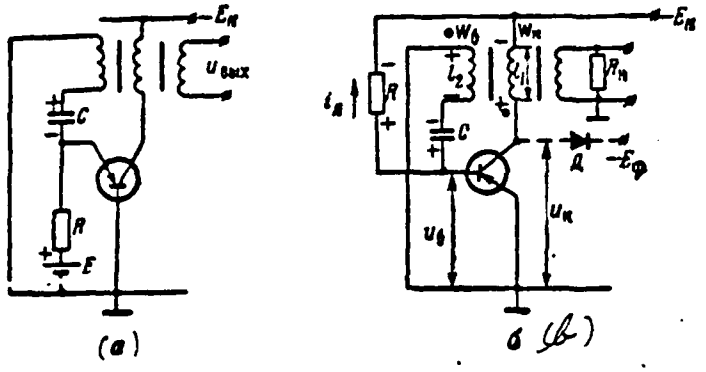

Figure VII.10. Transistor Blocking Oscillator:
(a) -- Common-base circuit; (b) -- Common-emitter circuit.

Two transistor blocking oscillator circuits, one with a common base (Figure VII.10a) and the other with a common emitter (VII.10b), are depicted in Figure VII.10. Negative bias to base is accomplished in both circuits, which insures good pulse repetition period stability. Thus, for instance, leakage resistance R in the common-emitter blocking oscillator circuit is connected to supply source $E_к$, which insures capacitor C recharge rather than discharge. In this sense,

this circuit is analogous to the retarding-field blocking oscillator circuit. The reasons behind only this method of resistance connection were examined in Chapter VI, § 7).

We will examine the physical processes in a blocking oscillator circuit in general terms (Figure VII.10b).

Capacitor C, charged during pulse shaping to maximum voltage $u_c = U_{c\,макс}$, recharges across the transformer secondary winding and resistance R. Recharging current creates across the resistance a drop in voltage whose polarity is shown in Figure VII.10b. As a result, base potential turns out to be positive relative to emitter and the transistor will be in the blanked state. Positive base voltage decreases due to capacitor recharge (VII.11a). The transistor unblanks /326

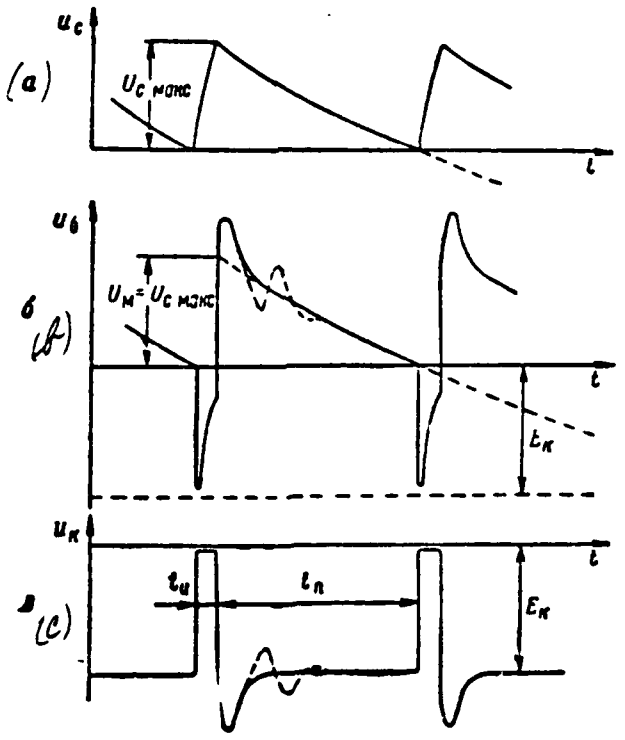

Figure VII.11. Common-Emitter Blocking Oscillator Voltage Curves.

at the moment it reaches cutoff voltage, approximately equalling zero and current $i_к$ appears in the collector network. The appearance and increase in voltage $i_к$ causes onset of self-inductance emf e_2 in the primary winding, which constrains the voltage $i_к$ increase. Mutual induction emf e_2 of identical polarity arises in the secondary winding, at which time base potential decreases. A further collector current rise results. Base current $i_б$, which constrains the voltage e_2 rise, appears and rises, given positive base voltages. Thus, a forward avalanche-like process is accomplished in the circuit and is similar to a tube blocking oscillator circuit. The forward avalanche ceases due to characteristic nonlinearity of collector current achieving saturation. Capacitor C voltage virtually remains unchanged during the avalanche-like process since reversal rate is high and shaped pulse rise time is slight.

Collector voltage in the saturation mode almost equals zero (Figure VII.11c).

Input current does not control collector current upon conclusion of a forward avalanche due to presence of saturation and mutual inductance emf drops sharply. Self-induction emf with a sign identical to that of mutual induction emf arises in the secondary winding because base current dynamic characteristic slope has a high value and because of the current $i_б$ decrease. Presence of coupling among transformer windings leads to onset of self-induction emf in the primary network and collector potential remains close to zero as usual. /327

Presence of self-induction emf in the base winding leads to base current charging capacitor C. Capacitor voltage here increases rather rapidly since emitter-base path direct resistance is very slight. Base potential increases due to capacitor C charging and current in the input network decreases, facilitating transistor exit from saturation. The tilt shaping process ceases at the moment base current decreases to the point at which the magnitude of current gain β is sufficient for onset of a reverse avalanche-like process. The collector current decrease elicits appearance of self-induction emf in the primary winding, while emf polarity will be opposite to that which arose as current $i_к$ rose. Base /328 potential increases and current in the input network decreases due to positive feedback action, which in turn causes a further collector current decrease, and so forth. A reverse avalanche-like process arises in the circuit, which leads to transistor blanking. Collector voltage decreases to source $E_к$ voltage and

below. This is explained by the fact that magnetizing current reached a specific value while the tilt was being shaped and it is unable to disappear instantaneously following transistor blanking. Self-induction emf leading to a negative collector current "bump" arises as a result. Resultant collector voltage significantly may exceed collector junction breakdown voltage. Nonetheless, there will be no irreversible changes in the pn-junction structure thanks to the short duration that this "bump" is active.

We will note that the "bump" may convert to stray oscillations (indicated by the dotted line in the curves of voltages $u_б$ and $u_к$), given high stray loop Q.

The relatively-slow capacitor C recharging process described above begins anew following transistor blanking.

EXERCISE VII.4

Connection of pulse transformer windings in a common-emitter transistor blocking oscillator is depicted in Figure VII.10b (dots denote winding ends here). Indicate how the pulse transformer windings must be connected in the Figure VII.10a circuit. (Page 488)

Specific special features inherent only in transistors are not considered in the processes examined. Thus, for example, the inertness of the processes linked with carrier diffusion plays a material role during pulse porch and droop shaping. This leads to pulse porch, and especially droop, stretching. The rate of regenerative process flow in high-frequency transistors is constrained by pn-junctions capacitances. Pulse rise and decay time in blocking oscillators containing modern transistors comprises hundredths of usec.

The capacitor C recharging process during resting time is complicated compared to the process in tube circuits by the presence of the shunting action of blanked pn-junctions. Consideration is taken of shunting just as was the case in for a multivibrator (Chapter VI, § 7).

However, it should be noted that shunting in a common-base circuit differs from that in a common-emitter circuit. Capacitor C discharging currents in both

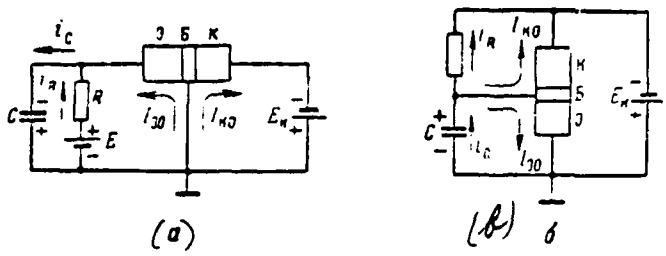

Figure VII.12. Blocking Oscillator Capacitor Recharging Network: (a) -- Common-base circuit; (b) -- Common-emitter circuit.

circuits are depicted in Figure VII.12. As is evident from the figure, along with the current $I_{к0}$ unstable component, one more current $I_{кu}$ component, having the identical sequence, is added to the capacitor discharging current in the common-emitter circuit.

A change in environmental temperature in this case leads to a more /329 significant change in the shunting component of the current and, consequently, to a more significant change in resting time between pulses.

A decrease in the influence of transistor shunting action requires an increase in the current i_R component through a decrease in resistance R. This essentially requires that the following conditions be satisfied

$$i_R > 10(I_{к.т} + I_{кu})_{макс}$$

Corresponding capacitor capacitance selection insures the requisite pulse repetition period value. The given pulse duration value constrains the maximum possible capacitance value.

The resting time temperature stability increase is achieved also by introduction

into the circuit of an additional compensating element, whose parameters change when the temperature changes. An example of temperature stabilization with the

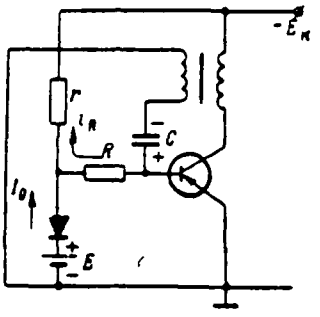

Figure VII.13. Blocking Oscillator Circuit with Resting Time Temperature Stability.

use of semiconductor diode D is depicted in Figure VII.13. Back currents across emitter and collector junctions increase when temperature increases, but current across resistance R decreases. The latter occurs because back current I_0 across the diode pn-junction also increases with a temperature increase and, consequently, the voltage drop across resistance r increases. This leads to a current decrease across resistance R. A current decrease across the resistance compensates for the capacitor C discharging current increase flowing across the transistor /330 pn-junction. Normal circuit operation is insured, given the following resistance ratios: $R_{вар} \gg R > r$. Good results are obtained when compensating diode heat inertness is identical to transistor heat inertness.

It also is necessary to point out that the collector voltage "bump" during transformation to the secondary winding significantly may increase base voltage, with shunting action sharply increasing at that time. This may radically reduce resting time.

EXERCISE VII.5

A diode sometimes shunts pulse transformer winding [illegible] so there will be no "bump" increasing shunting activity. Think how the damping diode in the Figure VII.10b circuit needs to be connected. (Page 489)

The formula for computation of resting time between pulses without considering shunting may be proven analogously to the formula for determination of pulse duration in a multivibrator (VI.101), i. e.,

$$t_n = \tau \ln\left(1 + \frac{U_M}{E}\right).$$

Here, the capacitor recharge time constant is $\tau = RC$, the voltage level to which the exponential curve will strive (see Figure VII.11b) equals $E_к$, while it is possible to approximate the U_M magnitude as

$$U_M = nE_к, \tag{VII.17}$$

where $n = \frac{w_б}{w_к}$ -- transformation ratio.

Actually, the transistor will be in saturation during tilt shaping and, therefore, the voltage drop across the collector winding almost equals $E_к$. Then base collector voltage will approximate $\approx E_к$. Capacitor C charges approximately to this voltage. A positive "bump" in the base winding, in view of its brief duration, may be disregarded. Consequently, the resting time formula acquires the form

$$t_n \approx RC \ln\left(1 + \frac{nE_к}{E_к}\right) = RC \ln(1 + n). \tag{VII.18}$$

This formula may, with sufficient precision, determine pulse spacing. Since usually $t_и \ll t_п$, then

$$T_0 = t_и + t_п \approx t_п.$$

The effect of the accumulation of carriers linked with transistor bottoming exerts a material impact on generated pulse duration, as do such external circuit elements as inductance L, capacitance C, and reduced load impedance $R'_н$. The operating point sometimes is prevented from approaching the bottoming region by using clamping diode D (Figure VII.10b) to clamp collector voltage at th -(0.5 ÷ 1) V level in order to reduce pulse duration.

A blocking oscillator may operate in the monostable mode. Introduction of positive bias source $E_{см}$ into the base network, as depicted in Figure VII.14a

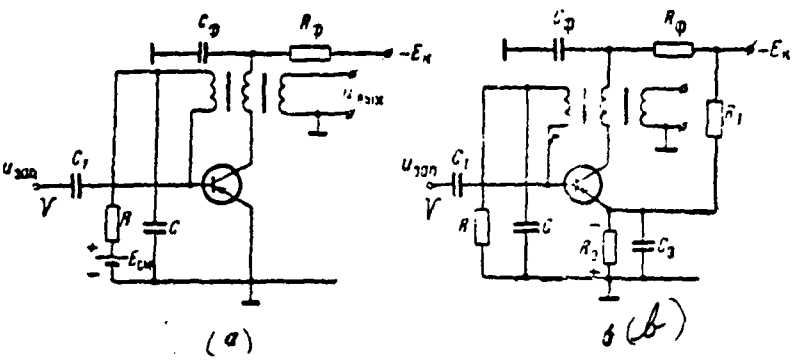

Figure VII.14. Monostable Transistor Blocking Oscillator Circuits: (a) -- With separate bias source; (b) -- With voltage divider.

or use of negative bias in the emitter network (Figure VII.14b) is necessary to accomplish this. In the latter case, bias is created due to source $E_п$ in the divider in resistances R_1, R_2. Resistance R_2 shunts capacitor C_3 of relatively-large capacitance (to unities of microfarads). A bias voltage magnitude ranging from 1--2 V is selected.

P16A and P16B pulse transistors may be used in blocking oscillator circuits. High-frequency transistors such as P403, P416, and so on are used for generation of short-duration pulses ($t_и < 1.0$ usec).

Ferrite-ring transformers with a small number of winding turns (5--40 turns) are used as pulse transformers.

CHAPTER VII /332

PULSE GENERATOR SYNCHRONIZATION. PULSE FREQUENCY DIVIDERS

§ 1. SYNCHRONIZATION AND FREQUENCY DIVISION PRINCIPLES

The essence of synchronization is that the operating rhythm of a self-excited pulse oscillator is set from without by sync signals produced by another oscillator (synchronizing generator or master oscillator). Pulse generators in RLS pulse devices are synchronized in the following three instances.

First, when there is a requirement to increase the repetition frequency stability of pulses produced by a self-excited oscillator. In this event, a highly-stable synchronizing generator provides synchronization.

Second, when there is a requirement strictly to match the operation over time of several self-excited oscillators. In this case, all self-excited oscillators are synchronized from the same synchronizing generator and, therefore, produce pulses strictly synchronized at identical moments in time.

Third, when there is a requirement for precise division of the pulse repetition frequency into whole number multiples. In this instance, a synchronization mode is insured in which the synchronized generator produces pulses by a whole number multiple shorter than those produced by the synchronizing generator.

The first problem, increasing the repetition frequency stability of pulses produced by synchronizing generators, usually is solved in the second and third instances. Therefore, as a rule, synchronizing signals must differ from the highly-stable repetition frequency. Sinusoidal voltage produced by a highly-stable self-excited master oscillator (usually with quartz frequency stabilization) may be used as the synchronizing signal. But, short pulses with a steep porch obtained, for example, by clipping and differentiating master oscillator sinusoidal voltage (Figure I.9) or produced by a special highly-stable sync pulse generator are used more often. In future, we will examine synchronization by means of short /333 pulses, which is of the greatest practical use.

Coordination of synchronizing and synchronized generators is explained in Figure VIII.1. The former produces a periodic sync pulse train with frequency

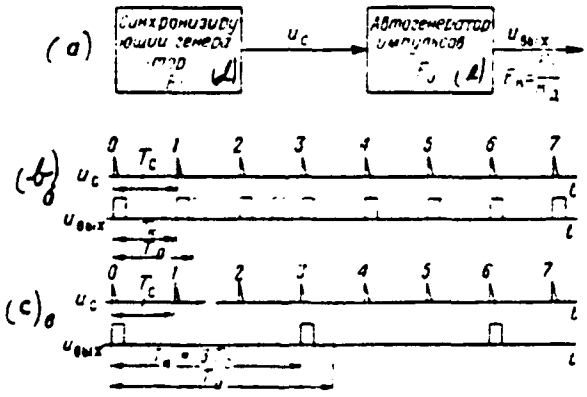

Figure VIII.1. Principle of Self-Excited Pulse Generator Synchronization. (d) -- Synchronizing generator F_c; (e) -- Self-excited pulse generator F_0.

F_c (with period T_c). These pulses are supplied to the self-excited oscillator with inherent pulse repetition frequency F_0 (with period T_0). Under the stimulus of the sync pulses, the self-excited oscillator operates with forced repetition frequency $F_k = \frac{F_c}{K_k}$ (with period $T_k = K_k T_c$), where K_k -- whole number referred to as the scaling factor. If $K_k = 1$, then $F_k = F_c$ and the process is referred

to as synchronization at the basic frequency or simply synchronization (Figure VIII.1b). If $K_1 \neq 1$, then the process is referred to as synchronization on the k-th subharmonic or pulse-rate division to the K_1-th multiple ($K_1 = 3$ in Figure VIII.c, i. e., three-to-one frequency demultiplication occurs).

Regardless of the K_1 value, the synchronization mechanism consists of the fact that, during each free-running cycle, forced generator reversal occurs due to sync pulse stimulus, precluding its natural reversal due to the stimulus of internal forces. A positive sync pulse is supplied for this purpose to the grid of a tube blanked in a quasistable state, causing its "premature" unblanking.* But, hence it follows that synchronizing generator circuit parameters must be selected so that the period of its inherent self-excited oscillations (without /334 synchronization) mandatorily somewhat exceeds the period of forced oscillations:

$$T_0 > T_1 = K_1 T_c. \qquad \text{(VIII.1)}$$

Usually, $T_0 = (1.2\text{--}1.5) T_1$ (pulses which would be produced by the generator with the inherent frequency are depicted by the dotted line in Figure VIII.1).

Self-excited oscillator forced reversal occurs with each sync pulse for synchronization on the basic frequency. The circuit reverses in the frequency division mode only with each k-th pulse and does not react to the remaining (intermediate) pulses. It may be said that, in this event, synchronization occurs with periodic "passes" of series of k—1 pulses (sync pulses 1 and 2, 4 and 5, and so forth "are passed" in Figure VIII.1c, for instance). This occurs in the following manner.

As is known, self-excited oscillator blanked tube negative grid voltage gradually rises by the law of exponents (see Figures VI.27 and VII.7, for instance). Thus, it is possible to select a sync pulse amplitude U_c so that it turns out to be insufficient for unblanking the tube with the (k—1)-th pulse, when grid voltage still is too negative (and, consequently, particularly with the 1-st, 2-d. . . (k—2)-th pulses), but sufficient for unblanking the tube with the k-th pulse,

*The identical principle was used for forced monostable multivibrator and blocking oscillator cutoff (Chapter VI, § 3).

when this voltage succeeds in approaching the cutoff voltage level by a magnitude less than $U_{\text{г}}$. It is evident that this condition is satisfied more easily, the greater the grid voltage increment during the sync pulse period, i. e., the higher the rate of change of the grid voltage rise. Here, frequency division stability increases since requirements decrease for stability of both sync pulse amplitude and of the operating mode of the self-excited oscillator itself. Therefore, multivibrators and retarding- field blocking oscillators usually are used for frequency division (Chapter VI, § 4, Chapter VII, § 3).

The same methods that were used to trigger monostable circuits (it is possible, for example, to synchronize a blocking oscillator with positive pulses supplied to the plate network and to synchronize a multivibrator with negative pulses supplied to grid of an unblanked or plate of a blanked tube) are used to supply positive sync pulses to grid of a blanked self-excited oscillator tube in the quasistable state.

Monostable blocking oscillators and multivibrators, as well as flip-flops, also may be used for frequency division. The special operating features of these dividers will be examined below.

In any event, it is difficult to obtain stable frequency division by a factor of more than 5—10 with the aid of one oscillator-divider (K_3 always equals 2 for a flip-flop). Several dividers are connected in series when there is a /335 requirement for a large number of frequency division multiples. Here, each subsequent divider is synchronized (and is triggered in the event monostable circuits or flip-flops are used) by the pulses from the preceding divider's output. The resultant scaling factor is compared to the product of the scaling factors of all the dividers within the circuit.

Synchronization and frequency division using tube circuits are examined below. Synchronization and frequency division using transistor circuits are based on identical principles.

§ 2. BLOCKING OSCILLATOR SYNCHRONIZATION

A standard synchronizing blocking oscillator circuit is depicted in Figure VIII.2. The process of blocking oscillator synchronization on the basic frequency

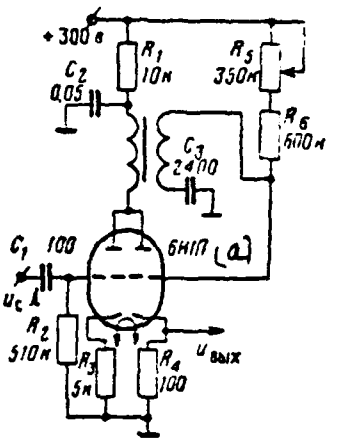

Figure VIII.2. Blocking Oscillator in the Synchronization Mode.
(a) -- 6N1P.

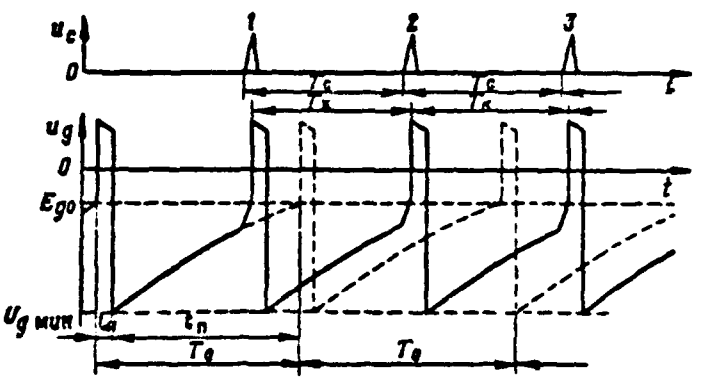

Figure VIII.3. Blocking Oscillator Synchronization on the Basic Frequency.

is explained in Figure VIII.3, while three-to-one frequency demultiplication is explained in Figure VIII.4. For clarity, the shape of the positive sync pulses is accepted as being square, while blocking oscillator grid voltage is depicted without stray excursions and oscillations. The law of change for this voltage if no sync pulses are supplied to the circuit is depicted by the dotted line.

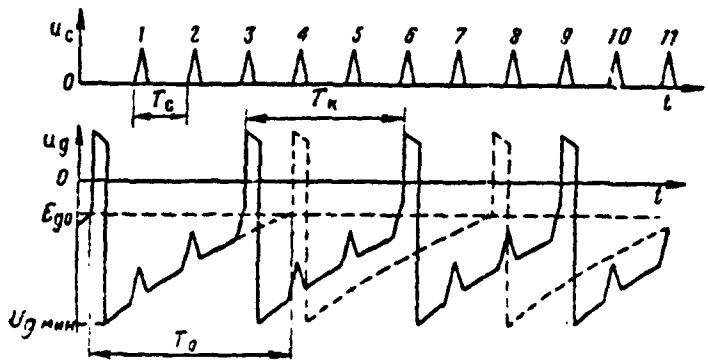

Figure VIII.4. Frequency Division Using a Blocking Oscillator ($K_1 = 3$).

In the first case, when each sync pulse is active, resultant grid voltage exceeds the cutoff voltage level $(u_c + U_C > E_{go})$, the tube unblanks, and forced circuit reversal occurs. In the second example, there is synchronization only with every third pulse since the tube remains blanked while the first two pulses are active.

EXERCISE VIII.1

Determine the maximum scaling factor which may be obtained with the aid of the Figure VIII.2 circuit if E_{go} = -10 V, $U_{g\,мин}$ = -50 V, and sync pulses with frequency F_c = 10 kHz are supplied to circuit input. (Page 489)

In general form, we will establish conditions insuring K_1 -to-one frequency demultiplication. We will assume for simplified discussion that:

-- steps in the circuit occur instantaneously;

-- the duration of the pulse shaped by the blocking oscillator is infini- 336
tesimally slight compared with the period of the inherent oscillations ($t_и \ll T_0$), i. e., there are no time intervals when the blocking oscillator would not be subjected to synchronization;

-- negative grid voltage during resting times rises according to a linear law.

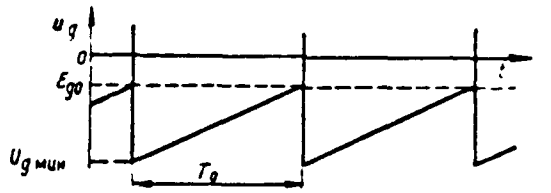

Figure VIII.5. Blocking Oscillator Grid Voltage Idealized Shape.

The idealized shape of blocking oscillator grid voltage is depicted in Figure VIII.5 and corresponds with sufficient precision to the true shape for a retarding-field blocking oscillator operating with high duty ratio $Q = \frac{T_0}{\tau_u} \gg 1$ In addition, it should be considered that sync pulse duration is infinitesimally small compared /337 to their pulse spacing T_c.

The idealized law of voltage u_g change for one oscillation period T_0 and the sync pulses travelling with spacing T_c applied to this voltage are depicted

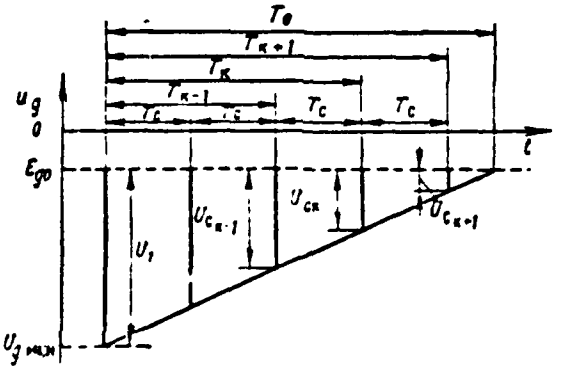

Figure VIII.6. Minimum Sync Pulse Amplitudes at Blocking Oscillator Grid.

in Figure VIII.6. The varied amplitude of these pulses is selected from condition $U_c = |u_g - E_{g0}|$, i. e., is minimally necessary for tube unblanking. In actuality, all sync pulses have identical amplitude. The amplitude of each pulse depicted in Figure VIII.6 should be understood as the minimum amplitude of all pulses during

which synchronization will be insured by this particular (not the previous and not the subsequent) pulse.

$K_д$ -to-one frequency demultiplication will occur if synchronization occurs with the k-th sync pulse (here, forced pulse spacing will equal $T_k = K_д T_c$). But, this requires that sync pulse amplitude at least equal value U_{ck} (otherwise, synchronization will occur only with the subsequent (k+1)-th pulse) and will /338 be no greater than value $U_{c\,k-1}$ (otherwise, synchronization already will have occurred with the (k—1)-th pulse):

$$U_{c\,k-1} \geqslant U_c \geqslant U_{ck}. \tag{VIII.2}$$

Having divided all the terms of this dual inequality by constant magnitude $|U_{g\,max} - E_{g0}|$ for the given blocking oscillator, we will get

$$\frac{U_{c\,k-1}}{|U_{g\,max} - E_{g0}|} \geqslant \frac{U_c}{|U_{g\,max} - E_{g0}|} \geqslant \frac{U_{ck}}{|U_{g\,max} - E_{g0}|}.$$

But, from the similarity of triangles with corresponding legs $U_{c\,k-1}$ and $U_c = |U_{g\,max} - E_{g0}|$

$$\frac{U_{c\,k-1}}{|U_{g\,max} - E_{g0}|} = \frac{T_0 - T_{k-1}}{T_0} = 1 - (K_д - 1)\frac{T_c}{T_0},$$

and, from the similarity of triangles with corresponding legs U_{ck} and U_1

$$\frac{U_{ck}}{|U_{g\,max} - E_{g0}|} = \frac{T_0 - T_k}{T_0} = 1 - K_д \frac{T_c}{T_0}.$$

Therefore, in final form, $K_д$ -to-one frequency demultiplication condition (VIII.2) may be written

$$1 - (K_д - 1)\frac{T_c}{T_0} \geqslant \frac{U_c}{|U_{g\,max} - E_{g0}|} \geqslant 1 - K_д \frac{T_c}{T_0}. \tag{VIII.3}$$

In accordance with (VIII.3) in generalized coordinates $\frac{T_c}{T_0}$ and $\frac{U_c}{|U_{g\,max} - E_{g0}|}$, the graph of the synchronization zone for various $K_д$ values is depicted in Figure VIII.7. The graph is plotted based on the following circumstances. The left term of inequality (VIII.3) is an upper bound equation and the right term is a lower bound equation of the synchronization zone for a given $K_д$ value. The lower bound of each zone simultaneously is the upper bound of the subsequent zone for

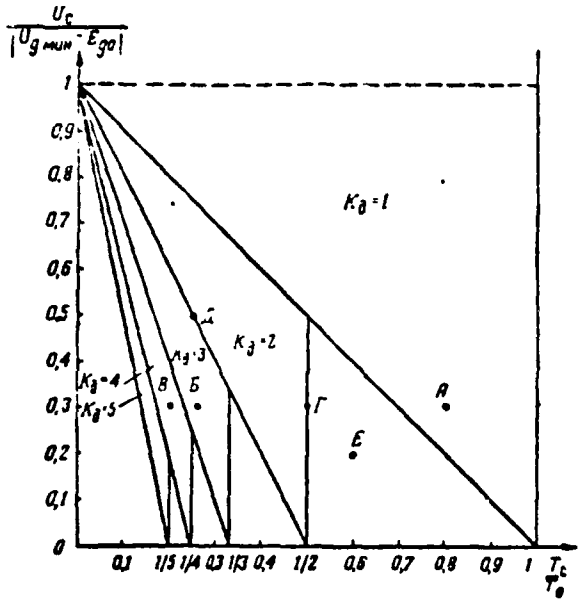

Figure VIII.7. Blocking Oscillator Synchronization Zones.

a value greater by unity of $K_д$: $1 - K'_д \frac{T_c}{T_0} = 1 - (K'_д + 1 - 1)\frac{T_c}{T_0}$. Zone bounds (with the exception of the upper bound of the zone for $K_д$ = 1) are sloping line segments. Assuming $\frac{T_c}{T_0} = 0$, in the equation for any bound, we will find that all bounds pass through point $\frac{U_c}{|U_{g\,min} - E_{g0}|} = 1$ on the Y-axis. Assuming $1 - K_д \frac{T_c}{T_0} = 0$, for a lower bound equation, we find that the lower bound of every zone passes through point $\frac{T_c}{T_0} = \frac{1}{K_д}$ on the X-axis. If $\frac{T_c}{T_0} > \frac{1}{K_д}$, then /339 $T_c = K_д T_c > T_0$, which will contradict the basic synchronization condition (VIII.1); here, $K'_д$-to-one frequency demultiplication will become impossible regardless of values $\frac{U_{g\,min} - E_{g0}}{U_{g\,min} - E_{g0}}$ since the k-th pulse will arrive after spontaneous circuit reversal already has occurred. Consequently, each zone is bounded on the right by vertical line $\frac{T_c}{T_0} = \frac{1}{K_д}$. The upper bound for the zone where $K_д$ = 1 is depicted on the graph by a dotted line and is conditional. Actually, this bound corresponds in Figure VIII.6 to amplitude $U_c = U_1$ during which the circuit will be reversed

by the first pulse, regardless of the moment of its arrival. But, the same thing also will occur all the more so given even greater sync pulse amplitude $U_c > U_1$, i. e., $\frac{U_c}{|U_{g\,min} - E_{go}|} > 1$. However, too great a sync pulse amplitude where $K_2 = 1$ may impact adversely on circuit operation.

The coordinates of all points falling within a given zone correspond to values $\frac{U_c}{|U_{g\,min} - E_{go}|}$ and $\frac{T_c}{T_0}$ during which K_2-to-one frequency demultiplication /340 will occur. Thus, for example, the curves depicted in Figure VIII.3 ($K_2 = 1$) correspond to point A $\left(\frac{T_c}{T_0} = 0{,}8;\ \frac{U_c}{|U_{g\,min} - E_{go}|} = 0{,}3\right)$, while the curves depicted in Figure VIII.4 ($K_2 = 3$) correspond to point Б $-\left(\frac{T_c}{T_0} = 0{,}25;\ \frac{U_c}{|U_{g\,min} - E_{go}|} = 0{,}3\right)$.

Most stable frequency division results at points which are centers of the circles inscribed in each zone, i. e., equidistant from all zone bounds (in this case, division of a frequency into the given number of multiples is retained during the greatest stray changes of values U_c, $U_{g\,min}$, E_{go}, T_0, T_c).

It is evident from the synchronization zone graph that an increase in K_2 means a reduction in division stability since the area of the zones is reduced. Therefore, in practice, it is difficult using a blocking oscillator to obtain a scaling factor exceeding $K_2 \approx 10 \div 15$.

EXERCISE VIII.2

Draw the sync pulse train and blocking oscillator grid voltage curves idealized in accordance with Figure VIII.5 for points В, Г, Д, Е depicted in Figure VIII.7. Explain the division process in each instance. Disregard sync pulse duration in all instances and use fixed values T_0, E_{go}, and $U_{g\,min}$ (identical blocking oscillators are used). (Page 489)

§ 3. MULTIVIBRATOR SYNCHRONIZATION

In principle, the multivibrator synchronization process is similar to the blocking oscillator synchronization process and usually is accomplished by supplying positive sync pulses to grid of one of the multivibrator tubes.

A typical synchronized multivibrator circuit is depicted in Figure VIII.8. A free-running multivibrator, as opposed to a blocking oscillator, operates with a relatively-low duty ratio ($Q \lesssim 100 \div 200$). Therefore, it is impossible with

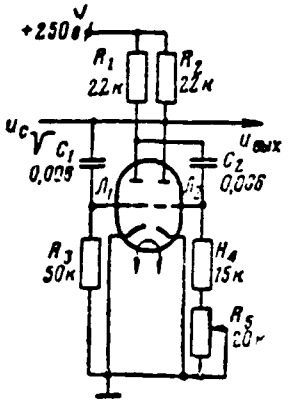

Figure VIII.8. Multivibrator in the Synchronization Mode.

a multivibrator to disregard a portion of the self-oscillation period, when a given tube is unblanked, i. e., the multivibrator will not be subjected to synchronization.

The solid line in Figure VIII.9 depicts the idealized law of grid voltage change for one multivibrator tube for one period of inherent oscillations $T_o = T_{o1} + T_{o2}$, as well as the sync pulses applied to this voltage with the minimum amplitude of each pulse required for synchronization $U_c = |u_g - E_{go}|$. The addition shown by a dotted line brings the picture to Figure VIII.6 for a case of very high duty ratio (blocking oscillator synchronization). However, sync pulses which arrived at interval T_{o1} (they also are shown by a dotted line) in reality may not reverse the circuit regardless of their amplitude since the given multivibrator tube is unblanked at that interval. Consequently, multivibrator frequency division may be obtained not only by "passage" of pulses of insufficient amplitude arriving at interval T_{02}, but also by "passage" of pulses of any amplitude arriving at interval T_{o1}.

EXERCISE VIII.3

Draw the sync pulse train and voltage u_{g2} and $u_{a_1} - u_{g_2}$ curves and determine

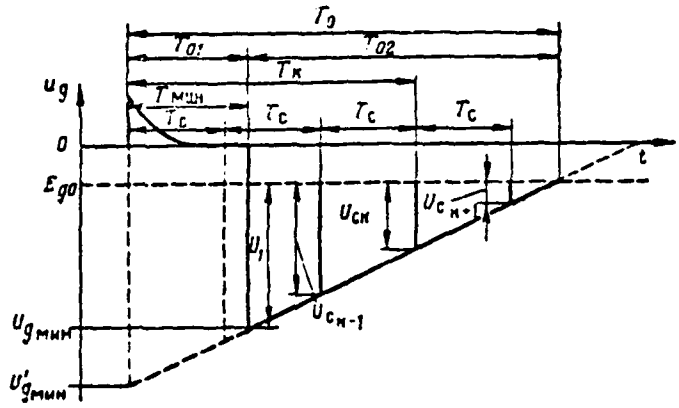

Figure VIII.9. Minimum Sync Pulse Amplitudes at Multivibrator Grid.

scaling factor K for the Figure VIII.8 multivibrator circuit if control R_5 is in the middle position $T_c = \frac{T_0}{2}$, while pulse amplitude U_c is sufficient for circuit reversal at any moment in time. Assume as you plot the curves that sync pulses begin to act only from the second circuit oscillation period. (Page 491)

A graph of multivibrator synchronization zones is depicted in Figure VIII.10 and is plotted based on the following considerations. We will plot the synchronization zone for a case of very high duty ratio, initially just as we did in Figure VIII.7, in generalized coordinates $\frac{T_c}{T_0}$ and $\frac{U_c}{U_{g\,мин} - E_{g0}}$, where $U_{g\,мин}$ /342 -- fictitious value for minimum grid voltage shown in Figure VIII.9. Next, we will consider that, since synchronization actually is impossible at time interval T_{01}, the forced oscillation period is bounded by condition $T_c = K_1 T_c \geq T_{мин} = T_{01}$. Hence, we will get

$$\left(\frac{T_c}{T_0}\right)_{мин} = \frac{1}{K_1 T_c}. \qquad \text{(VIII.4)}$$

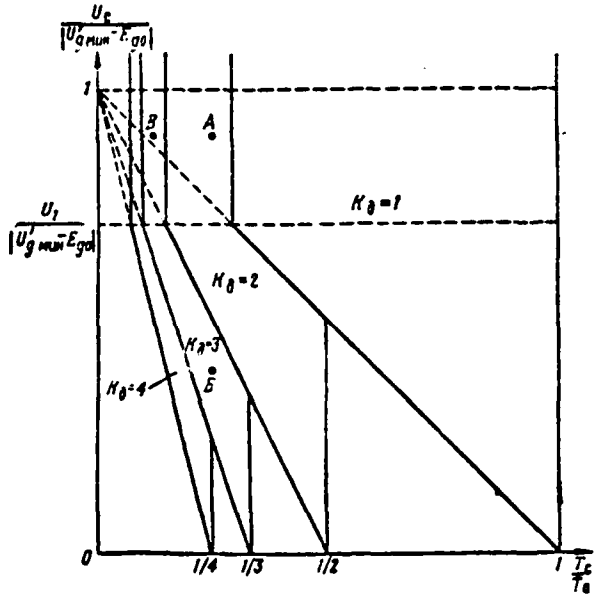

Figure VIII.10. Multivibrator Synchronization Zones.

This condition additionally constrains each synchronization zone from the left with a vertical line.

We will find the Y-coordinates of their points of intersection with the zone's previous lower bounds in order to simplify plotting of additional left bounds. We will use the expression for a lower bound from ratio (VIII.3) for this purpose and we will substitute ratio (VIII.4) in it:

$$\left[\frac{U_c}{|U_{g\,min}-E_{g0}|}\right]_{T_c=T_{min}}=1-K_1\left(\frac{T_c}{T_1}\right)_{min}=1-\frac{T_{01}}{T_0}=\frac{T_0-T_{01}}{T_0}=\text{const}$$

But, considering the similarity of the corresponding triangles in Figure VIII.9, we also may write /343

$$\left[\frac{U_c}{|U_{g\,min}-E_{g0}|}\right]_{T_c=T_{min}}=\frac{T_1-T_2}{T_1}=\frac{T_{12}}{T_1}=\frac{U_1}{|U_{g\,min}-E_{g0}|}=\text{const}, \qquad \text{(VIII.5)}$$

where $U_1=|U_{g\,min}-E_{g0}|$ -- largest minimum pulse amplitude realistically required for multivibrator synchronization.

Thus, all zone left bounds intersect lower bounds at the identical level, which does not depend on the K_3 value. The vertical bands formed above this level for all zones (except the zone for $K_3 = 1$) correspond to frequency division due to change $K_3 - 1$ of sync pulses at interval T_{01}. The dotted line plotted at level $\frac{U}{U_{g\,max} - E_{gc}} = 1$ is only the conditional upper bound of all zones since the synchronization mode does not change when the amplitude of these pulses rises.

This method of multivibrator synchronization with pulses supplied to grid of one tube provides synchronization only of the oscillation period. Inherent circuit parameters determine the magnitude of interval T_{01}, when the given tube remains unblanked. It is possible to supply negative sync pulses simultaneously to both multivibrator grids (just as during symmetrical flip-flop triggering) when there is a requirement also to synchronize this part of the period. The unblanked tube amplifies and inverts these pulses and they then are supplied to unblanked tube grid, each time causing forced circuit reversal.

EXERCISE VIII.4

Draw the sync pulse train and multivibrator grid voltage curves for points *A, B,* depicted in Figure VIII.7. Assume that values T_0, T_{01}, E_{go}, and $U_{g\,max}$ for all cases are constant and that $\frac{U}{U_{g\,max} - E_{gc}} = 0.8$. (Page 492)

§ 4. FREQUENCY DIVISION USING MONOSTABLE BLOCKING OSCILLATORS AND MULTIVIBRATORS

Use of monostable circuits for frequency division is based on the fact that a monostable circuit turns out to be insensitive to trigger pulse stimulus for a certain time following triggering. The interval of insensitivity equals the sum of the time the circuit remains in a quasistable state and a part (for a blocking oscillator) or all (for a multivibrator) of the time needed to reestablish the circuit to an equilibrium state.

The frequency division process when a monostable blocking oscillator /344 is used is explained in Figure VIII.11. Positive trigger pulses are supplied to blocking oscillator tube grid. The circuit is triggered by the first pulse and produces a pulse whose duration t_u is determined by blocking oscillator inherent parameters. The circuit does not react to the next k—1-th trigger pulses

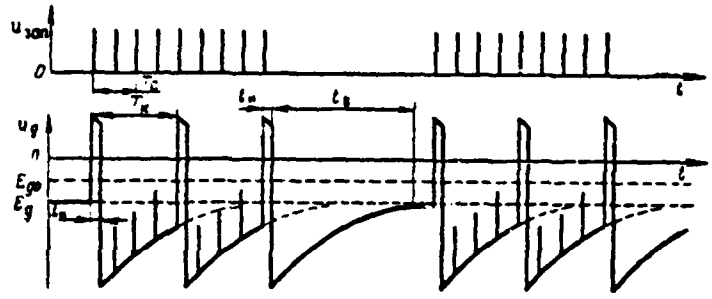

Figure VIII.11. Frequency Division Using a Monostable Blocking Oscillator ($K_д$ = 4)

and only the k-th pulse again induces a circuit reversal. Thus, frequency division using a monostable blocking oscillator occurs in a manner identical to that using a free-running blocking oscillator. The only exception is that the monostable blocking oscillator will be in an equilibrium state (its tube is blanked by negative bias E_g) prior to arrival of the first and after arrival of the last pulse and does not produce any pulses. Therefore, a monostable blocking oscillator is used, for example, when trigger pulses, as depicted in Figure VIII.11, are supplied in the form of individual series (packets) and there is a requirement for division of the pulse repetition frequency within each series. Negative grid voltage in a monostable blocking oscillator upon completion of a counter reversal will strive toward value E_g, which is not the case with a free-running circuit. Therefore, all other things being equal, trigger pulse amplitude must be greater by magnitude $|E_c - E_{c0}|$ than synch pulse amplitude for a free-running circuit.

The frequency division process using a monostable multivibrator is explained in Figure VIII.12. The multivibrator is triggered by negative pulses stimulating the grid of a tube unblanked in a circuit equilibrium state. This tube blanks after the circuit is triggered by the first pulse and the circuit does not react to the subsequent k—1-th negative pulses. Subsequent triggering will occur with the k-th pulse only after a spontaneous counter reversal and reestablishment of the circuit to the initial equilibrium state. The scaling factor does not change when trigger pulse amplitude changes (just as long as this amplitude is sufficient

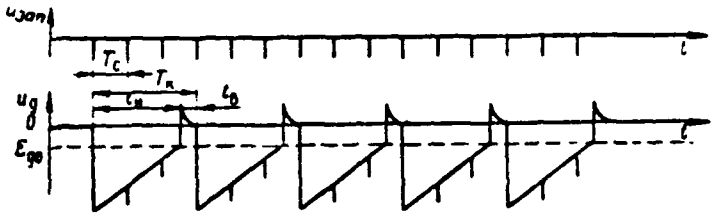

Figure VIII.12. Frequency Division Using a Monostable Multivibrator ($K_д = 3$)

to trigger the circuit). Therefore, higher frequency division stability results than when a multivibrator free-running circuit is used.

EXERCISE VIII.5

What constrains minimum trigger pulse spacing and maximum frequency scaling factor when a monostable multivibrator is used? (Page 493)

Use of monostable circuits also makes it possible to accomplish frequency division in those instances when sync pulse repetition frequency may change, but the scaling factor must remain constant. Step (accumulator) frequency dividers, which are a combination accumulator (capacitance) pulse register and monostable pulse generator, are used to solve this problem.

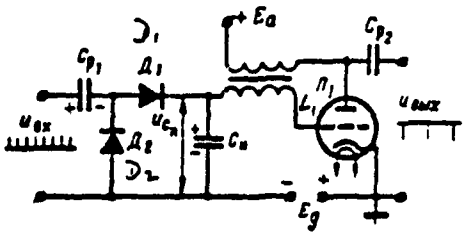

Figure VIII.13. Step Frequency Divider Circuit.

A typical step frequency divider circu[illegible] depicted in Figure VIII.13.

It will comprise an accumulator register made up of diodes D_1, D_2 and capacitors C_p, $C_н$, a blocking oscillator assembled on triode L_1. The curves in Figure

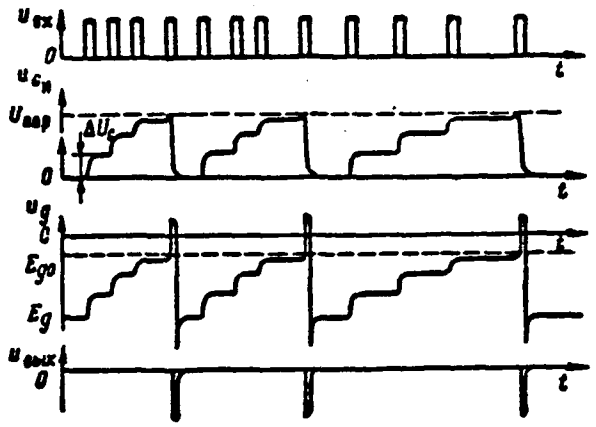

Figure VIII.14. Voltage Curves for a Step Frequency Divider Circuit ($K_1 = 4$).

VIII.14. for scaling factor $K_1 = 4$ explain how the circuit operates.

Positive-polarity input pulses charge coupling capacitor C_p, and reservoir /346 capacitor $C_н$ across diode D_1 resulting in a rise in voltage $u_{C_н}$ by magnitude ΔU_C during the time each pulse is active. Voltage $u_{C_н}$ remains essentially constant during resting times since capacitor $C_н$ may discharge only across stray leakage resistance $R_{ут}$. Capacitor C_p, on the other hand, rapidly discharges completely across diode D_2 and input pulse generator output resistance (diode D_2 functions as a zero lower clamp). Voltage $u_{C_н}$ rises in steps (is accumulated) due to input pulse arrival); voltage $u_g = E_g + u_{C_н}$ rises simultaneously by the same law, but from negative level E_g. Selected circuit parameters are such that voltage $u_{C_н}$ will exceed threshold level $U_{пор}$ at which voltage u_g exceeds cutoff voltage E_{go} when the k-th pulse is active. As a result, the blocking oscillator will be triggered by the k-th pulse and produce pulse $u_{вых}$.

Capacitor $C_н$ during onset of the blocking process will strive to recharge itself with triode grid current. Therefore, it rapidly discharges to zero, after which the grid current network prior to triode blanking closes across diodes D_1, D_2. Thus, the blocking oscillator not only produces output pulses, but also simultaneously insures a voltage "[illegible]", "discharge." Then the circuit operating

cycle is repeated, with the blocking oscillator tripping every time from the k-th pulse regardless of circuit input pulse repetition frequency.

The scaling factor K_c value will depend on amplitude $U_{вх}$, cutoff E_{go} /347 and bias E_g voltages, and the ratios of capacitances C_{p1} and $C_{вх}$ forming the capacitance divider. The height of steps ΔU_c decreases with the arrival of each subsequent pulse prior to blocking oscillator tripping since voltage $u_{C_{вх}}$, stored following the action of the preceding pulse, opposes capacitor charging. Stable circuit operation requires that the height of the k-th step be greater by approximately a factor of 2 than the possible threshold voltage instability. This hinders obtaining a scaling factor exceeding 10.

An increase in K_c requires that the number of stages be increased, i. e., their magnitude decreased, since voltage $u_{C_{вх}}$ in principle may not exceed value $U_{вх}$. Therefore, usually $C_{вх} > C_p$. In addition to this, there is a requirement that capacitors $C_{вх}$ and C_p be charged completely while the pulse is active (here, the amplitude of the k-th step will be maximum). Therefore, the charging time constant must be selected from condition $\tau_з \ll t_и$, which, in turn, requires an insignificant amount of generator output resistance $R_{вых}$. On the other hand, the capacitor $C_{вх}$ discharging time constant must be as large as possible (to satisfy the condition $\tau_р \gg t_{и\,max}$) so that the possible voltage $u_{r_{вх}}$ decrease during resting times will comprise an insignificant part of the magnitude of the k-th step (otherwise, the circuit may not trip). That is why normal leakage resistance R_g is absent from the circuit. This does not impact upon blocking generator operation since the grid current time constant closes across diodes D_1, D_2.

§ 5. FREQUENCY DIVISION AND PULSE COUNT COMPUTATION USING FLIP-FLOPS

Symmetrical flip-flops with symmetrical (counting) triggering with negative pulses are used for frequency division (see Figure VI.12). A flip-flop has two equilibrium states and reverses with each trigger pulse. A flip-flop must be triggered twice in order for one square pulse to be shaped at the plate of one of the flip-flop tubes. Therefore, a flip-flop always will divide trigger pulse repetition frequency only twice. It is important to note that this scaling factor will not depend on trigger pulse amplitude (as long as it is sufficient for reliable flip-flop tripping) and stray mode changes and circuit parameters (only if circuit

reversal conditions and existence of two equilibrium states are satisfied). Therefore, frequency division using flip-flops is the most stable and reliable.

Sequential frequency division using several flip-flops is employed when there is a need to divide a frequency more than twice. Since each flip-flop will /348 divide a repetition frequency twice, then, when n flip-flops are used, the resultant

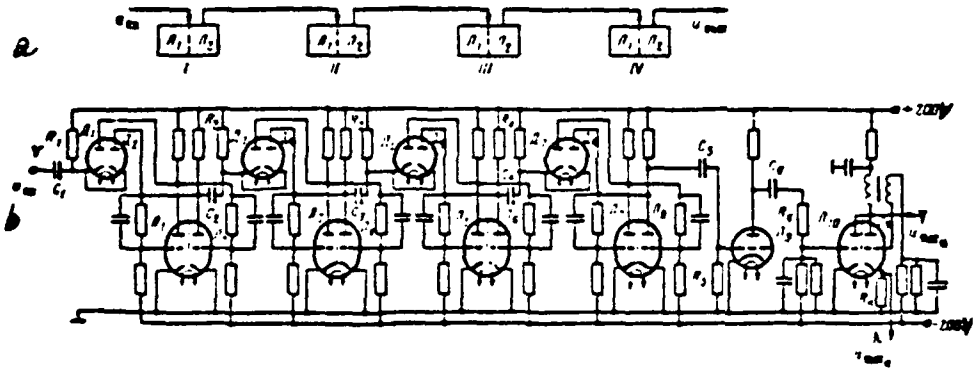

Figure VIII.15. Functional (a) and Schematic (b) Diagrams for a Four Flip-Flop Frequency Divider Where $K_д = 16$.

scaling factor will equal

$$K_д = 2^n. \qquad \text{(VIII.6)}$$

A functional diagram (Figure VIII.15a) and schematic diagram (Figure VIII.15b) of a four flip-flop divider with resultant scaling factor $K_д = 2^4 = 16$. are presented in the form of an example. The curves for the triggering and output voltages of all flip-flops depicted in Figure VIII.16 explain the operation of this circuit.

All flip-flops are assembled on dual triodes ($Л_1$, $Л_2$; $Л_3$, $Л_4$; $Л_5$, $Л_6$; $Л_7$, $Л_8$) and have identical circuits with identical parameters. Negative pulses along a symmetrical trigger circuit trigger all flip-flops across diodes $Д_1$, $Д_2$, $Д_3$,

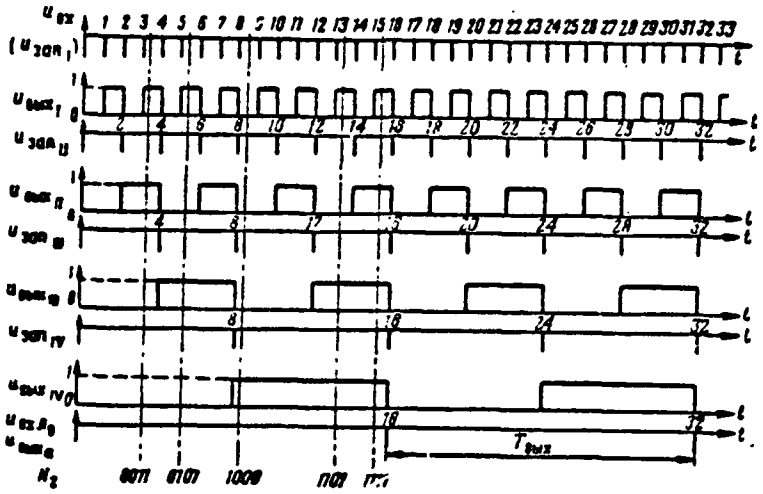

Figure VIII.16. Voltage Curves for the Figure VIII.15 Divider.

D_4, D_5, D_6, D_7, D_8. Negative trigger pulses are supplied across transient network C_1R_1 to first flip-flop input. Each flip-flop output voltage is picked off the right triode plate (L_2, L_4, L_6, L_8) and differentiated by the subsequent flip-flop input R-C network (networks C_2R_2, C_3R_3, C_4R_4). Flip-flop output voltages in Figure VIII.16 for clarity are depicted relative to level $U_{a\,max}$, while only short negative pulse which trigger the subsequent flip-flop are depicted as the result of their differentiation (positive pulses are not depicted since they cannot symmetrically trigger a flip-flop). Network C_5R_5 differentiates fourth flip-flop output voltage and it is supplied to an amplifier assembled on triode L_9. Positive pulses arising in this triode's plate network trigger a monostable blocking oscillator assembled on triode L_{11} across transient network C_6R_6 and trigger triode L_{10}. The blocking oscillator produces output pulses coinciding with the last flip-flop output voltage drop. Divider output pulses may be picked off the blocking oscillator plate network and cathode load impedance R_k.

It follows from the Figure VIII.16 curves that the first flip-flop will divide input pulse repetition frequency twice, the first two flip-flops 4 times, the first three flip-flops 8 times, and all four flip-flops 16 times. We will note

that divider output pulses are produced at the moment of simultaneous unblanking of the output tubes of all flip-flops.

Series flip-flop connection is used also to count the number of input pulses in the binary computational system. An number N in a binary system is represented by the sum of the powers of the digit 2 (the foundation of this system) in the form

$$N = \sum_{i=1}^{m} a_i 2^{i-1} = a_m 2^{m-1} + a_{m-1} 2^{m-2} + \ldots + a_3 2^2 + a_2 2^1 + a_1 2^0. \qquad \text{(VIII.7)}$$

where i -- position number; m — quantity of positions required to represent a /350 given number; a_i -- factors, each assigned one of two values, 0 or 1.

The values of coefficients a_i are successive when representing a number, while coefficients 2^{i-1} are in descending order. For example, the digit 2 is written in the form 10 ($1 \times 2 + 0 \times 2^0$), the digit 5 in the form 101 ($1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0$), the digit 14 is written in the form 1110 ($1 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 0 \times 2^0$), and so forth. Thus, any number in a binary system is written using only the digits 0 and 1. Meanwhile, the two possible flip-flop equilibrium states correspond to these two digits.* We will use "1" for that flip-flop equilibrium state in which its output voltage is maximum (output tube blanked), and use "0" for its second equilibrium state, when flip-flop output voltage is minimum (output tube unblanked).

All flip-flops in the Figure VIII.15 circuit will switch from state "0" to state "1" and back due to input pulse arrival. But the first flip-flop trips from every input pulse, the second flip-flop from every second pulse, the third flip-flop from every fourth pulse, and the fourth flip-flip trips from every eighth pulse. Therefore, in expansion of (VIII.7) for the number of the input pulse, the state of the first flip-flop determines the quantity of unities of the /351 first (least significant) digit, i. e., it shows whether or not term 2^0 will be maintained in this expansion; the state of the second flip-flop determines the quantity of unities of the second digit, i. e., indicates whether or not term 2^1 will be maintained in this expansion, and so on.

*Therefore, a flip-flop is referred to as a binary element in computer technology.

Consequently, if, for a given moment in time, the states of all flip-flops, beginning with the last and ending with the first (in descending order of digits), are written successively using the digit 0 or 1, we will have a *binary record* of the number of input pulses N which had arrived at the circuit by that moment in time. For example, in Figure VIII.16, flip-flop states upon arrival of the third pulse are represented as 0011 (3), upon arrival of the fifth pulse -- 0101 (5), upon arrival of the eighth pulse -- 1000 (8), and so forth. Since there are four flip-flops in the circuit being examined, then the maximum number of pulses which it may calculate equals the greatest number which is represented in binary code with four digits N_{max} = 1111 (15). The 16-th pulse will convert the circuit to initial state 0000 and the count begins anew.

Essentially, NIXIE tubes connected to each flip-flop output tube plate may be used to indicate flip-flop states in order to count the number of pulses.

EXERCISE VIII.6

What will be the scaling factor for a circuit comprising six sequentially-operating flip-flops? How many pulses will this circuit be able to count? (Page 493)

§ 6. SEVERAL COMPLEX FREQUENCY DIVIDER CIRCUITS

1. Dividers With Feedback

Feedback is used in dividers if it is impossible to obtain the requisite scaling factor by using several sequential monostable circuits or flip-flop divider stages as a result of multiplying the possible scaling factors of each stage together (i. e., expanded to the corresponding multipliers): $K_1 = K_{11}K_{12} \ldots K_{1n}$.

The principle of using feedback in dividers involves divider output pulses being supplied to several specially-selected preceding divider stages and causing their out-of-sequence (premature) triggering. But, out-of-sequence tripping of any stage under the stimulus of an output pulse leads to all subsequent stages also tripping accordingly earlier than is the case for normal circuit operation without feedback. Here, the circuit's subsequent output pulse, which again acts upon the stages enveloped by feedback, also will appear correspondingly earlier,

and so forth. As a result, divider output pulse repetition frequency will be reduced, i. e., the circuit scaling factor will decrease. It is possible to shorten "normal" circuit operating rhythm in which the assigned scaling factor value /352 will result through selection of the number of stages which must be enveloped by feedback.

We will examine use of feedback in flip-flop dividers, which have the greatest division stability. As we know, such dividers without use of feedback will divide a pulse repetition frequency 2^n times, where n -- number of flip-flops, and count the pulses in a binary system. Let the requirement be to obtain scaling factor $K_1 = 2^n$, while $2^n > K_1 > 2^{n-1}$. It is evident from the outset that solution of this problem requires use of n flip-flops (the n—1-th flip-flop will provide scaling factor $2^{n-1} < K_1$). But, it is necessary through use of feedback to reduce the scaling factor by $2^n - K_1$ unities, i. e., to bring about an artificial shift of the pulse count by this magnitude, in order to reproduce every k-th pulse at circuit output.

Which flip-flops should be enveloped in feedback for their out-of-sequence reversal ("malfunction") by output pulses? It is evident from examination of the divider operation in Figure VIII.16 that a "malfunction" of the first flip-flop will provide a count shift by 1 (2^0), a "malfunction" of the second flip-flop by 2 (2^1), "malfunction" of the third flip-flop by 4 (2^2), and so on. Therefore, if digit $2^n - K_1$ is written in the binary system, then the presence in this notation of a unity of the lowest order will impact upon the requirement for a "malfunction" of the first flip-flop, presence of a unity of the next higher order digit on the necessity for "malfunction" of the second flip-flop, presence of a unity of the next highest order digit on the necessity for a "malfunction" of the third flip-flop, and so forth.

Output pulses must reverse the flip-flops to which they are supplied along the feedback network only in one direction -- from equilibrium state "0," when output tubes are unblanked, to equilibrium state "1," when output tubes are blanked.* Therefore, asymmetrical circuits for triggering across output (unblanked) tubes

*We will recall that output pulses are produced at the moment of simultaneous unblanking of the output tubes of all flip-flops (see Figure VIII.16).

usually are used for flip-flop "malfunction." "Malfunction" pulses must be delayed somewhat relative to the regular trigger pulses supplied to these flip-flops from the output of the preceding flip-flops in order to insure initially regular, and then irregular, reversal of flip-flops enveloped by feedback. Flip-flop resolving time (see Chapter VI, § 2) determines requisite delay time and, by connection to the feedback network, creates a delay line or R-C integrator. However, it is possible to do without a special delay device since the natural stray output pulse delay accumu[illegible]ng due to finite triggering time and flip-flop reversal suffices.

We will examine as our example how to use flip-flops to obtain scaling /353 factor $K_д = 9$. Since $2^4 > 9 > 2^3$, then the required flip-flop number $n = 4$. Next, we will find the required scaling factor decrease (pulse count shift), which feedback must insure: $2^4 - 9 = 7$, and we will write this number in the binary system: 0111. It follows from this that obtaining $K_д = 9$ means supplying delayed output pulses ("malfunction" pulses) along the feedback network to the first, second, and third flip-flops.

The corresponding divider functional diagram and its voltage curves are depicted in Figure VIII.17. The first circuit output pulse appears under the stimulus only of the 16-th input pulse. Consequently, until that moment, the feedback network is inoperative and sixteen-to-one sequential frequency demultiplication occurs, while the voltage curves in the circuit in no way differ from the Figure VIII.16 curves. A "malfunction" of the corresponding flip-flops occurs only /354 upon appearance of the 1-st output pulse and a nine-to-one scaling-down process occurs. Therefore, the interval during which the first 16 trigger pulses are supplied determines the rise time of the given division mode, which in general equals

$$t_{вкл.д} = T_{вх} \cdot 2^n. \qquad \text{(VIII.8)}$$

EXERCISE VIII.7

a) Redraw the Figure VIII.15 divider schematic diagram, introducing minimal changes to obtain $K_д = 9$.

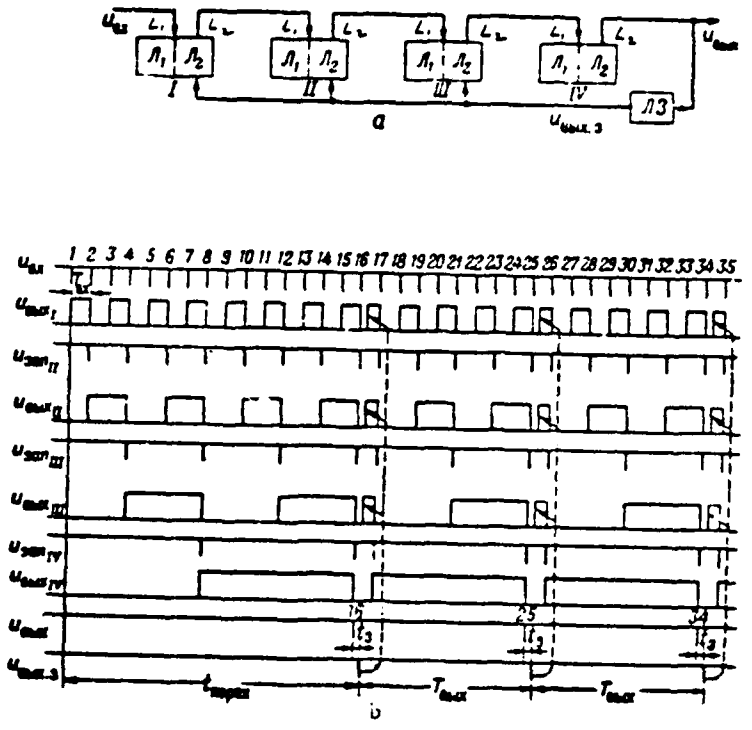

Figure VIII.17. Flip-Flop Frequency Divider Functional Diagram Where $K_д$ = 9 (a) and Its Voltage Curves (b).

b) Determine the scaling factor and draw the voltage curves for the Figure VIII.18a circuits.

c) Determine the scaling factor for the Figure VIII.18b circuits.

d) Compile a divider functional diagram where $K_д$ = 5 and draw the voltage curves for this circuit.

e) Compile a divider functional diagram where $K_д$ = 42. (Page 493)

2. Reference Train Pulse Gating Dividers

Significant output pulse spacing instability arises in multistage frequency

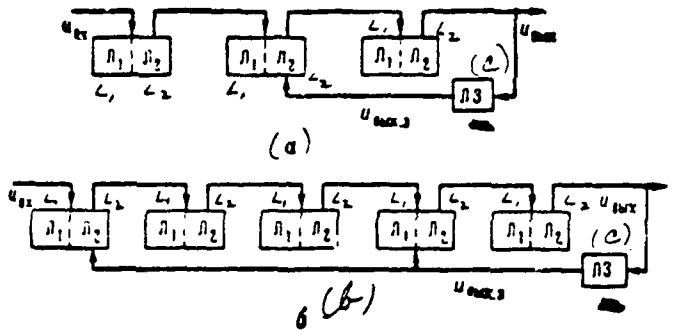

Figure VIII.18. Flip-Flop Frequency Divider Functional Circuits. (c) -- LZ [delay line].

dividers due to stray fluctuations in triggering time and reversal of each stage. This instability essentially may be eliminated through use of reference

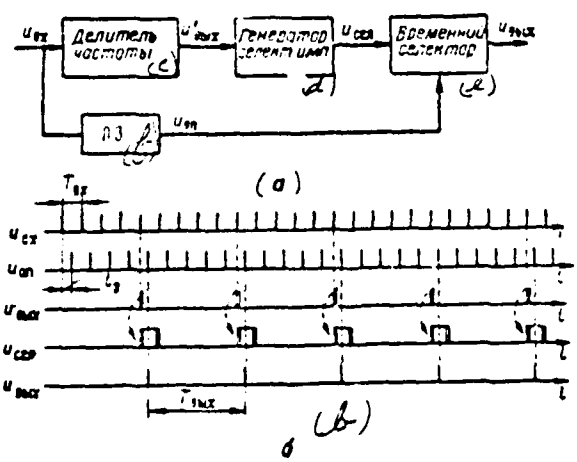

Figure VIII.19. Reference Train Pulse Gating Frequency Divider Functional Circuit (a) and Voltage Curves (b). (c) -- Frequency divider; (d) -- Gate generator; (e) -- Time gate; (f) -- LZ.

train pulse gating dividers. One possible functional circuit for this type divider and its voltage curves are depicted in Figure VIII.19.

The circuit oper rinciple comprises the following. Input pulses are supplied to a multistage frequency divider with assigned value $K_д$ and simultaneously to delay line LZ. Flowing through the delay line, these pulses are delayed by identical time $t_з < \frac{T_{вх}}{2}$. Delayed input pulses are referred to as reference train pulses $u_{оп}$. Divider output pulses $u_{вых}$ with assigned pulse spacing $T_{вых} = K_д T_{вх}$, /355 but possessing time instability, trigger a gate generator. This generator produces gate pulses $u_{сел}$ with duration $t_{сел}$. It is evident that gate pulses also will be unstable over time. Gate and reference train pulses are supplied to a time gate, which is a coincidence circuit and which passes to output only those reference train pulses which coincided with the gate pulses. Thus, the k-th reference train pulses rather than divider output pulses are used as the circuit output signal. Divider and gate generator instability will have no impact whatsoever on the time position of these pulses.

EXERCISE VIII.8

Point out the basic circumstances behind selection of reference train delay time $t_з$ and gate pulse duration $t_{сел}$. (Page 495)

CHAPTER IX /356

SAWTOOTH (LINEARLY-CHANGING) VOLTAGE GENERATORS

§ 1. GENERAL INFORMATION ON SAWTOOTH GENERATORS

1. Sawtooth Voltage Parameters and Acquisition Principles

Voltages which at given time intervals change at constant rate $\left(\frac{du}{dt} = \text{const}\right)$ are referred to as sawtooth or linearly-changing voltages. Sloping line segments graphically reflect the shape of the voltages at these intervals. In essence, the passage of time is modelled electrically with the aid of sawtooth voltages. Therefore, they are used widely in RLS pulse devices, either for linear control over time of electrical processes (to create cathode ray tube [CRT] beam sweeps linear over time, for example) or for linear conversions of electrical magnitudes into time intervals (to obtain pulse variable time delay and pulse signal time modulation and demodulation, for instance).

A sector of linear voltage change is referred to as a working or forward stroke. A sector of voltage recovery to the intitial level upon completion of a working stroke essentially is not used and is referred to as flyback. Flyback shape is slight, but its duration must, as a rule, be as small as possible.

Sawtooth voltage is referred to linearly-rising or linearly-falling, depending on whether it rises or falls during a working stroke.

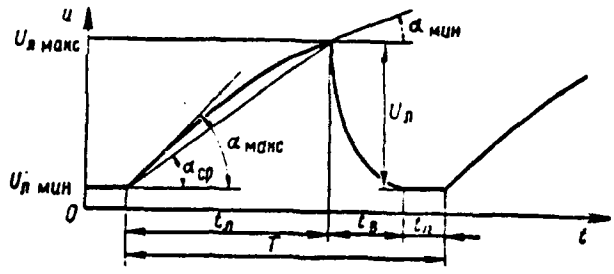

Figure IX.1. Sawtooth Voltage Parameters.

The following parameters characterize sawtooth voltage (Figure IX.1):

-- linear sector (working stroke) duration $t_л$;

-- recovery time (flyback duration) $t_в$;

-- resting time $t_п$; /357

-- change (repetition) cycle $T = t_л + t_в + t_п$;

-- linear sector amplitude (saw amplitude) $U_л = U_{л\ макс} - U_{л\ мин}$;

-- average rate of change during a working stroke (saw slope)

$$\overline{V} = \frac{U_л}{t_л} = \operatorname{tg} \alpha_{ср}, \tag{IX.1}$$

-- nonlinearity factor

$$\gamma_н = \frac{\left(\frac{du_л}{dt}\right)_{макс} - \left(\frac{du_л}{dt}\right)_{мин}}{\left(\frac{du_л}{dt}\right)_{макс}} = \frac{\operatorname{tg} \alpha_{макс} - \operatorname{tg} \alpha_{мин}}{\operatorname{tg} \alpha_{макс}}, \tag{IX.2}$$

where $\left(\frac{du_л}{dt}\right)_{макс} = \operatorname{tg} \alpha_{макс}$; $\left(\frac{du_л}{dt}\right)_{мин} = \operatorname{tg} \alpha_{мин}$ -- maximum and minimum rate of sawtooth voltage change, respectively, during a working stroke.

Nonlinearity factor (IX.2) indicates the relative magnitude of the rate of sawtooth voltage change (slope) during a working stroke. The smaller the $\gamma_н$ value, the closer the law of voltage change is to the linear. $\left(\frac{du_л}{dt}\right)_{макс} = \left(\frac{du_л}{dt}\right)_{мин} = \frac{du_л}{dt} = \overline{V} = \text{const}$ and $\gamma_н = 0$ for ideally-linear voltage. Realistically, always $\gamma_н > 0$.

It is desirable, along with the requirements for sawtooth voltage linearity,

for its amplitude $U_{s.}$ to be as large as possible. In principle, however, this amplitude may not exceed circuit supply source voltage E_a. In that sense, the supply source voltage utilization factor determines sawtooth generator efficiency

$$\xi_a = \frac{U_s}{E_a} (\xi_a < 1). \tag{IX.3}$$

Sawtooth voltage is shaped in the majority of sawtooth generator (GPN) /358 practical circuits in a capacitor as it charges (discharges, recharges) across a resistance. Thus, R-C integrator processes (see Chapter II, § 3) are used to obtain sawtooth voltage and only the initial, most linear exponential voltage sector is used as a working stroke of a sawtooth voltage. Therefore, the following inequality is a condition for obtaining a working stroke of high linearity (II.26)

$$t_1 \ll \tau_1 \quad \text{or} \quad \frac{t_1}{\tau_1} \ll 1, \tag{IX.4}$$

where τ_1 -- R-C network time constant for the process (capacitor charging, discharging, or recharging), which is used to shape the working stroke.

Consequently, a working stroke must be shaped during partial capacitor charging (discharging, recharging), when the voltage in it still is relatively unchanged from its initial value. Therefore, a contradiction always exists between the requirements for obtaining sawtooth voltage of high linearity and of great amplitude. The higher the linearity, the less the amplitude U_s.

Capacitor voltage must be reestablished to the initial value during recovery (flyback) $t_в$. Therefore, in accordance with (XI.15)

$$t_в \approx 3\tau_в. \tag{IX.5}$$

where $\tau_в$ -- R-C network time constant for a process during which flyback shaping occurs.

The simplest equivalent circuit to which any generator of linearly-changing voltage may be reduced is depicted in Figure IX.2a. This circuit includes an

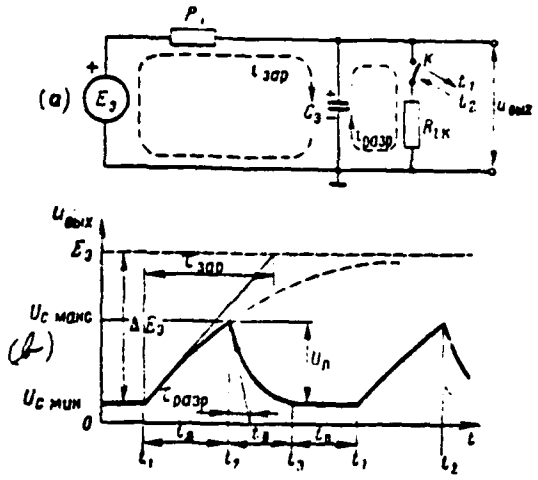

Figure IX.2. General Equivalent Circuit of a Linearly-Rising Voltage Generator (a) and Its Output Voltage (b).

integrator with equivalent parameters $R_э C_э$, equivalent constant voltage source $E_э$, and switching element -- switch K with internal resistance $R_{iк}$. Actual circuit output voltage is depicted in Figure IX.2b. The circuit operates in the following manner.

We will assume that switch K was closed in the initial state ($t < t_1$) and minimum voltage equal to the voltage drop across resistance $R_{iк}$ was established in the capacitor: $U_{c\,мин} \approx \frac{E_э}{R_э + R_{iк}} R_{iк}$. The switch opens at moment t_1 and capacitor $C_э$ charges from source $E_э$ across resistance $R_э$. Here, capacitor voltage rises along an exponential curve with time constant $\tau_{зар} = \tau_1 \approx R_э C_э$, striving towards value $E_э$. However, at moment t_2, long before the charging process ceases, the switch closes and the capacitor discharges across resistance $R_{iк}$. Here, capacitor voltage drops from maximum value $U_{c\,макс}$ achieved by moment t_2 during the charging process along an exponential curve with time constant $\tau_{разр} = \tau_2 \approx R_{iк} C_э$ initial value $U_{c\,мин}$. The circuit is in the initial state when discharge is complete and the processes may be repeated for shaping of the subsequent "saw tooth." Thus, the working stroke of a linearly-rising voltage is shaped during partial charging of the capacitor, when switch K is open ($t_1 = t_2 - t_1 < \tau_{зар}$); flyback (circuit recovery) occurs during complete capacitor discharge ($t_2 \approx 3\tau_{разр}$). In order to

obtain $t_1 \gg t_н$, when working stroke linearity is high, condition $\tau_{нар} \gg \tau_{нзар}$ must be satisfied, i. e., $R_1 \gg R_{ін}$. In addition, the smaller resistance $R_{ін}$, the less the $U_{C\,мин}$ value, i. e., the greater the saw amplitude $U_п = U_{C\,макс} - U_{C\,мин}$, all other conditions being equal. Therefore, the basic switch requirement is low internal resistance magnitude in the conducting state.

Diodes, triodes (tubes or semiconductor), pentodes, thyratrons, and relay contacts may be used as switches in GPN circuits.

EXERCISE IX.1

Compile an equivalent circuit for a linearly-falling voltage generator, using elements identical to those in Figure IX.2a. Draw the circuit output voltage curve. What ratios must be satisfied in the circuit so that its output voltage parameters are the same as those of the linearly-rising voltage depicted in Figure IX.2b? (Page 495)

There are three basic GPN operating modes, depending on the method of /360 switch control (throwover), in the Figure IX.2a equivalent circuit: external control, monostable (triggering), and free-running. The essence of these modes is explained in Figure IX.3.

The duration of external control pulses $t_п = t_н$ determines the duration of the working stroke (length of time switch K remains in the open state) in the external control mode (Figure IX.3a).

The GPN is triggered by short external pulses (switch K opens due to the action of these pulses) in the monostable (triggering) mode, while processes occurring in the GPN circuit itself determine working stroke duration (i. e., the moment switch K closes)(Figure IX.3b).

The GPN operates free of external stimuli in the free-running mode and processes occurring in the GPN circuit itself determine the moments switch K opens and closes (Figure IX.3c).*

*In essence, the external control mode also is monostable. Therefore, it is more accurate to term the second mode triggering, rather than monostable.

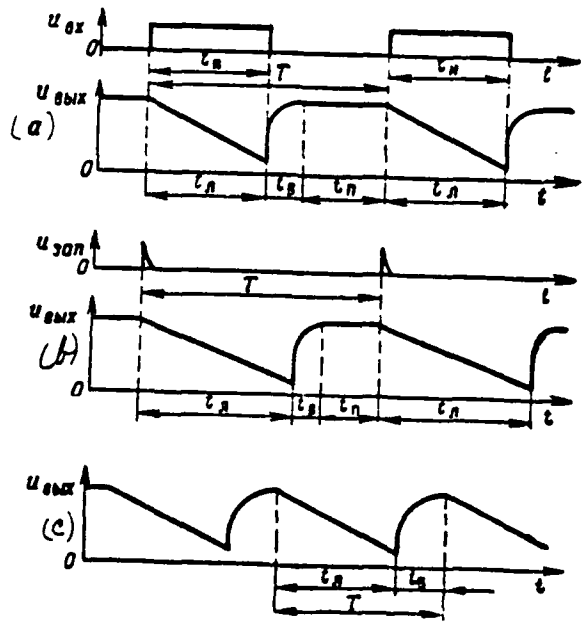

Figure IX.3. GPN Operating Modes:
(a) -- External control; (b) — Monostable; (c) -- Free-running.

2. Expressing Sawtooth Voltage Parameters Via Exponential Voltage Parameters. /361
Formulation of the Linearity Problem

We will express sawtooth voltage parameters via exponential voltage parameters, the initial sector of which is used as the working stroke. We will use ΔE_1 to designate the equivalent voltage drop that stimulates a change in capacitor voltage during the working stroke. (For the Figure IX.2 circuit $\Delta E_1 = E_1 - U_{C\,min}$. The magnitude of this drop clearly is determined as the voltage step at circuit output obtained when the circuit is manipulated if capacitor C is cut out of the circuit.) Then the capacitor voltage rise process during the working stroke is described by expression

$$u_в = u_C = \Delta E_1 \left(1 - e^{-\frac{t}{\tau_1}}\right). \tag{IX.6}$$

Differentiating (IX.6) over time, we will find that the voltage rate change is

maximum at the beginning of the working stroke (t = 0) and is minimum at the end of the working stroke (t = $t_{раб}$):

$$\left(\frac{du_{\text{э}}}{dt}\right)_{\text{макс}} = \frac{\Delta E_{\text{э}}}{\tau_{\text{э}}}; \left(\frac{du_{\text{э}}}{dt}\right)_{\text{мин}} = \frac{\Delta E_{\text{э}}}{\tau_{\text{э}}} e^{-\frac{t_{\text{раб}}}{\tau_{\text{э}}}}. \tag{IX.7}$$

Therefore, based on (IX.2), for the nonlinearity factor we will get:

$$\beta_{\text{н}} = \frac{\left(\frac{du_{\text{э}}}{dt}\right)_{\text{макс}} - \left(\frac{du_{\text{э}}}{dt}\right)_{\text{мин}}}{\left(\frac{du_{\text{э}}}{dt}\right)_{\text{макс}}} = 1 - e^{-\frac{t_{\text{раб}}}{\tau_{\text{э}}}}. \tag{IX.8}$$

When the condition that the initial sector of exponential curve (IX.4) is used is satisfied, it is possible to use approximate formula $1 - e^{-x} \approx x$, if $x \ll 1 \left(x = \frac{t_{\text{раб}}}{\tau_{\text{э}}}\right)$, and to consider that

$$\beta_{\text{н}} \approx \frac{t_{\text{раб}}}{\tau_{\text{э}}} \tag{IX.8a}$$

But, $\frac{du_{\text{э}}}{dt} = \frac{du_C}{dt} = \frac{i_C}{C}$, where i_C -- capacitor charging current during the working stroke. This current decreases by an exponential law from initial (maximum) value $I_{\text{э}}$ at the beginning of the working stroke to finite (minimum) value $I_{\text{к}} = I_{\text{э}} e^{-\frac{t_{\text{раб}}}{\tau_{\text{э}}}}$ at the end of the working stroke.

Therefore

$$\left(\frac{du_{\text{э}}}{dt}\right)_{\text{макс}} = \frac{I_{\text{э}}}{C}, \left(\frac{du_{\text{э}}}{dt}\right)_{\text{мин}} = \frac{I_{\text{к}}}{C} \tag{IX.9}$$

ano the expression for the nonlinearity factor may be written in the form /362

$$\beta_{\text{н}} = \frac{I_{\text{э}} - I_{\text{к}}}{I_{\text{э}}}. \tag{IX.10}$$

Assuming in (IX.6) that $t = t_{раб}$, we will get the expression for sawtooth voltage amplitude

$$U_{\text{п}} = U_{C\,\text{макс}} - U_{C\,\text{мин}} = \Delta E_{\text{э}} \left(1 - e^{-\frac{t_{\text{раб}}}{\tau_{\text{э}}}}\right). \tag{IX.11}$$

or, considering (IX.8),

$$U_a = \Delta E_0 \beta_н \qquad \text{(IX.12)}$$

Hence, on the basis of (IX.3), the supply source voltage utilization factor equals

$$\xi_a = \frac{U_a}{E_a} = \frac{\Delta E_0}{E_a}\beta_н \qquad \text{(IX.13)}$$

Assuming $\xi_a = 1$ (realistically, $\xi_a < 1$), from the last expression we will get maximum nonlinearity factor value

$$\beta_{н\,макс} = \frac{E_a}{\Delta E_0}, \qquad \text{(IX.14)}$$

when the working stroke is obtained during complete capacitor charging, i. e., its duration is maximum ($t_н \approx 3\tau_1$).

Finally, if one considers the rate of voltage rise during the working stroke (saw slope) as constant and equal to the rate of exponential voltage rise at the beginning of the working stroke, then, on the basis of (IX.1), (IX.7), and (IX.9), we will get

$$V = \overline{V} = V_{макс} = \left(\frac{du_1}{dt}\right)_{макс} = \frac{U_a}{t_н} = \frac{\Delta E_0}{\tau_a} = \frac{I_н}{C} = \text{const} \qquad \text{(IX.15)}$$

The resultant expressions are justified for linearly-falling voltage as well.

How does one go about increasing working stroke linearity -- linearizing exponential voltage? Ratio (IX.10) answers that question, since it demonstrates that the nonlinearity factor will equal zero if capacitor current constancy is provided during the working stroke shaping process: $\beta_н = 0$ when $I_н = I_к = I = \text{const}$. Actually, in this case

$$u_a = u_C = \frac{1}{C}\int_0^t i_C\,dt = \frac{1}{C}\int_0^t I\,dt = \frac{I}{C}t \text{ или } \frac{du_a}{dt} = \frac{I}{C} = \text{const} \qquad \text{(IX.16)}$$

-- capacitor voltage changes by a linear law (with constant rate (IX.15).

Thus, sawtooth voltage linearization requires that capacitor current be stablized during the working stroke. The following three linearization methods are /363 used in GPN circuits with increased linearity:

-- use of current-stabilizing one-ports [two-terminal networks];
-- use of compensating positive voltage feedback;
-- use of compensating negative voltage feedback.

We will examine the essence of these methods below.

§ 2. SAWTOOTH GENERATORS WITH A LINEAR R-C INTEGRATOR

1. Limitations Arising From Linear R-C Integrator Use

If a linear R-C integrator is used in a GPN, then its equivalent circuit corresponds to Figure IX2a when actual parameters replace equivalent parameters:

$$R_э = R;\ C_э = C;\ \tau_э \approx \tau_{зар} = RC;\ E_э = E_а;$$
$$\Delta E_э = E_а - U'_{C\ max} \approx E_а \ (\text{при } U'_{C\ max} \ll E_а). \qquad (X.17)$$

Therefore, based on (IX.8a), (IX.12), (IX.13), (IX.14), and (IX.15), output voltage parameters will equal

$$\delta_н \approx \frac{t_н}{RC};\ U_н = E_а\delta_н;\ \xi_а = \delta_н;\ \delta_{н\ max} = 1;\ V = \frac{E_а}{RC} \qquad (X.18)$$

Consequently, in principle it is impossible to obtain $U'_н > E_а\xi_н$, i. e., $\xi_э > \xi_н$, when a linear R-C network is used.

If, for example, source voltage equals E_a = 300 V, and the nonlinearity factor must not exceed 1%, then saw amplitude may not be more than 3 V, while its increase during a given E_a value may be achieved only at the cost of a deterioration of linearity, and an improvement in linearity by the loss of a further decrease in amplitude. Therefore, linear R-C integrator GPN are used only when high linearity ($\delta_н \geq 10\%$) and great saw amplitude are not required. It is more precise to refer to the output voltage of such GPN as exponentially- rather than linearly-changing and the GPN as exponential voltage or sweep generators.

EXERCISE IX.2

What is the physical cause of the fact that voltage u_C during capacitor charging across a resistance changes essentially linearly only at the beginning of the charging process (when $t \ll \tau_{разр}$), while $u_C \ll E_a$? (Page 497)

2. Triode Exponential Sweep Generator

The generator circuit and input and output voltage curves are depicted in Figure (IX.4). The generator operates in the external control mode and produces

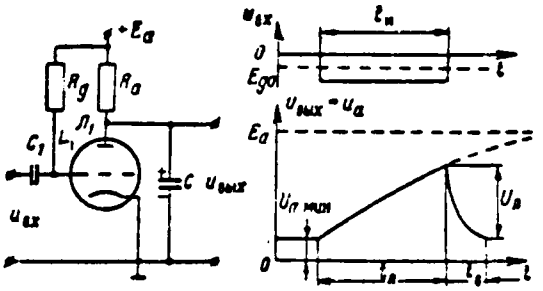

Figure IX.4. Triode Exponential Sweep Generator.

linearly-rising voltage. Triode L_1 functions as switch K--discharging tube. /364 Output voltage is shaped in capacitor C, i. e., picked off triode plate: $u_{вых} = u_C = u_a$. The circuit operates as follows. Negative square pulses of sufficient amplitude to blank the triode are supplied to triode grid. The triode is unblanked during resting times and minimum voltage is established at circuit output

$$U_{C\,мин} = U_{a\,мин} = E_a - I_{a\,мин} R_a = I_{a\,мин} R_{i\,мин} \qquad (IX.19)$$

where $R_{i\,мин}$ -- triode internal resistance to direct current.

Upon arrival of the subsequent pulse, which blanks the triode, capacitor

C charges across resistance R_a from plate voltage source E_a. Here, output voltage rises from value $u_{C\,мин}$ by the law of exponents

$$u_C = (E_a - U_{a\,мин})\left(1 - e^{-\frac{t}{\tau_{зар}}}\right) + U_{a\,мин}, \qquad (IX.20)$$

where $\tau_{зар} = R_a C$ -- capacitor charging time constant.*

At the moment the input pulse ceases ($t = t_и$), this voltage attains /365 maximum value

$$U_{C\,макс} = (E_a - U_{a\,мин})\left(1 - e^{-\frac{t_и}{\tau_{зар}}}\right) + U_{a\,мин}, \qquad (IX.20a)$$

after which the triode unblanks and rapid capacitor discharge occurs across it. Output voltage drops to initial level $U_{C\,мин}$ during the discharge process by the law of exponents:

$$u_C = (U_{C\,макс} - U_{C\,мин}) e^{-\frac{t - t_и}{\tau_{разр}}} + U_{C\,мин},$$

where $\tau_{разр} = R_{i_0} C$ -- capacitor discharge time constant.

Then the process repeats itself. Output voltage forward stroke and flyback duration obtained equal, respectively

$$t_а = t_и;\ t_в \approx 3\tau_{разр} = 3R_{i_0}C, \qquad (IX.21)$$

---

*Expression (IX.20) corresponds to (XI.10) and also may be obtained from evident ratio $u_C = E_a - u_R = E_a - i_{зар}R_a$. Capacitor charging current decreases by law $i_з = I_з e^{-\frac{t}{\tau_{зар}}}$, while the maximum value of this current equals $I_з = \frac{E_a - U_{a\,мин}}{R_a}$. Thus,

$$u_C = E_a - \frac{E_a - U_{a\,мин}}{R_a} R_a e^{-\frac{t}{\tau_{зар}}} = E_a - (E_a - U_{a\,мин}) e^{-\frac{t}{\tau_{зар}}} + U_{a\,мин} - U_{a\,мин} =$$

$$= (E_a - U_{a\,мин})\left(1 - e^{-\frac{t}{\tau_{зар}}}\right) + U_{a\,мин}.$$

while its amplitude

$$U_a = U_{C\,max} - U_{C\,min} = (E_a - U_{a\,min})\left(1 - e^{-\frac{t_и}{\tau_{зар}}}\right) \qquad (IX.22)$$

Given assigned ratio $\frac{t_и}{\tau_{зар}}$, the greater the E_a and the less the $U_{a\,min}$ value, the greater the U_a value. It follows from ratio (IX.19) that both internal resistance R_{io} and its quiescent current $I_{a0} = \frac{E_a}{R_{io} + R_a}$ must be as small as possible for a $U_{a\,max}$ decrease. The former provides triode type selection and connection of its grid across a large resistance to plus source bus $+E_a$ (here, due to grid clamping, grid potential is clamped at slight positive level $U_{go} \gtrsim 0$). Sufficiently-high plate load impedance R_a must be selected in order to decrease plate current I_{ao} when R_{io} is slight.

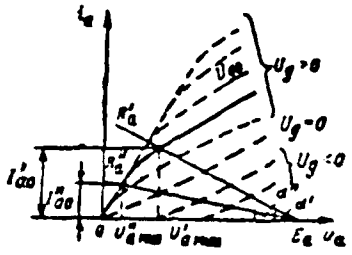

Figure IX.5. For Determination of Value $U_{a\,max}$ ($R''_a > R'_a$).

Value $U_{a\,min}$ is determined, as depicted in Figure IX.5, by the point of intersection of the triode plate characteristic for value $u_g = U_{go}$ and load line $i_a = \frac{E_a - u_a}{R_a}$ (see Chapter III, § 3, Figure III.13a). This point must fall in the characteristic of the critical mode corresponding to triode dynamic saturation, /366 given proper resistance R_a selection.* (It is demonstrated in Figure IX.5 that triode dynamic saturation is insured where resistance $R''_a \gtrsim R'_a$, i. e., resistance R'_a is not large enough). Charging time constant $\tau_{зар} = R_a C$ is selected from compromise circumstances: on the one hand, its value must be sufficiently great

*We will recall that the load line intersects on the X-axis of segments $u_a = E_a$ and sloped towards it at angle $\alpha = \operatorname{arctg}\frac{1}{R_a}$.

for obtaining sufficiently-slight nonlinearity factor $\beta_н = \frac{t_н}{\tau_{зар}}$, and, on the other, is sufficiently slight to obtain assigned saw amplitude $U_п = E_п\beta_н$.

Capacitor C capacitance should be as slight as possible to reduce recovery time $t_в \approx 3R_а C$. However, this capacitance significantly must exceed circuit stray capacitance $C_п$, which is the sum of triode output capacitance, circuit capacitance, and the input capacitance of the subsequent stage, comprising about 10--15 pF. This is necessary to decrease the impact of capacitance $C_п$ changes on output voltage parameters. Condition $C \gg C_п$, given selected magnitude $\tau_{зар} = R_а C$, may constrain the maximum resistance $R_а$ magnitude.

EXERCISE IX.3

Draw the output voltage curves for the circuit examined (Figure IX.4) for several control pulse spacings if, at moment t', while the second pulse is active:

a) control pulses ceased arriving;

b) the triode partially lost emission;

c) the triode completely lost emission. (Page 497)

One can envision a "stepped" (discrete) change in the scale of the scanning range in range displays with an exponential sweep. *Working* stroke, i. e., control pulse, duration $(t_н = t_и)$ changes spasmodically for this purpose. It is desirable when switching scale that there is no change on the screen, first, of sweep origin position and, second, sweep trace length. Sweep voltage $U_{н.нач}$ initial level constancy satisfies the first requirement, while constancy of its amplitude $U_п$ provides the second. But, the rate of sweep voltage v rise must be changed accordingly to retain sweep amplitude when working stroke duration changes. Actually, if $U_п = \text{const}$, when the scale is switched, then $\frac{t_{н1}}{t_{н2}} = \frac{v_2}{v_1} = \frac{tg\,\alpha_2}{tg\,\alpha_1}$ (Figure IX.6).

EXERCISE IX.4

What switchings must be made in the Figure IX.4 circuit in order to change sweep voltage during transition from scale 1 to scale 2 in accordance with Figure IX.6 $(U_{п1} = U_{п2})$ when the linearity condition is satisfied? How will nonlinearity factor $\beta_н$ change here? (Page 498)

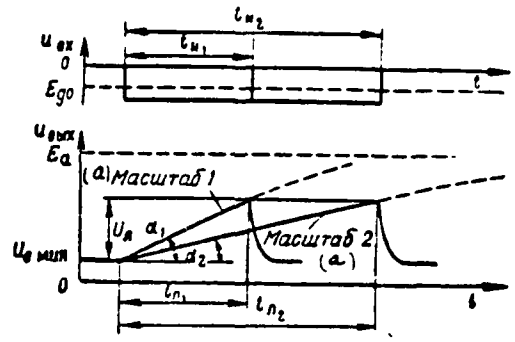

Figure IX.6. For Exercise IX.4. (a) -- Scale.

We now will examine how capacitor leakage resistance $R_{ут}$ and load impedance $R_н$ (input resistance of the subsequent stage) affect output voltage shape. In

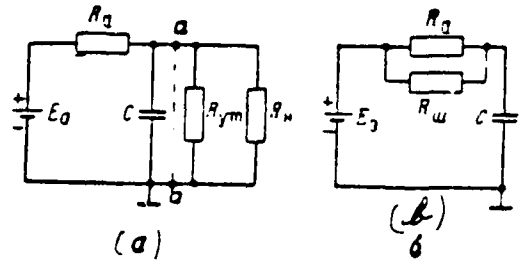

Figure IX.7. For Calculation of the Influence of Resistances Shunting Capacitor C.

accordance with the Figure IX.7a circuit, both capacitances shunt capacitor C.

Transforming this circuit by the theorem on the equivalent generator relative to points aa, we will shift to the circuit in Figure IX.7b, where

$$R_э = \frac{R_{ут}R_г}{R_{ут}+R_г};\quad E_э = \frac{E_г R_н}{R_н + R_г}\ .$$

The capacitor in the resultant circuit will charge with shorter time constant $\left(\tau_{зар} = \frac{R_э R_н}{R_э + R_н} C < \tau_{зар} = R_г C\right)$ from an equivalent lowered voltage source $(E_э < E_г)$. The decrease in the charging time constant during the given working stroke /368

duration leads to an increase in the nonlinearity factor. Actually, based on (IX.8a), we will get

$$\gamma_н = \frac{t_н}{\tau_{нар}} = \frac{t_н}{\frac{R_a R_н}{R_a + R_н} C} = \frac{t_н}{R_a C}\left(\frac{R_a + R_н}{R_н}\right) = \gamma_н\left(1 + \frac{R_a}{R_н}\right). \qquad (IX.23)$$

The reduction in equivalent generator voltage will not impact upon voltage amplitude since the rate of capacitor voltage rise will increase to the same degree due to a decrease in $\tau_{нар}$

$$U'_н = E_a\gamma'_н = \frac{E_a}{1 + \frac{R_a}{R_н}}\gamma_н\left(1 + \frac{R_a}{R_н}\right) = E_a\gamma_н = U_н. \qquad (IX.23a)$$

Thus, capacitor shunting by resistances leads to a deterioration in sawtooth voltage linearity, which is justified for any GPN circuits. Therefore, output voltage in many practical GPN circuits is picked not directly off a capacitor, but off those circuit points, the voltage between which changes by the same law as is the case for the capacitor, but connection to which the capacitor essentially does not shunt the load. Output voltage is picked off the capacitor across a buffer stage with high input resistance -- a cathode follower, if such points are absent in the circuit, as is the case with the circuit being examined.

Negative pulses blanking the triode and positive pulses unblanking it also may be used to control an expcnential sweep generator. In this event, circuit recovery (C discharge) occurs while the pulses are active and their duration must be sufficiently great: $t_н \geqslant t_в$. The working stroke is shaped during resting times $t_н = t_в$. when the triode must be blanked. This is done either with an outside negative bias source or through dynamic bias resulting from passage of positive pulses across coupling capacitor C_1.

The possibility of output voltage distortions due to control pulse action directly at circuit output across triode transfer capacitance C_{cg} is a shortcoming of this circuit. These distortions essentially may be eliminated if a pentode is used as switch in place of the diode.

3. Diode Exponential Sweep Generator

Generator circuits and voltage curves are depicted in Figure IX.8. The generator operates in the external control mode ($t_и = t_в$) and produces linearly-rising voltage.

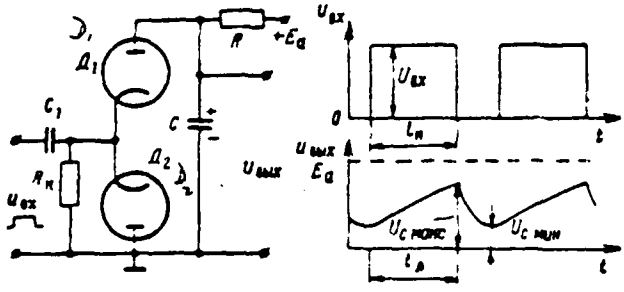

Figure IX.8. Diode Exponential Sweep Generator.

Diode D_1 plays the role of switch--discharging tube and positive-polarity /369 control pulses are supplied across coupling network $C_1R_к$ to its cathode. Diode D_1 blanks ($u_{вых} < 0$) while the control pulse is active and capacitor C charges from source $E_а$ across resistance R. Diode D_1 is unblocked ($u_{вых} > 0$) during resting times $t_в$ and the capacitor discharges across the diode and resistance $R_к$ with time constant $\tau_{разр} \approx R_к C$ (we will disregard diode internal resistance R_i $(R_i \ll R_к)$. Here, capacitor voltage will strive towards the initial value equalling (if one disregards R_i) $U_{C\,нач} \approx \frac{E_а R_к}{R + R_к}$. It is evident that circuit recovery time equals $t_в \approx 3\tau_{разр} = 3R_к C$.

Ratios (IX.18) as usual determine output voltage parameters.

EXERCISE IX.5

a) Explain the purpose of diode D_2.

b) Prove the circumstances for selection of the $R_к$ magnitude.

c) Formulate the requirements for control pulse amplitude $U_{вх}$. (Page 498)

4. Thyratron Exponential Sweep Generator

The generator circuit is depicted in Figure IX.9a. The generator produces linearly-rising voltage and may operate both in the free-running and external

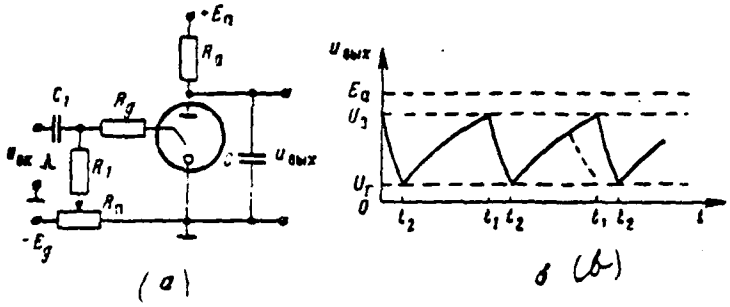

Figure IX.9. Thyratron Exponential Sweep Generator (a) and Its Output Voltage Curves for the Free-Running Mode.

synchronization mode. The thyratron plays the role of switch--discharging tube. Plate voltage at which ionization of the thyratron gas occurs, i. e., thyratron "firing," is referred to as firing potential $U_з$. Plate voltage at which gas deionization occurs, i. e., thyraton "quenching," is referred to as quenching potential $U_г$. The special feature of the thyratron used in this circuit is that firing potential significantly exceeds quenching potential $U_з > U_г$. Self-excited relaxation oscillations arise in the circuit due to this particular feature and it lacks the positive feedback network mandatory in other self-excited /370 pulse generators.

We will examine circuit operation in the free-running mode. The output voltage curve for this instance is depicted in Figure IX.9b. The thyratron does not fire at the moment plate voltage $+E_a$ source is connected since plate potential is unable with a jump to reach firing potential due to presence of capacitor C. Capacitor C charges from source $+E_a$ across resistance R_a since the thyratron will not conduct. Here, capacitor voltage (at thyratron plate) rises along an exponential curve with time constant $\tau_{зар} = R_a C$. The thyratron fires at moment t_1 when this voltage reaches value $U_з$ and a rapid capacitor discharge occurs across it with time constant $\tau_{разр} = R_i C$, where R_i -- slight internal resistance of the conducting thyratron. The thyratron quenches when capacitor voltage decreases to value $U_г$ (moment t_2), resulting in capacitor C beginning to charge anew, and so forth.

Potentiometer $R_п$ makes it possible to control the magnitude of thyratron negative grid bias and thereby to change firing potential $U_з$ (quenching potential $U_г$ essentially does not depend on the grid voltage). Resistance R_g constrains conducting thyratron grid current. Ratios (IX.18) for output voltage parameters remain justified for this circuit as well if the condition whereby the C charging exponential curve is used as initial sector working stroke is satisfied: $\frac{t_р}{\tau_{зар}} \ll 1$. However, saw amplitude here will not depend on source voltage E_a, working stroke duration, and the charging time constant and always equals $U_п = U_з - U_г$, while circuit parameters exclusively determine working stroke and flyback duration and, consequently, saw frequency.

EXERCISE IX.6 /371

Based upon the expression describing the laws of capacitor C voltage change during its charging and discharging, prove the formulas for output voltage forward stroke and flyback duration $t_р$ and $t_в$. How will a decrease in potential $U_г$ and source voltage E_a increase impact on output voltage parameters? (Page 499)

Along with simplicity, circuit advantages include slight flyback time, which is explained by insignificant conducting thyratron resistance (R_i = 40 ÷ 80 ohms) and very low (about 10 V) level $U_{с мин} = U_г$. Firing and quenching potential instability, as well as the possibility of premature thyratron firing due to finite deionization time $t_д$ following thyratron quenching (moment t_2), are considered circuit shortcomings. Premature firing leads to a reduction in working stroke duration and a decrease in saw amplitude (dotted curve in Figure IX.9b). Therefore, the deionization process must cease completely still at the beginning of the working stroke, while voltage u_C has only risen slightly, i. e., condition $t_д \gg t_р$ must be satisfied. But, this constrains maximum saw frequency to values of 50--100 kHz.

Positive pulses supplied to thyratron grid across isolating circuit C_1R_1 are used for external generator synchronization to stabilize saw frequency. Sync. pulse spacing must be somewhat less than the inherent oscillations of the circuit. In this event, every pulse in the steady-state mode forcibly will ignite the thyratron slightly before the capacitor voltage reaches value $U_з$. Values $t_п$ and $U_п$ will decrease accordingly.

§ 3. SAWTOOTH GENERATORS WITH CURRENT-STABILIZING TWO-TERMINAL NETWORKS

1. Sawtooth Voltage Linearization Principle Using Current-Stabilizing Two-Terminal Networks

Nonlinear resistance, whose magnitude changes in proportion to the voltage applied to it, resulting in the force of the current passing across it remaining constant ($i_{тт} = \frac{u_{тт}}{R} = \text{const}$), is referred to as a current-stabilizing two-terminal network [one-port].*

Volt-ampere characteristic $i_{тт} = f(u_{тт})$ of an ideal current-stabilizing two-terminal network is depicted in Figure IX.10a. We will connect such a two-terminal network

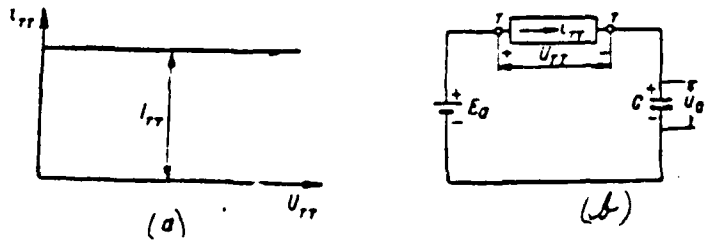

Figure IX.10. Ideal Current-Stabilizing Two-Terminal Network Volt-Ampere Characteristic (a) and Its Connecting Circuit to a Capacitor Charging Circuit (b).

to a capacitor charging network using the Figure IX.10b circuit. Voltage applied to the two-terminal network equals $u_{тт} = E_0 - u_C$ and it decreases due to the voltage u_C rise as the capacitor charges. However, the current passing across the /372 two-terminal network and discharging the capacitor $i_{тт} = i_{нач.}$ remains constant. Therefore, in accordance with ratios (IX.16), voltage u_C rises strictly by a linear law. It is evident that if the current-stabilizing two-terminal network is connected to the capacitor discharging network, then the voltage in it will decrease also by a strictly-linear law.

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*Here and in future, we will use TT to designate current-stabilizing two-terminal network terminals.

Naturally, the characteristics of actual current-stabilizing two-terminal networks differ from those of an ideal network and their use makes it possible to increase sawtooth voltage linearity only to a certain degree.

The pentode, whose volt-ampere (static plate) characteristic $i_a = \phi(u_a)$ is depicted in Figure IX.11 and, given clamped control and screen grid voltages,

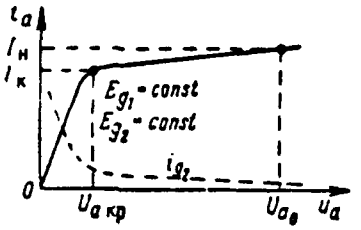


Figure IX.11. Pentode Volt-Ampere Characteristic.

plays the current-stabilizing two-terminal network TT role in tube circuits is depicted in Figure IX.11 and has a virtually horizontal sector (see Chapter III, § 2, Figure III.5). The voltage applied to it $u_{тт} = u_a$ drops from certain initial maximum value U_{ao} during capacitor charging (discharging) across the pentode. However, as long as it remains greater than critical plate voltage $U_{a\,кр}$, plate current changes slightly i_a = const. Given $u_a = U_{a\,кр}$, current stabilization is disrupted since intense cathode current redistribution between plate and screen grid begins (current i_a drops sharply, while current i_{g2} rises). Thus, pentode voltage may range from $U_{a\,макс} = U_{a0}$ only to $U_{a\,мин} = U_{a\,кр}$ when working stroke linearity rises. This constrains the maximum sawtooth voltage amplitude by magnitude

$$U_{a\,макс} = U_{a0} - U_{a\,кр} \qquad (IX.24)$$

Value U_{ao} may be compared to plate supply source voltage and comprise /373 several hundred volts and pentode properties ($U_{a\,кр}$ = 30 ÷ 60 V) determine value $U_{a\,мин}$.

Three variations of pentode use as a current-stabilizing two-terminal network are possible in practical circuits. The two-terminal networks corresponding to

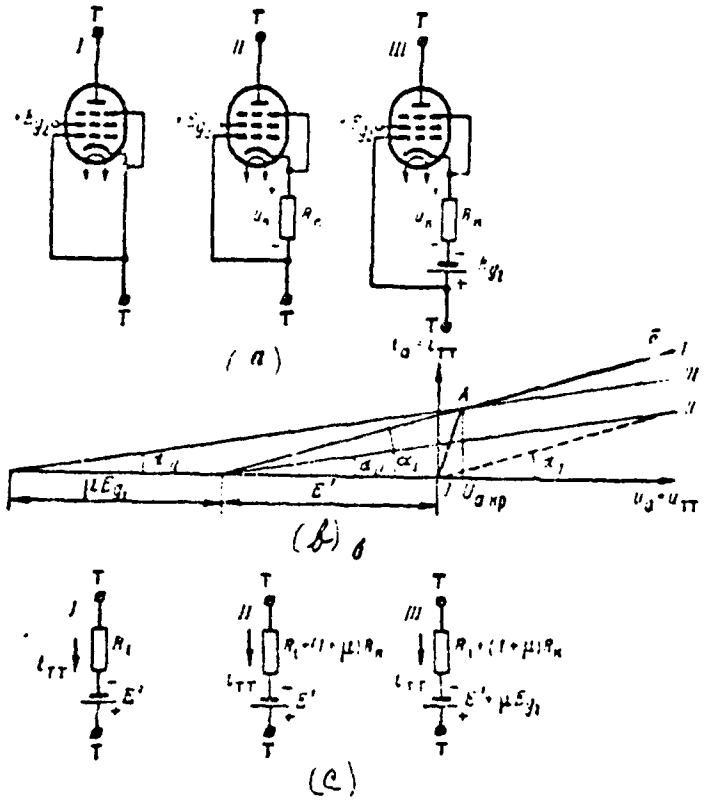


Figure IX.12. Pentode Current-Stabilizing Two-Terminal Network Circuits (a), Volt-Ampere Characteristics (b), and Equivalent Circuits (c).

these variants (a), a simplified plot of their volt-ampere characteristics (b), and the equivalent circuits to which they will be reduced (c) are depicted in Figure IX.12.

Variant I. Clamped Grid Potential Pentode (Figure IX.12a, I).

Broken line OAB may be used to approximate the pentode volt-ampere /374 characteristic where $E_{g1} = 0$ and $E_{g2} = \text{const}$ (Figure IX.12b). Line I coinciding with current-stabilizing sector AB, accumulates at the X-axis at angle $\alpha_1 = \arctg \frac{1}{R_i}$, where $R_i = \frac{\Delta u_a}{\Delta i_a}$ -- pentode internal resistance to alternating current, and intersects segment E' on this axis. Therefore, the sector AB may be written in the form $i = \frac{u_a - E'}{R_i}$. Hence, the equivalent circuit for nonlinear two-terminal network

TT where $u_a \geq U_{a\,sp}$ is represented in the form of sequential connection of linear resistance R_i and fictitious constant voltage source E', which maintains current $i_a = i_{a\,sp}$ (Figure IX.12c, I).* The greater the value of R_i and E' (i. e., the more horizontal sector AB), the higher the current-stabilizing action of the pentode, given the assigned average current i_a value. This is explained physically by the fact that, when E' increases, the voltage u_a change during the working stroke exerts an ever decreasing influence on current magnitude. Ideal current stabilization requires that $E' = \infty$, $R_i = \infty$, i. e., sector AB would be horizontal (see Figure IX.10a). Most pentodes have an E' value on the order of several kilovolts, which significantly exceeds plate supply voltage: $E' \gg E_a$.

It is easy to determine the parameters of sawtooth voltage obtained when a capacitor charges across the pentode on the Figure IX.12c, I equivalent circuit on Figure IX.10,b replaces the two-terminal network TT. Then, considering that $\tau_{ch} = \tau_{dap} = R_i C$; $\Delta E_a \approx E_a + E'$ (we disregard value $U_{c\,max} \ll E_a$) in the case under examination, based on (IX.8a, IX.12, and IX.13) we will get

$$\beta_u = \frac{t_a}{R_i C}; \quad U'_a = (E_a + E')\beta_u; \quad \xi_a = \frac{E_a + E'}{E_a}\beta_u \qquad \text{(IX.25)}$$

Comparing these ratios with ratios (IX.18) for the case in which the capacitor charges across resistance R and considering that $E' \gg E_a$, we see that, in this case, saw amplitude U'_a and the source voltage utilization factor are significantly greater, given identical nonlinearity factor β_u . Essentially, this linearization method makes it possible to obtain $\beta_u \leq 1\%$ where $\xi_a = 0.5—0.8$.

Variant II. Pentode enveloped by negative current feedback (Figure IX.12a, II).

Negative feedback is created due the voltage drop across pentode cathode load impedance R_k: $u_k = i_a R_k = -u_{gk}$. As indicated in § III.4, negative feedback action increases two-terminal network resistance to alternating current and provides additional pentode current stabilization. As a result, working stroke linearity rises in comparision to the previous circuit. Here, however, negative bias /375

*Introduction of source E' ascribes to R_i a sense of resistance to alternating current.

$u_{g1} < 0$ reduces average pentode current value. Therefore, during identical time t_1, the capacitor will charge (discharge) to a lesser degree than in the previous instance (where $u_{g1} = 0$), i. e., saw amplitude and source voltage utilization factor will decrease.

Considering negative coupling action, in accordance with (III.74) two-terminal network TT resistance equals $R_{TT} = R_1 + (1-\mu)R_2$, where μ -- pentode static gain ($\mu \gg 1$). Therefore, line II in Figure IX.12b, coinciding with the current-stabilizing sector of this two-terminal network's volt-ampere characteristic, slopes at a lesser angle $\alpha_{II} = \operatorname{arctg}\frac{1}{R_{TT}}$, than line I (which also provides better current stabilization) and passes under it (which corresponds to a lesser current value).

The line II equation is written as $i_a = \frac{u_a - E}{R_{TT}}$, hence the two-terminal network equivalent circuit is represented in accordance with Figure IX.12c, II. Merging the Figure IX.10b two-terminal network circuit with this equivalent circuit and considering that, in this case, $\tau_a = \tau_{sep} = R_{TT}C = [R_1 + (1+\mu)R_2]C$, $\Delta E_a \approx E_a - E$, based on (IX.8a, IX.12, and IX.13), we will get:

$$\beta_H = \frac{t_1}{[R_1 + (1+\mu)R_2]C}; \quad U_a = (E_a - E)\beta_H; \quad \xi_a = \frac{E_a - E}{E_a}\beta_H. \qquad \text{(IX.26)}$$

Comparing these ratios with (IX.25), we see that, given the same magnitude t_1 as was the case in the previous variant, the nonlinearity factor significantly decreases; however, here, saw amplitude and source voltage utilization factor decrease by the identical factor. Essentially, this linearization method makes it possible to reduce value β_H to tenths of a percent.

Variant III. Pentode enveloped by negative current feedback, with positive constant bias in the control grid network (Figure IX.12a, III).

The current-stabilizing action of this two-terminal network is approximately the same as for two-terminal network II (also provided by negative feedback). However, positive bias E_{g1} increases the pentode current direct component, thanks to which the capacitor charges (discharges) to a great degree during the same working stroke time. Therefore, values U_a and ξ_a will rise while high linearity is retained. Line III in Figure IX.12b, coinciding with the current-stabilizing

sector of the volt-ampere characteristic of this two-terminal network, is sloped at the identical angle as was line II, $\alpha_{III} = \alpha_{II} = \text{arc tg}\frac{1}{R_{i\,\text{тт}}}$, but it passes above it, intersecting large segment $E' + \mu E_{g1}$ on the X-axis.*

The line III equation is $I_a = \frac{E_a + E' + \mu E_{g1}}{R_{i\,\text{тт}}}$, hence the equivalent two- /376
terminal network equation is in accordance with Figure IX.12c, III. Merging the Figure IX.10b two-terminal network TT with this equivalent circuit and considering that, in this instance, $\tau_1 = \tau_{\text{зар}} = R_{i\,\text{тт}}C = [R_i + (1-\alpha)R_k]C$, $\Delta E_c \approx E_a + E' + \mu E_{g1}$ ($\mu E_{g1} \gg E' \gg E_a$), based on (IX.8a, IX.12, and IX.13) we will get

$$\beta_k = \frac{t_p}{[R_i + (1+\mu)R_k]C}; \quad U_a = (E_a + E' + \mu E_{g1})\beta_k;$$
$$\xi_a = \frac{E_a + E' + \mu E_{g1}}{E_a}\beta_k. \qquad \text{(IX.27)}$$

Comparing these ratios with (IX.26), we see that, given the same magnitude t_p extant in the previous variant, the same slight nonlinearity factor is retained. However, saw amplitude and source voltage utilization factor increase significantly.

The results obtained for capacitor charging across the three current-stabilizing two-terminal networks examined are compiled in Table 2, with expressions (IX.18) initially introduced for comparison for a case in which a capacitor charges across linear resistance R. Maximum nonlinearity values $\beta_{k\,\text{макс}}$ (IX.14) also are presented there.

These results also are explained in Figure (IX.13), where the approximate shape of linearly-rising voltage is depicted for identical working stroke time t_p for all four instances ($R = R_i$ is assumed for clarity).

All ratios remain in force for linearly-falling voltages shaped by /377
means of capacitor discharge. There is a requirement only to replace plate supply source voltage E_a in the formulas for U_a and in the numerator of formulas for

*Under the influence of positive bias E_{g1}, plate current rises in the same manner as it would if plate voltage rose by magnitude μE_{g1}.

Table 2

(a)				
(c)	$\frac{t_1}{RC}$	$E_a\xi_н$	$\xi_н$	1
(d)	$\frac{t_1}{R_iC}$	$(E_a - E)\xi_н$	$\frac{E_a - E}{E_a}\xi_н$	$\frac{E_a}{E_a - E}$
(d)		$(E_1 - E)\xi_н$	$\frac{E_1 - E}{E_1}\xi_н$	$\frac{E_a}{E_1 - E}$
(d)		$(E_1 + E + \mu E_g)\xi_н$	$\frac{E_1 - E - \mu E_g}{E_a}\xi_н$	$\frac{E_1}{E_a + E + \mu E_g}$

KEY: (a) -- Element across which the capacitor charges; (b) -- Where; (c) -- Resistance; (d) -- One-port.

ξ_a with the maximum capacitor voltage at the beginning of the working stroke $U_{C\,макс}$ (often $U_{C\,макс} = E_a$).

Besides a pentode, a triode, whose internal resistance to direct current is less than that of a pentode, may be used as a current-stabilizing one-port for sawtooth voltage linearization. However, since a triode volt-ampere characteristic does not have a "horizontal" sector, in this c[ase] powerful negative current feedback and positive bias in the grid network (variant III) are mandatory. Here, ratios (IX.27) determine sawtooth voltage parameters if E' = 0 is placed /378 in them:

$$\xi_н = \frac{r_i}{(R_i + r_i + \mu)R_{ш}C};\quad U_1 = (E_a + \mu E_{g1})\xi_н$$
$$\xi_a = \frac{E_1 + \mu E_g}{E_a}\xi_a \qquad (IX.27a)$$

2. Linearly-Rising Voltage Generators with a Current-Stabilizing Pentode

Two linearly-rising voltage generator circuits and the curves of their input (for comparison simplicity, they are identical) and output voltages are depicted in Figure IX.14. Both circuits operate in the external control mode. They differ from the triode exponential sweep generator (Figure IX.4) only in that a current

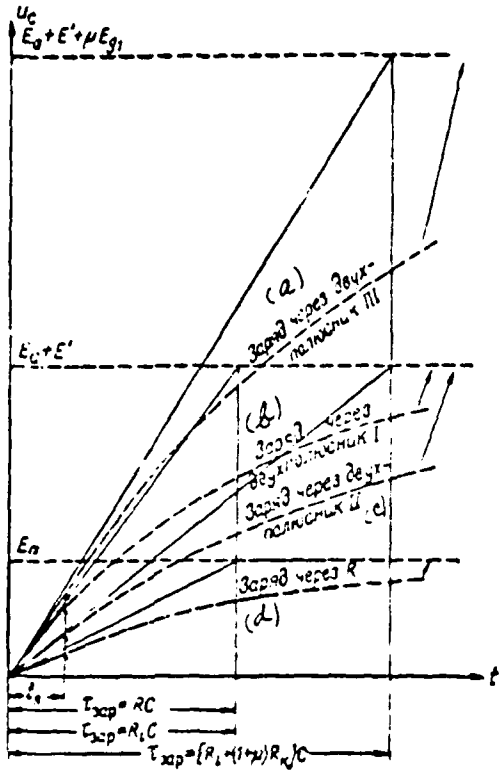


Figure IX.13 Comparative Shape of Linearly-Rising Voltage For Cases Examined in Table 2.

Key: a) charge through two-terminal network III; b) charge through two-terminal network I; c) charge through two-terminal network II; d) charge through R.

stabilizing two-terminal network II is connected in both circuits in place of plate load impedance R_a. As a result, as was indicated above, output voltage linearity is increased significantly. Triode L_1 in both instances as usual functions as switch K--discharging tube; rapid capacitor C discharge occurs across it during resting times between control pulses. Pentode L_2, enveloped by negative current feedback (variant II in Figure IX.12) is used in the Figure IX.14a circuit as the current-stabilizing two-terminal network across which capacitor C charges while control pulses are active. Ratios (IX.26) determine the output voltage parameters of this circuit. Pentode L_2, also enveloped by negative current feedback but with additional positive bias E_{g1} in the control grid network (variant III in Figure IX.12), is used in the Figure IX.14b circuit as the current-stabilizing

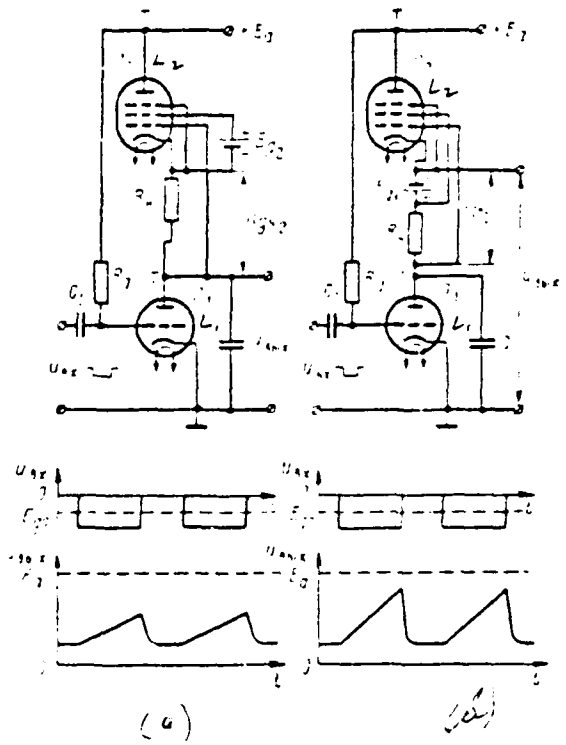


Figure IX.14. Current-Stabilizing Pentode Linearly-Rising Voltage Generators.

two-terminal network. Bias source E_{g1} also provides screen grid potential. Circuit output voltage is picked off between pentode cathode and "ground" rather than from the capacitor. Here, it differs from linearly-rising voltage u_C by essentially fixed magnitude [illegible] comprising only several volts.* But the deleterious influence of load impedance on the nonlinearity factor decreases. Ratios (IX.27) [illegible] the output voltage parameters of this circuit.

*The magnitude of the voltage [illegible] change during the capacitor charging process is [illegible] times smaller than the voltage [illegible] change (between pentode plate and cathode), i.e., from only amplitude [illegible]. Therefore, one may disregard the [illegible] change.

EXERCISE IX.7

a) Explain why negative feedback action in the Figure IX.14a circuit leads to output voltage linearization.

b) How does connection of positive bias E_{g1} to the control grid network /379 impact upon Figure IX.14b circuit output voltage parameters? (Page 499)

Independent voltage E_{g1}, E_{g2} sources need to be used in the Figure IX.14 circuits since, as a result of the increase in L_2 cathode potential as the capacitor charges, not a single one of the poles of these sources has a clamped potential and, consequently, cannot be connected to circuit chassis ("grounded"). The following circuit does not have this shortcoming.

3. Linearly-Rising Voltage Generator with a Charged Capacitor as Positive /380 Bias Source

The generator circuit and curves of voltages explaining its operation are depicted in Figure IX.15. Triode L_1, to whose grid negative control pulses are supplied, as usual plays the role of switch--discharging tube for capacitor C. Triode L_2, enveloped by negative current feedback with positive bias in the control grid, is the current-stabilizing two-terminal network TT across which capacitor C charges. Resistance $R_{\text{н}}$ creates the negative feedback, while capacitor C_2 creates positive bias. Triode L_3 will serve for capacitor C_2 replenishment during resting times between input pulses.

The circuit operates as follows. Triodes L_1 and L_3 are unblanked during resting times between input pulses. Capacitor C discharges across triode L_1 to voltage $U_{C\min} = U_{a1\min}$ with time constant $\tau_{разр} = R_{a1}C \ll \tau_{и}$. Triode L_1 positive grid decreases its internal resistance to direct current R_{i01}, i. e., reduces values $U_{a1\min}$ and $U_{C\min}$. Capacitor C_2 is charged by triode L_3 current to voltage $u_{C2} = I_{a3}R_{\text{п}}$ applied with a "plus" to triode L_2 grid. Potentiometer $R_{\text{п}}$ may be used to control the current I_{a3} magnitude and, consequently, voltage u_{C2} as well.

Triode L_1 and, immediately thereafter, triode L_3 are blanked upon input pulse arrival and capacitor C charges across current-stabilizing triode L_2. Simultaneously

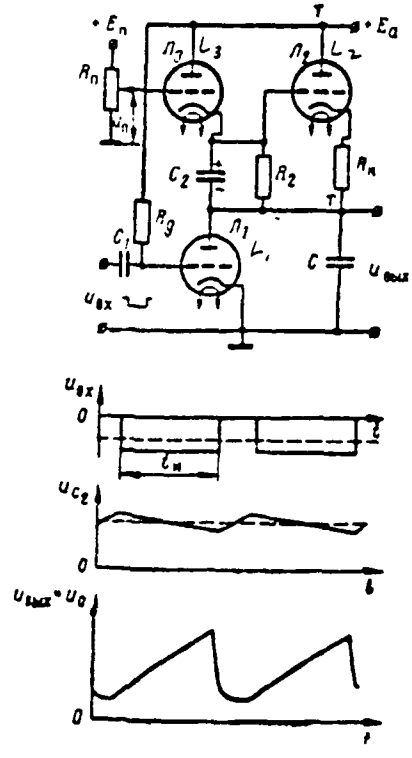


Figure IX.15. Linearly-Rising Voltage Generator With Charged Capacitor As Positive Bias Source.

capacitor C_2 discharges across resistance R_2, whose selected magnitude is /381 large enough (on the order of unities of megohms) to satisfy condition $\tau_{разр} = R_2 C_2 \gg t_и$. Therefore, voltage u_{C2} decreases slightly while the pulse is active and plays the role of constant positive bias in the triode L_2 control grid network.

Triodes L_1 and L_3 are unlanked again when the pulse ceases, capacitor C rapidly discharges across triode L_1, and capacitor C_2 recharges across triode L_3. Output voltage is picked off capacitor C and ratios (IX.27a) determine its parameters. The circuit makes it possible to obtain sawtooth voltage with amplitude U_1 = 100 ÷ 200 V and nonlinearity factor $\beta_н$ = 1—3%.

The linearity of this voltage at the very onset of the working stroke deteriorates because triode L_3 blanks somewhat later than does triode L_1. Actually, a certain amount of time is required after triode L_1 blanks for capacitor C voltage to rise to that $\Delta U_C'$ magnitude at which triode L_3 cathode potential will increase enough for its blanking. It is evident that $\Delta U_C' = E_{a} - U_{c3}$, where $U_{c3} \approx U_{} - U_{} - U_{}$.

But, as long as triode L_3 remains unblanked, C charging occurs not only by triode L_2 stabilizing current, but also by triode L_3 current across resistance R_2. Value $\Delta U_C'$ will not exceed several volts, given a sufficiently high R_2 magnitude.

EXERCISE IX.8

a) Draw and explain the approximate shape of distortions at the onset of the working stroke arising due to nonsimultaneous triode L_1 and L_3 blanking.

b) How will output voltage parameters change, given an "upward" shift of the Figure IX.15 potentiometer R_1 arm? (Page 500)

4. Linearly-Falling Voltage Generator with a Current-Stabilizing Pentode

The generator circuit and the curves of its input and output voltages are depicted in Figure IX.16. The circuit operates in the external control mode and shapes the working stroke by means of capacitor discharge across a pentode (variant I in Figure IX.12). Triode L_1, to whose input positive-polarity control pulses are supplied, functions as the switch. This triode unblanks when the control pulse is active and capacitor C charges rapidly across it from voltage source $+E_a$. The capacitor charges to voltage $U_{C\,max} = U_{a2\,max} = E_a - U_{a1\,min}$ since pentode L_2 simultaneously is unblanked here. But, pentode internal resistance to direct current is much greater than that of the triode $R_{io2} \gg R_{io1}$. Therefore, $u_{a2} \gg u_{a1}$ and $U_{C\,max} \approx E_a$.

Triode L_1 is blanked during resting times since its cathode potential /382 $u_{k1} = u_C$ greatly exceeds grid potential where $u_{c1} = 0$. Here, capacitor C is discharged by virtually constant current across pentode L_2. Voltage u_C is reduced virtually by a linear law during the discharge process to value $U_{C\,min}$, which

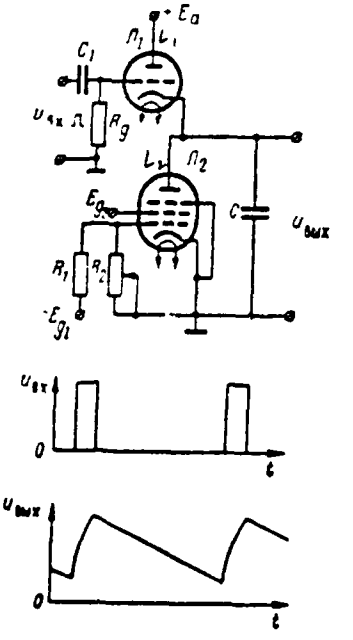


Figure IX.16. Linearly-Falling Voltage Generator With Current-. ..ilizing Pentode.

is attained by the time the subsequent control pulse begins. The action of the subsequent pulse causes the process to repeat.

Pentode current, i. e., the rate of capacitor C discharge, is controlled by variable resistance R_2, which supplies the magnitude of negative bias to the pentode control grid. Given the assigned working stroke duration ($t_з = t_и$), this makes it possible to change the $U_{c\,max}$ value and, consequently, sawtooth voltage amplitude $U_з$. Value $U_{c\,max}$ decreases when negative bias decreases (when the R_2 arms is shifted "upwards"). However, there is a requirement to satisfy condition $U_{c\,max} > U_{c\,кр}$ in order that capacitor discharging current stabilization at the end of the working stroke is not disrupted. Here, triode L_1 also is maintained in the blanked state until the end of the working stroke since $U_{c\,max} > E_{g1}$.*

*Dynamic bias arising in the triode L_1 grid when positive control pulses pass across capacitor C_1 facilitate L_1 blanking (see Chapter II, § 5).

Pulses of significant amplitude $U_{вх} \approx U_{с\,макс}$ are required for circuit control. Actually, there is a requirement that $U_{вх} - U_{с\,макс} > E_{з0}$ in order for triode L_1 to be unblanked during the entire control pulse duration. Otherwise, the triode will blank before the control pulse ceases due to the cathode potential increase, which leads to a reduction in value $U_{с\,макс}$ and amplitude $U_п$. Ratios (IX.25) determine circuit output voltage parameters and, in practice, one may obtain $\beta_п \geq 1\%$ where $\xi_a = 0.6—0.8$. Resistance $R_к$ may be connected to the pentode cathode network to increase linearity. In this event, capacitor discharge during the working stroke is more constant, but by less current (variant II in Figure IX.12), resulting in the fact that, in accordance with (IX.26), value ξ_a, i. e., linearly-falling voltage amplitude, will decrease along with the $\beta_п$ decrease.

EXERCISE IX.9

Draw the approximate shape of the Figure IX.16 circuit output voltage if $U_{г\,макс} < U_{а\,нр}$.

(Page 500)

§ 4. SAWTOOTH GENERATOR WITH COMPENSATING POSITIVE VOLTAGE FEEDBACK

1. Sawtooth Voltage Linearization Principle Using Positive Feedback

Charging current equals $i_C = \frac{E - u_C}{R}$ as a capacitor charges from source E across a resistance and it decreases due to the rise in voltage u_C, which opposes source voltage E. The nonlinearity of the voltage u_C rise law (see Exercise IX.2) is a result of the current decrease.

The essence of this linearization method is that voltage u_C action is neutralized by special compensation voltage $u_к$, which will be introduced into the charging network through the positive feedback loop. Compensation voltage must equal voltage u_C, but act opposite in phase with it: $u_к = -u_C$. Here, capacitor charging current turns out to be constant

$$i_C = \frac{E - u_C + u_к}{R} = \text{const}^*. \qquad \text{(IX.28)}$$

*One should understand u_C and $u_к$ as being variable components (increments) of these voltages.

and, in accordance with (IX.16), capacitor voltage will rise by a linear law.

We will assume that one of the capacitor plates is "grounded" (has chassis clamped potential). Then the capacitor charging circuit during the working stroke

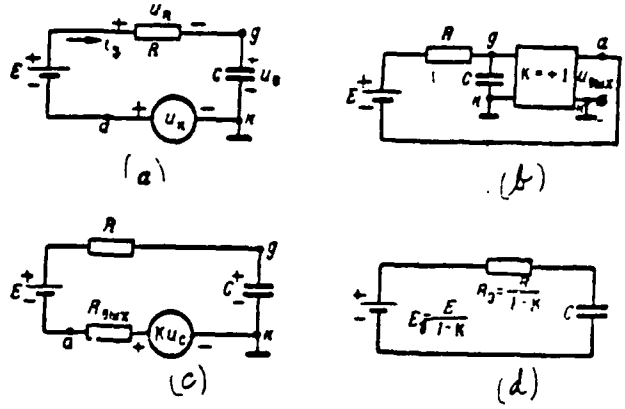


Figure IX.17. For Compensating Positive Voltage Feedback Use.

is depicted as shown in Figure IX.17a. Capacitor voltage itself, which across an amplifier with gain K = 1 will be introduced in reverse into the charging network, is used as compensation voltage. It is evident from Figure IX.17a that only points gk may be amplifier input terminals, while points ak may be output terminals. Therefore, the amplifier connection circuit corresponds to Figure IX.17b. Point a potential also must rise if point g potential rises. Consequently, the amplifier must not invert the input voltage phase (K = +1). In addition, it must have high input resistance so as not to shunt capacitor C and slight output resistance /384 so that a low-resistance load may be connected. A cathode follower satisfies these requirements (see Chapter III, § 4).

Feedback active in the circuit is positive since the point g potential rise across the amplifier, source E, and resistance R again is transmitted to the "upper" capacitor plate (at amplifier input).

The equivalent circuit for the Figure IX.17c variable components, where Ku_C -- amplifier output voltage and $R_{вых}$ -- its output resistance, corresponds to

the Figure IX.17b circuit. Considering that $R_{вых} \ll R$, for this circuit we will get

$$i_C = \frac{E - u_C + Ku_C}{R + R_{вых}} \approx \frac{E - u_C(1-K)}{R},$$

hence

$$u_C = \frac{1}{C}\int_0^t i_C\,dt = \frac{E}{RC}t - \frac{1-K}{RC}\int_0^t u_C\,dt, \text{ or } \frac{du_C}{dt} + \frac{1-K}{RC}u_C - \frac{E}{RC} = 0.$$

The solution of the last equation (given zero initial conditions) is

$$u_C = \frac{E}{1-K}\left(1 - e^{-\frac{t}{RC}\frac{1}{1-K}}\right). \qquad \text{(IX.29)}$$

The Figure IX.17d equivalent circuit corresponds to expression (IX.29), from which it follows that the examined linearization method is equivalent to an increase, by a factor of $\frac{1}{1-K}$, both of source voltage, i. e., extant charging voltage drop, and of charging resistance, i. e., of the charging time constant. /385 Therefore, equivalent charging network parameters (see Figure IX.2) will equal

$$\mathcal{E}_э = \frac{E}{1-K};\ R_э = \frac{R}{1-K};\ \tau_э = R_э C = \frac{RC}{1-K} \qquad \text{(IX.30)}$$

Considering (IX.30), based on (IX.8a, IX.12, IX.13, and IX.14) we will get

$$\beta_н = \frac{t_а}{RC}(1-K);\ U_а = \frac{E}{1-K}\beta_н;\ \xi_а = \frac{1}{1-K}\beta_н;\ \beta_{н\,макс} = 1-K. \qquad \text{(IX.31)}$$

It follows from these expressions that the closer the amplifier gain is to unity (where K = 1, $\beta_н$ = 0), the greater the resultant sawtooth voltage linearity. Given the assigned nonlinearity factor value $\beta_н$ = const, sawtooth voltage amplitude $U_а$ and source voltage utilization factor $\xi_а$ rises by a factor of $\frac{1}{1-K}$ compared to a linear R-C integrator (we will recall that they may not exceed values $U_{а\,макс} = E_а$, $\xi_{а\,макс} = 1$). Essentially, the result is $\beta_н$ = 2—3% where $\xi_а$ = 0.6—0.8 for a cathode follower with K = 0.95—0.98.

EXERCISE IX.10

a) Using the Figure IX.17b circuit, explain why capacitor charging current remains constant.

b) Plot on one graph the capacitor voltage curves when the capacitor charges across a resistance and based on the Figure IX.17b circuit, given identical C and R values. Assume K = 0.8 for ease in plotting. (Page 501)

Practical realization of the Figure IX.17b capacitor charging circuit during the working stroke is complicated because the charging voltage E source turns out to be insulated from "ground" (not one of its terminals has chassis potential). This rules out direct use of plate voltage source E_a as the source. Therefore, a capacitor of large capacitance, preliminarily (during time t_3) charged to voltage E_a, plays the role of source E during the working stroke shaping process in practical positive-feedback GPN circuits.

2. Linearly-Rising Voltage Generator with a Capacitor as Charging Voltage Source

The generator circuit and the curves of the voltages at its characteristic points are depicted in Figure IX.18. The generator operates in the external control mode. Linearly-rising voltage is shaped in capacitor C, while capacitor C_2 plays the role of charging voltage source ($C_2 \geq C$). Triode L_1 is the switching element and negative-polarity control pulses blanking it during working /386 stroke period $t_1 - t_2$ are supplied to its input. A cathode follower is assembled on triode L_2 and positive feedback is accomplished across it, linearizing the working stroke, while circuit output voltage is picked off it. Capacitor C_2 recharges across diode D during resting times. The circuit operates as follows.

Initial state. Tubes L_1, L_2 and diode D are unblanked prior to control pulse arrival. Capacitor C discharges across triode L_1 to minimum voltage $U_{c\,min} = U_{a_1\,min} = \frac{E_a}{R_{do} + R + R_{io1}} R_{io1}$, where R_{do}, R_{io1} -- diode D and triode L_1, respectively, internal resistance to direct current. Since $R \gg R_{do}$, R_{io1} (triode L_1 positive grid insures that R_{io1} is very slight), voltage $U_{c\,min}$ comprises only several volts. Capacitor C_2 is charged from voltage source E_a across diode D

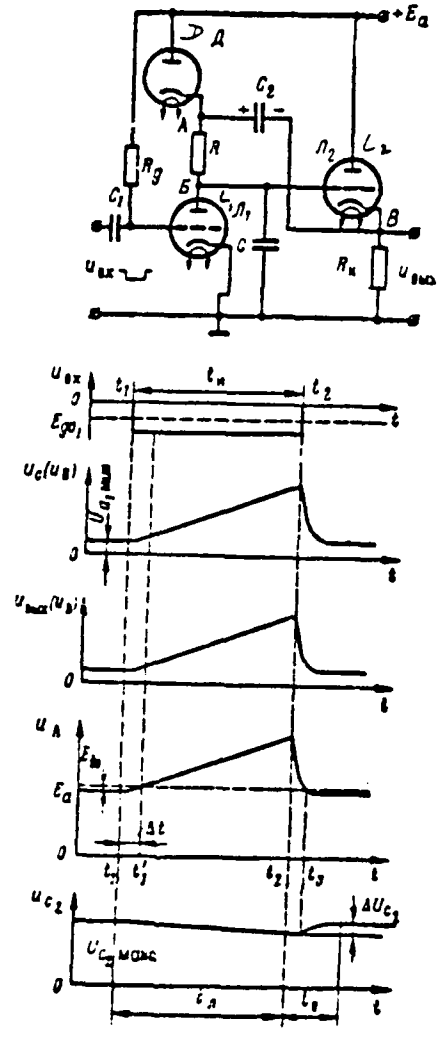


Figure IX.18. Linearly-Rising Voltage Generator With A Capacitor As Charging Voltage Source.

and resistance R_a to maximum voltage almost equalling E_a: $U_{C_1\,макс} = E_a - u_g - u_a \approx E_a$ ($u_g \ll E_a$; $u_a \ll E_a$). Circuit output voltage is minimum since minimum voltage $U_{C_1\,мин}$ is applied to cathode follower input.

Operating stage. A control pulse blanks triode L_1 at moment t_1. In /387 this connection, capacitor C begins to charge from source E_a along network $+E_a$, diode D, R, C, $-E_a$ (chassis). The voltage u_C increase (of point $Б$ potential) is transmitted across the cathode follower to point B and leads to a rise in point A potential since $u_A = u_B + u_{C2}$, and, as long as the diode is unblanked, voltage u_{C2} = const. As a result, diode cathode potential u_A will exceed value E_a (the potential of its plate). At moment t_1', when this excess will equal diode cutoff voltage $E_{зап}$ (see Figure III.2), the diode blanks and cuts source E_a off from capacitor C. From this moment on, capacitor C continues to charge only from capacitor C_2 along network C_2, R, C, $R_{вых.к}$, C_2, where $R_{вых.к}$ -- cathode follower output resistance. Since $C_2 \gg C$, voltage u_{C2} during the capacitor C charging process decreases by slight magnitude ΔU_{C2}. The increments of point $Б$ potentials will be identical: $-\Delta u_Б = +\Delta u_B = +\Delta u_A$ if one considers that u_{C2} = const during working stroke time, while cathode follower gain K = 1. Therefore, the difference in potentials is $u_{AБ} = u_R = i_{зар} R = \text{const}$, i. e., capacitor C is charged by constant current $i_{зар} = \text{const}$. As a result, voltages u_C and $u_{вых}$ rise by a linear law. Condition $\tau_{зар} = RC > t_и$ must be satisfied in order that this law be retained further during the entire working stroke $t_и = t_{и.м}$. In actuality, the capacitor charging process will continue until the end of the working stroke if capacitor C during time $t_и$ does not succeed in charging to "source" voltage, i. e., if $U_{C\,макс} < u_{C2} \approx E_a$. But, since the rate of voltage u_C rise, in accordance with (IX.15) and (IX.30), equals $V \simeq \frac{E_a}{RC} \simeq \text{const}$, then $u_C \simeq \frac{E_a}{RC} t$ and $U_{C\,макс} \simeq \frac{E_a}{RC} t_и < E_a$, hence $t_и < RC$.

Significant nonlinearity arises only in the beginning of the working stroke at interval $\Delta t = t_1' - t_1$, given that this condition is satisfied. Actually, diode D still is unblanked during this interval and shunts resistance $R_к$. But, in accordance with (III.68), cathode follower gain turns out to be significantly less than unity, i. e., $+\Delta u_B < -\Delta u_Б$, given slight equivalent resistance in the cathode network. As a result, first, the rate of output voltage rise turns out to be much less than the rate of voltage u_C rise and, second, current $i_{зар}$ stabilization is insufficient ($u_{AБ} = \text{const}$) due to positive feedback weakening when K < 1 and voltages u_C and $u_{вых}$ are not linearized. A diode with the lowest possible value $E_{зап}$ must be used to decrease the initial nonlinear sector.

Recovery. At the moment the control pulse ceases t_2, triode L_1 unblanks and capacitor C rapidly discharges across it to initial voltage $U_{C\,нач}$. Here,

the potentials of points $B(u_C)$, $B(u_{вых})$, and A rapidly decrease by the law of exponents. Diode D unblanks at the end of this process, at moment t_3, when /388 potential u_A drops virtually to its initial value (it will become equal to E_a + $E_{зап}$). Capacitor C_2 is replenished after this along network $+E_a$, diode D, C_2, $R_{вых.}$, $-E_a$ (chassis) to initial voltage $U_{C_2\,max} \approx E_a$. Thus, capacitor C_2 replenishment begins after capacitor C discharging essentially ends. In the main, the time of capacitor C_2 replenishment across the diode determines circuit recovery time since $\tau_{разр} = CR_{вых} \ll \tau_{зар2} = C_2(R_i - R_{вых.})$:

$$t_в \approx 3\tau_{зар2}$$

Sufficiently-large resistance $R_к$ is selected to increase cathode follower gain. Therefore, the triode L_2 operating point following capacitor C discharge is established at the initial nonlinear sector of this triode's characteristic close to blanking voltage (see Figure III.23 and Exercise III.9). This leads to onset of additional nonlinear distortions at the beginning of the working stroke. In addition, at moment t_3, when diode D unblanks, initial capacitor C_2 replenishment current, passing across resistance $R_к$, will increase L_2 cathode potential by magnitude $\Delta U_к = \Delta U_{C_2} = E_{зап} - U_{C_2\,max}$. Triode L_2 will blank if the magnitude of this step exceeds value $E_{зап2} - U_{C_2\,min}$. In this case, right up until it unblanks, resistance $R_к \gg R_{вых.}$ will enter the C_2 charging circuit instead of cathode follower output resistance $R_{вых.} \approx \frac{1}{S_2}$, resulting in a rise in circuit recovery time. This can lead to capacitor C_2 not succeeding in being replenished fully during the resting time between control pulses, given a slight control pulse duty ratio. A voltage $U_{C_2\,max}$ decrease leads to reduction in the rate of output voltage rise during the working stroke and, consequently, that of saw amplitude as well. The "lower" end of resistance $R_к$ often is connected to the negative voltage source $E_к < 0$ (see the next circuit in Figure IX.19) rather than to chassis in order to eliminate these undesirable phenomena. Since this is equivalent to supplying positive bias $E_к$ to cathode follower grid, then its operating point in the initial mode shifts to the linear sector of the characteristic, the initial value of its current rises, and triode L_2 does not blank at moment t_3.

Ratios (IX.31) determine circuit output voltage parameters. However, the resultant nonlinearity factor is greater than value $k_н = \frac{t_и}{2\tau_1}(1 - k'$ mainly because

"source" voltage u_{C2} during a forward stroke decreases somewhat. Realistically, value β is at least 0.5%.

EXERCISE IX.11 /389

How will the output voltage parameters of the examined circuit [illegible] change when resistance R increases? Draw the output voltage curve when this resistance increases by a factor of 2. (Page 501)

3. Linearly-Rising Voltage Generator Circuit Variant With Improved Linearity

A variant of the previous GPN circuit with additional output voltage nonlinearity compensation and voltage curves at characteristic points are depicted in Figure

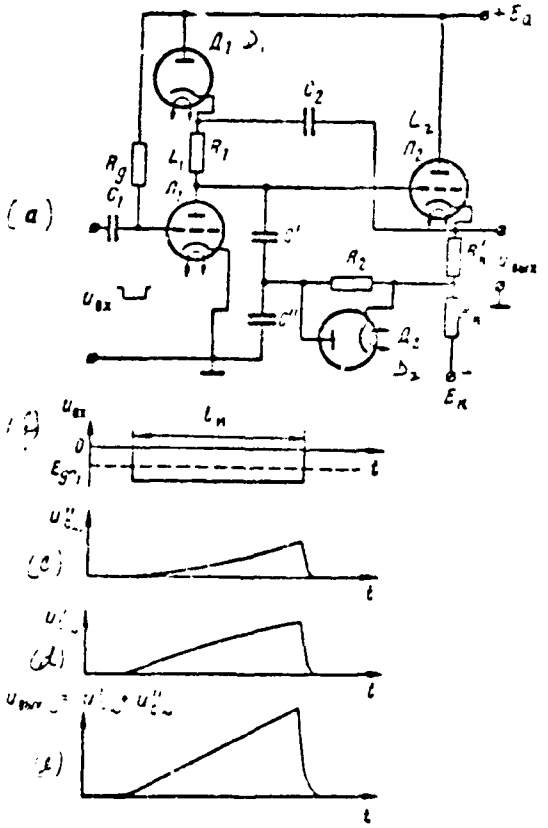


Figure IX.13. Variant of the Previous GPN Circuit (Figure IX.18) With Improved Linearity.

IX.19. The circuit differs from its predecessor (Figure IX.18) in that /390 charging capacitor C is replaced by two series-connected capacitors C' and C": $C = \frac{C'C''}{C'+C''}$. Part of the output voltage $u'_{вых} = \frac{u_{вых}}{R_к - R'_к} R'_к$ is supplied across resistance R_2 to capacitor C" with resistance $R'_к$, which is included in the cathode follower load $R_к = R_к - R'_к$.

We will assume that voltage $u_{вых}$ during the working stroke rises by a strictly linear law. Then, voltage $u'_{вых} = Kt_{вых}t$, where K -- proportional factor, will rise by the identical law. This voltage is applied to integrator C". One may consider, if the time constant of this network is sufficiently great: $\tau_2 = R_2C'' \gg t_1$, that, under the stimulus of voltage $u'_{вых}$, its output voltage will rise in proportion to the integral of the input voltage: $u''_C = \frac{1}{\tau_2}\int Kt_{вых}dt = \frac{K}{\tau_2}t_{вых}^2$, i. e., by the square law.

Actually, capacitor C" also is charged by capacitor C_2 discharging current, while if the integrator was absent ($R_2 = \infty$), the voltage u''_C would rise by an exponential curve with a decreasing rate while this current is flowing. It is possible to select the ratios among circuit parameters (C', C", $R_к$, $R'_к$), so that, as a result of the total charging of capacitor C" under the influence of voltages $u'_{вых}$ and u_{C2}, the square relationship would predominate all the same over the exponential and resultant voltage u''_C will increase at an increasing rate (Figure IX.19c). Voltage u'_C, just as previously, rises under the influence of voltage u_{C2} by the law of exponents (Figure IX.19d). Therefore, total voltage $u_C = u'_C + u''_C$ and, consequently, circuit output voltage as well, are linearized significantly (Figure IX.19e). The circuit makes it possible to reduce value $\beta_к$ to 0.1%.

EXERCISE IX.12

a) Why is it necessary to divide resistance $R_к$ into two resistances $R_к$ and $R'_к$? Examine individually where $R_к = 0$ and $R'_к = 0$?

b) What is the purpose of diode D_2? (Page 502)

§ 5. SAWTOOTH GENERATORS WITH COMPENSATING NEGATIVE VOLTAGE FEEDBACK

1. Sawtooth Voltage Linearization Principle Using Negative Feedback

This method of sawtooth voltage linearization basically is similar to the previous method: capacitor charging current $i_C = \frac{E - u_C - u_k}{R} = \text{const}$, is stabilized with the aid of compensation voltage u_k equal to capacitor voltage u_C, but acting opposite in phase to it ($u_k = -u_C$), resulting, in accordance with (IX.16), in capacitor voltage rising by a linear law. The difference is that compensation voltage will be introduced into the capacitor charging network via the negative feedback network. Here, if previously the potential of one capacitor plate is clamped at the "ground" potential level when positive feedback is used (see Figure

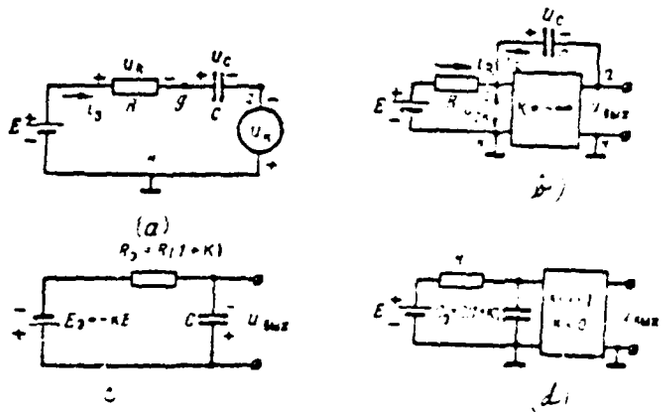


Figure IX.20. For Compensating Negative Voltage Feedback Gen.

IX.17), then, in this case, the negative "terminal" of charging voltage source E is "grounded" and that side of the capacitor [illegible] may be "grounded." Compensation voltage, just as was the case in the previous circuit, will be introduced into the charging network via an amplifier, which, as usual, must have one input and one output terminal "grounded" (connected to a common bus--chassis). Therefore, the capacitor charging circuit during the working stroke is depicted in Figure IX.20a, while only points g and k in this circuit [illegible] be amplifier input and points k output terminals.

An amplifier connection circuit corresponding to those conditions is /392 depicted in Figure IX.20b. Voltage u_C rises and voltage u_K decreases by a linear law during the capacitor charging process when compensation condition $u_K = -u_C$ is satisfied. The linearity of this voltage will deteriorate if sawtooth voltage is picked off the capacitor due to load impedance shunting the capacitor. Therefore, sawtooth voltage is picked off amplifier output $u_{вых} = u_K$ and falls linearly.

We will explain which requirements the amplifier must satisfy. An increase during the capacitor charging process of the potential of point g in Figure IX.20a must be compensated for by an identical decrease in point a potential in order to stabilize charging current. In this event, the difference in potentials is $u_{ga} = \text{const}$, while since $u_{g1} = E_1 - i_3 R$, then $i_3 = \text{const}$. (on the contrary, point a potential in Figure IX.17a must rise). Consequently, the amplifier must invert the input voltage phase, i. e., must have negative gain K. The feedback extant in the circuit is negative since the rise in point g potential elicits a decrease greater by a factor of $|K|$ in point a potential, which is transmitted in reverse across the capacitor to amplifier input.

But, what must the magnitude of amplifier gain $|K| = \left|\frac{\Delta u_{ga}}{\Delta u_{ga}}\right|$ be? Amplifier input voltage increments must be infinitely small: $\Delta u_{ga} = \Delta u_C + \Delta u_a = 0$ when $\Delta u_{ga} = -\Delta u_C$. Output voltage increments $\Delta u_{вых} = \Delta u_a = \Delta u_{ga}$ must be finite. But, this is only possible, given infinitely great gain magnitude $|K| = \left|\frac{\Delta u_{ga}}{\Delta u_{ga}}\right| = \infty$. Thus, an amplifier with gain $K = -\infty$ is required for an ideal linearly-falling voltage.

GPN circuits converted to an equivalent circuit shown in Figure IX.20b are referred to as electronic integrators. Actual amplifiers used in similar circuits have finite gain, with one striving to obtain the highest possible value $|K| \gg 1$. Several amplifying triode or pentode stages with plate loads often are used for this. The number of stages must be odd (one such stage may be used in the simplest case) in order to obtain overall negative gain since each such stage inverts the phase of its input voltage.

We will assume that the Figure IX.20b amplifier output voltage equals infinity (the amplfier operates without grid currents) $R_{вх} = \infty$; $i_{ga} = 0$ in order to find the law of circuit output voltage change $u_{final\ K}$. Then, currents flowing across resistance

R and across capacitor C must equal $i_R = i_C$. But, from Kirchhoff's second /393 law for the input loop encompassing source E, resistance R, and points g, k we have $E = u_R + u_{gk} = i_R R + u_{gk}$, hence $i_R = \frac{E - u_{gk}}{R}$. For the loop encompassing points k, g, capacitor C, points a, k we have $u_C = u_{gk} - u_{вых}$, hence $i_C = C\frac{du_C}{dt} = C\frac{d(u_{gk} - u_{вых})}{dt}$. Equating resultant expressions for currents i_R and i_C, we will get $\frac{E - u_{gk}}{R} = C\frac{d(u_{gk} - u_{вых})}{dt}$ or, considering that $u_{gk} = -\frac{u_{вых}}{K}$, we will get $\frac{E + \frac{u_{вых}}{K}}{R} = C\frac{d\left(-\frac{u_{вых}}{K} - u_{вых}\right)}{dt}$, hence $u_{вых} - RC(K+1)\frac{du_{вых}}{dt} = -KE$, or $\frac{du_{вых}}{dt} = -\frac{KE}{RC(K+1)} - \frac{u_{вых}}{RC(K+1)}$. Solution of this equation for zero initial conditions takes the form

$$u_{вых} = u_C = -KE\left[1 - e^{-\frac{t}{RC(K+1)}}\right]. \qquad (IX.32)$$

The Figure IX.20c equivalent circuit corresponds to expression (IX.32).

Thus, this method of sawtooth voltage linearization is equivalent tc an increase by a factor of $|K|$ in extant charging voltage drop (given a simultaneous change in its polarity) and an increase by a factor of K + 1 in the equivalent charging network time constant:

$$\Delta E_э = E_э = -KE;\ \tau_э = RC(K+1). \qquad (IX.33)$$

In accordance with this, based on Figure IX.20d the integrator may be represented also in the form of a series-connected R-C integrator with equivalent time constant $\tau_э = RC(1 + K)$ and an inertia-free sign inverter with high negative gain.

Based on (IX.8a, IX.12, IX.13, and IX.14) and considering (IX.33) for the given sawtooth voltage linearization method we will get

$$\beta_э = \frac{t_э}{RC(K+1)};\ U_э = KE\beta_э;\ i_э = K\beta_н;\ \beta_{н\,макс} = \frac{1}{1+K}. \qquad (IX.34)$$

It follows from these expressions that the greater the amplifier gain magnitude (for an ideal integrator where $K = -\infty$, $\beta_н = 0$), the greater the sawtooth voltage linearity. Given assigned nonlinearity factor value $\beta_н = \text{const}$, sawtooth voltage

amplitude U_t and source voltage utilization factor ξ_a rise by a factor of K compared to a conventional R-C integrator.

Essentially, a $\beta_н$ value on the order of tenths or hundredths of a /394 percent is possible if amplifier gain comprises several hundred percent.

EXERCISE IX.13

a) Explain why Figure IX.20b circuit capacitor charging current is kept almost constant when there is a finite, but sufficiently high, negative K.

b) Plot the following voltage curves on one graph: u_C -- capacitor voltage when it charges across a resistance, $u_{вх}$ -- at amplifier input, and $-u_{вых}$ -- at amplifier output for capacitor charging in the integrator circuit (Figure IX.20b), given identical C and R values. What determines the rate of change at the beginning of the working stroke and linearity for each of these voltages? For plotting convenience, assume that $K \approx K + 1 = -10$.

c) What must the K value be in a circuit using compensating negative feedback (Figure IX.20b) in order to obtain, all other things being equal, that degree of sawtooth voltage linearity found in a circuit using compensating positive feedback (Figure IX.17b) where K = 0.95? (Page 502)

As follows from Figure IX.20a, b, and d, there is no requirement to use an independent (insulated from ground) charging voltage source E when using negative feedback GPN since the negative terminal of this source is "grounded." Therefore, realization of such GPN essentially is simpler than positive feedback GPN. As a rule, amplifier plate voltage source E_a, whose "minus" as usual is "grounded," is used as source E.

There is a multitude of various practical negative feedback GPN circuits (in particular, widely-used phantastron circuits, which will be examined below, fall into this category). The basic characteristic features of these circuits are presence of an inverting amplifier with high gain (usually a pentode) and integrating elements: resistance R in the amplifier input network and negative feedback capacitor C connecting amplifier output (directly or via a cathode follower)

with its input. Here, any GPN circuit operating on this principle may be converted to the Figure IX.20b equivalent integrator circuit for the operating stage (the period when the output voltage working stroke is shaped), while ratios (IX.34) determine its output voltage parameters.

2. Externally-Controlled Pentode Linearly-Falling Voltage Generator

The generator circuit and the curves of the voltages at its characteristic points are depicted in Figure IX.21. An amplifier with plate load R_a and large

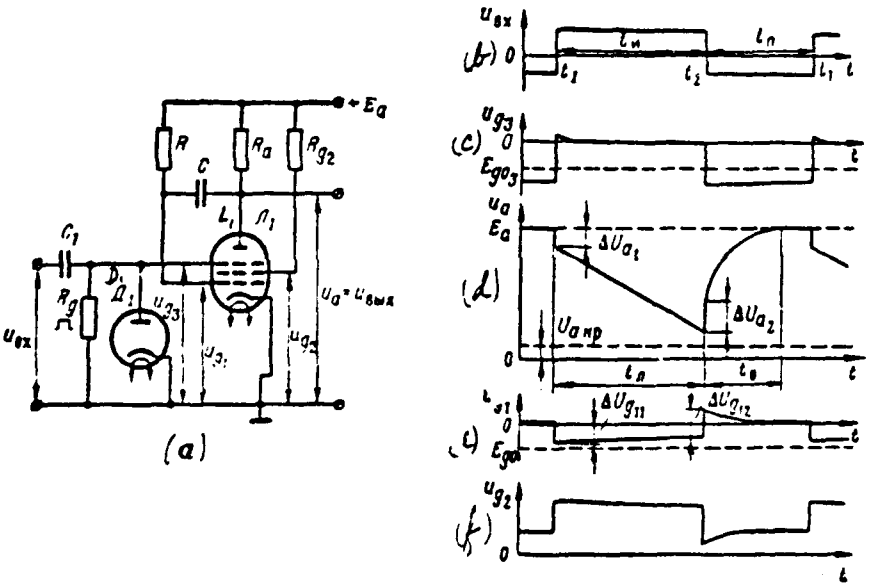


Figure IX.21. Pentode Linearly-Falling Voltage Generator in the External Control Mode.

gain $|K| = SR_a \gg 1$ is assembled on pentode L_1. A pentode screen grid controls the circuit: positive-polarity control pulses (Figure IX.21b) are supplied /395

across transient network C_1R_g to this grid. Diode D_1, which is a control pulse zero upper clamp, is connected at the output of this network. Circuit output voltage is picked off pentode plate load impedance R_a: $u_{вых} = u_a$.

EXERCISE IX.14

Compare the Figure IX.20b and IX.21 circuits. In the latter, find integrating network elements, trace the feedback network, and indicate that the feedback is negative. What voltage in this circuit is integrated to obtain the output voltage working stroke? (Page 504)

Input pulse amplitude must exceed pentode blanking voltage for circuit control, i. e., based on plate current $U_{вх} > |E_{гр}|$. Voltage u_{g3} essentially equals zero as a result of diode D_1 clamping action while the pulses are active, this voltage is negative during resting times due to dynamic bias in capacitor C_1, and it equals pulse amplitude (IX.21c). Therefore, the pentode is unblanked while the pulses are active and is blanked with respect to plate current during resting times. Constant negative bias $E_{g3} < E_{go3}$ is supplied to the suppressor grid if dynamic bias does not provide for pentode blanking with respect to suppressor grid /396 during resting times (given a high pulse duty ratio, for example).

The circuit operates in the following way.

Initial equilibrium state ($t < t_1$). The pentode is blanked with respect to plate current in the initial state by negative suppressor grid voltage $U_{go3} < E_{go3}$ and $i_a = 0$. Capacitor recharging voltage also is absent ($i_C = 0$) since capacitor C voltage does not change in the equilibrium state. Therefore, current $i_{Ra} = i_a + i_C = 0$ does not flow across plate load impedance R_a, there is no voltage drop across this resistance, and plate voltage equals source voltage $U_{ao} = E_a - i_{Ra}R_a = E_a$. The control grid is connected across resistance R to bus $+E_a$. Therefore, the pentode is unblanked with respect to cathode current, which, where $i_a = 0$, comprises control and screen grid currents: $i_к = i_{g1} + i_{g2}$. Resistance R usually is on the order of unities of megohms ($R \gg R_{g2}$). Therefore, screen grid current prevails: $i_{g2} \gg i_{g1}$ and $i_к \approx i_{g2}$.

Control grid current flows along the network $+E_a$, resistance R, control

grid--cathode path, chassis ($-E_a$). Essentially, the entire voltage drop in this network occurs at large resistance R ($R \gg r_{i*}$) and control grid potential only slightly exceeds cathode potential $U_{glo} \approx 0$.*

Screen grid current flows along network $+E_a$, resistance R_{g2}, screen grid--cathode path, chassis ($-E_a$). Here, the positive screen grid potential relative to cathode $U_{g2} = E_a - I_{g2}R_{g2} > 0$ turns out to be slight and usually comprises 30--50 V due to the significant voltage drop across resistance R_{g2}. Capacitor C is charged to initial voltage equalling the potential difference between pentode plate and control grid: $U_{Co} = U_{ao} - U_{glo} \approx E_a$ with a "plus" to plate.

Operating stage ($t_1 < t < t_2$). The circuit is triggered at moment t_1 during control pulse porch action. The pentode unblanks with respect to plate current at that moment. Positive plate current step $+\Delta I_{a1}$ causes a negative plate voltage step by magnitude $-\Delta U_{a1} = -\Delta I_{a1}R_a$. This step completely is transmitted across feedback capacitor C to the pentode control grid: $-\Delta U_{g11} = -\Delta U_{a1}$. However, the control grid potential reduction constrains the plate current rise, i. e., a plate voltage decrease. Therefore, positive feedback action at moment t_1 will lead to a reduction in the magnitude of the negative step of voltages u_a and u_{g1}, which may not exceed cutoff voltage E_{go1}.

$$\Delta U_{a1} = \Delta U_{g11} < |E_{go1}| \qquad \text{(IX.35)}$$

Actually, if $\Delta U_{g11} \geq |E_{g1}|$, then the pentode would be blanked with respect to control grid, which, however, cannot be since the reason for its blanking is absent here: $\Delta I_{a1} = 0$, $\Delta U_{a1} = \Delta U_{g11} = 0$. Thus, voltage u_{g1} will become negative, but will not reach cutoff voltage, immediately after the circuit is triggered.

It may be demonstrated (see Exercise IX.15) that, given sufficiently-high resistance R and R_a values,

$$\Delta U_{a1} = \Delta U_{g11} \approx |E_{go1}| \qquad \text{(IX.35a)}$$

*Grid clamping (voltage E_a = const in this case), already familiar to us, occu in the control grid network.

Where $u_{g1} < 0$, control grid current ceases ($i_{g1} = 0$). Therefore, pentode cathode current following triggering will comprise plate current and screen grid current $i_k = i_a + i_{g2}$.

Cathode current at the moment of triggering decreases with a jump due to the reduction in control grid potential. Plate current rises (appears) with a jump simultaneously at the moment of triggering. Both causes stipulate a spasmodic screen grid current decrease, which symbolically may be written $i_{g2} = i_a' - i_{g2}''$. As a result, screen grid voltage rises with a jump by magnitude $\Delta U_{g21} = \Delta I_{g21} R_{g2}$.

A quasistable state is established in the circuit while the control pulse is active following triggering, during the process of which linearly-falling voltage also is shaped at output. Here, the following processes transpire. Control grid potential (capacitor C left plate) will strive to rise since control grid current ceased. This leads to a rise in cathode and plate currents, i. e., to a reduction in plate potential (capacitor C right plate). As a result, immediately following triggering, the capacitor C recharging process begins across the pentode along network $+E_a$, resistance R, capacitor C, pentode plate--cathode, chassis ($-E_a$). Here, negative control grid potential is maintained by recharging current i_C since

$$u_{g1} = E_a - i_C R. \tag{IX.36}$$

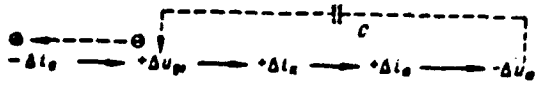
Ohm's law determines the initial value of this current if one considers the potential difference at the ends of resistance R, which arises immediately following triggering:

$$I_C = \frac{E_a + \Delta U_{g1}}{R} = \frac{E_a + \Delta U_a}{R} \approx \frac{E_a + |E_{g1}|}{R}. \tag{IX.37}$$

capacitor C

If there is no negative feedback, then current i_C during the recharging process will decrease from initial value I_C by an exponential curve with time constant $\tau = C(R + R_i) \approx CR(R \gg R_i)$. However, negative feedback constrains the current i_C decrease. Actually, the decrease in this current leads, in accordance with (IX.36), to a voltage u_{g1} increase and, consequently, to a cathode and plate current rise, i. e., to a plate voltage drop. But, the voltage u_a decrease across /398 capacitor C is transmitted to the control grid, constraining the voltage increase in it, i. e., a current i_C decrease. As a result, the decrease in this current is delayed to a greater degree, the greater the pentode gain $K = -\frac{\Delta u_a}{\Delta u_{g1}}$.

Symbolically, negative feedback action during a working stroke may be represented in the following way:



(IX.38)

It was demonstrated above that recharging current i_C stabilization by negative feedback leads to an increase in the capacitor C recharging time constant by a factor of K + 1. Therefore, voltage u_{g1} rises now by an exponential curve with equivalent time constant $\tau_1 = RC(K+1) \gg \tau = RC$, i.e., significantly more slowly. Voltage u_{g1} rises slightly and virtually linearly during the time of the working stroke if feedback action continues during the entire working stroke and condition $t_1 = t_2 \ll \tau_1$ is satisfied. Plate voltage, changing opposite in phase to grid voltage, also drops by an almost linear law corresponding to the initial sector of the exponential curve with identical time constant τ_1. However, the rate of this voltage's decrease and, consequently, the bounds of its change as well during the working stroke, is greater than voltage u_{g1} by a factor of K. Essentially, when the K value is large enough, voltage u_{g1} during the working stroke succeeds in rising only by fractions of volts, while plate voltage drops by hundreds of volts.

The slow rise in control grid voltage elicits an also slow (due to the cathode current rise) screen grid current i_{g2} rise. Therefore, screen grid voltage u_{g2} decreases somewhat during the working stroke.

The working stroke shaping process is explained additionally in Figure IX.22, where the pentode dynamic characteristic and the plate voltage curve obtained from it are plotted. (The latter does not differ from the Figure IX.21d curve, but is turned 90° relative to it to obtain clear coupling with the dynamic characteristic). A family of pentode static characteristics for the corresponding operating stages of potentials $u_{g2} \approx$ const; $u_{g3} \approx$ const and the ranging values $u_{g1} < 0$ during the working stroke is used to plot the dynamic characteristic. The special features of plotting a dynamic characteristic in this case are stipulated

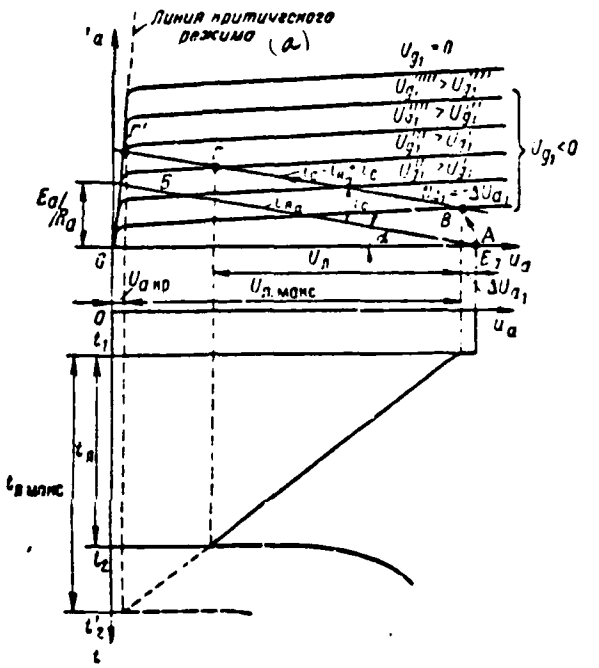


Figure IX.22. For Shaping the Output Voltage Working Stroke. (a) -- Criticality line.

because both plate load current i_{Ra} as well as capacitor recharging current i_C flow across the pentode in the operating stage:

$$i_a = i_{Ra} + i_C$$

Therefore, load line AB, which reflects the relationship of plate load current $i_{Ra} = \frac{E_a - u_a}{R_a}$ only to plate voltage, is plotted initially. This line is sloped to the X-axis at angle $\alpha = \text{arc tg}\, 1/R_a$ and intersects at the axes of segment $u_a = E_a$ $(i_a = 0)$ and $i_{Ra} = \frac{E_a}{R_a}$ $(u_a = 0)$. Recharging current i_C during the working stroke may be considered constant and equal to its initial value (IX.37) $i_C = I_C$. Then the relationship of overall plate current to plate voltage will be reflected by line $B\Gamma$ parallel to line AB, but raised above the latter by magnitude I_C.

Plate voltage corresponds to point A in the initial state (prior to triggering): $U_{ao} = E_a$ since the pentode is blanked with respect to plate current. The point representing circuit state at the moment of triggering (t_1) shifts with a jump from point A to point *B*, falling at the intersection of line *BГ* and the static characteristic of initial value $u_{g1} = -\Delta U_{g11}$ received with a jump. Plate voltage is reduced with a jump by magnitude $\Delta U_{a1} = \Delta U_{g11}$ accordingly. /400

Next, the depicted point gradually shifts to the left along line *BГ* during the capacitor C recharging process due to the voltage u_{g1} rise. Here, plate current rises and plate voltage drops by a linear law as a result of negative feedback action described above. However, this process may be continued until such time as the depicted point coincides with point *Г'*, falling on the criticality line, i. e., until control grid voltage exceeds value $u_{g1}^{\cdots}$. Dynamic saturation arrives when there is a further voltage u_{g1} rise: plate current no longer rises (pentode gain drops to zero) and plate voltage is clamped at minimum level $U_{a\,кр}$. Consequently, the latter must end before plate voltage drops to value $U_{a\,кр}$ in order for plate voltage linearity to be retained until the end of the working stroke (the Figure IX.22 working stroke ends at moment t_2, with representative point *Г* corresponding to this in the characteristic).*

The rate of plate voltage decrease in the linear sector, based on (IX.15) and considering (IX.33) (if the magnitude of the ΔU_{a1} jump is disregarded) equals

$$V \approx \frac{E_a}{RC}. \tag{IX.39}$$

Hence, resultant saw amplitude equals

$$U_{\text{п}} = V t_{\text{р}} = \frac{E_a}{RC} t_{\text{р}} \tag{IX.40}$$

It is evident from Figure IX.22 that the maximum possible saw amplitude results when the working stroke ends at moment t_2' (to which representative point *Г'* corresponds) equals

$$U_{\text{п макс}} = E_a - \Delta U_{a1} - U_{a\,кр}. \tag{IX.41}$$

*We will recall that control pulse duration $\tau_1 = t_{\text{р}}$ determines working stroke duration in the circuit.

Given large resistance, $R_{\text{н}}$, $U_{a\,\text{нр}} \ll E_a$; $\Delta U_{a1} \ll E_a$ и $U_{\text{з макс}} \approx E_a$. Therefore, resultant plate voltage utilization factor $\xi_{\text{макс}} = \frac{U_{\text{з макс}}}{E_a}$ is close to unity (essentially, $\xi_{\text{макс}} = 0.8\text{--}0.9$, given β_0 values on the order of tenths of a percent). Maximum working stroke duration corresponds to value $U_{\text{з макс}}$ and, in accordance with (IX.40), this duration equals

$$t_{\text{з макс}} = U_{\text{з макс}} \frac{RC}{E_a} \approx RC. \qquad \text{(IX.42)}$$

Recovery. We will return to Figure IX.21. The control pulse ceases /401 at moment t_2 and the pentode is blanked with respect to the suppressor grid. Capacitor C, discharged by the end of the working stroke to voltage $U_{C\,\text{мин}} \approx U_{\text{з мин}}$, must be charged to initial voltage $U_{Co} = E_a$ in connection with the increase in plate potential when the plate current ceases. The time for charging this capacitor also determines circuit recovery time.

Capacitor C at the recovery stage is charged by control grid current along network $+E_a$, resistance R_a, capacitor C, control grid--cathode path, $-E_a$ (chassis). The network time constant equals

$$\tau_{\text{зар}} = C(R_a + r_{g\text{к}1}) \approx CR_a. \qquad \text{(IX.43)}$$

At moment t_2 due to the voltage drop created by initial charging current in resistance $r_{g\text{к}1}$, control grid and plate potentials rise with a jump by magnitude

$$\Delta U_{g12} = \Delta U_{a2} = \frac{E_a - U_{a\,\text{мин}}}{R_a + r_{g\text{к}1}} r_{g\text{к}1} \approx E_a \frac{r_{g\text{к}1}}{R_a}. \qquad \text{(IX.44)}$$

Then, because charging current decreases by the law of exponents, control grid potential will drop by an exponential curve to initial value $U_{g1o} \approx 0$, while plate voltage rises by an exponential curve to source voltage E_a.

The charging time constant (IX.43) determines circuit recovery time and equals

$$t_в \approx 3\tau_{\text{зар}} = 3R_aC. \qquad \text{(IX.45)}$$

The control grid only controls screen grid current i_{g2} after the pentode blanks with respect to plate current. Since screen grid potential changes opposite

in phase with this current ($u_{g2} = E_a - i_{g2}R_{g2}$), then an exponential current i_{g2} bump and negative exponential voltage u_{g2} excursion arise at moment t_2. The duration of this excursion also corresponds to recovery time $t_в$. The circuit will remain in the initial state following recovery until arrival of the subsequent control pulse.

Basic circuit parameter selection. Pentode L_1 must have high plate-grid transconductance S in order to have high gain. It is desirable to have a low blanking voltage in the third grid in order to decrease control pulse amplitude. The pentode is blanked with respect to plate current during switching pulse resting times and significant plate current virtually totally (less slight control grid current) flows across the screen grid, causing it to heat up. Therefore, safe power dissipation with respect to the screen grid must be as great as possible.* In practice, 6Zh2P, 6Zh5P, and 6Zh4 pentodes usually are used in this type /402 of GPN circuit. Large R_a resistance must be selected in order to obtain high gain. However, an extraordinary R_a increase still does not lead to a rise in K due to the decrease in plate current transconductance. In addition, the resistance R_a magnitude, in accordance with (IX.45), impacts upon circuit recovery time. Essentially, resistance R_a ranges from 0.2—1 megohm. Capacitor C and resistance R are integrator elements, whose time constant RC must be as high as possible to obtain output voltage linearity. However, an increase in this time constant leads, in accordance with (IX.39) and (IX.40), to a decrease in the rate of output voltage change and of its amplitude. This circumstance also is decisive for selection of the magnitude of the RC product.

In accordance with (IX.45), capacitance C must be minimal to reduce recovery time. Here, however, it significantly must exceed circuit stray output capacitance $C_т = C_{вых} + C_м$, having a magnitude of 10—15 pf.

Given the selected capacitance C magnitude, the requisite RC value is insured by the resistance R selection. The decrease in current i_C constrains the maximum R value and, consequently, pentode plate current $i_a = i_{Ra} + i_C$. As noted above,

*An additional 5—10 kilohms of damping resistance sometimes is connected in series to the screen grid network to facilitate the heat situation, given a high switching pulse duty ratio.

the plate current decrease leads to a decrease in the slope of the plate-grid characteristic sector used. A current i_{g1} rise constrains minimum value R and, consequently, dissipation power in the pentode control grid. Selected capacitance C usually ranges from hundreds or thousands of pF, while resistance R ranges from hundreds of kilohms to tens of megohms.

EXERCISE IX.15

a) Attempt to prove ratio (IX.35a) for the magnitude of the voltage u_{g1} and u_a jump at the moment of triggering.

b) We know that voltages u_{g1} and u_a change opposite in phase for a pentode unblanked with respect to plate current. Therefore, control grid voltage must rise linearly to obtain linearly-falling plate voltage (see Figure IX.21 curves). However, on the other hand, in accordance with (IX.16), capacitor recharging current during the working stroke must be strictly constant $i_C = I_C = \text{const}$ to obtain ideal linear output voltage. But, in this case, control grid voltage $u_{g1} = E_a - i_C R$ also will be constant. Consequently, linearly-falling plate voltage must be obtained when control grid voltage is constant. How do you explain this contradiction?

c) Imagine that Figure IX.21 resistance R_1 (sufficiently slight so as not to disrupt circuit operation) is connected to the pentode cathode network. Draw the shape of the voltage which may be obtained across this resistance. (Page 504)

This circuit requires supply of control pulses of great amplitude and has a long recovery time. The first shortcoming is caused because precise clamping of the initial output voltage value at level E_a requires a complete absence /403 of pentode plate current in the initial state. Reliable pentode blanking with respect to the third grid occurs when negative bias $U_{g3} = -U_{з1}$ of approximately -100 ÷ -200 V.

The second drawback stems from the fact that plate load impedance R_a is included in ratio (IX.45), which must be large in order to obtain high gain, i. e., high output voltage linearity. The control pulse duty ratio must be at least 5—10 due to the long recovery time.

3. Linearly-Falling Voltage Generator Circuit Variants With Reduced Recovery Time

Clamping diode GPN. The generator circuit and output voltage curve are depicted in Figure IX.23. The circuit differs from the Figure IX.21a circuit GPN only in the

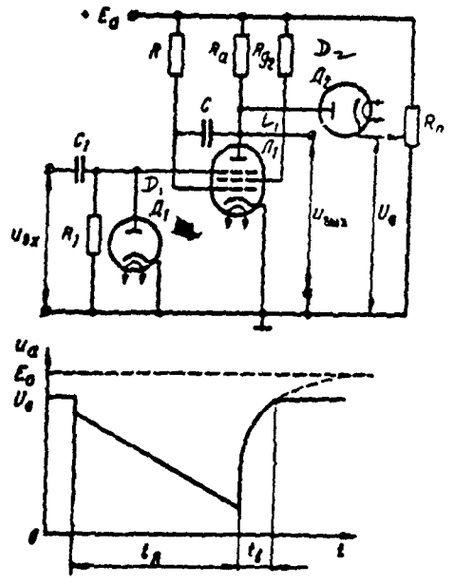


Figure IX.23. Clamping Diode Linearly-Falling Voltage Generator.

presence of clamping diode D_2. Positive voltage $U_0 < E_a$ is applied from potentiometer R_n to the cathode of this diode.

Diode D_2 is unblanked in the initial state since diode plate is connected across resistance R_a to bus $+E_a$ and there is no pentode plate current prior to circuit triggering. This diode's current flows along network $+E_a$, resistance R_a, diode D_2, the "lower" portion of resistance R_n, chassis $(-E_a)$. Conducting diode internal resistance is slight ($R_{i2} \ll R_a$) and, due to the voltage drop across resistance R_a, the potential of its plate (and, consequently, of pentode plate) is clamped at the level of its cathode potential $U_{ac} = U_0$. Capacitor C is charged to this voltage in the initial state.

Pentode plate voltage decreases with a jump at the moment of triggering, /404 i. e., diode plate potential will become less than the potential of its cathode and diode D_2 blanks. Diode D_2 remains blanked during the entire operating stage since pentode plate voltage then decreases and does not impact upon the linearly-falling voltage shaping process. Capacitor C begins to charge following control pulse cessation and plate voltage rises along an exponential curve with previous time constant $\tau_{вых} = R_a C$, striving towards level E_a (Figure IX.23 dotted line curve). However, as soon as plate voltage achieves value U_o, diode D_2 unblanks and the further rise of this voltage ceases. As a result, recovery time $t_в$ decreases significantly due to severing of the "tail" of the voltage u_a exponential curve. The sawtooth voltage amplitude decrease due to the decrease in its initial level is a shortcoming of this method.* However, reducing this level by no more than 20% ($U_o \geq 0.8E_a$) results in a recovery time decrease by a factor of 1—3.

Use of a clamping diode also makes a decrease in control pulse amplitude possible.

EXERCISE IX.16

a) What type circuit is formed with the aid of diode D_2 (Figure IX.23): clamping, parallel, or series diode limiter?

b) Why does use of a clamping diode $Д_з$ make a decrease in control pulse amplitude possible? (Page 505)

Cathode follower GPN. The generator circuit and output voltage curve are depicted in Figure IX.24. The circuit differs from the IX.21a GPN circuit only by presence of a cathode follower assembled on triode L_2. Pentode L_1 plate voltage is supplied to cathode follower input, resulting in triode L_2 always being unblanked. Capacitor C is connected between the pentode control grid and cathode follower output (but not the pentode plate). Therefore, the negative feedback circuit connecting pentode plate with its control grid, is closed across the cathode follower.

*Since plate voltage U_{min}, minimum level here remains as before, then the decrease in plate voltage initial level leads also to a reduction in maximum working stroke duration $t_{в\ max}$ (value U_o must replace value E_a in formula (IX.42)).

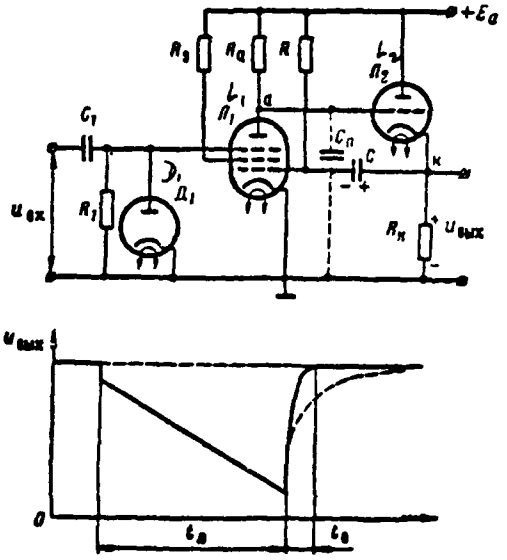


Figure IX.24. Cathode Follower Linearly-Falling Voltage Generator.

Resistance $R_к$ is sufficiently large so that the cathode follower transfer constant will be close to unity. In this event, potentials of points a and k change to an identical degree (these points notionally may be connected for voltage u_a and $u_к$ increments). Therefore, connection of the cathode follower does not change the nature of the processes in the operating stage and essentially does not have a deleterious effect on output voltage working stroke linearity. However, capacitor C is charged following control pulse cessation by pentode L_1 control grid /405 current across slight cathode follower output resistance $R_{вых\ к} \approx \frac{1}{S_2}$, rather than across large resistance R_a, along network $+E_a$, triode L_2, capacitor C, pentode control grid--cathode path, chassis $(-E_a)$. As a result, capacitor C charging time constant turns out to equal

$$\tau_{зар} = (R_{вых\ к} + r_{гк1})\,C, \qquad (IX.46)$$

i. e., decreases compared to time constant (IX.43) almost at ratio $R_a/R_{вых\ ка}$ (essentially by a factor of 1,000). Circuit recovery time is reduced accordingly

$$t_в \approx 3\tau_{зар} = 3(R_{вых\ ка} + r_{i2l})C. \qquad (IX.46a)$$

Given slight magnitudes of resistance $R_{вых\ ка}$ and capacitor C capacitance, charging of the latter along the aforementioned network may cease earlier than charging of stray capacitance $C_a = C_{a1} + C_м + C_{вх\ ка}$, which shunts pentode output (dotted line in the Figure IX.24 circuit). This capacitance is charged during circuit recovery across resistance R_a. In this event, stray capacitance charging duration determines recovery time

$$t_в \approx 3R_a C_a. \qquad (IX.46b)$$

Circuit output voltage is picked off the cathode follower load. Thus, /406 besides reducing recovery time, the cathode follower plays the role of buffer amplifier. Having high input resistance, it does not shunt pentode output. In addition, the circuit may operate a low-resistance load since cathode follower output resistance is slight.

EXERCISE IX.17

Will sawtooth voltage be shaped at pentode plate in the Figure IX.24 circuit if triode L_2 completely lost emission ($i_{a2} = 0$)? Draw the u_{g3}, u_{a1}, u_{g1}, and $u_{вых}$ voltage curves for this instance. Disregard the influence of stray capacitance C_a .

(Page 506)

4. Monostable Screen Grid Coupling Phantastron

Square positive-polarity switching pulses from an external source were supplied to pentode suppressor grid in the external control mode of the GPN circuit depicted in Figure IX.12a. Output pulse working stroke duration $t_и = t_в$ determined the duration of these pulses. However, the circuit itself shaped pulses of identical shape, polarity, and duration in the pentode screen grid (Figure IX.12f). They also may be used as switching pulses if supplied to the suppressor grid.

Negative voltage feedback linearly-falling voltage generators, whose own circuitry produces switching pulses, are referred to as phantastrons. The circuit is referred to as a screen grid coupling circuit if the pentode suppressor grid is coupled to the screen grid in the phantastron circuit.* Just as is the case for any trigger circuit, in order for a phantastron to operate in a monostable mode, there is a requirement to provide:

-- an initial state of stable equilibrium (prior to triggering);

-- the possibility of forming two spasmodic changes (avalanche-like processes): one during triggering at the beginning of the working stroke for circuit "reversal" while the trigger pulse is active and a second at the end of the working stroke for spontaneous circuit return to the initial state.

Positive feedback, absent in the Figure IX.21a GPN circuit, must be active in order to obtain avalanche-like processes in a phantastron.** Positive /407 feedback is created due to the transitron effect, the essence of which was examined in Chapter III, § 2 (see Figure III.6). We will recall that the transitron effect is based upon the redistribution of overall pentode cathode current between plate and screen grid during a suppressor grid potential change and onset of screen grid current as a result of this falling sector of the characteristic $i_{g2} = \Phi(u_{g3})$. Any voltage u_{g3} increment within this sector leads to a cophasal (of the same sign) voltage u_{g2} increment. (Actually, voltage u_{g3} rises, for example, then current i_{g2} decreases, while screen grid voltage $u_{g2} = E_a - i_{g2}R_{g2}$ also rises.) The resultant u_{g2} increment arising as a result of the initial u_{g3} change, acting in phase backwards on the suppressor grid, maintains the initial u_{g3} change if the screen grid is coupled with the suppressor grid. The result is a closed positive feedback network, whose action may be depicted symbolically as:

$$\pm\Delta u_{g3} \longrightarrow \pm\Delta i_a \longrightarrow \pm\Delta i_{g2} \longrightarrow \pm\Delta u_{g2} \qquad \text{(IX.47)}$$

Gain is this loop equals $K_{g2} = \frac{\Delta u_{g2}}{\Delta u_{g3}}$ and will depend on the slope of the falling sector of the screen current characteristic $S_{g2} = -\frac{\Delta i_{g2}}{\Delta u_{g2}}$. The self-excitation

*It might be more precise to call it a circuit with suppressor and screen grid coupling.

**In addition, in accordance with the principle being examined for shaping linearly-falling voltage in a phantastron, negative feedback between pentode plate and control grid as usual must be active during the operating stage.

condition will be satisfied when $K_{g2} \gtrsim 1$, i. e., any u_{g3} increment will lead to onset of an avalanche-like process.

The circuit for a phantastron in the monostable mode with screen grid coupling and voltage curves in its characteristic points are depicted in Figure IX.25.

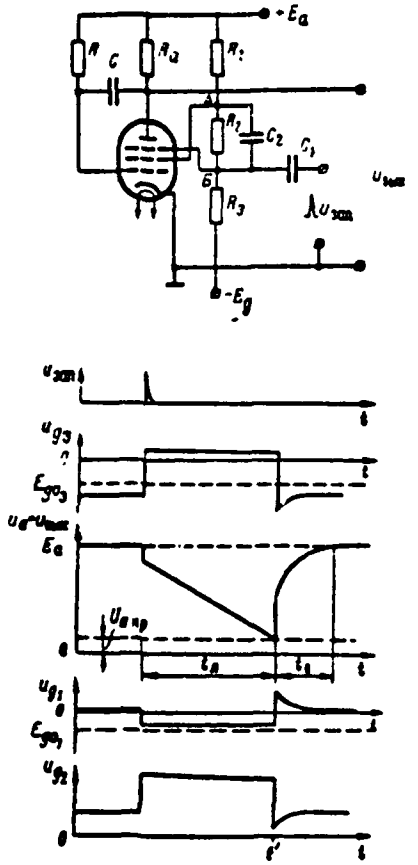


Figure IX.25. Monostable Screen Grid Coupling Phantastron.

Resistance R and capacitor C, as usual, are integrator elements. Divider R_1, R_2, R_3 connected between buses $+E_a$ and $-E_a$ supply screen and suppressor grid initial potentials. The suppressor grid is coupled with the screen grid across resistance R_2 shunted by accelerating capacitance C_2. The purpose of this capacitance is identical to that in flip-flop circuits (see Chapter VI, § 2). Short positive-

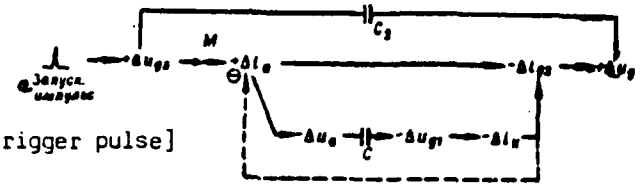
polarity pulses supplied to suppressor grid across transient capacitor C_1 trigger the circuit. Output voltage is picked off pentode plate.

We will examine circuit operation.

Initial state. Divider R_1, R_2, R_3 parameters and negative bias E_g magnitude are selected so that the potential of point A, to which the screen grid is connected, is positive and sufficiently large, while the potential of point $Б$, to which the suppressor grid is connected, is negative and exceeds in magnitude pentode blanking with respect to suppressor grid (see Exercise IX.18). Therefore, /408 the pentode is blanked with respect to plate current and plate voltage equals E_a. Control grid potential approximates zero due to the flow of control grid current across large resistance R. Here, significant cathode current virtually completely (less slight current i_{g1}) flows along the screen grid network $i_к \approx i_{g2}$ and screen grid potential u_{g2} is reduced to a slight positive magnitude due to the voltage drop across resistance R_1. This is a stable circuit state and continues until trigger pulse arrival.*

Circuit triggering. The pentode unblanks with respect to plate current while a positive trigger pulse acts upon the suppressor grid. Onset of plate current leads to action of the aforementioned positive feedback loop (IX.47) based on the transitron effect: current i_{g2} decreases and there is an increase in voltage u_{g2}, which across accelerating capacitance C_2 is transmitted backwards to the suppressor grid. A parallel branch, amplifying loop action, is connected to the loop in sector $i_a \rightarrow i_{g2}$. This branch arises because a plate current rise means a plate voltage reduction, which is transmitted across capacitor C to the control grid and leads to a reduction in cathode current $i_к = i_a + i_{g2}$. Therefore, current i_{g2} is reduced for two reasons: not only due to the current i_a rise, but /409 also due to the current $i_к$ reduction. The avalanche-like process at the moment of triggering symbolically may be depicted in the following manner:

*Thus, the circuit state prior to triggering does not differ from a circuit with external control, with the exception that, in the circuit being examined, a special negative bias voltage source $E_g < 0$ is used for pentode blanking with respect to the suppressor grid.



[KEY: (a) -- Trigger pulse]

(IX.48)

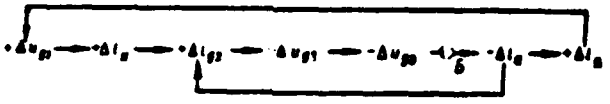
The avalanche-like process ceases when voltage u_{g3} with a jump achieves a slight positive value at which the suppressor grid loses its controlling properties due to a decrease in transconductance $i_a = \Phi(u_{g3})$ and $i_{g2} = \Psi(u_{g3})$ (see Figure III.6) and positive feedback loop gain drops. This is equivalent in symbolic rendition (IX.48) to disruption of the positive feedback loop in the common sector at point M. In addition, along with the positive feedback, negative feedback exists in the circuit and it exerts a braking influence at the moment of triggering (depicted by the dotted line in the symbolic rendition). Actually, the current i_k decrease in and of itself facilitates a decrease rather than an increase in current i_a, i. e., an increase in voltages u_a and u_{g1}, while the latter leads to a rise in current i_k, i. e., will constrain its decrease. The effectiveness of negative feedback action rises due to the plate current rise resulting from the increase in gain with respect to the plate network. It is evident that positive feedback action may prevail over negative feedback action only until such time that the rate of current i_{g2} decrease exceeds the rate of current i_k decrease since, here, a current i_a rise is possible. The current i_k decrease ceases when this condition is violated since it could lead already to a current i_a decrease, i. e., to a rise in voltages u_a and u_{g1}. Therefore, the avalanche-like process ends.

Operating stage. Only the negative feedback network (IX.38) is active in the circuit at the moment of triggering following reversal. Just as was the case in the Figure IX.21 circuit, the same processes occur here involving capacitance C recharging by constant current across the unblanked triode. The only difference is that voltage u_{g3} gradually is reduced during the working stroke due to the slight rise in suppressor grid current because of the cathode current increase.* Otherwise, operating stage voltage curves do not differ from the corresponding

*This voltage may be clamped at level $u_{g3} = 0$ if a zero upper clamp (analogous to the Figure IX.21 circuit) is connected parallel to the suppressor grid--cathode path.

Figure IX.21 curves. The operating stage continues until plate voltage, /410 decreasing by a linear law, reaches minimum (critical) value $U_{a\,кр}$.

Recovery. Pentode amplifying qualities disappear when plate voltage reaches value $U_{a\,кр}$, the negative feedback network breaks, and voltage u_{g1} begins rapidly to rise with time constant $\tau = RC$ (see Exercise IX.18c). Here, the positive feedback loop closes: the voltage u_{g1} rise will lead to a current i_A increase and, since plate current no longer rises, to a current i_{g2} increase. The latter leads to a voltage u_{g2} decrease, which is transmitted to the suppressor grid across accelerating capacitance C_2. The voltage u_{g3} decrease causes a current i_a decrease, i. e., a plate voltage increase, which is transmitted backwards to the control grid across capacitance C. The action of this loop is amplified due to the transitron effect: a current i_a decrease when current i_A increases forces a current i_{g2} rise. As a result, a second avalanche-like process arises in the circuit. This process symbolically may be written in the form



(IX.49)

Positive feedback action ceases when voltage u_{g3} is reduced to pentode blanking voltage with respect to the suppressor grid E_{go3}, i. e., plate current disappears (in symbolic rendition (IX.49) this is equivalent to disruption of both loops in the common sector at point δ). Voltages u_a and u_{g1} rise with a jump by magnitude (IX.44) $\Delta U_{a2} \approx E_a \frac{r_{ai}}{R_a}$ as a result of the spasmodic cessation of plate current, while voltages u_{g2} and u_{g3} drop with a jump as a result of the positive plate current jump. Then, as was the case in the Figure IX.21 circuit, capacitor C charges along network $+E_a$, resistance R_a, capacitor C, control grid—cathode sector, chassis $(-E_a)$. As usual, the charging circuit time constant equals $\tau_{нар} \approx R_a C$ and, in accordance with (IX.45), determines circuit recovery time. The curves of the voltages in the recovery stage differ from the corresponding Figure IX.21 curves only in the voltage u_{g3} negative exponential excursion. This excursion is similar to the voltage u_{g2} exponential excursion and arises for the identical reason -- due to the current i_{g2} exponential bump. Actually, since screen and suppressor grids are connected to one divider, then the change in point A potential will be accompanied by an identical change in point δ potential (Figure IX.25).

Voltage u_{g3} takes on the initial negative value supplied from the divider upon conclusion of the recovery process.

A cathode follower connected as shown in Figure IX.24 may be used in /411 the circuit to reduce recovery time and the possibility of operating a low-resistance load.

Circuit triggering by pulses supplied to plate often is used along with the examined method of triggering with respect to the suppressor grid. This triggering method decreases trigger pulse amplitude several-fold. The physical processes in the circuit remain identical here.

EXERCISE IX.18

a) Compute initial voltages U_{g2} and U_{g3} in the Figure IX.25 phantastron if E_a = 300 V, E_a = -250 V, R_1 = 20 kilohm, R_2 = 75 kilohm, R_3 = 55 kilohm, I_{g2} = 3 mA.

b) What does working stroke duration τ_1 for the examined phantastron circuit equal?

c) How may one change (increase, for instance) working stroke duration τ_1 without changing recovery time τ_2 ? How will this impact upon output voltage linearity?

d) Draw a monostable screen grid coupling phantastron circuit with a cathode follower and triggered with respect to the plate network. Explain the triggering process. What must trigger pulse polarity be? Why must the amplitude of these pulses be less than when the phantastron is triggered directly with respect to the suppressor grid? (Page 506)

5. Variant Using a Phantastron as a Variable Pulse Delay Circuit

The monostable screen grid coupling phantastron examinec above often is used as a variable pulse delay circuit. The time delay obtained with the aid of such a circuit may be altered over a broad range — from several microseconds to several

milliseconds. Control voltage $u_{упр}$ supplied to circuit input provides the delay magnitude and it changes in proportion to the change in this voltage

$$\Delta t_з = K'_з \Delta u_{упр}, \qquad (IX.50)$$

where $K'_з \left[\frac{мксек}{в}\right]$ -- proportionality factor, referred to as delay control transconductance.*

A variant of such a circuit and the curves of voltages in its characteristic points are depicted in Figure IX.26. The circuit is a monostable cathode follower

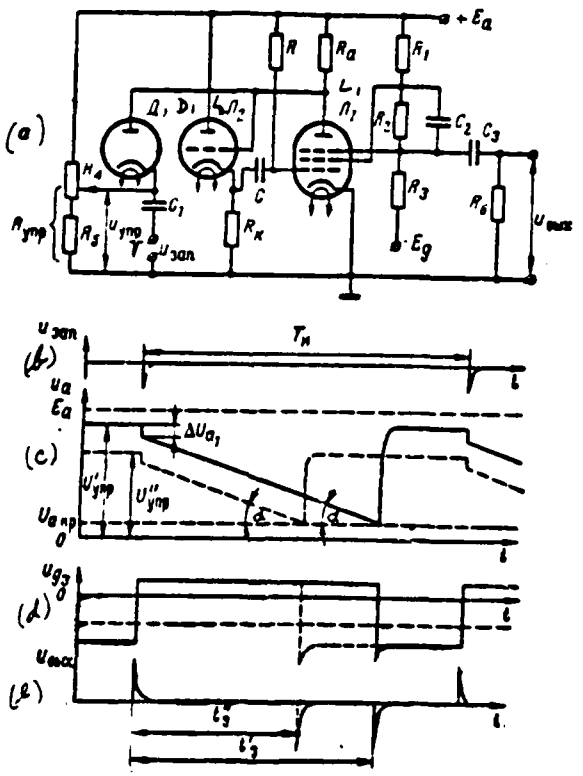


Figure IX.26. Variable Pulse Delay Circuit.

*Delay control transconductance $K'_з$ indicates how many microseconds delay time $t_з$ changes when control voltage changes 1 V.

phantastron (triode L_2) and clamping diode D_1. The cathode follower is connected as depicted in Figure IX.24 and will serve to reduce recovery time. The clamping diode is connected as depicted in Figure IX.23, but already will serve to clamp plate voltage initial level rather than to reduce recovery time and, at the /412 same time, is a trigger tube. Negative pulses with respect to the plate network trigger this circuit across this diode (see Exercise IX.18d).

Control voltage $u_{упр} < E_a$ is supplied to diode cathode from potentiometer R_4 of divider R_4, R_5, while negative-polarity trigger pulses are supplied across separating capacitor C_1. Output voltage is picked off pentode third grid across differentiator C_3R_6. In the initial state, the pentode, just as in Figure IX.25, is blanked with respect to the third grid by negative bias picked off divider R_1, R_2, R_3. Therefore, there is no pentode plate current ($i_a = 0$) and no voltage drop is created across resistance R_a. Diode D_1 [illegible]he initial state is unblanked since the potential of its plate connected to bus + alwa/s exceeds the potential of its cathode supplied from the potentiometer: $u_{ка} = u_{упр} < E_a$. Diode current /413 $i_д$ flows along network $+E_a$, resistance R_a, diode D_1, resistance $R_{упр}$ (into which the "lower" portion of resistance R_4 and resistance R_5 are introduced), chassis ($-E_a$). Here, the potential of connected diode and pentode plates is reduced by the magnitude of the voltage drop across resistance R_a and will become equal to $U_{a0} = E_a - i_д R_a$. Diode current

$$i_д = \frac{E_a - u_{упр}}{R_a + R_д + R_{упр}} \approx \frac{E_a - u_{упр}}{R_a}$$

($R_a \gg R_д + R_{упр}$, where $R_д$ -- unblanked diode internal resistance). Consequently,

$$U_{a0} \approx E_a - \frac{E_a - u_{упр}}{R_a} R_a = u_{упр} \qquad (IX.51)$$

-- initial phantastron plate voltage level equal to control voltage.

Rather than being supplied from a potentiometer, control voltage in practical circuits may be produced by the preceding electronic circuit. Then, resistance $R_{упр}$ should be understood to be the output resistance of this circuit's final stage. This resistance must be sufficiently low so that, as usual, condition $R_a \gg R_д + R_{упр}$

is satisfied, i. e., $U_{a0} \approx u_{упр}$. Therefore, a cathode follower is used as the stage off which control voltage is picked.

A positive-polarity trigger pulse reduces diode cathode potential, i. e., causes a brief current i_a increase. Here, a negative plate voltage u_a "bump" arises due to the increase in the voltage drop across resistance R_a. Next, the process we already have examined whereby the phantastron is triggered with respect to the plate network occurs: a negative plate voltage pulse across cathode follower L_2 and capacitor C acts upon the pentode control grid; pentode cathode current and, consequently, screen grid current as well, decrease, while screen grid potential rises; a positive voltage u_{g2} pulse is transmitted across capacitor C_2 to the third grid and unblanks the pentode with respect to plate current. A spasmodic plate voltage decrease by magnitude ΔU_{a1} occurs at the moment of triggering, resulting in plate voltage becoming less than control voltage. Here, diode D_1 plate potential will become less than the potential of its cathode and the diode blanks. Thus, immediately following triggering, diode D_1 cuts input networks off from the phantastron and these networks exert no further impact on its operation. A temporarily-stable circuit state occurs following triggering and linearly-falling voltage is shaped at plate during this state. The operating stage continues until such time that plate voltage attains critical value $U_{a кр}$. Therefore, the /414 sawtooth voltage amplitude equals

$$U_a = u_{упр} - \Delta U_{a1} - U_{a кр} \qquad (IX.52)$$

Circuit recovery to the initial state then occurs. The essence of the processes occurring during the working stroke and during circuit recovery is identical to that in the phantastron circuit examined in Figure IX.25.

As was the case for circuits examined previously (see Figures IX.21 and IX.25), a virtually square positive-polarity pulse is shaped in the third grid during the working stroke. This pulse acts upon differentiator C_3R_6 input (see Figure IX.26). A positive exponential pulse, corresponding to the moment of circuit triggering, and a negative exponential pulse, corresponding to the moment the working stroke ceases, arise at the output of this network. The negative pulse also is an output pulse: it turns out to be a pulse delayed relative to the moment

of circuit triggering by time $t_1 = t_1'$. Thus, the circuit-generated time delay equals working stroke duration.

The initial plate voltage level ($U_{a0} = u_{ynp}$) changes when control voltage changes. However, the rate of plate voltage decrease in the linear sector (saw slope), in accordance with (IX.39), remains as before: $v' \approx \frac{r_a}{RC} \approx \text{const}$. Nor does the minimum plate voltage level, from which circuit recovery begins, change: $U_{a\,min} = U_{a\,kp} = \text{const}$ (only the pentode characteristics and resistance R_a magnitude determine value $U_{a\,kp}$). Therefore, a control voltage changes will lead to a proportional change in working stroke time, i. e., delay time t_3. The relationship of Δt_3 to Δu_{ynp} clearly is explained in Figure IX.26c, d, e, where voltage curves for two control voltage values are presented: U''_{ynp} (solid line) and U'_{ynp} (dotted line).

EXERCISE IX.19

a) A square pulse from the third (or from the second) pentode grid, rather than sawtooth voltage shaped at plate is used in the examined circuit to obtain output voltage -- a delayed pulse. What is the significance here of plate voltage linearity?

b) Use circuit parameters to express delay control transconductance K_3 in ratio (IX.50).

c) How are maximum and minimum delay time obtained and what do they equal? Why has resistance R_5 been included?

d) How will presence of stray capacitances shunting the pentode plate--cathode and suppressor grid--cathode paths impact upon circuit operation?

e) What will be obtained at circuit output if positive-polarity rather /415 than negative-polarity trigger pulses act upon its input (on diode D_1 cathode)?

(Page 508)

*An analogous result will be obtained if a differentiated pulse of voltage from the screen grid is used as circuit output voltage: this pulse also has positive polarity and duration equalling t_3 .

6. Free-Running Screen Grid Coupling Phantastron

Examing the operation of a screen grid coupling phantastron circuit (Figure IX.25), we saw that this circuit remained in a state of stable equilibrium, provided by the supply of constant negative bias to the suppressor grid, prior to triggering. The circuit operating cycle began from the moment of triggering and ended by independent circuit return to the initial state. Trigger pulse action boiled down to pentode blanking with respect to the suppressor grid. Consequently, providing the circuit with automatic triggering -- spontaneous pentode blanking with respect to the suppressor grid upon completion of each cycle -- suffices to convert this circuit to the free-running mode.* In other words, there is a requirement to insure pentode blanking with respect to the suppressor grid only during circuit recovery time. This task will be accomplished if negative blanking pulses produced by the circuit itself act upon the suppressor grid, while each pulse must coincide with circuit recovery time. Automatic triggering then will occur at the moment each such pulse ceases (droops).

Where does one obtain these pulses? Examining Figure IX.25 voltage curves, we note that negative pulses of sufficient amplitudes with porches which, as is required, coincide with the moments the operating stage ceases (moment t'), are shaped at pentode screen grid. True, each such pulse continues right up to the next external triggering, which will be absent in the free-running mode. However, it is possible simply to clip these pulses to the requisite magnitude at level E_{go3} if they are supplied across an R-C differentiator to the suppressor grid. This idea is explained in Figure IX.27, where the input and output voltages of the differentiator coupling the screen and suppressor grids are depicted. The task is simplified by the fact that such a differentiator already exists in /416 the Figure IX.25 circuit: accelerating capacitor C_2 and resistance R_3. There is a need only to remove resistance R_2 (there is no requirement for a voltage divider to supply suppressor grid constant negative potential in the free-running mode) and disconnect negative bias source E_g. Here, capacitor C_2 will play a dual role: first, the positive feedback network between screen and suppressor

*Here, the circuit initial state ceases being stable and it is converted to a quasistable state, like the circuit state in the operating stage.

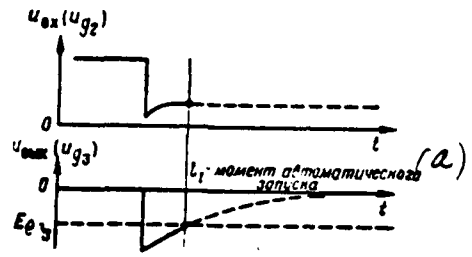


Figure IX.27. For Screen Grid Coupling Phantastron Automatic Triggering. (a) -- Moment of automatic triggering.

grids closes across it (we will recall that positive feedback is required to create spasmodic transitions at the beginning and end of the working stroke); second, it (along with resistance R_3) will be a timing element. The resultant free-running screen grid coupling phantastron circuit and curves of the voltages in it are depicted in Figure IX.28. We will examine circuit operation, beginning with its state at the end of a working stroke.

We already are aware of the processes during the working stroke: just as was the case in the negative feedback GPN circuits examined earlier, capacitor C is recharged across unblanked pentode by virtually constant current along network $+E_a$, resistance R, capacitor C, plate--cathode path, chassis $(-E_a)$. Negative feedback network action provides recharging current constancy. Here, negative voltage, which rises slowly, is maintained in the control grid, while plate voltage drops by a virtually linear law. The screen grid current flowing across resistance R_{g2} is slight (since the pentode is unblanked with respect to plate current). Therefore, voltage u_{g2} is high. Circuit parameters are selected (see below) so that the transient process in differentiator C_2R_3 ends long before the end of the working stroke. Therefore, no current flows across capacitor C_2 and resistance R_3, there is no voltage drop across the latter, and suppressor grid potential equals cathode potential $u_{g3} = 0$. Capacitor C_2 is charged here to voltage u_{g2} with a "plus" to screen grid.

The operating stage continues until moment t_2, when linearly-falling plate voltage attains minimum value $U_{a\,мр}$. At that moment, negative feedback action

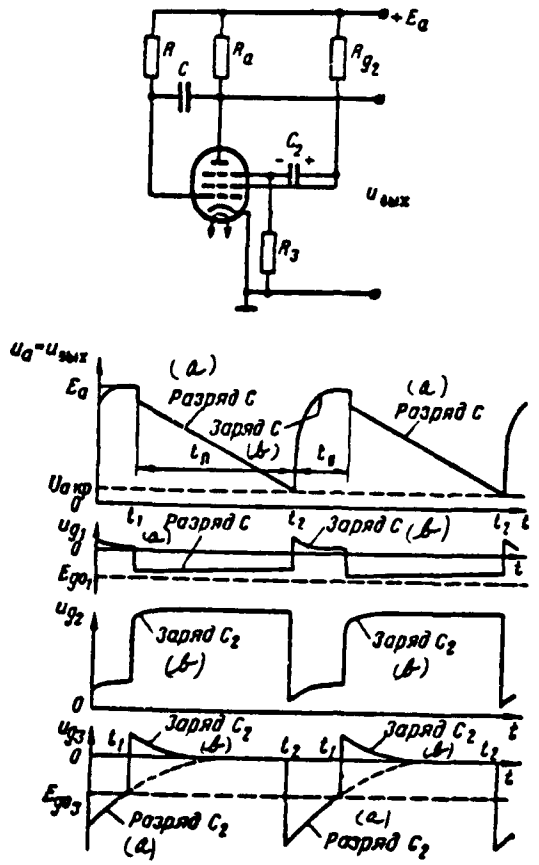


Figure IX.28. Free-Running Screen Grid Coupling Phantastron.
(a) -- Discharge; (b) -- Charge.

ceases, but the positive feedback network closes (IX.49), resulting in the already-familiar avalanche-like process occurring: voltages u_a and u_{g1} rise with a jump, while voltages u_{g2} and u_{g3} fall with a jump. The negative suppressor grid voltage step leads to pentode blanking with respect to plate current: $|\Delta U_{g3}| > |E_{go3}|$. Then, capacitor C charges in connection with the voltage u_a increase, while capacitor C_2 discharges in connection with the voltage u_{g2} decrease. Control grid current charges capacitor C along network $+E_a$, resistance R_a, capacitor C, control grid--cathode path, chassis $(-E_a)$. This current decreases along an exponential curve with time constant $\tau_{зар} \approx CR_a$. Therefore, plate voltage

rises along an exponential curve, striving to level $+E_a$, while voltage u_{g1}, /417 with the identical time constant, decreases, striving towards level $u_{g1} \approx 0$. These levels are maintained then until the beginning of the next cycle. The voltage u_{g1} positive exponential excursion leads to a current $i_a \approx i_{g2}$ exponential "bump." Therefore, a voltage u_{g2} negative excursion of identical shape is created.

Screen grid current discharges capacitor C_2 along network capacitor C_2 right ("plus") plate, screen grid-cathode path, resistance R_3, C_2 left ("minus") plate. This network's time constant equals $\tau_{разр2} = C_2(r_{i_{a2}} + R_3)$. As discharging /418 current pass across resistance R_3, a voltage drop across it arises and is applied with a "minus" to suppressor grid. Negative voltage u_{g3} rises along an exponential curve with time constant $\tau_{разр2}$, as a result of the decrease of this current, striving to the zero level. However, at moment t_1, when this voltage, rising, attains the blanking voltage E_{go3} level, the pentode is unblanked with respect to plate current and the positive feedback network (IX.48) goes into action. An avalanche-like process, identical to the one when a phantastron is triggered externally, occurs here. As a res. t, voltages u_a and u_{g1} are reduced with a jump, while voltages u_{g2} and u_{g3} rise. A quasistable circuit state corresponding to the operating stage and described above then arises. The only difference from the Figure IX.25 circuit is that capacitor C_2 at moment t_1 begins to charge along network $+E_a$, resistance R_{g2}, capacitor C_2, resistance R_3, chassis $(-E_a)$ in connection with the rise in screen grid potential. This network's time constant equals $\tau_{разр2} = C_2(R_{g2}+R_3)$. Charging current will drop along an exponential curve with the identical time constant, reducing screen grid and increasing suppressor grid potential. Therefore, voltage u_{g2} rises along an exponential curve, while negative voltage u_{g3} will drop to the zero level. Next, the processes automatically repeat themselves.

The desire is to select those circuit parameters insuring that the effective linearly-falling output voltage sector would occupy the basic range of the period, i. e., the ineffective range of the period $t_в = t_1 - t_2$ would be as small as possible. The capacitor C_2 discharging time constant mainly determines ineffective range duration. However, this duration must be sufficient for complete capacitor C charging, i. e., no less than recovery time $t_в \approx 3\tau_{разр} = 3CR_a$. Resistance R_a is decreased to tens and hundreds of kilohms that, however, leads to corresponding deterioration of working stroke linearity due to a pentode gain decrease. It

is also possible to use a cathode follower, which simultaneously in this case is a buffer (see Figures IX.24 and IX.26), is this circuit to reduce recovery time.

The deterioration in working stroke linearity compared to previous circuits also occurs due to the positive exponential voltage u_{g3} bump at the beginning of the operating stage. This bump disrupts plate current constancy and, consequently, capacitor C discharging current, and must be as short as possible. Usually, the ineffective range of the period comprises tenths or hundredths of a complete period of oscillation $T=t_a+t_b$. Therefore, $T \approx t_a$. Ratio (IX.42) determines output voltage working stroke duration t_a = RC. Resistance R controls this duration and, consequently, phantastron oscillation frequency $F=\frac{1}{T}$. Oscillation frequency ranges from unities to several thousand hertz, depending upon circuit parameters.

EXERCISE IX.20 /419

Draw the curves of voltages u_a and u_{g3} in the scale used in Figure IX.28 if:

a) resistance R_a is increased by a factor of 3;
b) resistance R_3 is increased by a factor of 2;
c) capacitance C_2 is decreased by a factor of 3;
d) resistance R is decreased by a factor of 2;

How will these changes in the circuit impact upon output voltage parameters (amplitude, linearity, oscillation frequency, stability)? (Page 509)

7. Monostable Cathode-Coupling Phantastron

We will return again to the externally-controlled GPN circuit depicted in Figure IX.21. If cathode load impedance R_k is connected to the pentode L_1 cathode network, then a virtually square pulse of voltage $u_k = i_k R_k$ of negative polarity will be shaped in this resistance during the working stroke (see Exercise IX.15c). The potential of this grid relative to cathode will become equal to voltage u_k with an opposite sign: $u_{g3}=-u_k$ if now pentode suppressor grid is connected to the lower resistance R_k terminal. Consequently, a positive-polarity pulse from resistance R_k will act upon the suppressor grid. This pulse also may be used as a switching pulse produced by the circuit itself instead of an external

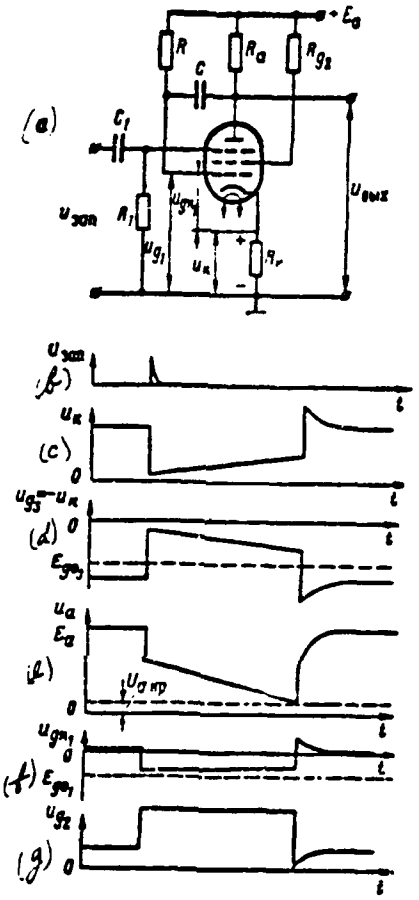


Figure IX.29. Monostable Cathode-Coupling Phantastron.

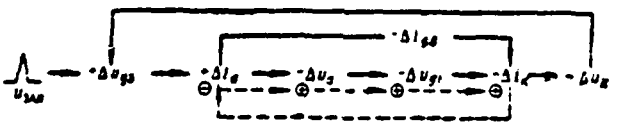
control pulse. Circuits that operate on this principle are referred to as cathode-coupling phantastrons. A monostable cathode-coupling phantastron circuit and the curves of its voltages at its characteristic points are depicted in Figure IX.29.

Positive pulses acting across transiert network C_1R_1 to the pentode /420 suppressor grid trigger the phantastron.

We will examine circuit operation.

Initial state. Due to control grid current flow across large resistance R, its potential approximates cathode potential $U_{g1o} \approx 0$ in the initial state and large cathode current I_{k0} flows across the pentode. This current creates across cathode load impedance R_k voltage drop $U_{k0} \approx I_{k0} R_k$, which acts upon the suppressor grid like negative bias and blanks the pentode with respect to plate current: $U_{g30} = -U_{k0} < E_{g03}$. Therefore, plate voltage is maximum and equals $+E_a$. Since $i_a = 0$, large current $I_{g20} \approx I_{k0}$ flows through the screen grid network and screen grid voltage is slight. Thus, circuit initial state prior to triggering is identical to that in a monostable screen grid coupling phantastron (see Figure IX.25), with one difference: the large voltage drop across resistance R_k, rather than the external source of negative bias E_g, insures pentode blanking with respect to plate current.

Circuit triggering. The pentode is blanked with respect to plate current while a positive trigger pulse acts upon the suppressor grid and plate voltage is reduced. This voltage reduction is transmitted across capacitor C to the control grid and leads to a cathode current decrease. Here, the voltage u_k drop decreases, *i. e.*, suppressor grid voltage $u_{g3} = -u_k$ rises. This leads to a further plate current rise. Thus, a positive feedback network, whose action facilitates the transitron effect, is formed: a current i_a increases means a current i_k decrease due to a screen grid current i_{g2} decrease. As a result, an avalanche-like process arises, which symbolically may be depicted in the following manner:



(IX.53)

The negative feedback loop simultaneously is active, exerting a constraining action at the moment of triggering (depicted by the dotted line and encircled signs).

The avalanche-like process ceases when transconductance $i_{g2} = \varphi(u_{g3})$ drops to such an extent due to the current i_{g2} decrease that the plate current rise already may not be accompanied by a current i_k decrease. Thus, at the moment of triggering, voltages u_a and u_k drop with a jump, while voltages u_{g2} and u_{g3} rise. The negative plate voltage step across capacitor C is transmitted to /421

the control grid. The voltage steps may be written $-\Delta U_{g1} = -\Delta U_a = -\Delta U_{gk1} - \Delta U_k$ since the voltage between control grid and "ground" equals $u_{g1} = u_{gk1} - u_k$ (see Figure IX.29a). Here, resultant step ΔU_{gk1} also is negative since tube gain with respect to the cathode network always is less than unity and, consequently $\Delta U_k < \Delta U_{g1}$. The magnitude of step ΔU_{gk1}, as in previous circuits, may not exceed control grid blanking voltage $\Delta U_{gk1} < |E_{g1}|$. However, plate voltage step ΔU_a is several-fold greater since the sum of $\Delta U_{gk1} + \Delta U_k$ determines it in a cathode-coupling phantastron.

Operating stage. As was the case in the phantastron circuits previously examined, virtually constant current recharges capacitor C across the unblanked pentode following circuit reversal. As usual, negative feedback network action (IX.38) insures recharging current constancy. The curves of the operating stage voltages essentially do not differ from the corresponding Figure IX.25 curves. The voltage between screen grid and "ground" during the working stroke changes within smaller limits (more constant) since it equals $u_{g2} = u_{gk2} + u_k$. Meanwhile, if the first term decreases in connection with the gradual current i_{g2} rise, then the second, on the other hand, rises.

Recovery. Pentode amplifying properties disappear, the negative feedback network is disrupted, capacitor C recharging current begins rapidly to decrease, and control grid voltage rapidly begins to rise when plate voltage attains critical value $U_{a\,кр}$. Here, the positive feedback network again closes and an avalanche-like process leading to spasmodic voltage changes arises in the circuit. Positive feedback action ceases at the moment the pentode is blanked with respect to plate current, followed by capacitor C charging to the initial voltage with time constant $\tau_{вар} = CR_a$. Curves of the voltages in the recovery stage do not differ from the corresponding Figure IX.25 curves.

Just as was the case for a screen grid coupling phantastron, negative pulses supplied to plate may trigger a cathode-coupling phantastron and a cathode follower also may be used to decrease recovery time. The following are cathode-coupling phantastron advantages over screen grid coupling phantastrons: absence of a special negative bias E_g source, good positive pulse shape obtained in the screen grid, and the possibility of obtaining a negative pulse shaped in resistance R_k. However, the circuit more often is used as a delay circuit operating on the same principle as the Figure IX.26 circuit due to the large magnitude of the negative plate voltage step at the moment of triggering.

EXERCISE IX.21 /422

a) How will presence of cathode load impedance $R_к$ impact upon the linearity of phanatastron output voltage in the operating stage?

b) Use a symbolic rendition to explain the avalanche-like process (positive feedback action) at the moment the operating stage ceases.

c) Draw a cathode-coupling phantastron circuit with plate network triggering operating as a variable delay circuit and producing delayed positive-polarity pulses. (Page 511)

§ 6. TRAPEZOIDAL VOLTAGE (SAWTOOTH CURRENT) GENERATOR

Cathode-ray tubes [CRT] with an electromagnetically-controlled beam, which have advantages over CRT with an electrostatically-controlled beam, usually are used in radar station displays. A magnetic field created by deflecting coils deflects the electron beam in magnetically-controlled tubes. The electron beam is deflected in a plane perpendicular to magnetic field direction. Beam deflection magnitude is proportional to magnetic field strength, which in turn is proportional to the current flowing through the coil. Therefore, the law of current change for the coil deflecting the beam in a given plane determines beam behaviour over time. It follows from this that the current of the appropriate coil must change by a linear law during the sweep working stroke in order to create a sweep linear over time (evenly-divided scale) in a display:

$$i_к = V_i t, \qquad (IX.54)$$

where $V_i = \frac{di_к}{dt} = \text{const}$ -- proportionality factor equal to the rate of current change and determining the sweep rate for a given tube type.

The law of coil current change during flyback is not applicable since the tube is blanked during this time.

We will explain the shape of the voltage which must be applied to a coil so that linearly-changing current will flow through it (Figure IX.30).

Any coil has inductance $L_к$ and resistance $r_к$. Therefore, it may be represented in the form of a series connection of these elements (Figure IX.30a).

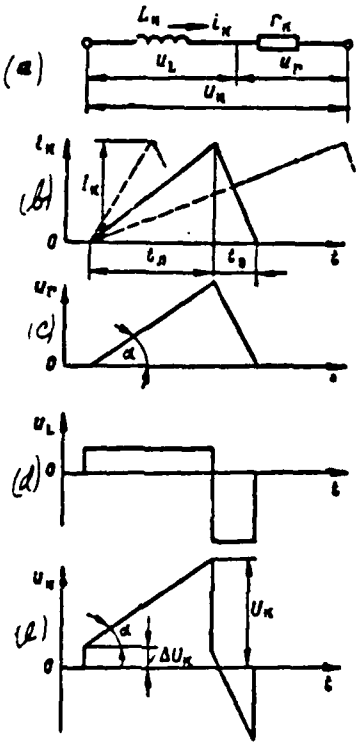


Figure IX.30. For Determination of the Shape of Deflecting Coil Voltage To Create a Linear Sweep.

Voltage applied to the coil equals the sum of the voltage drops across the resistance and inductance:

$$u_к = u_r + u_L = i_к r_к + L_к \frac{di_к}{dt}. \qquad \text{(IX.55)}$$

For given values $r_к$ = const and $L_к$ = const, the first term of this expression is proportional to current $i_к$, while the second is proportional to the rate of

change of this current $\frac{dI_к}{dt}$. If the current changes by linear law (IX.54), /423 then expression (IX.55) may be represented in the form

$$u_к = V_1 r_к t + L_к V_1, \tag{IX.55a}$$

from which it follows that the voltage drop across resistance $r_к$ also changes by a linear law, while the voltage drop across inductance $L_к$ (equalizing self-induction emf) is a constant magnitude.

In this connection, the curves of voltages u_r, u_L and $u_к = u_r + u_L$ are plotted in Figure IX.30 for sawtooth voltage $i_к$.*

So, trapezoidal voltage must be applied to the coil in order to obtain linearly-changing current in it. During the working stroke, this voltage has a blanking level with height $\Delta U_к = u_L = L_к V_1$ and a linear sloping sector with slope $\operatorname{tg}\alpha = V_1 r_к$.

We will express the rate of current change in expression (IX.55a) by means of working stroke duration and current amplitude $V_1 = \frac{I_к}{t_р}$ to explain the coupling of the voltage $u_к$ shape with coil and sweep parameters.

Then we will get

$$u_к = \frac{I_к}{t_р} r_к t + \frac{I_к}{t_р} L_к = \\ = I_к r_к \left(\frac{t}{t_р} + \frac{\tau_к}{t_р}\right). \tag{IX.55b}$$

where $\tau_к = \frac{L_к}{r_к}$ — coil time constant.

It is possible to disregard the first term in parentheses given fast sweeps, when $t_р \ll \tau_к$, i. e., $\frac{\tau_к}{t_р} \gg 1$ ($\frac{t}{t_р} < 1$ during the working stroke) and consider $u_к \approx I_к r_к \frac{\tau_к}{t_р} = I_к \frac{L_к}{t_р}$ = const. Consequently, for fast sweeps, trapezoidal sweep /424 voltage may be replaced with square voltage. Given slow sweeps when, on the other

*Current $i_к$ flyback also is assumed to be linear for simplicity.

hand, $t_1 \gg \tau_к$, i. e., $\frac{\tau_к}{t_1} \ll 1$, it is possible to disregard the second term in parentheses and consider $u_к \approx I_к \frac{r_к}{t_1} t$. Consequently, for slow sweeps, trapezoidal sweep voltage may be replaced with sawtooth voltage. Where $t_1 = \tau_к$ $u_к = I_к r_к + I_к r_к \frac{t}{t_1}$, i. e., trapezoidal voltage at the end of the working stroke ($t = t_1$) equals doubled blanking level height $U_к = 2\Delta U_к$.

A triode exponential sweep generator (Figure IX.4) may be used to obtain trapezoidal voltage in the simplest case if its R-C integrator is replaced with

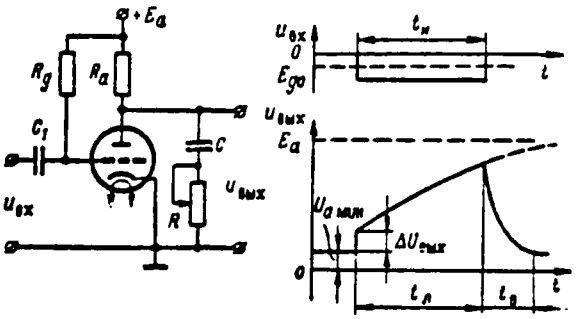


Figure IX.31. Triode Trapezoidal Voltage Generator.

an integrodifferentiating R-C network. The circuit for such a generator and the curves of the voltages in it are depicted in Figure IX.31. This circuit differs from the Figure IX.4 circuit only in the presence of additional resistance R connected in series with capacitor C to the output network. Triode L_1 is unblanked in the initial state and, as usual, output voltage equals value $U_{а\,мин}$ (IX.19). Capacitor C charges along network $+E_а$, resistance $R_а$, capacitor C, resistance R, chassis ($-E_а$) while a control pulse blanks the triode. Capacitor charging current equals $i_з = I_з e^{-\frac{t}{\tau_{зар}}} = \frac{E_а - U_{а\,мин}}{R_а + R} e^{-\frac{t}{\tau_{зар}}}$, where $\tau_{зар} = C(R_а + R)$ -- charging network time constant. This current is maximum at the moment of triode blanking and creates in resistance R voltage step

$$\Delta U_{вых} = I_з R = \frac{E_а - U_{а\,мин}}{1 + \frac{R_а}{R}}. \qquad (IX.56)$$

Then, output voltage rises by the law of exponents, striving towards /425
level $+E_a$, in connection with capacitor charging.

The complete law of output voltage change during a working stroke is described by the expression

$$u_{вых} = E_a - i_3 R_a = E_a - \frac{E_a - U'_{a\,мин}}{1 + \frac{R}{R_a}} e^{-\frac{t}{\tau_{зар}}} =$$

$$= (E_a - U'_{a\,мин})\left(1 - \frac{e^{-\frac{t}{\tau_{зар}}}}{1 + \frac{R}{R_a}}\right) + U'_{a\,мин} =$$

$$U'_{a\,мин} - \frac{E_a - U'_{a\,мин}}{1 + \frac{R_a}{R}} + \frac{E_a - U'_{a\,мин}}{1 + \frac{R}{R_a}}\left[1 - e^{-\frac{t}{C\frac{R_a R}{R_a + R}}}\right] \qquad (IX.57)$$

The first term of this expression is the initial output voltage value, the second is the magnitude of the step at the beginning of the working stroke (blanking level height), the third is the law of exponential output voltage rise after the step. Triode L_1 unblanks at the moment the control pulse ceases and capacitor C rapidly discharges across the triode and resistance R to initial voltage $U'_{a\,мин}$. Thus, as usual, control pulse duration $t_3 = t_и$ determines working stroke time, while circuit recovery time rises somewhat in comparison with (IX.21): $t_в \approx \tau_{зар} = 3C(R_{i0}+R)$.

Condition $t_3 \ll \tau_{зар}$ must be satisfied to obtain a sufficiently-slight working stroke nonlinearity factor. Here, the exponential output voltage sector may be considered linear, i. e., capacitor charging current as constant $(i_3 = I_3)$. Then, a trapezoidal pulse of output voltage during a working stroke will be described by expression $u_{вых} - U'_{a\,мин} \approx I_3 R + \frac{I_3}{C} t$. Proportionality condition $\frac{I_3 R}{V_1 L_и} = \frac{I_3 t}{C V_1 r_и t}$ or $\frac{R}{L_и} = \frac{1}{C r_и}$ must be satisfied for this pulse to be similar to the requisite voltage shape in the coil (IX.55a), hence we will get

$$CR = \frac{L_и}{r_и} \qquad \text{or} \qquad \tau_{вых} = \tau_и \qquad (IX.58)$$

-- the generator output network time constant must equal the coil time constant. Satisfaction of this condition for selected C magnitude is achieved by resistance R control.

A deflecting coil for a trapezoidal voltage generator is a low-resistance load ($r_к \ll R_и$). Therefore, it always is connected to the generator across /426 a buffer stage -- a sweep current generator. A cathode follower is used in the simplest instance as a buffer stage. If a paraphase (symmetrical) sweep is used, then the trapezoidal voltage generator controls the paraphase sweep voltage amplifier, while the latter controls a push-pull sweep current amplifier, to the output of which the deflecting coils are connected.

The Figure IX.30a equivalent coil circuit did not consider coil stray distributed capacitance $C_к$. This capacitance shunts resistance $r_к$ and inductance $L_к$ and may attain significant magnitude (up to 100 pF) for multiturn coils. Capacitance $C_к$ influence manifests itself in distortions of the current sweep initial sector for two reasons. First, capacitance $C_к$ may not instantaneously charge itself and, therefore, makes instantaneous onset of the voltage blanking level at the beginning of the working stroke physically impossible. Second, along with inductance $L_к$, capacitance $C_к$ forms a parallel oscillatory loop providing shock excitation at the moment the working stroke ceases. Damping oscillations arising in the loop at this time constrain minimum flyback time and are accumulated at the onset of the forward motion.

A special pulse of great amplitude and slight duration sometimes is added to the trapezoidal voltage at the beginning of the working stroke in order to force capacitance $C_к$ charging at the beginning of the working stroke, i. e., to increase the blanking level slope. Coil shunting by resistance $R_ш$ is used to eliminate damping oscillations arising in the coil loop. In accordance with (II.57), shunting resistance magnitude must satisfy condition $R_ш < R_{кр} = \frac{1}{2}\sqrt{\frac{L_к}{C_к}}$ in order to convert the loop into an aperiodic loop, i. e., to introduce damping less than at the critical level into it. In addition, shunting resistance must be sufficiently great so that the basic portion of the generator current will pass through the coil, creating a sweep, while only an insignificant portion of the current will branch to resistance .

EXERCISE IX.22

a) Plot the curves of the coil voltage $u_к = u_r + u_L$ if sweep working stroke time

t_1 compared to its Figure IX.30 value is decreased by a factor of 2; increased by a factor of 2. Retain the present current amplitude $I_к$ (overall sweep dimensions) and flyback time $t_в$.

How must the parameters of the trapezoidal voltage generator circuit (IX.31) be changed in order, given satisfaction of the $u_{вых}$ and $u_к$ similarity condition (IX.58) and initial output voltage level constancy, to provide the voltage $u_{вых}$ shape changes corresponding to the resultant curves?

b) How will trapezoidal voltage generator output voltage change compared to that depicted in Figure IX.31 if, without changing control pulse duration, resistance R is decreased; increased? (Page 511)

§ 7. TRANSISTOR SAWTOOTH GENERATORS

1. R-C Integrator Exponential Voltage Generator /427

The generator circuit is depicted in Figure IX.32a. Here, resistance $R_к$ and capacitor C form an integrator. Transistor T, connected in a common-emitter

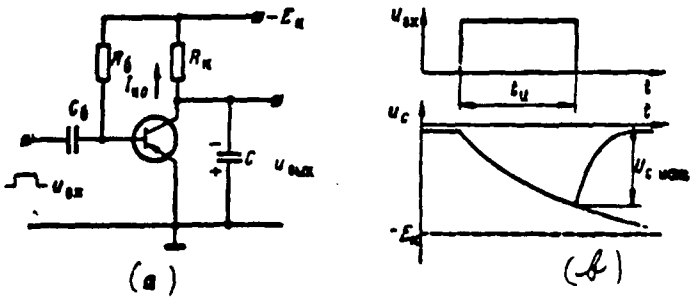


Figure IX.32. R-C Integrator Transistor Trapezoidal Voltage Generator Circuit (a) and Voltage Curves (b).

circuit, operates in the switching mode. Circuit advantages include simplicity and relatively short recovery time.

Voltage curves explaining the operation of this circuit are depicted in Figure IX.32b.

The transistor is in a state of saturation in the initial state and collector voltage approximates zero (Figure IX.33). Input current (base current $i_б$) equal

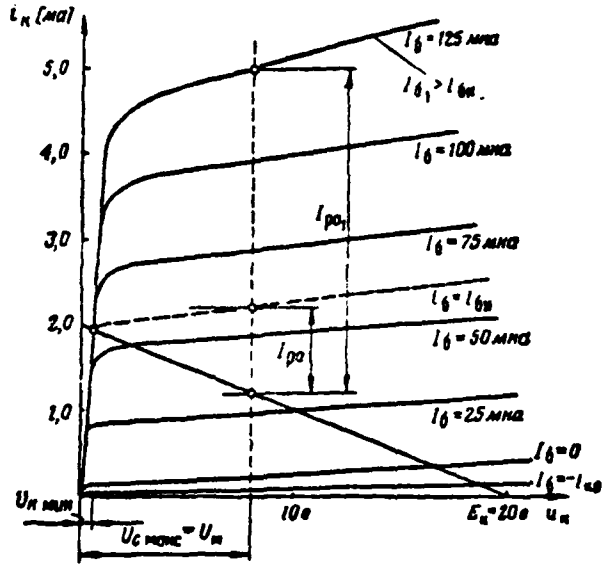


Figure IX.33. Transistor Characteristics in the Common-Emitter Circuit Illustrating Operation of the Figure IX.32 Circuit.

to or exceeding magnitude $I_{бн}$ supports this state.

Initial capacitor voltage U_{Co} equalling collector voltage is measured in tenths of a volt.

While a positive square pulse blanks the transistor, capacitor C charges by a law described in its first approximation by the expression

$$u_C \simeq (E_к - I_{к0}R_к)\left(1 - e^{-\frac{t}{R_к C}}\right). \qquad (IX.59)$$

The time the transistor exits from saturation (first carrier clean-out) and the time lag stipulated by transistor frequency properties are not considered here since they are slight compared with switching pulse duration. Transistor shunting action also is not considered.

It is evident from expression (IX.59) that the rate of output voltage /428
change will depend on the current $I_{к0}$ magnitude and, at the initial moment, equals

$$p = \frac{du_C}{dt}\Big|_{t=0} = \frac{E_к}{\tau} - \frac{I_{к0}}{C}, \qquad (IX.60)$$

where $\tau = R_к C$.

Capacitor C capacitance must be sufficiently great to decrease the influence of current $I_{к0}$ on the rate and, consequently, also on the amplitude for the given forward motion duration $t_и$. Here, there is a requirement to decrease resistance magnitude to insure the assigned output voltage rate change value. A safe collector current $R_к$ magnitude determines the minimum $I_{к.н}$ value.

There is a requirement to select $\tau \gg t_и$ to provide a slight nonlinearity factor value, just as was the case in R-C integrator tube generators, which leads to a low supply source utilization factor value $\eta = \frac{U_и}{E_к}$, where $U_и$ -- sawtooth voltage amplitude.

One must turn to the form of the conventional integrator to evaluate /429
the nonlinearity factor magnitude considering Figure IX.32a circuit shunting.

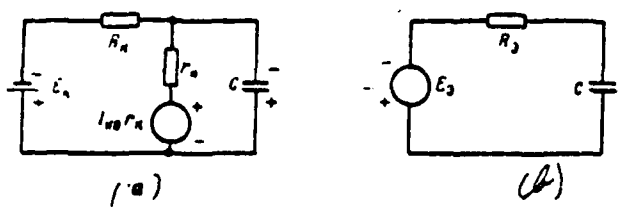


Figure IX.34. Capacitor Charging Circuit:
(a) -- Equivalent circuit; (b) -- Reduced circuit.

We will consider that subsequent stage input resistance is sufficiently great (an emitter follower on composite transistors is used, for example) and load shunting action may be disregarded. The Figure IX.34a circuit may characterize transistor T in the blanked state.

One considers the shunting action of the blanked transistor in this circuit by introducing shunting voltage generator $E_ш = I_{ко} r_к$ and collector junction resistance $r_к$. Considering initial capacitor voltage $U_{Co} = 0$ and transforming the circuit by the theorem about an equivalent generator, we get an integrator (Figure IX.34b), where

$$E_э = \frac{r_к}{R_к + r_к}[E_к - I_{ко}R_к], \tag{IX.61}$$

$$R_э = \frac{R_к r_к}{R_к + r_к}. \tag{IX.62}$$

Hence, the nonlinearity factor may be written in the form

$$\beta_ш = \frac{U'_м}{E_э} = \frac{U'_м}{E_к} \cdot \frac{\left(1 + \frac{R_к}{r_к}\right)}{\left(1 - \frac{I_{ко}R_к}{E_к}\right)}, \tag{IX.63}$$

where $U'_м$ — sawtooth voltage amplitude determined, where $t_и \ll \tau_э = R_э C$, from the formula

$$U_м = E_э \frac{t_и}{\tau_э}. \tag{IX.64}$$

In practical calculations where $r_к \gg R_к$ and current $I_{ко}$ magnitude is slight, the formula is simplified and has the form

$$U'_м \approx E_к \frac{t_и}{\tau}. \tag{IX.65}$$

In those cases when condition $r_к \gg R_к$ is satisfied, the approximate /430 nonlinearity factor magnitude may be obtained directly from expression (IX.59):

$$\beta_ш = \frac{U_м}{E_к - I_{ко}R_к}.$$

This is in complete conformity with formula (IX.63) for the assumptions made.

Capacitor C discharge across transistor T begins when input pulse action ceases. Capacitor voltage decreases from maximum value $U_{C\,макс}$ to minimum value $U_{C\,мин}$. The transistor is in the active region during the entire capacitor discharge

process and it may be looked upon as a current $\beta I_б$ generator. The transistor converts to the saturation mode only when capacitor discharge ceases.

We will present the equivalent capacitor discharge circuit in the form depicted in Figure IX.35a for recovery time evaluation. This circuit may be corrected

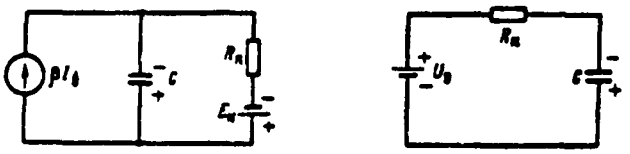


Figure IX.35. Equivalent Capacitor Discharge Circuit:
(a) -- With current generator; (b) -- With voltage generator.

to the form of a conventional R-C network, as depicted in Figure IX.35b. Here,

$$U_0 = \beta I_б R_к - E_к. \tag{IX.66}$$

In this case, capacitor voltage changes by the law

$$u_C = -(U_н + U_0)e^{-\frac{t}{R_к C}} + U_н, \tag{IX.67}$$

which is illustrated in Figure IX.36.

Discharge ceases at the moment when u_C 0. Then recovery time may be determined directly from expression (IX.67):

$$t_в = R_к C \ln\left(1 + \frac{U_н}{U_0}\right). \tag{IX.68}$$

The resultant formula is simplified if $U_н < E_к \ll \beta I_б R_к$ (which essentially takes place):

$$t_в \approx R_к C \frac{U_н}{\beta I_б R_к} = \frac{C U_н}{\beta I_б}. \tag{IX.68a}$$

It is evident from this that a recovery time decrease requires that /431 one have the greatest possible current $I_б$ value, which corresponds to greater transistor bottoming in the initial mode. This phenomenon may be explained by using Figure IX.33, where initial discharging current values were demonstrated for instances when the transistor was at saturation threshold $i_б = I_{бн}$ and in a bottoming state $i_б = I_{б1} > I_{бн}$. Discharging current is determined as the difference in the collector current $I_к$ ordinates corresponding to the current characteristic where $i_б$ = const and the load line.

In the first instance (where $i_б = I_{б1}$), recovery is slow since the initial discharging current $I_{р0}$ magnitude is slight, while its relative decrease during

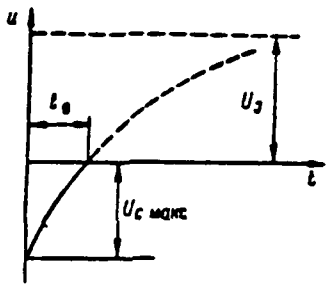


Figure IX.36. For Recovery Time Determination.

the discharge process is great. In the second instance (where $i_б = I_{б1}$), recovery occurs relative more rapidly since discharging current $I_{р0}$ is greater and the relative decrease less.

Safe magnitude of the power dissipated by the transistor determines the clamping of the maximum discharging current magnitude.

This GPN circuit will find practical use in those instances when there is a requirement for voltage with a nonlinearity factor $\beta_н$ = 10--15%.

EXERCISE IX.23

a) What link exists between circuit temperature stability (the requirement

for constant amplitude, for example) and the requirement for rapid recovery to the initial state?

b) Determine safe switching pulse duty ratio in the Figure IX.32 GPN circuit if: $t_и$ = 1,000 usec, $R_к$ = 10 kilohm, C = 0.25 uF, $R_б$ = 160 kilohm, $E_к$ = -20 V.

The transistor characteristics used in the circuit are depicted in Figure IX.33. Disregard transistor shunting action. (Page 512)

2. Current-Stabilizing One-Port Sawtooth Generator

The inability simultaneously to obtain great sawtooth voltage amplitude and a low nonlinearity factor is a shortcoming of the GPN circuit examined above.

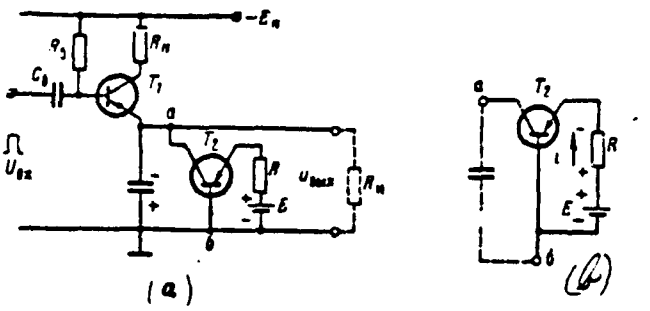


Figure IX.37. Transistor Current-Stabilizing One-Port GPN Schematic Diagram (a) and Equivalent Circuit (b).

Therefore, circuits utilizing the current-stabilizing properties of transistors have found wide use. One such example is the circuit depicted in Figure IX.37a. Here, transistor T_1 plays the role of switch, while transistor T_2, connected as a common-base circuit, acts as a current regulator. The stabilizing properties of one-port *аб* (Figure IX.37b) determines such an important GPN indicator as the nonlinearity factor.

We will assume that internal element resistances (load impedance $R_н$, blanked transistor T_1 resistance, capacitor C leakage resistance) connected to the one-port

is very great at the sawtooth voltage shaping stage. Then, all one-port collector current flows only across capacitor C and its change determines the degree of output voltage linearity, i. e.,

$$\beta_н = \frac{I_{нач} - I_{кон}}{I_{нач}} = \frac{\Delta I}{I_{нач}}.$$

Transistor T_2 collector characteristics, which in external form are reminiscent of pentode volt-ampere characteristics, are represented in Figure IX.38. In this

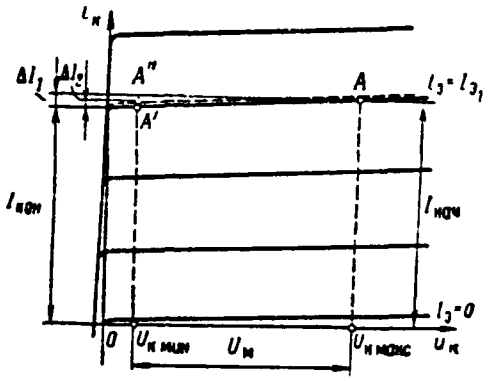


Figure IX.38. Common-Base Transistor Circuit Characteristics Illustrating Operation of the Figure IX.37 GPN Circuit.

case, a slight discharging current change corresponds to a capacitor C voltage change ranging from $U_{Co} = U_{к\ нас}$ to $U_C = U_{к\ мин}$, which is caused by the form of the transistor characteristics.

Negative feedback caused by the presence of resistance R in the emitter network constrains the tendencies of discharging current to change, along with the current-stabilizing action of the transistor itself, and this increases the degree of output voltage linearity. Actually, if one assumes R = 0, then the point representing system state (point A in Figure IX.38), due to capacitor discharge, will shift along one of the transistor static characteristics ($i_э = I_{э1}$) and, by the end of the working stroke ($U_C = U_{к\ мин}$), will occupy a position corresponding to point A'. The magnitude of the collector current drop equals ΔI_1. Given resistance R in the emitter circuit, current $i_к$ will strive to decrease due to

capacitor discharge but here voltage in the base--emitter sector will decrease /433 since $u_{к1} \approx -E + i_к R$. The latter circumstance leads to the fact that a slight emitter current increase occurs in the discharging process and the representative point shifts, not along one characteristic, but changes to characteristics corresponding to a large current $i_э$ value. By the end of the working stroke, the representative point will occupy a position corresponding to point A". The magnitude of the collector current drop equals ΔI_2 and turns out to be significantly less than in the previous case.

The magnitude of resistance R must be increased to increase one-port current-stabilizing properties. However, a significant R increase is undesirable since voltage E must be increased to the same degree to insure the given initial discharging current $I_{нач}$ magnitude.

EXERCISE IX.24

Think about why there is a requirement to increase source voltage E when resistance R increases. Upon which output voltage parameter does the voltage E magnitude impact where R = const? (Page 513)

It is possible to obtain an analytical expression for nonlinearity factor $\beta_н$, stemming from the following circumstances. Magnitude $\beta_н$ is determined by the known ratio

$$\beta_н = \frac{\Delta I}{I_{нач}},$$

where ΔI — one-port $аб$ current change.

The ΔI change may be expressed by the voltage change between points a and $б$ (Figure IX.37b), i. e., the capacitor C voltage change, and the internal /434 resistance of this one-port, which in this case is common-base circuit output resistance determined in accordance with (III.101). It follows from what has been stated that

$$\Delta I = \frac{U'_{к\,макс} - U'_{к\,мин}}{R_{вых\,б}} = \frac{U'_к}{R_{вых\,б}}. \qquad (IX.69)$$

Hence

$$\beta_н = \frac{U_н}{R_{вых\,ф} I_{нач}} = \frac{U}{I_{нач}\left(r_к + r_б - r_G \frac{2r_к + r_б}{R + r_э + r_б}\right)}. \qquad (IX.70)$$

When resistance R increases, output resistance will rise, striving within the range to value

$$R_{вых\,ф} = r_к + r_б \approx r_к.$$

Consequently, the minimum nonlinearity factor value given the assigned amplitude and initial current, is determined by the expression

$$\beta_{н\,min} = \frac{U_н}{I_{нач} r_к}. \qquad (IX.71)$$

Under actual conditions, this $\beta_н$ value may not be realized since one may not have a resistance R magnitude that is too large for the reason stated above. Usually, the selected resistance R magnitude is such that, when

$$R_{вых\,ф} \approx 0{,}9 r_к$$

and therefore

$$\beta_н = 1{,}1 \frac{U_н}{I_{нач} r_к}. \qquad (IX.72)$$

In addition, the shunting action of internal element resistances also leads to a nonlinearity factor increase. Essentially, it is necessary to reckon only with load impedance $R_н$, since the back resistance of blanked transistor T_1 emitter junction $r_{э\,обр} > r_н$. A composite transistor emitter follower is used as a matching device to eliminate the shunting action of load.

Having familiarized ourselves with the principle of discharging current stabilization, we briefly will examine the physical processes in a GPN circuit during a complete cycle, i. e., during period T.

Current-stabilizing transistor T_2 and switching transistor T_1 are unblanked

in the initial state since their base voltages are negative relative to the emitters. Transistor T_1 voltage is slight and capacitor C charges to voltage approximating $E_к$.

Transistor T_1 (Figure IX.37a) unblanks when a positive-polarity switching pulse is supplied to input (Figure IX.39a). Capacitor C begins to discharge /435

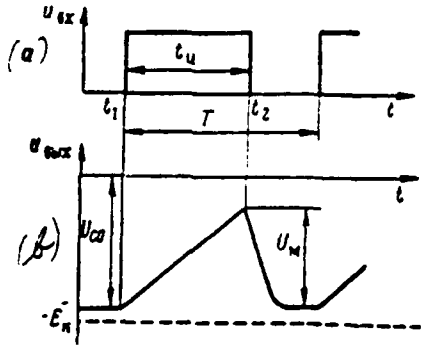


Figure iX.39. Curves of Voltages at Figure IX.37 GPN Circuit Input and Output.

across current-stabilizing transistor T_2. Discharging current remains essentially constant, while capacitor voltage remains linear (Figure IX.39b) since switching pulse duration is less than complete capacitor C discharging time. Sawtooth voltage amplitude may be determined from the formula

$$U_м \simeq \frac{I_{ср} t_и}{C}, \qquad (IX.73)$$

where

$$I_{ср} = \frac{I_{нач} + I_{кон}}{2} = I_{нач}\left(1 - \frac{\beta_м}{2}\right). \qquad (IX.74)$$

Transistor T_1 unblanks when the switching pulse ceases and capacitor C charges to the initial value. *There is a requirement to insure a transistor* T_1 saturation *mode for the purpose of reducing circuit recovery time, so this selection is made*

$$R_б < \beta_{мин} R_к.$$

EXERCISE IX.25

What is the purpose for connecting resistance $R_к$ to the transistor T_1 collector network? (Page 513)

In conclusion, we will introduce a circuit used in practice (Figure IX.40). A divider composed of resistances R_1--R_2--R_3 is used in the circuit instead of

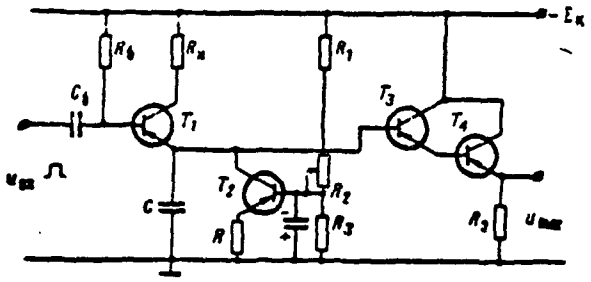


Figure IX.40. Practical Transistor Current-Stabilizing One-Port GPN Circuit.

a negative bias source. Variable resistance R_2 makes it possible to control output voltage amplitude. The following transistors are used in this circuit: P16A, P16B, MP42B, and P26B as switching transistor T_1; P16B, P26B, and P106 as /436 current-stabilizing transistor T_2; P16A, P16B, P26B, and MP42 in the emitter follower.

3. Positive Voltage Feedback Sawtooth Generator

A transistor positive voltage feedback GPN circuit (Figure IX.41) is analogous to the electron tube circuit (Figure IX.18). Transistor T_1, playing the role of switch, is unblanked and will be at saturation in the initial state. This is achieved through selection of resistance $R_б < \beta_{min} R_к$. Diode D also is unblanked. Capacitor C voltage approximates zero. Transistor T_2 is connected to the emitter follower circuit and is intended to accomplish positive voltage feedback. Capacitor C is charged to voltage $U_{C2\,нач}$ approximately equalling $E_к$, since the voltage drop across conducting diode D internal resistance and resistance $R_э$ are slight.

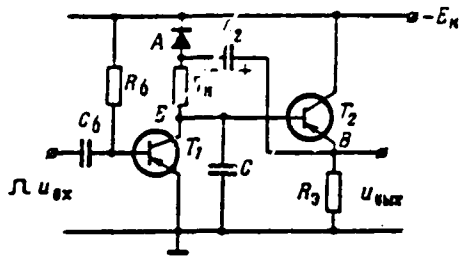


Figure IX.41. Transistor Positive Feedback GPN Circuit.

Switching transistor T_1 and diode D are blanked when a positive-polarity switching pulse arrives and capacitor C begins to charge. Capacitor C_2, whose selected capacitance is significantly greater than that of capacitor C, plays the role of voltage source. As was the case for the tube circuit, charging current virtually does not change and the rate of capacitance C voltage rise remains unchanged. This is because emitter follower output voltage (point $В$) /437 decreases simultaneously with a capacitor C voltage decrease. This voltage change across feedback capacitor C_2 is transmitted to diode D plate (point A). Since emitter follower transfer constant $K_{эп} \approx 1$, then the potential difference between points A and $Б$ is retained as constant and the current flowing across resistance $R_к$ and capacitor C will be constant. Consequently, capacitor C voltage will change by a linear law (Figure IX.42b).

Transistor T_1 unblanks when the switching pulse ceases and capacitor C discharges across it. Discharging time is determined just as it was for the R-C integrator GPN circuit. Discharging time $t_р$ turns out to be insignificant since a bottoming mode is provided for transistor T_1. Reestablishment of capacitor C_2 charging begins after capacitor C discharge since diode D remains blanked during this entire time and the capacitor C_2 charging network turns out to be open. Therefore, overall circuit recovery time will be determined by the expression

$$t_в = t_р + t_в, \qquad (IX.75)$$

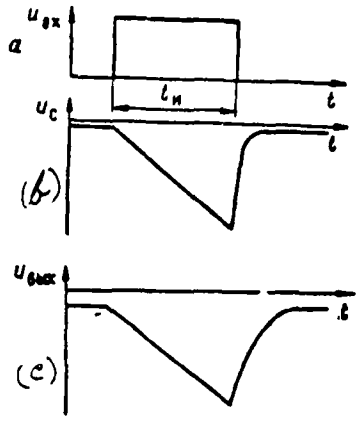


Figure IX.42. Voltage Curves for a Positive Feedback GPN Circuit.

where $t_р$ -- capacitor C discharging time;
$t_з$ -- capacitor C_2 milking time:

$$t_з = (3 \div 5)\, C_2 (R_к + R_э).$$

The second term in expression (IX.75) has great weight since capacitor C_2 capacitance magnitude is significantly greater than that of capacitor C. The magnitude of resistance $R_э$ must be decreased in order to decrease capacitor C_2 charging time. However, transistor T_2 input resistance and emitter follower transfer constant $K_{эп}$ decrease here, which leads to a deterioration in the linearity of the shaped voltage.

EXERCISE IX.26

How can circuit recovery time $t_в$ be decreased without harming output voltage linearity? (Page 513)

The amplitude of the generated voltage is determined by known formula /438

$$U_м \approx \frac{I_{нач} t_и}{C}.$$

where $I_{нач}$ -- initial charging current value:

$$I_{нач} = \frac{E_к}{R_к}.$$

The nonlinearity factor for the given sawtooth generator may be written by means of an analogy with the nonlinearity factor for an electron tube circuit

$$\gamma_н = \frac{U_н}{E_к}\left(1 - K_{эп} + \frac{C}{C_э}\right), \qquad \text{(IX.76)}$$

where $K_{эп}$ -- emitter follower gain:

$$K_{эп} = \frac{R_э}{r_э + R_э + r_б(1-\alpha)}.$$

The shunting action of blanked transistor T_1 is not considered in expression (IX.76) since the resistance $R_к$ magnitude usually is much less than transistor T_1 resistance $r_к$.

P25B, P26B, and P104 transistors are used in the circuit in the emitter follower and P16A, P26, and P106 transistors are used as the switching element. D101, D201, D204, and other such diodes may be used as diode D.

The major advantage of this generator is its slight output resistance, which equals emitter follower output resistance during the working stroke.

4. Negative Voltage Feedback Sawtooth Generator (Integrator)

The simplest circuit for a generator of this type is depicted in Figure IX.43a. Transistor T is blanked in the initial state due to bias source $E_{см}$. Base potential equals zero. Capacitor C is charged to voltage $E_к$.

Diode D blanks and transistor T unblanks when a negative-polarity switching pulse is supplied to input. The sum of the capacitor C discharging currents and the current flowing across resistance $R_к$ determines collector current following unblanking. Evidently this mode occurs when transistor T base voltage is negative. Consequently, base voltage step ΔU (Figure IX.44c) and the collector voltage step equal to it (Figure IX.44b) turn out to be negative. It is possible to eliminate

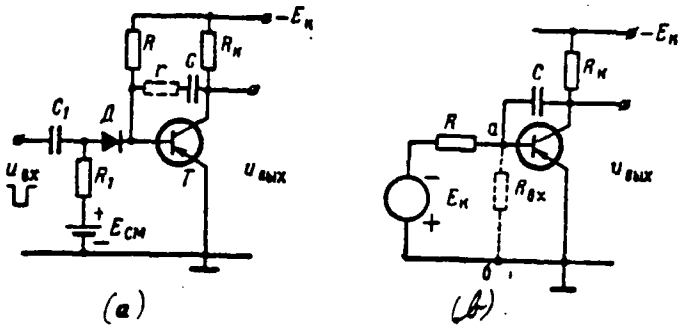


Figure IX.43. Transistor Negative Feedback GPN Circuit: (a) -- Equivalent circuit; (b) -- Simplified circuit.

the collector voltage step if relatively-slight resistance r (depicted by the dotted line in the figure) is connected in series with capacitor C. As was the case previously, transistor T base voltage decreases with a jump by magnitude ΔU the moment the switching pulse is supplied. However, capacitor C discharging current creates a voltage drop across resistance r of such polarity that the collector voltage step is determined by the difference:

$$\Delta U_к = \Delta U - I_{р\,нач} r,$$

where $I_{р\,нач} \approx \frac{E_к}{R}$ -- initial discharging current value.

Having selected resistance r magnitude from the condition

$$\Delta U = \frac{E_к}{R} r,$$

it is possible to obtain complete initial collector voltage compensation.

The generator circuit in running order is a conventional integrating amplifier with a feedback network formed by capacitor C and resistance R. Voltage $-E_к$ is supplied to integrator input.

The physical processes occurring in the circuit are analogous to the processes

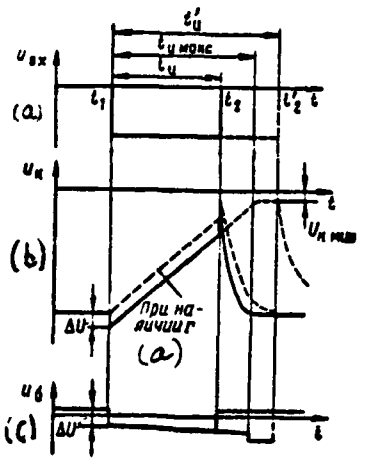


Figure IX.44. Voltage Curves for the Figure IX.43 GPN Circuit.

in an identical tube generator, i. e., capacitor C discharge with virtually constant current occurs in the circuit as a result of negative feedback. Actually, the discharging current decrease causes a decrease in base potential and, /440 consequently, a collector current increase. Collector potential increases, thus constraining the discharging current decrease. The capacitor C discharge with constant current stipulates output voltage linearity. The representative point attains the criticality line ($u_к \approx 0$) if switching pulse duration exceeds the R-C time constant and the transistor loses amplifying properties. Capacitor linear discharge ceases and a horizontal sector appears in the collector voltage curve.

Shaped voltage U_M amplitude almost equals supply source voltage $E_к$, i. e., the source voltage utilization factor approximates unity. The slight deviation from unity is explained by the fact that, on the one hand, initial voltage does not equal $E_к$, differing by magnitude $I_{к0}R_к$, and, on the other, the voltage drop across the saturated transistor $U_{к\,нас}$ differs from zero. Magnitude $U_{к\,нас}$ does not exceed 0.1--0.2 V for low-power alloy transistors. Current $I_{к0}$ magnitude for P14 and P15 germanium transistors at room temperature does not exceed 5--10 uA or 1.0 uA for P104 germanium transistors. Resistance $R_к$ magnitude usually is no more than 10 kilohms. Therefore, sawtooth voltage amplitude U_M differs

from $E_к$ by no more than 0.2—0.3 V. Since the rate of output voltage change is determined by the expression

$$p = \frac{du_C}{dt} \approx \frac{I_{нач}}{C} = \frac{E_к}{RC},$$

and maximum amplitude $U_м \approx E_к$, then the maximum switching pulse duration at which voltage linearity is provided during a complete forward motion equals

$$t_{и\ макс} \approx RC. \qquad \text{(IX.77)}$$

Diode D unblanks the moment the switching pulse ceases. Base and collector voltage increase with a jump.

EXERCISE IX.27

Why isn't the collector voltage step compensated for when the switching pulse ceases? (Page 513)

Capacitor C charging begins after this. Recovery time may be considered to equal

$$t_в = (3 \div 5) C [R_к + R_д + R_1] \approx (3 \div 5) CR_к,$$

since usually $R_к \gg (R_д + R_1)$.

The same methods used in tube circuits to reduce recovery time may be used here. For example, clamping the initial level in the transistor collector /441 at level $-E_ф$ (in absolute value less than voltage $E_к$) with the aid of diode D_2, as shown in Figure IX.45, often is used. In this event, recovery time is determined by the formula

$$t_в = CR_д \ln \frac{E_к}{E_к - E_ф}. \qquad \text{(IX.78)}$$

Just as was the case in tube circuits, this method leads to a decrease in output voltage amplitude for given supply source $E_к$.

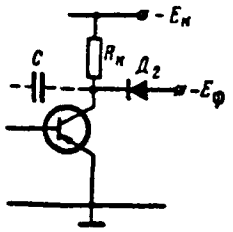


Figure IX.45. Clamping Diode Connection To Reduce Recovery Time.

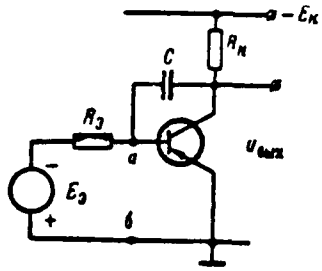


Figure IX.46. Corrected Positive Feedback GPN Circuit During a Working Stroke.

The nonlinearity factor in the transistor integrator circuit is determined, just as it was for the electron tube integrator circuit, i. e.,

$$\beta_н = \frac{t_н}{\tau_э}.$$

The difference lies only in determination of the equivalent time constant $\tau_э$. It is necessary to consider that a transistor, as opposed to an electron tube, has finite input resistance value $R_{вх}$.

A simplified integrator circuit in running order is presented in Figure IX.43b. Here, input resistance conditionally is depicted by the dotted line. After transformation by the theorem of the equivalent generator, the input network has the form depicted in Figure IX.46. Here, resistance $R_э = \frac{RR_{вх}}{R + R_{вх}}$.

Consequently, the equivalent time constant is determined by the expression

$$\tau_э = CR_э(K+1) = C\frac{R_{вх}R}{R_{вх}+R}(1+K) = (1+K)RC\frac{1}{1+\frac{R}{R_{вх}}}. \qquad (IX.79)$$

where K -- common-emitter amplifier gain; /442

$R_{вх}$ -- common-emitter amplifier input resistance.

Input resistance and gain may be determined by formulas (III.114) and (III.117), respectively.

Thus, finally, the nonlinearity factor magnitude will be written in the form

$$\beta_{\text{н}} = \frac{t_{\text{н}}}{(1 + K_j)RC}\left(1 + \frac{R}{R_{\text{вх}}}\right). \qquad \text{(IX.80)}$$

CHAPTER X /443

EXERCISE ANSWERS AND EXPLANATIONS

EXERCISE I.1

a) For passive response RLS, emitted radio waves are distributed to the object (target), reflected from it, and returned to the RLS. Therefore, the time from the moment of pulse radiation to the moment of its receipt is $t_r = \frac{2r}{C}$, hence $r = \frac{C}{2} t_r$.

For active response RLS, there is a requirement additionally to consider relaying time at the object (transponder tripping time) t_p. Therefore, $t_r = \frac{2r}{C} + t_p$, hence $r = C \frac{t_r - t_p}{2}$.

b) From the aforementioned condition, $t_r < T_п$ must be satisfied, hence $r_{max} =$. Where T = 600 usec, $r_{max} = \frac{3 \cdot 10^8 \cdot 600 \cdot 10^{-6}}{2} \approx 90$ km.

c) Gate pulse delay time must correspond to second target lag time $t_з = \frac{2r_1}{C} = \frac{2 \cdot 85 \cdot 10^3}{3 \cdot 10^8} \approx 567$ usec. The shorter the gate pulse $t_{з.и}$ duration, the more accurate (precise) the target signal gating. However, this duration must be sufficient so the target gated pulse completely will pass through the receiver even when there is a possible gate pulse delay inaccuracy. Therefore, $t_{з.и} = t_п + 2\tau_{ош}$, where $t_п$ -- received target pulse duration, $\tau_{ош}$ -- maximum error in the automatic tracking system producing the gate pulses.

d) Individual measurement of range to each of two targets from the display is possible if the pulses from these targets are visible individually, i. e., the pulse from the most-distant target arises after cessation of the pulse from the nearest target (otherwise, the pulses will combine). Consequently, the minimal difference in lag times is $\Delta t_{min} = t_{z2} - t_{z1} = t_u$, hence $\Delta r_{min} = C \frac{\Delta t_{min}}{2} = C \frac{t_u}{2}$. For example, where t_u = 0.5 usec, Δr_{min} = 75 meters. The requirement is that only the pulse from a given target must coincide with strobe pulses for the automatic tracking system to track that target. Consequently, in this case, the total duration of the strobe pulse pair $t_{стр\Sigma}$: $\Delta r_{min} = C \frac{\Delta t_{стр\Sigma}}{2}$ constrains this value.

e) Calibrating pulse spacing to create range marks at interval Δr_u = 5 km must equal $T_u = \frac{2\Delta r_u}{C} \approx$ 33 usec or their frequency $F_u = \frac{1}{T_u}$ = 30 kHz.

f) The number of pulses in a packet (see Figure I.8) equals $N_u = \frac{T_n}{T_u}$, /444 where $T_n = t_{обл} = \frac{\Theta_{обл}}{\Omega_{сн}}$ -- packet duration (target painting time), $\Omega_{сн} = \frac{\Delta_{сн}}{T_{пх}}$ -- scanning rate, $T_{пх} = T_{сн} - T_{ох}$ -- beam forward stroke time, $T_{сн} = \frac{1}{F_{сн}}$ -- scanning period. In accordance with the conditions of the problem, $T_{сн} = \frac{10^3}{20}$ = 50 usec; $T_{пх}$ = 50 -- 10 = 40 usec; $t_{обл} = \frac{2}{0.75} \approx 2.67$ usec; $T_u = \frac{1}{F_u} = \frac{10^3}{2.5 \cdot 10^3} = 0.4$ usec; and $N_u = \frac{2.67}{0.4} \approx 6.7$ pulses. Rounding off the result to the nearest whole number, we will get N_u = 6 pulses.

Where $t_з$ = 32 usec, $\varphi_u = \Omega_{сн} t_з = 0.75 \cdot 32 = 24°$.

EXERCISE I.2

A functional diagram of a synchronizer and range display corresponding to the Figure I.9 curves is depicted in Figure X.1.

EXERCISE II.1

The given curves are depicted in Figure X.2. First off, we will recall that, in the graphs, circuit time constant T equals a subtangent--the segment intercepting the tangent to the initial point of the exponential curve on the horizontal line towards which the exponential curve will strive to infinity (see Attachment 3). This circumstance facilitates plotting and comparing exponential curves.

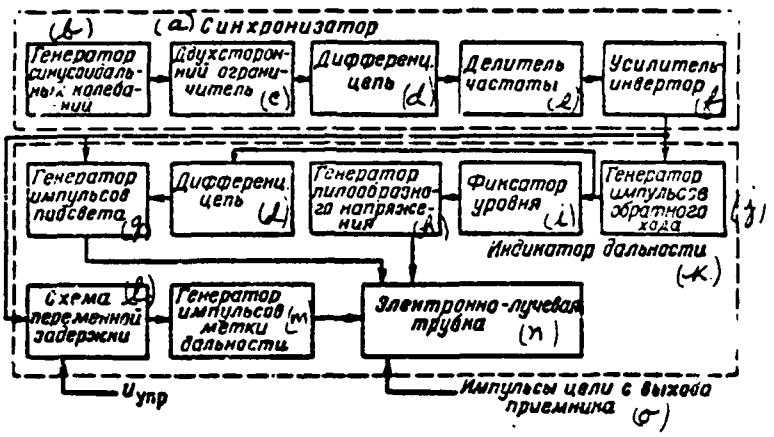


Figure X.1. For Exercise I.2.

KEY: (a) -- Synchronizer; (b) -- Harmonic oscillator; (c) -- Bidirectional clamps; (d) -- Differentiator; (e) -- Frequency divider; (f) -- Amplifier-inverter; (g) -- Intensifier pulse generator; (h) -- sawtooth generator; (i) -- Clamp; (j) -- Flyback pulse generator; (k) -- Range display; (l) -- Variable delay circuit; (m) -- Range marker pulse generator; (n) -- Cathode-ray tube; (o) -- Target pulses from receiver output.

The letter a in Figure X.2 designates initial curves corresponding to Figure II.2a, i. e., time constant $T = RC$.

The voltage towards which the capacitor will strive to charge, initial current i_0 values, and voltage u_R decrease accordingly when source voltage decreases by a factor of 2 $\left(E' = \frac{E}{2}\right)$. The circuit time constant, i. e., the duration /445 of the charging process, remains unchanged. Therefore, in accordance with (XI.13), the rate of function u_C, i_0, and u_R change decreases by a factor of 2 (curves).

Time constant $\tau = C'R = 2\tau$ rises by a factor of 2 when the capacitance increases by a factor of 2 ($C' = 2C$). Therefore, the duration of the charging process increases by a factor of 2, i. e., the rate of function u_C, i_0, and u_R change decreases by a factor of 2 (curves).

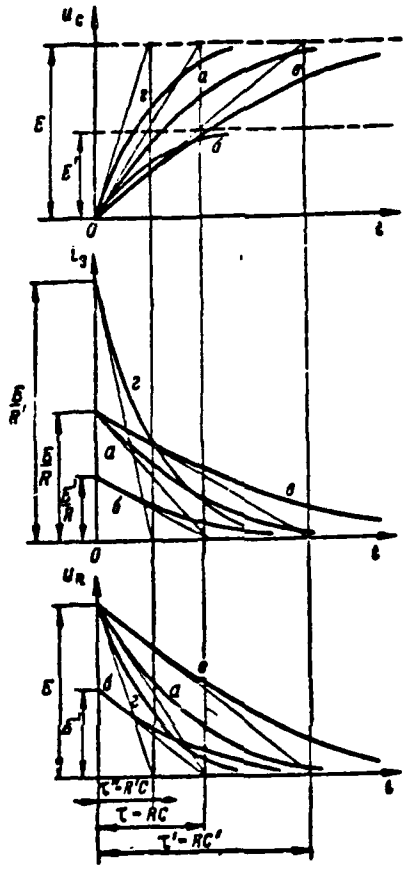


Figure X.2. Voltage and Current Curves As A Capacitor Charges Across Resistance: (a) -- For Initial Values E, R, C; (b) -- For $E_1 = \frac{E}{2}$; (c) -- For $C_1 = 2C$; (d) -- For $R_1 = \frac{R}{2}$.

Circuit time constant $\tau' = CR' = \frac{\tau}{2}$ decreases by a factor of 2 when the /446 resistance decreases by a factor of 2 ($R' = \frac{R}{2}$). Therefore, charging time decreases by a factor of 2, i. e., the rate of function u_C, i_3, and u_R change rises by a factor of 2. In addition, the initial charging current value rises by a factor of 2 $I_3 = \frac{E}{R}$ (curve 2).

EXERCISE II.2

These curves are plotted in Figure X.3. Inductance L discharging time constant

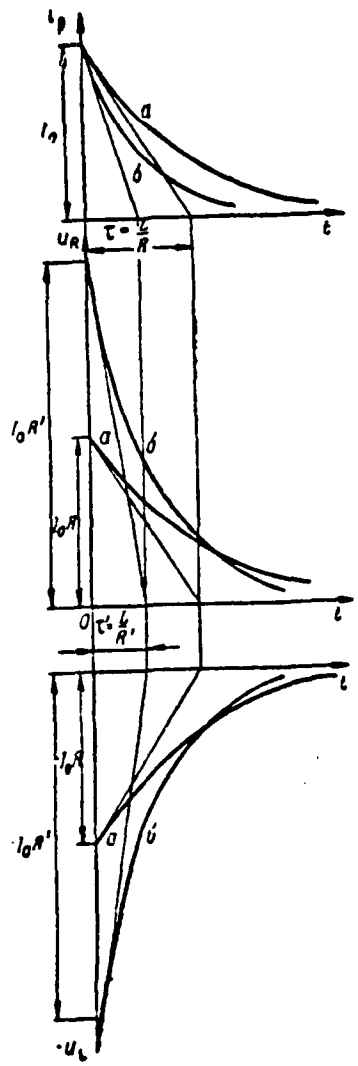


Figure X.3. Current and Voltage Curves When Inductance Discharges Across Resistance: (a) -- For initial values I_0, L, R; (b) -- For $R_1 = 2R$.

changes by a factor of 2 $\tau' = \frac{L}{R'} = \frac{\tau}{2}$, where $\tau = \frac{L}{R}$ -- initial time constant, when resistance R is increased by a factor of 2 (R' = 2R). Therefore, the duration of the charging process is reduced by a factor of 2. The initial value of the current in inductance $I_0 = I_p$ does not change since the previous inductance charging circuit parameters determine it and they are retained at the moment discharging begins. Therefore, the discharging current i_p decrease occurs faster by a factor of 2.

Initial voltage value $u_R = -u_L$ increases by a factor of 2: $U_R' = I_0 R' = 2I_0 R$; $U_L' = -I_0 R' = 2I_0 R$. This is explained from the physical point of view by the fact that, when resistance R increases, the power dissipated in this resistance in the form of heat rises $P = i_p^2 R$. Therefore, the electromagnetic energy stored in the inductance magnetic field is expended more rapidly and, consequently, the rate of current i_p decrease rises. But, here, self-induction emf rises $e_L = -L\frac{di_p}{dt}$; consequently, voltages $u_L = -e_L$ and $u_R = -u_L$. Since the initial values of voltages u_R and u_L rise by a factor of 2, while the time constant decreases by a factor of 2, the rate of decrease of these voltages increases by a factor of 4.

Thus, the resistance R increase in the inductance discharging circuit, given the identical initial discharging current, causes a proportional rise of /447 initial U_L and U_R values. This circumstance is of important practical significance. First, it must be considered in circuits where a disruption of the inductance coil supply circuit from the constant voltage supply occurs.

It is a case where inductance coil discharge to the large resistance of the disruption path itself occurs when this circuit is broken. Therefore, at the moment of disruption, coil voltage rises with a jump to such a large magnitude (where $R = \infty$ $u_L = \infty$), and an electrical breakdown between coil turns or to "ground" may occur. To avoid a breakdown, the coil usually is shunted by a special resistance $R_ш$, the magnitude of which is sufficiently small so that the voltage u_L "bump" is within tolerances when the circuit is disrupted..

Second, the possibility of obtaining large voltage u_L at the moment the inductance supply circuit is disrupted specially may be used in those instances when there is a requirement to obtain pulse voltages of great amplitude exceeding

constant supply voltage. A pulse modulator with an inductive energy integrator is one of the devices in which this principle of increasing voltage is used (see Chapter II, § 1).

EXERCISE II.3

a) During resting time $t_п$ energy $W_п = P_{ср} t_п \approx P_{ср} T_и$ (where $Q \gg 1$, $t_п \approx T_и$), where $P_{ср}$ -- average power consumed from the supply source, i. e., average transmitter power, is stored in the integrator. Since modulating pulse energy equals $W_и = P_и t_и$, where $P_и$ -- pulse power and, with respect to the law of power retention, $W_п = W_и$, then $P_{ср} T_и = P_и t_и$. Consequently, $P_и = P_{ср} \frac{T_и}{t_и} = P_{ср} Q$, which corresponds to formula (I.6).

b) There is a requirement that, during pulse time $t_и$, capacitor $C_М$ be discharged slightly (see Figure II.7), i. e., that condition $\tau_р \gg t_и$ be satisfied, in order to decrease pulse tilt reduction $\Delta U_и = \Delta U_C$ in a modulator with a capacitive integrator. In this case, charging current amplitude $I_1 = \frac{\Delta U_C}{R_0}$ also decreases, which will lead to a reduction in losses in the charging network and, due to this, to an increase in modulator efficiency. However, given a slight ΔU_C magnitude, only an insignificant portion of the energy stored in the capacitor is supplied to the microwave oscillator during the discharging process

$$\Delta W_C = W_{C\,макс} - W_{C\,мин} = \frac{C_и (U^2_{C\,макс} - U^2_{C\,мин})}{2} = \frac{C_и \Delta U_C (U_{C\,макс} + U_{C\,мин})}{2}.$$

Hence, it follows that an increase in pulse energy, given source voltage $E_0 = U_{C\,макс}$ and ΔU_C value, is possible only due to an increase in capacitor $C_М$ capacitance.

c) Condition $\tau_з \ll t_п$ must be satisfied for complete choke charging, i. e., charging current to rise to its maximum value $I_L = \frac{E_0}{R_з}$, to occur in a modulator with a capacitive integrator during resting time. Here, pulse amplitude equals $U_и = I_L R_з = E_0 \frac{R_з}{R_0}$ and condition $U_а \gg E_0$ will be satisfied when $R_з \gg R_0$, i. e., $\tau_з \ll \tau_1$. Pulse tilt reduction $\Delta U_и = \Delta I_L R_з$ will be slight if during discharge time $t_и$ the current ΔI_L decrease will be slight, i. e., $\tau_з \gg t_и$. Simultaneous satisfaction of conditions $\tau_з \ll t_п$, $\tau_з \ll \tau_р$, $\tau_р \gg t_и$ is possible only when the shaped pulse duty ratio is high (where $t_и \ll t_п$).

EXERCISE II.4

a) R-C integrator output voltage is picked off capacitor C, while resistance R is connected in series between network input and output. Therefore, the following are R-C integrators: network C_2R_2 in Figure II.14; R_1C_1 in Figure II.16; /448 R_aC_a (plate filter) and $R_{c3}C_{c3}$ (screen grid supply network) in Figure II.18; R_aC in Figure IX.4.

b) The time constant of the Figure II.11b R-C network for the parameters given equals $\tau = RC = 10^3 \cdot 300 \cdot 10^{-12} = 10^{-6} = 3$ usec. However, it is impossible to designate network purpose. One may only assert that it is not an integrator (but this is evident without knowing network parameters). It is impossible to determine if this is a differentiator or a transient network, even knowing its time constant, if input pulse duration is not given. Where $t_и \gg \tau$, it will be a differentiator, and will be a transient network when $t_и < \tau$.

The Figure II.11d R-L network, where $\tau \gg t_и$, transmits a pulse virtually without distortions (see the Figure II.10c voltage u_L curve where $\tau = \tau_2 > t_и$). However, it may not be used as a transient network because its input and output are not separated with respect to the d-c component.

EXERCISE II.5

a) In accordance with (XI.15), complete capacitor charging time is $t_{зар.пол} = 3\tau$. Therefore, if $t_{и.вх} > 3\tau$, then capacitor charging essentially ceases ($U_{вых} = U_{вх}$) and output pulse porch duration corresponds to complete charging time $t_ф = 3\tau$. If

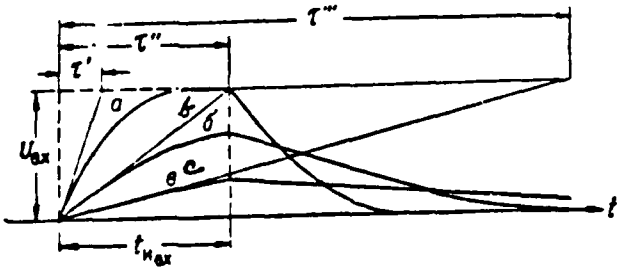


Figure X.4. Ratio of Pulse Shape at R-C Integrator Output To Its Time Constant $(\tau_1 < \tau_2 < \tau_3)$.

$t_{и\,вх} < 3\tau$, then the capacitor charging does not cease while the input pulse is active ($U_{вых} < U_{вх}$) and $t_ф = t_{и\,вх}$. Thus, $t_ф < t_{и\,вх}$. Complete capacitor discharging time following input pulse cessation $t_{сп} \approx 3\tau$* determines output pulse decay time. Complete output pulse duration

$$t_{и\,вых} = t_{и\,вх} + t_{сп} \approx t_{и\,вх} + 3\tau$$

b) These curves are plotted in Figure X.4. Where R = 1 kilohm, C = 1,000 pF, network time constant $\tau = 10^3 \cdot 10^{-9} \cdot 10^6 = 1$ usec, i. e., $t_{и\,вх} = 4\tau$. Since $t_ф \approx 3\tau$, then $U_{вых} \approx U_{вх}$, $t_{и\,вых} \approx t_{и\,вх} + 3\tau = 7$ usec (curve a).

Where R = 20 kilohm, C = 200 pF, $\tau' = 20 \cdot 10^3 \cdot 200 \cdot 10^{-12} \cdot 10^6 = 4$ usec, i. e., $t_{и\,вх} = \tau'$. With respect to time constant determination, we will get $U_{вых} \approx 0{,}63\ U_{вх}$, $t_{и\,вых} \approx 16$ usec (curve b).

Where R = 2 kilohm, C = 0.006 uF, $\tau'' = 2 \cdot 10^3 \cdot 6 \cdot 10^{-9} \cdot 10^6 = 12$ usec, i. e., $\tau'' = 3t_{и\,вх}$. In this event, the output voltage porch virtually is linear and, therefore, $U_{вых} \approx U_{вх} \frac{t_{и\,вх}}{\tau''} = \frac{U_{вх}}{3}$ (curve c).

EXERCISE II.6 /449

The time constant for stretching network $T = R_2C_2$ must satisfy conditions $\tau > t_{и1}$, $3\tau < t_{и2}$, $3\tau < T_{и2} - t_{и1} - t_{и2}$ for normal operation of the Figure II.14 coincidence circuit. Second grid voltage (capacitor C_2 voltage) rises slightly while pulse A is active when the first condition is satisfied, resulting in the pentode not unblanking while this pulse is active. In addition, when this condition is satisfied, while pulse $б$ is active, second grid voltage decreases slightly from its maximum value, which also insures that the pentode unblanks while this pulse is active.

Satisfaction of the second condition insures completion of the capacitor C_2 charging process while pulse $u_{вх2}$ is active, resulting in voltage u_{C2} succeeding in rising to its amplitide $U_{вх2}$ by the end of this pulse. This makes it possible to use pulses $u_{вх2}$ of minimum amplitude, which must only be sufficient for pentode unblanking with respect to the second grid.

*If resting time between input pulses is sufficiently great for completion of the discharging process, $t_п > 3\tau$.

Satisfaction of the third condition insures completion of the capacitor C_2 discharging process during resting times. Otherwise, there would be residual voltage exceeding second grid potential present in the capacitor at the beginning of the subsequent pulse [illegible]. As a result, pentode unblanking might become possible in spite of the first condition being satisfied.

EXERCISE II.7

a) Triggering pulse duration determines maximum time delay [illegible] in the Figure II.15 circuit and will be obtained if capacitor C_1 voltage at the moment the triggering pulse ceases still continues to rise at a sufficiently-high rate. This requires satisfaction of condition $\tau = R_1C_1 > \frac{t_{in}}{3}$ (capacitor charging must not cease during time [illegible]).

b) In the Figure II.16 circuit, triode L_1 unblanks at moment $t = t_1$, when $u_g = E_{go}$. Therefore, in accordance with (II.37) $E_{go} = U_{go} + (E_a - U_{go})\left(1 - e^{-\frac{t_1}{\tau}}\right)$, hence

$$e^{\frac{t_1}{\tau}} = \frac{E_a - U_{go}}{E_a - E_{go}} \qquad \text{or} \qquad t_3 = t_1 = \tau \ln \frac{E_a - U_{go}}{E_a - E_{go}}.$$

Initial negative triode grid voltage equals

$$U_{go} = E_g + \frac{E_a - E_g}{R_1 + R_2} R_2 = -300 + \frac{600}{2.2 \cdot 10^6} \cdot 2 \cdot 10^6 \approx -245 \text{ V},$$

while the integrator time constant comprises

$$\tau = R_1C_1 = 2 \cdot 10^6 \cdot 2 \cdot 10^{-6} = 4 \text{ sec}.$$

The unknown time delay will equal

$$t_3 = t_1 = 4 \ln \frac{300 + 245}{300 + 8} = 4 \ln 1.77 \approx 2.3 \text{ sec}.$$

The circuit will trip without a time delay if, due to assembly error, capacitor C is disconnected from triode grid or chassis. Here, triode grid voltage rises with a jump to value [illegible] at the moment of triggering (relay P_1 trips).

EXERCISE II.8 /450

Proportional relationship (II.38) $U_{вых} \sim f_{вх}$ is obtained when network output voltage rises by a linear law while the input pulse is active (i. e., corresponds to the initial sector of the exponential curve). But, this requires that $\tau > t_{вх\ макс}$. The amplitude of each output pulse must not depend on the previous pulse and the network output voltage during resting times must disappear completely. This means that condition $\tau \leq \frac{t_{п\ мин}}{3} = \frac{T_и - t_{и.вх.макс}}{3}$ must be satisfied.

EXERCISE II.9

It is possible qualitatively to explain the form of an R-C integrator AChKh (Figure II.18b). Capacitor C connected in parallel to circuit output terminals is an infinitely-large resistance $X_C = \frac{1}{j\omega C} = \infty$ for constant voltage (ω = 0). Therefore, constant voltage will be transmitted in full (without attenuation) to network output, i. e., $K(0) = K(\omega)_{макс} = 1$. Capacitor resistance decreases with an increase in harmonic input voltage frequency, resulting in output voltage and, consequently, AChKh value, drop. Within the range $\omega \to \infty$ $X_C \to 0$, i. e., network output is shunted for a short time, while output voltage disappears. Therefore, the AChKh asymptotically will strive towards zero.

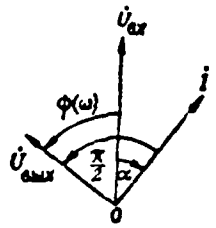


Figure X.5. R-C Integrator Vector Diagram.

It is convenient to explain the shape of this network AChKh (Figure II.18c) using a vector diagram of the complex amplitudes in the network depicted in Figure X.5.*

*Positive phase angles are computed clockwise in Figure X.5.

First, we will recall that current flowing across a resistance always leads the phase in this capacitance by angle $\frac{\pi}{2}$. Since this particular network includes series-connected resistance and capacitance, then the complex amplitude vector of the network current $\dot{I}$ will lead the complex amplitude vector $U_{вх}$ by angle $\varphi: \frac{\pi}{2} > \varphi > 0$. The magnitude of this angle will depend on the ratio of the active and capacitive resistance in the network, so, since the latter will depend on frequency, then $\varphi = \varphi(\omega)$. Output voltage is picked off capacitance C. Therefore, the vector of complex amplitude $U_{вых}$ always will lag behind vector $\dot{I}$ by angle $\frac{\pi}{2}$. As a result, vector $\dot{U}_{вых}$ will lag behind vector $\dot{U}_{вх}$ by angle $\psi(\omega) = \varphi(\omega) - \frac{\pi}{2}$. Consequently, output voltage always will lag input voltage in phase (all resultant AChKh values are negative). As a result of the infinitely-large capacitive resistance, for constant voltage $\varphi(0) = \frac{\pi}{2}$ and $\psi(0) = 0$, i. e., there is no phase shift. Angle $\varphi(\omega)$ decreases and the output voltage phase lags more and more behind input voltage phase when the frequency increases as a result of the decrease in capacitive resistance. Therefore, within the range $\omega \to \infty$ $X_C \to 0$, $\varphi(\omega) \to 0$ and $\psi(\omega) \to -\frac{\pi}{2}$.

EXERCISE II.10 /451

These curves are plotted in Figure X.6 ($u_{вых}$ curves corresponding to Figure II.21 and the paragraph c problem are depicted by the dotted line).

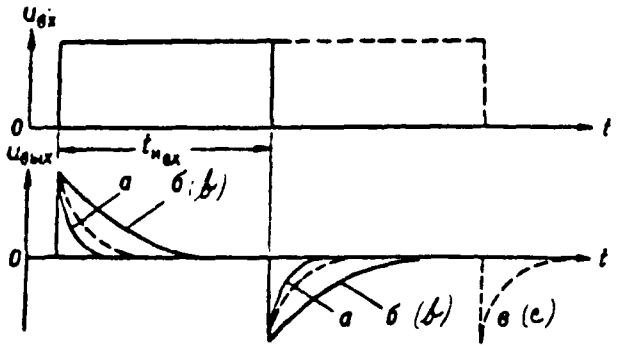


Figure X.6. Differentiator Output Voltage Change:
(a) -- Where τ Decreases by a Factor of 2; (b) -- Where τ Increases By a Factor of 2; (c) -- Where $t_{имп}$ Increases By a Factor of 2.

Capacitor charging and discharging are faster when time constant τ decreases, resulting in output pulses being clipped accordingly (curve a).

Capacitor charging and discharging are slower, resulting in output pulses being stretched accordingly (curve b), when time constant τ decreases.

Output pulse shape does not change when $t_{имп}$ increases, but a pulse corresponding to the input pulse droop displaces accordingly (curve c).

EXERCISE II.11

a) These voltage curves are depicted in Figure X.7. Pulses $u_{вых1}$ with a vertical porch and exponential droop, amplitude $U_{вых1}=U_{вх}$, and duration $t_{и вых1}\approx 3\tau$ (curves $u_{вых1}$ in Figure X.7b-d) arise at R-C chopper output when a change in

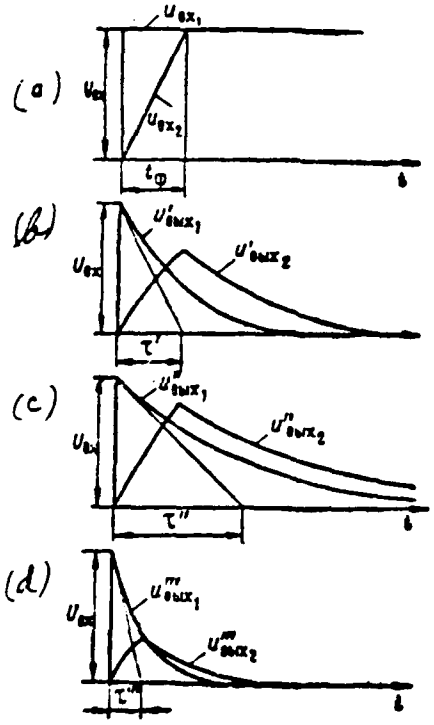


Figure X.7. Passage of Changes in Voltage with Vertical and Sloping Porches Across a Stretching R-C Network At Different τ Values.

voltage $u_{вх1}$ with a vertical porch is active at its input. In accordance with

Figure II.22, pulses $u_{вых2}$ with an exponential porch and droop (curves $u_{вых2}$ in Figure X.7b, c, d) arise when change in voltage $u_{вх2}$ with a sloping linear porch is active at network input. Based on (II.44), we will get:
where $\tau' = t_\phi\, U'_{вых2} \approx 0.63 U_{вх}$* (Figure X.7b); $\tau'' = 2t_\phi\, U''_{вых2} \approx 0.8 U_{вх}$ (Figure X.7c);
where $\tau''' = 0.5 t_\phi\, U'''_{вых2} \approx 0.43 U_{вх}$ (Figure X.7d).

b) In accordance with (II.31), inequality $\tau \ll t_\phi$ is the condition for pulse porch differentiation. However, here, based on (II.44a), we will get $\frac{U_{вых}}{U_{вх}} \ll 1$. Thus, the more precisely the porch is differentiated, the less the network /452 output voltage.

EXERCISE II.12

The expression for the complex frequency characteristic for the Figure II.25c compensated voltage divider equals:

$$\dot{K}(\omega) = \frac{\dot{U}_{вых}}{\dot{U}_{вх}} = \frac{\dot{Z}_2}{\dot{Z}_1 + \dot{Z}_2},$$

where $\dot{Z}_1 = \dfrac{\dfrac{R_1 \frac{1}{j\omega C_в}}{R_1 + \frac{1}{j\omega C_в}}}{} = \dfrac{R_1}{1 + j\omega C_в R_1} = \dfrac{R_1}{1 + j\omega\tau_1}$;

$$\dot{Z}_2 = \frac{\dfrac{R_2 \frac{1}{j\omega C_{вх}}}{R_2 + \frac{1}{j\omega C_{вх}}}}{} = \frac{R_2}{1 + j\omega C_{вх} R_2} = \frac{R_2}{1 + j\omega\tau_2};\ \tau_1 = C_в R_1;\ \tau_2 = C_{вх} R_2.$$

Therefore, /453

$$\dot{K}(\omega) = \frac{\dfrac{R_2}{1 + j\omega\tau_2}}{\dfrac{R_1}{1 + j\omega\tau_1} + \dfrac{R_2}{1 + j\omega\tau_2}}.$$

*The graph in Figure 6b (page 526) may be used for approximate determination of exponential function $\left(1 - e^{-\frac{t_\phi}{\tau}}\right)$ for given values $\frac{t_\phi}{\tau}$.

Where $\tau_1 = \tau_2$ (this equates to ratio (II.46)), we will get $\dot{K}(\omega) = \frac{R_2}{R_1 + R_2} = \text{const}$, which corresponds to undistorted pulse transmission condition (XI.24).

EXERCISE II.13

a) *The Figure III.18 transient networks are* $C_{p_1}R_{g_1}$, $C_{p_2}R_{ex}$; Figure III.29 -- $C_{p_1}R_{g_1}$, $C_{p_2}R_{g_2}$; Figure VI.5 -- $C_{p_1}R_{g_1}$, $C_{p_2}R_{g_2}$; Figure VI.10 -- all networks $C_{p_1}R_{p_1}$, $C_{p_2}R_{p_2}$.

b) These curves are plotted in Figure X.8. They reflect the process of capacitor charging across a resistance and demonstrate that a transient R-C network

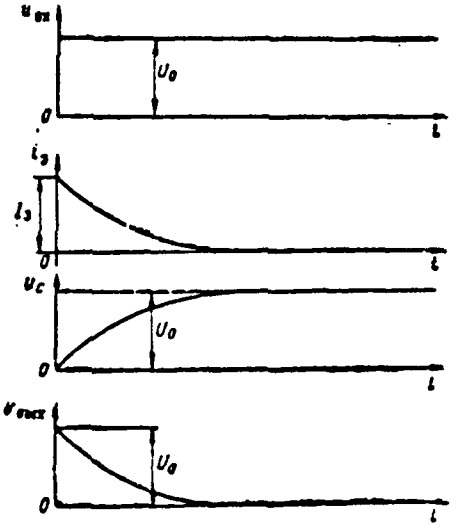


Figure X.8. Constant Voltage Action on an R-C Network.

does not pass constant voltage (following complete capacitor charging $u_{вых} = 0$). Thus, when pulse voltage is active, its d-c component will act upon the network. Consequently, when pulse voltage is transmitted across a transient R-C network, losses will occur in its d-c component.

EXERCISE II.14

a) These curves are depicted in Figure X.9. A change in input voltage initial level does not impact upon output voltage since this level acts like constant

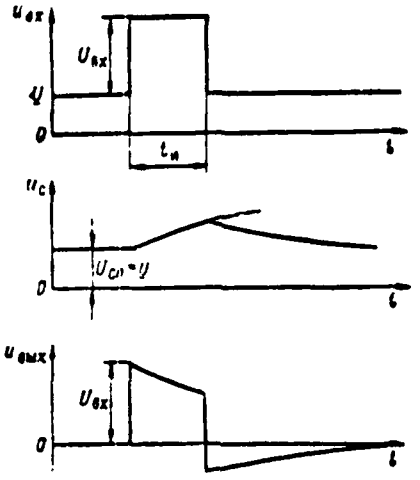


Figure X.9. Passage Across R-C Network of Single Pulse With $U>0$.

voltage which does not pass to network output. Capacitor C voltage magnitude changes only by magnitude $U_{вх}$.

b) Output voltage shape under the given conditions is depicted in Figure X.10 and corresponds to ratio (II.50). Since $\tau_3 \gg t_и$, the reduction in output pulse tilt is slight but, where $R_р \gg R_и$, the capacitor will discharge very slowly after the input pulse ceases, resulting in the fact that negative residual voltage will be active at network output for a long time.

EXERCISE II.15

a) The output voltage of both a linear and a nonlinear transient R-C network remains unchanged, given any changes in initial level, i. e., of the input voltage d-c component. This is because d-c component $U_{вх=}$, regardless of its magnitude

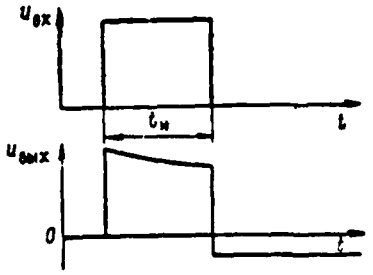


Figure X.10. Passage Across Transient R-C Network of Single Pulse Where $R_з \ll R_р$, $\tau_з \gg t_и$.

and sign, is always balanced in the steady-state mode by the voltage in the /455 network blocking capacitor.

b) Since $\underline{U}_{вых} = -U_c$, in any case it is possible to blank a tube with respect to dynamic bias only given positive input pulse polarity. Here, in accordance with (II.54), it is necessary when a linear transient network is used for $\frac{U_{вх}}{Q} = -\underline{U}_{вых} > |E_{go}|$. In accordance with (II.55), it is necessary when a nonlinear network is used that $U_{вх}\frac{1}{\frac{R_з}{R_р}\frac{t_п}{t_и}+1} = -\underline{U}_{вых} > |E_{go}|$. Since $t_п \gg t_и$, then the minimum input pulse amplitude required to satisfy this condition will be obtained when $R_з \ll R_р$. However, in any event, inequality $U_{вх} > |E_{go}|$ must be satisfied.

EXERCISE II.16

These voltage curves are depicted in Figure X.11. The triode is unblanked prior to the beginning of input pulse action in the circuit with a loop connected to the plate network and its plate current also flows completely across inductance L in the direction from $+E_a$. Since coil resistance is slight, there essentially is no voltage drop across the loop and $u_{вых} \approx E_a$. When pulse $u_{вх}$ arrives, its porch blanks the triode and loop shock excitation occurs. Since current i_L initially retains its direction, it charges capacitor C, passing across it "from below upwards" and increasing the potential of its "lower" plate. Therefore, the first half-cycle of output voltage oscillations is positive. In accordance with the condition, while the pulse is active oscillations are damped completely, until cessation of pulse $u_{вых} = E_a$ (triode blanked). The pulse $u_{вх}$ droop again unblanks the

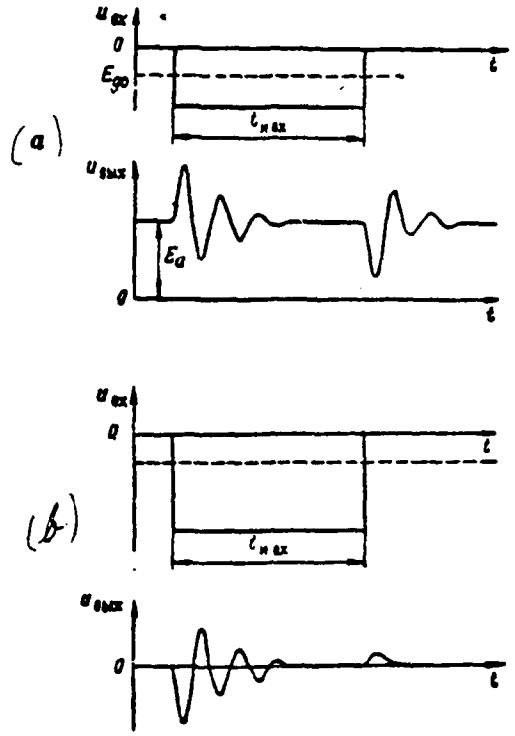


Figure 4.11. Voltage Curves in Shock Excitation Circuits: (a) -- With loop connected to the plate network; (b) -- With loop connected to the cathode network.

triode and excites the loop with a positive plate current change. Since current in the inductance may not rise instantaneously, plate current initially passes completely across capacitor C in the direction "from above downwards." Therefore, the first half-cycle of output voltage oscillations is negative (plate potential drops when current i_a rises). Arising oscillations are damped somewhat more rapidly due to the slight shunting of the loop by high triode internal resistance. Thus, output voltage will retain the d-c component equalling E_a, while the polarity of its first half-cycle is opposite in polarity to the input voltage change. We also will note that the maximum $u_{вых}$ value significantly may exceed level $+E_a$.

Prior to the beginning of pulse action, current i_a completely passes across the inductance in the direction from cathode to "ground" in the circuit with loop

connected to the cathode network. Here, $u_{вых} = 0$. The triode is blanked when pulse $u_{вх}$ porch is active. Current i_L initially retains its direction and charges capacitor C, decreasing the potential of its "upper" plate. Therefore, the first half-cycle of output voltage oscillations will be negative. The capacitor immediately begins to charge with plate current when the input pulse droop unblanks the triode and the output voltage "bump" $u_{вых} = u_c$ will be positive. No oscillations will arise here because of powerful loop shunting by slight cathode network output resistance.

EXERCISE II.17

Current steps in a network containing an inductance physically are impossible (see Attachment 2). However, current steps in each of the windings of an IT [pulse transformer] with slight leakage inductances are possible if only the difference in these steps, computed for one of the windings and, in accordance with (II.65), equalling the magnetization current i_M change, equals zero. Actually, since the magnetization current $W_L = L_м \frac{i_м^2}{2}$ itself determines overall IT magnetic field energy where $L_{р1} = L_{р2} = 0$, then only steps of this current are impracticable. Steps of currents i_1 and i_2 are possible, but must occur simultaneously and be coupled in such a way that if a current i_1 change accomplishes additional IT core magnetization, then a current i_2 change correspondingly must demagnetize it (or vice versa).

EXERCISE III.1

a) We will assume that grid voltage $u_g = 0$. Here, plate current I_a for a given U_a value passes across the tube (for example, see points $б, б'$ in Figure III.3). There are two ways to reduce plate current to zero, i. e., to change it by magnitude $\Delta I_a = I_a - 0 = I_a$: either by decreasing plate voltage to zero, i. e., by changing it by magnitude $\Delta U_a = U_a - 0 = U_a$, or by reducing grid voltage to the triode blanking level, i. e., changing it by magnitude $\Delta U_g = 0 - E_{go} = -E_{go}$. Therefore, in accordance with triode gain determination (III.15), we will get

$$\mu = \frac{\Delta U_a}{\Delta U_g} = -\frac{U_a}{E_{go}} .$$

b) Triode internal resistance to alternating current at points a, b, and

c (in Figure III.3b) is approximately identical since plate transconductance /457 at these points is virtually identical and equals

$R_i = \frac{\Delta u_a}{\Delta i_a} = \operatorname{ctg} \alpha = \frac{\delta \theta}{2\theta} = \frac{75 \cdot 10^{-3}}{6 \cdot 10^{-3}}$ = 12.5 kilohms.

Triode interral resistance to direct current $R_{i0} = \frac{U_a}{I_a}$ equals

$a - R_{i0} = \frac{125 \cdot 10^{-3}}{14.4 \cdot 10^{-3}} \approx 8.7$ kilohms $< R_i$ for point a; $\delta - R_{i0} = \frac{125 \cdot 10^{-3}}{8 \cdot 10^{-3}}$ = 15.6 kilohms $> R_i$ for point b; $\vartheta - R_{i0} = \frac{125 \cdot 10^{-3}}{2.4 \cdot 10^{-3}}$ = 52 kilohm $\gg R_i$ for point c.

Thus, when grid voltage U_g changes from +4 to -4 V, $R_i \approx$ const, while value R_{io} rises approximately by a factor of 6.

c) The greater (all other conditions being equal) the triode plate voltage, i. e., plate accelerating field, the more electrons that will pass through grid to plate and, consequently, the fewer of them that will be "intercepted" by the grid, i. e., participate in formation of grid current i_g. Therefore, the greater the voltage U_a, the "lower" the grid characteristic will pass.

EXERCISE III.2

a) Screen grid current i_{g2} in a pentode may equal zero only in the event the pentode is blanked with respect to cathode current by negative bias in the control grid ($u_{g1} < E_{go1}$). If $u_{g1} > E_{go1}$, current i_{g2} must exist since $U_{g2} > 0$ and the screen grid always "intercepts" some of the electrons passing across grid g_1. The ratio of voltages U_{g3} and U_a only influences the magnitude of this current.

b) If voltage u_{g3} is supplied to suppressor grid when $U_a > 0$, then the accelerating action of the field between plate and this grid increases; therefore, it is impossible for secondary electrons discharged from plate to hit grid g_3 and, consequently, there is no dynatron effect.

c) The appropriate cathode current change $i_k = i_a + i_{g2}$ explains the relative position of current i_a and i_{g2} characteristics in Figure III.6 for various U_{g1} values ($U'_{g1} < 0$ and $U''_{g1} = 0$). The speed of electrons flying off grid g_2 increases with a voltage U_{g1} increase and a more powerful braking action on the part of

grid g_3 is required for their full return to this grid. Therefore, blanking voltage E_{go3} rises in magnitude: $E''_{go3} < E'_{go3}$ when $U''_{g1} > U'_{g1}$.

EXERCISE III.3

a) A positive plate current pulse arises when a positive pulse is active in the Figure III.7 and III.9 circuits. Here, voltage $u_a = E_a - i_a R_a$ will decrease, while voltage $u_k = i_a R_k$ will rise. Consequently, a negative-polarity pulse will be obtained from the plate outputs of these circuits, while a positive-polarity pulse will be obtained from the cathode outputs.

A pulse of increased amplitude may be obtained in the Figure III.7 circuit from the plate output if, based upon (III.28), $R_a > \frac{R_i + (1+\mu)R_k}{\mu - 1}$, while a pulse of decreased amplitude always will be obtained from the cathode output, in accordance with (III.32) or (III.34).

Based on (III.36) and (III.37), a pulse of increased amplitude may be obtained in the Figure III.9 circuit from the plate output (where $R_a > \frac{R_i + R_k}{\mu - 1}$) and from the cathode output (where $R_k > \frac{R_i + R_a}{\mu - 1}$).

Cathode potential will rise in the grounded-grid circuit (Figure III.10) when a positive pulse is active and, since voltage $u_{gk} = -u_{ak}$, plate current /458 will decrease. Here, plate voltage will rise, i. e., a pulse also of positive polarity arises at output. The amplitude of this pulse will be greater than at input if $R_a > \frac{R_i}{\mu}$ in accordance with (III.39).

b) There is no negative feedback in the Figure III.9 circuit ($u_{gk-} = u_{ak-}$) and resistance R_k only decreases the plate current value. Therefore, $I_{a-} = \frac{\mu u_{gk}}{R_i + R_i + R_k} = \frac{\mu u_{ak}}{R_a + R_i + R_k}$ and, consequently,

$$K_a = \frac{u_{a-}}{u_{ak-}} = -\frac{I_{a-} R_a}{u_{ak-}} = -\frac{\mu R_a}{R_a + R_i + R_k};$$

$$K_k = \frac{u_{k-}}{u_{ak-}} = \frac{I_{a-} R_k}{u_{ak-}} = \frac{\mu R_k}{R_a + R_i + R_k}.$$

EXERCISE III.4

a) These graphs are depicted in Figure X.12. The u_g values used extend beyond the boundaries of the characteristic A'A" linear sector when input pulses

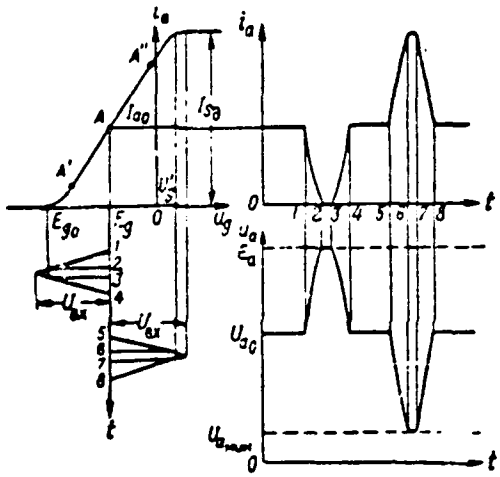


Figure X.12. For Explanation of Plate Grid Amplifier Operation.

with an amplitude increased by a factor of 2 relative to the Figure III.12 amplitude are active. As a result, nonlinear distortions of the shape of current i_a and voltage u_a pulses arise. Since $U_{m} > |E_{g_1} - E_{g_0}|$, then the tube turns out to be blanked when a negative pulse porch is active in the $u_g \ll E_{go}$ region, i. e., in the interval between moments 2 and 3. In this interval, $i_a = 0$ and, in accordance with (III.21), plate voltage attains maximum possible value $U_{a\,max} = E_a$. Tube dynamic saturation occurs when a positive pulse is active in the region $u_g \geqslant U_g'$, i. e., in the interval between moments t_6 and t_7. In this interval, current i_a attains maximum value /459 $I_{a\,max} = I_{s_a}$, while plate voltage is minimal and, in accordance with (III.21), equals $U_{a\,min} = E_a - I_{s_a} R_a$. Thus, there is negative pulse clipping due to lower plate current cutoff (tube blanking) and positive pulse clipping due to upper plate current cutoff (tube dynamic saturation) when input pulse amplitude increases.

b) Bias voltage E_g should be increased, the operating point having been shifted to point A', when only positive pulses are amplified. In this case, the

amplitude of the pulse during which no nonlinear distortions have yet occurred will be maximum and equal the projection of the entire sector A'A" to the X-axis. Bias voltage should be decreased in magnitude (operating point shift to point A") for the identical circumstances when only positive polarity pulses are amplified.

c) In order to obtain only the a-c plate voltage component at stage output, this voltage must be picked off across the transient R-C network.

EXERCISE III.5

a) For any current i_a value, $u_a = E_a$ when $R_a = 0$. Therefore, a vertical line passing through point $u_a = E_a$ of the X-axis depicts the dynamic plate

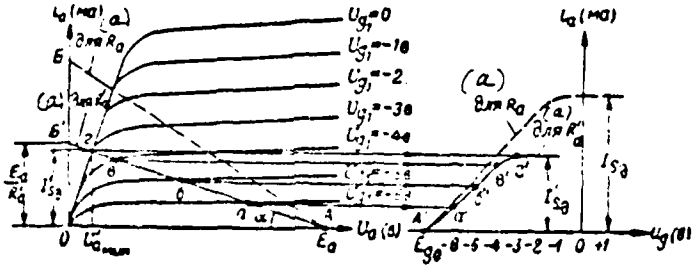


Figure X.13. Pentode Dynamic Characteristic ($R_a' = 2R_a$).

characteristic. (This also follows from the fact that $\alpha = \operatorname{arctg} \frac{1}{R_a} = \frac{\pi}{2}$ when $R_a = 0$). The dynamic transfer characteristic coincides with the static transfer characteristic for value $u_a = E_a$.

b. Pentode dynamic characteristics for $R_a' = 2R_a$ are plotted in Figure X.13 (the dotted line depicts characteristics corresponding to the previous R_a value in Figure I.I.13c, d). The load line is flatter (segment $OB' = \frac{E_a}{R_a'}$ is less by a factor of 2 than segment $OB = \frac{E_a}{R_a}$, angle $\alpha' = \operatorname{arctg} \frac{1}{R_a'}$ commensurately is decreased). Therefore, maximum current I_{s_a}' and minimum voltage $U_{a\,min}'$ are decreased and pentode dynamic saturation begins at less voltage $U_{g1}' = -3$ V (point A'). This is explained physically by the fact that, given a resistance R_a increase, the

voltage drop across it rises for the identical current i_g values, as a result of which plate voltage decreases and, when there is an increase in control /460 grid voltage, redistribution of cathode current between plate and screen grid begins, given a lesser U_{g1} value.

The dynamic transfer characteristic begins from the same point A' (resistance R_a magnitude does not affect blanking voltage), while its transconductance decreases, which also follows from ratio (III.46).

EXERCISE III.6

a) Presenting expression (III.49) considering (III.19) in the form $K = -\frac{SR_a}{1 + R_a R_i}$ and considering that, for a pentode, the values of transconductance S and internal resistance to alternating current R are greater than for a triode, we will see that the greatest gain will result when a pentode is used.

The influence of the total stray capacitance of the circuit $C_a = C_{a1} + C_{a\,mn}$, where capacitances C_{a1} and $C_{a\,mn}$ are determined in accordance with (III.56), cause the high-frequency pulse distortions. Capacitances C_{ag} and C_{a1} are significantly less for a pentode than for a triode due to presence of screen and suppressor grids. Therefore, there are fewer high-frequency distortions when a pentode is used. The influence of the transient R-C network causes low-frequency distortions and essentially they do not depend on tube parameters.

b) In accordance with (III.49), amplification must become maximum ($K = -\mu$) where $R_a = \infty$. Realistically, in this case the tube plate current network will be blanked, no plate voltage will be supplied to the tube ($U_a = 0$), and, consequently, $K = 0$.

In accordance with (III.21), when $R_a = 0$, plate voltage will rise to supply source voltage $u_a = E_a = \text{const}$ and, consequently, as was the case in the previous example, we will get $K = 0$. The plate voltage rise in this event will lead also to an increase in the plate current d-c component, i. e., of power dissipated in the plate. As a result, the tube may malfunction due to electrode overheating.

c) The output voltage of an amplifying stage with a plate load changes opposite

in phase with input voltage. Consequently, when negative pulses are supplied to the three-stage amplifier input, they will be inverted three times and positive-polarity pulses will be obtained at amplifier output.

EXERCISE III.7

a) Breakdown capacitor $C_к$ in the self-bias cell briefly shunts resistance $R_к$. Since there will be no voltage drop across this resistance, negative bias in the control grid will disappear ($U_g = -U_к = 0$) As a result, the plate current d-c component will rise and the plate voltage d-c component will decrease. Here, the stage will convert to the dynamic saturation mode (for a pentode) or will approximate it (for a triode). Displacement of the operating point to the region of the upper "bend" in the dynamic transfer characteristic will lead to a decrease in gain and onset of nonlinear distortions.

In addition, control grid current i_{g1} will arise when $u_{g1} > 0$, which will be accompanied by a rise in power consumed in the tube input network and additional nonlinear distortions due to the voltage drop across the output resistance of the input signal source. The rise in the plate current d-c component may lead to a tube malfunction due to overheating of its electrodes.

b) A tube may be blanked ($E_g < E_{go}$) only with the aid of self- or dynamic bias (in the latter case, only upon arrival of positive input pulses of sufficiently great amplitude). Tube self-blanking with the aid of self-bias physically is impossible since all currents in a tube would cease when it blanks and, therefore, $U_к = -U_к = -(I_a + I_{g1})R_к = 0$, i. e., the reason for its blanking would disappear.

c) Given a slight relative reduction in capacitor $C_ф$ voltage, its /461 discharge during pulse time $t_и$ must occur by an essentially linear law. Therefore, using the first ratio (XI.16), where $t = t_и$, $X(0) = E_ф$, we will get $\Delta U = E_ф -$

$U_{ф\,min} = E_ф - E_ф\left(1 - \frac{t_и}{\tau_{разр}}\right) = E_ф \frac{t_и}{\tau_{разр}}$, hence $\tau_{разр} = C_ф(R_i + R_a) = \frac{E_ф t_и}{\Delta U}$ or $C_ф = \frac{E_ф t_и}{\Delta U (R_i + R_a)}$.

Consequently, $C_ф > \frac{10 \cdot 10^{-6}}{0{,}01 \cdot 5 \cdot 10^3}$ = 2,000 pF.

d) As usual, considering that capacitor $C_ф$ discharge with current i_a while

the pulse is active occurs by a linear law, we may write $i_c = C\frac{\Delta U_C}{\Delta t}$, i. e.,

$i_c = C_\phi \frac{\Delta U_a}{t_u}$, hence $C_\phi = i_a \frac{t_u}{\Delta U_a} = \frac{i_a t_u}{E_a - 0.5} = \frac{0.75\cdot 10^{-3}\cdot 10^{6}}{150\cdot 0.05} = 0.1$ uF

During resting time, capacitor C_ϕ must succeed in charging to voltage E_a. Assuming on the basis of the second condition (III.60) $\tau_{зар} = C_\phi R_\phi = \frac{T_u}{4}$ ($T_u \approx t_u$), we will get $R_\phi = \frac{T_u}{4C_\phi} = \frac{2000\cdot 10^{-6}\cdot 10^{6}}{4\cdot 0.1\cdot 10^{-6}} = 5$ kilohms.

EXERCISE III.8

a) Tube plate current may flow across resistance R_a only in one direction, from cathode to circuit chassis. Therefore, voltage $u_a \geq 0$ for an unblanked tube and $u_a = 0$ for a blanked tube, but it may never be negative.

b) Tube self-blanking with voltage drop U_{a0} created by its plate quiescent current physically is impossible (see Exercise III.7). Therefore, the tube may be brought as close as desired to the cut-off area by increasing resistance R_a, but always $U_{a0} = -U_{k0} > E_{c0}$.

c) Capacitor R_a shunting of resistance C_a will not alter the stage operating mode with respect to d-c: the d-c component of current i_a as usual will pass across resistance R_a, creating voltage drop $U_{a0} = -U_{k0}$ in it. However, when input voltage is active, the current a-c component, just as in the self-bias cell, will close across capacitor C_a. Therefore, no output signal arises: $u_{a\sim} = u_{вых\sim} = 0$. There will be no negative a-c component feedback: $u_{gc\sim} = u_{вх\sim}$.

EXERCISE III.9

a) In accordance with Figure III.23, the representative point for a cathode follower will not leave the boundaries of the essentially linear sector of dynamic characteristic A_2A_3 if input voltage changes in the range $\Delta U_{вх.д} = U_{вх\,макс} + |U_{вх\,мин}|$. For a plate-load amplifier $u_{вх\sim} = u_{gc\sim}$ and a significantly lesser range of changes $\Delta U_{вх.д} = \Delta U_{gc} = |U_{gc\,мин}|$ corresponds to the identical sector of the characteristic. Using (III.34), we will get $\frac{\Delta U_{вх.д}}{\Delta U_{вх.п}} = \frac{\Delta U_{вх.д}}{\Delta U_{gc}} = \frac{1}{1-K_{оп}} > 1$. It also follows from

from this that, given an identical range of input voltage changes, the sector of the dynamic characteristic used in a cathode follower will be shorter by a factor of $\frac{1}{1-K_{en}}$ and, consequently, (given proper operating point selection), more linear than in a plate-load amplifier.

b) This plot is shown in Figure X.14, where the Figure III.23 plot for the previous R_a value (α , I_{ao}, $U_{ex\ max}$ and $U_{ex\ min}$) is repeated as a dotted line

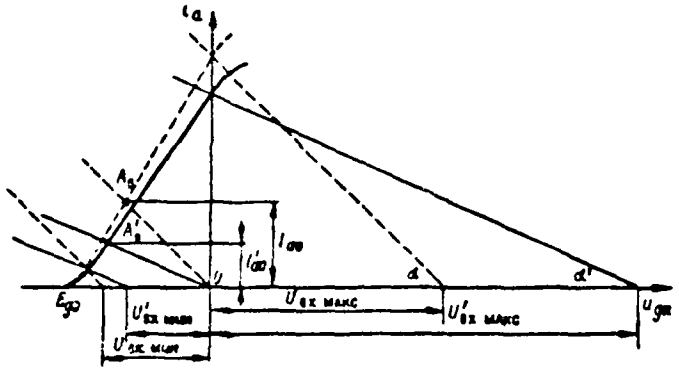


Figure X.14. For Explanation of Cathode Follower Operation When Resistance $R_a (R'_a > R_a)$ Is Increased.

for comparision purposes. Dynamic transfer characteristic transconductance, in accordance with (III.65), decreases somewhat when resistance R_a $(R'_a > R_a)$ is increased (usually $R_a < R_i$), while feedforwards, in accordance with (III.67), are flatter ($\alpha' < \alpha$). Therefore, operating point A_0 will shift "downwards" along the dynamic characteristic, i. e., negative bias U_{g0} will rise with respect to magnitude, while quiescent current I_{a0} will decrease. Value $U_{ex\ max}$ will decrease with respect to magnitude, while value $U_{ex\ min}$ will rise. This makes it possible to transmit across the cathode follower positive pulses of greater amplitude, without entering the region $u_{gk} > 0$. The maximum resistance R_a magnitude is clipped by the approach of the operating point to the region of the lower dynamic characteristic bend.

EXERCISE III.10

a) Having divided the numerator and denominator of expressions (III.68)

and (III.69) by the product R_iR_k, we will get:

$$K_{ck} = \frac{S}{1/R_i + 1/R_k + S}; \quad R_{вых.ск} = \frac{1}{1/R_i + 1/R_k + S}.$$

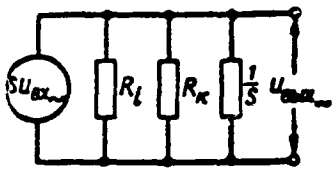


Figure X.15. Equivalent Cathode Follower Circuit With Current Generator.

The equivalent cathode follower circuit depicted in Figure X.15 also corresponds to these expressions.

b) There is no break in curves u_{gk} and u_k at moment t_4 in Figure III.26 for two reasons. First, at interval t_4--t_3 when the tube is blanked, capacitance $C_{вых}$ will strive to discharge across resistance R_k to zero (where $i_a = 0$, $u_k = 0$); after the tube unblanks ($t > t_4$), discharge of this capacitance occurs, even though across lesser resistance $R_{вых.ск}$, but only to voltage $U_{a0} = I_{a0}R_k$. Second, from the moment of tube unblanking, transconductance S rises, while resistance $R_{вых.ск} \approx \frac{1}{S}$ decreases only gradually due to operating point displacement to the linear sector of the characteristic.

EXERCISE III.11 /463

Operation of the Figure III.27a circuit is explained in Figure X.16a. We will get $u_{gk} = E_g + u_{вх\sim} - i_aR_a$ when positive bias E_g is supplied, hence the feedforward equation (III.66) will be written in the form $i_a = \frac{E_g + u_{вх\sim}}{R_a} - \frac{u_{gk}}{R_a}$. Therefore, bias line 0 (straight line for value $u_{вх\sim} = 0$) intersects on the X-axis segment $U_{gk} = E_g$, i. e., is located to the right of the bias line for $E_g = 0$ (dotted line). As a result, operating point A_0 shifts "upwards" along dynamic characteristic D, i. e., quiescent current I_{a0} rises. Values $U_{вх.макс}$ and $U_{вх.мин}$, which are constrained by lines 1 and 2 and which are computed relative to bias E_g, determine the dynamic range. All lines are sloped to the same angle $\alpha = \operatorname{arctg}\frac{1}{R_a}$. The plot for the Figure III.27b circuit is completely analogous. Gain for both circuits equals $K_{ck} = \frac{1}{1 + 1/SR_k}$.

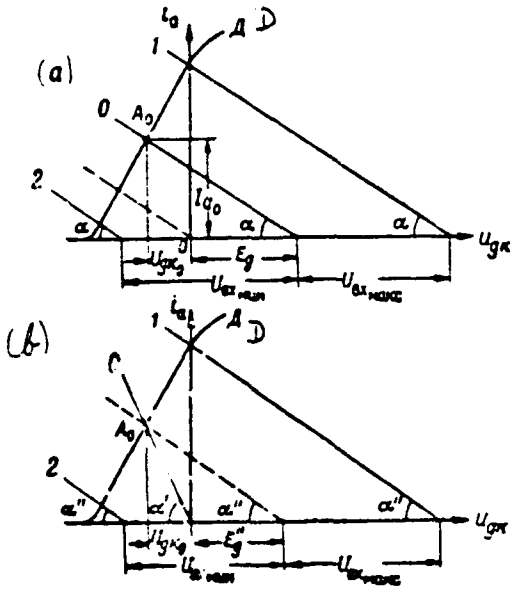


Figure X.16. For Explanation of Cathode Follower Circuit Variants.

Operation of the Figure III.27c circuit is explained in Figure X.16b. Self-bias for this circuit is obtained only at resistance $R_{к1}$. Therefore, bias line 0 passes through the origin of the coordinates and is sloped at angle $\alpha = \arctg \frac{1}{R_{к1}}$. This line also determines operating point A_0 position. The a-c component /464 of the feedback voltage arises only at resistance $R_{к2}$ when input voltage is active. Therefore, stage operation with respect to the a-c component is characterized by feedforwards sloped at angle $\alpha' = \arctg \frac{1}{R_{к1}} < \alpha$. The line indicated by the dots passes through the operating point and is sloped at angle α''. It intersects on the X-axis the segment equalling E_g''. This signifies that the position of the operating point would be the same as if outside bias $E_g'' > 0$ is introduced into the circuit with respect to one of the previous variants in place of self-bias. Values $U_{вх\ макс}$ and $U_{вх\ мин}$ are constrained by lines 1 and 2 and are computed relative to magnitude E_g''. Circuit gain equals

$$K_{ос} = \frac{1}{1 + I_{a0} R_{к2}}$$

The Figure III.27d circuit is plotted in the same manner. But, since feedback voltage is picked off in this circuit from both resistances $R_{к1}$ and $R_{к2}$,

feedforwards are sloped at angle $\alpha = \operatorname{arc\,tg} \frac{1}{R_{a1} + R_{a2}}$ For this reason, stage gain equals

$$K_{ka} = \frac{1}{1 + 1/S(R_{a1} + R_{a2})}.$$

EXERCISE III.12

When equality (III.76a) is satisfied, in accordance with (III.75), stage gains will be equal in magnitude and opposite in sign $K_{a1} = -K_{a2} = K$. Consequently,

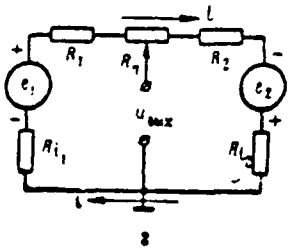


Figure X.17. Difference Circuit Equivalent Circuit.

negative voltage $e_1 = Ku_{вх1}$ arises at the first stage cathode output when negative-polarity input voltages are active, while positive voltage $e_2 = Ku_{вх2}$ arises at second stage plate output. Representing triodes L_1 and L_2 with emf generators e_1 and e_2 with internal resistances R_{i1} and R_{i2}, we will get the equivalent circuit for an a-c component device depicted in Figure X.17. Differing polarities of emf e_1 and e_2 are represented in this circuit by their opposites in phase relative to "ground," i. e., matched connection. Therefore, current i passing across divider R_1, R_3, R_2 will equal

$$i = \frac{e_1 - e_2}{R_1 + R_3 + R_2 + R_{i1} + R_{i2}}.$$

We will assume that the circuit is completely symmetrical, i. e., $R_{i1} = R_{i2}$, $R_1 = R_2$, and the potentiometer R_3 arm is set strictly in the middle position.

Then, examining the loop: generator e_1--resistance R_1--potentiometer arm--

circuit output terminals--resistance R_{il}, in accordance with Kirchhoff's second law we will get

$$e_1 = iR_1 + i\frac{R_\pi}{2} + u_{вых} + iR_{i1}.$$

hence

$$u_{вых} = e_1 - i\left(R_1 + R_{i1} + \frac{R_\pi}{2}\right) = e_1 - \frac{(e_1 + e_2)\left(R_1 + R_{i1} + \frac{R_\pi}{2}\right)}{R_1 + R_\pi + R_2 + R_{i1} + R_{i2}}.$$

or, where /465

$$R_1 = R_{i1},\ R_2 = R_1,\quad u_{вых} = e_1 - \frac{e_1 + e_2}{2} = \frac{e_1 - e_2}{2}.$$

Therefore,

$$u_{вых} = K\frac{U_{вх1} - U_{вх2}}{2}.$$

EXERCISE III.13

The relationship of gain K_u to generator resistance R_1 is explained by the fact that a voltage drop across this resistance is created due to input current, while the voltage drop across transistor input decreases.

EXERCISE III.14

Emitter current is input current in a common-base amplifier. But, base current, comprising a small portion of the emitter current, is input current for a common-emitter amplifier. This current flows across the signal source and transistor input network. Consequently, it is possible to use a source with a greater internal resistance than in a common-base amplifier.

Connection of resistance to an emitter network leads to appearance of negative feedback, resulting in a decrease in input current magnitude, i. e., input resistance rises.

EXERCISE III.15

It is evident from Figure III.44 that transistor T_1 collector current equals $-i_{ex}\alpha$, while base current equals $i_{b1}=i_{ex}(1-\alpha_1)$. But, transistor T_1 base current is input current for transistor T_2 and, therefore, its collector current

$$i_{k2}=i_{c1}\alpha_2=i_{ex}(1-\alpha_1)\alpha_2.$$

Output current equals the sum of the collector currents:

$$i_{вых}=\alpha_1+i_{k2}=i_{ex}(\alpha_1+\alpha_2-\alpha_1\alpha_2)$$

Hence, current gain

$$\alpha_2=\frac{i_{вых}}{i_{ex}}=\alpha_1+\alpha_2-\alpha_1\alpha_2$$

EXERCISE III.16

Current gain magnitude $\alpha_2 = 0.99996$ is determined from formula (III.129). Further, we determine input resistance magnitude from formula (III.125)

$$R_{ex.\,вх}=\frac{R_н}{1-\alpha}=2.5 \text{ megohms.}$$

EXERCISE III.17

Transistors P15 and P103 meet the stipulated conditions.

EXERCISE III.18

1. The load line will be plotted in the collector characteristic family:

$$u_к=0,\ i_к=\frac{E_к}{R_к}=3.0 \text{ ма},\ i_к=0,\ u_к=E_к=12 \text{ В}.$$

2. The operating point position is determined by the intersection of the load line and static collector characteristic, corresponding to bias current

$$I_{б\,см}=\frac{E_б}{R_б}=\text{[illegible]}.$$

Initial collector voltage $U_{к0} = -5$ V corresponds to the operating point /466 where temperature is 20° C and is $U_{к0} = -4.3$ V at an increased temperature.

3. Intersection of the load line with the criticality line determines minimal collector voltage $U_{к.мин}$: $U_{к.мин} = -1.2$ V.

4. Maximum positive pulse amplitude at output where t = 20° C equals

$$U_м = U_{к0} - U_{к.мин} \approx 3.8 \text{ V}.$$

Pulse amplitude where t = 30° C equals

$$U'_м = U'_{к0} - U_{к.мин} \approx 3.1 \text{ V}.$$

5. The change in amplitude with a change in temperature comprises

$$\Delta U_м = U_м - U'_м = 0.7 \text{ V}.$$

EXERCISE IV.1

These voltage curves are depicted in Figure X.18.

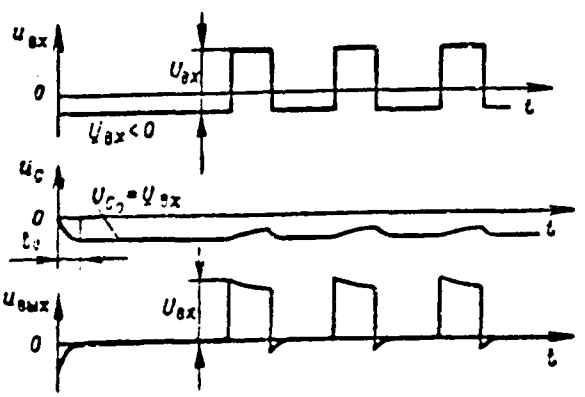


Figure X.18. Zero Lower Clamp Operation Given Negative Input Voltage Initial Level.

EXERCISE IV.2

These curves are depicted in Figure X.19.

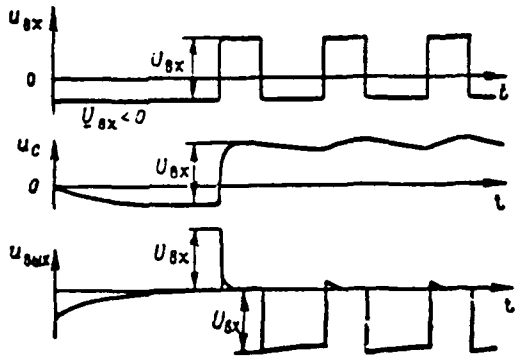


Figure X.19. Zero Upper Clamp Operation Given Action of Positive Pulses With $U_{вх}<0$.

EXERCISE IV.3

a) These curves are depicted in Figure X.20.

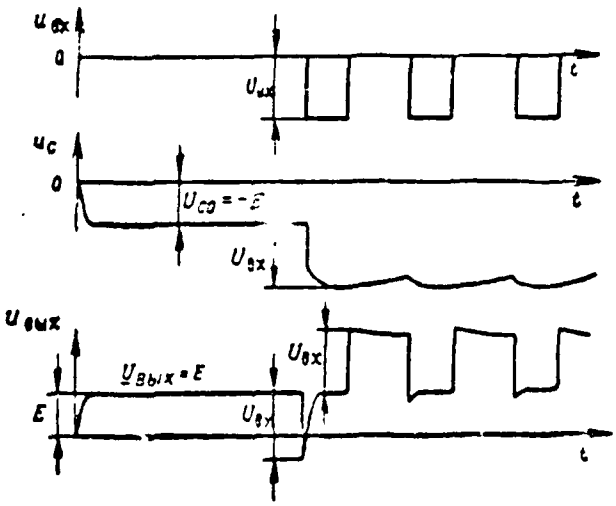


Figure X.20. Lower Positive Clamp Operation Given Action of Negative Pulses With $U_{вх}=0$.

b) A negative lower clamp is depicted in Figure IV.11a, a positive upper clamp in Figure IV.11b, and a negative upper clamp in Figure IV.11c.

EXERCISE IV.4

This circuit is depicted in Figure X.21. Residual voltage U_{C_0} applied with a "minus" to CRT control electrode arises in capacitor C_1 when positive intensifier

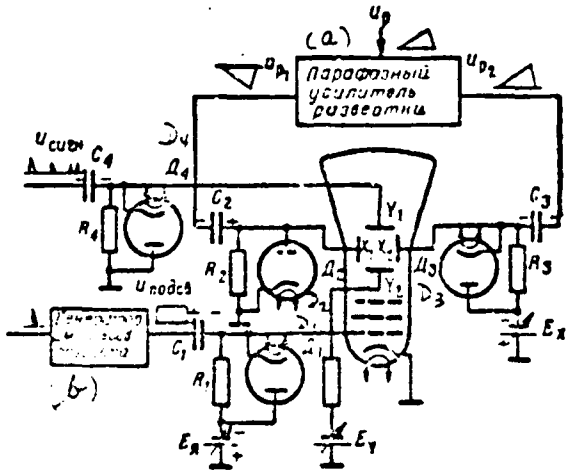


Figure X.21. For Exercise IV.4. (a) -- Paraphase sweep amplifier; (b) -- Intensifier pulse generator.

pulses flow across transient network C_1R_1. As a result, sweep brightness will decrease. A zero lower clamp, diode D_1 (along with voltage source E_1, which supplies sweep brightness, diode D_1 forms a negative lower clamp), should be connected in order to insure complete capacitor C_1 discharge during resting times between intensifier pulses and thereby to stabilize sweep brightness. Residual voltage U_{C_2}, applied with a "plus" to left plate C_2, arises in capacitor C_2 when negative sawtooth pulses of voltage u_{p_1} flow across transient network C_2R_2. Residual voltage U_{C_3}, applied with a "minus" to right plate C_3, arises in capacitor C_3 when positive sawtooth pulses of voltage u_{p_2} flow across transient network C_3R_3. As a result, the sweep line on the CRT screen will [illegible] to the left. A zero upper clamp, diode D_2, should be connected to network C_2R_2 output, while a zero lower clamp, diode D_3 (along with bias source E_3 supplying sweep origin from the left edge

of the screen, diode D_3 forms a negative lower clamp), should be connected to the network C_3R_3 output to stabilize the sweep position with respect to the horizontal.

Unstable residual voltage U_{Co4} applied with a "minus" to upper plate Y_1 arises in capacitor C_4 when positive target video pulses flow across transient network C_4R_4. As a result, the sweep line will shift downwards from the CRT horizontal diameter. A zero lower clamp, diode D_4, should be added to stabilize the sweep position with respect to the vertical.

EXERCISE V.1

a) It follows from examination of the characteristics depicted in Figure V.3 that displacement of the characteristic along the X-axis corresponds to a change in clipping thresnold , while displacement of the characteristic along the Y-axis corresponds to a change in clipping level U_0.

b) The characteristics and curves of the input and output voltages for the given limiter types are shown in Figure X.22.

EXERCISE V.2

a) In the Figure V.7 limiter circuit, the diode is unblanked when , with (transfer mode); the diode is blanked when , with (limiting mode). Consequently, the circuit sets an upper bound with a zero /469 clipping threshold and level (Figure V.1a).

For the Figure V.7b limiter circuit, the diode is unblanked when , i. e., , here ; the diode is blanked when , here . Consequently, the circuit sets an upper bound with negative and equal clipping threshold and level (Figure V.1d).

For the Figure V.7c limiter circuit, the diode is unblanked when , i. e., , here ; the diode is blanked when , here . Consequently, the circuit sets an upper bound with positive clipping threshold and zero level (Figure V.1c).

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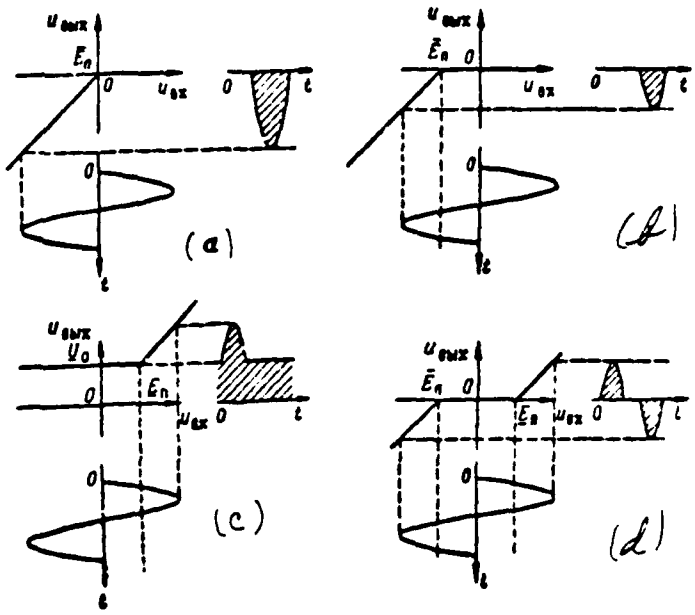


Figure X.22. Limiter Input (Sinusoidal) and Output Voltage Characteristics and Curves: (a) -- Upper where $E_п - U_0 = 0$; (b) -- Upper where $E_п < 0$, $U_0 = 0$; (c) -- Lower where $E_п - U_0 > 0$; (d) -- "External" clipper-limiter where $E_п < 0$, $E_п > 0$, $U_0 - U_0 = 0$.

For the Figure V.7d limiter circuit, the diode is unblanked when $u_{вх} - E < 0$, i. e., $u_{вх} < E$, here $u_{вых} = u_{вх}$; the diode is blanked when $u_{вх} - E > 0$, here $u_{вых} = E$. Consequently, the circuit sets an upper bound with negative and equal clipping threshold and level $E_п = U_0 = E$ (Figure V.1b).

b) The curves depicted in Figure V.8 correspond to an upper bound with zero clipping threshold and negative clipping level. We will get the corresponding limiter circuit for the following reasons. A lower bound with threshold $E_п = 0$ requires that the diode be connected so that it would conduct when $u_{вх} > 0$ and be blanked when $u_{вх} < 0$. But, this requires that no external bias must act upon the /470 diode. On the other hand, negative (relative to "ground") bias source $E_1 = U_0$ must be connected to the limiter output network to obtain $U_0 < 0$. Equal bias of opposite polarity $E_2 = -E_1$ must compensate for the action of this source so that it does not disrupt the clipping threshold. Bias source E_2 must not be part

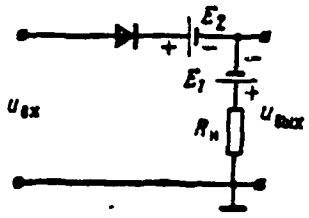


Figure X.23. Series Diode Lower Limiter Circuit ($\underline{E}_0=0$; $\underline{U}_0=-E_1$).

of the limiter output network so as not to influence the clipping level. A limiter circuit with these properties is depicted in Figure X.23.

EXERCISE V.3

Diode D_1 in the Figure V.9b limiter circuit is unblanked when $u_{вх}>E_1$. Consequently, the circuit branch with diode D_1 and bias source E_1 sets a lower bound with positive threshold $\underline{E}_0=E_1$. Diode D_2 is unblanked when $u_{вх}<-E_2$. Consequently, the circuit branch with diode D_2 and bias source E_2 sets an upper bound with negative threshold $\bar{E}_0=-E_2$. Since $\bar{E}_0<\underline{E}_0$, then, "external" clipping will occur as a result. As long as input voltage varies within the range $\underline{E}_0=E>u_{вх}>\bar{E}_0=-E_2$, both diodes will be blanked and, since bias sources are not included in the limiter output network, $u_{вых}=0$. Consequently, the overall clipping level equals $\underline{U}_0=\bar{U}_0=0$. The action of this type limiter corresponds to Figure V.1o.

EXERCISE V.4

For the Figure V.12a limiter circuit, the diode is blanked (transfer mode) when $u_{вх}<E$. Here $u_{вых}=u_{вх}-E$ — output voltage decreases by magnitude E. A bound will be set when the diode unblanks, i. e., when $u_{вх}>E$. Here $u'_{вых}=0$ (the bias source will not be included in the output network). Consequently, the circuit will set an upper bound with positive clipping threshold $\bar{E}_0=E$ and zero clipping level $\bar{U}_0=0$ (Figure V.1c).

For the Figure V.12b limiter circuit, the diode is blanked (transfer mode)

when $u_{вх} > E$. Here $u_{вых} = u_{вх}$ (the bias source is cut out from blanked diode output and does not impact upon magnitude $u_{вых}$). A bound will be set when the diode unblanks, i. e., when $u_{вх} < E$. Here $u'_{вых} = E$. Consequently, the circuit sets a "lower" bound with a positive clipping threshold and level $E_з = U_з = E$ (Figure V.1g).

For the Figure V.12c circuit, both diodes will be blanked (transfer mode) as long as $E_1 > u_{вх} > E_2$. Here $u_{вых} = u_{вх}$. When $u_{вх} > E_1$, diode D_1 unblanks and $u_{вых} = E_1 > 0$ (source E_2 is cut out by blanked diode D_2). When $u_{вх} < E_1$, diode D_2 unblanks and $u'_{вых} = E_2 < 0$ (source E_1 is cut out by blanked diode D_1). Thus, the circuit sets an "external" bilateral bound: "upper" with positive threshold and level $E_в = U_в = E_1 > 0$; "lower" with negative threshold and level $E_н = U_н = E_1 < 0$ (Figure V.1k).

EXERCISE V.5 /471

a) These limiter and clamp circuits are depicted in Figure X.24. In spite of the seeming similarity of these circuits, they have the following major differences. First, the limiter circuit must contain limiting resistance R_0 /471

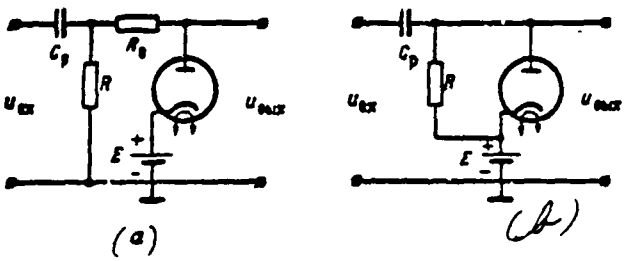


Figure X.24. Parallel Upper Diode Limiter Circuit With Positive Clipping Threshold and Level (a) and Positive Upper Clamp Circuit (b) When Connected to Transient R-C Networks.

R_0 ($R_0 > R_д$), which are absent in the clamp circuit. Second, bias E in the limiter circuit is applied to the diode and thereby changes value $u_{вх}$ at which the diode unblanks, i. e., determines clipping threshold $E_з = E$; bias E in the clamp circuit does not impact upon diode operation (the source E "minus" is separated from the capacitor C, diode plate) and supplies only clamped level $U_{вых} = E$.

b) A comparison of series and parallel diode limiter properties is presented in Table 3.

Table 3

Comparison Criteria	Diode Limiter Type	
	Series	Parallel
Circuit Characteristic Features	Diode connected in series with the load	Diode connected parallel with the load; limiting resistance R_0 present
When Will Limiting Occur	When diode is blanked	When diode is unblanked
Limiting Quality	Strict	Not strict
Basic Ratios in the Circuit and What They Provide	$R_н \gg R_д$ — improved transfer mode (K increase)	$R_0 \gg R_д$ — improved limiting mode (K' decrease) $R_н \gg R_0$ — improved transfer mode (K increase)

c) Diode limiter circuits considering input voltage generator internal resistances $R_г$ and bias source $R_б$ are depicted in Figure X.25.

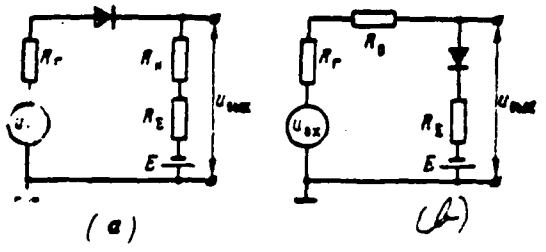


Figure X.25. For Consideration of Generator Internal Resistances $R_г$ and Bias Source $R_б$ Impact Upon Diode Limiter Operation.

For the series limiter (Figure X.25a), resistance $R_г$ reduces voltage $u_{вых}$ and the differential transfer constant in the transfer mode. Actually, considering $R_г$, expression (V.1) must be written in the form $u_{вых} = iR_н = \frac{u_{вх}}{R_г - R_д + R_н} R_н$ and condition (V.2), insuring that $K \approx 1$, in the form $R_н \gg R_д + R_г$. Resistance $R_б$ may be computed as part of load resistance $R_н$ and only facilitates satisfaction of condition (V.2).

For the parallel limiter (Figure X.25b), resistance R_r may be considered in limiting resistance R_0 and only facilitates satisfaction of condition (V.8) $R_0 \gg R_\partial$, which increases limiting strictness. Resistance R_ε in the limiting mode is added to unblanked diode resistance R_∂ and thereby limiting strictness deteriorates.

Consequently, it is more advantageous to connect series diode limiters to a circuit with slight output resistance R_r. Here, it is possible to include in them bias sources with great internal resistance R_ε. Parallel diode limiters may be connected to circuits with great resistance R_r, and resistance R_ε for them must be as small as possible.

EXERCISE V.6

It follows from examination of the Figure V.14 curves that distortions in pulse shape caused by the influence of stray capacitances will be absent at a series diode limiter output, given condition $\Delta U_{вых} = U_{вх} \frac{C_{ab}}{C_{ab} + C_0} = U$. However, such an ideal result may be obtained only where $R_r = 0$ (see Chapter II, § 4).

EXERCISE V.7

Diodes D_1 are limiting and diodes D_2 are compensating in all Figure V.17 circuits. Since dual diodes are used in the circuits, the characteristics of the limiting and compensating diodes in each circuit are identical and shift in an essentially identical manner during changes in filament voltage or during tube replacement or aging ($E_{д1} = E_{д2}$). An upper series diode limiter with positive clipping threshold and level $E_0 = U_0 = E > 0$ is depicted in Figure V.17a. As long as diode D_1 is blanked ($u_{вх} > E$), diode D_2 initial current creates across resistance R_0 voltage drop $U_{вх} = I_{вх} R_0 = E_{д2}$ applied with a "minus" to diode D_1 plate, i. e., compensating action of "bias" $E_{д1}$ (diode D_1 characteristic shift).

A lower series diode limiter with positive clipping threshold and level /473 $E_0 = U_0 = E > 0$ is depicted in Figure V.17b. Bias source E supplies value $E_0 = U_0$ across diode D_2. This diode's current ($u_{вх} < E$), given blanked diode D_1, creates

across resistance $R_н^*$ voltage drop $U_в = I_2 R_н^* = E + E_{д02}$, applied with a "minus" to diode D_1 plate. Voltage $E_{д02}$ is created due to diode D_2 initial current I_{o2} and compensates for the action of "bias" $E_{д01}$.

An upper series diode limiter with positive clipping threshold and level $E_в = U_{огр} > 0$ is depicted in Figure V.17c. The voltage drop across diode D_2 and resistance R_2 arising due to diode D_2 current flow determines value E and it equals

$$E = \left(E_в - E_д \frac{R_3}{R_1 + R_3}\right) \frac{R_2}{R_2 + R_3} = E_в \frac{R_1 R_2}{(R_1 + R_3)(R_2 + R_3)}^{**}$$

In addition, due to diode D_2 initial current I_{o2}, negative voltage $E_{д02} \frac{R_2}{R_2 + R_3} \approx E_{д02}$ (where $R_2 \gg R_3$), which compensates for the action of "bias" $E_{д01}$.

EXERCISE V.8

An upper parallel diode limiter circuit with positive clipping threshold and level $E_в = U_{огр} = E$ is depicted in Figure V.20a. Voltage $u_{вх}$ at the transient network output in the steady-state mode will have negative initial level $U'_{вх} = -\delta U_C$ due to residual coupling capacitor $C_р$ voltage when Figure V.20b voltage is supplied to the transient R-C network. Dynamic bias magnitude will be determined from (II.50) considering that $R_э = \frac{RR_д}{R + R_д} < R_р = R$.

Circuit output voltage is depicted in Figure X.26a. There is a requirement to insure rapid capacitor $C_р$ discharge during resting times between positive pulses $u_{вх}$, i. e., to decrease constant discharging time (where $R_р \ll R_э$, $\delta U_C \approx 0$) in order to eliminate dynamic bias δU_C. It is necessary to use a zero lower clamp for this purpose. A limiter circuit with such a clamp (diode D_2) is depicted in Figure X.26b, while its output voltage is shown in Figure X.26c. Positive square pulses beginning at the zero level with amplitude $U_{вых} = E$ are obtained when the clamp is connected at limiter output.

EXERCISE V.9 /474

a) For the Figure V.23a circuit, bias E_g is applied with a "minus" to cathode,

*For simplicity, we disregard diode D_2 internal resistance ($R_{д2} \ll R_н$).

**We disregard diode D_2 internal resistance ($R_{д2} \ll R_3 + R_2$).

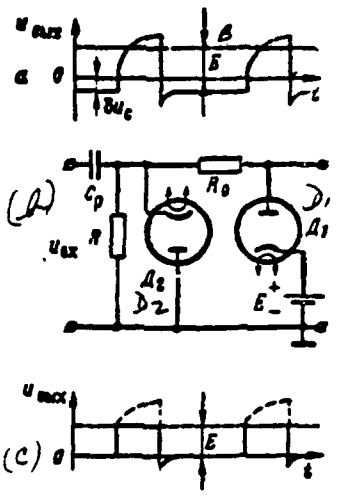


Figure X.26. For Action of a Clamp Connected to Limiter Input.

i. e., promotes the onset of grid current. Therefore, the limiting mode will begin when $u_{ex}+E_g>0$, $u_{ex}>-E_g$, the clipping threshold will be negative $\bar{E}_s = -E_g<0$, and output voltage will correspond to Figure V.24b.

For the V.23b circuit, bias E_g is applied with a "plus" to cathode, i. e., hinders onset of grid current. Therefore, the limiting mode will begin when $u_{ex}-E_g>0$, $u_{ex}>E_g$, the clipping threshold will be positive $E_s = E_g>0$, and output voltage will correspond to Figure V.24c. The same thing ($\bar{E}_s>0$) will occur for the Figure V.23 c, d circuits: in the first instance, bias applied with a "plus" to cathode arises in resistance R_s due to plate current; in the second case, bias applied with a "minus" to grid arises in resistance R_g due to plate current flow. Thus, only the clipping threshold may be increased by using self-bias.

b) Lower grid limiting cannot be accomplished since grid current may flow only in one direction, from grid to cathode.

EXERCISE V.10

When E_g E_{go}, the clipping threshold of the given input voltage (Figure X.27a) is positive $E_s>0$, while output voltage corresponds to Figure X.27b;

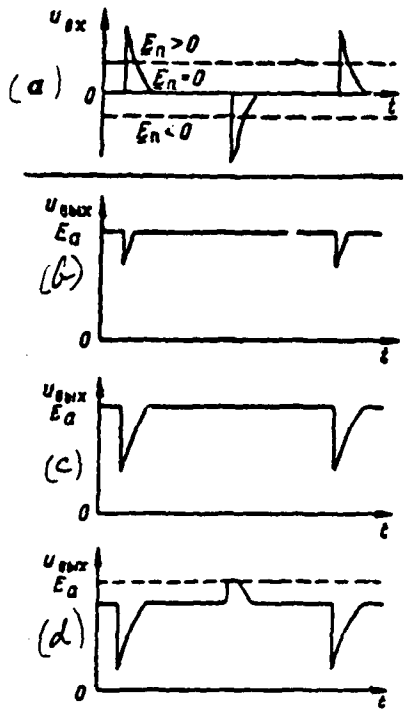


Figure X.27. Plate Current Lower Cutoff Limiter Input (a) and Output Voltages: (b) -- Where $E_g < E_{go}$ ($E_п>0$); (c) -- Where $E_g = E_{go}$ ($E_п=0$); (d) -- Where $E_g > E_{go}$ ($E_п<0$).

where $E_g = E_{go}$, $E_п=0$, while output voltage corresponds to Figure X.27c; where $E_g > E_{go}$, $E_п<0$, while output voltage corresponds to Figure X.27d.

EXERCISE V.11

The output voltage of the plate current upper cutoff limiter depicted in Figure V.30d is repeated in Figure X.28 by means of the dotted line. In this case, $E_п=0$, $U_г=U_{г.огр}$. Only a portion of the negative half-waves $u_{вх}$, which also will be reproduced opposite in phase at output, will "approach" the transfer /475 characteristic linear sector when the negative bias E_g magnitude is decreased. Consequently, when $E'_g < E_g$, the clipping threshold will decrease ($\bar{E}'_п < \bar{E}_п$), while the clipping level remains unchanged (Figure X.28, curve a).

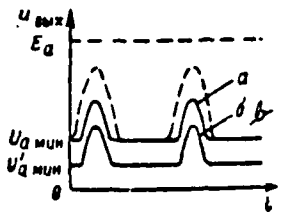


Figure X.28. Plate Current Upper Cutoff Limiter Output Voltages.

Plate voltage is reduced when plate load impedance R_a is increased. As a result, first, dynamic saturation begins where there is less control grid voltage and, second, I_s, and $U_{a\ мин}$ threshold values decrease (see Chapter III, § 3). The first will lead to a clipping threshold decrease (where bias E_g is unchanged), while the second will lead to a clipping level decrease $U'_0 = U_{a\ мин} < U_{a\ мин}$ (Figure X.28, curve b).

EXERCISE V.12

There is no analogy between resistance R and grid limiter network resistance. Resistance R may not lead to signal clipping when there is no saturation.

EXERCISE V.13

a) We determine the minimum safe saturation current value $I_{кн} \geq 0.6$ uA from ratio (V.16). Consequently, load impedance $R_к \leq \frac{E_к}{I_{кн}} = 25$ kilohms.

b) Collector voltage amplitude decreases with a resistance $R_к$ increase since product $I_{кн}R_к$ increases, while voltage $U_{к\ мин}$ essentially remains unchanged. This is illustrated in Figure V.36 where $R'_к > R_к$.

EXERCISE V.14

It is evident from Figure V.37 that the time interval determined by the segment intercepting the tangent to curve $i_к(t)$ at level $I_{кн}$ equals $\tau_з \frac{I_{кн}}{3I_б}$.

EXERCISE V.15

Time constant $\tau = RC$ must be selected so that capacitor charging will conclude before the transistor begins to cut off, i. e., condition $t_u > (3-5)RC$ must be satisfied. In other words, time constant RC determines circuit speed of response.

EXERCISE VI.1

a) Triode L_1 was blanked ($u_{a1} = U_{a\,max}$) when triode L_2 was unblanked ($u_{a2} = U_{a\,min}$). In this event, when triode L_1 malfunctions, its plate voltage will remain unchanged. Consequently, triode L_2 will be unblanked, as usual, and its output voltage will not change.

Triode L_1 was unblanked ($u_{a1} = U_{a\,min}$) when triode L_2 was blanked ($u_{a2} = U_{a\,max}$). In this case, when triode L_1 malfunctions, which is equivalent to its blanking, its plate voltage will rise to value $U_{a\,max}$. Consequently, triode L_2 unblanks and its plate voltage will decrease to value $U_{a\,min}$.

Thus, when triode L_1 malfunctions, triode L_2 will be unblanked in any case. When malfunctioning triode L_1 is replaced by a working one, the latter immediately will be blanked due to the action of voltage $u_{a2} = U_{a\,max}$, while triode L_2, as usual, remains unblanked.

b) Reversing a flip-flop from a given initial state requires either that triode L_2 be unblanked by a positive-polarity pulse or triode L_1 be blanked by a negative-polarity pulse. In any case, the reversal process will have an active (avalanche-like) nature only in the time interval when both triodes are /476 unblanked. The curves for supply of a positive pulse to triode L_2 grid are depicted in Figure X.29a, while supply of a negative pulse to triode L_1 grid are depicted in Figure X.29b (we disregard the influence of stray capacitances). In accordance with (VI.11a), initial grid voltages equal:

$$u_{g1} = U_{g1\,max} = 2E_{go}; \quad u_{g1} = U_{g1\,min} \approx 0.$$

In the first case, beginning at the moment of trigger pulse t_1 action, voltage u_{g2} rises and, at moment t_2 ($u_{g2} = E_{go2}$), triode L_2 unblanks. Here, the positive

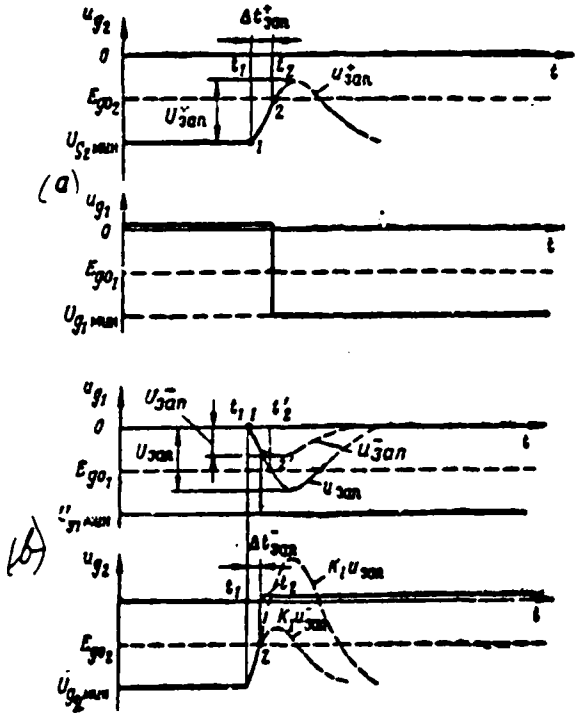


Figure X.29. For Explanation of the Flip-Flop Triggering Process: (a) -- With a positive pulse; (b) -- With a negative pulse. (Influence of Stray Capacitances Not Considered)

feedback loop closes and an instantaneous (with respect to the condition) circuit reversal occurs, resulting in grid voltages taking on new values with a jump. $U_{g1\ max}=2E_{go1}$; $U_{g1\ min}=0$. Inequality (VI.3a) $U^{+}_{3an}>|U_{g\ max}-E_{go}|$ determines the minimum required positive trigger pulse amplitude, while the reversal occurs with a delay equal to trigger time $\Delta t^{+}_{3an}=t_2-t_1$ due to finite pulse porch steepness.

In the second case, beginning from the same moment t_1, voltage u_{g1} decreases. Since triode L_1 is unblanked, it amplifies and inverts the negative pulse. /477 Therefore, a positive pulse amplified by a factor of K_1, where formula (VI.14a) determines gain K_1 magnitude, is transmitted to the triode L_2 grid. Consequently, when voltage u_{g1} decreases, voltage u_{g2} rises at a rate greater by a factor of K_1 than the trigger pulse porch steepness at triode L_1 grid. As a result, triode L_2 unblanks (at moment t_2 when $u_{g2}=E_{go2}$) before it is possible for triode L_1 to blank (time t_2'). Here, the positive feedback loop closes (triode L_1 also unblanks

at moment t_2) and an active circuit reversal occurs. The reversal occurs with a delay equal to triggering time $\Delta t_{зап} = t_2 - t_1 \approx \Delta t_{зап}^{+}$, i. e., the flip-flop will reverse earlier than is the case in the first instance.

Negative trigger pulse amplitude may be decreased by a factor of K_1 due to its amplification by triode L_1, i. e., may be insufficient to blank triode L_1 directly and must only satisfy condition (VI.3): $U_{зап}^{-} > \frac{|U_{g\,max} - E_{g2}|}{K_1}$. Pulses $u_{вых}$ and $K_1 u_{зап}$ in Figure X.29b are depicted for the amplitude identical to that in Figure X.29a (i. e., excessively high) $U_{зап} = U_{зап}^{+}$, while pulses $u_{зап}^{-}$ and $K_1 U_{зап}^{-}$ are depicted for amplitude $U_{зап}^{-}$ decreased by a factor of K_1.

EXERCISE VI.2

a) Connection of resistance $R_к$ will lead to a decrease in unblanked tube current, given the identical plate load impedance R_a magnitude. Therefore, unblanked tube plate potential $U_{a\,max} = E_a - I_a R_a$ will rise. The amplitude of pulses $U_{вых} = U_{a\,max\,a} - U_{a\,max}$ will decrease since value $U_{a\,max\,a}$ will remain unchanged for a blanked tube.

If resistance R_a is decreased so that the current across the unblanked tube remains unchanged when resistance $R_к$ is connected, then the value $U_{a\,max}$ rise occurs due to the decrease in resistance R_a. An increase in R_a, in accordance with (VI.8), will lead to a decrease in value $U_{a\,max\,a}$, which also will lead to a decrease in $U_{вых}$.

b) Triode cathodes will turn out to be "grounded" with respect to the d-c component and self-bias will disappear when capacitor $C_к$ breaks down. Both tubes always will be unblanked since the output voltages of the Figure VI.6 dividers always are positive relative to "ground." Due to the flow of tube grid currents, the potentials of their grids simultaneously will be clipped at level $U_{g\,max\,a} \approx 0$, while plate potentials are clamped at level $U_{a\,max}$. Circuit reversal will become impossible (the positive feedback loop always will be open) since none of the grid potentials of any of the tubes will be able to increase. Consequently, the circuit never will be able to leave the stated equilibrium state. Disappearance of outside negative bias E_g in the Figure VI.5 circuit will lead to the identical result.

c) As usual, it is more advantageous to trigger with negative pulses across unblanked triodes since the mechanism of triggering to plates is identical to the mechanism for triggering to grids. These pulses should be supplied each time to the blanked triode plate, from which it will be transmitted across the appropriate divider to the unblanked triode grid.

The amplitude of trigger pulses must be greater by a factor opposite to the transfer constant of this divider when triggering to plates than when triggering to grids.

EXERCISE VI.3

a) False (repeat) triggering by a pulse of opposite polarity arising as a result of differentiation of the trigger pulse droop by an input network is possible, given slight coupling capacitor capacitance after a flip-flop is triggered by a trigger pulse porch. A negative pulse will cause false triggering when positive pulses are used for triggering and a positive pulse will cause false triggering when negative pulses are used. But, since flip-flop sensitivity to negative pulses is greater than to positive pulses, then, in the first case, the probability /478 of false triggering rises (if a positive pulse triggers the flip-flop, it is mandatory that a negative pulse trigger it). Consequently, triggering with negative pulses also is more advantageous from the point of view of decreasing the danger of misoperations.

b) An increase in accelerating capacitor capacitance will lead to a reduction in triggering time and reversal time, but it will increase recovery time and worsen the shape of the output voltages following reversal (see Figure VI.7).

c) The effect depicted in Figure VI.9 may arise if trigger pulse spacing $T_{вх}$ is somewhat less than flip-flop resolving time $t_{разр}$.

In this event, accelerating capacitors do not succeed in discharging completely during resting times between trigger pulses and, therefore, prior to the moment of the next triggering, blanked triode grid voltage turns out to be less than its fixed value $U_{з.вых}$ (see Figure VI.7b). Initially, the amplitude of the positive pulses in the blanked triode grids turns out all the same to be sufficient to

trigger the circuit (pulses 1—6). However, since for accelerating capacitors discharging time constants (VI.26) are greater than charging time constants (VI.25), then residual voltage acting like dynamic bias in the grids is accumulated gradually in these capacitors due to sequential circuit reversals. Therefore, grid potentials will decrease gradually and, given the action of a certain pulse (pulse 7), the unblanked triode (L_2) already does not unblank. Since the circuit will not reverse, then the next negative pulse (pulse 8) acts upon the blanked triode grid and also will be "passed through."

But, during time $t=3T_{...}$, the accelerating capacitor connected to plate of the triode unblanked during this entire time (L_1) succeeds in discharging completely. Following this, circuit triggering will be restored with arrival of the next pulse (pulse 9) at the grid of this triode. Then, the processes repeat themselves: the flip-flop regularly is tripped by several pulses (9—14), two pulses (15, 16) "pass through," and so forth.

EXERCISE VI.4

a) For Figure VI.10a, the circuit for a divider supplying grid voltage of blanked triode L_2, considering finite back resistance $R_{i\,обр}$ of blanked diode

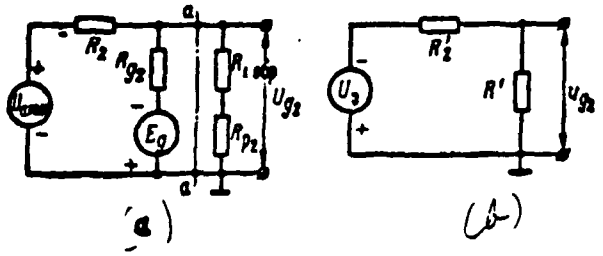


Figure X.30. For Exercise VI.4.

D_2 may be depicted as shown in Figure X.30a. Having used the theorem on the equivalent generator relative to points aa, we convert this circuit to the form depicted in Figure X.30b. In this circuit, $R_2' = \frac{R_3 R_{g2}}{R_3 + R_{g2}}$, $R' = R_{i\,обр} - R_{g2}$, while

equivalent generator voltage equals triode L_2 estimated negative grid voltage (where $R_{сед}=\infty$):

$$U_э = \frac{U_{a\,max} + E_g}{R_1 + R_{g1}} R_{g1} = U_{g1\,max} < E_{g1}$$

Therefore, triode L_2 grid voltage will turn out to equal $U_{g1} = U_{g1\,max}\frac{R'}{R' + R_2}$, /479 i. e., it will rise relative to estimated value $U_{g1\,max}$. Triode L_2 blanking reliability will decrease as a result.

b) When Figure VI.10c triode L_4 malfunctions, a positive pulse supplied to this tridode grid will not impact upon the flip-flop circuit. Therefore, a further reversal will become impossible after subsequent flip-flop triggering across triode L_3, i. e., the circuit will remain in a state whereby triode L_1 is blanked and triode L_2 is unblanked.

EXERCISE VI.5

a) Diode D_2 in the Figure VI.12c circuit may be broken down by great reverse voltage $E_a - U_{a\,max}$ when triode L_1 is unblanked and triode L_2 is blanked. A diode D_2 breakdown will lead to the following consequences.

First, the next negative trigger pulse after the moment of breakdown acts not only upon triode L_1 grid (across diode D_1), but also across breakdown diode D_2 to triode L_2 grid. As a result, both triodes will turn out to be blanked and, in the best case, only passive circuit reversal may occur, given presence of sufficiently-great accelerating capacitances (see Figure VI.13d, e).

Second, slight resistance $R_э$ across breakdown diode D_2 will shunt resistance R_{a1}, resulting in the fact that triode L_1 plate load impedance will decrease. This will lead to an unblanked triode L_1 plate voltage rise and thus a rise in blanked triode L_2 grid voltage. Consequently, the amplitude of output changes in triode L_1 grid will decrease and triode L_2 blanking reliability will deteriorate. In addition, the triode L_1 plate load decrease will lead to a decrease in flip-flop arm gain K_1. This may impact unfavorably on the speed of the subsequent (active) circuit reversal.

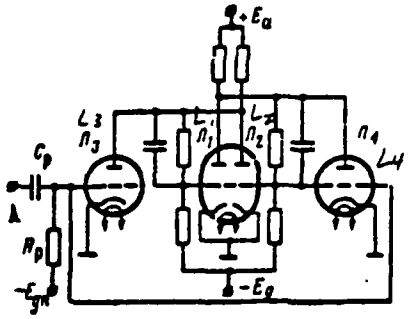


Figure X.31. Flip-Flop Symmetrical Trigger Circuit Across Trigger Triodes.

b) A circuit for symmetrical triggering across trigger triodes L_3, L_4 is presented in Figure X.31 (it is derived from the Figure VI.10c asymmetrical trigger circuit by connection of triode L_3, L_4 grids).

In the initial state, both triodes are blanked by negative bias E_{g} . Positive-polarity trigger pulses act simultaneously on their grids. Selected pulse amplitude is such that the only trigger triode unblanking each time is the one connected to plate of the flip-flop blanked triode. A negative pulse amplified by a trigger triode arises in the flip-flop plate and this pulse acts upon grid of the flip-flop unblanked triode, it is amplified by this triode, and it unblanks the blanked triode, causing circuit reversal. The other trigger triode, connected to flip-flop unblanked triode plate, is not unblanked by the trigger pulse since its plate voltage is so slight.

EXERCISE VI.6

a) Negative bias E_g in a cathode-coupling flip-flop impacts upon the triode L_2 operating mode with respect to direct current. It must be less than in a symmetrical flip-flop since voltage u_{g2} additionally is reduced, given presence of cathode coupling (triode L_2 cathode potential increases relative to "ground") /480 by magnitude U_{k1} when triode L_2 is blanked and by magnitude U_{k2} when triode L_2 is unblanked.

b) Unblanked triode current I_{a1} or I_{a2}, increasing cathode potential relative

to "ground," flows across resistance R in both stable equilibrium states. Therefore, voltage u_a, as was depicted in Figure VI.15d, always is positive.

The law of change for this voltage is explained in the following manner. Unblanked triode L_2 operates in the grid limiting mode where $U_{g2\,макс} \approx 0$. Here, $U_{a2} = I_{a2}R_a$. Unblanked triode L_1, as a result of negative feedback action, operates with negative bias and $U_{g1\,макс} = -U_{a1} = -i_{a1}R_a$. Therefore, $I_{a2} > I_{a1}$ for stable equilibrium states, hence $U_{a2} > U_{a1}$. The latter inequality also results because voltage U_{a2} must be sufficient to blank triode L_1 $(U_{a2} > |E_{g01}|)$ when triode L_2 is unblanked, while voltage U_{a1} must not blank this triode $(U_{a1} < |E_{g01}|)$ when triode L_1 is unblanked since this is done by plate current I_{a1}. Consequently, voltage u_a is greater when triode L_2 is unblanked and less when triode L_2 is blanked, i. e., it changes opposite in phase with L_2 output stage plate voltage. This conclusion also is justified for monostable cathode-coupling multivibrators (see Figure VI.18).

EXERCISE VI.7

a) These voltage curves are depicted in Figure X.32. At the moments of reversal, voltages u_{a1} and u_a change with a jump in the identical directions

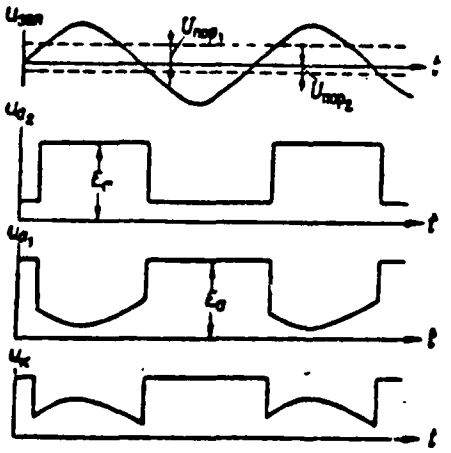


Figure X.32. Cathode-Coupling Flip-Flop Voltage Curves For the Shaping Mode.

as was the case for pulse triggering (see Figure VI.15 and Exercise VI.6b). But, in the shaping mode when triode L_1 is unblanked, its plate current I_{a1} changes in phase with control voltage. Since $u_{a1} = E_a - i_{a1}R_{a1}$ while $u_a = u_{a1} = i_{a1}R_a$ here, then the appropriate control voltage sector will be reproduced opposite in phase at triode L_1 plate and in phase at its cathode. Consequently, square pulses are shaped only at triode L_2 plate.

b) The triode L_1 grid in a cathode-coupling flip-flop is not connected with any other circuit point. Control voltage applied to triode L_1 grid in a symmetrical flip-flop (see Figure VI.5a) would "get through" in stable equilibrium states across resistance R_2 of the second plate-grid coupling to triode L_2 plate. As a result, distortions similar to the control voltage shape would accumulate at voltage u_{a2} pulse tilts and bases.

EXERCISE VI.8

a) If condition (VI.39a) $U_{g1\,max} < E_{go}$ is not satisfied, then triode L_2 will not be blanked when a trigger pulse acts to unblank triode L_1. Therefore, triode L_1 again will be blanked by voltage $U_{k0} = I_{a0}R_k > |E_{go}|$ upon trigger pulse cessation, /481 i. e., no circuit reversal will occur. It will remain in the initial stable state.

b) These curves are depicted in Figure X.33. Given the established conditions, $T_{min} - t_u < t_u$, i. e., trigger pulse spacing is insufficient to complete the multivibrator restoration process (capacitor C_1 charging) following a counter reversal. Therefore, negative voltage u_{g1} does not succeed in rising to its fixed value $U_{g1} = -U_{k0}$ prior to the moment the second trigger pulse arrives and a trigger pulse of greater amplitude is required to trigger the circuit (triode L_1 unblanking).

In addition, prior to the moment the second trigger pulse arrives, voltage u_{a1} does not succeed in attaining fixed value $U_{a1\,max} = E_a$, while positive voltage u_{g2} does not succed in dropping to zero. Therefore, during the second triggering, voltage u_{g2} will drop with a jump by magnitude $\Delta U'_{a1} < \Delta U_{a1}$ to a less negative level then during the first triggering: $U'_{g2,max} > U_{g2,max}$. Consequently, following the second triggering, this voltage will attain level E_{go2} in less time than following the first triggering: $t'_u < t_u$. But, now more time $T_{min} - t'_u = t > T_{min} - t_u$ during which recovery essentially may be completed remains for circuit recovery prior

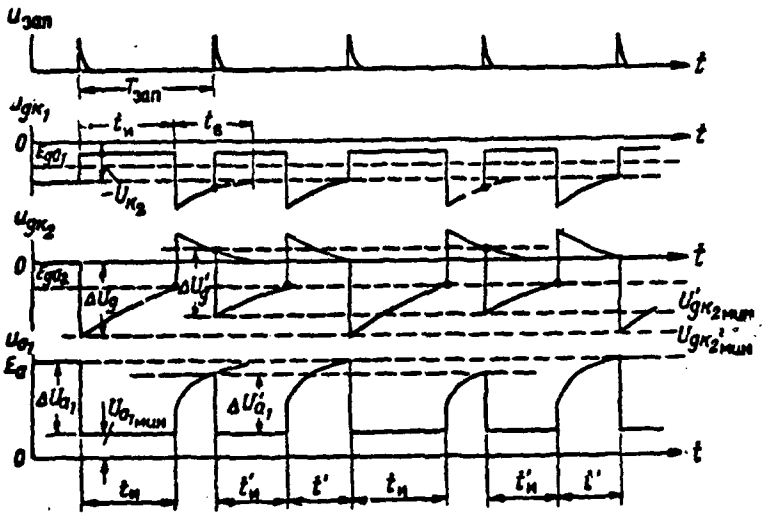


Figure X.33. Cathode-Coupling Monostable Multivibrator Voltage Curves Where $t_в < T_{зап} < t_и + t_в$.

to arrival of the third pulse. Then the third pulse will occur with normal initial conditions and resultant quasistable state time will be identical to that following the first triggering, i. e., it will equal $t_и$. As a result, again there will be insufficient time for circuit recovery prior to arrival of the fourth pulse, and so on. Thus, the circuit sequentially will shape pulses of different duration $t_и$ and $t'_и$.

c) These curves are depicted in Figure X.34, given these conditions. We will begin with examination of the processes from moment t" of circuit counter

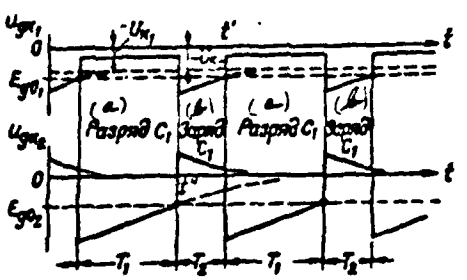


Figure X.34. Free-Running Cathode-Coupling Multivibrator Operation. (a) -- C_1 Discharge; (b) -- C_1 Charge.

reversal. At that moment, when triode L_2 unblanks, triode L_1, just as before, will be blanked by a negative voltage u_{g1} "bump." Actually, at moment t", /482 voltage u_a with a jump will rise to value $U_{a\,max} = U_{a2} + I_a R_a$, which will exceed cutoff voltage magnitude $|E_{go1}|$ when $U_{a2} = |E_{go1}|$. Next, in connection with a capacitor C_1 charging current decrease, voltage u_a also will decrease, while negative voltage u_{g1} will rise, striving towards fixed value U_{a2} at which triode L_1 blanking already is not insured $U_{a2} < |E_{go1}|$. Therefore, spontaneous triode L_1 unblanking, i. e., a "direct" circuit reversal, will occur at moment t', when voltage u_{g1} equates to cutoff voltage E_{go1}. Then the processes repeat themselves. Consequently, the circuit converts to the free-running mode. Here, the capacitor C_1 discharging process, i. e., ratio (VI.49), as was the case in the monostable mode, determines the time T_1 the circuit remains in the former quasistable state (triode L_1 is unblanked, triode L_2 is blanked). The capacitor C_1 charging process with time constant $\tau_{зар1} \approx C_1 R_{a1}$ determines the time T_2 the circuit remains in the new quasistable state (triode L_1 is blanked, triode L_2 is unblanked).

EXERCISE VI.9

a) These voltage curves are depicted in Figure X.35. A bias voltage E_{a1} increase leads to a linear rise in current I_{a1} (see Figure VI.22). Expression

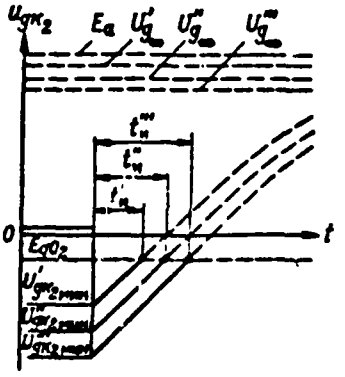


Figure X.35. For Exercise VI.9a.

(VI.51a) determines the magnitude of the triode L_2 grid voltage negative step at the moment of circuit reversal in a quasistable state:

$$U_{g2\,max} = -I_{a1}(R_{a1} + R_k) + I_{a2}R_k.$$

i. e., it will depend linearly on current I_{a1} magnitude. Voltage u_{g2} will begin to rise from a more negative level, striving in accordance with (VI.52) towards value $U_{g2,\infty} = E_a - I_{a1}R_k$, which also (even though to a lesser degree) will decrease, when voltage E_{c2} increases. Recharging time constant τ_{rec} does not change when magnitude E_{c2} changes. Therefore, the graphs of voltage u_{g2} in a quasistable stage for various E_{c2} values is a family of essentially parallel segments of virtually straight lines. As a result, the duration of the shaped pulses turns out to be linearly-dependent on the magnitude of voltage $U_{g2\,max}$, i. e., on voltage E_{c2} in the final analysis.

b) It is possible to control pulse duration by the voltage E_{c2} magnitude in a cathode-coupling "zero"-grid monostable multivibrator, too. Just as in a retarding-field multivibrator, a voltage E_{c2} increase will lead to value $U_{g2\,max}$ becoming more negative, resulting in a pulse duration rise. However, since a capacitor C_1 discharge, rather than a recharge, occurs in a circuit with a "zero" grid in a quasistable state, resulting in the law of voltage u_{g2} rise /483 corresponding to a more-linear sector of the exponential curve, the resultant relationship of t_u to E_{c2} is significantly less linear than in a retarding-field circuit.

c) It is sufficient to violate condition (VI.51), which insures triode L_1 blanking in a stable state, to convert a cathode-coupling retarding-field monostable multivibrator to the free-running mode. This may be accomplished either through a decrease in resistance R_k or by an increase in voltage E_{c2} or, finally, by an increase in resistance R_{a2}. Here, triode L_1 will be blanked following a circuit counter reversal only for a limited time due to an increase in cathode potential as capacitor C_1 charging current flows across resistance R_k (see Exercise VI.8c).

EXERCISE VI.10

The duration of the shaped pulse is determined in an identical manner, both

when a forced-cutoff monostable multivibrator and when an asymmetrically-triggered flip-flop are used. The determinant is the time interval between the external pulse reversing the circuit in one direction and the external pulse reversing the circuit in the other direction. However, a monostable multivibrator always will be in the single possible stable condition to which it automatically transfers when external pulses disappear (interruptions in pulse arrival) prior to arrival of the first trigger pulse. Consequently, a monostable multivibrator without fail will be tripped by the first trigger pulse. There is no guarantee of this with a flip-flop, which may be in one of two possible stable states and will be tripped by the first trigger pulse in only one of these states.

EXERCISE VI.11

a) These voltage curves for a basic asymmetrical multivibrator circuit are depicted in Figure X.36. Based on ratio (VI.71 and VI.72), we will get $T_1 = 2T_2$

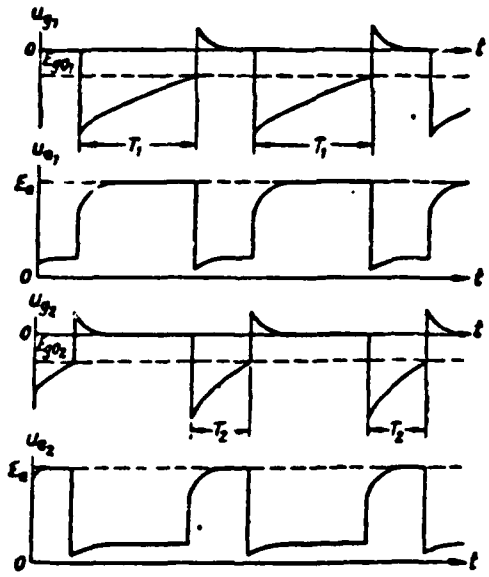


Figure X.36. Basic Asymmetrical Multivibrator Circuit Voltage Curves ($R_{g1} = 2R_{g2}$)

when $R_{g1} = 2R_{g2}$. The interval T_2 reduction by a factor of 2 is explained by the decrease in the capacitor C_1 discharging time constant, which results in an increase in the rate of triode L_2 negative grid voltage rise when this triode is blanked.

b) Supplying outside negative bias sufficient to blank the triode to the grid network of one triode (L_1, for example) $E_{g1} < E_{go1}$ is sufficient to convert

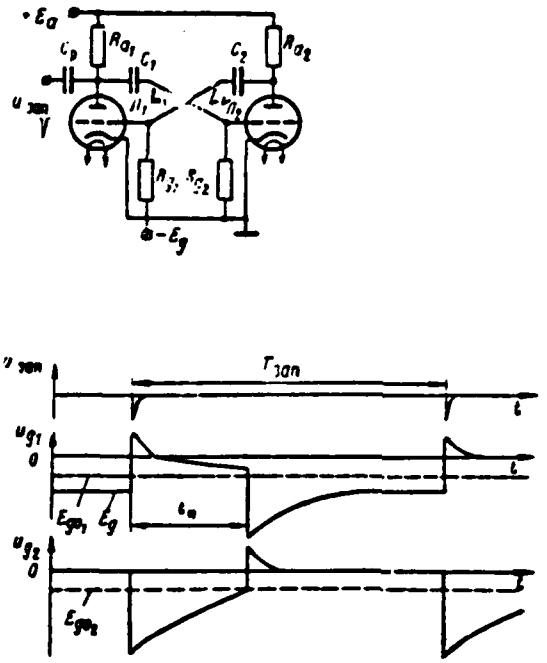


Figure X.37. Basic Monostable Multivibrator Circuit.

a basic multivibrator circuit to the monostable mode. A stable state then arises in the multivibrator (triode L_1 is blanked, triode L_2 is unblanked), and only an external pulse may remove it from this state. The resultant circuit and the given voltage curves in it are depicted in Figure X.37.

Circuit triggering requires that the amplitude of a positive trigger pulse amplified by triode L_2 in the triode L_1 grid be sufficient for its unblanking: $U^{+}_{вх} > |E_{g1} - E_{go1}|$. Here, circuit reversal in the quasistable state will occur (triode L_1 is unblanked, triode L_2 is blanked).

Bias source E_{g1} is not included in the capacitor C_2 charging and discharging network, but is a part of the capacitor C_1 charging and discharging network.

Therefore, the voltage u_{g2} curve will remain identical, while the voltage /485 u_{g1} curve will change in the following way compared to the free-running circuit. Following a positive step, at the moment of triggering voltage u_{g1} will decrease in connection with the capacitor C_2 charging current decrease, striving now, however, towards value $E_{g1} < 0$ rather than towards the zero level. Here, as long as $u_{g1} > 0$, capacitor C_2 charging occurs by triode L_1 grid current, i. e., with slight time constant $\tau_{зар1} = C_2 R_{a2}$. But, when $u_{g1} < 0$, grid current ceases and further charging of this capacitor occurs already with significantly-large time constant $\tau_{зар2} \approx C_2 (R_{a1} + R_g) (R_{g1} \gg R_{a2})$. Therefore, the voltage u_{g1} decrease occurs initially at a high, then at a low, rate.

There is a negative voltage u_{g1} step at the moment of circuit counter reversal, followed by a gradual rise in this voltage in connection with a capacitor C_2 discharging current decrease. However, since it will strive towards a negative E_g value, triode L_1 remains blanked and triode L_2 unblanked until arrival of a new trigger pulse.

Triode L_2 must unblank before triode L_1 blanks in order for an active circuit counter reversal to occur. Here, the amount of time the circuit remains in a quasistable state (generated pulse duration $t_и$) is determined just as interval T_1 was for a free-running circuit. Otherwise, only a passive circuit reversal will occur at the moment triode L_1 is blanked, while the stability of this moment (i. e., pulse duration) deteriorates in connection with the slow voltage u_{g1} approximation to cutoff voltage E_{go1}.

EXERCISE VI.12

Duration of pulses generated by a free-running retarding-field multivibrator is determined from the same circumstances as was the case for a monostable retarding-field multivibrator. Here, it is neccessary only to consider that, in this circuit, cathode load impedance $R_к$ is absent. Assuming that $R_к = 0$ in ratio (VI.55), we will get $T_1 = C_1 R_{g1} \frac{I_{a1} R_{a1} + E_{g1}}{E_a}$ and analogously $T_2 = C_2 R_{g2} \frac{I_{a2} R_{a2} + E_{g2}}{E_a}$.

Comparing these expressions with expressions (VI.71 and VI.72), we see that, all other conditions being equal, pulse duration in a retarding-field circuit is less than in a basic circuit (with "zero" grids). Therefore, the required magnitude of resistances R_{g1} and R_{g2} is greater in a retarding-field circuit than in a basic circuit.

EXERCISE VI.13

a) Diode D in the Figure VI.34 circuit boosts the capacitor C discharging process arising when the circuit reverses during a reference voltage return stroke. If this diode malfunctions, then great resistance R_{g2} will enter the discharging network, which greatly will stretch the voltage u_{g2} negative exponential "bump" (see Figure VI.35d).

This will manifest itself primarily when there are large voltage $u_{уп}$ values approximating maximum voltage $u_{оп}$. Actually, as depicted in Figure X.38, in this case the interval between the moments of circuit tripping t_1 and t_2 will

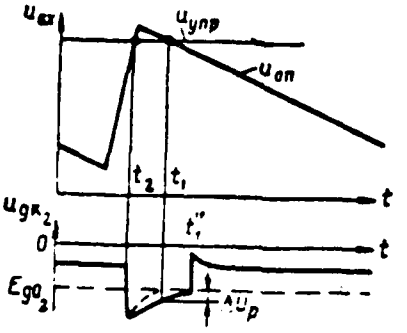


Figure X.38. For Exercise VI.13.

be slight (a counter reversal occurs at the end of the return stroke, while a forward reversal occurs at the beginning of a reference voltage forward stroke) and, prior to moment t_1, capacitor discharge will not succeed in concluding.*

*Comparison error Δt_1, caused by voltage ΔU_1 is not reflected in Figure X.38 for the purposes of simplicity.

Because of this, at moment t_1 given voltage equality $u_{гор}=u_{оп}$, voltage $u_{бал}$ will be less than cutoff voltage E_{go2} by magnitude $\Delta U_p = I_{p_1} R_{g1}$, where I_{p_1} -- discharging current value at moment t_1. As a result, triode L_2 unblanks later, at moment t_1''. The lag in the moment of direct circuit cripping will be greater, /486 the greater the voltage $u_{гор}$ ($u_{гор}<U_{оп\ макс}$).

b) The polarity of the diode D connection should be changed when linearly-rising reference voltage is used.

EXERCISE VI.14

It is evident from expression (VI.82) that, given a sufficiently-great factor β value, resistance R_1 magnitude turns out to be many times greater than resistance $R_н$. Therefore, the amplitude of a pulse with growth β rises, approximating value

$$U_н \approx E_г - I_{нр} R_г \approx E_г.$$

EXERCISE VI.15

Output pulse $U_{вых2}$, rise time $t_ф^{(+)}$ (Figure VI.37) decreases with an increase in capacitor C_1 capacitance. The decrease in capacitor C_2 capacitance leads also t a reduction in rise time $t_ф^{(-)}$. Consequently, output pulse $U_{вых2}$ shape improves. However, output pulse $U_{вых1}$ shape deteriorates here.

EXERCISE VI.16

Considering that collector and emitter currents are approximately the same, it is possible to determine bias voltage $U_{р_0}$ from the formula

$$U_{р_0} = I_0 R_0 \approx I_г R_0 = \frac{E_г}{R_г + R_0} \cdot R_0 \approx E_г \frac{R_0}{R_г}.$$

EXERCISE VI.17

A decrease in resistance R_0 magnitude requires an identical increase in capacitor C capacitance to obtain a pulse of a given duration. But, this leads

to an increase in the capacitor C charging time constant and, consequently, to negative pulse porch or positive pulse droop stretching.

EXERCISE VI.18

1. The recharging time constant $\tau = R_6C$ = 1 usec. Pulse duration determined from formula (VI.102) comprises

$$t_и = 0.7R_6C = 0.7 \cdot 10^{-3} \text{ sec} = 700 \text{ μsec}.$$

2. We determine shunting resistance magnitude /487

$$R_ш = \frac{E_п}{I_{ок}}.$$

For a P14 transistor, where t = +20° C $R_ш$ = 3.0 megohms; where t = +65° C, $R_ш$ = 0.5 megohms.

For a P106 transistor, where t = +20° C $R_ш$ = 30.0 megohms; where t = +65° C, $R_ш$ = 5.0 megohms.

3. We determine duration considering shunting using formula (VI.107).

When P14 transistors are used, when t = +20° C $t'_и = 10^{-3} \ln 1.97$ = 686 usec; where t = +65° C $t'_и = 10^{-3} \ln 1.93$ = 600 usec.

When P106 transistors are used, when t = +20° C $t'_и = 10^{-3} \ln 1.99$ = 696 usec; when t = +65° C $t'_и = 10^{-3} \ln 1.98$ = 690 usec.

4. The relative pulse duration change (in percent) comprises:

when a P14 transistor is used

$$\delta\% = \frac{t_и - t'_и}{t_и} \cdot 100\% = 11.7\%$$

when P106 transistors are used

$$\delta_0 = 10\%$$

Conclusions. Comparison of results obtained indicates that formula (VI.102) provides an error exceeding 10% when germanium transistors are used at room temperature and is unacceptable for an increased temperature. Consequently, formula (VI.107) must be used.

Formula (VI.102) provides satisfactory results over a broad range of temperature changes when silicon transistors are used.

EXERCISE VI.19

a) In accordance with formula (VI.121), a change in C capacitance, recharging resistance $R_з$, and initial capacitor C voltage may be used to control pulse duration.

Design complexity is the basic drawback of using a change in C capacitance to control $t_и$.

A change in resistance $R_з$ also is inadvisible since the transistor T_2 operating mode changes, as does circuit temperature stability.

The method whereby initial capacitor voltage changes but transistor modes

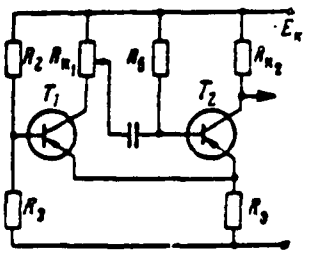


Figure X.39. Pulse Duration Control in a Transistor Monostable Multivibrator.

do not provides the best results. For that purpose, capacitor C is connected to a part of resistance $R_{ш}$ rather than to the transistor T_1 collector, as depicted in Figure X.39.

b) A change in resistance R_2 and R_3 does not impact upon the duration of the shaped pulse. Only the transistor T_1 mode changes.

EXERCISE VI.20 /488

Maximum pulse duty ratio

$$Q = 1 + \frac{t_и}{t_{восст}} = 1 + \frac{R_{ш}C \ln 2}{(4 \div 5) RC} = 1 + \frac{0{,}7R_{ш}}{(4 \div 5) R}.$$

$Q = 70 \div 80$ when $R_{ш} = 100$ kilohms and $R = 200$ ohms.

EXERCISE VII.1

The Figure VII.5 oscillograms in the order indicated correspond to points А, Б and В, respectively (Figure VII.2a). Due to transformer coupling in load winding w_3, the signal has a shape identical to that of voltage e_1 in winding w_1. Consequently, the shapes of pulses at load and at tube plate also must coincide since $u_a = E_a - e_1$.

The difference may lie in selected pulse polarity at load and its amplitude. The decrease in magnetizing current by an aperiodic law causes the "bumps" in the aforementioned oscillograms.

The pulse at cathode load is shaped due to plate and grid current flow and always is of positive polarity. It will not comprise a "bump" since plate and grid currents disappear instantaneously after the tube blanks.

The grid current decrease explains the flat pulse tilt (see Figure VII.4d).

EXERCISE VII.2

Fixed and variable resistances usually are connected instead of resistance R (Figure VII.7a) to change pulse repetition frequency within minor limits. The repetition frequency change in this case is accomplished best by switching two different resistances. It is undesirable to change capacitor C capacitance for two reasons: first, the duration of the shaped pulse will change and, second, tilt slope will change, which often is undesirable.

EXERCISE VII.3

It is evident from Figure VII.8b that, where $\Delta U_{C_3} \ll \Delta U_C$, pulse spacing T_0 must fall within the limits

$$T_3\left(n+\frac{1}{4}\right)<T_0<T_3\left(1+\frac{1}{2}\right).$$

where n -- number of complete resonant loop oscillation periods contained in resting time interval t_3.

EXERCISE VII.4

Pulse transformer windings in a common-emitter circuit are connected in opposition since the transformer must be an inverting transformer to accomplish positive feedback (see the polarity of self-induction emf e_1 and self-induction emf e_2 in Figure VII.10b). There is no signal inversion in a common-base transistor circuit. Therefore, pulse transformer windings must be matched. For conditional depiction of such a connection, the points must be placed at the ends of windings connected to collector and base outputs, respectively.

EXERCISE VII.5

The diode must be connected as depicted in Figure X.40. In this case, diode D unblanks and shunts the transformer winding when collector voltage is reduced below the E_3 level due to self-induction emf.

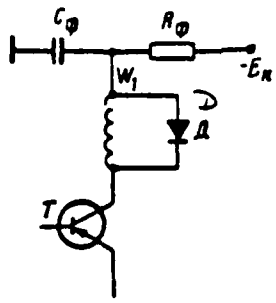


Figure X.40. Damping Diode Connection.

EXERCISE VIII.1

Solution of the problem requires comparison of sync pulse repetition period

$T_c = \frac{1}{F_c} = \frac{10^6}{10^4}$ = 100 usec with blocking oscillator inherent self-excited oscillation period (inherent pulse spacing) T_0. The latter for a retarding-field blocking oscillator (Figure VIII.2) is determined from formula (VII.12)

$$T_0 \approx 2.3RC \lg \frac{E_a + |U_{C\,max}|}{E_a + |E_{go}|}.$$

where $U_{C\,max} = -U_{g\,max}$ (see Figure VII.7b);
C — capacitance;
R — grid (timing) network resistance.

The greater the scaling factor, the greater period T_0 will be, given the assigned T_0 magnitude. Period T_0 for the Figure VIII.2 circuit will be maximum for the extreme "upper" potentiometer R_5 arm position when $R = R_{max} = R_3 + R_4$. Thus, for this circuit considering its parameters for given values $U_{g\,max}$ and E_{go}:

$$T_{0\,max} \approx 2.3\,(R_4 + R_5)\,C_1 \lg \frac{E_a + |U_{g\,max}|}{E_a + |E_{go}|} =$$

$$= 2.3 \cdot 950 \cdot 10^3 \cdot 2400 \cdot 10^{-12} \cdot 10^6 \lg \frac{350}{310} \approx 2250 \cdot 0.122 = 278 \text{ usec.}$$

— inherent period of oscillations will exceed sync pulse spacing by a factor

of 2.78. Consequently, the maximum possible scaling factor is $K_{3\,max} = 2$ (the third sync pulse will arrive already after spontaneous circuit reversal).

EXERCISE VIII.2

For point B located inside the $K_3 = 4$ zone, we have

$$\frac{T_c}{T_0} = 1.2; \quad \frac{U_c}{|U_{g\,max} - E_{go}|} = 0.3.$$

The corresponding curves are depicted in Figure X.41a and demonstrate /490 that, in this case, four-to-one stable frequency demultiplication will occur.

For point F located on the right edge of the $K_3 = 2$ zone, we have: $\frac{T_c}{T_0} = 0.5$; $\frac{U_c}{|U_{g\,max} - E_{go}|} = 0.3$. The corresponding curves are depicted in Figure /491 X.41b and demonstrate that, in this case, two-to-one unstable frequency demultiplication will occur. Actually, under the given conditions, periods of inherent and forced oscillations theoretically coincide $T_0 = T_3$. In practice, this will lead to the fact that, even when there are slight changes in the magnitudes of T_c or T_0, oscillations will occur, some with an inherent and some with a forced period.

For point A falling on the common boundary of the $K_3 = 2$ and $K_3 = 3$ zones, we have: $\frac{T_c}{T_0} = 0.25$; $\frac{U_c}{|U_{g\,max} - E_{go}|} = 0.5$. The corresponding curves are depicted in Figure X.41c and demonstrate that, in this event, first two-to-one, then three-to-one, unstable frequency demultiplication will occur. This is explained by the fact that, under the given conditions, grid voltage rises exactly to the cutoff voltage level under the action of each second pulse following a reversal. Here, depending on fluctuating changes of magnitudes $\frac{U_c}{|U_{g\,max} - E_{go}|}$ and $\frac{T_c}{T_0}$, the circuit may either reverse (and then $K_3 = 2$) or not reverse (but then it will reverse with the third pulse and $K_3 = 3$). Thus, the period of forced oscillations randomly will take on the value $T_3 = 3T_c$ or $T_3' = 2T_c$.

For point E falling below the $K_3 = 1$ zone and to the right of the $K_3 = 2$ zone, we have: $\frac{T_c}{T_0} = 0.6$; $\frac{U_c}{|U_{g\,max} - E_{go}|} = 0.2$. The corresponding curves are depicted

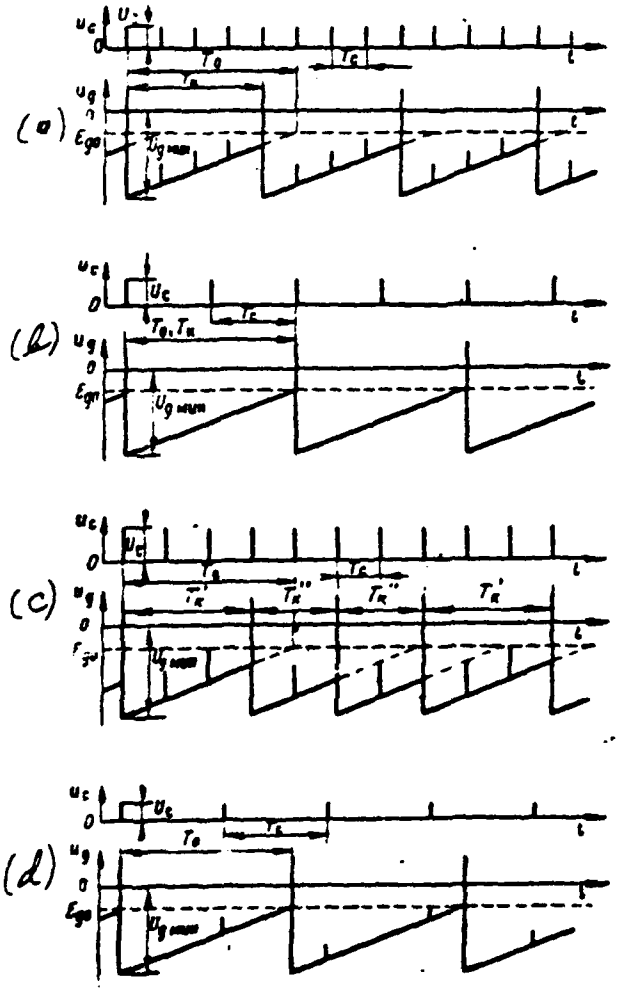


Figure X.41. Idealized Voltage Curves for a Blocking Oscillator in the Synchronization Mode.

in Figure X.41d and demonstrate that, in this event, the blocking oscillator will produce oscillations with inherent period T_0 and there will be no frequency division.

EXERCISE VIII.3

Frequency division using the Figure VIII.8 multivibrator circuit

under the given conditions is possible only due to "pass through" of negative sync pulses arriving at interval T_{o1} (when triode L_2 is unblanked and triode L_1 is blanked). To find this interval, it is sufficient to determine the duty ratio of the inherent multivibrator oscillations. When the potentiometer R_5 arm is

in the middle position: $R_{g1} = R_3 = 50$ kilohms, $R_{g2} = R_4 + \frac{R_5}{2} = 25$ kilohms. Therefore, based on formulas (VII.71, VII.72), considering that $C_1 = C_2$, $R_1 = R_2$, $E_{go1} = E_{go2}$, we will get $T_{o1} = 2T_{o2}$.

Thus, we have $T_0 = T_{o1} + T_{o2} = 1.5T_{o1} = 3T_c$ or $\frac{T_0}{T_c} \approx 3.3$. But, this means that three /492 pulses to which the circuit will not react always will arrive in interval T_{o1},

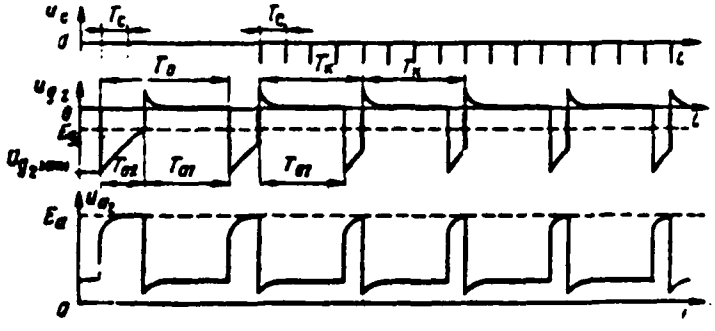


Figure X.42. Idealized Voltage Curves for a Multivibrator in the Synchronization Mode.
($T_{o1} = 2T_{o2}$, $T_0 = 3T_c$)

the fourth pulse without fail (based on the condition that amplitude U_0 is sufficiently great) will force a circuit reversal. Consequently, $K_3 = 4$. These curves are presented in Figure X.42.

EXERCISE VIII.4

For point A located in the $K_3 = 2$ zone, we have $\frac{T_c}{T_0} = 0.25$; $\frac{U_c}{|U'_{g\max} - E_{g0}|} = 0.9 > \frac{U_1}{|U'_{g\max} - E_{g0}|} = 0.6$. The corresponding curves are depicted in Figure X.43a and demonstrate that, in this case, two-to-one frequency division will occur because one pulse each time arrives in interval T_{01}, while the subsequent one will force the circuit to reverse.

For point B. located in the $K_3 = 3$ zone, we have: $\frac{T_c}{T_0} = 0.25$; /493 $\frac{U_c}{|U'_{g\max} - E_{g0}|} = 0.4 < \frac{U_1}{|U'_{g\max} - E_{g0}|} = 0.6$. The corresponding curves are depicted in Figure X.43b and demonstrate that, in this event, three-to-one frequency division will occur because one pulse each time arrives at interval T_{01}, the subsequent pulse does not impact upon the circuit due to its insufficient amplitude, and only the third pulse will force the circuit to reverse.

For point B. located in the same $K_3 = 3$ zone, but in its vertical band, we have: $\frac{T_c}{T_0} = 0.15$; $\frac{U_c}{|U'_{g\max} - E_{g0}|} = 0.9$. The corresponding curves are depicted in Figure X.43c and demonstrate that, in this case, three-to-one frequency division also will occur, but each time two pulses already arrive at interval T_{01} and the third reverses the circuit.

EXERCISE VIII.5

Circuit recovery time $T_{c\,\min} = t_0$ constrains trigger pulse spacing when a monostable multivibrator is used as a frequency divider (see Figure VIII.12). When $T_c = T_{c\,\min}$, $\frac{t_0}{T_{c\,\min}} = \frac{t_0}{t_0}$ pulses to which the circuit does not react arrive during time t_0 of the quasistable state. After this, the circuit will be triggered by the pulse which arrived immediately following circuit recovery. The resultant maximum scaling factor equals

$$K_{3\,\max} = \frac{t_0}{t_0} + 1 = \frac{t_0 + t_0}{t_0}.$$

EXERCISE VIII.6

$K_д = 2^6 = 64$ when six sequentially-operating flip-flops are used. The maximum number of pulses this circuit will be able to count is $N_{max} = 111111$ (63).

EXERCISE VIII.7

a) The functional diagram and voltage curves for an amplifier where $K_у = 9$ were depicted in Figure VIII.17. Bringing the Figure VIII.15b circuit to the given mode requires that the first, second, and third flip-flops be enveloped by feedback. Since each flip-flop's negative output pulses are produced when output (right) tubes unblank (see Figure VIII.16) when the divider is operating without feedback, then pulses supplied from divider output to the stipulated flip-flops with respect to feedback must reverse them in the opposite direction, i. e., lead to blanking of the right-hand tubes. Positive-polarity pulses picked off output blocking oscillator resistance $R_к$ may be used for this purpose, supplying them to the right-hand tube cathodes (which is equivalent to supplying negative

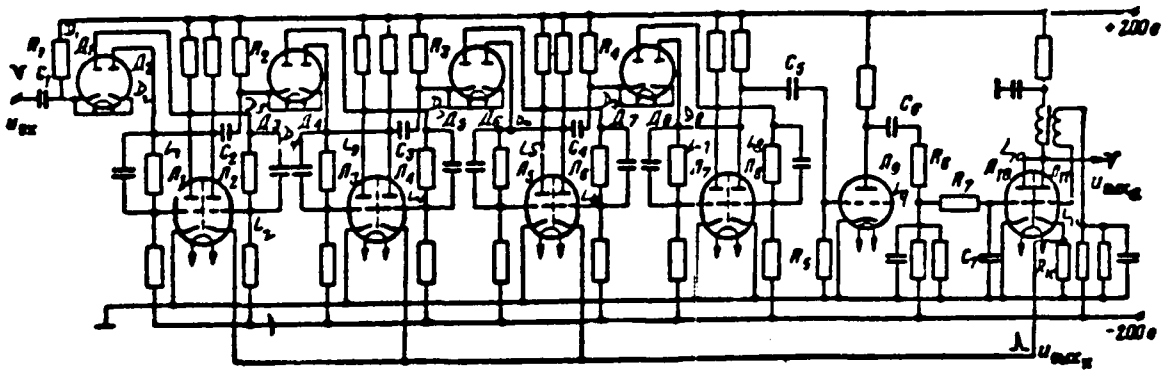


Figure X.44. $K_д$ = 9 Flip-Flop Divider Schematic Diagram.

pulses to the grids of these tubes). Requisite pulse delay may be obtained in the feedback network by using an R-C integrator connected at blocking oscillator

trigger tube L_{10} input. The schematic diagram of a $K_д = 9$ divider circuit obtained in this manner is depicted in Figure X.44.

b) For the Figure VIII.18a circuit, n = 3 and $K_д = 2^3 = 8$ in the absence of feedback. A "malfunction" with the help of feedback of the second flip-flop

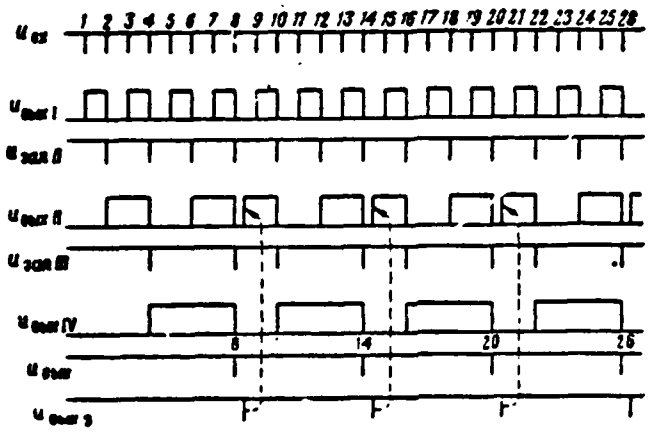


Figure X.45. Voltage Curves for the Figure VIII.18a Divider Circuit.

will provide a decrease in $K_д$ (counter shift) by 010 (2 unities). Therefore, the resultant scaling factor is $K_д = 8-2 = 6$. The circuit voltage curves are depicted in Figure X.45.

c) For the Figure VIII.18b circuit, n = 5 and $K_д = 2^5 = 32$ in the absence of feedback. A "malfunction" with the help of feedback of the first and fourth flip-flops will provide a decrease in $K_д$ (counter shift) by 01001 (9 unities). Therefore, the resultant scaling factor is $K_д = 32-9 = 23$.

d) Obtaining $K_д = 5$ requires that the circuit include three flip-flops /495 ($2^3 > 5 > 2^2$), which without feedback would provide eight-to-one frequency division. In order for $K_д = 5$, the pulse counter must be shifted by 8—5 = 3 unities, i. e., by 011. Consequently, feedback must be supplied to the first and second flip-flops. A functional diagram of a $K_д = 5$ divider and its voltage curves are depicted in Figure X.46.

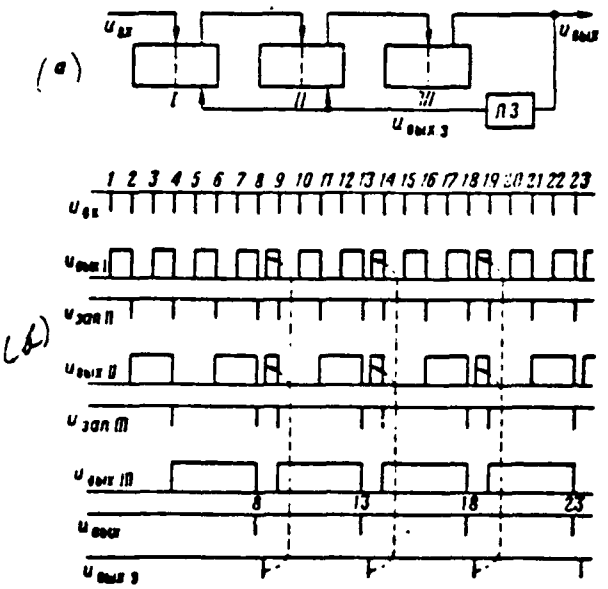


Figure X.46. $K_д$ = 5 Flip-Flop Divider Functional Diagram (a) and Voltage Curves (b).

e) Obtaining $K_д$ = 42 requires that the circuit contain six flip-flops /495 ($2^6 > 42 > 2^5$), which, without feedback, would provide 2^6 = 64 fold frequency

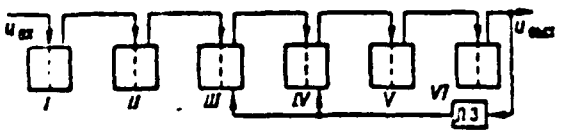


Figure X.47. $K_д$ = 42 Flip-Flop Divider Functional Diagram.

division. In order for $K_д$ = 42, the pulse count must be shifted 64--42 = 12 unities, i. e., by 1100. Consequently, feedback must be supplied to the third and fourth flip-flops. A functional diagram of this divider is depicted in Figure X.47.

EXERCISE VIII.8

Reference train pulse delay time t_0 must exceed the maximum possible magnitude of divider output pulse time lag instability. Otherwise, the divider output pulse may arise later than the corresponding reference train pulse and it will turn out to be impossible to gate the latter.

Gate pulse duration must satisfy condition $T_{вх} > t_{гат} > t_0$ in order to guarantee gating of the requisite reference train pulse and not allow the subsequent reference train pulse to pass through to circuit output.

EXERCISE IX.1

A linearly-falling voltage generator circuit and its output voltage are depicted in Figure X.48. In the initial state ($t < t_1$, switch K closed), the capacitor

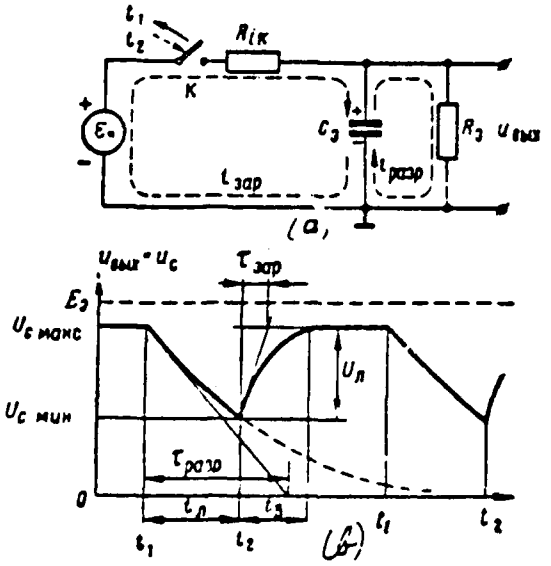


Figure X.48. Linearly-Falling Voltage Generator Equivalent Circuit and Output Voltage Curves.

is charged to voltage $U_{C\,макс} = \frac{E_3}{R_{1K} + R_0} R_0$.

Forward stroke shaping occurs due to the partial capacitor C_0 discharge across resistance R_0 during the time switch K is open. Therefore, working stroke linearity is insured if $\tau_{разр} = \tau_2 = C_0 R_0 \gg t_2 = t_2 - t_1$. Circuit recovery /496 (return stroke shaping) occurs during complete capacitor charging when switch K is closed. During the recovery process, output voltage rises from value $U_{C\ мин}$ achieved at the end of the working stroke to value $U_{C\ макс}$ with time constant $\tau_{зар} = \tau_1 = C_0 \frac{R_{1к} R_0}{R_{1к} + R_0}$. Here, $t_0 \approx 3\tau_{зар}$. In order to obtain $t_2 \gg t_0$ given a high degree of working stroke linearity, it is necessary to satisfy the condition $\tau_{разр} \ll \tau_{зар}$, i. e., $R_0 \gg R_{1к}$ (here, $\tau_{зар} \approx C_0 R_{1к}$). Besides, the lower the switch internal resistance in a conducting state, the greater the $U_{C\ макс}$ value (where /497 $R_0 \gg R_{1к}$ $U_{C\ макс} \approx E_0$), i. e., saw amplitude $U_2 = U_{C\ макс} - U_{C\ мин}$. Thus, the same ratios must be satisfied as was the case in the linearly-rising voltage generator.

EXERCISE IX.2

The linearity of the R-C integrator collector voltage in the beginning of the charging process (where $\frac{t}{\tau_{зар}} \ll 1$) is explained by the fact that as long as this voltage, rising gradually, remains still much less than source voltage, it virtually will not counteract the latter. Therefore, capacitor charging current essentially remains constant: where $u_C \ll E_0$ $i_3 = \frac{E_0 - u_C}{R} \approx \frac{E_0}{R}$. But, when charging current is constant, capacitor voltage rises by a linear law.

EXERCISE IX.3

Given these malfunctions, exponential sweep generator output voltage curves arising at moment t' are depicted in Figure X.49.

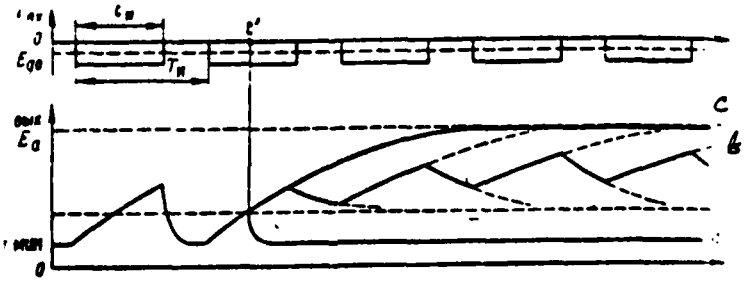


Figure X.49. Manifestation of Exponential Sweep Generator Malfunctions.

a) If disabling pulses stop arriving at circuit input at moment t', then, beginning at that moment, the triode always will be unblanked and the capacitor rapidly will discharge across it to voltage $U_{c\,нач}$, after which output voltage will not change $u_{вых}=U_{c\,нач}=\text{const}$ (curve a). An input pulse amplitude decrease to value $U_{вх}<|E_{зап}|$ will lead to the same result.

b) A partial loss of emission in a triode will lead to a decrease in /498 quiescent current I_{ao}, which is equivalent to an increase in triode resistance to direct current R_{io}. This entails, first, an increase in voltage $U_{c\,нач}$ initial level, towards which the capacitor will strive to discharge and, second, an increase in discharging time constant $\tau_{разр}=CR_{io}$, i. e., in circuit recovery time. As a result, saw amplitude will decrease, while its average level gradually rises to a value when dynamic equilibrium will be established in the capacitor: the amount of electricity obtained during charging time $\tau_з$ compares with the amount of electricity lost during discharging time $\tau_р$ (curve b).

c) It will be impossible for the capacitor to discharge across the triode when the latter completely loses its conductivity and, beginning at moment t', the capacitor will charge completely across source E_a. As a result, output voltage will attain level E_a during time interval $t=3\tau_{зар}$ and then will remain constant (curve c).

EXERCISE IX.4

The rate of voltage change during a working stroke when converting from scale 1 to scale 2 must be reduced by a factor of 2: $v_2=\operatorname{tg}\alpha_2=\frac{1}{2}v_1=\frac{1}{2}\operatorname{tg}\alpha_1$. But, since $v_{t=0}=\frac{E_a}{\tau_{зар}}$, then this requires that capacitor charging time constant $\tau_{зар}=CR_a$ be increased by a factor of 2. An increase for this reason in resistance R_a will lead to an undesirable change in level $U_{c\,нач}$. Therefore, it is advisible to increase capacitor C capacitance by a factor of 2.* Consequently, it is necessary accordingly to change magnitude C simultaneously with a change in control pulse

*Even though time constant $\tau_{разр}=CR_{io}$, i. e., circuit recovery time, will rise here.

duration during the scale switch. If here $\frac{t_{y1}}{\tau_{зар1}} = \frac{t_{y2}}{\tau_{зар2}}$, then nonlinearity factor $\gamma_н = \frac{t_н}{\tau_{зар}}$ will not change.

EXERCISE IX.5

a) Diode D_2 is a lower zero clamp and is intended to stabilize the initial level of diode L_1 cathode potential, i. e., of value $U_{c\,нач}$.

b) Resistance $R_з$ must be as small as possible to reduce circuit recovery time $t_в$ and decrease level $U_{c\,нач}$. But, the requirement to satisfy the /499 condition for undistorted input pulse transmission across isolating circuit $\tau = C_p R_з \gg t_н$ constrains the ability to decrease this resistance. In addition, a resistance $R_з$ decrease loads the input pulse generator.

c) Control pulse amplitude must be sufficient for reliable diode L_1 blanking during the entire working stroke. Control pulse amplitude must satisfy the condition $U_{з1} > U_{c\,нач}$ since diode plate potential rises to value $U_{а\,нач} = U_{c\,нач}$. by the end of the working stroke.

EXERCISE IX.6

The following expression describes the law of capacitor voltage rise during a working stroke for the Figure IX.9 GPN circuit

$$u_C = U_г + (E_а - U_г)\left(1 - e^{-\frac{t}{\tau_{зар}}}\right).$$

where $\tau_{зар} = R_а C$ -- charging network time constant.

The working stroke ends when voltage u_C attains firing potential $U_{c\,нач} = U_з$ when $t = t_н$, hence

$$U_з = U_г + (E_а - U_г)\left(1 - e^{-\frac{t_н}{\tau_{зар}}}\right).$$

Solving this equation for $t_н$, considering that $U_г \ll E_а$, we will get:

$$t_н = \tau_{зар} \ln \frac{E_а - U_г}{E_а - U_з} \approx \tau_{зар} \ln \frac{E_а}{E_а - U_з} = \tau_{зар} \ln \frac{1}{1 - \frac{U_з}{E_а}}.$$

The law for capacitor voltage decrease during a return stroke is described by $u_C = U_{c0} e^{-\frac{t}{\tau_{разр}}}$, where $\tau_{разр} = R_i C$ -- discharging network time constant. The return stroke ends when this voltage is reduced to quenching potential: $U_{C\,мин} = U_г$ where $t = t_в$, hence $U_г = U_{c0} e^{-\frac{t_в}{\tau_{разр}}}$. Solving this equation for $t_в$, we will get

$$t_в = \tau_{разр} \ln \frac{U_0}{U_г}.$$

Values $t_в$ and $t_р$ and, consequently, saw change period $T = t_в + t_р$ decrease, i. e., sweep frequency rises, when firing potential increases. Saw amplitude $U_п = U_0 - U_г$ drops, while nonlinearity factor $\gamma_н = \frac{t_г}{\tau_{разр}}$ decreases due to the reduction in working stroke duration.

Only value $t_в$ ($t_р$=const) is reduced when source voltage E_a arises, with sweep frequency rising as a result. Saw amplitude remains unchanged, while the nonlinearity factor decreases.

EXERCISE IX.7

a) Voltage drop $u_{упр} = -u_к = -i_{a2} R_к$ applied with a "minus" to the pentode control grid is created in the Figure IX.14a GPN circuit as capacitor C charges across pentode L_1 in resistance $R_к$. Capacitor voltage rises because of the charging process, while the voltage applied to the "TT" one-port drops ($u_C + u_{уп} = E_к$). Here, pentode plate current will strive to decrease. But, the current i_{a2} increase leads to a decrease in negative bias magnitude $u_{упр} = -u_к$, i. e., in pentode /500 internal resistance to d-c R_{io}, which, in turn, constrains the current decrease. As a result, pentode internal resistance to a-c R_i rises, pentode current stabilizes, and output linearity increases.

b) Connection of positive bias source E_{g1} to the pentode control grid network (Figure IX.14b) decreases pentode internal resistance to d-c, i. e., increases the average capacitor C charging current value. As a result, the capacitor charges at a high rate, which leads to a rise in saw amplitude $U_п$ and source voltage utilization factor ξ_a. Output voltage linearity remains as before since pentode internal resistance to a-c and, consequently, negative feedback action as usual determines its current-stabilizing action (see p. [illegible]).

EXERCISE IX.8

a) For the Figure IX.15 circuit, the approximate shape of the output voltage distortions arising due to noncoincidence of triode L_1 and L_2 blanking is depicted

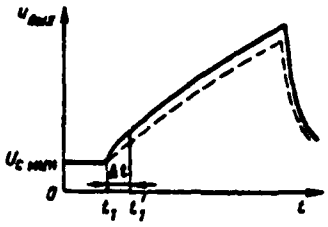


Figure X.50. Figure IX.19 GPN Circuit Output Voltage Distortions.

in Figure X.50. Here, t_1 -- moment the control pulse front blanks triode L_1, t_1' -- moment of triode L_3 blanking, while the dotted line depicts output voltage shape if these triodes were to be blanked simultaneously at moment t_1. Triode L_2 and L_3 currents flow across capacitor C in interval $\Delta t = t_1' - t_1$. Consequently, capacitor discharge occurs more rapidly than when triode L_3 is blanked (only with triode L_2 current). However, triode L_3 current gradually decreases in connection with the rise in the potential of upper capacitor C plate and triode L_3 cathode when its grid potential is clamped. Therefore, an exponential sector arises at the beginning of the working stroke (in interval Δt). At moment t_1', triode L_3 is blanked, capacitor C charging with stabilized triode L_2 current continues, and output voltage rises further by a linear law.

b) Triode L_3 grid potential rises (relative to "ground") when the Figure IX.15 potentiometer R_a arm is moved "upwards." Therefore, during resting times between control pulses, capacitor C_2 charging across triodes L_3 and L_1 will occur with more current and the average voltage u_{C2} level will rise. Capacitor C during a working stroke will be charged with greater current since this voltage plays the role of positive bias in the charging triode L_2 grid network. As a result, sawtooth voltage amplitude U_a and source voltage ξ_a utilization factor will rise. Nonlinear distortions at the beginning of the working stroke simultaneously will rise since a greater capacitor C voltage increment will be necessary due to the voltage U_a increase for triode L_3 blanking following triode L_1 blanking (the initial level of voltage $U_{c\,нач}$ in capacitor C remains unchanged).

EXERCISE IX.9

Pentode plate current radically decreases when $U_{c\ min} = U_{s\ min} < U_{s\ sp}$ (see Figure IX.11). As a result, the capacitor discharge rate at the end of a working stroke

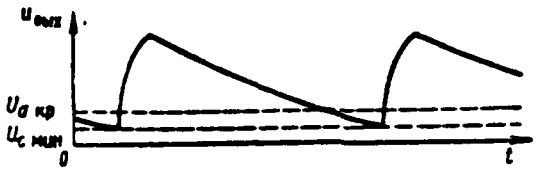


Figure X.51. Figure IX.16 GPN Circuit Output Voltage Distortions Where $U_{c\ min} < U_{s\ sp}$.

decreases. The approximate form of the output voltage distortions arising at this time is depicted in Figure X.51.

EXERCISE IX.10 /501

a) In the Figure IX.17b circuit, when the capacitor charges, the rise in voltage u_C, i. e., the potential of the resistance R right terminal, is transmitted across an amplifier with gain K = +1 and source E to the left terminal of this resistance. As a result, potential difference at the ends of resistance R and, consequently, the current flowing across it remain constant:

$$u_R = \text{const}, \quad i_1 = \frac{u_R}{R} = \text{const}$$

b) These curves are depicted in Figure X.52. Voltage u_C when capacitor C is charged from source E across a resistance rises along exponential curve a with time constant $\tau_{зар} = RC$, striving towards value E. When the capacitor charges in accordance with the Figure IX.17b circuit, based on the Figure IX.17d equivalent circuit, voltage u_C rises along exponential curve b with the equivalent time constant $\tau_1 = \frac{RC}{1-K}$, striving towards the equivalent voltage $E_э = \frac{E}{1-K}$. When K = 0.8, $\tau_э = 5\tau_{зар}$, $E_э = 5E$. Given identical working stroke duration $t_и$ = const, nonlinearity factor $\beta_н$ decreases by a factor of $s = \frac{1}{1-K}$, while voltage amplitude rises.

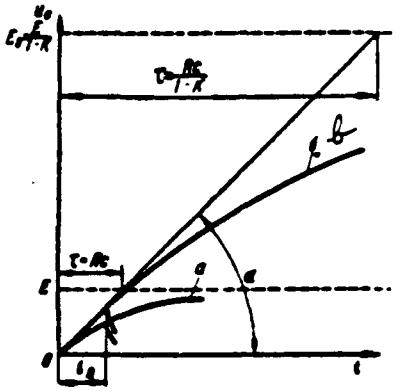


Figure X.52. Capacitor Voltage Curves When Charged Across Resistance R and Using Compensating Positive Feedback.

The rate of voltage rise at the beginning of the working stroke in both cases remains identical and equals

$$V = \frac{E}{\tau} = \frac{E_0}{\tau_0} = \operatorname{tg}\alpha.$$

EXERCISE XI.11

An increase in resistance R in the Figure IX.18 GPN circuit will lead to a proportional decrease in the initial levels of voltage $U_{c\,нач}$ and output voltage $U_{вых\,нач}$. In addition, capacitor C charging current during the working stroke, i. e., the rate of output voltage rise, and, consequently, its amplitude $U_л$ (where $t_л$ = const) will decrease accordingly. Output voltage linearity will rise /502 and the value of the nonlinearity factor $\varepsilon_л \approx \frac{t_л}{RC}(1-K)$ will decrease. The change in resistance R essentially will not be reflected in circuit recovery time $t_в$. Therefore, output voltage will correspond to Figure X.53 (R" = 2R').

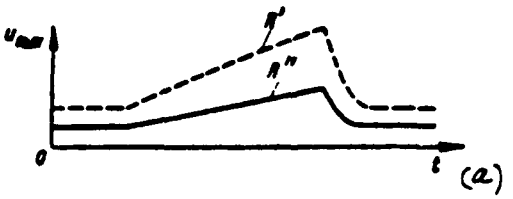


Figure X.53. Figure IX.18 GPN Circuit Output Voltage Change When Resistance R Increases (R" = 2R'). (a) -- Output voltage.

EXERCISE IX.12

a) When $R_k' = 0$ in the Figure IX.19 GPN circuit, capacitor C' voltage would turn out to be applied between triode L_2 grid and cathode $u_C' = u_{g2k}$, while triode L_2 grid current would arise during the capacitor C' charging process. Here, capacitor C' would turn out to shunted by slight resistance r_{g2k} and voltage linearity would be reduced radically.

If one assumes that $R_k' = 0$, the integrator input voltage $u_{вых2}'$ would be absent and, consequently, there would be no additional output voltage linearization.

b) Rapid capacitor C" discharge occurs across diode D_2 during resting times between control pulses. This explains the strict clamping of the voltage $u_{C\,min}'$ initial level. Capacitor C" would discharge across large resistance R_2 if this diode is absent, which would lead to an increase in circuit recovery time.

EXERCISE IX.13

a) For the Figure IX.20b equivalent integrator circuit, a capacitor charging current decrease $i_C = i_R$ occurs due to the amplifier input voltage u_{g2} rise counteracting source voltage E: $i_R = \frac{E - u_{g2}}{R}$. It is possible to explain the stabilization of this current and, consequently, linearization of the output voltage in this circuit in the following manner. We will assume that the potential of the capacitor C left plate (point g) rose by magnitude Δu_{g2} during the capacitor charging process. Then the potential of the C right plate (point a) will decrease by magnitude $\Delta u_{вых2} = -K\Delta u_{g2}$ as a result of amplifier action. The change in C plate potential difference will comprise

$$\Delta u_C = \Delta u_{g2} - \Delta u_{вых2} = \Delta u_{g2}(1 + K).$$

hence $\Delta u_{g2} = \frac{\Delta u_C}{1 + K}$. Consequently, increment Δu_{g2} corresponds to increment Δu_C less by a factor of 1 + K. Therefore, given sufficiently-great magnitude K, the u_{g2} changes during the C charging process will be insignificant and the current maintained is virtually constant and proportional only to source voltage E: $u_{g2} \approx 0$, $i_R \approx \frac{E}{R}$ = const. The decrease in the range of change of voltage /503

$u_{вх}$ and current i_R during a working stroke is equivalent by a factor of 1 + K to an identical increase in capacitor capacitance and, consequently, to the integrator time constant: $\tau_э = RC(1+K)$.

b) These curves are depicted in Figure X.54. Voltage u_C rises along exponential curve a with time constant $\tau = RC$, striving towards value E, as capacitor C charges

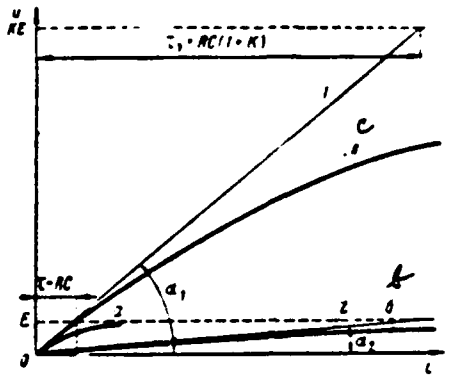


Figure X.54. Voltage u_C at R-C Integrator Output (a) and in the Integrator Circuit: at Amplifier Input $u_{вх}$ (b) and at Its Output $u_{вых}$ (c).

and from source E across resistance R. The rate of rise of this voltage at the beginning of a working stroke equals $V = \frac{E}{RC} = \operatorname{tg}\alpha_1$ (tangent 1), while the nonlinearity factor when $t_р \ll RC$ $\gamma_1 \approx \frac{t_р}{RC}$. It is convenient to use the Figure IX.20d equivalent integrator circuit to plot the curves of voltages $u_{вх}$ and $u_{вых}$. Voltage $u_{вх}$ rises along exponential curve b with equivalent time constant $\tau_э = RC(1+K)$, as usual striving towards value E. The rate that this voltage rises when t = 0 is less by a factor of 1 + K $V_{вх} = \frac{E}{RC(1+K)} = \operatorname{tg}\alpha_2$ (tangent 2), and linearity $\gamma_э = \frac{t_р}{RC(1+K)}$ rises accordingly during the identical working stroke duration. The range of the voltage $u_{вх}$ change during a working stroke decreases in comparison to an R-C integrator by a factor of K due to the decrease in rate $V_{вх}$.

Amplifier output voltage repeats the shape of the input voltage, but it is

inverted and amplified by a factor of K. Therefore, voltage $-u_{...}$ changes along exponential curve c with the same time constant τ_0, but will strive towards level KE. Consequently, the linearity of this voltage also increases by a factor of K: $\beta_n = \frac{t_3}{RC(K+1)}$, but the rate of its change rises by a factor of K and, just as was the case for exponential curve a, is determined by time constant $\tau = RC$: $v'_{max} = \frac{KE}{RC(K+1)} \approx \frac{E}{RC} = tg\beta_3$. The amplitude of the linearized sawtooth voltage rises accordingly when t_a = const.

c) For a circuit using positive feedback (Figure IX.17b) /504

$\beta_n' = \frac{t_3(1-K_1)}{RC}$ and $\beta_{n2} = \frac{t_3}{RC(1+K_2)}$ for one using negative feedback (Figure IX.20b). Comparing these expressions given identical t_a, R. and C values, we will get $1-K_1 = \frac{1}{1+K_2}$, hence for given value $K_1 = 0.95 : K_2 = \frac{1}{1-K_1} - 1 = \frac{1}{1-K_1} = 20$. Essentially, even one amplifying stage with a pentode plate load makes it possible to obtain a significantly higher K_2 value. This is explained by the fact that sawtooth voltage linearity when negative voltage feedback is used may be significantly better than when positive feedback is used.

EXERCISE IX.14

Resistance R in the pentode control grid network and capacitor C connected between its plate (amplifier output) and control grid (amplifier input) are integrator network elements in the Figure IX.21 GPN circuit. The feedback network connects amplifier output with its input across capacitor C. Feedback is negative since amplifier plate and grid voltages change opposite in phase and any change in plate voltage transmitted across capacitor C to the control grid will counteract the cause of this change. The pentode control grid across resistance R is connected to plate voltage source $+E_a$, which also plays the role of constant input voltage E in the Figure IX.20b integrator circuit. Consequently, output voltage working stroke is obtained through voltage $+E_a$ integration.

EXERCISE IX.15

a) The magnitude of the plate and control grid voltage negative step at the moment of triggering $-\Delta U_{a1} = -\Delta U_{g11}$ may be determined from the following

circumstances. When the pentode is unblanked with respect to plate current, both plate load current and capacitor recharging current $i_a = i_{Ra} + i_C$ will pass across it. At the moment of triggering, voltage drop ΔU_{a1} across resistance R_a and voltage drop $E_a + \Delta U_{g11} = E_a + \Delta U_{a1}$ across resistance R arise with a jump (due to the ΔU_{g11} negative jump, the potential difference in resistance R increases). Therefore, after the step, plate load current, capacitor recharging current, and complete plate current, respectively, will equal:

$$I_{Ra} = \frac{\Delta U_{a1}}{R_a}; \quad I_C = \frac{E_a + \Delta U_{a1}}{R}; \quad I_a = \frac{\Delta U_{a1}}{R_a} + \frac{E_a + \Delta U_{a1}}{R}.$$

But, the plate current value found may also be expressed using transfer characteristic slope and control grid voltage resulting after the step:

$$I_a = S(|E_{g1}| - \Delta U_{g11}) = S(|E_{g1}| - \Delta U_{a1}).$$

Consequently,

$$\frac{\Delta U_{a1}}{R_a} + \frac{E_a + \Delta U_{a1}}{R} = S(|E_{g1}| - \Delta U_{a1}).$$

hence

$$\Delta U_{a1} = \frac{|E_{g1}| - E_a/SR}{1 + 1/SR + 1/SR_a}.$$

When resistance R and R_a values are sufficiently great, it is possible /505 to disregard the second term in the numerator and the second and third terms in the denominator. Then we will get

$$\Delta U_{a1} \approx |E_{g1}|$$

b) A contradiction is only apparent. Actually, in accordance with (IX.34), pentode gain must be infinitely great for precise capacitor C discharging current stabilization at the operating stage, i. e., for ideal output voltage linearization. But, where $K = \frac{\Delta u_a}{\Delta u_{g1}} = \infty$, finite plate voltage changes are obtained for infinitely-small control grid voltage increments, i. e., where $u_{g1} \approx$ const. Actually, gain always is finite. Therefore, a voltage u_a decrease must be accompanied by a voltage u_{g1} increase, i. e., by a decrease in discharging current $I_C = \frac{E_a - u_a}{R}$,

which also is the reason for disruption in output voltage linearity. The greater the K value, the higher the current i_c constancy, the smaller boundaries within which voltage u_{g1} changes during a working stroke, and the higher the output voltage linearity.

c) The curve of the voltage which would result in cathode load impedance $R_к$ is depicted in Figure X.55. This voltage equals $u_к = i_к R_к$ and repeats the

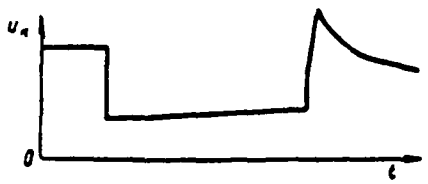


Figure X.55. Resistance $R_к$ Voltage Curve in the Figure IX.21 GPN Circuit.

law of cathode current change and, consequently, pentode control grid voltages (see Figure IX.21e). But, voltage $u_к$ always will be positive since cathode current never equals zero and passes across resistance $R_к$ only in one direction--from cathode to chassis. Thus, a negative-polarity pulse would be shaped in resistance $R_к$ during a working stroke. This circumstance, as will be explained below, is used in a cathode-coupling phantastron.

EXERCISE IX.16

a) Diode D_2 clamps initial output voltage at level $U_0 < E_к$ in the Figure IX.23 GPN circuit. Diode current passes along the network $+E_a$, resistance R_a, diode D_2, "lower" portion of resistance $R_к$, chassis $(-E_a)$.

Considering that diode D_2 is unblanked only when pentode L_1 is blanked with respect to plate current and disregarding slight resistance $R_к$, it is possible to represent the diode connection circuit as depicted in Figure X.56. It follows from this circuit that a parallel upper diode limiter with positive clipping threshold $E_к = U_0 > 0$ actually is formed with the help of clamping diode D_2.

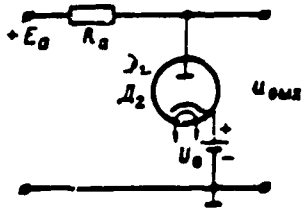


Figure X.56. Clamping Diode Circuit Connection Per Figure XI.23.

б) The great control pulse amplitude in the Figure IX.21а circuit (without clamping diode) is stipulated by the requirement for complete pentode blanking with respect to plate current in the initial state. This requirement is lifted when a clamping diode is included in accordance with Figure IX.23 since the flow in the initial state of slight pentode plate current does not impact upon /506 initial output voltage level. Actually, if pentode plate current does not exceed value $I_a = \frac{E_a - U_0}{R_a}$, then pentode plate potential will be reduced due to the flow of this current to no more than value $E_a - I_a R_a = E_a - \frac{E_a - U_0}{R_a} R_a = U_0$, the clamping diode as usual will be unblanked, and it will place a bound on output voltage at given level U_0. Therefore, control pulse amplitude may be decreased essentially by a factor of 1.5—2 when the clamping diode is used.

EXERCISE IX.17

If triode L_2 in the Figure IX.24 GPN circuit lost emission, then the capacitor C right plate will turn out to be cut off from pentode plate, i. e., the negative feedback network will be broken. Therefore, the GPN circuit will turn out to be disrupted and there will be no sawtooth voltage shaped at pentode plate (in spite of its continuity). The curves of the voltages in the circuit for this instance are depicted in Figure X.57. Control pulses unblanking the pentode with respect to the third grid will be inverted in the plate network. Voltage u_{g1} essentially will be constant and equal cathode potential ($u_{g1} \approx 0$) due to grid limiting in resistance R. No current will flow across capacitor C and resistance R_a so there will be no output voltage.

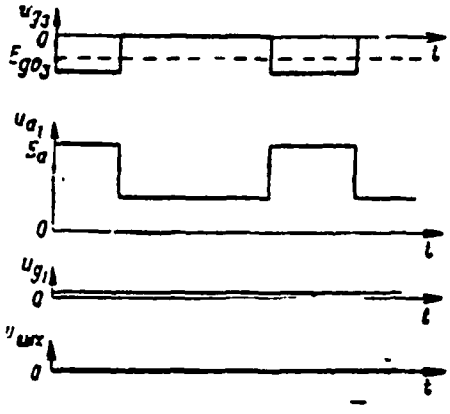


Figure X.57. Figure IX.24 GPN Circuit Voltage Curves Given a Cathode Follower Malfunction.

EXERCISE IX.18

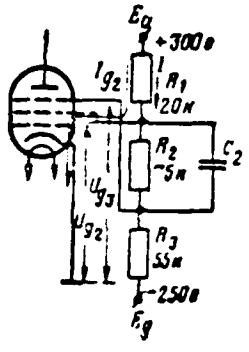


Figure X.58. Circuit Supplying Initial Grid Potentials g_2 and g_3 in a Monostable Screen Grid Coupling Phantastron.

a) The circuit supplying initial phantastron second and third grid potentials depicted in Figure IX.25 is shown separately in Figure X.58 for the given parameters.

We will consider that capacitance C_2 does not exert any influence whatever on distribution of constant potentials, the second poles of supply sources E_a and E_g are connected to "ground" (chassis), and these sources are matched. We will examine closed loop source E_a--resistance R_1--resistance R_2--resistance R_3--source E_g--"ground" ($+E_a$, $-E_a$). Current I will flow (from E_a to E_g), along with

current I_{g2} flowing only across resistance R_1, is this loop. Therefore, based on Kirchhoff's second law /507

$$E_a + E_g = (I_{g2} + I) R_1 + IR_2 + IR_3.$$

hence

$$I = \frac{E_a + E_g - I_{g2}R_1}{R_1 + R_2 + R_3}.$$

or, for given values E_a, E_g, R_1, R_2, R_3, and I_{g2}

$$I = \frac{300 + 250 - 3 \cdot 10^{-6} \cdot 20 \cdot 10^6}{(20 + 75 + 55) 10^3} \approx 0.00327 \text{ a} = 3.27 \text{ mA}.$$

To compute voltage U_{g2}, we will examine this closed loop source E_a--resistance R_1--second grid--"ground" ($-E_a$). In accordance with Kirchhoff's second law, for the second loop

$$E_a = (I + I_{g2}) R_1 + U_{g2}.$$

hence

$$U_{g2} = E_a - (I + I_{g2}) R_1.$$

or

$$U_{g2} = 300 - (3 + 3.27) \cdot 10^{-6} \cdot 20 \cdot 10^6 = 175 \text{ V}.$$

To compute voltage U_{g3}, we will examine closed loop "ground" ($+E_g$)--third grid--resistance R_3--source E_g. In accordance with Kirchhoff's second law, for this loop considering voltage polarity relative to "ground"

$$-E_g = U_{g3} - IR_3.$$

hence

$$U_{g1} = -E_g + IR_1$$

or

$$U_{g1} = -250 + 3{,}27 \cdot 10^{-3} \cdot 55 \cdot 10^3 = -70 \text{ V}.$$

(the pentode is blanked with respect to plate current).

b) For the Figure IX.25 phantastron circuit, the working stroke begins at the moment of triggering and ends when linearly-falling pentode plate voltage attains minimum value $U_{a\,min} = U_{a\,p}$. Therefore, the duration of the working stroke generated by the circuit equals the maximum duration of the working stroke for the Figure IX.21 circuit and is determined by ratio (IX.42) $t_a = RC$.

c) It is possible to increase either resistance R or capacitance C in order to increase interval t_a. In accordance with (IX.39), either will lead to a decrease in the rate of the plate voltage drop across the linear sector and, since values $U_{a\,max} = E_a$ and $U_{a\,min} = U_{a\,p}$ remain as usual, to a rise in value t_a. However, a capacitance C increase will lead to a rise in recovery time (IX.45): $t_в \approx 3CR_a$. A change in resistance R magnitude (just as that of capacitance C) will not impact upon output voltage linearity. Actually, in accordance with (IX.34), the nonlinearity factor equals $\beta_a = \frac{t_a}{RC(K+1)}$ or, when $t_a = RC$

$$\beta_{a\,нелс} = \frac{1}{1+K}.$$

d) The circuit for a monostable screen grid coupling phantastron with cathode follower and triggering with respect to the plate network is depicted in Figure X.59. Trigger pulses are supplied to plate across transient capacitor C_1 and must be of negative polarity. In this event, a negative pulse transmitted across cathode follower L_2 and capacitor C from plate to pentode control grid elicits a reduction in cathode and screen currents. The latter will lead to a "bump" /508 in voltage u_{g2} transmitted across capacitor C_2 to suppressor grid, causing the

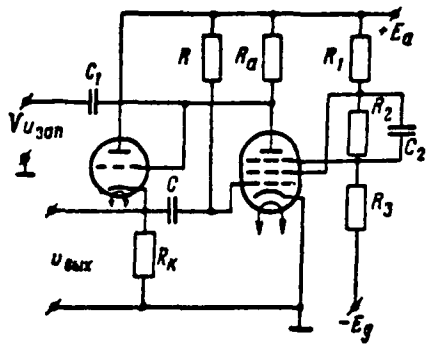


Figure X.59. Monostable Screen Grid Coupling Phantastron With Cathode Follower and Plate Network Triggering.

pentode to unblank with respect to plate current, i. e., circuit triggering. (A negative pulse of voltage u_{g3} arises when a positive-polarity pulse is supplied to plate and circuit triggering will not occur.

A trigger pulse transmitted from control to screen grid is amplified, with simultaneous inversion by a factor of $K_0 = -\frac{\Delta u_{g2}}{\Delta u_{g1}}$ in the screen grid network. Therefore, the amplitude of the negative trigger pulses supplied to plate may be less by a factor of K_0 than that of positive pulses supplied directly to suppressor grid.

EXERCISE IX.19

a) Although plate voltage in a variable delay circuit is not used also as output voltage, it is its linearity that provides linear coupling of control voltage changes and delay time (IX.50). This clearly can be seen by examining Figure IX.26c.

b) We will get $t_з = \frac{U_з}{V}$ from ratio $\frac{U_з}{t_з} = V$ or, since, in accordance with (IX.52), saw amplitude equals

$$U_з = u_{упр} - \Delta U'_{з1} - U_{з\,упр}$$

then

$$t_з = \frac{u_{упр}}{V} - \frac{\Delta U_{з1} + U_{з\,упр}}{V}.$$

Since ΔU_{al} = const and $U_{a\,sp}$ = const, then the second term on the right side of this expression is a constant magnitude and, for control voltage increments, we will get $\Delta t_3 = \frac{1}{V}\Delta u_{ymp}$. Comparing these this equality with equality (IX.50), we will see that the delay control slope is a magnitude op ite to saw slope: $K_3 = \frac{1}{V}$. But, in accordance with (IX.39) $V = \frac{E_a}{RC}$ and

$$K_3 = \frac{RC}{E_a}.$$

c) Maximum delay time will be obtained when the arm of potentiometer /509 R_4 in Figure IX.26a is shifted to the extreme "upper" position, when $u_{ymp} = U_{gr\,max} = E_a$. Here, resultant working stroke duration will be identical to that in a phantastron with a clamping diode: $t_{3\,max} = t_{5\,max} = RC$. Control voltage and delay time decrease when the potentiometer R_4 arm is shifted "downwards." Minimum delay time equals zero and will be obtained for value $U_{ymp\,min} = \Delta U_{a1} + U_{a\,sp}$. when $t_3 = 0$.

Resistance R_5 is included to place a lower control voltage bound at level $U_{gr\,min} > 0$. In addition, if this resistance is absent, then given the "lower" potentiometer R_4 arm position, the trigger pulse supply network across transient capacitor C_1 would turn out to be shorted and the circuit would not trigger.

d) The presence of stray capacitances shunting plate--cathode and grid--cathode paths will lead to stretching of the plate voltage steps at the beginning and

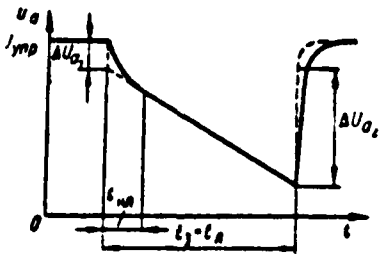


Figure X.60 Stray Capacitance Impact Upon Variable Delay Circuit Plate Voltage Shape.

end of the working stroke (Figure X.60). Stretching of the negative-going pulse arising at the moment the circuit triggers leads to onset of an interval of plate voltage $t_{н.з}$ nonlinearity immediately following triggering. Proportional relationship (IX.50) will be disrupted in this interval, i. e., for slight delay time values $t_з < t_{н.з}$.*

Positive-going pulse u_a stretching upon conclusion of the working stroke leads to a slight circuit recovery time increase.

e) Diode current and, consequently, the voltage drop across resistance R_a will decrease, i. e., a positive plate voltage pulse will arise, when a positive pulse acts upon diode D_1 cathode. This pulse will be transmitted across cathode follower L_2 and capacitor C to pentode L_1 control grid and will cause a cathode current "bump" and, consequently, screen grid current (there is no plate current since the pentode is blanked with respect to the third grid). The current I_{g2} "bump" will create a negative voltage u_{g2} pulse, which will be transmitted across capacitor C_2 to the third grid and across differentiating network capacitor C_3 to circuit output. Thus, a phantastron will not be triggered by positive trigger pulse action and a negative pulse will arise directly at the moment of "triggering" (this corresponds to false value $t_3 = 0$), regardless of the value of the control voltage at circuit output. Therefore, it is inadmissible to supply positive pulses to circuit input.

EXERCISE IX.20

These curves are depicted in Figure X.61a-d, respectively.

a) Capacitor C charging time constant $\tau_{зар} = CR_a$, i. e., circuit recovery time $t_в = 3\tau_{зар}$, rises when resistance R_a increases. Output voltage will not succeed in attaining level E_a by the start of the subsequent cycle (moments t_1) since the duration of the nonoperating portion of the period does not change ($t_{раб.макс} = C_1(R_3 + r_{ген})$ = const). Therefore, maximum saw level amplitude and stability will decrease. Working stroke and oscillation period will be reduced due to the reduction in level $U_{в.макс}$. On the other hand, a resistance R_a increase will

*Boosting capacitance C_2 reduces the nonlinearity interval to several usec.

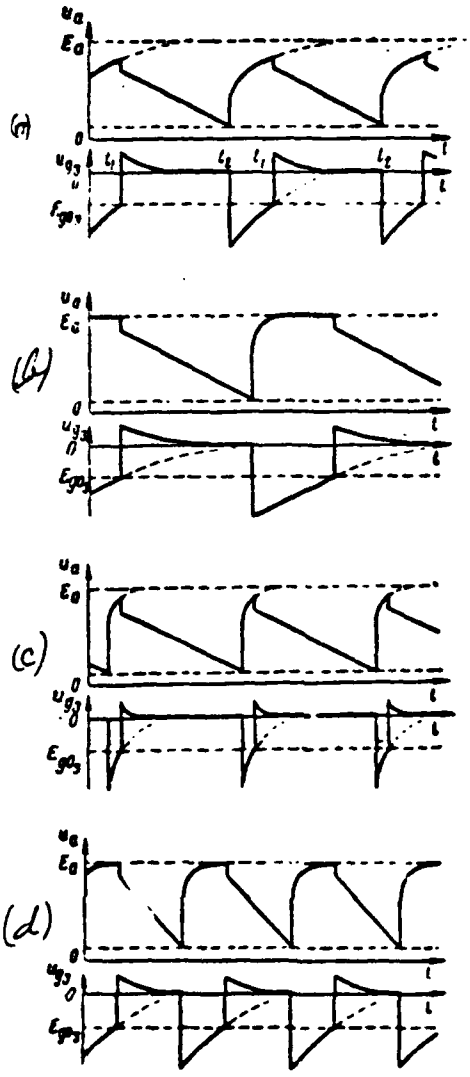


Figure X.61. Free-Running Screen Grid Coupling Phantastron Voltage Curves Where Circuit Parameters Change.

lead to a rise in pentode gain $K \approx SR_a$ (if the transfer characteristic slope /510 decrease still has not manifested itself). As a result, the capacitor C equivalent discharging time constant $\tau = RC(K+1)$ will rise, i. e., output voltage linearity will deteriorate.

b) Capacitor C_2 charging and discharging time constants $\tau_{зар3}=C_2(R_{e3}+R_3)$, $\tau_{разр3}=C_2(R_3+r_{раз3})$ will rise when resistance R_3 increases. As a result of this, the rate of voltage u_{g3} exponential changes will decrease following positive and negative steps.

Stretching of the negative exponential sectors of voltage u_{g3} will lead to pentode blanking with respect to suppressor grid for a longer time and duration of the nonoperating portion of the period will rise. Thus, period of oscillations will rise, i. e., their frequency will decrease. Maximum saw level stability will deteriorate due to more complete capacitor C charging. Stretching of voltage u_{g3} positive exponential sectors will lead to working stroke linearity deterioration in most of its sector. Otherwise, output voltage parameters do not change.

c) A decrease in capacitor C_2 capacitance will lead to a proportional decrease in its charging and discharging time constants, i. e., to a rise in the rate of voltage u_{g3} exponential changes following positive and negative steps. The pentode will be blanked with respect to the suppressor grid for a shorter time as a result of acceleration of capacitor C_2 discharge, i. e., the duration of the nonoperating portion will be reduced. Output voltage will not attain level E_a since /511 capacitor C does not succeed in discharging during the short time ($\tau_{разр}$ = CR_a = const). Therefore, saw amplitude and working stroke duration will decrease. The period of oscillations will decrease, while the frequency will rise. Output voltage linearity will deteriorate in a lesser initial sector as a result of the acceleration of the capacitor C_2 charge.

d) A resistance R decrease will lead to a proportional rise in the capacitor C discharge rate $\left(V \approx \frac{E_a}{RC}\right)$, i. e., to an increase in output voltage operating sector transconductance. Working stroke duration will decrease by an identical factor since maximum and minimum output voltage levels will remain unchanged. Oscillation frequency will rise accordingly. Output voltage linearity will remain as usual (without consideration for the influence of positive voltage u_{g3} excursions) since, at the same time magnitude t_a changes, time constant τ = RC(K+1) will change by the same factor and nonlinearity factor $\varepsilon = \frac{t_a}{RC(K+1)}$ will not change.

An increase in operating sector transconductance will lead to more precise registration of the moments of working stroke cessation t_2 due to the increase

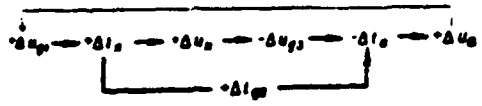
in the angle at which linearly-falling voltage intersects level $U_{зап}$. Therefore, oscillation period stability will improve.

EXERCISE IX.21

a) Resistance R_4 in the Figure IX.29 phantastron circuit decreases pentode gain with respect to the plate network. As a result of this, equivalent time constant $\tau_э = RC(1+K)$ decreases, while nonlinearity factor $\beta_н = \frac{t_и}{RC(1+K)}$ rises.

Therefore, plate voltage linearity in a cathode-coupling phantastron is not as good as it is in a screen grid coupling phantastron.

b) It is possible to depict the avalanche-like process in a cathode-coupling phantastron at the moment the operating stage ceases (when plate voltage attains value $U_{зап}$) symbolically in the following form:



c) This circuit is depicted in Figure IX.62. Delay time is controlled just

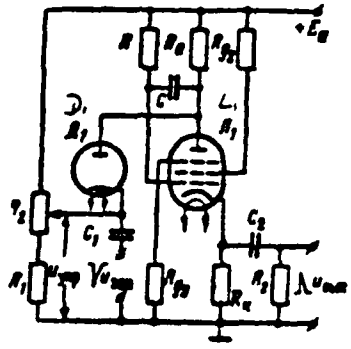


Figure X.62. Cathode-Coupling Phantastron Used as Variable Delay Circuit.

as it was in the Figure IX.26 circuit due to the change in the initial plate voltage level $U_{зап} = u_{гр0}$.

Positive-polarity delayed pulses are obtained through network C_2R_2 differentiation of the droop of the negative pulse shaped in resistance R_4 (see Figure IX.29c).

EXERCISE IX.22

a) These coil current curves are depicted in Figure X.63a and the coil voltage curves corresponding to them are plotted in Figure X.63b (the dotted line repeats the Figure IX.30 curves).

The rate of the current rise during a working stroke is increased by a factor of 2 if working stroke duration is increased by a factor of 2 $\left(t_4' = \frac{1}{2} t_4\right)$. Therefore, the voltage u_4 blanking level height and the steepness of its sloping sector /512 will be increased by a factor of 2. Obtaining the corresponding changes in the shape of the Figure IX.31 generator output voltage while retaining similarity condition (IX.58) and value U_{4max} requires that resistance R be increased and capacitance C be decreased by the identical factor. Control pulse duration must be decreased by a factor of 2.

The rate of current rise will decrease by a factor of 2 if working stroke duration is increased by that factor $(t_4'' = 2t_4)$.

Therefore, voltage u_4 blanking level height and the steepness of its sloping sector will decrease by a factor of 2. Accordingly, resistance R in the generator circuit should be decreased, while capacitance C should be increased. Control pulse duration must be increased by a factor of 2.

b) Generator output voltage curves for $R' < R$ and $R'' > R$ when t_4 = const are depicted in Figure X.63c (the dotted line repeats the Figure IX.31 curve). A resistance R decrease provides a decrease in blanking level height, a rise in the steepness of the sloping sector, and recovery time reduction; the opposite occurs when resistance R is increased.

EXERCISE IX.23

a) A recovery time decrease requires a capacitance C magnitude decrease

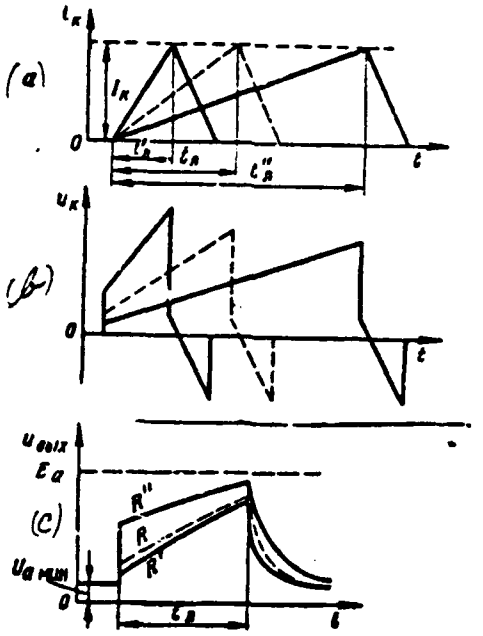


Figure X.63. For Exercise IX.22.

(see IX.68a). But, given a slight capacitance magnitude, the rate of ouptput voltage change and thereby amplitude, for the given switching pulse duration, significantly will depend upon the temperature-unstable current $I_{к0}$ magnitude (see IX.60).

b) The safe duty ratio magnitude determined as $Q = \frac{t_и + t_п}{t_и}$ may be /513 computed if resting time duration $t_п$ equals circuit recovery time $t_в$. Formula (IX.68a) must be used to determine magnitude $t_в$.

Current gain β magnitude in this formula will be found from collector characteristics and input current $I_б = \frac{E_к}{R_б}$, while sawtooth voltage amplitude is determined in accordance with (IX.65).

Answer: Q = 3.5.

EXERCISE IX.24

Source voltage E magnitude impacts upon emitter current magnitude and, consequently, also on average discharging current value $I_{cp} = \frac{I_{1ст} + I_{2ст}}{2}$ (Figure IX.38). Therefore, in accordance with (IX.73), source voltage E magnitude impacts upon sawtooth voltage amplitude.

EXERCISE IX.25

There can be no collector T_1 saturation mode if resistance $R_к$ is absent from the collector T_1 network. The voltage between transistor T_1 collector and emitter will change significantly when temperature changes. Consequently, the initial capacitor C voltage value will change.

Therefore, the transistor T_1 saturation mode, including resistance $R_к$ in the collector network, is used for voltage U_{co} temperature stabilization. Selected resistance $R_к$ magnitude is such that the voltage drop across it in the initial state will not exceed 2—3 V.

EXERCISE IX.26

Recovery time will be small if, first, the transistor T_1 bottoming mode is used and, second, the smallest possible resistance $R_б$ magnitude is selected.

Transistors with a high α value should be used to increase the emitter follower transfer constant and input resistance. Use of composite transistors in the emitter follower provides good results.

EXERCISE IX.27

The collector voltage step is not compensated for since the amplifier turns out to be blanked when the switching pulse ceases.

CHAPTER XI /514

ATTACHMENTS

ATTACHMENT 1

1. Pulse Signal Frequency Spectra*

A pulse signal may be represented as the sum of the harmonic functions of time--cosinusoidal and sinusoidal components.

The combination of these components is called the frequency spectrum and the individual components are called harmonics.

An infinite trigonometric Fourier series determines the frequency spectrum of a periodic video pulse train (I.2) and, for pulses of unit amplitude (U = 1 V), may be written in the form

$$f(t \pm nT_{\text{п}}) = U_{\text{ср}} + \sum_{k=1}^{\infty} U_k \cos(K\Omega_{\text{п}} t - \varphi_k). \qquad \text{(XI.1)}$$

*The strict spectra theory is presented in widespread special literature (see L-5 for example).

**Where U = 1 V and $U_{\text{п}} = f(t)$.

where $U_{=}$ -- d-c component equal, in accordance with (I.5) $U_{=} = \frac{1}{T_и}\int_0^{T_и} f(t)\,dt$;

$\Omega = 2\pi F_и = \frac{2\pi}{T_и}$ -- angular pulse repetition frequency [PRF];

K -- harmonic number;

$U_к$ -- amplitude;

$\varphi_к$ -- initial phase of the k-th harmonic.

Its K number determines the frequency of each spectrum harmonic and equals $\Omega_к = K\Omega_и$; the first (fundamental) harmonic with frequency $\Omega_1 = \Omega_и$ corresponds to value K = 1; the second harmonic with frequency $\Omega_2 = 2\Omega_и$ corresponds to value K = 2, and so on. Thus, the spectrum of a periodic train of video pulses will comprise an infinitely-large number of harmonics, whose frequencies are the squares of the PRF. Since it will not comprise harmonics of other frequencies in this spectrum, it is a discrete (line) spectrum, while the frequencies of any two adjacent harmonics are separated by interval $\Delta\omega_к = \Omega_и$.

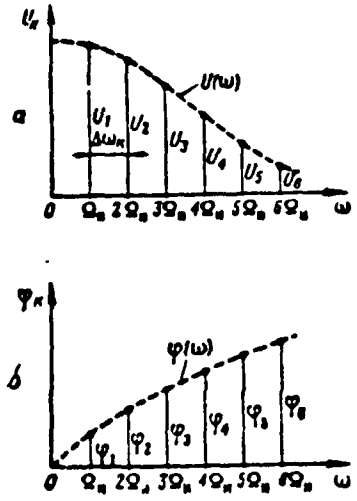


Figure 1. Approximate Form of the Amplitude (a) and Phase (b) Spectra of a Periodic Train of Video Pulses.

The approximate form of the amplitude spectrum (combination of harmonic amplitudes) and phase spectrum (combination of harmonic initial phases) of a periodic train of video pulses is depicted in Figure 1.

The concept of the complex amplitude of the k-th harmonic $\dot{C}_k = C_k e^{-j\varphi_k}$ usually is used to determine harmonic amplitudes and initial phases.

A complex amplitude is expressed by pulse signal parameters with integral ratio

$$\dot{C}_k = \frac{2}{T_u}\int_0^{T_u} f(t)\, e^{-jk\Omega_u t}\, dt. \qquad \text{(XI.2)}$$

It is more convenient to determine the continuous envelope of complex /515 amplitudes as a function of the current value of frequency ω instead of computing complex amplitudes C_k (i. e., values C_k and φ_k):

$$\dot{C}(\omega) = C(\omega)\, e^{-j\varphi(\omega)} = \frac{2}{T_u}\int_0^{t_u} f(t)\, e^{-j\omega t}\, dt. \qquad \text{(XI.3)}$$

Modulus $C(\omega)$ and argument $\varphi(\omega)$ of this expression are the envelopes of the amplitude and phase spectra, respectively (dotted lines in Figure 1.). Finding these envelopes and knowing PRF ω_u, it is possible when necessary simply to establish the internal spectrum structure: the ordinates of functions $C(\omega)$ at points $k\omega_u$ will provide the amplitude values of individual harmonics C_k, while the ordinates of functions $\varphi(\omega)$ at these same points will provide the values of their initial phases φ_k.

We will note that, in accordance with expression (3), where $\omega = 0$

$$\dot{C}(0) = C(0) = \frac{2}{T_u}\int_0^{T_u} f(t)\, dt = 2U_{=} \qquad \text{(XI.4)}$$

Pulse duration usually is limited at the zero level and, since f(t) = 0 during resting times, it is sufficient to accomplish integration in expressions (XI.2) and (XI.3) only within the limits of pulse duration t_u :

$$\dot{C}(\omega) = \frac{2}{T_u}\int_0^{t_u} f(t)\, e^{-j\omega t}\, dt. \qquad \text{(XI.5)}$$

As an example, we will find the spectrum of a periodic train of square pulses

with a unit amplitude. For a square pulse, representing it in the form of a precise function of time in accordance with Figure I.2 we have

$$f(t) = \begin{cases} 1 \text{ where } -\frac{t_и}{2} < t < +\frac{t_и}{2}, \\ 0 \text{ the rest of the time} \end{cases} \qquad \text{(XI.6)}$$

Therefore, based on expression (XI.5), we will get

$$\dot{U}(\omega) = \frac{2}{T_и} \int_{-\frac{t_и}{2}}^{+\frac{t_и}{2}} e^{-j\omega t}\, dt = \frac{2}{j\omega T_и}\left(e^{j\omega\frac{t_и}{2}} - e^{-j\omega\frac{t_и}{2}}\right) = \frac{4}{\omega T_и}\sin\frac{\omega t_и}{2}^{*},$$

or, using ratios $T_и = Qt_и$, $\omega = 2\pi f$ (Q -- duty ratio, f -- current frequency value in Hertz): /516

$$U(f) = \frac{2}{Q}\,\frac{\sin \pi f t_и}{\pi f t_и}. \qquad \text{(XI.7)}$$

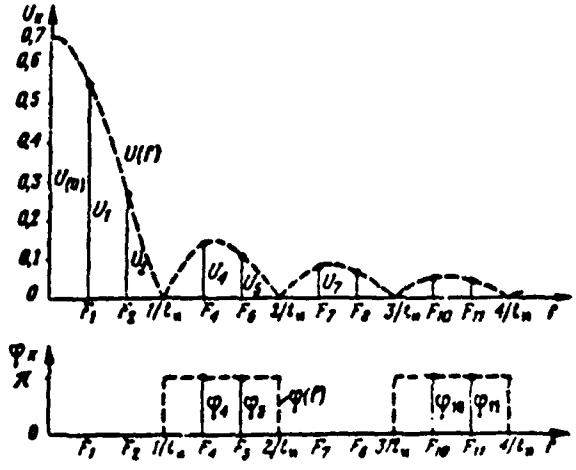


Figure 2. Amplitude (a) and Phase (b) Spectra of a Periodic Train of Square Video Pulses with Unit Amplitude with Q = 3.

A graph of modulus U(f) and argument $\phi(f)$ of this function for value Q = 3 are depicted by dotted lines in Figure 2.

*Based on the Euler formula, $\frac{e^{j\alpha} - e^{-j\alpha}}{2j} = \sin\alpha$.

The first graph shows that the spectrum harmonic amplitude envelope decreases non-monotonously with a rise in frequency, periodically reverting to zero at points $f = \frac{m}{t_и}$ (m = 1, 2, 3, . . .).

The second graph demonstrates that harmonic initial phases change with a jump by π at these same points.*

Since PRF $F_п = \frac{1}{T_п} = \frac{1}{Qt_и}$, then the first harmonic frequency is $F_1 = F_п = \frac{1}{3t_и}$ when Q = 3; the second is $F_2 = 2F_п = \frac{2}{3t_и}$; the third is $F_3 = 3F_п = \frac{1}{t_и}$, which coincides with the point at which the spectrum envelope reverts to zero for the first time; the fourth is $F_4 = 4F_п = \frac{4}{3t_и}$, and so on. Consequently, the third, six, and other multiple-three harmonics are absent in the spectrum.

We will investigate the part various spectrum components play in shaping the initial pulse train.

To do so, we will determine and sequentially sum the d-c component just for the first four harmonics of the spectrum found. In accordance with Figure 2 graphs (or with direct substitution of corresponding frequency values $F_k = KF_п$ into /517 expression (XI.7)), we will get: U(0) ≈ 0.66; U_1 ≈ 0.55; Φ_1 ≈ 0; U_2 ≈ 0.27, Φ_2 = 0; U_3 = 0; U_4 ≈ 0.14, $\Phi_4 = \pi$. Consequently, considering (XI.4), the d-c component equals $U_- = \frac{U(0)}{2} \approx 0.33$, while, in accordance with (XI.1), the expressions for the first, second, and fourth harmonics (the third harmonic is absent) will be written in the form

$$u_1 = U_1 \cos(\Omega_п t - \varphi_1) = 0.55 \cos 2\pi F_1 t = 0.55 \cos \frac{2\pi}{T_п} t;$$

$$u_2 = U_2 \cos(2\Omega_п t - \varphi_2) = 0.27 \cos 2\pi F_2 t = 0.27 \cos \frac{4\pi}{T_п} t.$$

$$u_4 = U_4 \cos(4\Omega_п t - \varphi_4) = 0.14 \cos(2\pi F_4 t - \pi) = -0.14 \cos \frac{8\pi}{T_п} t.$$

Serial summing of these components is done in Figure 3. The d-c component, the first harmonic, and their sum are depicted in Figure 3a. The second harmonic is added to this sum in Figure 3b. The fourth harmonic is added to the sum of the d-c component and the first two harmonics in Figure 3c. The initial train

*At points $f = \frac{m}{t_и}$ (m = 1, 2, 3, . . .), $\sin \pi f t_и = \sin m\pi = 0$ and changes sign.

of square pulses where Q = 3 is depicted in Figure 3d for evaluation of the result obtained.

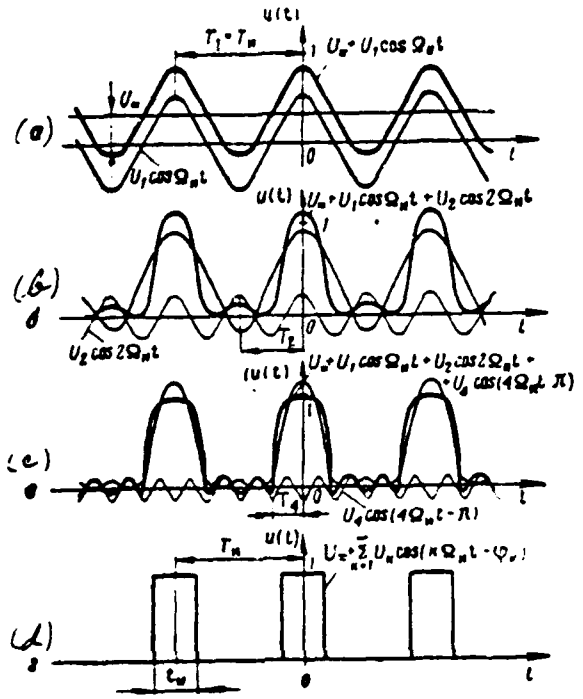


Figure 3. Reconstruction of a Periodic Train of Square Video Pulses with Q = 3 with Frequency Spectrum Component Summing.

It is now possible to draw the following conclusions. The d-c component, /518 as already demonstrated above, determines only the average pulse signal value for the period and does not impact upon pulse shape (should it be absent, the entire signal would only shift "downwards" along the vertical by value U_-). The first harmonic provides a somewhat coarse framework for the pulse signal and determines PRF. Addition of the second harmonic increases pulse steepness and "frees" resting times, resulting already in formation of a smooth (almost bell-like) pulse train shape. The impact of the fourth harmonic, which acts opposite in phase to the first and second harmonics ($\Phi_4 = \pi$), manifests itself in a further increase in the rate of pulse rise, as well as in the flattening of their tilts. However, pulse shape after its addition still is far from square, and oscillating voltage remains in the resting times. Final pulse shaping, formation of vertical

porches and flat tilts, will occur due to all remaining spectrum harmonics we have not considered (fifth, seventh, eighth, tenth, and so forth). It is apparent that the shaping of radical pulse envelope breaks ("corners") and steep porches may result from action only of voltages changing rapidly over time--high-frequency harmonics. Consequently, precise reproduction of the pulse shape requires summation of the entire infinitely-large number of the harmonics of their spectrum.

We will explain briefly the overall relationships of envelope shape and spectrum structure to periodic pulse signal parameters using our example (see Figure 2).

It follows from expression (5) that only pulse shape f(t) and duration $\tau_и$ determine the form of the spectrum envelope and it will not depend on PRF $F_и$. Actually, due to factor $\frac{2}{T_и}$, when there is a change in frequency $F_и$ (repetition frequency $T_и = \frac{1}{F_и}$), the amplitude of all spectrum harmonics will change proportionally, as will the frequency interval $\Delta f_и = F_и$ between adjacent harmonics--spectral energy distribution. The shape of the spectrum envelope (both amplitude and phase) does not change.

Intervals between adjacent harmonics increase with a pulse repetition increase (period $T_и$ decrease), i. e., the spectrum will become more clearly defined or "more transparent", while harmonic amplitudes rise. On the other hand, given a repetition frequency decrease (period $T_и$ increase), intervals between adjacent harmonics decrease, i. e., the spectrum will become "denser," while harmonic amplitudes decrease.*

The relationship of the spectrum envelope to square pulse duration is evident from the following. Point $f = \frac{1}{\tau_и}$, at which the spectrum envelope reverts to zero for the first time, withdraws to the high-frequency range when there is a

*In the range where $F_и \to 0$ ($T_и \to \infty$), we will convert from a periodic train of video pulses to a single video pulse. Here, intervals between harmonics $\Delta f_и$ and amplitudes of all harmonics will become infinitely small. Thus, the sum of an infinitely-large number of harmonic components infinitely small in amplitude and infinitely close in frequency may represent the single pulse. In other words, a single pulse has a continuous, rather than a discrete, spectrum comprising the harmonics of all frequencies.

decrease in pulse duration $t_и$. Here, the first and all subsequent "lobes" of the spectrum expand. In the range where $t_и \to 0$ $f = \frac{1}{t_и} \to \infty$ and the amplitudes of all spectrum harmonics turn out to be identical. Consequently, the spectrum of a pulse of infinitely-slight duration is uniform in the entire frequency range.

All points $f = \frac{m}{t_и}$ in which the spectrum envelope reverts to zero, shift towards f = 0 when pulse duration increases, i. e., the spectrum will become narrower and is concentrated in a band of lower frequencies. Where $t_и \to \infty$ $\frac{m}{t_и} \to 0$, the spectrum of an infinitely-long pulse (if the latter is a precise function /519 of time) degenerates into a d-c component. This is natural since such a pulse is constant voltage, which may not contain harmonic components.

It is possible to demonstrate that, for any other pulse shape as well, pulse spectrum width Δf_s is coupled with its duration by inversely-proportional relationship

$$\Delta f_s = \frac{b}{t_и} \qquad (XI.8)$$

where b — factor depending on pulse shape and the method (level) used to compute $t_и$ and Δf_s.

The concept of spectrum width requires refinement since, theoretically, pulse spectra are limitless with respect to frequency. Spectrum width usually is determined from power considerations as the band of frequencies adjacent to point f = 0, in which the overwhelming portion of complete pulse energy is concentrated.* This band is referred to as the spectrum active power width or intrinsic amplitude band. Thus, for example, taking the width of the first lobe (it will comprise more than 90% of pulse energy) as the square pulse spectrum width, we obtain $\Delta f_s = \frac{1}{t_и}$ (b = 1). Consequently, $\Delta f_s = 10^6$ Hz when $t_и$ = 1 usec.**

The spectrum envelope for pulses of another shape has another form. However,

*Energy transferred by each harmonic is proportional to the square of its amplitude.

**Such a significant video pulse spectrum width, in particular, explains why high-frequency feeders are used for their distortionless transmission.

the overall tendency towards a decrease in harmonic amplitudes with a rise in frequency (harmonic numbers) always is preserved. This is coupled from the physical point of view with the fact that the main part of the pulse signal energy always is concentrated in the low-frequency band of the spectrum and, with an increase in the frequency of the harmonics, their power "contribution" drops. This is stipulated mathematically by the influence of multiplier $e^{-j\omega t}$ in expression (XI.5) on the integration result. Actually, in the low-frequency band, for which condition $\omega t_и \ll 1$ is satisfied, i. e.,

$$\omega \ll \frac{1}{t_и}, \; e^{-j\omega t} \approx 1 \quad \text{и} \quad U(\omega) \approx \frac{2}{T_и} \int_0^{t_и} f(t)\,dt = \text{const.}$$

harmonic amplitude essentially is constant and equals double the d-c component value.

Harmonic amplitudes decrease in connection with the nature of the function $e^{-j\omega t}$ change when frequency increases, when the latter's value ω will equal $\approx \frac{1}{t_и}$.*

Square pulses have a broader spectrum. This is explained by the role of high-frequency harmonics in shaping of vertical porches and flat tilts of such pulses (see Figure 3). Bell-shaped pulses (see Figure I.2g), a shape described by function $f(t) = e^{-at^2}$ (Gausse curve) without breaks and linear sectors, have the most concentrated spectrum. The spectrum of such pulses is narrower by a factor of approximately 2 than the spectrum of square pulses.

ATTACHMENT 2 /520

PULSE DEVICE LINEAR AND NONLINEAR ELEMENTS

Categorization of all pulse circuit elements as linear or nonlinear is critical for analysis of physical processes in pulse devices.

*Function $e^{-j\omega t}$ is periodic $e^{-j\omega t} = \cos\omega t - j\sin\omega t$ with modulus $|e^{-j\omega t}| = \sqrt{\cos^2\omega t + \sin^2\omega t} = 1$. Where $t = t_и$ and frequency ω increases, harmonic amplitudes decrease in connection with the decrease in the area of cosinusoidal and sinusoidal component half-cycles.

Linear elements are those characterized by the independence of their parameters from the magnitude of the voltage applied to them and the current passing across

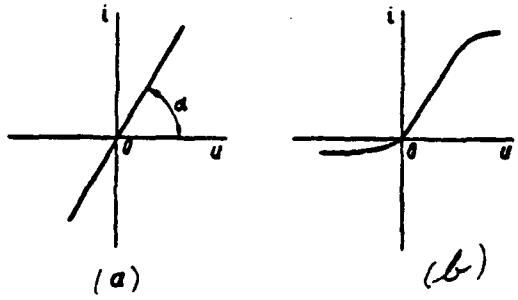


Figure 4. Volt-Ampere Characteristics of Linear (a) and Nonlinear (b) Elements.

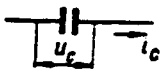
them. Therefore, the volt-ampere characteristic of a linear element--relationship $i = \Phi(u)$--is a straight line (Figure 4a). The linearity of this characteristic signifies the constancy of ratio $\frac{U}{I}$, equalling element resistance, i. e., the validity of Ohm's law. Three types of linear elements exist: resistance R (elements in which accumulation of electrical energy is impossible and only its conversion into heat energy occurs), capacitance C (elements capable of accumulating the energy of an electrical field), and inductance L (elements capable of accumulating the energy of a magnetic field).

R, L, and C descriptions and units of measurement, their designations in circuits, basic integrodifferentiating ratios characterizing these elements, expressions of their a-c resistance, as well as their characteristic properties in fixed and transient modes, are depicted in Table 4.

Capacitances and inductances, being reservoirs of the energy of electric and magnetic fields, respectively, exert a decisive impact on the nature of transient processes. Therefore, we will dwell on the table's last two entries.

In a capacitor, electrical field energy is stored between its plates and equals $W_C = \frac{Cu_C^2}{2}$, where u_C — capacitor voltage proportional to the charge (amount of electricity) q in its plates $u_C = \frac{q}{C}$. Since energy W_C will depend

Table 4

(a) Элемент и его условное изображение на схемах	(b) Единицы измерения: (c) название	(d) размерность и соотношения	(e) Обозначение номинала на схемах	(f) Основные уравнения	(g) Сопротивление переменному току	(h) Влияние на стационарный режим цепи	(i) Влияние на переходные процессы
(j) Активное сопротивление R (резистор) 	(k) Ом	(l) $ом = \frac{1\ в}{1\ а}$	150; 500	$u_R = i_R R$, $i_R = \frac{u_R}{R}$	R	Создает падение напряжения u_R, ограничивает величину тока i_R (m)	—
	(o) Килоом (ком)	$1\ ком = 10^3\ ом$	15к; 100к				
	(p) Мегом (Мом)	$1\ Мом = 10^6\ ом$	2.0; 4.5				
(q) Емкость C (конденсатор) 	(r) Фарада (ф)	$ф = \frac{а \cdot сек}{в}$ (cc)		$u_C = u_C(0) + \frac{1}{C}\int i_C\,dt$, $i_C = C\frac{du_C}{dt}$	$\frac{1}{j\omega C}$	Не пропускает постоянный ток $I_C = 0$ (n)	Невозможны скачки напряжения u_C (u)
	(s) Микрофарада (мкф)	$1\ мкф = 10^{-6}\ ф$	0.01; 0.4; 2.0				
	(t) Пикофарада (пф)	$1\ пф = 10^{-12}\ ф$	200; 6800				
(v) Индуктивность L (катушка индуктивности) 	(w) Генри (гн)	$гн = \frac{в \cdot сек}{а}$	(z) Не проставляются	$u_L = L\frac{di_L}{dt}$, $i_L = i_L(0) + \frac{1}{L}\int u_L\,dt$	$j\omega L$	(aa) Отсутствует падение напряжения $U_L = 0$	(bb) Невозможны скачки тока i_L
	(x) Миллигенри (мгн)	$1\ мгн = 10^{-3}\ гн$					
	(y) Микрогенри (мкгн)	$1\ мкгн = 10^{-6}\ гн$					

KEY: (a) -- Element and its conditional designation in circuits; (b) -- Units of measurement; (c) -- Name; (d) -- Dimensions of a quantity and ratios; (e) -- Designation of nominal value in circuits; (f) -- Basic equations*; (g) -- Resistance to a-c; (h) -- Impact upon network fixed mode; (i) -- Impact on transient processes; (j) -- Resistance R (resistor); (k) -- ohm; (l) -- ohm = $\frac{1\ V}{1\ A}$; (m) -- Creates voltage drop u_R; clips current value i_R; (n) -- Does not pass direct current $I_C = 0$; (o) -- Kilohm (K); (p) -- Megohm (M); (q) -- Capacitance C (capacitor); (r) -- Farad (F); (s) -- Microfarad (mF); (t) -- Picofarad (pF); (u) -- Voltage u_C steps are impossible; (v) -- Inductance L (inductance coil); (w) -- Henry (H); (x) -- Millihenry (mH); (y) -- Microhenry (uH); (z) -- Not notated; (aa) -- Voltage drop $U_L = 0$ absent; (bb) -- Voltage i_L jumps are impossible; (cc) -- a x sec.

*Initial voltage and current values (where t = 0) are designated U(0) and I(0), respectively.

on charge q magnitude and is not coupled with movement of charges, i. e., with the current passing across the capacitance, it has the nature of potential energy. We now will assume that capacitor voltage instantaneously changes by value ΔU_C. Then the energy stored in the capacitor also must change instantaneously by a magnitude proportional to ΔU_C^2. But, an instantaneous change of this energy requires infinitely-great power (current across the capacitor): where /522

$\Delta t \to 0\ P_C = \frac{\Delta W_C}{\Delta t} = \frac{dw_C}{dt} \to \infty$, which is physically unrealistic. Consequently, the amount of electricity and capacitance voltage may rise (when C charges) or fall (when C discharges) only gradually. This signifies that capacitance voltage steps physically are impossible. It is precisely as impossible, for example, instantaneously to change the water level in a tank: that would require creation of an infinitely-large stream of water filling or draining the tank. Given any realistically-constrained inflow or outflow of water, its level will change only gradually. An important result flows therefrom: distortionless voltage steps in a network are transmitted across a capacitance.

Actually, in any closed network, input and output terminals separated by capacitance C (Figure 5a), in accordance with Kirchhoff's second law, must satisfy

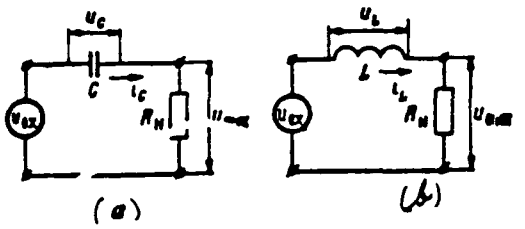


Figure 5. For Transmission of Voltage Steps Across a Capacitance and Inductance.

condition $u_{вх} = u_C + u_{вых}$. If input voltage changes with a jump by magnitude $\Delta U_{вх}$, then, since voltage u_C may not change instantaneously, output voltage also must change with a jump by magnitude $\Delta U_{вых} = \Delta U_{вх}$.

Magnetic field energy in an inductance coil is stored in surrounding space and equals $W_L = \frac{Li_L^2}{2}$. Since this energy will depend on current passing across

the coil, i. e., on the rate of charge displacement, it has the nature of kinetic energy. Therefore, current steps passing across an inductance physically are impossible. They also would require infinitely-great power in the network: $\Delta t \to 0\ P_L = \frac{\Delta W_L}{\Delta t} = \frac{dw_L}{dt} \to \infty$. It is precisely as impossible, for example, instantaneously to change the speed of a moving body possessing specific kinetic energy. An important result flows from this fact as well: voltage steps may not be transmitted across an inductance.

Actually, in any closed network, input and output terminals separated by inductance L (see Figure 5b), in accordance with Kirchhoff's second law, must satisfy condition $u_{вх} = u_L + u_{вых}$. If input voltage changes with a jump by magnitude $\Delta U_{вх}$, then, since current i_L may not change instantaneously ($\Delta I_L = 0$), a step of output voltage also is impossible ($\Delta U_{вых} = \Delta I_L R_н = 0$) . Here, an input voltage step is compensated for completely by a voltage step in the same inductance $\Delta U_L = \Delta U_{вх}$, which balances self-induction emf $e_L = -L\frac{di_L}{dt} = -u_L$ arising in the inductance.

It should be noted that, since there are stray capacitances and inductances in any real network, transient processes may not occur instantaneously in the network. This, in particular, explains the inability to shape, transmit, and amplify pulses of an ideally-square shape.

The relationship of nonlinear element parameters to currents and voltages, i. e., they have nonlinear volt-ampere characteristics (Figure 4b), characterizes *nonlinear elements*. Therefore, we will not apply Ohm's law to nonlinear elements. These include vacuum tubes, ion and semiconductor instruments, and saturated-core inductances. It should be noted that, in many instances, when amplifying pulse signals, for example, nonlinear elements are used in the region where their volt-ampere characteristics may be considered to approximate linear characteristics. In other cases, in pulse amplitude clippers and pulse generators, for example, nonlinearity of the characteristics of these elements, on the other hand, plays a determinant role.

Networks comprising only linear elements are referred to as linear networks, while networks containing nonlinear elements are referred to as nonlinear networks. The difference in these networks, from a mathematical point of view, is that processes

in linear networks are described by differential equations with constant coefficients, while those in nonlinear networks are described by differential equations with variable coefficients. The applicability of the principle of superposition to linear networks is their basic characteristic property from the physical point of view.

Overall, the principle of superposition (also referred to as the principle of independent action) may be formulated in the following manner: in a linear system, the resultant effect of the sum of the actions equals the sum of the effects caused by each action. Consequently, if any number of independent emf connected in any manner act upon a linear network, then the resultant current and voltage in any network element equals the algebraic sum of the individual currents or voltage drops caused by the action of each emf. The principle of superposition is the basis for superposable methods of linear system analysis, whose essence is that a signal of complex shape acting upon a linear system input is the sum of the elementary standard signals, after which the system output signal (reaction, response) will be found as the sum of system reactions to all elementary signals.

The method of frequency analysis and the method of transient characteristics are fundamental superposable methods.

Kirchhoff's laws, the concepts of voltage and current generators, and the equivalent generator theorem also lie at the foundation of linear network analysis as a result of the principle of superposition.

ATTACHMENT 3

EXPONENTIAL PROCESSES

The differential equations of linear networks comprising one reactive element (capacitance or inductance) will be reduced to the form

$$\tau \frac{dx}{dt} + x = y. \qquad \text{(XI.9)}$$

where $x = x(t)$ — desired time function (the law of change of voltage or current at network output);

$y = y(t)$ -- known time function describing the action of external effects on the network (of applied voltage or current);

T -- constant coefficient depending only on the parameters of a network having a time difference and referred to as network time constant.

If, at moment $t = 0$, the network is subjected to a switching drop (step change) of constant voltage or current, then a transient process arises in it described by general solution of equation (XI.9) for $y = Y = \text{const}$. This solution is written in the form

$$x(t) = X(\infty) + [X(0) - X(\infty)]e^{-\frac{t}{T}}. \qquad \text{(XI.10)}$$

where $X(0)$ -- initial (for $t = 0$);

$X(\infty)$ -- final (for $t = \infty$) value of the voltage or current at network output;

$e = 2.718\ldots$ -- logarithm base.

If a network short circuit occurs at $t = 0$, then $X(\infty) = 0$ and, based on (XI.10) we obtain

$$x_1(t) = X(0)e^{-\frac{t}{T}} \qquad \text{(XI.11)}$$

If this network is connected to a constant voltage or current source, then, given zero initial conditions, i. e., when $X(0) = 0$, based on (XI.10) we obtain

$$x_2(t) = X(\infty)\left[1 - e^{-\frac{t}{T}}\right]. \qquad \text{(XI.12)}$$

The graphs of functions $x_1(t)$ and $x_2(t)$ are depicted in Figure 6. In the first instance, they are falling and, in the second instance, rising exponential curves.

Function $x_1(t)$ has initial value $X(0)$ (where $t = 0$, $e^{-\frac{t}{T}} = 1$), and then

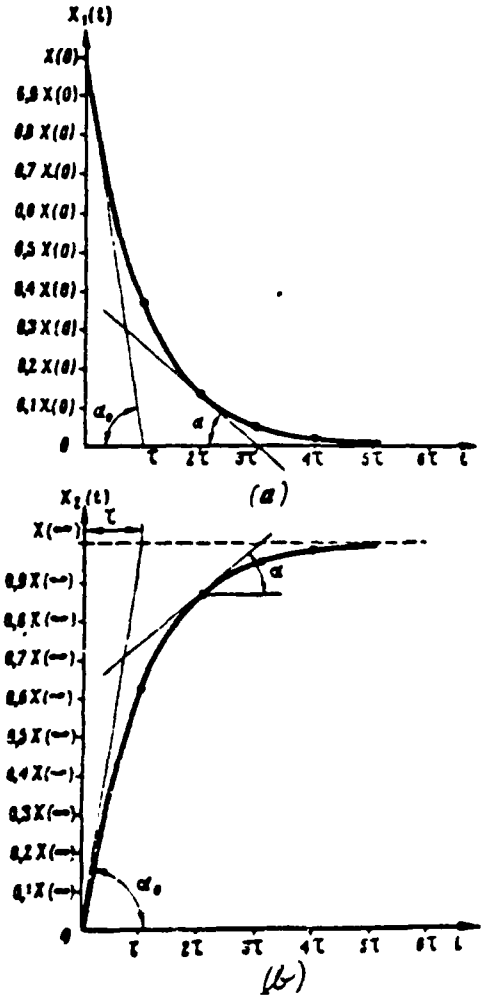


Figure 6. Graphs of Exponential Functions.

monotonously decreases, asymptotically striving towards zero at infinity (where $t \to \infty$, $e^{-\frac{t}{\tau}} \to 0$).

Function $x_2(t)$ at the initial moment in time equals zero (where $t = 0$, $1 - e^{-\frac{t}{\tau}} = 0$), then monotonously rises, asymtotically striving at infinity to value $X(\infty)$ (where $t \to \infty$, $1 - e^{-\frac{t}{\tau}} \to 1$). The magnitude of the degree indicator $\frac{t}{\tau}$ for

given moments in time t determines instantaneous exponential function values. Approximate values of these functions computed for different moments in time expressed in unities of the time constant are depicted in Table 5.

Table 5

(а) Время процесса t	τ	2τ	3τ	4τ	5τ
$x_1(t)$	$0.368X(0)$	$0.135X(0)$	$0.05X(0)$	$0.018X(0)$	$0.007X(0)$
$x_2(t)$	$0.632X(\infty)$	$0.865X(\infty)$	$0.95X(\infty)$	$0.982X(\infty)$	$0.993X(\infty)$

KEY: (а) -- Process time t.

Data from this table may be used for approximate plotting of exponential curves with respect to the points. It is evident from the table that the time constant equals the interval during which function $x_1(t)$ decreases to value $0.368X(0)$ (by a factor of e) or function $x_2(t)$ rises to value $0.632X(\infty)$ (by a factor of $1-e^{-1}$).

The rates of change of functions $x_1(t)$ and $x_2(t)$, respectively, equal:

$$v = \frac{dx_1(t)}{dt} = -\frac{X(0)}{\tau}e^{-\frac{t}{\tau}}, \quad v_1 = \frac{dx_2(t)}{dt} = \frac{X(\infty)}{\tau}e^{-\frac{t}{\tau}}. \tag{XI.13}$$

i. e., in both instances they decrease monotonously with respect to magnitude /526 also by an exponential law. The instantaneous magnitude of this rate in the graphs (the slope of the exponential curves) equals the tangent of the slope of a tangent line drawn to the exponent at a given point: $V = \operatorname{tg}\alpha$. The maximum value of the rate is obtained at initial moment in time t = 0:

$$|V_{max}| = \frac{X(0)}{\tau} = \operatorname{tg}\alpha_0, \quad |V_{1max}| = \frac{X(\infty)}{\tau} = \operatorname{tg}\alpha_1 \tag{XI.14}$$

where $\operatorname{tg}\alpha_0$ -- tangent of the slope of the tangent line to the exponent at the initial point $\left(\alpha_0 < \frac{\pi}{2}\right)$.

Therefore, time constant τ may be determined graphically as the magnitude of the subtangent line to the exponential curve (Figure 6).

Theoretically, transient processes described by exponential functions will last an infinitely-long time. In practice, the accepted duration of these processes equals the time interval up to the end of which exponential functions still differ slightly from their steady-state values $X(\infty)$. An often-used transient process duration equals

$$t_{перех} = 3\tau \qquad \text{(XI.15)}$$

(in accordance with Table 5, at moment $t = 3\tau$, exponential functions differ from their steady-state values by only 5%).

Expanding term $e^{-\frac{t}{\tau}}$ into a Maclaurin series, we obtain

$$e^{-\frac{t}{\tau}} = 1 - \frac{t}{\tau} + \frac{t^2}{2!\tau^2} - \frac{t^3}{3!\tau^3} + \frac{t^4}{4!\tau^4} - \dots$$

Where $\frac{t}{\tau} < 1$ in this expansion, it is possible to disregard all terms, beginning with the third, due to their insignificance compared to the second term. Therefore, initial sectors of exponential functions in region $t \ll \tau$ may be approximated somewhat by straight lines (by tangent lines at the initial points):

$$x_1(t) \approx X(0)\left[1 - \frac{t}{\tau}\right]; \quad x_2(t) \approx X(\infty)\frac{t}{\tau} \qquad \text{(XI.16)}$$

This stipulates use of the initial sectors of exponential curves as linearly-changing voltages (currents).

ATTACHMENT 4

VOLTAGE AND CURRENT GENERATORS. GENERATOR-LOAD MATCHING CONDITIONS

Electrical signal energy sources always have a certain amount of internal resistance R_i. For convenience in circuit analysis, this internal resistance conditionally is depicted outside of the source itself, connecting it either in series with the source or in parallel to it. In the first case (Figure 7a), the source is referred to as an emf or voltage generator relative to load impedance $R_н$. Here, zero internal resistance is ascribed to the emf generator itself so that source emf $E_г$ does not depend on load impedance magnitude. In the second case

(Figure 7b), the source is referred to as a current generator. Here, infinitely-large internal resistance is ascribed to the current generator itself so /527 that current I_r supplied by the source does not depend on the load impedance magnitude.

Both source depiction methods are equivalent for an external network (they provide identical load current and voltage values) if

$$I_r = \frac{E_r}{R_r} \qquad \text{(XI.17)}$$

Actually, load current for an emf generator equals $I_н = \frac{E_r}{R_r + R_н}$. For a current generator, load voltage equals $U_н = I_r \frac{R_r R_н}{R_r + R_н}$ and, consequently, load current $I_н = \frac{U_н}{R_н} = I_r \frac{R_r}{R_r + R_н}$. Equating current $I_н$ values for both cases, we obtain $\frac{E_r}{R_r + R_н} = I_r \frac{R_r}{R_r + R_н}$, hence $I_r = \frac{E_r}{R_r}$.

The concepts of emf and current generators are used widely for vacuum tube and semiconductor instrument representation by equivalent circuits in the linear region of their characteristics.

The power an emf generator supplies to load (consumed load) equals

$$P_н = I_н^2 R_н = \frac{E_r^2 R_н}{(R_r + R_н)^2}.$$

Investigating this function to the maximum (differentiating it with respect to $R_н$ and equating the resultant derivative to zero), we will find that this power will be maximum if

$$R_r = R_н, \qquad \text{(XI.18)}$$

and will comprise $P_{н\,max} = \frac{E_r^2}{4R_н}$ -- half the generator power $P_r = E_r I_r = \frac{E_r^2}{2R_н}$. The second half of the generator power is consumed in its internal resistance R_r.

Condition (18) is referred to as the generator-load matching condition. This condition must be supplemented by the condition of mutual reactive component

compensation, given presence of generator and load reactive component resistances in a-c systems:

$$X_r = -X_н \qquad \text{(XI.18a)}$$

ATTACHMENT 5 /528

EQUIVALENT GENERATOR THEOREM

We will assume that there exists a linear network comprising emf sources and having two output terminals aa to which load impedance $R_н$ is connected (Figure

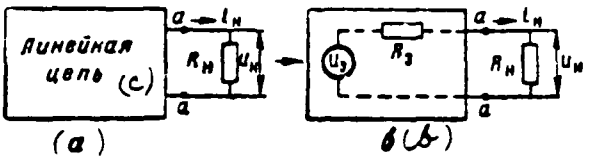


Figure 8. For Formulation of the Equivalent Generator Theorem. (c) — Linear network).

8a). In accordance with the equivalent generator theorem, equivalent generator voltage $u_э$ with internal resistance $R_э$ may represent this network (Figure 8b). The electromotive force of the equivalent generator is determined as the voltage at network output terminals when the load is cut out (idling voltage), while its internal resistance $R_э$ is determined as network output voltage which the load "sees" confronting it. Source internal resistances must replace all emf sources in the network in order to compute resistance $R_э$; here, sources whose internal resistance is not considered (accepted as equalling zero) are short-circuited. Use of the equivalent generator theorem makes it possible simply to compute load impedance current and voltage by the formulas:*

$$i_н = \frac{u_э}{R_э + R_н}; \quad u_н = \frac{u_э R_н}{R_э + R_н} \qquad \text{(XI.19)}$$

*Generally, resistances $R_э$ and $R_э$ may be complex.

Proof of the equivalent generator theorem is based on the principle of superposition.

This theorem is used often in pulse technology to compute complex charging (discharging, recharging) network time constants of capacitances and inductances. Here, the points at which a capacitance or inducatance is connected to the rest of the circuit usually are used as equivalent generator output terminals, thus leaving all emf sources and resistances in the equivalent generator. It is sufficient for network time constant computation to determine only resistance R_0, which will be the equivalent resistance in the charging (discharging, recharging) network.

ATTACHMENT 6 /529

LINEAR NETWORK FREQUENCY CHARACTERISTICS

Resistances of capacitances and inductances to a-c will depend on frequency. Therefore, linear networks, which are comprised of these elements, possess

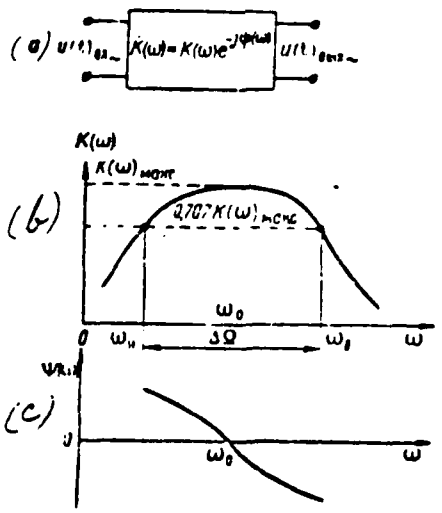


Figure 9. Linear Four-Terminal Network (a), Its Amplitude-Frequency (b), and Phase-Frequency (c) Characteristics.

frequency-selective properties, i. e., they react differently to the harmonic

effects of different frequencies. Frequency- selective properties are evaluated with the aid of network frequency characteristics. Examination of this question requires that we represent the linear network in the most general form by a linear four-terminal network (Figure 9a). We will assume that harmonic voltage $\dot{U}_{вх}e^{j\omega t}$ is supplied to the input of this four-terminal network. Here, $\dot{U}_{вх}=U_{вх}e^{j\varphi_{вх}}$ — complex amplitude, $U_{вх}$ -- real amplitude, $\varphi_{вх}$ -- initial phase, $\omega=2\pi f$ -- input voltage angular frequency.

Harmonic voltage $\dot{U}_{вых}e^{j\omega t}$ of identical frequency ω also arises in the steady-state mode at four-terminal network output but, overall, with a distinct complex amplitude $\dot{U}_{вых}=U_{вых}e^{j\varphi_{вых}}$, i. e., with another real amplitude $U_{вых}$ and with initial phase $\varphi_{вых}$. If now only the frequency of the input voltage is changed (where $U_{вх}=\text{const}$), then the complex amplitude of the output voltage, i. e., its real amplitude and phase, also will change, thus being a function of frequency, i. e., $\dot{U}_{вых}=\dot{U}(\omega)_{вых}=U(\omega)_{вых}e^{j\varphi(\omega)_{вых}}$.

The ratio of harmonic voltage complex amplitudes at four-terminal output and input to the frequency function is referred to as the system complex frequency characteristic:

$$K(\omega)=\frac{\dot{U}(\omega)_{вых}}{\dot{U}_{вх}}=\frac{U(\omega)_{вых}}{U_{вх}}e^{j[\varphi(\omega)_{вых}-\varphi_{вх}]} \qquad \text{(XI.20)}$$

The modulus of this characteristic, equal to the ratio of output and /530 input voltage real amplitudes to the frequency function, is referred to as the amplitude-frequency characteristic (abbreviated AChKh):

$$K(\omega)=\frac{U(\omega)_{вых}}{U_{вх}} \qquad \text{(XI.21)}$$

The argument of the complex frequency characteristic, equal to the phase shift (difference) between output and input voltages in the frequency function, is referred to as the phase-frequency characteristic (abbreviated FChKh):

$$\varphi(\omega)=\varphi(\omega)_{вых}-\varphi_{вх} \qquad \text{(XI.22)}$$

If the complex frequency characteristic, using the algebraic form of writing

a complex number, is written in the form $K(\omega)=A(\omega)-jB(\omega)$, then the AChKh and FChKh values, respectively, will be found from the formulas:

$$K(\omega)=\sqrt{A(\omega)^2+B(\omega)^2},\quad \varphi(\omega)=\operatorname{arctg}\frac{B(\omega)}{A(\omega)}. \tag{XI.23}$$

A possible form of the frequency characteristics is depicted in Figure 9b, c. Knowledge of these characteristics makes it possible, with respect to known harmonic input voltage amplitude, phase, and frequency, to determine harmonic output voltage amplitude and phase. Actually, based on (21) and (22), we obtain:

$$U(\omega)_{вых}=K(\omega)U_{вх},\quad \varphi(\omega)_{вых}=\varphi_{вх}+\psi(\omega).$$

where $K(\omega)$ and $\Phi(\omega)$ -- AKhCh and FChKh ordinates corresponding to input voltage frequency ω. Thus, linear system frequency characteristics completely determine passage of the harmonic voltage of any given frequency across the system.

As shown in Figure 9b, the amplitude-frequency characteristic generally may have "dips" (reductions) in the low-frequency ($\omega<\omega_0$) and high-frequency band ($\omega>\omega_0$). An AChKh "dip" in any frequency band demonstrates that the transmission across a given network of harmonic voltages of these frequencies occurs with a relative decrease in their amplitude. Bandwith $\Delta\Omega$ — the band of frequencies within which AChKh ordinates decrease relative to its maximum value by no more than a factor of $\sqrt{2}$, is an AChKh response criterion.*

Consequently, bandwidth is restricted to frequencies whose AChKh value is $\frac{K(\omega)_{max}}{\sqrt{2}}\approx 0{,}707K(\omega)_{max}$. These are referred to as the upper- $(\omega_в)$ and lower- $(\omega_н)$ frequency limits, respectively. The weaker the expressed network frequency-selective properties, the broader the bandwidth, and vice versa.

Examining the movement of the phase-frequency characteristic in Figure 9c, we will note that its positive values ($\Phi(\omega)>0$) correspond to output voltage phase lead, while the negative values ($\Phi(\omega)<0$), on the contrary, correspond to output voltage phase lag (delay) relative to input voltage.

*Determination of bandwidth at any other, predetermined, level also is possible.

ATTACHMENT 7 /531

ESSENCE OF LINEAR CIRCUIT FREQUENCY ANALYSIS. PULSE DISTORTIONLESS TRANSMISSION CONDITIONS. LINEAR DISTORTIONS

Linear network frequency characteristics (21) and (22) completely determine the passage of a harmonic oscillation of a given frequency across the network. But, any pulse signal may be represented by its own frequency spectrum--in the form of the combination of the harmonic oscillations of different frequencies (see Attachment 1). Since the principle of superposition is valid for linear systems, it is possible to examine the effect of each spectrum harmonic independent of the action of all other harmonics. Therefore, finding the frequency spectrum of a pulse signal acting upon a linear network input and knowing its frequency characteristics, it is possible to find the result of the effect of each spectrum harmonic on this network. It is evident that each harmonic with frequency ω_1 during passage across a linear network will change in amplitude by a factor of

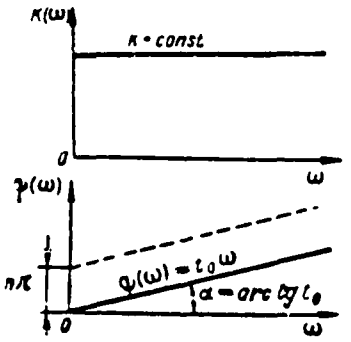


Figure 10. Ideal Distortionless Linear Network Frequency Characteristics.

$K(\omega_1)$ and displace in phase by angle $\varphi(\omega_1)$.* As a result, a combination of harmonic components, which forms the output signal frequency spectrum, arises

*In principle, it is impossible for the harmonic of new frequencies to appear at linear network output since the frequency of each harmonic does not change.

at network output. Finding this spectrum, it is possible to use it to determine the output signal itself as a function of time $f(t)_{вых}$.

It is evident that the signal at network output will be similar to the signal at input $f(t)_{вых} \sim f(t)_{вх}$, i. e., distortionless transmission of pulses across a linear network will occur if the spectrum at network output will turn out to be similar to the spectrum at input, i. e., if amplitude and phase ratios between all spectrum harmonics remain unchanged during passage across this network. But, this requires that the network amplitude-frequency characteristic be expressed as a constant magnitude, i. e., that the bandwidth be infinite, while the network phase-frequency characteristic must be linear and pass through the origin of the coordinates (Figure 10):

$$\begin{gathered} K(\omega) = K = \text{const} \ (\Delta\Omega = \infty); \\ \psi(\omega) = t_0\omega. \end{gathered} \tag{XI.24}$$

where t_0 — tangent of the AChKh slope to the frequency axis. Actually, AChKh constancy in the entire frequency band denotes that the amplitudes of all spectrum harmonics change by identical factor K during passage across the network. FChKh linearity denotes that the time delay of all spectrum harmonics at network output also will be identical

$$\frac{\psi(\omega_1)}{\omega_1} = \frac{\psi(\omega_2)}{\omega_2} = \ldots = \operatorname{tg}\alpha = t_0 = \text{const}.$$

Therefore, the signal at network output completely lags by time t_0 (phase delay time) and will change with respect to magnitude by a factor of K, /532 while its shape will remain unchanged.* Thus, expression (24) is a condition of distortionless pulse transmission across a linear network.

Realistically, due to influence of capacitances and inductances, linear network frequency characteristics always differ from the ideal characteristics (Figure 9). As a result, when a pulse signal passes across a real linear network, the amplitude

*It is possible to show that the same result will be obtained if $\psi(\omega) = t_0\omega + n\pi$, where n — any whole number (dotted line in Figure 10), while the output signal changes its polarity in the event n is an odd number.

and phase ratios among the harmonics of its spectrum change and the shape of the signal at output differs from that at input. Signal shape distortions caused by linear network frequency-selective properties are referred to as linear or frequency distortions. There are two types of linear distortions: low-frequency, caused by the AChKh "dip" in the low-frequency range, and high-frequency, caused by the FChKn "dip" in the high-frequency range.

The approximate nature of linear distortions in the shape of a square pulse is depicted in Figure 11. It stems from the relative role of the pulse spectrum

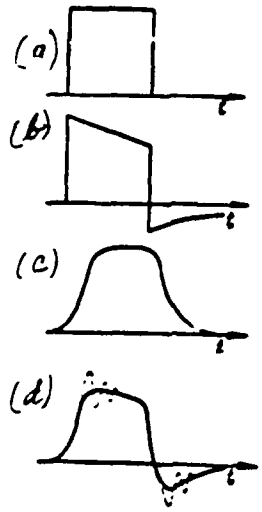


Figure 11. Linear Distortions of a Square Pulse (a); (b) -- Low-Frequency; (c) -- High-Frequency; (d) -- Total.

low- and high-frequency harmonics in shaping its envelope (see Attachment 1).

Low-frequency distortions arise due to relative suppression of low-frequency harmonics in the output signal spectrum and manifest themselves in pulse tilt reduction and, upon its cessation, onset of an opposite-polarity output voltage excursion (Figure 11b).

If the d-c component of the input pulse spectrum does not pass across the

linear network at all (K(0) = 0), i. e., is absent at network output, then the algebraic sum of the areas of the different signs bounded by the graph of the output voltage will equal zero. High-frequency distortions arise due to relative suppression of high-frequency harmonics in the output signal spectrum and manifest themselves in stretching of pulse porches and impartation of a flat character to its envelope (Figure 11c). Given both types of distortions, the resultant pulse envelope is flat, with stretched porches, receeding tilt, and an opposite-polarity excursion (Figure 11d). If the network has an oscillatory character (it includes both capacitances and inductances), then damping oscillations additionally may be imparted to the output pulse envelope (depicted by the dotted line in Figure 11d). These oscillations arise as a result of oscillatory network shock excitation when input pulse porches are active (see Chapter II, § 6).

Thus, from the spectral point of view, linear distortions result from deformation of the signal spectrum envelope--disruption of the amplitude and phase ratios among its harmonics when spectrum frequency structure is retained.*

Networks will strive for the shape of the frequency characteristics to approximate the shape of the ideal frequency characteristics (24) to the maximum in order to decrease pulse linear distortions. Special frequency correction measures--compensation for the AChKh "dips" in the low- and high-frequency range (see Chapter III, § 3)--are used to this end.

ATTACHMENT 8 /533

ESSENCE OF THE TRANSIENT CHARACTERISTICS METHOD

The transient characteristics method is founded on the principle of superposition, just as is the frequency method of linear network analysis. We will introduce initially the concept of the unit function (connection function) and the transient characteristic for familiarization with the essence of this method. Unit function $\sigma(t)$ is a step (change) of voltage or current of unit amplitude

*From the spectral point of view, nonlinear distortions are the result of signal spectrum transformation--its enrichment by new frequencies of harmonics.

and is plotted in Figure 12a. Unit function $\sigma(t-t')$, delayed relative to moment t = 0 by interval t' is plotted in Figure 12b.

The unit function is used as the standard linear network input signal, making it possible to study its transient mode. The shape of a linear network output signal, arising when the unit function acts upon the network, is referred to as network transient characteristic h(t). Thus,

$$h(t) = u(t)_{вых} \quad \text{where} \quad u(t)_{вх} = \sigma(t). \tag{XI.25}$$

Due to network linearity, input signal delay by time t' will cause an identical output signal delay, while an increase in the input signal by factor a will cause a rise in output signal by the identical factor. Therefore, response h(t--t') corresponds to input signal $\sigma(t-t')$ while response ah(t--t') corresponds to input signal $a\sigma(t-t')$.

These circumstances make it possible to use known network transient characteristic h(t) to find its response to input voltage of random shape, having

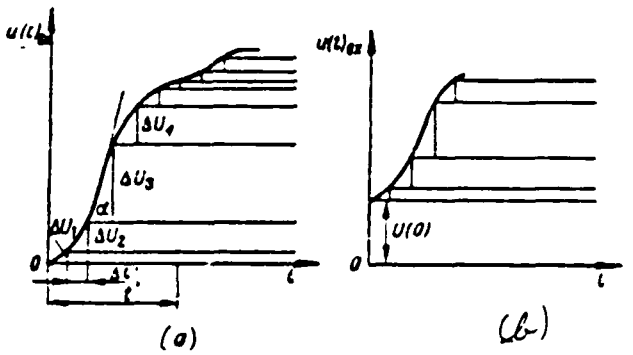


Figure 13. Representation of Randomly-Shaped Voltage By the Sum of the Elementary Stages.

represented beforehand this voltage as the sum of an infinitely-large number of elementary steps of infinitely-slight amplitude delayed relative to one another by infinitely-short time intervals. This is explained in Figure 13a, where voltage

$u(t)_{вх}$ is represented approximately first by the sum of a finite number of /534 steps with amplitude ΔU_1, ΔU_2, ΔU_3. . . and with identical delay of each step relative to the previous one equalling $\Delta t'$. The step envelope obtained in this manner will more accurately correspond to the shape of voltage $u(t)_{вх}$ the greater the number of steps used for its approximation. Precise correspondence is obtained when the range of the number of stages is increased to infinity, where

$$\Delta t \to dt,\ \Delta U \sim \left(\frac{du_{вх}}{dt}\right)_{t=t'} dt' \quad \left(\frac{du_{вх}}{dt} = tg\alpha\right)$$

and each step arising at moment t = t' will be expressed as $du(t)_{вх} = \left(\frac{du_{вх}}{dt}\right)_{t=t'} \cdot 1(t-t')\,dt$. It is necessary to add all elementary steps operative in the interval from 0 to 1, in order to obtain the resultant input voltage value at moment t:

$$u(t)_{вх} = \int_0^t \left(\frac{du_{вх}}{dt}\right)_{t=t'} 1(t-t')\,dt$$

The network response to each elementary step is expressed through the network transient characteristic as

$$du(t)_{вых} = du(t)_{вх} h(t-t').$$

In accordance with the principle of superposition, a complete network response equals the sum of the responses to all elementary steps. Therefore, output voltage will be found using the formula

$$u(t)_{вых} = \int_0^t \left(\frac{du_{вх}}{dt}\right)_{t=t'} h(t-t')\,dt \qquad (XI.26)$$

The ratio is referred to as the Duhamel integral.*

If the input voltage has finite step $U(0)_{вх}$ when t = 0 (Figure 13b), then a response to this step, equalling $U(0)_{вх} h(t)$, will be added at network output.

*Here, t' -- integration variable, t -- derivative, but constant for the moment in time summation process.

ATTACHMENT 9

VACUUM TUBE AND TRANSISTOR PARAMETERS

1. Parameters of Triodes Used in Pulse circuits

Tube Type	U_f V	I_f A	U_a V	U_g V	I_a mA	S mA/V
6S1P	6.3	0.15	250	-7	6.1	2.26
6S3P	6.3	0.3	150	--	16	19.5
6S15P	6.3	0.44	150	--	40	45
6S26B-K	6.3	0.22	120	--	9	5.2
6S28B	6.3	0.31	120	--	16	19
6S37B	6.3	0.44	80	--	40	16.5
6S51N	6.3	0.13	75	--	10	11.5
6N1P	6.3	0.6	250	--	7.5	4.35
6N2P	6.3	0.34	250	-1.5	2.3	2.1
6N3P	6.3	0.35	150	--	8.5	5.9
6N6P	6.3	0.75	120	-2	30	11.0
6N8S	6.3	0.6	250	-8	9	2.6
6N9S	6.3	0.3	250	-2	2.3	1.6
6N14P	6.3	0.35	90	-1.3	10.5	6.8
6N15P	6.3	0.45	100	--	9	5.6
6N16B	6.3	0.4	100	-2.4	8.0	5.0
6N23P	6.3	0.3	120	--	15	2.7
[illegible]	6.3	0.6	150	--	14	9.5

1. Continued.

μ	R_k K	R_g ohm	P_{max} W	C_{gk} pF	C_{ak} pF	C_{ag} pF
26.2	11.6	--	1.8	1.4	1.1	1.35
50	--	100	3	6.7	1.65	2.4
52	1.24	30	7.8	11.0	1.8	5.0
25	--	220	1.4	3.3	3.5	1.4
40	--	100	2.4	5.8	2.2	3.0
13	--	43	4.5	6	4.7	3.9
32	--	132	1.0	4.7	2.2	1.75
35	11	600	2.2	3.8	1.75	1.85
98	50	--	1.0	2.35	2.9	0.7
36	6.2	240	1.5	2.7	1.55	1.6
20	--	--	4.8	4.5	2.1	3.5
20	7.7	--	2.75	2.9	1.0	3.9
70	44	--	1.1	3.0	3.5	2.8
25	--	--	1.5	4.9	2.9	0.3
				2.1	1.15	1.8
38	6.8	50	1.6	2.0	0.4	1.4
25	--	--	0.9	2.7	1.65	1.5
32	--	680	1.8	3.6	2.0	1.5
48	5	100	2.6	4.0	2.2	1.9

2. Parameters of Tetrodes and Pentodes Used in Pulse Circuits.

Tube Type	U_f V	I_f A	U_a V	U_{g2} V	R_k ohm or U_{g1} V	I_a mA
6Zh1P	6.3	0.175	120	120	-2.0 V	6.2
6Zh2P	6.3	0.175	120	120	-2.0 V	5.5
6Zh3P	6.3	0.3	250	150	-1.6 V	7.0
6Zh4	6.3	0.45	300	150	-2.0 V	10.0
6Zh5P	6.3	0.45	300	150	160 ohms	9.5
6Zh8	6.3	0.3	250	100	-3.0 V	3.0
6Zh9P	6.3	0.3	150	150	80 ohms	15.5
6Zh10P	6.3	0.3	200	100	80 ohms	6.5
6Zh11P	6.3	0.44	150	150	50 ohms	25.0
6Zh20P	6.3	0.45	150	150	70 ohms	16.5
6Zh21P	6.3	0.34	150	150	-1.1 V	15.0
6Zh22P	6.3	0.46	150	150	-1.2 V	27.0
6Zh32P	6.3	0.2	250	140	-2.0 V	3.0
6Zh38P	6.3	0.18	150	100	80 ohms	13.0
6P1P	6.3	0.5	250	250	-12.5 V	44.0
6P9	6.3	0.65	300	150	-3.0 V	30.0
6P14P	6.3	0.76	250	250	-6.5 V (120 ohms)	48.0
6P15P	6.3	0.76	300	150	75 ohms	30.0

.. Continued.

I_{g2} mA	S mA/V	R_i K	P_a W	P_{g2} W	[illegible] pF	[illegible] pF	[illegible] pF
3.2	5.2	300	1.8	0.55	4.1	2.45	0.035
5.5	3.7	350	1.8	0.85	4.1	2.3	0.035
2.0	5.0	500	2.5	0.55	6.5	1.5	0.025
2.2	9.0	1000	3.3	0.45	9.0	5.0	0.015
3.5	9.0	240	3.6	0.5	8.5	2.2	0.03
0.8	1.65	--	2.8	0.7	6.0	7.0	0.005
4.5	17.5	150	3.0	0.75	8.5	3.5	0.03
5.5	9.5	100	3.0	0.75	8.5	4.1	0.025
7.5	28	36	4.9	1.15	14.0	3.5	0.04
6.0	16.5	90	4.0	1.2	8.6	2.45	0.04
6.0	15.0	95	4.0	1.2	5.9	1.9	0.035
9.0	25	55	7.0	1.8	9.0	2.4	0.05
1.0	1.8	2500	1.0	0.2	4.0	5.5	0.05
3.2	10.6	175	2.5	0.65	5.8	2.4	0.02
7.0	4.9	42.5	12.0	2.5	6.5	3.6	0.7
6.5	11.7	80	9.0	1.5	13.0	7.5	0.06
7.0	11.3	30	12.0	2.0	11.0	7.0	0.2
4.5	14.7	100	12.0	1.5	13.5	7.0	0.07

3. Parameters of Transistors Used in Pulse Circuits.

Type	Material and Conductivity Type	f_α MHz	P_c mW	$V_{(BR)CBO}$ V	I_E mA	$I_{C(max)}$ mA	β
MP20A	GE pnp	1.0	150	50	20	300	50-150
MP26A	GE pnp	0.2	200	70	—	400	20-40
MP26B	Ge pnp	0.2	200	70	—	400	30-80
MP39	Ge pnp	0.5	150	15	20	150	12
MP39B	Ge pnp	0.5	150	15	20	150	20-60
MP40	Ge pnp	1.0	150	15	20	150	20-40
MP41	Ge pnp	1.0	150	15	20	150	30-60
MP42	Ge pnp	1.0	200	15	50	300	20-60
MP42A	Ge pnp	1.0	200	15	50	300	30-90
MP42B	Ge pnp	1.0	200	15	50	300	45-135
P101	Si npn	0.2	150	20	20	100	9-18
P102	Si npn	0.5	150	10	20	100	15-30
P103	Si npn	1.0	150	10	20	100	18-35
P104	Si pnp	0.1	150	60	10	50	13-35
P105	Si pnp	0.2	150	40	10	50	15-40
P106	Si pnp	0.5	150	15	10	50	15-35
P401	Ge pnp	30	100	10	10	20	16-300
P402	Ge pnp	60	100	10	10	20	16-250
P403	Ge pnp	120	100	10	10	20	30-100
P403A	Ge pnp	120	100	10	10	20	16-200
P414	Ge pnp	60	100	10	10	30	25-100
P414A	Ge pnp	60	100	10	10	30	60-120
P415	Ge pnp	120	100	10	10	30	25-100
P415A	Ge pnp	120	100	10	10	30	60-120
P416	Ge pnp	40	100	12	25	120	20-80

3. Continued.

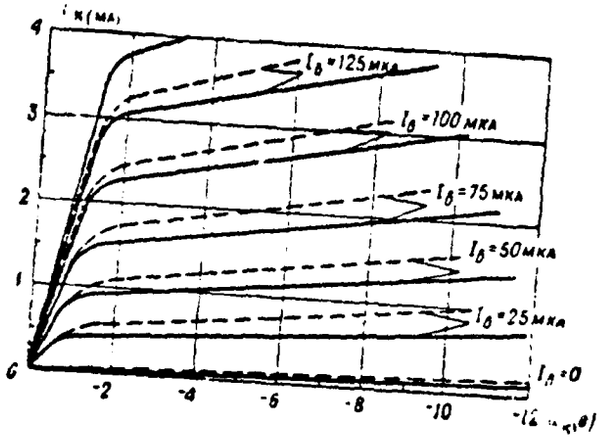
Back Current I_{ko} at 20° C uA	For U_k V	C_k pF	τ_{RC} psec	Frequency f (MHz) for which values C_k and are determined
50	30	—	—	—
75	70	50	8000	0.5
75	70	50	8000	0.5
15	5	60	13200	0.5
15	5	60	13200	0.5
15	5	60	13200	0.5
15	5	60	13200	0.5
25	15	—	—	—
25	15	—	—	—
25	15	—	—	—
3	20	150	—	0.5
3	10	150	—	0.5
3	10	150	—	0.5
50	20	40-80	—	0.465
50	20	40-80	—	0.465
50	15	40-80	—	0.465
10	5	15	3500	5.0
5	5	10	1000	5.0
5	5	10	500	5.0
5	5	10	500	5.0
4	10	10	1000	5.0
4	10	10	1000	5.0
4	10	10	500	5.0
4	10	10	500	5.0
3	10	8	500	5.0

3. Continued.

Type	Material and Conductivity Type	f_α MHz	P_c mW	$V_{cb(max)}$ V	I_c mA	$I_{c(max)}$ mA	β
P416A	Ge pnp	60	100	12	25	120	60-125
P416B	Ge pnp	80	100	12	25	120	100-250
P601	Ge pnp	20	1000	25	200	1500	20
P602	Ge pnp	20	1000	30	200	1500	40-100
P604	Ge pnp	20	400	45	200	500	10
P605	Ge pnp	40	400	45	200	1500	20-60
P606	Ge pnp	40	400	35	200	1500	20-60
P607	Ge pnp	60	1500	30	300	600	20-80
P608	Ge pnp	90	1500	30	300	600	40-120
P609	Ge pnp	120	1500	30	300	600	40-120

3. Continued.

Back Current I_{ko} at 20° C uA	For U_k V	C_c pF	$C_c r_b$ psec	Frequency f (MHz) for which values C_k and are determined
3	10	8	500	5.0
3	10	8	500	5.0
200	10	200	750	5.0
100	10	200	750	5.0
2000	45	200	500	5.0
2000	45	170	500	5.0
2000	45	130	500	5.0
300	30	50	500	5.0
300	30	50	500	5.0
500	30	50	500	5.0



4. P13 Transistor Collector Characteristics When Connected to a Common-Base Circuit For Normal Temperature 20° C (Solid Lines) and Increased Temperature 30° C (Dotted Lines).

REFERENCES

1. Ицхоки Я. С. Импульсные устройства. М., изд-во «Советское радио» 1959.
2. Меерович Л. А., Зеличенко Л. Г. Импульсная техника. М., изд-во «Советское радио», 1954.
3. Фролкин В. Т. Импульсные устройства. М., изд-во «Машиностроение», 1965.
4. Миллман Я. и Тауб Г. Импульсные цифровые устройства. М., Госэнергоиздат, 1960.
5. Харкевич А. А. Основы радиотехники. М., Связьиздат, 1963.
6. Гольденберг Л. М. Основы импульсной техники. М., изд-во «Связь», 1964.
7. Кривицкий Б. Х. Элементы и устройства импульсной техники. М., изд-во «Советское радио», 1961.
8. Регельсон Л. М. Анализ работы блокинг-генератора. М., изд. МГУ, 1965.
9. [illegible] К. Э., Степаненко И. П. Электронные усилители. М., Физ[illegible]
10. Григорьянц В. Г. Технические показатели радиолокационных станций. М., Воениздат, 1963.
11. Егоров Е. С., Немахин Б. Н. и др. Апериодические электронные усилители. М., изд. АРТА, 1960.
12. Егоров Е. С., Климушев Б. Я. и др. Расчет импульсных устройств. М., изд. АРТА, 1960.
13. Тищенко А. М., Лебедев Б. М. и др. Расчет и проектирование импульсных устройств на транзисторах. М., изд-во «Советское радио», 1964.
14. Яковлев В. Н. Импульсные схемы на транзисторах. Киев, изд-во «Техника», 1968.
15. Степаненко И. П. Основы теории транзисторов и транзисторных схем. М., Госэнергоиздат, 1963.
16. Шац С. Я. Транзисторы и основы их применения. М., Судпромгиз, [illegible]
17. Сборник «Полупроводниковая электроника». М., Госэнергоиздат, 1959.
18. Файзуллаев Б. Н. Полупроводниковые каскады в переходном режиме. М., изд-во «Связь», 1965.
19. Харлэ Р. Б. Логические схемы на транзисторах. М., изд-во «Мир», 1965.
20. Будинский Я. Усилители низкой частоты на транзисторах. М., Связьиздат, 1963.
21. Гурлев Д. С. Справочник по электронным приборам. Киев, изд-во «Техника», 1966.

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