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PSEUDOMORPHIC INTERFACES

School of Electrical Engineering
Purdue University
West Lafayette, Indiana 47907

9 June 1989

Final Technical Report for
Period 15 June 1987 - 31 December 1988

Prepared for

OFFICE OF NAVAL RESEARCH
800 North Quincy Street
Arlington, VA 22217

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Unclassified
SECURITY CLASSIFICATION OF THIS PAGE

REPORT DOCUMENTATION PAGE

1a REPORT SECURITY CLASSIFICATION: Unclassified	1b RESTRICTIVE MARKINGS:
2a SECURITY CLASSIFICATION AUTHORITY: N/A since unclassified	3. DISTRIBUTION / AVAILABILITY OF REPORT:
2b. DECLASSIFICATION / DOWNGRADING SCHEDULE: N/A since unclassified	
4. PERFORMING ORGANIZATION REPORT NUMBER(S):	5. MONITORING ORGANIZATION REPORT NUMBER(S):
6a. NAME OF PERFORMING ORGANIZATION: Purdue University; 6b. OFFICE SYMBOL (If applicable):	7a NAME OF MONITORING ORGANIZATION: Office of Naval Research
6c. ADDRESS (City, State, and ZIP Code): School of Electrical Engineering, West Lafayette, IN 47907	7b. ADDRESS (City, State, and ZIP Code): Arlington, VA 22217
8a. NAME OF FUNDING / SPONSORING ORGANIZATION: Office of Naval Research; 8b. OFFICE SYMBOL (If applicable): Code 1114	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER: N00014-86-K-0522
8c. ADDRESS (City, State, and ZIP Code): Arlington, VA 22217	10 SOURCE OF FUNDING NUMBERS: PROGRAM ELEMENT NO. / PROJECT NO. / TASK NO. / WORK UNIT ACCESSION NO

11. TITLE (Include Security Classification): Pseudomorphic Interfaces

12. PERSONAL AUTHOR(S): M. R. Melloch, R. L. Gunshor, L. A. Kolodziejski, J. A. Cooper, Jr., and R. F. Pierret

13a. TYPE OF REPORT	13b. TIME COVERED	14. DATE OF REPORT (Year, Month, Day)	15. PAGE COUNT
Final Report	FROM 870615 TO 881231	880609	35

16. SUPPLEMENTARY NOTATION

17. COSATI CODES			18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
FIELD	GROUP	SUB-GROUP	

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

This report covers the research work on Pseudomorphic ZnSe/epitaxial GaAs Interfaces performed from June 15, 1987 through December 31, 1988 under contract N00014-87-K-0522 sponsored by the Office of Naval Research. The objectives of this work were to develop the epitaxial growth of ZnSe on epitaxially grown GaAs, fully characterize this interface electrically, and fabricate a depletion mode field effect transistor which incorporates this interface in the device structure.

The electrical quality of our ZnSe/GaAs interfaces was investigated with capacitance versus voltage (CV) and current versus voltage (IV) measurements. The CV characteristics of annealed Au/ZnSe/p-GaAs capacitors were nearly ideal, exhibiting interface state densities ($2.5 \times 10^{}$ cm^{-2}) which compare favorably with the densities reported at typical AlGaAs interfaces. The occurrence of both hole accumulation (for p-type GaAs) and inversion (for n-type GaAs) at the ZnSe/GaAs interface indicates the presence of a substantial valence band offset. The lack of accumulation or inversion layers for electrons suggests a relatively small conduction band discontinuity.

(CONTINUED)

20. DISTRIBUTION / AVAILABILITY OF ABSTRACT	21. ABSTRACT SECURITY CLASSIFICATION	
☐ UNCLASSIFIED/UNLIMITED ☐ SAME AS RPT. ☒ DTIC USERS	Unclassified	
22a NAME OF RESPONSIBLE INDIVIDUAL: Max Yoder	22b. TELEPHONE (Include Area Code): 202-696-4218	22c. OFFICE SYMBOL: ONR, Code 1114

DD FORM 1473, 84 MAR — 83 APR edition may be used until exhausted. All other editions are obsolete.

SECURITY CLASSIFICATION OF THIS PAGE
Unclassified

19. ABSTRACT (continued)

The fabrication and IV characteristics of the first depletion-mode field-effect transistors based on a pseudomorphic ZnSe/n-GaAs heterointerface are described. The IV characteristics of the transistors are close to ideal; channel modulation indicates that the Fermi level is not pinned at the ZnSe/GaAs interface.

Finally, the research supported by this contract has resulted in 3 journal publications and 7 conference presentations.

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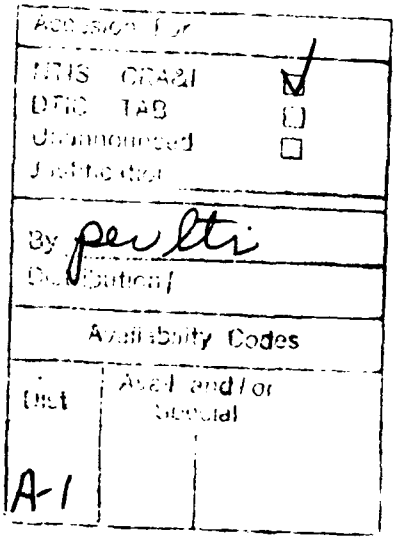


CHAPTER 1

INTRODUCTION

An unpassivated GaAs surface possesses a large surface recombination velocity which limits the performance of GaAs/(Al, Ga)As heterojunction bipolar transistors, heterojunction lasers and GaAs solar cells. Proper passivation of the GaAs surface is increasingly important as the device size decreases. Despite numerous efforts, surface passivation of GaAs using deposited insulator/GaAs or native oxide/GaAs has not yet yielded satisfactory results [1]. Recently, progress [2] [3] [4] has been reported in reducing the surface states of GaAs by photochemical washing, sulfide treatment, and by rf plasma cleaning the GaAs surface in H_2 and N_2. An alternative way of passivating the GaAs surface is to grow an epitaxial layer of a high quality semiconductor to preserve the interface. With some exceptions [5], the semiconductor is usually chosen to be of a wider band gap than GaAs. High quality GaAs field effect transistors have been fabricated using (Al, Ga)As as a potential barrier layer [6] [7]. The high quality of the AlGaAs/GaAs interface can be attributed to the nearly identical lattice match between GaAs and (Al, Ga)As, and to the ability to fabricate such a heterointerface without growth interruption at the electrical junction.

In comparison to GaAs, ZnSe has a band gap twice that of GaAs; ZnSe possesses a close lattice constant (0.25% mismatch); and the two semiconductors have highly compatible thermal expansion coefficients. The wider band gap of ZnSe (2.67 eV at room temperature), compared to that of (Al,Ga)As (2.0 eV for an Al mole fraction of 0.5), suggests a variety of device applications where ZnSe may present a alternative to (Al, Ga)As for passivation of GaAs. Photoluminescence [8] [9], transmission electron microscopy (TEM) [8-10], and piezo-modulated reflectance spectroscopy [11] indicate high quality pseudomorphic ZnSe is grown by molecular beam epitaxy onto epitaxial

layers of GaAs. The high resolution TEM images suggest that the ZnSe/GaAs interface possesses a similar degree of structural perfection as the (Al, Ga)As/GaAs interface. If in addition the ZnSe/GaAs interface is of similar electrical quality as the AlGaAs/GaAs interface, there are many potential device applications for this II-VI/III-V heterojunction.

In chapter 2 we present an electrical characterization of the pseudomorphic ZnSe/GaAs heterojunction consisting of capacitance - voltage (C-V) and current-voltage (I-V) measurements of metal/ZnSe/GaAs capacitors. Both p and n type GaAs epitaxial layers are investigated. Improvements in the electrical properties resulting from a post growth annealing procedure will be discussed. In chapter 3 we present a field effect transistor where the pseudomorphic ZnSe [8][9] forms a pseudo-insulator on doped epitaxial layers of GaAs [10]. Typical transistor characteristics were exhibited, and channel modulation indicated that the Fermi level could be varied over a large portion of the GaAs bandgap.

CHAPTER 2

ELECTRICAL CHARACTERIZATION OF THE PSEUDOMORPHIC ZnSe/GaAs INTERFACE

2.1 MBE Growth and Device Fabrication

The heterostructures used in this study were grown by two different growth procedures. The first growth procedure consisted of depositing the ZnSe and GaAs in two separate Perkin-Elmer 400 model molecular beam epitaxy (MBE) systems. The growths were performed on (100) p^+ (n^+) GaAs substrates which were readied for insertion into the MBE system using conventional chemical etching techniques. The Be- (Si-) doped 1.5 to 2.0 μm thick p- (n-) GaAs layers were grown at 600 °C from elemental Ga and As_2; The As_2 was derived from a cracking oven. To simulate an "as-grown" surface for subsequent nucleation of ZnSe, the completed GaAs epilayer was passivated with amorphous arsenic [12] [13]. The Mo sample holder containing the In-soldered, arsenic passivated, GaAs sample was then removed from the introduction chamber of the III-V system and transferred in air to the introduction chamber of the II-VI system. The passivating arsenic layer was thermally desorbed at approximately 290 °C in the II-VI analytical chamber and the sample was subsequently moved to the growth chamber for ZnSe epitaxy. Finally, 1000 Å of undoped ZnSe was grown using elemental vacuum distilled sources with a Zn to Se flux ratio of unity and a substrate temperature of 320 °C. The nucleation of the ZnSe on the GaAs epilayer was monitored with reflection high energy electron diffraction. Oscillations in the specular spot, indicative of two-dimensional layer-by-layer growth, were observed for up to 120 periods as reported by Studtmann et al. [10].

The second growth procedure involved growth of the films in a modular Perkin-Elmer model 430 MBE system. Since the ZnSe and GaAs growth chambers in this system are connected by a high vacuum transfer tube, no amorphous arsenic passivation was necessary. Otherwise the growth procedures were similar to those described above.

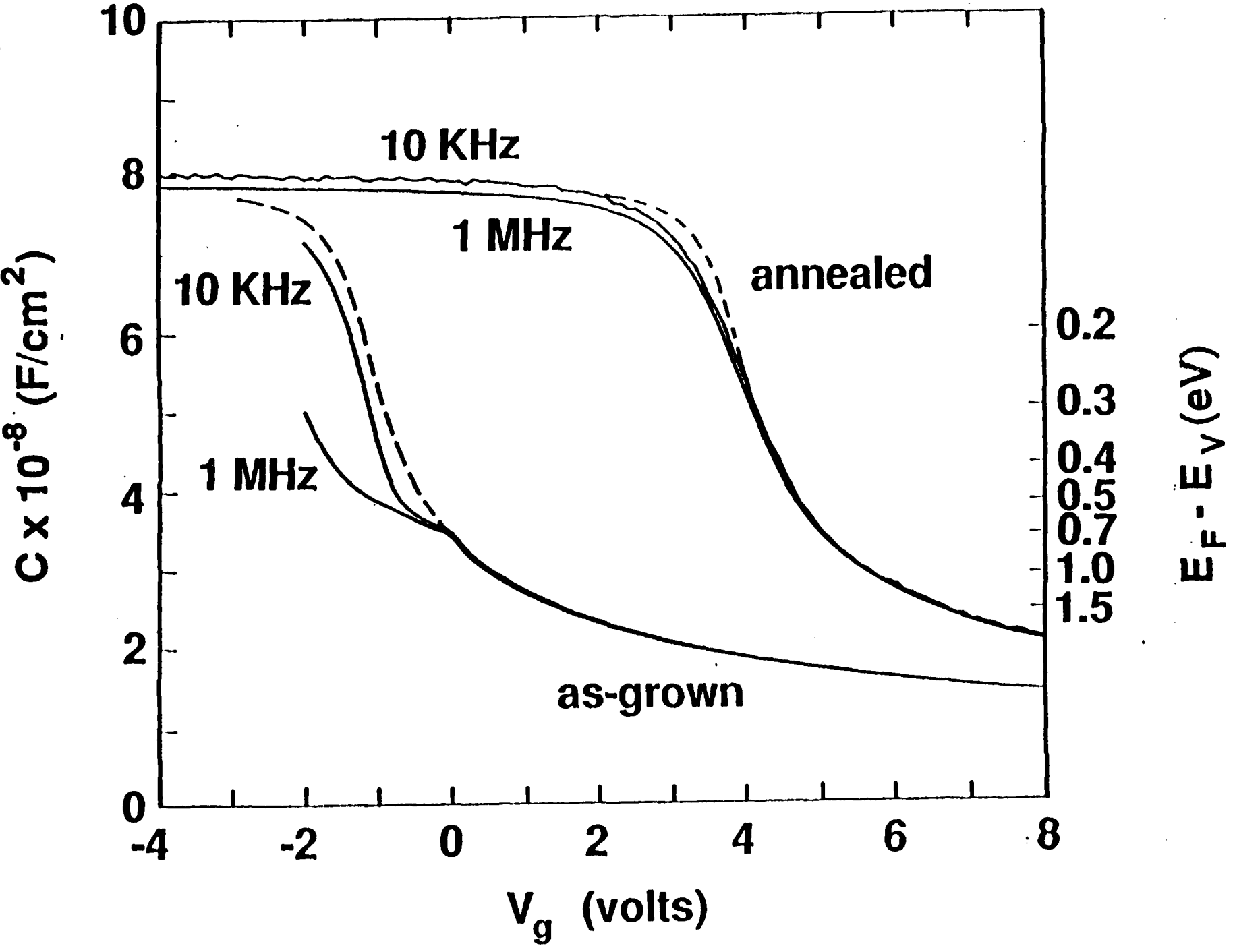
Circular capacitors were formed by evaporating Au or Al on the ZnSe/GaAs heterostructure, followed by a conventional lift-off procedure. The gate areas are either $1.2\times10^{-4}cm^2$ or $3.1\times10^{-4}cm^2$. For each sample grown by the above mentioned methods, two sets of metal/ZnSe/GaAs capacitors from adjacent parts of the wafer were studied: one set consisted of capacitors fabricated on as-grown samples, whereas the other set consisted of capacitors fabricated on samples which were subjected to post growth annealing. The post growth annealing was performed in a conventional tube furnace at 600 °C for 30 minutes in flowing nitrogen gas; a GaAs or ZnSe proximity cap was used. TEM examination has shown that the annealed samples have a similar structural quality as the as-grown samples.

The C-V measurements were made with an HP 4275A or HP 4274A LCR meter and the I-V measurements were made with an HP 4140B picoammeter. Most of the room temperature measurements were made on a probe station, whereas the measurements at 77K were made by mounting the sample on a 24 pin dual-in-line package and submerging it in liquid nitrogen. When the device was mounted in a package, the contact to the gate was made by ultrasonic bonding. All of the data presented in this paper were taken in the dark.

2.2 Hole Accumulation and Interface State Density

Fig. 1 shows the typical C-V characteristics exhibited by the Au/ZnSe/p-GaAs MIS capacitors fabricated on samples grown by the arsenic passivated transfer procedure. For comparison is shown a theoretical deep depletion C-V characteristic for an MIS capacitor with no interface states (dashed lines). The flat band voltage of the theoretical curve has been shifted for ease of comparison. The doping of the GaAs epilayer is determined by C-V profiling, and remains unchanged after the post growth annealing. The thickness of the pseudo-insulating ZnSe layer is 940 Å as measured by TEM. For the annealed sample, the capacitance value under negative gate bias corresponds well with the expected accumulation capacitance. The accumulation hole density is estimated from the annealed C-V curve to be greater than $3\times10^{12}cm^{-2}$. At positive bias ($V_g > 3$ V) a depletion region starts to form in p-GaAs, as indicated by the decrease in the measured capacitance value. This depletion characteristic persists for all the larger positive gate bias voltages; no electron inversion is observed. In depletion bias, the Fermi level at the interface moves from the valence band towards the conduction band, converting the interface from p-type to n-type. Once the total band bending in the GaAs epilayer is close to the GaAs band gap, an inversion layer of electrons is expected to form. However, if the conduction band discontinuity at the ZnSe/GaAs interface is small, such that the rate at which electrons emit over the barrier is larger than the rate at which they are supplied, an inversion layer will not form [14]. In such cases, an equilibrium condition is not obtained and the device will be in deep depletion as seen in Fig. 1. Although the valence band discontinuity for this II-VI/III-V heterojunction has been both predicted and measured by several methods, the values vary widely, and no consensus has been reached [15-18].

The C-V measurements were made over a range of frequencies, however only the 10 kHz and 1 MHz frequency data are shown in Fig. 1 for clarity. The capacitance


10
8
6
4
2
0
-4
-2
0
2
4
6
8
10 KHz
1 MHz
annealed
10 KHz
1 MHz
as-grown
C x 10^-8 (F/cm^2)
V_g (volts)
0.2
0.3
0.4
0.5
0.7
1.0
1.5
E_F - E_V (eV)

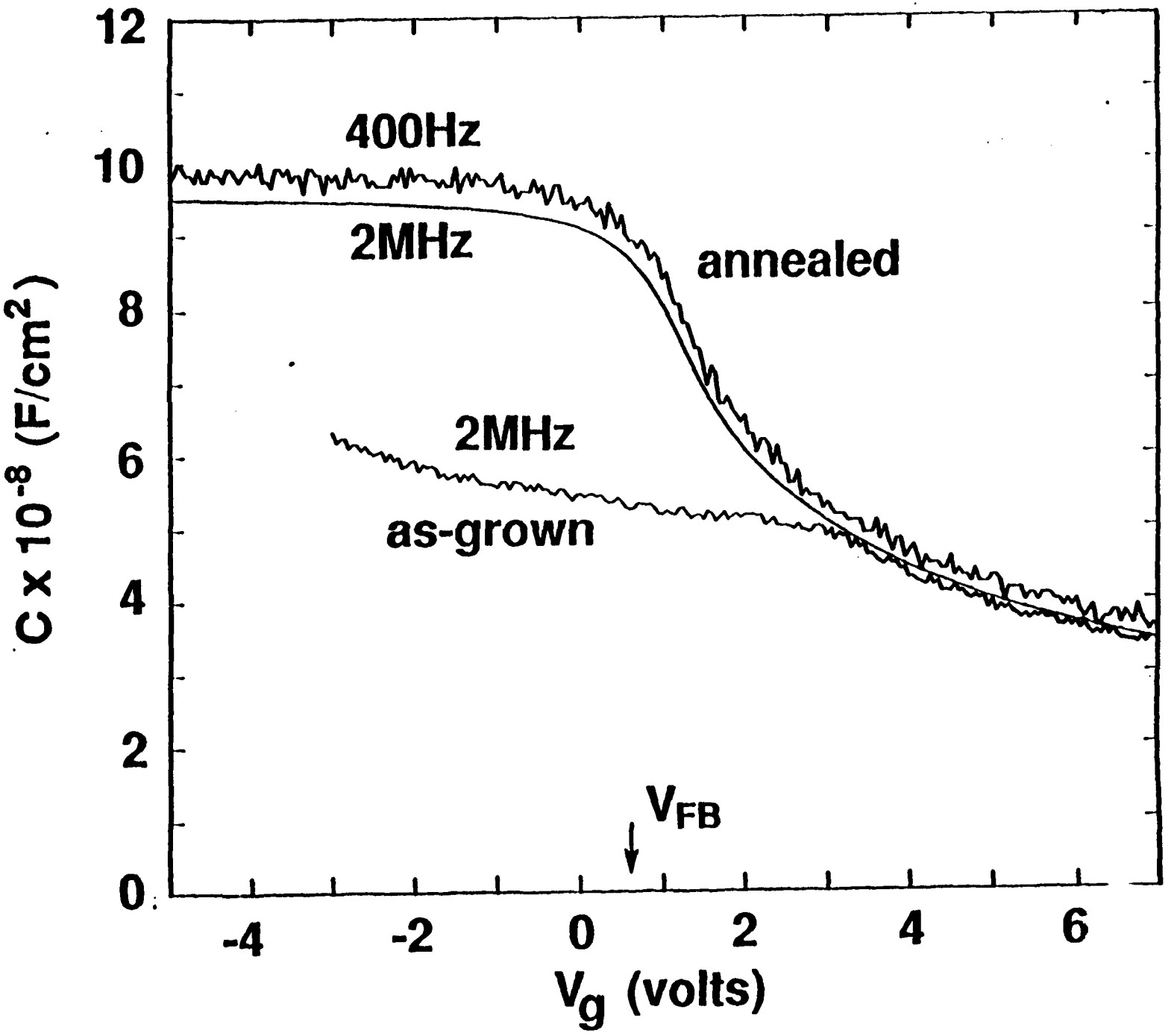
variation in the accumulation region in general was about 2% as the frequency was varied from 10 kHz to 4 MHz. The gate voltage has been swept in both directions, with the hysteresis observed typically less than 100 mV. By comparing the measured C-V data for the annealed capacitors with the theoretical curve (calculated without surface states), it is seen that the Au/ZnSe/p-GaAs capacitors exhibit nearly ideal C-V characteristics.

The large deviation of the flat band voltage from zero in the annealed samples (as shown in Fig. 1), has been completely eliminated in the samples transferred between the growth chambers in an ultra high vacuum. The C-V characteristics obtained from the samples grown in the modular MBE system, after the same post growth annealing procedure (Fig. 2) show a flat band voltage of approximately 0.6 V, and an otherwise similar interface quality to those obtained from the passivated samples transferred in air.

Capacitance-voltage measurements at 77 K show nearly identical characteristics as those taken at room temperature. This presents additional evidence for the conclusion that the shift in the flat band voltage, before and after the post growth annealing in the arsenic passivated samples, is caused by negative fixed charges in the interfacial region, and not by interface states. The change in the flat band voltage going from room temperature to 77 K is typically less than 0.4 volts, corresponding to an interface state density of 2.5×10^{11} cm^{-2} [19]. This feature is in clear contrast with the typical interfacial trap response in terms of the collapse of accumulation capacitance and/or the large shift along the voltage axis in typical "non-epitaxial" GaAs MIS capacitors [20].

In contrast to the C-V data taken on the capacitors which have been thermally processed, are the C-V characteristics exhibited by as-grown capacitors, shown in both Fig. 1 and Fig. 2. The movement of the Fermi level in the 'as-grown' samples is

Fig 2

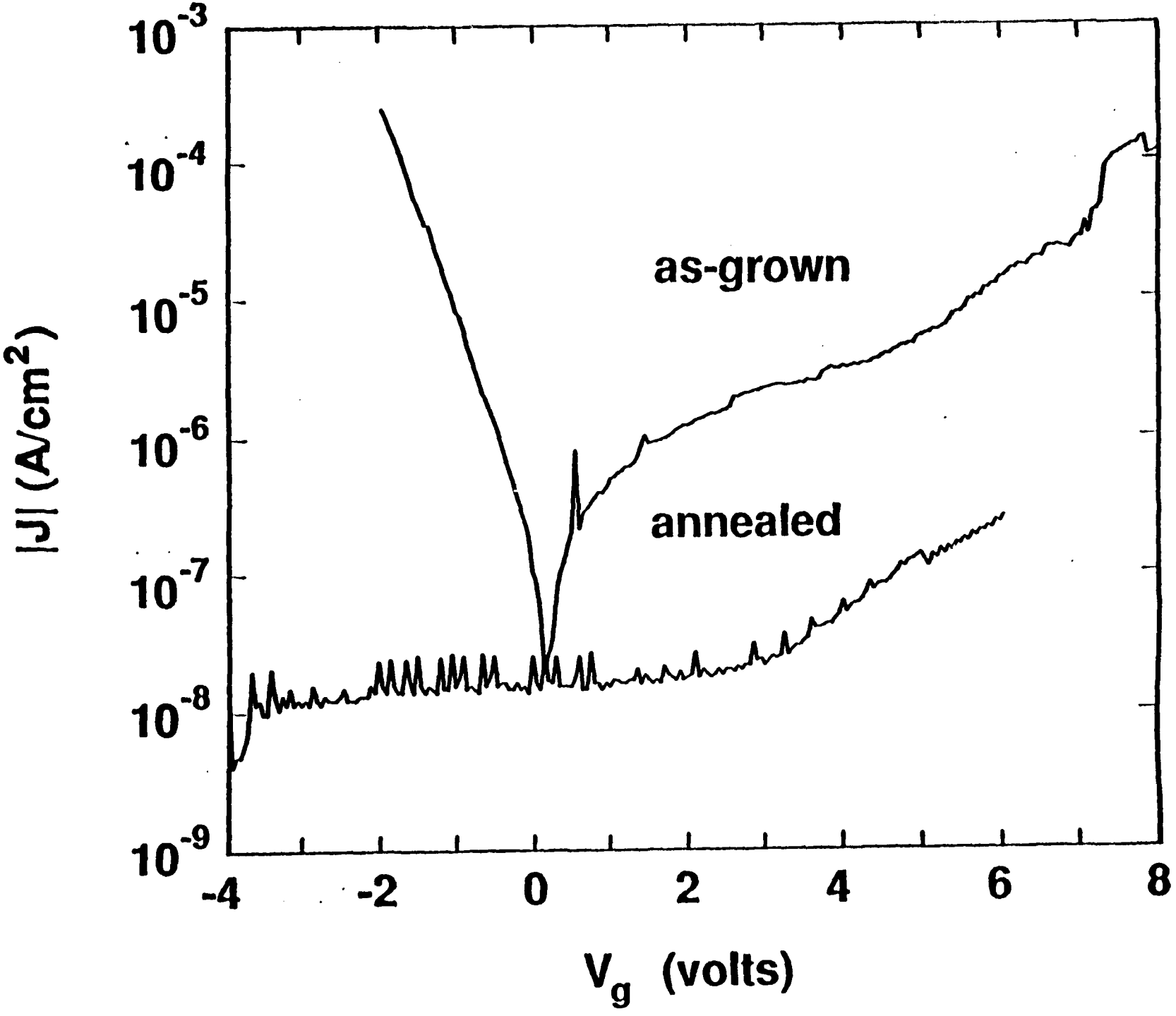

12
10
8
6
4
2
0
400Hz
2MHz
annealed
2MHz
as-grown
V_{FB}
-4
-2
0
2
4
6
C x 10^{-8} (F/cm^2)
V_g (volts)

limited to a range starting around the midgap of GaAs to the conduction band. No frequency dependence of the C-V characteristic has been observed in this depletion portion of the C-V curve. The flow of current from p-GaAs towards the gate limits the gate voltage sweep in the negative direction (towards accumulation). An interface states-related stretching of the C-V curve is also seen in Fig. 2.

A considerable difference in the I-V characteristic was also found between the annealed and as-grown samples. Fig. 3 shows the current density versus voltage for both types of Au/ZnSe/p-GaAs capacitors grown with the arsenic passivated transfer procedure. For the as-grown sample, a rapid increase in current density is seen under negative gate bias, which suggests that the ZnSe layer has not provided good confinement to holes. After the thermal processing however, very little current is seen up to at least -4 V. The current level is typically a few pA for V_g between -4 and 0 volts, which corresponds to the noise limit in our apparatus. The valence band discontinuity at the ZnSe/GaAs interface is now effectively confining holes.

Fig. 4 shows the interface state density (estimated with Terman's method [21]), as a function of position in the GaAs band gap, for both as-grown and annealed samples. The experimental high frequency C-V curves used in the calculation are the same as those shown in Fig. 1. As the Fermi level moves away from the valence band edge towards the GaAs mid-gap, the interface state density decreases below the detectability limit of the method ($5\times10^{10}cm^{-2}eV^{-1}$). In fact, the small interface state density close to the mid-gap can be seen directly from the annealed C-V characteristic in Fig. 1 where very little interface trap related stretching is present for $E_F - E_V > 0.3$ eV. In the as-grown case, the surface state density is routinely greater than 1×10^{12} cm^{-2} eV^{-1}. The surface state densities at positions closer to the valence band cannot be determined in the as-grown structure due to current flow (see Fig. 3). Recent data for surface state densities, obtained on the (Al, Ga)As/GaAs interface reported by Chung et al.[22], is

Fig 3


10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
|J| (A/cm^2)
as-grown
annealed
-4
-2
0
2
4
6
8
V_g (volts)

ZnSe/GaAs
(Al,Ga)As/GaAs
as-grown
annealed
detectability
limit
$D_{it} \times 10^{11}$ (cm^{-2} eV^{-1})
20
15
10
5
0
E_V
0.5
1.0
E_C
$E_{VB} - E_{VB}$ (eV)

Fig 4

also included for comparison in Fig. 4. Although their capacitor structure is somewhat different from the capacitors under study here, it is clear that the surface state densities are of comparable magnitude for the annealed metal/ZnSe/epitaxial p-GaAs capacitors reported in this work.

2.3 Observation of Hole Inversion

The large potential barrier in the valence band at the ZnSe/GaAs interface, demonstrated in the previous section, suggests that a hole inversion layer can be retained in ZnSe/n-GaAs samples. However, hole inversion has not yet been observed in as-grown samples; this may be partially explained by the fact that the leakage rate across the ZnSe layer is too high to prevent the holes from being swept to the gate in the as-grown samples. After the post deposition annealing, C-V measurements show the emergence of a high density mobile hole inversion layer. The first suggestion of the existence of this mobile inversion layer comes from the frequency dependence of the capacitance as shown in Fig. 5. The curves are taken on a sample grown by the As passivated transfer procedure, and the measurements were performed in the dark at room temperature. In these samples, as discussed previously, after annealing a fixed negative charge exists at the ZnSe/GaAs interfacial region, which causes a positive shift in the flat band voltage of metal/ZnSe/p-GaAs capacitors, as seen in Fig. 1. This negative charge, when sufficiently high in density, can induce field inversion in the entire sample [23], creating a reservoir of free holes outside the gated area. As an a.c. perturbation signal is applied to the gate, the free holes in the reservoir flow laterally in and out of the gated area. When this lateral current flow can completely follow the a.c. signal, the charge re-arrangement occurs right at the ZnSe/n-GaAs interface, and the measured capacitance in this low frequency limit corresponds to the capacitance of the insulating layer. At higher a.c. perturbation frequencies, the R-C time constant, originating from

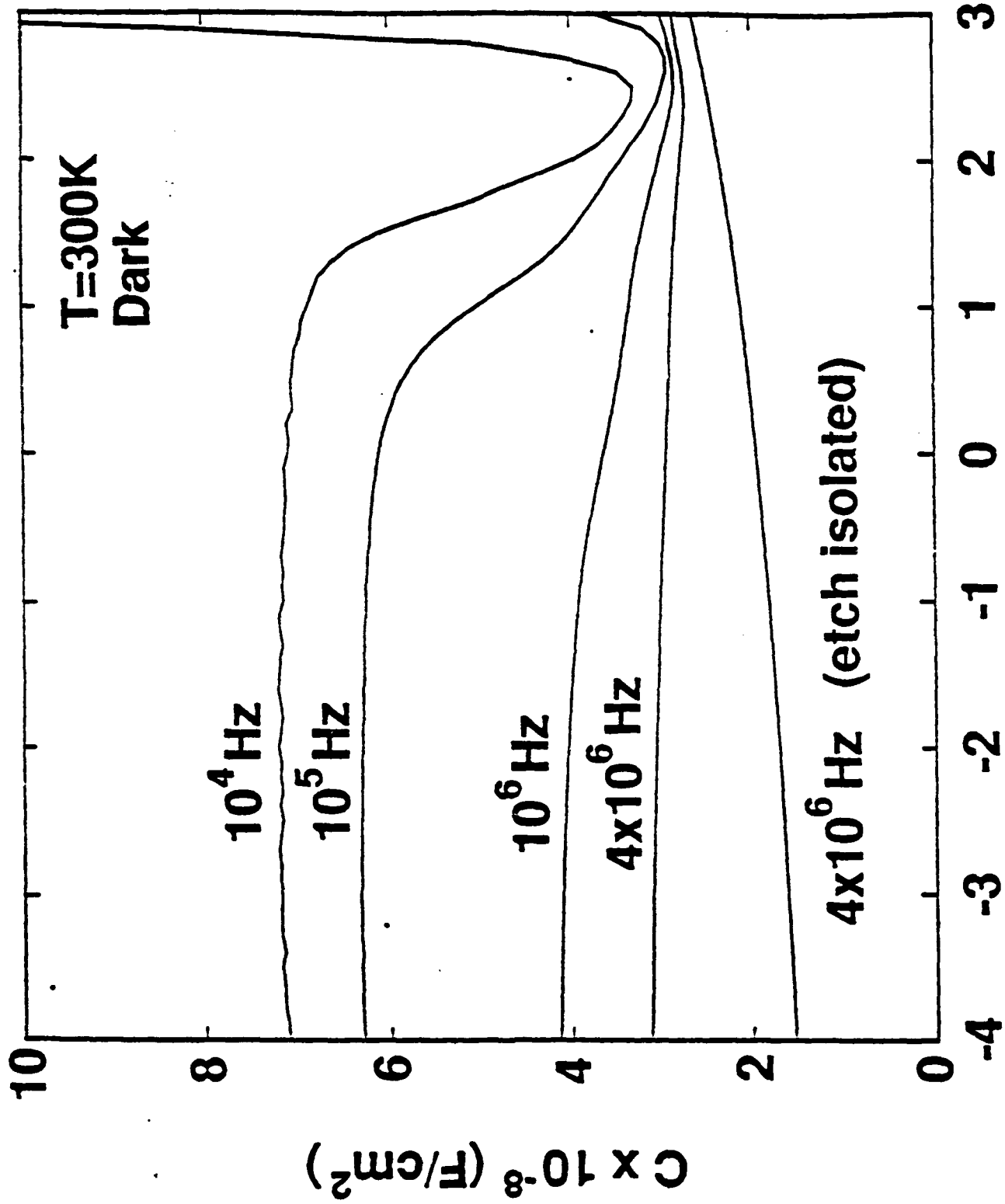

T=300K
Dark
10^4Hz
10^5Hz
10^6Hz
$4x10^6$Hz
$4x10^6$Hz (etch isolated)
C x 10^{-8} (F/cm^2)
V_g (volts)
10
8
6
4
2
0
-4
-3
-2
-1
0
1
2
3

Fig. 5

the distributed resistance to the lateral current flow, eventually becomes large compared to the period of the perturbation signal, and high frequency inversion capacitance results. Assuming the 10 kHz curve to be at the low frequency limit, we obtain a ZnSe insulating layer thickness of 1100 Å, a value within 10% of the thickness obtained from the growth rate.

The full extent of the inversion ledge has not been shown in Fig. 5. However, from the 6 V inversion ledge length shown in the figure, and a ZnSe layer capacitance of 7.9×10^{-8} we estimate the inversion hole concentration to be at least 3×10^{12} cm^{-2}, a value much larger than is usually observed in AlAs/GaAs heterostructures ($\Delta E_v = 0.55$ eV, the largest in the (Al,Ga)As/GaAs system) with a similar GaAs doping density [24]. The gate bias limit in the positive direction is determined by the current flow across the device; the apparent sharp increase in capacitance at gate voltages larger than 2.2 volts is caused by the d.c. current flow.

With a mobile field inversion layer capable of responding to an a.c. perturbation of up to 10 kHz, a deep depletion C-V characteristic cannot be obtained at normal gate voltage sweep rates. However, when the ZnSe outside of the gated area was removed by a selective chemical etching (made of saturated solution of $K_2Cr_2O_7$ in 10 ml H_2SO_4 : 150 ml H_2O), the frequency dependence disappeared since the reservoir of holes no longer exist after the etching. Because the inversion layer is now populated by the much slower thermal generation process, a deep depletion C-V characteristic is observed (bottom curve in Fig. 5). The etching experiment, which consists of a few etching-measuring steps, also shows that after the post growth annealing, the negative charge is located close to the ZnSe/GaAs interface.

The lateral current flow between the field inversion layer and the area under the gate can be controlled by placing a guard ring around the capacitor (Fig. 6). When the guard ring is biased positive, the inversion hole density under the ring decreases,

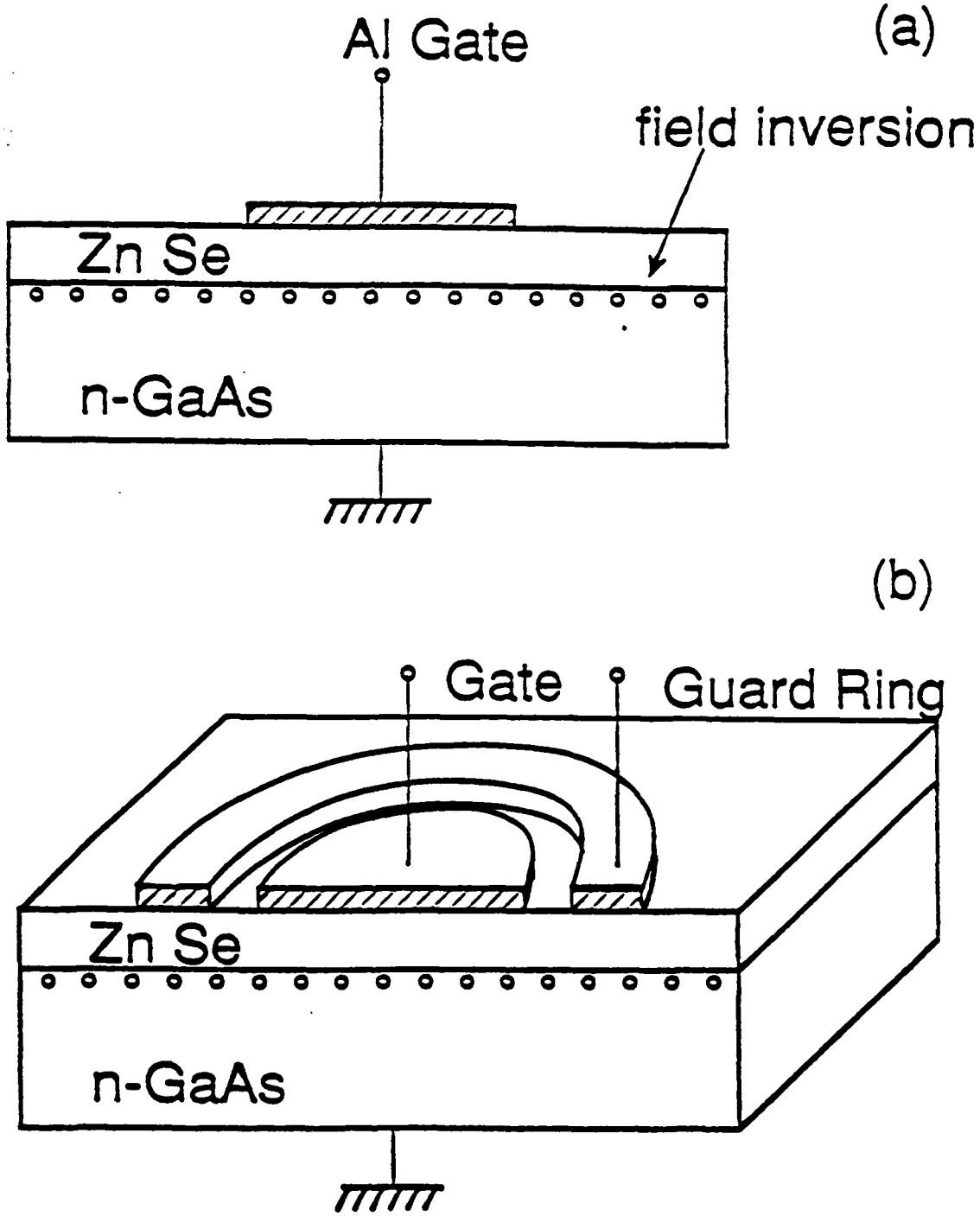

Al Gate
(a)
field inversion
Zn Se
n-GaAs
(b)
Gate
Guard Ring
Zn Se
n-GaAs

Fig 6

adding resistance to the lateral current flow, and increasing the R-C time constant. Therefore, at a fixed frequency, one can switch from a low frequency type of C-V characteristic to a high frequency one, by reverse biasing the guard ring. Fig. 7 shows the C-V characteristics of an Al/ZnSe/n-GaAs ring-dot capacitor at 10 kHz. When the guard ring is at open circuit, the C-V characteristics are similar to the ones shown in Fig. 5. When the guard ring is biased at +2 volts, a high frequency inversion capacitance is observed due to the further increase in the R-C time constant. Deep depletion is not observed with the ring-dot capacitor, because the amount of positive bias that can be applied to the guard ring is limited by the current flow.

A hole inversion layer is also observed in annealed samples grown with a modular MBE system. The C-V and I-V characteristics for a Au/ZnSe/n-GaAs capacitor are shown in Fig. 8. The doping in the n-type GaAs epi layer is 4×10^{16} cm^{-3}, and the insulating ZnSe layer thickness is 990 Å as measured by transmission electron microscopy. Since the fixed negative charge in the interfacial region is greatly reduced for samples grown in a modular MBE system, a field inversion layer does not exist after annealing. Without a field inversion layer, thermal generation is the only source for supplying minority carriers in these samples. At a gate bias sweep rate of 0.01 V/sec, the thermal generation rate can keep up with the gate bias sweep, and a flat hole inversion ledge is observed, as shown in the upper trace. When the gate bias sweep rate is increased to 0.25 V/sec, the generation rate cannot supply holes fast enough, and the C-V characteristic showed a deep depletion, as in the lower trace.

In contrast to the Au/ZnSe/p-GaAs samples where a hole accumulation layer is observed, the Au/ZnSe/n-GaAs sample does not show electron accumulation even at liquid nitrogen temperatures. This observation indicates the presence of a much smaller potential barrier for electrons than for holes at this heterointerface.

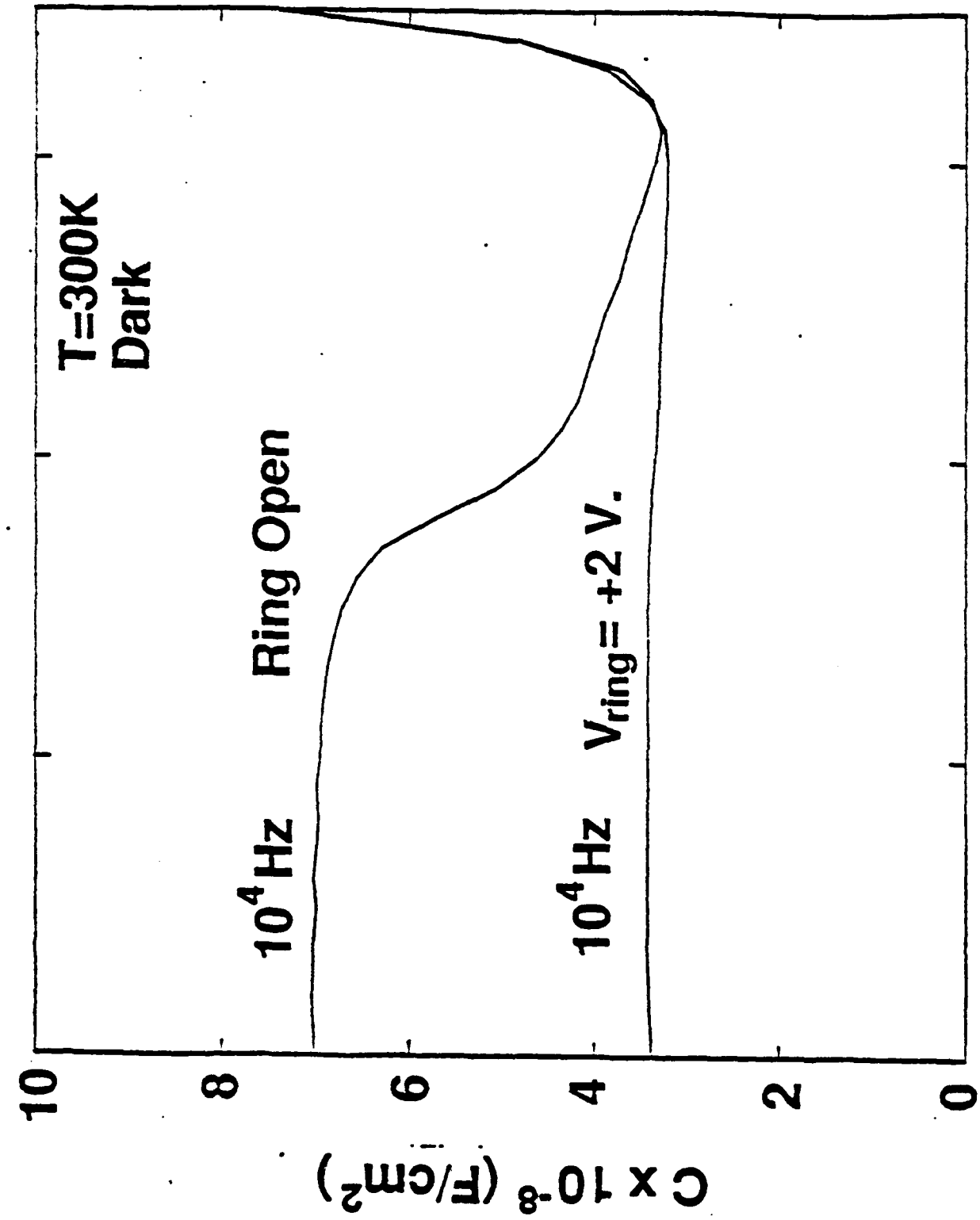
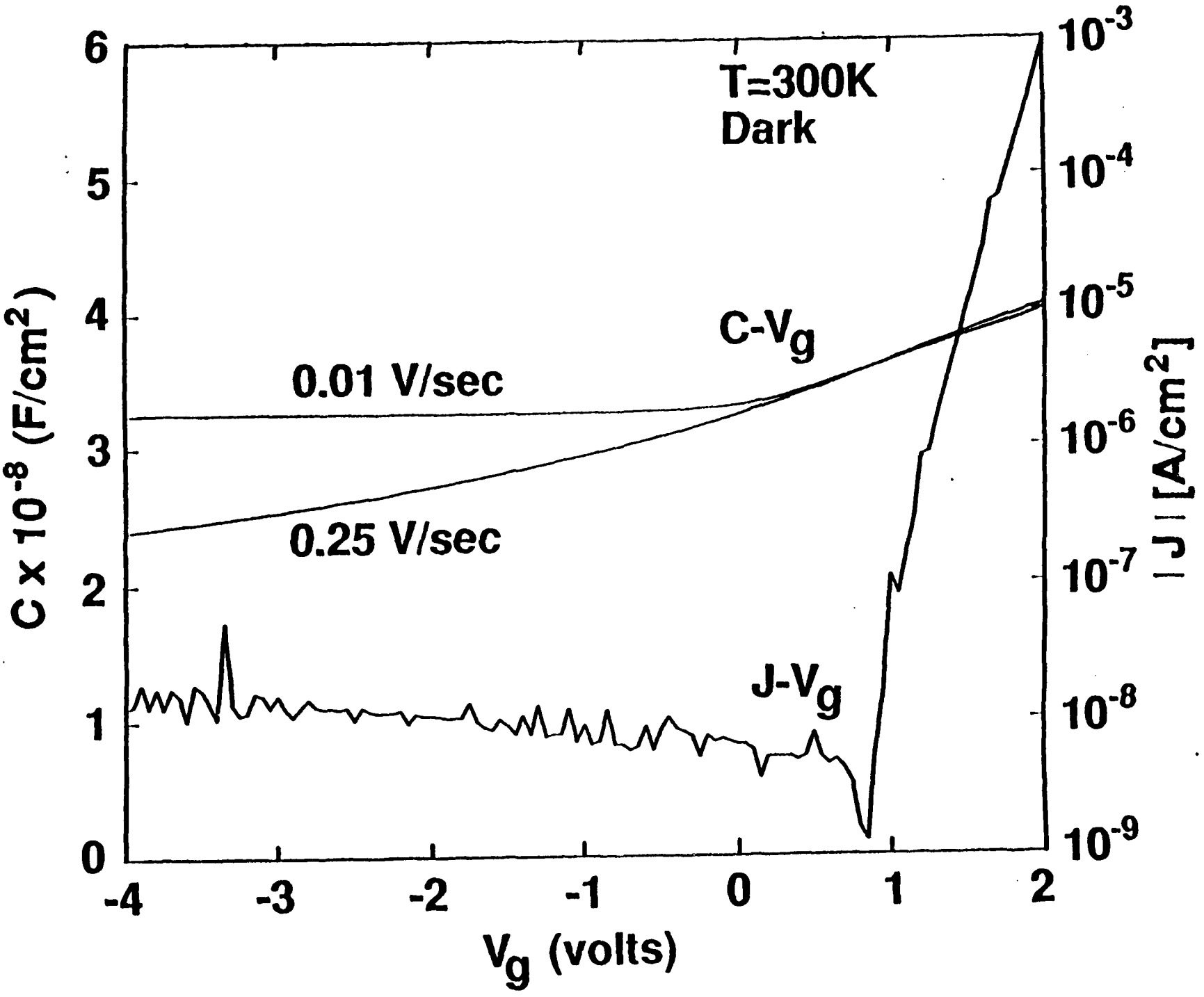

T=300K
Dark
Ring Open
10^4Hz
10^4Hz V_{ring}= +2 V.
C x 10^{-8} (F/cm^2)
10
8
6
4
2
0
-1
0
1
2
V_g (volts)

Fig 7

Fig 8


T=300K
Dark
C-Vg
0.01 V/sec
0.25 V/sec
J-Vg
C x 10-8 (F/cm2)
|J| [A/cm2]
Vg (volts)
6
5
4
3
2
1
0
10-3
10-4
10-5
10-6
10-7
10-8
10-9
-4
-3
-2
-1
0
1
2

2.4 Summary

The C-V characteristics of the annealed epitaxial ZnSe/GaAs heterointerface are seen to compare favorably with the theoretical C-V behavior. The specific changes in the interfacial region produced by the post growth anneal procedure are not yet understood. However, the thermal processing of the interface would be expected to substantially alter both the structural and chemical nature of the II-VI/III-V interface. For example, recent work reported by Tu and Kahn [25] [26] suggests that, for ZnSe evaporated on (100) GaAs at comparable temperatures as reported here, a layer of GaSe can form at the interface; for subsequent high temperature processing (T_{anneal} of 500-540 °C) of their interface, a layer of Ga_2Se_3 was detected by Auger electron spectroscopy. In a model [27] which has been recently proposed, the "optimum" bonding of ZnSe to a GaAs (100) surface will require a degree of mixing at the interface. Further experiments and analysis of the annealed interface are clearly required to understand the physical mechanism giving rise to the improved electrical performance of the epitaxial ZnSe/GaAs interface. Variations to the temperature of nucleation of ZnSe on GaAs, or to the stoichiometries of the epitaxial layers, may also provide an interface capable of exhibiting acceptable electrical properties. Preliminary results, where the interface has been thermally modified during its formation, suggest that similar improvements in the electrical properties of the interface can be achieved, although the ex-situ anneal has thus far resulted in a more ideal C-V characteristic.

CHAPTER 3

PSEUDOMORPHIC ZnSe/n-GaAs FIELD EFFECT TRANSISTORS

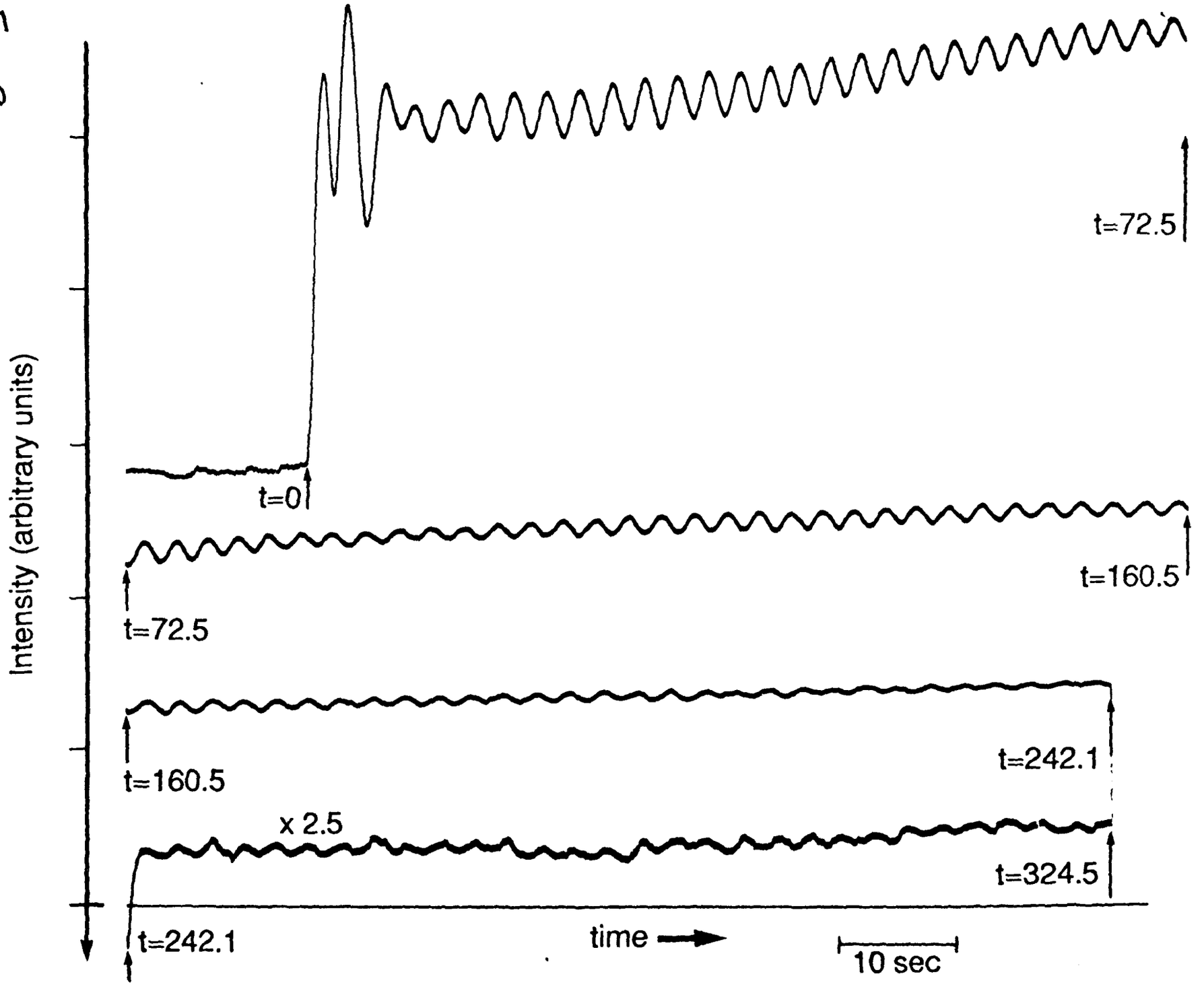
3.1 MBE Growth and transistor fabrication

The heterostructures used for fabrication of the transistors were grown in two separate Perkin Elmer model 400 MBE systems using the interrupted growth technique described in chapter 2. The Si-doped GaAs epilayers (4000Å, $1.5x10^{16}cm^{-3}$) were grown (with elemental Ga and As_2 sources) on undoped, semi-insulating GaAs substrates after the initial deposition of a 1.5 micron buffer layer; the substrate temperature was maintained at 600°C. In order to preserve the "as-grown" GaAs surface for subsequent ZnSe nucleation, the GaAs was passivated with an amorphous layer of arsenic. The passivating layer was deposited by closing the Ga shutter to terminate the growth of the final epilayer and cooling the sample to room temperature (typically requiring 30-35 minutes). The Mo sample holder with the GaAs wafer was then transferred in air from the introduction chamber of the III-V machine to the introduction chamber of the II-VI machine. Auger electron spectroscopy (AES) performed in the II-VI analysis chamber, showed an As peak but no Ga peak, confirming the presence of the passivating layer of As. While the sample remained in the analytical chamber, the As was thermally desorbed at approximately 270°C; at this point AES showed the presence of both As and Ga as well as a small oxygen peak. After the desorption of the oxygen at 510°C, the wafer was transferred to the growth chamber for the growth of the ZnSe. The 1000Å ZnSe epilayer was grown at a substrate temperature of 320°C using elemental Zn and Se sources with a unity Zn to Se flux ratio (as measured with a quartz crystal monitor).

The nucleation of ZnSe on GaAs epilayers, using the aforementioned interrupted growth technique, was monitored by RHEED. Viewing in the [210], one could readily see (with the unaided eye) strong periodic variations in the intensity of the specular spot immediately after opening the Zn and Se source shutters. Fig. 9 shows the recorded intensity variation, lasting for 120 periods and corresponding to one third of the ZnSe growth duration. The intensity oscillations are characteristic of two-dimensional nucleation and layer-by-layer growth where each oscillation represents the completion of the growth of a monolayer of ZnSe [28]. In the case of an As-deficient bulk GaAs substrate (resulting from the common practice of desorbing the oxide in the absence of impinging As for II-VI MBE), the intensity oscillations are not observed as three-dimensional nucleation occurs [8,28]. Recent work [29] suggests that two-dimensional growth can occur on a GaAs substrate if the oxide desorption occurs in the presence of an As flux.

X-ray diffraction measurements [30] of the lattice parameter of ZnSe (grown on GaAs) as a function of film thickness have revealed a substantial decrease in the perpendicular lattice parameter for ZnSe film thicknesses in the vicinity of 2000Å. The x-ray data is interpreted as an indication of ZnSe layer thicknesses for which strain, arising from the 0.25% lattice constant mismatch, is being relieved through the generation of misfit dislocations. Consequently, the 1000Å ZnSe films were expected to be pseudomorphic such that the parallel lattice parameter of the epilayer was the same as that of the substrate; in this case misfit dislocations have not been generated to disrupt the coherent interface. The microstructure of the ZnSe/GaAs heterointerface was examined with cross-sectional and plan-view [9] transmission electron microscopy (TEM). Fig. 10 shows a cross-sectional bright field image of the 1000Å ZnSe epilayer grown on the MBE-grown GaAs layer. The interface appears as a sharp straight line with the epilayer free of the evidence of threading dislocations. High resolution

Fig 9


Intensity (arbitrary units)
t=72.5
t=0
t=160.5
t=72.5
t=242.1
t=160.5
x 2.5
t=324.5
t=242.1
time
10 sec

300A

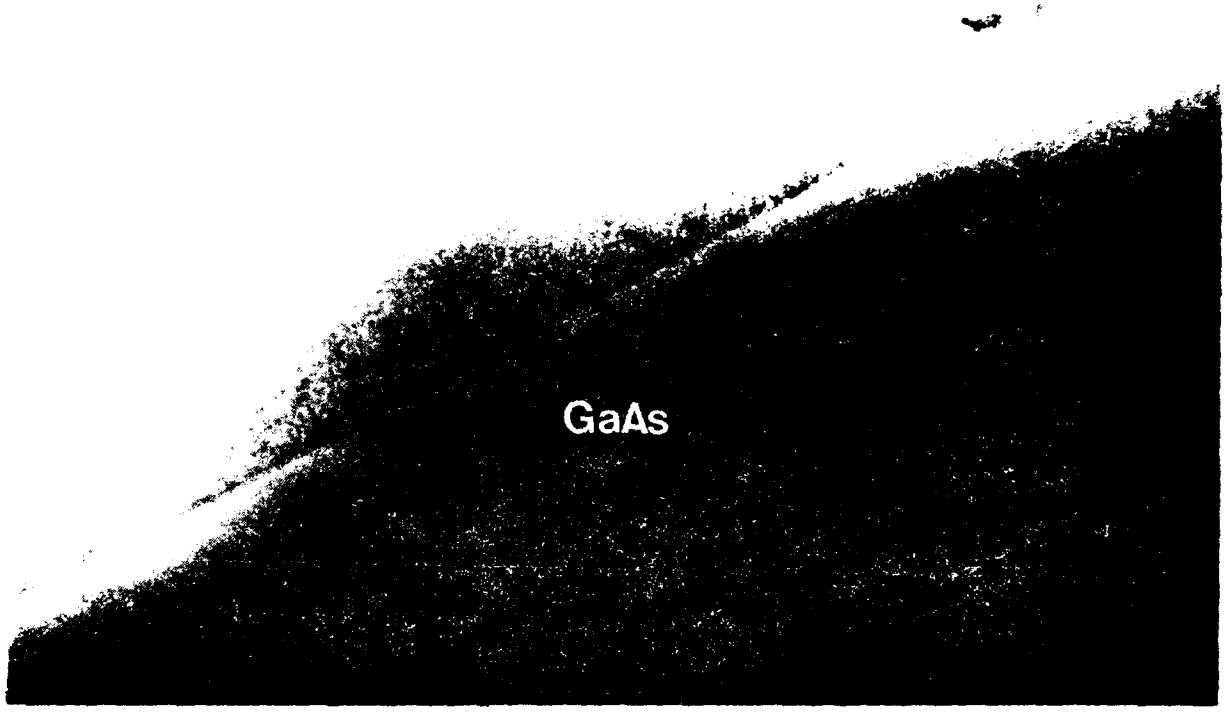


Fig 10

electron microscope images [9] show defect-free, coherent contact between the two crystals suggesting that the ZnSe/GaAs interface is similar in perfection to the interface seen between (Ga,Al)As and GaAs. Photoluminescence studies [8] of the 1000Å ZnSe layer, the TEM investigations [8,9], and x-ray diffraction measurements [30] of the lattice parameter all confirm the pseudomorphic nature of the film.

A schematic diagram of the planar geometry, depletion mode devices is shown in Fig. 11. The transistors reported here had gate width/length of 45μm/45μm and 45μm/2μm. The devices were isolated using wet chemical etching where the ZnSe was selectively etched at 100Å/sec with 400ml H_2O : 0.2g $K_2Cr_2O_7$: 4ml HNO_3. A second chemical etch of 400ml H_2O : 12ml H_3PO_4 : 3ml H_2O_2 removed 0.5μm of GaAs. Isolation of the devices was confirmed by electrical probing. The source and drain were defined by a liftoff of thermally evaporated 88% Au-12%Ge (3000Å) and alloyed at 450°C for 90 seconds. The gate metal was 3000Å of aluminum and was also defined by liftoff.

3.2 Electrical Characterization

Fig. 12 shows the I_D vs V_{DS} transistor characteristics of the long channel device at room temperature. (The top curve in all figures represents a gate voltage of 0 volts and the voltage is stepped -0.5 volts per curve.) The long channel FET curves show good depletion mode characteristics with complete pinchoff and current saturation [31]. The modulation of the channel carrier concentration indicates that the Fermi level positioning at the ZnSe/n-GaAs (epi) interface can be varied by at least 0.6eV. For normal operation of the device, $2.5 \leq V_{GS} \leq 0$, the gate current is less than 3nA. As would be expected in a semiconductor heterostructure, measurable gate current is observed for a sufficiently positive gate bias. The transconductance of the device at zero gate voltage is 3.5mS/mm. Although the transconductance (g_m) appears to be

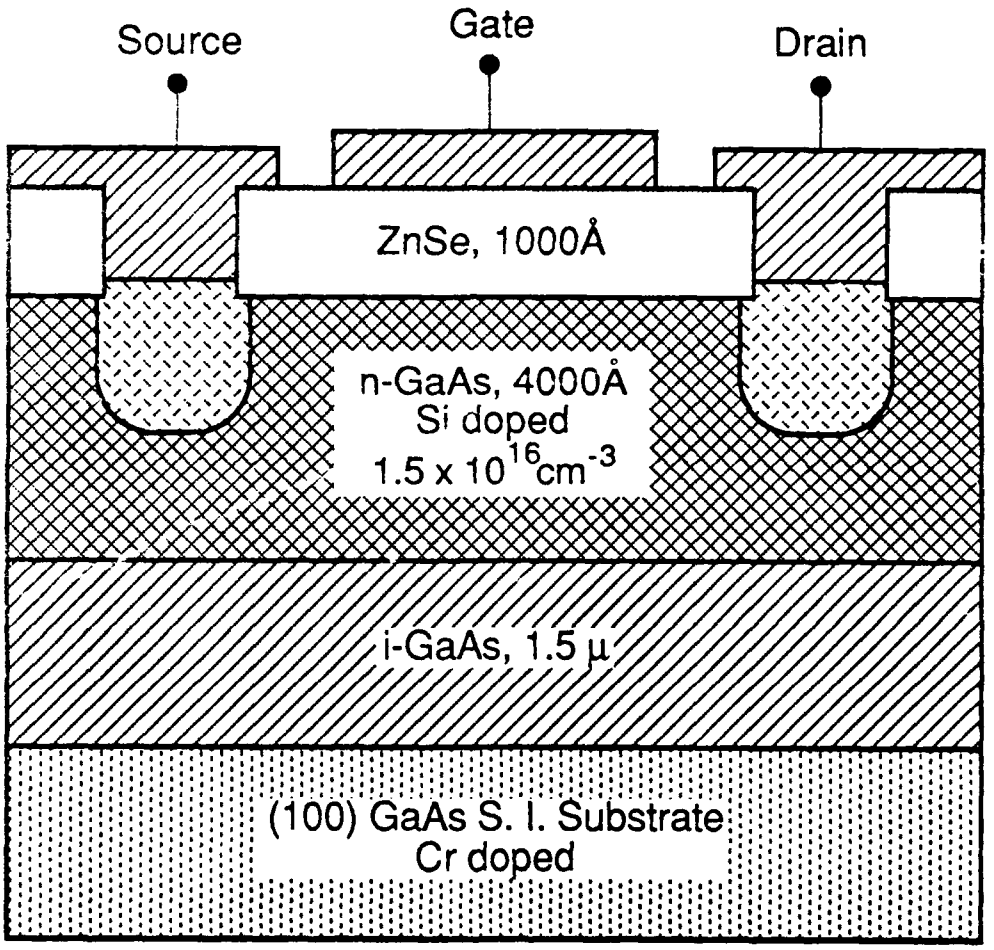

Source
Gate
Drain
ZnSe, 1000Å
n-GaAs, 4000Å
Si doped
1.5 x 10^16 cm^-3
i-GaAs, 1.5 μ
(100) GaAs S. I. Substrate
Cr doped

Fig 11

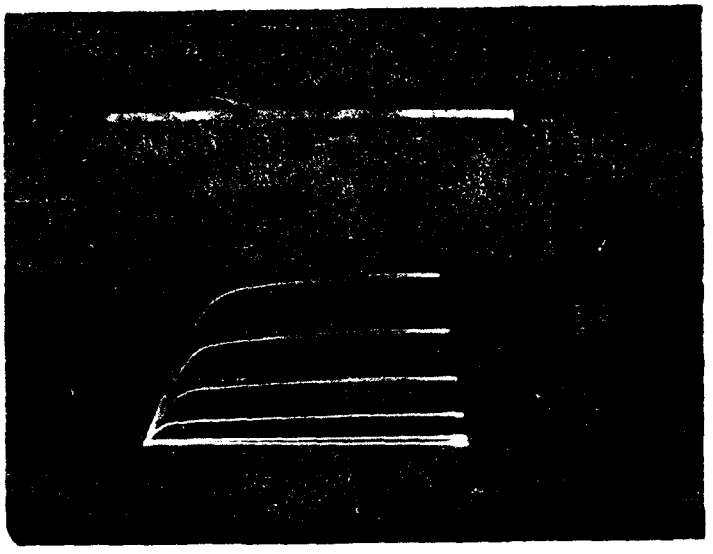


Fig 12

low, g_m agrees fairly well with a theoretical calculation of g_{max} when the effect of series resistance (R_s) is included. Parallel conduction in the ZnSe is not considered as contributing to the low g_m because resistivity measurements of thick ZnSe grown under similar conditions have demonstrated substantial resistivity parallel to the interface. A g_{max} of 8.5mS/mm is calculated using $qN_Da\mu Z/L$ where q, N_D, a, μ, Z, and L are the electronic charge, donor density, channel thickness, electron mobility, gate width and gate length respectively. R_s in this nonoptional device is large (180Ωmm) due to the large source/drain-to-gate spacing of 20μm and contributes to the low transconductance; the calculated g_m corrected for series resistance is 5.1mS/mm. N_D is confirmed from a measurement of $1/C^2$ versus voltage and is estimated from N_D. The breakdown between the gate and the drain is about 42V which is expected for this value of N_D.

The I-V curves for the 2μm gate device at room temperature and 77°K appear in Fig. 13(a) and 13(b) respectively. Compared with Fig. 12, the transconductance in this transistor is almost independent of gate potential, a characteristic of a velocity saturated GaAs transistor. The measured transconductance is 6.5 mS/mm and the corrected g_m including the series resistance (160Ωmm) is 13.5 mS/mm. The FET characteristics show slight looping at room temperature indicating the presence of charge trapping. Most likely, the ZnSe/n-GaAs epilayer interface is contributing to the charge storage. As is seen in Fig. 13(b), the looping is not present at 77°K.

Although small looping in the FET characteristics is present, the growth of the ZnSe/GaAs (epi) heterostructure is in its infancy. For the devices reported here, a particular set of growth conditions were employed resulting in one single interface condition. The strength of the interrupted MBE growth process is the ability to systematically control the interface and film properties to reduce the number of states that contribute to charge trapping. Growth parameters such as substrate temperature, flux

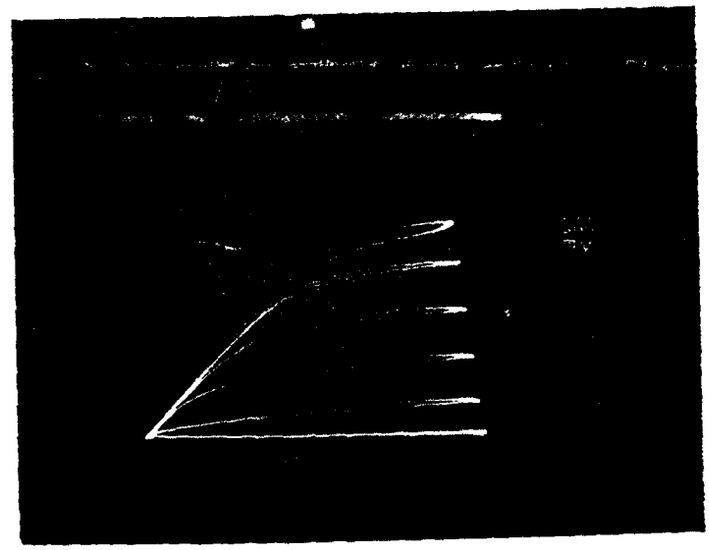


Fig 13a

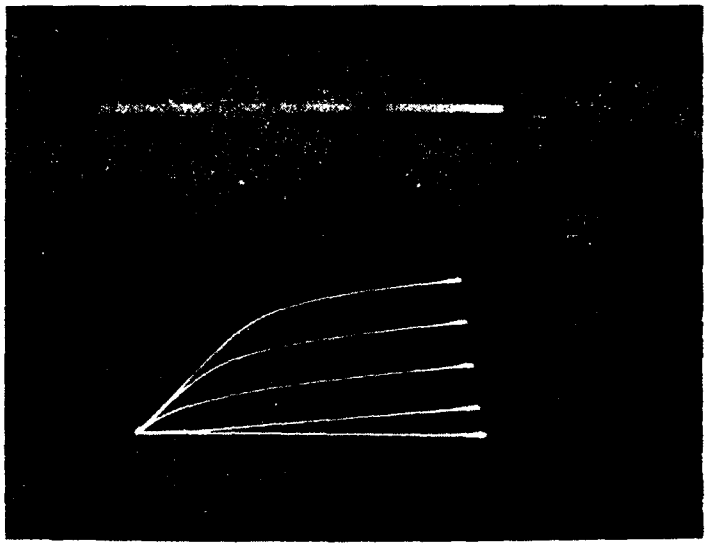


Fig 13b

ratios, and crystal stoichiometry can be used to alter the interface leading to improved device performance.

3.3 Summary

In summary, we have fabricated the first field effect transistors incorporating the ZnSe/n-GaAs heterojunction; the heterojunction was formed by interrupted growth using two separate MBE systems. RHEED intensity oscillations revealed a two-dimensional nucleation and a layer-by-layer ZnSe epitaxy on MBE-grown GaAs epi-layers. The electrical characteristics of the transistors were nearly ideal, but showed some hysteresis consistent with charge trapping. With improved techniques for hetero-junction fabrication such as reported here, the utilization of the ZnSe/GaAs heteroin-terface for device applications appears promising.

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Appendix A

Journal Publications and Conference Presentations acknowledging support from Contract N00014-87-K-0522.

Journal Publications

[1] G. D. Studtmann, R. L. Gunshor, L. A. Kolodziejski, M. R. Melloch, J. A. Cooper, Jr., R. F. Pierret, and D. P. Munich, "Pseudomorphic ZnSe/n-GaAs Doped-Channel Field-Effect Transistors by Interrupted Molecular Beam Epitaxy," Appl. Phys. Lett. 52, 1249 (1988).

[2] Q-D. Qian, J. Qiu, M. R. Melloch, J. A. Cooper, Jr., L. A. Kolodziejski, M. Kobayashi, and R. L. Gunshor, "Low Interface State Density at an Epitaxial ZnSe/Epitaxial GaAs Interface," Appl. Phys. Lett. 54, 1359 (1989).

[3] Q-D. Qian, J. Qiu, M. Kobayashi, R. L. Gunshor, M. R. Melloch, and J. A. Cooper, Jr., "Electrical Characterization of an Epitaxial ZnSe/Epitaxial GaAs Heterointerface," J. Vac. Sci. and Tech. B, July/August 1989.

Conference Presentations

[1] R. L. Gunshor, L. A. Kolodziejski, M. R. Melloch, N. Otsuka, and A. V. Nurmikko, "II-VI/III-V Heterointerfaces: Epilayer-on-Epilayer Structures," NATO Advanced Research Workshop on Growth and Optical Properties of Wide Gap II-VI's Low Dimensional Semiconductors, Regensburg, F. R. Germany, August 2-5, 1988.

[2] Q-D. Qian, J. Qiu, G. D. Studtmann, R. L. Gunshor, L. A. Kolodziejski, M. R. Melloch, J. A. Cooper, Jr., and M. Kobayashi, "Passivation of Epitaxial GaAs with Epitaxial ZnSe," 5th International Molecular Beam Epitaxy Conference,

Sapporo, Japan.

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[5] Q-D. Qian, J. Qiu, M. Kobayashi, R. L. Gunshor, M. R. Melloch, and J. A. Cooper, Jr., "Electrical Characterization of an Epitaxial ZnSe/Epitaxial GaAs Heterointerface," 16th Conference on Physics and Chemistry of Semiconductor Interfaces," Bozeman, Montana, Feb. 7-9, 1989.

[6] Q-D. Qian, J. Qiu, M. Kobayashi, R> L. Gunshor, L. A. Kolodziejski, M. R. Melloch, J. A. Cooper, Jr., J. M. Gonsalues, and N. Otsuka, "Low Interface State Density at an MBE Grown Pseudomorphic ZnSe/Epitaxial GaAs Interface," March Meeting of the American Physical Society, St. Louis, Missouri, March 20-24, 1989.

[7] Q-D. Qian, J. Qiu, M. Kobayashi, R. L. Gunshor, L. A. Kolodziejski, M. R. Melloch, J. A. Cooper, Jr., J. M. Gonsalues, and N. Otsuka, "Low Interface State Density at a Pseudomorphic ZnSe/Epitaxial GaAs Interface," 1989 Spring Meeting of the Materials Research Society, San Diego, CA, April 24-29, 1989.