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ADVANCED GaAs PROCESS MODELING

Thomas W. Sigmon

Stanford Electronics Laboratory
Stanford University
Stanford, CA 94305

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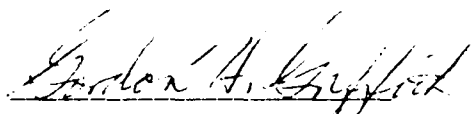
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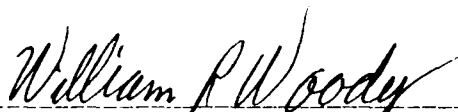


WILLIAM C. MITCHEL
Project Monitor
Electronic & Optical Materials Branch



GORDON H. GRIFFITH, Chief
Electronic & Optical Materials Branch
Electromagnetic Mat'ls & Surv. Division

FOR THE COMMANDER



WILLIAM R. WOODY, Actg Chief
Electromagnetic Mat'ls & Surv Div
Materials Laboratory

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<p>(U) The objective of the program was to develop physical models for substrate and process defects and variations which affect the electrical parameters of MESFET structures fabricated on this material by direct ion implantation processes. Verification of these models was to be carried out where possible by fabrication of specially designed device structures capable of providing statistically significant data. In order to remove, as much as possible, unwanted process variations all device processing was carried out under a subcontract with the Rockwell MRDC GaAs pilot line facility. The primary successes of the program include: 1) development of a physical model to explain the effect of dislocations on the fluctuations in threshold voltage observed experimentally, 2) development of analytical Pearson IV models for the profiles of the technologically significant ions Si, Se, and Be in 100 oriented GaAs for specific tilt and rotation angles of the substrates with respect to the implant beam, 3) development of a one dimensional device and process simulator which allows exploration of the effect of certain process variables on the significant MESFET electrical parameters.</p>			
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I. EXECUTIVE SUMMARY

The Advanced Growth and Process Modeling for GaAs Program was conducted by the GaAs process modeling and technology group of Professor T.W. Sigmon in the Solid State Laboratory of the Electrical Engineering Department at Stanford University. The period of performance began in December 1985 and ended in October 1988. This document is the final report of the program and presents and discusses the major achievements and significant findings.

The objective of the program was to develop physical models for substrate and process defects and variations which affect the electrical parameters of MESFET structures fabricated on this material by direct ion implantation processes. Verification of these models was to be carried out where possible by fabrication of specially designed device structures capable of providing statistically significant data. In order to remove, as much as possible, unwanted process variations all device processing was carried out under a subcontract with the Rockwell MRDC GaAs pilot line facility.

The technical approach of the program was to concentrate on direct ion implanted MESFET process technology fabricated on EL2 compensated semi-insulating substrates. This decision was supported by the improved manufacturability provided by this approach over epi-growth processes. Following our assessment of this technological approach to fabricate MESFET circuits and to complement other programs being administered by AFWAL/MLPO the following specific areas were singled out for investigation.

- 1.) Development of models to determine the effect of substrate impurities and deep levels (EL2, Cr) on MESFET electrical parameters.
- 2.) Development of analytical models to calculate ion implantation profiles in GaAs including *both* channeling and encapsulation effects.
- 3.) Development of a process model (GATES) to allow calculation of the effects and study the sensitivity of the above effects on MESFET electrical parameters.
- 4.) Development of a physical model for how dislocations affect MESFET electrical parameters, extension of this model to *waferscale* by the use of Monte Carlo techniques.

- 5.) Design of a Dense Row Pattern (DRP) of MESFETs and the appropriate automatic test algorithms for verification of the predictions of the above models.

The primary successes of the program include: i.) development of a physical model to explain the effect of dislocations on the fluctuations in threshold voltage observed experimentally, ii.) development of analytical Pearson IV models for the profiles of the technologically significant ions Si, Se, and Be in <100> oriented GaAs for specific tilt and rotation angles of the substrates with respect to the implant beam, iii.) development of a one dimensional device and process simulator which allows exploration of the effect of certain process variables on the significant MESFET electrical parameters.

II. MECHANISM OF EL2 EFFECTS ON GaAs FIELD-EFFECT TRANSISTOR THRESHOLD VOLTAGES

2.1 Background

In recent years much effort has been devoted to characterizing the concentration of the deep-donor EL2, present in semi-insulating liquid-encapsulated-Czochralski (LEC)-grown GaAs (1-3). The average EL2 concentration varies across wafers, possibly originating from changes in the thermal stress during boule growth (4). Also, local fluctuations in the EL2 concentration over 50- to 500- μm distances have been observed around individual dislocations and around clusters or lines of dislocations (1-3).

These fluctuations in EL2 concentrations are a possible candidate for explaining threshold voltage fluctuations in ion-implanted metal-semiconductor field-effect transistors (MESFETs). Dobrilla et al. (2) measured threshold voltages in ion-implanted MESFETs where the EL2 concentration varied from 7 to $10 \times 10^{15} \text{ cm}^{-3}$. A linear correlation was found; V_{th} decreased by 63 mV per 10^{15} EL2/cm^3 , though the magnitude of the variations over the range of $3 \times 10^{15} \text{ cm}^{-3}$ were as small as the random fluctuations in threshold voltages.

In this work we discuss a mechanism for EL2 effects on threshold voltages which focuses on its role in fixing the substrate barrier height. We are not so much concerned with the presence of EL2, but with its absence, due to outdiffusion.

2.2 Model and Calculations

Makram-Ebeid et al. (6) found that for capless annealing with AsH_3 overpressures at temperatures between 750 and 900°C, the EL2 concentrations varies as

$$[\text{EL2}] = [\text{EL2}]_{\infty} \operatorname{erf} \left[x/2\sqrt{Dt} \right], \quad (2.1)$$

where $2\sqrt{Dt}$ is between 0.5 to 5 μm for 20 min anneals. For other annealing caps, similar diffusion lengths, but more complicated profile types were observed. Since most MESFETs are fabricated with implant depths $x < 1 \mu\text{m}$, and are annealed for 10-30 min at these temperatures, EL2 outdiffusion can be present to some degree in all furnace-annealed, ion-implanted MESFETs.

To explain our model we consider the energy band diagrams associated with two possible EL2 outdiffusion profiles, EL2 and EL2', in Fig. 2.1. For EL2', annealing for a longer time or higher temperature is assumed. At the

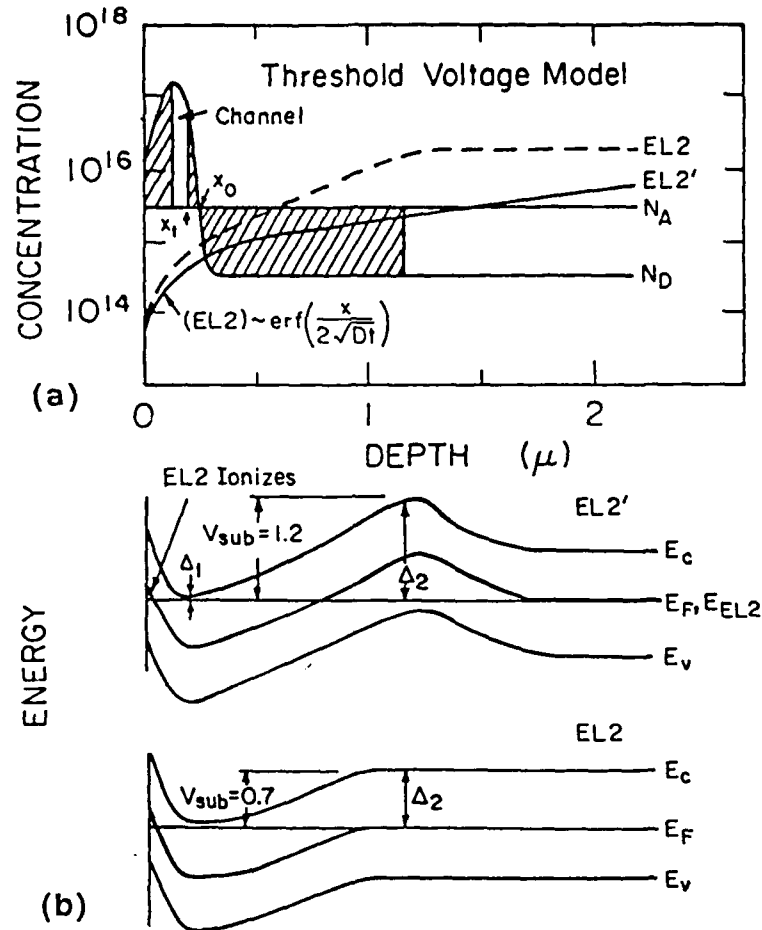


Fig. 2.1. (a) Concentration profiles of implanted donor (N_D), background acceptor (N_A), and two different EL2 profiles. The shaded areas show the substrate and Schottky barrier depletion regions. (b). Energy band diagrams for the profiles EL2 and EL2' in 1(a).

intersection x_0 , between the implanted shallow donor and the background shallow acceptor [usually carbon, present in concentrations of 1 to $6 \times 10^{15} \text{ cm}^{-3}$ in LEC GaAs (7)], a depletion region forms around a barrier of height V_{sub} . The magnitude of V_{sub} depends on the differences between $\Delta_2 = E_c - E_F$ on the substrate side of the region and Δ_1 ($\sim 0.05 \text{ V}$) on the channel side. For EL2 concentrations higher than the acceptor concentration on the substrate side,

the Fermi level is pinned to the mid-gap EL2 energy level, so that $\Delta_2 \sim 0.75$ V and $V_{\text{sub}} \sim 0.7$ V. When EL2' is less than the acceptor concentration on the substrate side, the Fermi level will be closer to the valence band so that $\Delta_2 \sim V_{\text{sub}} = 1.2$ V $\sim E_{\text{gap}}$. The larger substrate barrier height in the latter case pushes the depletion region in the n-layer toward the surface, reducing the width of the channel, and resulting in less negative threshold voltages being needed to fully deplete the channel.

Therefore there are two possible ways EL2 can affect threshold voltages. If EL2 is initially dominant on the substrate side, annealing for longer times can shift the substrate barrier height, and therefore V_{th} . If the anneal time at the average bulk EL2 concentration is such to give a substrate barrier height between 0.7 and 1.2 V, local fluctuations in the bulk EL2 concentration can give fluctuating threshold voltages.

To test these ideas, two model calculations are made. In the abrupt-depletion model, (5) we integrate over the substrate depletion region and do a three-component Fermi-level analysis on the substrate side to determine self-consistently how large V_{sub} and the depletion widths must be to satisfy $V_{\text{sub}} = \Delta_2 - \Delta_1$. In this model, the contribution of the ionized EL2 in the depletion region is neglected; only its effect in determining the Fermi-level position at the edge of the depletion region is included.

In a second calculation, Poisson's Equation (8) is solved for the electron concentration $n(x)$, including the shallow donor and acceptor and partially ionized EL2. No bias is applied, and as a boundary condition, $dn(x)/dx$ is assumed to vanish at the surface. Figure 2.2 shows the calculated $N_{\text{D}}(x)$, $N_{\text{A}}(x)$, and electron concentrations $n(x)$ for various EL2 outdiffusion profiles. The shape of the implanted donor profiles is not Gaussian, but has a significant channeling tail (See Section IV) measured using secondary-ion mass spectroscopy (SIMS) (9). For Si ions implanted with energies less than 200 keV, these tails are nearly independent of the wafer orientation for tilt angles greater than 4° . However, the electron concentration profiles are nearly always Gaussian. In the abrupt-depletion approximation, $n(x)$ vanishes for $x > x_t$, where x_t is the channel edge of the substrate depletion region. In the Poisson solution, $n(x)$ does not vanish, but shows a Debye tail. In the literature, LSS donor profiles are often compared with electron profiles, measured using the capacitance-voltage (CV) technique (10). Figure 2.2 demonstrates that the apparent good agreement between Gaussian LSS implant

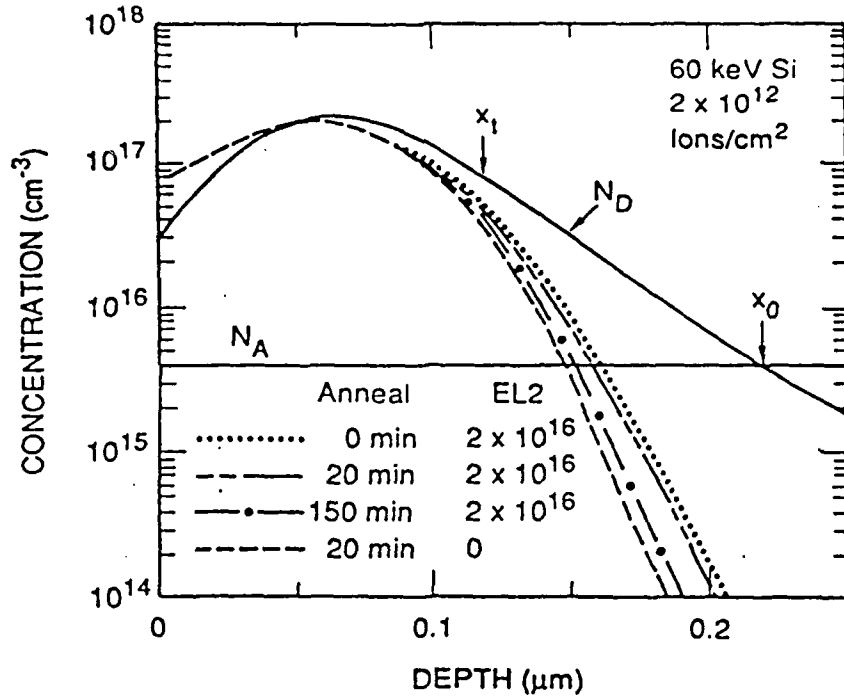


Fig. 2.2. Donor N_D , acceptor N_A , and calculated electron concentration profiles for several different outdiffused EL2 profiles, assuming implanted 60 keV Si ions with a dose of 2×10^{12} ions/cm². (The anneal time in minutes and the bulk EL2 concentration in 10^{16} cm⁻³ are given). The positions of the substrate junction x_0 and the shallow edge x_t of the substrate junction in the abrupt depletion approximation are shown by arrows. The implanted profile is from a fit to SIMS data.

profiles and CV profiles occurs because ion implantation into EL2 (or Cr) compensated GaAs is like implantation into p-layers; the donor channeling tails are consumed by the background acceptor concentrations.

For the EL2 profiles used to calculate the electron profiles shown in Fig. 2.2, we assumed an error-function-type outdiffusion with a diffusion constant $D = 3 \times 10^{-11}$ cm²/sec, measured for an 800°C capless anneal with AsH₃ overpressure (6). As the annealing time increases, V_{SUB} increases from 0.7 to 1.2V, and the electron concentration profiles are narrower.

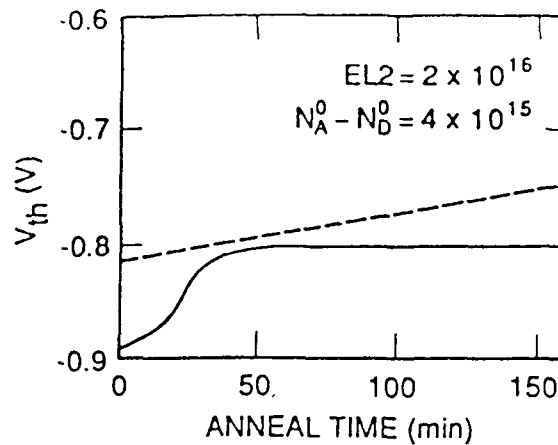
Figure 2.3 shows the EL2 effects on threshold voltages. Using the Poisson solution of $n(x)$, V_{th} is calculated using

$$V_{th} = V_{bi} - \frac{q}{\epsilon_0 \epsilon_R} \int_0^{\infty} x dx n(x), \quad (2.2)$$

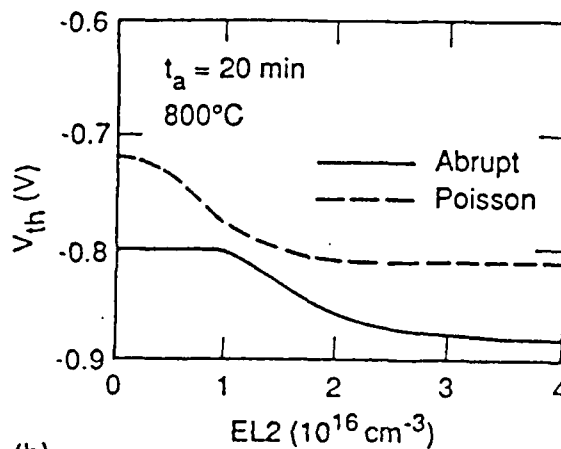
where V_{bi} is the Schottky barrier height. With the abrupt-depletion approximation, one must first calculate x_t by integrating over the substrate barrier. Then V_{th} is obtained from (5)

$$V_{th} = V_{bi} - \frac{q}{\epsilon_0 \epsilon R} \int_0^{x_t} x dx (\eta N_D(x) - N_A(x)) - \Delta_1, \quad (2.3)$$

where η is the donor activation (assumed unity in Fig. 2.3).



(a)



(b)

Fig. 2.3. (a) Calculated threshold voltages for 60 keV Si ions vs anneal time for a constant bulk EL2 and acceptor concentration of 2×10^{16} and $4 \times 10^{15} \text{ cm}^{-3}$, respectively. (b) V_{th} vs bulk EL2 concentration for a 20 min anneal at 800°C .

In Fig. 2.3a, as the annealing time t_A increases, V_{th} increases rapidly in the abrupt-depletion model near $t_A \sim 20$ min. This is the point where the EL2 concentration falls below N_A on the deep side of the substrate depletion region. For $t_A < 10$ min and $t_A > 30$ min, V_{sub} is either 0.7 or 1.2 V, and V_{th} does not vary much with annealing time. With the Poisson solution, the change is less rapid, and occurs over the whole range of annealing times, due in part to the inclusion of the partially ionized EL2 in determining the depth of the substrate depletion region. If t_A is constant, and the EL2 bulk concentration increases, V_{th} decreases with both solvers, as shown in Fig. 2.3b. When the bulk EL2 concentration falls below 10^{16} cm^{-3} , V_{th} increases by about 75 mV.

2.3 Conclusion

We conclude that for special cases, local fluctuations in EL2 concentrations from 3 to 20×10^{15} cm^{-3} could possibly affect MESFET threshold voltages. However, the effect is never sufficiently large to explain the measurements of Dobrilla et al. (2). The largest effect we calculated for the MESFETs measured ($V_{th} = -200$ mV) is a shift of 13 mV/ 10^{15} EL2/ cm^3 , compared with 63 mV measured. The calculations assumed a 15 min anneal at 800°C , error function-type outdiffusion, $D = 3 \times 10^{-11}$ cm^2/sec , implanted 60-keV Si ions with a dose of 1.5×10^{12} ions/ cm^2 , $\approx 90\%$, and $N_A = 4 \times 10^{15}$ cm^{-3} . The magnitude of the effect depends sensitively on the anneal time; the shift is less than 5 mV/ 10^{15} EL2- cm^{-3} for $t_A < 10$ min and $t_A > 25$ min. If this were the major mechanism for threshold-voltage fluctuations in MESFETs, it would be fairly easy to eliminate by preannealing the wafers before implantation for long times to drive out the EL2, using a buried p-layer (11) to fix V_{sub} to ~ 1.2 V, or by annealing the whole boule for a long time to obtain a uniform EL2 concentration (12).

By comparing the calculated magnitude of EL2 effects with reported threshold-voltage standard nonuniformities (13), we conclude that this mechanism is probably not the most important mechanism for giving MESFET threshold-voltage fluctuations; other mechanisms such as the dislocation-increased carrier-activation (DICA) model (13) are less fragile and give larger fluctuations.

III. SUBSTRATE-IMPURITIES EFFECTS ON GaAs MESFETs

3.1 Background

Materials nonuniformities in Liquid-Encapsulated-Czochralski (LEC) grown GaAs substrates have caused difficulties in the GaAs semiconductor industry. There are two important classes of materials effects: the effect of dislocations [13-15] and of background impurities [16-19]. We discussed calculations of the effects of dislocations on the properties of ion-implanted GaAs MESFETs, in our Interim Report.

While dislocations can have a local effect on MESFET threshold voltages and other device characteristics, impurities will affect device characteristics approximately uniformly across an entire wafer [16] when they are uniformly distributed. As typical GaAs MESFETs are fabricated with active channel donor-impurity peak concentrations of about 10^{17} cm^{-3} , background impurity levels above 10^{15} cm^{-3} may affect device characteristics. In LEC-grown GaAs, shallow acceptor levels of carbon are present which vary from 1 to $6 \times 10^{15} \text{ cm}^{-3}$ [18]. Background donor levels of S or Si are also present, but at concentrations well below 10^{15} cm^{-3} , and usually below the C concentration [17,19]. Bulk LEC grown GaAs is semi-insulating due to the presence of the deep-donor EL2 at levels of about 10^{16} cm^{-3} [19]. Excess EL2 over the shallow acceptor pins the Fermi level at the middle of the energy gap, resulting in small electron concentrations and high resistivity in the intrinsic material. In Horizontal-Bridgman (HB) grown GaAs, an excess of background shallow donors over shallow acceptors is usually present, and the deep acceptor Cr is added to pin the Fermi level to midgap. Unfortunately, both Cr [20] and EL2 [6] outdiffuse in the near surface at temperatures characteristic of the post-implant anneals. For this reason, Cr-doped wafers have been abandoned by many of the MESFET manufacturers in favor of the LEC-grown, EL2-pinned GaAs substrates. The outdiffusion of the EL2 can have an effect on GaAs MESFET threshold voltages [21], but it is relatively minor when compared with that of Cr outdiffusion.

The incorporation of impurities from the GaAs melt generally varies from wafer to wafer, and from boule-to-boule so that impurity effects can result in boule-scale nonuniformities in device characteristics. To reduce these effects it is common to qualify boules. Test MESFET or Schottky diode structures are fabricated on wafers taken from near the seed and tail,

threshold voltages are measured, and the ion-implant doses needed to obtain uniform device characteristics are calculated [22]. Since the segregation of impurities varies regularly along the growth direction [16], the doses needed to obtain the desired device characteristics on the remaining untested wafers of the boule are simply interpolated.

It is clearly desirable to reduce impurity levels as much as possible, to below 10^{15} cm^{-3} , to minimize impurity effects on MESFET devices. However, eliminating background acceptor impurities in LEC GaAs is undesirable, since these background acceptors minimize the channeling tails of the implanted donor ion distributions. If the wafer-to-wafer impurity levels cannot be tightly controlled, the next best thing to do is to eliminate background impurities altogether. However, if the wafer manufacturers succeed in this, it will be necessary for the device manufacturers to add a buried p layer to obtain sharp electron profiles, low substrate leakage, and device isolation.

In Section 3.2 we discuss the results of model calculations of impurity effects on GaAs MESFET threshold voltages and electron profiles. The dependence of threshold voltages on acceptor concentrations is found to be significant. To reduce this dependence, buried p layers (Sect. 3.2), fabricated by implanting Be ions can be used. Calculations are presented which vary the Be ion implant energy and dose, and calculate the effect of varying background C concentrations. In Section.3.3 we discuss the conclusions of this effort.

3.2 Model Calculations

In Figure 3.1 we compare electron profiles, $n(x)$, for several different GaAs substrates described in Table 3.1. To display electron profiles in a way that is comparable to the original donor profiles, $N_D(x)$, Poisson's equation is solved [25] using the boundary condition

$$\frac{dn(x)}{dx} = 0 \text{ at } x=0, x_{\max}, \quad (3.1)$$

where x_{\max} is the maximum depth ($2 \mu\text{m}$ in Fig. 3.1) used in the calculation. In reality, with a Schottky barrier at the surface having a typical intrinsic barrier height of 0.78 V, $n(x)$ should vanish at the surface when no bias or when reverse bias is applied. The boundary condition, Eq.(3.1), allows deferring the choice of biasing conditions to a later time, and reflects the physical property that electrons do not leave the surface nor the interior boundary. At

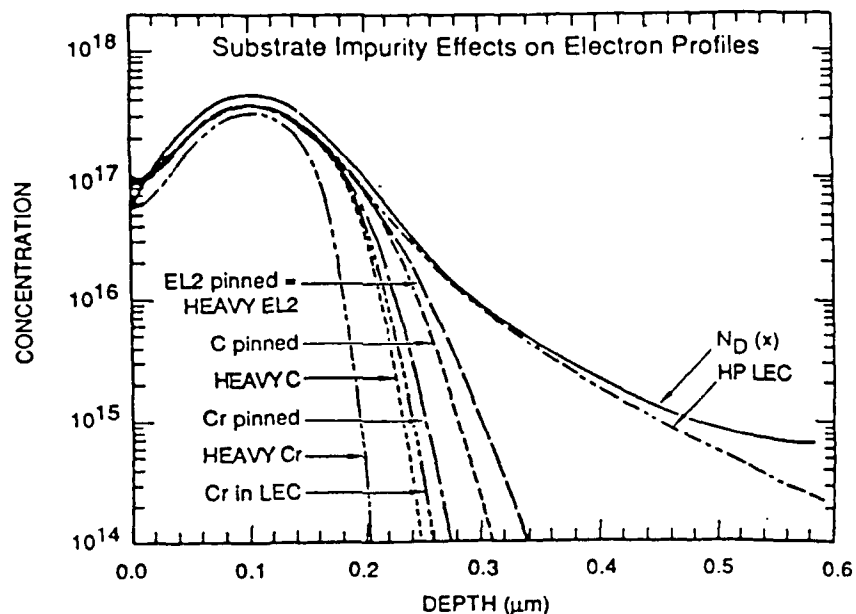


Fig. 3.1. Calculated substrate-impurity effects on electron profiles in a channel of MESFETs implanted using 5×10^{12} Si ions/cm². The various substrates modeled have assumed depth-independent impurity concentrations listed in Table 3.1.

small depths, the electron concentrations are a factor of $\eta = 0.8$ below the donor concentrations, except at the surface, where η is the assumed activation. The electron profile near the surface is not meaningful, as it will usually vanish under normal bias conditions. The donor profile for 100 keV Si ions, used in Fig. 3.1, was measured using secondary-ion mass spectroscopy (SIMS). Although the wafer was oriented to avoid implanting into channels, the donor profile is not Gaussian, but shows an exponential tail, due to ions scattered into channels in any of the hundreds of collisions the Si ion undergoes before it stops. The ion dose used, 5×10^{12} cm⁻², was chosen to be typical for a microwave MESFET.

The results shown in Fig. 3.1 can be understood in terms of two factors: the magnitude of the background acceptor concentration and the substrate barrier height. This is illustrated in Fig. 3.2 where we show dopant concentrations and band diagrams corresponding to cases where the substrate Fermi level is pinned at mid-gap by excess EL2 or Cr, and for cases where the Fermi level is pinned by excess shallow acceptors. Near the intersection of the implanted shallow donor and background shallow acceptor in Fig. 3.2a, a p-n junction, called the substrate barrier, is formed. In the abrupt depletion

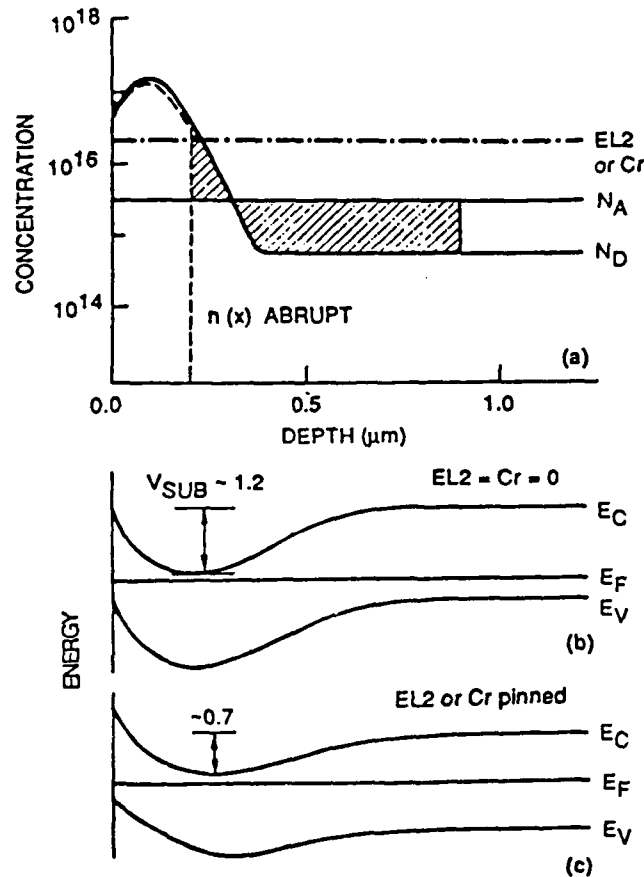


Fig. 3.2. (a) Dopant concentrations and abrupt-depletion electron profiles vs depth. The corresponding energy-band diagrams are shown for cases where the deep donor or acceptor concentrations exceed the shallow dopant concentrations in the substrates (c), and for cases where the substrate is shallow-p-type below the channel (b).

model, $n(x)$ would follow the active donor concentration up to the shallow side of the substrate barrier, then it would fall off vertically. The Poisson solutions give approximately this behavior, except that $n(x)$ does not decrease abruptly, falling instead with a typical Debye tail into the substrate depletion region. As the background acceptor concentration increases, the intersection between the implanted donor and acceptor profiles moves closer to the surface, therefore the electron concentration profile is shallower. The other factor is the substrate barrier height, which changes from about 0.7 V, when the substrate Fermi level is pinned at mid-gap by EL2 or Cr to about 1.2 V, when the substrate Fermi level is pinned by excess shallow acceptors. In the latter case,

the larger substrate barrier height increases the width of the substrate depletion region, so that the electron profiles for $V_{sub} \sim 1.2$ V are narrower than those for $V_{sub} \sim 0.7$ V. In our calculations, we assume that the representative dominant shallow acceptor is C, shallow donor is Si, and deep acceptor Cr. Other acceptor concentrations of Fe, Mn, and Cu, having different energy levels may be present in LEC GaAs [17,19], which can give other barrier heights between 0.7 and 1.2 V.

Consider the electron profiles for a typical LEC substrate where the Fermi level is pinned by EL2. If we assume that deep acceptors are absent, the shallow donor concentration is small, the shallow acceptor concentration is $3 \times 10^{15} \text{ cm}^{-3}$, and the EL2 concentration is $2 \times 10^{16} \text{ cm}^{-3}$ (Table 3.1). The

Table 3.1. Modeled Substrates and Calculated Threshold Voltages.

Substrate	N_A	N_D	EL2	Cr	V_{th}	ΔV_{th}
	Concentrations in 10^{16} cm^{-3}				(V)	(mV)
1. EL2 pinned	0.3	0.05	2	0	-6.26	320
2. Heavy EL2	0.3	0.05	5	0	-6.27	600
3. C pinned	0.3	0.05	0	0	-6.11	-
4. Heavy C	1	0.05	0	0	-5.29	-
5. Cr pinned	0.1	0.2	0	1	-5.59	190
6. Heavy Cr	0.1	0.2	0	5	-3.53	300
7. Cr in LEC	0.3	0.05	2	1	-5.32	340
8. HP LEC	0.03	0	2	0	-6.77	350

intersection between the shallow donor and acceptor profiles occurs at $0.38 \mu\text{m}$, and the donor side of the substrate depletion region extends about $0.1 \mu\text{m}$ to shallower depths. Therefore, for $x > 0.25 \mu\text{m}$, $n(x)$ falls off exponentially. Increasing the magnitude of the EL2 concentration has no effect on the electron concentrations. Most of the EL2 is un-ionized, except for the part equal to the shallow acceptor concentration, $N_A = 3 \times 10^{15} \text{ cm}^{-3}$. The Fermi level and therefore the substrate barrier height is fixed at about 0.7 V, independent of the EL2 concentration for any concentration much above the shallow

acceptor. This suggests that the EL2 concentration should have only a minor effect on MESFET device characteristics, unless the concentration falls below the background acceptor level, which could be caused by outdiffusion [21]. For this case, the electron profile would follow that for the C-pinned substrate case in Fig. 3.1. There, the substrate barrier height is 1.2 V, and $n(x)$ falls off at shallower depths than where the substrate is EL2 pinned. Increasing the C concentration, causes the point of intersection between the shallow donor and acceptor to be closer to the surface, resulting in a narrower electron profile. This is found for the high carbon concentration case in Fig. 3.1, where the shallow acceptor concentration is assumed to be $1 \times 10^{16} \text{ cm}^{-3}$, and the EL2, Cr, and shallow donor concentrations are assumed to be either zero or negligible.

For the deep-acceptor-pinned substrate, if we assume that the Cr concentration is $1 \times 10^{16} \text{ cm}^{-3}$, and the background shallow donor exceeds the background shallow acceptor, as in typical HB-grown, Cr-doped GaAs the substrate barrier is formed between the shallow donor and deep acceptor. The higher Cr concentration used in the Cr-pinned case (1×10^{16}) shifts the substrate junction to shallower depths, resulting in $n(x)$ falling off faster. Also, the electron concentrations are reduced by the background acceptors. This is best seen in the case of a high concentration Cr substrate, where, even at the peak of the n-doping one obtains significantly reduced electron concentrations by acceptors. For high-Cr doping, the p-n junction is formed at the most shallow depth, so that the narrowest electron profile is obtained explaining the improved performance in microwave FETs fabricated on Cr-doped substrates. Finally, for Cr-doped, LEC-substrates, $n(x)$ falls off just slightly faster than the case of Cr-pinned substrates. The effect of the EL2 present in the Cr-in-LEC substrates is unimportant, since the Fermi level is pinned at mid-gap by the Cr, so EL2 does not play a role. A slightly higher total acceptor concentration is assumed for the LEC substrates, than for the Cr substrates. Note that the electron profiles are steeper for the high-C substrates (total acceptor= 10^{16} cm^{-3}) than for the Cr-pinned ones (total acceptor= 1.1×10^{16}), due to the larger substrate barrier height for the C-pinned substrates. This suggests that for microwave-device applications, where steep electron profiles are required, it could be more advantageous to rely on buried p layers to sharpen the channel electron profile than Cr doping [23]. We have not considered Cr outdiffusion in Fig. 3.1 [20], which is difficult to control, and can also lead to changes in threshold voltages. For MMIC applications,

there should be advantages in using the easily controlled buried p layer instead of Cr [23].

Finally we consider the case of implantation into high-purity (HP) LEC substrates. In this case the p-n junction moves to very large depths, so that $n(x)$ follows $N_D(x)$ to very large depths. We assume that the background acceptor level will still exceed the background donor level, though both are small. If the background shallow acceptor did not exceed shallow donor, the deep-donor EL2 could not compensate the background impurity, and one could not obtain a semi-insulating substrate. For microwave device applications, slowly falling electron profiles like those obtained for HP-LEC substrates give poor transconductances at low gate biases [24]. We therefore conclude that background acceptor impurity concentrations greater than 10^{15} cm^{-3} are desirable, but they must be uniform.

Table 3.1 also gives calculated threshold voltages for MESFETs implanted with 5×10^{12} 100-keV Si ions/cm². Roughly speaking, the pinchoff voltage, V_p , is proportional to the average depth of the electron distribution, so that the threshold voltage V_{th} ($\sim V_{bi} - V_p$, $V_{bi} \sim 0.78 \text{ V}$) should be more negative for deeper electron distributions. By comparing the electron profiles in Fig. 3.1 and the threshold voltages in Table 3.1, we see that this is indeed the case, V_{th} varies from -3.53 to -6.77 V as one goes from the steepest electron profile (Heavy Cr) to the case where $n(x) \sim N_d(x)$ (HP LEC).

At small depths for negative gate biases near threshold, the deep levels are pulled above the Fermi level. The neutral deep donors are ionized, releasing electrons into the channel, and the deep acceptors neutralize, releasing electrons into the channel. In either case, the voltage needed to pinch off the channel increases. The calculated relative shifts in the threshold voltages listed in Table 3.1 are generally less than 15%, even for the highest EL2 and Cr concentrations. Such shifts are potentially observable in threshold-voltage temperature dependences, due to the strong dependence of the rate of trap emptying on temperature [25]. The calculated shifts assume that the deep level concentrations are independent of depth. Due to the outdiffusion of both Cr [20] and EL2 [6], the magnitudes of the deep level concentrations at shallow depths may be very small, so that much smaller threshold-voltage shifts should be observed.

Figure 3.3 shows the calculated effect of varying C concentrations on MESFET threshold voltages. Carbon is usually measured by local-

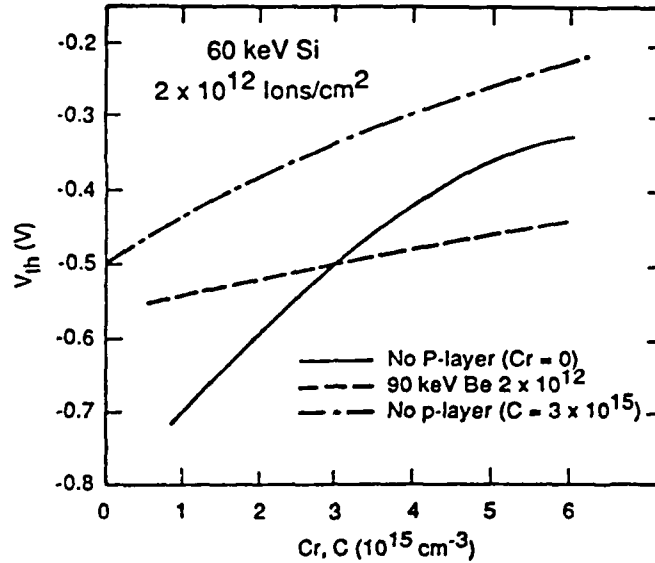


Fig. 3.3.

The calculated dependence of MESFET threshold voltages on the background shallow acceptor (C) or deep acceptor (Cr) background levels. The ion dose and activation was adjusted to give a threshold voltage of -0.5 V for a C level of $3 \times 10^{15} \text{ cm}^{-3}$ and $\text{Cr} = 0$. As one increases either the C or Cr concentrations, V_{th} becomes more positive, with approximately the same slope. The buried p layer reduces the dependence on the C or Cr levels.

vibrational-mode analysis [18]. In recent years the usually accepted LVM absorption coefficient [25] has inflated by a factor of 3 to 4 so that the commonly observed range of carbon concentrations in LEC GaAs has changed from 0.5 to 4×10^{16} [16] to 0.1 to $1 \times 10^{16} \text{ cm}^{-3}$ [18]. This background acceptor has two effects on the MESFET threshold voltages. In the abrupt depletion approximation, V_p varies roughly as

$$V_p \sim \int_0^{x_t} x dx [\eta N_D(x) - N_A(x)], \quad (3.2)$$

where x_t is the position of abrupt depletion edge. For higher C concentrations, the substrate p-n junction moves to shallower depths, so that x_t and V_p decrease. Second, the background acceptor concentration directly subtracts

from the active donor concentration to give a smaller pinchoff voltage, and therefore a more positive V_{th} value.

For carbon concentrations varying from 1 to $6 \times 10^{15} \text{ cm}^{-3}$, significant changes in the threshold voltages are obtained, which must be compensated for from wafer to wafer to give uniform threshold voltages.

Deep and shallow acceptors have nearly equal effects on threshold voltages (Fig. 3.3). Although models of substrate compensation and resistivity in LEC GaAs usually neglect deep acceptors [18], Cr, Fe, Cu, and Mn acceptors are probably present, with concentrations ranging from 10^{14} to 10^{16} cm^{-3} . Though close to the limits of SIMS sensitivity, Hobgood et al. [17] reported levels of Mn ($< 1.2 \times 10^{15}$), Cr ($< 1 \times 10^{15}$), and Fe ($< \text{mid } 10^{15} \text{ cm}^{-3}$) for LEC GaAs pulled from pyrolytic Boron nitride crucibles. Kirkpatrick et al. [19] report similar levels (Mn $\sim 1 \times 10^{15}$, Cr $< 5 \times 10^{14}$, Fe $\sim 3 \times 10^{15}$). If these concentrations also vary from wafer to wafer, and are all electrically active, significant effects on MESFET threshold voltages such as those shown in Fig. 3.3 should be observed.

3.3 Conclusions

Background impurities of shallow and deep acceptors in GaAs substrates play an important role in both determining the shape of the electron profiles in MESFET channels and in giving improved long-term threshold-voltage uniformities in the GaAs MESFET industry. Wafer manufacturers should strive to reduce impurity levels as much as possible. Uniformity of the impurity must be achieved to increase MESFET parameter control on a wafer to wafer and boule to boule basis.

IV. ION-IMPLANTATION INTO GaAs PROFILE DETERMINATION

4.1 Ion Implantation Profile Determination in GaAs

4.1.1 Background

For controlled profiles when ion implanting into crystalline materials, the wafers must be tilted and rotated precisely with respect to the beam to minimize axial and planar channeling (26-33). This, however, does not completely eliminate channeling effects, since the ions undergo hundreds of collisions before they come to rest, and have a finite probability of scattering into a channel during any single collision. In a channel, the ion stopping power is reduced, resulting in a fraction of the ions coming to rest at depths deeper than would occur in an amorphous material. This partial channeling is responsible for the exponential tails observed in implanted atomic-impurity profiles in crystalline materials.

Several methods are available to calculate profiles of ions implanted into amorphous materials (34-38). Figure 4.1 compares a measured profile

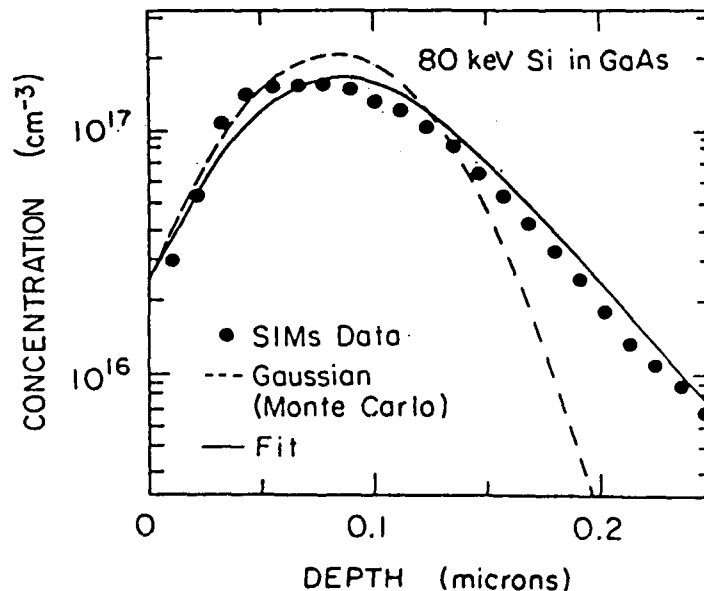


Fig. 4.1. Comparison of a measured 80-keV Si²⁹ implant concentration profile with a profile calculated using the TRIM Monte-Carlo code (35), and with a fit.

for 80-keV Si ions implanted into GaAs with a profile calculated using the TRIM Monte-Carlo code (35) for an identical implant into amorphous GaAs. Similar results are obtained when comparing with other implant calculations; (34, 36-38) the amorphous codes predict a narrower distribution and fail to predict the exponentially falling channeling tails.

In this effort development of techniques to simulate ion implantation profiles in GaAs, was pursued. GaAs metal-semiconductor field-effect transistor (MESFET) device characteristics depend critically on the threshold voltage, V_{th} , which in turn depends on the pinch-off voltage, V_p , given by

$$V_p \approx V_{bi} - V_{th}$$

$$V_p \sim \frac{q}{\epsilon_0 \epsilon_r} \int_0^{\infty} x dx N_D(x), \quad (4.1)$$

(30) where V_{bi} (~0.8 V) is the barrier height of the Schottky gate junction. The pinch-off voltage is directly proportional to the first moment of the implanted donor concentration distribution $N_D(x)$. As a result of channeling, a fraction of the ions are implanted at deeper depths, resulting in higher moments, and pinch-off voltages, and more negative threshold voltages, than calculated for equal-dose implants into amorphous material. Since quantities like the drain source current at zero gate voltage depend upon the square of the threshold voltage, it is vital to correctly model implant profiles into crystalline GaAs to be able to correctly predict device characteristics.

The method we adopted to simulate ion-implantation profiles in GaAs is to fit analytical distributions to measured profiles. The advantage of this method is that numerical profiles can be calculated rapidly, as opposed to Monte-Carlo or Boltzmann-transport calculations (35-36). Also, presently, Monte-Carlo and Boltzmann transport codes incorporating crystalline structures have not been sufficiently developed to be widely available (40-44). The disadvantage of our approach is that one can never fully explore all implant profiles of conceivable use. In this work, we discuss profiles for Be, Si, and Se ions in GaAs. These ions were chosen because Si and Se are the most widely used donor impurities in GaAs MESFET technology, and Be is used to produce buried acceptor layers in MESFETs. Furthermore, these three ions encompass a wide range of possible atomic numbers, so that eventually it may

be possible to interpolate parameters for calculating the profiles of intermediate atomic numbers using data from these three.

In Sect. 4.1.2 we describe the secondary-ion-mass-spectrometry (SIMS) measurements. In Sect. 4.1.3, results of profile studies are described for (A) the ion-energy dependence in bare, uncapped GaAs wafers, (B) the wafer tilt and rotation dependence, (C) the dependence on the ion dose, and (D) on the wafer dislocation density. In Sect. 4.1.3.E methods are formulated for calculating the profiles of ions implanted through SiO₂ or Si₃N₄ caps, and in Sect. 4.1.3.F measurements of the profiles for "knock-on" Si and O atoms, resulting from implantation through SiO₂ caps are discussed. Section 4.1.3.G comments on the relationship between SIMS measurements of donor profiles and electron carrier profiles in liquid-encapsulated-Czochralski (LEC) grown GaAs. Finally, Sect.4.1.4 contains the conclusions.

4.1.2 Experimental Measurements

Samples of commercial, high-pressure, LEC-grown, (100)-oriented GaAs wafers were implanted with Be⁹, Si²⁹, and Se⁸⁰ ions at doses of approximately 10¹³ cm⁻² (except where noted). SIMS measurements of the as-implanted profiles were made at Charles Evans and Associates. This ion dose was chosen to obtain adequate SIMS statistics for modeling. Unless specified, the wafer tilt and rotation angles were 7° and 9° from the wafer major flat, respectively. The samples were cleaved parallel to the major (011) flat, and were bonded to Si wafers at the desired rotation for implantation, or were implanted using a goniometer to position the samples.

For each measured SIMS profile, a constant background concentration, obtained by averaging the concentrations in the deep, flat portions of the spectra was subtracted. Also, since these profiles often show a high, unphysical concentration in the first few channels, we replaced the near-surface concentrations C_i by values obtained by extrapolating the first few realistic points in each spectrum to shallower depths. Using these corrected profiles, we then calculated the moments of the distribution (xⁿ) using

$$\langle x^n \rangle = \frac{\sum_i x_i^n C_i}{\sum_i C_i} \quad (4.2)$$

For Pearson-type distributions, the normalized moments are defined as (45-46)

$$R_p = \langle x^1 \rangle$$

$$\Delta R_p = \sqrt{\langle x^2 \rangle - \langle x \rangle^2}$$

$$\gamma = \frac{\langle x - R_p \rangle^3}{\Delta R_p^3}$$

and

$$\beta = \frac{\langle x - R_p \rangle^4}{\Delta R_p^4} \quad (4.3)$$

where the first moment R_p is referred to as the projected range, and is the position of the peak of the distribution for Gaussian distributions. ΔR_p is the width of the distribution, projected on the depth axis. The normalized third moment γ describes the skew of the distribution. Positive values of the order of unity and larger describe distributions falling off approximately exponentially at large depths, while negative values describe distributions skewed toward shallower depths. The kurtosis factor β mainly decides the type of mathematical function best describing the distribution according to whether it falls between certain ranges that are functions of γ (see e.g. Eq. 4.4) below) (45-47).

We, are mainly interested in the shapes of the distributions. In most of the data shown below, the profiles have been normalized to arbitrary peak heights; the absolute peak heights can be obtained by normalizing the integrated area to the implanted ion doses.

To reduce SIMS artifacts and uncertainties, we measured most atom distributions at least twice, using two different SIMS setups. Also, some distributions were independently implanted at several different times using up to two different implanters. When differences were observed, different samples were measured two additional times using the same SIMS setup. These precautions were taken to increase our confidence that these data, especially for the energy dependence of the unencapsulated implants, are accurate, and are independent of either the SIMS measurement or the ion-implant apparatus.

4.1.3 Results

4.1.3.1 Ion-Energy Dependence

Figures 4.2 and 4.3 show moments for the distributions of Be, Si, and Se ions implanted into GaAs as a function of the ion energy, while Figs. 4.4, 4.5, and 4.6 compare the measured distributions with profiles calculated using Pearson-IV distributions. To use a Pearson-IV

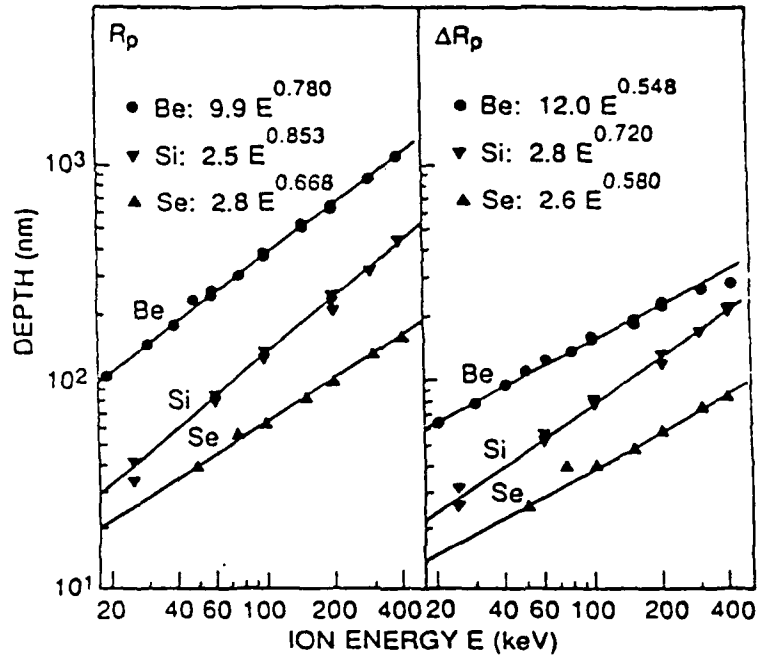


Fig. 4.2. Measured moments R_p and ΔR_p of concentration distributions of 20 to 400-keV Be, Si, and Se ions implanted into GaAs, and power-law fits (for ion energies in keV). The 10^{13} -ions/cm² implants were done into bare wafers at a tilt and rotation angle of 7° and 9°, respectively.

distribution for any set of moments, the value of the normalized fourth moment β must be greater than β_0 , defined as (45-47)

$$\beta_0 = \frac{39\gamma^2 + 48 + 6(\gamma^2 + 4)^{3/2}}{32 - \gamma^2} \quad (4.4)$$

We found that the measured moments for the profiles typically satisfy this criterion. Using Pearson-IV distributions to predict the profiles of ions implanted into crystals has the advantage of built-in exponential tails. An alternative way often used for fitting measured implant profiles is to add an exponential tail to a Gaussian distribution (46), which is calculated using an

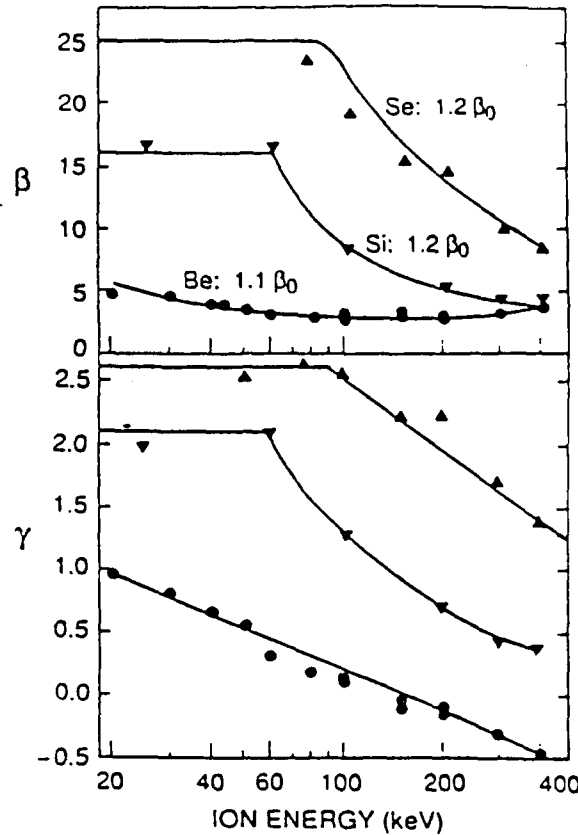


Fig. 4.3.

Normalized third and fourth moments γ and β of concentration distributions of Be, Si, and Se ions implanted into GaAs, as in Fig. 4.2. β_0 is defined in Eq. (4.4). The γ values were fit to $\gamma = 2.38 - 1.1 \ln E$, for Be, $\gamma = \text{minimum} (2.1, 95E^{-0.93})$, for Si, and $\gamma = \text{minimum} (2.6, 6.2 - 1.8 \ln E)$, for Se, where E is the ion energy in keV.

amorphous implant code. Such distributions require the same number of fitting parameters, but the parameters are not as straightforwardly obtained from the distribution moments as they are for Pearson-IV distributions. On the other hand, the Pearson-IV distribution is more complicated to compute than a Gaussian, and can easily give computer overflow errors if not properly calculated (48).

The moments R_p and ΔR_p shown in Figs. 4.1.2 and 4.3 were fit to power-law functions of the ion energy, γ was fit to either a linear function of $\log(E)$ or a power-law function of E , with a maximum, and β was fit to a constant multiplied by β_0 . Due to statistical uncertainties, the third and fourth moments are less accurate than the first two; however, they also have

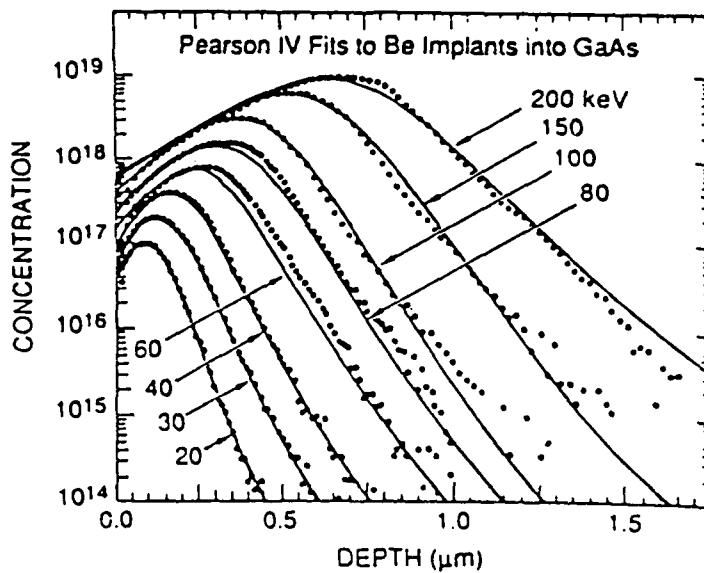


Fig. 4.4. SIMS measured profiles for 20-200keV Be ions in GaAs, compared with Pearson-IV fits calculated with the parameters given in Figs. 4.2 and 4.3. The concentration distributions are normalized to arbitrary peak heights.

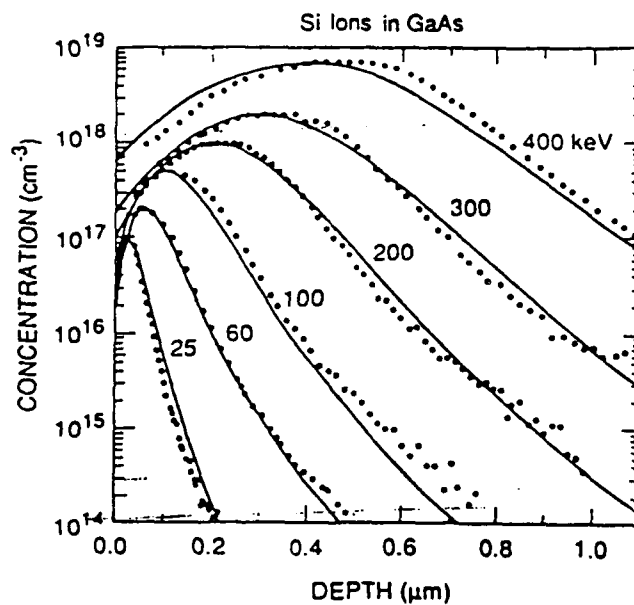


Fig. 4.5. SIMS measured profiles for 25-400 keV Si ions in GaAs, compared with Pearson-IV fits.

less effect on the derived distributions. We have little data to support the use of a constant γ value for Si and Se ions below 100 keV; the present form was

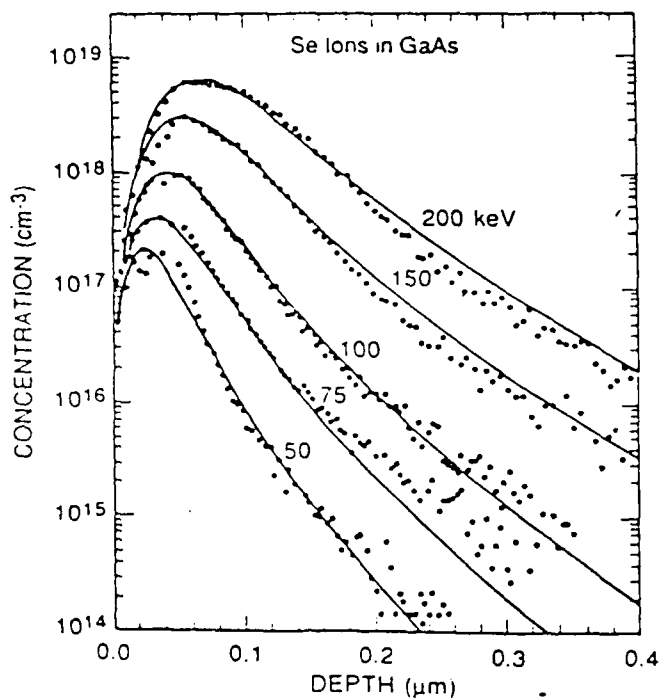


Fig. 4.6. SIMS measured profiles for 50-200-keV Se ions in GaAs, compared with Pearson-IV fits.

chosen for simplicity, instead of some more complicated parabolic function of the $\log(E)$.

4.1.3.2 Tilt and Rotation Dependence

We investigated the effect of varying the wafer tilt and rotation angles θ_{tilt} and θ_{rot} to reduce the magnitudes of the channeling tails. Ziegler and Levers (28) have mapped the channel directions in Si (essentially the same lattice structure as GaAs) using He-backscattering. As a function of the rotation angle, planar channeling should occur at 0° , 18° , and 45° from the (001) pole, and axial channeling should occur at various tilt angles for a rotation angle of 22° . The map suggests that the best rotation angle, with a standard tilt of about 7° , should be at about 9° or 36° from the major flat on (011) for SEMI-standard (100)-oriented LEC GaAs. On the other hand, the widest planar channel is the (011). To avoid this channel, the impinging angle θ_{110} , given by (31),

$$\tan\theta_{110} = \tan\theta_{\text{tilt}} \sin\theta_{\text{rot}}, \quad (4.5)$$

should be greater than about twice the critical angle ψ_c , given by (31)

$$\psi_c(\text{planar}) \approx 0.7 \sqrt{2\pi Z_1 Z_2 e^2 N d_p a / E}, \quad (4.6)$$

where Z_1 and Z_2 are the projectile and target (~ 32 for GaAs) atomic numbers, N is the target-atom density, d_p the distance between planes, and a is the Firsov screening length. For 60 keV Si ions, $2\psi_c$ is equal to $\sim 7^\circ$. For these ions θ_{110} is less than twice the critical angle for every tilt angles less than 10° and every rotation angle, suggesting that avoiding planar channeling is impossible for this implant.

However, the magnitude of the channeling tails possibly can be reduced by keeping the tilt and rotation angles as large as possible. Several authors have suggested using tilt angles of at least 7° and rotation angles of 45° for implantation into Si and GaAs (26-27, 30-31). Even if θ_{110} is larger than $2\psi_c$ this will not completely avoid channeling, since partial channeling results from the multiple collisions the ion undergoes in the crystal. As an example, for 60-keV Si ions, the TRIM Monte-Carlo code (35) calculates that after penetrating 10 nm of GaAs, the distribution of ion angles is Gaussian [as in most theories of multiple scatterings (49)] with a width $\sigma_\theta = 20^\circ$. Therefore, although one may use angles that avoid directly impinging on a channel, scattering into any number of axial or planar channels is possible after the ion enters the crystal. For high index planar and axial channels, the ion lifetimes in the channel are short. Nevertheless, this type of channeling will contribute to the channeling tails. Therefore independent of the initial tilt and rotation angles chosen for the implant, there will doubtless be some minimum channeling tail.

We made a series of measurements at different tilt and rotation angles. A simple goniometer was constructed for our implanter, that allowed samples, cleaved parallel to the wafer flat, to be implanted at precisely selected tilt and rotation angles. The uncertainties in these angles are approximately $\pm 1^\circ$. Samples were also implanted in a standard implanter at a tilt angle of 7° . Here the different rotation angles were obtained by bonding the samples to 4-inch Si wafers at the desired rotation angles, allowing the simultaneous implantation of six different rotation angles. The relative uncertainties in these rotation angles are less than 1.5° (resulting from the accuracy of the bonding and the beam scan angle over the limited part of the Si wafer where

the samples were placed). The absolute uncertainty is about 2.5° , due to the placement of the Si wafer in the implanter.

Figure 4.7 shows SIMS results, obtained for 60-keV Si for selected tilt angles, with a constant rotation angle of 10° . Narrower profiles are obtained at large tilt angles for two reasons: the reduction of ion channeling and the simple projection of the distributions onto the depth direction, according to $\cos \theta_{\text{tilt}}$. For the small tilt angles shown in Fig. 4.7, the

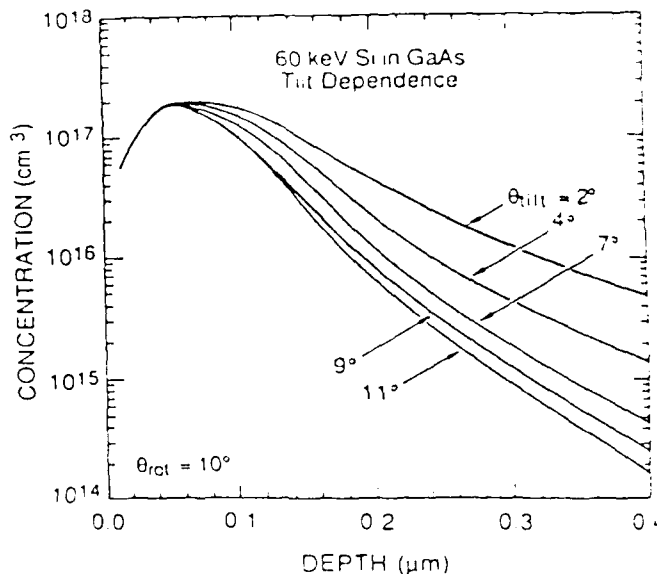


Fig. 4.7.

Measured concentration profiles for 60-keV Si ions implanted into bare GaAs wafers at tilt angles from 2° to 11° , for a constant rotation angle of 10° (except: $\theta_{\text{rot}}=26^\circ$ for $\theta_{\text{tilt}}=11^\circ$). The measured profiles are smoothed for clarity.

projection narrows the profiles by only 0.98, which is clearly a negligible effect compared to the observed narrowing between 2° and 11° . The broader width of the profiles at low angles is due to a combination of axial and planar channeling. One cannot completely avoid the channeling tails; for $\theta > 10^\circ$, the profiles are nearly independent of the tilt angle (aside from the projection effect), but do not approach the Gaussian, predicted for implantation into amorphous material. Similar results were obtained for 100- and 240-keV Si ion implantation into GaAs, (26,31) and for Implantation of various ions into Si wafers (29, 31-33).

In Fig. 4.8 we plot the rotation-angle dependence for 20-keV Be implantation into GaAs, for a tilt angle of 7° . Since in this case $2\psi_c$ is $\sim 11^\circ$, channeling into the (011) plane cannot be avoided for any rotation angle at this tilt, although slightly narrower profiles can be obtained at large rotation angles, as is clearly seen in the figure.

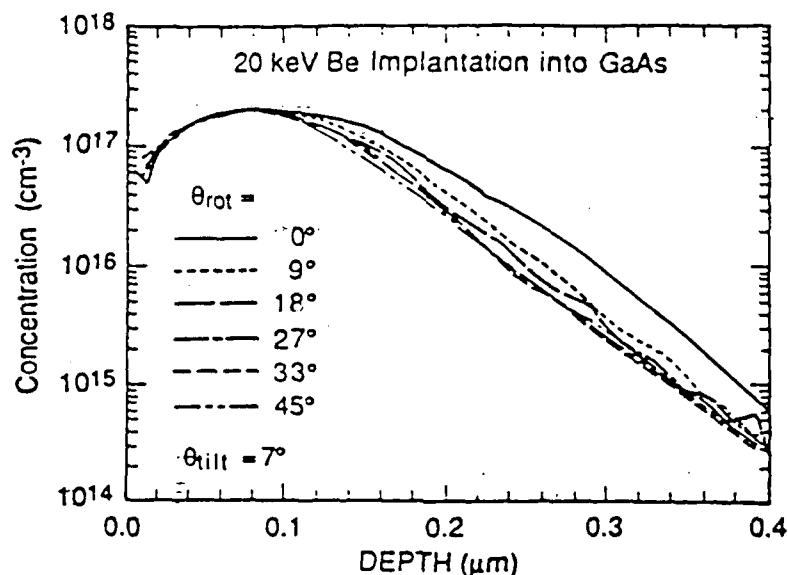


Fig. 4.8. Measured concentration profiles for 20-keV Be ions implanted into GaAs for selected rotation angles from 0° to 45° , for a constant tilt angle of 7° .

For 200-keV Be ion implantation, $2\psi_c$ is 3° . With $\theta_{\text{tilt}}=7^\circ$, θ_{110} is greater than $2\psi_c$ for rotation angles greater than 10° , significantly reducing (011) planar channeling. As is seen in Fig. 4.9, the profile for 0° rotation is much broader than those obtained for all other angles, in agreement with this expectation. In several cases, we purposely implanted at rotation angles to enhance channeling into minor planes mapped by Ziegler and Lever (28). Aside from the (011), the most significant should be the (400) at a rotation angle of 45° . However, impinging on these minor planes is seen to have no measurable effect on the channeling tails; identical profiles are seen at nearby rotation angles.

By implanting through amorphous overlayers, a reduction in the dependence of the implant profiles on the tilt and rotation angles can be achieved (26). The overlayer scatters the beam sufficiently to reduce the fraction of ions directly impinging upon the axial or planar channels. For

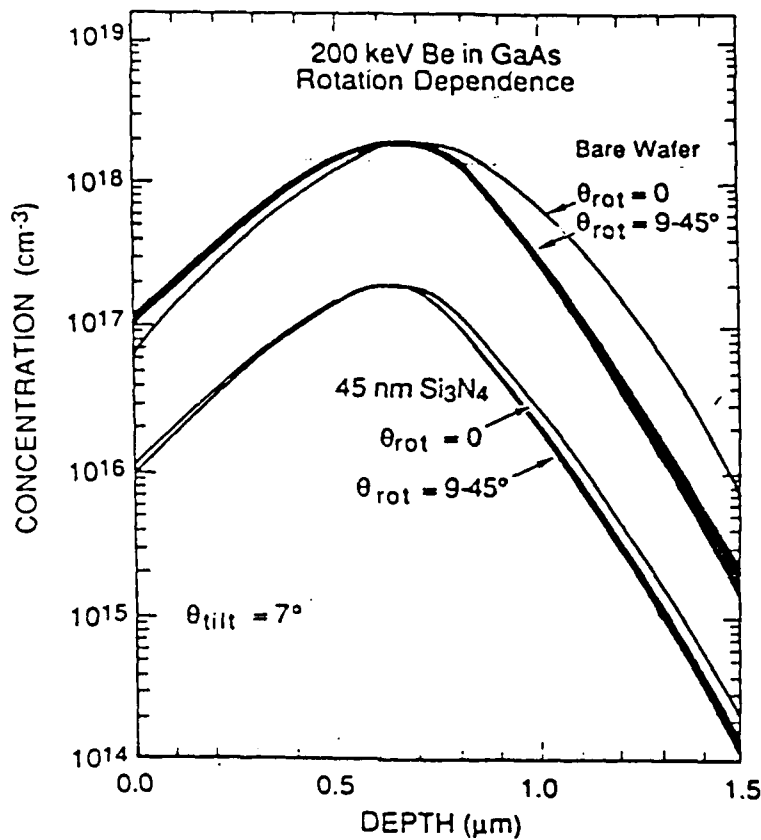


Fig. 4.9. Measured concentration profiles for 200-keV Be ions implanted into bare and capped (45-nm Si₃N₄) GaAs wafers for selected rotation angles from 0° to 45° and at a constant tilt angle of 7°. The wide black lines indicate the envelope of the data obtained for five rotation angles between 9° and 45°.

example, the difference between the profiles resulting from the $\theta_{rot}=0^\circ$ implant and other rotation angles for 200 keV Be ions implanted through a 45-nm cap Si₃N₄ layer is smaller than that seen for the bare-wafer implants (Fig. 4.9).

4.1.3.3 Dose Dependence

Due to the lattice displacements produced by the stopping of heavy ions in crystalline GaAs, one can expect to heavily damage the crystal in the region where the ion comes to rest. At high doses, a profile that is closer to Gaussian or Pearson-I profiles, predicted by the amorphous implant codes should then be obtained (35). On the other hand, high implant ion currents can cause the wafer temperatures to rise, resulting in some self annealing taking place, thus repairing the damage, and resulting in the same relative channeling tails

being obtained for both low and high doses. In some Si device fabrication processes, the crystal is purposely heavily damaged to suppress channeling. Producing heavy damage in GaAs is not desirable, since residual defects usually remain following the post-implant anneal, resulting in electrically active traps, low ion activation, and poor electron mobilities.

To be of use for the fabrication of MESFET devices, the profiles calculated with our analytical formulas should be valid for doses between 10^{12} and 10^{13} ions/cm², typically used for the MESFET active channel. Doses higher than 10^{13} ions/cm² are sometimes used to implant the source and drain contact regions of MESFETs, but device characteristics are not critically dependent on the shape of those profiles. To assure that the profiles are independent of ion dose below the 10^{13} dose we used for most of our work, implants of 3×10^{12} to 10^{15} ions/cm² were done. Figure 4.10 shows profiles for 100 keV Si ions,

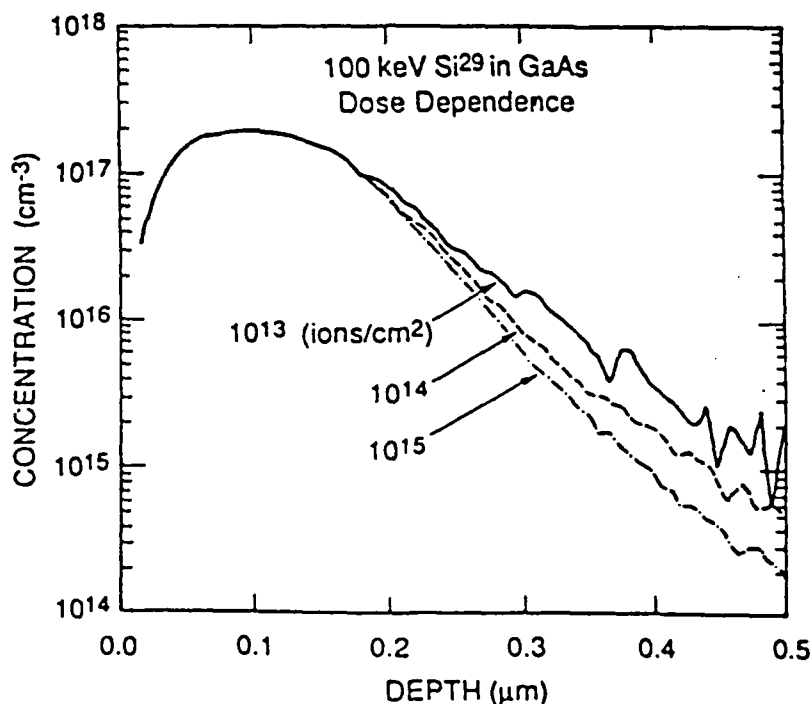


Fig. 4.10. Measured concentration profiles for 100-keV ²⁹Si ions implanted into bare GaAs wafers at doses of 10^{13} , 10^{14} , and 10^{15} ions/cm². The profiles have been normalized to the same peak height, 2×10^{17} cm⁻³.

normalized to same peak concentration. At higher doses, narrower profiles are observed. Yeo et.al. (50) obtained similar results for 120-keV Mg ions in

GaAs, and we obtained similar results for 40 and 200-keV Be and 25-, 60- and 200-keV Si ion implants. The reduction of the channeling tails is smaller for Be than for the more heavily damaging Si ions. Consistent results are obtained below 10^{13} ions/cm², so that the results given in Sect. 4.1 for profiles measured for 10^{13} ions/cm² doses should be valid for implant doses of 10^{12} cm⁻².

Selenium produces the most damage, and Se-ion implantation showed the greatest effect of increasing dose on the profiles, as seen in Fig. 4.11.

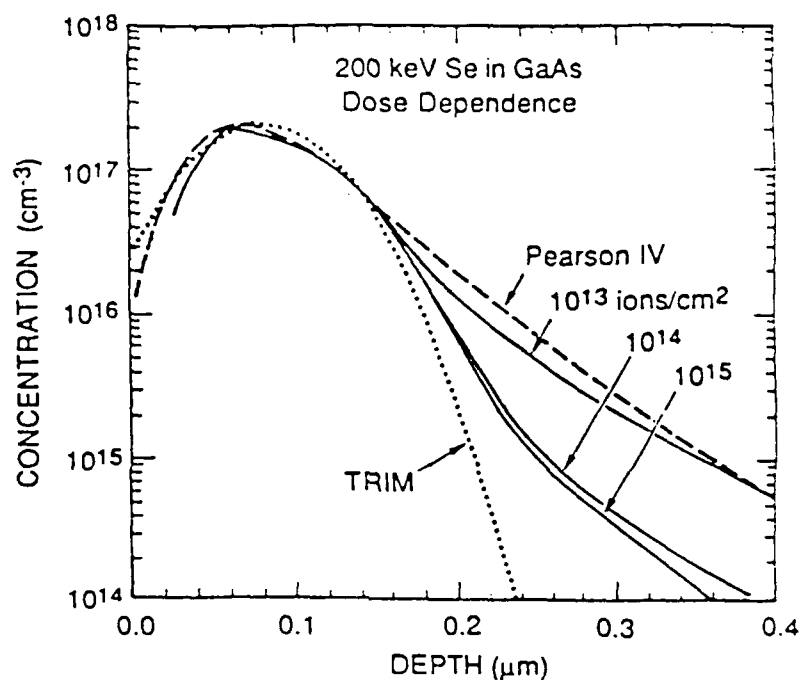


Fig. 4.11. Normalized, measured concentration profiles for 200-keV Se ions implanted into bare GaAs wafers at doses of 10^{13} , 10^{14} , and 10^{15} ions/cm². Fitted Pearson-IV profiles, and a TRIM (Ref. 35) calculated profile for implantation into amorphous GaAs are shown for comparison.

Between 10^{13} and 5×10^{13} ions/cm² the magnitudes of the channeling tails decreased, with the reduction beginning to saturate above 10^{14} cm⁻². Despite the very high doses and resultant damage, we never obtained profiles close to those for implantation into amorphous GaAs (35). This may be due to self-annealing effects associated with wafer heating for the high doses. (In the high-current Se implants, the wafer temperatures became sufficiently high to partially melt the photoresist used to bond the samples onto Si wafers.)

Figure 4.11 suggests that to obtain narrower profiles, a room-temperature damage implant with As (being similar to Se) at 5×10^{13} ion/cm² is sufficient. The additional damage may result in high post-implant trap concentrations, (51) though there is some evidence that using As ions may result in increased activation for subsequent Si implants (52).

4.1.3.4 Dislocation Density Dependence

The commercial, high-pressure-grown GaAs wafers used in our studies have typical dislocation densities of 3 to 8×10^4 cm⁻² (53). In a typical SIMS measurement, the sputter crater diameter is about 100 μm, so approximately 6 dislocations are expected to be present in every measurement. To investigate whether these dislocations might scatter the implant-ion beam sufficiently to affect the channeling tails (54), we compared profiles for low-dislocation, In-doped wafers and conventional wafers (55), both implanted with 10^{13} 60-keV Si, 200-keV Se, and 100-keV Be ions/cm². For the (2%) In-doped wafers, varying dislocation densities are obtained in the middle of the wafer (3000 cm⁻²), in a ring approximately 1-inch in diameter on a 3-inch wafer (500 cm⁻²), and on the outer part of the wafer (800 cm⁻²). We also compared conventional wafers having a dislocation density equal to 45000 cm⁻². As seen in Fig. 4.12, identical implant profiles are obtained with all dislocation densities for Se. Similar results are obtained for Si and Be implantation.

We conclude that the results obtained in Sect.3.1 for implantation into high-dislocation material should also be valid for implantation into low-dislocation, In-doped material.

4.1.3.5 Implantation Through Caps

In the fabrication of GaAs devices, implantation through 40- to 100-nm Si₃N₄ or SiO₂ encapsulants is sometimes done. These caps prevent the decomposition of the GaAs during subsequent post-implant annealing, and also prevent the deposition of contaminants onto the surface and possible surface decomposition resulting from wafer heating during the implant and other processing. We have seen in Sect. 3.2 that implanting through caps reduces the dependence of the channeling tails on the wafer rotation angle, a variable not often accurately controlled in many manufacturing facilities.

We have measured the profiles for Si, Se, and Be ions in GaAs, implanted through 40 to 200-nm plasma-enhanced chemical-vapor-deposition (PECVD)

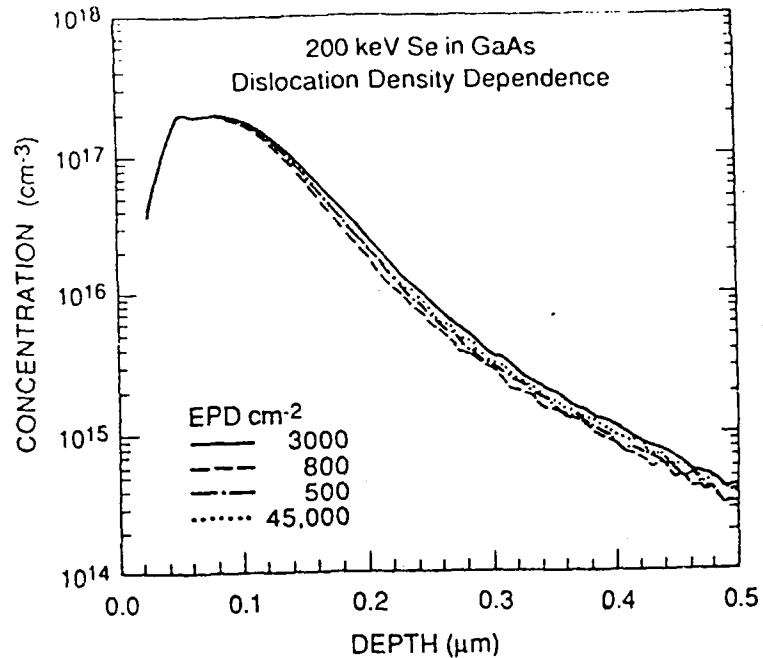


Fig. 4.12. Measured concentration profiles for 200-keV Se ions implanted into bare GaAs wafers with selected dislocation densities, obtained by using In-doped GaAs wafers (etch-pit density - 500, 800, and 3000 cm^{-2}) and conventional wafers (EPD = 45000 cm^{-2}).

Si_3N_4 and CVD SiO_2 layers. The estimated cap densities are 2.9 and 2.2 g/cm^3 , respectively.

For Be ions, implanting through caps mainly just shifts the origin of the implant profiles. The range scaling theory (45-47) was developed to describe the concentration distributions both in the cap $C_{\text{cap}}(x)$ and the semiconductor C_s . Since the caps are amorphous, TRIM (35) or other amorphous profile simulators can be used to calculate those concentration distributions. In the underlying semiconductor, the concentration is given by

$$C(x) = C_s(x - t_{\text{cap}}R_{ps}/R_{\text{pcap}}) \quad (4.7)$$

where x is measured from the surface of the semiconductor, and R_{ps} and R_{pcap} are the projected ranges of the ions in the semiconductor and in the encapsulant, respectively. In the present case, we use the Pearson-IV profiles, derived for implantation into unencapsulated wafers in Sect. 3.1, to estimate C_s . The amorphous implants are usually described analytically by Gaussians (Si

and Se ions) or by Pearson-I profiles (Be ions). The ion dose lost in the cap is obtained by integrating over the profile in the cap:

$$\Phi_{\text{cap}} = \int_0^{t_{\text{cap}}} dx' C_{\text{cap}}(x'), \quad (4.8)$$

and the concentration in the GaAs is then normalized to the total implant dose $\Phi_{\text{minus}} - \Phi_{\text{cap}}$.

For the ion range in the semiconductor, R_{ps} , a choice must be made whether to use the amorphous range, consistent with R_{pcap} , or the larger, experimentally determined projected range shown in Fig. 4.12, which is influenced by channeling. In fitting the measured profiles of Be ions implanted through caps, we find that using the amorphous range gives better agreement with the data, as shown in Fig. 4.13. Similar results are obtained for 100- to 400-keV Be^+ ion implants through 50 to 200 nm Si_3N_4 and SiO_2 caps.

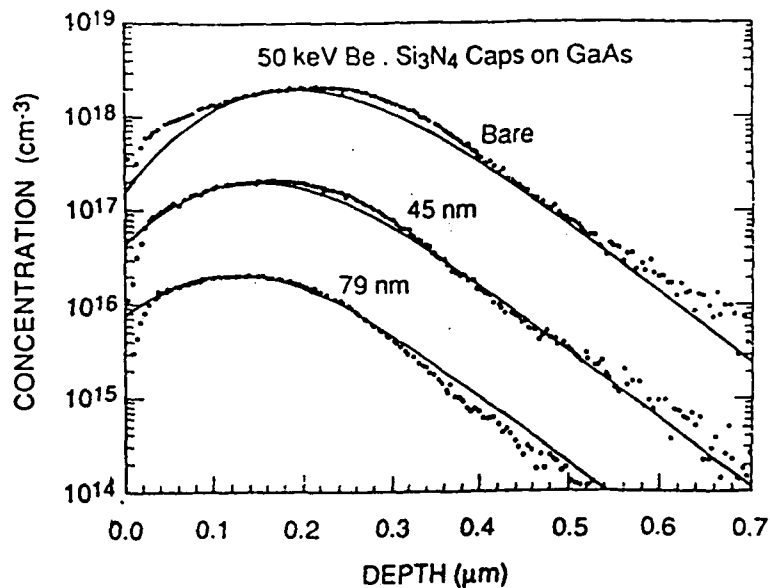


Fig. 4.13. Measured concentration profiles for 50-keV Be implanted into bare GaAs wafers and wafers with 45- and 79-nm CVD Si_3N_4 caps, compared with fits using the range-scale theory, Eq. (4.7).

We have also calculated the amorphous ranges, and the longitudinal and lateral straggling parameters using the TRIM Monte-Carlo code (35). In this calculation, about 2000 to 5000 ion trajectories are followed, and the ranges are fit to power-law functions of the ion energy, e.g.,

$$R_{pi} = A E^B. \quad (4.9)$$

The parameters A and B determined for implantation into GaAs, Si₃N₄ and SiO₂ are listed in Table 4.1. For caps with different densities, one scales the three moments inversely with density. For the densities listed, we generally find that the ratio of R_p values in Eq. (4.7) is near unit for Si₃N₄ and about 2/3 for SiO₂ encapsulants.

TABLE 4.1. Amorphous ranges R_p, straggling ΔR_p, and lateral straggling ΔR_l Power-law parameter [Eq. (35)]^a.

Ion	Substrate ^b	R _p		ΔR _p		ΔR _l	
		A	B	A	B	A	B
Si ²⁹	GaAs	13.021	0.951	13.461	0.777	11.477	0.831
Si	Si ₃ N ₄	11.187	0.983	9.223	0.773	5.371	0.870
Si	SiO ₂	13.850	1.020	12.349	0.793	6.341	0.919
Se ⁸⁰	GaAs	6.049	0.932	4.698	0.830	3.423	0.860
Se	Si ₃ N ₄	7.853	0.902	3.211	0.836	2.319	0.839
Se	SiO ₂	11.499	0.892	4.893	0.813	3.536	0.822
Mg ²⁴	GaAs	15.770	0.952	15.898	0.781	13.095	0.851
Mg	Si ₃ N ₄	13.532	0.986	13.175	0.732	6.596	0.881
Mg	SiO ₂	17.901	1.002	15.381	0.779	8.765	0.903
Be ⁹	GaAs	54.931	0.846	47.144	0.647	55.350	0.694
Be	Si ₃ N ₄	47.828	0.882	39.607	0.583	28.388	0.724
Be	SiO ₂	69.352	0.882	60.177	0.576	56.138	0.585

^aThe moments are in Å, when the ion energy is in keV.

^bDensities: GaAs: 5.32 g/cm³; Si₃N₄: 3 g/cm³; SiO₂: 2.2 g/cm³.

The magnitudes of the channeling tails are reduced when Si and Se ions are implanted through caps. This is illustrated in Fig. 4.14, together with the method used to fit this reduction. For 100-keV Si implants through 79 nm Si₃N₄ caps, simply shifting the Pearson-IV profile, obtained for implants into bare wafers, results in a larger magnitude of the tail at large depths, though it accurately predicts the shape of the measured distributions at large

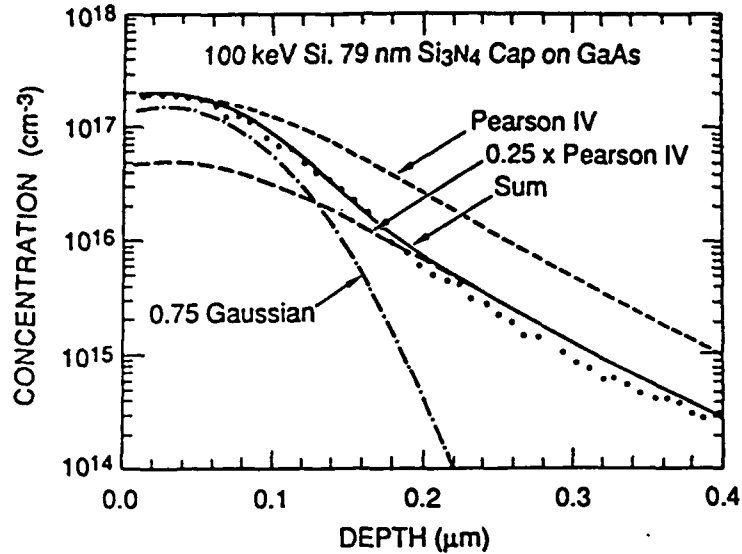


Fig. 4.14. Measured concentration profiles for 100-keV Si implanted into GaAs through 79-nm CVD Si₃N₄ caps compared with calculated fits.

depths. We fit the measured distribution by reducing the magnitude of the shifted Pearson-IV (calculated using Eq. (4.7), by a factor of 0.25. For the remaining part of the distribution, a shifted Gaussian, calculated using the TRIM parameters in Table 4.1, and Eq. (4.7) is used to describe the shift. Both the Pearson-IV and Gaussian distributions are normalized to unity at $x=R_p$, so the mixture can be described by a single parameter f

$$C(x)=(1-f)C_{S\text{Gaus}}(x) + fC_{S\text{PIV}}(x) \quad (4.10)$$

The net concentration is then normalized to the integrated dose or to an arbitrary peak height, as shown in Fig. 4.14.

Presently, insufficient data exists to obtain a universal parameterization for the parameter f . Probably, f depends on the ratio of the cap thickness to R_p in the semiconductor. Fits for other 100-keV Si ion implants are shown in Fig. 4.15. The Pearson-IV fraction is seen to decrease as the cap thickness increases. Apparently, for the relatively deeper Be ion implants, the cap thickness is not sufficiently large compared to R_p to observe a reduction in f . Also, electronic stopping dominates the Be energy loss in the caps, so the Be ions are not scattered as much as the Si and Se ions. As more

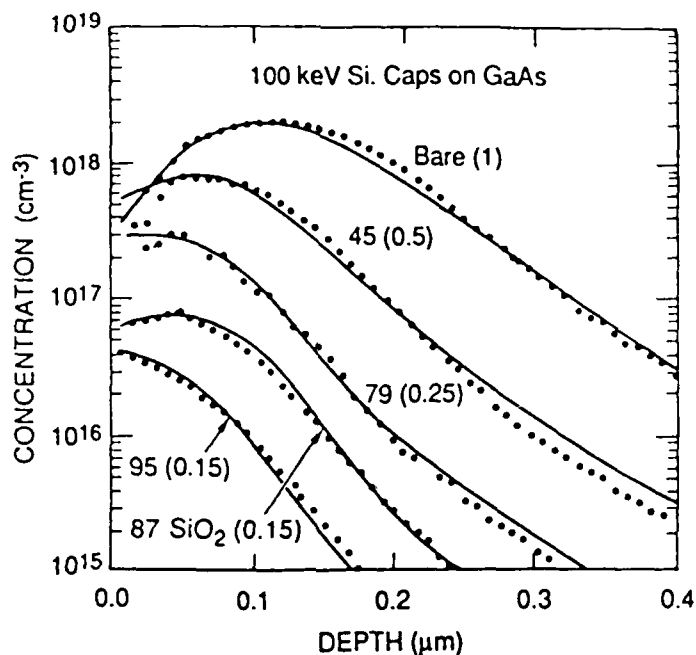


Fig. 4.15. Measured concentration profiles for 100-keV Si implanted through PECVD Si_3N_4 and one CVD SiO_2 cap into GaAs. The numbers give the cap thickness in nm, and the numbers in parentheses give the Pearson-IV mixing factor f defined in Eq. (4.40).

data becomes available for Si and Se implantation, further parameterization of this effect will be done.

4.1.3.6 Knock-on Distributions

When one implants into GaAs through Si_3N_4 or SiO_2 caps, Si and N or O atoms are knocked forward by the implant ion into the GaAs (36, 56). The "knock-on" Si recoils in the GaAs are additional donors, which add to the effective concentration of donors in the GaAs, while the O recoils can either form deep-donor traps or can compensate the implanted donors.

It is difficult to measure the knock-on distributions, except for high implant doses. In the SIMS analysis of GaAs substrates, masses associated with O, N, and Si^{28} typically have large backgrounds. (Mass 28 is probably due to CO molecules.) We have measured knock-on distributions for an implant dose of 2×10^{15} 200-keV Se ions/cm² implanted through 87-nm SiO_2 caps. This dose is sufficiently high so we can measure knock-on Si^{29} from caps having the normal 4.7% Si^{29} abundance. The O knock-on distribution was measured by taking the difference between the O found after implanting through a SiO_2

cap, and the O background found after implanting through a 74-nm sputtered Si_3N_4 cap. Similar Si knock-on distributions were observed for implants through the Si_3N_4 cap, but N atom concentrations could not be measured.

Figure 4.16 compares the measured knock-on distributions with TRIM calculations. As usual, the Se-ion distribution has a large channeling tail, though it is not as large for these high dose implants, as it would be for a low-dose one (Fig. 4.11). The magnitudes of the Si and O knock-on concentrations agree roughly with the TRIM calculations for shallow depths, but like the Se ion implants, they exhibit longer tails than predicted by TRIM.

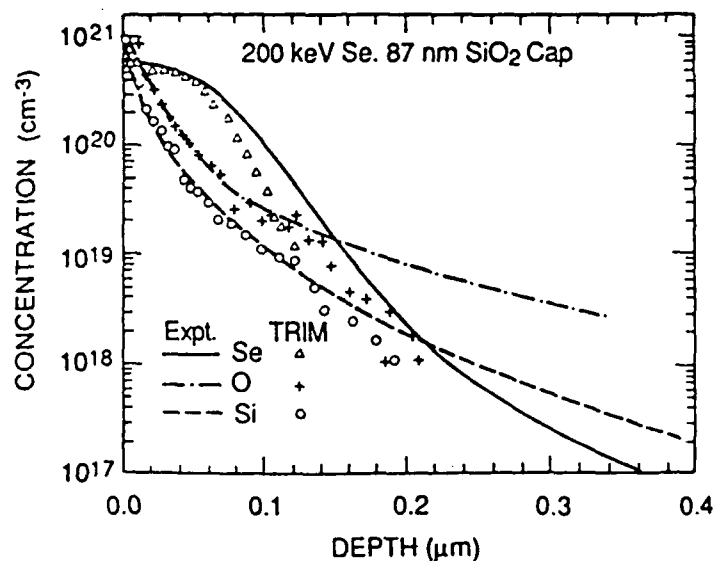


Fig. 4.16. Measured (lines) and TRIM calculations (points) of the concentration profiles of Se ions, and recoiled Si and O atoms, after implantation of 2×10^{15} 200-keV Se ions/cm² through an 87-nm SiO_2 cap on GaAs.

Since the recoil concentrations are largest at the surface where channeling tails are still not significant, we conclude that TRIM profiles may be adequate for simulating recoil-atom profiles for MESFET process and device modeling.

4.1.4 Conclusions

Profiles measured for Be, Si, and Se implantation into unencapsulated GaAs wafers at energies between 20 and 400 keV have been fit to Pearson-IV distributions, and the resulting fitting parameters were fit to functions of the

ion energy to derive simple, analytical formulas for implant profiles for any energy between about 10 and 400 keV.

Profile measurements for selected wafer tilt and rotation angles show that the narrowest profiles for a given ion energy occur for tilt angles greater than 7° , and rotation angles of 45° . Implantation through wafers encapsulated with Si_3N_4 or SiO_2 layers reduces the dependence of the profiles on the rotation angle.

The profiles are not dependent on the wafer dislocation density for densities between 500 and $50,000 \text{ cm}^{-2}$, nor on In doping of the wafers. Channeling tails on the profiles can be reduced slightly for Si and Be ions by using high ion doses of either the bombarding ion or a similar, but electrically-inactive, damage-producing ion. Se ions have the greatest effect on reducing channeling tails, though it is unclear whether the possibly beneficial effect of reducing tails might be outweighed by undesirable effects of trap formation, low ion activation, and poor electron mobilities.

For Be implants through SiO_2 and Si_3N_4 encapsulants on GaAs, the profiles in the GaAs can be predicted by simply shifting the profile for implantation into unencapsulated wafers by an amount related to the cap thickness. For Si and Se, our measurements suggest that the channeling tails are reduced slightly by implanting through caps. We presently have insufficient data to derive a universal function describing this reduction. The distributions of Si knock-on ions after implantation through caps are predicted accurately using TRIM Monte-Carlo calculations at shallow depths.

4.2 Device Sensitivity Resulting From Ion Implantation

4.2.1 Background

Ion implantation is the most widely used process in the semiconductor industry for introducing controlled impurity concentrations into Si, GaAs, and other materials. However, many effects are associated with ion implantation that require a clear, quantitative understanding to maximize the performance and uniformity of devices manufactured using technique.

The present work examines how implantation profiles can affect GaAs MESFET electrical device characteristics. To illuminate implantation effects, we have used the process and device model discussed in Section V to calculate device threshold voltages, currents, and transconductances. Our present calculations mainly address the issues of how to maximize the performance and uniformity of GaAs MESFETs. In consideration of device performance, a primary topic we consider is how much the shapes of the implant and resulting electron carrier profiles limit the ultimate transconductances obtainable for ion implanted MESFET's. In Sections 4.2.2 and 4.2.2 transconductance calculations for different energy implants and MESFET biases are shown. Four possible effects on device uniformity related to implanted channels are considered in the remaining part of Sect. III: the effects of cap thickness and etch-depth fluctuations on MESFET threshold-voltage uniformity, dopant diffusion during post-implant annealing, and the effects of Si-recoil ion distributions for implants through caps.

4.2.2 Transconductance

4.2.2.1 Profile Width Effects

Narrower carrier profiles give higher MESFET transconductances. For FET's operating in the saturated-current regime, and fabricated using epitaxial layers of thickness a , the transconductances vary as [64, Eq.(23b)]

$$g_m = \frac{\epsilon_0 \epsilon_r W v_s}{a} \sqrt{\frac{V_{bi} - V_{th}}{V_{bi} - V_g}} \quad (4.11)$$

where W is the FET width, v_s is the saturated electron velocity, and V_g is the gate voltage. A similar relationship should be approximately valid for ion-implanted MESFET's, where a is some effective implant layer thickness that depends on the ion energy. To gauge the dependence of a and therefore g_m on

the implant energy, we plot in Fig. 4.17, transconductances for FETs with constant threshold voltage ($V_{th}=-0.5$ V), constant V_{bi} , constant gate voltage ($V_g=0V$), and width ($W=1$ mm). Although this model uses saturated velocities that depend logarithmically on the absolute doping, the average saturated velocity is approximately 1.2×10^7 cm/s for all profiles shown in Fig. 4.17., therefore the transconductance variations with implant energy directly reflect the variations of the effective layer thicknesses. The threshold voltages are kept constant by varying the ion doses, shown in Fig. 4.17.

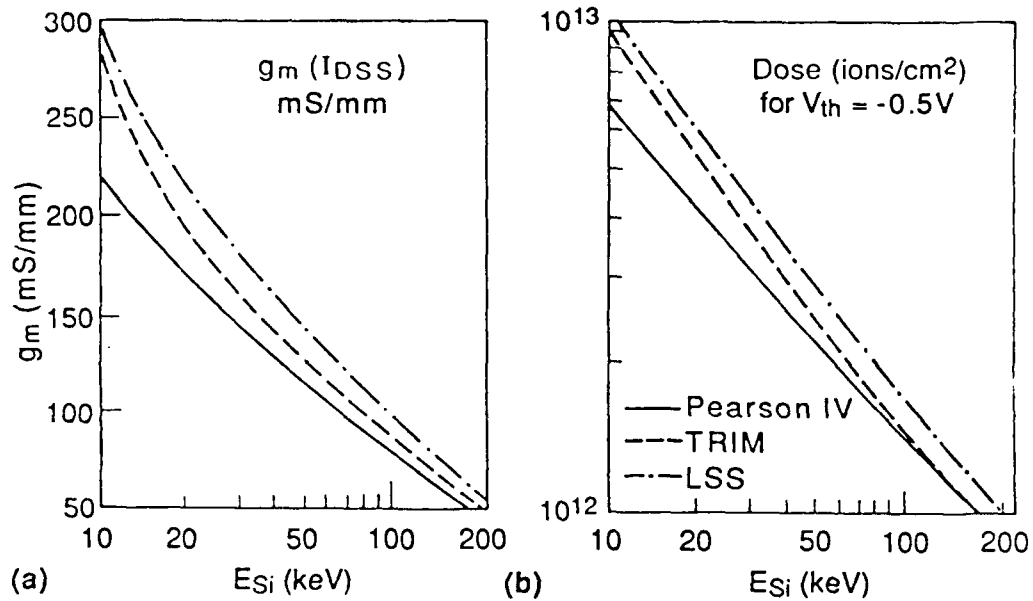


Fig. 4.17. Calculated transconductances g_m at zero-gate voltage and the dose needed to obtain a constant threshold voltage of -0.5 V for MESFETs fabricated by implanting Si ions with energies between 10 and 200 keV into GaAs. For the solid line, a Pearson-IV profile, based on fits to measurements was used. For the dashed and dash-dotted lines, Gaussian profiles were used, based on TRIM [35] and LSS [34] calculations of R_p and ΔR_p .

Three different types of profiles are compared in Fig. 4.17, profiles derived from the LSS tables [34], TRIM Monte-Carlo profiles [35], and measured profiles, fit to Pearson-IV functions (See Section 4.1). The LSS tables predict lower values of R_p than TRIM, which in turn predicts lower values than are observed experimentally. Since the parameter a is roughly proportional to R_p ,

and the pinch-off voltage varies roughly as the product of the dose and a , to keep V_p and therefore V_{th} constant, higher doses are required when using LSS profiles when compared to the Pearson-IV profiles to obtain the same threshold voltage. With the doses adjusted, the resulting transconductances for the LSS profiles are larger than for either the TRIM or measured profiles.

None of the transconductances increase inversely with the ion energy E . In part this occurs because R_p only varies as $NE^{0.85}$, but other factors, such as ΔR_p , the profile shapes, and the absolute magnitude of the donor doping, compared to the wafer acceptor impurity concentrations also play a role in determining the effective layer thickness. As the ion energy decreases from 200 to 20 keV, the transconductances for the measured profiles only increase by a factor of 3 to 4. Between 30 and 10 keV, g_m only increases from 150 to 225 mS/mm, much less than a factor of three. Sugitani et al. [59] noted a similar slow increase in effective layer thicknesses for 10, 20, and 30-keV Si implants in GaAs, derived by fitting observed distributions to Gaussian functions, and relating a to the first and second moments of the distributions.

Since Se implant profiles for ion energies scaled according to $E_{Se} = 0.829 E_{Si}^{1.28}$ are essentially identical to Si profiles implanted at an energy E_{Si} , [57] the results shown in Fig. 4.17 may also be applied to Se channel implants.

4.2.2.2 Maximizing Low-Bias Transconductances

For MESFETs fabricated for small-signal microwave amplifier applications, high transconductances are needed at low gate voltages (low DC source-drain currents I_{DS}) to achieve high gain at low power levels. The best practical channel profile for achieving this is a "box" or epitaxial-layer profile, where the donor-impurity concentration falls off from a constant value to background levels over a few atomic layers. Gaussian implant profiles are less desirable, but the observed implant profiles, with their exponential tails due to ion channeling, are even less optimal. Figure 4.18 compares calculated transconductances as a function of I_{DS}/I_{DSS} for each of these profiles ($I_{DSS} = I_{DS}(V_g=0, V_d=3 \text{ V})$). The box profile has a constant doping concentration of $3 \times 10^{17} \text{ cm}^{-3}$, to a depth of $a=0.165 \text{ }\mu\text{m}$. The implant profiles for 100-keV Si use a Gaussian profile, derived from TRIM Monte-Carlo [35] calculation, and a Pearson-IV profile, derived from SIMS measurements. For both the Gaussian and Pearson-IV profiles, a dose of $5 \times 10^{12} \text{ ions/cm}^2$ is used, with recess etching to obtain a -3 V threshold voltage performed. The channel

donor profiles are shown in Fig. 4.18b. Figure 4.18a shows that at a gate-bias of $0.1I_{DSS}$, the transconductances are only 70 mS/mm for the Pearson-IV,

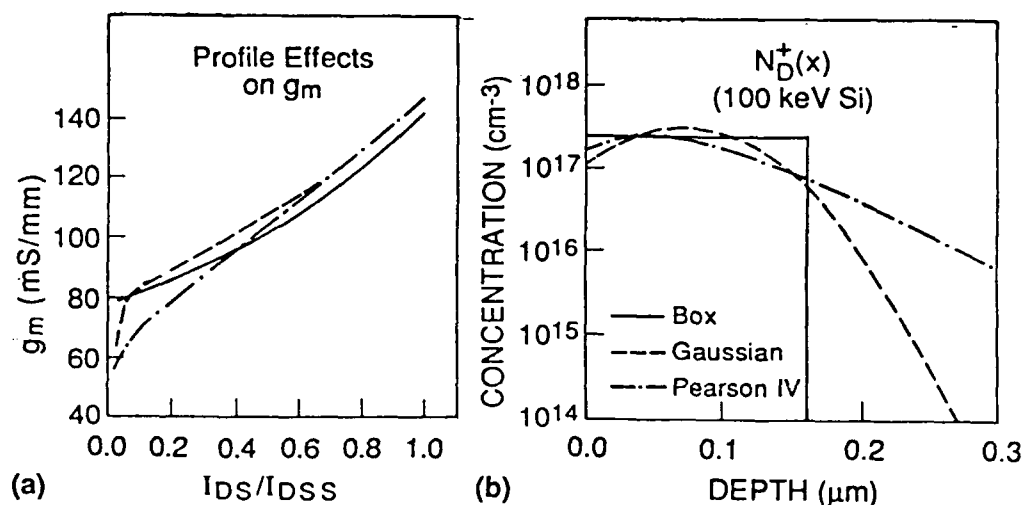


Fig. 4.18. (a) Transconductances of recess-etched MESFET's versus the DC source-drain current, normalized to the zero-gate voltage value. Calculations were made using Pearson-IV profiles, Gaussian profiles, and constant-doping (BOX) donor profiles, which are shown in (b).

but 80 mS/mm for the box profile. Due to differences in the exact shapes and magnitudes of the doping profiles, the three do not give exactly identical transconductances at high I_{DS} . If they are normalized to the same transconductance at I_{DSS} , the differences between the transconductances for the box and Pearson-IV profiles become even greater.

Although the Pearson-IV donor profiles are very broad when compared to the other two profiles, much of the channeling tail is cut off by the depletion region of the substrate junction created by the implanted donors and the substrate acceptor concentration, assumed in Fig. 4.18 to be $3 \times 10^{15} \text{ cm}^{-3}$ for LEC GaAs wafers. The resulting electron profiles are therefore more Gaussian than the donor atom profiles, which significantly improves the low-bias transconductances. Figure 4.19 shows electron profiles and the corresponding transconductances for various substrate acceptor concentrations for devices implanted with 5×10^{12} , 100-keV Si ions/cm², and etched to achieve a -3 V threshold voltage. For a high-purity wafer without

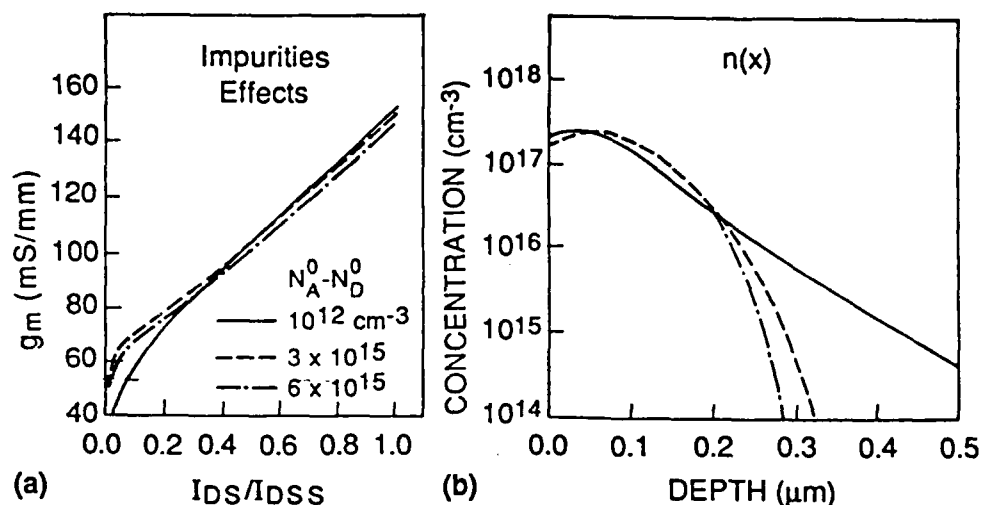


Fig. 4.19. Transconductances of recess-etched MESFET's versus the DC source-drain current (normalized to the zero-gate-voltage value), calculated using simulations of measured implant profiles for 5×10^{12} 100-keV Si ions/cm 2 , and assuming various wafer acceptor impurity concentrations. The corresponding electron carrier profiles after recess etching to obtain a -3 V threshold voltage are shown in b.

acceptor impurities, the electron and donor profiles are nearly identical, with the transconductance at $0.1 I_{DSS}$ being less than 60 mS/mm. Carbon acceptor concentrations between 1 and $6 \times 10^{15} \text{ cm}^{-3}$ can be present in LEC-grown GaAs. Figure 4.19 suggests that the mid-range concentration of $3 \times 10^{15} \text{ cm}^{-3}$ is nearly optimal. For higher concentrations, the corresponding transconductances at all biases are lower, which is due to a combination of profile-shape effects and compensation effects on the electron saturated velocities.

4.2.3 Diffusion During Annealing

For Si and Se ions implanted to concentrations less than 10^{18} cm^{-3} in GaAs, the diffusion constants for typical furnace anneals ($T_A < 900^\circ\text{C}$) are less than $10^{-14} \text{ cm}^2/\text{s}$ (Se) and $10^{-15} \text{ cm}^2/\text{s}$ (Si) [60-61]. Ohnuma et al. [62], using capacitance-voltage techniques to measure electron profiles on Cr-doped substrates, observed larger diffusion constants for Si ions annealed under SiO_2 caps. However, SIMS measurements of the Si-atomic impurity profiles in undoped LEC-grown GaAs give much smaller diffusion constants, suggesting that the Cr doping could have influenced Ohnuma's results [63]. Also, neither the outdiffusion of Si or Se ions into Si_3N_4 or SiO_2 caps nor the indiffusion of Si

from the caps has been observed. Assuming that the diffusion coefficients $D(T_A)$ for anneal temperature T_A are independent of electric-field and dopant concentration effects, the diffused concentration $C(x)$ after a time t is calculated from the as-implanted concentration $C'(x)$ using [70]

$$C(x) = \int_0^{\infty} dx' C'(x') \left[\exp\left[-\frac{(x-x')^2}{4Dt}\right] + \exp\left[-\frac{(x+x')^2}{4Dt}\right] \right]. \quad (4.12)$$

This equation satisfies Fick's diffusion equation, with a boundary condition at the surface ($x=0$)

$$\frac{dC}{dx} = 0, \quad (4.13)$$

corresponding to no transport of the implanted species across the GaAs/cap interface.

To first order, expressing C' as a Gaussian with a width σ , the post-anneal distribution remains Gaussian with a width σ , given by [64]

$$\sigma'^2 = \sigma^2 + 2Dt. \quad (4.14)$$

This suggests that diffusion during annealing primarily affects just the width of the distribution. Since MESFET pinch-off voltages are roughly proportional to the first moment of this distribution R_p , the larger width σ due to diffusion has little effect on threshold voltages, or on other device characteristics. The threshold voltage begins to change only when the diffusion length $\sim 2\sqrt{Dt}$ approaches the value of R_p . Then, dopants diffusing toward the surface are reflected inward, whereas dopants diffusing inward continue to move inward and the net moment of the distribution increases, leading to larger pinch-off and more negative threshold voltages.

Using this argument, we derive the following criterion for how diffusion during annealing affects MESFET threshold voltages. If

$$\sqrt{4Dt} > R_p - t_{\text{cap}} R_{ps}/R_{\text{pcap}}. \quad (4.15)$$

Where R_{ps} and R_{pcap} are the projected ranges in amorphous GaAs and in the

Where R_{ps} and R_{pcap} are the projected ranges in amorphous GaAs and in the cap, T_{cap} is the cap thickness, and R_p is the range in crystalline GaAs [62]. The factor involving t_{cap} describes shifts in the distributions due to implanting through caps, as described in ref. [57]. Figure 4.20 illustrates this criterion

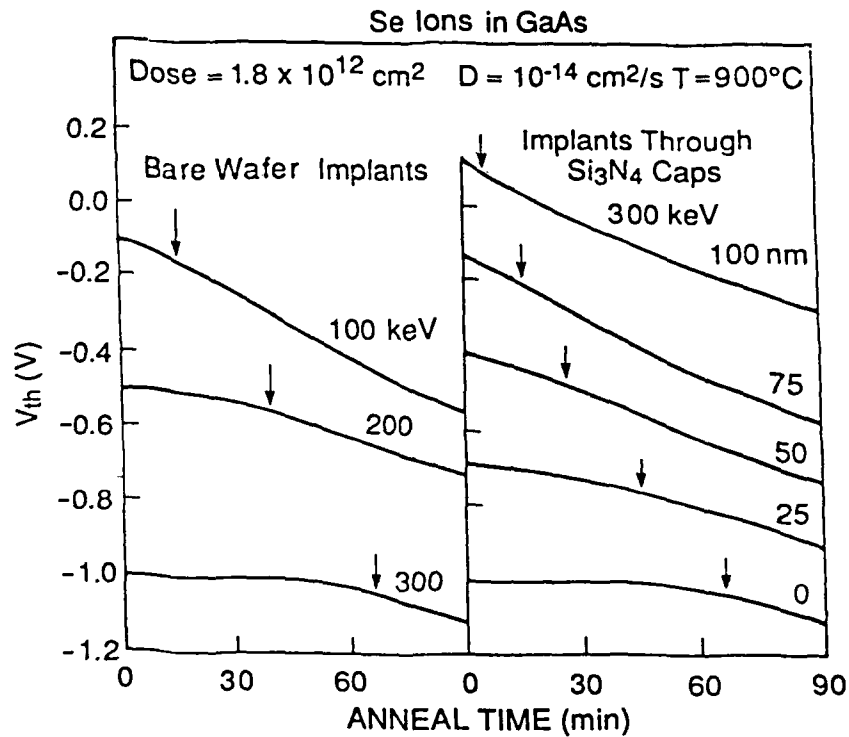


Fig. 4.20. Threshold voltages versus annealing time for 100-, 200- and 300-keV Se ions implanted into bare wafers and for 300-keV Se ions implanted through 25- to 100 nm Si_3N_4 caps. The arrows indicate the minimum time where Eq. (4.15) is satisfied.

by showing calculated threshold voltages versus anneal time for a 900°C anneal of implanted Se. The diffusion constant used, 10^{-14} cm^2/s , is for Se ions at a dose of approximately 3×10^{12} ions/ cm^2 [60]. The arrows in Fig. 4.20 indicate the minimum annealing time t where Eq. (4.15) is satisfied. The device threshold voltages change by less than 50 mV up to where Eq. (4.15) is satisfied, then decrease more steeply for longer anneals. Using this criterion, we can conclude that diffusion during annealing is more important for low-energy implants, and for implants through thick caps, where the effective moment of the implant distribution is smallest.

For MESFET technology the diffusion of Si and Se ions during annealing is usually negligible. Since the diffusion coefficients for Si and Se at typical 800-850°C anneal temperatures are generally smaller than 10^{-14} cm²/s, Eq. (4.15) is rarely satisfied. The use of rapid thermal annealing is becoming popular for various reasons. While short anneal times do limit diffusion, our results show that this should not be a major reason for adopting the rapid thermal annealing technique.

4.2.4 Process Sensitivity

4.2.4.1 Encapsulant Thickness

Implanting through Si₃N₄ or SiO₂ caps has the beneficial effect of reducing the sensitivity of device threshold voltages and other characteristics to implant tilt and rotation angles [62]. On the other hand, the threshold voltages then become sensitive to the cap thickness and density. Figure 4.21 illustrates changes in threshold voltage due to changes in cap

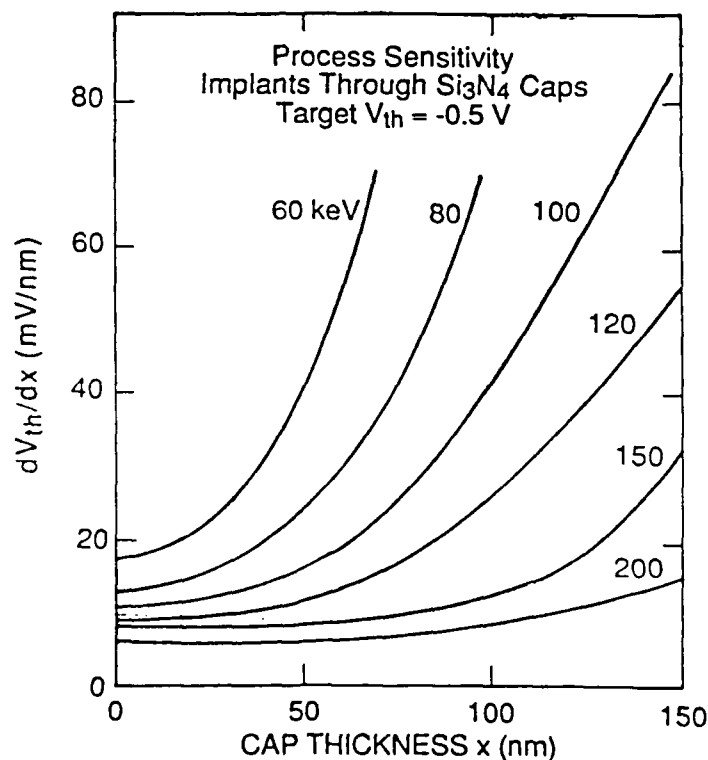


Fig. 4.21.

Changes in threshold voltages due to changes in the cap thickness for 60- to 200-keV Si ion-implanted devices with doses varied to achieve a constant -0.5 V threshold voltage.

thickness for MESFETs implanted with 60- to 200-keV Si ions in the channel. These calculations are for a constant threshold voltage of -0.5 V, so for increasing cap thickness or decreasing implant energy, the ion dose is increased. Once the dose is adjusted, the change in threshold voltage due to a 1- to 2-nm change in cap thickness is calculated. Clearly, the minimum sensitivity occurs only at vanishing cap thickness. The sensitivities are largest for low ion energies, where the ratio of cap thickness to the projected range in GaAs is largest. To achieve a uniform wafer-to-wafer threshold-voltage uniformity of <20 mV for 80-keV Si ions implanted through 50 nm caps, the cap thickness must be controlled to within <1 nm.

4.2.4.2 Recess Etching

For devices with recess-etched gates, the etch depth must be tightly controlled for good uniformity. Figure 4.22 shows calculated sensitivities

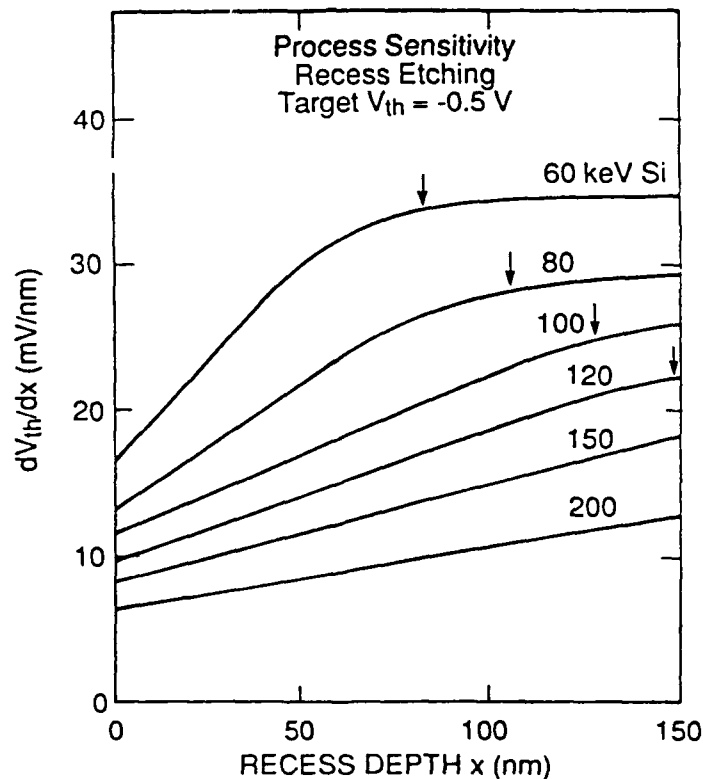


Fig. 4.22.

Changes in threshold voltage due to changes in recess etch depth for 60- to 200-keV Si ion-implanted devices with doses varied to achieve a constant -0.5 V threshold voltage. The implants are done into unencapsulated wafers.

of threshold voltages due to small etch depth variations for 60- to 200-keV Si ion-implanted MESFETs. Here the initial implants are done into unencapsulated wafers with the doses adjusted to obtain constant -0.5 V threshold voltages. Unlike the quadratic sensitivity to cap thickness, the changes in threshold voltage with etch depth are nearly linear, and approach constants when the etch depth exceeds the peak position of the implant concentration (indicated by arrows in Fig. 4.22). Also, the sensitivity to etch depth is smaller than that to cap thickness.

4.2.5 Recoil Ion Effects

When ions are implanted through Si₃N₄ and SiO₂ layers, Si, O or N atoms are knocked forward into the GaAs. The Si ions can be additional donors, adding to the implanted donor concentrations. The N ions are electrically inactive in GaAs, but do contribute more damage in the near-surface region. The O ions can either form deep-donor traps similar to EL2 or can complex with and therefore compensate some of the Si donors, leading to smaller electron concentrations [65].

At the shallow depths where the recoil atom concentrations are large compared to those of the implanted ions, the recoil concentrations can be predicted accurately using the TRIM Monte-Carlo code [57,35]. An extensive set of TRIM calculations were made of recoil-atom distributions, resulting from Si and Se implants through Si₃N₄ and SiO₂ caps at energies between 60 and 400 keV (100 to 400 keV for Se). The recoil-atom distributions were accurately fit to the expression [66]

$$C_R(x) = \frac{A}{x^n + 0.1} \exp(-(x/B)^2), \quad (4.16)$$

where x is the depth in the GaAs in nm, and n (~ 1 to 1.5), B and A are parameters dependent on the ion energy, the cap thickness, the implant ion, and the recoil atom (Si, O, or N).

Figure 4.23 shows calculations of Si recoil-atom concentrations resulting from a 300-keV Se implant through a 100 nm Si₃N₄ overlayer. The parameter B for this implant is approximately 300 nm, therefore the recoil-atom concentrations fall off as a power law function of depth for most depths shown in Fig. 4.23.

Figures 4.24 and 4.25 show the effects of Si recoil atoms on MESFET threshold voltages. For these calculations, the ion dose was adjusted to obtain

an initial threshold voltage of -0.5 V, then the recoil atom distribution was added, and the threshold voltage was recomputed. For a Si ion primary implant, the threshold voltages become as much as 60 mV more negative, while for the larger-mass Se ions, 300 mV changes are found. For a Be implant, with

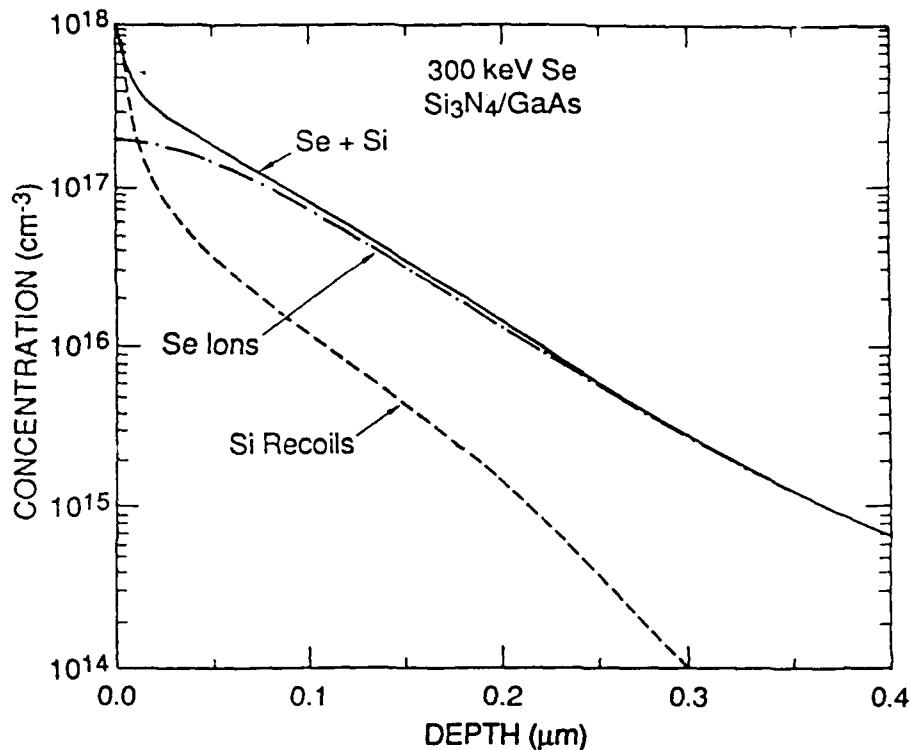


Fig. 4.23. Concentrations of Se ions implanted through 100 nm Si_3N_4 caps and the concentrations of knocked-on Si atoms from the cap.

a typical buried-p-layer implant dose, the change in threshold voltage due to recoils is less than 3 mV. The maximum cap thicknesses t_{cap} considered in these calculations are about $1.5R_{\text{ps}}$, where R_{ps} is the projected ion range in amorphous GaAs [57].

4.2.6 Conclusions

In this paper we have addressed several ion-implantation effects on GaAs MESFET's. With decreasing channel implant energy E , transconductances increase less quickly than $1/E$, the increase over a factor of 10 reduction in E is found to be only a factor of 3 to 4. At low gate biases, transconductances for implanted devices are smaller than for box profiles. The presence of substrate acceptors or implanted buried p layers is found to improve low-bias transconductances.

A criterion has been derived to determine whether or not dopant diffusion during post-implant annealing affects device characteristics. For Si and Se at typical channel implant doses and energies, and with typical 800-

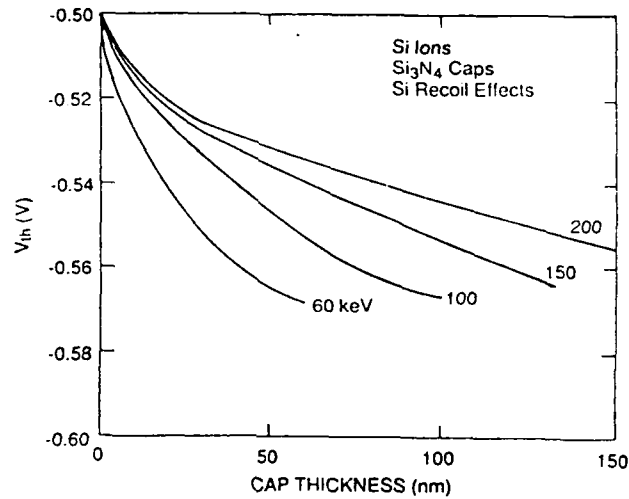


Fig. 4.24.

The effects of knocked -on Si atoms on device threshold voltages when 60- to 200-keV Si ions are implanted through Si_3N_4 caps. Without recoils, a -0.5 V threshold voltage was obtained for all ion energies and cap thicknesses, then the recoil distributions were added, resulting in the threshold voltages shown.

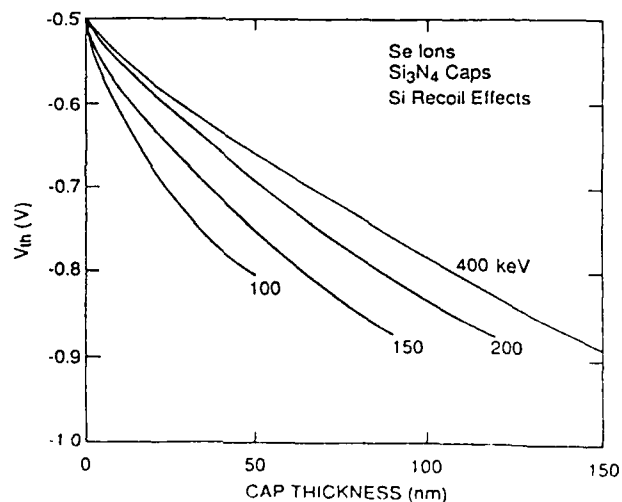


Fig. 4.25.

Same as Fig. 4.24 for Se ion implantation through Si_3N_4 caps.

850°C furnace or rapid thermal anneals, dopant diffusion effects on MESFET threshold voltages are insignificant.

Calculations are presented for the effects of cap-thickness and recess-etch depth fluctuations on threshold voltages. Also, for implantation through these SiO_2 and Si_3N_4 layers, Si atoms from the cap which are knocked forward into the GaAs change threshold voltages by up to 60 mV for Si or 300 mV for Se ion implantation (for a target threshold voltage of -0.5 V).

A quantitative understanding of these effects should greatly benefit the design and optimization of GaAs MESFETs for digital and monolithic-microwave applications.

V. DEVELOPMENT OF PROCESS MODEL

5.1 Background

There is currently a need for process and device modeling tools in the GaAs monolithic-microwave integrated-circuits industry. Crucial to the evolution of high yield GaAs MMIC's the development of processes that tightly control device electrical characteristics, such as ion-implanted MESFET threshold voltages or saturated currents. Process and device modeling can provide a quantitative understanding of materials effects (wafer impurities, dislocations), ion-implant effects (wafer tilt and rotation angles, annealing encapsulant effects), or how day-to-day process variations affect circuit uniformity. Also, the design of MMIC's is crucially dependent on device modeling tools that can accurately predict circuit performance before fabrication. Traditionally MESFET's are fabricated then measured and the device characteristics are fitted to mathematical expressions, suitable for use in SPICE [67-69] or Harmonic balance [70] codes to predict circuit performance. As the measurement techniques used to obtain small-signal parameters are not always unambiguous, device modeling codes that predict these quantities are of great benefit.

In this section we describe a combined process and device model developed under this program for GaAs MESFET technology: Instead of attempting to solve ab initio equations for the transport of ions in matter for ion implant process modeling or multi-dimensional Poisson's and current-continuity equations for device modeling, our code uses analytical models. More than 10 years of GaAs materials and device research has resulted in the availability of many useful process and device models for GaAs MESFETs. The emphasis in the development of the model is the integration of these into a software package that provides an easy-to-use tool for non-modeling-professional process development or manufacturing engineers.

Figure 5.1 we show an overview of the model [71]. The process model section calculates ion-implant impurity profiles in one dimension, and includes the diffusion of dopants during annealing, recess etching, and the indiffusion of dopants from the surface (used in some JFET fabrication processes). To model materials effects, background shallow acceptor and donor [72], EL2 [60], and deep-acceptor (e.g. Cr [20]) concentration profiles

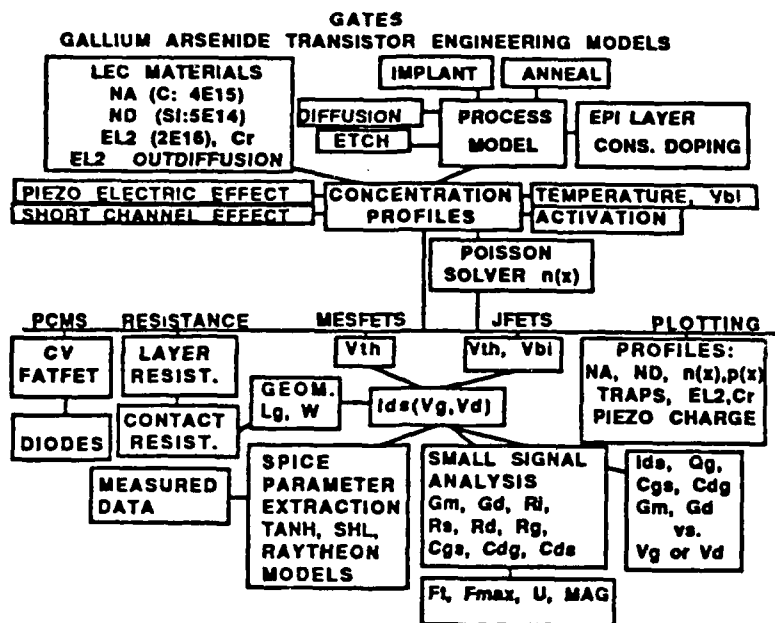


Fig. 5.1. Overview of GATES.

can be constructed. Piezoelectric effects are calculated using the dielectric-edge approximation [73], and short-channel effects, due to the encroachment of n^+ implant profiles into the channel region, are calculated using a method proposed by Chen et al. [74]. Threshold voltages and carrier profiles are obtained from either a Poisson solver [8] or an abrupt-depletion approximation for arbitrary carrier profiles [5], and I_{ds} is calculated using the two-piece mobility approximation [58,75], where compensation effects on mobility and saturated velocity are included [75,76]. For the source and drain resistances for four general types of MESFET topologies, we calculate layer resistivities for arbitrary implants, then we sum the resistances of the various regions between the contact and the gate, according to the specific FET geometry. The contact resistance is calculated using a ND^{-1} dependence [77], though usually the user must override the default values, due to the large process variations in Au/Ge contact resistances [77]. Also, all of the transconductances, capacitances, and resistances, used to determine small- or large-signal characteristics are obtained analytically. For parameter extraction, the I-V curves can be fit to SPICE formulas proposed by Curtice

[67], Statz et al.[68], or Larson [69]. Concentration profiles or electrical characteristics can be plotted.

Sections 5.2 and 5.3 describe the process and device models incorporated into the code. Piezoelectric and short-channel effects are not discussed, as the methods used are similar to those of Chen et al. [74]. As with any modeling program, calibrating some physical parameters is of vital importance.

5.2 Process Models

5.2.1 Ion Implantation

The code allows for four different kinds of profiles in one dimension: implants for the channel donor N_D^- , the source and drain regions N_D^+ , another donor implant N_D' , and an acceptor implant N_A . Multiple implants can be added to any one of these profiles.

Pearson-IV functions [47] are used to model the profiles of Be, Si, and Se ions, [See Section 4.1]. For maximum cross wafer device uniformity and the narrowest profiles for a given ion energy, the code assumes implants are performed at a tilt angle of at least 9° and a rotation angle of 45° from the major flat (011).

In calculating Be profiles in GaAs-implanted through SiO_2 or Si_3N_4 caps, measured profiles for implantation into bare wafers are shifted toward the surface by an amount tR_{pS}/R_{pC} , where t is the cap thickness, and R_{pS} and R_{pC} are the projected ranges in the semiconductor and cap [57] (Fig. 5.2).

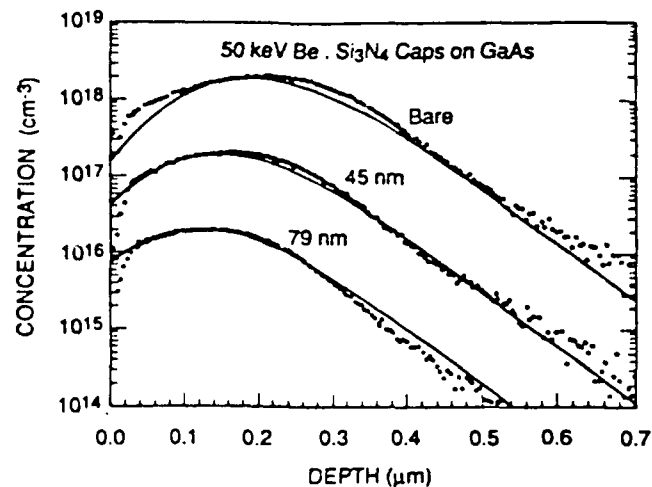


Fig. 5.2. Measured concentration profiles for 50-keV Be ions implanted into bare GaAs wafers and into wafers with 45 and 79 nm CVD Si_3N_4 caps, compared with fits using the range-scaling theory.

Moments of ion distributions in the amorphous cap are interpolated from tables of values, calculated using the TRIM Monte-Carlo code [35]. The dose in the GaAs is normalized to incident ion dose reduced by that lost in the cap. Consistent with TRIM results, a Pearson-I distribution [47] is assumed in the cap.

For Si and Se ions, implanting through caps reduces the magnitudes of the channeling tails. This effect is simulated by mixing a shifted Pearson-IV function with a shifted TRIM-calculated Gaussian function, using

$$C(x) = (1-p)C_{\text{Gaus}}(y) + pC_{\text{PIV}}(y), \quad (5.1)$$

where $y=x-tR_{\text{pS}}/R_{\text{pC}}$, and C_{Gaus} and C_{PIV} are normalized to 1 at $x=R_{\text{p}}$. $C(x)$ is normalized to the dose in the GaAs. This method is illustrated in Fig. 5.3. The mixing factor p ($<1.$) depends on the ratio of the cap thickness t to R_{pS} , but has only been characterized for a few cases [57].

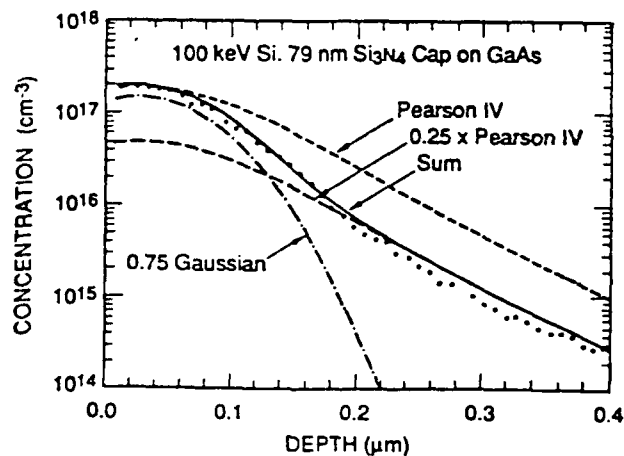


Fig. 5.3. Measured concentration profiles for 100-keV Si ions implanted into GaAs through a 79nm CVD Si_3N_4 cap, compared with fits using Eq. (5.1).

When ions are implanted through SiO_2 and Si_3N_4 caps, Si, O, or N ions are knocked into the GaAs, where the Si ions are additional donors, increasing carrier densities. Knock-on atom distributions are calculated using TRIM [35], and are fit to the expression

$$C_r(x) = \frac{A}{x^a + b} \exp(-(x/a)^2), \quad (5.2)$$

where $b=0.1$ and x is the depth in nm. The parameters $A, a,$ and n for Si, O, or N atoms can be interpolated from tables as a function of cap (SiO_2 or Si_3N_4), cap thickness ($0 < t < 1.3R_p S$), ion (Si or Se), and ion energy (60 to 400 keV). The knock-on concentrations are only significant compared to the implant-ion distribution near the surface (where channeling tails are unimportant), and MESFET pinchoff voltages are increased by $<1\%$ (Be), 5-10% (Si), and 20-30% (Se).

5.2.2 Substrate Materials

Four significant impurities can be found in liquid-encapsulated Czochralski (LEC) or horizontal-Bridgman (HB) grown GaAs substrates [72,74,78]. Table 5.1 gives typical ranges and default values of these

Table 5.1. Wafer Impurity Concentrations (10^{15} cm^{-3}).

Impurity	Ion	LEC wafers		HB wafers	
		Range	Default	Range	Default
Shallow Acceptor	C	1-6	3	$\ll \text{Si}$	0
Shallow Donor	Si	$\ll \text{C}$	0	5-15	10
Deep Donor	EL2	5-20	20	$\ll \text{Cr}$	0
Deep Acceptor	Cr	$\ll \text{EL2}$	0	20-100	50

impurities in modern, manufactured wafers. Both types of wafers are semi-insulating. In LEC wafers, the Fermi level is pinned mid-gap by the compensation of the dominant shallow acceptor by the native deep-donor defect, EL2. In HB wafers, the dominant donor impurities are compensated by added mid-gap acceptor, Cr. The code allows varying these concentrations, to observe their effect.

5.2.3 Diffusion

Dopant diffusion during post-implant annealing is calculated using [47]

$$C(x) = \int_0^{\infty} dx' C'(x') \left[\exp\left[-\frac{(x-x')^2}{4Dt}\right] + \exp\left[-\frac{(x+x')^2}{4Dt}\right] \right], \quad (5.3)$$

where C' and C are the as-implanted and annealed distributions, $D(T)$ is the assumed constant, concentration-independent diffusion coefficient at the anneal temperature T , and t is the anneal time. This expression is a solution

of Fick's equation when no outdiffusion from the substrate is present ($dC/dx=0$ at $x=0$).

The diffusion constants for low-concentration Si, Se and Be ions in GaAs are so small that dopant diffusion during typical furnace anneals is an insignificant factor in MESFET fabrication. MESFET threshold voltages are affected when the diffusion length $\sqrt{4Dt}$ exceeds the mean ion range in the semiconductor, $R_{pS}-tR_{pS}/R_{pC}$ [79]. With typical diffusion constants for Se ions at channel concentrations of 10^{17} cm^{-3} , ($10^{-14} \text{ cm}^2/\text{s}$ at 900°C [60]), anneal times greater than 20 min for bare-wafer implants are needed to affect threshold voltages more than a few percent. Si diffusion constants are not well characterized, but are much smaller [61,63,80]. Buried p layer diffusion could also affect threshold voltages, but diffusion constants for Be or Mg ions at concentrations $<10^{16} \text{ cm}^{-3}$ are not well characterized [81,23,82]. In one case, SIMS measurements detected no diffusion in a Be buried p layer for a typical furnace anneal [23]. It is not well known whether the constant-D assumption, implicit in Eq.(5.3), is valid at these low dopant concentrations, but this assumption has generally been used in the extraction of reported diffusion coefficients.

5.2.4 Recess Etching

Recess etching is modeled by shifting the profiles toward the surface. Automatic etching to a desired threshold voltage or saturated current can be done.

5.2.5 Epitaxial Layers

Competing with ion-implanted MESFET technology is epitaxial-doped-layer growth, best controlled by molecular beam epitaxy or MOCVD methods. Layer thicknesses and doping concentrations can be input to the code. Implant profiles for the source and drain regions can then be added to these profiles to simulate epitaxial-fabricated MESFET's.

5.2.6 Activation

Typical Si and Se donor activation coefficients are between 70% and 95%, and at the small concentrations used for buried p layers, near 100% acceptor activation is usually found. The default donor and acceptor activations used are therefore 80% and 100% for Si and Se, respectively.. Within the expected range of possible activation achieved with different annealing caps [82], temperature and dose [83], and other factors, greatly

varying threshold voltages are predicted. The donor activation can be calibrated using measured threshold voltages.

For the high donor concentrations, used for N_D^+ implants and sometimes for low-energy, high-dose channel implants, the activation may be concentration or depth dependent [84]. At low concentrations, the electron and donor concentrations differ by a constant factor, but above a certain donor concentration, the electron profile is nearly flat (Fig. 5.4).

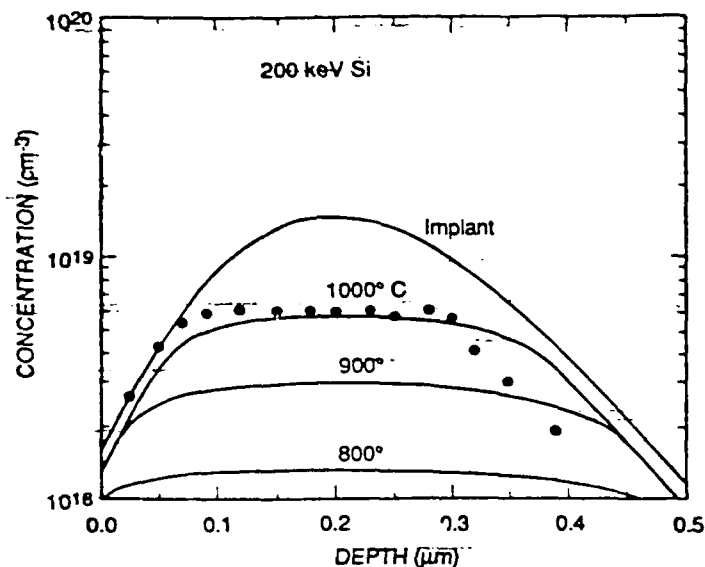


Fig. 5.4. Implant profile for 200-keV Si ions implanted with a dose of 4×10^{14} ions/cm², and GATES calculations of electron carrier densities for anneal temperatures of 800°, 900°, and 1000°C, using Eq. (5.4). The reason for the difference at large depths is not known.

This saturation is modeled by assuming that for amphoteric Si ions, high-concentration activation is controlled by the distribution of Si between Ga and As sites. Assuming equilibrium conditions, this is calculated using [85,13]

$$\frac{[Si_{As}^-]}{[Si_{Ga}^+]} = \gamma = \frac{1}{K_v} \left[\frac{[Si]}{n_i} \right]^4 \left[\frac{1-\gamma}{1+\gamma} \right]^4, \quad (5.4)$$

where K_v is the equilibrium constant for the reaction between Si on As and Ga sites and Ga and As vacancies (see calibration in Sect. IV), $[Si]$ is the total Si concentration, and n_i is the intrinsic electron concentration at the anneal temperature. This model predicts that γ increases from 0 as $[Si]$ increases,

therefore the activation coefficient $\eta=(1-\gamma)/(1+\gamma)$ decreases from unity. Since the low-concentration activation coefficient η_0 is less than unity, we hypothesize a minimum $\gamma=(1-\eta_0)/(1+\eta_0)$. The model predicts that the saturated electron concentration increases (therefore n^+ layer resistivities decrease [86]) with higher anneal temperature. (The opposite effect can occur if As loss is significant. Then K_v decreases with higher temperature, leading to larger γ values, and lower activation.)

5.3 Device Modeling

5.3.1 Threshold Voltages

To simulate device I-V characteristics, carrier densities are required, which are calculated from the derived impurity profiles by solving Poisson's equation in one dimension using a Newton iteration method [8], and using the boundary condition at the surface, $dn(x)/dx=0$. This gives a gate-bias-independent electron profile resembling the active donor profile (Fig. 5.), except near the surface, where the boundary condition forces $n(x)$ to depart from the usually steeply increasing profile, and at large depths, where the substrate junction acts to cut off the tails in the implant profiles (Fig. 5). The MESFET pinchoff V_p and threshold voltages V_{th} are defined as [5]

$$V_p = \frac{q}{\epsilon_0 \epsilon_r} \int_0^{\infty} x dx n(x), \quad V_{th} = V_{bi} - V_p, \quad (5.5)$$

where $V_{bi} \sim 0.78$ V is the Schottky barrier height, which is nearly constant over widely varying process and operating conditions [86]

5.3.2 Layer Resistivity

The conductivity of an implanted layer is given by [86]

$$\sigma = qW/L \int_{x_0}^{\infty} dx n(x) \mu(x), \quad (5.6)$$

where W and L are the layer width and length, and $\mu(x)$ is the electron mobility, which depends on the carrier concentration and on the

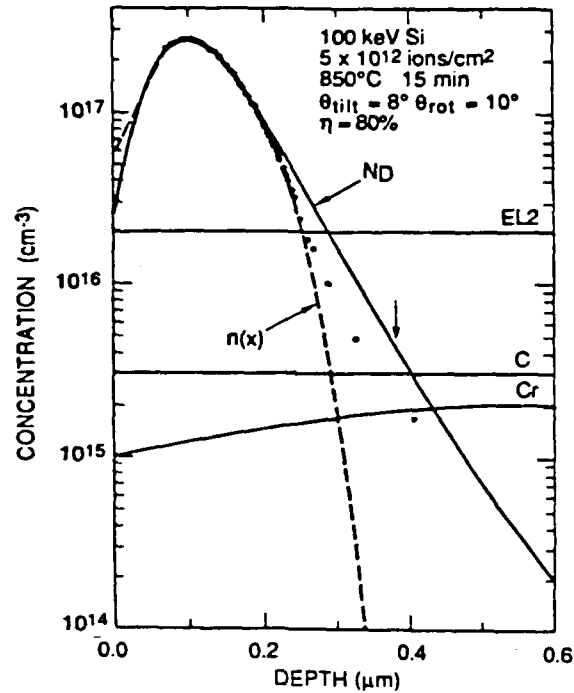


Fig. 5.5.

Comparison of measured Si^{29} donor profiles (solid line), resulting calculated electron profiles (solutions to Poisson's equation for $n(x)$ with zero bias; dashed line), and measured electron profiles, determined using the CV method (points). Also shown are the EL2, C, and Cr concentrations used in the calculations of $n(x)$.

compensation ratio at each depth [75,76]. Similarly, we define the saturated current as

$$I_{\text{sat}} = qW \int_{x_0}^{\infty} dx n(x)v_s(x), \quad (5.7)$$

where v_s is the saturated electron velocity, also depending on the carrier density and compensation, therefore the depth. The code uses Caughey-Thomas expressions for electron mobilities [87] which give good fits to the values tabulated by Walukiewicz et al. [76]. The electron saturated velocity is related to the mobility using $v_{\text{sat}} = (0.64 + 1.38\mu - 0.82\mu^2) \times 10^7 \text{ cm/s}$ (μ is in $\text{m}^2/\text{V/s}$), which was suggested by Xu and Shur [88]. The constants were adjusted to obtain slightly better agreement with Xu and Shur's calculations over the small range of mobilities normally encountered.

GaAs surfaces are pinned by the presence of a surface potential V_{sf} , which is approximately 0.6 V, independent of most types of layers on the surface [89]. This surface potential depletes carriers immediately below the surface, so that instead of integrating from $x=0$ in Eqs.(5.6)-(5.7), the lower limit is x_0 , which in the abrupt depletion approximation [5], is obtained from

$$V_{sf} = \frac{q}{\epsilon_0 \epsilon_r} \int_0^{x_0} x dx n(x), \quad (5.8)$$

5.4 Conclusions

We have described an approach to modeling GaAs MESFET's that makes extensive use of analytical models. This approach provides a tool which has allowed calculations of parameters useful in correlation substrate and process defects with device characteristics.

VI. COMPARISON OF THRESHOLD VOLTAGE FLUCTUATIONS FOR Si AND Se IMPLANTED GaAs MESFETs

6.1 Background

The effect of process variables on LSI circuits is an unresolved issue in GaAs technology. The final parameters are affected by each of the process and material variables. The standard deviation of any MESFET parameter across a 3 inch wafer will vary according to the summation of the standard deviation of each variable. LSI design requires a limited variance on the parameters of these FETs in order to achieve functionality of the desired circuits. The outcome of this scenario is that a manufacturing line establishes a process and limits, as much as possible, any changes to that process.

In the design of an experiment one must choose which steps of the process can be varied without disturbing the process or equipment. Thus, we chose the active implant species as one process variable in our experiment. Both silicon and selenium were chosen as channel implant species, since both are routinely used at the Rockwell GaAs pilot line and should give different results in the planned experiments.

One topic disputed in the literature is the effect of dislocation density on the threshold voltages of MESFETs fabricated on GaAs. Another similar issue is EL2 (a deep level trap) which correlates after crystal growth with dislocation density. That is, dislocation density and EL2 both demonstrate a "W" pattern in distribution on LEC grown wafers throughout a boule. The EL2 distribution, however, will level off following a long term anneal of 10 hours at 850C. It has been assumed that the anneal after implant will also diffuse the distribution. Industry wide whole boule annealing was initially initiated to reduce residual stress in boules to limit cracking during grinding and slicing. The Rockwell grown material used in these experiments was grown under reduced temperature gradients, and thereby there was no concern of cracking and it therefore, did not receive a WHOLE Boule Anneal (WHOBAs). No boule grown under a heat shield at Rockwell has ever cracked during processing. Thus, that these wafers had not been whole boule annealed added an unforeseen material variable not realized until the final stages of the effort.

Another material variable over which there is little control is stoichiometry, the atomic ratio between Ga and As in the boule. This is a known contributor to EL2, however, the control of stoichiometry has always

been done on a macroscopic level with LEC crystal growth. The growth runs are monitored for loss of arsenic via loss in gross weight of the charge which is compensated for by extra arsenic being added to the initial charge. As can be seen from the As-Ga phase diagram this will not control stoichiometry on a macroscopic level. What is needed is to control the As pressure directly with a separate As source. Industry's approach to the dislocation question has been to dope GaAs with In to lower the dislocation density. This works by the larger In atom substituting for Ga and blocking the propagation of dislocations through the material.

Thus our experiments contained one process variable, implant species, and three material variables: In-doping, whole boule annealing, and growth technique (LEC vs VGF). The first lot contained 4 wafers of non-whole annealed In-doped low dislocation material and 4 wafers of annealed high dislocation standard material. The implant species for this lot was Se. Lot #2 was identical to lot #1 except the active channel was implanted with Si. Lot #3 would contain:

Lot #3 (unfinished)

- 4- standard high dislocation, WHOBA LEC wafers;
- 2- In doped, low dislocation, non-WHOBA LEC wafers;
- 2- In doped, low dislocation, WHOBA LEC wafers;
- 2 - non-doped, low dislocation, WHOBA VGF wafers.

This lot was not completed due to exhaustion of the processing and measurement funds by lots 1 and 2.

6.2 Physical Modeling

6.2.1 Model

In the interim technical report issued for this contract (90), we proposed a quantitative relation for carrier activation in Si ion implanted GaAs based on results obtained from several authors (91). This model assumed that a localized defect related to stoichiometry imbalance, namely Ga vacancies (V_{Ga}), was responsible for causing variations observed in the activation of Si implanted GaAs. The value for the activation ratio as a function of V_{Ga} obtained was

$$\eta = \frac{1 - A/V_{Ga}}{1 + A/V_{Ga}} \quad (6.1)$$

where A is a material and temperature related constant. Using the data of (91) relating MESFET threshold voltage to the proximity from a dislocation for Si channel implants, we derived a V_{Ga} concentration dependence as a function of the distance r to a dislocation,

$$V_{Ga}/A = \Delta_B + \Delta_0 \exp [-(r/\sigma)^{1.5}] \quad (6.2)$$

In Eqn. 6.2, Δ_B is the background ratio of Ga vacancies in the material and Δ_0 and σ are chosen for a best fit of the experimental data. The background ratio, Δ_B , is chosen to give the correct *average* percent carrier activation and depends upon the process and implanted atom. For instance, to achieve a 70% activation for Si implanted GaAs annealed under a Si_3N_4 cap, $\Delta_B = 5.6$.

The activation of Si, a Group IV dopant, in GaAs is strongly dependent on the availability of V_{Ga} . For wafers in which there is a non uniform variation in V_{Ga} , a resultant variation in the activation of electrically active Si should result. Selenium, however, being a Group VI element should be much less dependent on the local concentration of V_{Ga} , resulting in a small variation in activation when compared to that of the silicon. The net result should be an increased fluctuation in MESFET electrical parameters for wafers in which a nonuniform distribution of V_{Ga} exists. In the following we describe a numerical and experimental approach with which we verify this hypothesis.

6.2.2 Numerical Calculations

Before the Monte-Carlo calculations can be made we must estimate the base activation of the implanted channel layers. We use our process model GATES to derive the base activation of the Si and Se ions obtained from actual measurements on the devices. For Se, an implantation of 320 keV ions at a total dose of $2.2 \times 10^{12} \text{ cm}^{-2}$ through a 750 \AA Si_3N_4 cap of density 3.3 is used. Including the Si recoils from the cap in the total active dose, an 80% activation is required to achieve the experimentally observed average threshold voltage of $V_T = -0.55 \text{ V}$. Although piezoelectric effects are not completely negligible, even for $L_g = 2 \text{ mm}$, we neglect these in the present calculations. For the Si implants, using 145 keV, identical encapsulant and a dose of $2.2 \times 10^{12} \text{ cm}^{-2}$, we arrive at an activation of 64% to fit the experimentally observed V_T of -0.4 V .

Equation 6.2 forms the basis for our Monte-Carlo calculations. Although we do not expect the parameters derived from the experimental data used to be universally valid, they are used for all the calculations performed following.

Also, since they are likely to vary in unknown ways with substrate factors (e.g. Ga-As stoichiometry, background impurities, boule annealing, etc.) and processing (type of anneal, encapsulant, anneal time, ion dose and energy, etc.) we expect only qualitative agreement with measurements.

We model the device to dislocation distance as a random variable. This is justified since dislocations are, to first order, randomly distributed. We assume that the dislocations are distributed randomly over a wafer area of dimensions $y = 200 \mu\text{m}$ by N_F , where N_F is the number of FET's averaged. The FET's are arranged in a row at $y=100\mu\text{m}$ and are a distance p apart. For any FET in the row, V_{G_a}/A is obtained by summing Eqn. 6.2 over the randomly distributed dislocations in the area which have $r \leq 100 \mu\text{m}$. One then obtains the spatially dependent activation η for the FET and calculates its threshold voltage. A simple average of the threshold voltages of the N_F FET's is then calculated and the standard deviation, ΔV_T obtained. Figure 6.1 shows the threshold

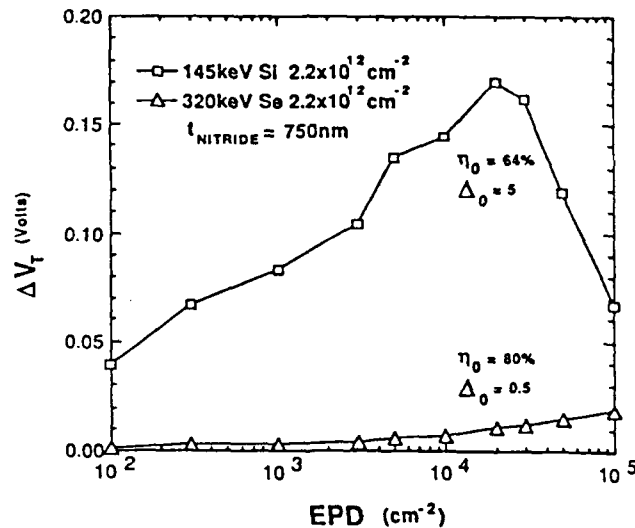


Fig. 6.1. Plot of threshold voltage fluctuation, ΔV_T , versus EPD for Si and Se implanted GaAs MESFETs. The plots are a result of a Monte-Carlo calculation which takes into account the effect of dislocations on MESFET devices. The background activations assumed for the calculations were 64 and 80% for Si and Se, respectively.

voltage standard deviation for 500 FETs, placed $p = 10 \mu\text{m}$ apart for Si and Se channel implants versus Etch Pit Density (EPD). For the Si implanted wafers with $\eta_0 = 64\%$, V_T decreases with increasing EPD, and ΔV_T varies from zero at

zero EPD (no dislocations gives no threshold voltage fluctuations in the present model), to a maximum at $EPD \approx 10^4$ to $2 \times 10^4 \text{ cm}^{-2}$, falling off rapidly at higher EPD. For the Se implanted wafers, a value of $\eta_0 = 80\%$ is used and it is seen that the ΔV_T variations are small ($< 0.01 \text{ V}$) at $EPDs \approx 10^3 \text{ cm}^{-2}$ gradually increasing to $\approx 0.015 \text{ V}$ at $EPDs \approx 5 \times 10^4 \text{ cm}^{-2}$.

6.3 Experimental Approach

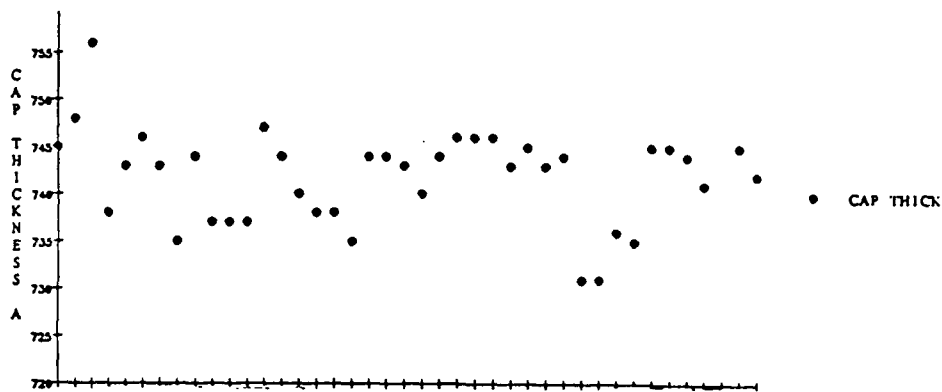
6.3.1 Test Mask Design

The mask was laid out with a line of MESFETs as dense as the Rockwell depletion mode design rules would allow. A group of ten FETs arranged with common gate pads, common source pads and common backgates with separate drains were grouped together in a dense row pattern (DRP). The MESFETs were 5μ wide, 3μ in gate length separated by 10μ . Three rows of 80 DRPs were laid in a field. There are 44 fields per wafer. Therefore a single row across a 3 inch wafer crosses 8 fields or 640 DRPs or 6400 FETs. Five different backgate lengths were split among the fields with backgate lengths of 5, 10, 15, 20, and 50μ .

6.3.2 Process Description

The process chosen for the fabrication of the MESFETs was the then standard depletion mode process at the Rockwell pilot line. Prior to processing, incoming material is qualified and characterized. This involves using a Schottky diode mask set on two representative wafers from each boule. This yields information about the activation of the implant in this material. The boules are rejected or accepted based on C-V measurement results obtained from these diodes.

A) After wafer qualification and acceptance, the GaAs surface is prepared and a Si_3N_4 cap is deposited. The implant profile is dependent on the Si_3N_4 cap thickness and therefore MESFET threshold uniformity can be affected by the reproducibility of the Si_3N_4 cap thickness. Fig 6.2 shows the excellent control over Si_3N_4 thickness at the pilot line. This figure shows the variation in cap thickness over 41 wafer lots. Each data point represents a lot of 5 to 20 wafers. After cap deposition, implant regions are defined and implanted. Two N-implants are required. The first being the standard selenium implant for the channel of the FETs and, as stated earlier, was the process variable of the experiment, the exchange of silicon for selenium. The second N-implant is followed by a deep p-well implant through the N-implant mask. The p-well implant is necessary to improve the radiation hardness of the array.



Sputtered Si_3N_4 cap thickness for 41 lots.

Fig. 6.2. Sputtered Si_3N_4 cap thickness for 41 lots.

B) After implant definition, an SiO_2 layer is deposited using plasma enhanced chemical vapor deposition (PECVD). The SiO_2 layer prevents degradation of the GaAs during implant anneal. After SiO_2 deposition, the wafers are annealed to remove the implant damage.

C) Ohmic and Schottky contacts are made after anneal. The contacts are defined in resist, the SiO_2 cap is opened up using reactive ion etching (RIE) and the Si_3N_4 cap is opened up using a barrel plasma process. After opening the dielectric, ohmic metal is deposited and lifted off. The dielectrics assist in the lift-off process by providing an undercut profile. After ohmic metal definition, the metal is alloyed to provide low contact resistances. Proton isolation implant follows, which is required to increase the resistivity of the substrate thereby decreasing the effect of backgating in LSI circuits. The gate contact areas are defined similar to the ohmic contacts and Ti/Pt metal is deposited and lifted to form the Schottky contacts.

D) A first level SiO_xN_y dielectric is deposited, the wafer is patterned and the metal-1 pattern is recessed through the dielectric vias to the contact metals. Metal 1 is then evaporated and lifted. This results in contact pads for our DRPs and the process was terminated at this point.

6.3.3 Automated Measurements

DC parametric tests were performed on one row of 6400 FETs on each wafer of lots 1 & 2. A Data General MV 4000 computer was programmed to

control the testing, analyze and store the results. The Data General controlled a HP 4145A Semiconductor Analyzer used in conjunction with an Electroglas 1034x automatic prober. (see Fig. 6.3)

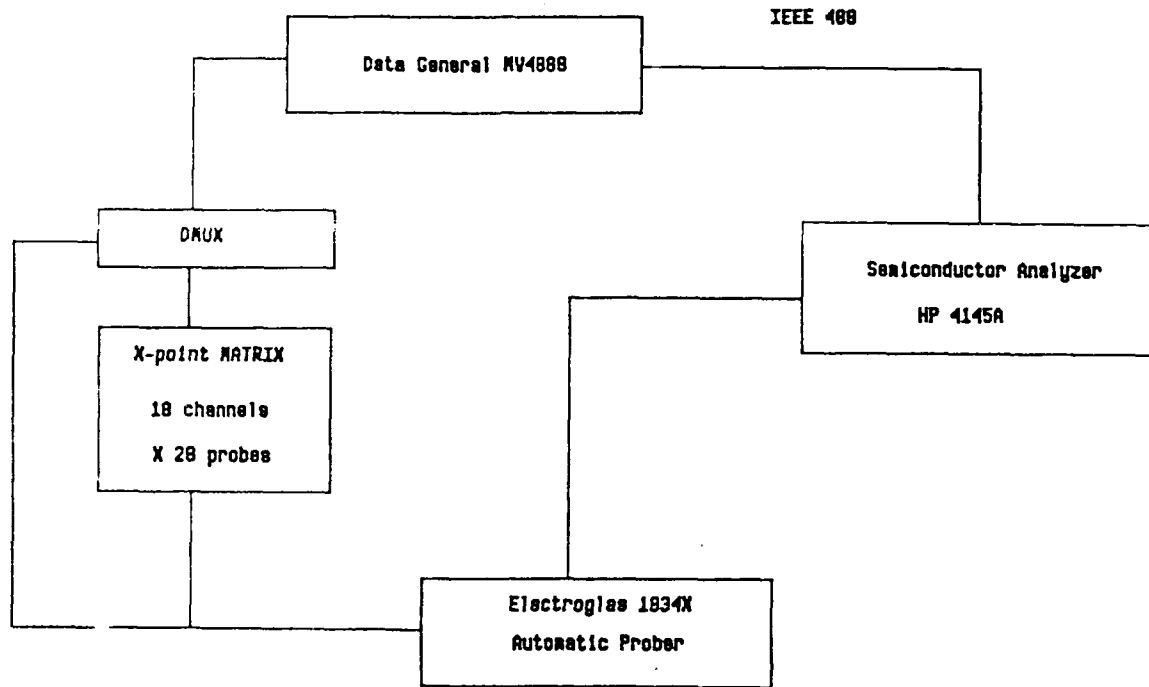


Fig. 6.3. Automatic measurement system block diagram.

Two scans of current vs voltage were made: I_{dS} vs V_g under constant V_{dS} ; and I_{dS} vs V_{dS} under constant V_g , for each FET. This data is digitized and stored on the MV4000 for later analysis. An analysis program performs a least squares fit to determine the parameters V_{th} , I_{dss} , R_{on} , K , G_m , I_{leak} . Next a plotting program graphs the resulting data vs their relative position across the 3 inch wafer, numbering the FETS from 1-6400. The data is then averaged over each DRP eliminating any unwanted correlation associated with drain position or number.

It will be seen from the selenium implant data that no significant differences are observed for V_T between the various starting materials. However, the silicon implanted FETs yielded data with good correlation to material properties.

6.4 Experimental Results

We have measured the fluctuation in MESFET device parameters using a Dense Row Pattern (DRP) of MESFETs. The devices have a 3 μm gate length a 5mm gate width and are spaced on 10 μm centers. This allows up to 6400 FET's to be measured on a line across a three inch wafer. A complete set of Process Control Monitors (PCM) is available for each set of 800 MESFETs. The test structures are fabricated using a simplified, six mask process with all process variables except material and channel implants held constant to minimize process induced defects. The MESFETs are fabricated in a foundry with a proven process (Rockwell MRDC). This approach minimizes unknown variables, thereby allowing enhancement of the effect of material and channel implant variations to be studied, while allowing statistically significant quantities of data to be taken. Each wafer has 6400 MESFETs measured and characterized using an automatic tester and methods developed previously at Rockwell and described above.

We have chosen to study a matrix of material variation using both Si and Se channel implants. This is to examine, in detail, their effect on threshold voltage fluctuations for the two different channel implants, allowing elucidation of the effect described above. Material variations include both low, GaAs(In), dislocation and high dislocation boules with and without whole boule annealing.

6.4.1 Correlation Experiments

In Table 6.1 we show a summary of the measurements completed to date. Each value for V_T and ΔV_T represents the global average of 6400 MESFETs measured on each wafer. The measurement pattern is shown in Fig. 6.4. Each reticule in Fig. 6.4 consists of 800 MESFETs and a PCM. Two different substrate materials are used, MA7041 a whole boule annealed, high dislocation density source (EPD = $5 \times 10^4 \text{ cm}^{-2}$) and R169, a Rockwell grown, non-whole boule annealed low dislocation density source (EPD = 10^3 cm^{-2}). Data are shown for both Se and Si implanted channels. It is seen from these data that the average fluctuation in ΔV_T is about twice as large for the Si implanted wafers when compared to the Se implanted ones.

It can also be noted from Table 6.1 that both the high and low dislocation density materials exhibit similar threshold fluctuations when using the same ion for the channel implant. This can be understood from Fig. 6.4 where we have plotted the results of Monte-Carlo calculations for ΔV_T versus Etch Pit

Density (EPD) with the base activation, η_0 , as a variable. The calculations are for 145 keV, $2.2 \times 10^{12} \text{ cm}^{-2}$ Si and 320 keV, $2.2 \times 10^{12} \text{ cm}^{-2}$ Se channel implants through a 75 nm Si_3N_4 encapsulant, the conditions used in the device fabrication. The interesting result of this calculation is that for certain conditions, namely low activation and high sensitivity to the presence of a dislocation (large Δ_0) a drifted gaussian distribution results which is

Table 6.1. Global average of V_T and ΔV_T for Se and Si implanted MESFET's. Both whole boule annealed high dislocation ($5 \times 10^4 \text{ cm}^{-2}$, MA 7041) and non-whole boule annealed low dislocation (10^3 cm^{-2} , R169) results are listed.

Boule No.	Wafer No.	Channel Implant Ion					
		Se			Si		
		V_T	DV_T	%	V_T	DV_T	%
R169	28	-0.557	0.035	6.28			
In Doped	29	-0.537	0.033	6.15			
	31	-0.519	0.031	5.97			
	32	-0.534	0.044	8.24			
	30				-0.339	0.066	16.56
	33				-0.423	0.060	14.03
MA 7041	148	-0.556	0.041	7.37			
High Disl.	150	-0.455	0.024	5.27			
	151	-0.551	0.028	5.01			
	64				-0.319	0.050	15.64
	65				-0.424	0.055	12.92

strongly influenced by the base activation. For the Si channel implants we calculate a value for η_0 of $\approx 64\%$, and for Se $\approx 80\%$. Using average EPDs of 5×10^4 and 10^3 cm^{-2} , it can be seen from Fig. 6.5 that almost identical ΔV_T s, in the range of about 50 mV result, in reasonable agreement with the experimental values. The results of a similar calculation for the Se implants are also shown on this figure, however since the base activation is such that little threshold fluctuations are seen, it is difficult to differentiate between the fluctuations caused by processing variables versus those caused by dislocations.

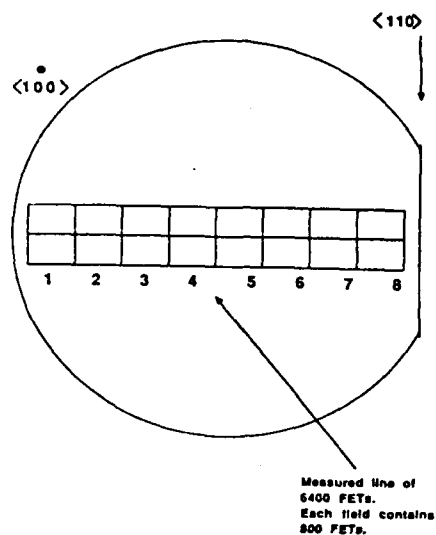


Fig. 6.4. Diagram of the measurement pattern and its location with respect to the wafer orientation. A total of 6400 FETs are measured on each wafer. Each reticule contains 800 FETs and one PCM.

In Fig 6.5 we show selected V_T data taken for both Se and Si channel implants into both high and low EPD material. The higher fluctuation in the Si threshold voltages (Fig. 6.5 b and c) are quite obvious in this data. In Fig. 6.5.d, a negative step in threshold voltage is seen beginning at about FET 2000 and disappears again at about FET 5000. This corresponds well with the value of EL2 mapped for wafers grown from the same boule. In Fig. 6.6, we show a plot of EL2 versus wafer location for an unannealed In doped Rockwell wafer taken by optical absorption at 1100 nm. By comparing the measurement pattern of Fig. 6.6 with the measured EL2 map, a distinct correlation can be made between the measured V_T and the EL2 density, particularly at the center of the wafer which is seen to be rich in EL2. Since EL2 is generally believed to be related to the As antisite, As_{Ga} , the central region in the GaAs(In) wafer should be rich in GaV_a . This will increase the silicon activation, resulting in a more negative V_T as seen in the experimental results.

6.4.2 Backgating Measurements

A considerable effort in programming of the testing and analysis was made on the problem of backgating. Whereas previous backgating work

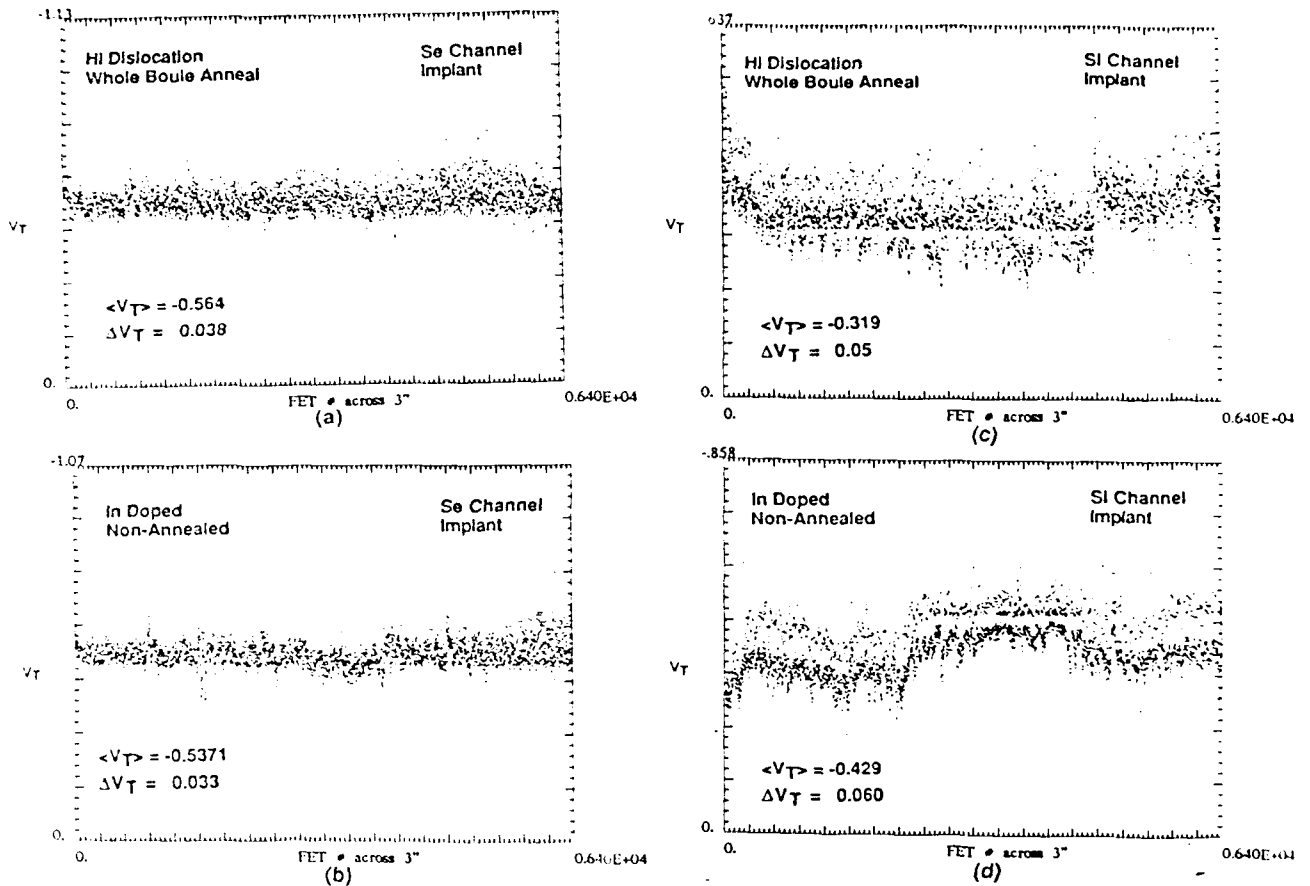


Fig. 6.5. Selected V_T data taken for both Se and Si channel implants into both high ($5 \times 10^4 \text{ cm}^{-2}$) and low (10^3 cm^{-2}) dislocation material. Approximately 6400 devices are measured and their important parameters extracted numerically for this test.

reported in the literature is done on single devices, an attempt was made to measure the effect over 6400 FETs as was done for the other DC parameters. Although many test runs were made and data taken, the results are not promising. There are two significant reasons for this: 1) A good model of the backgating phenomenon has not been defined, that is, to determine V_T , for example a least squares fit of the square root of I_{DS} vs V_{GS} is made on digitized data. No similar standard exists for backgating. Some investigators report a 10% shift in V_T , and some a 10% shift in I_{DSS} . Likewise there is no standard geometry for the placement of the backgate. 2) The initial mask set, while

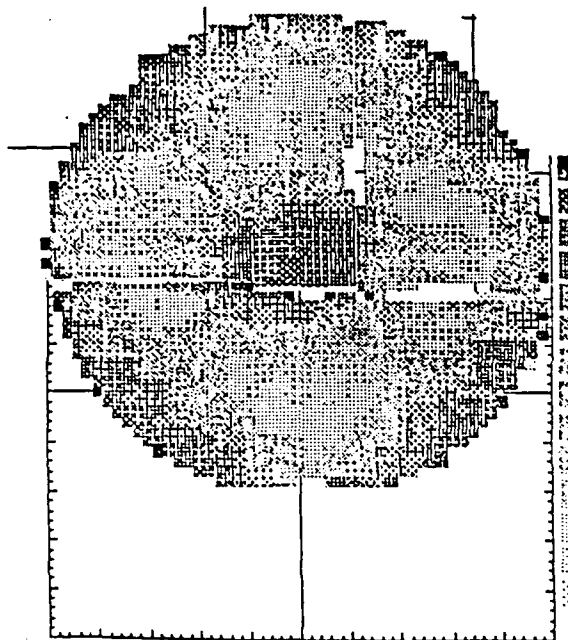


Fig. 6.6.

EL2 map of an In doped, low dislocation wafer from the same boule as the device wafers. A region of high EL2 (and dislocation density) is seen in the center of this wafer. Increasing darkness in the gray scale corresponds to increasing EL2 content.

concentrating on minimizing processing risks, was made using only one metalization layer. This forces the interconnect metal to lye on bare GaAs. In the backgating measurements this affected the data by causing the results to be dependent on the drain number of the FET in the DRP. There remains a need in the GaAs industry for a more comprehensive backgate model and testing procedures.

6.4.3 Etching Experiments

Four of the wafers in lot #2 were to be used to correlate the dislocation density with the measured electrical results. First the interconnect metals were removed by ion milling. This left a demarcation on the bare GaAs substrate of the gate location of each FET. These wafers were then immersed in fresh molten KOH at 450C for 20-25 minutes. This is a standard etchant commonly used to reveal dislocations. The wafers were then cooled and rinsed in deionized water. Photomicrographs were taken of an entire row containing the electrically tested FETs. Three sets of photos were analyzed, R169-32&33

(In-low dislocation), and MA7041-64 (standard LEC). A DRP consists of units of 10 FETs with common source and gate. The parameters of each set of 10 FETs were averaged along the DRP. This set of 640 DRPs are compared to an estimate made for the dislocation density. The estimate of the dislocation density was taken as follows: the number of dislocations within a 150 m circle centered about each DRP subset was counted for the 640 DRPs. Due to the high number of dislocations in standard material, only three fields were counted on MA7041-64. This estimate of the dislocation density was plotted vs the standard deviation of the threshold voltage of each of the FET subsets. Figure 6.7 shows the results of these plots. Figure 6.7 shows the standard deviation of

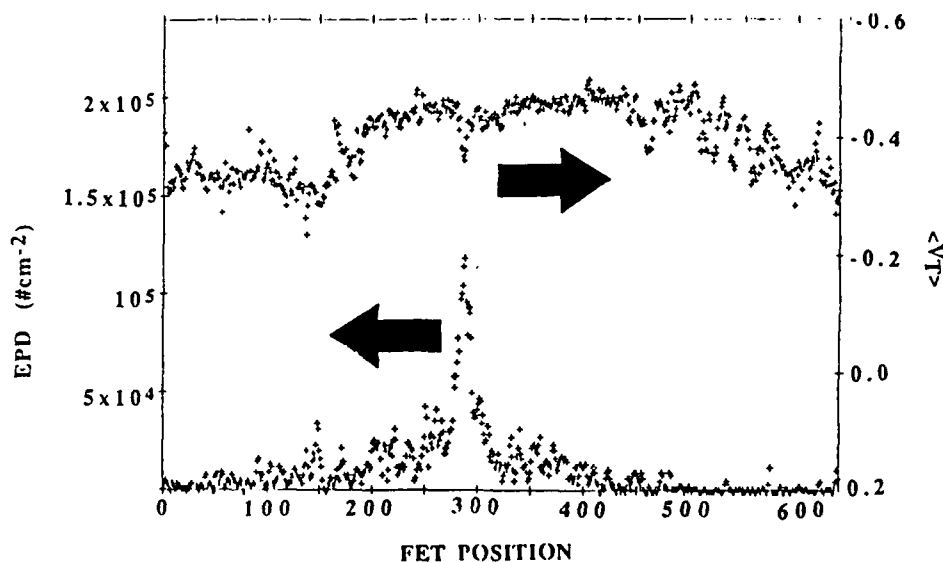


Fig. 6.7. Measured standard deviation of V_T and EPD for wafer R169-32.

V_T across wafer R169-32 and shows the dislocation density across these same FETs. Note where there is a jump in dislocation density there is a substantial dip (more negative) in the corresponding V_T . Figure 6.8 shows a photo of that region. This represents the only region in the low dislocation material where the dislocation cells are near the the measured FETs. This cellular structure observed is due to constitutional supercooling of the In-GaAs alloy. That is, due to the segregation coefficient of In in GaAs, as the bulk growth proceeds In is rejected from the growth interface resulting in an increase in

In concentration in the melt. Finally enough In is present in the melt to cause disruption of the crystal growth. When this occurs a breakdown of the



Fig. 6.8. Photographs of etched Wafer R169-32. The black dots represent etch pits. The outline of the devices can be seen.

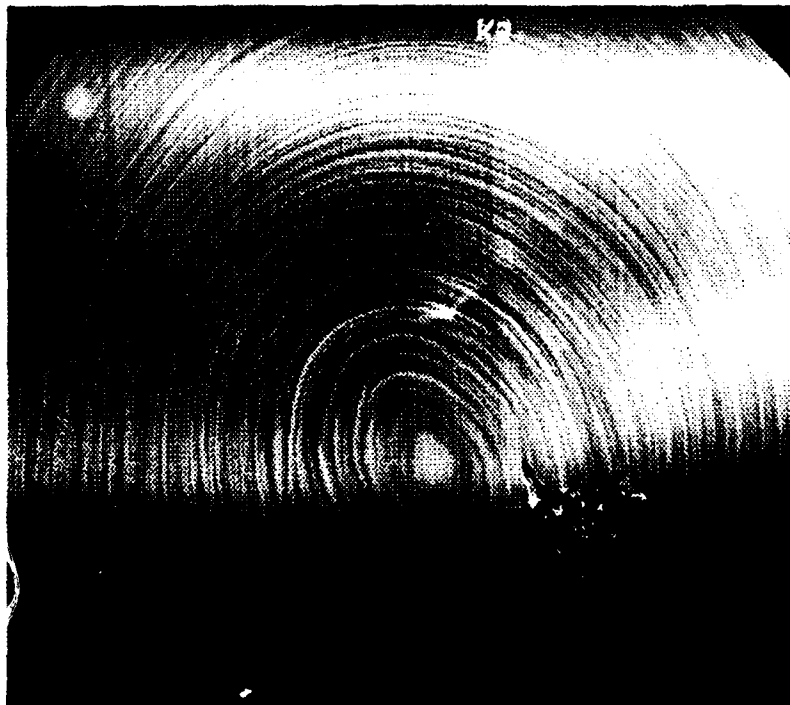


Fig. 6.9. Reflection X-ray topograph of In doped Wafer R169-18. The disrupted area in the lower right indicates a loss of crystallinity.

crystalline structure results. This phenomenon can be observed in Figure 6.9, a reflection X-ray photograph of wafer R169-18. The disrupted area on the X-ray photo is an indication of the loss of crystallinity in that area. This wafer is from the same boule as R169-32 only it is 14 wafers toward the seed end in front of it. This breakdown induces dislocations which trail into the line of FETs as observed in Fig 6.8 above. The FETs measured electrically were not in the area of the breakdown.

6.5 Conclusions

The results we have observed indicate that a strong correlation of V_T with dislocation density does exist. However, the number of process and material variables which are uncontrolled tend to mask the correlation. A way to resolve these cross correlated results is to increase the amount of data for statistical purposes. The model developed during this effort has predicted the results quite adequately. Processing of Lot #3 would certainly strengthen the final conclusions, as it would include both WHOBA In doped material (to redistribute the EL2) and VGF AT&T material (low EPD uniform EL2).

REFERENCES

1. P. Dobrilla, J.S. Blakemore, *J. Appl. Phys.* **61**, 1442 (1987).
2. P. Dobrilla, J. S. Blakemore, A.J. McCamant, K. R. Gleason, R.Y. Koyama, *Appl. Phys. Lett.* **47**, 602 (1985).
3. D.J. Stirland, M.R. Brozel, I. Grant, *Appl. Phys. Lett.* **46**, 1066 (1985).
4. K.J. Kuhn and T.W. Sigmon in *Semi-insulating III-V Materials-1986* (to be published by Shiva Press, Nautwich, UK).
5. C.H. Chen, M. Shur, A. Peczalski, *IEEE Trans. Electron Devices* **ED33**, 792 (1986).
6. S. Makram-Ebeid, D. Gaufard, P. Devillard, G.M. Martin, *Appl. Phys. Lett.* **40**, 161 (1982).
7. C.G. Kirkpatrick, R.T. Chen, D.E. Holmes, K.R. Elliott, in *Gallium Arsenide* (M.J. Howes and D.V. Morgan, Ed., New York, Wiley, 1984) ch. 1.
8. R.W. Klopfenstein, C.P. Wu, *IEEE Trans. Electron Devices* **ED22**, 329 (1975).
9. R.G. Wilson in *GaAs and Related Compounds 1984* (Inst. Phys. Conf. Series 74, 1984), p. 71.
10. D.V. Morgan, F.H. Eisen in *Gallium Arsenide* (M.J. Howes and D.V. Morgan, Ed., New York, Wiley, 1984) Ch. 5.
11. Y. Umemoto, S.Takahashi, M. Matsunaga, M. Nakamura, K. Ueyanagi, *IEEE 1982 GaAs IC Symp. Technical Digest*, p. 173.
12. D. Rumsby, R.M. Ware, B. Smith, M. Tybjerg, M.R. Brozel, and E.J. Foulkes, in *IEEE 1983 GaAs IC Symp. Technical Digest*, p. 34.
13. R. Anholt, T.W. Sigmon, *IEEE Elect. Device Lett.* **EDL8**, 16 (1987).
14. R. Anholt, T.W. Sigmon, unpublished.
15. S. Miyazawa, K. Wada, *Appl. Phys. Lett.* **48**, 905 (1986).
16. R.T. Chen, D.E. Holmes, P. Asbeck, *Appl. Phys. Lett.* **45**, 459 (1984).
17. H.M. Hobgood, G.W. Eldrige, D.L. Barrett, R. N. Thomas, *IEEE Trans. Elect. Devices* **ED28**, 140 (1981).
18. W.M. Duncan, G.H. Westphal, *1986 GaAs and Related Compounds Conference* (Hilger, Bristol, Inst. Phys. Conf. Series 83, 1987), p. 39
19. C.G. Kirkpatrick, R.T. Chen, D.E. Holmes, and K.R. Elliott in *Gallium Arsenide* (ed. by M.J. Howes and D.V. Morgan, Wiley, New York, 1985), p.61.
20. M.D. Deal, D.A. Stevenson, *J. Appl. Phys.* **59**, 2398 (1986).

21. R. Anholt, T.W. Sigmon, to be published J. Appl. Phys.
22. C.G. Kirkpatrick, in *1986 GaAs IC Symposium* (IEEE-Press), p.105.
23. H.M. Macksey, G.E. Brehm, S.E. Matteson, IEEE Electron Device Lett. *EDL8*, 116 (1987).
24. R.S. Butlin, D.Parker, I. Crossley, J.Turner, *1977 GaAs and Related Compounds* (Inst. Physics Conf. Series No. 33a), p. 327.
25. Y. Homma, Y. Ishii, T. Kobayashi, J. Osaka, J. Appl. Phys. *57*, 2931 (1985).
26. R.T. Blunt and P. Davies, J. Appl. Phys. *60* , 1015-1018, 1986.
27. J. Kasahara, H. Sakurai, T. Suzuki, M. Arai, and N. Watanabe, Technical Digest, 1985 GaAs IC Symposium, p. 37.
28. J.F. Ziegler and R.F. Lever, Appl. Phys. Lett. *46*, 358-361, 1985.
29. K. Cho, W.R. Allen, T.G. Finstad, W.K. Chu, G.J. Liu, and J.J. Wortman, Nucl. Inst. Meth. *B7/8*, 265-272, 1985.
30. D. Rosenblatt, W.R. Hitchens, R. Anholt, T.W. Sigmon, IEEE Elect. Dev. Letters *EDL9*, 139 (1988).
31. M.I. Current, N.L.Turner, T.C. Smith, D. Crane, Nucl. Inst. Methods *B6*, 336 (1985).
32. R.B. Liebert, D.F. Downey, V.K. Bason, Nucl. Inst. Methods *B21*, 391 (1987).
33. A.E. Mitchel, R.H.Kasel, S.R. Mader, B.J. Masters, J.A. Gardner, Appl. Phys. Lett. *44*, 404 (1984).
34. J.F. Gibbons, W.S. Johnson, and S.W. Mylroie, *Projected Range Statistics* (Stoudsburg, Pa., Dowden, Hutchinson, and Ross, 1975).
35. J.P. Biersack and L.G. Haggmark, Nucl. Inst. Methods *174*, 257 (1980).
36. L.A. Christel, J.F. Gibbons, S. Mylroie, J. Appl. Phys. *51*, 6176 (1980).
37. J.P. Biersack and J.F. Ziegler *Ion Implantation Techniques* (New York, Springer, 1982), p. 122.
38. J.F. Ziegler, J.P. Biersack, and U. Littmark, *The Stopping and Range of Ions in Solids* (New York, Pergammon, 1985), vol 1.
39. S. Sze, *Physics of Semiconductor Devices* (Wiley, New York, 1981), Ch. 6.
40. M.T. Robinson and O.E. Oen, Phys. Rev. *132*, 2385 (1963).
41. O.S. Oen and M.T. Robinson Nucl. Inst. Methods *132*, 647 (1976).

42. M.T. Robinson in *Sputtering by Particle Bombardment I* (ed. by R. Behrisch, New York, Springer, 1981), Ch. 3.
43. M. Giles, IEEE Trans. Computer Aided Design CAD-5, 679 (1986).
44. T. Takeda, S. Tazawa, and A. Yoshii, IEEE Trans. Electron Devices ED33, 1278 (1986).
45. H. Ryssel and I. Ruge *Ion Implantation* (New York, Wiley, 1986).
46. S. Selberherr *Analysis and Simulation of Semiconductor Devices* (Wien, Springer, 1984), ch. 3
47. H. Ryssel and J.P. Biersack, in *Process and Device Modeling* (ed. by W.L. Engl, Amsterdam, North-Holland, 1986).
48. Formulas for Pearson-IV distributions can be found in refs. 40 to 51. To avoid computer overflow errors, calculate the log of the distribution, and subtract the log of the distribution at $x=R_p$ before taking the exponential, and normalizing the resulting distribution to the ion dose.
49. J.D. Jackson, *Classical Electrodynamics* (New York, Wiley, 1962), Ch. 13.
50. Y.K. Yeo, Y.S. Park, F.L. Pedrotti, B.D. Choe, J. Appl. Phys. 53, 6148 (1982).
51. D.W.E. Allsopp, A.R. Peaker, Sol. State Elec. 29, 467 (1986).
52. A.R. von Neida, S.J. Pearton, M. Stavola, R. Carusso, Appl. Phys. Lett. 49, 1708 (1986).
53. Boule data sheet, Dowa Chemical Co.
54. W.A. Coghlan, M.N. Rhee, J.M. Williams, L.A. Streit, P. Williams, Nucl. Inst. Methods B16, 171 (1986).
55. The In-doped wafers were grown by D. Holmes and co-workers at Rockwell International.
56. M.J. Tejwani, P. Riemenschneider, Nucl. Inst. Methods B21, 471 (1987).
57. R. Anholt, P. Balasingam, S. Chou, T.W. Sigmon, "Ion-Implantation into GaAs," J. Appl. Phys, 64 (7), 3429-3439, (October 1988).
58. R.A. Pucel, H.A. Haus, H. Statz, "Signal and noise properties of GaAs FETs" Ad. Electronics Elec. Phys. 38 193 (1975).
59. S.Sugitani, K. Yamasaki, H. Yamazaki "Characterization of a thin Si-implanted and rapid-thermal annealed n-GaAs layer," Appl. Phys. Lett. 51, 806 (1987).
60. J. Kasahara and N. Watanabe, "Redistribution of implanted impurities in semi-insulating GaAs" in *Semi-Insulating III-V Materials*, Evian, 1982 (Shiva Pub. Ltd., Nantwich, 1983), p. 238.

61. M.D. Deal, S.E. Hansen, R. Anholt, S. Chou, J.D. Plummer, R.W. Dutton, T.W. Sigmon, D.A. Stevenson, C.R. Helms, J.C. Bravman, "SUPREM 3.5, Process Modeling of GaAs," *Technical Digest, 1987 IEEE IEDM Conference*, p. 256.
62. T. Ohnuma, T. Hirao, T. Sugawa "Study of encapsulants for annealing Si-implanted GaAs," *J. Electrochem. Soc.* 129. 837 (1982).
63. H. Kanber, M. Feng, V.K. Eu, R.C. Rush, W.B. Henderson, "Correlation between chemical and electrical profiles in Si, Se, and S implanted GaAs," *J. Elec. Mat.* 11 1083 (1982).
64. T.E. Seidel, A.U. Macrae, *Trans. Metal. Soc. AIME* 245. 491 (1969).
65. H.C. Gatos, M. Skowronski, L. Pawlowicz, J. Lagowski "Oxygen in GaAs: direct and indirect effects.", in *GaAs and Related Compounds Biarritz*, 1984, (Bristol, Adam Hilger, Inst. Phys. Conf. Series No. 74, 1985), p. 41.
66. R. Anholt, T.W. Sigmon, "Recoil Ion distributions in GaAs," unpublished.
67. W.R. Curtice, "A MESFET model for use with GaAs IC's," *IEEE Trans. Microwave Theory Tech.* MTT28, 448-456, May 1980.
68. H. Statz, P. Newman, I.R. Smith, R.A. Pucel, H.A. Haus, "GaAs FET Device and Circuit Simulation in SPICE", *IEEE Trans. Elect. Devices* ED34, 160-169, Feb. 1987.
69. L.E. Larson, "Improved GaAs MESFET equivalent circuit model," *IEEE J. Sol. State Circuits*, SC22, No. 4, 567 (1987).
70. M.A. Khatibzadeh, R.J. Trew, "A large signal, analytic model for GaAs MESFET's," *IEEE Trans. Microwave Theory and Techniques* MTT36, 231 (1988).
71. R. Anholt, T.W. Sigmon, and M. Deal, "Process and Device models for GaAs MESFET technology," *Technical digest, 1987 GaAs IC Symposium*, p. 53-56. (Gates was called GEM in this paper.).
72. W. Duncan and G.H. Westphal, "Effects of residual acceptors on the electrical treatment of low-pressure LEC," in *GaAs and Related Compounds 1986* (Bristol, Adam Hilger, Inst. Phys. Conf. Ser. NO. 83, 1987), p. 39.
73. P.M. Asbeck, C.P. Lee, M.C.F. Chang, "Piezoelectric effects in GaAs FETs," *IEEE Trans. Elect. Devices* ED31, 1377-1380, Oct. 1984.
74. C.H. Chen, A. Peczalski, M.S. Shur, and H.K. Chung, "Orientation and ion-implanted transverse effects in self-aligned GaAs MESFETs," *IEEE Trans. Elect. Devices* ED34, 1470-1481, July 1987.
75. J.M. Golio and R.J. Trew, "Profiles studies of ion-implanted MESFETs," *IEEE Trans. Elect. Devices* ED30, 1844-1849, Dec. 1983.

76. W. Walukiewicz, L. Lagowski, L. Jastrzebski, M. Lichtensteiger, H.C. Gatos, "Electron mobility and free-carrier absorption in GaAs: determination of the compensation ratio," *J. Appl. Phys.* 50, 899-908, Feb. 1979.
77. N. Braslau, "Alloyed ohmic contacts to GaAs," *J. Vac. Sci.* 19, 803-807, Sept. 1981.
78. R.N. Thomas, H.M. Hobgood, G.W. Eldridge, D.L. Barrett, T.T. Braggins, L.B. Ta, S.K. Wang, "High purity LEC growth and implantation of GaAs for MMIC's," *Semiconductors and Semimetals* 20, 1 (1984).
79. R. Anholt, T.W. Sigmon, "Ion-implant effects on GaAs MESFET's," paper submitted to *IEEE Trans. Elect. Devices*, 1988.
80. Based on SIMS comparisons of as-implanted and annealed Si profiles using SiO₂ caps, we discount the CV measurements of diffusion constants of T. Ohnuma, T. Hirao, T. Sugawa, "Study of encapsulants for annealing Si-implanted GaAs," *J. Electrochem. Soc.* 129, 837 (1982).
81. W.V. McLevige, M.J. Helix, K.V. Vaidyanathan, B.G. Streetman, "Electrical profiling and optical activation studies of Be-implanted GaAs," *J. Appl. Phys.* 48, 3342 (1977).
82. F. Hyuga, K. Watanabe, J. Osaka, K. Hoshikawa, "Activation Mechanism of Si implanted into semi-insulating GaAs," *Appl. Phys. Lett.* 48, 1072 (1986).
83. Y.K. Yec, R.L. Hengehold, Y.Y. Kim, A. Ezis, Y.S. Park, J.H. Ehret, "Substrate dependent electrical properties of low-dose Si implants in GaAs," *J. Appl. Phys.* 58, 4083 (1985).
84. D.E. Davies, P.J. McNally, J.P. Lorenzo, M. Julien, "Incoherent annealing of implanted layers in GaAs," *IEEE Electron Device Lett.* EDL3, 102 (1982).
85. M. Greiner, "Silicon Diffusion in GaAs using Rapid Thermal Processing," Ph.D. thesis, Stanford University, 1984.
86. A. Chandra, C. Wood, D.W. Woodard, L.F. Eastman, "Substrate and Interface Depletion Corrections to Free-Carrier Density Determinations," *Solid. State Elec.* 22, 645 (1979).
87. C.M. Maziar and M.S. Lundstrom, "Caughey-Thomas parameters for electron mobilities in GaAs," *Elect. Lett.* 22, 565 (1986).
88. J.S. Xu and M.S. Shur, "Velocity field dependence in GaAs," *IEEE Trans. Elect. Dev.* ED34, 1831 (1987).
89. W.E. Spicer and S.J. Eglash, "Unified defect model and its application of GaAs IC's," Ch. 3 of *VLSI Electronics Microstructure Science* (Academic, New York, 1985), Vol. 10, p. 79.

90. T.W. Sigmon and R.E. Anholt, "Advanced Growth and Process Modeling for GaAs," Interim Report, Feb. 1987.
91. S. Miyazawa and K. Wade, Appl. Phys. Lett. 48, 905 (1986).