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INVESTIGATION OF RADIATION EFFECTS ON SEMICONDUCTOR DEVICES AND INTEGRATED CIRCUITS

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19 ABSTRACT (Continue on reverse if necessary and identify by block number)

Results of a study of radiation effects on electronic materials, devices, and integrated circuits are presented in this report. Emphasis was placed on determining the underlying mechanisms responsible for observed radiation effects with a view toward gaining understanding of value in the development of radiation-hardened devices. Measurements and analyses were performed of the effects of single energetic neutrons and protons on silicon integrated circuits. In addition, a detailed description is given of the effects of radiation-induced displacement damage on device depletion regions. Single event upset studies included charge collection and transient current measurements on Si and GaAs devices following a single alpha-particle strike. The angular dependence of charge funneling was also investigated. The mechanisms of ionizing radiation effects on Si MOS devices were explored in detail using the thermally stimulated current technique and other measurement approaches. Data obtained by several techniques show that use of the radiation-induced shift of the capacitance-voltage curve at midgap is not generally valid for determining oxide trapped charge.

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Single Event Phenomena
Thermally Stimulated Current
Charge Collection
Proton Effects

Hole Traps
Permanent Damage
Ionizing Radiation Effects
Neutron Effects

Accession For		
NTIS GRA&I	☒	
DTIC TAB	☐	
Unannounced	☐	
Justification		
By		
Distribution/		
Availability Codes		
	Avail and/or	
Dist	Special	
A-1		

QUALITY INSPECTED 2

CONVERSION TABLE

Conversion factors for U.S. Customary to metric (SI) units of measurement

MULTIPLY ⟶ BY ⟶ TO GET

TO GET ⟵ BY ⟵ DIVIDE

angstrom	1.000 000 X E -10	meters (m)
atmosphere (normal)	1.013 25 X E +2	kilo pascal (kPa)
bar	1.000 000 X E +2	kilo pascal (kPa)
barn	1.000 000 X E -28	meter^2 (m^2)
British thermal unit (thermochemical)	1.054 350 X E +3	joule (J)
calorie (thermochemical)	4.184 000	joule (J)
cal (thermochemical)/cm^2	4.184 000 X E -2	mega joule/m^2 (MJ/m^2)
curie	3.700 000 X E +1	*giga becquerel (GBq)
degree (angle)	1.745 329 X E -2	radian (rad)
degree Fahrenheit	$t_K = (t°f + 459.67)/1.8$	degree kelvin (K)
electron volt	1.602 19 X E -19	joule (J)
erg	1.000 000 X E -7	joule (J)
erg/second	1.000 000 X E -7	watt (W)
foot	3.048 000 X E -1	meter (m)
foot-pound-force	1.355 818	joule (J)
gallon (U.S. liquid)	3.785 412 X E -3	meter^3 (m^3)
inch	2.540 000 X E -2	meter (m)
jerk	1.000 000 X E +9	joule (J)
joule/kilogram (J/kg) (radiation dose absorbed)	1.000 000	Gray (Gy)
kilotons	4.183	terajoules
kip (1000 lbf)	4.448 222 X E +3	newton (N)
kip/inch^2 (ksi)	6.894 757 X E +3	kilo pascal (kPa)
ktap	1.000 000 X E +2	newton-second/m^2 (N-s/m^2)
micron	1 000 000 X E -6	meter (m)
mil	2.540 000 X E -5	meter (m)
mile (international)	1.609 344 X E +3	meter (m)
ounce	2.834 952 X E -2	kilogram (kg)
pound-force (lbs avoirdupois)	4.448 222	newton (N)
pound-force inch	1.129 848 X E -1	newton-meter (N·m)
pound-force/inch	1.751 268 X E +2	newton/meter (N/m)
pound-force/foot^2	4.788 026 X E -2	kilo pascal (kPa)
pound-force/inch^2 (psi)	6.894 757	kilo pascal (kPa)
pound-mass (lbm avoirdupois)	4.535 924 X E -1	kilogram (kg)
pound-mass-foot^2 (moment of inertia)	4.214 011 X E -2	kilogram-meter^2 (kg·m^2)
pound-mass/foot^3	1.601 846 X E +1	kilogram/meter^3 (kg/m^3)
rad (radiation dose absorbed)	1.000 000 X E -2	**Gray (Gy)
roentgen	2.579 760 X E -4	coulomb/kilogram (C/kg)
shake	1.000 000 X E -8	second (s)
slug	1.459 390 X E +1	kilogram (kg)
torr (mm Hg, 0° C)	1.333 22 X E -1	kilo pascal (kPa)

*The becquerel (Bq) is the SI unit of radioactivity; 1 Bq = 1 event/s.
**The Gray (Gy) is the SI unit of absorbed radiation.

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SECTION 1

INTRODUCTION

Results of a study of radiation effects on electronic materials, devices, and integrated circuits are presented in this report. Emphasis was placed on determining the underlying mechanisms responsible for observed radiation effects with a view toward gaining understanding of value in the development of radiation-hardened devices. The primary topics investigated and reported on herein are displacement damage effects, single event phenomena in gallium arsenide and silicon devices, and ionizing radiation effects on silicon MOS devices. Section 2 presents a detailed description of the effects of radiation-induced displacement damage on device depletion regions. In Section 3, results of single event upset studies are given. Section 4 presents a review of the MOS physics studies performed on this program.

The technical papers prepared and published as a direct result of work performed under this contract are listed here. These papers are presented in Appendices A through H of this report.

A. M.A. Hopkins and J.R. Srour, "Charge Collection Measurements on GaAs Devices Fabricated on Semi-Insulating Substrates," IEEE Transactions on Nuclear Science, Vol. NS-31, pp. 1116-1120, December 1984.

B. J.R. Srour and R.A. Hartmann, "Effects of Single Neutron Interactions in Silicon Integrated Circuits," IEEE Transactions on Nuclear Science, Vol. NS-32, pp. 4195-4200, December 1985.

C. Z. Shanfield, M.M. Moriwaki, W.M. Digby, J.R. Srour, and D.E. Campbell, "Characteristics of SEU Current Transients and Collected Charge in GaAs and Si Devices," IEEE Transactions on Nuclear Science, Vol. NS-32, pp. 4104-4109, December 1985.

D. Z. Shanfield and M.M. Moriwaki, "Radiation-Induced Hole Trapping and Interface State Characteristics of Al-gate and Poly-Si Gate MOS Capacitors," IEEE Transactions on Nuclear Science, Vol. NS-32, pp. 3929-3934, December 1985.

E. Z. Shanfield and M.M. Moriwaki, "Investigation of Trapped Oxide Charge in MOS Devices," in Proceedings of the 1986 International Symposium for Testing and Failure Analysis, American Society of Metals (Symposium held 20-24 October 1986, Los Angeles, CA), pp. 219-222.

F. J.R. Srour, R.A. Hartmann, and K.S. Kitazaki, "Permanent Damage Produced by Single Proton Interactions in Silicon Devices," IEEE Transactions on Nuclear Science, Vol. NS-33, pp. 1597-1604, December 1986.

G. Z. Shanfield and M.M. Moriwaki, "Critical Evaluation of the Midgap-Voltage-Shift Method for Determining Oxide Trapped Charge in Irradiated MOS Devices," IEEE Transactions on Nuclear Science, Vol. NS-34, pp. 1159-1164, December 1987.

H. Z. Shanfield, K.S. Kitazaki, M.M. Moriwaki, and D.E. Campbell, "Angular Dependence of Charge Funneling in Si and GaAs Devices," IEEE Transactions on Nuclear Science, Vol. NS-34, pp. 1341-1346, December 1987.

Items B and F received the Outstanding Paper Award for the IEEE Nuclear and Space Radiation Effects Conferences for 1985 and 1986, respectively. For completeness, one additional paper is noted here that is based on work performed under this contract: Z. Shanfield and M.M. Moriwaki, "Effects of Processing Variations on the Radiation Sensitivity of MOS Devices," Journal of Radiation Effects Research and Engineering, Vol. 5, No. 1A, pp. 1-10, Winter 1986.

SECTION 2

DISPLACEMENT DAMAGE EFFECTS IN
DEVICE DEPLETION REGIONS

2.1 INTRODUCTION.

All silicon devices and integrated circuits contain depletion regions. Thus, it is necessary that radiation effects on such regions be well understood. In bipolar transistors, for example, properties of the emitter-base and base-collector space-charge regions are important contributors to device characteristics such as current gain and leakage current. The dark current in PIN diodes is due to carriers thermally generated in the depleted intrinsic region. In MOS technology, generation centers in depletion regions and at oxide-silicon interfaces also give rise to leakage current. For example, the dark current in charge-coupled devices (CCDs) is due to carrier generation at such sites.

In this section, the effects of radiation-induced displacement damage on device depletion regions are reviewed. Previous work is reinterpreted in some cases, and results of recent analyses are also presented. Emphasis is placed on describing the universal effects on device leakage current produced by bulk generation centers in depletion regions. Interface (or surface) effects are also noted where appropriate. In addition, the effects of *recombination* centers in device space-charge regions are also described.

2.2 TERMINOLOGY.

The material presented in this section is intended to be generic and thus applicable to any silicon device. The nomenclature used is described here to clarify the discussion that follows.

The basic building blocks of bipolar and MOS technologies are pn-junction diodes and MOS capacitors, respectively, which are shown schematically in Figures 2.1 and 2.2. For simplicity, the doping concentrations in the n- and p-type material are assumed equal in Figure 2.1. This results in the metallurgical junction being at the center of the space-charge region. In addition, the minority-carrier diffusion lengths, L_n and L_p,

are also assumed equal. In general, the junction region of width W is called a space-charge region because it contains a spatially fixed charge density due to the presence of ionized donors and acceptors. The variation in space-charge-region width with change in applied bias is shown schematically in Figure 2.1. The depletion approximation for pn junctions assumes that the space-charge region is depleted of free carriers. Thus, the term *depletion region* arises. Under reverse-bias conditions, the space-charge region is essentially free of carriers. Under forward bias, free carriers are injected into this region. It is common practice to refer to the space-charge region under all bias conditions as the depletion region (or layer), and we do so here.
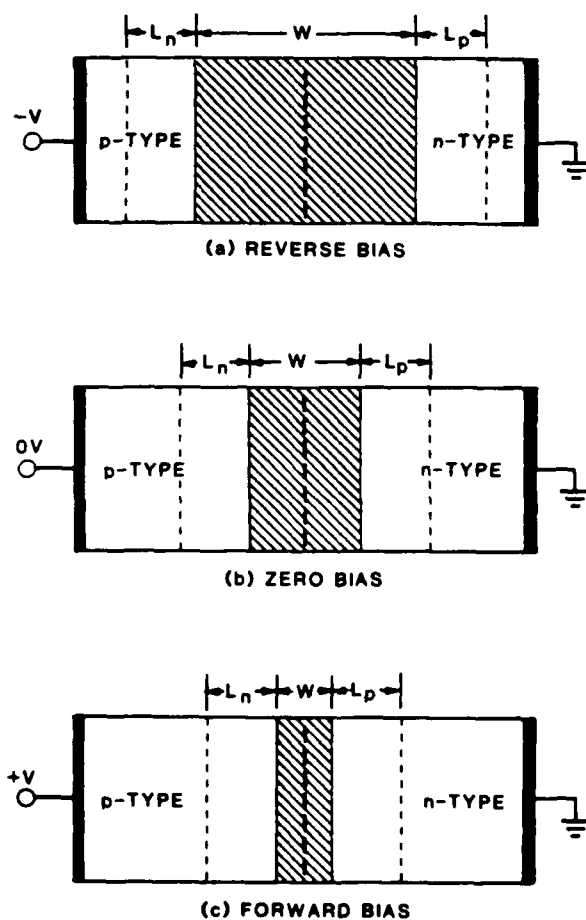
Figure 2.1. Schematic illustration of a pn-junction diode under reverse-, zero-, and forward-bias conditions.

V_g

METAL

SiO_2

s_0 s s_0

$\tau_g \cdot \tau_s$

DEPLETION
REGION τ_r n-Si
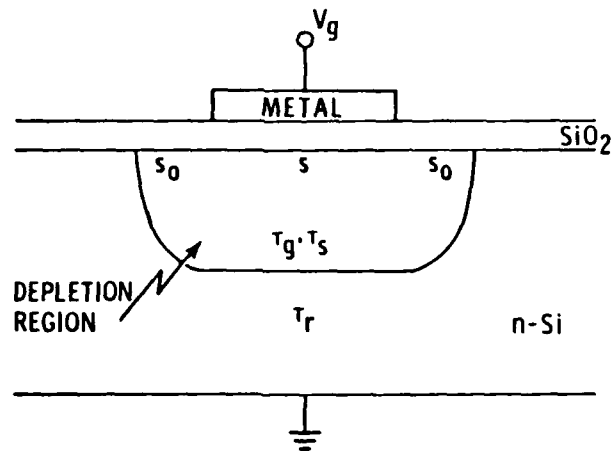
Figure 2.2. Schematic illustration of an MOS capacitor on n-type silicon
with an applied bias V_g more negative than the flatband volt-
age. The laterally depleted region is illustrated. This region is
characterized by s_0 which is the maximum value of the surface
generation velocity s. In the depletion region, the other impor-
tant parameters are the generation lifetime τ_g and the storage
time τ_s. In the neutral bulk, recombination lifetime τ_r is the
parameter of interest.

In general, thermal generation of carriers and carrier recombination occur in all
regions of a semiconductor. The effectiveness of these processes depends on several
variables, including temperature, carrier concentration, generation and recombination
center concentrations, and capture cross sections. For example, the generation process
dominates in a depletion region under reverse-bias conditions. The generation lifetime,
τ_g, is a characteristic time associated with the thermal generation process. As another
example, recombination dominates in neutral regions of a device. The recombination
lifetime, τ_r, is the mean time between recombination events. The MOS capacitor in
Figure 2.2 shows τ_g as the important parameter in the depletion region. (Storage time,
τ_s, and surface generation velocity, s, are also important, as noted below.) In the
neutral bulk, τ_r is the parameter of interest. The generation and recombination lifetime
concepts have been discussed by Schroder.[1]

2.3 CARRIER GENERATION IN DEVICES.

In general, thermal generation of carriers in all regions of a semiconductor device contributes to leakage current. The first quantitative description of the effects of carrier generation on device properties was given by Sah, Noyce, and Shockley.[2] They focused on effects of importance to pn-junction diodes and bipolar transistors; the same concepts can also be applied to describe phenomena occurring in MOS devices.[3] (For detailed discussions of the effects of generation and recombination on device properties, the interested reader is referred to standard device physics textbooks.)

Referring to the reverse-bias case in Figure 2.1, the current that flows under such conditions is usually described as having two components: 1) a *generation* current component due to carriers thermally generated in, and subsequently swept out of, the depletion region; 2) a *diffusion* current component due to carriers generated in the neutral bulk region within a diffusion length of the depletion region edge. For the latter component, minority carriers diffuse to the depletion region where they are swept across, thereby contributing to current flow in the external circuit. For silicon devices at room temperature, leakage current in pn junctions is dominated by the generation current and that component is emphasized in this review. A brief discussion of the relative importance of the two components is given here.

Moll[4] has given an excellent qualitative description of the relative importance of the diffusion and generation components of the reverse leakage current in a pn-junction diode. The thermal generation rate within a diffusion length of the depletion region edge is proportional to the minority-carrier density, which is quite low. As discussed in Section 2.4, the generation rate in the depletion region is proportional to n_i, which is orders-of-magnitude larger than the minority-carrier concentration in the neutral bulk. Thus, for silicon devices at room temperature, generation current dominates. The diffusion current is proportional to $n_i{}^2$ whereas generation current is proportional to n_i. Analytical and experimental consideration of the temperature dependence of the reverse current has shown[5] that the diffusion current becomes important for Si devices at temperatures $\gtrsim 100°C$. The transition temperature for dominance by diffusion depends on bandgap energy which reflects the dependence of n_i on bandgap. For Ge devices,

the transition occurs below room temperature. In the case of GaAs, the transition temperature is considerably higher than that for Si.[5]

Now consider carrier generation in the silicon MOS capacitor shown in Figure 2.2. The important parameters associated with the generation process are surface generation velocity, generation lifetime, and storage time. Recombination lifetime is important for neutral bulk properties, as noted above. Storage time is defined as the time required for an inversion layer to be established in an MOS capacitor driven into deep depletion. This quantity is readily obtained from measurements of capacitance versus time (C-t) following application of a voltage step which drives a device into a deeply-depleted state. Establishment of an inversion layer in such a transient measurement occurs via thermal generation of carriers in the space-charge region and at the interface. In an unirradiated silicon MOS capacitor at room temperature, τ_r and τ_g are typically on the order of microseconds whereas τ_s is on the order of seconds to minutes. Figure 2.3 shows a schematic illustration of a C-t measurement for the case in which an MOS capacitor is driven from inversion to deeper inversion.

Generation lifetime is of fundamental importance because it provides a direct measure of properties of bulk generation centers, and thereby provides information regarding radiation-induced dark current increases. To obtain τ_g, a typical approach has been to make a C-t measurement and interpret the results using Zerbst analysis.[6,7] In principle, this analysis yields the generation lifetime and the surface generation velocity at the SiO_2-Si interface. In practice, there are potential problems with Zerbst analysis. An important issue is the proper separation of surface and bulk generation processes. Schroder and Nathanson[7] pointed out that for an MOS capacitor biased into depletion there exists a laterally depleted region in addition to that directly under the gate electrode, as shown in Figure 2.2. Effects associated with the laterally depleted region have been discussed by Pierret and Small.[8] Surface generation velocity s (and surface recombination velocity) is a function of surface potential.[9] The maximum value of s, denoted as s_0, will occur when a surface is depleted. The value of s in either accumulation or inversion will be significantly less than s_0. During a C-t measurement in which a device is driven from accumulation into deep depletion, the surface generation velocity under the gate electrode after pulsing should initially equal s_0 but will then decrease as
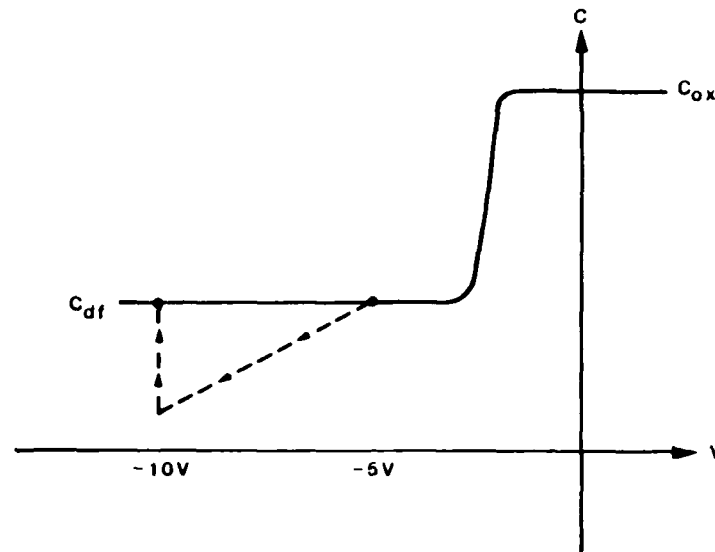
Figure 2.3. Schematic illustration of a capacitance vs. time measurement. For the case illustrated, a voltage step is applied which drives the MOS capacitor from inversion (at -5 V) into deep depletion (at -10 V). The capacitance then recovers slowly to its final value, C_{df}, as the inversion layer is re-established through the thermal generation process.

a function of time as the inversion layer forms. This layer does not form in the laterally depleted region, however. Thus, the situation shown in Figure 2.2 exists in which the lateral region is characterized by s_0 and the gate region is characterized by s.

In a C-t measurement, carrier generation at interface states under the gate electrode can be made negligible compared to other generation components by pulsing a device from inversion to stronger inversion instead of pulsing from accumulation to inversion.[8] In this situation, one obtains an *effective* generation lifetime from analysis of C-t data since generation at the laterally depleted surface can still be important. The effect of the lateral component diminishes as the size of an MOS capacitor increases. Devices can be employed that are large enough such that generation in the lateral region is unimportant. In this manner, generation lifetime associated purely with the depletion-region bulk can be obtained.

Zerbst analysis involves obtaining C-t data and then determining the quantities

$$-\frac{d}{dt}\left(\frac{1}{C}^2\right) \quad \text{and} \quad \left(\frac{1}{C}-\frac{1}{C_{df}}\right) \quad ,$$

where C_{df} is the inversion capacitance. Figure 2.4 shows an example Zerbst plot for an unirradiated device.[10] The slope of the straight-line fit shown yields τ_g and the y-intercept yields s. Note that although generation at the Si-SiO$_2$ interface was suppressed in this example by driving the device from inversion to stronger inversion in the C-t measurement, a finite, but quite small, value for s is still obtained.
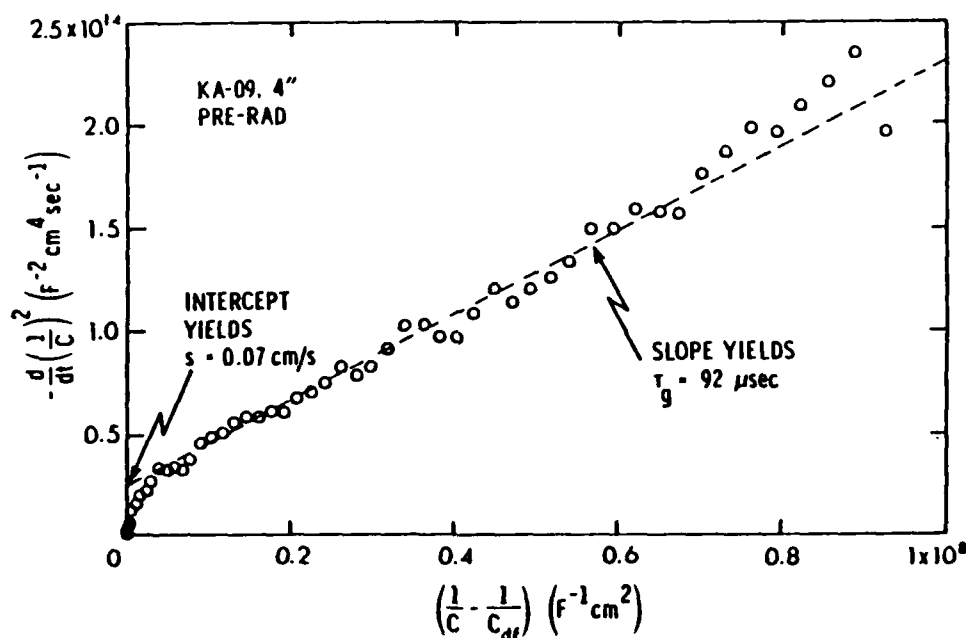
Figure 2.4. Zerbst plot for an unirradiated MOS capacitor.[10] Values for generation lifetime and surface generation velocity are shown.

2.4 RADIATION-INDUCED CHANGES IN DARK CURRENT.

Section 2.3 gave a general description of carrier generation processes in devices and noted that generation at interfaces can be important. However, in many situations generation in the depletion region bulk will dominate, particularly for the case of irradiated silicon devices at room temperature following introduction of generation centers by displacement damage. The present section focuses on this important case of radiation-induced dark current produced by bulk centers.

The thermal generation rate G in a depletion region is given by

$$G = -n_i/\tau_g \quad , \tag{2.1}$$

where n_i is the intrinsic carrier concentration. The thermal generation (or dark) current density J_d due to a depletion region of width W is given by

$$J_d = \int_0^W q|G|dx \cong q|G|W = qn_iW/\tau_g \quad , \tag{2.2}$$

where q is the electronic charge. (The approximation is due to the assumption of a uniform generation rate over the entire depleted region.)

Radiation-induced displacement damage introduces generation centers in depletion regions which degrade τ_g and thereby enhance the thermal generation rate. This degradation process can be expressed as

$$(1/\tau_g) = (1/\tau_{go}) + (\phi/K_g) \quad , \tag{2.3}$$

where τ_{go} and τ_g are the pre- and post-irradiation values of generation lifetime, respectively, ϕ is the bombarding particle fluence, and K_g is generation-lifetime damage coefficient. Substituting Eq. (2.3) into Eq. (2.2), we obtain

$$J_d = qn_iW[(1/\tau_{go}) + (\phi/K_g)] = J_{do} + qn_iW\phi/K_g \quad , \tag{2.4}$$

where J_{do} is the pre-irradiation value of dark current density. Thus, the radiation-induced change in dark current density is given by

$$\Delta J_d = J_d - J_{do} = qn_iW\phi/K_g \tag{2.5}$$

If K_g is known for a given particle type and particle energy, then Eq. (2.5) can be used to calculate the radiation-induced dark current density at any fluence of interest.

Consider neutron bombardment of silicon devices as an important example. Values for K_g have been determined by various workers, or can be derived from their data.

Table 2.1 lists these values for the cases of fission (reactor) neutrons and 14-MeV neutrons. The important note to the table mentions that all K_g values listed are based on the generation rate given by Eq. (2.1). (Schroder[1] has discussed the confusion of some workers, including the present authors, concerning the correct expression for G.) For fission neutrons, the average K_g value for measurements on bipolar devices is 3.8 $\times$ 10^7 n-sec/cm^2, whereas measurements by Srour et al.[10] on MOS capacitors yielded a value a factor of 2.7 lower (i.e., more damage in the MOS case). The reason for this discrepancy is not clear at present, although transient annealing [11,12] is one possibility. The K_g value obtained using MOS capacitors was measured after two hours at room temperature following irradiation.[10] Dark current reduction by about a factor of two has been observed over the interval from two hours to about two weeks after neutron bombardment,[13] which is in the proper direction to account for the discrepancy noted for the data in Table 2.1. The same discrepancy is evident for the 14-MeV neutron data, where the average K_g value for bipolar devices is 2.6 times larger than that for MOS devices.

Two examples are now given to illustrate the applicability of calculating neutron-induced changes in dark current density using Eq. (2.5). Figure 2.5 shows the increase in dark current density produced by fission neutron bombardment of a buried-channel charge- coupled device.[11] Results of calculations using Eq. (2.5) are also shown, and agreement with experiment is quite good. To perform these calculations, the MOS-derived K_g value[10] of 1.4 $\times$ 10^7 n-sec/cm^2 was employed.

Figure 2.6 compares dark current measurements on PIN diodes[21] with calculations made using the same damage coefficient value. Agreement is excellent at the lowest fluence, with a trend toward increasing disagreement at higher fluences. If the average bipolar-derived K_g value is used (from Table 2.1), good agreement is obtained at the two highest fluences.

The above comparisons indicate that more work is needed to resolve the "MOS-vs-bipolar" discrepancy and thereby improve the modeling and subsequent calculations of neutron-induced dark current. However, the present state of knowledge is sufficient to permit reasonably accurate dark current predictions for any neutron-irradiated silicon

Table 2.1. Values for generation lifetime damage coefficient obtained from measurements performed on neutron-irradiated silicon devices by various investigators.

Investigators	Radiation	K_g (n-sec/cm²)	Devices
Fitzgerald and Snow[14]	Fission Neutrons	4.0×10^7	p^+n gate-controlled diodes
Larin[15]	Fission Neutrons	4.5×10^7	npn mesa transistors
Kawamoto and Oldham[16]	Fission Neutrons	4.0×10^7	p^+n gate-controlled diodes
Gregory and Gwyn[17]	Fission Neutrons	2.6×10^7 3.7×10^7	2N5004 (npn planar) 2N5005 (pnp planar)
Srour et al.[10]	Fission Neutrons	1.4×10^7 (a)	MOS capacitors
Kern and McKenzie[18]	14.8-MeV Neutrons	1.7×10^7	JFETs (2N4416)
Holmes et al.[19]	14-MeV Neutrons	1.5×10^7 (a)	pn-junction diodes (vidicon)
Srour et al.[20]	14-MeV Neutrons	6.2×10^6 (a)	MOS capacitors

a. The referenced authors assumed $G = -n_i/2\tau_g$. The K_g value given here is a factor of two larger than the value they obtained. This correction was applied so that all damage coefficients in this table can be compared directly; i.e., all were determined using $G = -n_i/\tau_g$, which is the proper approach.
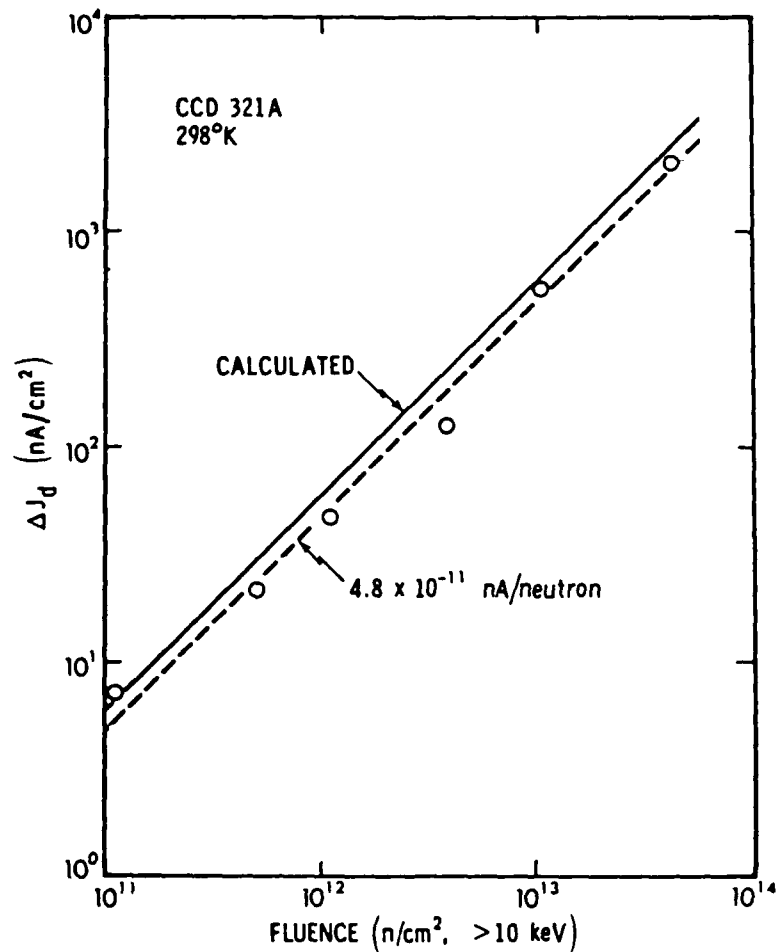
Figure 2.5. Change in dark current density for a neutron-irradiated charge-coupled device. Results of model calculations are also shown. A generation-lifetime damage coefficient of 1.4×10^7 n-sec/cm^2 was used to perform these calculations.

device. If the mean K_g value for bipolar devices in Table 2.1 is averaged with the MOS value, the following results are obtained:

$$\bar{K}_g \text{ (fission)} = 2.6 \times 10^7 \text{ n-sec/cm}^2$$

and

$$\bar{K}_g \text{ (14-MeV)} = 1.1 \times 10^7 \text{ n-sec/cm}^2.$$

2–11
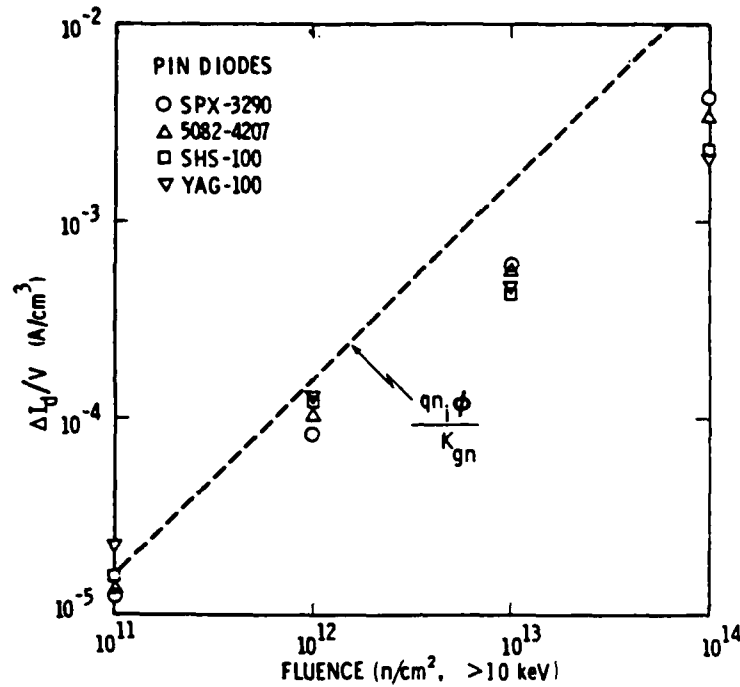
Figure 2.6. Neutron-induced change in dark current per unit volume for various PIN photodiodes. Data points were derived from the work of Kalma and Hardwick.[21] The dashed line is the calculated result based on $K_g = 1.4 \times 10^7$ n-sec/cm^2.

These mean damage coefficients are accurate to within $\pm 50\%$. Combining these values with Eq. (2.5) yields the following relations for the mean neutron-induced dark current per unit volume $(\Delta \bar{I}_{dv})$ due to generation centers in silicon depletion regions:

$$\Delta \bar{I}_{dv} \text{ (fission)} = 9 \times 10^{-17} \phi \text{ A/cm}^3 \tag{2.6}$$

and

$$\Delta \bar{I}_{dv} \text{ (14-MeV)} = 2 \times 10^{-16} \phi \text{ A/cm}^3. \tag{2.7}$$

Figure 2.7 shows plots of these equations as a function of fluence.

The use of Eqs. (2.6) and (2.7) in practice is straightforward. Depletion region dimensions for the device or circuit of interest are needed first. Then neutron-induced

2-12
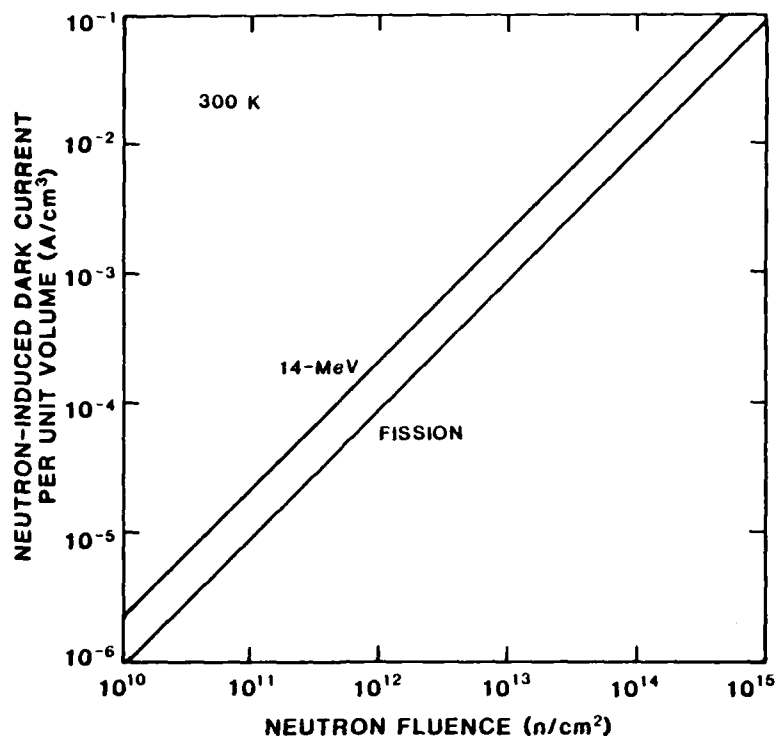
Figure 2.7. Neutron-induced dark current per unit depletion region volume
for silicon devices versus neutron fluence. Calculated curves are
shown for fission and 14-MeV neutron bombardment.

dark current (ΔI_d) at a given fluence can be calculated readily. Figure 2.8 shows calcu-
lated values of ΔI_d as a function of depletion region volume for various fission neutron
fluences. As an example, if the dimensions of the depleted region in a PIN diode are
0.3 cm $\times$ 0.3 cm $\times$ 100 μm, the neutron-induced dark current after 10^{13} n/cm^2 is 0.8
μA (or a dark current density of 9 μA/cm^2). As another example, if the base-collecter
depletion region dimensions in a VLSI bipolar transistor are 1 μm $\times$ 1 μm $\times$ 0.2 μm,
we obtain $\Delta I_d = 0.18$ fA and $\Delta J_d = 18$ nA/cm^2 at the same fluence.

In the above example, neutron effects on dark current in silicon devices were
considered. The same concepts and approach are applicable for any bombarding particle
that produces displacement damage in depletion regions. It is necessary to know the
value of generation-lifetime damage coefficient for the particle and energy of interest.
Using the generation rate definition given in Eq. (2.1), the following values of K_g are
appropriate for proton-irradiated silicon:[22] 2.2 $\times$ 10^7 p-sec/cm^2 at 99 MeV and 2.4 $\times$ 10^7
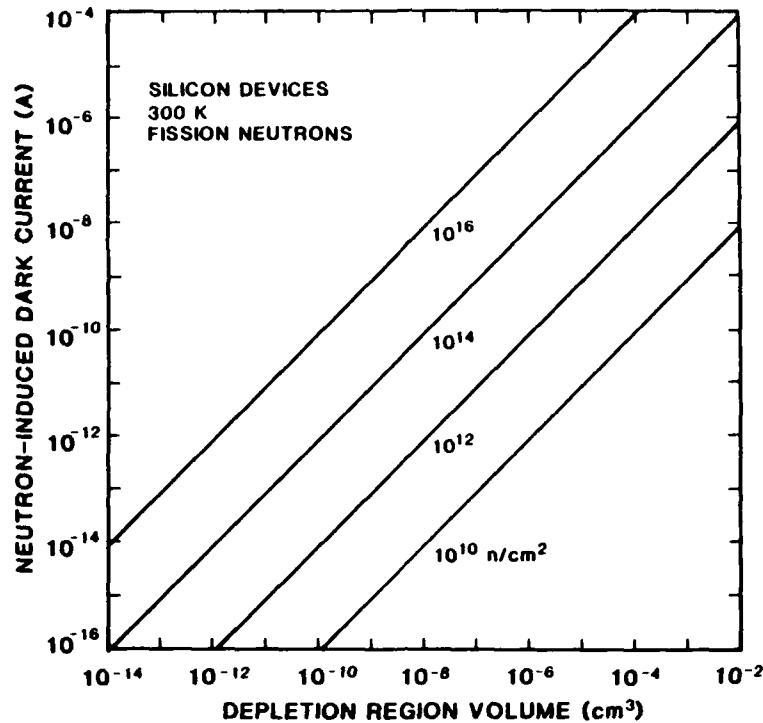
Figure 2.8. Neutron-induced dark current versus depletion region volume
with fission neutron fluence as a parameter. The calculated
results shown here apply for silicon devices at 300 K.

p-sec/cm^2 at 147 MeV. These coefficients are close in value to the mean value for fission
neutron bombardment given above. Thus, Eq. (2.6) also gives reasonably accurate
values of $\Delta \bar{I}_{dv}$ for proton bombardment for energies in the 100- to 150-MeV range.
Evidently the effectiveness of depletion region damage produced by such particles is
comparable to that produced by fission neutron bombardment.

The issue arises regarding how radiation-induced changes in dark current can be
reduced or avoided. One straightforward approach in principle is to reduce the device
operating temperature. (In practice, device functionality at reduced temperatures and
other constraints imposed by the specific electronic subsystem need to be considered.)
Consider the example of a neutron-irradiated silicon charge-coupled device. At room
temperature, the post-irradiation dark current is due to neutron-induced generation
centers in depletion regions in a CCD, as illustrated by Figure 2.5. Referring to Eq.
(2.5), the temperature dependence of neutron-induced dark current is dominated by

that of n_i since K_g is only weakly dependent on temperature.[10] The dramatic reduction in dark current that can be achieved by lowering the operating temperature is due to the strong temperature dependence of the carrier generation rate (proportional to n_i). Detailed consideration of the temperature dependence of J_d for a fission-neutron-irradiated CCD[10] allows the information displayed in Figure 2.9 to be determined. This graph illustrates the effectiveness of lowering the operating temperature of a CCD to avoid neutron-induced dark current problems. As an example, assume that the maximum post-irradiation normalized dark current density that can be tolerated is unity, which is the value of J_{do} at 303 K in Figure 2.9. If the expected fluence is 10^{13} n/cm^2, then this figure indicates that operating the device at $T \leq 269$ K will keep $J_d \leq$ unity following irradiation. Thus, a relatively moderate lowering of the operating temperature will result in substantial radiation tolerance in terms of neutron-induced increases in dark current. This conclusion applies for *any* silicon device in which the leakage current increase produced by bombardment with *any* particle is attributable to radiation-induced generation centers in device depletion regions.

2.5 SINGLE PARTICLE EFFECTS.

The discussion and analyses given in Section 2.4 apply for the case of a relatively high particle fluence, i.e., a fluence large enough to produce many primary interactions between incident particles and Si atoms in a specific depletion region. If the particle fluence is reduced so that only one primary interaction is expected, the issue arises regarding how large the increase in dark current would be. (Note that one *primary* interaction can produce many individual defects, particularly in the case of fast neutron bombardment.) This issue has been explored experimentally for incident 14-MeV neutrons[13] and 99- and 147-MeV protons[22] using a charge-coupled device as a test vehicle. Key findings of those studies are reviewed here. (See Appendices B and F of this report for a detailed description.)

Using the generation rate definition given by Eq. (2.1), the average increase in dark current density produced by a single particle interaction in a device depletion region can be expressed as [22,23]
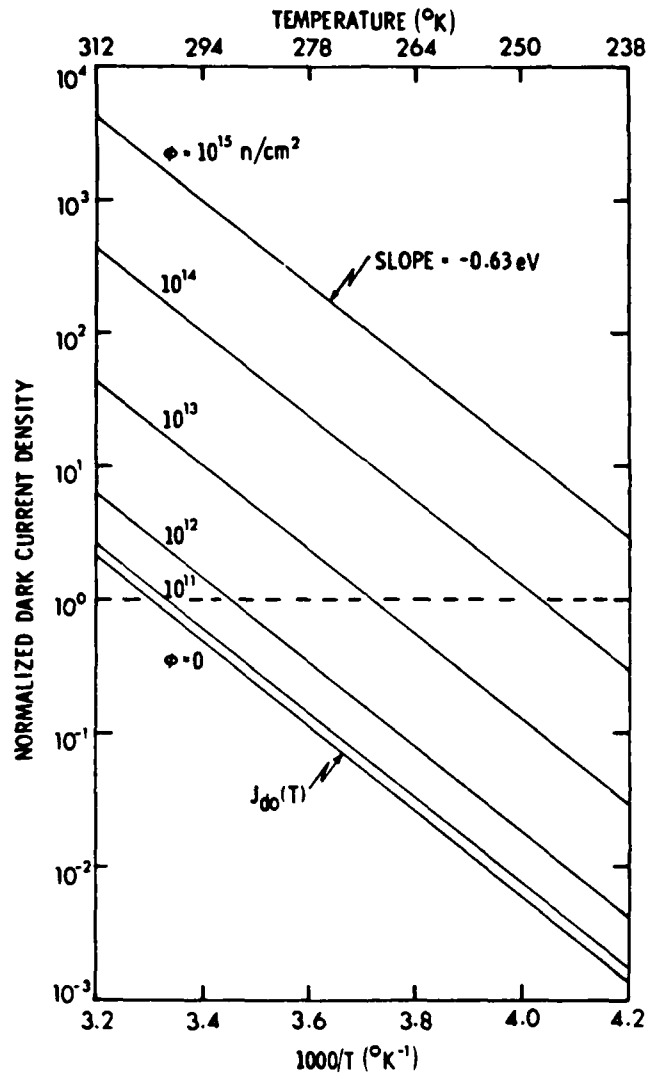
Figure 2.9. Normalized dark current density vs. reciprocal temperature
with neutron fluence as a parameter. The effect of a reduced
operating temperature on radiation tolerance is illustrated.[10]

$$\Delta \bar{J}_{d1} = qn_i / A K_g \, \bar{N} \, \sigma_t \qquad (2.8)$$

In this equation, A is the depletion region area, $\bar{N}$ is the atomic density (5 ×
10^{22} cm^{-3} for Si), and σ_t is the total interaction cross section. (Note that the right-
hand side of Eq. (2.8) differs by a factor of 2 from that in Refs. 22 and 23 because,
in the present work, the thermal generation rate definition given by Eq. (2.1) is being
utilized). Equation (2.8) yields an *average* increase in dark current density because the

2–16

damage coefficient, K_g, is only applicable for the case of many interactions in a given depletion region. Incident particles, such as 14-MeV neutrons, will produce primary knock-on atoms having a spectrum of energies.[23] A single-particle interaction will produce a knock-on with some specific energy within that spectrum. The damage coefficient is a measure of the effects of a primary recoil having the mean energy for a particular recoil spectrum.

Charge-coupled devices were used as test vehicles in the single-particle displacement damage experiments.[13,22] The Texas Instruments TC104 3456-element linear image sensor was employed. Figure 4 in Appendix B shows the change in dark current density measured following 14-MeV neutron bombardment. After a fluence of 1×10^7 n/cm^2, two cells exhibited an increase, as shown in the upper part of the figure. At that fluence, only two to three primary interactions were expected in the CCD depletion regions, which agrees with the measurements. Thus, the effects produced by single neutron interactions were observed. The lower portion of the figure shows that nine newly damaged cells were observed after 3×10^7 n/cm^2.

Figure 5 in Appendix B shows the distribution of damage events measured after 1×10^{10} n/cm^2. Note the relatively long tail to the distribution consisting of large-amplitude events. The number of damaged CCD cells contributing to the distribution shown in that figure is 1389. Multiple interactions occurred in some cells, and the Poisson distribution can be used to determine the total number of primary interactions.[13,22] The result is 1776 interactions. Using the mean measured value of ΔJ_d, we obtain an experimental value for the average change in dark current density per primary interaction ($\Delta \bar{J}_{d1}$) of 1.2 nA/cm^2. Equation (2.8) yields a calculated value for $\Delta \bar{J}_{d1}$ of 1.3 nA/cm^2 by using the mean K_g value of 1.1×10^7 n-sec/cm^2 given in Section 2.4. The very good agreement between measurements and calculations indicates that this mean damage coefficient value is quite appropriate for determining the effects of 14-MeV neutron bombardment. This agreement also suggests that measurement of $\Delta \bar{J}_{d1}$ for a given particle type and energy is an accurate method for determining K_g through use of Eq. (2.8). This approach was followed for proton-irradiated CCDs.

Figure 4 in Appendix F shows the measured change in dark current density for CCDs irradiated with 99-MeV protons to three fluences. Individual damage events are

quite evident, and the number of events increases with fluence. Figure 3 in Appendix F shows that the measured number of damaged cells agreed reasonably well with the calculated number for two proton energies. Figure 5 in that appendix shows the measured damage distribution for 99-MeV proton bombardment. This distribution is similar to that obtained for neutron bombardment. The measured mean values of ΔJ_d for 99- and 147-MeV proton irradiation were used to determine K_g, and the resulting values are given in Section 2.4.

For both the neutron and proton single-particle experiments, increases in dark current density by more than two orders of magnitude were observed for individual damaged cells at relatively low fluences. These large events raise the issue of whether such effects present a problem for VLSI/ULSI circuits. This issue is now considered briefly. (See Appendices B and F for further discussion.)

As noted earlier, all silicon integrated circuits contain depletion regions. If a single energetic particle produces displacement damage in that region, the dark (or leakage) current will increase. Decreasing circuit dimensions will increase the dark current *density*. Whether this single-particle effect will present a problem depends on geometry, the type of circuit, specifications, and performance requirements. It is likely that displacement damage effects at relatively low fluences will be a problem for small-geometry charge-integration and charge-transfer devices because proper operation typically requires a low dark current density.

The damaged region produced by a single particle interaction (or several interactions) can be viewed as a steady-state source of thermally generated charge when the damage is present in device depletion regions. This charge generator results in a dc current flow. Whether the total charge generated in a specific time, or the dc current level, presents a problem depends on the type of circuit, its properties, and the application. As an example, damage regions produced by energetic neutrons and protons may cause a problem in 1- and 4-Mbit NMOS DRAMs due to the generation of excess dark charge.[13,22] The worst-case damaged cell in the proton study described above had a proton-induced dark current density of 27.5 nA/cm^2. (Such a situation can occur in a dense array at a relatively low fluence, so we use the largest event as a worst-case example.) The thermally generated charge Q_g generated by that damage in time t (in

seconds) can be expressed as $Q_g = 63t$ femtocoulombs. (This expression is independent of dimensions as long as the damage is completely contained within the depletion region.) Thus, a steady-state current of 63 fA will flow and generate, for example, 6.3 fC in a time of 100 msec. This worst-case calculation can be used to estimate whether a problem will occur in a given situation. The approach outlined here is applicable for assessing the susceptibility of any integrated circuit to the permanent effects of single incident particles. Limits eventually may be placed on circuit dimensions to avoid problems caused by permanent damage at low particle fluences.

2.6 RECOMBINATION IN DEPLETION REGIONS.

When a device space-charge region is fully depleted of free carriers, emission processes dominate and thermal generation at centers near midgap give rise to leakage current. For a forward-biased pn junction, carriers are injected continuously into the space-charge region. Under such conditions, carrier recombination dominates. This is an important process for bipolar transistors. Recombination in the emitter-base depletion region is one of the factors that determines current gain. Recombination centers are introduced in this region by radiation, and these centers contribute to current gain degradation.

Analogous to the reverse-bias situation discussed in Section 2.3, the current in a forward-biased pn junction has two components: a diffusion component and a recombination component.[5] Of interest here is the latter current which is due to recombination in the depletion region. The following approximate expression can be written for the recombination current density under forward bias condition:[5]

$$J_r \cong (qn_iW/\tau_r)\exp(qV/2kT). \qquad (2.9)$$

In this equation, τ_r is the recombination lifetime in the depletion region and V is the applied voltage. (Note the similarity between the prefactor here and the expression for J_d given by Eq. (2.2).) Analogous to Eq. (2.5), we can express the increase in recombination current by bombarding particles that introduce displacement damage as

$$\Delta J_r = (q n_i W \phi / K_r) \exp(q V / 2kT). \tag{2.10}$$

In general, the damage coefficient K_r (and τ_r) will depend on injection level. Gregory and Gwyn[17] have treated the case of neutron effects on space-charge-region recombination in irradiated bipolar transistors. They found that such recombination dominated the radiation response of narrow-base transistors of that era.

As a final note, the dominant current mechanism under forward bias depends on the applied voltage and on temperature.[5] For example, in silicon devices at room temperature J_r will dominate for $V \lesssim 0.4$ volts. At higher voltages, the diffusion current dominates. These dependences provide a method for sorting out the dominant mechanisms in radiation effects studies.

SECTION 3

SINGLE EVENT UPSET STUDIES

3.1 INTRODUCTION.

Several studies of single-event-upset phenomena were performed during this program. Portions of that work were published as technical journal articles, and those papers are presented in Appendices A, C, and H of this report. Additional results are described in this section. Section 3.2 presents results of an investigation performed in collaboration with Harry Diamond Laboratories in which oscillatory phenomena in GaAs devices were examined. Section 3.3 describes results of charge collection measurements performed on Si and GaAs devices fabricated on epitaxial layers. In Section 3.4, a description is given of the system used to perform transient current measurements following a single particle strike.

3.2 INVESTIGATION OF OSCILLATIONS OBSERVED IN CHARGE COLLECTION MEASUREMENTS ON GaAs DEVICES.

Charge collection measurements on GaAs Schottky-barrier diodes performed by R. Gilbert of Harry Diamond Laboratories (HDL) exhibited pronounced oscillations. Those data were presented at the 1985 Single Event Symposium and at the 1985 IEEE Nuclear and Space Radiation Effects Conference.[24] These oscillations were initially attributed to a space-charge instability resulting from the negative-slope portion of the GaAs velocity-field relationship, thereby explaining why oscillations were observed for GaAs and not Si devices. We subsequently investigated this effect and concluded that it is due to reflections of the current pulse in the coaxial cable between the device, the FET probe, and the biasing resistor. That is, the oscillations were due to the test circuit configuration and not to physical mechanisms occurring in the device. The experimental evidence supporting that conclusion is now described.

In August 1985, one of the GaAs diodes that exhibited oscillations at HDL was sent to Northrop Research and Technology Center (NRTC) to confirm and further investigate this phenomenon. This diode was similar in configuration to devices that we

had used for previous experiments.[25,26] Along with the diode, HDL sent diagrams of the experimental set-up and photographs of the oscillations which were measured to occur at a frequency of 520 MHz. Figure 3.1 shows one of the charge collection waveforms obtained by Gilbert for a diode biased at -50 V and struck by a 5-MeV alpha particle.
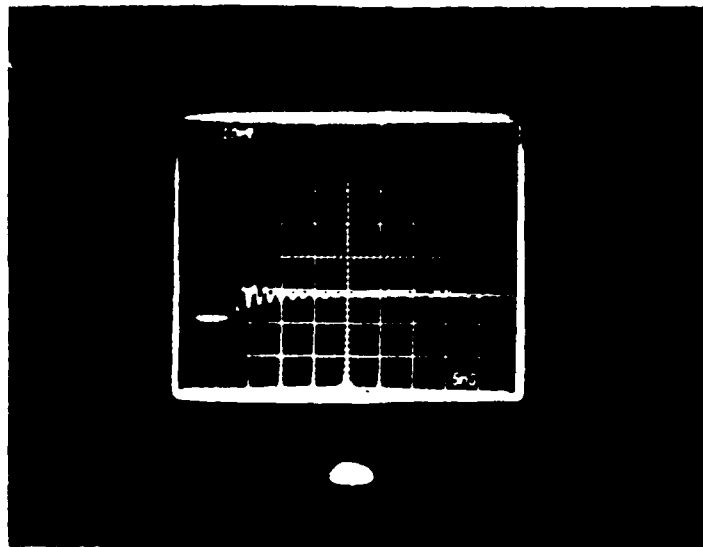
Figure 3.1. Example of charge collection waveform showing oscillations measured at HDL for a GaAs diode biased at -50 V and struck by a 5-MeV alpha particle.

Circuit effects and reflections for both charge collection and current transient measurements were previously investigated at NRTC. As a result, we raised the possibility that the oscillations observed at HDL were not due to device effects but were caused by the test circuit. There are two main differences between our previous charge collection measurements (which did not show any significant oscillations) and the HDL measurements. Although HDL used a similar Au–n-type GaAs Schottky-barrier diode configuration, their diode was much larger - - 1.0 mm as opposed to our 0.25-mm diameter Au dots. This area difference results in an increase in the device capacitance by a factor of 16. The second major difference was the biasing configuration. We had been using series biasing while HDL utilized a parallel set-up, as illustrated in Figure 3.2.

To determine the cause of the oscillations, the HDL diode was first placed in our existing series-bias configuration to see if the larger capacitance was responsible.
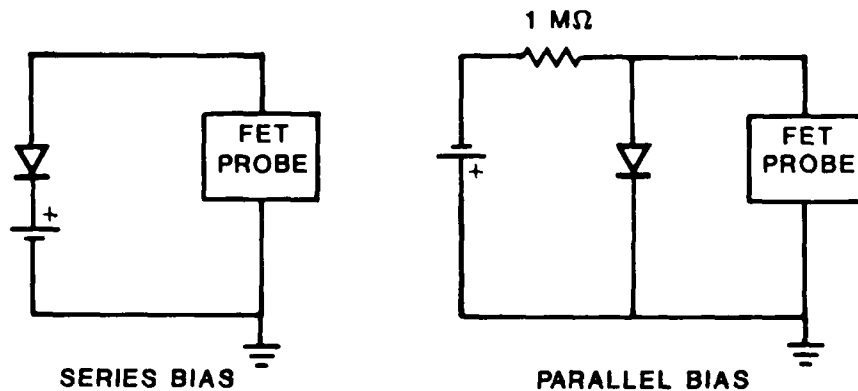
Figure 3.2. Schematic representation of charge collection biasing configu-
rations.

Relatively minor ringing was observed, as shown in Figure 3.3, but this effect was not as large in amplitude as in the HDL data. Since their device did not oscillate in our biasing set-up, we then tried the parallel biasing configuration and very severe oscillations were observed, even larger in amplitude than measured at HDL, as shown in Figure 3.4. These data were obtained using a Tektronix 7912 digitizer and analyzed using an HP 9826 computer. The frequency of these oscillations was only 150 MHz, in contrast to ~500 MHz as observed by HDL, so this led to the speculation that reflections were the cause. When the 1-MΩ isolation resistor was moved from the power supply (40 cm from the device) to a position directly under the TO-5 header, the reflection time became so short that the oscillations were above the bandwidth of our measurement system. A waveform obtained with this configuration is shown in Figure 3.5.

Further testing was performed by moving the isolation resistor back to the power supply and using longer cables and various other diodes, both GaAs and Si. The longer cables resulted in longer reflection times, as shown in Figure 3.6 for the HDL diode with a 320-cm cable. It is interesting to note that the longer cable reduces the signal amplitude and presents the current pulse from being integrated by the FET probe. Both Si and GaAs devices exhibited reflections, although the magnitude varied from device to device. Results for a 50 ohm-cm Si sample that showed oscillations at ~200 MHz are shown in Figure 3.7.
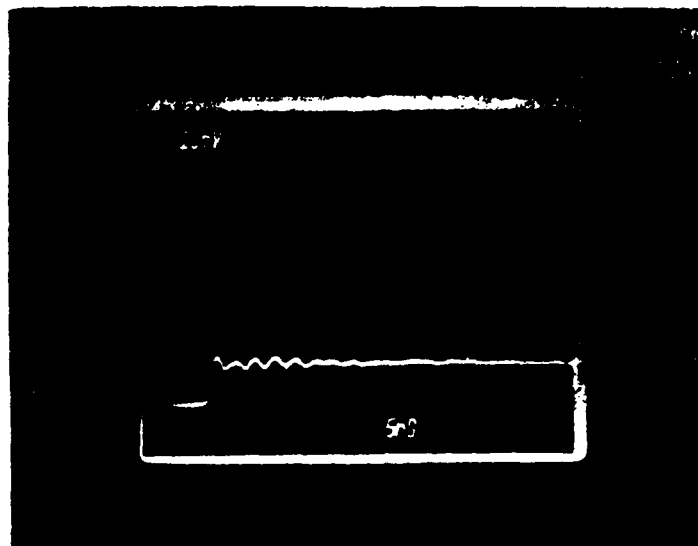
Figure 3.3. Charge collection waveform for a GaAs diode biased at -50 V
using the series configuration.
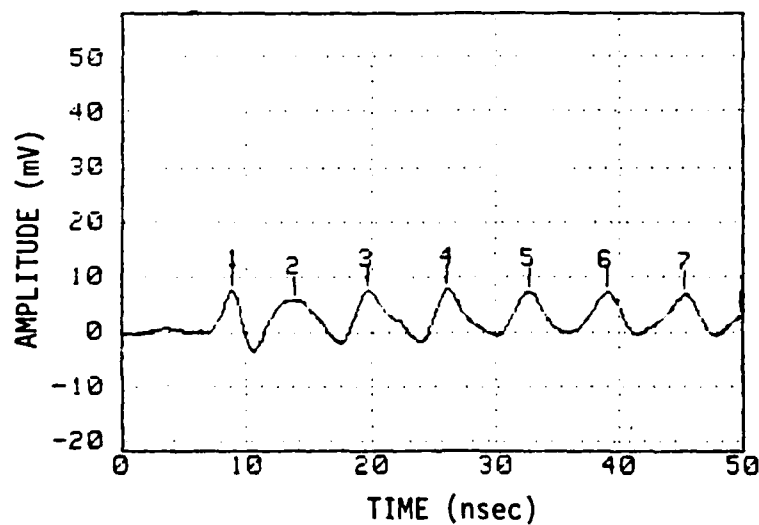
Figure 3.4. Charge collection waveform for a GaAs diode biased at -50V
using the parallel configuration. The distance between the de-
vice and the isolation resistor was 40 cm.

The reflection waveforms observed for a 50-ohm cable placed between the device
and the FET probe (DC input impedance = 100 KΩ) appeared to be similar to those
obtained with a cable between the device and isolation resistor. Figure 3.8 shows the
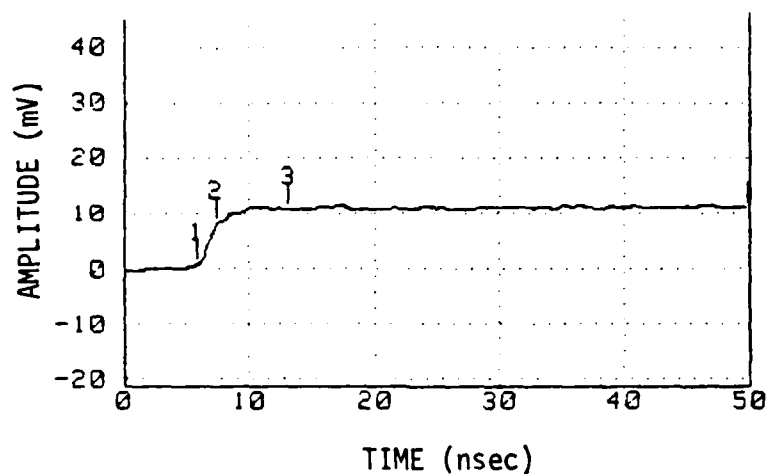
Figure 3.5. Charge collection biasing waveform for a GaAs diode obtained using the parallel configuration. The isolation resistor was mounted directly under the TO-5 header.
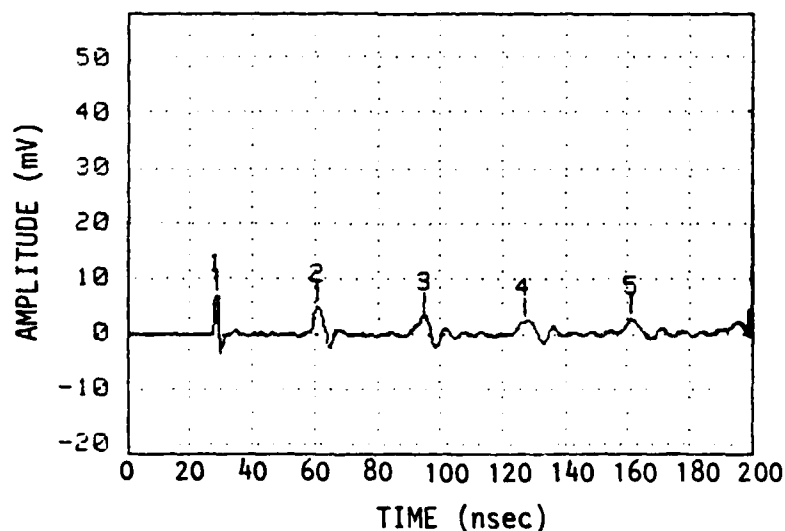
Figure 3.6. Charge collection waveform for a GaAs diode obtained using the parallel biasing configuration. The isolation resistor was ~320 cm from the device.

reflections with a 140-cm cable from the device to the probe and a short cable connecting the device to the resistor. The time between the major peaks is 15 nsec, which corresponds to 148 cm (down and back) at the cable propagation velocity of 0.66c,
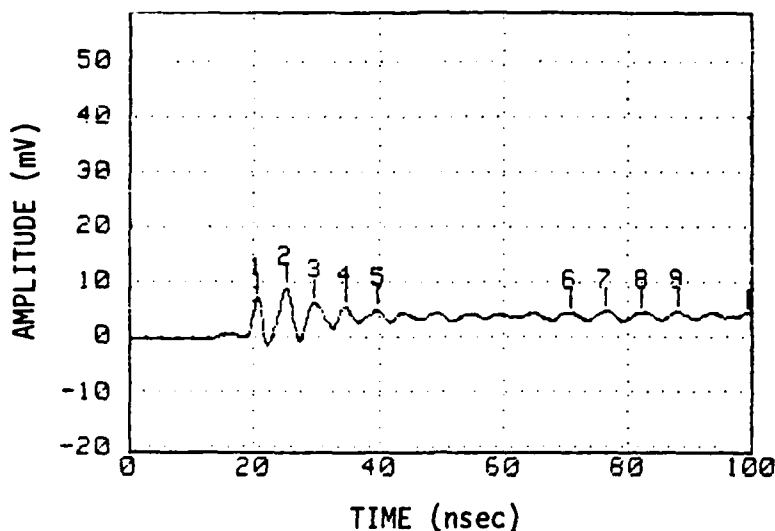
Figure 3.7. Charge collection waveform for a Si diode obtained using the
parallel biasing configuration.

where c is the velocity of light. Figure 3.9 shows the opposite case with the 140-cm
cable placed between the device and the resistor and a short cable connecting the de-
vice to the probe. Once again, the time between major peaks is 15 nsec. The source of
the secondary 3-nsec oscillations was not determined, but does not correspond to the
shorter cable length.

Both the series and parallel biasing methods can be effective if used carefully,
but cable lengths should be kept to a minimum. The distances should be much less
than half as far as a signal would travel in the risetime of the measurement equipment.
This is especially true of the mismatch in the parallel biasing configuration at the
isolation resistor. This resistor is necessary for protecting the instrumentation from
device breakdown and to prevent the power supply from shunting the current pulse.
In the series biasing configuration, the high DC impedance of the probe protects the
device. The power supply, in series with the device and the probe, is a virtual short
to the high-frequency current pulse. (Additional study of circuit effects and reflections
was performed later in this program to insure an undistorted signal for charge collection
experiments and to make possible very-high-bandwidth transient current measurements.

3–6
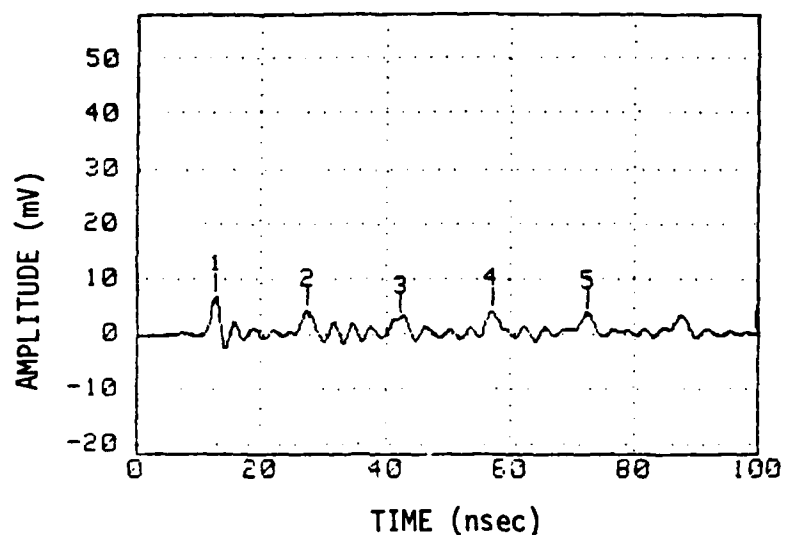
Figure 3.8. Charge collection waveform for a GaAs diode obtained using the parallel biasing configuration. A 140-cm cable connected the device to the FET probe. A short cable connected the device to the isolation resistor.
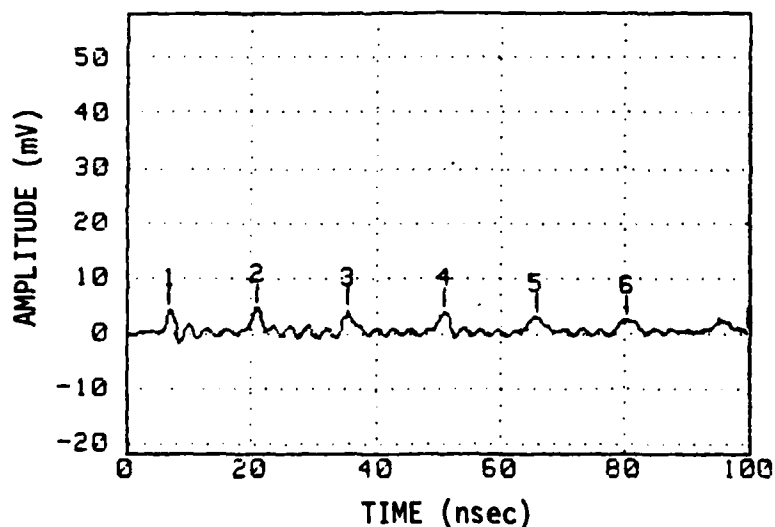
Figure 3.9. Charge collection waveform for a GaAs diode obtained using the parallel biasing configuration. A 140-cm cable connected the device to the isolation resistor, while a short cable connected the device to the FET probe.

Results of such experiments are described in Appendix H. Further description of the transient current measurement system is presented in Section 3.4.)

3.3 CHARGE COLLECTION PHENOMENA IN Si AND GaAs DEVICES FABRICATED ON EPITAXIAL LAYERS.

3.3.1 Introduction and Experimental Information.

The basic mechanisms involved in the charge funneling process in semiconductor devices have been studied extensively at NRTC[25-28] and elsewhere.[29-33] We have extended our investigation of charge collection phenomena in Si devices fabricated on bulk substrates[27] to include devices fabricated on epitaxial layers of various thicknesses. These devices have vertical geometries that are more relevant to integrated circuits. We have also continued our studies of charge collection mechanisms in GaAs devices fabricated on semi-insulating (SI) substrates in order to address several issues which were raised previously.[26] Results are reported in this section.

The set of second-generation devices studied was designed to minimize surface leakage currents as well as to insure a laterally uniform electric field distribution. Each Si n^+p or p^+n diode was fabricated on an epi layer with a doping density of $\sim 10^{15}$ cm^{-3}. The epi-layer thicknesses before processing were 8, 13, and 23 μm for the n^+p devices; the thickness for p^+n devices was 13 μm. The epi layers were grown on substrates with a resistivity of ~ 0.02 Ω-cm in all cases. The basic design features for Si devices are shown in Figure 3.10, where a p^+n device is used as an example. The active area is defined by a circular junction having a diameter of either 100 μm or 250 μm and an Al contact 1 μm in thickness. A 1-μm thermal oxide isolates the Al metallization from the p^+ region except at locations where relatively small contact holes are defined. This design reduces surface leakage currents. In order to obtain high breakdown voltages, junction curvature effects were minimized by utilizing a 3-μm diffusion depth for the p^+ or n^+ top layer. The epi-layer ohmic contact consists of a 1-μm thick and 20-μm wide Al metallization ring surrounding the active area at a separation of 13 μm from the active area. Electrical contact from the ring through the oxide to a 1-μm deep n^+ or p^+ diffusion is made through contact holes. Bonding pads to the ohmic and active

regions complete the device. The capacitance of the active-region bonding pad shunts the junction capacitance and was found to have a value of 0.3 pF.

(a)

(b)
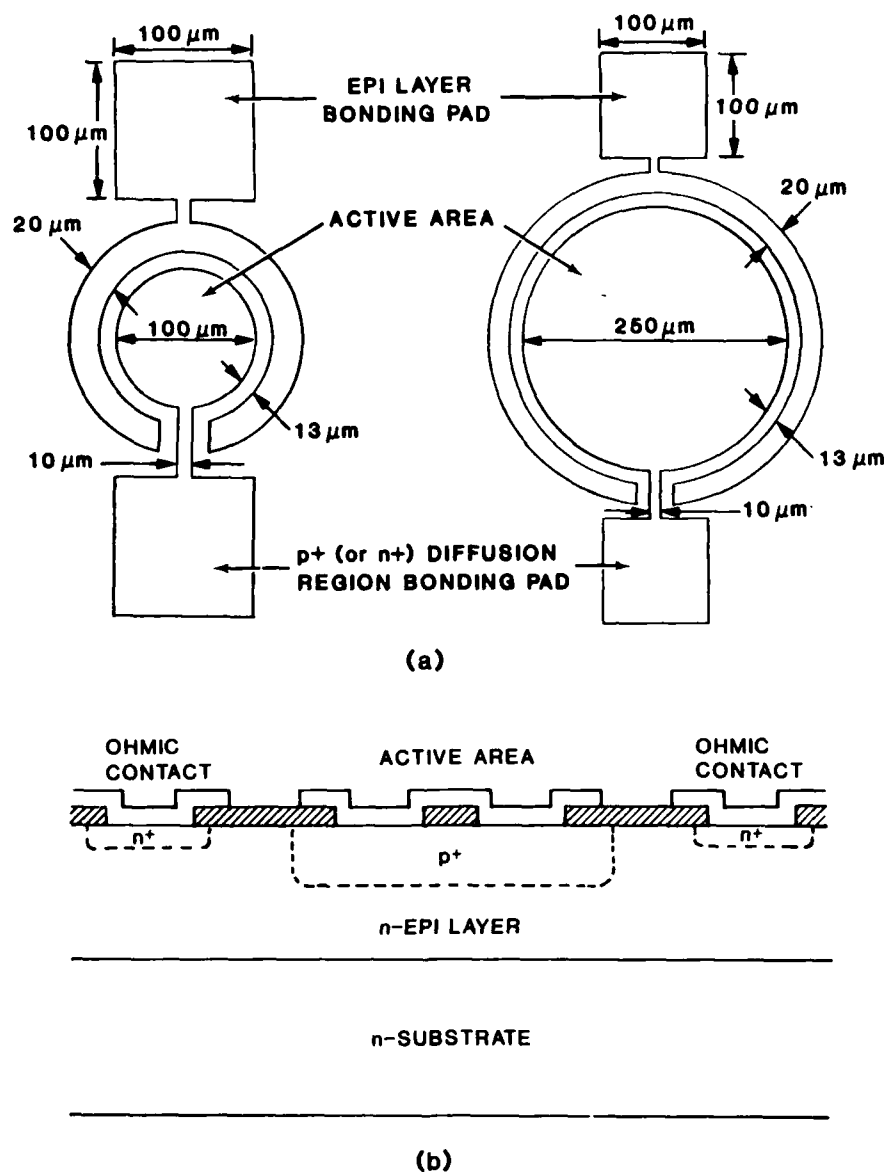
Figure 3.10. Schematic diagram of Si diodes: (a) top view; (b) side view.

GaAs p$^+$n diodes were fabricated on a 10-μm epi layer with a doping concentration of 5×10^{15} cm^{-3} and grown on undoped SI GaAs substrates. Figure 3.11 shows the device configuration. The circular active region of the diode has a mesa structure and is 100 μm or 250 μm in diameter. The p$^+$ layer is formed by a Be implant to a

junction depth of 0.3 μm. The active region is surrounded by a relatively wide Au/Ge metallization ring which serves as the ohmic contact. The ohmic contact was placed close to the junction to minimize the RC risetime associated with the diode.

All test devices were mounted on TO-5 headers using silver paint. Accurate computer-controlled C-V measurements were made by directly probing the devices. All parasitic shunting capacitances such as the capacitance of the active-area contact pad were subtracted from the measured capacitance. The data were then stored and later analyzed by computer to obtain doping profiles as a function of depletion width. From such profiles, the thickness of the epi layer can be determined. Charge collection measurements were performed by applying a reverse bias to the ohmic contact pad utilizing a probe attached to a rigid high-bandwidth coaxial cable. The current pulse generated by a 5.1-MeV alpha particle strike was integrated by the sum of the device junction capacitance and the input capacitance of a Tektronix P6201 FET probe. The rest of the measurement system and the alpha-particle source information are the same as described previously.[25] For measurements of the angular dependence, a test fixture[28] was used which allowed the angle of incidence of the alpha particle to be varied from +90° to −90°, with an uncertainty of ±4°. The charge collection data were analyzed by computer to obtain the prompt and total (i.e., the sum of the prompt and the diffusion) charge, and their standard deviations, from the measured waveforms. To aid in the interpretation of results for various simple device geometries, analysis software was also written to calculate the amount of charge generated by the alpha particles in the depletion and epi-layer regions as the angle of incidence and bias are varied.

3.3.2   Results for Silicon Devices.

The doping profiles for the devices studied were found to be relatively uniform, with a variation of less than 10% over the range of depletion widths examined. The average doping concentration for each device was within 20% of the expected value of 10^{15} cm^{-3}. It is estimated that less than 0.5 μm of the n$^+$ or p$^+$ top layer was depleted when the highest voltage utilized was applied. When the epi layer becomes fully depleted, the depletion region can include the epi-substrate interface region where a sharp increase in the doping profile occurs. For n$^+$p devices with the thickest epi layer, such a condition was not reached. A nominal value of ~19 μm after processing
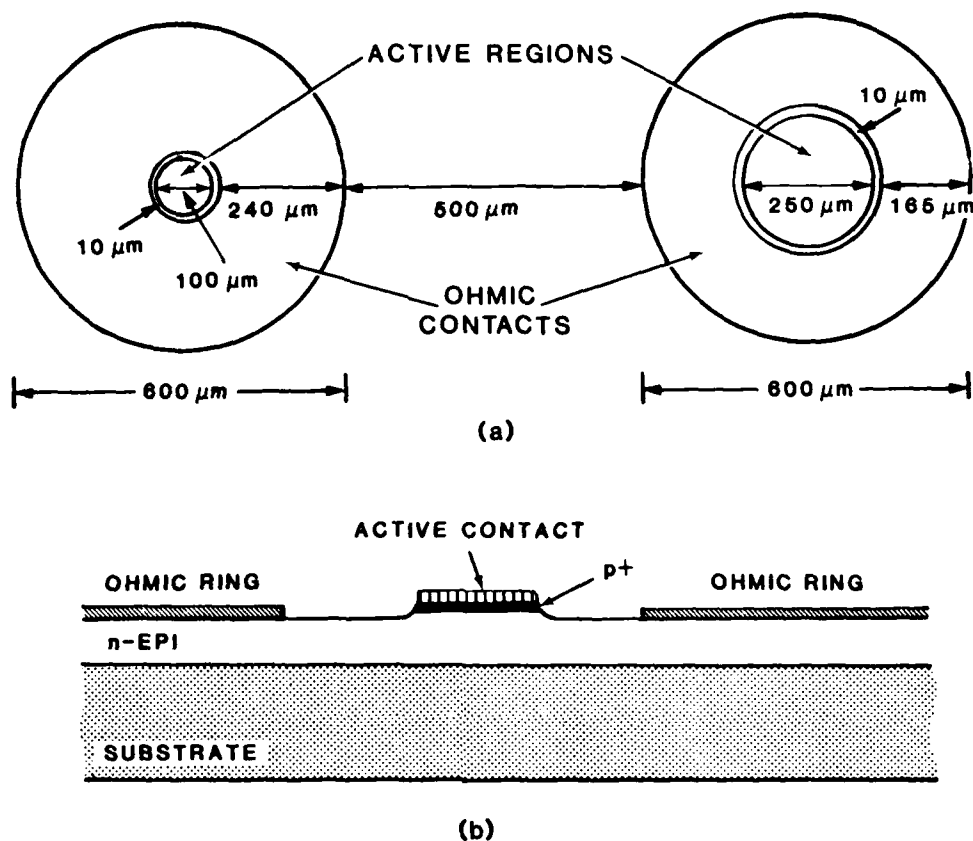
Figure 3.11. Schematic diagram of GaAs diodes: (a) top view; (b) side view.

was assumed for the epi-layer thickness in those devices. For the other n^+p devices, epi-layer thicknesses (i.e., the thickness of the region beneath the n^+ diffusion) were determined to be 2 and 6 μm from the doping profiles. The epi-layer thickness for the p^+n devices was similarly determined to be 7 μm.

Results of charge collection measurements as a function of depletion width are shown in Figures 3.12 and 3.13 in terms of the total and prompt collected charge, respectively. Certain features of the data are evident in Figure 3.12. The total collected charge for the 19-μm device increases gradually and then saturates at a value near 140 fC. The total collected charge for the 6-μm device behaves in a similar manner but saturates at a somewhat lower value of $\sim$115 fC. A more drastic decrease to $\sim$80 fC is observed for the 2-μm device. It is clear from these results that as the epi layer is made thinner, the amount of total charge collected is reduced. Data for a 7-μm p^+n

device are also included in Figure 3.12 for comparison. The total charge is relatively constant at a value of ~130 fC over a reasonably wide depletion width range. This device exhibits behavior similar to that for the n^+p device with the 19-μm epi layer. Information regarding prompt recombination can be deduced from the data in Figure 3.12, and that discussion is deferred until the prompt data are described.
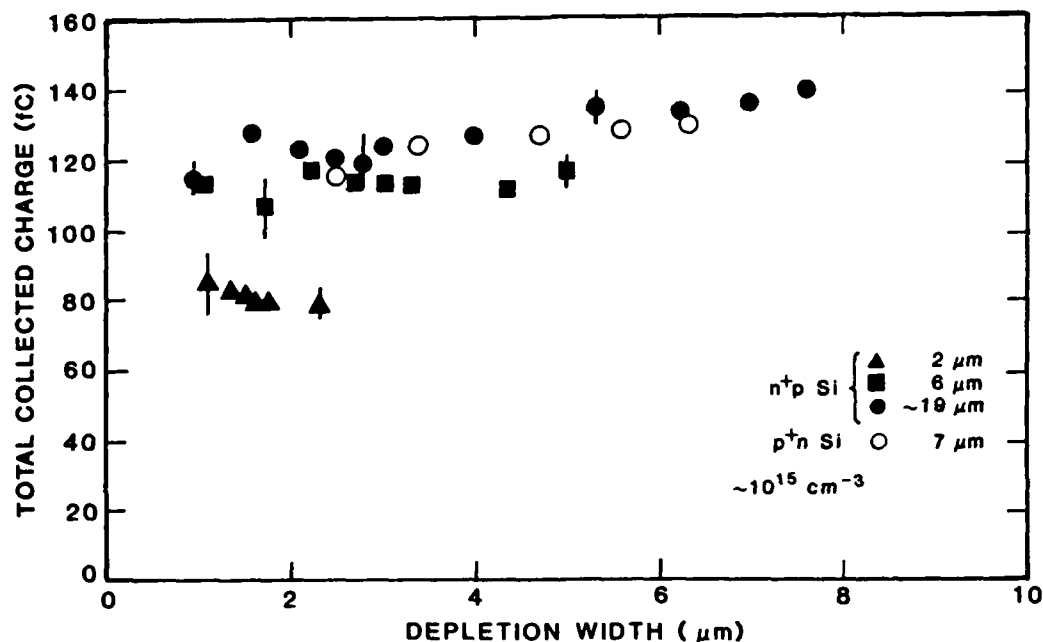
Figure 3.12. Total collected charge as a function of depletion width for Si diodes with various epi layer thicknesses.

The prompt component of collected charge for these same devices is shown in Figure 3.13. Several noteworthy features are evident. First, the amount of prompt charge is observed to be affected by the epi-layer thickness. Data for the 19-μm n^+p device follow typical[29] bulk-like (i.e., non-epi) behavior. The prompt charge increases from a value of 45 fC at a depletion width of 1 μm and saturates at a value of ~130 fC as collection due to funneling extends to the end of the alpha particle track. This occurs at depletion widths above 7.5 μm. For the 6-μm device, the prompt charge initially follows bulk-like behavior as the depletion width is increased. However, at a depletion width of 2.2 μm, the prompt charge saturates at a value of ~80 fC. When the epi-layer thickness is decreased to 2 μm, the amount of prompt charge collected is reduced to 45 fC.

3-12
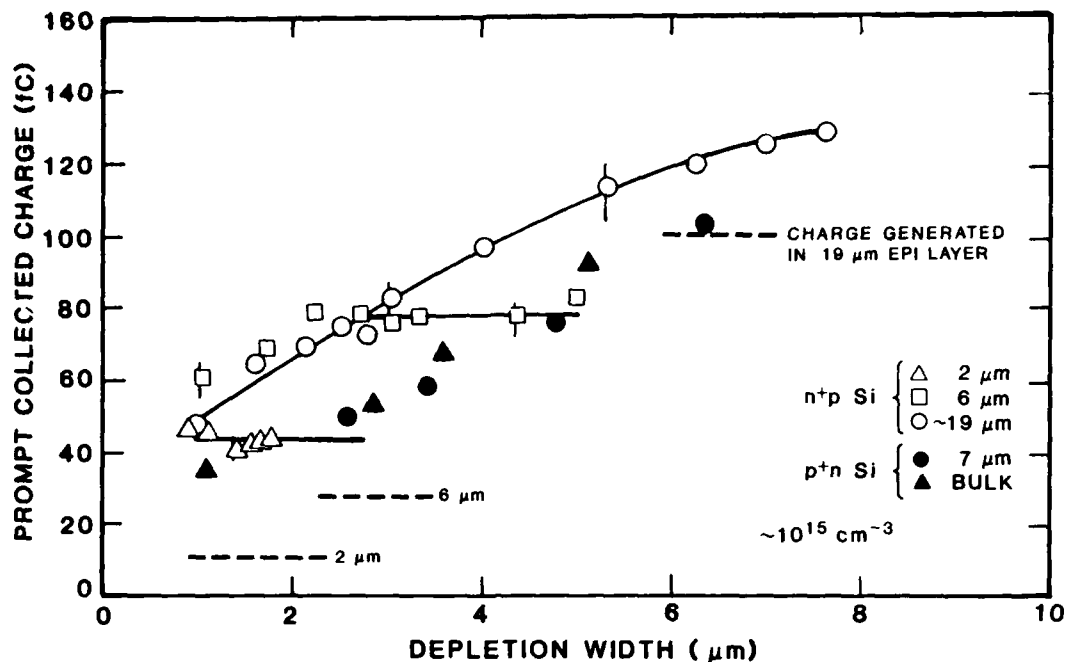
Figure 3.13. Prompt collected charge for Si diodes. The bulk p⁺n data were obtained from Ref. 29 and were normalized in a manner described in the text.

Second, data for the 7-μm p⁺n device show behavior different from that observed for n⁺p devices with a comparable epi-layer thickness. As illustrated in Figure 3.13, the prompt charge increases linearly with depletion width and does not exhibit the saturation that was observed in the n⁺p devices. Both the total and prompt charge for this p⁺n device behave like an n⁺p device with a much larger epi-layer thickness.

In order to investigate the contributions of the n⁺ or p⁺ top layer, the epi layer, and the substrate to the prompt and total collected charge, the amount of charge generated in each layer was calculated. For the 19-μm device, for example, the following values were determined. While passing through the metallization and the oxide regions, the alpha-particle energy decreases from 5.1 MeV to 4.85 MeV. The ionization track extends 24.7 μm into the silicon, with a total of 214 fC of charge generated along its entire length. As the alpha particle penetrates into the silicon, its energy further decreases to 4.4 MeV at the n⁺p junction. This energy loss results in 19 fC generated in the diffused layer. At the epi-substrate interface, the alpha-particle energy becomes

0.62 MeV after producing 168 fC of charge in the epi layer. The remaining energy is lost in the substrate where 27 fC is generated.

Auger recombination[34-36] is believed to be an important recombination mechanism at the high excess charge densities present in the plasma generated by the alpha particle.[26] This mechanism has been used to account partially for a 15% charge loss in GaAs n-type Schottky-barrier diodes[25] and, as discussed in Appendix H, may explain a 40% charge loss observed in Si n-type Schottky diodes. These recombination percentages were determined by measuring the prompt collected charge when an incident alpha particle is stopped completely within the depletion region. For this situation, all charge is collected promptly, with no delayed component being evident. Closer analysis of the present data for the 19-μm device also revealed a charge loss. For these diodes, the depletion width was increased until all charge generated by the incident particle that does not recombine promptly was collected. When this occurs, the prompt and total charge saturate to nearly the same value. This is true for devices with bulk semiconducting substrates or with relatively thick epi layers such as the 19-μm device discussed here. The total collected charge included a relatively small contribution from the diffusion of charge generated in the n^+ top layer. A maximum collected charge of ~140 fC is observed for the 19-μm device when the total and prompt charge saturate. As noted above, the total generated charge, neglecting recombination, is 214 fC. Thus, approximately 35% of the generated charge is not collected.

Consideration of the total collected charge for 2-, 6-, and 19-μm devices (Figure 3.12) along with the knowledge of the charge generated in each device region (i.e., the diffused layer, the epi layer, and the substrate) allows more detailed recombination information to be deduced. Such an analysis of the data indicates that approximately 60% of the charge generated in the substrate recombines promptly and approximately 25% of the charge in the epi layer recombines. Charge loss is most likely due to Auger recombination and can occur through band-to-band or trap-assisted processes.[34,35] The apparently greater amount of carrier recombination in the substrate may be attributed either to the higher excess carrier density or to the relatively high substrate doping density. Both of these conditions result in a higher recombination rate.

For simplicity, we assume here an overall 35% charge loss for all n^+p devices. Under this assumption, the net amount of charge generated in the epi layer is 9 fC for the 2-μm device, 27 fC for the 6-μm device, and 108 fC for the 19-μm device. These values are represented by the dashed lines in Figure 3.13. It is evident that the maximum amount of prompt collected charge is greater than that generated in the epi layer. The contribution from the n^+ top layer to the prompt charge is estimated to be less than 10 fC. The substrate, therefore, must be contributing the additional prompt charge. For the 2-μm device, the substrate supplies charge amounting to an additional effective collection length of 7 μm into the substrate. For the 6-μm device, the additional collection length is 9 μm.

The reason for the bulk-like behavior of the charge collection data for the 7-μm p^+n device is not clear at present. In comparing the present results with data for a device fabricated on a bulk substrate, a large discrepancy was found between p^+n results shown in Figures 3.12 and 3.13 and those reported by McLean and Oldham.[29] This discrepancy can be resolved by noting that a maximum collected charge of $\sim$75 fC can be extrapolated from their data. This suggests a 65% charge loss, while an overall 40% charge loss is calculated from the 7-μm data shown in Figures 3.12 and 3.13. After the data of McLean and Oldham were normalized using this ratio of charge losses, their results were then compared with our findings. As shown in Figure 3.13, the agreement between their data (solid triangles) and the present 7-μm data is very good. Auger recombination most likely plays a role in the 65% charge loss. Using the approach described in Appendix H and assuming a value for the Auger coefficient[36] of 3×10^{-31} cm^6/sec, a 60% charge loss is calculated. This demonstrates the consistency of bulk data with behavior for the 7-μm p^+n epi device.

Finally, as the voltage applied to the 2-μm n^+p device is increased to 80 V, corresponding to a depletion width of 3 μm, the avalanche regime is reached. Because of the large electric field present across the epi layer, avalanche multiplication occurs during the charge collection process, which results in values of the prompt and total collected charge as large as 340 fC and 1200 fC, respectively. No evidence of multiplication was observed in the other devices.

3.3.3 Results for GaAs Devices.

GaAs devices are often fabricated on Cr-doped or undoped SI GaAs substrates for electrical isolation. An important technological question is how these substrates affect the radiation sensitivity of such devices. A previous study[26] focused on single alpha-particle-induced transient upset in GaAs Schottky diodes with Cr-doped SI GaAs substrates. Although we subsequently found that the charge collection waveforms were risetime-limited due to a large series resistance associated with previously used samples, it is clear from the earlier data that there is a significant reduction in the observed charge collection as compared to that for devices fabricated on semiconducting GaAs substrates. This reduction was believed to be the result of a longer time for funnel formation in the semi-insulating substrate.[26] Because the charge collection process occurs more slowly, recombination in the SI GaAs substrate can be important. While the prompt charge observed in devices with bulk semiconducting substrates continues to increase with applied bias,[25] a saturation in the amount of prompt charge occurs for those devices with Cr-doped SI GaAs substrates.[26] However, the amount of charge collected is in excess of that generated in the epi layer. On the basis of these results, several important issues arise. The amount of excess charge must be established quantitatively, and the role of the substrate in the charge collection process must be determined. The effects of scaling the epi layer thickness on the amount of collected charge also need to be addressed. Here we present preliminary data which focus on the first issue. In order to compare with earlier data for devices with Cr-doped substrates, devices fabricated on undoped SI GaAs substrates were studied.

Figure 3.14 shows the collected charge from two p^+n diodes fabricated on GaAs epi layers. The doping profiles were found to be uniform and the carrier concentration in the 9-μm epi layer was determined to be 6×10^{15} cm^{-3}. The epi layer could not be fully depleted at 70 V due to breakdown. At normal incidence, the alpha particle penetrates into the substrate. Taking 15% prompt recombination into account,[25,28] the amount of free charge remaining in the epi layer after recombination was determined to be 60 fC. As shown in the figure, the prompt and total collected charge increase monotonically and appear to saturate at roughly this value which is shown dashed. However, before clear evidence of saturation occurs, the collected charge increases rapidly above 40 V,

indicating either the onset of another charge generation mechanism or enhanced charge collection from the substrate, or a combination of both. In order to determine if charge collection from the SI GaAs substrate can account for this rise, the angle of incidence of the alpha particle was increased to 65°. At this angle, the alpha particle stops in the relatively thick epi layer at a distance of ~1.8 μm from the epi-substrate interface. The energy loss of the alpha particle in the epi layer is 4.7 MeV, with the remainder of the 5.1 MeV deposited in the metallization and the p^+ top layer. Assuming 15% prompt recombination and 4.8 eV per electron-hole pair, 132 fC of charge remains in the epi layer after recombination at this angle. No charge collection from the substrate should occur for this situation. Figure 3.15 shows the results of these measurements. The total and prompt collected charge saturate monotonically to the expected value of generated charge, which is shown as a dashed line. However, above 50 V a rapid rise is again observed. Note that charge collection is mostly prompt and that the amount of collected charge is greater than that generated. These results suggest that as these charge carriers are swept out by funneling, they undergo multiplication in the epi layer. (Other workers have also considered charge multiplication effects in single-event-upset measurements.[37,38]) This process could cause the rise in the collected charge observed in Figures 3.14 and 3.15 as the applied bias is increased to the breakdown voltage (70 to 80 V).

From the above discussion, the interpretation of charge collection data near the breakdown voltage of a device must take avalanche multiplication into consideration. Charge collection data for previous GaAs devices, discussed above,[26] clearly showed saturation with increasing applied bias. The present GaAs devices exhibit multiplication as the bias is increased. This makes the observation of saturation difficult. To avoid the complicating effects of avalanche multiplication in future investigations of the dependence of collected charge on epi-layer thickness, devices should be designed such that higher breakdown voltages are realized. This may be accomplished, for example, by utilizing a lower doping concentration.

Finally, the effects of multiplication evidently are also manifested in the angular dependence of the collected charge. Figures 3.16, 3.17, and 3.18 show data taken at applied biases of 17 V, 34 V, and 55 V, respectively. The dashed and solid lines are
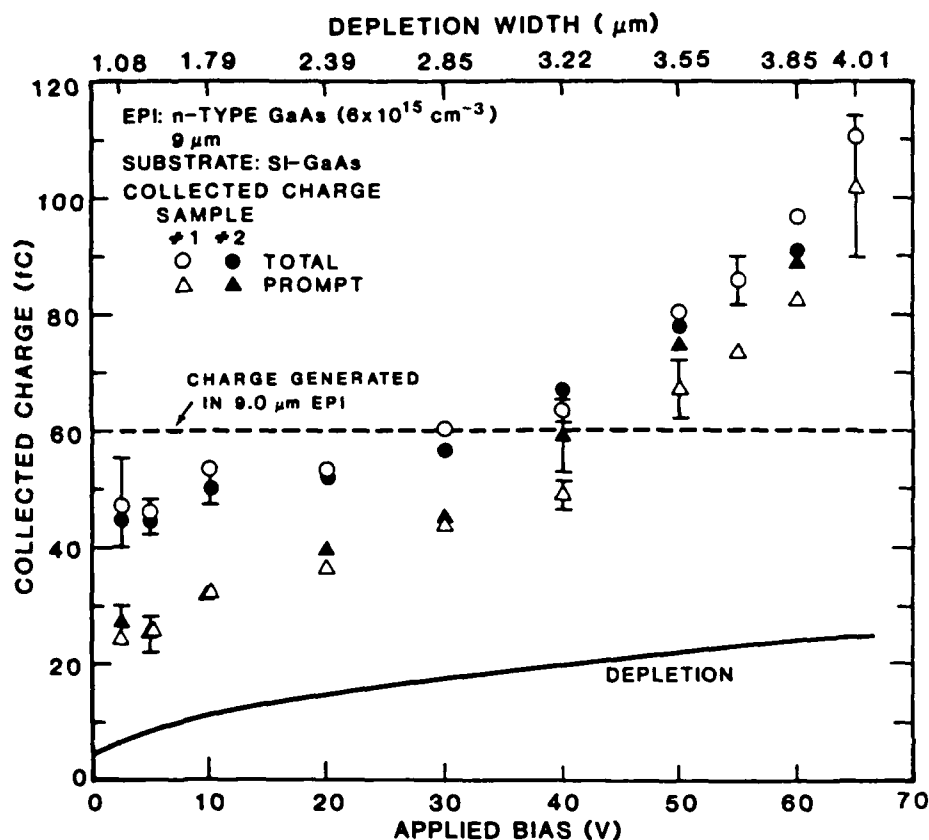
Figure 3.14. Collected charge for p^+n GaAs diodes.

the calculated amounts of net charge generated in the epi layer and in the depletion region, respectively, after 15% prompt recombination has occurred. The decrease in these calculated values at large angles is the result of increasing energy loss in the metallization and in the p^+ top layer. The diffusion charge from the epi layer was subtracted from the prompt charge in the manner described in Appendix H, and the result is designated as the funnel collected charge in the figures. For these devices, an insignificant amount of charge, 5 fC, is generated in the p^+ top layer for angles less than 65°. As the angle of incidence is increased, different behavior of the collected charge is observed for each applied bias. For a bias of 17 V, the funnel charge increases monotonically. Upon comparing these data with those shown in Appendix H, this behavior is found to be qualitatively consistent with that observed in devices which show no multiplication effects. At the higher biases of 34 V and 55 V, however, the

DEPLETION WIDTH (μm)
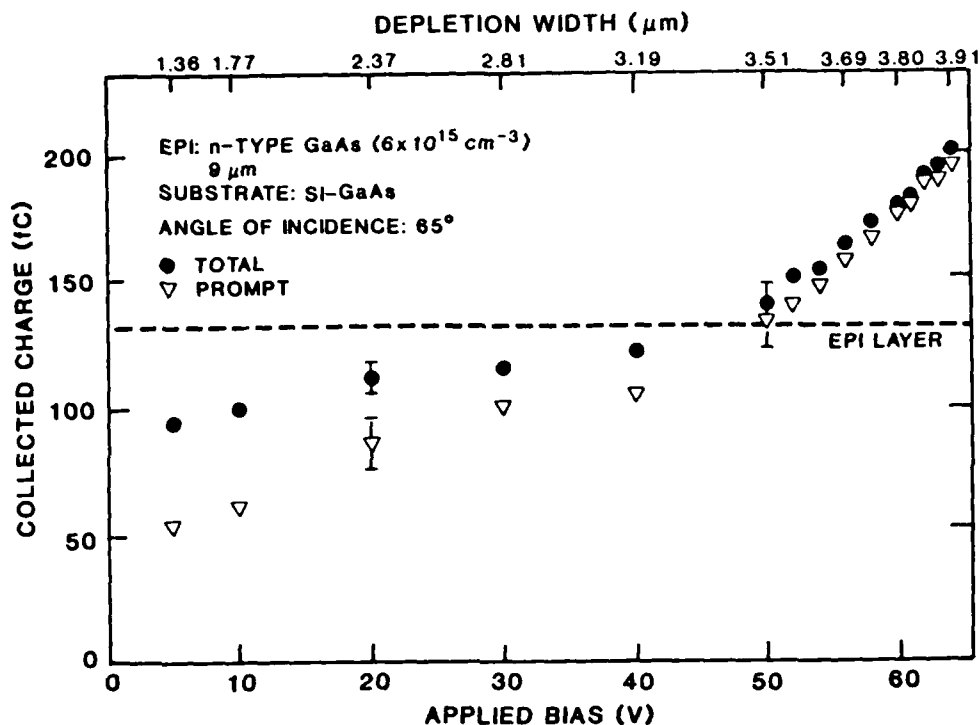
Figure 3.15. Collected charge for a p^+n GaAs diode. The angle of incidence of the alpha particle was 65°.

funnel charge becomes relatively constant for angles less than 30°. Although these results are preliminary, they suggest that, while multiplication is present to some degree for these biases at normal incidence, the multiplication factor decreases as the angle of incidence is increased. Multiplication is again observed at 65° as evidenced by the results shown in Figure 3.15. At present, we have not ruled out the possibility that the alpha particles may traverse relatively low electric field regions which become more accessible at intermediate angles due to the device geometry. The effects of multiplication on the angular dependence data can be more easily seen in the behavior of the normalized funnel charge as a function of angle. In Figure 3.19, the funnel charge is normalized to the amount of charge generated in the depletion region. The dashed lines aid the reader in visualizing trends in the data. The sloping solid lines at higher angles are the expected values of the net charge generated within the GaAs epi layer normalized to the net charge generated only in the depletion region. Consistent with the discussion

relating to Figure 3.18, the behavior of the normalized funnel charge for a bias of 55 V reflects the apparent angular dependence of the multiplication process.
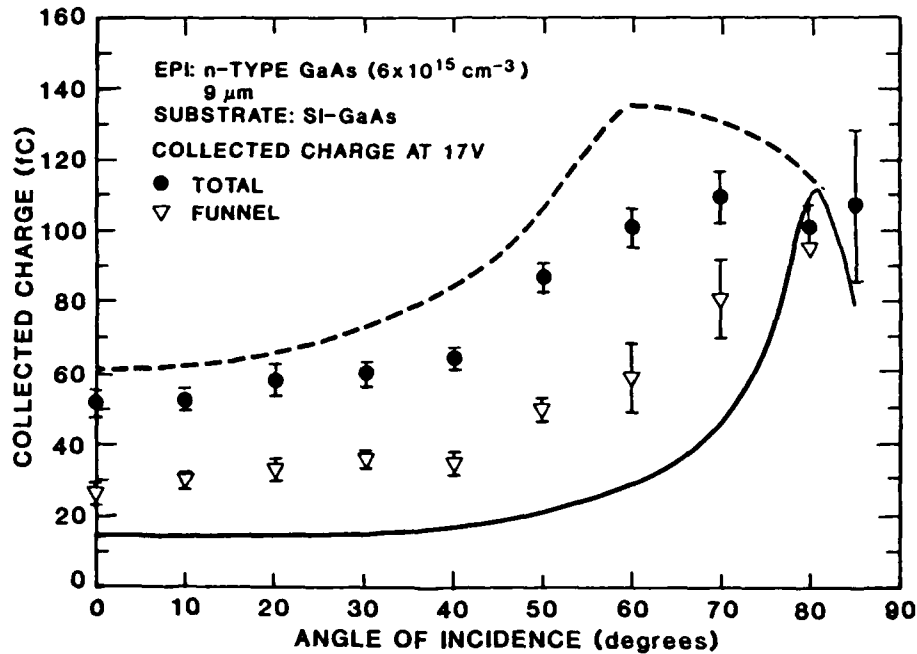
Figure 3.16. Collected charge as a function of angle of incidence for a p^+n GaAs diode biased to 17 V. The dashed and solid lines are the calculated amounts of net charge generated in the 9-μm epi layer and in the depletion region, respectively.

3.3.4 Concluding Remarks.

In conclusion, we have presented data which show that, for Si n^+p devices fabricated on epi layers, the amount of charge collected decreases as the epi layer is made thinner. In addition, the substrate contributes to the collected charge. Silicon p^+n devices with relatively thin epi layers, however, behave more like n^+p devices fabricated on bulk material. Recombination information was also obtained for Si devices. Evidence for avalanche multiplication was obtained for GaAs devices fabricated on epi layers. Multiplication results in an increase in the amount of collected charge near the breakdown voltage and thereby can increase the susceptibility of devices to single-event upset under specific conditions.
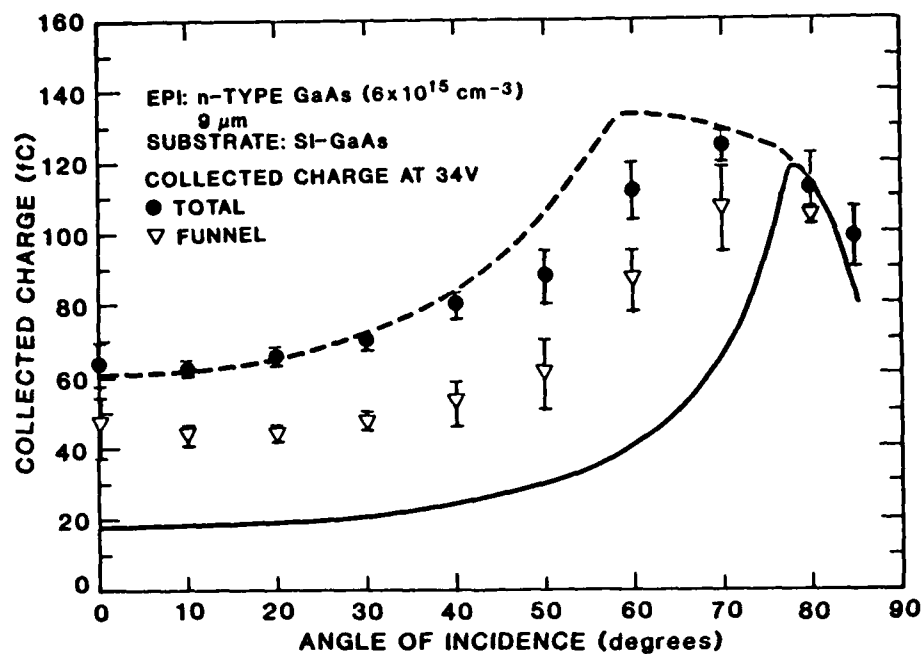
Figure 3.17. Collected charge as a function of angle of incidence for a p$^+$n
GaAs diode biased to 34 V.
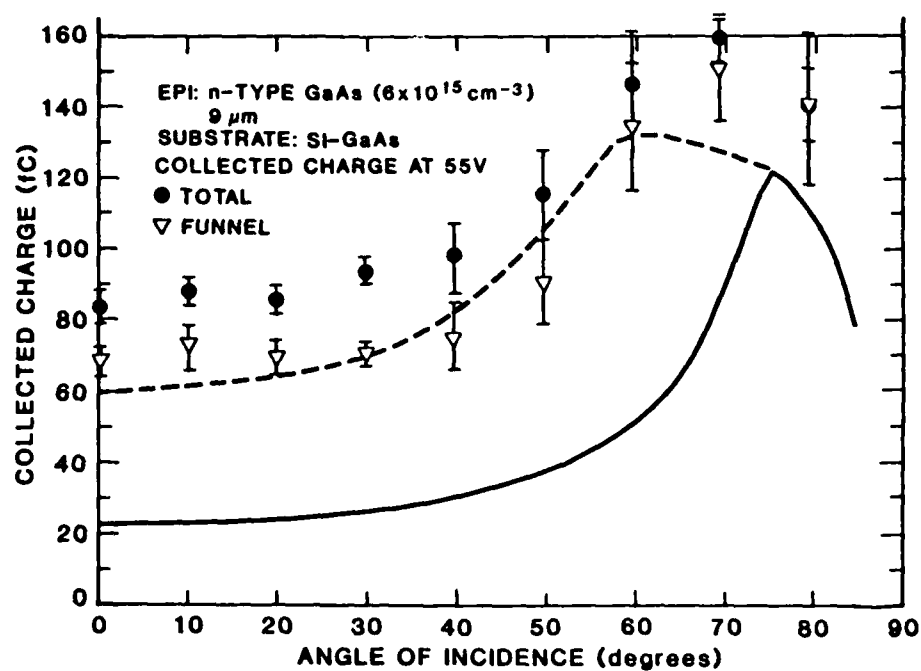
Figure 3.18. Collected charge as a function of angle of incidence for a p$^+$n
GaAs diode biased to 55 V.
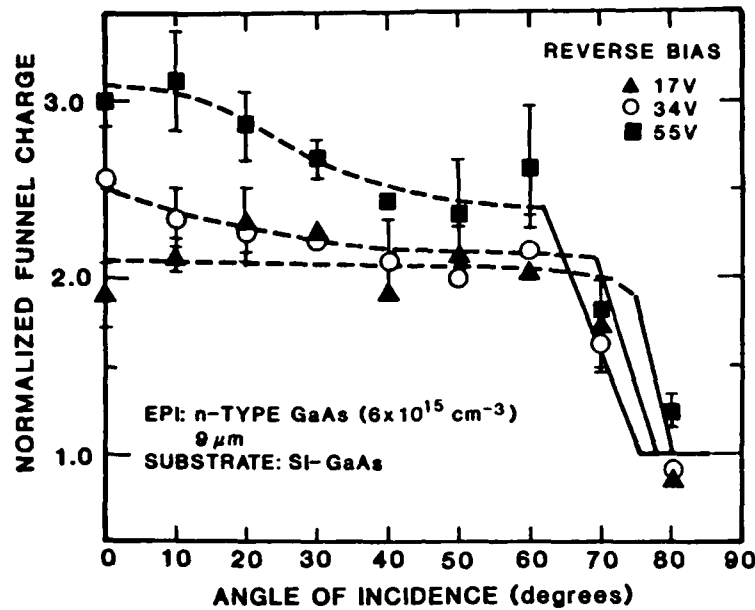
Figure 3.19. Funnel charge normalized to the net charge generated in the original depletion region as a function of angle of incidence for a p^+n GaAs diode with various applied biases.

3.4 TRANSIENT CURRENT MEASUREMENT SYSTEM.

Appendices C and H describe results of transient current measurements performed on Si and GaAs devices following a single alpha-particle strike. The earlier study (Appendix C) was the first report of such measurements. As discussed in that appendix, time-domain-reflectometry measurements performed on the original measurement system revealed that there were impedance mismatches where the probe and its connecting cable contacted the sample. This mismatch produced a significant distortion of the measured waveform. The measurement system was redesigned to yield more accurate current transient waveforms. A brief description of the redesigned system is given in Appendix H. Additional information about this measurement system is given here.

The sample was mounted directly on a 50-Ω microstrip to eliminate the probe-to-sample contact. The microstrips were fabricated at Northrop and consisted of an alumina substrate with evaporated aluminum conductors on the top and the bottom. The sample contacts were then wire-bonded directly to the microstrip. The current

signal was transferred to high-frequency semi-rigid coaxial cable via a SMA launcher. To isolate the DC bias supply from the transient signal, a Picosecond Pulse Labs 5550A bias tee was employed. Figure 3.20 shows the amount of signal reflection due to the microstrip and launcher fixtures. The high reflection coefficient at the end of the microstrip occurred because the sample was not connected for this measurement, resulting in infinite impedance, and thus the signal was fully reflected. The figure shows that there is less than 5% reflection of the transient current signal due to the microstrip and launcher. The bias tee had a reflection coefficient of only 9%. Thus, signal distortion due to reflections was quite low. In addition, the system allowed the angle between the alpha particle track and the sample surface to be varied between 0° and nearly 90°. The measurement system is shown in Figure 3.21. This system was used with a 4-GHz oscilloscope provided by D. Campbell at Lawrence Livermore National Laboratory for transient current measurements. The results of those measurements are presented in Appendix H.
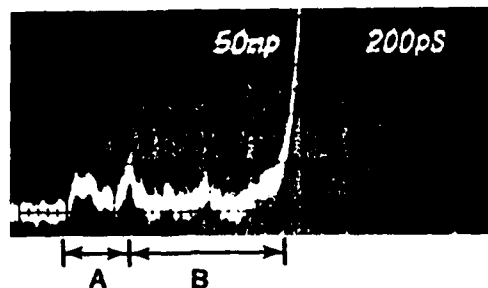
Figure 3.20. Time-domain reflectometry measurement for the present microstrip with a SMA launcher. One vertical division is equivalent to a 5% reflection coefficient. Region A corresponds to the launcher and Region B corresponds to the microstrip.
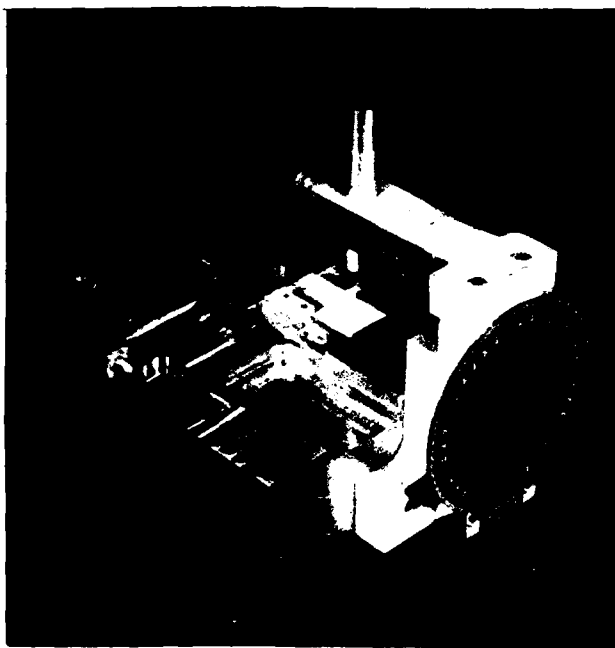
Figure 3.21. Photograph of transient current measurement fixture.

SECTION 4

MECHANISMS OF IONIZING RADIATION
EFFECTS ON MOS DEVICES

4.1 INTRODUCTION.

A Program Review for the present contract was held on 18-19 November 1987. The major topic covered by NRTC at that meeting was a comprehensive review of the progress made in the investigation of ionizing radiation effects on MOS devices. In that mechanisms-oriented study, extensive use was made of the thermally stimulated current (TSC) measurement technique. Other techniques for characterizing the radiation response of MOS devices were also employed. In this section, the charts shown at the Program Review are presented and described briefly. Several comments made at the briefing are also noted. These charts provide an overview of the TSC technique and summarize the key findings made during this program regarding total dose effects.

TSC measurements have been successfully applied by NRTC personnel, under DNA sponsorship, to the study of ionizing radiation effects on silicon MOS devices. The work performed and achievements made are documented in several published papers:

- Z. Shanfield, "Thermally Stimulated Current Measurements on Irradiated MOS Capacitors," IEEE Trans. Nucl. Sci. NS-30, 4064 (1983).

- Z. Shanfield and M.M. Moriwaki, "Characteristics of Hole Traps in Dry and Pyrogenic Gate Oxides," IEEE Trans. Nucl. Sci. NS-31, 1242 (1984).

- Z. Shanfield and M.M. Moriwaki, "Radiation-Induced Hole Trapping and Interface State Characteristics of Al-gate and Poly-Si Gate MOS Capacitors," IEEE Trans. Nucl. Sci. NS-32, 3929 (1985).

- Z. Shanfield and M.M. Moriwaki, "Investigation of Trapped Oxide Charge in MOS Devices," in Proceedings of the 1986 International Symposium for Testing and Failure Analysis, American Society of Metals (Symposium held 20-24 October 1986, Los Angeles, CA), pp. 219-222.

- Z. Shanfield and M.M. Moriwaki, "Critical Evaluation of the Midgap-Voltage-Shift Method for Determining Oxide Trapped Charge in Irradiated MOS Devices," IEEE Trans. Nucl. Sci. NS-34, 1159 (1987).

An additional study that made use of the TSC technique was also published: Z. Shanfield and M.M. Moriwaki, "Effects of Processing Variations on the Radiation Sensitivity of MOS Devices," Journal of Radiation Effects Research and Engineering, Vol. 5, No. 1A, pp. 1-10, Winter 1986.

4.2 REVIEW OF MOS MECHANISMS STUDIES.

An outline of the presentation made at the Program Review is shown in Figure 4.1. At that review, the experimental approach was discussed in detail, especially the underlying assumptions. (Appendices D, E, and G and citations therein in the present report give details regarding many of the figures shown in this presentation, including those dealing with experimental techniques.) The two specific areas of interest noted in Figure 4.1 received considerable attention in our studies. The presentation also included discussion of unresolved MOS hardening issues.

The effects of total ionizing dose on MOS devices are presented in Figure 4.2. Figure 4.3 gives an overview of the goals of MOS mechanisms research in terms of achieiving ultra-hardened devices. The general approach outlined in that figure is repeated as new technologies, DoD missions, and requirements arise.

As noted above, this program involved utilization of a variety of experimental techniques and capabilities that are available at NRTC (Figure 4.4). A number of these techniques were incorporated into an automated measurement system for MOS devices which is illustrated schematically in Figure 4.5.

The primary technique that was used in our studies of the ionizing radiation response of MOS devices was TSC, which is presently unique to NRTC in terms of the specific application. A detailed description of this technique is now presented in a series of charts. The important features are given in Figure 4.6. The TSC technique measures the radiation-induced holes trapped in the oxide near the SiO_2-Si interface. (The coupling of TSC and C-V measurements to determine N_{it} is described in detail

OUTLINE

○ EXPERIMENTAL APPROACH

    BACKGROUND

    CHARACTERIZATION CAPABILITIES

    THERMALLY STIMULATED CURRENT (TSC) TECHNIQUE

    CONDUCTANCE TECHNIQUE

○ SPECIFIC AREAS OF INVESTIGATION

    OVERVIEW

    SPECTROSCOPY OF OXIDE TRAPPED CHARGE AND INTERFACE STATES

    EVALUATION OF THE MIDGAP TECHNIQUE FOR DETERMINING N_{ot}

○ MOS ISSUES

○ MOS SUMMARY

Figure 4.1. Outline of the presentation on MOS mechanisms studies.

TOTAL DOSE EFFECTS ON MOS DEVICES

○ IONIZING RADIATION INTERACTS WITH SiO_2 and Si/SiO_2 INTERFACE

○ INTERFACE STATE GENERATION

○ OXIDE CHARGE TRAPPING

○ DEGRADATION OF DEVICE OPERATING PARAMETERS

Figure 4.2. Listing of the effects of total ionizing dose on MOS devices.

later in the presentation.) The TSC measurement approach is illustrated schematically in Figure 4.7. Important points are that the temperature is ramped linearly with time and that the trapped hole density measured by TSC (denoted here as D_{ot} but on other charts as D_{TSC}) is obtained from the difference between currents (1) and (2).

The parameters, signal levels, and measurement conditions for TSC measurements are given in Figure 4.8. The temperature scan is slow ($\sim$18 minutes) and the electric field is intentionally kept as low as possible to minimize perturbations of the test capacitor. The use of this low field may result in "field reversal" which is discussed

GOALS OF MOS DEVICE RESEARCH


```
┌─────────────────────────────────┐
│ DETERMINE PHYSICAL/CHEMICAL     │
│ NATURE OF HOLE TRAPS            │
│ AND INTERFACE STATES            │
└─────────────────────────────────┘
                │
                ▼
┌─────────────────────────────────┐
│ DETERMINE WHICH PROCESSING      │
│ PROCEDURES GIVE RISE TO HOLE    │
│ TRAPS AND INTERFACE STATES      │
└─────────────────────────────────┘
                │
                ▼
┌─────────────────────────────────┐
│ ACHIEVE HARDNESS ENGINEERING    │
└─────────────────────────────────┘
                │
                ▼
┌─────────────────────────────────┐
│ REALIZE ULTRA-HARD MOS DEVICES  │
└─────────────────────────────────┘
```
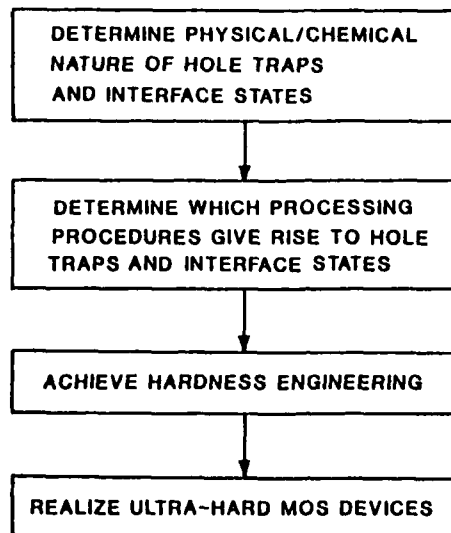
Figure 4.3. Overview of the goals of MOS mechanisms research.

MOS CHARACTERIZATION CAPABILITIES

o HIGH FREQUENCY C-V / TERMAN ANALYSIS

o QUASI-STATIC C-V / Q-V MEASUREMENTS

o CONDUCTANCE VERSUS FREQUENCY AND BIAS

o JENQ TECHNIQUE

o DLTS

o FAST RAMP TECHNIQUE

o THERMALLY STIMULATED CURRENT

o TRANSISTOR CHARACTERIZATION

o FROM ~4K TO 400°C

Figure 4.4. MOS measurement techniques and capabilities at NRTC.

below. The sequence of measurements included in the TSC experimental procedure are listed in Figure 4.9. Most irradiations are performed with an applied field of +1.0 MV/cm. An example of the observed currents is shown in Figure 4.10 where the solid

FUNCTIONAL DIAGRAM OF MOS CHARACTERIZATION SYSTEM
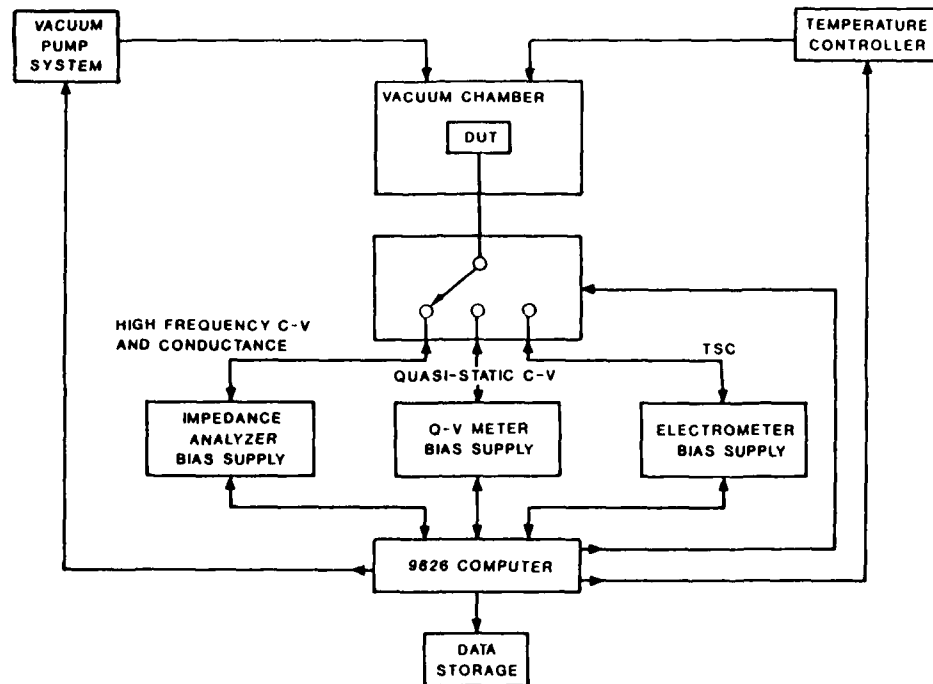
Figure 4.5. Schematic diagram of the automated measurement system used for MOS measurements.

TSC TECHNIQUE

○ EQUIVALENT TO BIAS-TEMPERATURE ANNEAL

○ DETERMINES DENSITY AND ACTIVATION ENERGIES OF CHARGE DISTRI-
BUTIONS IN THE <u>INSULATOR</u> OF AN MIS DEVICE. MEASURES CHARGE
DISTRIBUTION CHANGES THAT OCCUR <u>DURING</u> THE MEASUREMENT

○ MEASURES RADIATION-INDUCED HOLES TRAPPED IN SiO_2 NEAR THE
SiO_2/Si INTERFACE

○ DETERMINES N_{it} vs ψ_s WHEN COUPLED WITH C-V

Figure 4.6. Listing of the main features of the TSC measurement technique
(ψ_s is the surface potential).

curve is the "data" and the dashed curve is the "baseline" (corresponding to curves (1) and (2) in Figure 4.7, respectively). Example C-V curves are presented in Figure 4.11. In most cases, curve C overlays curve A.

SCHEMATIC REPRESENTATION OF TSC TECHNIQUE
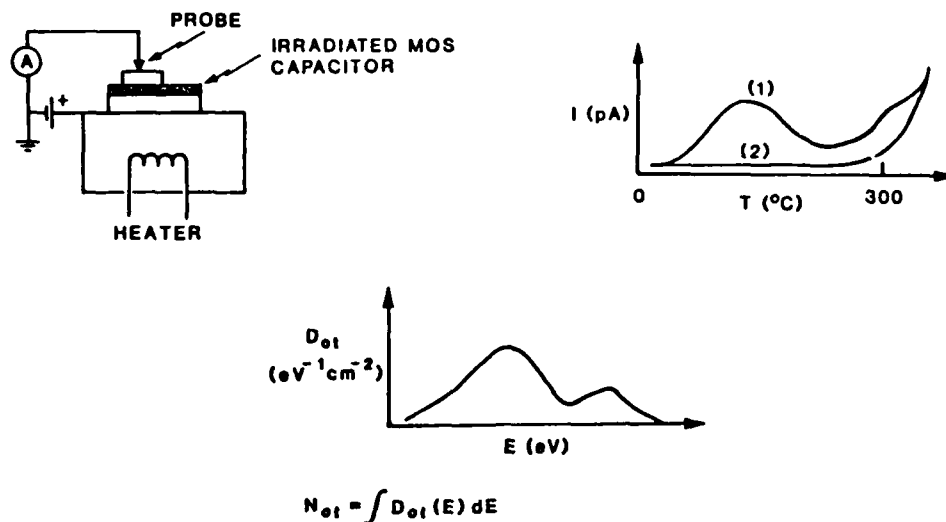
Figure 4.7. Illustration of the key features of the TSC measurement technique.

TSC MEASUREMENT PARAMETERS

- LINEAR TEMPERATURE SCAN FROM ROOM TEMPERATURE TO 400°C AT RATE OF 0.35°C SEC (~ 18 MINUTES)

- SAMPLE IN VACUUM

- CURRENT LEVELS FROM <0.1 pA to 10's OF pA

- GATE BIASED WITH OXIDE FIELD OF - 0.5 MV / cm

Figure 4.8. TSC measurement conditions.

A band diagram representing the MOS capacitor during the TSC measurement procedure is shown in Figure 4.12. The energy position of the trapped holes is only schematic since TSC determines activation energies, not absolute energy levels. The conversion from temperature to activation energy using the theory of Simmons et al.[39] is summarized in Figure 4.13. The only arbitrary parameter is ν, the attempt-to-escape frequency, which affects the conversion only weakly because of the logarithmic dependence.

EXPERIMENTAL PROCEDURE

o PRE-IRRADIATION

    - CV

    - TSC "DATA" (- V_{GATE})

    - CV

    - TSC "BASELINE" (- V_{GATE})

    - CV

o IRRADIATION + V_{GATE} ROOM TEMPERATURE

o POST IRRADIATION

    - CV

    - TSC "DATA" (- V_{GATE})

    - CV

    - TSC "BASELINE" (- V_{GATE})

    - CV

Figure 4.9. Listing of the sequence of measurements included in the TSC experimental procedure.
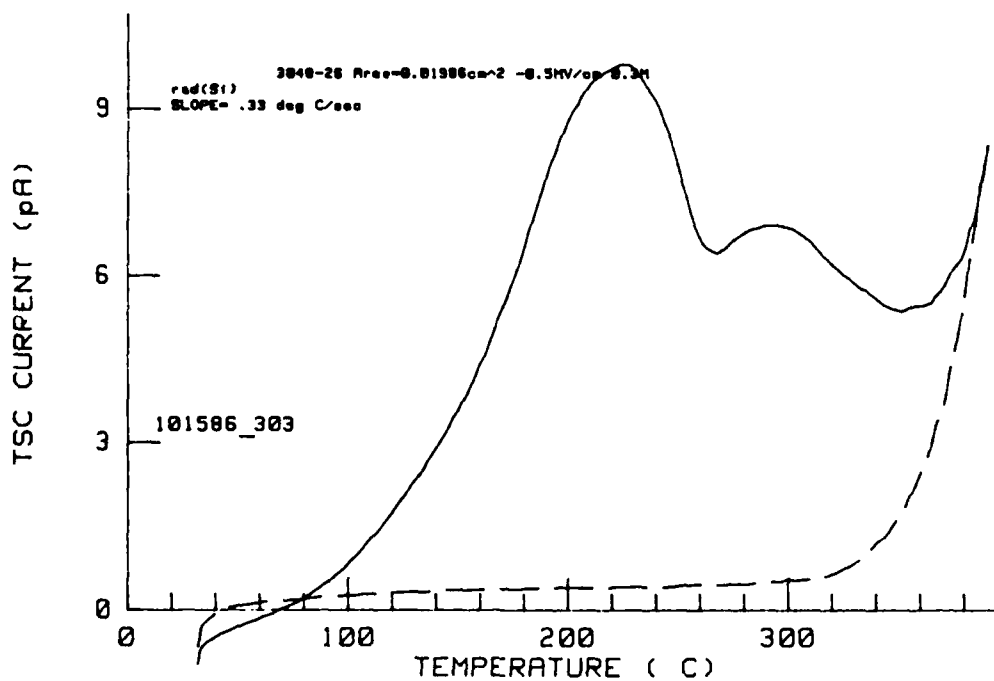
Figure 4.10. Example TSC data.
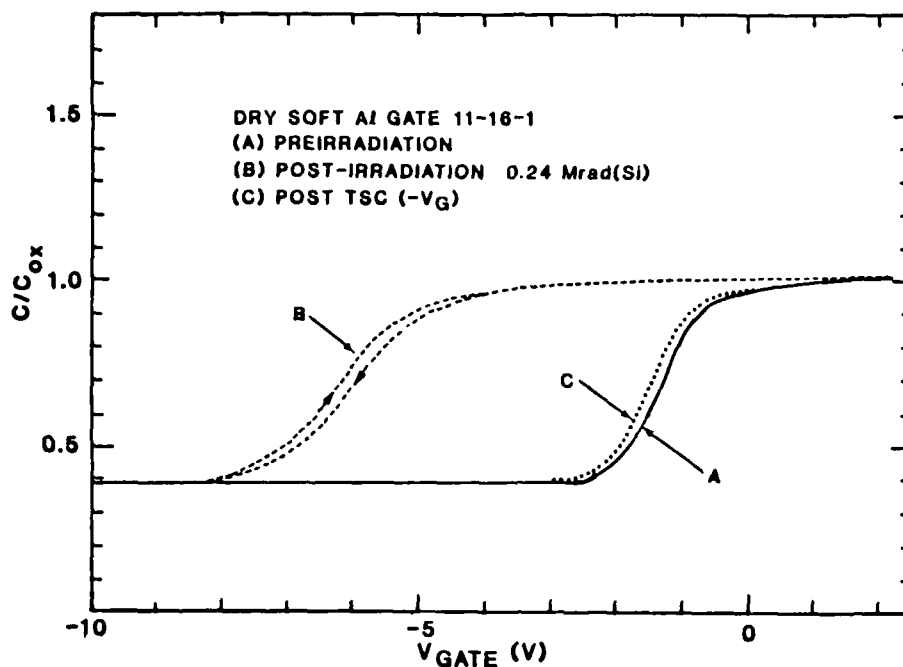
Figure 4.11. Example C-V curves obtained during the TSC measurement procedure.

A functional diagram of the TSC measurement system is given in Figure 4.14, while Figures 4.15 through 4.17 are photographs of the equipment. The most critical element in the system is the sample mounting fixture which is shown schematically in Figure 4.18. Capacitors to be tested are bonded with silver epoxy to a Au-Cr coated alumina substrate which is mounted by machinable ceramic lugs to a copper block containing the heater. The heater is electrically isolated from this block which is guarded and has its own return to system electrical ground. The TSC current is measured by biasing the substrate while a probe is brought in contact with the gate electrode of the capacitor to complete the electrical circuit. The probe manipulator is on a separate grounded platform. Without these extensive precautions, unacceptable thermally induced leakage currents occur which may obscure the signal from the test device.

The physics of the TSC process is now described. The fundamental points regarding the TSC process are listed in Figure 4.19. The effects of MOS capacitor bias on the TSC measurement process are illustrated in Figure 4.20. The TSC measurement process involves applying a negative bias to a MOS capacitor, often one which has been

MOS BAND DIAGRAM DURING TSC
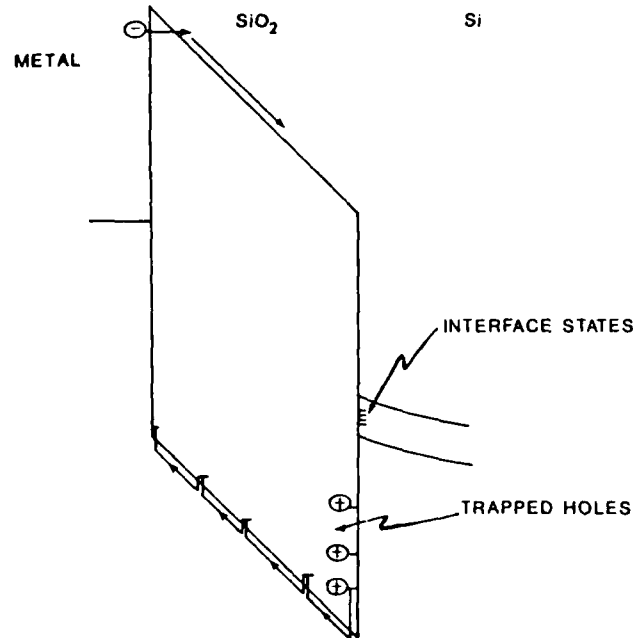
Figure 4.12. Energy band diagram for an MOS capacitor during TSC measurements.

CONVERSION OF TEMPERATURE SCALE TO ACTIVATION ENERGY SCALE

(THEORY OF SIMMONS)

$T = T_0 + \beta t \quad (\beta \approx 0.35°C/\ sec)$

$E_t - E_v = \Delta E = T \ (1.92 \times 10^{-4} \log_{10} \frac{\nu}{\beta} + 3.2 \times 10^{-4}) - 0.015$

$\nu = 10^{10} - 10^{12} \ sec^{-1}$

Figure 4.13. Description of the method used to convert temperature to activation energy.

irradiated previously. An explanation of this process is given in Figure 4.20 through the use of band diagrams and charge distributions in the device. A capacitor without oxide charge is shown in the upper left. Once charge generated by irradiation is trapped in

FUNCTIONAL DIAGRAM OF TSC MEASUREMENT SYSTEM
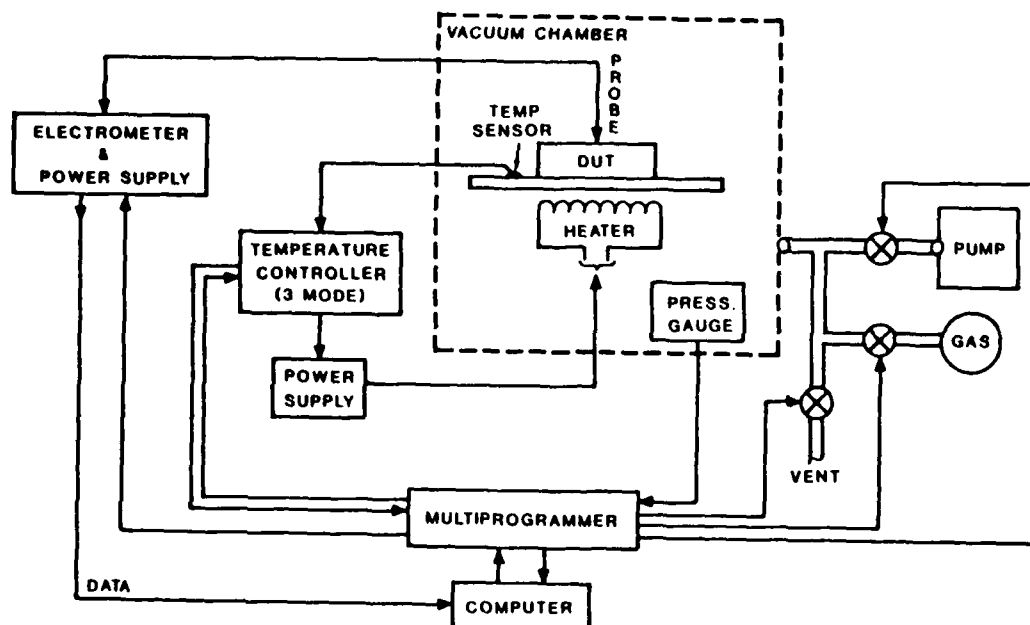
Figure 4.14. Schematic diagram of the TSC measurement system.

the oxide near the Si-SiO$_2$ interface, negative image charge is induced predominantly in the Si. In the lower left, sufficient oxide charge is indicated to cause accumulation in the n-type Si sample. At the elevated temperatures and for the relative slow temperature ramp used during TSC measurements, the capacitor is in thermal equilibrium. When a positive charge in the oxide is thermally released and travels across the oxide to the gate electrode, the induced charge imbalance is corrected by the movement of an electron in the external circuit which contributes to the TSC signal. The amount of charge measured is proportional to the fraction of the distance across the oxide that the positive charge moves in the oxide. This effect is illustrated by the data in Figure 4.21 which shows TSC spectra for holes moving to the gate (negative gate bias) and to the Si (positive gate bias). Using the difference in magnitude of the measured charge, its location in the oxide can be estimated to be 75 to 125 Å from the Si-SiO$_2$ interface for the example case of a 1000-Å oxide.

The reason for the lack of an effect of interface state annealing on the TSC signal can be explained using Figure 4.22. Charged interface states contribute to the charge

Figure 4.15. Photograph of the MOS characterization system which includes TSC measurements.

balance of the capacitor in equilibrium. A large number of negatively charged interface states would result in less accumulation. If these interface states anneal, the charge then would transfer into the accumulation layer without contributing current in the external circuit. Changes in band-bending induced thermally and induced by oxide charge annealing would also simply redistribute the charge on the Si side of the oxide without causing charge flow in the external circuit.

As a test of this model, capacitors were irradiated to various doses such that the fixed bias (–5 V) used for the TSC measurement resulted in band-bending which ranged from near flatband to inversion (Figure 4.23). For different band-bending conditions, different interface states should be charged. The TSC spectra (Figure 4.24) all showed the same signature which is not expected if charged interface states contributed to the TSC signal.

4–11
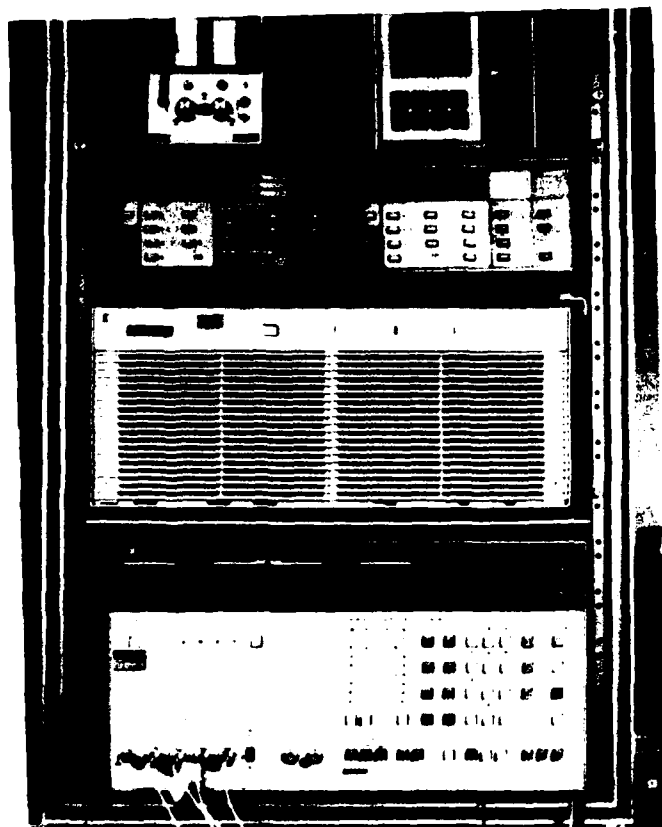
Figure 4.16. Photograph of the measurement electronics used for MOS characterization, including TSC measurements.

Another measurement used in our study of radiation effects on MOS devices is the conductance technique. The features of that technique are listed in Figure 4.25, while the underlying theory is given in Figure 4.26. Among the important parameters measured by the conductance technique are density of interface states, surface potential fluctuations, capture cross sections, and response time (Figure 4.27). Surface potential fluctuations (σ_s) can be used to determine whether the interface state is a donor or acceptor. The effects of surface potential fluctuations on interface state measurements by the conductance technique are discussed by Nicollian and Brews.[3]

Experimental details associated with our implementation of the conductance technique are given in Figure 4.28. The steps involved in determining interface state parameters are listed in Figure 4.29. Figure 4.30 shows an example of raw conductance data for an irradiated sample, while Figure 4.31 shows the reduced data that is used

Figure 4.17. Photograph of the sample chamber used in TSC measurements.

SAMPLE MOUNTING FIXTURE
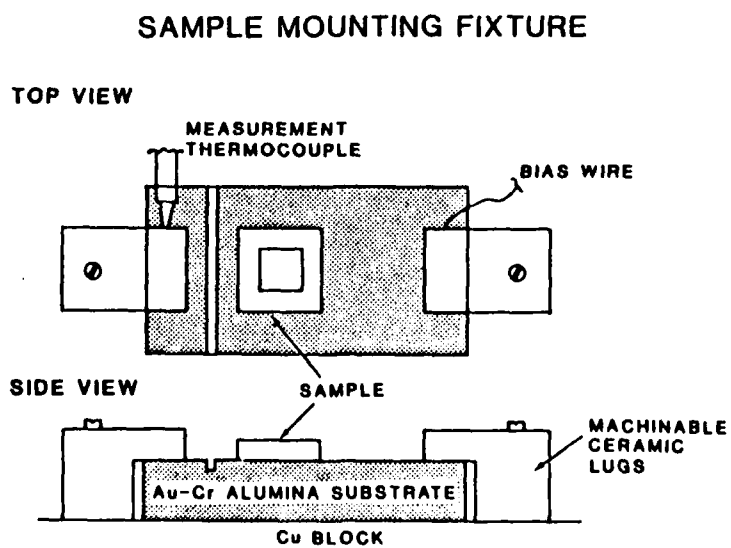
Figure 4.18. Schematic illustration of the TSC sample mounting fixture.

4-13

PHYSICS OF THE TSC PROCESS

○ BIASED MOS CAPACITOR IN THERMAL EQUILIBRIUM

○ DEVICE <u>NOT</u> A CURRENT SOURCE

○ MEASURED CURRENT IS THE CHARGE NECESSARY TO KEEP MOS
CAPACITOR IN EQUILIBRIUM AFTER PERTURBATION OF THE CHARGE
<u>IN</u> THE OXIDE

Figure 4.19. Fundamental features of the TSC measurement.

TSC PROCESS

NO OXIDE CHARGE

OXIDE CHARGE MOVES ACROSS
OXIDE AND RECOMBINES. CHARGE
ON CAPACITOR NOT IN BALANCE

OXIDE CHARGE

ELECTRONS FLOW IN EXTERNAL
CIRCUIT FROM Si TO GATE TO
RE-ESTABLISH CHARGE BALANCE
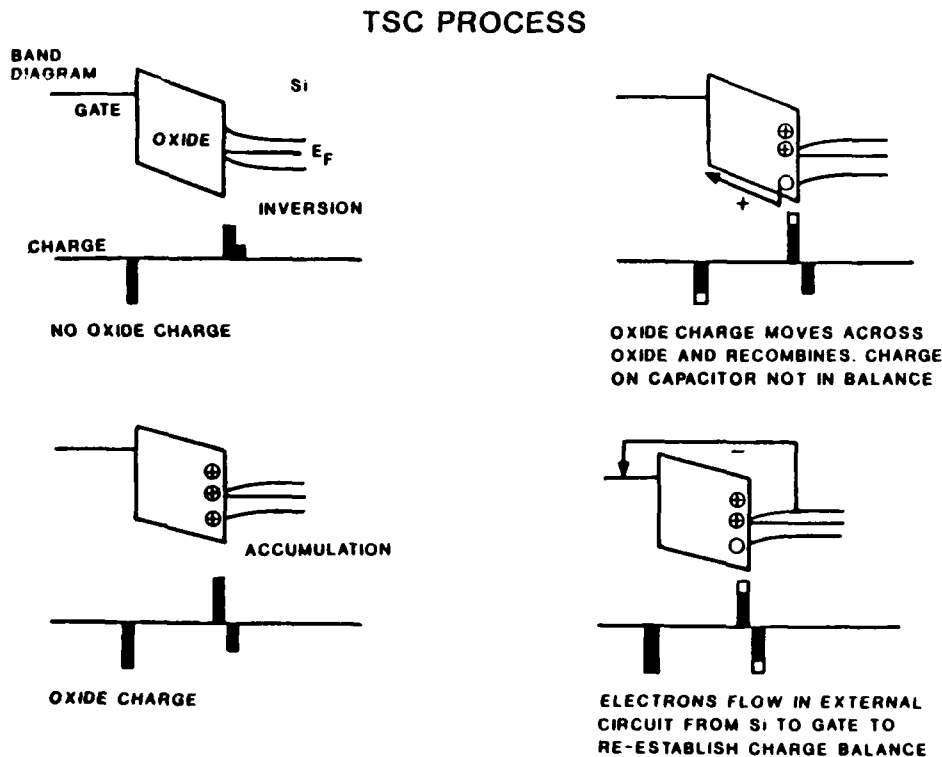
Figure 4.20. Illustration of the TSC measurement process in terms of pos-
itive charge movement in the oxide and electron flow in the
external circuit.

to calculate interface state parameters. Results obtained from these and other data are
presented below.

Results obtained in specific areas investigated during this program are now pre-
sented. First, an overview is given (Figure 4.32). Spectroscopy of oxide trapped charge

EFFECT OF TSC BIAS POLARITY

TEMPERATURE (°C)

AI GATE
DRY OXIDE
POA
0.21 Mrad(Si) (+1 MV/cm)

TSC
(~0.5 MV/cm)

TSC
(+0.5 MV/cm)

ACTIVATION ENERGY (eV)
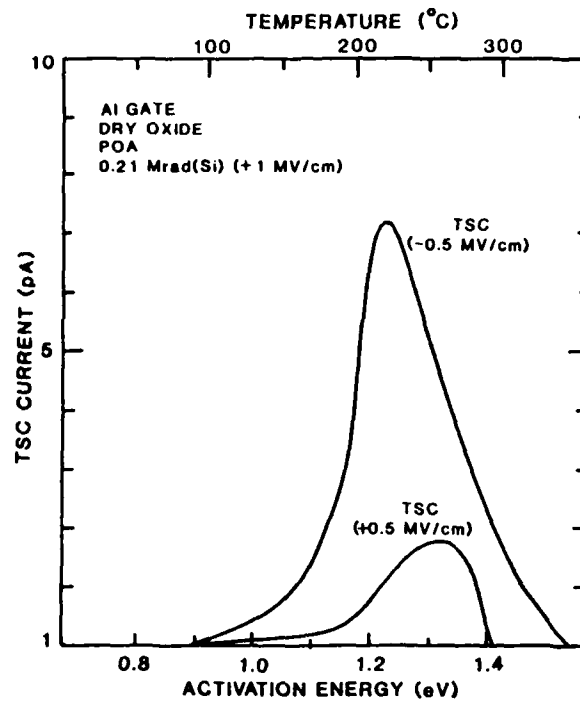
Figure 4.21. Example TSC spectra for the cases of positive and negative gate bias applied during the measurement.

EFFECT OF INTERFACE STATES

GATE   OXIDE   Si

⊕
⊕
⊕

CHARGED
INTERFACE
STATE

87106
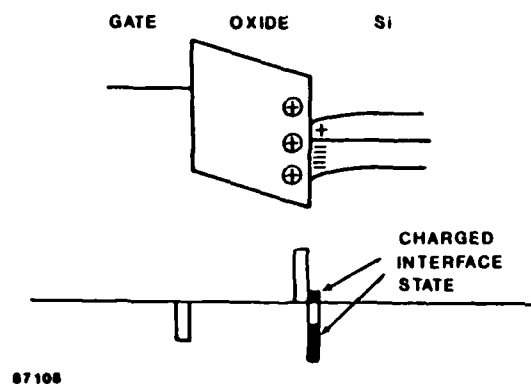
○ OXIDE CHARGE ANNEALING

○ CHARGED INTERFACE STATE ANNEALING

Figure 4.22. Illustration of charged interface states and their potential effect on TSC measurements.

4-15

EFFECT OF BAND BENDING ON TSC MEASUREMENTS
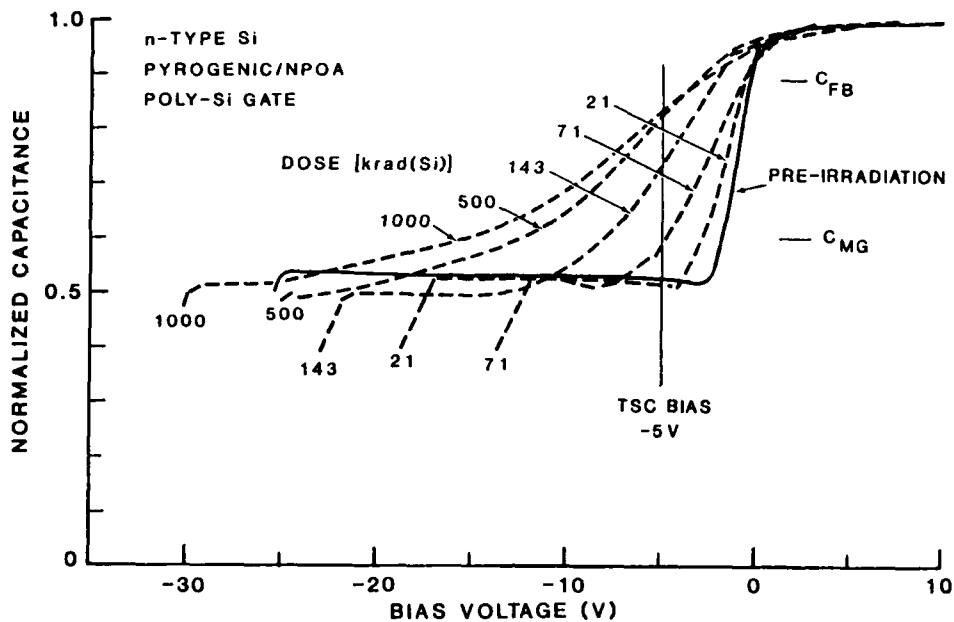
Figure 4.23. Capacitance-voltage curves obtained as a function of dose in an examination of potential interface state effects on TSC measurements.

was performed using TSC, and oxide trapped charge (N_{ot}) and interface charge density (N_{it}) were determined. In addition, a critical evaluation was performed of the midgap technique for determining N_{ot}. Examples of the spectroscopy of oxide trapped charge are presented in Figures 4.33 and 4.34. Integration of the density of states yields N_{ot} which is plotted as a function of dose in Figure 4.35. The method used to determine N_{it} by combining data from TSC and high-frequency C-V measurements is described in Figure 4.36. Examples of results obtained using this approach to determine N_{it} are given in Figure 4.37 as a function of surface potential and in Figure 4.38 as a function of dose.

During this review, issues were raised regarding whether the measured TSC signal yields all the oxide trapped charge. The first issue concerned the saturation of N_{TSC} shown in Figure 4.35. Specifically, can the trapping of holes in the oxide result in field collapse in the region between the charge near the Si-SiO$_2$ interface and the gate during irradiation? Analysis of this situation shows that for field collapse to occur, the C-V

EFFECT OF BAND BENDING ON TSC DENSITY OF STATES
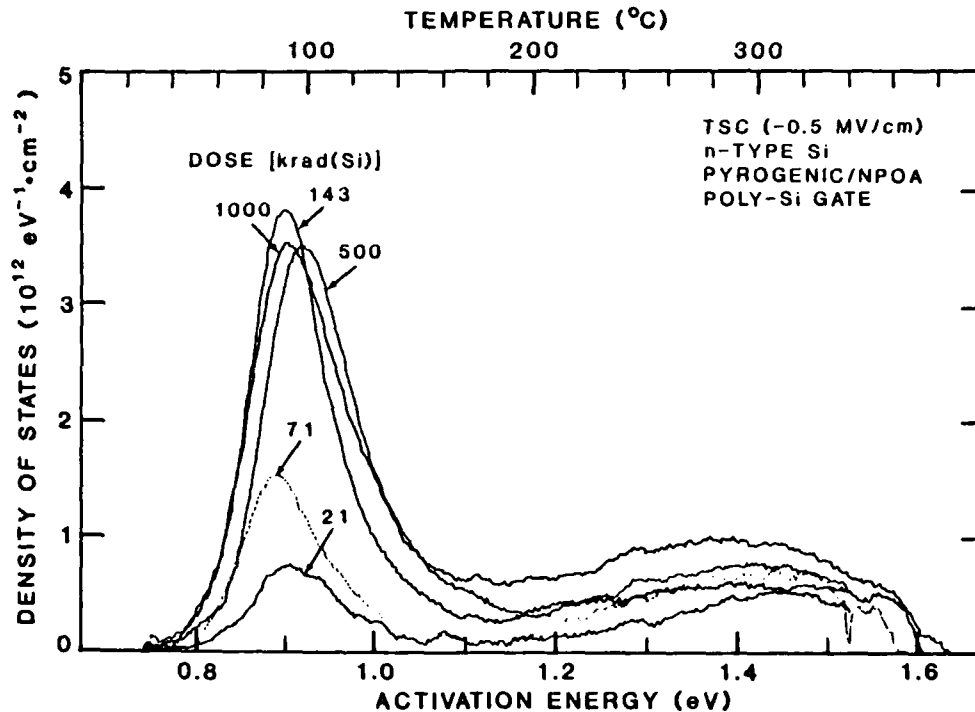
Figure 4.24. TSC spectra obtained as a function of dose in an examination
of potential interface state effects on TSC measurements.

shift ΔV must be equal to the applied TSC bias times the ratio of the oxide thickness
to the distance of the charge distribution from the Si-SiO$_2$ interface. Assuming that
the trapped hole distribution is within a distance from the interface of 10% of the
oxide thickness, then no field collapse occurred for the samples in this investigation.
The second issue raised was the possibility of field reversal in the region between the
charge distribution and the Si during the TSC measurement. Analysis shows that this
is possible. When ΔV induced by irradiation is equal to the applied TSC bias, the
field in this region goes to zero. A ΔV of twice the TSC bias would result in a field of
approximately the same magnitude as that due to the applied bias but with opposite
polarity. Such a situation could result in a TSC signal which is less than that due to
the actual amount of hole trapping in the oxide. The technique described in Figure 4.36
would then give too positive a value of N_{it}. Some of our measurements indicate that this
does not occur. However, the data obtained thus far is not conclusive, and additional

CONDUCTANCE TECHNIQUE

o MEASURES THE FREQUENCY AND BIAS DEPENDENCE OF THE ADMITTANCE OF MOS CAPACITORS

o CONDUCTANCE IS THE REAL COMPONENT OF COMPLEX ADMITTANCE

DISSIPATIVE ENERGY LOSS

o CAPACITANCE PROPORTIONAL TO IMAGINARY COMPONENT OF COMPLEX ADMITTANCE

INTERFACE STATES STORE CHARGE

o DETERMINATION OF INTERFACE STATE PARAMETERS DEPENDS ON CIRCUIT MODEL

LUMPED CIRCUIT COMPONENTS

DISTRIBUTION OF INTERFACE STATES IN ENERGY AND SPACE

ANALYSIS SIMPLIFIED FOR DEPLETION REGION (MAJORITY CARRIERS)

Figure 4.25. Features of the conductance technique for determining interface state properties.

THEORY

o SHOCKLEY-READ STATISTICS:

NET INTERFACE STATE CURRENT = q (R - G)

WHERE R IS THE CAPTURE RATE AND G IS THE GENERATION RATE

o LEHOVEC DESCRIBED THE ADMITTANCE ASSOCIATED WITH A SINGLE INTERFACE STATE AS AN RC SERIES NETWORK WITH TIME CONSTANT τ

o LEHOVEC EXTENDED THE SINGLE INTERFACE STATE MODEL TO A CONTINUUM OF INTERFACE STATES

o DISCREPANCY BETWEEN MODEL AND EXPERIMENT RESOLVED BY ASSUMING THAT SURFACE POTENTIAL FLUCTUATIONS AFFECT τ - BREWS

INTERFACIAL CHARGES RANDOMLY LOCATED RESULT IN A SPATIAL DISTRIBUTION OF BANDBENDING

DISPERSION OF τ INCREASES RANGE OF FREQUENCY RESPONSE

Figure 4.26. Theory underlying the conductance technique.

DETERMINATION OF INTERFACE STATE PARAMETERS

o MEASURES FREQUENCY DEPENDENCE OF NET CAPTURE AND EMISSION
RATES OF CARRIERS FROM INTERFACE STATES IN SMALL ENERGY
INTERVAL CENTERED ON ψ_s

o THEORETICAL PREDICTIONS FIT EXPERIMENTAL DATA WELL

o MOS DEVICE PARAMETERS OBTAINED INCLUDE

D_{it} $(10^9 - 10^{12}$ eV^{-1} cm$^{-2})$

INTERFACE STATE CAPTURE CROSS SECTION

INTERFACE STATE RESPONSE TIME τ (CHARACTERISTIC TIME FOR
INTERFACE STATES TO REACH EQUILIBRIUM WITH Si)

SURFACE POTENTIAL FLUCTUATIONS (σ_s)

Figure 4.27. Parameters that can be determined by the conductance technique.

EXPERIMENTAL DETAILS

o HP 4192 IMPEDANCE ANALYZER

ADMITTANCE DATA TAKEN AS BIAS IS SWEPT

MEASUREMENT IS REPEATED FOR VARIOUS FREQUENCIES (5kHz to
1MHz)

o DATA ACQUISITION IS COMPUTER CONTROLLED

o INDUCTANCE ($<$ 0.5μH) AND SERIES RESISTANCE (0.5Ω) MINIMIZED IN
MEASUREMENT CIRCUIT

o INTERFACE CONDUCTANCE, G_p, EXTRACTED FROM MEASURED
CONDUCTANCE, G_m, USING ANALYSIS SOFTWARE

Figure 4.28. Information concerning the NRTC implementation of the conductance technique.

measurements will be required. Also, we have observed N_{TSC} to be both larger and smaller than $C_{ox}\Delta V$. The case where N_{TSC} is greater than $C_{ox}\Delta V$ is consistent with negative N_{it}. No other mechanism except negative N_{it} has been proposed to account for this case.

Results of measurements of radiation-induced oxide trapped charge by TSC spectroscopy and interface state determinations based on TSC and C-V are now presented.

STEPS IN DETERMINING INTERFACE STATE PARAMETERS

- G_m VERSUS V_G FOR VARIOUS FREQUENCIES

- CORRECTION OF SAMPLE SERIES RESISTANCE (MEASURED IN ACCUMULATION)

- CONVERSION TO INTERFACE STATE CONDUCTANCE (G_p/ω)

- DETERMINE $(G_p/\omega)_{peak}$, ω_{peak} FROM G_p/ω VERSUS ω

- CALCULATE D_{it}, σ_s, τ BY METHOD OF NICOLLIAN AND BREWS

- DETERMINE $\bar{\psi}_s$ USING TERMAN ANALYSIS

Figure 4.29. Listing of the steps involved in obtaining interface state parameters.

UNCORRECTED CONDUCTANCE DATA 100 krad(Si)
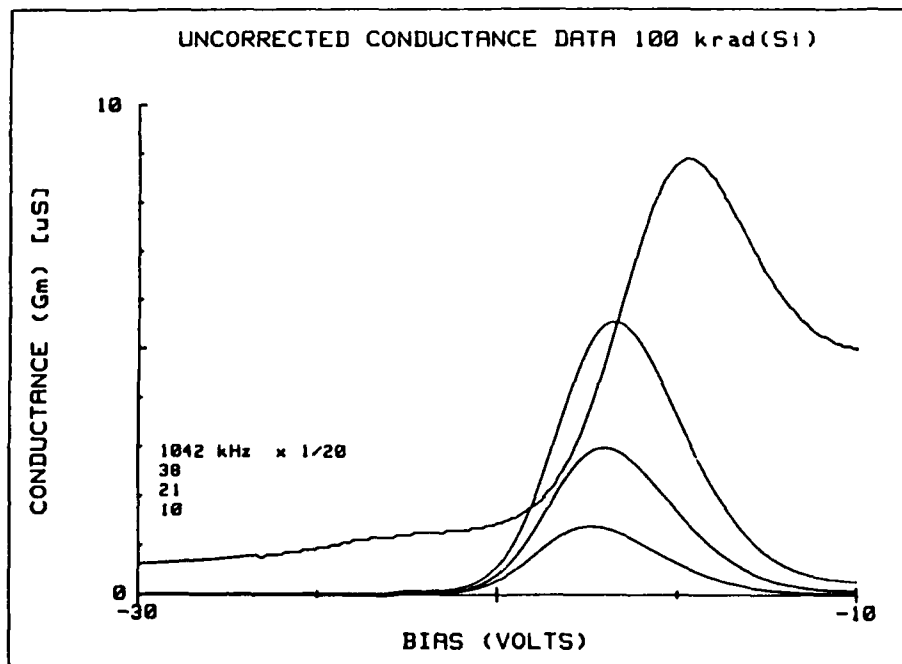
Figure 4.30. Example conductance data for an irradiated MOS capacitor.

The processing variations considered are listed in Figure 4.39. Most of these MOS capacitors were fabricated at Sandia National Laboratories. (Investigation of the two-step oxidation process (oxidation/anneal/oxidation) and the effects of post-oxidation anneal

```
POLY SI n-TYPE #4 WET/SOFT C1301A W#13 100Krad(SI)
@+1.0MV/cm Area=0.01444cm^2
```
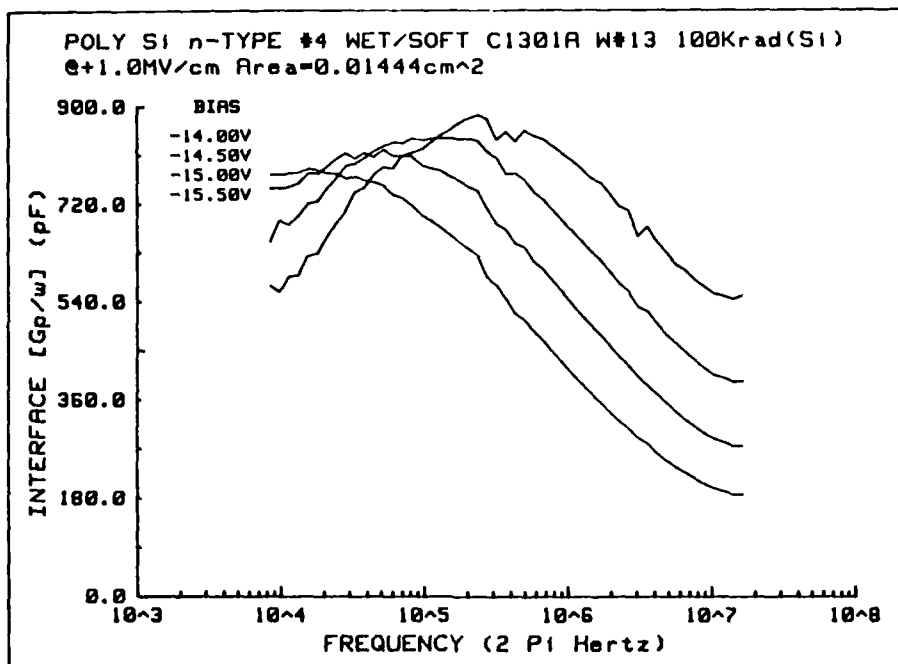
Figure 4.31. Reduced data used to calculate interface state parameters.

OVERVIEW

o SPECTROSCOPY OF OXIDE TRAPPED CHARGE

    ELECTRICAL MEASUREMENT SENSITIVITY

    GIVES PROCESSING SIGNATURE

o DETERMINATION OF N_{ot}

o DETERMINATION OF N_{it}

Figure 4.32. Overview of the areas investigated during this program.

(POA) duration (oxidation/POA/oxidation) were supported in part by Northrop and are included here for completeness.)

    TSC spectra for a poly-Si gate capacitor with a pyrogenic oxide for the case of no POA (NPOA) are shown in Figure 4.40. The 0.9-eV peak is associated with H or OH. For comparison, Figure 4.41 shows data for a dry-oxide capacitor. The 0.9-eV peak exists but is much smaller at the same dose. For these cases, H is introduced into the oxide during phosphine doping of the poly Si. If a high-temperature (1100°C) POA

4-21

SPECTROSCOPY OF OXIDE TRAPPED CHARGE
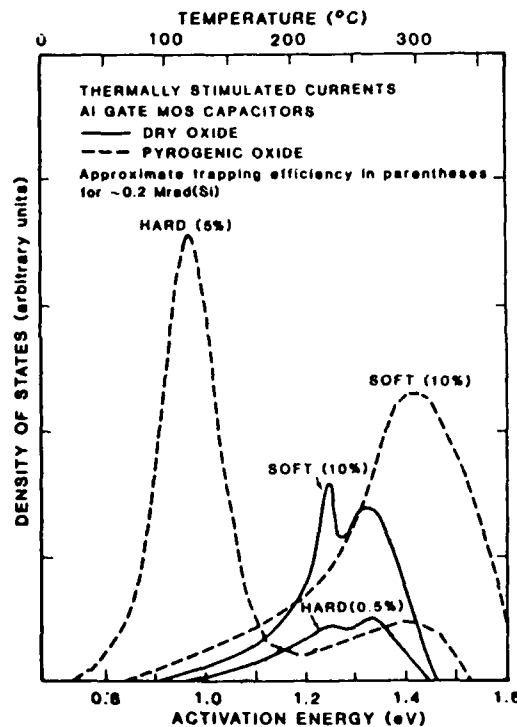
Figure 4.33. Example spectroscopy results obtained using TSC.

occurs before poly-Si processing, the 0.9-eV peak is absent while a broad distribution extends from 0.8 to 1.6 eV (Figure 4.43). Figure 4.43 summarizes the results for poly-Si gate devices.

TSC spectra for Al-gate MOS capacitors are shown in Figure 4.44. The pyrogenic oxide without POA shows the 0.9-eV peak, while after POA the same spectra as exhibited in Figure 4.42 occurs. The major difference is that without a high-temperature H source (steam-grown oxide or phosphine doping of the poly-Si gate) a different spectrum with overlapping peaks at 1.25 and 1.35 eV occurs. A variety of hole trapping sites may exist in the oxide, depending on the fabrication history of the devices.

Behavior of the oxide trapped charge density as a function of dose is shown in Figure 4.45. Although different processes result in different radiation sensitivities, in general a saturation of N_{ot} with dose always occurred between 200 to 500 krad(Si). As expected, samples that received a POA are the least radiation tolerant.

SPECTROSCOPY OF OXIDE TRAPPED CHARGE
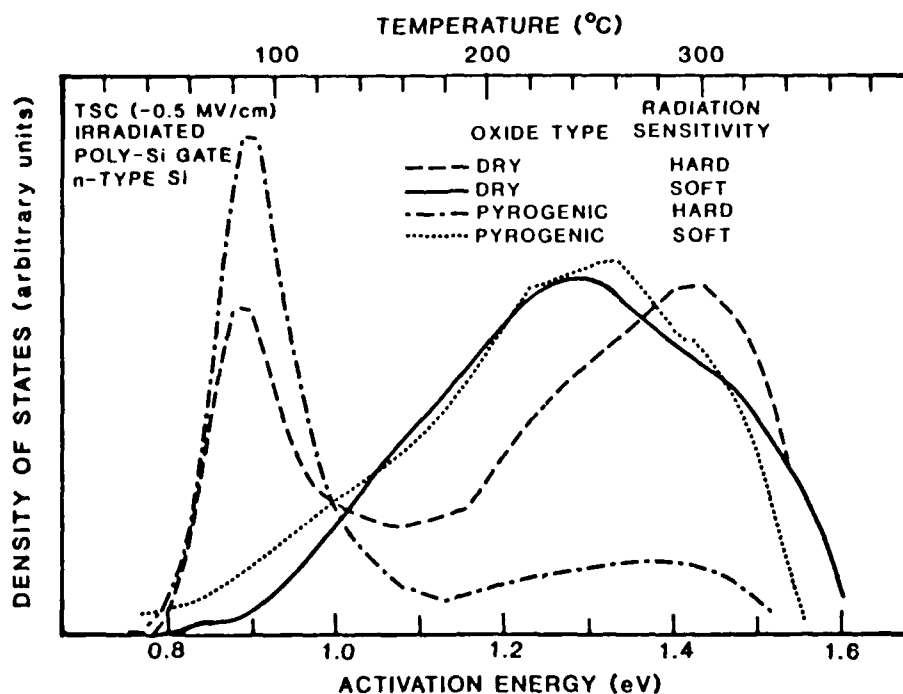
Figure 4.34. A second example of TSC spectroscopy results.

DETERMINATION OF N_{ot}
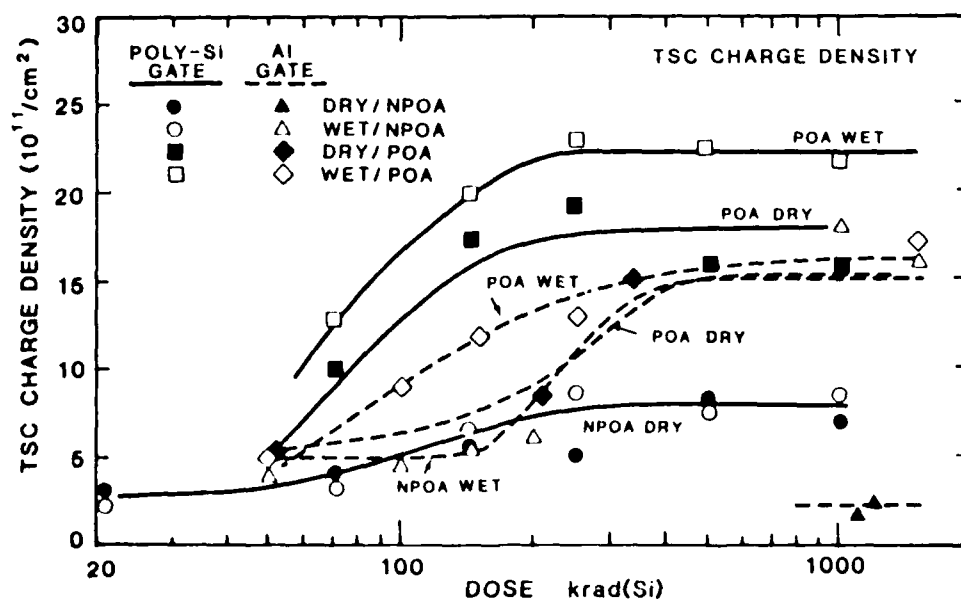
Figure 4.35. Oxide trapped charge versus dose based on TSC measurements.

DETERMINATION OF NET INTERFACE STATE CHARGE DENSITY

$$N_{it}(\psi) = \int_{E_V/q}^{E_C/q} d\zeta \left\{ -\left[f_0(\zeta - \psi) \right] D_{it}^a(\zeta) + \left[1 - f_0(\zeta - \psi) \right] D_{it}^d(\zeta) \right\}$$

$$N_{it}(\psi) = C_{ox} \left(V_{IRRAD}(\psi) - V_{PRE-IRRAD}(\psi) - \Delta V_{TSC} \right) \qquad \Delta V_{TSC} = \frac{Q_{TSC}}{C_{ox}}$$
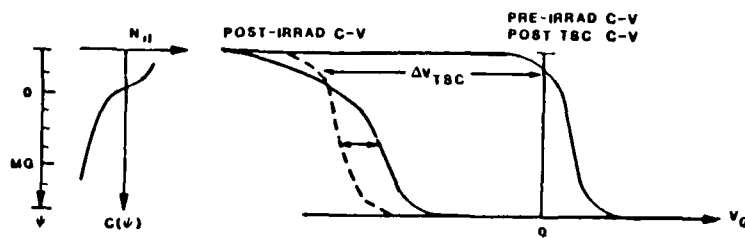
Figure 4.36. Description of the method used to determine N_{it} from TSC and C-V data.

DETERMINATION OF N_{ii}
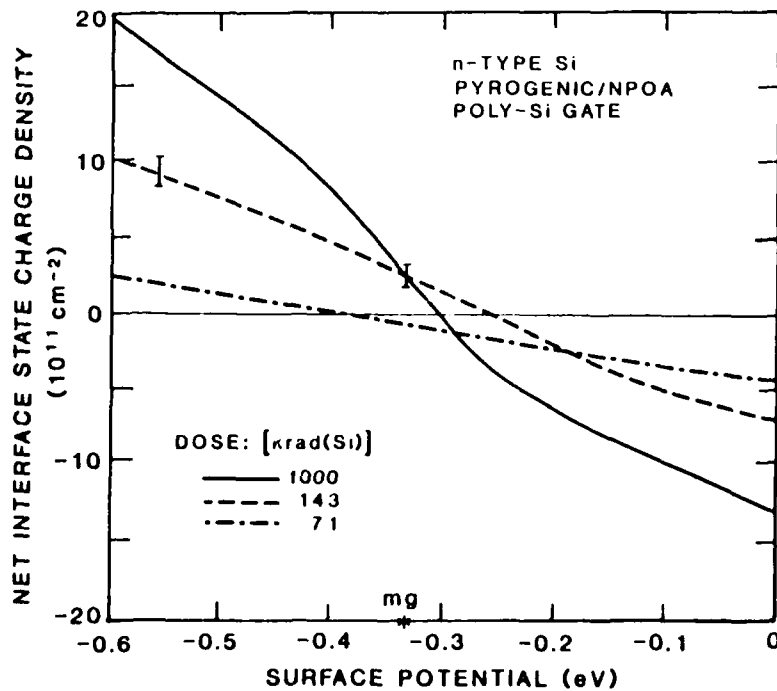
Figure 4.37. Interface state charge density versus surface potential.

DETERMINATION OF N $_{it}$
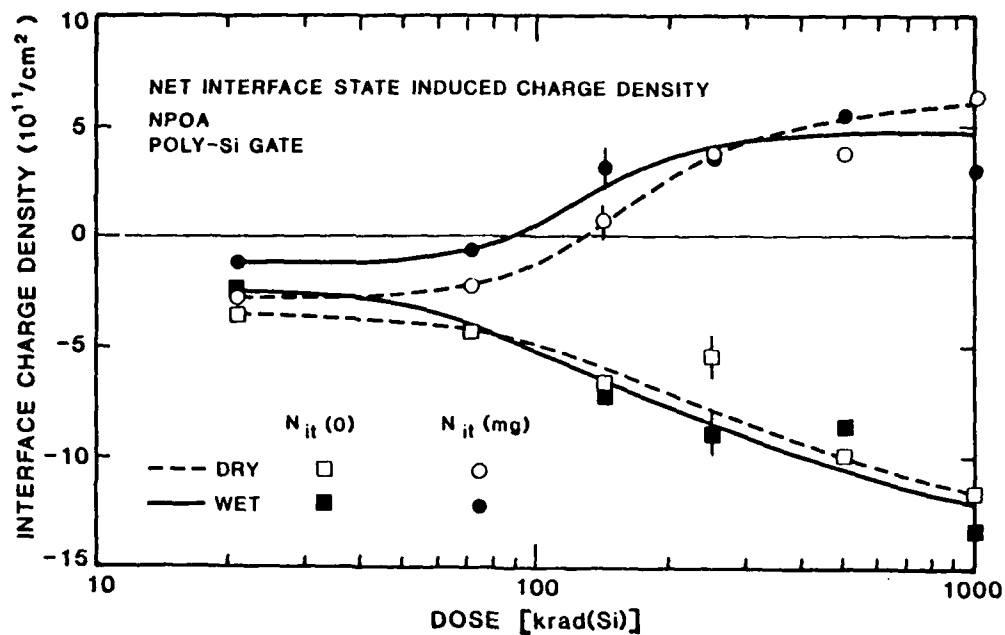
Figure 4.38. Interface state charge density versus dose.

EFFECTS OF PROCESSING ON MOS RADIATION HARDNESS

o Al vs POLY Si GATES

o DRY vs PYROGENIC OXIDES

o NPOA vs POA

o DURATION OF POA

o HIGH TEMPERATURE PROCESSES

o Na IMPURITY EFFECTS

o OXIDATION / POA / OXIDATION

Figure 4.39. Listing of device processing variations that were investigated.
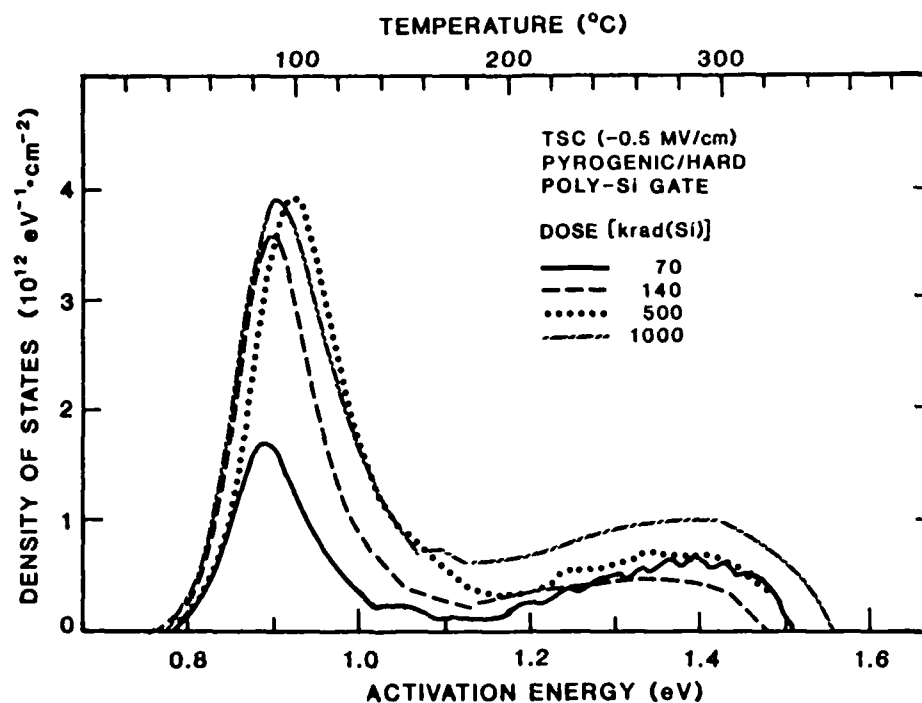
Figure 4.40. TSC spectra for a poly-Si gate MOS capacitor with a pyrogenic oxide for the case of no post-oxidation anneal.
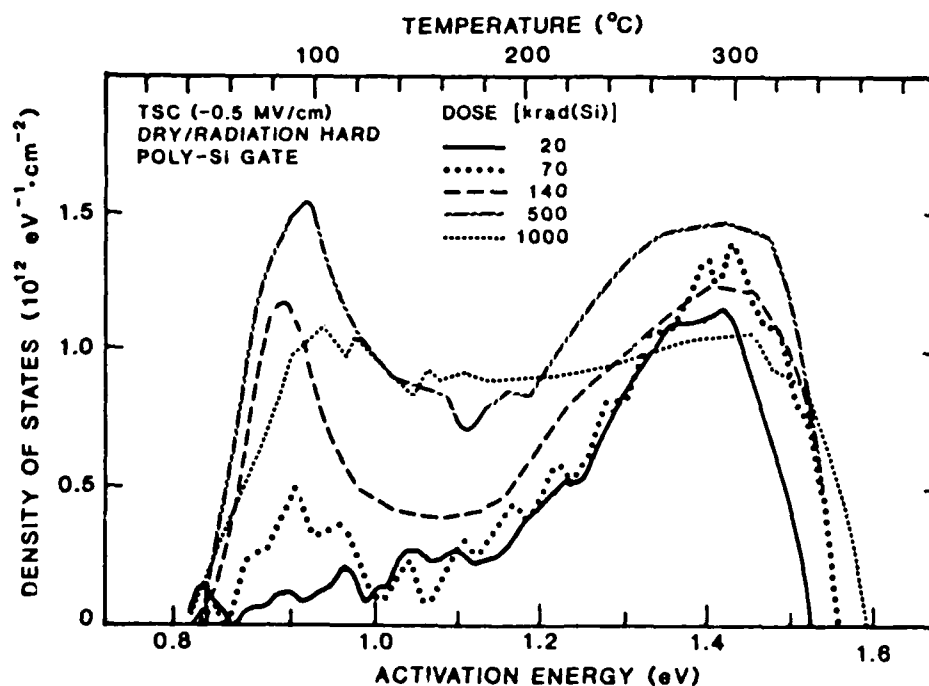
Figure 4.41. TSC spectra for a poly-Si gate MOS capacitor with a dry oxide for the case of no post-oxidation anneal.
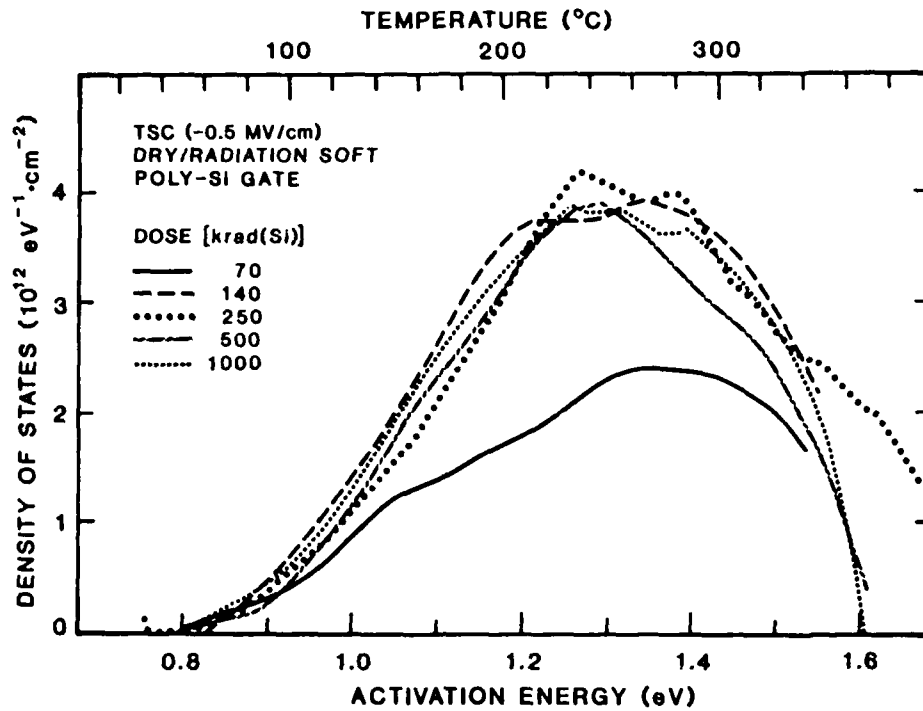
Figure 4.42. TSC spectra for a poly-Si gate MOS capacitor with a dry oxide. A post-oxidation anneal at 1100°C was used.
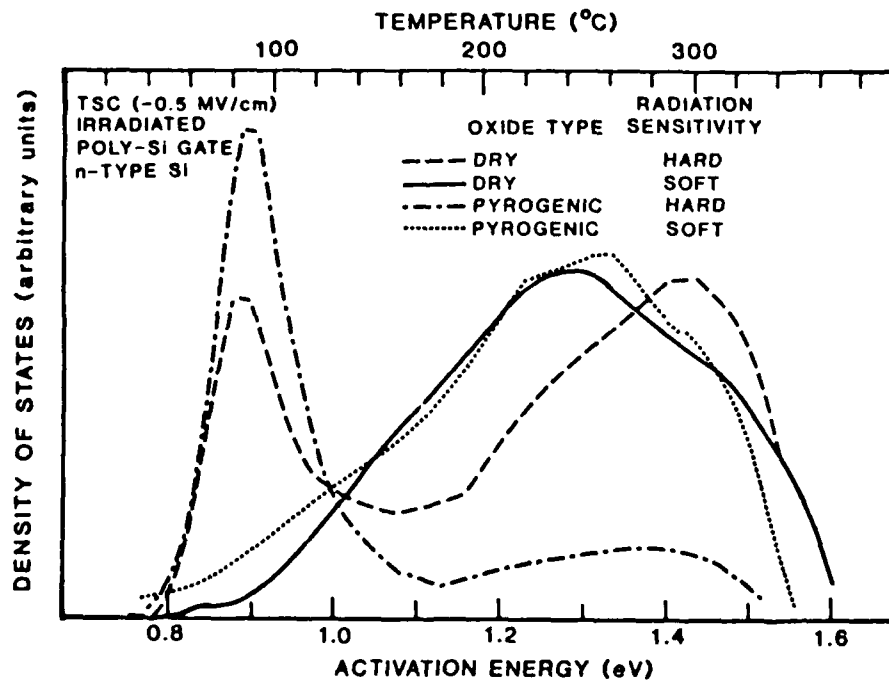
Figure 4.43. Summary of TSC results for irradiated poly-Si gate MOS capacitors.

The change in N_{it} with ionizing radiation is now described. The technique used to determine N_{it} was presented in Figure 4.36. The dependence of N_{it} on dose for NPOA capacitors is shown in Figures 4.46 and 4.47 for poly-Si and Al-gate devices, respectively. Note that N_{it} at midgap (mg) starts out at negative values for low-dose irradiations of poly-Si gate devices. The same effect is observed in Figure 4.48 where N_{it} is plotted versus surface potential. Here the dominant effects of irradiation are the generation of a donor above midgap and introduction of the P_b center. The donor saturates at $\sim$150 krad(Si) while the P_b center density continues to increase with dose. A very different behavior for N_{it} is observed for POA samples, as shown in Figures 4.49 and 4.50. For these devices, the existence of the donor above midgap dominates the radiation response of N_{it}. A model that describes the observed behavior is presented in Figure 4.51. A summary of the results in terms of radiation-induced oxide trapped charge and interface states for the Sandia devices studied is given in Figure 4.52. The dominant processing-related effects are attributed to the presence of H and the use of a POA.
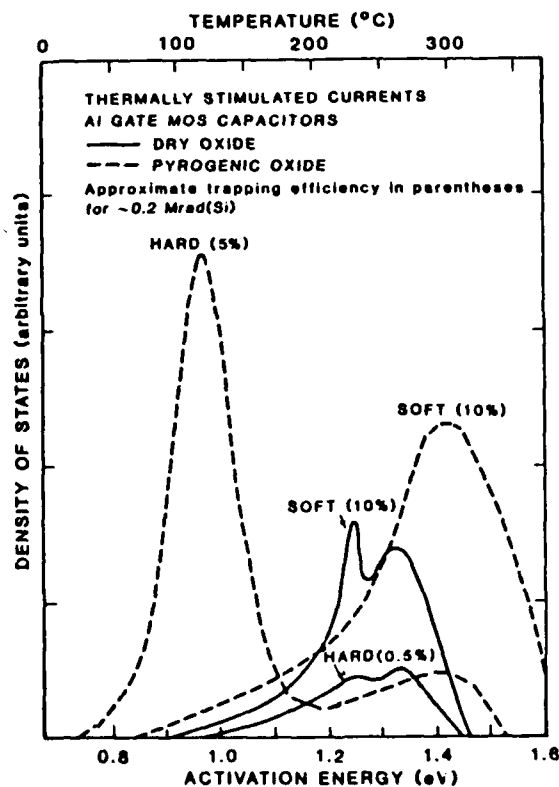
Figure 4.44. Summary of TSC results for irradiated Al-gate MOS capacitors.
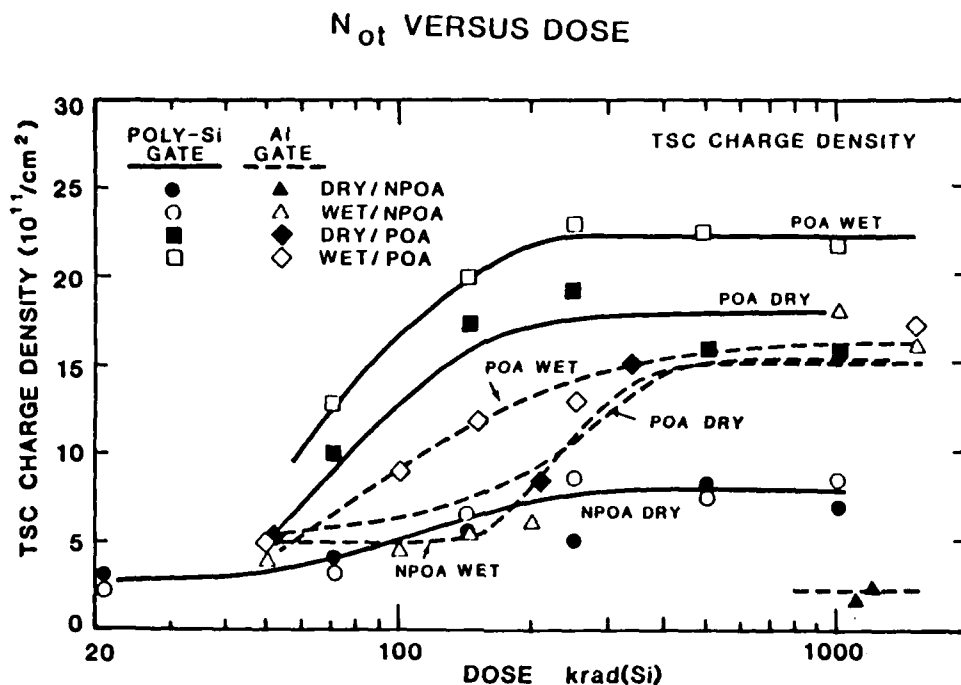
Figure 4.45. Oxide trapped charge versus dose for several types of MOS capacitors.

An additional set of Sandia MOS capacitors that had experienced the complete thermal history required for transistor fabrication was also investigated. (All results presented above were obtained using devices that had experienced the minimum processing necessary to produce capacitors.) Figure 4.53 presents TSC spectra obtained for this additional set of devices. Note the disappearance of the 0.9-eV peak after the TEOS intermediate dielectric densification. The corresponding N_{it} information is shown in Figures 4.54 and 4.55 for devices that experienced processing steps C and D. A summary of N_{it} data obtained at a relatively high dose is given in Figure 4.56 for all processing steps.

The effect of POA duration on the radiation response of MOS capacitors fabricated by Texas Instruments (TI) is shown in Figures 4.57 and 4.58. The TSC spectra reveal that a longer POA increases the 1.25-eV peak with respect to the 1.35-eV peak.

N it VERSUS DOSE
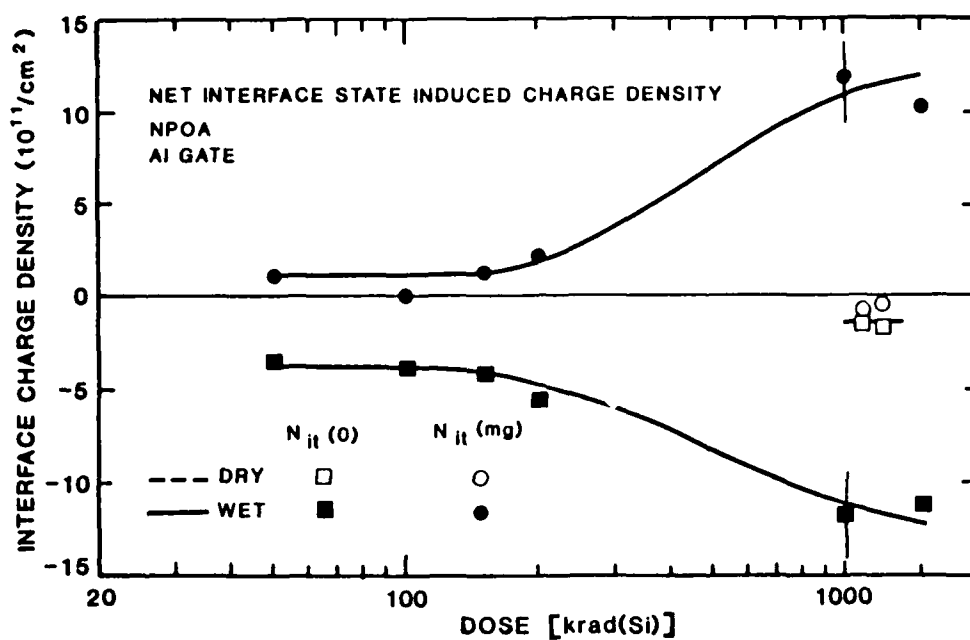
Figure 4.46. Net interface charge density versus dose for the case of NPOA Al-gate MOS capacitors.

N it VERSUS DOSE
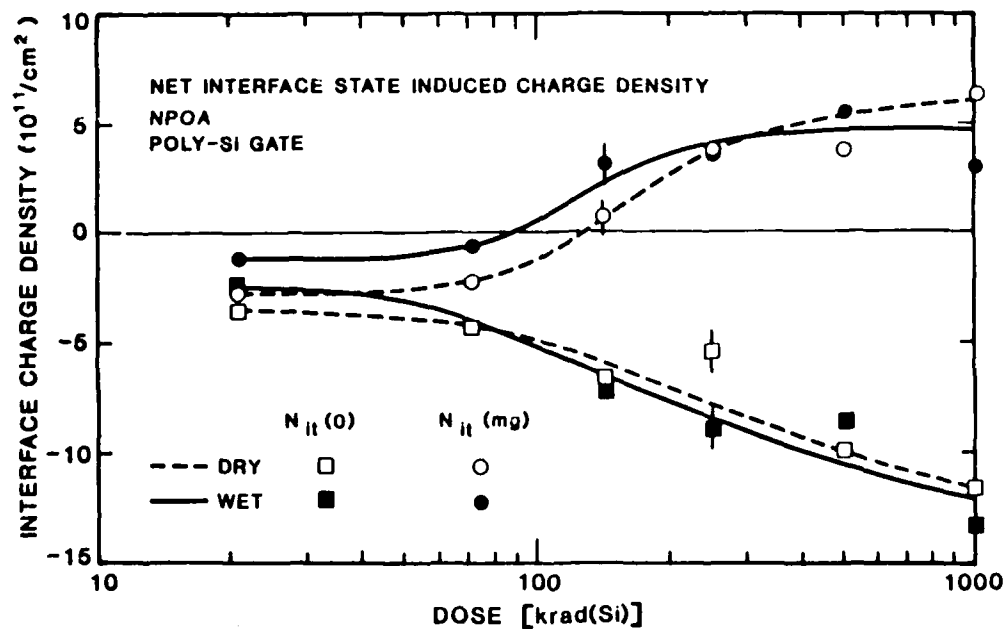
Figure 4.47. Net interface charge density versus dose for the case of NPOA poly-Si gate MOS capacitors.
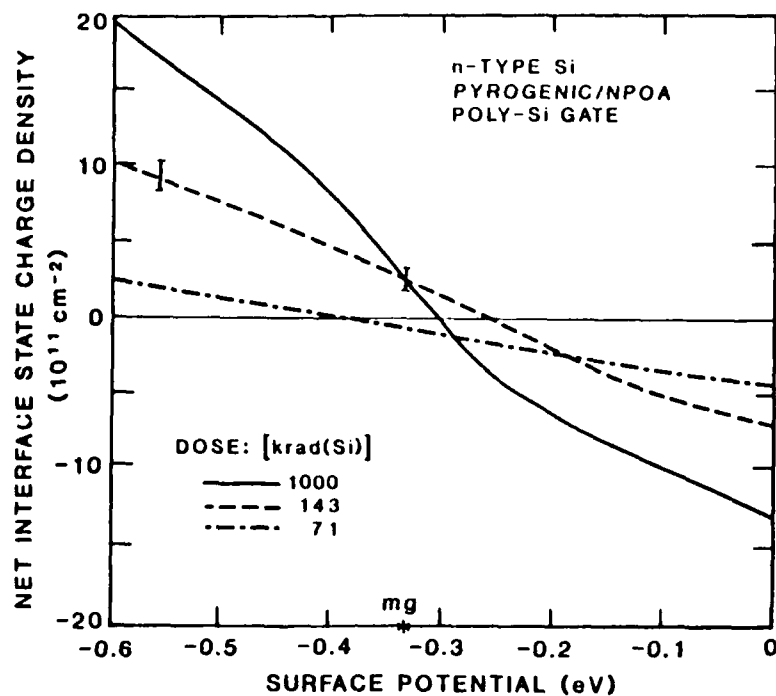
Figure 4.48. Net interface charge density versus surface potential for a NPOA poly-Si gate device irradiated to several dose levels.

N$_{it}$ VERSUS DOSE
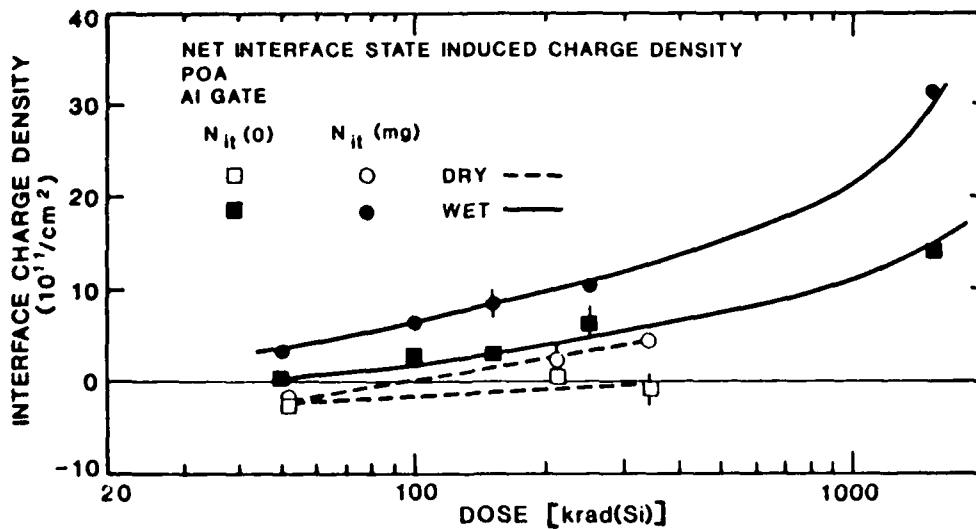
Figure 4.49. Net interface charge density versus dose for the case of POA Al-gate MOS capacitors.
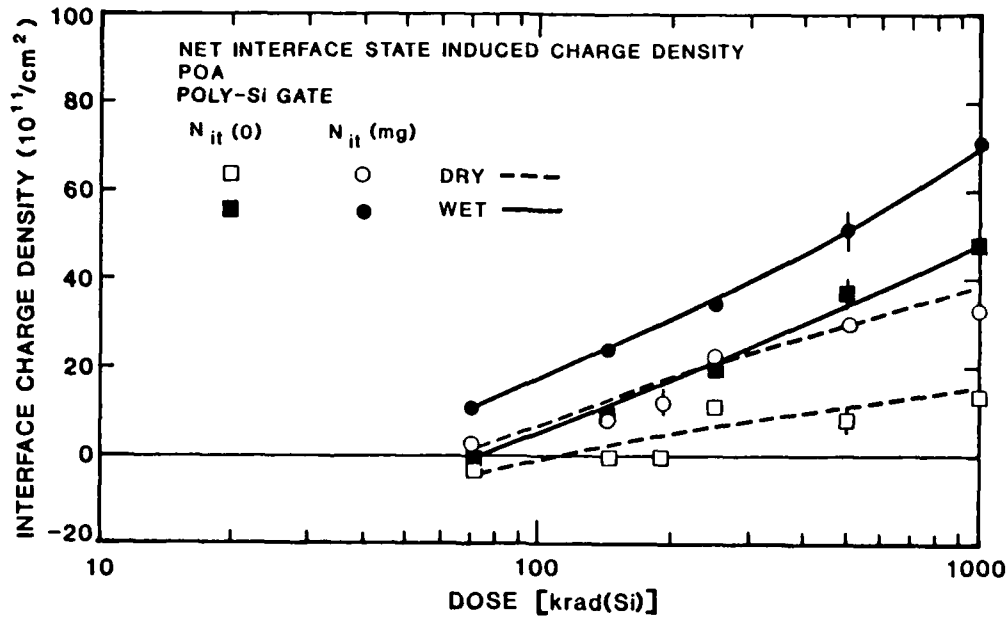
Figure 4.50. Net interface charge density versus dose for the case of POA
poly-Si gate MOS capacitors.

In both cases, the donor dominates N$_{it}$ (Figure 4.58). Note that these capacitors were fabricated on p-type Si.

The effects of reoxidation of the interface are presented in Figures 4.59 through 4.61 for devices fabricated at TI. Oxides were grown to 500 Å using ultra-dry oxygen. Those grown continuously are labeled "one-step". Those that were first grown to 250 Å, then received a POA for 5 hours at 1000°C, and then had an additional 250 Å grown are labeled "two-step". As shown by Figures 4.57, 4.59, and 4.60, the effect of the POA on the 0.9-eV peak is eliminated by the reoxidation. Differences in the high-energy portion of the TSC spectra are not completely eliminated. Although only the "one-step" N$_{it}$ is shown in Figure 4.61, approximately the same curves are obtained for the "two-step" case. Note that for these "NPOA" samples, an acceptor interface state is present below midgap.

PROPOSED INTERFACE STATE MODEL

Relative magnitude of each type depends on device processing and dose

ENERGY
(eV)
1.12 E_c $D_{it}(E)$

INV

II

I

0.56   MG — — — — — — — —

I

FB

III

0   E_v
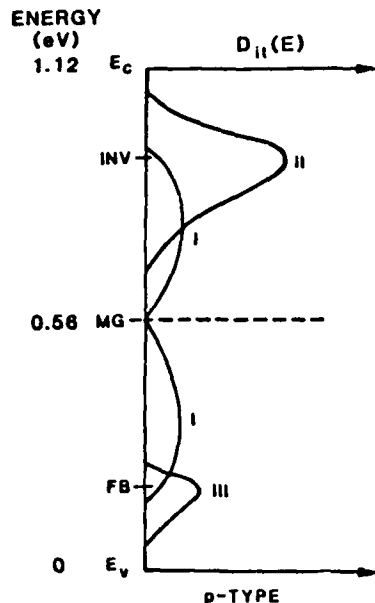
p-TYPE

TYPES OF INTERFACE STATES

I P_b CENTER

     Acceptor above midgap
     Donor below midgap

II   DONOR ABOVE MIDGAP

     Extends towards E_c
     Dominates at high dose and POA

III   ACCEPTOR NEAR FLATBAND

     Dominates at low and intermediate
     doses
     Observed for p-type Si

Figure 4.51. Illustration of a proposed model that accounts for radiation-
induced interface states.

A summary of the spectroscopy of oxide trapped charge and interface states is given in Figure 4.62. The role of hydrogen and high-temperature POA's is critical in determining the radiation response of MOS devices.

Evaluation of the validity of the midgap technique for determining N_{ot} is now presented. Specifically, we evaluated whether $C_{ox}\Delta V(mg)$ is, in general, equal to N_{ot} for devices fabricated on (100) silicon. To do this, N_{ot} was measured directly and compared with $C_{ox}\Delta V(mg)$. In addition, we attempted to determine whether interface states other than P_b centers exist. Our objectives also included determining under what conditions results from the midgap technique may give reasonable approximations to N_{ot} even if the underlying assumptions are not completely correct. The experimental approach is presented in Figure 4.63. Two fundamental tests of the midgap technique were applied in this study: (1) comparison of N_{ot} obtained from TSC measurements with $C_{ox}\Delta V(mg)$, and (2) determination of the types of interface states in the Si bandgap and comparison with the types assumed in the model of the P_b center. Test 1 assumes that the TSC technique determines N_{ot} accurately without either excess or insufficient current. This

PROCESS EFFECTS

Sandia Devices

Process	Oxide Trapped Charge	Interface States
DRY OXIDE		
Al gate NPOA	1.25 eV, 1.35 eV peaks	?
POA	above peaks increase	Pb saturates; donor dominates at high dose
Poly Si-gate NPOA	0.9 eV small	
	1.4 eV saturated ($>$ 20 krad(Si))	P_b dominates; donor saturates
POA	broad peak 0.8 - 1.6 eV	P_b saturates; donor dominates at high dose
PYROGENIC OXIDE		
Al gate NPOA	0.9 eV large	P_b dominates; donor saturates
POA	broad peak 0.8 - 1.6 eV	P_b saturates; donor dominates at high dose
Poly Si-gate NPOA	0.9 eV large	
	1.4 eV not saturated	P_b dominates; donor saturates
POA	broad peak 0.8 - 1.6 eV	P_b saturates; donor dominates at high dose

Figure 4.52. Summary of oxide-trapped-charge and interface-state results for devices fabricated using several processing approaches.

issue was addressed in the discussion of Figure 4.36. Test 2 examines whether any other interface states exist that are not P_b centers. If so, the underlying assumption of the midgap technique is compromised.

Results of Test 1 are given in Figure 4.64 for a large number of fabrication processes. In Figure 4.65 the fractional deviation of $C_{ox}\Delta V(mg)$ from N_{ot} is shown. Note that most of the deviations are less than 100%. Devices that have experienced some form of high-temperature POA deviate the most, with the deviation being positive. Positive deviations imply that a donor state exists above midgap, while negative deviations imply the existence of an acceptor below midgap. In many cases, depending on the process and dose, both negative and positive deviations occur.

Results of interface state density measurements (Test 2) using both the C-V technique (Terman analysis) and the conductance technique are given in Figure 4.66. The agreement between conductance measurements and Terman analysis is reasonably

TSC SPECTRA AT 4.4 Mrad(Si)
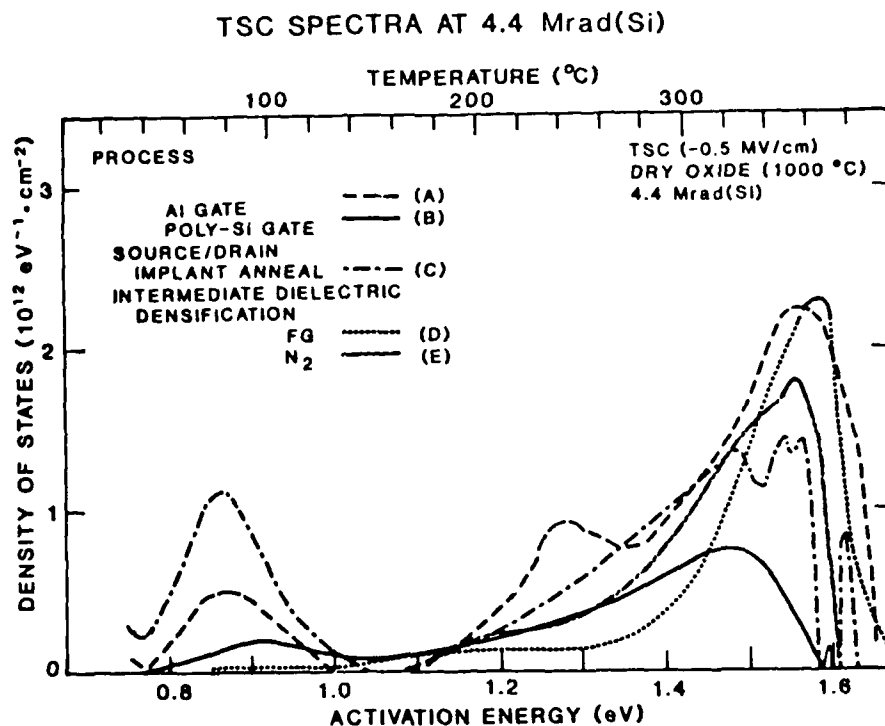
Figure 4.53. TSC spectra for MOS capacitors that had experienced the thermal history required in transistor fabrication.

good. Note the limited range of surface potential accessible by the conductance technique. Two types of data are plotted in Figure 4.67 for the same device used to obtain the data of Figure 4.66. The solid curve represents the N_{it} determined from combining the TSC and C-V data. In the limited range of surface potential shown (above midgap and below flatband), the dominant interface state is a donor. The decrease in surface potential fluctuations (solid dots) determined from conductance measurements also reveals independently that donor interface states dominate in this region of the bandgap. Thus, for this sample, both techniques show that interface states exist other than those associated with the P_b center.

We now present results of C-V measurements on a different sample which are inconsistent with assuming that P_b centers are the only interface states and that they contribute to the TSC current. Figure 4.68 shows the results of C-V measurements and Figure 4.69 shows interface state density D_{it} obtained from Terman analysis. Figure 4.70 presents the argument. The bias applied during the TSC measurement places the surface potential above midgap. If only P_b centers exist, the net interface state charge would then be negative. If these negatively charged interface states contribute to the

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SURFACE POTENTIAL DEPENDENCE OF N_{it} FOR PROCESS C
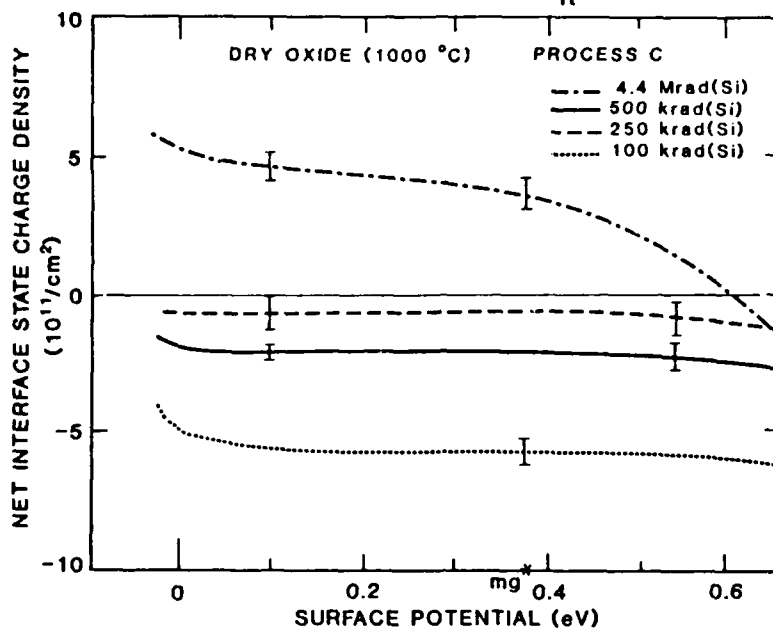
Figure 4.54. Net interface state charge density versus surface potential for MOS capacitors that experienced processing step C.

SURFACE POTENTIAL DEPENDENCE OF N_{it} FOR PROCESS D
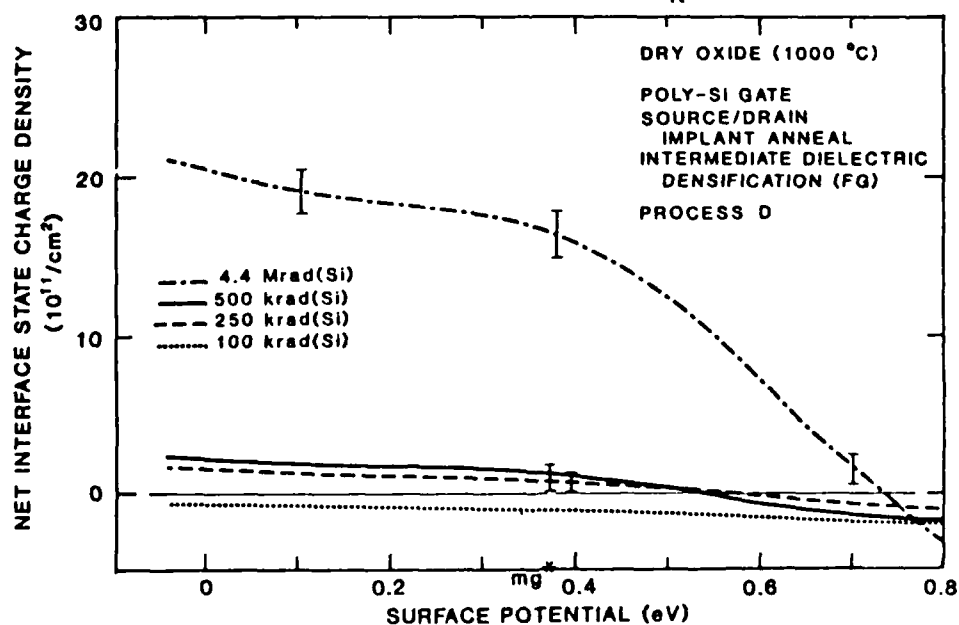
Figure 4.55. Net interface state charge density versus surface potential for MOS capacitors that experienced processing steps C and D.

SUMMARY OF PROCESS DEPENDENCE OF N_{it}
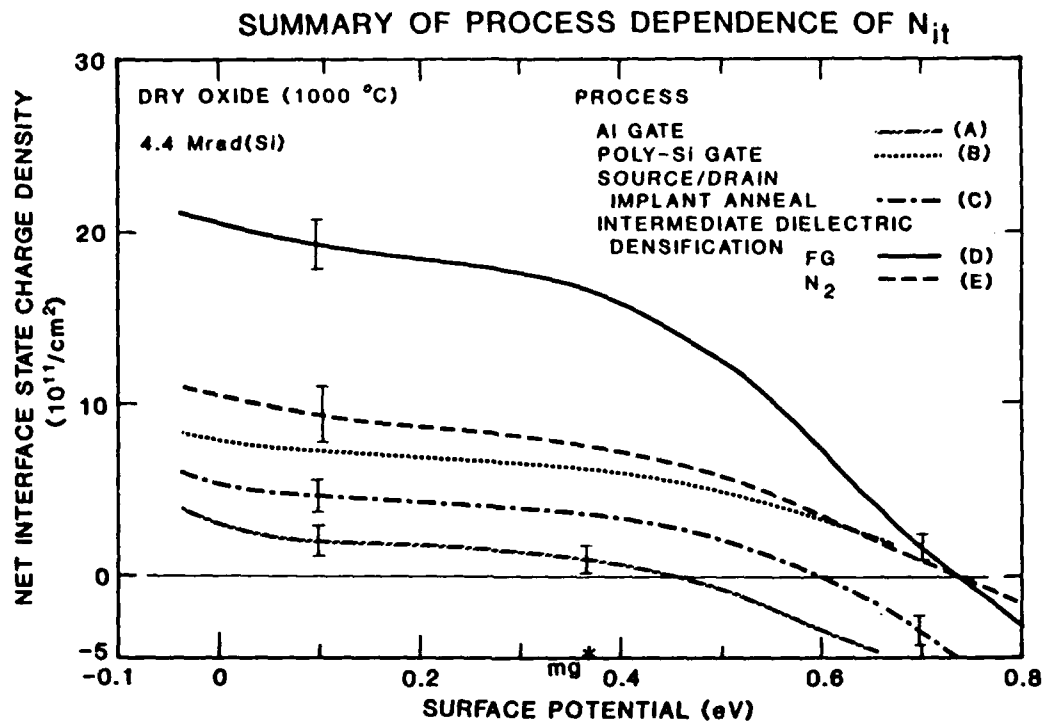
Figure 4.56. Summary of the device processing dependence of the net interface state charge density after exposure to 4.4 Mrad(Si).

EFFECTS OF POA DURATION
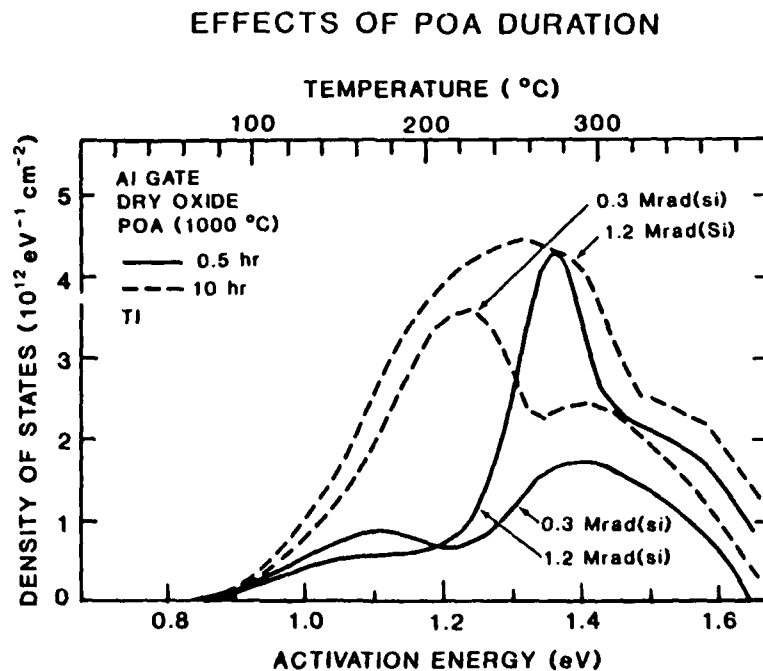
Figure 4.57. TSC spectra for two radiation doses and two POA times at 1000°C.

TEXAS INSTRUMENTS DRY OXIDE POA (1000°C) 0.5 hr NPMA
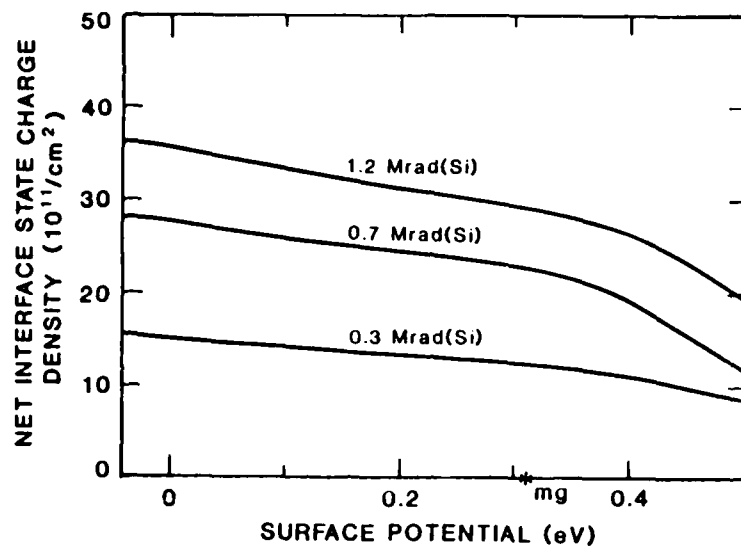
Figure 4.58. Net interface state charge density versus surface potential for a TI device that received a 0.5-h POA.
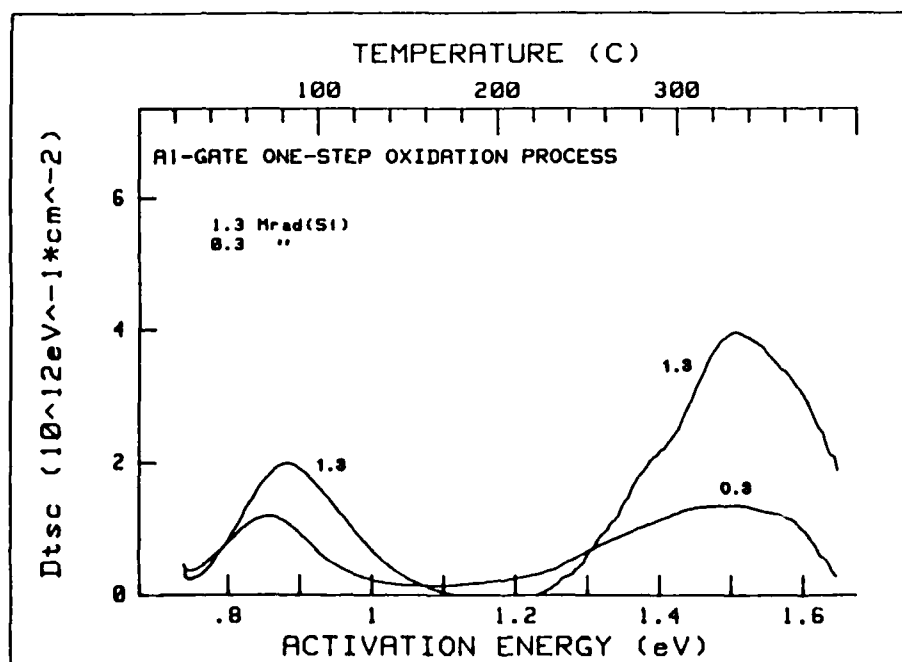
Figure 4.59. TSC spectra for an Al-gate MOS capacitor with a continuously grown 500-Å oxide.

4-38
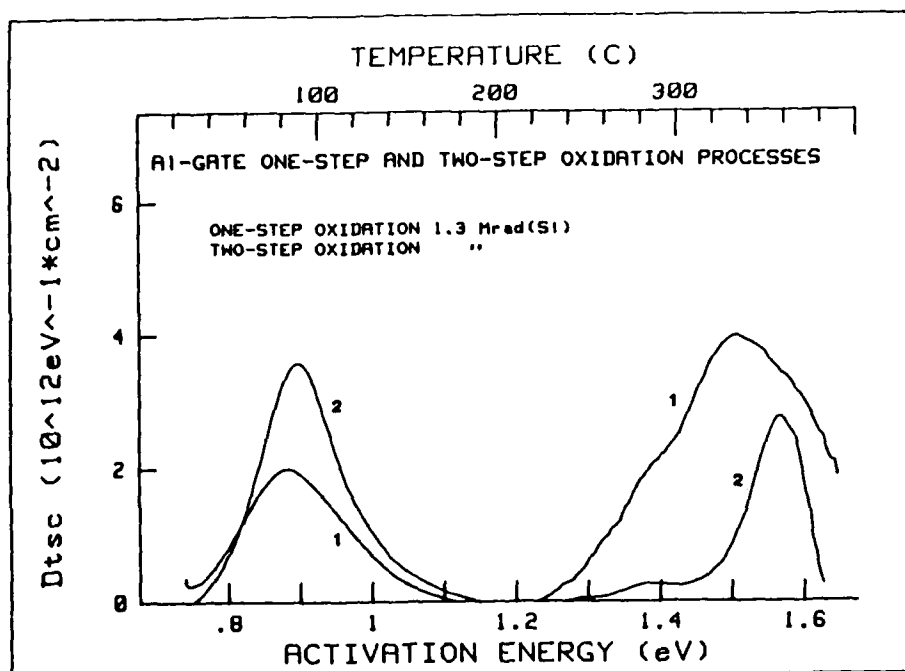
Figure 4.60. TSC spectra for Al-gate MOS capacitors fabricated using one-step and two-step oxidation processes, as defined in the text.
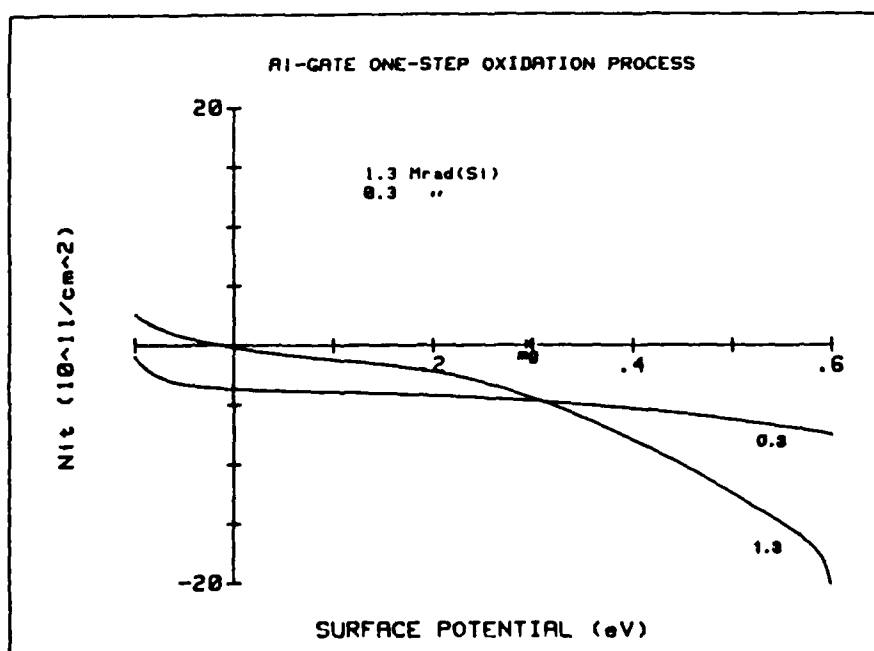
Figure 4.61. Interface state density versus surface potential for an irradiated Al-gate MOS capacitor fabricated using a one-step oxidation process.

SPECTROSCOPY CONCLUSIONS

o VARIOUS RADIATION-INDUCED OXIDE HOLE TRAP SITES EXIST WHICH DEPEND ON PROCESSING

o THREE DIFFERENT TYPES OF RADIATION-INDUCED INTERFACE STATES EXIST WHICH DEPEND ON PROCESSING

    DONOR INDUCED BY HIGH TEMPERATURE POA

o ROLE OF HIGH TEMPERATURES AND HYDROGEN CRITICAL

    POA: DONOR INTERFACE STATE DOMINATES. "PRECURSOR" OXIDE HOLE TRAP. HIGH TEMPERATURE EFFECTS CUMULATIVE?

    HYDROGEN: ROLE OF H IN GENERATING DONOR INTERFACE STATE NOT RESOLVED. INTERACTS WITH "PRECURSOR" OXIDE HOLE TRAPS.

o Na INDUCES HOLE TRAP SIMILAR TO THAT INTRODUCED BY HYDROGEN

o DIFFERENT PROCESS LINES PRODUCE DIFFERENT RESULTS

Figure 4.62. Summary of conclusions made based on oxide-trapped-charge and interface-state measurements.

EXPERIMENTAL APPROACH

o DETERMINE N_{ot} FROM THERMALLY STIMULATED CURRENT (TSC) MEASUREMENTS

o COMPARE TO ΔV(mg) FROM C-V MEASUREMENTS

o DETERMINE N_{it} FROM TSC/C-V MEASUREMENTS

o DETERMINE D_{it} FROM C-V (TERMAN) AND G-V MEASURMEMENTS

o DETERMINE DOMINANT TYPE OF INTERFACE STATES AT VARIOUS SURFACE POTENTIALS FROM TSC/C-V AND G-V MEASUREMENTS

Figure 4.63. Experimental approach used in evaluating the validity of the midgap technique for determining N_{ot}.

TSC signal, the signal would increase so that Q_{TSC} would be larger than $C_{ox}\Delta V$(mg), which contradicts the observed behavior.

Conclusions of this study of the validity of the midgap technique are the following: (a) $C_{ox}\Delta V$(mg) $\neq N_{ot}$, with the deviation usually being within 100% (except for
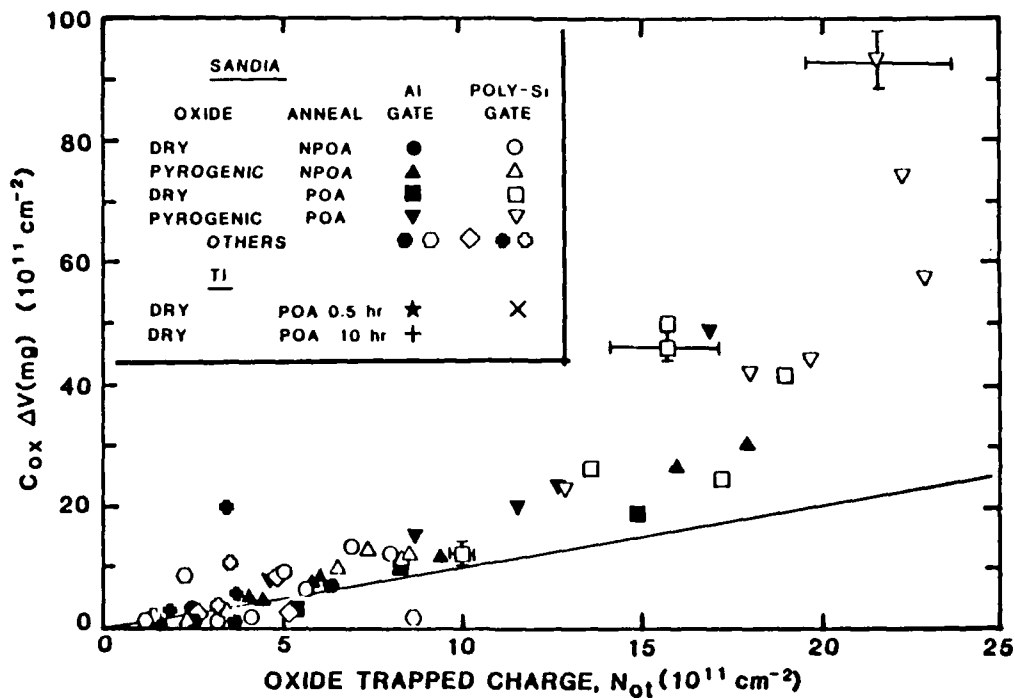
Figure 4.64. Comparison of TSC measurements of N_{ot} with those obtained using the voltage shift at midgap for devices fabricated using several processing variations.

devices that experienced a POA); (b) there is no universal surface potential for $N_{it} = 0$; (c) various types of hole traps exist in the oxide and at the interface, and the relative magnitudes of each depend on device processing and dose; (d) the utility of the midgap technique depends on the application. In addition, the assumption that P_b centers are the only interface states is not correct. From a practical viewpoint, the most important point is that the utility of the midgap technique needs to be evaluated for each application. If a possible error within a factor of 2 is acceptable for radiation-hardened devices, the midgap technique is a convenient measurement approach.

A number of outstanding issues related to total dose effects on MOS devices are listed in Figure 4.71. Other issues can certainly be added, and many of the issues listed are being addressed at present by various workers. Finally, a summary of key results obtained in the present investigation of MOS devices is presented in Figure 4.72.
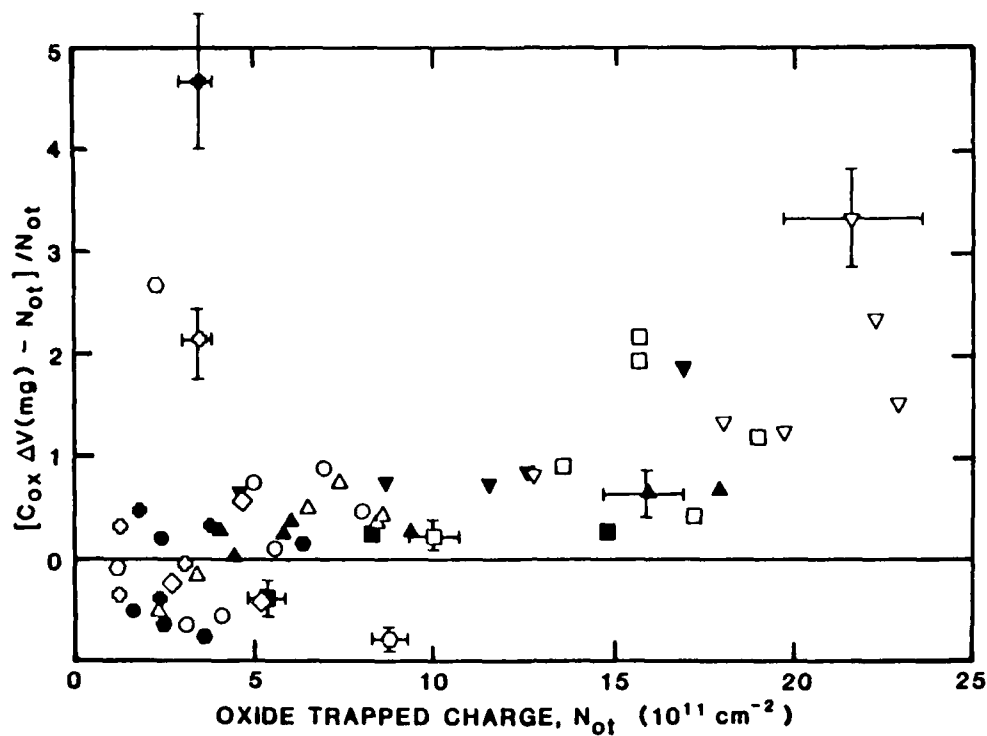
Figure 4.65. Fractional deviation of $C_{ox}\Delta V(mg)$ from N_{ot} (determined using TSC) versus N_{ot}.
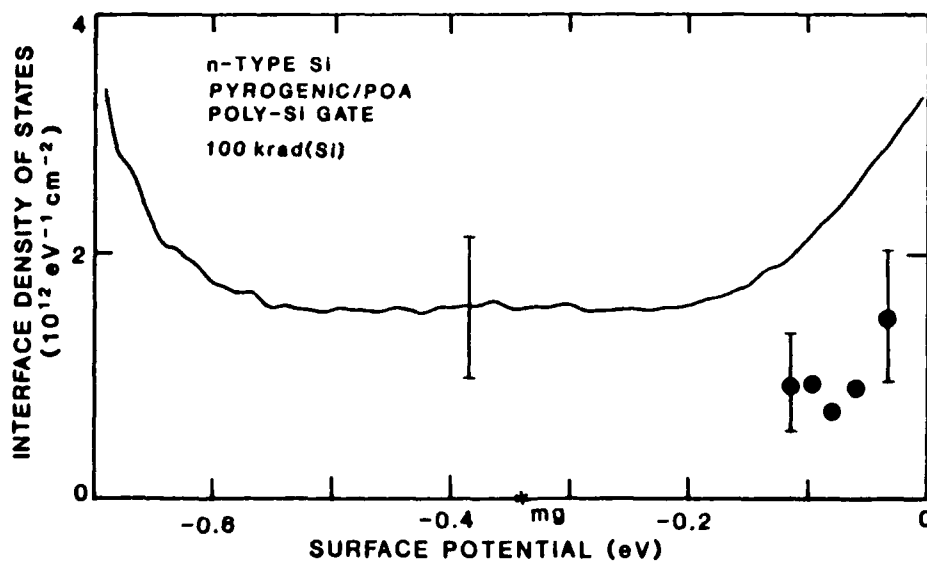
Figure 4.66. Comparison of interface state measurements made by the C-V, or Terman, technique (solid line) and the conductance technique (solid dots) on an irradiated MOS capacitor.
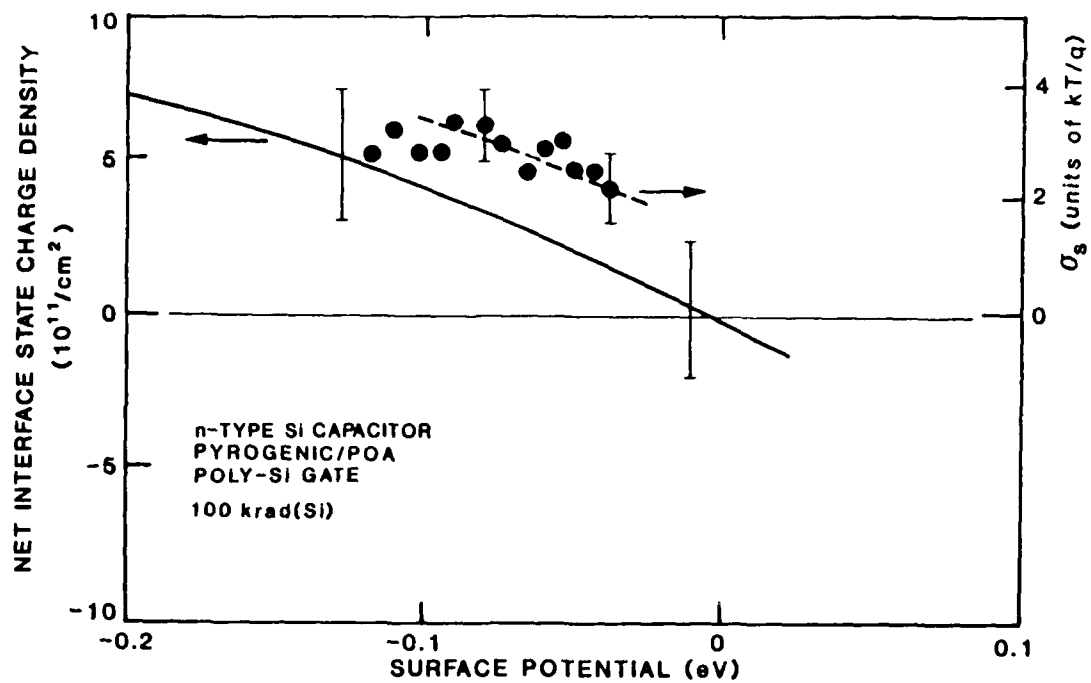
Figure 4.67. Interface state density determined from TSC and C-V data (left scale, solid line) and surface potential fluctuations (right scale, solid dots) versus surface potential.
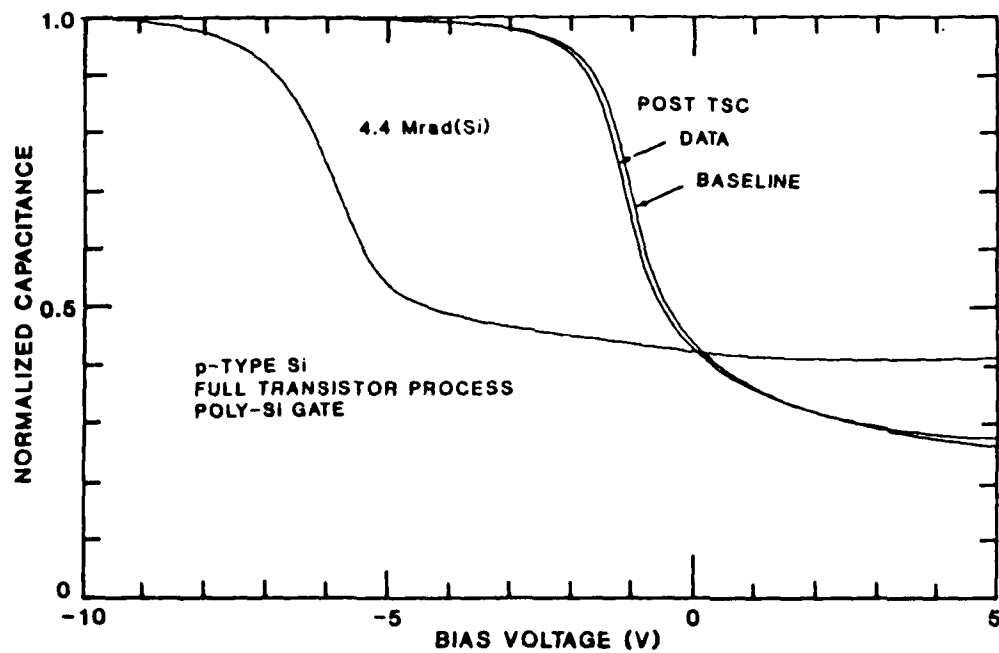
Figure 4.68. C-V data for an MOS capacitor after irradiation and after TSC measurements.
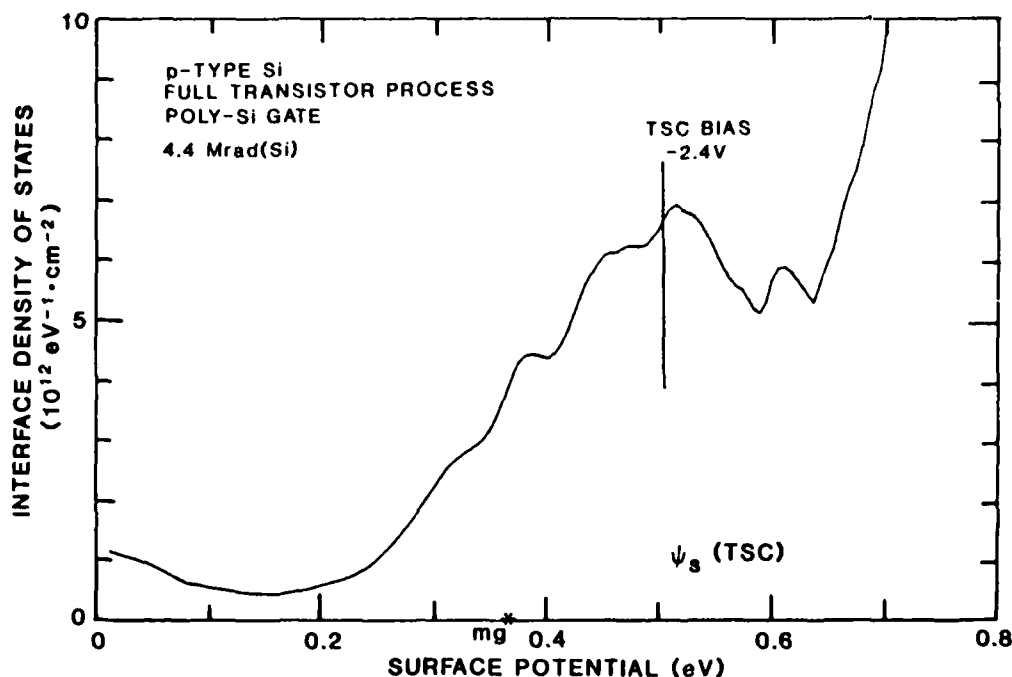
Figure 4.69. Interface state density vs surface potential for an irradiated MOS capacitor based on Terman analysis.

DATA INCONSISTENT WITH THE EXISTENCE OF ONLY P_b INTERFACE STATES

o $C_{ox}\Delta V(mg) = 19.3 \times 10^{11}$ /cm^2

   $Q_{TSC} = 3.4 \times 10^{11}$ /cm^2

o ASSUMPTIONS

   IF P_b CENTERS ONLY INTERFACE STATES THEN D_{it} FOR $\psi_s > \psi_{mg}$ ACCEPTORS

   INTERFACE STATES CONTRIBUTE TO Q_{TSC}

o DURING TSC ψ_s MOVES FROM ~0.5eV TOWARDS mg SO ELECTRONS RELEASED - WOULD INCREASE Q_{TSC}

o BANDBENDING SUCH THAT ELECTRONS CANNOT FLOW AWAY FROM SI - SiO_2 INTERFACE

Figure 4.70. Reasoning which leads to the conclusions that interface states exist in addition to the P_b center and that interface states do not contribute to the TSC charge for irradiated MOS capacitors.

MOS ISSUES

- RELATION BETWEEN ACTIVATION ENERGIES AND STRUCTURAL SITES AND IMPURITIES

- NATURE OF THE 0.9-eV PEAK. IS IT AN INTRINSIC DEFECT?

- ROLE OF H IN INTERFACE STATE FORMATION AND INFLUENCE ON DONOR GENERATION

- CONDITIONS FOR GENERATION OF THE ACCEPTOR INTERFACE STATE

- NATURE OF LOW-TEMPERATURE/FAST-GENERATION INTERFACE STATES

- EFFECTS OF TYPES AND DENSITY OF INTERFACE STATES ON CHANNEL MOBILITY

- NATURE OF INTERFACE STATES NEAR BAND EDGES

- DOSE RATE DEPENDENCE OF INTERFACE STATE INDEPENDENT OF N_{ot} "ANNEAL" EFFECTS

- NATURE OF THE "PRECURSOR" OXIDE CHARGE TRAP SITE GENERATED DURING POA

- CONNECTION BETWEEN Q_f GENERATED DURING PROCESSING AND Q_{ot} GENERATED BY IONIZING RADIATION

- RELATIONSHIP BETWEEN ROOM TEMPERATURE ANNEALING (TUNNELING MODEL) AND HIGH TEMPERATURE ANNEALING

    LONG-TERM VERSUS SHORT-TERM ANNEALING

    LOCATION OF CHARGE VERSUS ACTIVATION ENERGIES

    ROLE OF IMPURITIES IN NEUTRALIZING OXIDE TRAPPED CHARGE

- CONNECTION BETWEEN TSC RESULTS ON CAPACITORS WITH MOSFETS

- CRYSTAL ORIENTATION EFFECTS

- ACTUAL PROCESS DIFFERENCES OF DIFFERENT FABRICATION LINES

- EFFECTS OF RADIATION ON DEVICE RELIABILITY

    CHARGE TRAPPING NEAR GATE ELECTRODE

    EFFECTS OF OTHER STRESSES

    ELECTRON TRAPPING IN BULK

- FIELD OXIDES — SAME ISSUES AS FOR GATE OXIDES

- EFFECTS IN SEVERE RADIATION ENVIRONMENTS

- EFFECTS OF INTENTIONAL IMPURITIES IN GATE OXIDES — HCL, F

- MECHANISM FOR SATURATION OF HOLE TRAPS IN THE OXIDE

Figure 4.71. Issues that need to be addressed in studies of the mechanisms of ionizing radiation effects on Si MOS devices.

MOS SUMMARY

○ VARIOUS OXIDE HOLE TRAP SITES EXIST WHICH ARE PROCESS AND DOSE DEPENDENT

○ THREE DIFFERENT TYPES OF INTERFACE STATE EXIST WHICH ARE PROCESS AND DOSE DEPENDENT

○ QUANTITATIVE EVALUATION OF THE CRITICAL ROLE OF "HIGH" TEMPERATURE AND HYDROGEN ON RADIATION RESPONSE NOW POSSIBLE

○ DETERMINED LIMITATIONS OF THE MIDGAP TECHNIQUE FOR DETERMINING N_{ot}

○ NOMINALLY SIMILAR PROCESSES ON DIFFERENT FABRICATION LINES ARE SHOWN TO BE DIFFERENT IN TERMS OF THEIR RADIATION RESPONSE

Figure 4.72. Summary of key results obtained in the present investigation of the mechanisms of ionizing radiation effects on Si MOS devices.

SECTION 5

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APPENDIX A

Charge Collection Measurements on GaAs Devices
Fabricated on Semi-Insulating Substrates*

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ABSTRACT

Results of charge collection measurements on technologically important GaAs devices fabricated on semi-insulating (SI) substrates are described. Data are presented which suggest that charge funneling in SI GaAs is relatively unimportant compared to that which occurs in semiconducting silicon and GaAs. A qualitative comparison is made of charge collection in silicon and SI GaAs devices to examine their relative susceptibility to single-event upset.

INTRODUCTION

The inherent radiation tolerance of GaAs integrated circuits is well known.[1,2] However, the area of single-event upset in such circuits has only recently been addressed.[3,4] In previous work,[3] results of measurements on GaAs devices bombarded with single alpha particles were presented which revealed the important roles that charge funneling and recombination play in the charge collection process for devices fabricated using semiconducting material. The term charge funneling[5-8] refers to the redistribution of the potential present at a sensitive node (typically a reverse-biased junction) along the ion track, thereby causing a larger amount of charge to be collected by drift. This effect increases the susceptibility of a circuit to single-event upset. Another important mechanism in GaAs is recombination. Typical low-injection-level minority-carrier lifetimes are on the order of 10^{-8} sec. Hence, in examining charge collection processes in the nanosecond time regime, recombination must be considered.

In this paper, results of charge collection measurements on technologically important GaAs devices fabricated on semi-insulating (SI) substrates are described. Data are presented which suggest that charge funneling is relatively unimportant compared to that which occurs in semiconducting Si and GaAs. A qualitative comparison is made of charge collection mechanisms in devices fabricated using Si, semiconducting GaAs, and SI GaAs.

EXPERIMENTAL PROCEDURES

The devices used in this study include Schottky-barrier and pn-junction diodes fabricated on both Cr-doped and undoped SI substrates. Devices were fabricated at Northrop and at McDonnell-Douglas. The Northrop devices (Figure 1a) are Au—n-type GaAs Schottky-barrier diodes. These diodes contain an epi layer grown on a SI Cr-doped substrate. An ohmic contact was made to the epi layer by indium solder. The McDonnell-Douglas test structure is shown in Figure 1b.[9] This device is a pn-junction diode formed by ion implantation into an undoped SI GaAs substrate. The n region was formed by a Si[+] implant; Mg[+] ions were used for the p[+] doping. The ohmic contact to the n[+] region is AuGeNi with an Au overlay, while the p[+] region contact is Pt with an Au overlay.[9]

For both sample configurations, charge collection measurements were made under bias (with substrates

floating) following a single alpha event. The experimental configuration[3] is shown in Figure 2. A Cm[244] thin-foil source was used to bombard the devices. The source was collimated and placed ~9 mm from the device under test, so that near-normal incidence was achieved. This source emits primarily 5.8-MeV alpha particles which degrade to ~5.0 MeV before entering the GaAs due to the slight air gap and the metal electrode. (The Au thickness of 0.2 μm for Northrop devices degrades the particle energy by ~0.1 MeV; the amount of degradation is approximately the same for the McDonnell-Douglas devices.) The current pulse resulting from a single alpha event is integrated by the sum of the device capacitance and the input capacitance of the Tektronix P6201 FET probe.[3] This probe has unity gain and a 1-GHz bandwidth. The system mainframe is a Tektronix 7912AD transient digitizer with a bandwidth of 500 MHz. The overall system risetime (10 to 90%) is ~0.8 ns. In practice, measurements are system-bandwidth-limited for times <1.2 ns after the alpha strike. For the McDonnell-Douglas devices, where the measured signal is relatively small, a 5-GHz-bandwidth amplifier with 20-db gain was inserted between the FET probe and the system mainframe. This bandwidth is sufficiently high that insertion of the amplifier has a negligible effect on the overall system risetime. For measurements on the McDonnell-Douglas diodes, a desktop computer (HP9826) was connected to the digitizer for ease of analysis.

(a)

(b)
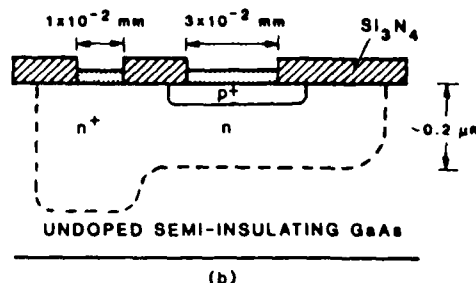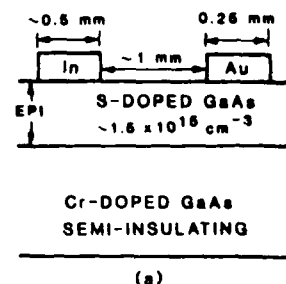
Figure 1. Schematic of device configurations: a) Schottky-barrier diode fabricated on an epi layer grown on a Cr-doped GaAs substrate; b) pn-junction diode fabricated by ion implantation of an undoped SI GaAs substrate.

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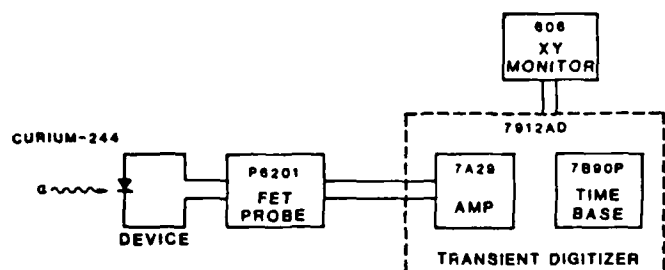
Figure 2. Experimental configuration used in charge collection measurements.

Figure 3. Example data trace for Northrop test devices.

RESULTS AND DISCUSSION

A typical data trace for a Northrop diode is shown in Figure 3. One feature to note is that the charge collection process is essentially complete in ~5 ns, which differs from our earlier study on semiconducting GaAs devices[3] where longer collection times were observed. (In the present Northrop SI devices, collection was complete in ~3 ns at high bias (30-60 V) and in ~7 ns at low bias (0-10 V). For the previous semiconducting devices, collection times were a factor of ~5 longer than these values.) This result suggests that the effective diffusion length in the SI devices is shorter than that in the semiconducting devices. Figure 4 shows a data trace for the McDonnell-Douglas test structure. (The HP9826 computer averaged the double-trace output of the 7912AD digitizer in this case.) In addition to the charge which is collected promptly (within 1-2 ns), there is a much slower charge collection process which appears to be completed in ~25 ns. (The collection process may actually continue but is masked by the RC roll-off of the measurement system.) At first glance this slower component might be interpreted as arising from diffusion of charge. However, the relatively small magnitude of the total collected charge (which implies a <u>short</u> diffusion length) appears to be inconsistent with the <u>long</u> temporal response (which implies a <u>long</u> diffusion length). This issue is discussed below. The random variations evident in the data trace are due to thermal noise associated with the FET probe. When comparing this trace with the trace in Figure 3, recall that an amplifier was inserted between the FET probe and the digitizer.

Figure 5 shows results of charge collection measurements as a function of applied reverse bias for a Northrop diode fabricated on a 6.8-μm epi layer doped to a concentration of ~1.5 x 10[15] cm[-3]. (The doping concentration increased gradually with depth into the epi layer.) Shown are the total measured charge, the "prompt" charge (i.e., the integrated charge at 1.5 ns),* and the calculated depletion region contribution to the measured charge. Because of observed variations in the amplitude of the collected charge, typically fifteen data traces were obtained at each bias and then averaged. The resulting error, which includes one standard deviation from the mean of the measured signal plus the uncertainty in the value of the integrating capacitance, is approximately ±14%. The depletion region width was

Figure 4. Example data trace for McDonnell-Douglas test devices.

found by capacitance measurements which are valid until the channel is nearly pinched off.[10] (Pinch-off occurs at a bias of ~70 V for this sample.) The amount of charge generated within that region was calculated using a Bragg curve for alpha particles in GaAs.[3] This result was then reduced by 15% because, in our earlier study on semiconducting GaAs,[3] approximately that percentage of the charge was lost to recombination before it could be collected by drift. Figure 6 shows the integrated charge along the track of a 5.0-MeV alpha particle in GaAs, which is derived from the Bragg curve. For the Northrop test device, 53 fC of charge is generated in the epi layer. Approximately 45 fc is the maximum charge available for collection via drift from that region, as indicated in Figure 5.

To explore the issue of whether charge funneling[†] from the SI substrate occurs, it is useful to compare the results of Figure 5 with those obtained previously for semiconducting GaAs devices.[3] Figure 7 illustrates that comparison. (The doping concentration for the semiconducting (SC) devices is approximately the same as that in the epi layer of the present SI devices, which permits a valid comparison to be made.) For biases ≲40 V, the prompt collected charge for SC devices is ~35% larger than that in the SI case. This comparison suggests that prompt funneling from the SI substrate is diminished compared to that in SC devices if we neglect collection via diffusion during the 1.5-ns

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*This definition of prompt is somewhat arbitrary. A time of 1.5 ns was chosen because it is just beyond the time period during which measurements are bandwidth limited (i.e., ≲1.2 ns). At earlier times, charge collection occurs via drift and diffusion. The data trace of Figure 3 shows continuous charge collection out to ~5 ns, and no transition point is observed. This behavior differs from that for semiconducting GaAs devices[3] in which a clear separation between drift and diffusion components was noted.

†The term funneling in the present paper refers to the charge collection process as described in References 5-8.

A-2
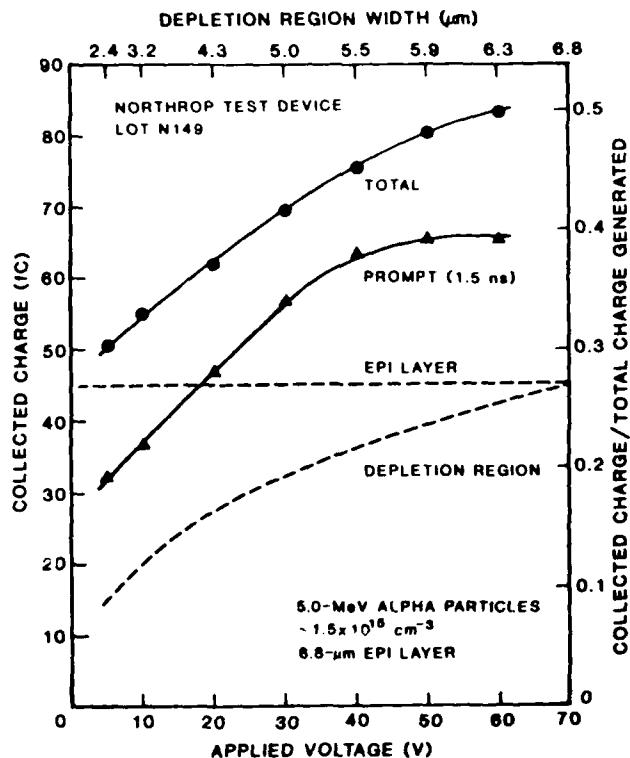
Figure 5. Collected charge vs applied reverse bias for 5.0-MeV alpha particles incident on a Schottky-barrier diode (Northrop test device). Also shown are values for the equilibrium depletion region width (upper scale) and the fraction of the total generated charge that is collected (right scale).

measurement period.* Further, the prompt SI data saturate for biases >40 V but the SC data do not. This is further evide ce that substrate funneling is relatively unimportant on a prompt timescale because, if it was occurring, the prompt charge would continue to increase as in the SC case.

To interpret the results of charge collection measurements on SI GaAs, it is appropriate[7] to consider the functional dependence of charge funneling on the dielectric relaxation time, τ_D ($\equiv \epsilon/\sigma$, where ϵ is the permittivity and σ is the conductivity of the material). This parameter is the characteristic time it takes for a solid to respond to charge imbalance. Therefore, one would expect the time associated with the formation of the funnel, and the time required for the charge to be collected via funneling, to vary with τ_D. This functional dependence has been verified quantitatively for silicon by Hsieh et al.[7] using computer simulations. In p-type Si with a doping density of 1×10^{15}, τ_D is approximately 14 ps and the potential spreading reaches a maximum at 25 ps.[7] In contrast, for p-type Si doped to 1×10^{13} cm^{-3}, the dielectric relaxation time is approximately 1 ns and the maximum potential distortion occurs in ~1 ns.[7] In SI GaAs, the resistivity is about 1×10^8 Ω-cm.[11] This value yields a dielectric relaxation time of ~100 μs. Based on the functional dependence just described, one would expect the funneling process to take a relatively long time in SI GaAs compared to semiconducting Si and semiconducting GaAs.

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*We calculate that the amount of charge collected by diffusion during this period is comparable for the SI and SC devices. This result is reasonably independent of the assumed carrier lifetime τ. (We assumed that $\tau(SI) \leq 5$ ns and $\tau(SC) \leq 25$ ns based on observed collection times.)
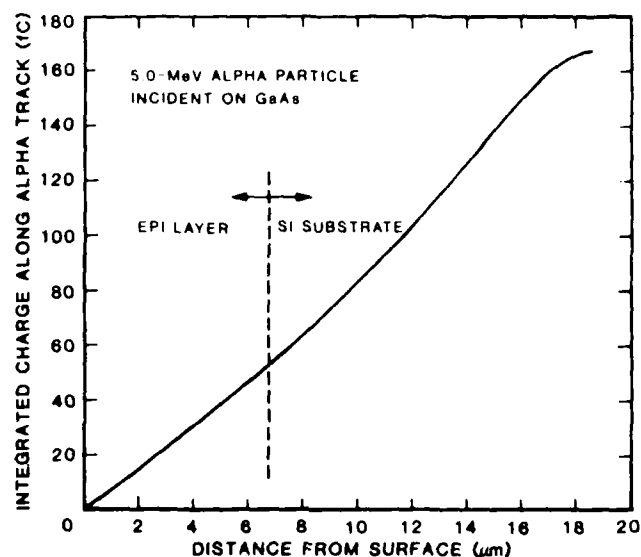
Figure 6. Integrated charge along the alpha-particle track vs distance from the device surface. The location of the interface between the epi layer and the SI substrate for the Northrop test device (data of Figure 5) is shown dashed.
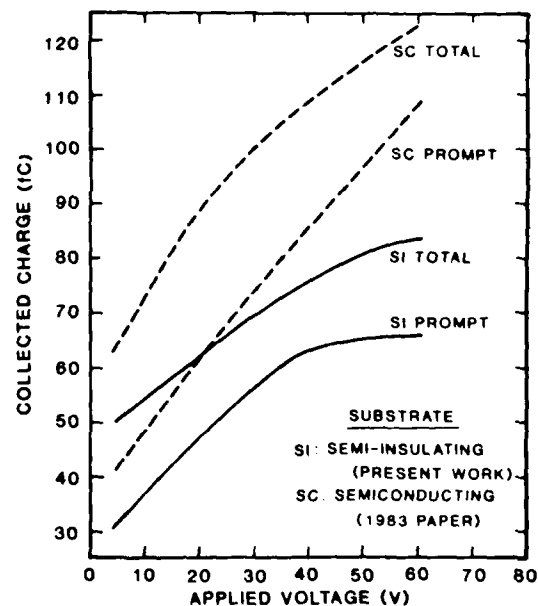
Figure 7. Comparison of charge collection results for GaAs diodes fabricated on semiconducting substrates[3] and semi-insulating substrates (data of Figure 5).

In our previous study,[3] the model of McLean and Oldham[8] was found to provide a reasonable description of the funneling process in SC GaAs. To determine whether their model predicts relatively slow funneling for SI GaAs, their expression for collection time was evaluated. The collection time is given by[8]

$$\tau_c = \left[\frac{3 N_0}{8 \pi \beta N_D v_p D^{1/2}} \right]^{2/3} , \qquad (1)$$

where N_0 is the plasma line density at the surface, N_D is the net substrate doping density, v_p is the effective

charge separation velocity, D is the ambipolar diffusion coefficient, and β is a factor dependent on the line density of the incident particle. Substituting in the appropriate values for SI GaAs,[3,11] a value of ~100 μs is obtained for τ_c. Thus, the model of McLean and Oldham also suggests a very slow funnel process. Because this process occurs so slowly, recombination and other processes should dominate. In Si GaAs, the minority-carrier lifetime (τ) is on the order of 10^{-8} sec,[11] which is orders of magnitude shorter than the dielectric relaxation time. (This condition defines a relaxation regime semiconductor.[12,13]) Based on the above analytical considerations, we therefore expect the charge funneling process, as it is presently understood, to be an unimportant mechanism in Si GaAs material because all carriers will be either collected or lost by the following competing processes long before funneling is established: recombination, diffusion, drift in the depletion region, and trapping. The present experimental results for Northrop SI devices appear to be consistent with this expectation.

Although funneling from the SI substrate appears to be relatively unimportant, the data of Figure 5 suggest that an additional charge collection mechanism is occurring. Thus far, we have considered drift in the depletion region, funneling in the SC epi layer, and diffusion from the epi layer and from the substrate. To illustrate that additional charge is collected, consider data obtained at 60 V. At equilibrium, the epi layer is almost fully depleted. All available charge in that layer (45 fC) will be collected promptly by drift in the depletion region and by funneling from the small undepleted SC region. Concurrently, collection via diffusion from the substrate occurs. Based on observed collection times and using Figure 6, we estimate that no more than 9 fC is collected during the 1.5-ns prompt measurement period, leaving at least 11 fC of prompt charge unaccounted for. An additional 18 fC is collected beyond 1.5 ns, and we estimate that no more than 8 fC of this delayed charge arrives via diffusion. The main point is that additional prompt and delayed charge appears to be collected by some process not yet discussed. Before suggesting possible mechanisms, an additional aspect of the experimental results is described.

The reader may wonder why data at and beyond pinch-off (≥ 70 V) are not shown in Figure 5. Such data were obtained, but an experimental limitation caused those results to have a large uncertainty associated with them. The collimator used with the present alpha source results in an area somewhat larger than that of the Schottky-barrier contact (Figure 1a) being bombarded. At a bias of 70 V, the equilibrium depletion region extends down to the substrate—epi-layer interface and a fringing field begins to develop in the substrate. An incident alpha striking the Northrop test device between the ohmic and rectifying contacts will generate some charge in that region of the substrate containing the fringing field. Such an occurrence will be recorded as a relatively low-amplitude charge collection event. Averaging those events with the direct strikes (i.e., those that pass through the Schottky barrier) will result in an apparent decrease in the collected charge for V > 70 V. These comments serve to point out that, in general, substrate fringing fields in SI GaAs devices can result in charge collection in a single-event experiment.

Returning to the issue of the additional charge collection, a few possible explanations are now given. One possibility involves funnel formation in the semiconducting epitaxial layer. As the field lines spread rapidly down the alpha track, one can picture the funnel as terminating at the interface in view of the long funnel formation time in the substrate. However, when the funnel reaches the interface, field lines can penetrate into the substrate and terminate on charged sites. This may result in a moderate "fringing" field. Charge generated in the substrate would then drift in that field and contribute to the collected charge. The timescale of this possible contribution would be the same as that of funneling in the epi layer, and its magnitude would depend on substrate mobilities and on the effect of substrate traps on the conductivity. Another possible source of the additional charge collection is the substrate—epi-layer interface junction. Ginell et al.[14] observed enhanced photocurrents in transient ionizing radiation response measurements on GaAs devices containing such a structure. A third possibility is that weak funneling from the substrate occurs over the measurement timescale (several nanoseconds), but this would be fortuitous and in disagreement with analytical predictions. Additional studies are needed to identify positively the mechanism responsible for the additional charge.

Figure 8 shows results of charge collection measurements as a function of applied forward bias for the McDonnell-Douglas test structure. Shown are the total charge, the charge collected in ~2 ns (defined as the prompt charge for this structure), and the calculated depletion region contribution to that charge. Since this is an enhancement-mode JFET test structure, the 0 V depletion layer extends beyond the semiconducting channel into the semi-insulating substrate. In fact, the depletion layer is not fully contained within the semiconducting channel until a forward bias of 0.3 V is applied. Below 0.3 V, fringing fields extend into the substrate so that a depletion region contribution has no meaning. Therefore, that contribution is shown only for forward biases above 0.3 V. The average magnitude of the prompt collected charge is ~3 fC. Based on Figure 6, this corresponds to an effective prompt collection distance of ~0.5 μm.

Data in Figure 8 are shown for most of the practical operating range for this JFET (0-1 V). For reverse bias, the applied field extends into the substrate. The collected charge increases with increasing reverse bias due to carrier transport in that region. (Such measurements were not performed extensively in the present study since they do not yield additional mechanistic insight.)
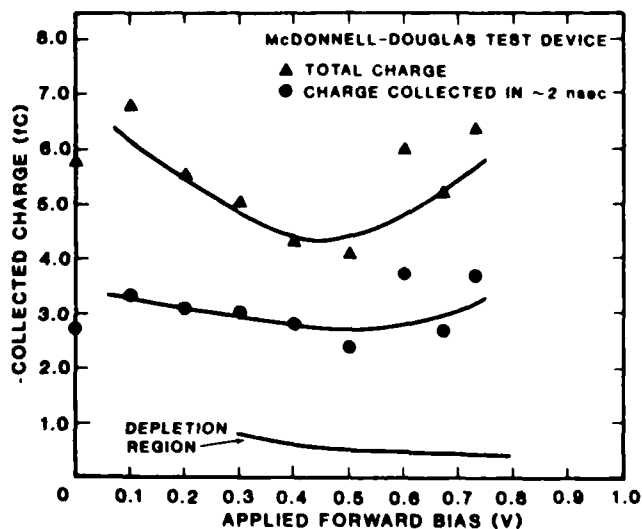
Figure 8. Collected charge vs applied forward bias for the McDonnell-Douglas test structure.

As mentioned earlier, data traces for the McDonnell-Douglas test device (e.g., Figure 4) exhibit a relatively long tail. This temporal response cannot be attributed to slow diffusion because the requisite long lifetime (and long diffusion length) would result in substantially more charge collection than observed. For example, if the substrate lifetime is 20 ns and the corresponding diffusion length is 6 μm (obtained using the ambipolar diffusion coefficient), Figure 6 indicates that $\sim$40 fC would be collected. Experimentally, a total charge of $\sim$5 fC is obtained. As in the case of the Northrop test device, additional charge collection mechanisms can be postulated. One possibility not mentioned above is that substrate trapping occurs within a diffusion length of the depletion region edge. To account for the data, trapped charge would then have to be released over the tens-of-nanoseconds measurement period.

CHARGE COLLECTION COMPARISON

Previously,[3] we compared charge collection in Si devices with that in semiconducting GaAs test structures. The conclusions were that those devices are expected to be comparable in their susceptibility to single-event upset (SEU) caused by prompt charge and that semiconducting GaAs devices appear to have a significant advantage in terms of total collected charge. In general, a thorough comparison of SEU susceptibility requires that other factors also be accounted for, including device geometries and circuit configurations. Conclusions made solely on the basis of charge collection data are still of value since they yield relative SEU tolerance under the condition that all other factors are equivalent for the technologies being compared. With this qualification, charge collection mechanisms in Si devices and SI GaAs devices are now compared based on the present results.

Qualitatively, we expect SI GaAs devices to be more immune to upset for the following reasons. First, consider current-sensitive circuit technologies, such as SRAMs. Because charge funneling appears to be relatively unimportant in SI GaAs, the prompt current will be relatively low compared to that in Si devices. (Figure 7 illustrates this point if one recalls that SC GaAs is comparable to Si in terms of prompt charge.[3]) In addition, the depletion layer in the thin semiconducting region in SI devices will contribute only a small amount of charge promptly. Now consider charge-sensitive technologies, such as CCDs and DRAMs. The total collected charge will be relatively low because of the short diffusion length in the SI GaAs substrate. Thus, we expect greater SEU immunity in SI GaAs devices than in their Si counterparts for both current-sensitive and charge-sensitive circuit realizations. Additional measurements and analyses are underway to investigate these expectations in more detail as well as to obtain further insight regarding charge collection mechanisms in GaAs devices.

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EFFECTS OF SINGLE NEUTRON INTERACTIONS IN SILICON INTEGRATED CIRCUITS[*]

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ABSTRACT

Measurements of the permanent effects of single fast neutron interactions in silicon depletion regions are reported for the first time. Increases in dark current density by as much as two orders of magnitude were observed for individual cells in an image sensor bombarded with 14-MeV neutrons. Single damage events and the distribution of a large number of events were measured. Experimental results are in good agreement with model calculations and statistical expectations. Long-term annealing data for single events are used in conjunction with previous macroscopic short-term annealing results to predict the early-time impact of individual damaged regions. Implications of the present results for VLSI/ULSI circuits are discussed, and examples of cases in which problems may occur are given. An approach is presented for assessing the susceptibility of any integrated circuit to the permanent effects of single neutron interactions.

INTRODUCTION

Energetic particles incident on integrated circuits produce ionization and displacement damage. The ionization created by single particles can cause soft errors to occur, and this subject is presently of considerable interest. We have performed research which focuses on the permanent effects associated with single-particle-induced displacement damage. Specifically, the effects of single fast neutrons on depletion regions in silicon devices are examined analytically and experimencally.

This paper begins with a review of our previously developed model[1] for the permanent increase in dark current density produced by a single neutron incident on a depletion region. Predictions appropriate for the present experimental conditions of 14-MeV neutron bombardment of a specific integrated circuit are also given. The concepts presented apply to bombardment with any energetic particle that produces displacement damage. Next, experimental findings are described, including the observation of single damage events, the distribution in magnitude of these events, and room-temperature annealing behavior. A discussion of the implications of these findings for VLSI/ULSI circuits is then given.

DESCRIPTION OF MODEL

A single fast neutron which interacts with a silicon atom in a device depletion region will give rise to many (several hundred for a 14-MeV neutron) stable defects in that region. Each of these defects produces energy levels in the bandgap, and those levels at or near midgap cause the dark current to increase via enhanced thermal generation. Thus, each defect causes an incremental permanent increase in dark current, and the magnitude of the total increase in current produced by a single neutron interaction is __independent__ of the shape of the damaged region. That is, the resulting increase is expected to be the same for a defect cluster as for a relatively isolated string of defects, assuming the same number of defects in both cases. As discussed previously,[2] clustered defects in a depletion region are expected to affect electrical properties in the same way

as isolated defects. (This statement is not true, however, for damage produced in neutral bulk material.)

It was previously shown[1] that the change in dark current density produced by a single neutron interaction in a device depletion region of area A can be expressed as

$$\Delta J_{d1} = q\, n_i / 2 A K_g\, p' \qquad (1)$$

In this equation, q is the electronic charge, n_i is the intrinsic carrier concentration, p' is the neutron scattering probability per centimeter of material, and K_g is an experimentally determined macroscopic generation lifetime damage coefficient. (Both p' and K_g are neutron energy dependent.) At 14 MeV, the scattering probability is[3] $0.09\ cm^{-1}$ and the damage coefficient is[4] 3.1×10^6 n-sec/cm^2. Using Eq. (1), we obtain $\Delta J_{d1} = 5.2 \times 10^{-15}/A$ amps/cm^2 at 303 K. Figure 1 presents ΔJ_{d1} versus depletion region area calculated using this expression. For the present test device, the predicted change in dark current density for a single 14-MeV neutron interaction is 2.3×10^{-9} amps/cm^2. For a 1 μm x 1 μm device, the prediction is 5.2×10^{-7} amps/cm^2. Note that these calculated values are for an "average" neutron interaction since a macroscopic value for K_g was employed (i.e., a value obtained for devices _damaged by many neutron interactions_). Actual increases in dark current density will be related to the distribution of primary knock-on energies produced. That distribution was previously calculated[1] for the case of 14-MeV neutrons incident on Si.

The neutron fluence ϕ_1 at which the mathematical expectation is that one interaction will occur in a depletion region of width x_d in one element of an array with D elements is given by[1]

$$\phi_1 = 1/A\, x_d\, p'\, D \quad . \qquad (2)$$

At 14 MeV, we obtain $\phi_1 = 11.1\,(VD)^{-1}$, where V is the depletion region volume. For the present test device (D = 3456), $\phi_1 = 3.5 \times 10^6$ n/cm^2. In summary, two simple expressions yield the model predictions: Eq. (1) gives the increase in dark current density produced by a single interaction and Eq. (2) gives the fluence at which a single interaction is expected to occur for a given integrated circuit. Note that there are no adjustable parameters in these equations.

EXPERIMENTAL METHODS

The integrated circuit selected for study was the Texas Instruments TC104 3456-element CCD linear image sensor. This device contains 3456 separate storage cells for imaging. The dimensions of each cell are 21.4 x 10.7 x 4 μm, where the latter value is the nominal depletion region width.[5] During operation as an image sensor, an incoming optical signal generates charge in the depletion region and this charge is integrated for a short time. Next, the charge in all storage cells is transferred to an adjacent CCD where it is clocked out rapidly. In the present study, the TC104
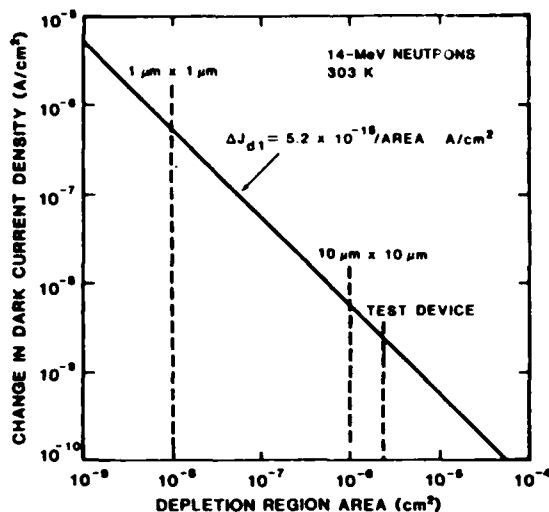
Figure 1. Calculated permanent change in dark current density produced by a single 14-MeV neutron interaction in a silicon depletion region as a function of the area of that region.

was operated in the dark and thermally generated dark current was allowed to accumulate in the storage cells. Two accumulation times were employed: 1 sec and 10 sec. Pre- and post-irradiation measurements of dark current density were made at 303 ± 0.2 K for each cell in the array using the experimental arrangement shown in Figure 2. Each current density measurement for a specific cell involved averaging 100 readings performed under computer control. To convert measured output signal to dark current density, a conversion factor of 1.25 ± 0.25 μV per electron[5] was employed.* (For an accumulation time of 1 sec, a 1-mV output signal corresponds to a dark current density of 5.6×10^{-11} A/cm^2.) The measured pre-irradiation dark current density for an individual cell was typically 2.5×10^{-10} A/cm^2 at 303 K; the dark current density for a small percentage of the cells was a factor of 2 to 3 larger than this.

The TC104 was bombarded with a steady-state 14-MeV neutron flux at room temperature with all leads shorted. Irradiations were performed at the ICT 14-MeV neutron facility at Lawrence Livermore National Laboratory. The test device was irradiated seven times over a 4-day period to the following cumulative fluences: 1×10^7, 3×10^7, 1×10^8, 3×10^8, 1×10^9, 3×10^9, and 1×10^{10} n/cm^2. The measured total ionizing dose (cumulative) for these irradiations was 13 rad(Si), and thus ionizing radiation effects on the TC104 can be neglected. Post-irradiation measurements were performed 2 to 3 hours after each bombardment, and were continued at intervals following the last irradiation.

MULTIPLE INTERACTION PROBABILITIES

The probability of multiple neutron interactions in a given cell can be determined using the Poisson distribution. The probability that x "successess" (i.e., interactions) occur in ϕ "trials" (i.e., bombardment with a neutron fluence ϕ) is given by

$$P(x,\lambda) = \lambda^x e^{-\lambda}/x! \quad , \quad (3)$$

where $\lambda = \phi \theta$ and θ is the probability of success in one trial. Using the depletion region dimensions for one cell in the present test device and a neutron scattering probability of 0.09 cm^{-1}, the calculated value for θ is 8.24×10^{-11}. Figure 3 shows interaction probabilities

*This factor was determined experimentally by the manufacturer and is considered to be an accurate value for any TC104 image sensor.[5]

for a specific cell in the 3456-element test device at the seven neutron fluences used experimentally. The probability of multiple interactions occurring is seen to be very low at the lower fluence values. After 10^{10} n/cm^2, probabilities for multiple events are considerably higher. For example, at that fluence $P = 0.041$ for three interactions. Thus, the expected number of cells experiencing three individual damage events is 141 for the entire array.

EXPERIMENTAL RESULTS

Single Damage Events

The first irradiation was performed at a fluence of 1×10^7 n/cm^2. Based on Eq. (2), we expected to observe 2 to 3 events at that fluence. Two events were recorded, as shown in Figure 4a where the change in dark current density (ΔJ_d) is plotted versus cell number. (An event is defined as a change in dark current density of more than 10%.)[†] Measured values of ΔJ_d were 5.3×10^{-10} A/cm^2 for cell #2702 and 2.5×10^{-9} for cell #3283. After 3×10^7 n/cm^2, nine new events were recorded (Figure 4b). These experimental results and those obtained at higher fluences are consistent with the model described above. Readily observable changes in dark current were produced by single neutron interactions, and, as shown below, many of these changes are large compared to the pre-irradiation dark current density.

Distribution of Damage Events

Figure 5 shows the distribution of damage events after a fluence of 1×10^{10} n/cm^2. Only new events are shown, and this distribution was obtained by subtracting the distribution obtained after 3×10^9 n/cm^2 from that measured at 10^{10} n/cm^2. The number of cells contributing to this distribution is 1389. The inset to Figure 5a expands the ordinate scale at high ΔJ_d values. Figure 5b shows the distribution for large changes ($10 < \Delta J_d < 40$ nA/cm^2).

The mean value of the distribution is 1.5 nA/cm^2 as compared to the predicted value of 2.3 nA/cm^2. (Increasing the noise discrimination level by a factor of two increases the experimental mean value to 1.6 nA/cm^2 and decreases the number of cells in the distribution to 1318.) The experimental dark current calibration factor was only known to within ± 20%. Also the value of K_g used in the model may not be the most appropriate one due to possible annealing effects (described below). Given these uncertainties, the agreement between experiment and model calculation is reasonably good.

The shape of the experimental distribution in Figure 5 is reasonably consistent with the calculated distribution,[1] although this comparison suggests the possibility that inelastic scattering may not be as important as indicated by calculations. This issue will require further study. Calculated and experimental results both show a large number of relatively low

[†]The percent standard deviation for pre-irradiation dark current density measurements was ~10% for a charge accumulation time of 1 sec. (For an accumulation time of 10 sec, the value was ~2%.) This was the basis for our definition of an event. Lowering the event threshold increases the number of "real" small-amplitude events, but also increases the number of false events. Increasing the threshold reduces the number of both types of events. As noted in the next subsection, our choice of 10% for the threshold appears to have been appropriate since the distribution of damage events was found to be relatively insensitive to a large change in threshold value.
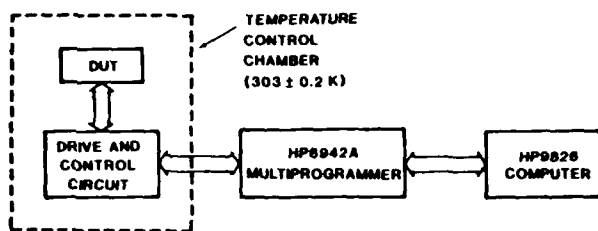
Figure 2. Schematic illustration of the apparatus for dark current measurements on the test device (DUT = device under test).

$$P(x,\lambda) = \frac{\lambda^x \, e^{-\lambda}}{x!}$$

$$\lambda = \phi\theta; \quad \phi = \text{FLUENCE}$$

$$\theta = 8.24 \times 10^{-11}$$
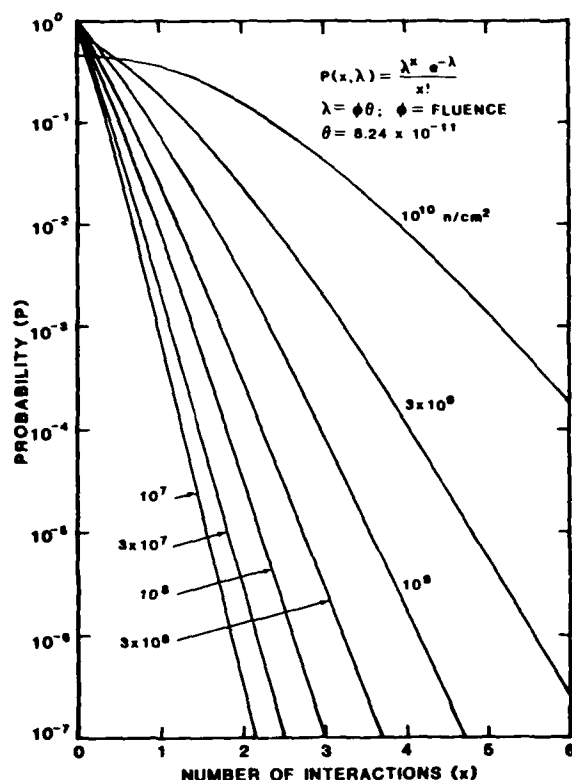
Figure 3. Probability of 14-MeV neutron inter-actions in a specific element of the test device at several fluences.

Figure 4. Measured change in dark current density produced by single 14-MeV neutron interactions. Irradiations were performed to two fluences: (a) 1×10^7 n/cm^2; (b) 3×10^7 n/cm^2. Individual damage events are evident.

amplitude events. Also, a long tail consisting of large-amplitude events occurs in both the calculated[1] and experimental distributions. It is notable that the largest events (Figure 5b) are a factor of ~20 greater than the mean experimental value of ΔJ_d. Also, four of the cells exhibited an increase in dark current density by a factor of ~100 compared to pre-irradiation values.

For the data of Figure 5, 1389 cells were damaged by an incremental fluence of 7×10^9 n/cm^2. Based on the Poisson distribution (Eq. (3)), we calculate the following distribution of multiple neutron interactions in these cells: 1027 cells experienced 1 interaction; 296 cells experienced 2 interactions; 3 interactions occurred in 57 of the cells; 8 cells had 4 interactions; and 1 cell had 5 interactions. Thus, 5% of the 1389 cells are calculated to have experienced multiple inter-actions. Therefore, it is likely that the relatively large magnitude events in Figure 5 are attributable

primarily to multiple interactions in individual cells.[*] Another possibility is that (n,p) and (n,α) interac-tions produce some of these large events.

Annealing

Data presented above were obtained within a few hours of each irradiation. Annealing of neutron-in-duced damage occurred, and this process was monitored over a six-week period following the set of seven irra-diations. Figure 6 presents dark current annealing factor (AF), as defined in the figure, versus time fol-lowing irradiation. The data points shown are the aver-age of AF values obtained for 183 cells in the image sensor. These cells are a subset of those that exhibi-ted a neutron-induced increase in dark current density only during the last irradiation performed (incremental fluence = 7×10^9 n/cm^2). A decrease in AF from a value of ~2.2 to unity is observed over the period from a few hours to 1000 hours. Thus, the damage in-duced by single neutron interactions decreased by a factor of 2.2 over the six-week room-temperature anneal-ing period.

In a previous study,[6] dark current AF was measured as a function of time for a charge-coupled device (Fairchild CCD 321A) bombarded with a burst of fission neutrons using a TRIGA reactor. The fluence used was was relatively high (1×10^{12} n/cm^2) compared to the present fluences, so many neutron interactions occurred in each cell of the CCD studied. Also, the neutron en-ergies employed (fission spectrum) are lower than that used here. (Short-term annealing in silicon devices exhibits a moderate neutron energy dependence at early times in neutral material.[7]) It is still useful, and

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[*] Note that the calculated distribution (Ref. 1) is for single neutron interactions, whereas a portion of the measured distribution (Fig. 5) is due to multiple in-teractions.
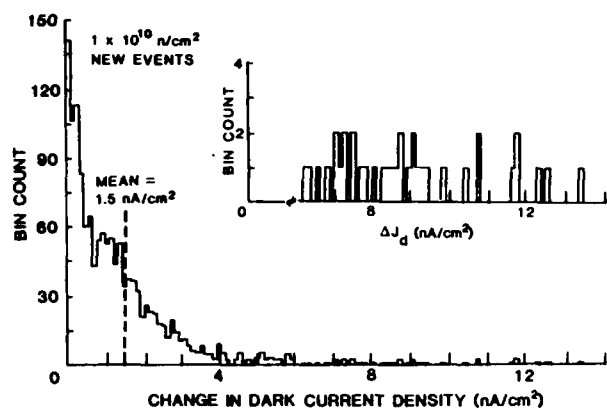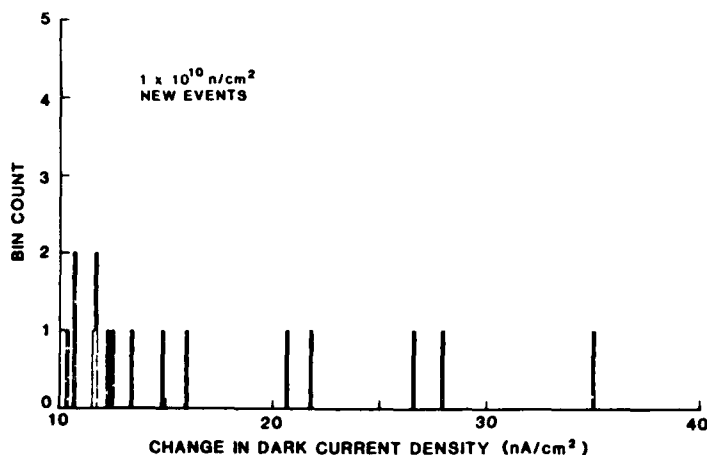
Figure 5. Measured distribution of new damage events after 1 x 10^{10} n/cm^2: (a) distribution from 0 to 14 nA/cm^2; (b) distribution from 10 to 40 nA/cm^2. The mean value of the entire distribution is 1.5 nA/cm^2.
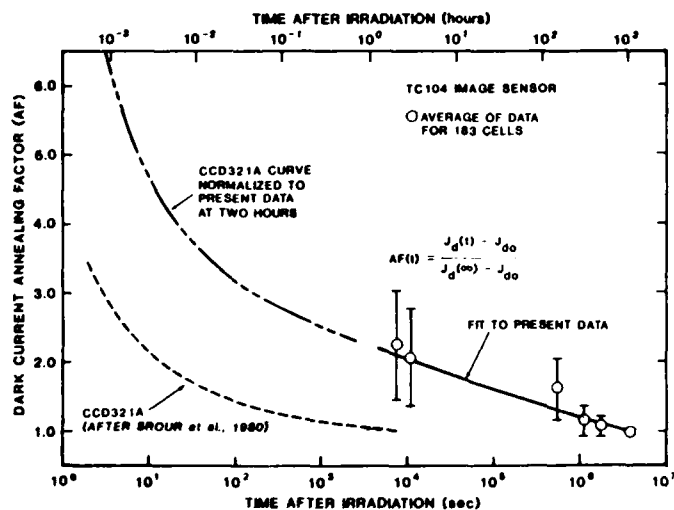
Figure 6. Dark current annealing factor versus time after irradiation for the TC104 image sensor irradiated to an incremental fluence of 7 x 10^9 n/cm^2. Data points are the average of values for 183 cells.

probably reasonably accurate, to employ the results of that earlier study[6] to estimate the magnitude of dark current increases due to single neutron interactions at times earlier than a few hours after irradiation. Figure 6 shows the CCD 321A results in the lower left-hand portion. That experiment ended approximately two hours after pulsed bombardment. However, the present results show considerable annealing beyond two hours. The CCD 321A curve was normalized to the present data by scaling it by a factor of 2.2, as shown in the figure. The resulting curve indicates that the magnitude of the damage introduced by a single neutron interaction will be about a factor of 3 larger a few seconds after the interaction occurs than at two hours later. (At times earlier than a few seconds, the amount of damage present presumably would be even larger since transient annealing in neutron-irradiated silicon generally is monotonic.)

The error bars shown in Figure 6 are equal to one standard deviation from the mean AF values. Considerable spread in AF values was observed. We examined whether the AF magnitude was correlated with the magnitude of the dark current increase. The correlation coefficient was relatively low (0.27), indicating only weak correlation. Results of previous work[7] revealed larger AF values for 14-MeV neutron bombardment than for fission neutron irradiation, which suggested a correlation of AF with the magnitude of the damage events. However, that study involved monitoring recombination lifetime in neutral material, whereas the present results are due to generation lifetime annealing in a depletion region. Further study is needed to explain the presently observed distribution in AF values.

As noted above, the 183 cells used to obtain the data points in Figure 6 were undamaged in the first six irradiations. They exhibited an increase in dark current only after the final incremental irradiation of 7 x 10^9 n/cm^2. Some of these cells experienced more than one neutron interaction during that irradiation. Using the Poisson distribution, the probabilities for a given cell to remain undamaged or to be damaged (i.e., one or more interactions) at 7 x 10^9 n/cm^2 are 0.562 and 0.438, respectively. The calculated result is that 74% of the 183 cells experienced one interaction, 21% experienced two interactions, and 5% experienced three or more interactions. Thus, the results of Figure 6 are predominantly attributable to annealing of single damage events. Annealing factor values for cells in which multiple interactions occurred represent a composite of the recovery behavior for multiple damage events.

Multiple Interactions

The experimental results were examined to determine whether the number of interactions per cell followed the Poisson distribution. Dark current changes experienced by each cell in all seven irradiations were tabulated and the number of cells experiencing a specific number of interactions was determined. Results are shown as data points in Figure 7. Also shown is the calculated Poisson distribution, and very good agreement with experimental findings is evident. (During any one of the seven irradiations, multiple interactions may occur in a specific cell. However, such an occurrence will only be counted as one interaction because only one dark current increase is measured. This effect is calculated to have only a minor impact on the data points in Figure 7.)
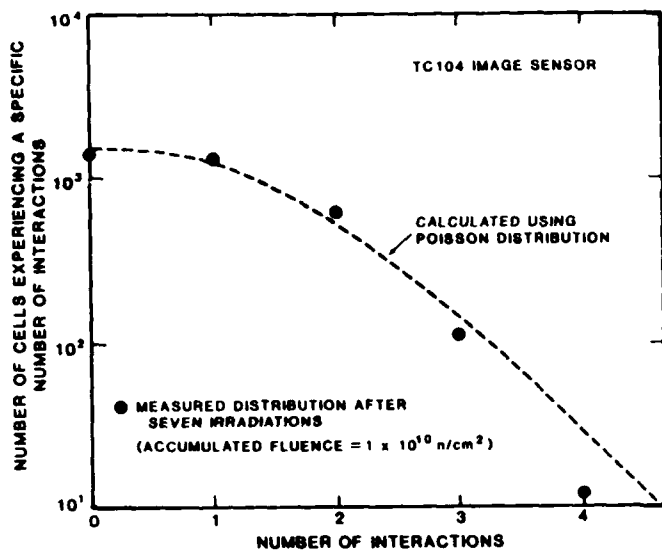
Figure 7. Comparison of measured and calculated distributions of the number of cells experiencing a specific number of interactions.

IMPLICATIONS FOR VLSI/ULSI CIRCUITS

The experimental results presented here are in good agreement with model calculations. Thus, we can employ this model with confidence to predict the expected effects of single neutron interactions in VLSI/ULSI circuits. Although the example of 14-MeV neutron bombardment is considered here, it is again noted that the concepts described will apply for other energetic particles, such as cosmic rays, which deposit a portion of their energy into displacement processes. (The case of 5-MeV alpha-particle bombardment was considered previously.[1])

Neutron interactions produced large changes in dark current density for cells in the present test circuit. Cell dimensions in the TC104 imaging array are relatively large. Figure 1 illustrates that as cell dimensions shrink the change in dark current density gets proportionately larger. Thus, the effect reported in this paper is likely to present a problem for small-geometry charge-integration and charge-transfer devices (imagers, CCDs, etc.) unless those devices are operated below room temperature.[1] Such devices typically require that the dark current density be low for proper operation, as evidenced by the TC104 image sensor. Also note that this single-particle effect will occur at a relatively low particle fluence.

Predicting the implications of the present phenomenon for other types of VLSI/ULSI circuits, such as memories, can be performed by simply viewing the damaged region produced by a single particle interaction as a charge generator. Neglecting annealing effects, this region is a steady-state source of thermally generated charge, which results in a dc current flow. Whether this charge or current presents a problem will depend on the nature of and specifications for the device or circuit being considered (function, timing requirements, critical charge, etc.). Many projections for VLSI/ULSI circuits have been, and continue to be, made. We take the approach here of describing the room-temperature behavior of a single damaged region contained in a depletion region of any device or circuit. The designer or user can apply this information to a specific case and determine whether a problem will occur.

Figure 8 is a plot of the thermally generated charge Q_g from a damaged region versus the time charge is allowed to accumulate in any device. Note that the curves shown
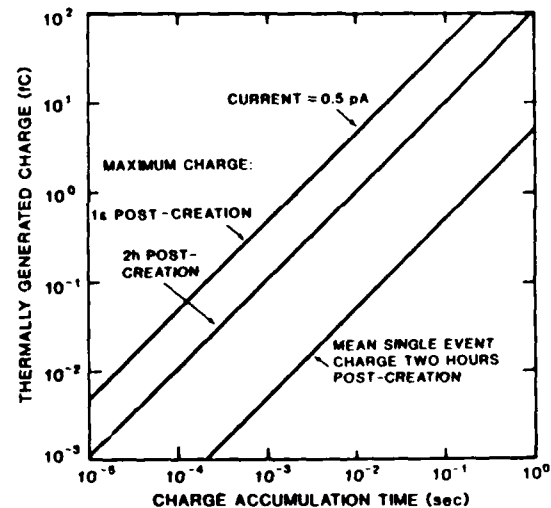
Figure 8. Thermally generated charge versus charge accumulation time for the damaged region produced by a 14-MeV neutron interaction in a depletion region. The lowest curve is for the mean damage event 2 h after creation of the damage. The two upper curves yield the maximum charge generated for two times post-creation: one second and two hours.

are independent of device geometry, i.e., depletion region dimensions (as long as the damaged region is completely enclosed in the depletion region). The lowermost curve was calculated based on the mean single event two hours after irradiation. (It is readily shown that Q_g in femtocoulombs is given by 5.2 t, where t = time in seconds. The predicted mean value of ΔJ_{dl} is used here for illustration.) The uppermost curve and the middle curve are for the largest event observed, which was a factor of ~20 greater than the mean event (Figure 4).* Shown are the maximum charge curves for 1 sec and 2 h following creation of the damaged region. Note that the worst-case dc current is 0.5 pA, although currents presumably would be larger at earlier times.

The use of Figure 8 can be illustrated by a few examples. If the dc current appropriate for a given situation (e.g., 0.5 pA at 1 sec post-creation) is too large for a specific circuit, then the permanent effects of single 14-MeV neutron interactions will be a problem. (Note that the maximum effect illustrated will occur at a fluence considerably greater than given by Eq. (2).) Again, projected device specifications, including leakage current tolerances, are needed for specific cases to assess this issue quantitatively. Now consider the charge tolerance of VLSI/ULSI devices. An appreciable amount of time is required to accumulate charge by the present mechanism. For example, it takes 100 msec to accumulate 50 fC for the worst case illustrated in Figure 8. Appropriate device operating times and charge tolerances are needed to assess the susceptibility of any circuit. One example is NMOS DRAMs. The stored charge in 1- and 4-Mbit DRAMs has been projected[8] to be ~150 fC; a charge of ~5 fC generated by leakage mechanisms is acceptable for such circuits.[8] If the refresh time is on the order of 50-100 msec, charge accumulated via the present single event phenomenon may be unacceptably large. This example suggests that single-particle-induced permanent damage may eventually cause limits to be placed on the dimensions of specific types of integrated circuits.

*
As discussed above, the observed large-magnitude events are probably due to multiple interactions. We use the largest event observed for illustration here since such events have a finite probability of occurring in a dense array at a relatively low fluence.

CONCLUDING REMARKS AND SUMMARY

Holmes et al.[9] performed 14-MeV neutron irradiations of a Si vidicon target containing 5×10^5 pn-junction diodes. They measured the average dark current for the entire array as opposed to the present direct measurements of single events in individual cells. Holmes deduced the behavior of individual devices by monitoring the brightness of cells on a video display. Although their measurements were macroscopic, they made statistical deductions regarding microscopic behavior which appear to be consistent with the present findings.

Silberberg et al.[10] recently reported that fast neutrons present in the earth's atmosphere between 10,000 and 60,000 ft are a major source of soft errors in that region. Based on the present findings, the importance of single-neutron-induced permanent damage for devices operating in the atmosphere should also be assessed. (The permanent effects of high-energy protons should be considered as well.)

Burke et al.[11] employed a CCD to study the microscopic aspects of energy deposition by gamma rays. The present work is another example of the utility of charge-coupled devices in basic studies of radiation effects phenomena.

In summary, this paper has presented the first direct measurements of the permanent effects of single fast neutron interactions in silicon depletion regions. Increases in dark current density by as much as two orders of magnitude were observed for individual cells in an image sensor bombarded with 14-MeV neutrons. Single damage events and the damage distribution were measured, and results were in good agreement with model calculations and statistical expectations. Implications of these findings for VLSI/ULSI circuits were considered, and an approach was given for assessing the susceptibility of any integrated circuit to the permanent effects of single neutron interactions.

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APPENDIX C

CHARACTERISTICS OF SEU CURRENT TRANSIENTS AND COLLECTED CHARGE IN GaAs AND Si DEVICES[*]

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ABSTRACT

Results of transient current and charge collection measurements on GaAs and Si devices bombarded with 5-MeV alpha particles are presented. Upper bounds for rise-time and charge collection time of ~ 120 psec and ~ 300 psec, respectively, were determined for the GaAs devices studied. The observed lack of funneling for lightly doped Si devices is consistent with the long dielectric relaxation time in the substrate material. Slow charge collection in lightly doped Si diodes is interpreted as arising from drift in low electric fields. Measurements of the bias and doping dependence of charge collection by funneling are in good agreement with the predictions of the McLean-Oldham model.

INTRODUCTION

A highly ionizing particle, such as a cosmic ray, that interacts in a semiconductor produces a track of dense ionization. If the track passes through a critical node of an electronic device, device operation will be upset if sufficient charge is collected at that node. This phenomenon is called single event upset (SEU) and has been extensively studied.[1] The charge collection processes and the timescales over which these processes operate are crucial in determining the magnitude of the SEU problem and upset rates. Charge is collected by both drift and diffusion. The drift component consists of charge created in the depletion region and charge which is collected from beyond that region by funneling. The term funneling refers to the redistribution of the electric field present at a sensitive node along the ion track.[2-5] The funneling process causes a larger amount of single-particle-induced charge to be collected promptly, thus increasing the likelihood of a soft error. The diffusion component is simply that charge which diffuses to the depletion region and is then swept to the sensitive node.

Various analytic models and computer simulations have been developed to explain charge funneling.[5-9] Computer simulations, although more accurate than existing phenomenological models, are expensive and time-consuming. The phenomenological McLean-Oldham model has been used successfully to predict some of the features of alpha-particle bombardment in silicon and GaAs devices.[5,6,10,11] Discrepancies between predictions and measurements have been found for the case of very high track densities such as those which occur with heavy ion bombardment.[6] To test the validity and applicability of the McLean-Oldham model, it is useful to study the dependences of charge collection on bias and doping in both silicon and GaAs. Such measurements should lead to a better understanding of the mechanisms involved in charge funneling and improvements in the analytic models.

In previous charge collection investigations, the magnitudes of the collected charge have been measured.[5,10] The temporal characteristics of the current transient have not been directly measured. The reason for this is that charge collection times when funneling dominates are predicted to be on the order of a few tenths of a nanosecond. Instrumentation to measure electrical processes on this timescale is not readily available in most laboratories. An oscilloscope with a risetime of ~ 120 ps was made available for this investigation. We have attempted to measure the current transient or at least place an upper bound on the collection time. Since this time is expected to be a function of doping density, investigation of the temporal form of the transient current was performed as a function of both doping and applied electric field. The collection time is expected to increase with lower doping so that the collection process may be more readily observable for high-resistivity samples.[4] Thus, charge collection measurements were also performed on very lightly doped Si to examine the possible relationship between dielectric relaxation time and the onset of charge funneling.[11]

EXPERIMENTAL DETAILS

The devices used in this investigation were Schottky-barrier diodes fabricated on both semiconducting (SC) and semi-insulating (SI) GaAs substrates and on high-resistivity p-type Si. The GaAs samples included 250-μm diameter Au$-$n-type GaAs Schottky-barrier diodes containing an epi layer that ranged from 7 μm to 20 μm. The doping concentration varied from 10^{15} to 7×10^{16} cm^{-3}. Examples of the device configurations and the results of α-particle-induced charge collection were previously reported in References 10 and 11 for SC and SI GaAs devices, respectively. The Si devices included Al$-$p-type Si Schottky-barrier diodes which were fabricated on 12-mil-thick Si wafers obtained from float-zone ingots. Substrate doping densities were 3×10^{13} cm^{-3} (2000 Ω-cm) and 1×10^{14} cm^{-3} (250 Ω-cm) for these devices. The device structure was planar with a square Al Schottky contact measuring 500 x 500 μm surrounded completely by an ohmic contact. The ohmic contact was formed by a p$^+$ diffusion starting ~ 5 μm from the edge of the Schottky contact. All devices were fabricated at Northrop. Charge collection measurements were made with the devices biased. Considerations based on device breakdown, turn-on voltage, and leakage current limited the voltage range and, hence, the depletion widths achievable.

Two measurement techniques were used in this investigation. In the first, for which measurements were bandwidth limited, the amount of collected charge was determined by integrating the current on the sum of the device capacitance and the input capacitance of the front-end circuitry. This requires a time constant for the front-end electronics much greater than the temporal characteristics of the signal. The resulting integration gives the collected charge as a function of time. The amount of charge measured at the risetime of the measurement system is the prompt

charge (assumed to be predominately drift) while that at saturation is the total charge (all contributions). This technique is referred to here as a charge collection measurement.

In the second technique, referred to as a transient current measurement, a measurement system with a fast risetime compared to the signal to be measured was needed to permit resolution of the temporal characteristics of the signal. This requires both an oscilloscope or digitizer and front-end circuitry having response times faster than the signal of interest. If these limits on the time constants are not met, the measured signal will be distorted and signal processing is then required to extract information from the measurement.[12]

The charge collection measurement technique has been described previously.[10] The current pulse resulting from a single 5.0-MeV alpha particle interaction is integrated by the sum of the device capacitance and the input capacitance of a Tektronix P6201 FET probe. The data trace was recorded using a Tektronix 7912 transient digitizer and a HP 9826 computer for analysis. The measurement system is bandwidth limited for times < 1.2 ns after an alpha particle strike. Typical data traces for two biases were presented in Reference 10 for SC substrates.

As described above, an accurate transient current measurement requires that the measurement system have a response time much faster than the temporal characteristics of the current. The measurement system includes not only the amplifiers, oscilloscope or digitizer, and associated circuit elements, but also the effective complex impedance contributions from the device which is undergoing bombardment. Ideally, the oscilloscope should have a bandwidth greater than any frequency component in the current transient. The front-end circuitry, including both the device and the probe assembly which connects the device to the measurement instrumentation, acts as a current-to-voltage converter. The probe should only be resistive. The device capacitance should be small so that the RC time constant is much less than the temporal characteristics of the current. In practice, the bandwidth (4 GHz) of the oscilloscope was found to be insufficient. The probe assembly was also not ideal, resulting in reflections. The Schottky-barrier diodes used can be electrically modeled as consisting of a bias-dependent capacitor and resistor in parallel with a current source. Depending on the geometry of the diode, a series resistor between the depletion region and the ohmic contact may also be needed in the model. These nonideal effects result in an effective RC time constant on the order of or larger than the time constant of the transient current. The measured voltage signal becomes a distorted image of the transient current. Using signal processing techniques with models for both the transfer functions of the probe assembly and the device, it is possible to remove some of this distortion.

The probe assembly used to measure the transient current consists of a rigid air-core coaxial cable to which was mounted the collimator containing the alpha source (Cm^{244}). A three-axis micropositioner and a microscope were used in aligning the device and microprobe point which connected the device to the central conductor of the coaxial cable. Time-domain reflectometry was used to measure impedance mismatch in the probe. The greatest mismatches occurred at the end of the probe and at the microprobe point connection to the device, resulting in oscillations in the measured signal.

The probe assembly was connected to two high-frequency amplifiers. The system was tested with the 500-MHz digitizer used for the charge collection measurements

and found to be limited by the digitizer bandwidth. The step response was also tested using an 18-GHz sampling system and was found to be stable. (The 4-GHz oscilloscope used during the transient current measurements was not available during this particular testing period.)

The transient current measurement system consisted of the probe, the amplifiers, and the 4-GHz oscilloscope. Data traces were stored on polaroid film, which was photographically enlarged to 8 x 10 inches. The enlargements were digitized for input into a HP 9826 computer by use of a graphics tablet.

Within the accuracy of the electrical models of the front-end circuitry (probe and device), digital signal processing was used to minimize distortion caused by the "RC" effects of the front-end circuitry.[13] The model used for processing is shown in Figure 1. Device parameters were either measured or calculated. Because of reflections at the end of the probe caused by impedance mismatch, an effective inductance was introduced into the model. Its value was determined from the observed oscillation frequency. The mismatch at the device was not modeled. This distortion will therefore remain in the derived current transient. Signal processing cannot overcome the bandwidth limitation of the oscilloscope. The model was analyzed in the frequency domain, then converted to the Z domain using the bilinear transformation.[12,13] A typical result of the signal processing is shown in Figure 2. The long tail in the original voltage signal is removed. A double hump resulting from the mismatch at the device was observed in some of the data. For signals having pronounced oscillation, digital signal processing was very effective in removing this distortion.

EXPERIMENTAL RESULTS AND DISCUSSION

Temporal Characteristics of Charge Collection

Measurements of transient current were made for both SC and SI GaAs diodes. The voltage signals were processed to minimize distortion, and results are presented in Figures 3 and 4 for SI and SC GaAs substrates, respectively. In Figure 3, the variation with bias is shown. The risetime for the current pulses is approximately 120 psec which is the result of the system bandwidth. The overall width of these pulses also reflects the bandwidth limitations of the measurement system. The current pulse due to charge funneling has a risetime of less than ~ 120 psec and a collection time of under ~ 300 psec. Because of the large standard deviation of signal amplitudes for each bias, the increase in amplitude with bias that is generally observed is not very evident.

In Figure 3, the transient currents for SI GaAs samples exhibit only one peak. There is a tail extending out to many nanoseconds, possibly due to diffusion, but this tail is within the noise introduced by the signal processing. This set of samples was mounted on TO-5 headers with the ohmic contact connected by a short wire to a lead in the header. The other contact was made with the microprobe point in the probe assembly. No oscillations were observed in the processed signal.

Figure 4 shows the processed transient currents for semiconducting GaAs devices as a function of doping for a bias of - 20 V. Again the risetime is attributed to the bandwidth limitation of the measurement system. The amplitude decreases as a function of increasing doping. Hsieh et al.[4] predict that the peak amplitude of the current transient should increase with doping while at the same time the pulse narrows. Since the present measurements are made under bandwidth-limited
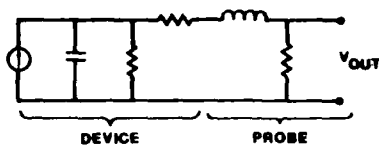
Figure 1. Model used for the device and probe assembly in digital signal processing of the measured voltages. An effective inductance was included to model the observed reflections.
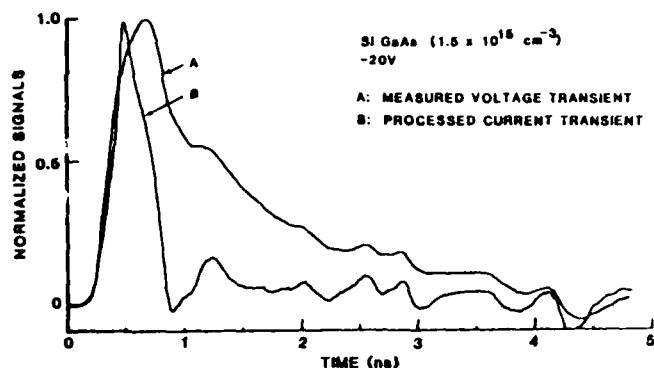
Figure 2. Examples of the measured voltage signal and the processed transient current. Signals have been normalized to their respective maxima.
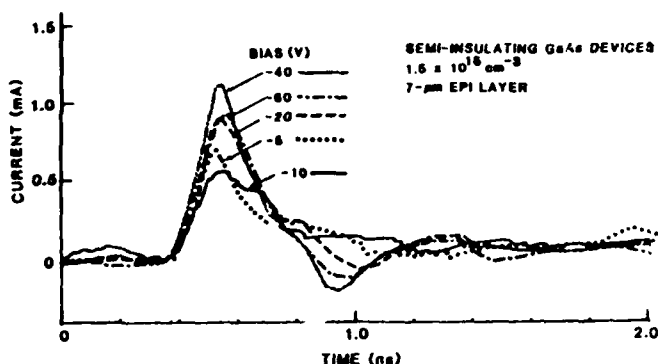
Figure 3. Processed transient currents as a function of bias for 1.5 x 10^{15} cm^{-3} n-type semi-insulating GaAs Schottky diodes. Signals are bandwidth limited.
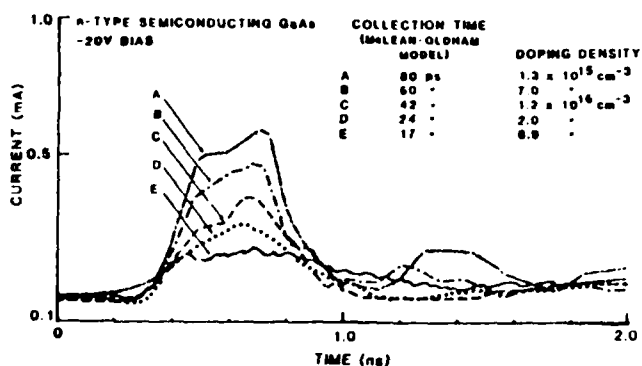
Figure 4. Processed transient currents as a function of doping for semiconducting GaAs Schottky diodes biased to -20V.

conditions, a certain amount of integration occurs. The amplitude behavior supports the interpretation that integration occurs since, from the McLean-Oldham model, collected charge varies as the doping to the -1/3 power.[5]

The shape of the processed transient currents for SC GaAs shown in Figure 4 indicates the presence of two peaks. The overall width is ~500 psec. The calculated collection times based on the McLean-Oldham model are given in the figure. The longest time is 80 ps, which is well below the resolution of the measurement system. The double peak makes any comparison even more difficult. The reason the transient currents for these SC GaAs samples are double-peaked while those for the SI GaAs devices have only a single peak is not yet understood. It should be noted that these SC samples were mounted on copper plugs where the ohmic contact is made through the substrate and the barrier contact is made with the microprobe point. It is possible that the different methods of mounting the SC GaAs devices compared to the SI devices result in the occurrence of the two humps.

Numerical integrations of the derived transient currents in Figures 3 and 4 were compared to the prompt charge determined using the charge collection technique. The integrated transient currents were found to be from 1.5 to 3 times as large as those determined from charge collection measurements. These discrepancies can be accounted for by noting the effects of reflection and approximations in the model used for signal processing that do not completely eliminate the distortion caused by integration in the front-end electronics.

Another approach to obtaining the temporal characteristics of the transient current was to make charge collection measurements on very lightly doped Si diodes. (These samples were not available at the time of transient current measurements.) Since the dielectric relaxation times for 250 and 2000 Ω-cm Si are ~0.25 and ~2 nsec, respectively, the onset of funneling may be observable in the 250 Ω-cm sample while no funneling should occur in the 2000 Ω-cm sample. Complicating the analysis, however, is the role of RC effects and the device geometry.

Figure 5 shows results of charge collection measurements on a Si Schottky-barrier diode fabricated on a substrate with a doping density of 3 x 10^{13} cm^{-3}. (Results for a device with a doping density of 1 x 10^{14} cm^{-3} were similar but exhibited a shorter timescale for collection.) The risetime for charge collection is observed to be as long as 30 nsec. Because of the complicated frequency dependence of the active probe impedance, signal processing is more difficult and has not yet been performed for charge collection measurements. However, both the magnitude and bias dependence of the expected RC time constants of the integrating circuit do not follow the observed temporal behavior. The magnitudes are expected to be many hundreds of nanoseconds as calculated from the dc impedance while the variation introduced by capacitance bias dependence should be approximately 15% compared to the observed 300%.

An alternative interpretation of the temporal results of Figure 5 is that charge collection occurs only by drift in the depletion region and diffusion beyond the depletion region. In these devices the ohmic contact is located laterally 5 μm from the Schottky barrier. Because of the low doping, the region between these two electrodes is depleted even at zero bias. The size of the Schottky contacts is 500 μm x 500 μm so that holes generated by an alpha particle must travel up to hundreds of micrometers laterally before being

C-3
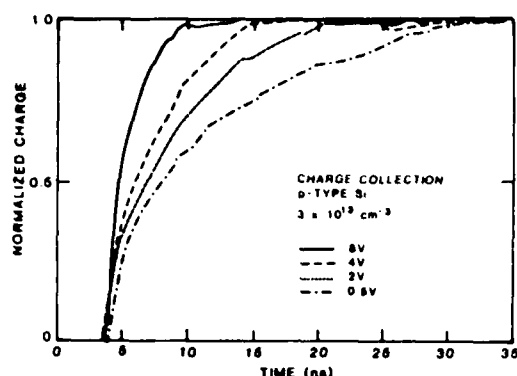
Figure 5. Charge collection data traces for various biases on a p-type Si Schottky diode with a substrate doping density of 3×10^{13} cm^{-3}.

collected at the ohmic contact. The geometry of these diodes requires that electric field lines within the depletion layer extend perpendicular to the surface, then, near the edge of the depletion layer, turn parallel to the surface before continuing toward the ohmic contact. Because of the low value of the electric field expected near the edge of the depletion layer, hole collection times of many nanoseconds should occur. The prompt risetime is therefore interpreted as being due to the rapid collection of electrons by drift perpendicular to the depletion region surface, while the gradual increase of charge toward saturation is the slow collection of holes. Similar mechanisms have been invoked to explain electron-beam-induced charge collection effects in GaAs.[14,15]

Doping and Bias Dependence of Collected Charge

Measurements of charge collection for various biases and doping densities were performed to examine the assumptions used to develop the McLean-Oldham (M-O) model. The results of these measurements on various GaAs and Si samples are shown in Figures 6-10. Figure 6 shows the prompt charge as a function of bias for GaAs and Si. At higher biases the data follow a square root dependence on bias while tending toward a weaker dependence at lower biases. The square root dependence is evident for both Si and GaAs samples and for doping densities of 3×10^{13} cm^{-3} in Si and $\sim 10^{15}$ cm^{-3} in GaAs. The deviation at high bias for the SI GaAs devices is due to depletion of the epi layer which was discussed previously.[11] The square-root bias dependence is predicted by the M-O model. It arises from the assumption of an effective funnel length over which all the potential drop occurs. The derivation of the square root dependence also assumes that the velocity of the minority carriers collected at a node is linearly proportional to the electric field and that the collection time is bias insensitive.[5] The first assumption appears to be inconsistent with modeling simulations;[9] however, our data support the prediction resulting from this assumption.

The flattening of the prompt charge at the lower biases in Figure 6 could be the result of various processes. Some diffusion charge is always collected within the "prompt" period. For long diffusion lengths and small depletion widths the amount of diffusion charge is approximately independent of bias. This charge will make a larger relative contribution to the collected charge at low bias where the collected charge due to drift is smaller. Another possible source for the low-bias deviation could arise from the weaker electric field across the depletion region. The M-O model assumes that the separation of charge at the outer edge of the radially expanding track occurs with a saturated velocity

for the majority carrier. If this velocity is less than saturated, the bias dependence of the collected charge approaches a one-third power.

Figure 7 shows prompt charge for GaAs devices as a function of doping density for a constant depletion width of 1 µm. The M-O model predicts that the charge collected due to funneling should depend on the doping density to the inverse one-third power. If the depletion width is held constant the dependence of charge on bias translates to a one-sixth power. This dependence is shown in the figure as a dashed line. Also shown is the predicted charge obtained by adding to the funneling contribution the charge obtained by drift in the depletion region (7 fC) and by diffusion during the prompt interval (9 fC). The agreement between the model and the data is very good. It is important to note that overall the dependence of the prompt collected charge on doping appears to be relatively weak for GaAs.

Figure 8 presents prompt and total collected charge for GaAs devices on SC substrates as a function of depletion width. The data include devices with concentrations from 3×10^{15} cm^{-3} to 7×10^{16} cm^{-3} and with epi thicknesses of ~ 10.5 µm. The prompt collected charge is observed to exhibit a linear dependence on depletion width and a weak dependence on doping concentration. The total collected charge, however, is relatively constant and has a value of ~ 105 fC for depletion widths greater than 0.8 µm. This observation implies that the diffusion length in the epi layer is long (~ 10 µm).

The linear dependence of the prompt collected charge on depletion width is consistent with the predictions of the M-O model. This observed dependence is a consequence of the square root dependence of depletion width on bias since the prompt charge also depends on the square root of bias. Using nominal values for the various parameters and a concentration of 3.4 $\times 10^{15}$ cm^{-3}, the prompt collected charge per micrometer (13.3 fC/µm) calculated from the model is in reasonably good agreement with that obtained from the slope in Figure 8 (15.8 fC/µm). In addition, the calculated effective funnel length, L_c, for a high electric field is in agreement with the experimentally derived value of ~ 1.8 W_d, where W_d is the depletion region width. This value is also consistent with previous results.[5,10,11]

Charge collection data as a function of bias for the lightly doped Si devices are shown in Figures 9 and 10. For the device doped to 1×10^{14} cm^{-3} (Fig. 9), prompt collected charge exceeds the charge generated in the depletion region. The prompt charge is also increasing with bias. The above effects are interpreted as arising from funneling. The dielectric relaxation time of ~ 0.25 nsec is well within the observation time used in the measurement (1.3 nsec). The total charge is independent of bias.

The bias dependence of collected charge for a device doped to 3×10^{13} cm^{-3} is shown in Figure 10. The prompt collected charge increases linearly with increasing bias and eventually equals the amount of charge generated within the depletion region. For this very low doping density, the dielectric relaxation time of the sample is ~ 2 nsec. Because of doping and geometry, the depletion region extends over about one-half of the track length. Charge collection by drift in the depletion region and by ambipolar diffusion in the neutral bulk should dominate charge collection and funneling should be negligible. An alternative explanation for these data is that the prompt collected charge is due to electrons flowing in the relatively small electric fields present and, hence, to
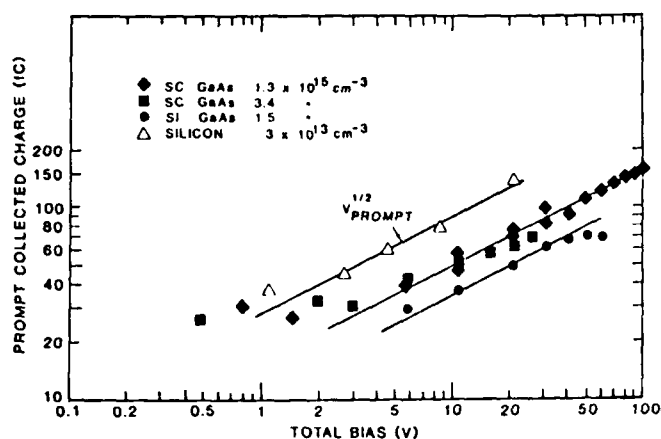
Figure 6. Collected prompt charge versus the sum of the applied and built-in bias for GaAs and Si Schottky diodes.
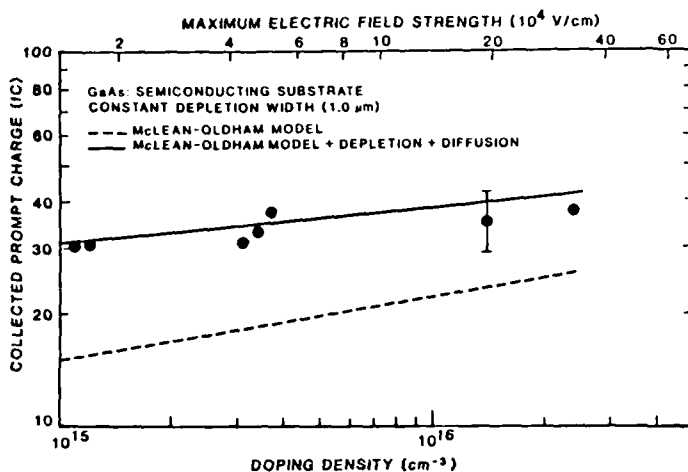
Figure 7. Collected prompt charge versus doping density for semiconducting GaAs diodes. The prediction from the McLean-Oldham model is discussed in the text.
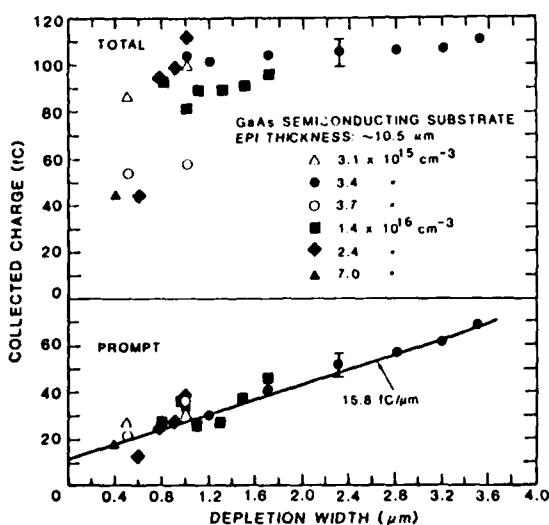
Figure 8. Collected prompt and total charge versus depletion width for semiconducting GaAs diodes for various doping densities.
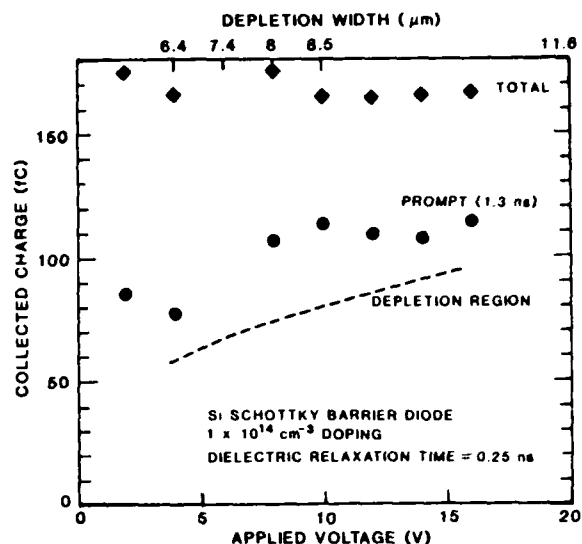
Figure 9. Collected prompt and total charge as a function of applied voltage for 5.0 MeV alpha particles incident on a p-type Si Schottky diode (doping density: 1×10^{14} cm^{-3}). Also shown are the values for the equilibrium depletion width (upper scale) and the amount of charge generated in the depletion layer by the alpha particle (dashed line).
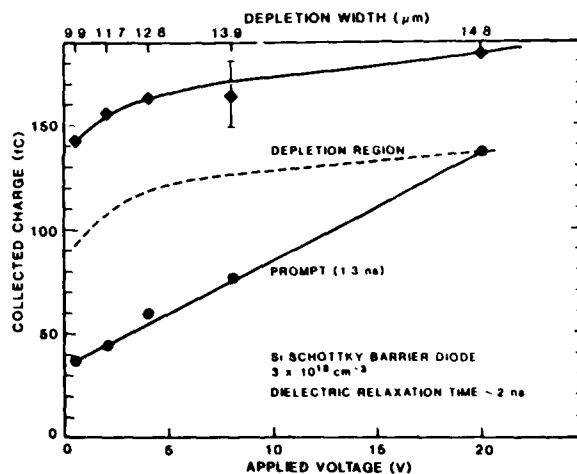
Figure 10. Collected prompt and total charge as a function of bias for a p-type Si Schottky diode (doping density: 3×10^{13} cm^{-3}).

a slow drift process, even within the depletion region. As the electric field increases, more prompt charge is collected. No risetime variations in the prompt component of the waveform of Figure 5 were observed because of bandwidth limitations. The total collected charge shows a much weaker dependence on bias. The minority-carrier lifetime in these materials is estimated to be ≥ 1 μsec, so the diffusion length is very long and, therefore, it is expected that all of the charge generated by the alpha particle, 220 fC, should be collected. However, the total charge collected is less than this value for the range of biases used. Furthermore, at high biases, the waveforms show that mostly prompt charge is collected. Further studies are planned to resolve this issue.

SUMMARY

Charge collection and transient current measurements on Si and GaAs Schottky diodes bombarded with alpha particles have been made to study SEU phenomena. Over the doping density range studied, the instrumentation bandwidth was insufficient to measure directly the risetime and collection times for charge funneling. Upper limits of 120 psec and 300 psec were determined for risetimes and collection times, respectively. Approaches to increasing the effective instrumentation bandwidth and to decreasing signal distortion are being investigated.

The bias and doping dependences of the magnitude of charge collection were also investigated for these devices. Predictions from the phenomenological McLean-Oldham model of a doping dependence to the 1/6 power for a constant depletion width and a bias dependence to the 1/2 power were found to be in good agreement with the measurements. Although some of the assumptions used in deriving that model appear to be inconsistent with computer simulations, model predictions for charge collection from alpha-particle-bombarded devices are consistent with experiment.

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APPENDIX D

RADIATION-INDUCED HOLE TRAPPING AND INTERFACE STATE CHARACTERISTICS OF Al-GATE AND POLY-Si GATE MOS CAPACITORS*

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ABSTRACT

Using the techniques of thermally stimulated current and high-frequency C-V measurements, the device processing dependence of radiation-induced hole traps and interface states in MOS capacitors has been investigated. It was found that the fabrication of poly-Si gates caused all investigated gate oxides to resemble those grown by pyrogenic techniques. The role of post-oxidation annealing (POA) in hole trap formation and interface state generation was investigated. The measurements imply that POA causes a "weakening" of bonds in SiO_2 which can become hole traps, and, in the presence of OH, lead to the annihilation of certain types of hole traps while generating new types of hole traps and interface states. Possible models and interface state distributions are discussed. Midgap voltage shifts were found not to be generally valid measures of hole trapping in these MOS devices.

INTRODUCTION

The role of hole trapping and interface state generation in the degradation of MOS devices exposed to ionizing radiation is well established.[1] Various device fabrication processes have been developed in order to minimize the radiation sensitivity of MOS electronic devices.[2] Although these process variations do lead to more radiation tolerant devices, the cause of this increased radiation hardness is not well understood. To progress beyond the present level of radiation sensitivity so that ultrahard MOS devices can be "engineered", a detailed understanding of processing effects is needed.

Previously reported differences in hole trapping characteristics between various fabrication processes in Al-gate MOS devices have shown for the first time that different fabrication processes result in different types of hole trapping sites.[3,4] For gate oxides grown using dry oxygen, the increased radiation sensitivity caused by post-oxidation anneal (POA) is a result of an increase in the number of the same type of hole trapping sites present before POA. For pyrogenically grown oxides, different hole trapping sites were observed. In these samples, the POA not only results in a decrease in the number of the type of trapping sites present before POA, but also generates new types of sites. It was speculated that the role of hydrogen (H) or the hydroxyl group (OH) plays a critical role in these observed differences between dry and pyrogenic oxides.[4]

The present investigation extends the previous measurements to include the more commercially prevalent poly-Si gate MOS devices. It is generally more difficult to produce radiation-insensitive devices using poly-Si gate technology. A major purpose of this investigation is to determine the cause of this difficulty. The experimental techniques used are thermally stimulated current (TSC) and high-frequency capacitance-voltage (C-V) measurements. A comprehensive series of TSC measurements on irradiated MOS capacitors was undertaken to determine the distribution of trapped holes and their associated thermal activation energies. By measuring TSC signatures from a controlled set of MOS capacitors encompassing various MOS device fabrication processes, differences in trapping sites caused by these processes can be determined. The TSC measurements were performed in conjunction with C-V techniques to monitor the amount of charge in the oxide and at the $Si-SiO_2$ interface. By combining TSC and C-V measurements, interface state charge was determined and the effects of process variations on interface state generation were examined.

EXPERIMENTAL DETAILS

The TSC technique has previously been described in detail.[3,4] A summary is given here. A TSC measurement is made by applying a bias across the insulator while recording the current flowing in the device as the sample temperature is raised. The measurement is repeated to determine the background current, which can be caused by displacement currents and by carrier injection. The difference between the two currents is interpreted as arising from the thermal depopulation of charged traps. For samples which have previously been irradiated under positive bias, a TSC measurement with a negative bias applied to the gate electrode will cause holes initially trapped near the $Si-SiO_2$ interface to be swept toward the gate and produce current peaks in the TSC spectrum at some temperatures. This process will also cause a positive flatband voltage shift as detected by C-V measurements. By using a bias sufficiently high that retrapping of the charge does not occur, the temperature scale of the TSC spectrum can be converted to an activation energy scale using the analysis of Simmons.[5] The parameter values used in the TSC measurements and analysis are those reported previously.[3,4] The Co^{60} irradiation procedure has also been previously described.[4] The measurement system has recently been automated to increase throughput of samples and to improve reproducibility of the results.

Devices were fabricated at Sandia National Laboratories. All capacitors were prepared on 0.8-1.2 Ω-cm n-type Si of (100) orientation. Al-gate device fabrication processes were previously descirbed.[4] For poly-Si gate devices, pyrogenic gate oxides were grown in steam at 850°C to a thickness of 1150 Å. Dry gate oxides were grown in dry oxygen at 1000°C to a thickness of 970 Å. Radiation-soft oxides were obtained by performing a POA in nitrogen at 1100°C. Poly-Si gates were phosphorus doped, then metallized with Al-Si and sintered at 450°C in nitrogen. No ion contamination was observed in any of these samples.

RESULTS AND DISCUSSION

Hole Trap Densities

Representative results of trapped hole density distributions derived from TSC measurements on Al-gate samples, which were previously reported,[4] are shown in Figure 1. For dry oxides, we observed a single activation energy distribution, peaked at ~1.3 eV, consisting of overlapping distributions which are
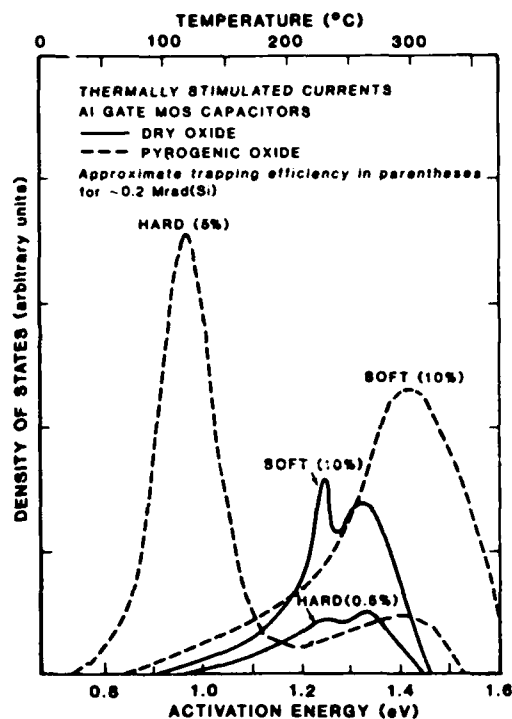
Figure 1. TSC spectra for irradiated Al-gate dry and pyrogenic oxides.

Figure 2. TSC spectra for irradiated poly-Si gate radiation-hard pyrogenic oxides.

Figure 3. TSC spectra for irradiated poly-Si gate radiation-hard dry oxides.

probably centered at 1.25 and 1.35 eV. In dry-processed thermal oxides, the same activation energy distributions exist for both radiation-hard and radiation-soft devices. Radiation-hard dry oxides simply have less traps than their soft counterparts. In contrast to dry oxides, pyrogenic-processed thermal oxides have more complex activation energy distributions, and major differences occur between hard and soft pyrogenic oxides. Radiation-soft pyrogenic oxides contain a single very broad peak, skewed to low energies, which starts at ~0.8 eV and has a maximum in the range from 1.3 to 1.5 eV. Radiation-hard pyrogenic oxides, however, have a well-defined peak at ~1.0 eV, and a small, broad, poorly defined peak near 1.4 eV. The interpretations of these results were that the local structure of hole traps in oxides grown by dry processes is different from that in oxides grown by pyrogenic processes, and that the POA also affects these local structures ifferently.[4]

Results of new TSC measurements on poly-Si gate samples are now described. In Figure 2 the density distributions of activation energies for radiation-hard pyrogenic oxides are shown for various irradiation doses. A large, well-defined peak occurs with an activation energy maximum in the region of ~0.95 eV while a small, broad, poorly defined peak occurs near 1.4 eV. The curves generally increase in amplitude as a function of dose with little change in shape. Saturation of the 0.95 eV peak is observed to occur at ~200 krad(Si). The activation energy distributions of trapped holes for radiation-hard dry oxides are shown in Figure 3. The locations of the peaks are generally the same as those for the pyrogenic oxide samples of Figure 2. The amplitude variation with dose, however, is different. The amplitude of the peak at ~1.4 eV is the same as that observed for the pyrogenic samples. It saturates at a dose as low as 20 krad(Si). The 0.9 eV peak is not visible at 20 krad(Si), but slowly grows with increased dose to approximately the same amplitude as the 1.4 eV peak. Note that the amplitude for this peak in these dry oxide samples is considerably smaller than in the pyrogenic oxide samples. Moreover, as the dose
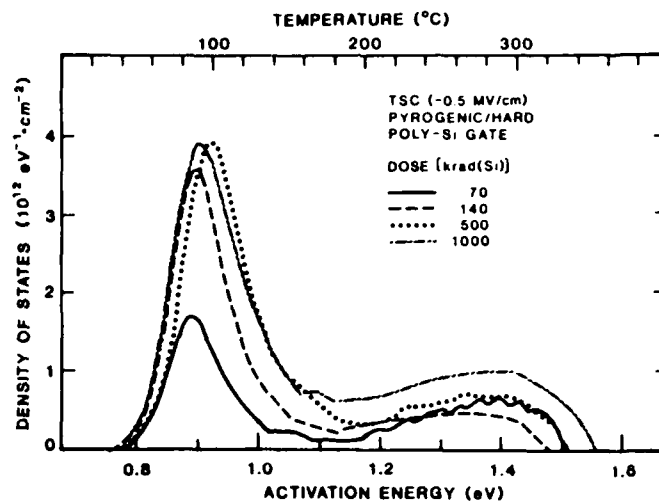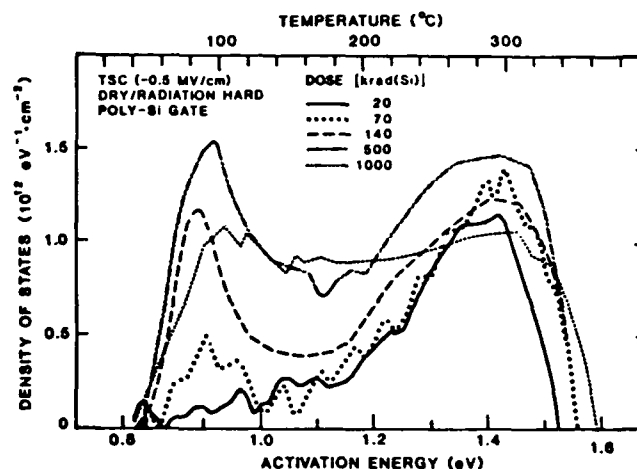
increases a new feature is revealed in the distribution for these dry samples. The amplitude in the activation energy region near 1.1 eV increases, resulting in a rectangular-like distribution of activation energies. Even though part of the contribution to this region can be attributed to overlap from the 0.9 and 1.4 eV peaks, the shape and dose dependence suggests that a new trap site occurs.

The results for radiation-soft oxides are shown in Figure 4. Except for amplitude, identical results were obtained for both dry and pyrogenic oxides. One very broad peak, skewed to low energies, starts at ~0.8 eV and has a maximum near ~1.4 eV. The position of this maximum varies from 1.3 to 1.5 eV and saturates for doses ⩾200 krad(Si). No reproducible structure was observed within these distributions.

A summary of the position of the various peaks observed in the distribution of activation energies for poly-Si gate samples is shown in Figure 5. It is seen that radiation-hard oxides are very similar, independent of the oxide growth process. The same is true for radiation-soft oxides. Comparison with Figure 1 shows that the distribution for poly-Si gate oxides corresponds closely to those for devices with pyrogenically grown Al-gate oxides. The process of fabricating the
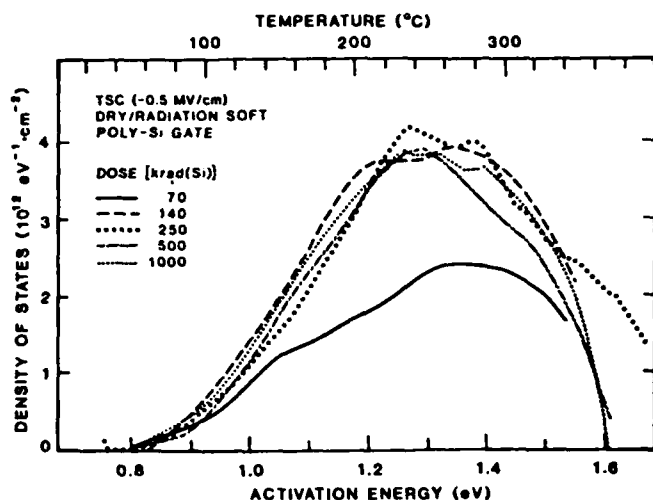
Figure 4. TSC spectra for irradiated poly-Si gate radiation-soft dry oxides.
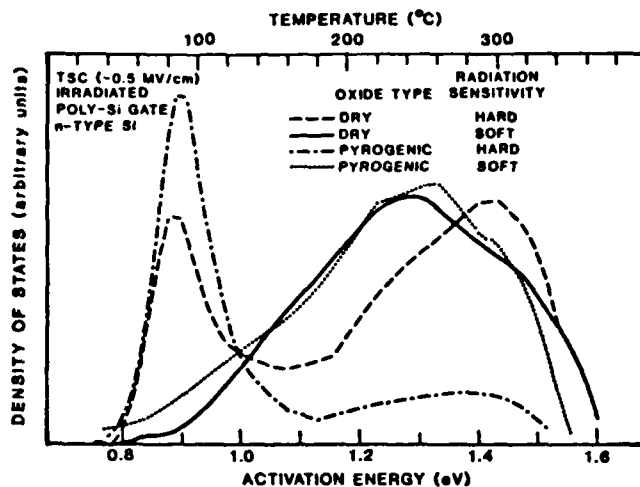
Figure 5. Comparison of the peak positions for irradiated poly-Si dry and pyrogenic oxide samples.

poly-Si gate appears to cause hole traps in both pyrogenic and dry oxides to resemble those observed in pyrogenic oxides contained in Al-gate devices.

The integrated TSC current, defined as the TSC charge density, for each of the process variations is shown in Figure 6. For all poly-Si gate samples, the charge increases with dose and saturates at ~200 krad(Si). For radiation-soft samples, the saturation level for the pyrogenic oxides is greater than for the dry. Saturation levels for both types of radiation-hard oxides are similar. For Al-gate technologies, the data are more scattered with saturation occurring between 200 to 300 krad(Si). Saturation levels for Al-gate radiation-soft oxides, both dry and pyrogenic, and radiation-hard pyrogenic oxides are similar. Only two data points are available for Al-gate radiation-hard dry oxides; they indicate that even above 1 Mrad(Si) such oxides are radiation tolerant.

An approximate estimate of the hole trap capture cross section can be obtained from the dose required to reach saturation. Hole trapping kinetics are assumed to be first order, resulting in an exponential dependence of TSC charge on dose. We define saturation to
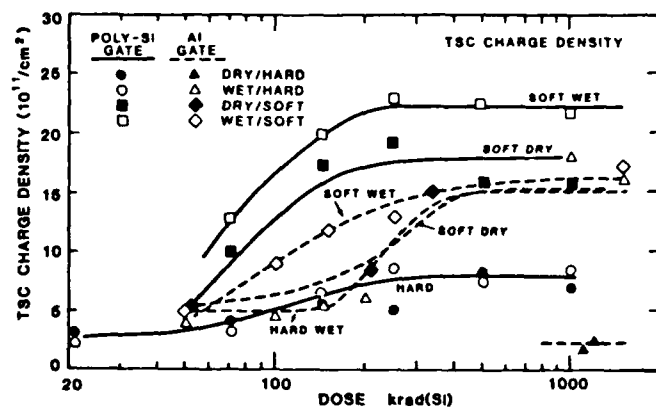
Figure 6. TSC charge density (obtained by integrating the TSC current) for various oxide processes.

occur when the exponential factor, which is the product of the cross section and the generated hole density, equals three. For saturation at a dose of 200 krad(Si), the capture cross section is ~1 x 10^{-13} cm^{-2}. This value is within the 10^{-13} to 10^{-14} cm^{-2} range reported in the literature.[6] For all samples except poly-Si gate radiation-hard dry oxides, the shape of the distribution of trapped holes does not change significantly with dose. The same approximate cross section, therefore, appears to apply to all hole trapping sites in these present devices. For poly-Si gate radiation-hard dry oxides, the site at ~1.1 eV seems to have a different cross section. Further measurements will be needed to accurately evaluate the magnitudes of cross sections for these various sites.

In our earlier paper on Al-gate samples,[4] we associated the difference between pyrogenic and dry oxide hole trapping to the role of H or OH. The similarity of the present results for poly-Si gate samples with those for the pyrogenic Al-gate devices implies that H or OH is present. The process of fabricating the poly-Si gate utilizes a high-temperature LPCVD reaction (600°C) with silane that involves the presence of large amounts of H. Also the n$^+$ doping of the gate and associated diffusion utilizes PH$_3$ at 900°C. Hydrogen, at high temperature, is therefore available for incorporation into the oxide during this processing step.

The specific procedure by which H is incorporated into radiation-hard oxides does affect the hole trap site formation. For pyrogenic oxides, the H or OH is initially incorporated during oxide growth. Nearly identical spectra are observed consisting of two peaks located at ~0.95 eV and ~1.4 eV. However, for dry oxides, where H or OH is incorporated during the poly-Si gate formation, three features are observed consisting of the two peaks described above for the pyrogenic oxides plus a new feature at ~1.1 eV. The dose dependences of the peaks at ~0.9 eV and ~1.4 eV behave similarly to those in the pyrogenic oxides while the feature at ~1.1 eV has a different cross section.

In contrast, radiation-soft samples, which have undergone a POA, have identical spectra. This is true even though in one case (poly-Si gate) the POA occurs before the H is introduced. In the other case (Al-gate) the POA occurs after the introduction of H. To explain these observations, it is postulated that the POA introduces a precursor site that, in the presence of H at high temperature, removes various trapping sites (those observed in all the radiation-hard processes) and introduces a new set of other trapping sites (those for radiation-soft oxides). The effect of the H may occur either during POA (for pyrogenic oxides) or later during

gate formation (for poly-Si gate samples). The Bond Strain Gradient models based on the XPS studies of MOS devices by Grunthaner et al.[7] invoked OH as such a "catalyst" that enhances the mobility of certain defects in SiO_2 near the SiO_2-Si interface.

The above observations suggest the following model. In oxides without the presence of appreciable OH, the radiation-induced trapped holes are stable. The POA simply introduces more of these sites by "weakening" bonds in the SiO_2 lattice near the Si-SiO_2 interface. For oxides which have not undergone POA, the presence of OH may allow the annihilation of these traps and the formation of new types of trap sites. For those oxides which have undergone POA, the POA-induced precursors, in conjunction with the OH, could annihilate these new sites and produce stable hole traps which have the higher activation energies observed. It is not known if the presence of OH results in the migration of defects to new physical locations in the oxide (as in the Grunthaner models[7]) or simply modifies the existing trap structure. Whether these conversions occur during device processing or irradiation also cannot be determined from our measurements.

Interface States

To investigate the effects of process variations on the generation of radiation-induced interface states, high-frequency (1 MHz) C-V measurements were taken before and after each post-irradiation TSC measurement. After the TSC measurement, the C-V curves closely resembled the C-V data obtained prior to irradiation, indicating that both irradiation-induced trapped holes and interface states had been eliminated. From the C-V data, midgap and flatband voltage shifts were obtained. As described earlier, the amount of radiation-induced oxide charge (trapped holes) present near the Si-SiO_2 interface was determined from the integrated TSC current. The difference between the charge density corresponding to the C-V voltage shift and the TSC charge density gives the net interface-state-induced charge density for a particular surface potential. This interface charge density is equivalent to the integration over the Si bandgap of the occupancy of donor interface states minus the occupancy of acceptor interface states.[8] Here we only investigate midgap and flatband conditions.

After irradiation the C-V curves were generally shifted in a negative voltage direction, indicative of the introduction of positive charge, and showed stretch-out, generally indicative of the presence of interface states.[8,9] The shifts at midgap are greater than those at flatband. All the Al-gate samples showed the above behavior except for dry radiation-hard oxides. For the poly-Si gate devices, the radiation-soft samples showed the same behavior. The radiation-hard oxides, on the other hand, displayed little or no flatband shift up to a dose of approximately 300 krad(Si). At higher doses, the flatband voltage shifted positive. In contrast, the midgap shifts were always negative. Al-gate radiation-hard dry oxides exhibited very small negative shifts at doses up to 1 Mrad(Si).

The net interface state charge density as a function of dose for radiation-hard oxides is shown in Figures 7 and 8 for poly-Si and Al-gate samples, respectively. There is very little difference between the results for dry and pyrogenic poly-Si gate devices with those for pyrogenic Al-gate samples. The Al-gate dry oxides show very little radiation sensitivity, which is consistent with the TSC results. The charge at flatband is always negative, with a suggestion of saturation at 1 Mrad(Si) for the Al-gate, but not for the poly-Si gate, samples. The net interface charge density at midgap rises from near zero (negative for poly-Si gate, positive
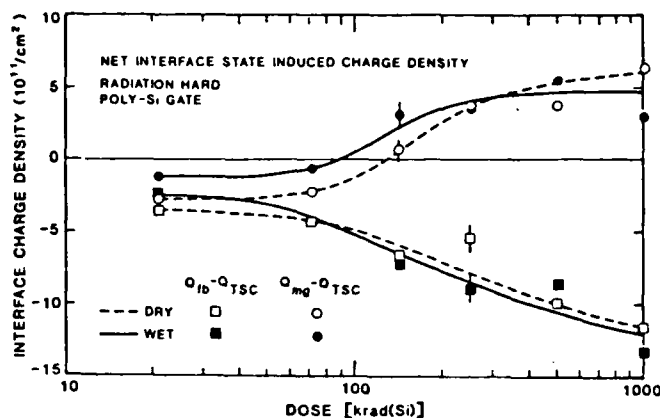
Figure 7. Interface charge density for irradiated poly-Si gate radiation-hard oxides.
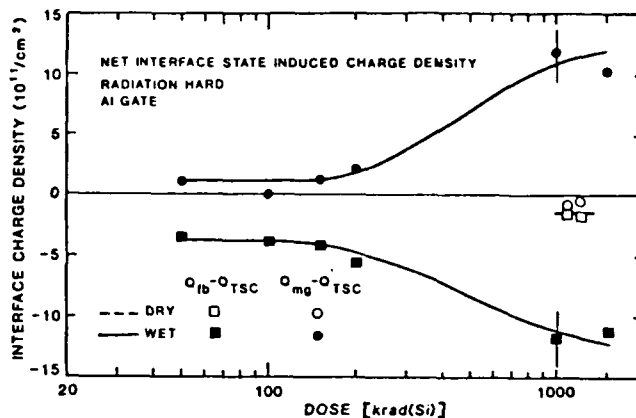
Figure 8. Interface charge density for irradiated Al-gate radiation-hard oxides.

for Al-gate) to a positive charge with increasing dose. Saturation occurs at about 300 krad(Si) for the poly-Si gate oxides. Insufficient data are available for the Al-gate oxides, but saturation appears to occur at least by 1 Mrad(Si).

The net interface-state-induced charge for radiation-soft devices is shown in Figures 9 and 10 for poly-Si and Al-gate samples, respectively. Here the behavior is very different from that for radiation-hard devices. Above 100 krad(Si), all charge is positive. No saturation is observed. For the Al-gate dry oxides, the variation with dose is very weak. The other processes show charge increasing monotonically with dose. It is observed that charge at midgap is always larger than at flatband and that pyrogenic oxides have greater net interface charge densities than dry oxides. The magnitudes of the charge densities for the poly-Si gate devices are approximately twice as large as those for the corresponding Al-gate devices.

It was previously suggested that midgap voltage shifts obtained from C-V data are a useful measure of hole trapping in MOS capacitors.[10] This suggestion is based on the observed correlations between the density of interface states and the results of ESR measurements on the P_b center.[11] The data presented in Figures 7-10 indicate that this suggestion is not generally true. At midgap there is a contribution to the voltage shift from the interface states, with the magnitude of this contribution depending on device processing.

The data presented in Figures 7-10 for the net
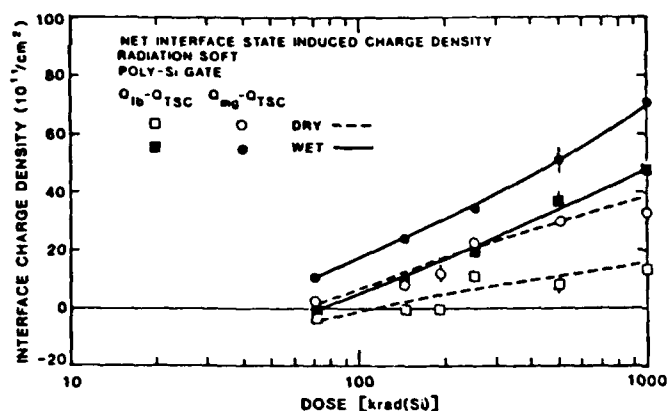
Figure 9. Interface charge density for irradiated poly-Si gate radiation-soft oxides.
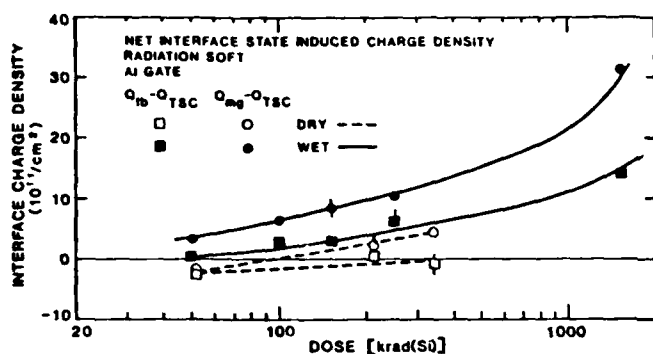
Figure 10. Interface charge density for irradiated Al-gate radiation-soft oxides.

interface-state-induced charge require a non-symmetric interface-state distribution about midgap. The interpretation of the ESR measurements of P_b centers assigns a distribution with donors predominantly below midgap and acceptors predominantly above midgap.[11] For radiation-hard oxides, the present measurements require that more donor states be above midgap than acceptor states below. The difference in the number of these states saturates at ~200 krad(Si). Between midgap and flatband the predominant interface state must still be an acceptor. For radiation-soft oxides, however, the predominant interface state in the upper half of the bandgap must be a donor. The number of these donor states increases with dose. The number of acceptors below midgap must be less than the number of these donors above midgap.

A suggested interface-state distribution which would explain these observations would consist of the P_b-associated interface states (donors predominantly below midgap, acceptors above) and an additional donor distribution predominantly above flatband. (Various interface-state distributions have been reported including those with peaks near and above flatband.[12]) For radiation-hard oxides, this second distribution would saturate at about 200 krad(Si) while the P_b-associated interface states would continue to increase. For radiation-soft oxides, the second distribution would grow much faster than the P_b associated one. More extensive analysis of the data as a function of surface potential, coupled with direct measurements of the interface-state distribution, will be required to obtain a complete interface-state distribution of donor and acceptor states.

The relative contributions of trapped holes and interface states to radiation sensitivity can be observed by comparing Figures 7-10 with Figure 6. The relative radiation tolerance of hard oxides results from the cancellation of trapped hole and interface-state charges measured at flatband. At midgap, the saturation at fairly low doses of both trapped holes and interface states results in small voltage shifts. The increasing generation of interface states with dose is the principal cause of the radiation sensitivity of the radiation-soft oxides. For MOS transistors, one measure of radiation sensitivity is threshold voltage shift. As has been discussed by others, the MOS capacitor inversion potential should be used for determination of radiation sensitivity.[10,13,14]

A comparison of the trends in the present samples for both hole trapping and interface-state generation indicates that all radiation-soft oxides containing H or OH have very similar characteristics. All radiation-hard oxides containing H or OH are also similar to each other. Within a particilar gate process, pyrogenic oxides have more interface states than dry oxides. This trend also is generally observed for hole trapping. As discussed previously for hole trap distributions, the presence of OH may enhance the mobility of defects. These defects, upon arrival at the interface, could lead to the generation of interface states.[7] The magnitudes of the interface-state charge density for radiation-hard oxides containing H or OH are similar. However, for radiation-soft oxides containing H or OH, the poly-Si gate devices generally have more interface states at a given dose than do Al-gate oxides. The introduction of H into the oxide at high temperature is therefore more detrimental during gate electrode processing than during oxide growth.

CONCLUSIONS

Using the techniques of thermally stimulated current and high-frequency C-V measurements, we have investigated the device processing dependence of radiation-induced hole traps and interface states in MOS capacitors. In terms of hole trap distributions and net interface charge densities, poly-Si gate devices resemble pyrogenic-grown Al-gate samples. The role of hydrogen or the hydroxyl group was discussed. It is believed that the role of post-oxidation annealing, which produces radiation sensitive oxides, is to "weaken" bonds in the SiO_2 which then can become hole traps. In these oxides, the introduction of OH may allow the annihilation of these traps, the production of new types of hole traps, and the generation of donor-like interface states, predominantly above the flatband potential. Differences in interface-state distributions between radiation-hard and radiation-soft oxides may arise from the more rapid growth of this donor site in the latter case. Oxides were observed to be radiation-hard either when the hole trap and interface-state charges partially cancelled or when both charges saturated with dose. Which of the above occurs depends on the surface potential used during the measurement of the voltage shift. It was also found that midgap voltage shifts are not a generally valid measure of hole trapping in MOS oxides.

The TSC technique has been shown to be a valuable tool in the study of the characteristics of hole trap sites in MOS devices. Coupled with other measurements, such as C-V, it can contribute to a more complete understanding of radiation effects in these devices.

ACKNOWLEDGMENTS

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INVESTIGATION OF TRAPPED OXIDE CHARGE IN MOS DEVICES*

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ABSTRACT

Using the techniques of thermally stimulated current and high-frequency C-V measurements, the device processing dependence of hole traps and interface states in MOS capacitors has been investigated. Both radiation- and bias-temperature-stress-induced degradation mechanisms were studied. It was found that the fabrication of poly-Si gate electrodes caused all investigated gate oxides to resemble those grown by pyrogenic techniques. The midgap voltage shift was found to be not a generally valid measure of hole trapping in the present devices. The TSC technique, coupled with C-V measurements, is shown to be a valuable tool for characterizing hole traps and interface states in MOS devices.

TRAPPED OXIDE CHARGE and interface states seriously affect the performance and reliability of silicon devices. These traps are created, activated, or filled in MOS devices when charge is produced in the oxide by ionizing radiation, injection, or bias-temperature stressing. The properties of hole traps and interface states are strongly process-dependent. Such dependences give clues to the nature of these centers and their physical and chemical characteristics. At present, most techniques used to reduce charge trapping and minimize the formation of interface states involve processing procedures that are empirical. To progress beyond the present level of tolerance to degradation mechanisms, a detailed understanding of the characteristics of oxide layers in MOS devices is necessary.

The purpose of the present investigation was to develop and utilize techniques that would yield basic information regarding the nature of

hole traps which have been found to exist preferentially near the Si-SiO$_2$ interface in MOS devices. The experimental technique used in this investigation is thermally-stimulated-current (TSC) measurements on MOS capacitors.[1,2] A comprehensive series of TSC measurements was undertaken to determine the density of trapped holes and their associated thermal activation energies. These measurements were performed on MOS capacitors in conjunction with conventional capacitance-voltage (C-V) techniques to monitor the amount of charge in the oxide. By combining TSC and C-V measurements, interface state charge was determined and the effects of process variations on interface state generation were examined.

EXPERIMENTAL TECHNIQUE

The TSC method is one of a number of techniques based on thermally stimulated relaxation[3] phenomena which includes thermally stimulated exoemission and capacitance, emission time spectroscopy, and DLTS. These techniques have been used for many years in the study of solids.[4] Extension of the thermally stimulated current technique to the study of hole traps in SiO$_2$ films is a straightforward application of previous work.

A TSC measurement is made by applying a bias across the insulator while recording the current flowing in the devices as the sample temperature is raised (Figure 1). This measurement is repeated to determine the background current, which can be caused by displacement currents and by carrier injection (Figure 1b, curve 2). The difference between the two currents is interpreted as arising from the thermal depopulation of charged traps (Figure 1c). For samples which have previously been irradiated under positive bias, a TSC measurement with a negative bias applied to the gate electrode will cause holes initially trapped near the Si-SiO$_2$ interface to be swept toward the gate and produce current peaks in the TSC spectrum at some temperatures. This process will also cause a positive flatband
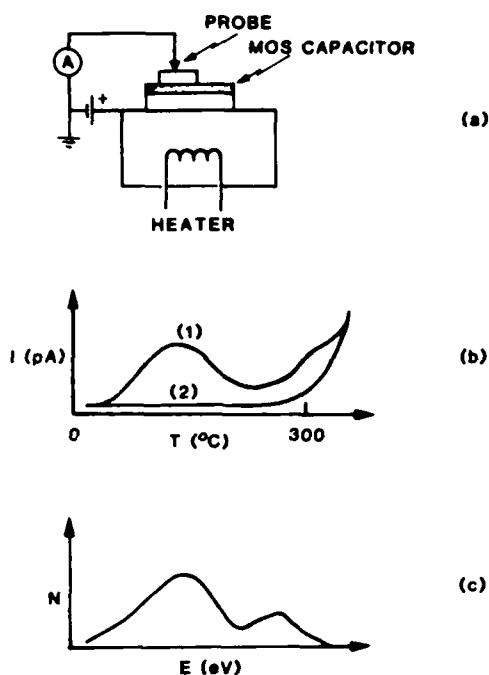
Fig. 1 — Schematic representation of the TSC technique: (a) experimental configuration; (b) example plots of experimental currents where (1) is the first measurement while (2) is the second measurement made immediately after (1) is taken and the device is allowed to cool; (c) resultant TSC spectrum.

voltage shift as detected by C-V measurements. In cases where the sample is not previously irradiated, the TSC measurement under either bias condition is the equivalent of bias-temperature (BT) stresing and can also result in the introduction of charge into the oxide. By using a bias sufficiently high that retrapping of the charge does not occur, the temperature scale of the TSC spectrum can be converted to an energy scale using the approach of Simmons.[5]

The raw data from a TSC measurement of current versus temperature is a signature of the thermal relaxation phenomena occurring in the oxide. To extract information regarding the microscopic nature of trapped holes, it is necessary to convert such data into activation energies. Simmons and coworkers have treated the problem of extracting activation energies from TSC data for the case where no retrapping occurs (such as at high fields).[5,6] Simmons' model assumes that there is a continuous distribution of occupied traps. He argues that without retrapping, the thermally activated process is governed by first-order kinetics and assumes that the "attempt-to-escape" frequency (or, equivalently, the capture cross section) is energy independent. Using this model,[5,6] Simmons showed that the TSC spectrum is a direct image of the occupied trap distribution and temperature is linearly related to the activation energy for thermally-stimulated emission of trapped charge.

Devices were fabricated at Sandia National Laboratories. All capacitors were prepared on 0.8-1.2 Ω-cm n-type Si of (100) orientation. For Al gate capacitors, dry oxides were grown at 1000°C to a thickness of approximately 700 Å, while pyrogenic oxides were steam grown at 850°C to 1000 Å. The steam was generated by in situ burning of H_2 in an O_2 atmosphere. For poly-Si gate devices, pyrogenic gate oxides were grown in steam at 850°C to a thickness of 1150 Å. Dry gate oxides were grown in dry oxygen at 1000°C to a thickness of 970 Å. Radiation-soft oxides were obtained by performing a post-oxidation anneal in nitrogen at 1100°C. Poly-Si gates were phosphorus doped, then metallized with Al-Si and sintered at 450°C in nitrogen.

RESULTS

Representative results of trapped hole density distributions derived from TSC measurements on irradiated Al-gate samples are shown in Figure 2.[2] For dry oxides, we observed a single activation energy distribution, peaked at ~1.3 eV, consisting of overlapping distributions which are probably centered at 1.25 and 1.35 eV. In dry-processed thermal oxides, the same activation energy distributions exist for both radiation-hard and radiation-soft devices. Dry, hard oxides simply have less traps than their soft counterparts. In contrast to dry oxides, pyrogenic-processed thermal oxides have more complex activation energy distributions, and major differences occur between hard and soft pyrogenic oxides. Radiation-soft pyrogenic oxides contain a single very broad peak, skewed to low energies, which starts at ~0.8 eV and has a maximum in the range from 1.3 to 1.5 eV. Radiation-hard pyrogenic oxides, however, have a well-defined peak at ~1.0 eV, and a small, broad, poorly defined peak near 1.4 eV. The interpretation of these results is that the local structure of hole traps in oxides grown by dry processes is different from that in oxides grown by pyrogenic processes, and that annealing also affects these local structures differently.[2]

A summary of the position of the various peaks observed in the distribution of activation energies for irradiated poly-Si gate samples is shown in Figure 3.[7] It is seen that radiation-hard oxides are very similar, independent of the oxide growth process. The same is true for radiation-soft oxides. Comparison with Figure 2 shows that the distribution for poly-Si gate oxides corresponds closely to those for devices with pyrogenically grown Al-gate oxides. The process of fabricating the poly-Si gate appears to cause hole traps in both pyrogenic and dry oxides to resemble those observed in pyrogenic oxides contained in Al-gate devices. Discussion of these comparisons of process variations and models for these observations are given in Reference 7.

A TSC measurement on an unirradiated sample is the equivalent of a BT stress.[1] In oxides contaminated with ions, the TSC measurement can

Fig. 2— TSC spectra for irradiated Al-gate dry and pyrogenic oxides.
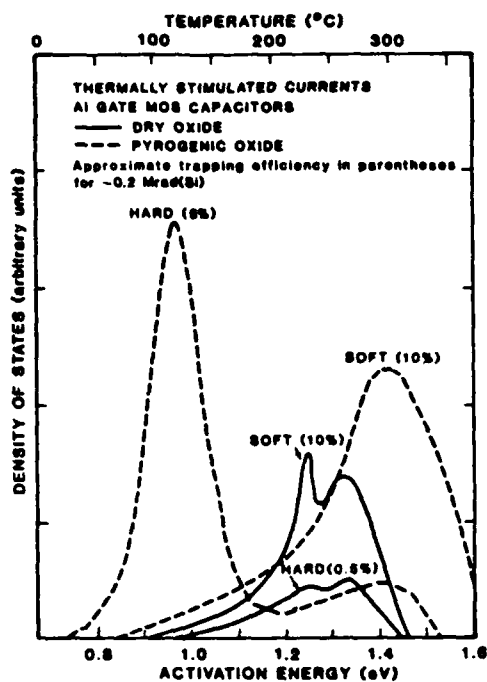
Fig. 3— Comparison of the peak positions for irradiated poly-Si dry and pyrogenic oxide samples.

be used to identify the species present.[8] In non-contaminated samples a BT instability is observed. The BT instability occurs when net charge is introduced into an oxide that is stressed under bias at elevated temperatures. Since in most measurements the low magnitude of the bias and temperature usually precludes charge injection, the process is often interpreted as the removal of charge of one polarity, resulting in the presence of charge of the opposite polarity in the oxide.[9] The location of the sites at which this process occurs has been assigned by various investigators to be either the $Si-SiO_2$[10] or gate electrode-SiO_2 interface.[1] In either case, the BT instability probes the bonding in the oxide and should therefore supply information on the differences in oxides produced by various processes.

BT-instability differences between dry and pyrogenic oxides are summarized in the schematic TSC spectrum shown in Figure 4. The fundamental point is that the activation energies are different, again implying that there are different structural sites in pyrogenic versus dry oxides. The spectrum for pyrogenic oxides is more complex than the single peak in the spectrum for dry. Pyrogenic oxides therefore have a more complex physical and chemical nature than do dry oxides.

To investigate the effects of process variations on the generation of radiation-induced interface states, high-frequency (1 MHz) C-V measurements were taken before and after each post-irradiation TSC measurement. From the C-V data, midgap and flatband voltage shifts were obtained. The amount of radiation-induced oxide
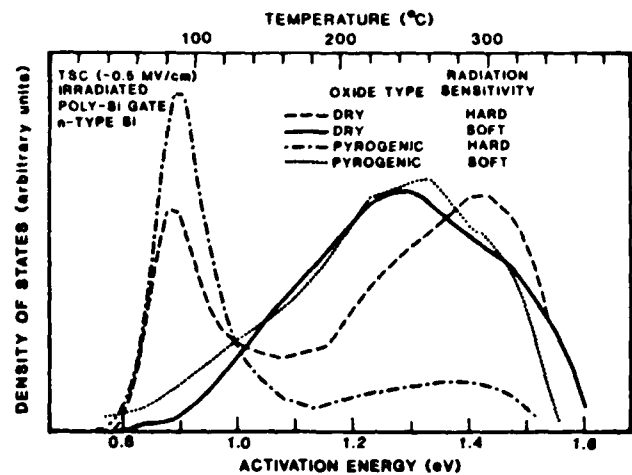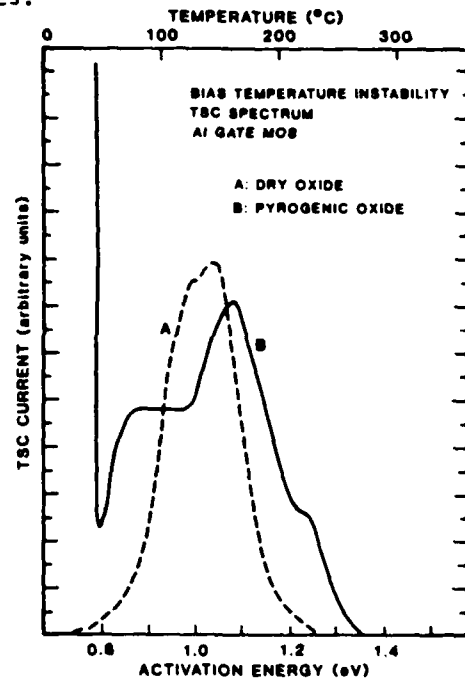
Fig. 4— Comparison of the TSC spectra associated with the negative BT instability for pyrogenic and dry oxides. The scale for the TSC current is arbitrary.

charge (trapped holes) present near the $Si-SiO_2$ interface was determined from the integrated TSC current. The difference between the charge density corresponding to the C-V voltage shift and the TSC charge density gives the net interface-state-induced charge density for a particular surface potential. This interface charge density is equivalent to the integration over the Si bandgap of the occupancy of donor interface states minus the occupancy of acceptor interface states.[11] Here we only investigate midgap and flatband conditions.
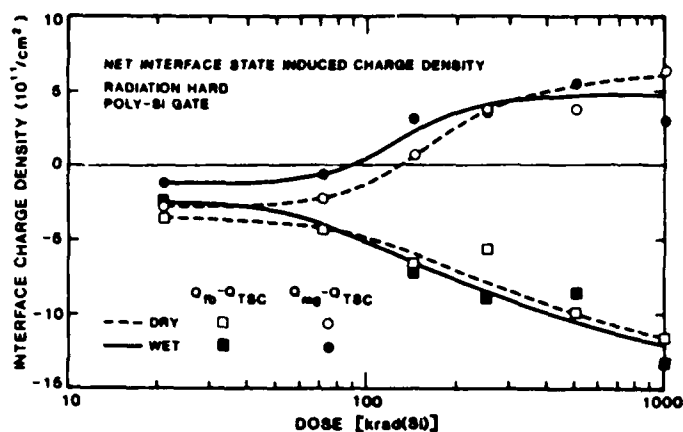
Fig. 5 — Interface charge density for irradiated poly-Si gate, radiation-hard oxides.
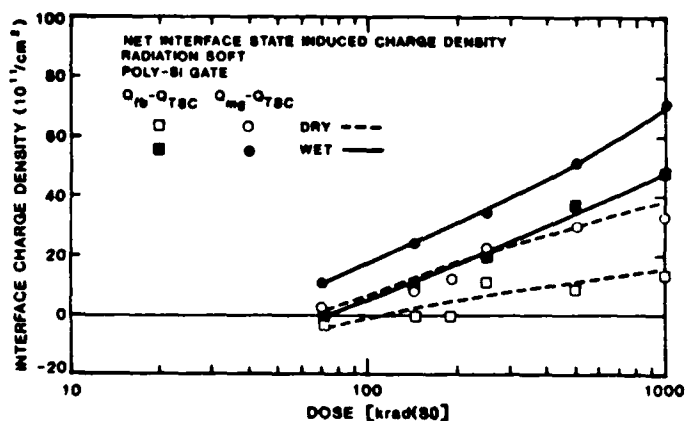
Fig. 6 — Interface charge density for irradiated poly-Si gate, radiation-soft oxides.

The net interface state charge density as a function of dose in radiation-hard and radiation-soft oxides is shown in Figures 5 and 6, respectively, for poly-Si gate devices. Al-gate devices yield similar results. For radiation-hard oxides, there is very little difference between the various processes except for the Al-gate dry oxides. Radiation-soft oxides are also very similar as a class. A detailed comparison, including models, is presented in Reference 7.

It was previously suggested that midgap voltage shifts obtained from C-V data are a useful measure of hole trapping in MOS capacitors.[12] This suggestion is based on the observed correlations between the density of interface states and the results of ESR measurements on the P_b center.[13] The data presented here indicate that this suggestion is not generally true. At midgap there is a contribution to the voltage shift from the interface states, with the magnitude of this contribution depending on device processing.

SUMMARY

Using the techniques of thermally stimulated current and high-frequency C-V measurements, we have investigated the device processing dependence in MOS capacitors of radiation- and BT-stress-induced hole traps and interface states. For both hole trap distributions and net interface charge densities, poly-Si gate devices resemble pyrogenic-grown Al-gate samples. The net interface charge density at midgap was found to be not a generally valid measure of hole trapping. The TSC technique was shown to be a valuable tool in the study of the characteristics of hole trap sites in MOS devices. Coupled with other measurements, such as C-V, it can contribute to a more complete understanding of charge trapping effects in MOS devices.

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APPENDIX F

PERMANENT DAMAGE PRODUCED BY SINGLE PROTON INTERACTIONS IN SILICON DEVICES[*]

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ABSTRACT

Results of measurements of the permanent damage produced by single energetic proton interactions in silicon depletion regions are presented. Single damage events and damage distributions were measured for an image sensor bombarded with 99- and 147-MeV protons. Increases in dark current density by more than two orders of magnitude were observed for individual damaged cells at relatively low fluences. Results are in good agreement with fundamental proton interaction concepts and with statistical expectations. Interesting phenomena are revealed in a study of room-temperature annealing, including damage production long after irradiation. Comparison of the effects of energetic proton bombardment with those produced by 14-MeV neutron irradiation is made, and similarities and differences are noted. Implications of this work for small-geometry integrated circuits are considered, and the relevance of this investigation to gaining increased understanding of proton damage mechanisms is discussed.

INTRODUCTION

Single energetic protons incident on silicon integrated circuits can cause transient upsets due to the ionization produced by nuclear reaction products.[1,2] Protons also displace lattice atoms, which results in permanent changes in the electrical properties of materials, devices, and integrated circuits. We have performed measurements of the permanent damage produced by single protons in silicon devices, and the results obtained are described herein. This study is similar in concept to our previous investigation of single 14-MeV neutron effects.[3] In the present work, the effects of energetic protons on depletion regions in silicon devices are examined experimentally and analytically.

We begin with a brief discussion of proton interactions with silicon, followed by a description of the model for permanent changes in dark current density due to displacement damage. The criterion for determining whether a single damage event occurred is discussed, as is the sensitivity of the experiment in detecting these events. Experimental results are presented, including the observation of single damage events, event amplitude distributions, and room-temperature annealing phenomena. Results of the present proton bombardments are then compared with previous 14-MeV neutron data. The implications of the present findings for small-geometry integrated circuits are described, and the relevance of this work to gaining increased understanding of the nature of proton damage in silicon is discussed.

PROTON INTERACTIONS WITH SILICON

Interactions of energetic protons with silicon and the subsequent effects of proton bombardment on material and device properties have been treated by various workers. (For example, see References 1, 2, 4-8.) In general, protons interact with Si atoms by elastic and nonelastic processes. The total elastic interaction process includes Rutherford (or coulomb) scattering and nuclear elastic scattering. Deviation from Rutherford scattering occurs when nuclear scattering becomes important. Both of these elastic processes can produce atomic displacements, although the nuclear elastic

interaction is much more effective because in this case a larger amount of energy is transferred to a Si primary recoil atom by an incident proton. The Si recoil subsequently loses its energy to ionization and to displacement processes. Nonelastic nuclear interactions are also important in silicon for proton energies greater than 10 MeV. (Nonelastic processes include all nuclear reactions except elastic scattering. Inelastic scattering (p, p′) and alpha particle production (p, α) are examples of nonelastic proton interactions.) Energetic recoils are produced by nonelastic interactions, which give rise to displacement damage and ionization.

The relative importance of the above processes can be assessed using interaction cross sections. Figure 1 shows the nonelastic nuclear interaction cross section as a function of proton energy for Si. (The scales at the top and at the right of the figure apply for this case.) The curve shown was derived from interaction probabilities given by Janni.[9] At the proton energies of interest in the present work, the nonelastic cross section is 0.4-0.5 barn.

Elastic cross sections are also shown in Figure 1. (This information is presented on the same figure as the nonelastic cross section curve for convenience of plotting only and not for comparison purposes.) Illustrated at two proton energies are cross sections for producing silicon recoils with energy E_r greater than a specific cutoff energy E_c. Petersen[2] presented such information previously for E_c values in the MeV range. We used the same procedure he employed to obtain cross sections over a broader energy range. Differential elastic scattering cross section data in the literature were transformed to the form $d\sigma_{el}/dE_r$, where σ_{el} is elastic cross section, and then integrated over recoil energy for E_r greater than specific cutoff energy values. (Relativistic effects were accounted for in making the transformation from angular data to $d\sigma_{el}/dE_r$.) The 95-MeV curve in Figure 1 was obtained from measurements performed on Al by Glassgold and Kellogg,[10] which should closely approximate the situation for Si. The curve shown for 155 MeV is based on Si measurements by Willis et al.[11] Calculated Rutherford scattering cross sections (relativistic) are also shown in the figure. Rutherford scattering dominates in the production of relatively low energy recoils ($\leq$ 5 keV). Nuclear elastic scattering is important in producing recoils with energy greater than 10 keV.[†] As discussed below, data presented in this paper were obtained at incident proton energies of 99 and 147 MeV. The 95- and 155-MeV elastic scattering curves in Figure 1 should provide good approximations to the actual cross sections for the proton energies used in our experiments.

DESCRIPTION OF MODEL

The model that forms the basis for the experiments and analyses presented in this paper was described previously.[3,12,13] A brief account is given here. As

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[†] Those portions of the 95- and 155-MeV curves shown solid in Figure 1 are based on experimental data. At 155 MeV, the transition from the solid curve to the linear Rutherford scattering regime, shown as a dashed curve, is approximate and was aided by results of calculations performed using the optical model.
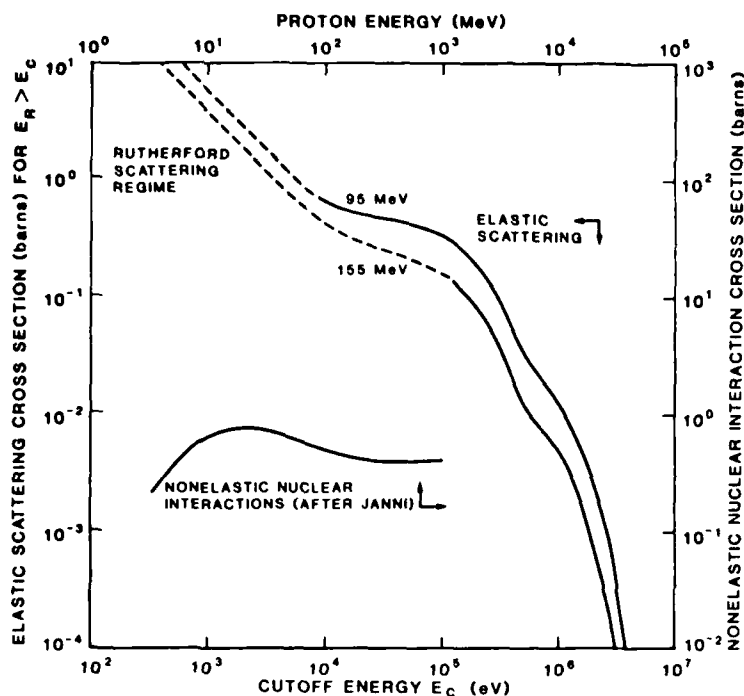
Figure 1. Interaction cross sections for proton-irradiated silicon. Nonelastic nuclear interaction cross sections were derived from interaction probabilities given by Janni.[9] (Use top and right scales.) Elastic scattering cross sections were obtained from differential cross section data in the literature[10,11] and from Rutherford scattering calculations. Shown are elastic cross sections for producing a Si recoil with energy E_r greater than specific values of cutoff energy E_c. (Use left and bottom scales.) The nonelastic interaction curve is presented in the same figure as the elastic scattering information for convenience of plotting only and not for comparison purposes.

described above, bombarding protons interact with Si atoms and produce energetic primary recoils. These recoils displace additional atoms, and those defects give rise to energy levels in the Si bandgap. Levels at or near midgap enhance the thermal generation rate in device depletion regions, and thereby cause the dark current to increase. Each defect acts independently and causes an incremental increase in dark current. Thus, the total increase in dark current caused by a single proton interaction is independent of the shape of the damaged region produced by the primary recoil. For example, a stable defect cluster in a depletion region is expected to increase the dark current by the same amount as a long string of defects if the number of defects is the same in both cases.

The proton fluence φ_1 at which the mathematical expectation is that one interaction will occur in a depletion region of width x_d in one element of an array with D elements is given by

$$\varphi_1 = 1/A \, x_d \bar{N} \sigma_t D \quad . \tag{1}$$

In this expression, A is the depletion region area, $\bar{N}$ is the atomic density ($= 5.0 \times 10^{22}$ cm^{-3} for Si), and σ_t is the total interaction cross section. The average increase in dark current density produced by a single interaction can be expressed as

$$\Delta J_{d1} = q \, n_i / 2 \, A \, K_g \bar{N} \sigma_t \quad , \tag{2}$$

where q is the electronic charge, n_i is the intrinsic carrier concentration, and K_g is the macroscopic generation lifetime damage coefficient.[13] The latter quantity has been determined experimentally for cases such as 14-MeV neutron bombardment of Si depletion regions.[14] However, to the authors' knowledge no measurements of K_g have been made for the proton energies of interest here. Thus, the experimental values of ΔJ_{d1} determined in the present work allow K_g to be calculated using Eq. (2).

DESCRIPTION OF EXPERIMENT

The test device studied was the Texas Instruments TC104 3456-element CCD linear image sensor. This device contains 3456 separate storage cells for imaging. Cell dimensions are 21.4 x 10.7 x 4 μm, with the latter value being the nominal depletion region width. The TC104 was operated in the dark, and thermally generated dark current was allowed to accumulate in the storage cells. Accumulation times of 1 sec and 10 sec were utilized. Pre- and post-irradiation measurements of dark current density were made at 303 $\pm$ 0.2 K for each cell in the array using a technique employed previously.[3] Each measurement of dark current density for a given cell involved averaging 100 readings obtained under computer control. The average pre-irradiation dark current density for individual cells in the devices focused on in this paper was 1 x 10^{-10} A/cm^2 at 303 K. For a fraction of the cells in these devices ($\sim$ 5%), the dark current density was a factor of 5 to 10 larger than the average value. (For a few cells, the pre-irradiation dark current density was a factor of $\sim$20 larger than the average.)

Steady-state proton bombardments of the test devices were performed at room temperature, with all leads shorted, at two facilities: 1) the cyclotron at the University of California at Davis (62-MeV proton energy at the silicon surface in the test devices); 2) the cyclotron at Harvard University (99-MeV and 147-MeV at the silicon surface). Because of dosimetry uncertainties in the 62-MeV proton experiments, this paper only presents results for 99- and 147-MeV irradiations. (Data obtained at 62 MeV were qualitatively similar to, and consistent with, findings at the two higher energies.) Results for irradiation of eight image sensors to the following proton fluences are described: 2.8 x 10^6, 2.8 x 10^7, 2.8 x 10^8, and 2.8 x 10^9 p/cm^2 at 99 MeV; 3.0 x 10^6, 3.0 x 10^7, 3.0 x 10^8, and 3.0 x 10^9 p/cm^2 at 147 MeV. Irradiation times were typically one to two minutes. At the highest proton fluence, the total ionizing dose received was $\sim$300 rad(Si). Separate irradiation of two additional devices was also performed using a Co-60 source to examine for any potential effects of ionizing radiation on the TC104.

Each device was stored at dry ice temperature within five minutes after proton irradiation to minimize annealing. Initial post-irradiation measurements

were performed over the period from three to seven days later. Before performing those measurements, each device was kept at room temperature for one hour. The average time at which measurements were made was one hour later, so the accumulated time at room temperature was ~2 h for the first data set obtained after irradiation. Additional post-irradiation measurements were performed after each of several room-temperature annealing periods. The last set of measurements was performed after approximately 1000 hours at room temperature.

EVENT CRITERION

Detailed examination was made of three pre-irradiation data runs obtained for each of the devices used in this study to establish an event criterion. This criterion was then employed to determine whether a proton-induced displacement damage event occurred in a given cell. It was found that, for 100 pre-irradiation measurements on any specific cell in ten devices, the standard deviation, expressed in terms of a dark output voltage, had an average value of 0.35 mV. This value is independent of charge accumulation time (i.e., 1 or 10 sec) and dark current amplitude for a given cell. Thus, as the first component in the event criterion we used two standard deviations, or 0.7 mV. This voltage value is equivalent to a measurement noise level of ~4 x 10^{-12} A/cm^2 for data obtained at an accumulation time of 10 sec.

The second component in the event criterion accounts for a systematic error that became evident when any two pre-irradiation data sets for a given device were compared. The percent change in dark current density for such data sets was found to be approximately constant for all cells in a specific device. This percentage had an average value ranging from 0.2 to 6.5% in thirty comparisons that were made (three for each of ten devices), with most of the values being less than 2%. A few individual cells in these comparisons exhibited percentage changes of up to 8% from run to run before irradiation. A value of 10% was selected for the systematic component of the event criterion. Thus, the rather conservative event selection criterion that was used is the following: an event is defined as having occurred if the dark voltage in a given cell changed after irradiation by more than 0.7 mV plus 10% of the pre-irradiation dark voltage. In terms of change in dark current density this criterion translates to the following typical value for 10-sec data: $\Delta J_d > 10^{-11}$ A/cm^2. (The event criterion varied from cell to cell in a given device due to variations in the pre-irradiation dark current density.)

DETECTION SENSITIVITY

An estimate of the average sensitivity of the present experiment for detecting radiation-induced defects can be made using the above event selection criterion plus previous data[3] obtained for 14-MeV neutron irradiations. The average primary recoil energy expended in displacement processes (E_{rd}) for 14-MeV neutron-irradiated Si was calculated by Stein to be 115 keV.[15] We previously calculated the primary recoil energy distribution for incident 14-MeV neutrons.[12] The average value of that distribution converts to an average energy expended in the production of displacements that agrees with Stein's value.[16] (This conversion was performed using the Lindhard model which gives the partitioning between ionization and displacement processes at a given recoil energy.) Sigmund[17] developed an expression for calculating an upper limit to the number N of atoms displaced by an energetic recoil:

$$N = (6 \epsilon_{\cdot}2/\pi^2)(E_{rd}/E_d) = 0.42(E_{rd}/E_d) , \qquad (3)$$

where E_d is the effective displacement energy. This relationship yields ~2000 defects for E_{rd} = 115 keV, assuming that E_d = 25 eV. This calculation applies to the damage produced immediately after neutron bombardment. That damage is unstable, and a significant amount of annealing occurs at room temperature. Based on previous transient annealing experiments,[18,19] a factor of 5 reduction in the number of defects is assumed as a conservative approximation to the situation that exists one to two hours after damage creation. Thus, 400 defects are assumed for the "stable" damage resulting from a single 14-MeV neutron interaction.

In our previous study,[3] the average change in dark current density due to neutron interactions in the TC104 was 1.5 nA/cm^2. This value is applicable for the 1389 cells that were damaged at a fluence of 7 x 10^9 n/cm^2. The corresponding number of single neutron interactions is 1776 since a significant fraction of these cells experienced multiple interactions.[3] Thus, the average change in dark current density per interaction is 1.17 nA/cm^2. Using this value, we obtain ~3 pA/cm^2 as the incremental dark current density produced per stable defect. Based on the typical event criterion given above, we then estimate that the present experiment is sensitive enough to detect a minimum of four simple defects in a single cell.* Using Eq. (3), the value of recoil energy which would produce four stable defects can be determined. That calculation then leads to a statement of the experimental sensitivity in terms of the ability to detect a proton interaction that produces a recoil with an energy greater than a certain value. We obtain E_{rd} = 1.2 keV, which is the energy needed to produce 20 defects initially (or four defects after transient annealing). Using the Lindhard model, a total primary recoil energy (i.e., displacement and ionization portions) of 1.5 keV is obtained. This calculation allows one to estimate the elastic scattering cross section appropriate for the detection sensitivity limit of the present experiment. Assuming that the effects of Si recoils with energy greater than 1.5 keV can be observed, the corresponding elastic cross section, from Figure 1, is 3.7 barns at a proton energy of 99 MeV. The cross section for 147-MeV protons is 2.6 barns. Adding the nonelastic cross sections to these values yields total interaction cross sections of 4.2 and 3.0 barns at 99 MeV and 147 MeV, respectively. These calculated values apply for the production of a detectable number of defects per interaction for the present experimental conditions.

MULTIPLE INTERACTION PROBABILITIES

A given cell in the test device may experience more than one interaction during proton bombardment. The probability for multiple interactions can be determined using the Poisson distribution:

$$P(x,\lambda) = \lambda^x e^{-\lambda}/x! . \qquad (4)$$

In this equation, P is the probability that x interactions occur in the same cell during irradiation to a fluence ϕ, λ is equal to $\phi\theta$, and θ is the probability that an interaction will occur at a fluence of 1 proton/cm^2 (i.e., θ = interaction probability per unit fluence, in cm^2). Using the cell dimensions for the present device and the interaction cross sections determined above (i.e., 4.2 and 3.0 barns), the calculated values for θ are 1.92 x 10^{-10} cm^2 at 99 MeV and 1.37 x 10^{-10} cm^2 at 147 MeV. Figure 2 shows interaction probabilities

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*It is assumed here that 3 pA/cm^2 also applies for defects produced by proton bombardment. This is reasonable since energetic Si recoils are produced by incident protons and neutrons, and the subsequent energy deposition process is the same in both cases.
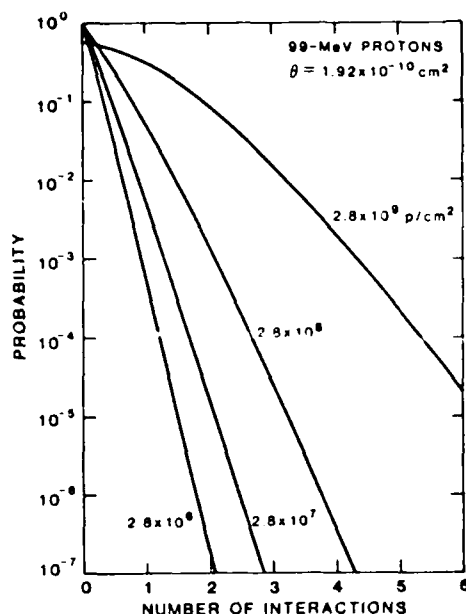
Figure 2. Probability of 99-MeV proton interactions in a specific cell of the test device at several fluences. The curves shown were calculated using Eq. (4) in the text.

for a specific cell in the TC104 at the four 99-MeV proton fluences used experimentally. At the highest fluence, the probabilities for 0, 1, 2, and 3 interactions in the same cell are 0.584, 0.314, 0.0846, and 0.0152, respectively. For example, 1086 cells in the TC104 are expected to experience one individual damage event at a fluence of 2.8×10^9 p/cm^2.

EXPERIMENTAL RESULTS

Number of Damaged Cells

Table 1 lists the measured number of cells that were damaged at several proton fluences. The event criterion given above was used to define whether a cell was damaged. Also given in the table is the calculated number of damaged cells. These calculations were performed by first using Eq. (4) to obtain the probability of zero interactions, $P(0,\lambda)$, as a function of fluence. The number of cells that experience one or more proton interactions at a given fluence is then given by (3456) times $(1 - P(0,\lambda))$. As illustrated in Figure 2, multiple interactions become important only at the highest fluence examined. Thus, the calculated number of damaged cells exhibits a linear increase with fluence at the lower fluences. Also note that Eq. (1) yields values for $\dot{q}_1$ of 1.5×10^6 and 2.1×10^6 p/cm^2 at 99 and 147 MeV, respectively. These values can be used to obtain the calculated numbers in Table 1 at the lower fluences. (However, multiple interactions need to be accounted for at the highest fluence.)

Figure 3 compares the measured and calculated results of Table 1. Agreement is quite good for 99-MeV proton bombardment, which indicates that the procedure described above for determining total cross section values appropriate for the present experimental conditions was reasonably accurate. This agreement further indicates that the analytical approaches employed here can be utilized with confidence in interpreting the experimental results. The calculated results overestimate experimental findings at 147 MeV (Figure 3), although agreement is still reasonably good (32% difference at the highest fluence).

Table 1. Measured and calculated number of cells in the TC104 image sensor that were damaged as a result of proton irradiations to several fluences. Measurements were performed two hours (at room temperature) after irradiation using a charge accumulation time of 10 sec.

(a) 99-MeV Proton Bombardment

Device Number	Fluence (p/cm^2)	Number of Damaged Cells Measured	Number of Damaged Cells Calculated
14	2.8×10^6	3	1.9
7	2.8×10^7	23	19
15	2.8×10^8	124	181
8	2.8×10^9	1432	1439

(b) 147-MeV Proton Bombardment

Device Number	Fluence (p/cm^2)	Measured	Calculated
9	3.0×10^6	2	1.4
13	3.0×10^7	6	14
17	3.0×10^8	86	140
18	3.0×10^9	884	1167
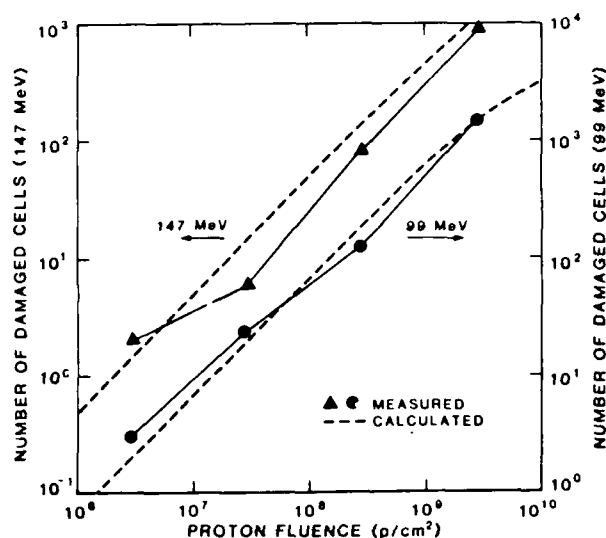
Figure 3. Comparison of the measured and calculated number of damaged cells produced by 99- and 147-MeV proton bombardment. (Values shown here are also listed in Table 1.)

Single Damage Events and Damage Distributions

Figure 4 presents the measured change in dark current density for all cells in the test devices after bombardment with 99-MeV protons. (Results of 147-MeV proton irradiations were very similar to these data.) Results are shown for three fluences. In Figure 4(a), several damaged cells are evident at the lowest fluence. (Relatively small events are not evident on the current density scale used in this figure.) Increasing the fluence increases the number of events; cells with a relatively large amount of damage also become evident (Figs. 4(b) and 4(c)). At 2.8×10^8 p/cm^2, of the 124 damaged cells, we calculate that 121 experienced one event and 3 experienced two interactions. At 2.8×10^9 p/cm^2, the number of cells experiencing 1, 2, 3, 4, and 5 events are calculated to be 1080, 291, 53, 7, and 1, respectively. Cells exhibiting a very large change in dark current density in Figure 4(c) may have experienced multiple interactions. Another potential source of the large damage events is (p,α) reactions in which energetic alpha particles are produced.[2] In addition, spallation (fission) reactions which deposit a large amount of energy also occur. The cross section
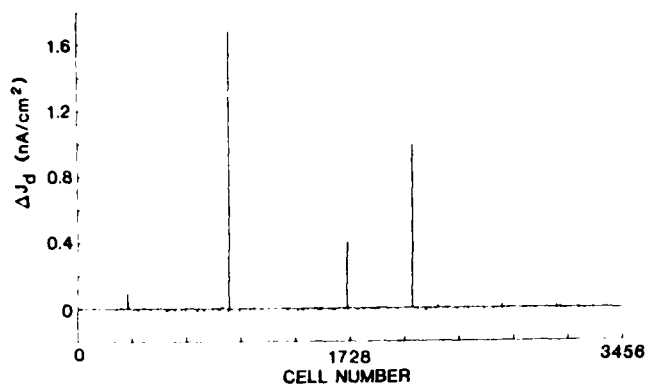
(a) Device Number 7; 2.8×10^7 p/cm^2.
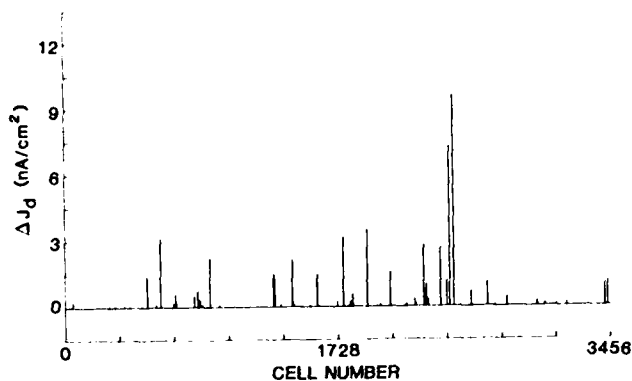
(b) Device Number 15; 2.8×10^8 p/cm^2.
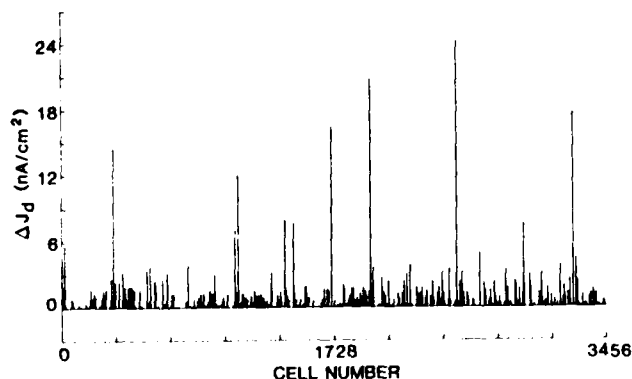
(c) Device Number 8; 2.8×10^9 p/cm^2.

Figure 4. Measured change in dark current density (ΔJ_d) produced by 99-MeV proton interactions in the TC104 test devices. Results obtained at three fluences are shown.

for fission reactions at the two proton energies of interest here is 0.02 barn.[2] At the highest fluences studied, it appears likely that several cells were damaged by energetic heavy fission fragments. (Comments similar to those made here for the 99-MeV data also apply for the 147-MeV results.)

Distributions of damaged cells at the highest fluences studied are shown in Figures 5 and 6 fo- 99- and 147-MeV proton bombardment, respectively. (Note that the ordinate is a logarithmic scale in both figures for the purpose of displaying those bins containing only a few cells.) The inset to each of these figures shows the tail of the distribution where heavily damaged cells re

evident.[*] For the six largest events shown in Figure 5, the dark current density changed by factors ranging from 66 to 481 due to proton interactions. The four most heavily damaged cells in Figure 6 (147 MeV) changed by factors of 160 to 351.

The mean values of each damage distribution are shown in Figures 5 and 6. Using the Poisson distribution, these values can be converted to the change in dark current density per interaction (ΔJ_{d1}). The results are 0.26 nA/cm^2 at 99 MeV (1849 interactions) and 0.34 nA/cm^2 at 147 MeV (1021 interactions). As noted above, Eq. (2) can be used to calculate the generation lifetime damage coefficient K_g when ΔJ_{d1} is known. We obtain K_g values of 1.1×10^7 and 1.2×10^7 proton-sec/cm^2 at 99- and 147-MeV, respectively.

Ionizing Radiation Effects

The TC104 image sensor is a commercially available MOS integrated circuit, and therefore is likely to be susceptible to ionizing radiation effects. To examine this issue, two previously unirradiated devices were irradiated to total doses of 300 and 1600 rad(Si), respectively, using a Co-60 source. (As noted above, the total dose received during the highest-fluence proton irradiation was ~300 rad(Si).) At 300 rad(Si), no changes in device properties were evident except that one cell exceeded the event criterion for an accumulation time of 10 sec. This finding strongly indicates that the damage events reported in the present study are due to proton-induced displacement effects and not to ionization. The device irradiated to 1600 rad(Si) did exhibit a response, however. For a 10-sec accumulation time, 464 very small damage events were evident. The mean value of ΔJ_d for these events was 7.5 pA/cm^2. Note that this value is less than the typical event criterion of 10 pA/cm^2 given above. Examination of the results revealed that events occurred in cells with a less-than-average pre-irradiation dark current; the event criterion is lower for such cells. We interpret the observations at 1600 rad(Si) as being due to a macroscopic effect of ionizing radiation on the test device. One possibility is charge buildup in the gate oxide which could widen the depletion region in all cells and thereby increase the dark current. Ionizing radiation may also affect the output stage. The effects observed are beginning to be important at 1600 rad(Si) but are unimportant at 300 rad(Si). Therefore, caution should be exercised when using the TC104 as a test device at fluences $>3 \times 10^9$ p/cm^2 for the proton energies studied here.

Room-Temperature Annealing

Post-irradiation data shown in Figures 3-6 were obtained after two hours at room temperature. Additional measurements were made at intervals to examine room-temperature annealing phenomena. The example discussed here is behavior for Device #8 which was irradiated to a 99-MeV proton fluence of 2.8×10^9 p/cm^2. (Results for Device #18, which was irradiated to 3.0×10^9 p/cm^2 (147 MeV) were similar.)

As noted in Table 1, 1432 cells were damaged in Device #8. The annealing behavior for a significant

[*] The TC104 test device begins to exhibit nonlinearity for dark voltages (V_d) >0.4 V. This situation was encountered for the heavily damaged cells at an accumulation time of 10 sec. To avoid this problem, the largest events shown in Figs. 5 and 6 are based on data obtained at an accumulation time of 1 sec. (Linear behavior is observed in the TC104 when one compares the change in dark voltage at the two experimental times, i.e., $\Delta V_d(10s)/\Delta V_d(1s) \cong 10$ as long as $V_d(10s)$ is < 0.4 V. However, sublinear behavior is observed when comparing dark voltage values, i.e., $V_d(10s)/V_d(1s) < 10$.
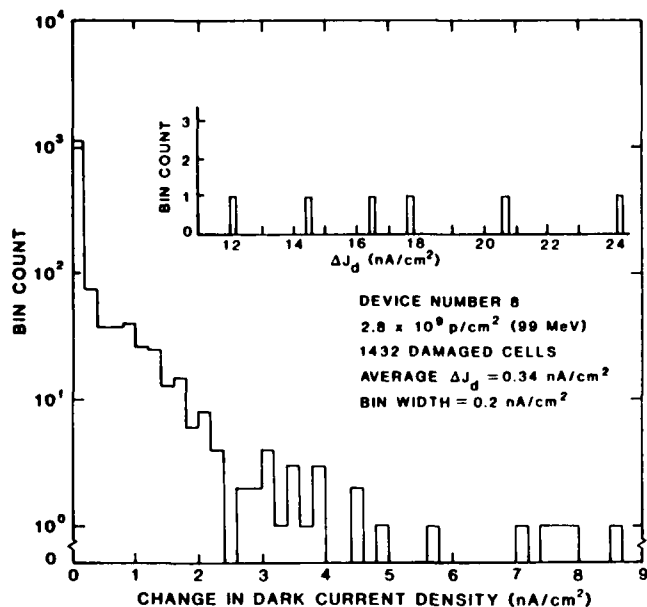
Figure 5. Measured distribution of damaged cells after a 99-MeV proton fluence of 2.8 x 10^9 p/cm^2. Note that the ordinate is a logarithmic scale, and that the inset shows the tail of the distribution.
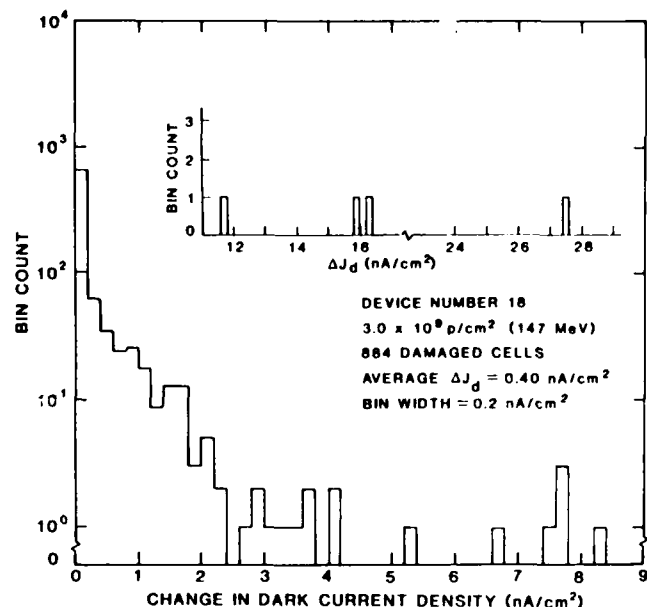
Figure 6. Measured distribution of damaged cells after a 147-MeV proton fluence of 3.0 x 10^9 p/cm^2. Note that the ordinate is a logarithmic scale, and that the inset shows the tail of the distribution.

subset of these cells was examined in detail. Data are presented in terms of a dark current annealing factor, AF, defined as

$$AF = (J_d(t) - J_{do})/(J_d(\infty) - J_{do}) \quad . \qquad (5)$$

In this equation, J_{do} is pre-irradiation dark current density, $J_d(\infty)$ is the dark current density at t = ∞ (~1000 hours here), and $J_d(t)$ is the dark current density at a given time during the room-temperature annealing period. (By definition, $AF(\infty)$ = 1.) Measurements were performed at four annealing times: 2, 22, 190, and ~1000 h. We first selected those cells that obeyed the event criterion at all of these times, not just at 2 h. In addition, the condition $J_d(\infty) \geq 2 J_{do}$ was imposed so that only cells with a significant amount of permanent damage were considered. Finally, cells with a dark voltage greater than 0.4 V were eliminated to avoid possible errors due to nonlinearity in the test device (discussed in a footnote above). The resulting population was 778 cells out of 1432 candidates.

Figure 7 shows the distribution of AF values for these 778 cells at 2 h. The mean is 1.77, but the distribution is broad. For 68% of the cells, AF is ≥ 1. However, the remainder of the cells have an annealing factor less than unity, which means there is less damage at 2 h than at 1000 h. In those cells, damage production occurred during the annealing period, which is an unexpected result. (Damage production is referred to here as reverse annealing.) Also note that one cell exhibited an exceptionally large annealing factor (46).

The mean annealing factor for the 778 cells exhibited well-behaved forward annealing (i.e., damage reduction) at all measurement times, with AF values being 1.47 at 22 h and 1.19 at 190 h. However, the detailed information available in Figure 7 illustrates that annealing is much more complex for individual damage regions. Evidently a variety of annealing components constitute the net forward annealing process that would be observed in a macroscopic study at much higher proton fluences. Results of our initial attempt to gain insight regarding these phenomena are summarized here.

In Figure 8, two of the annealing components for the 778 cells are illustrated. The upper curve represents mean AF values for that subset which exhibited monotonic forward annealing only (32% of the 778 cells). Maximum and minimum AF's are shown for each data point to illustrate that a broad distribution of values exists even for this well-behaved subset. The bottom curve represents that subset which exhibited monotonic reverse annealing only (10%). An additional subset (15%) exhibited negligible annealing, i.e., 0.8 ≤ AF ≤ 1.2 at all measurement times. The remaining subset (43%) exhibited "mixed" annealing, i.e., a combination of forward and reverse annealing.

Two additional observations made are noteworthy: 1) A small fraction (3.6%) of the 778 cells experienced "precipitous" annealing, i.e., the annealing factor changed by a factor of 5 or more (up or down) between any two measurement times. For forward annealing, these factors ranged from 5 to 49; for reverse annealing, the range was 5 to 13. (Nearly all of the precipitous annealing events were in the forward direction.) 2) The 2024 cells in Device #8 that did not meet the event criterion after irradiation (i.e., undamaged cells) were examined to see if any damage production occurred in them during the annealing period. At 1000 h, 33 of these cells (1.6%) had enough damage to pass that criterion. (As above, additional criteria imposed were $J_d(\infty) \geq 2 J_{do}$ and the dark voltage was ≤0.4 V.) The characteristics and behavior of these cells were relatively uniform. J_{do} was nearly a factor of 3 less than the average of all 3456 cells in Device #8. Also, the ratio of $J_d(\infty)/J_{do}$ had a value of 2 to 4 in nearly all cases for these 33 cells. The small J_{do} values, the relatively small event size, and the uniform behavior observed indicate that the apparent damage production process in previously undamaged cells during the annealing period is not the same process observed in a portion of the 778 damaged cells. Annealing behavior appears to be considerably more diverse in the latter case.

The general issue of damage production during annealing will require further study to determine the responsible mechanisms. Three possibilities that should
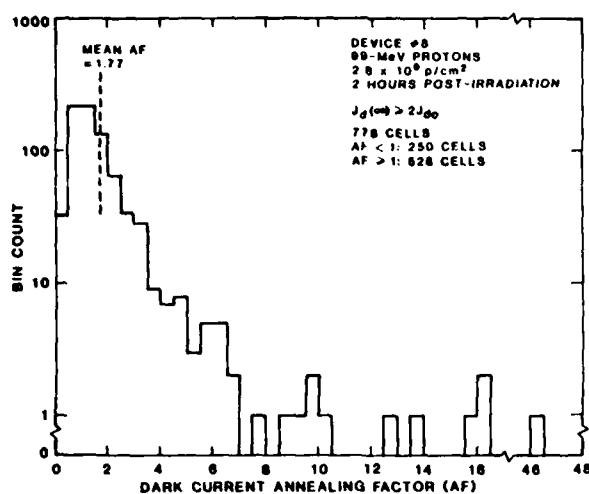
Figure 7. Distribution of dark current annealing factor values for 778 damaged cells in Device #8 two hours (at room temperature) after irradiation to 2.8×10^9 protons/cm^2 (99 MeV). Note that the ordinate is a logarithmic scale.
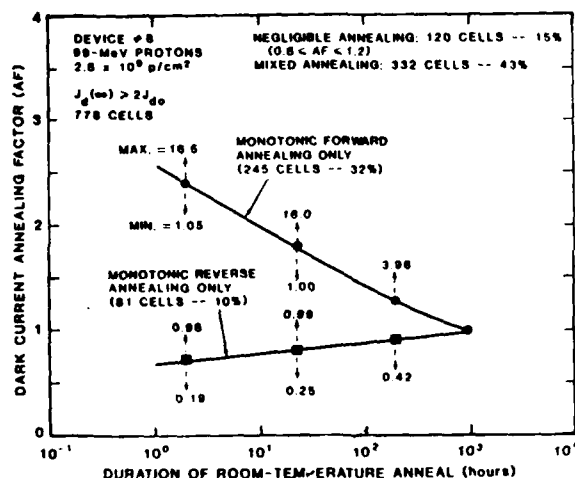
Figure 8. Dark current annealing factor versus time at room temperature for Device #8 after irradiation to 2.8×10^9 protons/cm^2 (99 MeV). Information is shown for the 778 cells considered in Figure 7. Numbers above and below the data points are the maximum and minimum AF values, respectively.

be considered are: 1) proton activation of materials in or surrounding the test device, and subsequent emission of particles (e.g., alphas and betas) that introduce displacement damage; 2) defect migration into a cell from a nearby damaged region; 3) defect reordering within a damaged cell, with the resultant stable configuration being more effective in producing dark-current generation, e.g., introduction of energy levels closer to midgap.

COMPARISON WITH 14-MeV NEUTRON DATA

In our previous study of single 14-MeV neutron effects,[3] the type of test device was the same as that employed here. This commonality allows comparisons to be made of proton and neutron findings. In general, similarities and differences are evident, and the results are consistent with expectations in both cases. For approximately the same number of damaged cells, neutron bombardment resulted in significantly fewer small damage events than proton irradiation. The reason for

this is that such events are produced largely through Rutherford scattering which does not occur for neutrons. However, the tail of the damage distribution is similar in both cases. The large events are roughly comparable in number and in magnitude.

Information presented in Table 2 can be used to account for this observation. First, consider nonelastic interactions for neutrons and protons. The nonelastic cross sections (σ_{non}) are within a factor of 2 to 2.5 of each other and the average energy that goes into displacement processes (E_{rdn}) is very similar. Thus, roughly comparable contributions by nonelastic processes to the tails of the neutron and proton damage distributions are expected. Now consider elastic scattering. The values of E_{rde} for protons in Table 2 are relatively low due to the influence of Rutherford scattering. However, the average recoil energy (displacement portion) for nuclear elastic scattering only is calculated to be 130 keV for incident 99- and 147-MeV protons.[5] The corresponding scattering cross sections are 0.43 and 0.30 barn, respectively.[5] These cross sections and the average proton recoil energy are roughly comparable to the corresponding elastic scattering values for 14-MeV neutrons. Thus, contributions to the proton and neutron damage distribution tails by elastic scattering are also expected to be similar.

Other quantities of interest are also listed in Table 2. Since more small events are produced in the proton case, it is reasonable that ΔJ_{d1} is lower than for neutron bombardment. Also note that ΔJ_{d1} for neutrons and protons scales reasonably well with E_{rd}, as expected (e.g., 115 keV/33 keV = 3.5 and 1.17 nA cm^{-2}/0.34 nA cm^{-2} = 3.4). Damage coefficient values are consistent with ΔJ_{d1} values. From a macroscopic viewpoint, K_g is a measure of the fluence required to decrease the generation lifetime (or increase the thermal generation rate) to a specific value. Thus, the higher proton fluence required to achieve a given increase in dark current is due to the lower value of ΔJ_{d1} for protons; this, in turn, is attributable to the fact that relatively low energy scattering events are more important in the proton case than for neutron bombardment.

Previous room-temperature annealing data for 14-MeV neutron bombardment[3] were re-analyzed in the present study using the same procedures and criteria that were applied to proton data. Results were reasonably similar in both cases, with one notable exception: negligible monotonic reverse annealing occurred in the 501 candidate neutron-irradiated cells examined. This observation indicates that reverse annealing is much less important in the 14-MeV neutron case. If activation is the responsible damage production mechanism, then examination of differences between proton and neutron activation for relevant materials should provide support. Again, the reverse annealing issue should be investigated further.

DISCUSSION

Implications of the present findings for small-geometry integrated circuits are now considered. This topic was discussed previously for single 14-MeV neutron bombardment.[3] As noted above, the permanent damage effects produced by neutron bombardment are similar to those in the neutron case. Thus, effects on VLSI/ULSI circuits are expected to be similar.

All silicon integrated circuits contain depletion regions. If a single energetic proton produces displacement damage in that region, the dark (or leakage) current will increase. Decreasing circuit dimensions will increase the dark current density. Whether this single-particle effect will present a problem depends on geometry, the type of circuit, specifications, and performance

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Table 2. Comparison of analytical and experimental values of several quantities for neutron- and proton-irradiated silicon.

		14-MeV Neutrons	99-MeV Protons	147-MeV Protons
Interaction Cross Section (barns)	elastic scattering (σ_{el})	0.75 (a)	3.7 (c)	2.6 (c)
	inelastic scattering (σ_{in})	~0.75 (a,b)	~0.1 (d)	
	nonelastic (σ_{non})	1.02 (a)	0.5 (e)	0.4 (e)
	total (σ_t)	1.8 (a)	4.2 (c)	3.0 (c)
Average Recoil Energy Into Displacement Processes (keV)	elastic scattering (E_{rde})	85 (f)	12 (c,h)	10 (c,h)
	inelastic scattering (E_{rdi})	130 (f)		
	nonelastic (E_{rdn})	140 (g)	180 (i)	170 (i)
	total (E_{rd})	115 (b)	32 (c,g)	33 (c,g)
Average Change in Dark Current Density per Interaction (ΔJ_{d1}), nA/cm^2		1.17 (j)	0.26 (j)	0.34 (j)
Generation Lifetime Damage Coefficient (K_g), particle-sec/cm^2		3.1×10^6 (k)	1.1×10^7 (j)	1.2×10^7 (j)

a. Reference 20.
b. Reference 15.
c. Applicable for the detection sensitivity of the present experiment (see text).
d. Estimated using information in References 2 and 21.
e. Reference 9.
f. Based on References 12 and 16.
g. Calculated using $E_{rd} = (E_{rde}\sigma_{el} + E_{rdn}\sigma_{non})/\sigma_t$.
h. Calculated from differential cross section data at 95 and 155-MeV (References 10 and 11). The Lindhard model was used for energy partitioning.
i. Based on average primary recoil energies given in Reference 5 and on energy partitioning using the Lindhard model.
j. Present work.
k. Reference 14.

requirements. It is likely that displacement damage effects at relatively low fluences will be a problem for small-geometry charge-integration and charge-transfer devices because proper operation typically requires a low dark current density.

The damaged region produced by a single proton interaction (or several interactions) can be viewed as a steady-state source of thermally generated charge when the damage is present in device depletion regions. This charge generator results in a dc current flow. Whether the total charge generated in a specific time, or the dc current level, presents a problem depends on the type of circuit, its properties, and the application. An example was presented previously[3] which indicated that damage regions produced by neutrons may cause a problem in 1- and 4-Mbit NMOS DRAMs due to the generation of excess dark charge. A similar expectation applies to energetic proton bombardment. The worst-case damaged cell in the present study had a proton-induced dark current density of 27.5 nA/cm^2 (Figure 6). (Such a situation can occur in a dense array at a relatively low fluence, so we use the largest event as a worst-case example.) The thermally generated charge Q_g generated by that damage in time t (in seconds) can be expressed as $Q_g = 63$ t femto-coulombs. (This expression is independent of dimensions as long as the damage is completely contained within the depletion region.) Thus, a steady-state current of 63 fA will flow and generate, for example, 6.3 fC in a time of 100 msec. This worst-case calculation can be used to estimate whether a problem will occur in a given situation. The approach outlined here is applicable for assessing the suscept ibility of any integrated circuit to the permanent effects of single incident protons. As noted previously,[3] limits eventually may be placed on circuit dimensions to avoid problems caused by permanent damage at low particle fluences.

The present work is relevant to gaining increased understanding of proton damage mechanisms in silicon. For example, the experimental and analytical approach followed here allows one to examine fundamental inter-action concepts. Comparison of proton and neutron data illustrated the expected importance of Rutherford scattering in the former case. In general, the information obtained is of value in correlating neutron and proton

damage effects. Further, details of annealing behavior can be explored at a level not previously achieved, as evidenced by the novel results presented above for annealing of individual damage events. An additional area of relevance has recently been pointed out by Burke.[22] He has shown that parameters obtained from low-fluence damage studies, such as that performed here, can be used in conjunction with appropriate analytic techniques to predict effects at high fluences. Determination of the damage event spectrum at low fluences may be an important step toward achieving the mechanistic insight required to model high-fluence phenomena.

SUMMARY

This paper has presented the first direct measurements of the permanent damage produced by single energetic proton interactions in silicon depletion regions. Single damage events and damage distributions were measured for an image sensor bombarded with 99- and 147-MeV protons. Increases in dark current density by more than two orders of magnitude were observed for individual damaged cells at relatively low fluences. Results were in good agreement with fundamental proton interaction concepts and with statistical expectations. Detailed study of room-temperature annealing revealed interesting phenomena, including damage production long after irradiation. Comparison of the effects of energetic proton bombardment with those produced by 14-MeV neutron irradiation was made, and similarities and differences were noted. Implications of the present work for small-geometry integrated circuits were considered, and the relevance of this investigation to gaining increased understanding of proton damage mechanisms in silicon was discussed.

ACKNOWLEDGMENTS

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Critical Evaluation of the Midgap-Voltage-Shift Method for Determining Oxide Trapped Charge in Irradiated MOS Devices[*]

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ABSTRACT

The validity of using midgap voltage shifts to determine radiation-induced oxide trapped charge is examined using thermally stimulated current (TSC), conductance, and C-V techniques. The assumption behind the midgap technique that all interface states are amphoteric P_b centers is shown to be not generally valid. Conductance measurements revealed a donor interface state in the upper half of the bandgap. Results obtained by combining data from TSC and high-frequency C-V measurements show the existence of three types of radiation-induced interface states: the P_b center, a donor state in the upper half of the bandgap, and an acceptor state in the lower half. No single surface potential exists that is the neutral point for N_{it} for all processes and radiation doses. Midgap voltage shifts do not generally correlate with oxide trapped charge determined from thermally stimulated current (TSC) measurements. The magnitude of the fractional deviation is typically less than a factor of unity but in some cases is as large as a factor of four. The significance of these errors needs to be determined for each application. Arguments and tests supporting the validity of using TSC measurements for determining oxide trapped charge are presented.

INTRODUCTION

Experimental evaluations of ionizing radiation effects on MOS devices are performed frequently, so assessment of the validity of the specific measurement methods used in these evaluations is important. Among the MOS device parameters which degrade by ionizing radiation are threshold voltage, transconductance or mobility, and leakage current. For MOS circuitry, radiation-induced degradation is manifested as a shift in threshold voltage and a reduction in channel mobility. The degradation of these parameters is the result of charge trapping at sites in the oxide and generation of interface states. An important measure of charge trapping in the oxide is the density of trapped holes, N_{ot}; for interface states, the net interface state charge density, N_{it}, is of interest. N_{ot} is the first moment of the oxide charge distribution.[1]

A variety of methods have been employed to measure the effects of charge trapping and interface states. Many of these are time consuming, restricted in their application and require sophisticated laboratory apparatus and analysis.[1] A simple method that is widely used for characterizing the radiation sensitivity of MOS devices involves the determination of voltage shifts (ΔV) from measurements of either I-V characteristics for MOSFETs or C-V characteristics for MOS capacitors. However, ΔV reflects the combined effects of N_{ot} and N_{it}. In many processing and circuit applications, an understanding of the separate effects of these two components is often required. Various methods have been proposed to separate these effects based on the variation of N_{it} with surface potential.[1-4] One such technique,[2,3] which has recently gained acceptance, is based on the assumption that, at a surface potential corresponding to midgap, N_{it} is zero. Therefore, ΔV measured at midgap determines N_{ot}. In this method, changes in the stretchout of C-V curves between midgap and some other surface potential, such as inversion, are used to determine N_{it} at that surface potential.

The assumption behind the midgap-voltage-shift technique is that interface states are amphoteric.[3] The behavior of amphoteric centers, which have been detected in ESR studies on MOS devices and are referred to as P_b centers in the literature, correlates very well with the behavior of interface states.[5,6] Such correlations involve comparing the density of P_b centers with the density of interface trap energy levels for various values of bias, radiation dose, oxide thickness, crystal orientation, and annealing temperature. These results, plus hyperfine measurements, have led to the conclusion that P_b centers are interface states. The P_b center results in a donor-like state when the surface potential, ψ_s, is below midgap and an acceptor-like state above midgap. At midgap, P_b centers are not charged. Since ESR measurements, especially on <111> Si surfaces, have not detected any other bias- and angular-dependent signal which could be assigned to interface states, interface states are assumed to be solely "P_b-like" centers and, therefore, amphoteric.[5,7]

Results obtained using other MOS measurement techniques have implied that other types of interface states exist.[8-13] C-V measurements have been interpreted as indicating the existence of a donor interface state in the upper half of the Si bandgap.[8] Analyses of subthreshold current measurements have also invoked a donor state in the upper half of the bandgap.[9] Conductance measurements on certain unirradiated devices indicate that donor-like states dominate the density of interface states above midgap while acceptors exist below midgap.[10] Other conductance measurements on irradiated samples indicate that although acceptors dominate in the upper half of the bandgap, donors are also present.[11] Thermally stimulated current (TSC) measurements on samples fabricated using a variety of processing procedures have previously detected the existence of not only the P_b center but also a donor interface state in the upper half of the bandgap and an acceptor in the lower half of the bandgap.[12]

The objective of this study was to determine the general validity of the midgap technique for determining oxide trapped charge in MOS devices fabricated on <100> Si, and if found not to be rigorously valid, then determine the degree of error. The experimental approach adopted was twofold: (1) de-

termine if any other type of interface state exists in addition to the amphoteric P_b centers and if, so, attempt to quantify the relative magnitudes; (2) measure N_{ot} directly and compare with the trapped charge density derived from the midgap technique, quantify any discrepancies, and use these discrepancies to determine the types of interface states that cause the discrepancies. If either (1) or (2) are found not to agree with the assumptions underlying the midgap technique, then its general validity becomes questionable. However, depending on the magnitude of the discrepancy, the technique may still be useful.

The organization of this paper is the following. First, the measurement techniques used are described, including TSC, C-V, and conductance measurements. Next, a comparison of N_{ot} obtained from TSC measurements with midgap shifts from C-V measurements are presented and discussed, including the types of interface states found. These interface states are then compared with the types derived from conductance measurements. Finally, the types of interface states reported in the literature will be compared to those observed in this work.

EXPERIMENTAL AND ANALYTICAL APPROACH

Three different measurement techniques were used in this study. The TSC technique was used to determine N_{ot} directly. C-V measurements were made to obtain radiation-induced voltage shifts and to derive the density of interface states, D_{it}. Combining results from both TSC and C-V measurements, N_{it} at various surface potentials (ψ_s) was obtained. Conductance measurements were used to determine independently both D_{it} and the dominant type of interface state.

The experimental procedure was the following. C-V measurements were made prior to each irradiation and before and after each TSC measurement. After irradiation, C-V curves were generally shifted in the negative voltage direction, indicating the introduction of radiation-induced trapped holes, and showed stretchout, which is generally indicative of the presence of interface states. The C-V curves taken after the TSC measurement were found to be nearly identical to those obtained prior to irradiation, showing that radiation-induced hole traps and interface states were eliminated. Conductance measurements were made on specific devices.

Measurements were made at both room temperature and 77K on a capacitor irradiated to 1 Mrad(Si). The significant stretchout observed in the room temperature data disappeared in the data taken at 77K, indicating that the stretchout was not caused by lateral nonuniformities. Although this test for lateral nonuniformities was made only on one type of sample, we assume the same conclusion applies to all the data.

The devices studied were MOS capacitors fabricated by various processes. One set of test capacitors was fabricated along with an integrated circuit while another set only experienced those processing steps necessary to produce capacitors. The MOS capacitors were prepared on doped n- and p-type Si of <100> orientation using conventional Al- and poly-Si gate device fabrication processes. Some of the processes were described earlier[12,13] and include a variety of gate oxides such as pyrogenic oxides grown in steam as well as dry oxides grown in oxygen. The oxides either underwent a post-oxidation anneal

(POA) in various ambient atmospheres or were left unannealed (NPOA). No ion contamination was observed in any of these samples. The devices were irradiated in a Co^{60} cell to various doses ranging from less than 100 krad(Si) to more than 4 Mrad(Si).

TSC Technique

TSC measurements have previously been used as a spectroscopic technique to supply information regarding the local bonding of the trapped holes in the oxide.[12,13] Here the TSC technique is used to determine the density of trapped holes. A full description of the technique, as well as other experimental details, have been presented previously.[12,13] The TSC measurement consists of recording the current flowing in a MOS capacitor as the temperature is raised. After a capacitor is irradiated under positive gate bias, TSC measurements are made under negative bias. Holes initially trapped near the Si-SiO_2 interface will be swept toward the gate and produce current peaks in the TSC signal at some elevated temperatures. The measurement is repeated to determine the background current. The difference between the two currents is interpreted as arising from the thermal depopulation of charged traps. Good signal-to-noise ratio and a high TSC signal measurement sensitivity of <0.01 pA result in an accurate determination of trapped charge density of states spectra. The worst-case error in a density of states value is estimated to be 10% and is primarily due to the subtraction of the background current. By using a bias such that device degradation and retrapping of the released charge do not occur, the temperature scale of the TSC spectrum can be converted to an activation energy scale using the analysis of Simmons.[14] This analysis converts the TSC data into a trapped hole density of states versus activation energy spectrum. By integrating this density of states, N_{ot} is directly obtained.

During TSC measurements both trapped holes and interface states are annealed and the surface potential changes with temperature. However, interface states do not contribute to the measured current. The reason is that the MOS capacitor is in thermal equilibrium throughout the TSC measurement. During this measurement the temperature is ramped from room temperature to 400°C in approximately 15 minutes. At these high temperatures, thermal relaxation is very fast. In fact, by ~270°C for the devices used in these measurements, the Si behaves like an intrinsic semiconductor.

The device physics that govern the MOS capacitor during TSC measurements are now described. When a fixed bias is applied across an MOS capacitor, a fixed amount of charge develops on the two sides of the dielectric. On the Si side, depending on the bandbending, the charge is shared among the inversion layer, depletion region, accumulation layer and the interface states. If there is no fixed charge in the oxide, the net charge on the Si side is equal in magnitude to that on the gate electrode side. Variations in ψ_s or the annealing of charged interface states change the distribution of charge on the Si side but not the net amount. Therefore, no deviation of charge from equilibrium occurs, and no external current flows in the biasing circuit.

When fixed charge exists in the oxide, compensating image charge is induced in both the Si and the gate electrode . If the charge in the oxide changes location, the image charge is also affected which perturbs the magnitude and balance on each

side of the oxide. Since the MOS capacitor is in thermal equilibrium, concurrent with the change in the oxide charge, current flows in the external biasing circuit to restore the proper magnitude of charge on each side of the oxide. Therefore, the TSC technique measures the charge perturbations induced by charge changes in the oxide, not the redistribution of charge on the Si side of the oxide between the inversion layer, depletion region, accumulation layer and interface states. These arguments are identical to those used to derive voltage shifts in MOS capacitors and are an application of Gauss' law.[1]

Consider the example of an MOS capacitor at room temperature fabricated on n-type Si biased with a constant negative voltage into inversion. Negative charge is induced on the gate while positive charge resides in the depletion region and inversion layer. Bandbending places the Fermi level at the interface near the valence band, so that donor states above the Fermi level are positively charged while acceptor states below are negatively charged. The introduction of trapped holes in the oxide near the Si-SiO$_2$ interface reduces the bandbending in the Si, thereby reducing the magnitude of positive charge in the inversion layer and at interface states. By Gauss' law, the electric field in the oxide between the oxide trapped charge and the gate electrode is almost the same with or without oxide trapped charge. Annealing of the oxide trapped charge near the Si-SiO$_2$ interface and its movement toward the gate upsets the image charges induced on the Si side, and results in a flow of electrons in the external circuit from the Si toward the gate. The degree of bandbending increases as a result of this charge redistribution. For the case of interface states, the emission of an electron during the annealing of a charged acceptor interface state results in the loss of an inversion layer hole and a decrease in the bandbending. The emission of a hole during the annealing of a charged donor interface state results in the addition of a hole to the inversion layer and an increase of the bandbending. In neither case does current flow in the external circuit.

If interface states were to contribute to the TSC signal, then their contribution should be evident in the TSC spectrum. Different parts of the interface state distribution can be charged by varying ψ_s, and only these charged interface states then would emit charge. The following TSC measurements were made to examine whether variations in ψ_s, leading to changes in the occupancy of the interface states, affect the TSC signal. Poly-Si gate capacitors with pyrogenic, NPOA oxides were irradiated to doses ranging from 21 krad(Si) to 1 Mrad(Si). The high-frequency C-V curves, shown in Figure 1, indicate significant stretchout. The TSC spectrum for this type of sample consisted of a well-defined peak at a relatively low temperature, which makes any changes due to the contribution from interface states easier to detect. As can be seen from the C-V curves, at the gate bias of -5V used during the TSC measurement, ψ_s at the beginning of the TSC measurement varies from inversion to approximately flatband, depending on radiation dose. During the TSC measurement, ψ_s changes with temperature and with the annealing of interface states and moves toward midgap. The TSC spectra for various doses, previously reported in Reference 12, are shown in Figure 2. Only two features are present: the large, low-activation-energy peak at 0.9 eV and the low-level broad distribution at ~1.4 eV. No features dependent on ψ_s are observed. These results support the conclusion that interface states do not contribute to the TSC signal.
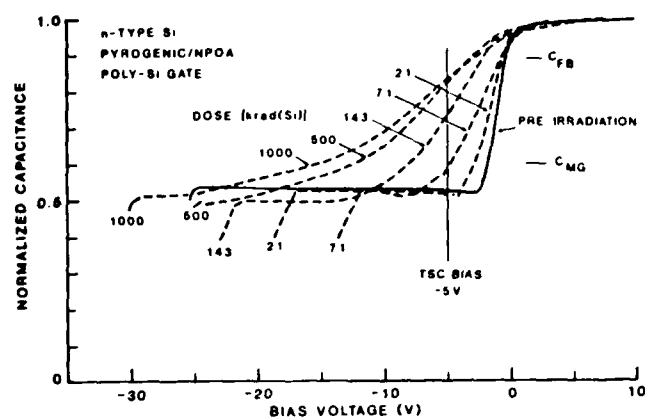
Figure 1. C-V data from a capacitor irradiated to various doses. The bias used during the TSC measurement is also shown to indicate the degree of bandbending. C_{fb} and C_{mg} are the capacitances at flatband and midgap, respectively.
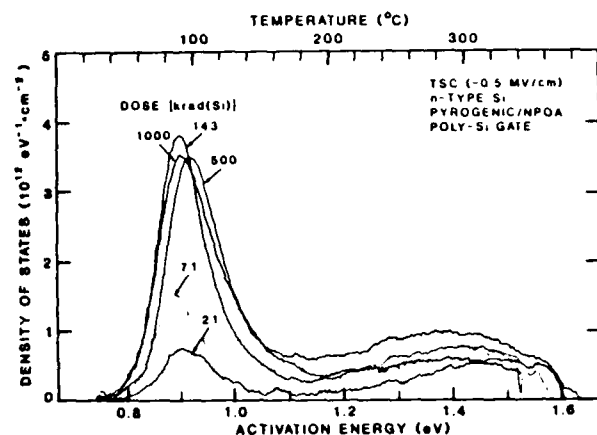
Figure 2. TSC-derived density of states for trapped holes versus activation energy.

TSC/C-V Technique

Voltage shifts obtained from C-V measurements taken after irradiation and after the TSC measurement yield the net charge removed from the capacitor during the anneal under bias that occurs during the TSC measurement process. The net charge density, qN_{total}, corresponding to the C-V voltage shift is equal to the sum of qN_{it}, and the charge density of trapped holes, qN_{ot}, present in the oxide near the Si-SiO$_2$ interface. The value of $qN_{it}(\psi_s)$ is the difference between the density of charged donor interface states, qN_{it}^+, and of charged acceptor interface states, qN_{it}^-. N_{it} can be expressed as the integral of the difference between the unoccupied donor density of states, $D_{it}^d(\psi_s)$, and the occupied acceptor density of states, $D_{it}^a(\psi_s)$.[1] Donor interface states above a given surface potential will contribute positive charge while acceptors below will contribute negative charge. As the value of ψ_s changes such that the Fermi level at the interface moves from a position near the valence band to one near the conduction band, the value of N_{it} decreases monotonically.

Data from C-V and TSC measurements can be used to determine N_{it} at various ψ_s. The difference between N_{total} and N_{ot} gives N_{it}:

$$N_{it}(\psi_s) = (C_{ox}/qA)(V_{post}(\psi_s) - V_{pre}(\psi_s)) - N_{ot} , \quad (1)$$

where C_{ox} is the oxide capacitance, A is the area of the device, and $V_{post}(\psi_s)$ and $V_{pre}(\psi_s)$ are the bias equivalent to a given surface potential from C-V curves taken after and before irradiation, respectively. The relationship between ψ_s and the applied bias is determined by Terman analysis.[1] The ideal depletion capacitance is calculated for a given ψ_s and matched to the same value of the depletion capacitance calculated from measured C-V curves. The value of the applied bias corresponding to the given ψ_s is used in Eq. (1). After correcting for inductance in the C-V measurement circuit, the error in the voltage shift is 5% for a surface potential corresponding to midgap and 10% at inversion. At accumulation, the errors are considerably larger. These uncertainties are mainly due to errors in the doping concentration which is used in calculating the ideal depletion capacitance.

In various interface state measurement techniques, such as Terman analysis, the results are given as the total interface state density, $D_{it}(\psi_s)$, which is the sum of $D_{it}^d(\psi_s)$ and $D_{it}^a(\psi_s)$. From C-V measurements, D_{it}^d and D_{it}^a cannot be determined separately. The sign of N_{it} obtained from Eq. (1), however, establishes the dominant type of radiation-induced interface state for a given surface potential.

The values of $D_{it}(\psi_s)$ can be directly calculated by differentiating $N_{it}(\psi_s)$.[1] The equivalence of this method for obtaining D_{it} to that used in Terman analysis can be seen by differentiating Eq.(1). The result is the difference between the interface density before and after irradiation obtained by the method of Terman analysis. Integrating D_{it} obtained from Terman analysis does not give N_{it} since the integration constant is not known.

Conductance Technique

An alternate technique for determining interface state properties is conductance measurements. From the analysis of such data, D_{it} and the dominant type of interface state at various values of ψ_s can be determined. If N_{ot} and its effect on the interface can be estimated, N_{it}^+ and N_{it}^- can be calculated.[1] Compared with C-V methods, the conductance technique has greater sensitivity when the density of interface states is low but is often limited to a narrower range of ψ_s. The conductance technique was first utilized by Nicollian and Goetzberger[16] and is described in detail elsewhere.[1] A brief summary is given here.

The analysis of conductance measurements is simplified when the MOS device is in depletion since generation and recombination of majority carriers by interface states located within a few kT of the Fermi level dominate over that of minority carriers. When an ac probe signal of an amplitude within the small-signal regime is applied to the MOS device, the position of the Fermi level will oscillate about a mean value of the surface potential, determined by the dc bias, leading to a change in the occupancy of the interface states near the Fermi level. The relative difference between the majority-carrier capture and emission rates and the frequency of the applied signal results in an energy loss which can be measured as the interface conductance, from which the interface state density, D_{it}, and the characteristic time constant are obtained. Nicollian and Goetzberger found that the dispersion in the interface time constants was greater than that predicted by Schottky-Reed-Hall models.[16] This led to the proposal that the dispersion was due to a statistical variation of the surface potential described by a Gaussian distribution with a standard deviation

of σ_s. Since the surface potential is affected by the presence of interface states, the dominant type of interface state can be readily determined from the behavior of σ_s as a function of mean surface potential.[1] If σ_s increases as the interface states are emptied, donor-like states dominate, while if σ_s decreases, acceptor states are present in greater numbers. If σ_s remains constant, then the sum of the number of donor and acceptor states is constant.

Estimates of N_{it}^+ and N_{it}^- for a given surface potential can be obtained from values of σ_s if the charge distribution and its effect on σ_s are known. In the original analysis of Brews,[17] an exponentially decaying charge distribution was assumed. Werner et al.[18] extended the analysis to include the case of a rectangular trapped hole charge distribution of a given width located in the oxide some distance from the Si-SiO$_2$ interface. As the charge distribution is placed farther away from the interface, the contribution to the statistical variation of the surface potential decreases rapidly. From these results, a corrected expression relating σ_s to N_{ot}, N_{it}^+, and N_{it}^- can be obtained.

An HP4192 impedance analyzer was used to obtain admittance data over a bias range corresponding to values of ψ_s extending from flatband to midgap at various frequencies. The frequency range extended from 1 kHz, below which the accuracy of the instrument is reduced significantly, to 3 MHz, where circuit resonance effects were noticeable. The data acquisition and analysis were automated.

After correcting for the oxide capacitance and series resistance, the interface conductance, G_p, was obtained for various biases and measurement frequencies. Plots of G_p/ω versus ω, where ω is the angular frequency, and G_p versus bias reveal the characteristic features of typical conductance behavior described by Nicollian and Brews.[1] The density of interface states, the standard deviation of the surface potential and the interface time constants were obtained. The error in G_p is 3% while the errors in D_{it} and σ_s are as large as 30% and 15%, respectively. These relatively large errors were caused by the large frequency increments and digitization associated with the present instrument.

RESULTS AND DISCUSSION

A comparison of the values of N_{ot} obtained from TSC measurements and N_{total} at midgap $(C_{ox}\Delta V(mg)/q)$ obtained from C-V measurements is shown in Figure 3. Also shown is a solid line representing $C_{ox}\Delta V(mg)/q$ equal to N_{ot}, the "midgap line". The inset magnifies the region near the origin. The various symbols identify different fabrication processes. Filled symbols indicate Al-gate capacitors. Error bars are shown for several data points to indicate the accuracy of the data.

The data shown in Figure 3 do not support the assumption that voltage shifts at midgap can in general be used to determine N_{ot}. Even at low values of N_{ot}, there are many data points with deviations from the midgap line which are larger than the error bars. At large values of N_{ot}, $C_{ox}\Delta V(mg)/q$ is consistently larger than N_{ot}.

How large is the discrepancy if $\Delta V(mg)$ is used to estimate N_{ot}? This fractional deviation of $C_{ox}\Delta V(mg)/q$ from N_{ot} is plotted in Figure 4. The figure shows that if the midgap tech-
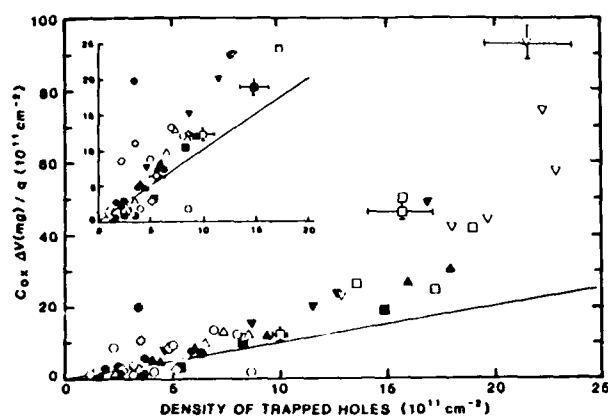
Figure 3. Number density determined from midgap voltage shifts versus density of trapped holes in the oxide determined from TSC measurements. Symbols represent samples fabricated by the various processes described in the text. The inset magnifies the region near the origin.
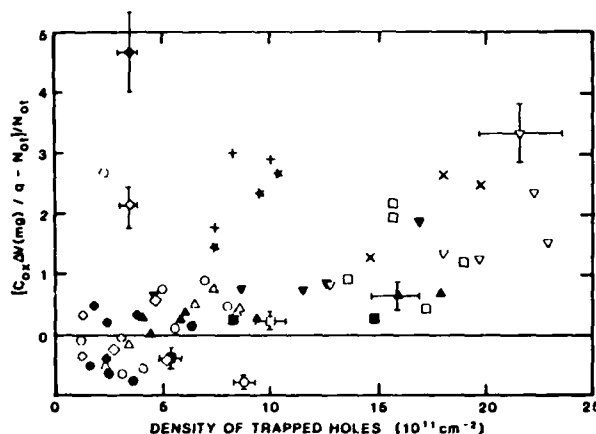

Figure 4. Fractional deviation of $C_{ox}\Delta V(mg)/q$ from the density of trapped holes in the oxide.

nique is used to estimate N_{ot}, most errors will be less than a factor of unity but some can be greater than a factor of four. The uncertainly in the data for several points are indicated. Again both negative and positive deviations occur. Two points should be noted from Figures 3 and 4. First, the data do not imply that there is a universal relationship between N_{ot} and either $C_{ox}\Delta V(mg)/q$ (Figure 3) or the fractional deviation of $C_{ox}\Delta V(mg)/q$ (Figure 4). Second, the data are not necessarily monotonic. As an example, data from test capacitors that have undergone a complete integrated circuit fabrication process (the open diamonds) first increase and then decrease with N_{ot}. These trends reflect the complex dose and processing dependence of the generation kinetics of radiation-induced interface states.

The data presented in Figure 4 were shown to be equivalent to $N_{it}(\psi_s(mg))/N_{ot}$, where $N_{it}(\psi_s(mg))$ is the net interface state charge density at midgap. Positive values indicate dominance of donor interface states in the upper half of the bandgap; negative values indicate dominance of acceptors in the lower half. At midgap, P_b centers would not contribute to N_{it}. Figure 4 indicates that for large N_{ot}, the donor dominates. At lower values of N_{ot}, either the donor or the acceptor may dominate depending on processing history and dose.

Values of N_{it} were not only obtained at midgap but also for a range of surface potentials. An example of the results is shown in Figure 5 for an n-type Si, pyrogenic capacitor. Results for this device were previously reported only for midgap and flatband surface potentials.[13] Two types of radiation-induced interface states are suggested by the data: the P_b center which continues to grow with dose and a donor-like state in the upper half of the Si bandgap which saturates above a dose of ~500 krad(Si). For other fabrication processes, the interface states exhibit different dose-dependent generation kinetics. An additional acceptor state below midgap was suggested by data for p-type Si capacitors. Samples from all fabrication processes investigated have shown a donor state extending from midgap toward the conduction band. The density of this state is very dose dependent and often extends above the surface potential that would correspond to flatband in an n-type Si device. The existence of this set of interface states with their complex generation kinetics disagrees with the underlying assumption of the midgap technique. We therefore conclude that the midgap technique is not a generally valid technique for determining N_{ot} and independent measurements are required to test its validity in each application.

We now show that the discrepancy between charge densities obtained from TSC measurements and C-V voltage shifts cannot be reconciled by assuming that only P_b-like interface states exist which contribute to the TSC signal. As a specific example, the post-irradiation and post-TSC C-V curves for a p-type capacitor irradiated to a dose of ~4.4Mrad (Si) are shown in Figure 6 . A large stretchout is seen from midgap to inversion. Terman analysis of the data in Figure 6 produces a D_{it} with a very large and broad distribution extending from below midgap toward the conduction band edge. $\Delta V(mg)$ is equivalent to a charge density of $19.7 \times 10^{11}cm^{-2}$ while the corresponding value obtained from the TSC current is $3.4 \times 10^{11}cm^{-2}$. During the TSC measurement the capacitor is biased at -2.4V which corresponds to a ψ_s of 0.15V above midgap (weak inversion) at the beginning of the TSC measurement. If P_b centers are the only type of interface state, then only acceptor levels are charged. As the TSC measurement proceeds, the Fermi level moves toward midgap and releases only electrons. However, the bandbending is such that electrons cannot flow in the external circuit. Even if they could, those electrons would increase the TSC signal and not decrease it as is observed. Therefore, the existence of only P_b-like interface states that contribute to the TSC signal can not, in general, explain the discrepancy between $\Delta V(mg)$ and TSC changes.
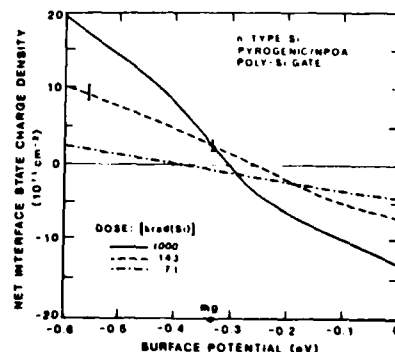

Figure 5. Net interface state charge density derived from combining TSC and C-V data as described in the text.
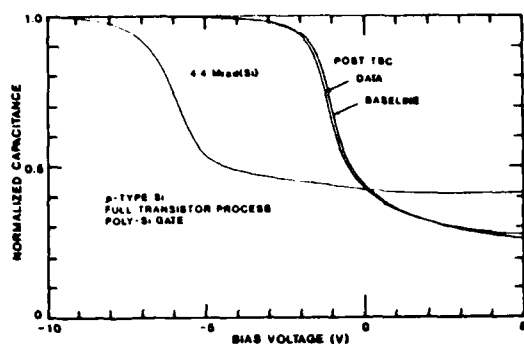
Figure 6. C-V data for a capacitor after irradiation to a dose of 4.4 Mrad(Si). Also shown are capacitance curves obtained after the TSC data and baseline measurements.

An independent determination of whether the amphoteric P_b center is the only type of interface state was obtained from conductance measurements. Typical conductance data are shown in Figure 7 for a POA pyrogenic oxide capacitor fabricated on n-type Si which was irradiated to a dose of 100 krad(Si). In Figure 8 the values of D_{it} derived from both Terman analysis of 1-MHz C-V data and from the conductance technique are plotted. Good agreement is observed. Values of σ_s for various surface potentials obtained from post-irradiation conductance measurements on the same sample are shown in Figure 9. These values tend to increase as the interface states are emptied. This increase in the surface potential fluctuation can only be due to an increase in the number of charged interface states such as would be expected from donor interface states. Therefore, these conductance measurements also indicate the existence of other than P_b-like interface states.

The net interface state charge density obtained by combining the data from TSC and C-V measurements is also shown in Figure 9 for the same sample. In this figure, flatband is at the origin of the surface potential axis with the valence band being toward the left. The values of N_{it} are observed to be positive and increase as the surface potential decreases. The sign of N_{it} indicates that a donor interface state is present in this part of the bandgap with a greater number density than that for acceptors. Therefore, both the conductance and TSC/C-V measurements independently show the existence of a donor interface state in the upper half of the bandgap.

The variation of σ_s with ψ_s has shown the dominance of a donor interface state in a range of ψ_s above midgap. We now show that the magnitude of σ_s is consistent with the results obtained from TSC/C-V measurements. The densities of donor and acceptor interface states, N_{it}^+ and N_{it}^-, are calculated as described earlier. For our calculation, in addition to the charged interface states, a rectangular charge distribution is assumed to be located in the oxide at a distance of ~30Å from the interface with a width of ~10Å. The value of N_{ot} obtained from TSC measurements was used for the magnitude of this charge. From the results of Werner et al.[19], a correction factor of ~0.5 was obtained. A free parameter λ, which characterizes the charge distribution associated with the interface states, can vary from 75 to 1200Å with the most likely value ranging from 75 to 200Å[10]. The calculated values of N_{it}^+ and N_{it}^- at ψ_s=-0.1 eV are 3.2±1 x 10^{11} cm^{-2} and -0.8±1 x 10^{11} cm^{-2} for λ=75Å, increasing to 10.7± 1 x 10^{12} cm^{-2} and 10.3±1
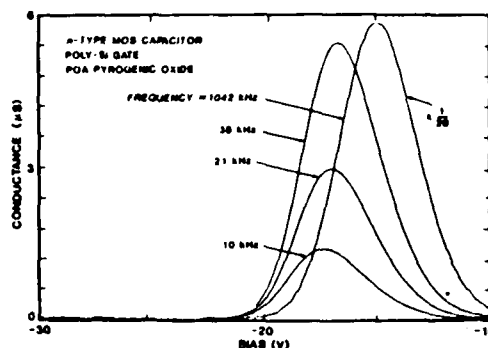
Figure 7. Conductance versus bias at various frequencies. The conductance has been corrected for series resistance.
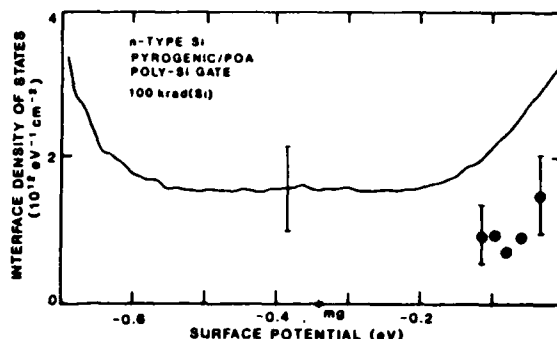
Figure 8. Radiation-induced interface state density obtained from Terman analysis of a high-frequency C-V measurement (solid line) and from a conductance measurement (solid circles).
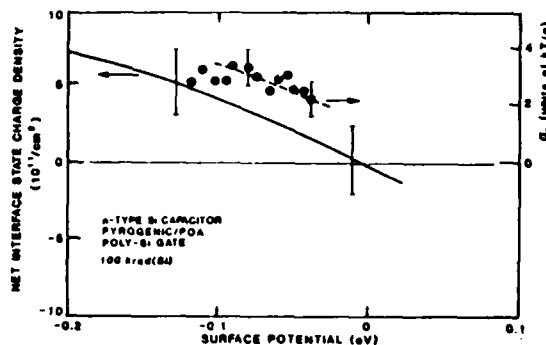
Figure 9. Net interface state charge density (solid line) showing the dominance of a donor interface state above flatband. The behavior of the standard deviation of the surface potential fluctuations derived from conductance measurements (solid circles) also suggests the dominance of the donor.

x 10^{12} cm^{-2} for λ=1000Å, respectively. In all cases, N_{it}^+ is approximately equal to or larger than N_{it}^-, consistent with the presence of donor interface states.

The interface time constants, τ, were also calculated from the conductance data. It was found that a semilogarithmic plot of τ versus surface potential is linear with a slope of $1/kT$. This behavior agrees with the expected exponential dependence of τ predicted from the interface trap model[1] and confirms that the energy loss measured by the admittance technique is due solely to majority carriers at the Si-SiO$_2$ interface.

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SUMMARY AND CONCLUSIONS

The use of the midgap technique is a convenient but not generally valid method for determining N_{ot} for MOS devices fabricated on <100> Si. This technique is based on the assumption that the value of N_{it} is zero at midgap which would be true if the interface states were solely amphoteric P_b centers. Both conductance and TSC/C-V measurements independently show that other interface states exist in addition to P_b centers, thereby making the general validity of the midgap technique questionable. From TSC/C-V measurements, values of $N_{it}(\psi_s)$ obtained for various fabrication processes and dose levels showed the existence of a donor in the upper half of the bandgap and an acceptor below midgap in addition to the amphoteric P_b center. No single surface potential exists that is the neutral point for N_{it} for all fabrication processes and radiation doses. The data presented here show that the charge associated with the radiation-induced midgap voltage shift observed in C-V measurements differs from the value of N_{ot} obtained from TSC measurements. For most capacitors measured, deviations are less than 100% but some are greater than a factor of four.

Arguments for the validity of the TSC technique for determining N_{ot} independent of other measurements were presented and tested experimentally by showing that the TSC density of states spectra are insensitive to variations in the surface potential. Discrepancies between N_{ot} obtained from TSC measurements and midgap voltage shifts generally can not be resolved by assuming the sole existence of amphoteric P_b-like interface states which contribute to the TSC signal.

The conclusions regarding interface states presented above are consistent with those in the literature. The existence of donor interface states in the upper half of the Si bandgap has been proposed previously by Sah et al.[8] who attributed peaks in the interface state density to donor states located in the upper half of the bandgap. They used Terman analysis to evaluate the data for samples which underwent photogenerated injection of holes. The assignment of a donor was based on annealing kinetics. Model calculations [19,20] have also predicted the existence of interface states throughout the Si bandgap. The assumptions in these models have not been sufficiently specific to assign a configuration or defect to an observed interface state. Calculations by Sakurai, et al.[20] have shown possible configurations for donors in the upper half of the bandgap. Ma[21] has also obtained results using quasistatic C-V measurements that show the slow conversion (50-150 hrs) of an interface state in the upper half of the bandgap to an interface state in the lower half of the bandgap. Such behavior does not seem to be consistent with interface states being solely P_b centers.

In conclusion, the data presented here from TSC, C-V, and conductance measurements all show that the voltage shift at midgap is not generally valid for determining radiation-induced oxide trapped charge. The use of the midgap-voltage-shift technique can result in deviations of less than 100% to greater than a factor of four. Whether these errors are significant will need to be assessed by the user of the midgap technique in each application.

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ANGULAR DEPENDENCE OF CHARGE FUNNELING IN Si AND GaAs DEVICES*

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ABSTRACT

Charge collection and transient current measurements on n-type GaAs and Si Schottky diodes bombarded with single alpha particles reveal a strong dependence on angle of incidence. Prompt recombination is evident in both materials. The magnitude of charge collected by funneling is proportional to the charge generated in the depletion region. An alternative interpretation of the data is that charge generated to a certain depth below the junction, proportional to the depletion width, is collected by funneling. The increased collection of charge with increasing angle appears to be due to a longer collection time. These measurements indicate that dynamic processes occur during charge funneling which are not fully described by existing phenomenological models.

INTRODUCTION

A high-energy charged particle, such as a cosmic ray, that interacts with a semiconductor material produces a track of dense ionization. If the track passes through a critical node in an electronic device, device operation can be upset if sufficient charge flows into that node.[1] Charge collection occurs by both drift and diffusion. The drift component consists of charge created in the depletion region and charge which is collected from beyond that region by funneling. Funneling refers to the redistribution of the depletion-region electric field into the previously neutral semiconductor and the subsequent collection of charge in the ion track by drift at the struck node.[2] The diffusion component is simply that charge which diffuses to the depletion region edge and is then collected at that node.

Various models have been proposed to explain charge funneling. One widely used analytic description is the McLean-Oldham (M-O) effective funnel length model[3] and its derivative.[4] These models are based on the following picture of charge funneling. After the passage of a highly ionizing charged particle through a junction in a semiconductor device, the resulting plasma is thermalized in a time on the order of picoseconds.

The separation of electron-hole pairs in the original depletion layer results in neutralization of the depletion layer electric field, collapse of the junction, and propagation of the electric field (initially confined to the depletion layer) along the track into the previously neutral substrate. The time necessary to establish the new field distribution is determined by the dielectric relaxation time of the substrate. At the same time the above effects are occurring, charge in the track separates radially by ambipolar diffusion. The result is rapid charge collection from the edge of the track by drift. Collection continues until the plasma density drops to approximately the substrate doping density. The duration of charge funneling is determined by the radial ambipolar diffusion process which is not expected to depend on angle of incidence. This picture of funneling implies that varying the angle between the ionized track (i.e., the incident particle) and the surface of the device should not affect either the collection time or the amount of charge collected.

The M-O model has been successful in describing the bias and doping dependence of the collected charge, especially for low LET particles.[3] However, no measurements of the angular dependence of charge funneling have been reported. Contrary to the expectation described above, we have observed a strong angular dependence of the funnel contribution to the collected charge. The objective of the present investigation is to determine experimentally the angular dependence of charge funneling and thereby obtain enhanced insight into collection processes and phenomena.

In this study, measurements have been made of the magnitude of the charge collected by the funneling and its temporal dependence in Schottky diodes fabricated on both n-type Si and GaAs. We first describe the experimental procedures used, followed by a presentation and discussion of the results for both types of devices. We then compare the data with expectations based on funneling models in the literature.

EXPERIMENTAL PROCEDURE

Charge collection and transient current measurements were made on diodes bombarded by alpha particles at various incident angles with various reverse biases applied. Devices studied were n-type GaAs Schottky-barrier diodes fabricated on a 20-μm epi layer doped to 1.4×10^{15} cm^{-3} and Si Schottky diodes fabricated on bulk n-type Si substrates doped to 2.5×10^{15} cm^{-3}. Figure 1 shows a schematic representation of a device and the track resulting from the passage of an alpha particle. Although only the Si diodes were fabricated on bulk material, the epi thickness for the GaAs diodes was greater than the alpha particle track length. We therefore assume that the GaAs results are representative of bulk semiconducting GaAs material. The Si diodes were 200 x 200 μm square with a 1-μm thick aluminum metallization. The gold metallization on the GaAs devices had a thickness of 0.2 μm and a 250-μm diameter. The same devices were previously used in an investigation of the doping and bias dependence of charge collection.[5]
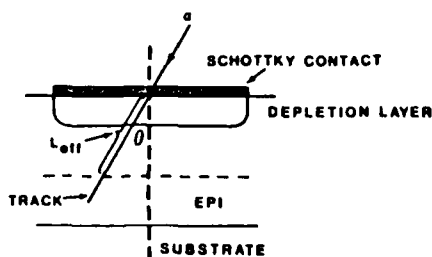
Figure 1. Schematic diagram of the Schottky diodes studied. The Si devices were fabricated in bulk substrates. The incident alpha particle track is also shown.

For both charge collection and transient current measurements, a Cm^{244} alpha particle source was mounted behind an aperture which limited the divergence of the beam to $\pm 4°$. The angle between the beam and the device surface could be varied from 0° to nearly 90° in either direction (0° was normal to the surface). After passing through ~9 mm of air, the particle energy decreased to 5.1 MeV. Charge collection measurements were made using the same techniques described previously.[6,7] Both prompt and total charge (the sum of the prompt and delayed diffusion currents) were measured. Typically, six measurements of collected charge were made on each device for each combination of bias and angle. The mean and standard deviation was calculated for both prompt and total charge. The measured prompt charge consists of charge collected by funneling and by diffusion during the first 1.3 ns which corresponds to the system risetime. Prompt charge was measured using a 500-MHz probe and a transient digitizer. To determine the funneling contribution, the diffusion component was subtracted from the prompt charge. That contribution occurring during the first 1.3 ns in GaAs was estimated using the Wirth and Rogers expression for transient diffusion current.[8] The parameters needed in their expression were estimated from an analysis of the delayed component of the collected charge. An average GaAs diffusion length of 4 μm was determined. Since diffusion lengths in Si are longer than the alpha track length, the Wirth and Rogers expression could not be used; the modified diffusion expressions of Sigridsson and Leman[9] were employed instead. In both materials, the largest diffusion contribution to the prompt charge occurred at low biases and small angles. For a 5-volt bias the contribution in GaAs ranged from 10% to 14%, while at 40 V the range was from 2% to 4%. In Si, the contributions were less than 7% at the biases and angles reported here.

When the total charge was collected within 15 to 20 ns, this system provided accurate total charge values; otherwise, the RC time of the electronics affected the data. When the collection time for the total charge was longer than 20 ns, a lower-bandwidth passive probe and amplifier were used to measure the total collected charge.[6] To verify the calibration of the passive probe system, a nuclear instrumentation preamplifier, a research amplifier and a multichannel analyzer were also used to measure the total collected charge.

The temporal characteristics of the SEU transient current were also measured for GaAs diodes. Devices were mounted on a 50-Ω microstrip fabricated on an alumina substrate. The signal was transferred to a semirigid coaxial cable via a SMA launcher. This signal was then amplified by either two or three amplifiers with bandwidths from 3 to 7 GHz and then was measured by a 4-GHz oscilloscope. To isolate the dc bias supply from the transient signal a Picosecond Pulse Labs 5550A bias tee was employed. This system has much better impedance uniformity ($\leq 9\%$) than the previously used system,[5] resulting in significantly less waveform distortion.

The measured waveforms obtained from the transient current measurements were recorded on photographic film, enlarged and then digitized for input into a computer for digital signal processing. The digital signal processing, which used a circuit model of the diode and front-end electronics similar to that previously described,[5] converted measured voltage to a current waveform. No inductance was necessary in the model because of the improvement in impedance matching for the various components. Also, instead of using a bilinear transformation for conversion from the frequency domain to the Z domain, a direct transformation was employed.[10] This transform produced improved agreement between the magnitudes of the collected charge obtained from the charge collection and the transient current measurements.

RESULTS

Results of the charge collection measurements are presented first. Data for a GaAs device biased to 5 V are shown in Figure 2. Error bars show the standard deviation for repeated measurements. Both the total charge collected and the charge collected by funneling are presented. The funnel charge increases by almost a factor of four as the angle of incidence increases from 0° to 80°. The total charge increases by a factor of two for the same change in angle. The increase in both total and funnel charge is less pronounced at higher biases. The calculated net charge generated in the initial depletion layer is shown as a solid line. (The net charge generated for GaAs refers to that charge which remains after an assumed 15% prompt recombination has occurred.)[6] The decrease in collected charge at large angles is the result of increasing energy loss of the incident alpha particle in the 0.2-μm Au layer.

Collected charge for a Si diode at various angles of incidence is shown in Figure 3 for the case of 10 V bias. The strong angular dependence of funnel charge is also evident in Si. The funnel charge increases by a factor of five as the angle of incidence increases from 0° to ~80°. The total charge, however, is constant independent of angle. An angle-independent total charge implies that the diffusion length is longer than the track length, which is consistent with the long minority-carrier lifetimes expected in high-quality Si with moderate excess carrier densities. The duration of the charge collection is ~300 ns at 0° which compares well with the calculated diffusion time of ~200 ns. The diffusion time was calculated by dividing the square of the track length by the diffusivity of ~30 cm^2 sec^{-1} for Si. The magnitude of the total collected charge, however, is considerably less than the charge generated in the Si (220 fC). Approximately 40% of the generated charge is not collected. Others have also reported similar loss of total charge in diodes fabricated on bulk Si.[3] This behavior of the total charge, i.e., the lack of angular dependence and partial collection of generated charge, can be reconciled by assuming the occurrence of prompt Auger recombination.[6] Prompt recombination is also supported by the observation that at high angles, where the
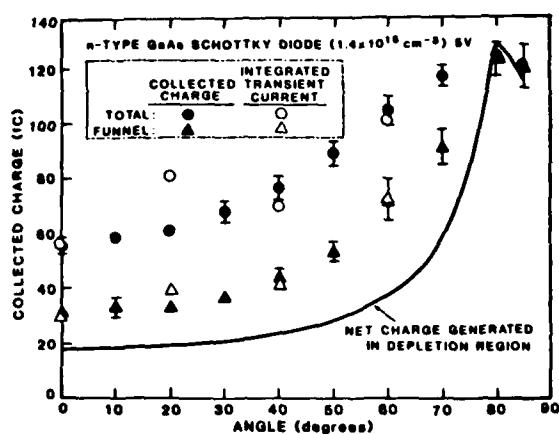
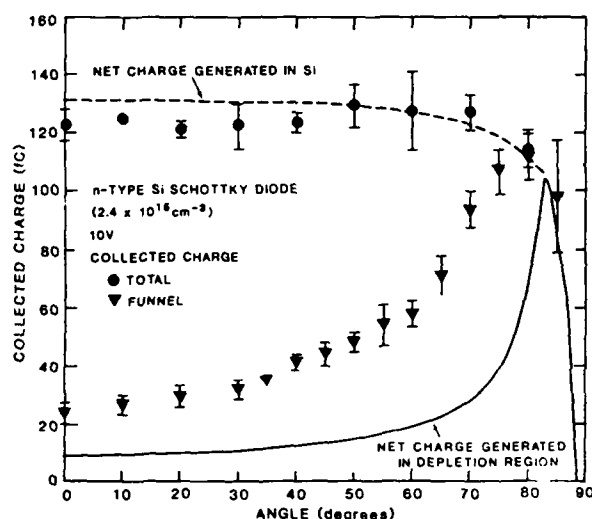Figure 2. Collected charge and integrated transient current versus angle of incidence for a GaAs diode.

Figure 3. Collected charge versus angle of incidence for a Si diode.

track is enclosed completely in the depletion layer, ~40% of the total generated charge is not collected. Preliminary charge collection measurements on diodes fabricated on higher resistivity Si also indicate prompt charge loss but of lower magnitude. For a surface barrier detector with even higher resistivity (> 1kΩ-cm), no recombination was observed using the charge collection instrumentation. Therefore, the prompt recombination process seems to be doping dependent.

To examine whether the assumption of Auger recombination is reasonable, we estimate the amount of charge that recombines following the procedure outlined by Hopkins and Srour.[6] Assuming that 50% of the charge is generated in a central core of ~40 Å diameter,[11] an excess density of 2×10^{21} cm^{-3} is obtained. Using an Auger coefficient[12] of ~10^{-31} cm^6 sec^{-1}, 85% of the core excess density recombines in ~50 ps, in reasonable agreement with the observed prompt recombination of ~40%. For the remainder of this paper, we assume 40% prompt charge recombination in the Si devices measured.

The funneling contribution to the prompt charge in both GaAs and Si diodes normalized to the net charge generated in

the original depletion layer is plotted in Figure 4 versus angle of incidence for various biases. For angles up to ~50°, the ratio is independent of angle and bias. The normalized funnel charge has a value of ~1.8 for GaAs and ~3.0 at Si at the biases measured. At higher angles, where all the unrecombined charge is collected promptly, the data follow the total net charge generated normalized to the net charge generated in the depletion layer, shown as a sloping line.
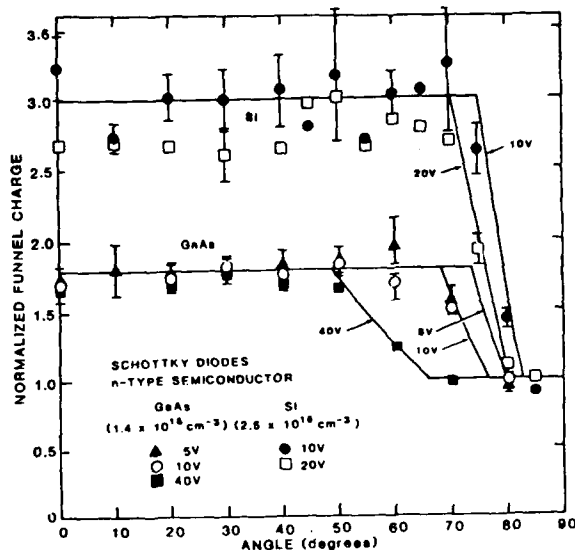

Figure 4. Funnel charge normalized to the net charge generated in the original depletion layer versus angle of incidence.

An alternate presentation of the data is shown in Figure 5 where the funnel charge has been converted to an effective funnel length, L_{eff}. The effective funnel length is defined as the distance down the track needed for integrating along the Bragg curve to obtain the experimentally determined funnel charge (see Figure 1). This L_{eff} is normalized to the length of the track in the original depletion layer. Figure 5 shows that the normalized L_{eff} is also constant out to ~50°. For GaAs, the normalized L_{eff} is also weakly dependent on reverse bias. The scatter in the data for Si diodes is larger so no conclusion regarding bias dependence can be made.

The difference between these two representations of the data, i.e., normalized funnel charge and normalized effective funnel length, arises because the charge generated varies with distance along the track.[13] If the charge generated per unit distance along the track was constant as is assumed in various models and simulations, both representations would be the same. However, these two representations have different implications for understanding the funneling process.

The variation in collected funnel charge with angle results from either a change in collection time or a change in the magnitude of the current or both. The constant value of the normalized funnel charge with angle and bias implies that charge generated in the original depletion region determines the magnitude of charge collected by funneling. This is the same region where it is assumed that neutralization of the electric field causes the collapse of the junction which initiates the funneling process. The behavior of the normalized charge implies that the charge generated in the original depletion region does more than just initiate charge funneling. It may also determine the magnitude of the current and its duration.
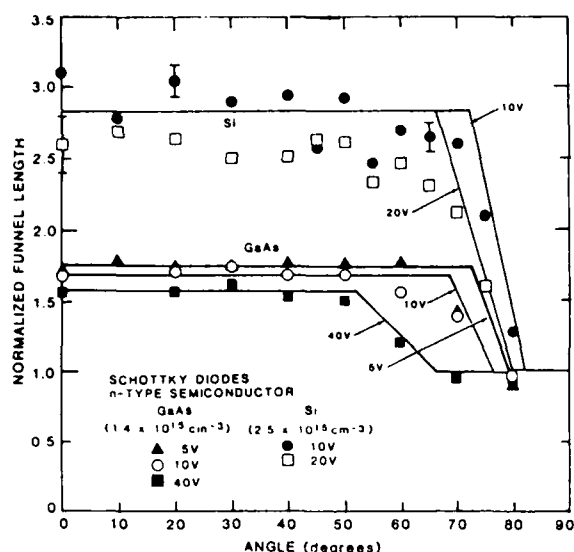
Figure 5. Funnel length normalized to the track length through the original depletion layer versus angle of incidence.

An alternative interpretation of the charge funneling process is obtained from the behavior of the normalized funnel length (Figure 5). The constant value of this length implies that all the net charge generated to a specific depth below the junction is collected by funneling. This depth is nearly proportional to the initial depletion layer width; the proportionality constant is weakly bias dependent and is smaller for larger biases, at least in GaAs. The existence of a fixed collection depth, independent of the amount of charge generated, can be interpreted to indicate that charge flows not only *along* the track toward the junction but also *perpendicular* to the junction. Such an interpretation is suggested by the two-dimensional modeling of Hsieh et al[2] which shows the loss of axial symmetry for field lines in small-area junctions at other than normal incidence. Therefore, large currents would flow directly toward the struck node rather than down the track. This view is again in contradiction to the M-O model[3] where all charge is assumed to be collected by funneling from a fixed distance along the track which is proportional to the original depletion width.

The increase in collected funnel charge with increasing angle must result from either an increase in collection time or an increase in current or both. In order to distinguish between these two possibilities, transient current measurements were made on GaAs devices. Waveforms for a GaAs diode reverse biased to 5 V and to 40 V are shown in Figures 6 and 7, respectively. Figure 6 shows that as the angle of incidence of the alpha particle increases, the duration of the transient current increases with little or no change in amplitude. At 40 V the waveforms are bandwidth-limited so there is no observed change in duration of the transient currents. A comparison of the integrated transient current with the collected charge for a diode biased at 5 V, shown in Figure 2, indicates good agreement.

Although Figure 6 shows that the widths of the waveforms increase with angle, the scatter in the waveforms is large and generally obscures this trend. The following analysis was therefore undertaken to substantiate this trend. For each transient current waveform, the full-width-half-maximum (FWHM) and the peak current amplitude (Ip) were determined and the mean and standard deviation for each bias and angle were calculated.
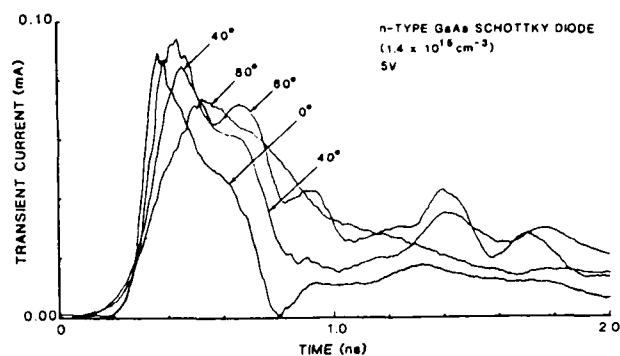
Figure 6. Transient current waveforms for a GaAs diode reverse biased to 5 V for various angles of incidence.
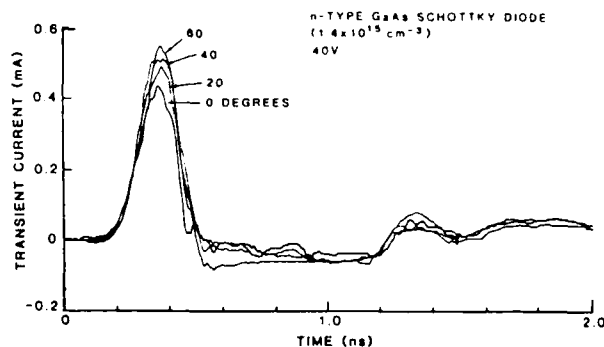
Figure 7. Transient current waveforms for a GaAs diode biased to 40 V for various angles of incidence.

Obviously, when the funnel charge (Q_f) varies, either the current magnitude or duration must change. In Figure 8, I_p and FWHM are plotted versus Q_f for data obtained at two different angles. The parameters presented in this figure were varied by changing the device bias. Varying the bias changes Q_f by a factor of ~2 and changes I_p by a factor of ~4. The FWHM decreases until the bandwidth-limited value of ~180 ps is reached. From Figure 8 we conclude that peak current changes as a function of funnel charge are readily observable in our data.
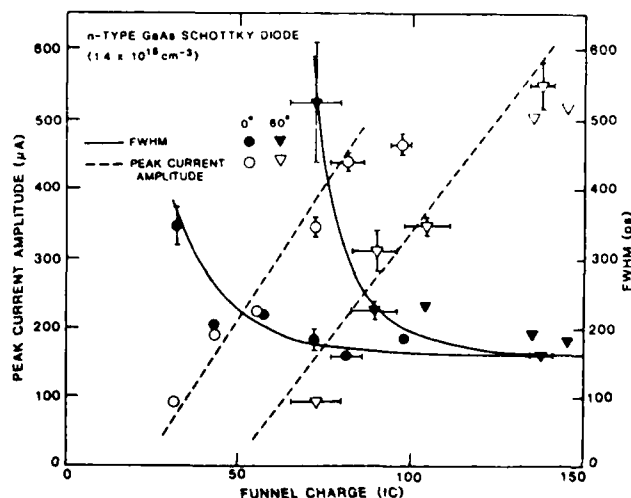
Figure 8. Peak current amplitude and FWHM versus funnel charge for measurements at 0° and 60°. The parameters were varied by changing the bias.

Similar data are plotted in Figure 9 which shows I_p and FWHM versus Q_f for 5 V and 40 V reverse bias. Here Q_f, I_p, and FWHM vary as the angle of incidence is varied. For the 5 V data there is no observed change in I_p with Q_f. The standard deviation of I_p is very small, while for FWHM it is large. Although FWHM does increase with increasing Q_f, the observed change is too small to explain the change in Q_f. The magnitude of I_p does change with Q_f in Figure 8, indicating that our measurements are capable of detecting such changes. However, since I_p does not change with Q_f, we interpret this data to imply that FWHM increases with increasing Q_f, at least for the 5 V data. At higher biases some increase in I_p is observed with increasing Q_f. In all these high-bias cases FWHM is bandwidth-limited so that part of this increase in I_p may be due to bandwidth-limited current integration.

Figure 9. Peak current amplitude and FWHM versus funnel charge for measurements at 5 and 40 V. The parameters were varied by changing the angle of incidence.
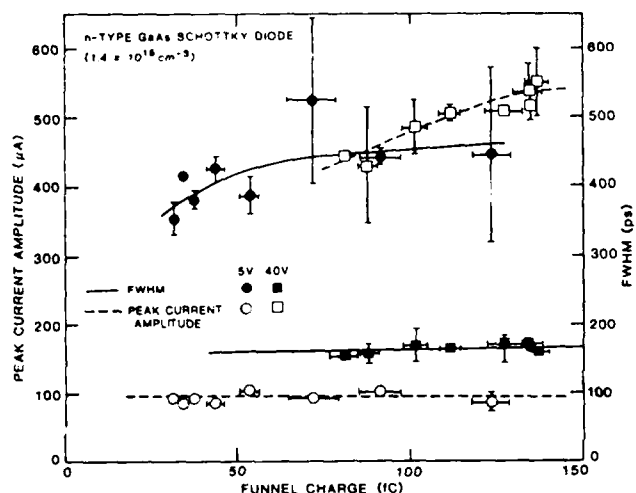
DISCUSSION

A summary of the experimental findings derived from measurements of the angular dependence of charge funneling is now given. A strong angular dependence of funnel charge occurs for both n-type Si and GaAs Schottky diodes. The normalized funnel charge and the normalized effective funnel lengths are independent of angle. The value of the normalized funnel charge is larger in Si than GaAs, assuming prompt recombination in both materials. The normalized effective funnel length has a weak bias dependence for GaAs. Transient current measurements imply that the collection time increases with increasing angle while no change occurs in the maximum current, at least for GaAs diodes biased to 5 V.

The above observations are inconsistent with the McLean-Oldham phenomenological funneling model. The M-O model does not address angular dependence directly. It assumes that the duration of the funnel process is determined by the time necessary for ambipolar diffusion to reduce the plasma density to approximately the background doping density with majority carriers being drawn off by drift into the substrate. The electric field acting on the majority carriers is estimated to be on the order of the average field in the original depletion layer. Ambipolar diffusion is not expected to have an angular dependence.

A possible modification of the M-O model to incorporate the angular dependence of charge funneling would be to allow the electric field to change with angle. If the total potential drop occurred along the track length within some fixed depth such as the initial depletion layer width, the electric field would decrease with angle. For GaAs diodes fabricated on p-type material, the field-dependent electron drift velocity would increase for fields >3kV/cm,[14] and one would predict that the funnel charge would increase with angle. For the n-type GaAs and Si diodes used in the present study, the hole drift velocity decreases with decreasing field. Such a dependence leads to the prediction that the collected funnel charge would decrease, in contradiction to the data.

The refinement of the M-O model developed by Shur et al.[4] does not appear to account for our data either. In that model the funnel charge is also proportional to the field-dependent minority-carrier mobility. The transient current increases linearly with time, with the maximum current occurring at the end of the collection process. The maximum current is also proportional to the field-dependent minority-carrier mobility. Changes of field with angle would result in predictions contrary to our data. Since the underlying physical assumptions in the Shur model are very similar to those in the M-O model, it is not surprising that the same discrepancies exist.

Numerical simulations of charge funneling have not addressed the issue of angular dependence quantitatively. Hsieh et al.[2] have reported qualitative results using two-dimensional simulation. Grubin et al.[15] have simulated charge funneling only for particles at normal incidence. Calculations of charge funneling parameters for devices that have been investigated experimentally are needed to test the validity of the results of these complex computer simulations.

A model that does predict the angular dependence observed here was formulated by Hu.[16] In that model the electric field within the original depletion layer drives majority carriers into the substrate and induces an electric field that drives minority carriers toward the junction. This charge imbalance results in the collapse of the depletion layer. The collection process continues until all the minority carriers are driven out of the original depletion region. The potential drop occurs along the track in the substrate and across the depletion layer as it is reestablished in time. The current during charge funneling is driven by the potential drop that occurs along the track in the substrate. This current decreases with time as majority carriers are removed from the region of the original depletion layer.

The charge collected by funneling in the Hu model depends explicitly on the charge generated in the original depletion layer, which agrees with the normalized funnel charge results shown in Figure 4. The predicted increase in collection time with angle is in agreement with our data as is the predicted angular independence of the maximum current. The Hu model predicts that the magnitude of the funnel charge is proportional to one plus the ratio of minority- to majority-carrier mobilities. As initially shown by M-O for n-type Si, this is in contradiction to experiment. Hu's model predicts that the normalized funnel charge should be ~1.05 and ~1.34 for n-type GaAs and Si diodes, respectively. These values are in marked disagreement with the observed values of ~1.8 and ~3.0. If the appropriate field to use in the charge funneling process

is the field across the original depletion layer, then high-field drift velocities should be used instead of mobilities. The predicted normalized funnel charge would then increase to only ~1.5 and ~1.7, respectively. Moreover, the maximum value of normalized funnel charge obtainable for n-type Si or GaAs in Hu's model is 2.0, in disagreement with the value of ~3.0 determined for Si.

CONCLUSIONS

The present work has shown that a strong angular dependence of charge funneling occurs in both n-type GaAs and Si Schottky diodes. In both materials, the funnel charge is proportional to the charge generated by the alpha particle in the original depletion region. The increase in collected charge with increasing angle is due primarily to longer collection times with little or no change in peak current, at least in GaAs. An alternative representation of the data implies that all unrecombined charge generated within a fixed depth below the junction is collected by funneling. This depth is proportional to the depletion layer thickness.

Although the McLean-Oldham effective funnel length model has been successful in predicting the bias and doping dependence of charge funneling, it does not predict the phenomena described above. Alternatively, a model proposed by Hu does predict the observed angular dependences but does not give the proper magnitudes of the ratio of collected charge in diodes fabricated on n- and p-type silicon.[3] A full examination of the assumptions underlying these two different phenomenological models is needed to aid the development of a more complete understanding of charge funneling.

The results of this study have different ramifications for different types of circuits. If a sensitive junction in a RAM has a relatively fast recovery time compared to the total collection time (e.g., CMOS RAMs,[17] the extrinsic base-emitter junction in I^2L RAMs,[18] or the collector-base and base-emitter junctions in TTL RAMs[19]), then the increased funnel charge at higher angles will increase the likelihood of upset. However, since the increased funnel charge is primarily due to an increased collection time, the occurrence of upset will also depend on the recovery time relative to the duration of the funnel process, so the additional susceptibility to upset can be tempered by design changes. In other circuits, such as DRAMs, the total charge determines the upset sensitivity.[17] In such total-charge-sensitive circuits, upset of Si devices should not show an angular dependence. The concept of effective LET may also need to be reexamined in light of the observed increase in collection time with angle, specifically for high-speed circuits. Finally, our data indicate that prompt recombination also occurs in Si as well as in GaAs. Further study is needed to quantify this effect.

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