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MULTIPURPOSE FIBER OPTIC TRANSCEIVER (MFOX)

RCA Corporation

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This report describes the family of fiber optic transmitters/receivers developed under the MFOX program. The intent of the program was to define, design, fabricate and test a minimum sized family of common module, fiber optic transceivers, which would satisfy a majority of current and future military point-to-point communications requirements. Levels 1, 2 and 4, described in Volume 1 have been designed, fabricated and tested to Mil-Qual specifications. The capabilities of these three links are described in detail in this report and provide digital transmission from 1 kbps to 50 Mbps interfacing multiple electrical levels (i.e. RS-232, Mil-Std-188-114, TTL, ECL) for maximum utility. 10 MHz analog video capability is also provided by utilizing Level 2 transceivers with peripheral modulators and demodulators. These units use LED emitters in the transmitters and pin-fet receivers which have been tested through rigorous burn-in and environmental test procedures to meet Mil-Qual for tactical Ground-Mobile environment. To fill out the MFOX family, two laser based transmitter/receiver links were fabricated to an experimental, feasibility level. These transceivers are
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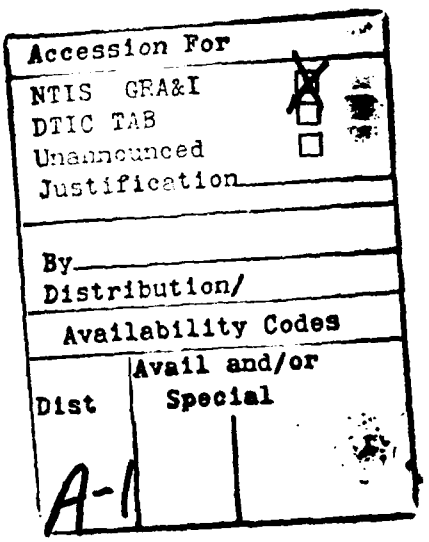
described in Volume II and provide digital transmission from 50 Mbps to 1 Gbps along with a 70 MHz IF analog interface. The 1 Gbps transceiver has been fabricated using single longitudinal mode DFB lasers and GaAs based circuitry.

Table of Contents



INTRODUCTION

This Volume contains the results of the work performed on the Experimental Development Models (EDMs) for Level 3 and Level 5 of the MFOX program. The major objective of these tasks was to develop approaches for using diode lasers in high-performance, military fiber optic systems, as upgrade elements of the MFOX transceiver family. In the course of this work, many of the technical and practical issues involved in using advanced optoelectronic and electronic components in tactical applications were addressed and solved. As a part of the approach, commercial components and chips were used in all designs. Only when commercial components were not available were custom components created. The designs are therefore well suited for transfer to engineering development as part of a next-phase development program.

The effort was highlighted by the following key accomplishments:

Level 3

- Design and development of a complete laser-based, tactical fiber-optic transceiver system at 1.3 μm.
- Digital transmission from 50 Mbit/s to 400 Mbit/s (NRZ).
- Analog transmission of a 70 MHz channel.
- Complete performance testing, including temperature testing from - 50°C to + 50°C.
- Development of laser stabilization, eliminating internal cooling.

Level 5

- Design and development of a single-mode, laser-based, fiber-optic transceiver system at 1.55 μm.
- Digital transmission from 200 Mbit/s to 1 Gbit/s (NRZ).
- Use of commercial GaAs logic circuits.
- Development of a custom, broadband pin FET receiver.
- Complete room-temperature performance testing.
- Extensive spectral characterization of single-longitudinal-mode DFB lasers.

The organization of Volume 2 is consistent with the Table of Contents of Volume 1. The two chapters of Volume 2 constitute Sections 3.3.4 and 3.3.5 of the Design Description. Reference is made to Sections 2.0 and 2.1 of Volume 1 for an overall description of the MFOX family.

Section 3.3.4

LEVEL 3 EM DESIGN DESCRIPTION

Introduction

The major objective of the Level 3 EM designs was to establish a feasible approach for using diode-laser-based transceivers to achieve higher data rates in tactical equipment. Diode laser operation over the specified temperature range is accomplished through two alternate modes of operation. One of these makes use of a thermoelectric cooler to hold the laser chip at a constant temperature despite ambient temperature excursions. The other mode eliminates the thermoelectric cooler and makes use of an optical-sensor-driven feedback circuit to maintain constant optical output despite temperature changes. This latter mode eliminates the high current drain and thermal dissipation problems of thermoelectric elements. Digital operation up to 400 Mbit/s NRZ (200 Mbit/s Manchester) approaches the performance limits of available high-speed, ECL, silicon, bipolar, digital circuits. An alternate 70-MHz analog channel for accommodating an FM carrier is also provided.

Level 3 Transmitter

The overall design configuration of the Level 3 transmitter is shown in Fig. 3.3.4-1. This block diagram indicates the major system elements: digital modulator, analog modulator, diode laser, and closed-loop optical-temperature output stabilization. The thermoelectric cooler and its closed-loop temperature stabilization system are not shown.

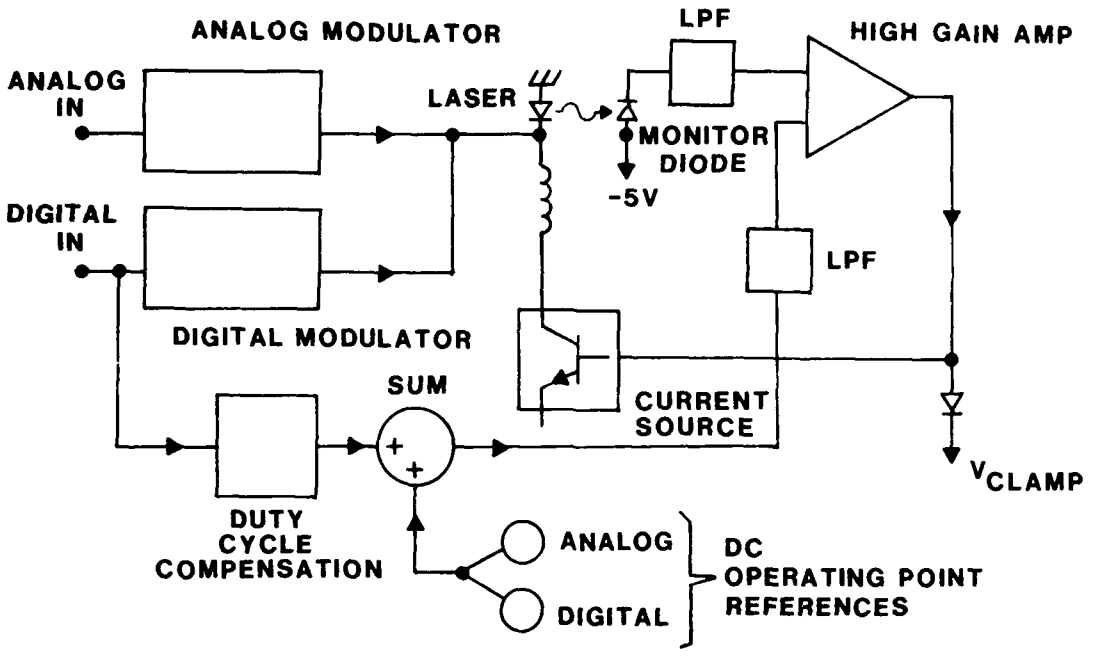


Figure 3.3.4-1. Block diagram of the Level 3 transmitter.

By the user selecting either the analog or digital signal inputs, the appropriate modulator circuits provides the high-frequency current to the laser as needed for proper laser modulation. The optical output of the laser is emitted into the fiber-optic pigtail incorporated into the laser package. Also incorporated in the package is a monitor photodiode that responds to the light emitted from the laser chip and serves as the input for the optical stabilization loop made up by the high-gain amplifier and current source. An additional duty-cycle compensation circuit senses the input digital signal and controls the operation of the feedback loop as the duty cycle changes. During initial set-up, the operating point references for both analog and digital operation are set to give appropriate optical output.

The following two figures show details of the modulator circuits. The 70-MHz analog modulator circuit is given in Fig. 3.3.4-2. Signal gain is provided by a series of ac-coupled gain stages following an input filter. An automatic gain control (AGC) loop maintains constant output amplitude and harmonic distortion levels independent of input signal level. Figure 3.3.4-3 shows the circuit for the digital modulator. This circuit uses a dual-differential, current-switching circuit based upon bipolar microwave transistors (HP5103) to drive the laser. The other

discrete transistors establish proper operating points for the switching circuit, and the ECL OR/NOR gate serves as the digital input buffer.

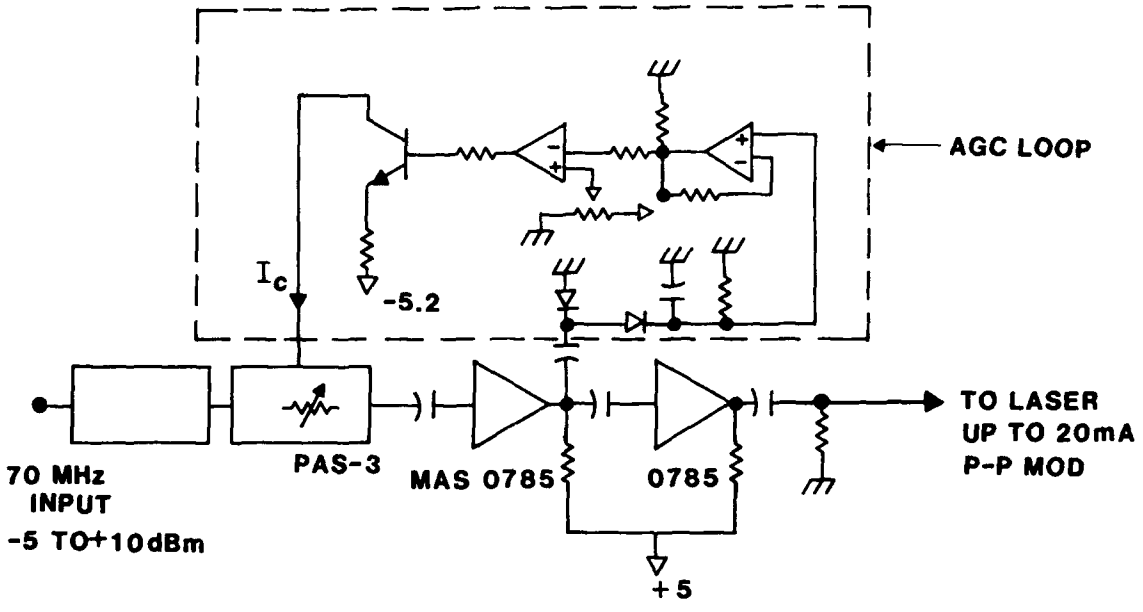


Figure 3.3.4-2. Circuit diagram of the 70 MHz modulator section of the Level 3 transmitter.

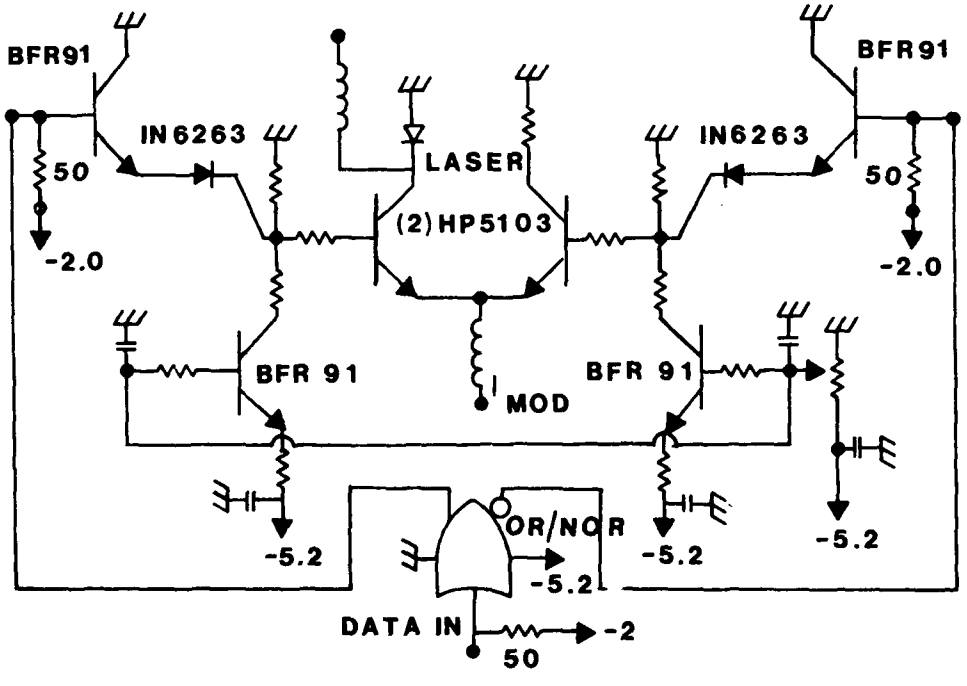


Figure 3.3.4-3. Circuit diagram of the digital modulator section of the Level 3 transmitter.

Circuitry for optical stabilization is shown in Figs. 3.3.4-4 and 3.3.4-5. The block diagram indicates the operation principles. An operating point in the absence of modulation is pre-determined for the specific laser unit at a designated temperature during the set-up of the transmitter. This bias current causes a nominal amount of light to fall on the monitor photodiode. The voltage from this photodiode is amplified and used to control the current bias source, thereby stabilizing the output of the laser. When digital modulation signals are applied, the photodiode response changes according to the modulation. If the duty cycle of the modulation is 50% (as it is for analog modulation), the average photodiode response is unchanged from the bias level, and the control loop operates as described above. Modulation that deviates from 50% duty cycle is treated with the duty-cycle conpensation network, which generates an output equal in magnitude and opposite in sign to the change in photodiode output caused by the laser modulation. This signal is also fed back into the bias current source, thereby maintaining the operating point of the laser despite digital-signal duty-cycle variations.

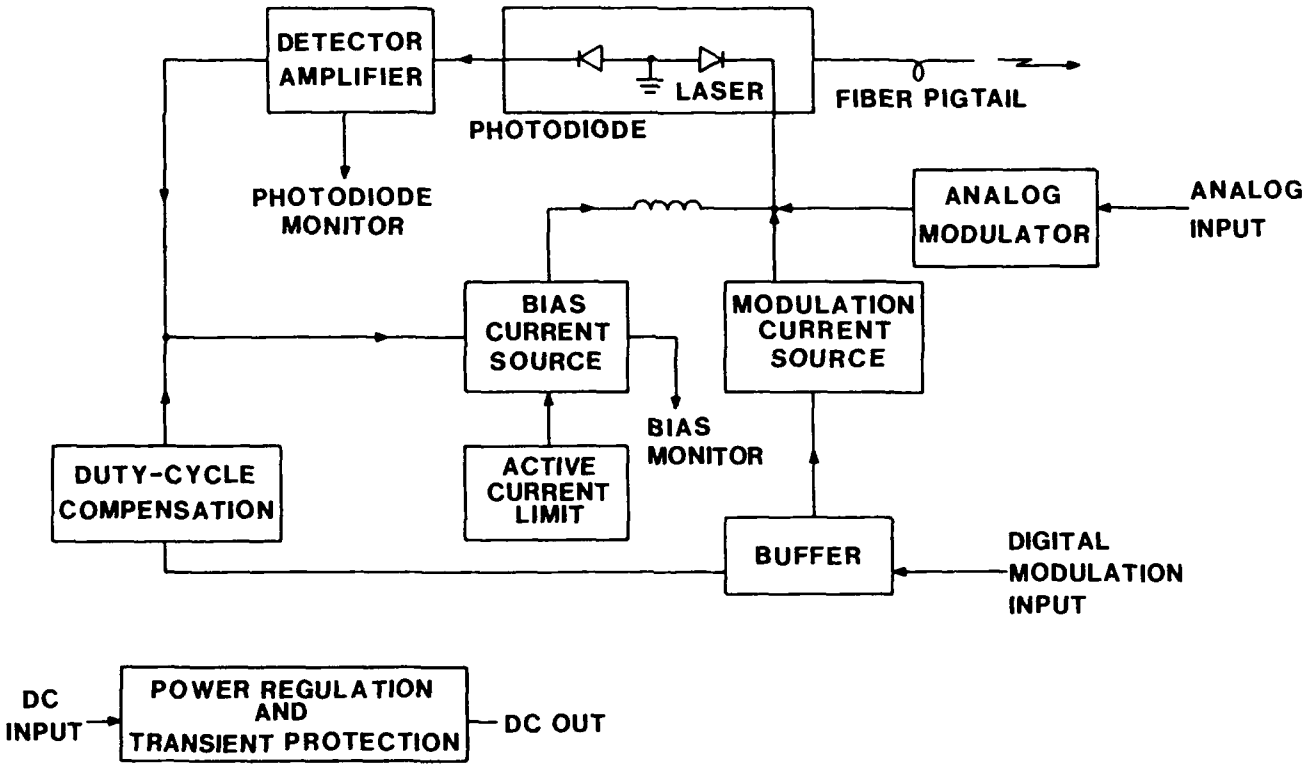


Figure 3.3.4-4. Block diagram of the feedback stabilization system for the Level 3 transmitter.

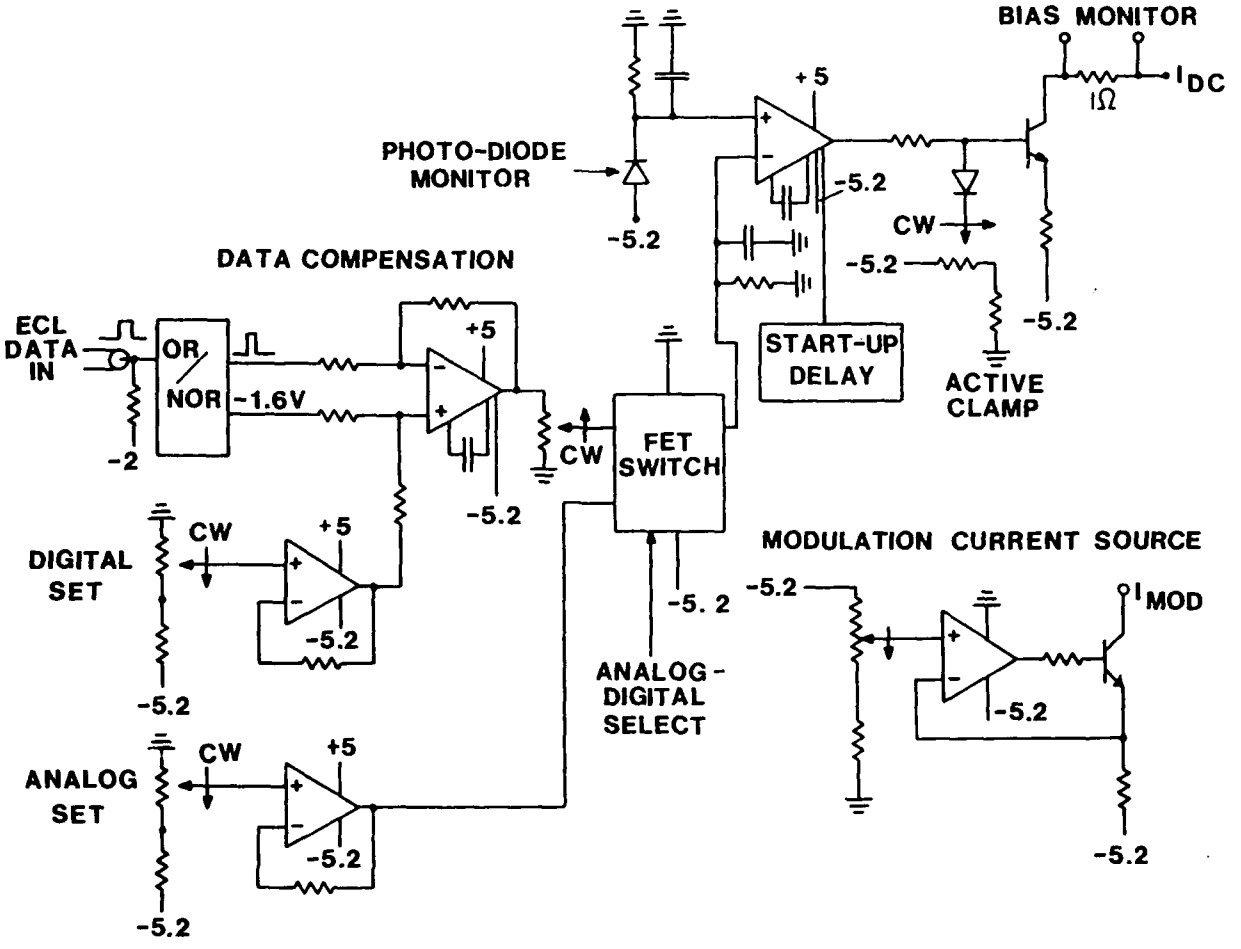


Figure 3.3.4-5. Circuit diagram of the feedback stabilization system for the Level 3 transmitter.

The performance of the Level 3 transmitter in generating digital optical signals is summarized in Fig. 3.3.4-6, which gives optical waveforms and corresponding electrical input waveforms for data rates ranging from 50 Mbit/s to 400 Mbit/s. Throughout this range the fidelity of the signals is excellent, both in pulse shape and in the absence of timing jitter. This performance is maintained as the ambient temperature is varied between -50°C and +50°C with the thermoelectric cooler disabled through action of the optical stabilization circuit. Figure 3.3.4-7 shows test results demonstrating this performance.

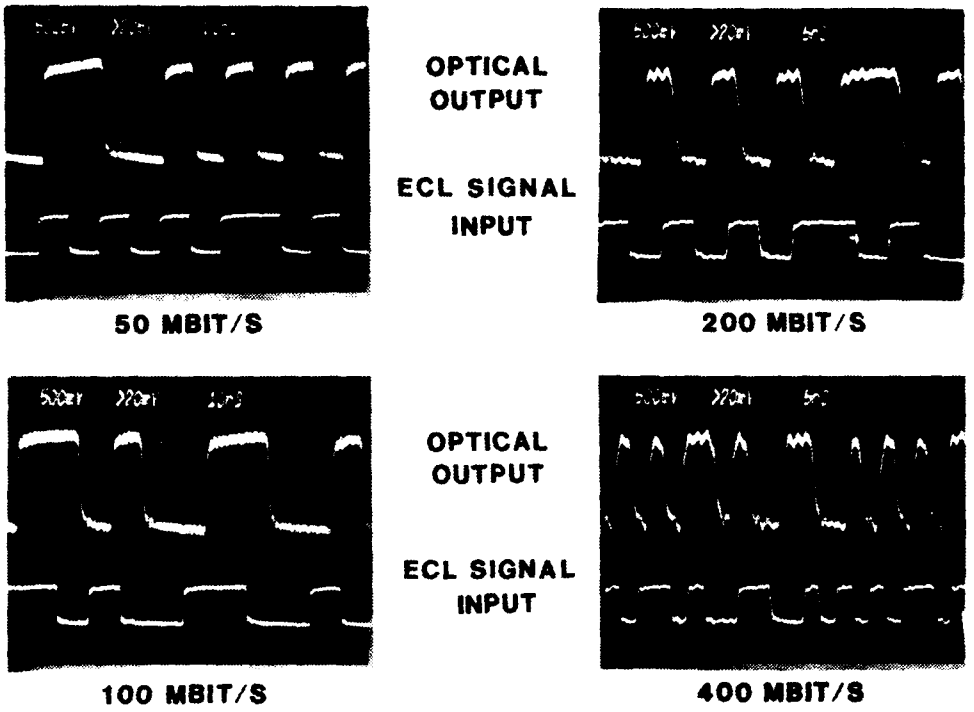


Figure 3.3.4-6. Digital waveforms of the Level 3 transmitter output.

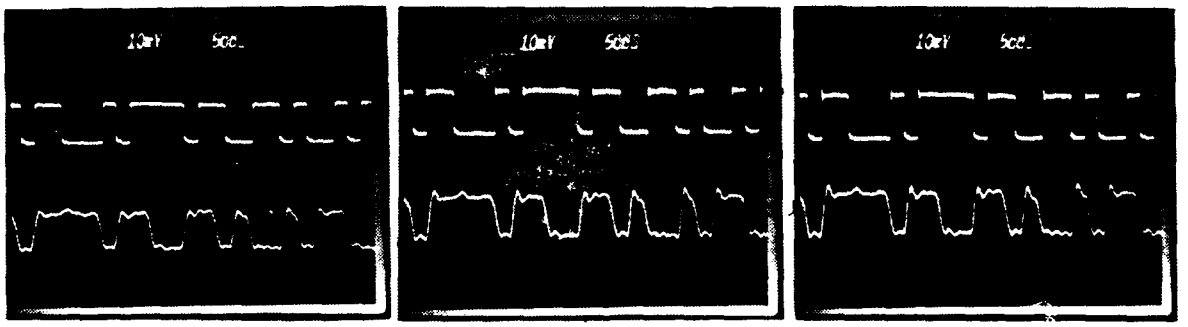


Figure 3.3.4-7. Digital performance of the Level 3 transmitter with TE cooling disabled.

Performance of the 70-MHz analog transmission channel of the Level 3 transmitter is summarized in Figs. 3.3.4-8 through 3.3.4-11. Figure 3.3.4-8 shows harmonic distortion at 60% modulation. Third-order intermodulation is 52 dB

below the carrier level, and second harmonic distortion is 42 dB below the carrier. Figure 3.3.4-9 shows the effectiveness of the AGC loop in stabilizing the output optical signal against changes in electrical input. Input variations that give 20-dB output variation with the loop disabled produce only a 1.4 dB output variation when the loop is active. Figures 3.3.4-10 and 3.3.4-11 show the analog performance as the temperature is varied between -50°C and +50°C with the thermoelectric cooler disabled. The carrier level is well stabilized by operation of the optical stabilization loop, but there is significant increase in harmonic distortion levels with decreasing temperature. Further tests showed that this increased distortion was the result of the rf amplifiers and not the optoelectronic devices.

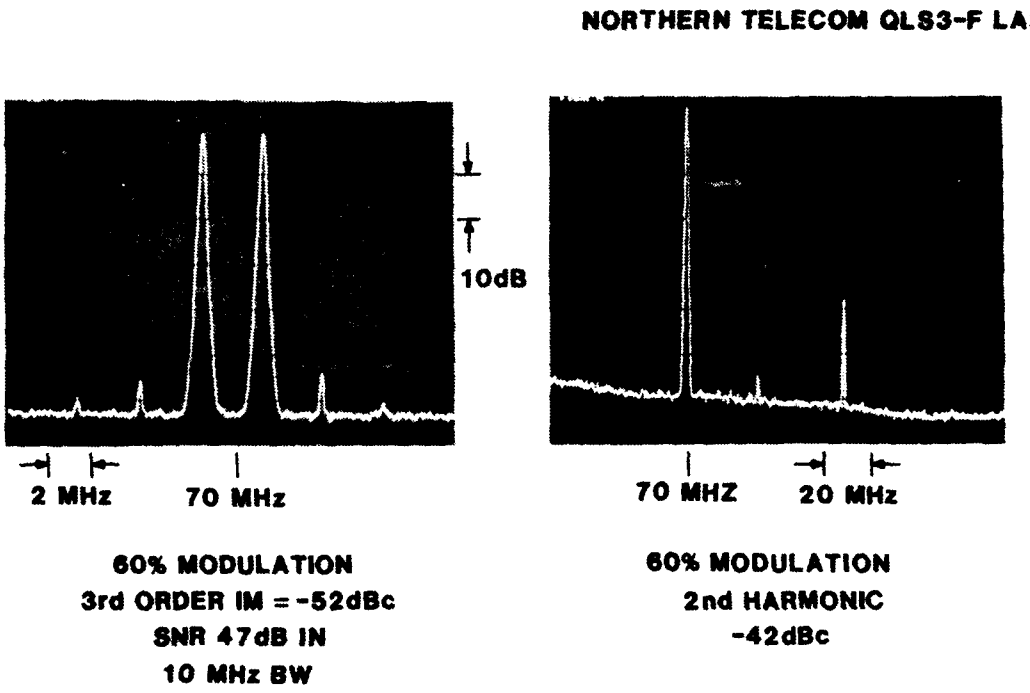


Figure 3.3.4-8. Performance of the 70 MHz analog modulator, showing 3rd order intermodulation at the operating point (60% modulation) as well as second harmonic distortion.

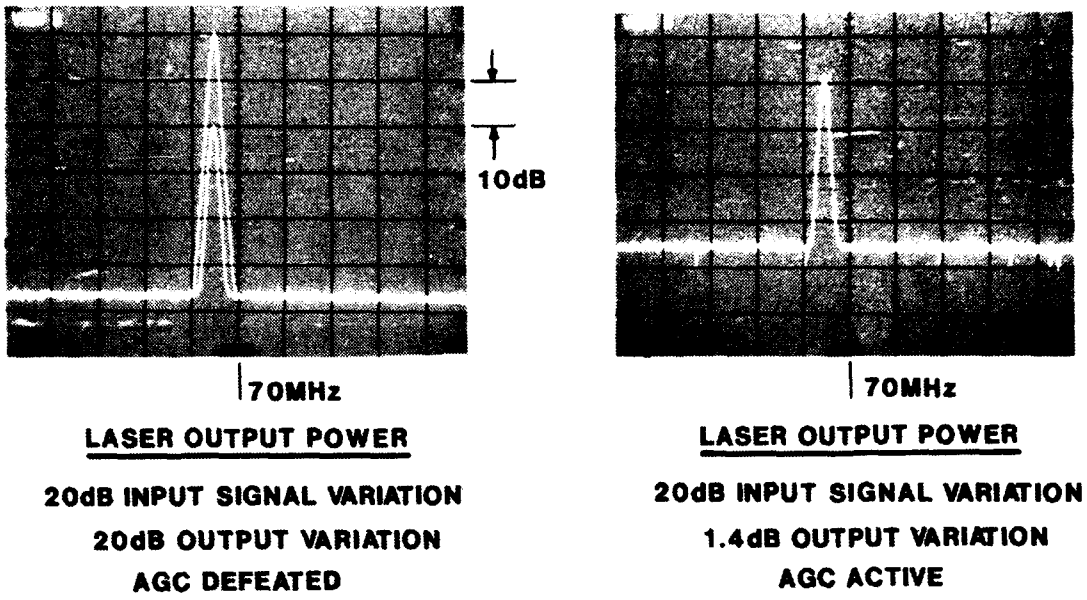


Figure 3.3.4-9. Performance of the 70 MHz analog modulator, illustrating operation of the input AGC unit.

Specific tests of the performance of the optical stabilization system are summarized in Figs. 3.3.4-12 through 3.3.4-14. Figure 3.3.4-12 shows digital optical signal levels as functions of temperature at different duty cycles. Figure 3.3.4-13 shows the monitor photodiode response (calibrated to optical power incident on the photodiode) under the same conditions. While the photodiode response is held extremely constant over temperature, there are noticeable variations in output optical signal, though not enough to seriously degrade system performance. A similar effect is seen in Fig. 3.3.4-14 for analog data. Our conclusion is that the optical coupling between the laser chip and the fiber optic changes with temperature, causing output changes to which the optical stabilization system does not respond.

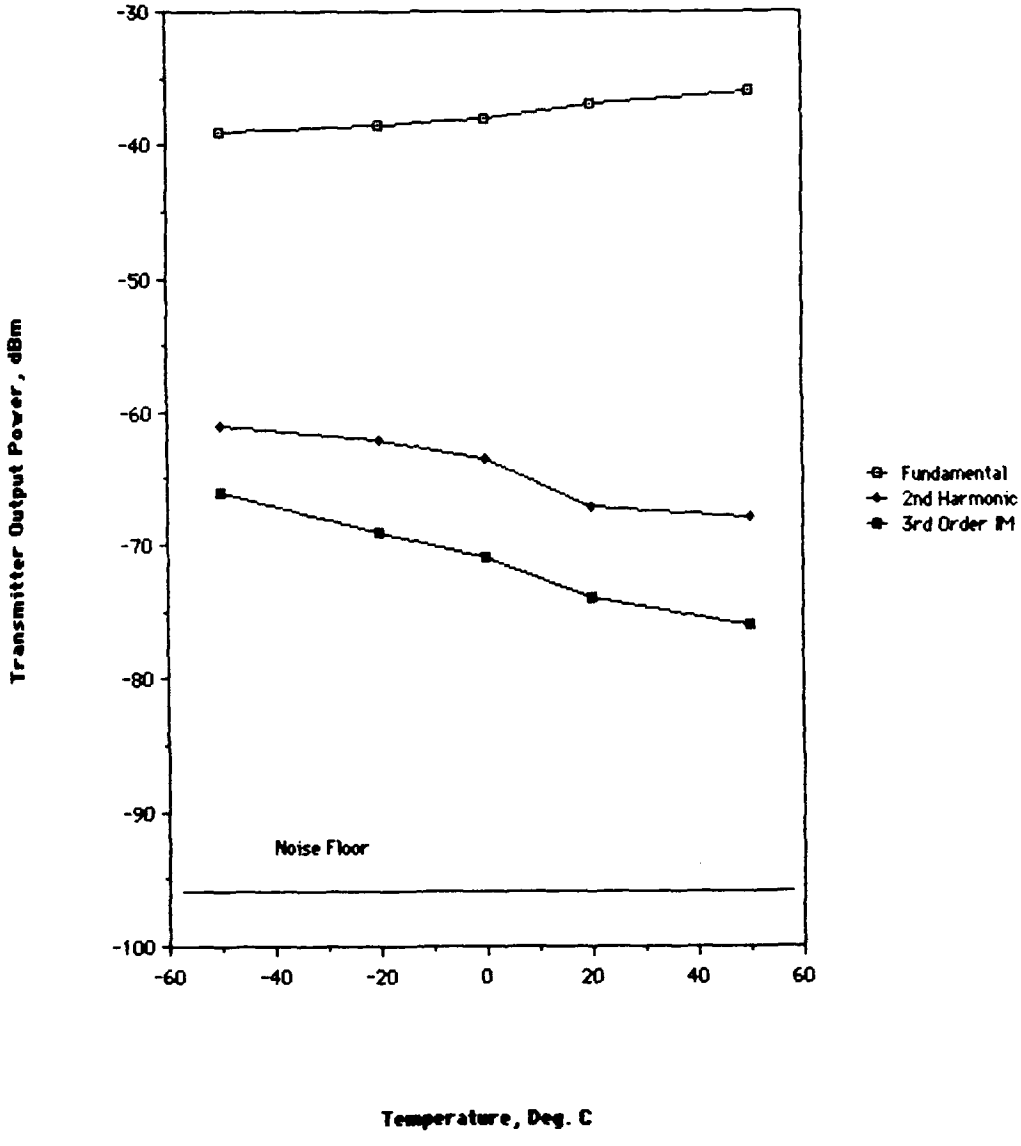


Figure 3.3.4-10. Performance of the 70 MHz analog modulator as a function of temperature with TE cooler disabled.

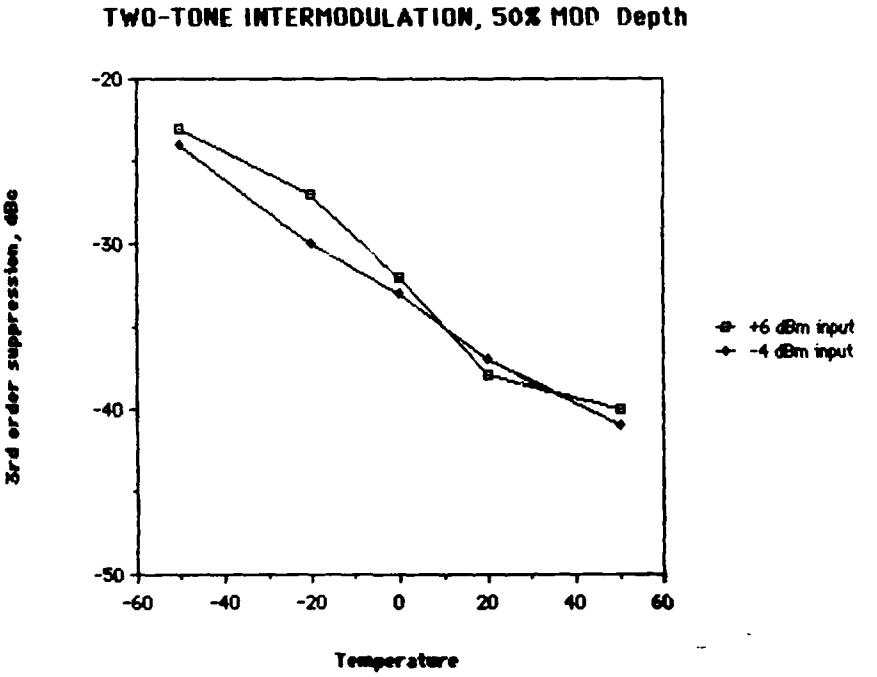


Figure 3.3.4-11. Third-order products as a function of temperature for transmitter input power levels of +6 and -4 dBm.

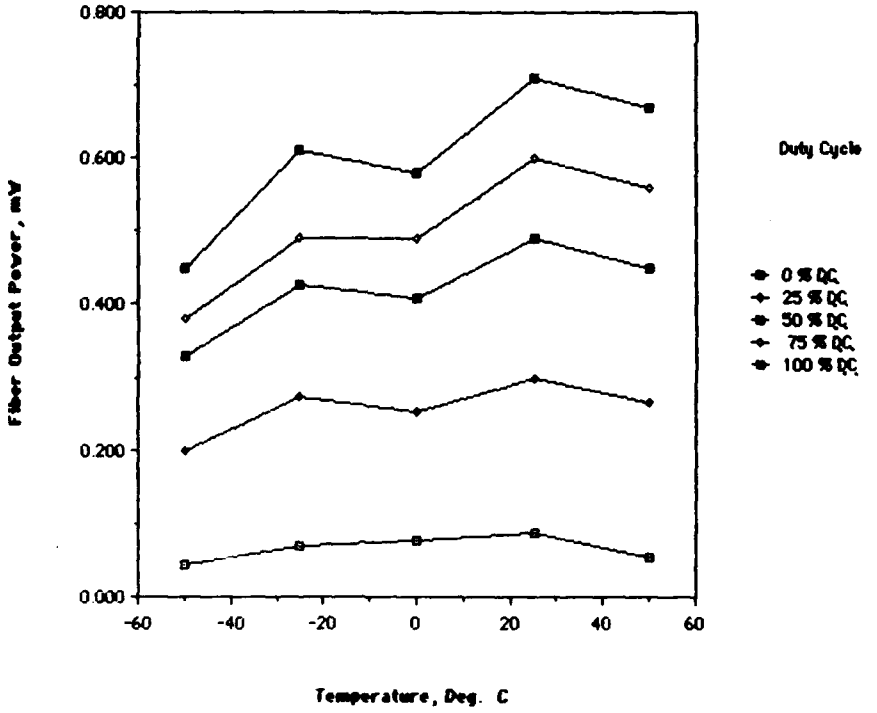


Figure 3.3.4-12. Stabilization circuit performance for the Level 3 transmitter, based on optical power at the fiber pigtail for various duty cycle values.

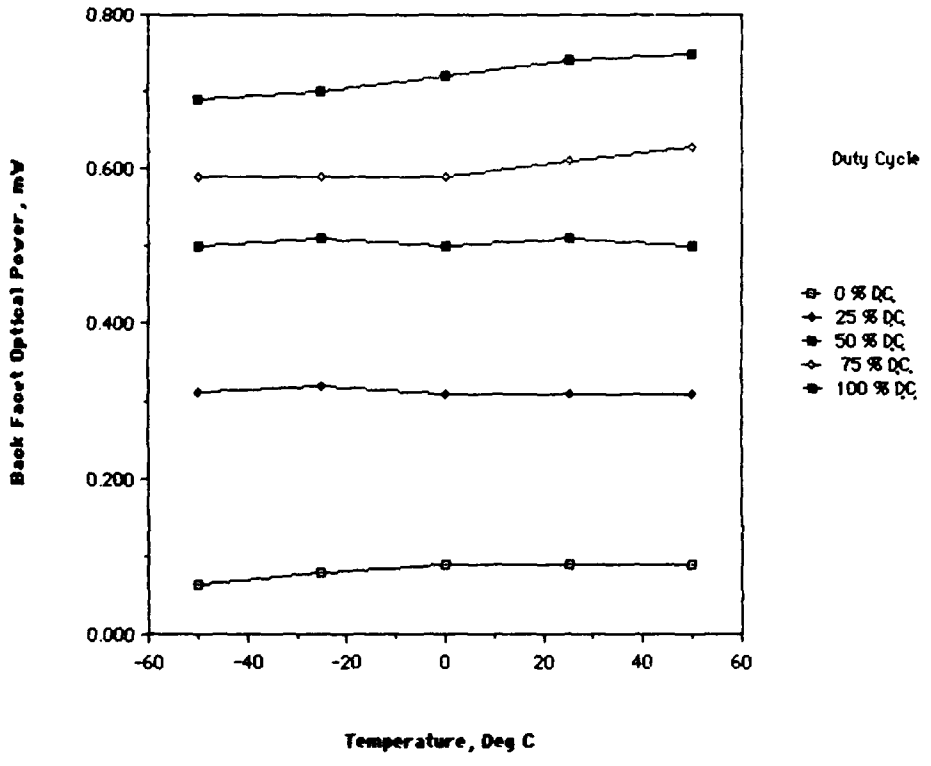


Figure 3.3.4-13. Same as 3.3.4-12, but based on back facet optical power.

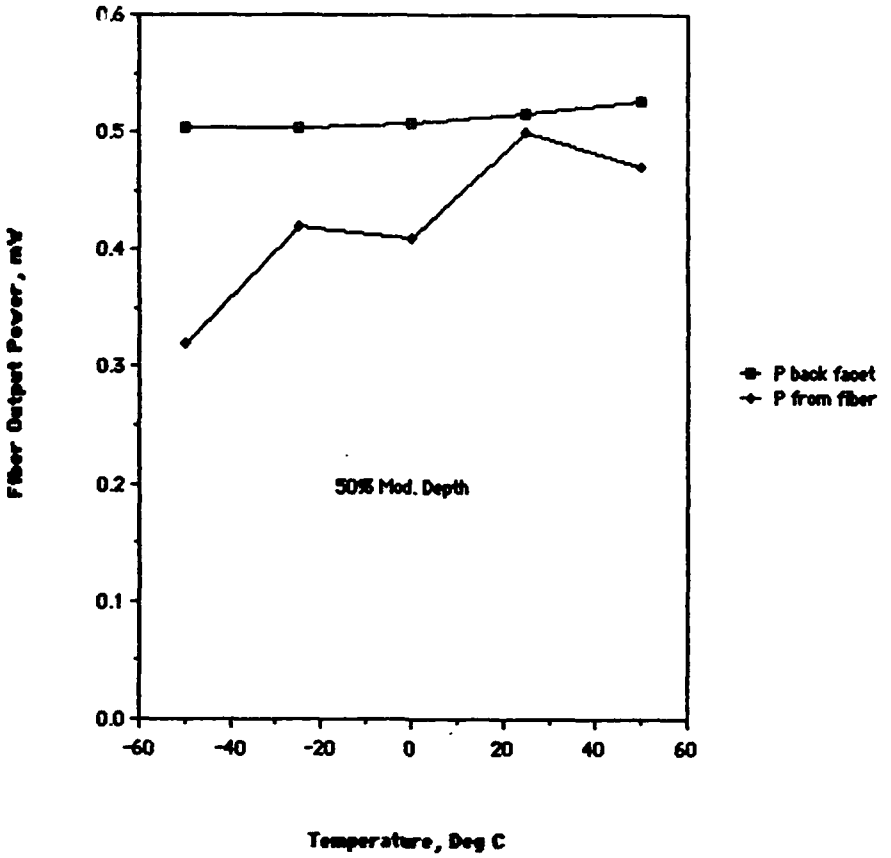


Figure 3.3.4-14. Stabilization circuit performance for the Level 3 transmitter with analog data, comparing rear facet power to power out of the fiber pigtail.

Tests were made of the sensitivity of high-speed performance to changes in negative and positive supply voltages. Figure 3.3.4-15 shows the measured rise and fall times as a function of the negative supply voltage. Significant degradation of high-frequency response is seen if the supply voltage is allowed to increase from the specified -5 V. The sensitivity to changes in the positive supply voltage (not shown) was much less critical.

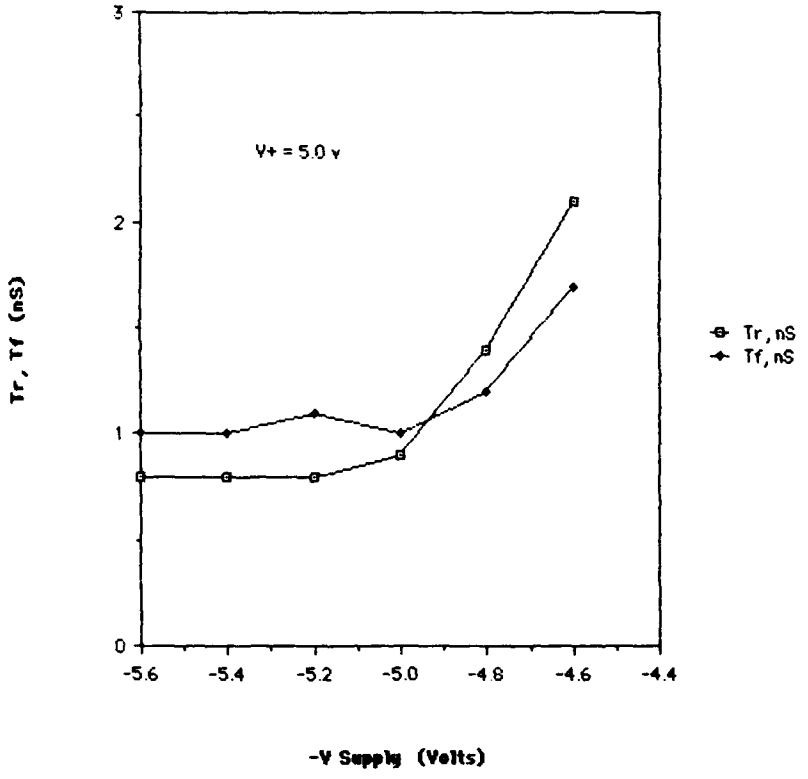


Figure 3.3.4-15. Rise and fall times of the Level 3 transmitter as functions of the -5.0-V supply value.

The electrical power consumption, a critical factor in tactical applications, is represented in Figs. 3.3.4-16 and 3.3.4-17. Figure 3.3.4-16 shows power consumption with and without the thermoelectric temperature-stabilization loop operating. Very significant reductions in power consumption are achieved at the extreme temperatures in the operational mode in which temperature stabilization is not used.

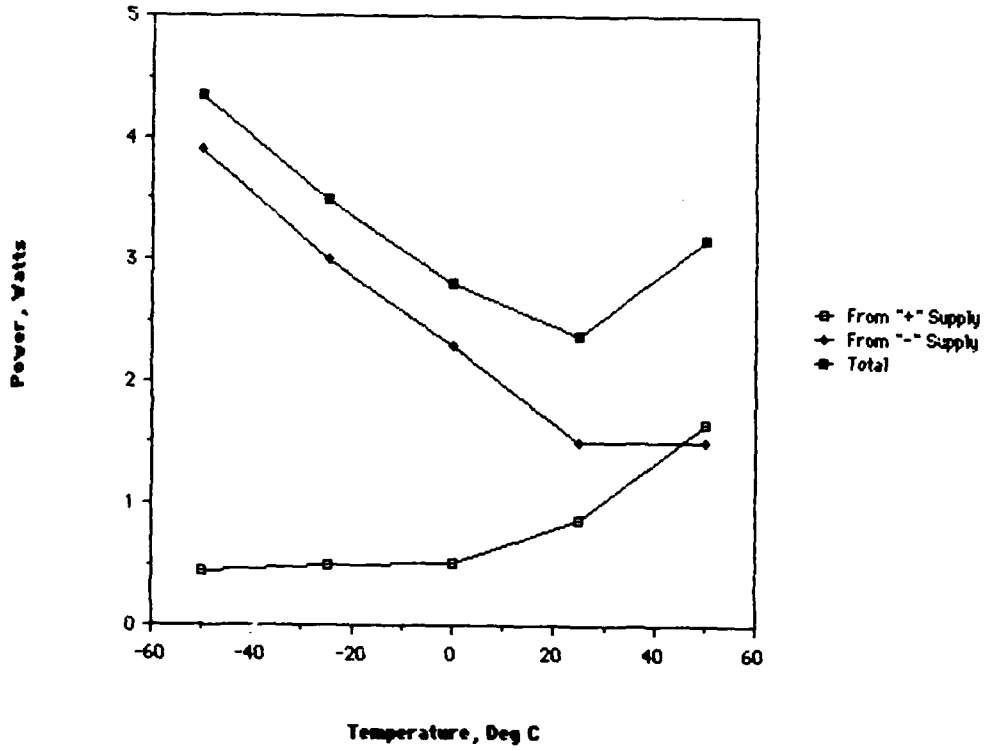


Figure 3.3.4-16. Total transmitter power consumption as a function of temperature.

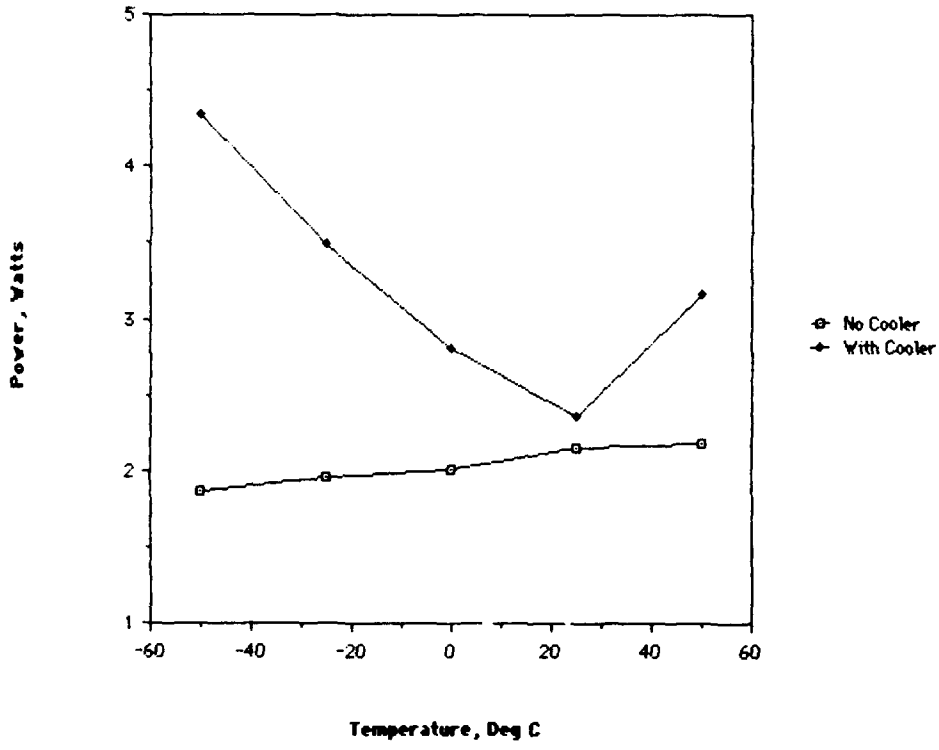


Figure 3.3.4-17. Total transmitter power consumption with and without the TE cooler operational.

Level 3 Receiver

The block diagram shown in Fig. 3.3.4-18 shows the overall design configuration of the Level 3 receiver. Both the digital and analog channels use the same pinFET receiver (a 300-MHz bandwidth version of the transimpedence component manufactured by RCA Electro-optics) followed by a buffer and a voltage-controlled attenuator. A 3-dB splitter separates the signals into the analog and digital signal paths. The analog signal path is simply a linear amplifier cascade followed by a 10-MHz bandpass filter centered at 70 MHz. The digital signal path also begins with a linear amplifier cascade, but this is controlled by an AGC loop that is fed back to the voltage controlled attenuator. The digital waveforms are converted into ECL level digital signals by a comparator that has its threshold set to track variations in the modulation duty cycle. Figure 3.3.4-19 gives the complete schematic for this circuit.

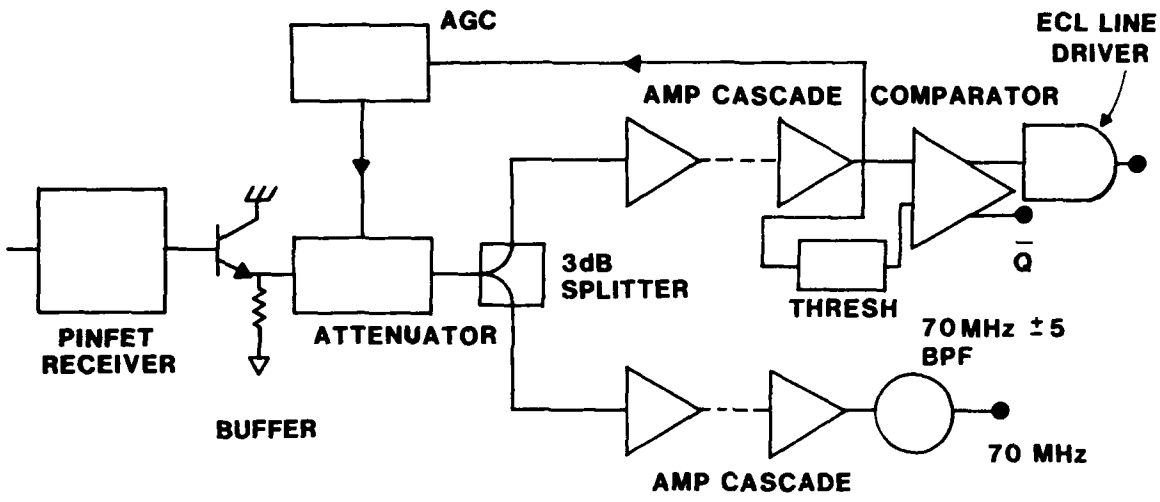


Figure 3.3.4-18. Block diagram of the Level 3 receiver.

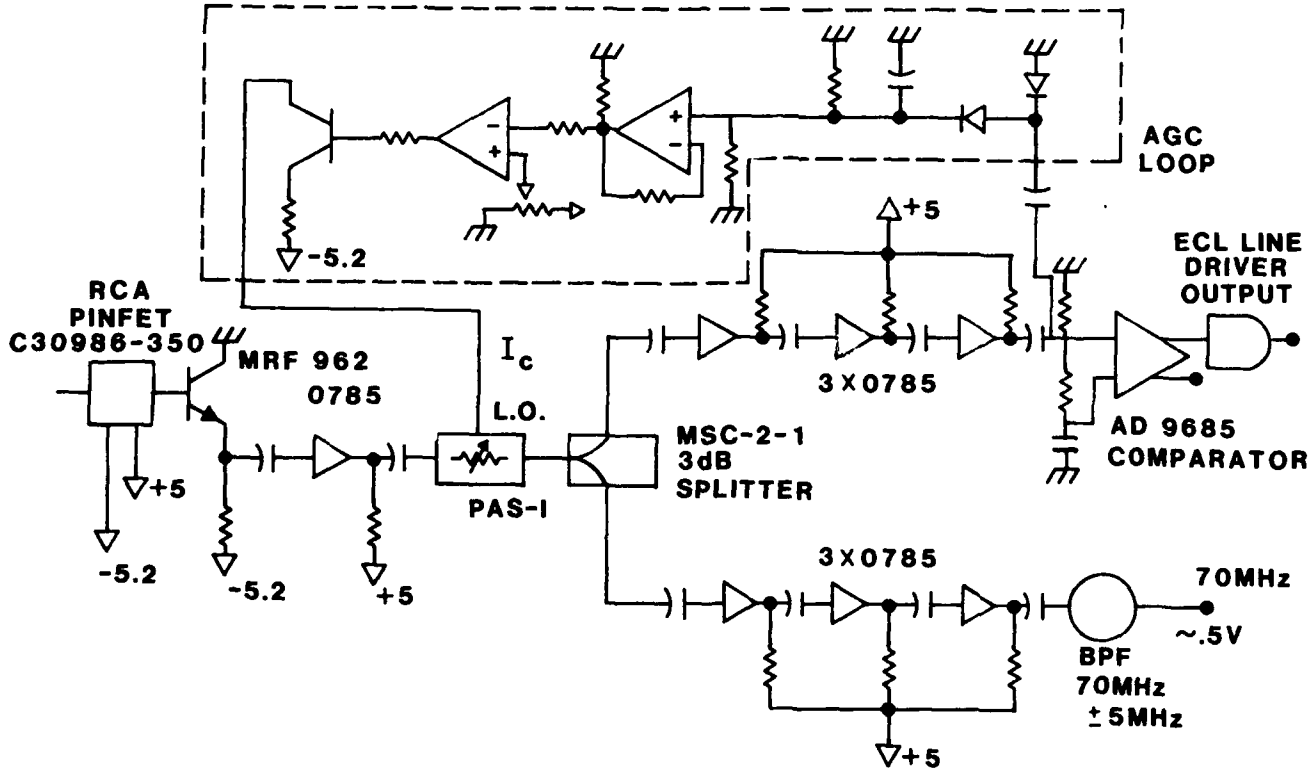


Figure 3.3.4-19. Circuit diagram of the Level 3 receiver.

Performance testing of the Level 3 receiver constitutes end-to-end characterization of the Level 3 transceiver system as well, since the Level 3

transmitter is used as the optical signal source. Since testing of the transmitter showed near-perfect signal fidelity over the specified range of digital data rates, the performance limits are set essentially by the receiver.

Figures 3.3.4-20 through 3.3.4-22 show direct characterization of the digital output waveforms. Figure 3.3.4-20 show a comparison of the output of the pinFET receiver with the digital receiver output at 200 Mbit/s Manchester. Figure 3.3.4-21 shows signal fidelity at various receiver temperatures from -50°C and +50°C. Virtually no change in signal waveform is observed. Figure 3.3.4-22 of this series shows digital eye diagrams at various data rates (with companion bit-error-rate curves).

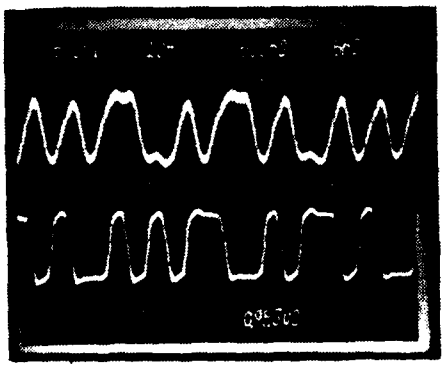


Figure 3.3.4-20. Data patterns at 200 Mbit/s, comparing pinFET output to that of the overall receiver.

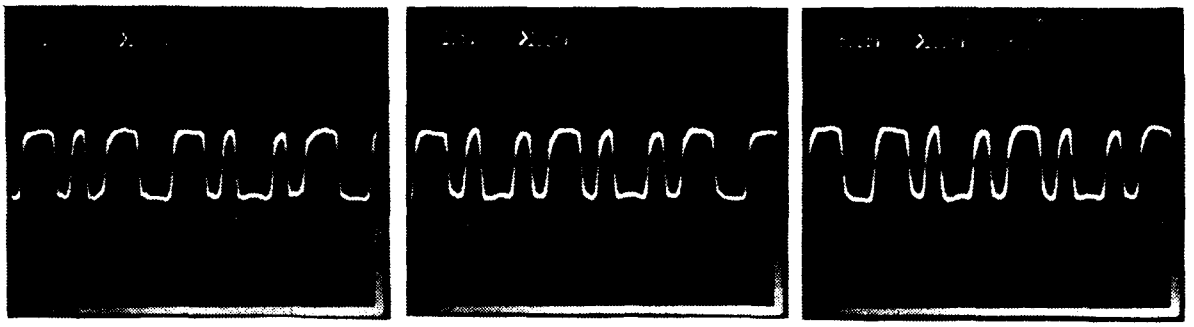


Figure 3.3.4-21. Receiver output data patterns vs temperature.

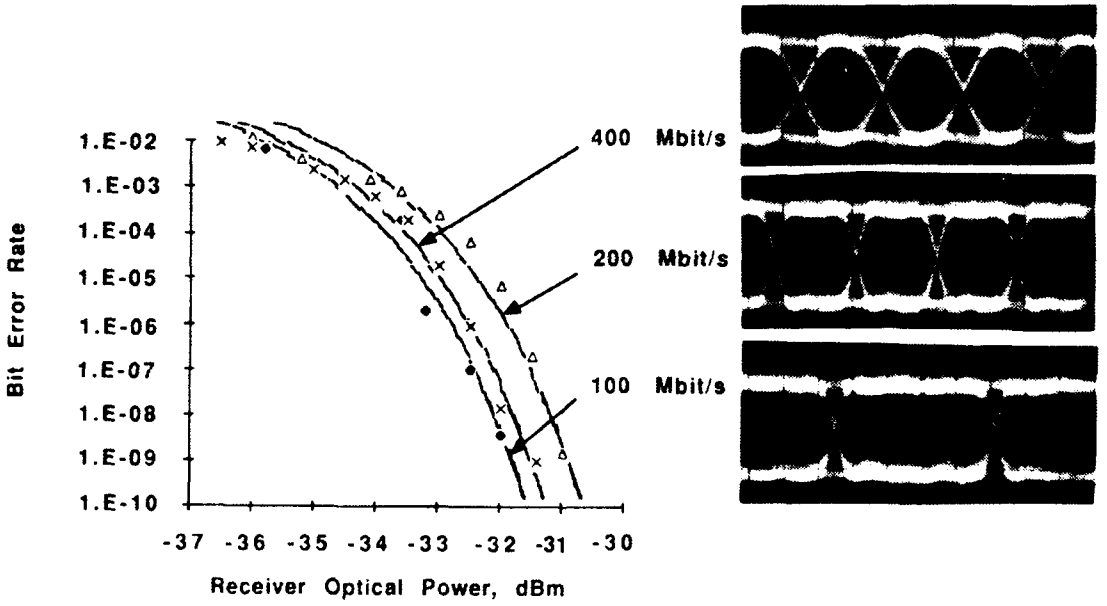


Figure 3.3.4-22. Digital eye patterns and BER measurements for 100, 200, and 400 Mbit/s NRZ data.

The overall receiver digital performance (and end-to-end system performance) is summarized in bit-error-rate (BER) measures against receiver input optical performance. This performance is shown for 50-Mbit/s and 400-Mbit/s pseudo random NRZ bit streams (PRBS) and for 200 Mbit/s Manchester

data in Figs. 3.3.4-23 through 3.3.4-25. In each case, receiver temperatures spanning the specified range are shown. Within the accuracy of measurement, these results indicate a receiver sensitivity of -31 dBm, with a variance of $\pm$1 dB at a BER of 10^{-9}.

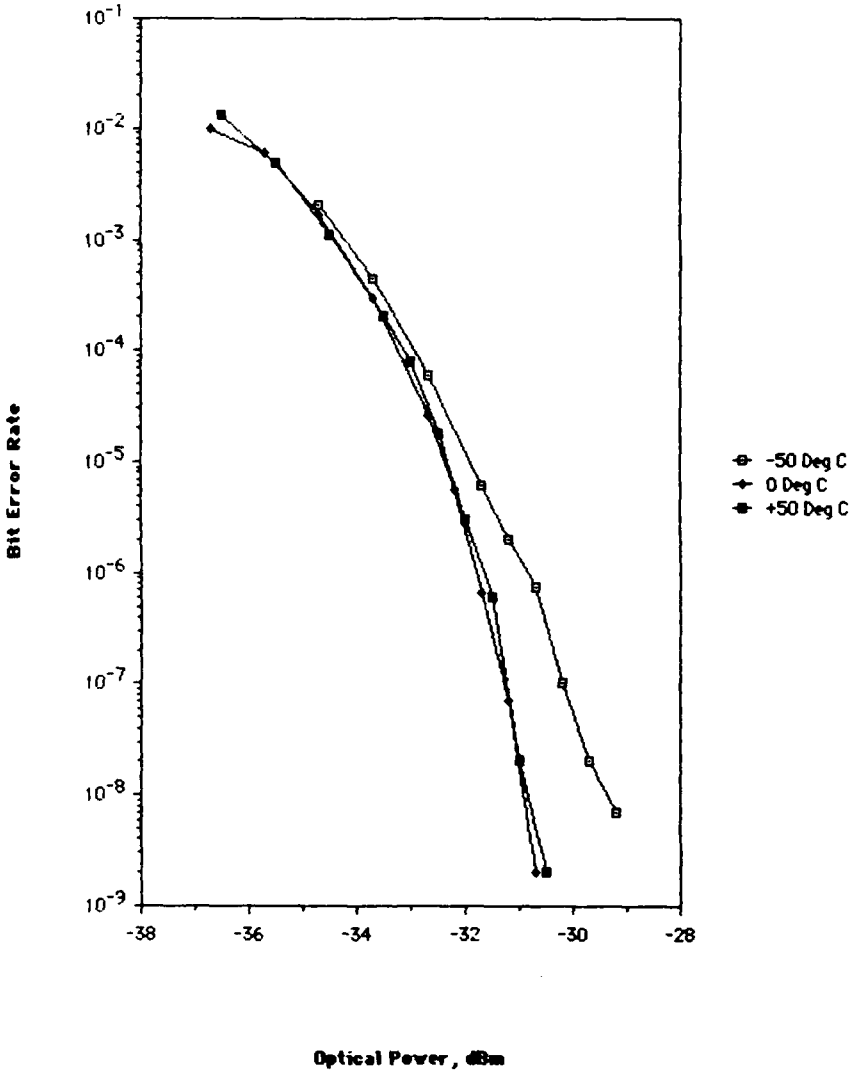


Figure 3.3.4-23. Level 3 receiver BER measurements at 50 Mbit/s PRBS vs temperature.

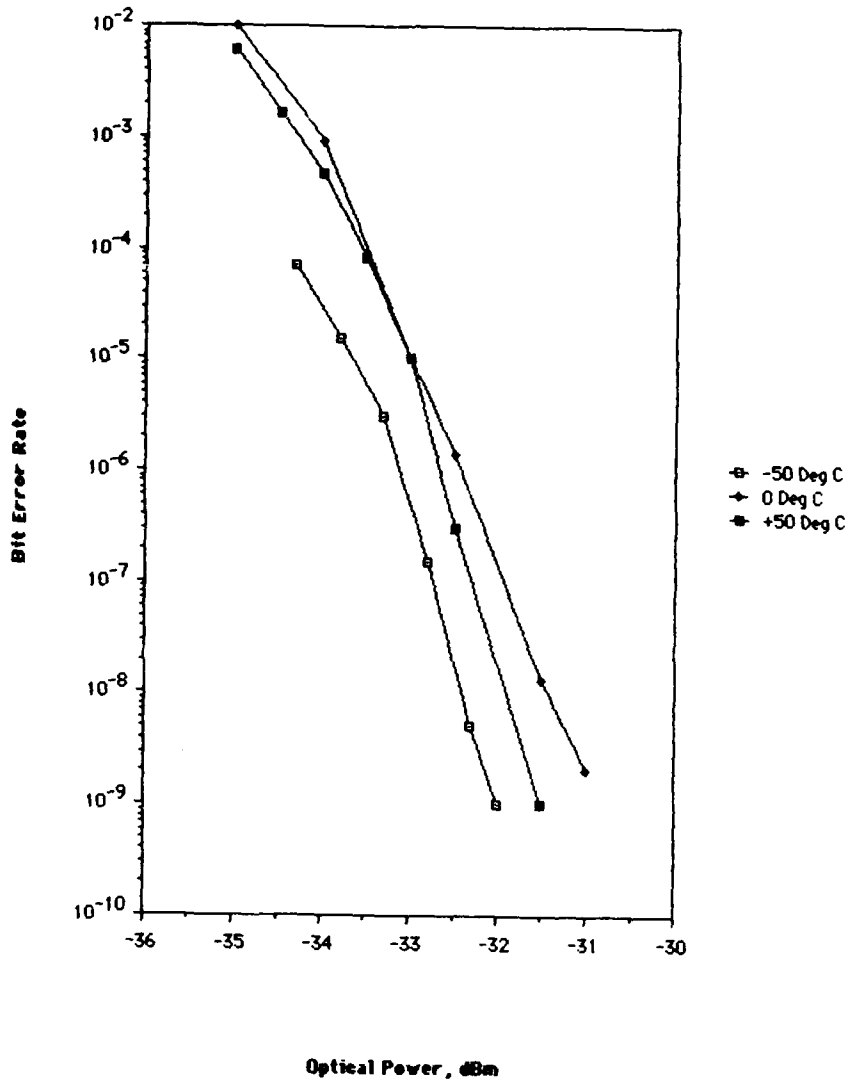


Figure 3.3.4-24. Level 3 receiver BER measurements at 400 Mbit/s PRBS vs temperature.

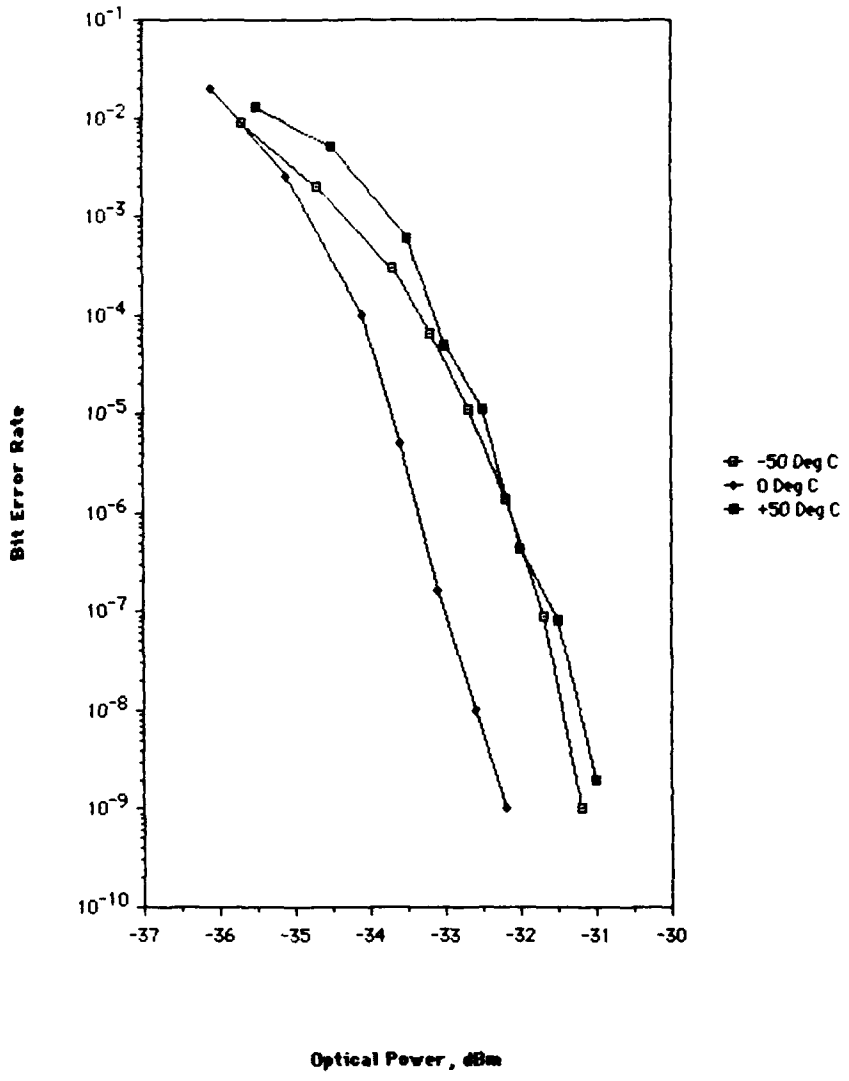


Figure 3.3.4-25. Level 3 receiver BER measurements at 200 Mbit/s Manchester vs temperature.

The dynamic range of optical signal power over which the receiver will give a specified BER was measured at 200 Mbit/s Manchester over the specified temperature range, with results given in Figs. 3.3.4-26 through 3.3.4-28. At a BER of 10^{-9} the dynamic range is measured to be within 19 to 21 dB.

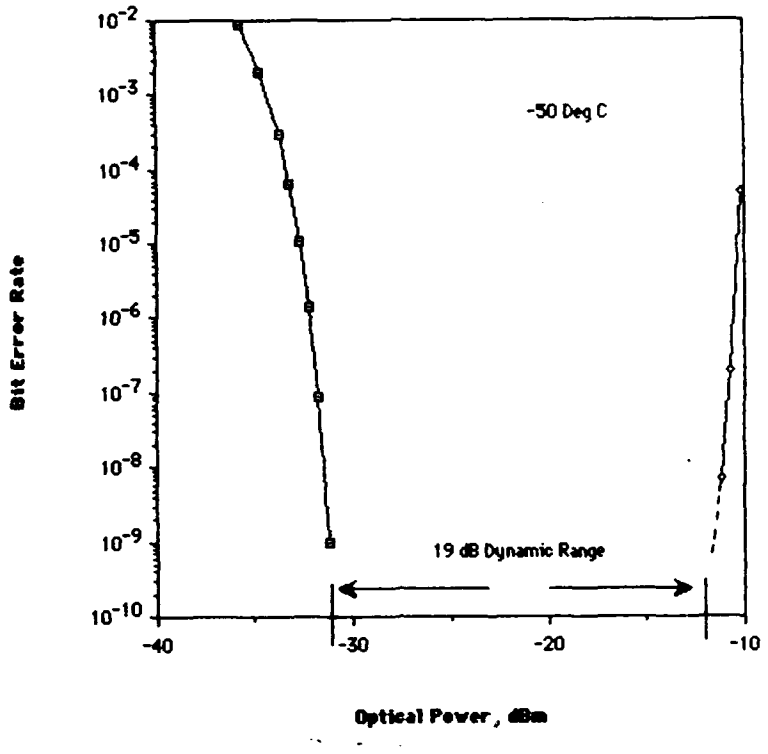


Figure 3.3.4-26. Dynamic range measurements for the Level 3 receiver, based on 200 Mbit/s Manchester data at -50 degree C.

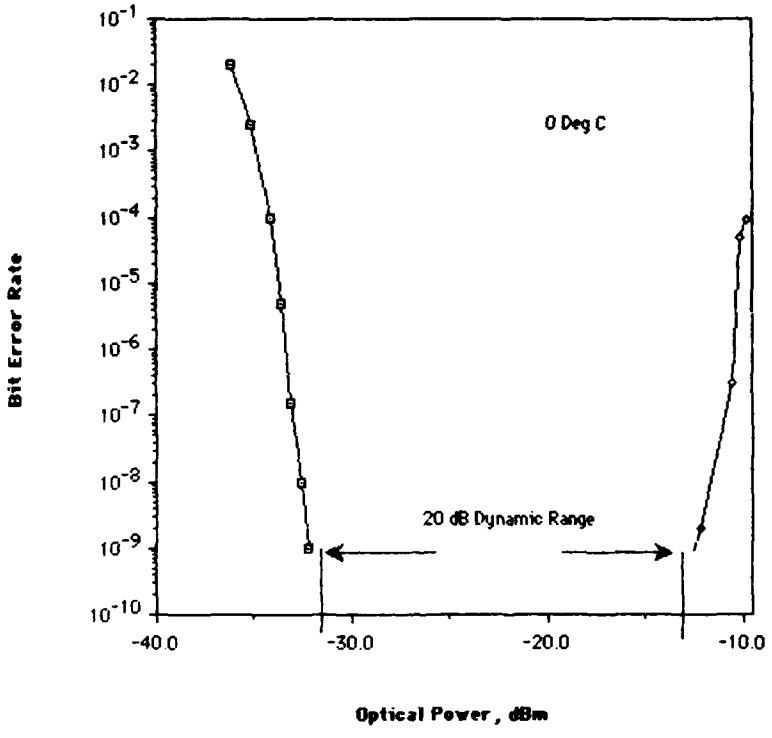


Figure 3.3.4-27. Dynamic range measurements for the Level 3 receiver, based on 200 Mbit/s Manchester data at 0 degree C.

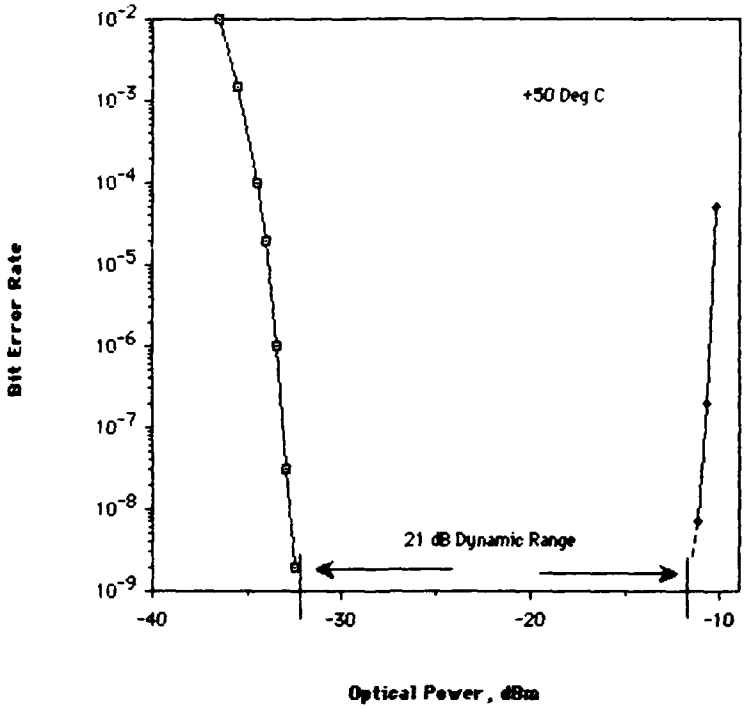


Figure 3.3.4-28. Dynamic range measurements for the Level 3 receiver, based on 200 Mbit/s Manchester data at +50 degree C.

At low data rates, the performance of the receiver becomes duty-cycle dependent. Figure 3.3.4-29 shows BER measurements at 50 Mbit/s at various duty cycles. The performance at 50% duty cycle (Manchester data) degrades as the duty cycle is reduced and becomes critical at about 35%. The receiver output for these three sequences is shown in Fig. 3.3.4-30. Timing jitter is evident at the end of the long pulse in the lowest-duty-cycle case. Droop in the ac-coupled analog signal amplifier chain is the cause of this degradation, as shown in Fig. 3.3.4-31. This effect can also be seen in the digital eye pattern taken at various receiver temperatures and data rates, as shown in Figs. 3.3.4-32 and 3.3.4-33. The 50-Mbit/s data shows increasing jitter with decreasing temperature, while the high-frequency results (400 Mbit/s PRBS) show no jitter or eye closure over the range of temperatures.

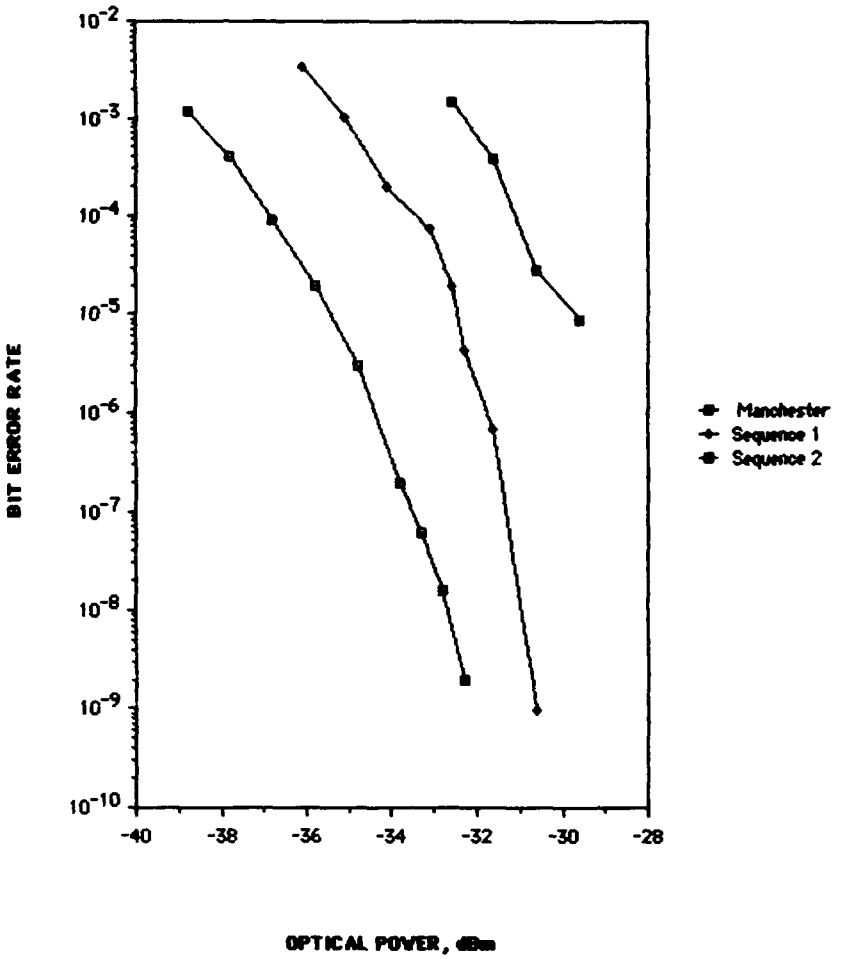


Figure 3.3.4-29. Level 3 receiver performance at low data rate (50 Mbit/s) vs duty cycle. The three data sequences correspond to Manchester (50% duty cycle), 40% duty cycle and 35% duty cycle.

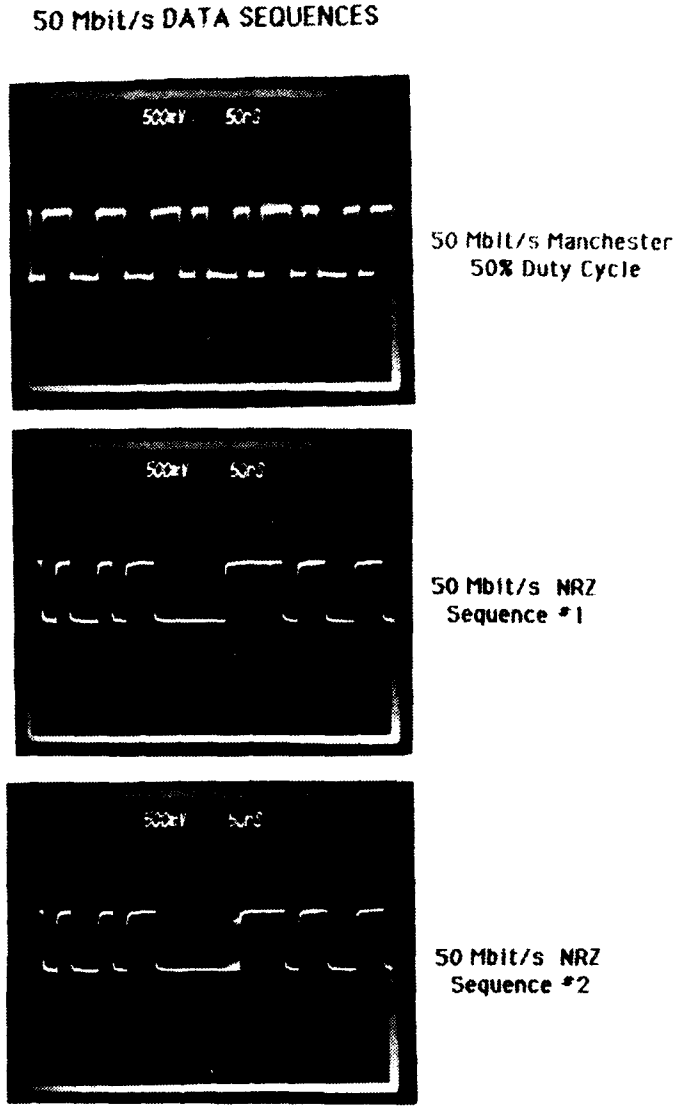


Figure 3.3.4-30. Level 3 receiver output under the conditions shown in Figure 3.3.4-29.

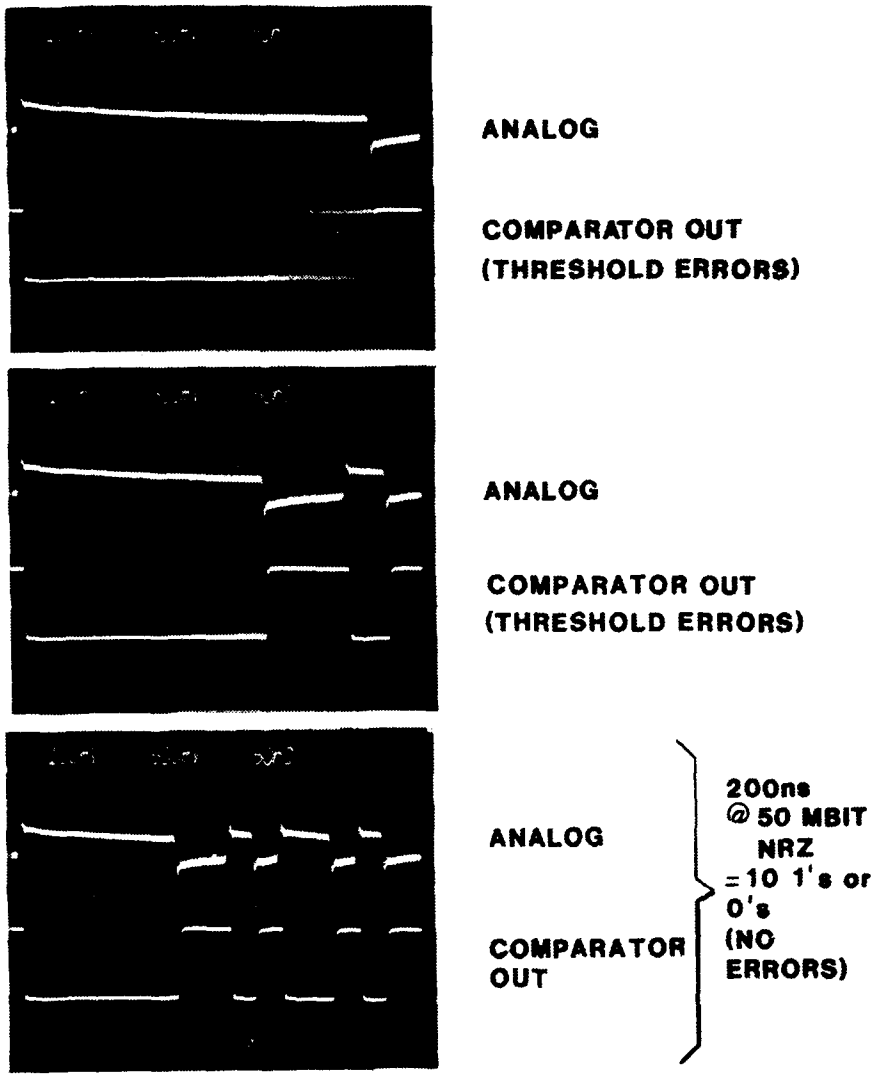
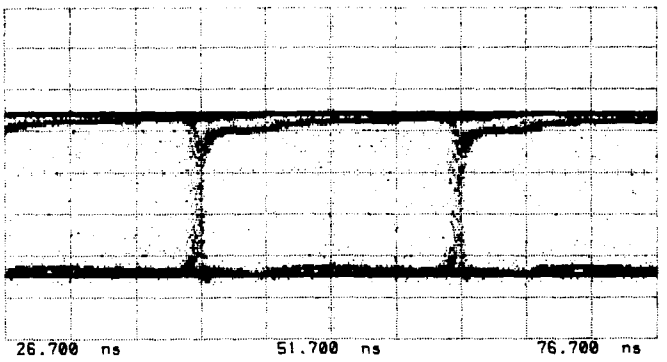
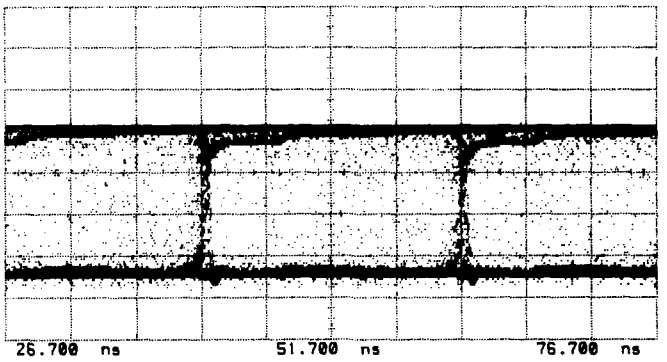


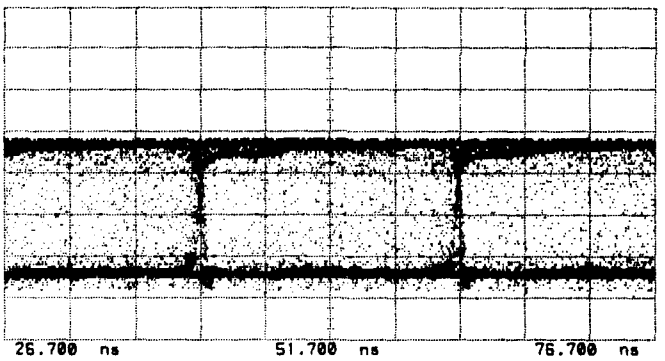
Figure 3.3.4-31. Level 3 receiver output an low data rates, illustrating droop in the analog circuitry and the corresponding threshold errors at the comparator.



+50 Deg C



0 Deg C



-50 Deg C

Figure 3.3.4-32. Eye patterns obtained through digital sampling at 50 Mbit/s PRBS for the Level 3 receiver.

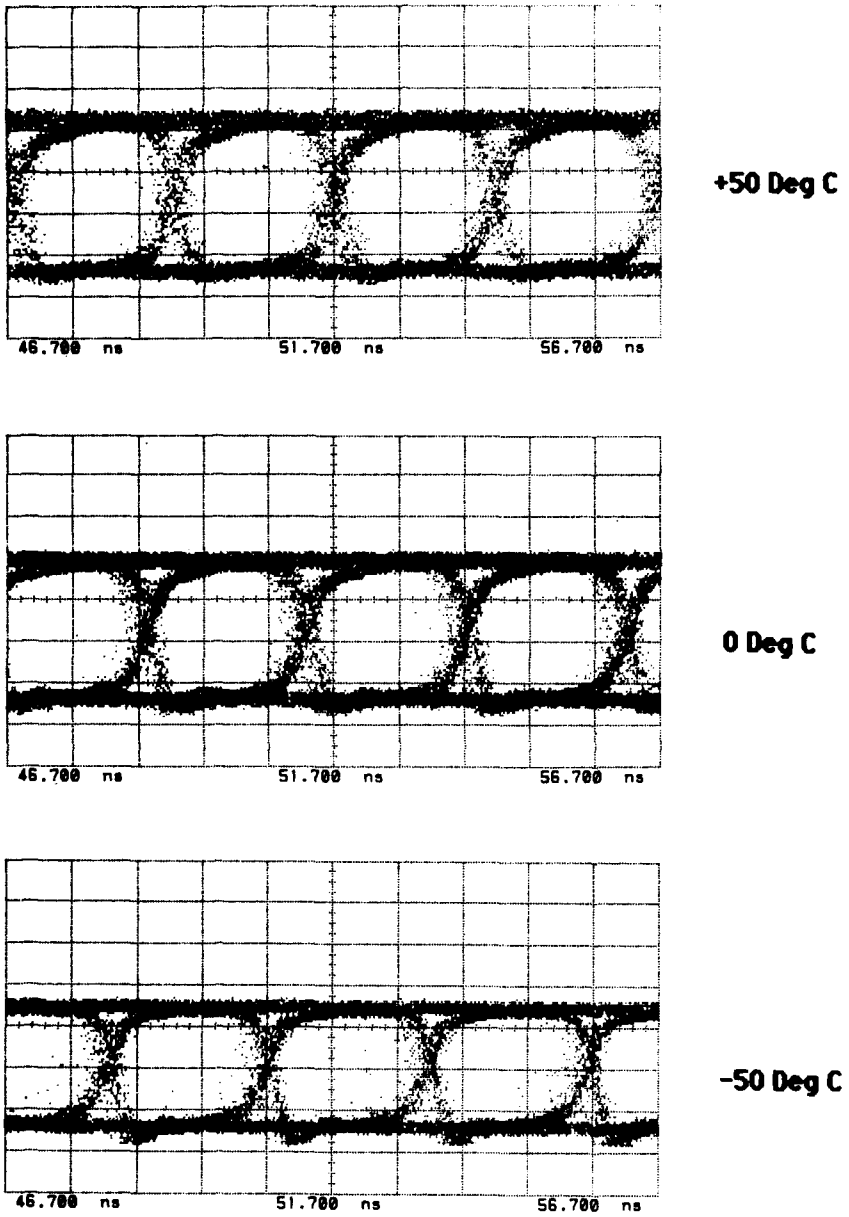


Figure 3.3.4-33. Eye patterns obtained through digital sampling at 400 Mbit/s PRBS for the Level 3 receiver.

The analog performance as a function of receiver temperature is indicated in Figures 3.3.4-34 through 3.3.4-36. Both the signal-to-noise ratio (SNR) and harmonic distortion performance degrade sharply at low temperatures. This degradation is attributed to a drop in gain of the linear amplifiers at low temperatures, seen most clearly in the drop in rms output voltage with decreasing temperature.

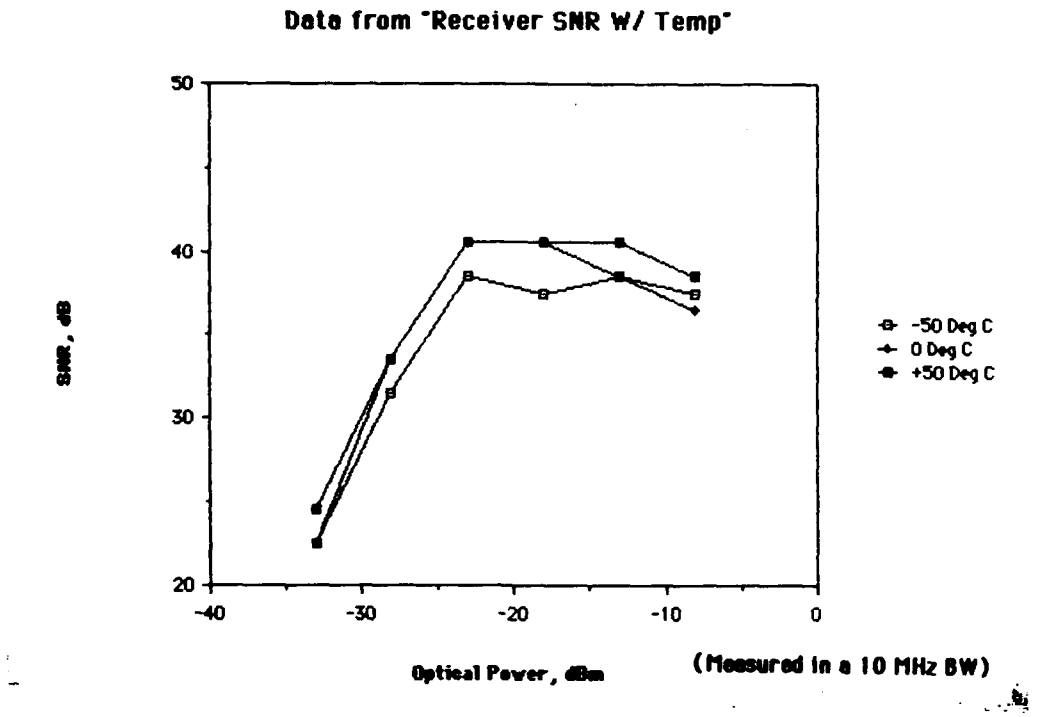


Figure 3.3.4-34. Analog Signal-to-Noise (SNR) measurements vs temperature for the Level 3 receiver.

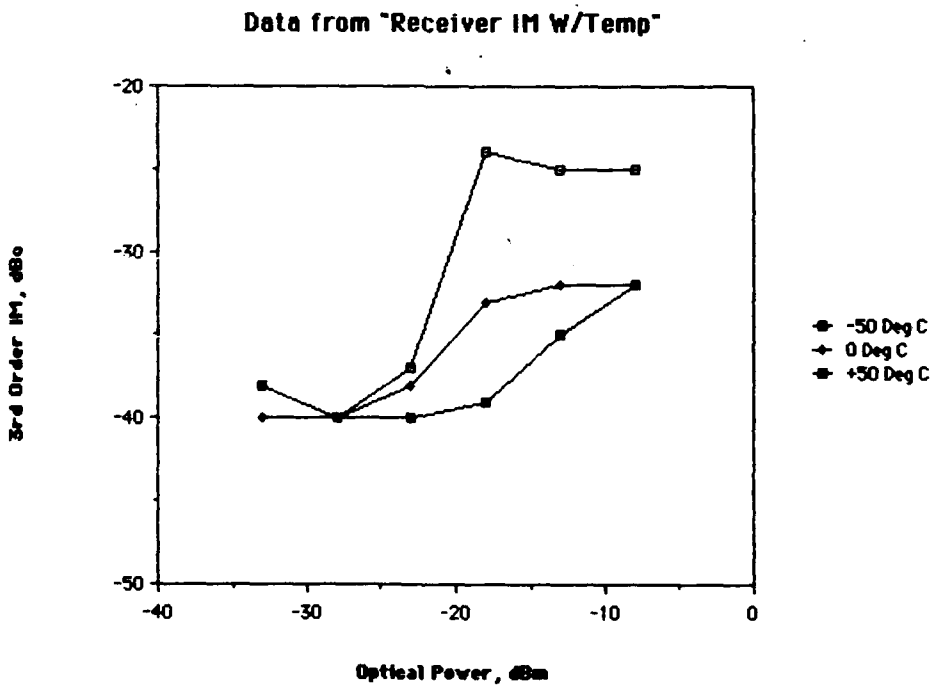


Figure 3.3.4-35. Analog 3rd order intermodulation distortion vs received optical input power at three temperatures.

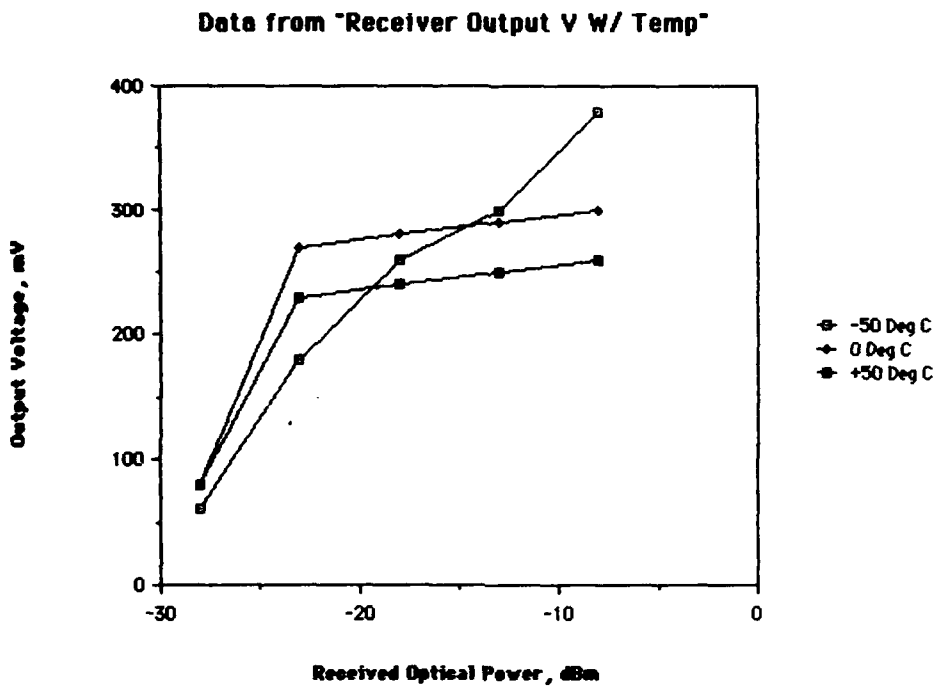


Figure 3.3.4-36. Analog rms output voltage vs input power at three temperatures.

Other operational issues were measured. The digital dynamic range was found to degrade significantly with supply voltage only when the positive supply dropped below +4.8 V from its nominal +5.2 V (Fig. 3.3.4-37). Even less sensitivity to negative supply voltage was found. The power consumption of the receiver as a function of temperature is given in Fig. 3.3.4-38. The drop in power consumption presumably corresponds to the drop in amplifier gain that is seen in the digital and analog performance at reduced temperatures.

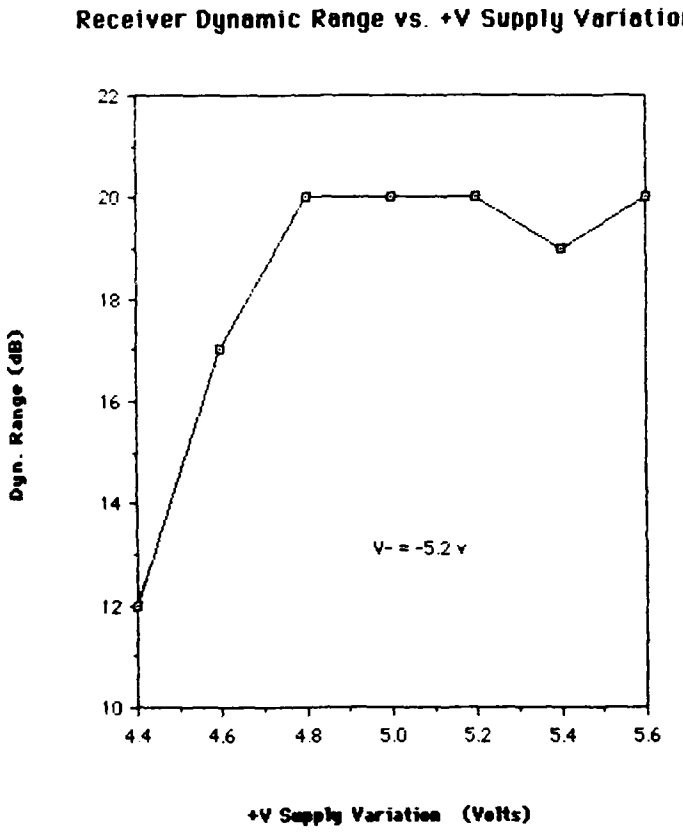


Figure 3.3.4-37. Level 3 receiver dynamic range as a function of +5 volt supply variations.

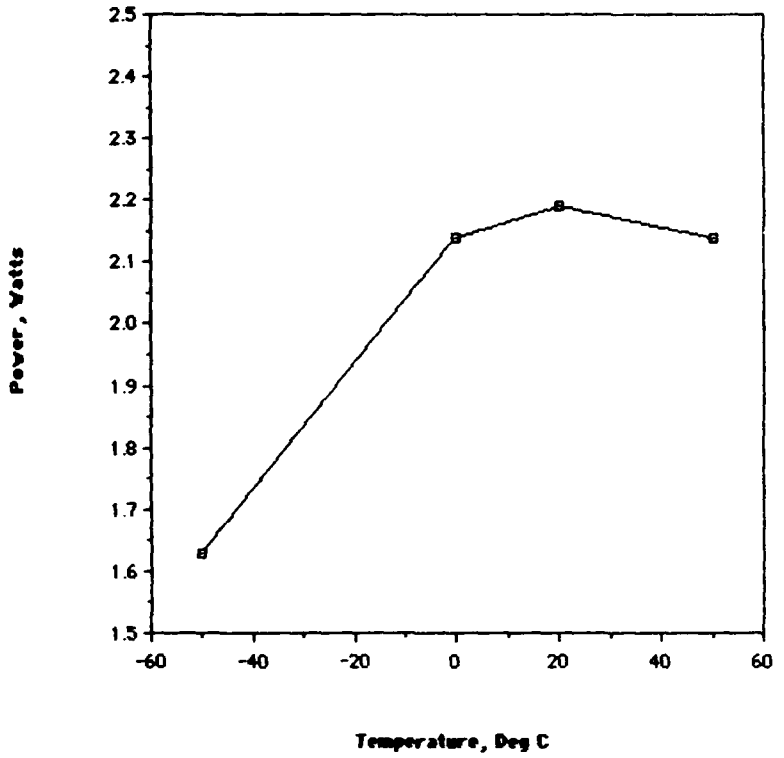


Figure 3.3.4-38. Level 3 receiver power consumption vs temperature.

Conclusions

All the requirements for the MFOX Level 3 transceivers were achieved in the work reported. The major conclusion of the effort is that high-performance, tactical military fiber-optic systems based on laser diode devices and operating at rates of 400 Mbit/s (NRZ) can be constructed using commercially available optoelectronic components and silicon digital circuits. Operation over the range of temperatures anticipated in tactical service (-50 to +50°C.), with minimal performance effects was demonstrated. Analog and digital channels were incorporated in the same unit with no performance interaction. The designs have been shown through testing to be insensitive to duty-cycle and digital data rates over the specified range, and are well suited for service in a general purpose off-the-shelf unit as part of the MFOX family.

Particular attention was paid to the matter of laser operation over wide temperature ranges. Conventionally, thermoelectric coolers incorporated in the laser package are used to stabilize the temperature of the laser chip. Since these thermoelectric units draw substantial current and represent a serious thermal

load themselves, their elimination would be an important attribute to tactical equipment. Using specially developed stabilization circuitry, operation without temperature stabilization and minimal variation in output power or waveform was demonstrated over the entire temperature range. The transmitter design allows cooled or uncooled operation as a user option.

The designs presented here are well suited for further engineering development by fabrication in a miniaturized hybrid circuit approach. Issues of optoelectronic device reliability would be appropriately addressed in this phase. Since the present design is based on the use of appropriately tested MIL QUAL parts, no significant redesign work is anticipated.

Section 3.3.5

LEVEL 5 EM DESIGN DESCRIPTION

Introduction

Level 5 EM transceivers were developed to demonstrate the maximum performance capabilities for units based on the most advanced optoelectronic and electronic devices available. Data rates exceeding 1 Gbit/s are achieved using GaAs digital integrated circuits and discrete FET devices. Optoelectronic performance commensurate with these speeds is accomplished with 1.55-μm, single-longitudinal-mode diode lasers in high-frequency packages. The only noncommercial component is the receiver pinFET detector/preamplifier, which was not available commercially and was therefore developed as a custom hybrid component for the MFOX program.

Level 5 Transmitter

The Level 5 transmitter makes use of advanced GaAs logic as well as high-current, discrete GaAs transistors. Figure 3.3.5-1 shows the block diagram of the transmitter. The digital input is formed by the GaAs comparator chip (Gigibit Logic 10GO12A GaAs). This chip directly drives the differential pair circuit that modulates the laser. To accommodate potential high current lasers and to make the design insensitive to the particular characteristics of the laser used, this circuit uses high-current, discrete GaAs FET power devices (NEC 800199). Figure 3.3.5-2 shows the complete circuit for the transmitter.

The diode laser used in the transmitter is a single-longitudinal-mode, distributed-feedback device (Lasertron QLM-1550M-DFB) operating at 1.55-μm emission wavelength. Because of its narrow spectral output, it is capable of long-range transmission over low-loss fiber at this wavelength, far from the dispersion minimum at approximately 1.3 μm. Figure 3.3.5-3 shows the spectrum of this device at 25°C. for operation at various modulation conditions (250, 500, and 1000 GHz at 95 depth of modulation) as well as unmodulated. The single-mode characteristic of the device is maintained under these conditions.

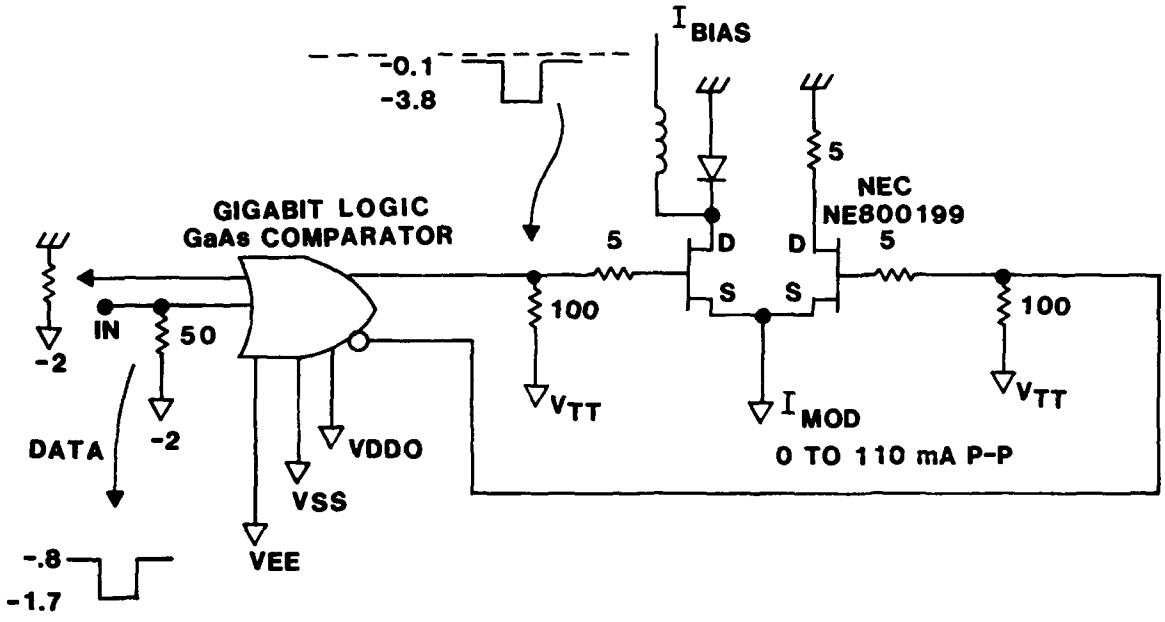


Figure 3.3.5-1 Block diagram of GaAs FET laser driver. Gigabit Logic 10G012A GaAs comparator IC receiver ECL level input data and drives differential pair of NEC 800199 power GaAs FET transistors.

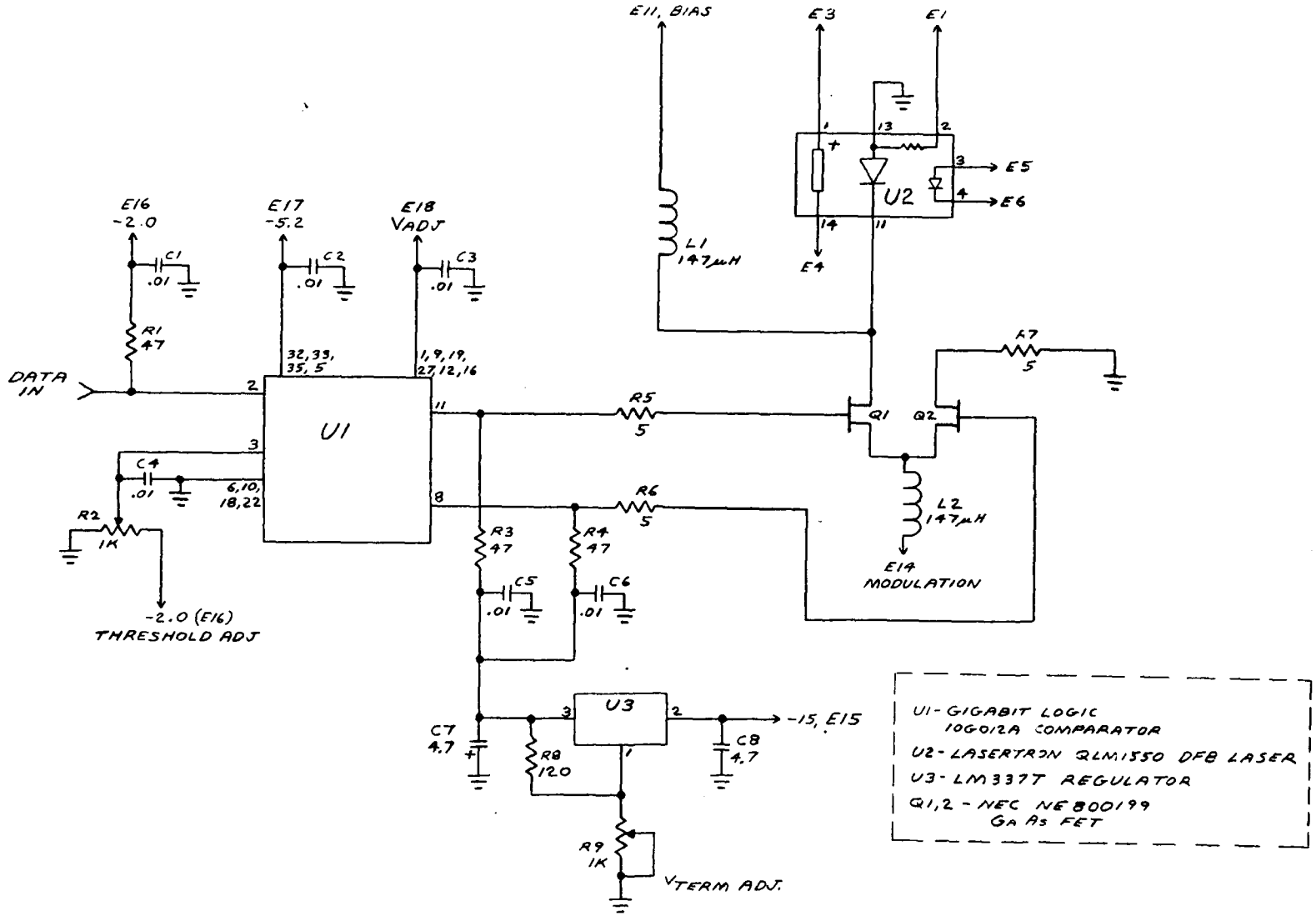


Figure 3.3.5-2 Schematic diagram of transmitter modulator.

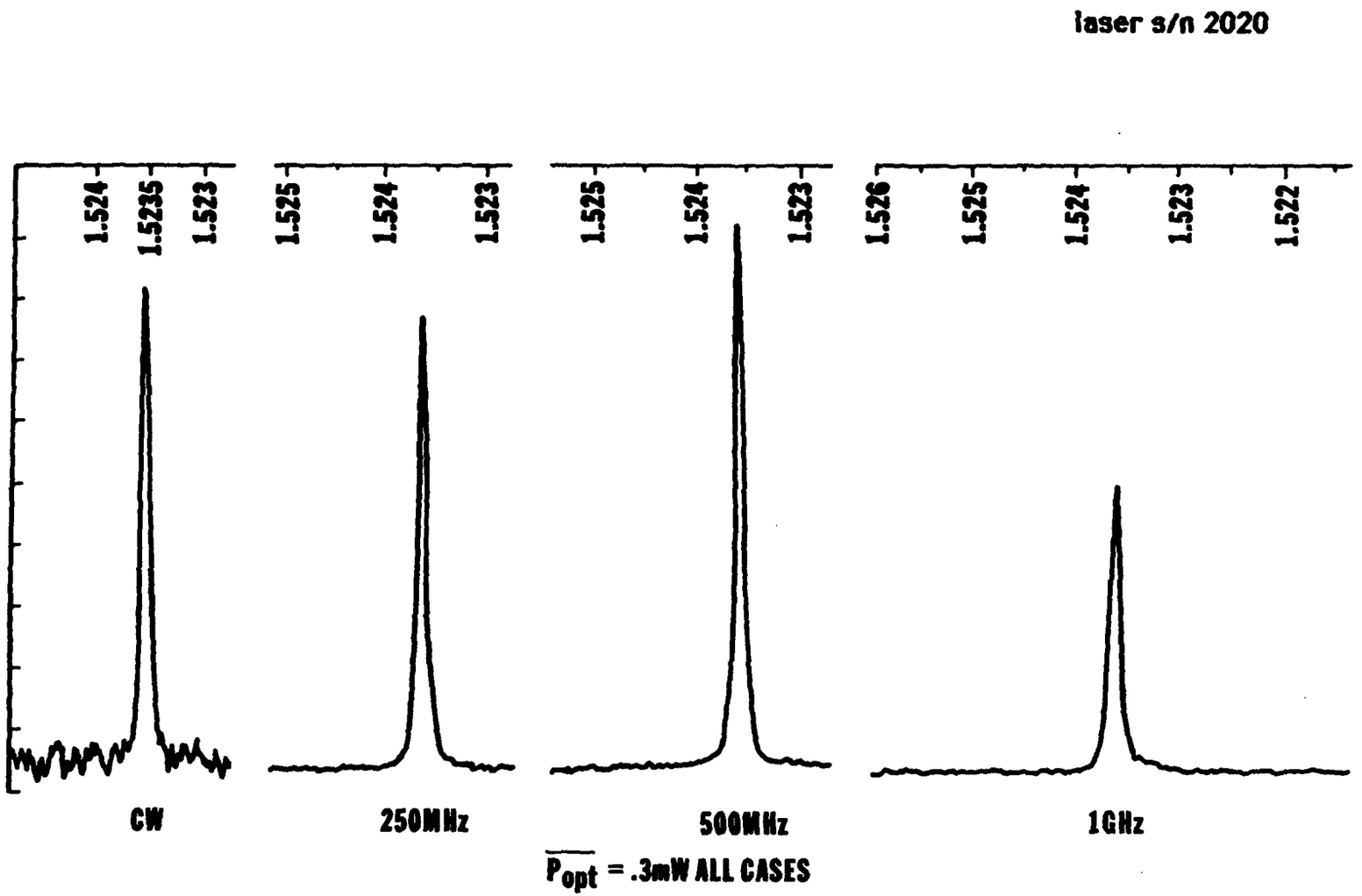


Figure 3.3.5-3 Optical spectra at 25°C of the Lasertron QLM-1550SM-DFB laser for CW, 250, 500, and 1000 MHz modulation. Modulation depth: 95%, vertical scale: linear.

The next two figures show the quality of the digital data output from the transmitter. Figure 3.3.5-4 shows the optical output waveforms and eye diagrams at 100-, 250-, 500-, and 1000-Mbit/s digital modulation rates. The output waveforms were produced with Manchester data. The eye diagrams were produced with NRZ format PRBS signals. Data at higher frequencies (1.5 and 2.0 Gbit/s) is shown in Fig. 3.3.4-5. Here, some jitter appears in the PRBS data. We attribute this jitter to the performance of the comparator chip in the transmitter.

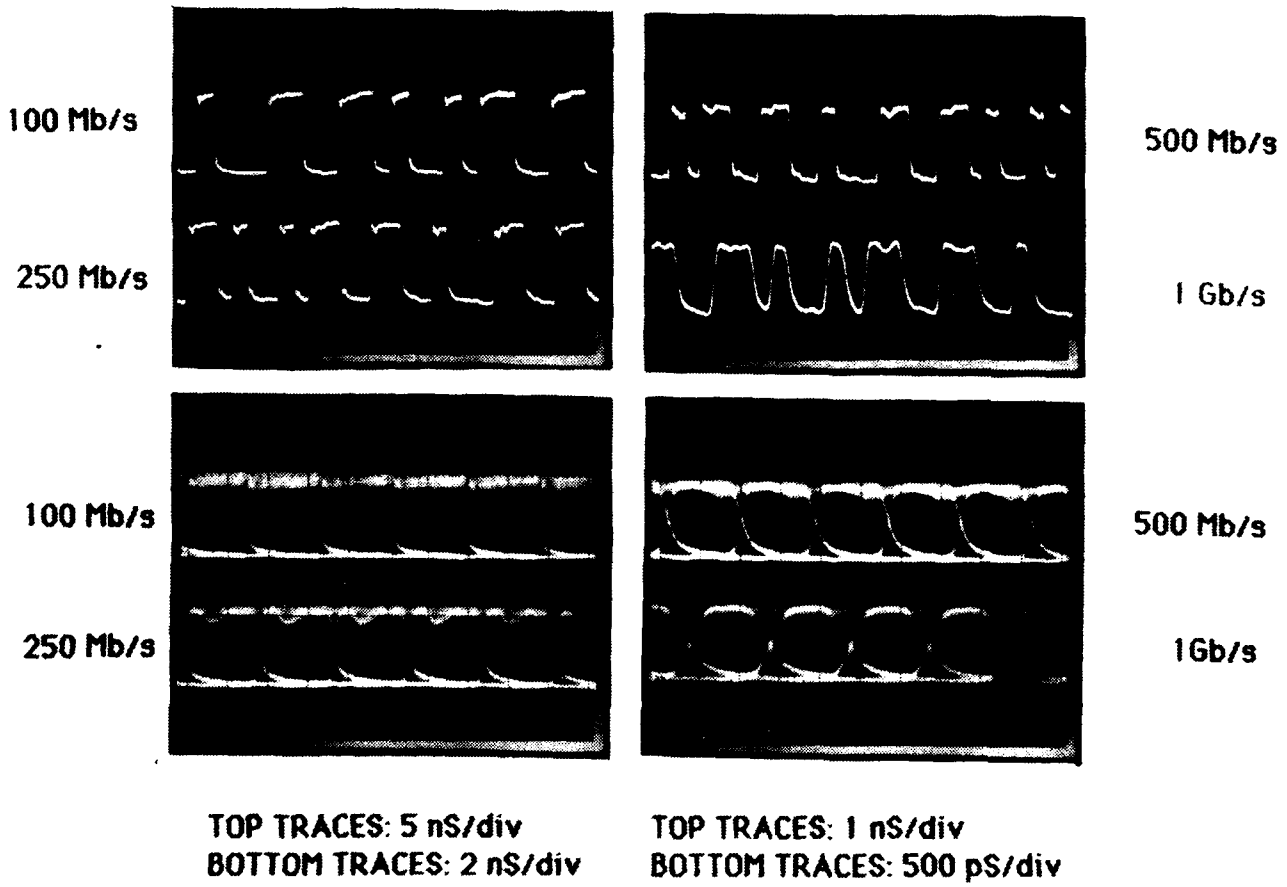
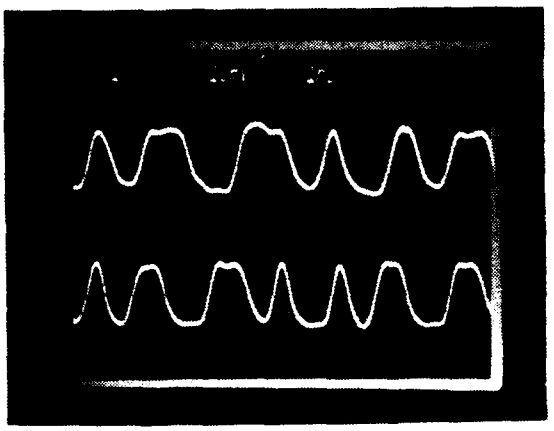
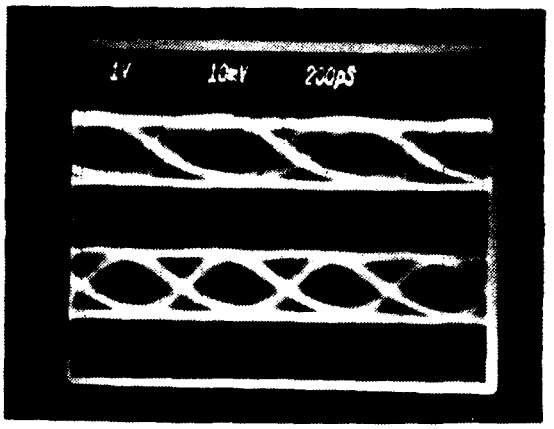


Figure 3.3.5-4 Transmitter digital data performance. Photos represent the optical output of the transmitter when modulated by ECL level input data of 100, 250, 500, and 1000 Mbit/s. Data format is Manchester for the top photos and PRBS NRZ for the eye pattern on the bottom photos.



TOP: 1.5 Gb/s NRZ

BOTTOM: 2.0 Gb/s NRZ



TOP: 1.5 Gb/s PRBS

BOTTOM: 2.0 Gb/s PRBS

Figure 3.3.5-5 **Transmitter digital data performance at 1.5 and 2.0 GBit/s NRZ. Left hand photos show Manchester encoded data while right hand photos show PRBS eye patterns.**

Level 5 Receiver

Figure 3.3.5-6 shows the block diagram of the Level 5 receiver. The key elements are the custom pinFET receiver, the gain postamplifier stages, and the threshold detection circuitry. The pinFET receiver is a hybrid circuit, shown schematically in Fig. 3.3.5-7. This buffered cascade design uses high-frequency, bipolar transistors following the GaAs FET transistor to provide gain and support the feedback loop. An emitter follower buffers the output. The remaining circuit is shown in Fig. 3.3.5-8. The pinFET receiver drives a cascade of low-noise gain stages (Avantek 0785 10 dB amplifiers). AGC action is provided through the voltage-controlled attenuator. The threshold detection is performed by a GaAs comparator chip (Gigibit logic 10G012A). This is connected to the output connector through an OR/NOR gate (Harris HMD11101) that serves as an output buffer.

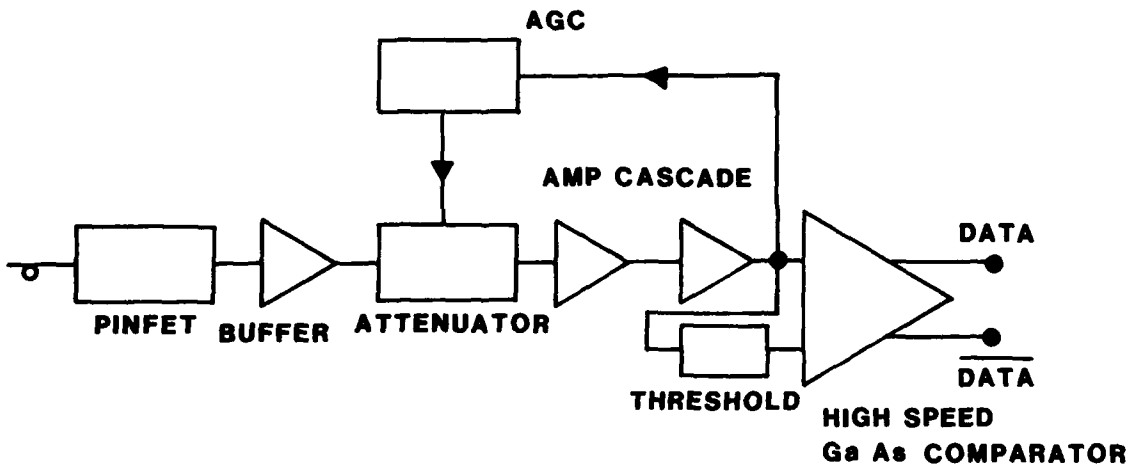


Figure 3.3.5-6. Block diagram of Level 5 receiver.

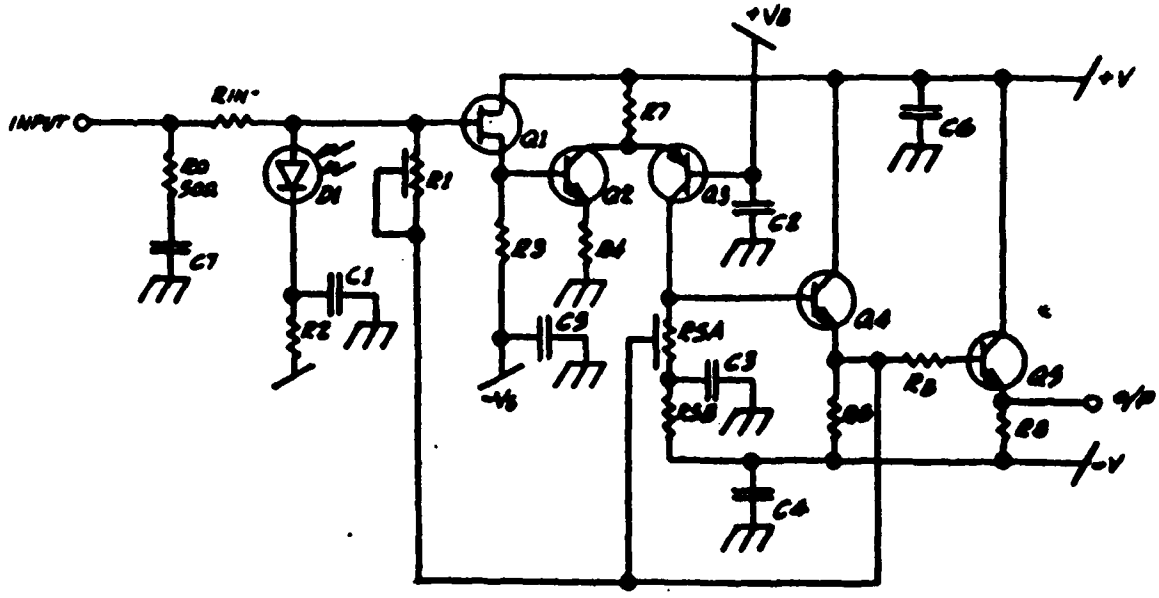


Figure 3.3.5-7. Schematic diagram of pinFET receiver built by RCA ElectroOptics.

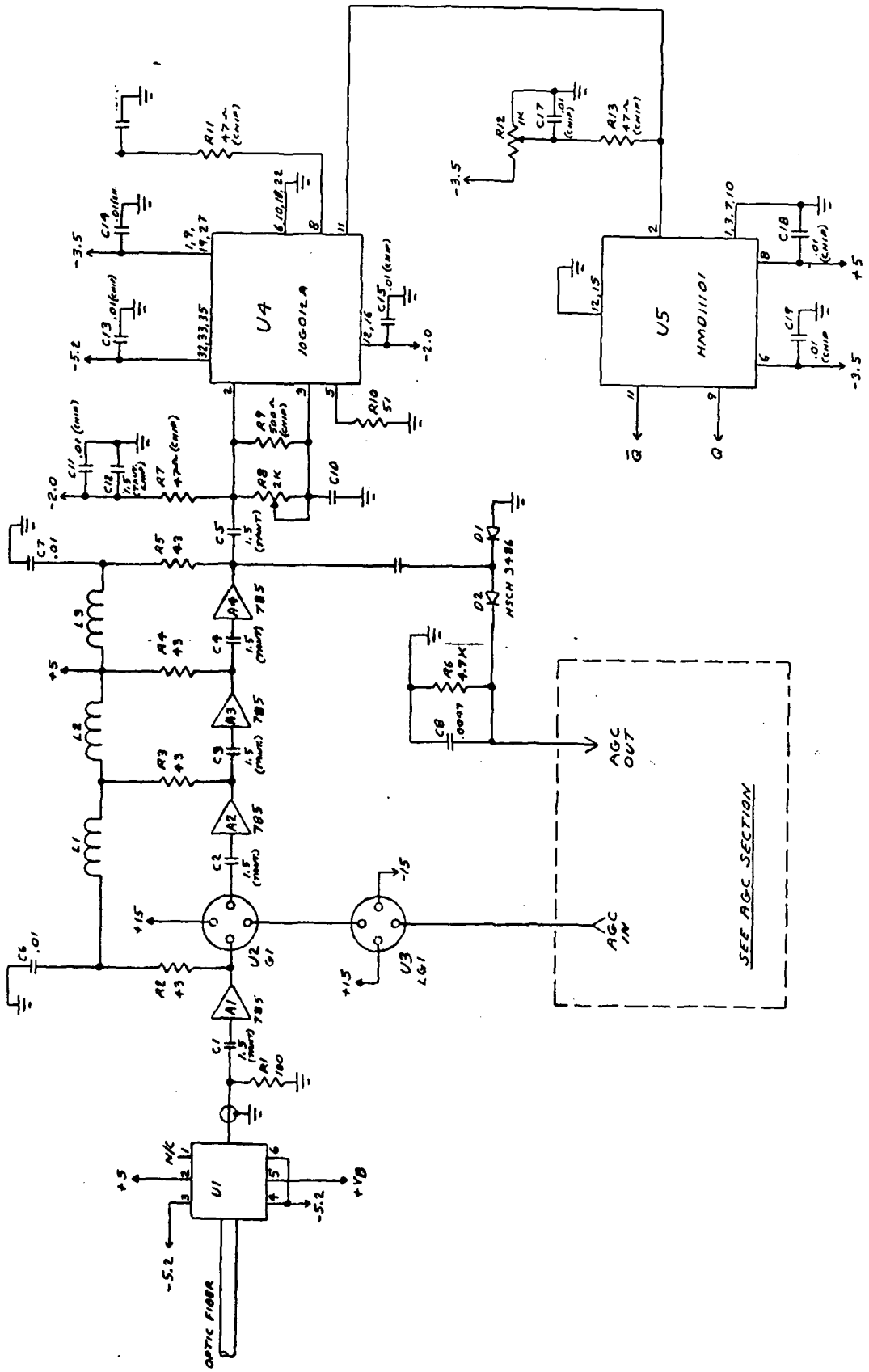


Figure 3.3.5-8. Schematic diagram of complete Level 5 receiver.

Since the pinFET receiver is a custom device, its performance was characterized in detail. Figure 3.3.5-9 summarizes the critical data. The spectrum analyzer top traces (on the left of the figure) show the frequency response of the unit at various values of the bandwidth control voltage, V_b. By way of comparison, the lower traces show the response of a high-speed pin photodiode (RCA type 979) in a broadband microwave mount. The oscilloscope tracings on the right show the response to digital data at 1 Gbit/s for each of the three values of V_b. The frequency response and data fidelity are very sensitive to small changes in the bandwidth control voltage.

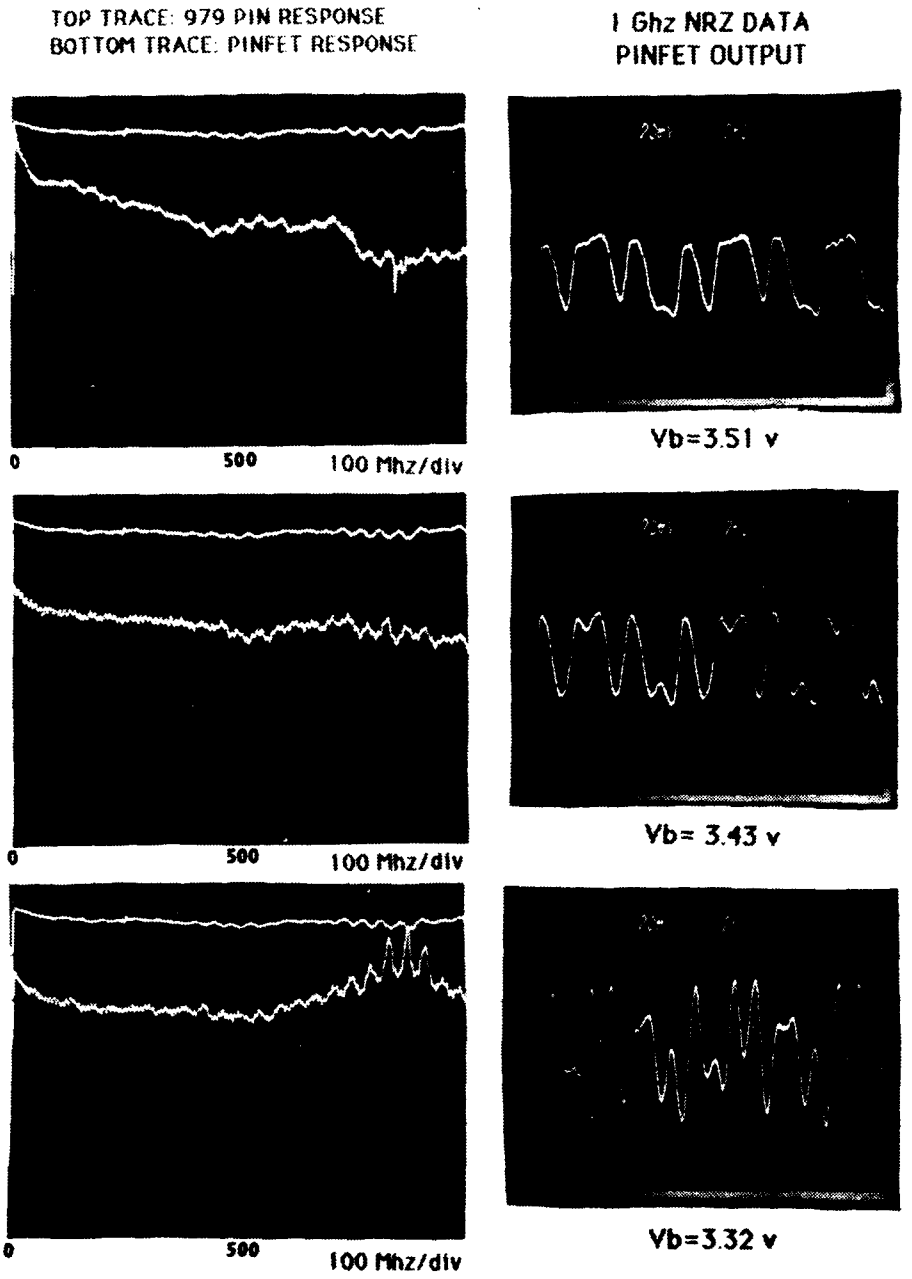


Figure 3.3.5-9. Performance data on pinFET receiver. Left hand photos compare the frequency response of the unit to the response of a high speed RCA type 979 pin photodiode in a broadband microwave mount. Three different values of the bandwidth control voltage V_b are represented. The right hand photos illustrate the data response at 1 Gbit/s for each of the bandwidth control voltages selected.

The output waveforms and eye patterns for the complete receiver are summarized in Fig. 3.3.5-10. The outputs shown are at ECL levels. The top pictures represent NRZ data at 100-, 250-, 500-, and 1000-Mbit/s, while the bottom pictures show PRBS (Psuedo Random Bit Stream) eye patterns at the same bit rates. The jitter at 1 Gbit/s is thought to be caused by the comparator.

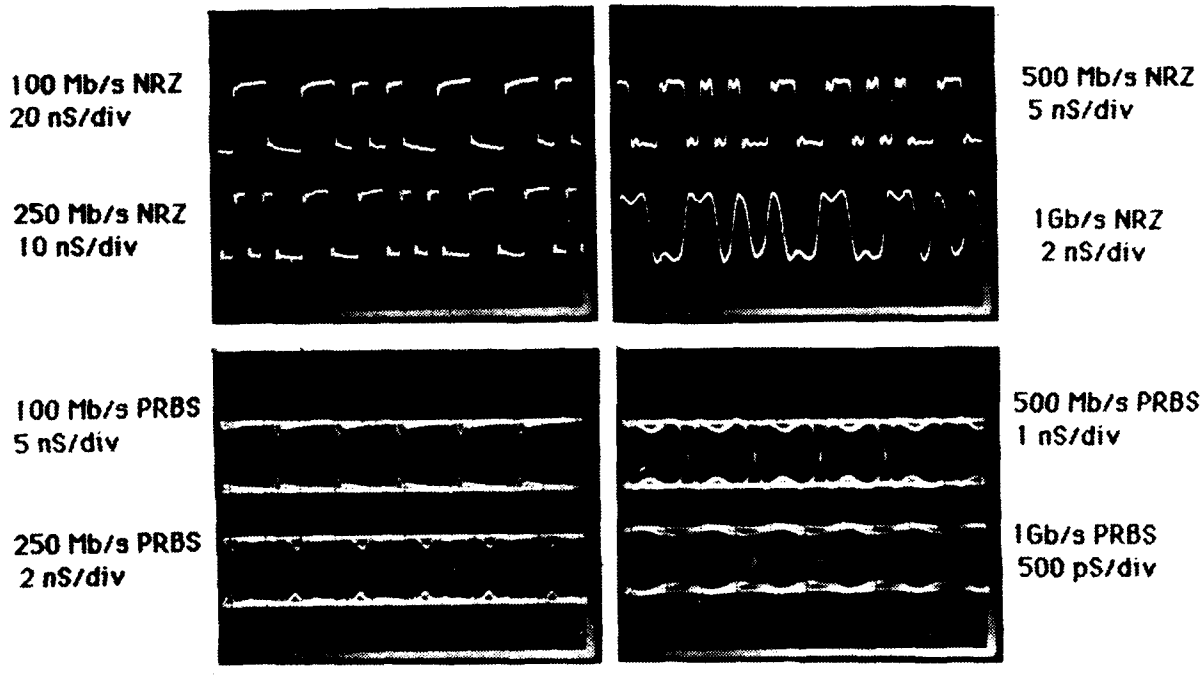


Figure 3.3.5-10. Performance data on the complete Level 5 receiver. Outputs shown are ECL level waveforms. The top photos represent NRZ data at 100, 230, 500, and 1000 Mbit/s, and the bottom photos are PRBS eye patterns at the same bit rates.

Figure 3.3.5-11 shows BER measurements for the receiver at 250-, 500-, and 1000-Mbit/s PRBS data. All data was taken at 25°C. The sensitivity at 10^{-9} BER is at least 24.5 dBm. A summary of these measurements and corresponding dynamic range results are shown in the table in Fig. 3.3.5-12. The dynamic range varies from 8 dB at 1000 Mbit/s to greater than 11 dB at 100 Mbit/s.

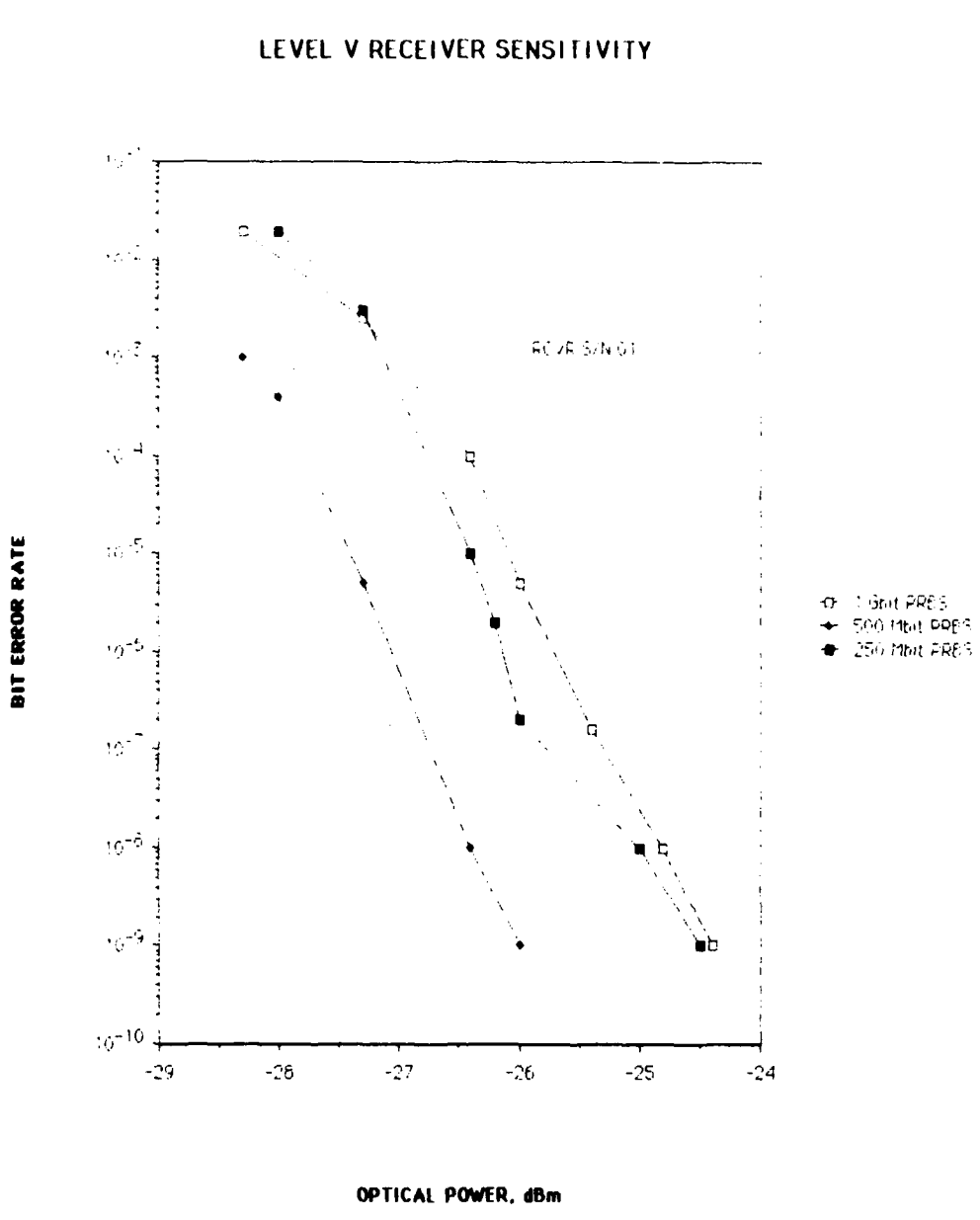


Figure 3.3.5-11. Bit Error Rate (BER) data for the Level 5 receiver at 250, 500 and 1000 Mbit/s PRBS, taken at 25°C.

s/n 01

	P min (sensitivity)	P max	Dynamic Range
1 Gbit/s	-25.2 dBm	-17.2 dBm	8 dB
500 Mbit/s Manch.	-24.2 dBm	-14.4 dBm	9.8 dB
250 Mbit/s Manch	-26 dBm	-15.9 dBm	10.1dB
100 Mbit/s PRBS	-25.8 dBm	> -14.8 dBm	> 11 dB

Figure 3.3.5-12. Summary of receiver sensitivity and dynamic range performance.

DFB Diode Laser Spectral Performance

Single-longitudinal-mode laser diodes were used for the Level 5 transmitter. These devices produce output in a narrow spectral line, in place of the much broader multi-line output of multi-mode lasers. Single-line output results from the inclusion of a grating structure within the laser cavity. This laser gives feedback at only one frequency resonant with its periodicity. The distributed feedback (DFB) structure yields narrow-linewidth output. This narrow, single-line spectrum allows minimum dispersion in long-range, fiber-optic transmission. Considerable data confirming the spectral characteristics of the lasers was taken and is included here.

Two types of lasers were evaluated for the Level 5 program: Lasertron QLM1550DFB-601 and Stantel LC113C-17. Three Lasertron units and one Stantel unit were available. Data for the units is grouped as follows: Stantel Serial # 8845, Figs. 3.3.5-13 through 18; Lasertron Serial # 2020, Figs. 3.3.5-19 through 23; Lasertron Serial # 3066, Figs. 3.3.5-24 through 27; Lasertron Serial # 3080, Figs. 3.3.5-28 through 31. In the two delivered transmitter units, Transmitter # 01 contained Lasertron Serial # 3080 and Transmitter # 02 contained Lasertron Serial # 2020. Data presented includes high-resolution (0.5 Å), scanned-spectrometer and lower resolution (> 1 Å), automated spectrometer measurements covering wide dynamic range. Some data on the Stantel device was supplied with the unit (Figs. 3.3.5-14 and 15).

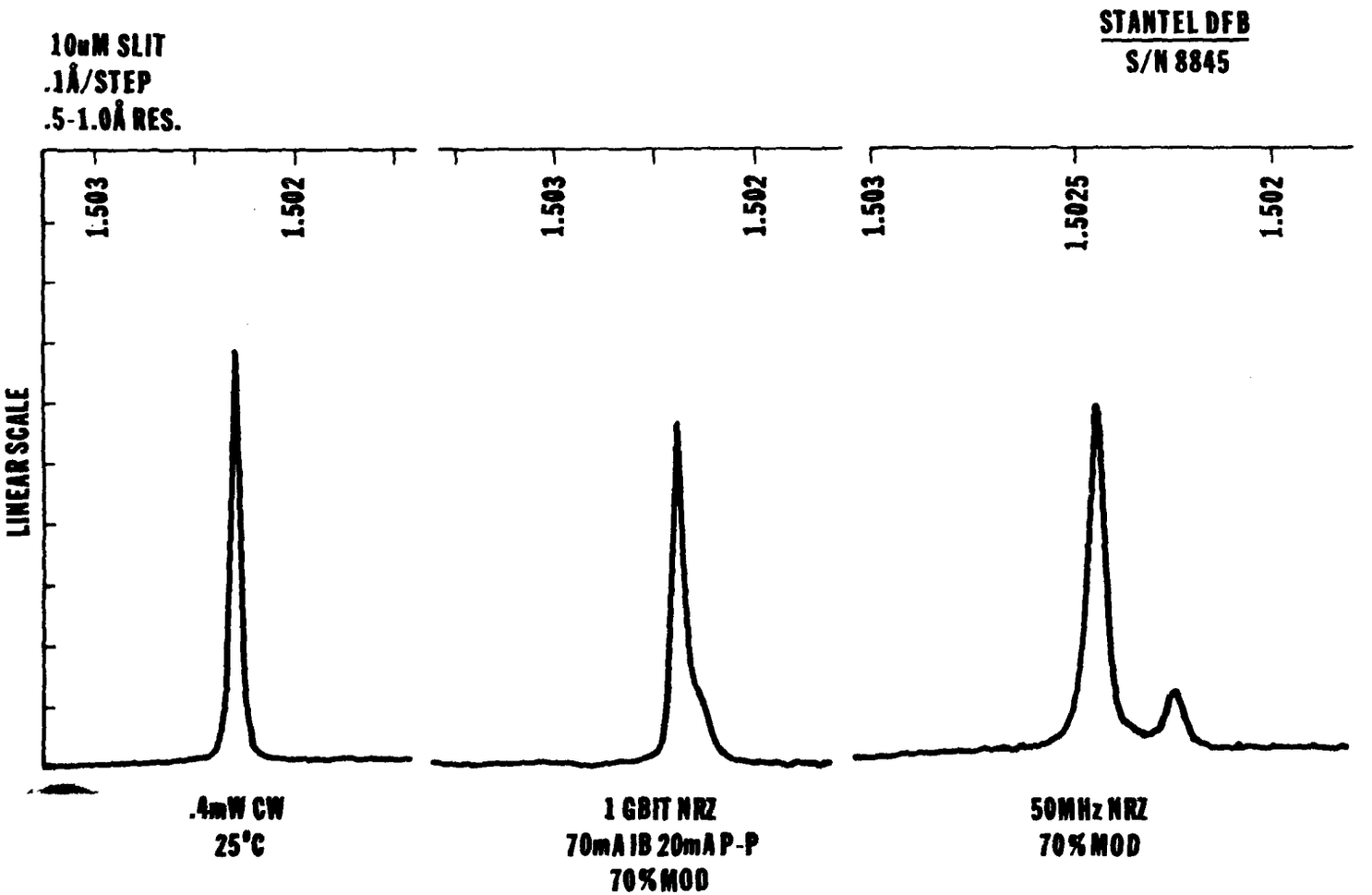


Figure 3.3.5-13. *Spectral response on a linear scale at 25°C. for cw, 50- and 1000-Mbit/s NRZ data (0.4 mW and 70% modulation depth).*

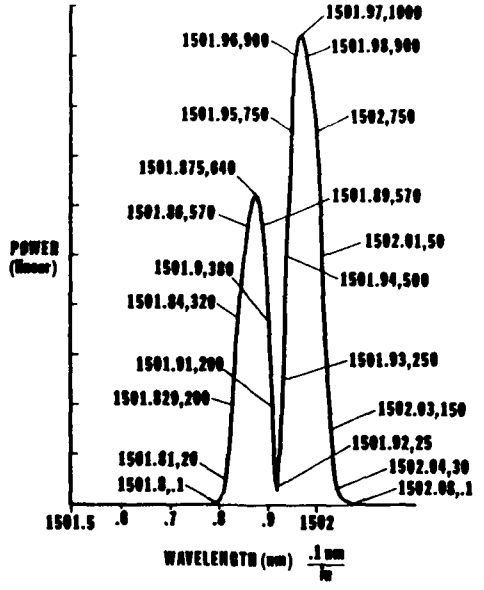


Figure 3.3.5-14 Spectral data at 10-kHz modulation rate.

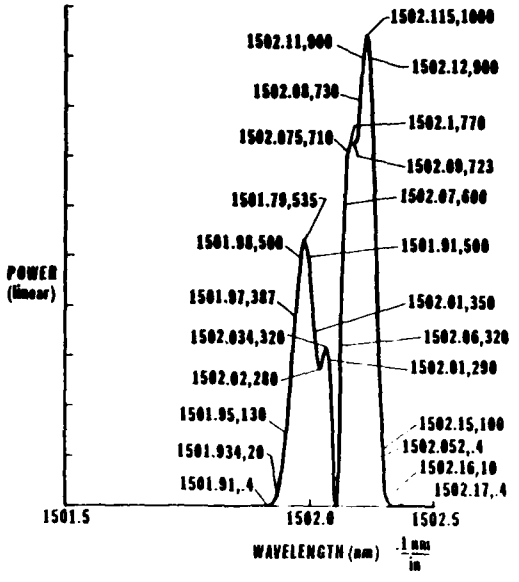


Figure 3.3.5-15 Spectral data at 100-MHz modulation rate.

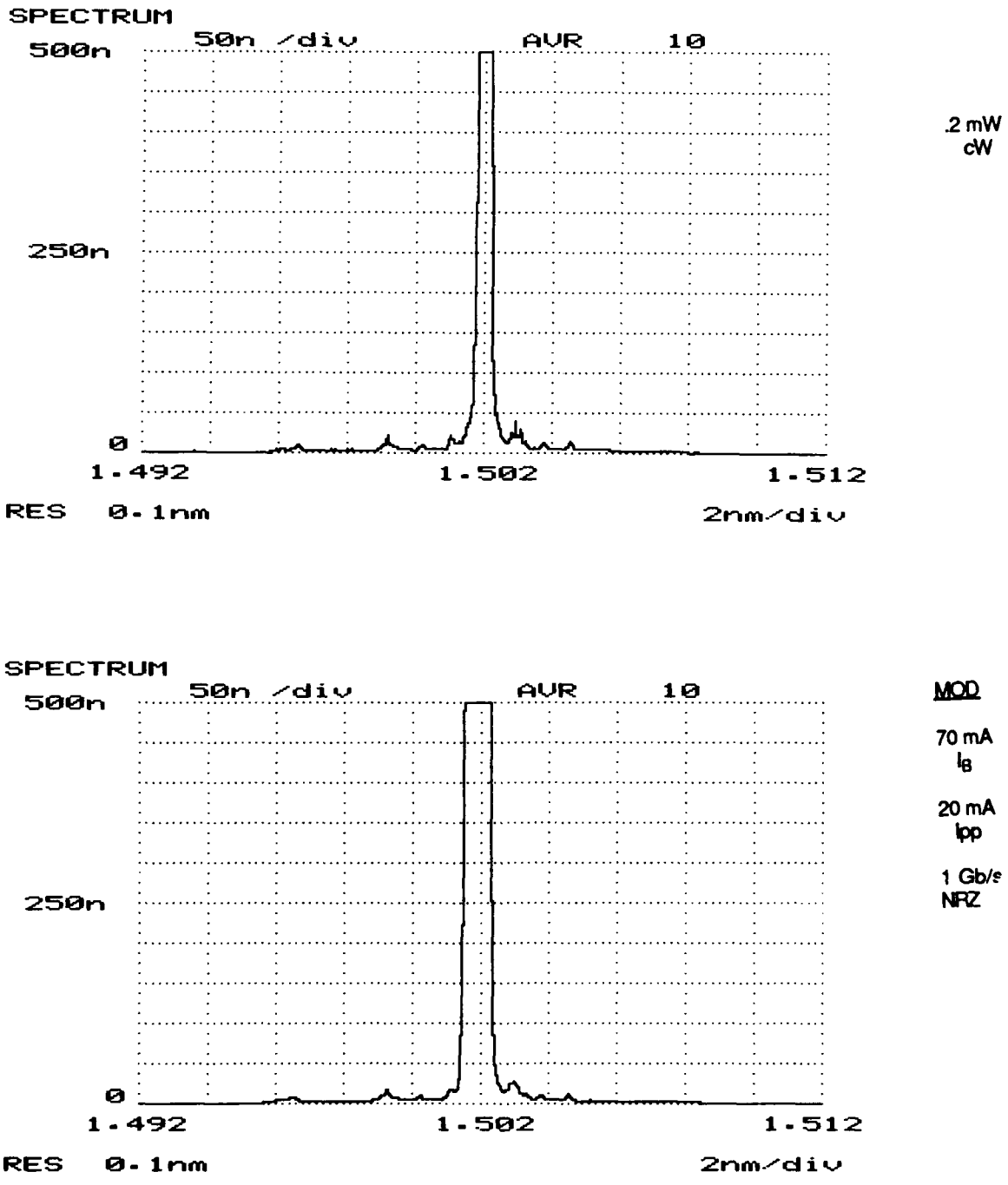


Figure 3.3.5-16. Spectral response on a linear scale, with 0.2-mW, cw output (top) and 1 Gbit/s NRZ at 70 % modulation (bottom).

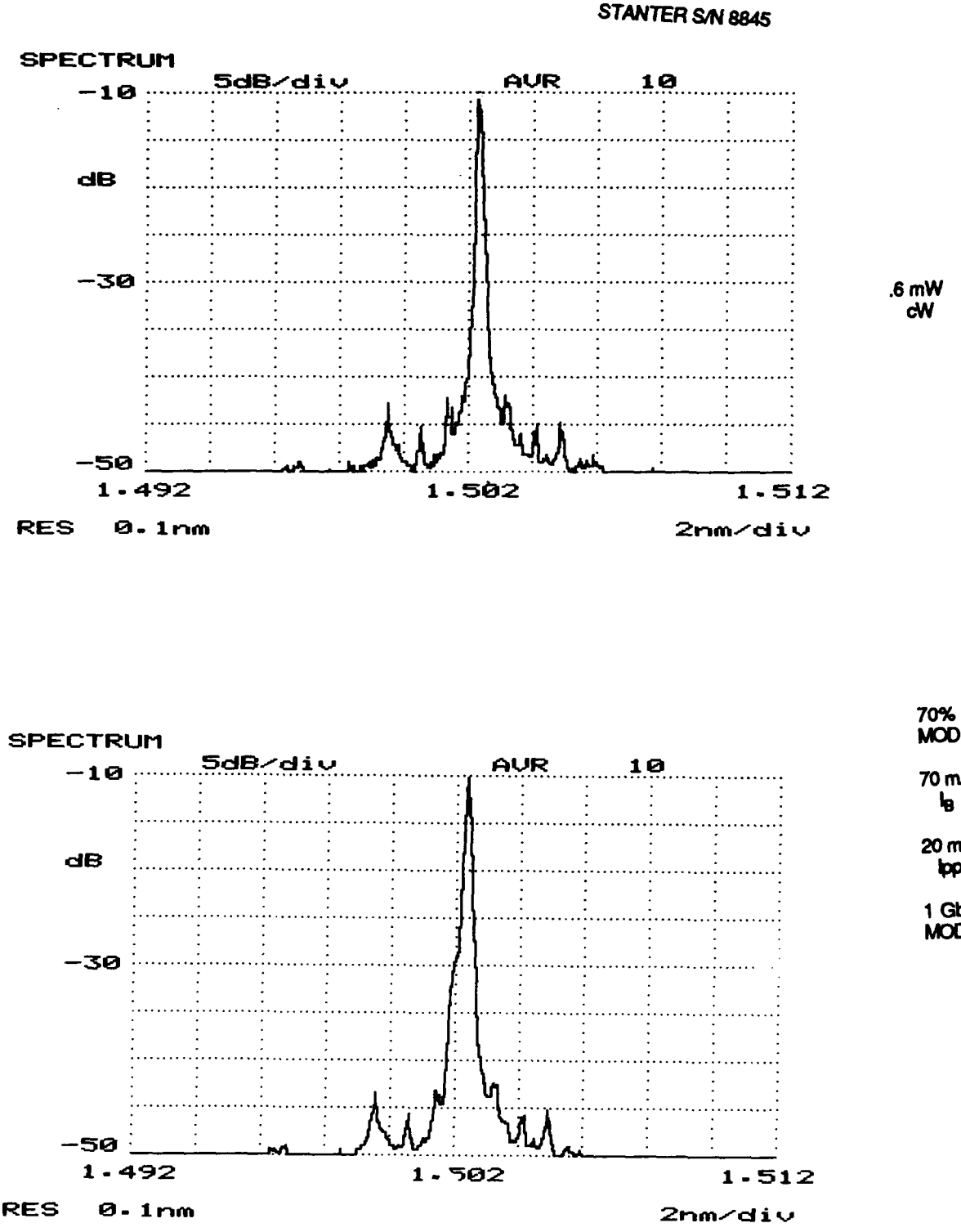


Figure 3.3.5-17. Spectral response on a log scale, with 0.2-mW, cw output (top) and 1 Gbit/s NRZ at 70 % modulation (bottom).

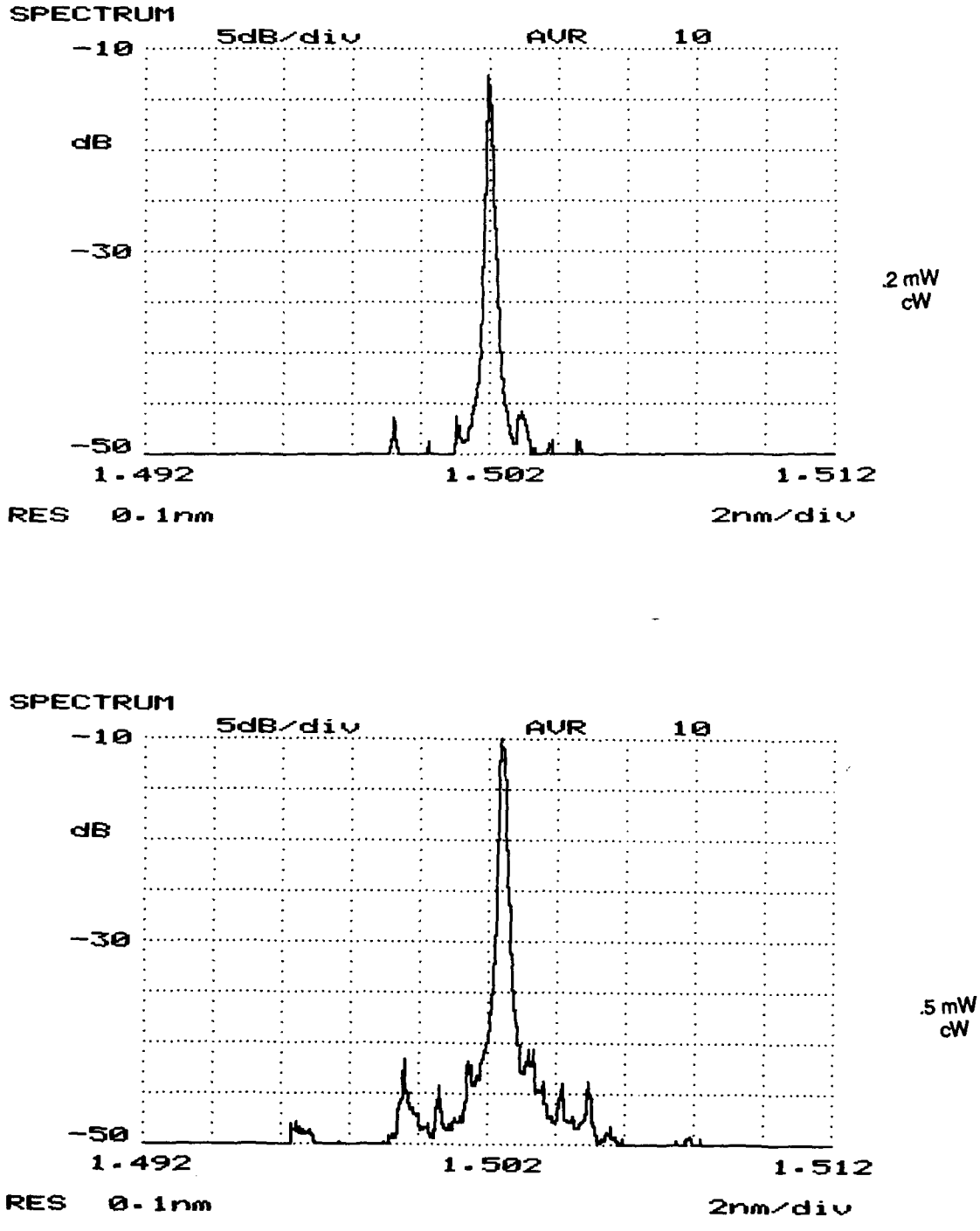


Figure 3.3.5-18. Spectral response at cw on a log scale, with 0.2-mW (top) and 0.5-mW (bottom) output powers.

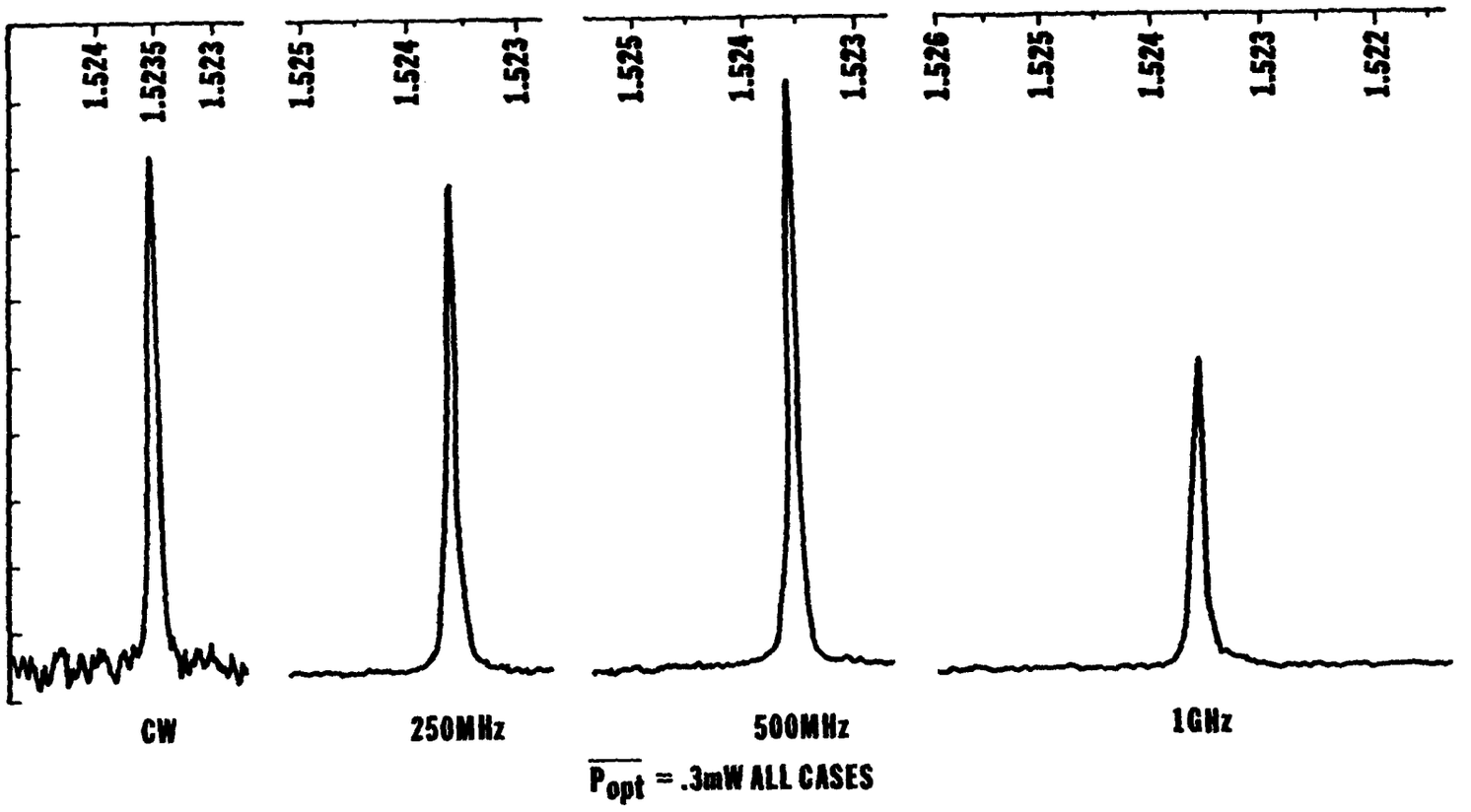


Figure 3.3.5-19. Spectral response on a linear scale at 0.3-mW average power output and cw, 250-, 500-, and 1000-MHz modulation.

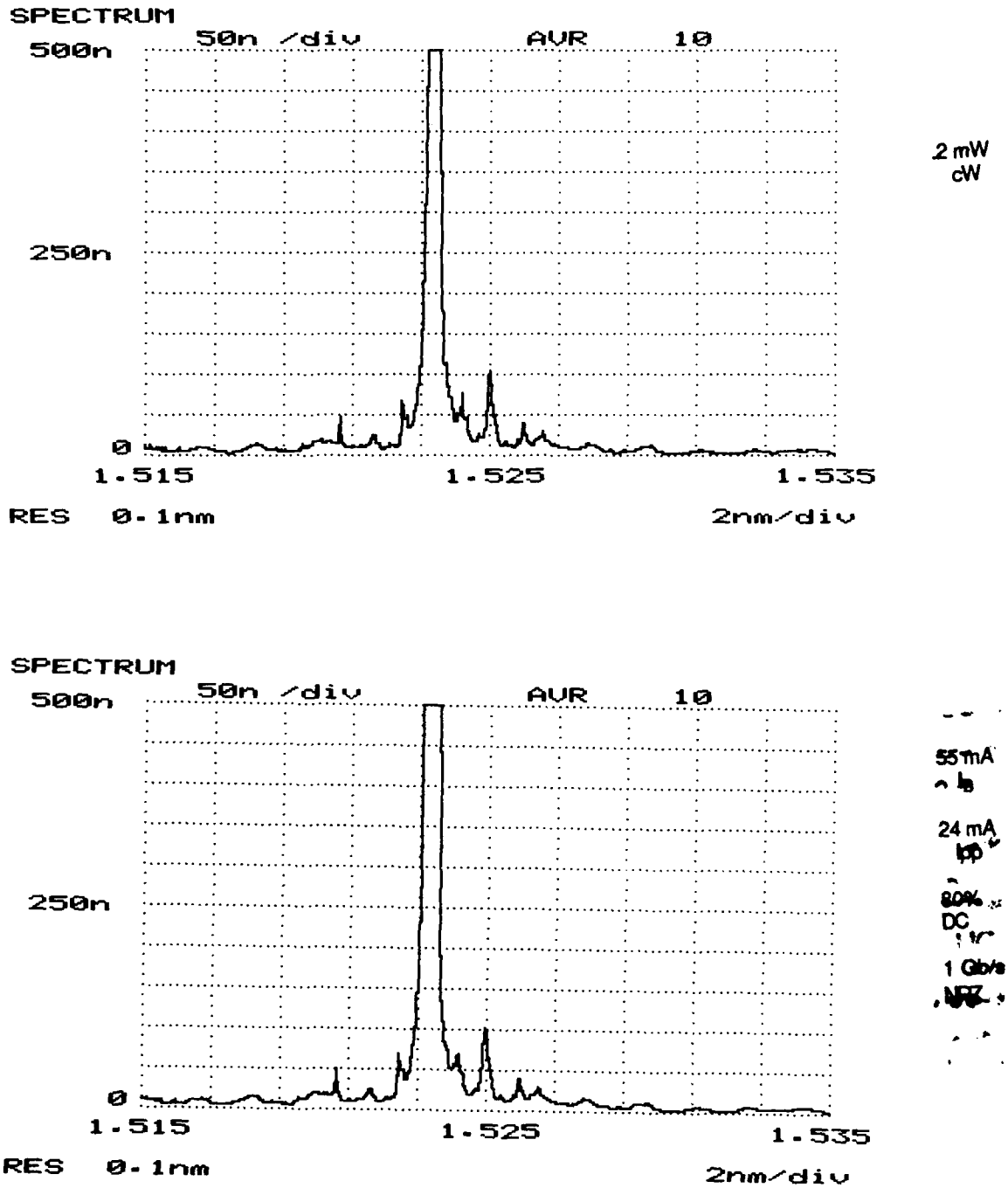


Figure 3.3.5-20. Spectral response on a linear scale, with 0.2-mW, cw output (top) and 1 Gbit/s NRZ at 80% modulation depth (bottom).

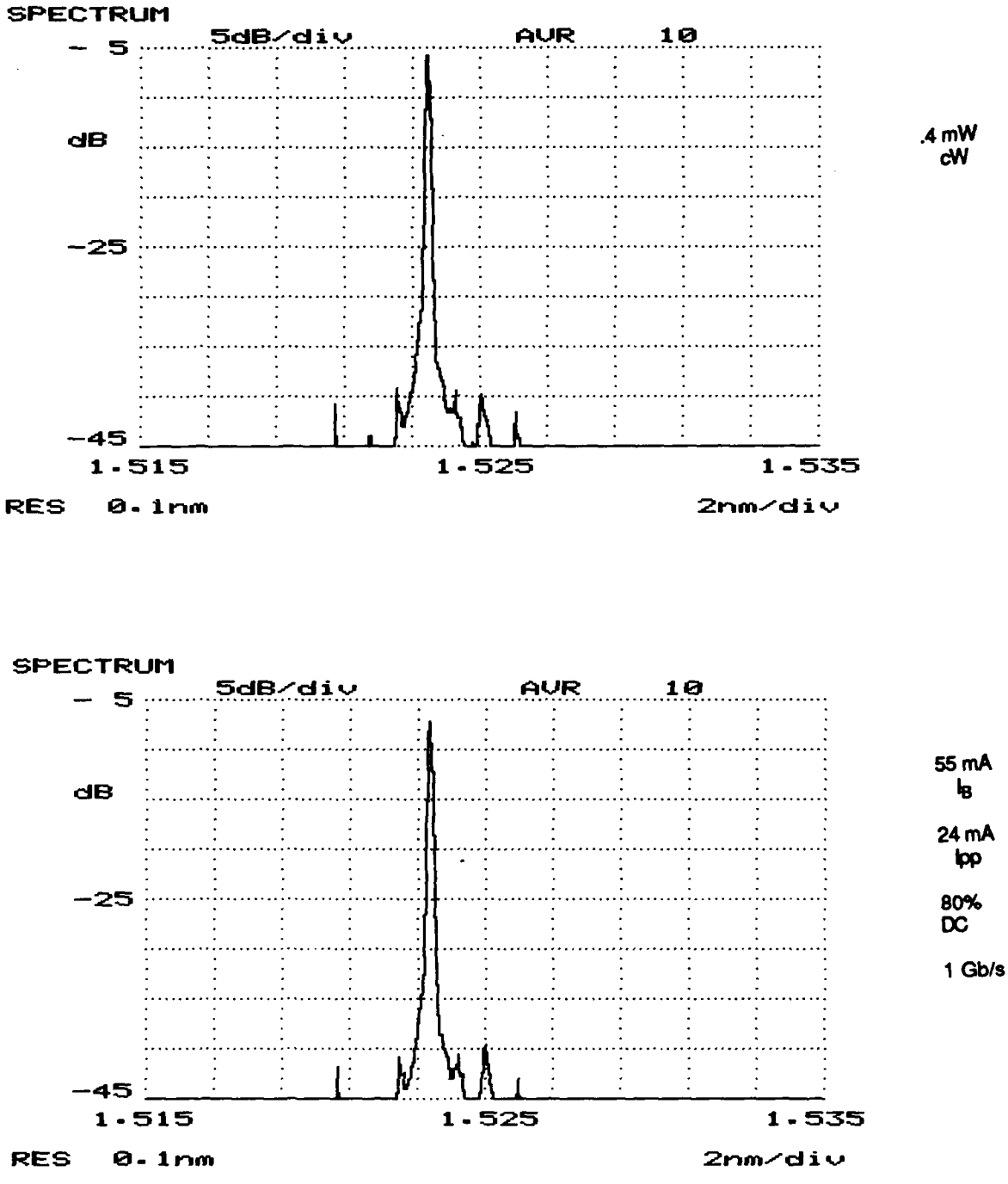


Figure 3.3.5-21. Spectral response on a log scale, with 0.4-mW, cw output (top) and 1 Gbit/s NRZ at 80% modulation depth (bottom).

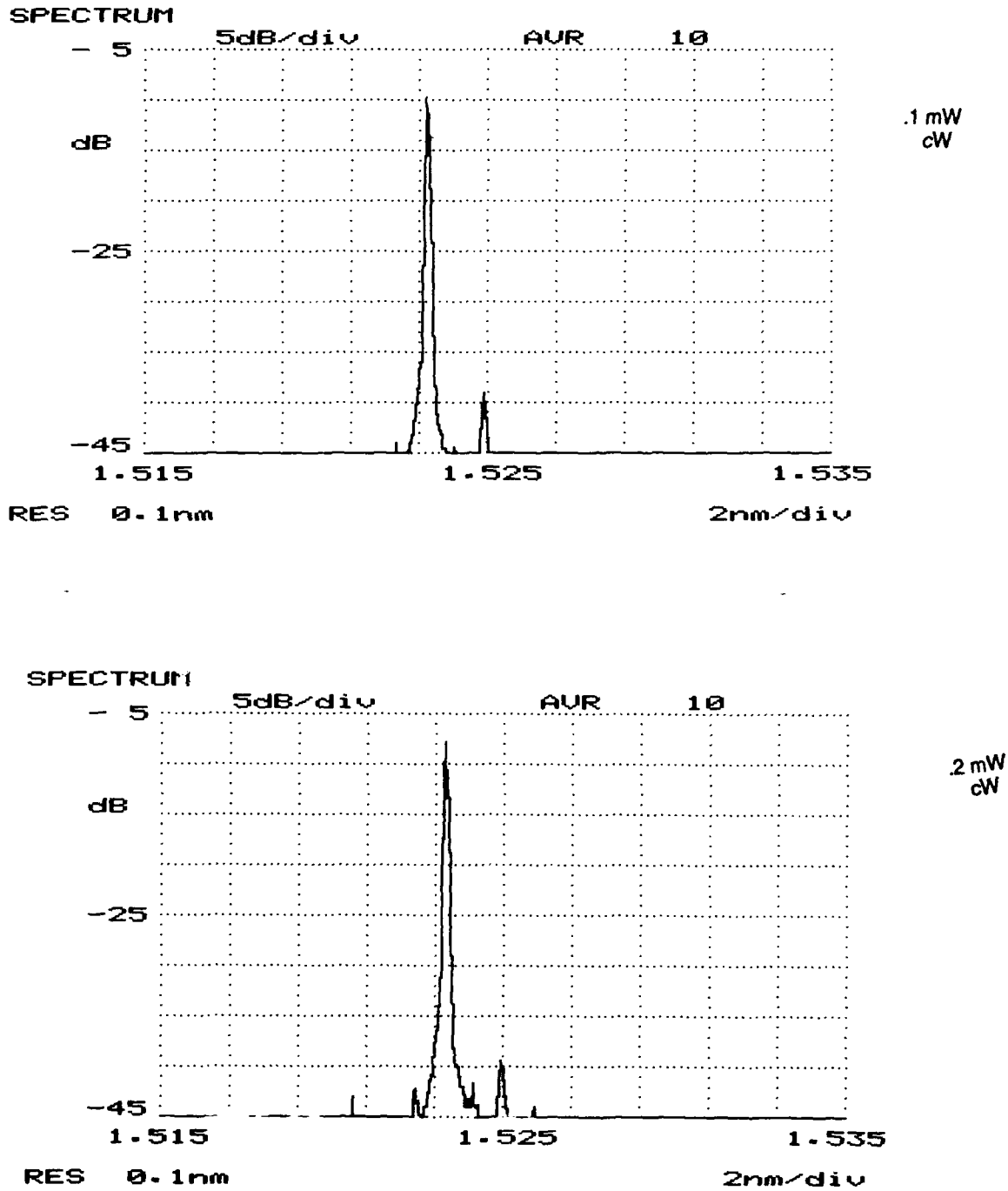


Figure 3.3.5-22. Spectral response at cw on a log scale, with 0.1-mW (top) and 0.2-mW (bottom) output powers.

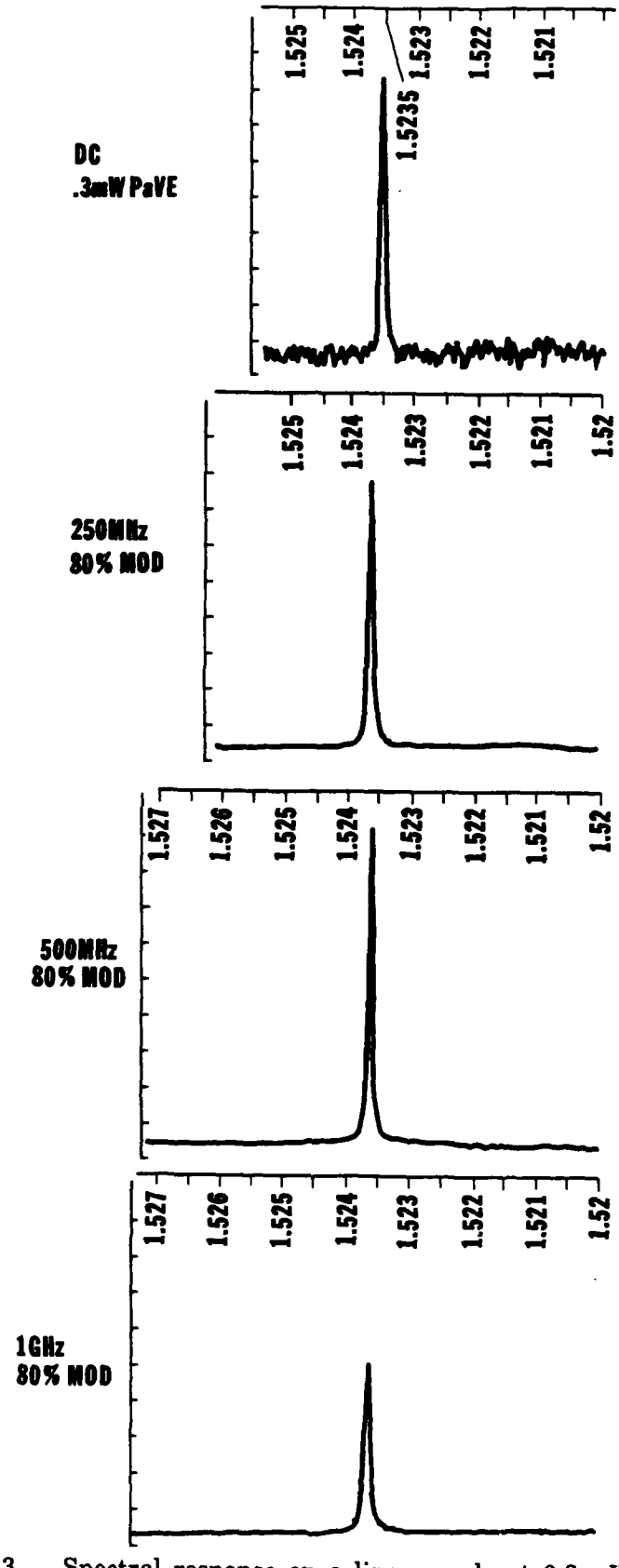


Figure 3.3.5-23. Spectral response on a linear scale at 0.3-mW average power output and cw, 250-, 500-, and 1000-MHz modulation, all at 80% modulation depth.

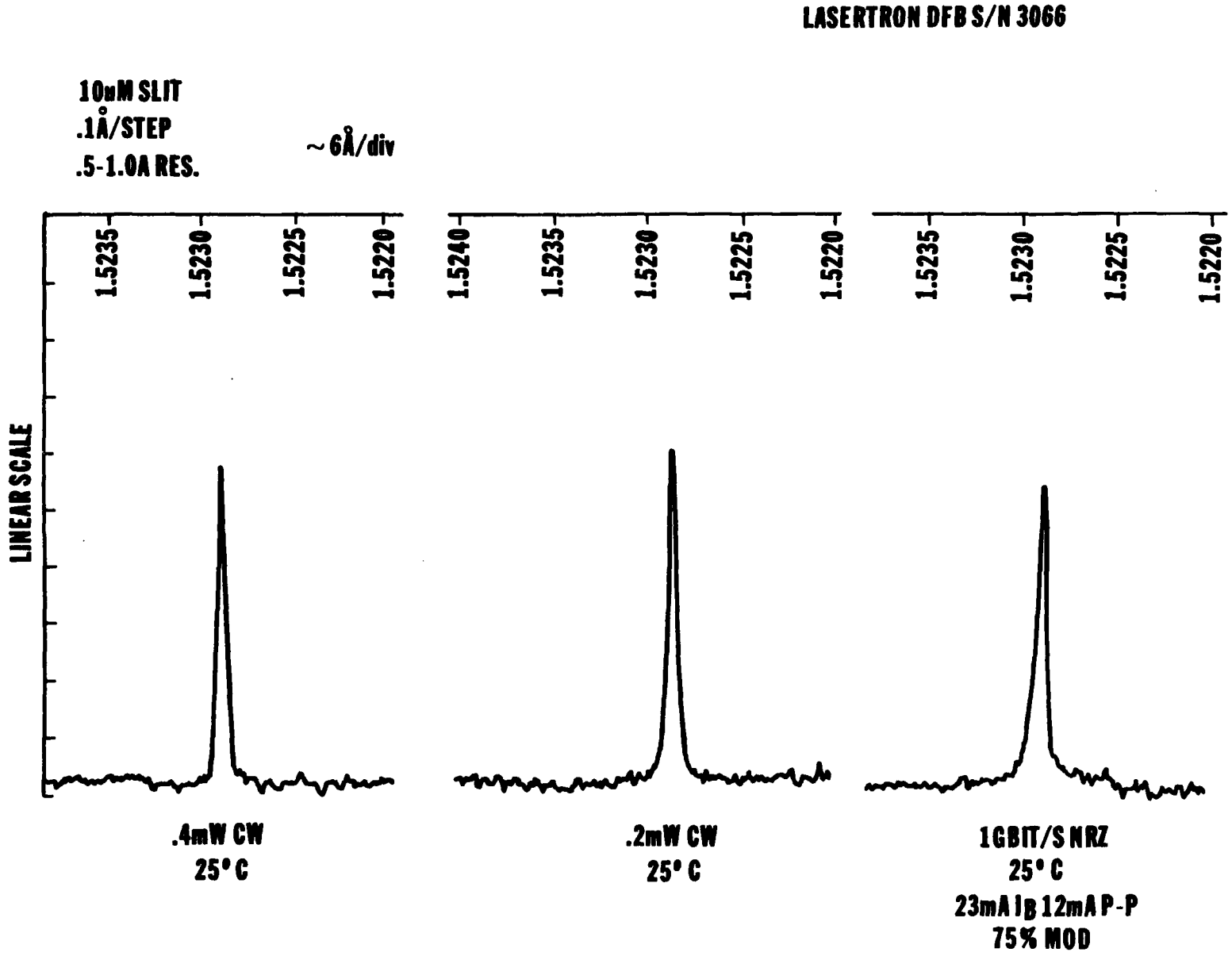


Figure 3.3.5-24. Spectral response on a linear scale, showing 0.2-mW cw, 0.4-mW cw, and 1 Gbit/s NRZ (75% modulation depth).

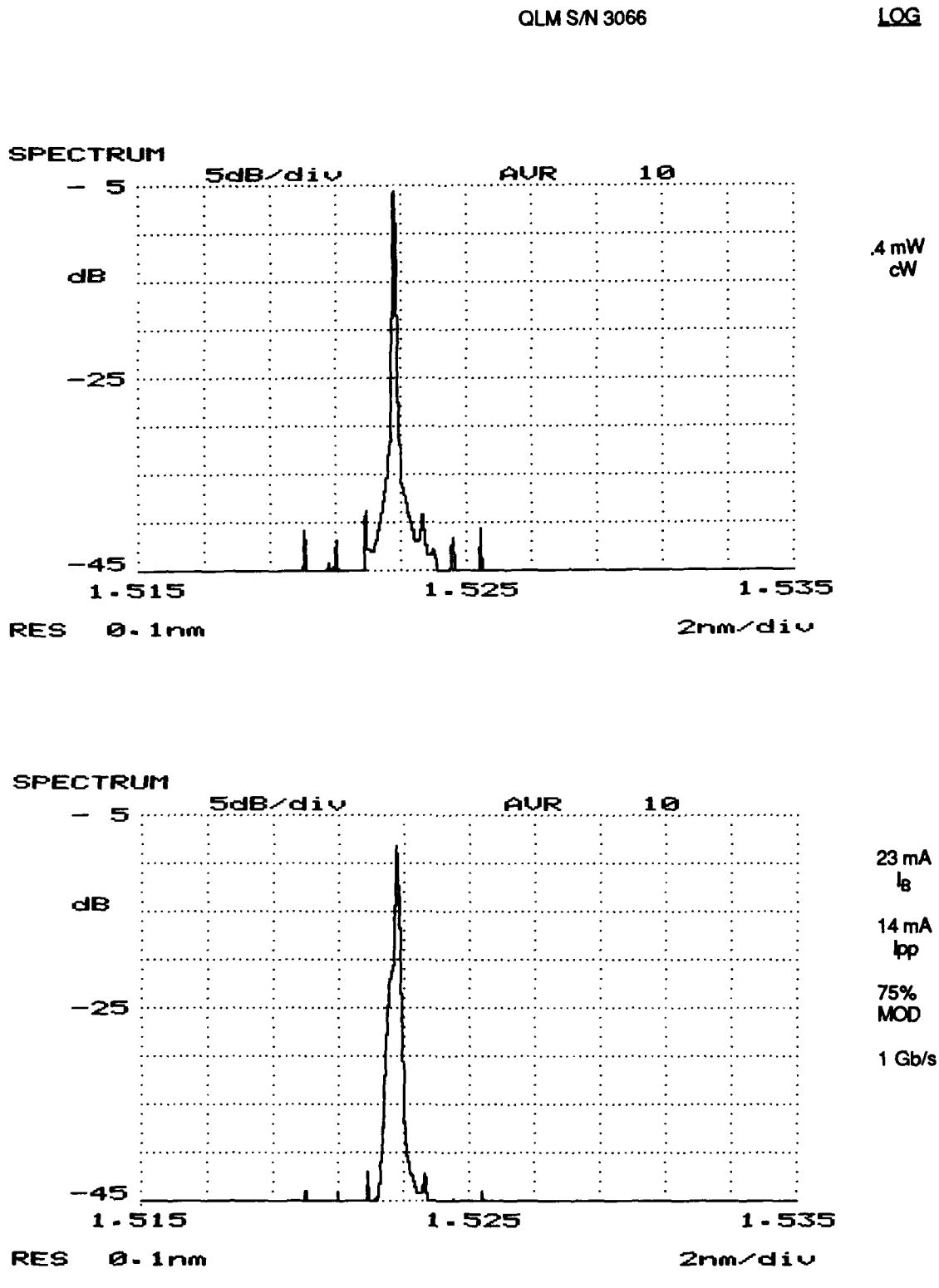
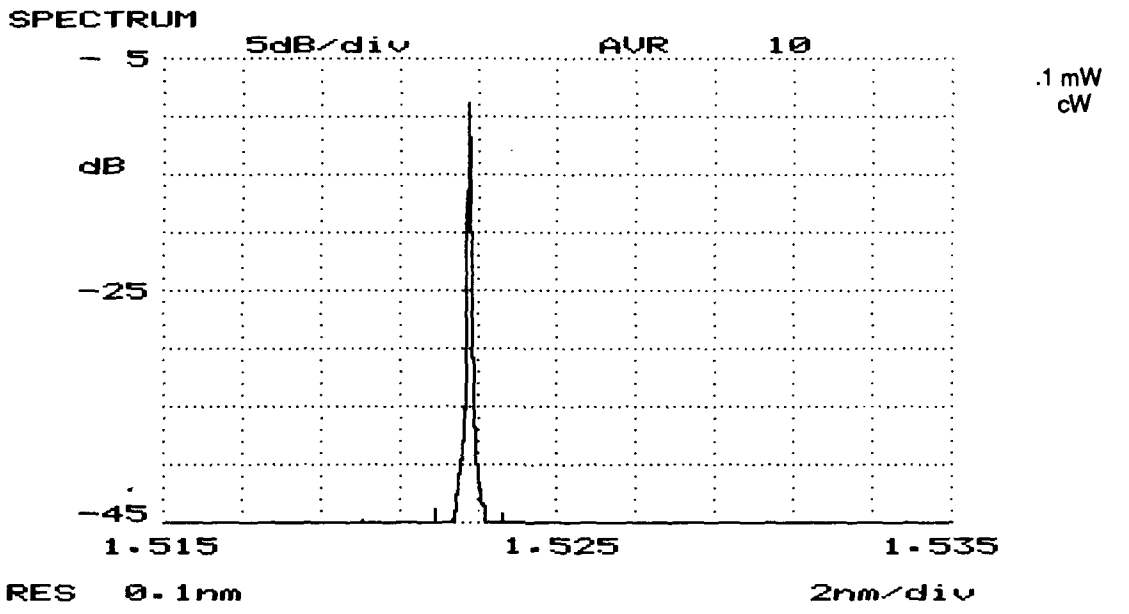


Figure 3.3.5-25. Spectral response on a log scale, with 0.4-mW, cw output (top) and 1 Gbit/s NRZ at 75% modulation depth (bottom).



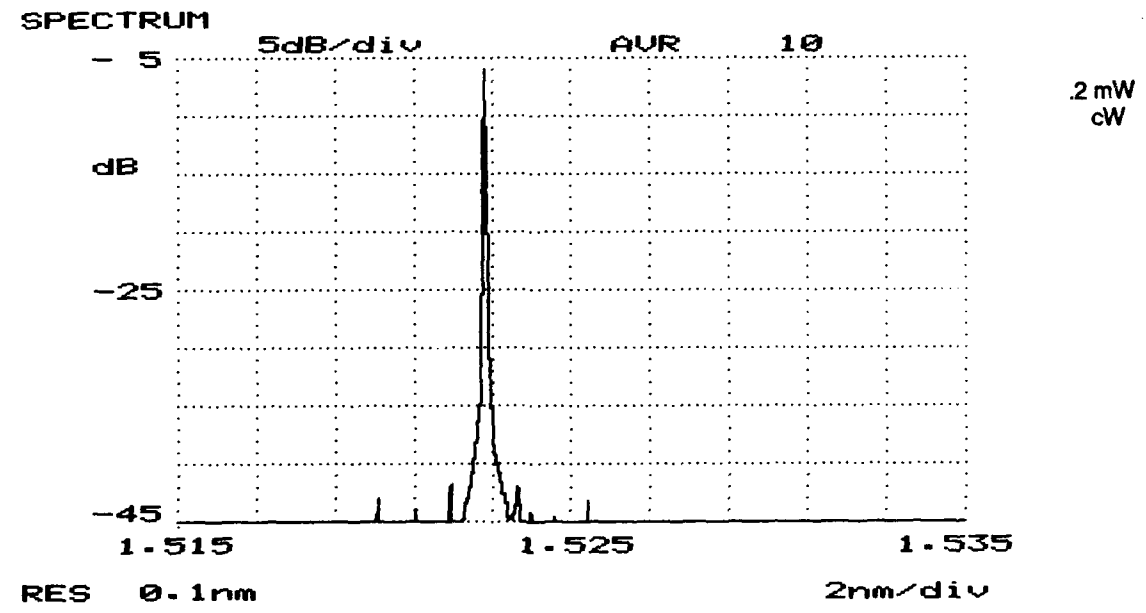


Figure 3.3.5-26. Spectral response at cw on a log scale, with 0.1-mW (top) and 0.2-mW (bottom) output powers.

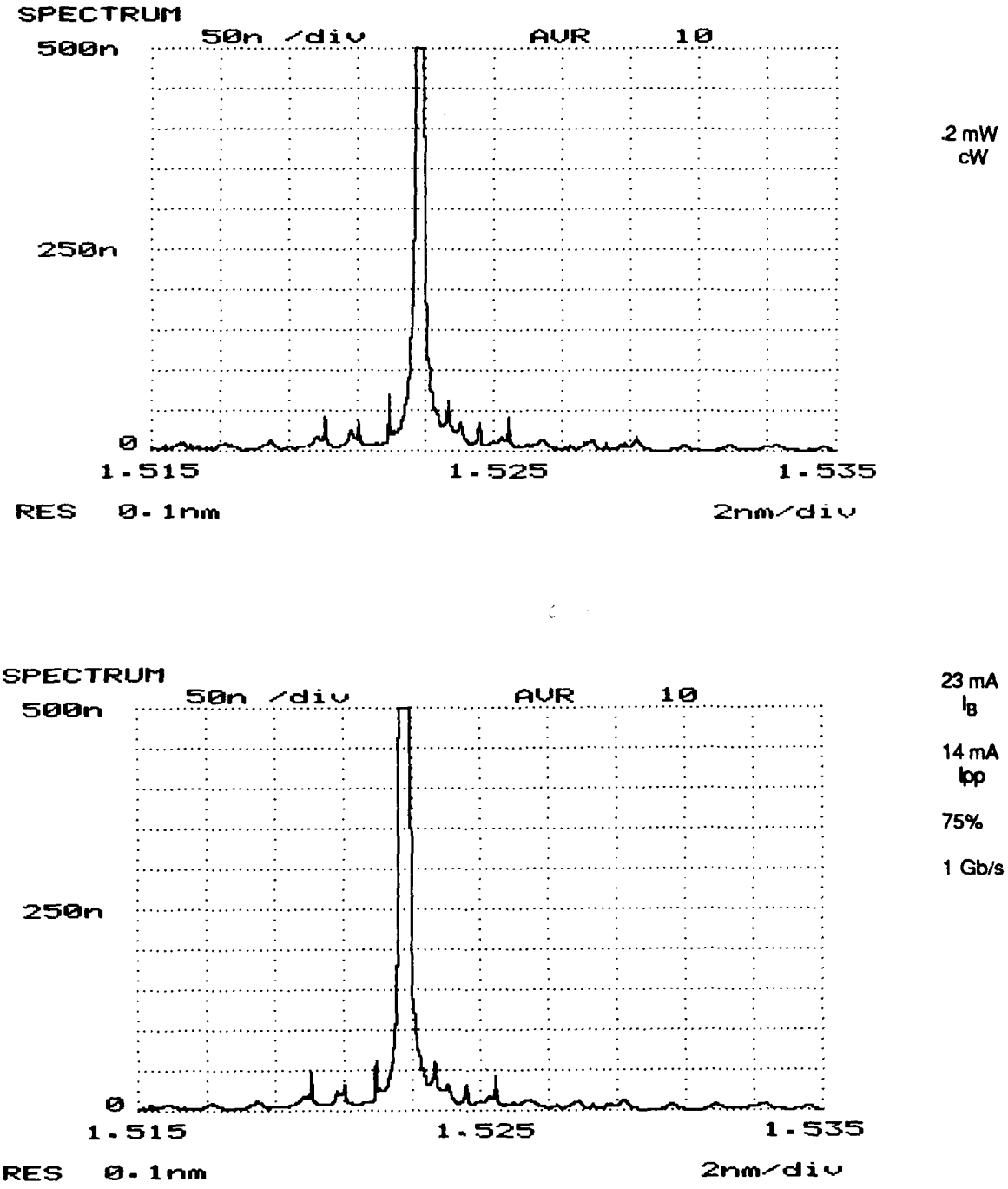


Figure 3.3.5-27. Spectral response on a linear scale, with 0.2-mW, cw output (top) and 1 Gbit/s NRZ at 75% modulation depth (bottom).

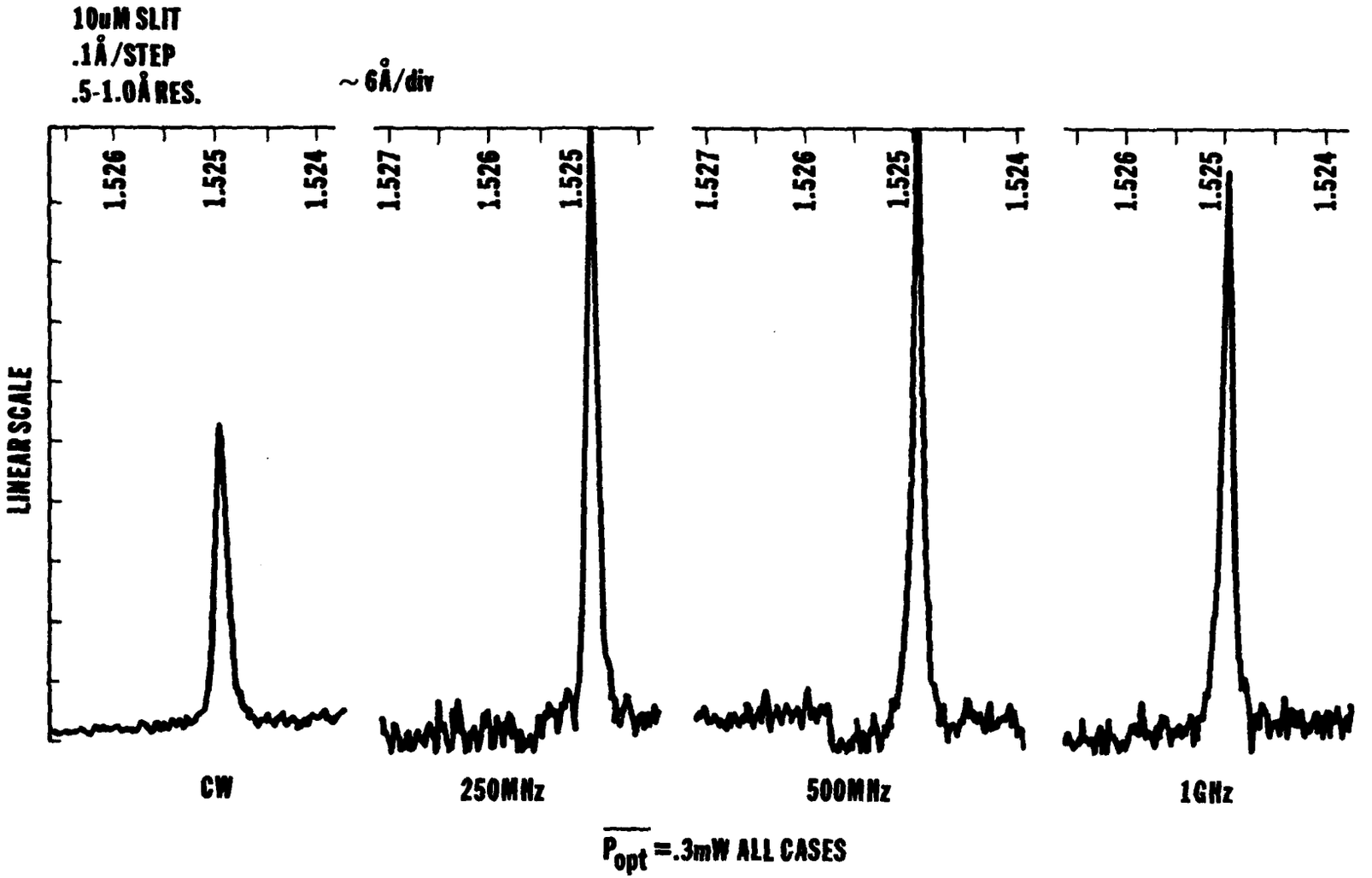


Figure 3.3.5-28. Spectral response on a linear scale at 0.3-mW average power output and cw, 250-, 500-, and 1000-MHz modulation.

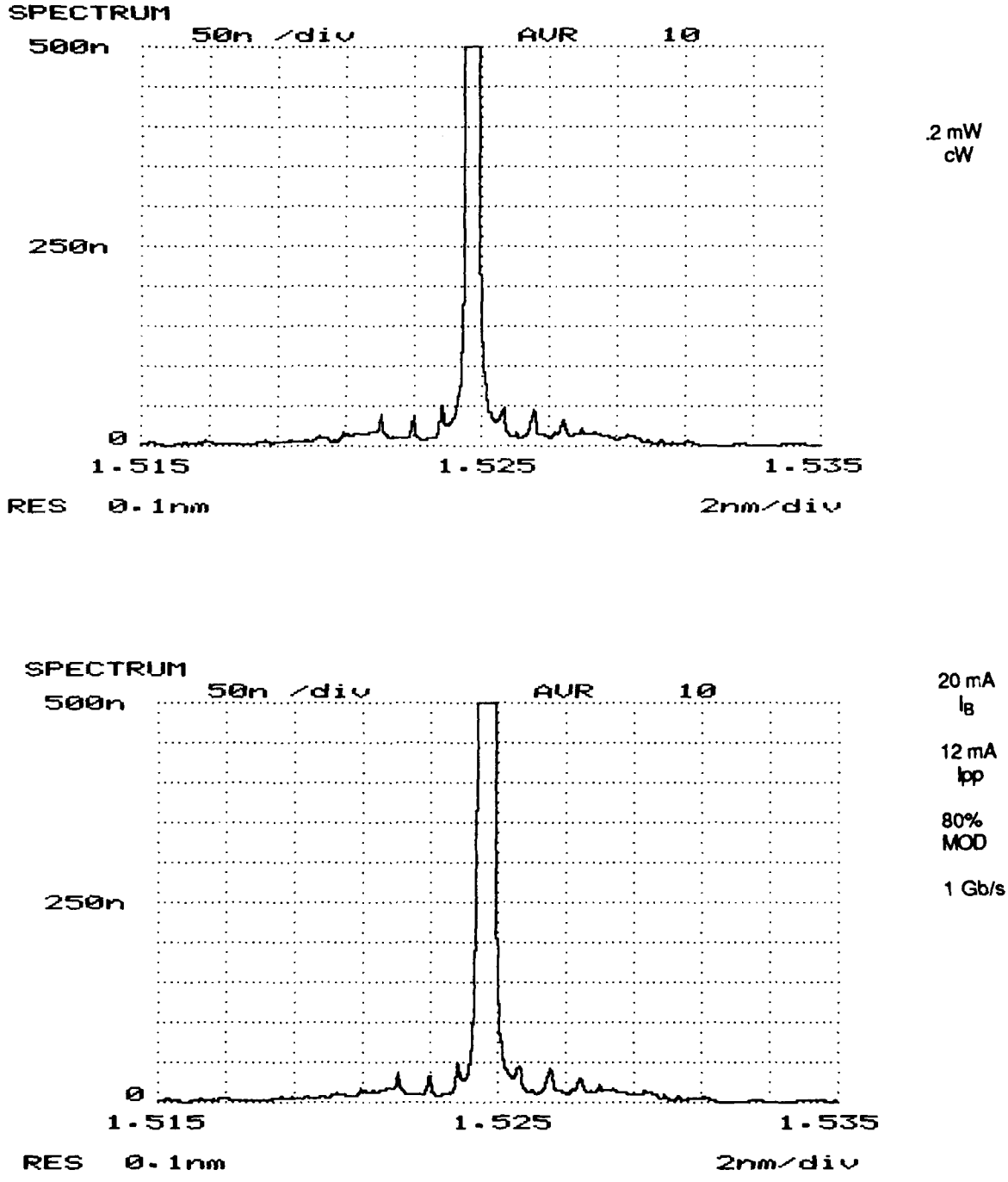


Figure 3.3.5-29. Spectral response on a linear scale, with 0.2-mW, cw output (top) and 1 Gbit/s NRZ at 80% modulation depth (bottom).

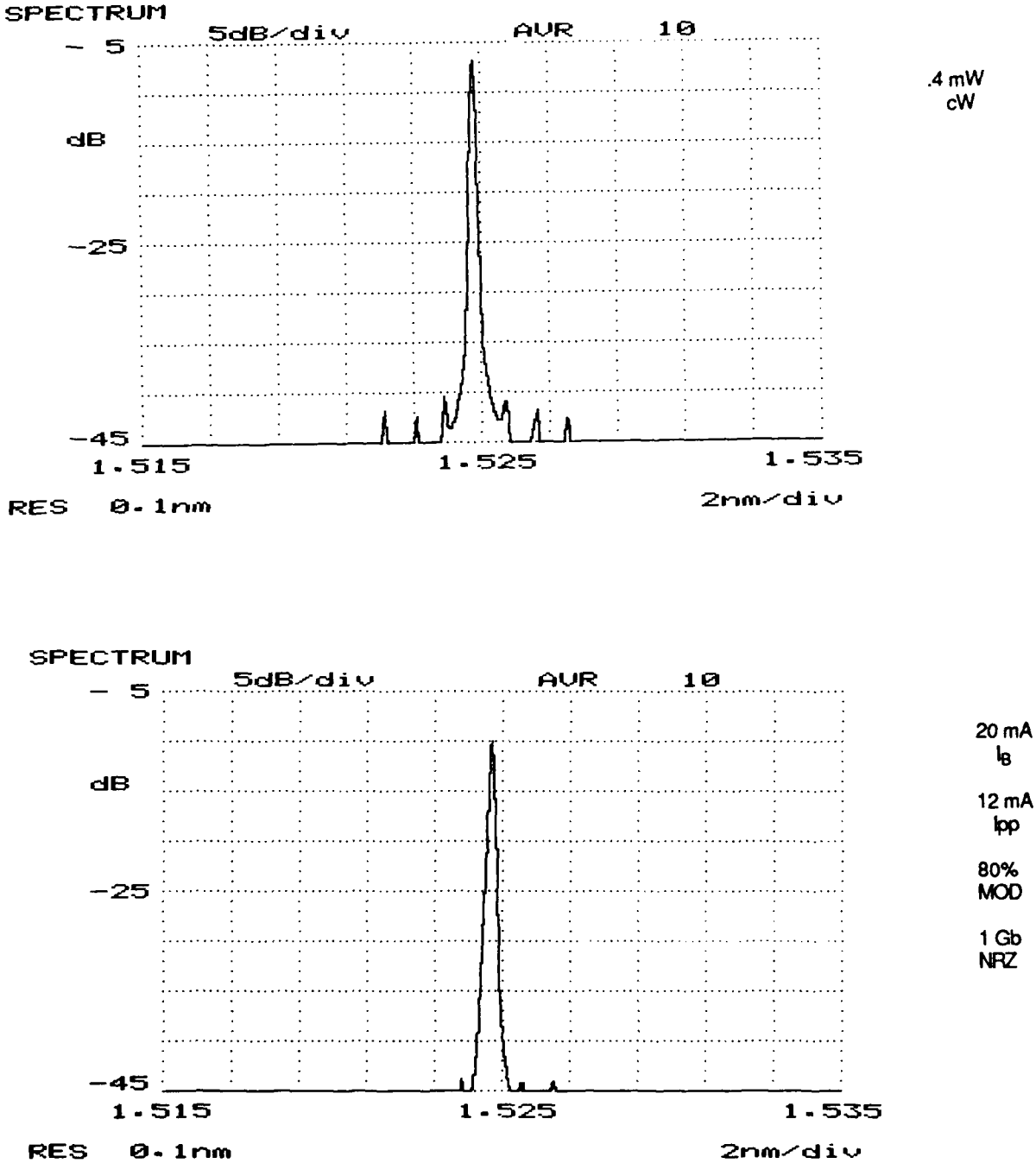


Figure 3.3.5-30. Spectral response on a log scale, with 0.4-mW, cw output (top) and 1 Gbit/s NRZ at 80% modulation depth (bottom).

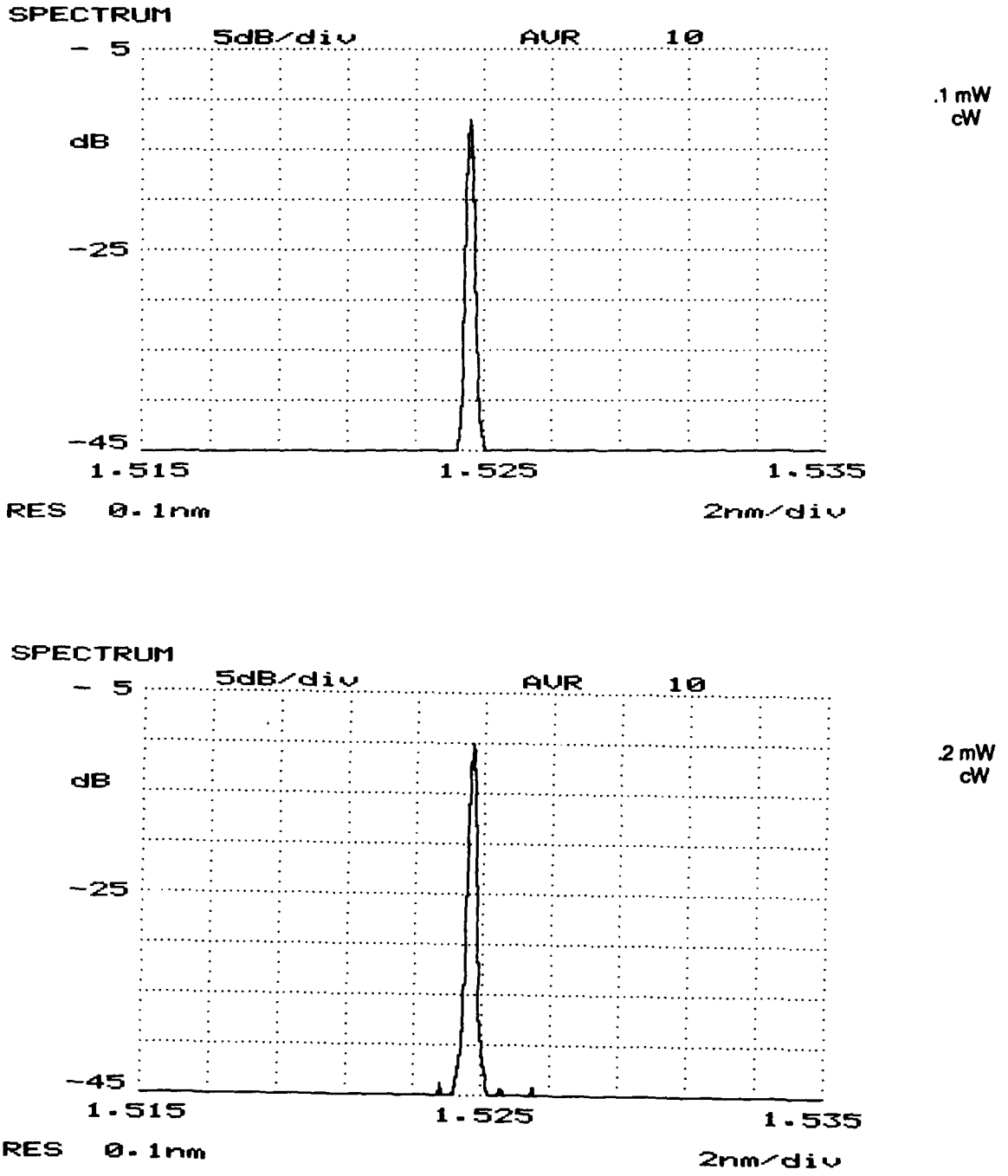


Figure 3.3.5-31. Spectral response at cw on a log scale, with 0.1-mW (top) and 0.2-mW (bottom) output powers.

Broadly speaking, the desired features of the lasers are low levels of spurious longitudinal modes and lack of broadening under modulation. Thirty dB suppression of spurious modes is a typical benchmark. The devices examined all appeared capable under these guidelines. The two best Lasertron units made up the deliverables. Linewidth broadening under modulation (spectral chirping) was not well resolved in the measurement systems used.

Conclusions

All requirements for the MFOX Level 5 transceivers were achieved in the course of this work. The major conclusion of the effort is that is is clearly feasible to construct effective units operating at frequencies up to 1 Gbit/s, using commercially available optoelectronic components. Specific problems in the availability of pinFET receivers for this frequency range are expected to be met in the on-going industrial activity toward high-bandwidth data transmission but could remain a problem unless specifically addressed in future engineering development.

The work carried out on the development of the transeivers confirms that the basic performance required is within the scope of commercially available GaAs digital logic circuits for both transmitters and receivers. Discrete devices used to drive the lasers could be replaced with IC logic gates if the laser drive currents for a particular device type are sufficiently low (< 20 to 25 mA). The power dissipation of commercial chips is a serious consideration in planning engineering development of these systems.

Operation at frequencies in excess of 1 Gbit/s was achieved with the chips used. Some instabilities were attributed to the comparator unit.

Laser operation with the DFB devices was fully adequate for efficient system operation at frequencies of at least 1 Gbit/s. In fact, transmitter operation at rates up to 2 Gbit/s was achieved. The commercial DFB lasers maintained their wavelength stability under modulation. Temperature stabilization of the chip was adequate to maintain wavelength control and stability, but the reliability of this operation remains to be investigated.

The major technical limitation for high-frequency transceiver operation is in the availability of a suitable broadband pinFET receiver. Since no commercial devices were available, we undertook the development of a custom unit. Its performance was adequate to demonstrate 1 Gbit/s operation as required. However, the critical dependence of the bandwidth on the bandwidth control

voltage would be a serious handicap in the development of reliable engineering units.