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Final Technical Report
February 1989



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MULTIPURPOSE FIBER OPTIC TRANSCEIVER (MFOX)

RCA Corporation

M. Howell, J. Cohen, J. Price, J. Connelly, M. Savoie, F. Lang

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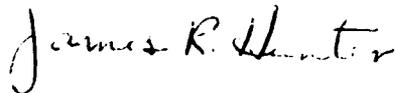
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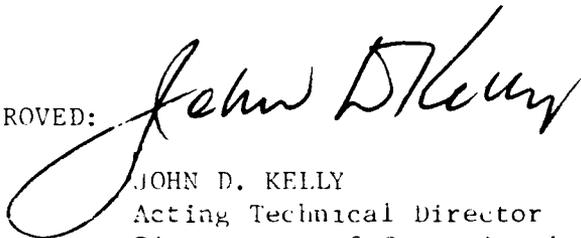
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19. ABSTRACT (Continue on reverse if necessary and identify by block number) This report describes the family of fiber optic transmitters/receivers developed under the MFOX program. The intent of the program was to define, design, fabricate and test a minimum sized family of common module, fiber optic transceivers, which would satisfy a majority of current and future military point-to-point communications requirements. Levels 1, 2 and 4, described in Volume 1 have been designed, fabricated and tested to Mil-Qual specifications. The capabilities of these three links are described in detail in this report and provide digital transmission from 1 kbps to 50 Mbps interfacing multiple electrical levels (i.e. RS-232, Mil-Std-188-114, TTL, ECL) for maximum utility. 10 MHz analog video capability is also provided by utilizing Level 2 transceivers with peripheral modulators and demodulators. These units use LED emitters in the transmitters and pin-fet receivers which have been tested through rigorous burn-in and environmental test procedures to meet Mil-Qual for tactical Ground-Mobile environment. To fill out the MFOX family, two laser based transmitter/receiver links were fabricated to an experimental, feasibility level. These transceivers are (see reverse)					
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described in Volume II and provide digital transmission from 50 Mbps to 1 Gbps along with a 70 MHz IF analog interface. The 1 Gbps transceiver has been fabricated using single longitudinal mode DFB lasers and GaAs based circuitry.

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1.0 Introduction

1.1 RCA under contract F30602-83-C-0142 has demonstrated the feasibility of a family of MFOX fiber optic components to address ground-based tactical communication needs. An earlier study included a survey and basic definition of a family of eight modules. These modules have been developed to the Advanced Development Model (ADM) level under this program to address current needs. Future needs are addressed with two types of Experimental Model (EM) Transceivers.

1.2 Both the ADM's and EM's were developed with the advantages of participative Design Reviews attended by a number of governmental activities. The active participation and support of Rome Air Development Center and the NASA Langley Research Center have been very beneficial to the outcome of this program. The support and capabilities of GE/RCA Aerospace and Defense activities in Camden and Moorestown, New Jersey, the David Sarnoff Research Center (now a part of SRI) at Princeton, New Jersey and the New Products E/O Division at Vaudrioul, Quebec combined to make this a successful program.

1.3 This Final Report is composed of two Volumes. Volume I will provide general overall coverage of both the Advanced Development Model (ADM) effort as well as the Experimental Model (EM) effort. Volume I will concentrate on the ADM effort, namely MFOX Levels I, II and IV. Volume II will concentrate on the EM effort, namely MFOX Levels III and V.

2.0 Technical Summary

2.1 MFOX Family Concept

The guiding principle underlying the design approach for MFOX is

that the needs of military communications with fiber optics can best be met by the development of families of components that meet the requirements of virtually all current and anticipated applications. This principle is realized in the MFOX family of fiber optic transceivers. With MFOX, developers of military fiber optic communication systems with requirements for ground-based point-to-point links will have available standardized, off-the-shelf fully military qualified components for the critical transmitter and receiver functions. Through designs based on the overall family concept, the designer will be assured that one or several configurations within the family will meet the requirements of the applications with state-of-the-art performance. As technology capability advances, new units will be added to the family while maintaining compatibility with the earlier components.

Within the MFOX program, two categories of units were developed to address near-term and future needs. Advanced Development Models (ADMs) address present and near-term requirements. In design, packaging and fabrication they have been carried to the point of development needed for transfer to engineering for manufacture.

Performance, environmental and quality assurance testing confirms the capability of the designs and their suitability to harsh military environments. Engineering Models (EMs) address future needs with breadboards that achieve the performance capabilities of advanced optoelectronic components and designs suitable for tactical environments. Packaging and fabrication issues are not addressed for these units.

For maximum cost-effectiveness and system utility, the MFOX

family of fiber optic transceivers was organized into five levels of function and performance during the first phase of the MFOX program. This organization was based upon a comprehensive survey of current and future military requirements in ground-based tactical communication requirements. The resulting levels have the following capabilities:

Level 1. The Phase 1 survey of current and potential military users of fiber optic ground links showed that a large fraction (48%) require only low digital data rates and relatively short transmission distances. Level 1 provides these users with a very versatile and economical transceiver set. It can transmit data at rates from essentially zero to 10 Mbit/s (Manchester or NRZ) with no constraint on the data format or duty cycle. The electronic data interfaces and alarms provide essential functions with minimum power consumption, volume and cost. Cost is also reduced by limiting the optical power and receiver sensitivity to that needed by the anticipated users as determined by link analysis with various types of fiber and connector loss characteristics. 1.3 μ m edge-emitting LED optical sources and InGaAs pin-FET detector-preamplifiers are the optoelectronic components.

Level 2. Some users (13%) require significantly higher digital data rates and longer ranges than could be accommodated by the Level 1 transceivers. For these users the Level 2 transceiver units are available. They transmit data from 200 Kbit/s to 50 Mbit/s (Manchester or NRZ). The transmission range is increased to the limit of the capability of LED sources and pin-FET receivers by design trade-offs which include emitter device selection for highest power, detector-preamplifier optimization for sensitivity and receiver design

for maximum threshold detection efficiency. These trade-offs require transmission data with a relatively constant duty cycle (near 50% at the low frequency limit), such as Manchester-encoded data. A set of encoder/decoder modules are provided to support this requirement up to 12 MHz if the input data is not Manchester by converting NRZ-formatted data to a Manchester line signal for transmission. Complete interface and alarm functions are included in the transceiver units.

Level 3. While the user survey showed that MFOX Levels 1 and 2 using LED technology could together meet all present digital requirements, projected future needs call for higher data rates and optical powers. Laser diode emitters are needed to support these requirements. MFOX Level 3 provides digital transmission capability from 50 Mbit/s to 400 Mbit/s and analog transmission at 70 MHz with a 20 MHz bandwidth. A 1.3 μm laser diode and high-bandwidth pin-FET detector are used. The data rates go to the upper limits of the fastest available standard ECL logic.

Level 4. Analog transmission of surveillance video and radar display signals were shown by the user survey to be a major application area for fiber optics (37% of users). The MFOX Level 4 provides for transmission of such signals with a video bandwidth of up to 10 MHz. The line signal for transmission is a frequency modulated pulse train (Pulse Frequency Modulation or PFM). This line signal is transmitted by using the Level 2 transmitters and receivers as the fiber optic interfaces. Modules are provided for conversion between the AM analog inputs and outputs and PFM line signals which are used by the Level 2 transceivers as though they were standard digital signals.

Figure 2.1-1

MFOX Transceiver Family Architecture

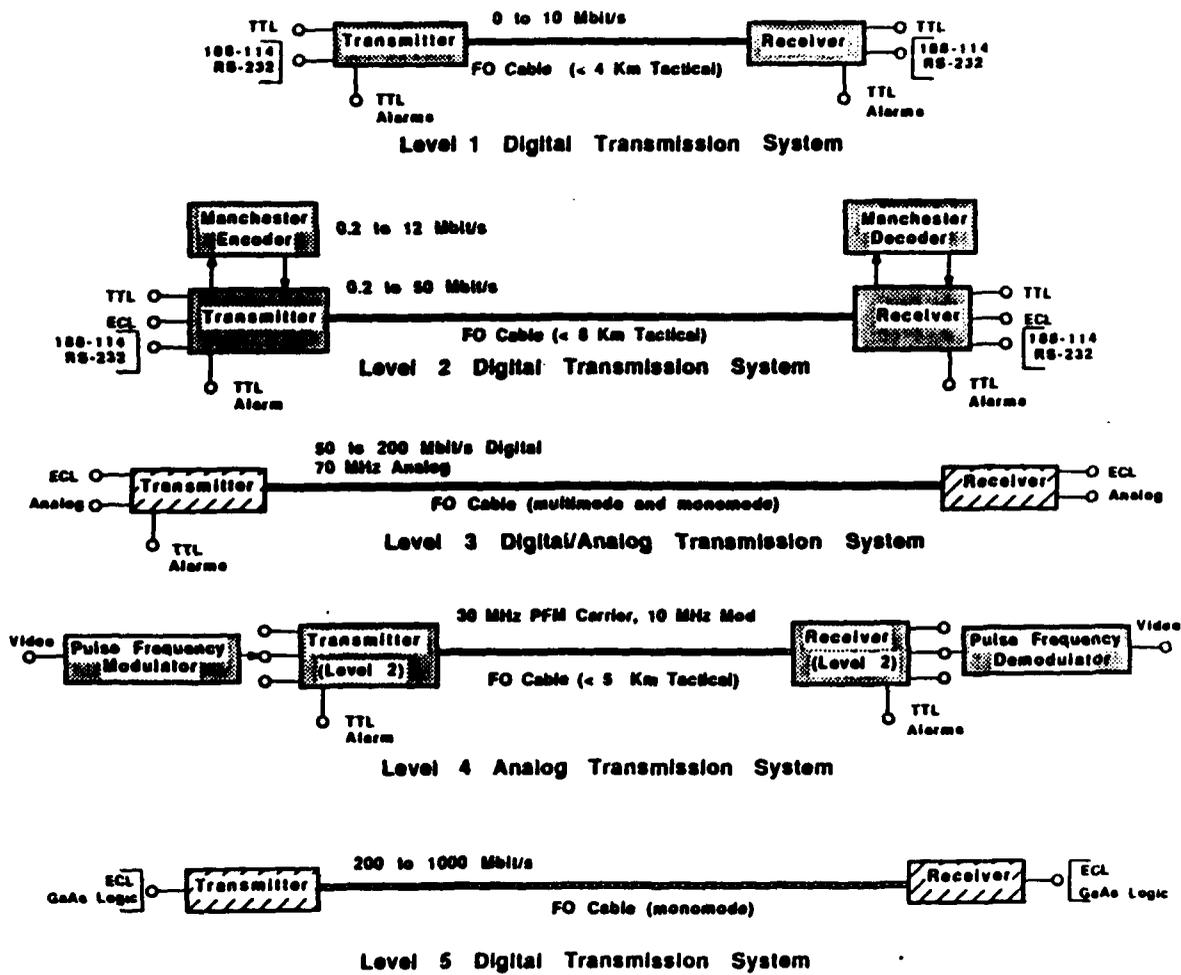
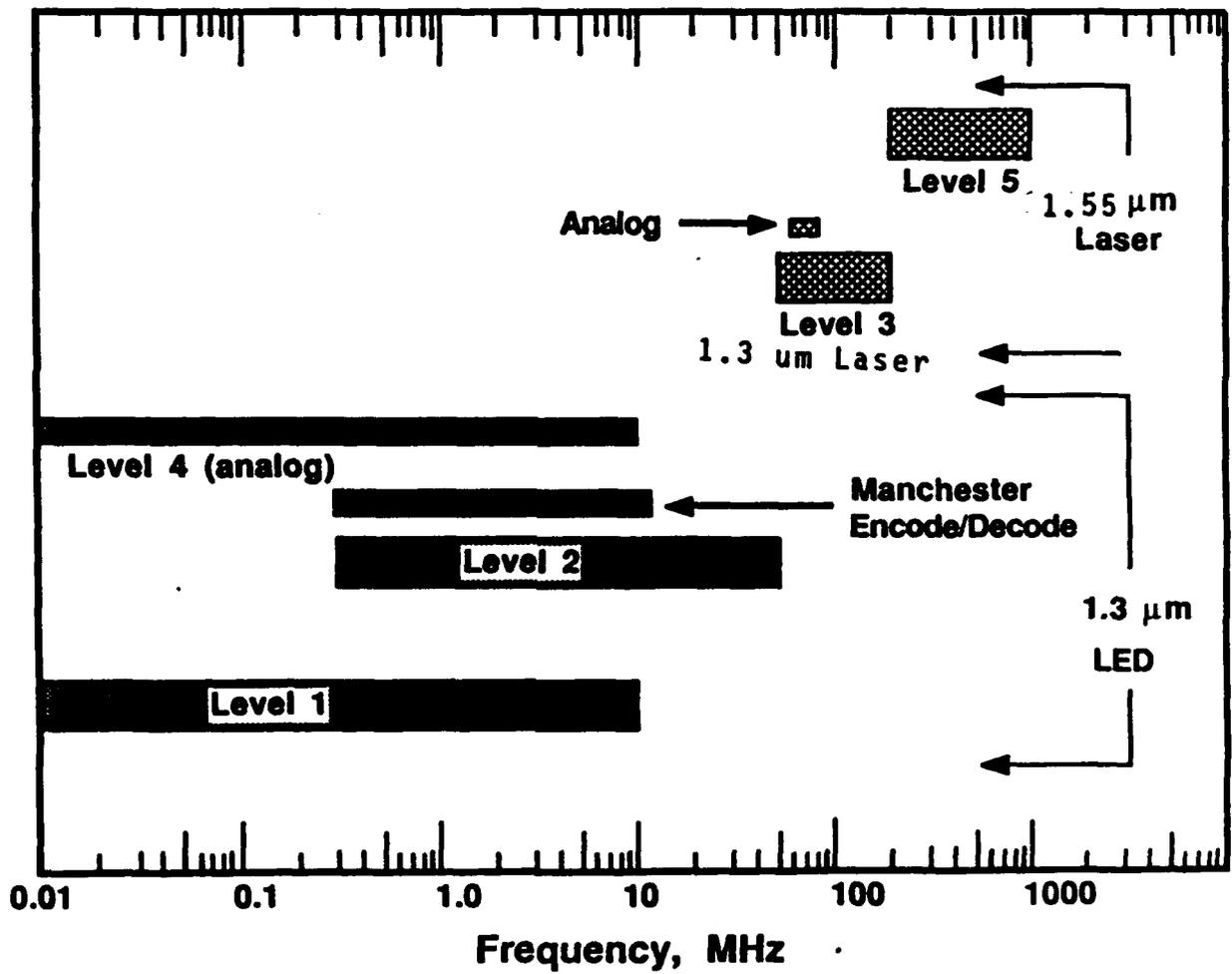


Figure 2.1-2

MFOX Transmission Frequencies



Level 5. Future applications are expected to call for digital transmission at very high data rates that are at the limits of the capability of present electronic and optoelectronic technology. Level 5 addresses these needs by providing transceivers with digital data rates from 200 Mbit/s (NRZ) to 1000 Mbit/s (NRZ). These units use high-speed GaAs logic in place of conventional silicon technology. The laser diodes and detectors are specially selected for operation at the high data rates, in some cases being RCA developmental devices.

In the second phase of development covered by this report, Level 1, 2 and 4 have been developed as ADMs and Levels 3 and 5 as EMs. The capabilities and architecture of the MFOX transceiver family are summarized in Figures 2.1-1 and 2.1-2. Figure 2.1-1 shows the structure of the MFOX family with an indication of the capabilities of each family element. The maximum link lengths indicated are only estimates, since they depend on the performance of optical fiber and connectors as well as that of the transceivers. Figure 2.1-2 shows graphically the spectrum of frequencies spanned by the MFOX transceivers.

The design of high performance military qualifiable transceivers to serve diverse applications in tactical field environments poses some unique technical issues. These issues were resolved in the MFOX development program as follows:

1. Wavelength choice. Fiber optic transmission is carried out in three optical wavelength bands corresponding to relative minima in the loss of glass optical fiber: 0.80 - 0.86 μm , 1.2 - 1.3 μm and 1.5 - 1.55 μm . Fiber loss in these bands is typically as low as 3 dB/Km, 0.5 dB/Km and 0.2 dB/Km, respectively. However, the performance,

demonstrated reliability and present availability of optoelectronic emitters and detectors is currently better for the first two wavelength bands than for the longest wavelengths. The modulation bandwidth of typical optical fiber is a maximum at 1.3 um because of the minimum in the optical dispersion of silica glasses at this wavelength.

Tactical fiber optic links are made up by connecting 1 Km lengths of cable with demountable connectors. The loss due to these connectors is in the range of 1 to 1.5 dB. The overall loss of a cable assembly will be determined by connector loss even if very low loss fiber is used. Long haul systems using installed fiber would benefit significantly in terms of maximum range from the use of the lowest loss fiber.

Analysis of the link requirements uncovered by the user survey showed that the performance capability of 1.3 um fiber optic systems was adequate to meet the extreme link lengths required. Operation at 1.55 um would offer no significant improvement in connectorized tactical systems because the connector loss dominates fiber loss, and would be a detriment in high data rate systems due to reduced transmission bandwidth of the fiber. However, the introduction of single longitudinal mode lasers based on Distributed Feedback (DFB) designs provides a means of overcoming this limitation, and this technology is incorporated in the Level 5 EM development.

The conclusion is that operation in the 1.3 um wavelength band is the best choice for the MFOX system, except for extreme long range installed fiber applications. Specific wavelength ranges will be determined in the final specifications by trading off details of fiber

loss and dispersion characteristics, LED and laser emission characteristics, the impact of these on system performance, and overall cost-effectiveness. The use of short wavelengths for short range, low data rate applications was considered, but the advantages to system designers and users of having a common transmission wavelength for the whole MFOX family (except for future advanced Level V development) was found to outweigh any component-cost factors favoring short wavelengths for these limited applications.

2. Electrical Signal Interfaces. The ultimate usefulness of the MFOX transceivers depends as much on their electrical interfaces and functions as on their optical performance. For signal interfaces the options range from providing a single serial input or output at one standard logic level (as is done in most commercial units) to incorporating full signal processing and multiplexing. The former approach yields the simplest and most inexpensive units, but places the burden on the system designer to adapt the interfaces of the overall system to the transceivers. The latter offers more flexibility at the cost of much more expensive, bulky and power consuming transceiver units.

This issue was addressed in detail during the phase 1 study. We found that many candidate retrofit systems, such as radar remoting, for MFOX transceivers do not provide or accept signals in the form that can go directly into a fiber optic link. Multiplexing of parallel digital data and treatment of analog signals is required. For the phase 1 study we made engineering estimates of the serial data rates that would result and that the transceivers would have to accommodate. Newer systems and systems under early development,

however, generally are designed to deal with broadband serial data and contain the necessary multiplexing and data conversion circuits. All systems show a great diversity of signal levels, formats and data rates.

Developing a relatively universal interface, while technically feasible, was found to be more of a limitation than an advantage for the MFOX family. No completely universal interface is possible, and it would be difficult to identify and fully characterize every candidate application. The large volume and power consumption of the resulting unit would prevent it from being used as a simple component. The cost would be much greater than that of simpler transceivers, and this cost would be paid by the many users that had no use for its universal interface. Therefore, approaches involving signal multiplexing as part of the transceivers were rejected.

Other interface features that increase the flexibility of the units and the ease of using them in diverse systems were found to be practical and cost-effective, so were incorporated into the MFOX family. Each unit accepts all of the standard signal levels appropriate for the data rates involved, including MIL-STD-188-114 and RS-232. Each unit spans a wide range of data rates or analog bandwidths. Data format and duty cycle are unlimited in the Level 1 units. In the Level 2 units the duty cycle is restricted by performance considerations to approximately fifty percent, but modems are provided for converting arbitrary format data to and from a Manchester format. These modems are pin-programmable to operate at any frequency from 0.2 MHz to 12 MHz. Data format conversion at higher frequencies can be done with fixed-frequency modems (not

provided) that connect to the Level 2 transceivers in the same way as the modems provided.

3. Transmitter Optoelectronic Performance. MFOX transmitters must operate over the wide temperature range (specified for MFOX as -46 °C to +52°C) experienced in tactical applications but are designed to achieve output signal powers and maximum modulation rates near the capability limits of the 1.3 um LED and diode laser devices used. Output signal parameters must be held within tight constraints over all operating conditions so that system performance can be reliably predicted. These requirements are met in the Level 1, 2 and 4 ADM programs through temperature compensation of optical output, careful thermal analysis of the transmitter packaging, and development of a special LED emitter component. The Level 3 and 5 experimental development programs are directed toward exploring the use and specification of laser transmitters for the same kinds of tactical conditions.

The Level 2 transmitters are specified at output powers and modulation bandwidths that require careful choice of the LED technology. InGaAsP edge emitting LEDs have significant advantages over surface emitters in terms of fiber-coupled output power and modulation rate. Their liabilities are a more rapid decrease in output power with increasing temperature and a tendency to develop lasing action at low temperatures, which were addressed by a special series of tests and device selection criteria developed by the RCA New Products Division. Careful testing of modulation and power characteristics enabled us to select edge-emitter wafer material best capable of meeting the MFOX requirements, which could not be achieved

with surface emitters. Control of the temperature-dependent characteristics of these devices was handled through component, circuit and transmitter packaging design.

Optical transmitters that must operate over a wide temperature range or at high ambient temperatures often include thermoelectric coolers in a temperature stabilization circuit to maintain the emitter chip at constant temperature. This approach was rejected for the MFOX Level 1 and 2 transmitters because of the power requirements for such coolers and the large increase in volume and weight that the current supply for the coolers would impose on the modules. Instead, LED emitter chips are designed for operation over a wide temperature range and selected during manufacture for suitable output characteristics at low and high temperatures. This selection includes elimination of lasing at low temperature and maintenance of power at high temperatures. The LED driver circuit controls the drive current to maintain output power within specifications over the entire MFOX temperature range.

4. Receiver Optoelectronic Performance. The sensitivity and dynamic range of the receiver complement the transmitter power and power variation in determining overall performance. MFOX receivers use InGaAs pin photodiodes in low-noise circuits with a GaAs FET first stage (pin-FET) to give high sensitivity. The preamplifier circuit has a transimpedance feedback loop to achieve high dynamic range and avoid the need for equalization filters that would necessarily be data rate and format dependent. Such receivers have sensitivity that depends on their bandwidth as shown in Figure 2.1-3.

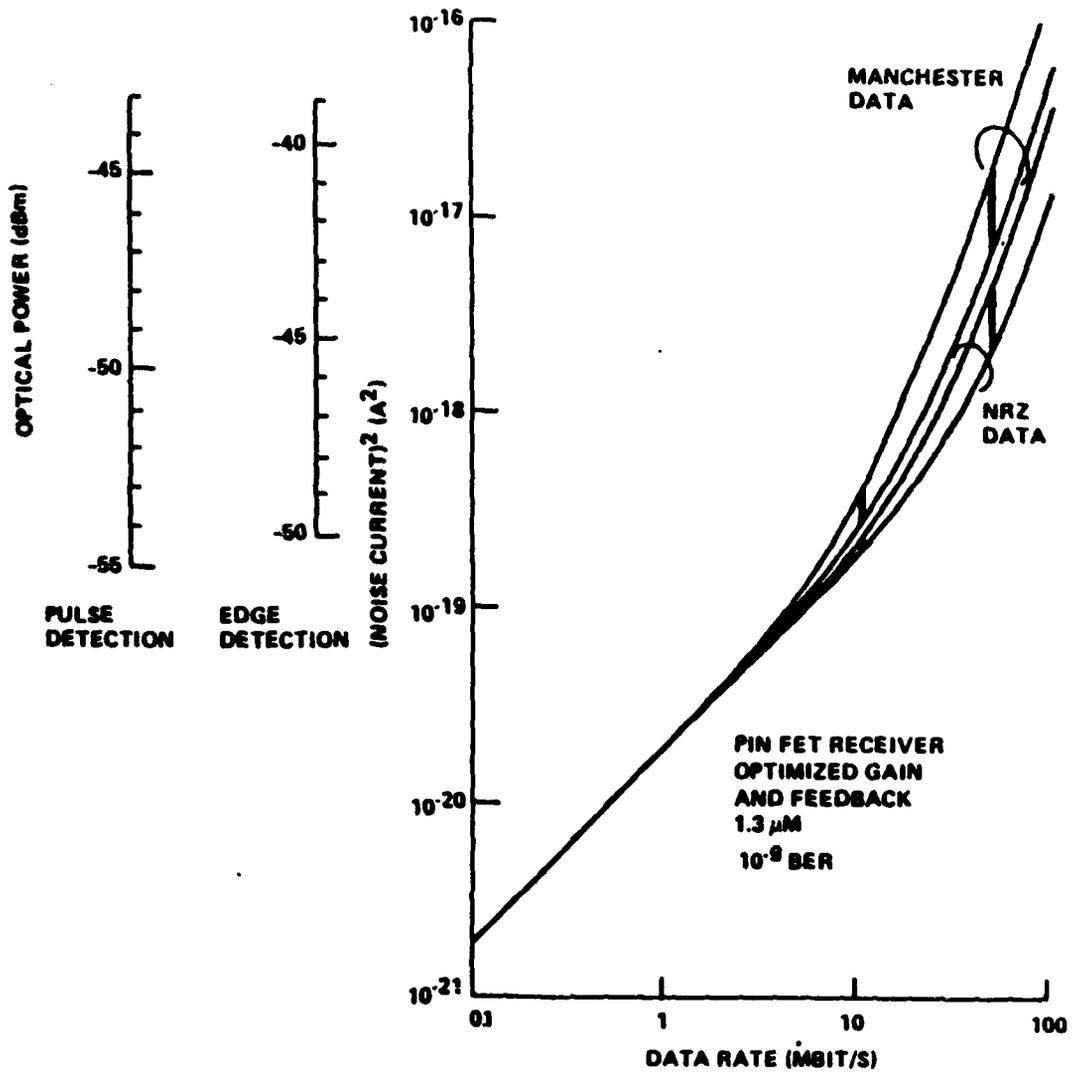
In designing the MFOX family architecture a trade-off was made

between the use of many receiver types, each optimized for a particular narrow range of the data rates, against fewer types with more compromise in sensitivity. The major guide in making this trade-off was the goal of meeting the full requirements of all the application systems identified in the program phase 1 study. This goal was almost completely achieved using the breakdown in data rates adapted.

Data format capabilities also affect receiver sensitivity and dynamic range. Data detection circuits based on edge detection of differentiated pulse waveforms can operate independently of the data format and at very low duty cycles, but impose at least a 4 dB penalty on receiver sensitivity. Pulse detection makes full use of the energy in the data stream, but requires that the data format avoid long intervals of constant signal level. Figure 2.1-3 shows the relative sensitivity of these two detection methods. In the MFOX family, Level 1 receivers use edge detection for data format independence, while Level 2 uses pulse detection for greatest sensitivity.

The major objective of the Level 3 EM designs was to establish a feasible approach for using diode laser based transceivers to achieve higher data rates in tactical equipment. Diode laser operation over the specified temperature range is accomplished through two alternate modes of operation. One of these makes use of a thermoelectric cooler to hold the laser chip at a constant temperature despite ambient temperature excursions. The other mode eliminates the thermoelectric cooler and makes use of an optical sensor driven feedback circuit to maintain constant optical output despite temperature changes. This latter mode eliminates the high current

2.1-3 Relative Sensitivities of Pulse Detection and Edge Detection



drain and thermal dissipation problems of thermoelectric elements. Digital operation up to 400 Mbit/s NRZ (200 Mbit/s Manchester) approaches the performance limits of available high speed ECL silicon bipolar digital circuits. An alternate 70 MHz analog channel for accommodating a FM carrier is also provided.

Level 5 EM transceivers were developed to demonstrate the maximum performance capabilities for units based on the most advanced optoelectronic and electronic devices available. Data rates exceeding 1 Gbit/s are achieved using GaAs digital integrated circuits and discrete FET devices. Optoelectronic performance commensurate with these speeds is accomplished with 1.55 μm single longitudinal mode diode lasers in high frequency packages. The only noncommercial component is the receiver pin-FET detector/preamplifier, which was not available commercially and developed as a custom hybrid component for the MFOX program.

2.2 Description of ADMS

2.2.1 Level 1 System

System Level 1 consists of two discrete units, a transmitter and a receiver. These units are small, lightweight and compact for the transmission of digital data in fiber optic point-to-point links. The units are powered by +5 V and -5.2 V DC from a host system. An alarm feature is provided to the host system as an aide in determining proper or improper data transmission. In the case of improper operation, the alarms when correctly interpreted, will indicate the source of the malfunction. Figure 2.2.1-1 provides a summary of Level 1 electrical and optical technical specifications. The system operates at data rates from 1.0 Kbps to 10 Mbps at link lengths to 4 Km.

The Level 1 transmitter and receiver are component size units. Their sizes and weights are shown in Figure 2.2.1-2. The mounting dimensions and envelope dimensions except for height are the same for both units. The transmitter and receiver are housed in aluminum cases having a black anodize finish. Four mounting holes located on the case flange allow #6 screw attachment. Gold plated feedthru pins exit the sides of the case to provide the electrical interface. The pins are .064 mm square right angle contacts on .254 cm centers. The optical hookup is made via a connectorized pigtail. The connector is an industry 906 series SM-A type.

Electrical

Supplies:

Transmitter: +5V @ 265 mA typ/-5.2V @ 100mA typ.

Receiver: +5V @ 135mA typ/-5.2V @ 35mA typ.

Data Interfaces:

Balanced TTL and MIL-STD-188-114 @ 1Kbps (NRZ) to 10Mbps (Manchester).
Unbalanced TTL @ 1Kbps (NRZ) to 1Mbps (Manchester).

Unbalanced MIL-STD-188-114 and RS-232C @ 1Kbps NRZ to 100Kbps (Manchester). No coding constraints on any interface. Interfaces are enabled and disabled by programming a TTL compatible Select bit.

Alarm Outputs:

Transmitter Interface Alarm: All alarms are TTL compatible triggered by improper interface operation or below specification data inputs.

Transmitter LED Alarm Triggered by open circuit emitter.

Transmitter Combined Alarm Triggered by either the Interface or LED Alarms.

Receiver Alarm Triggered by faulty receiver operation or below specification optical input.

Optical

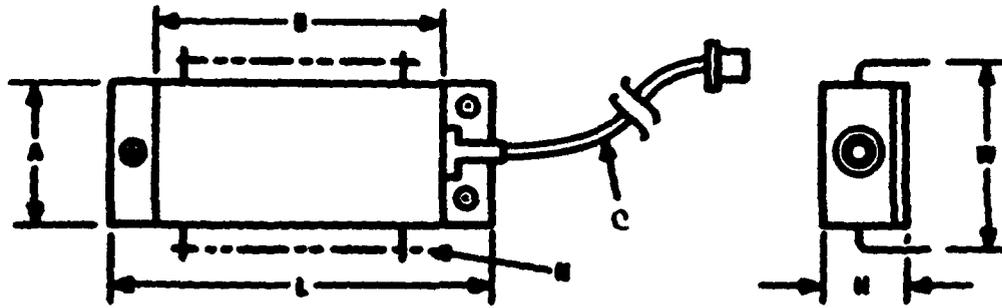
Transmitter Peak Optical Power: 25uW min/50uW max. over operating temperature range.

Wavelength: Peak = 1300nm \pm 3nm FWHM = 60nm typ.

Receiver Sensitivity: -34dBm min.

Receiver Dynamic Range: 15dB min.

Figure 2.2.1-1 Level 1 Transmitter and Receiver Specification Summary



PHYSICAL CHARACTERISTICS - MFOX TRANSCEIVER UNITS

	A cm.	B cm.	W cm.	L cm.	H cm.	WL L	N Pins	C
L1 Transmitter	3.56	11.86	4.06	13.38	1.45	117	16	Bushing with 1 meter optical fiber pigtail terminated in SMA-style connector
L1 Receiver	3.56	11.86	4.06	13.38	1.70	113	14	
L2 Encoder	4.57	9.96	5.08	11.48	1.09	82	22	NO PIGTAIL
L2 Decoder	5.59	11.23	6.10	12.75	1.09	115	26	
L2, L4 Transmitter	4.57	13.34	5.08	14.86	1.45	149	32	Bushing with 1 meter optical fiber pigtail terminated in SMA-style connector
L2, L4 Receiver	4.57	13.34	5.08	14.86	1.70	158	24	
L4 Modulator	4.57	9.96	5.08	11.48	1.60	94	18	NO PIGTAIL
L4 Demodulator	5.59	11.23	6.10	12.75	1.60	122	18	

Figure 2.2.1-2

2.2.2 Level 2 System

System Level 2 consists of several discrete units; a transmitter, a receiver, an encoder and a decoder. These units are small, lightweight and compact for the transmission of digital data in fiber optic point-to-point links. The transmitter and receiver may operate in a standalone configuration or with the encoder and decoder units when data format alteration is desired for optimum transmission. In links transmitting data of arbitrary format, encoder and decoder units must be installed to alter the format to Manchester. The encoder and decoder operate at data rates of 0.2 Mbps to 12 Mbps and the transmitter and receiver operate at data rates of 0.2 Mbps to 50 Mbps at link lengths to 8Km. The transmitter and receiver provide alarm signals to the host system as an aide in determining proper or improper operation. When correctly interpreted, the alarms will indicate the source of any malfunction. Figure 2.2.2-1 provides a summary of the Level 2 Transmitter and Receiver technical specifications and Figure 2.2.2-2 provides a summary of encoder and decoder specifications.

The Level 2 transmitter and receiver, encoder, and decoder are housed in aluminum cases having a black anodize finish. The size and weights of the units are shown in Figure 2.2.1-2. Mounting holes located on the case flanges allow #6 screw attachment. Gold plated feed-thru pins exit the sides of the case to provide the electrical interface. The pins are .064 mm square right angle contacts on .254 cm centers. The optical hookup for the transmitter and receiver is made via a connectorized pigtail. The connector is an industry 906 series SMA type.

Electrical

Supplies:

Transmitter: +5V @ 325mA typ/-5.2V @ 340mA typ.

Receiver: +5V @ 325mA typ/-5.2V @ 340mA typ.

Data Interfaces:

Host System Interfaces: Balanced TTL and MIL-STD-188-114 @ 0.2Mbps (NRZ) to 12Mbps (Manchester) Unbalanced TTL @ 0.2Mbps NRZ to 1Mbps (Manchester). Balanced and Unbalanced ECL @ 0.2Mbps (NRZ) to 50Mbps (Manchester). All data must be 50% duty cycle format. Interfaces are enabled by programming TTL compatible select bits.

Encoder/Decoder Interfaces

Unbalanced TTL data and clock @ 0.2Mbps (NRZ) to 12Mbps (NRZ). Balanced ECL Manchester encoded data @ 0.2Mbps to 12Mbps.

Modulator/Demodulator Interfaces

Balanced ECL at 20MHZ to 40MHZ.

Alarm Outputs:

All alarms are TTL compatible.

Transmitter Interface Alarm:

Triggered by improper TTL or MIL-STD-188-114 interface operation or below specification TTL or MIL-STD-188-114 data inputs.

Transmitter Encoder/ECL Alarm:

Triggered by improper or below specification ECL interface operation including encoder and modulator ECL inputs to the transmitter.

Transmitter LED Alarm

Triggered by open circuit emitter

Transmitter Combined Alarm

Triggered by the Interface Alarm, the Encoder/ECL alarm or the LED alarm.

Receiver Alarm

Triggered by faulty PINFET or Threshold circuits or below specification optical input.

Figure 2.2.2-1 Level 2 Transmitter and Receiver Specification Summary

Decoder Alarm

Triggered when the receiver is programmed for Decoder operation and improper or faulty Decoder to Receiver data interfacing occurs.

Figure 2.2.2-1 Level 2 Transmitter and Receiver Specification Summary
(Continued)

Combined Alarm	Triggered by the Receiver Alarm or the Decoder Alarm.
<u>Optical</u>	
Transmitter Peak Optical Power:	50uW min/100uW max over operating temperature range.
Wavelength:	Peak = 1300nm +3nm FWHM = 60nm typ
Receiver Sensitivity:	-40dBm min.

Figure 2.2.2-1 Level 2 System Specification Summary (Continued)

Electrical

Supplies:

Encoder:	+5V @ 95mA typ/-5.2V @ 120 mA typ.
Decoder:	+5V @ 120mA typ/-5.2 V @ 350 mA typ.

Transmitter/Receiver Interface:	Unbalanced TTL data and clock @ 0.2 Mbps (NRZ) to 12 Mbps (NRZ). Balanced ECL Manchester encoded data @ 0.2 Mbps to 12 Mbps.
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Control Inputs:

Encoder	3 frequency select inputs program the Encoder to 6 frequency ranges from 0.2 to 12 Mbps. 1 control sets the input clock-to-data phase relationship.
Decoder:	7 frequency select inputs program the Decoder in 20 frequency ranges from 0.2 to 12 Mbps. 1 control input sets the output clock-to-data phase relationship.

Figure 2.2.2-2 Level 2 Encoder and Decoder Specification Summary

2.2.3 Level 4 System

The Level 4 Modulator and Demodulator provide a means to send wideband analog signals over a fiber optic link using the Level 2 transmitter and receiver which usually carry digital data. Although primarily intended to carry monochrome surveillance and radar video, it is capable of high quality transmission of any of the color television signals commonly used throughout the world. Good linearity allow the system to carry television and radar video with multiple subcarriers.

Optional input/output coupling modes and flat or pre-emphasized signal processing allow the system to carry a wide variety of other analog signals that are within the 1.5 volt peak-to-peak amplitude range and the DC to 10MHZ frequency range. Figure 2.2.3-1 provides a summary of Level 4 technical specifications.

As with the other units, the Level 4 modulator and demodulator have an anodized aluminum case construction. The size and weights of the units are shown in Figure 2.2.1-2. Four mounting holes located on the case flange allow #6 screw attachment. Gold plated feed-thru pins exit the sides of the case to provide the electrical interface other than analog. The pins are .064 mm square right angle contacts on .254 cm centers. Electrical interface for analog signals is accomplished via a case mounted SMA connector per MIL-C-39012/61.

Electrical

Host System Analog Interface:

Input/Output Signal Amplitude:	1.5V pk-pk max.
Input/Output Impedance:	75 \pm 3 Ohms
DC Coupled Frequency Response:	DC to 8MHZ = +1dB DC to 10MHZ = -3, +1dB
AC Coupled Frequency Response	5HZ to 8MHZ = +1dB 2HZ to 10MHZ = -3, +1dB
Differential Gain Distortion	10% max.
Differential Phase Distortion	5 Deg. max.

Carrier Frequency:

AC Coupled:	30MHZ typ.
DC Restored	29.1MHZ typ.
Frequency Deviation	\pm 10MHZ max.
Transmitter/Receiver Interface:	Balanced ECL

Figure 2.2.3-1 Level 4 System Specification Summary

3.0 Design

3.1 Not Used

3.2 Generic Considerations

3.2.1 Advanced Development Modules

3.2.1.1 Electrical Concept

The eight MFOX ADMs are designed to be easily integrated into a multiplicity of systems requiring point-to-point transmission of information. Certain common design goals were implemented in every unit for increased flexibility and ease of use. This modular concept facilitates system integration of the ADMs.

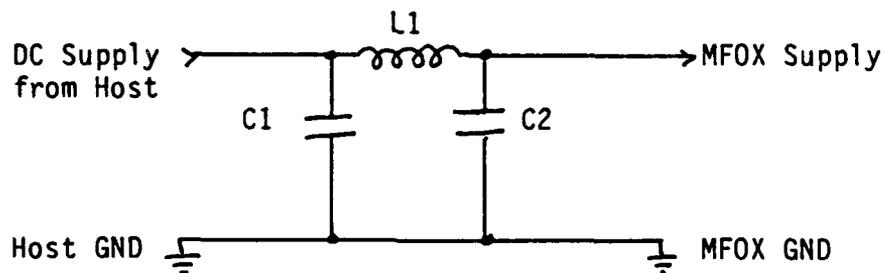
The MFOX ADM family common electrical concepts include a minimum number of supply voltages, similar EMI protection and reduction designs, test points for the isolation of faults and similar reliability, maintainability and safety design goals and implementation techniques.

3.2.1.1.1 Voltage Requirements

The Level 1 Transmitter, Level 1 Receiver, Level 2 Transmitter, Level 2 Receiver, Level 2 Encoder and Level 2 Decoder all require just two supply voltages. These are +5V and -5.2VDC. The Level 4 Modulator and Level 4 Demodulator require -5.2V, -12V and +12V DC. System Levels 1 and 2 therefore require only two different supply voltages while System Level 4 requires just four voltages. This minimization to a few standard voltages eases host system power supply requirements.

3.2.1.1.2 Conducted Susceptibility and Emissions

The MFOX design emphasizes the minimization of conducted emissions and susceptibility between the MFOX system and the host equipment power supplies. All power inputs are isolated from the MFOX circuitry by a two-pole inductive-capacitive filter. A filter circuit was chosen as the isolation mechanism because it meets unit size and weight requirements unlike more elegant but size-increasing solutions such as regulators or transformer isolation. Filter components were selected to minimize resonant frequency peaking (Q) and the voltage drop between the host power supplies and the MFOX circuitry and to maximize the attenuation of unwanted transients. A typical filter circuit and sample filter component values are shown in Figure 3.2.1.1.2-1. Filter component values vary from unit to unit. Details of each are provided in 3.3.



Sample Component Values: C1 = 0.1 μ F
C2 = 6.8 μ F
L1 = 50 μ H

Figure 3.2.1.1.2-1 Representative Power Supply Filter Circuit

Full benefit is derived from the filters when the MFOX units power supply returns are well-grounded. Mounting the units on a ground plane and tying signal ground to this plane for example, maximizes filter attenuation. Less desirable is a long return to power supply ground. Long lead lengths contribute inductance in the return path and provide a means for the pick-up of unwanted radiation. Conducted emissions and susceptibility testing was performed and is described in 4.0.

3.2.1.1.3 Radiated Susceptibility and Emissions

Several techniques common to the eight ADMs can be implemented to reduce radiated susceptibility and emissions. The unit cases can be grounded through two case mounting holes and two case pins to the host system's shield ground. Each unit case is isolated from signal ground, allowing the users maximum flexibility when shielding and grounding the system. All units can be operated with termination resistors at all data interfaces, thus reducing further undesirable interactions between host equipment and MFOX equipment. Radiated EMI testing results are discussed in 4.0.

3.2.1.1.4 Alarm Test Points

Although all alarm test points are contained in the transmitters and receivers, fault isolation to any unit is possible. The MFOX system is designed to aid the user in trouble shooting and detecting a failed condition anywhere in the link.

3.2.1.1.5 Reliability, Maintainability and Safety

ADM performance in these areas is covered as separate Contract Data Requirements List (CDRL) items. Consult CDRL B007 Reliability and Maintainability Allocations, Assessments and Analysis Report and

CDRL B008 Reliability and Maintainability Data Reporting and Feedback, Failure Summary Report for Reliability and Maintainability information. Consult CDRL B004 System Safety Hazard Analysis Report, CDRL B005 System Safety Engineering Report and CDRL B009 Safety Assessment Report for Safety information.

3.2.2 Mechanical Concept

The mechanical design of the ADM's was optimized to meet the challenging goals and requirements set forth by the Phase 1 Study and Subsequent Development Specification. The major emphasis was to maximize the utility of the MFOX units for multiple Air Force applications. A number of configurations were identified for both new and retrofit designs (see Figure 3.2.2-1). The greatest utility is seen where the units can be treated both as a printed circuit component and a stand alone.

3.2.2.1 Size

A primary design goal for maximum utility of the MFOX ADM's in multiple applications was to achieve printed circuit component sizes. The predominant factor influencing the size of the units is the electrical circuit packaging technique employed. A number of schemes were considered. Although resulting in the smallest size, LSI was not chosen due to the developmental lead time required and the small quantities involved. Conventional glass epoxy printed wiring was not considered after area studies indicated this approach would result in circuit areas two to three times that needed with a thick film ceramic approach. Other reasons pointed to thick film ceramic on ceramic technology as the best choice for circuit packaging. Leadless hermetic chip carrier (LHCC) packages screened to MIL-STD-833C and MIL

approved passive chip components were readily available. Further size reductions could be realized where necessary with subhybrid packaging. Testing is at the device level. Automated production facilities are in place for high volume build. For the above reasons LHCC ceramic on ceramic construction was chosen for the MFOX circuit design. Chip and wire thick film was also considered but not chosen because of the expensive assembly level test fallout and the increasing availability of parts for the LHCC approach.

Other factors influenced the size of the units. The need for modular and removable partitioned circuits adversely affected the size to a small degree. This was considered a positive trade-off in the interest of optimum circuit performance and maintainability.

3.2.2.2 Minimize Form Factors

In order to convey the notion of a transceiver family, commonality of design was stressed for the eight different unit types. During the layout of the top assemblies, efforts were accordingly made to minimize the case outline and mounting dimension variations. Dimensions were brought into agreement when small non-critical size increases would result.

3.2.2.3 Weight

Minimizing the weight of the units was another goal for maximizing utility in multiple applications. This is especially important for printed wiring board implementation where units having a large mass can cause excessive deflections during dynamic loading. This goal was met by employing thick film ceramic circuit technology for the circuit packaging which resulted in component size units. In addition to size, another significant determinant of weight was the

choice of outer case material. Weight was a contributing factor in the choice of aluminum over the other metallic materials considered, which included stainless steel, kovar, and copper. The weights of the units are shown in Figure 2.2.1-2. None of the weights, all less than 160 grams, would be considered excessive for printed circuit applications. In addition, the securely fastened units provide significant stiffening to limit damaging deflections of the host printed wiring board.

3.2.2.4 Grounding/Shielding

The packaging design employs the best grounding and shielding practices. The outer case of the units is aluminum to provide EMI and tempest protection. The aluminum has a non-conductive hardcoat finish allowing the unit to be mounted to a surface at any potential or noise level without degradation of the electrical performance. The case provides a true Faraday shield for the internal circuitry, i.e., the case is completely decoupled from any signal grounds routed internally. Signal ground returns through at least one isolated outer case feed-thru pin. Two pins other than signal ground are tied to the case to provide shield ground termination. The user is also given the option of strapping the case to the host frame or chassis by employing lugs with the hardware at two flange mounting holes where the non-conductive finish is masked. On the modulator and demodulator, the SMA coax connector is isolated from the outer case to avoid coupling of case ground and signal ground which is routed through the connector body.

The external exposure of the case feed-thru pins represents a compromise of the tempest and EMI integrity but was necessary to

enable printed wiring board implementation. Some shielding of the contacts may be necessary in high radiated noise environments or tempest sensitive situations.

Internally, the layout design of the ceramic circuit substrates provides adequate grounding and shielding practices for proper operation of the circuitry. Ground grids have been provided with the thick film construction. The electro-optic modules in the transmitter and receiver are packaged in gold plated kovar cases, which provide the necessary shielding for these circuits. The electro-optic module cases are floating (i.e. not tied to internal signal ground) where they come in contact with the outer case.

3.2.2.5 Maintainability

An early maintainability study indicated that the units were to be repaired. Considered were the cost of the units and subassemblies, logistics, repair capabilities, subassembly interchangeability and the developmental nature of the program. Accordingly, the packaging design made maintainability a goal.

Circuit partitioning in the transmitter and receivers had electrical performance as the primary consideration, but maintainability was also a goal. The electro-optic circuits in both the transmitters and receivers were separated into two modules. These modules in addition to the interface ceramic circuit assemblies are replaceable. The other MFOX units contain one removable ceramic circuit assembly. All subassemblies are accessible after removal of a screw attached lid.

Few repair operations require special tools. Any soldering operations can be accomplished with a low wattage soldering iron. No

wire bonding is required. Although not considered part of the maintainability plan for the MFOX units, repairs can be made to the ceramic circuit assemblies following removal from the case.

Performing ceramic circuit assembly repairs requires special tools, processes, and personnel training. The only other repair operation which may require special tools, is replacement of the fiber optic connectors. The connector termination procedure is provided in the instruction books, CDRL B017.

3.2.2.6 Hermeticity

Hermeticity is provided at the device level in the MFOX units. This was dictated by many aspects of the design. Thick film ceramic circuit packaging of the interface circuitry employs LHCC and subhybrid construction. Circuit partitioning and shielding requirements suggested the opto-electronic modules be contained in hermetically sealed kovar cases. Hermeticity could not be provided at the outer case because of maintainability requirements and the decision to use an aluminum alloy material.

3.2.2.7 Connectors

The MFOX transceivers were designed to be modular elements of any equipment which employs them. Accordingly, a connectorized interface for all electrical and optical I/O was seen as a necessity.

Choosing a modular electrical interface for both printed circuit and panel/bulkhead applications appeared to be a conflicting design requirement. Employing a case attached subminiature rectangular connector would be optimum for panel/bulkhead applications but could not be solder terminated to printed wiring boards. The right angle outer case feed-thru pin provide a workable interface for both

situations. The pins extend below the case mounting surface for solder termination to printed wiring boards. Also, the gold plated contacts are spaced on .254 cm centers allowing engagement with many available board and cable connectors. The I/O pins are retained in headers which are bonded into a pocket machined in the side walls of the case. Individual clearance holes are drilled completely through at the pin locations. The drilling of these holes, although requiring additional precision machining than a thru-slot, is necessary for the EMI/Tempest design.

The analog signal interface for the Level 4 modulator and demodulator is provided by a case attached SM-A coax connector per M39012/61. This is the Mil Qual connector generally employed with small component size form factors.

Optical hookup for the transmitters and receivers is accomplished via a fiber optic connector terminated to a one meter pigtail. Determining which available connector best suited the MFOX application was a significant engineering task due to the developing nature of the fiber optic industry and lack of standardization. Four candidates were evaluated on a number of performance characteristics. The industry style 906 series SMA connector was chosen for reasons which included the following:

- Insertion losses do not exceed those allowed by the system optical power budget.
- The military specifications being developed for single terminus fiber optic connectors were establishing a SMA configuration.

- Data was available collaborating compliance to MFOX environmental requirements.
- The SMA 906 series connectors were readily available.

3.2.2.8 Environmental Design

3.2.2.8.1 Low Temperature

Several risks were identified during the design phase of the program. Three were related to the fiber optic link. There was no existing data showing the optical fiber and connector termination could survive down to -46°C . Confidence testing was performed on two jumper cables connectorized at both ends and coupled together with an SMA adapter. Confidence testing was performed on the cables and coupling by passing a signal through the link which was monitored at low temperature. The testing showed no significant loss of optical power at -46°C or during temperature cycling between -46°C and $+52^{\circ}\text{C}$. A second low temperature risk for the optical link was mismatch and distortion of the optical alignment mechanisms internal to the PINFET and LED. This was especially critical for the latter which requires precise alignment of the LED die and fiber. The optical output of the LED die at low temperature was another issue. The current to the LED is regulated by a temperature compensation circuit. An oversupply of current at low temperature when the LED becomes highly efficient could cause lasing. The optical alignment and lasing issues were addressed by the New Products Division in their design and resulted in successful low temperature and temperature cycling confidence testing of the first transmitters and receivers assembled at GCSD. The risk of thermal and mechanical stressing of the interface ceramic circuit assemblies (CCA's) at low temperature was thought to have been retired

after successful confidence testing of the engineering evaluation units (EEU's). This returned as a problem however, during low temperature exposure of the ADMs in burn-in temperature cycling. The CCA's have a sandwich construction consisting of the thick film ceramic circuit bonded to an aluminum plate. The adhesive used must not only provide the bond strength, but also mechanical isolation of the ceramic substrate. A compliant adhesive will do this by converting the relative displacements of the two adherends to strain energy. If the adhesive is not compliant enough, backing plate displacements not accommodated by adhesive strain will induce stressing of the ceramic. Relative displacement of the backing plate with respect to the ceramic substrate can occur mechanically, by installation of a bowed CCA and thermally by an expansion coefficient mismatch. A combination of these added to cause microcracking of the ceramic substrates on some units. The adhesive used was a .013 cm thick rubberized epoxy preform, which was not sufficiently compliant at low temperature. Two corrective actions were implemented. The first was to change to a thicker and more compliant silicone adhesive. This better isolated the ceramic substrate, thus reducing the stresses induced by displacements of the backing plate. Also, the backing plate is now fixtured during the bonding process to reduce the CCA camber and resultant mechanical stressing during installation. No micro-cracking has occurred since the adhesive material and bonding process change were implemented.

3.2.2.8.2 High Temperature

The MFOX units are designed to operate in a maximum ambient of 52°C. With the low power dissipated by the MFOX circuits, maximum

allowable microcircuit chip and passive component junction temperatures are not approached at worst case. Operation at 52°C can pose a potential problem, however, for the LED which experiences optical power degradation with increasing temperature. This is discussed in paragraph 3.3.2.3.

3.2.2.8.3 Humidity

All exposed materials and finishes chosen for the MFOX units had existing data supporting their ability to withstand continuously humid environments. No related failures occurred during Qual testing.

3.2.2.8.4 Altitude

Typically vulnerable at high altitude might be the hermetic eutectically sealed leadless hermetic chip carriers and opto-electronic modules. All seals were subjected to fine and gross leak testing during component burn-in prior to incorporation into the MFOX circuits. No failures occurred during Qual testing.

3.2.2.8.5 Vibration

The internal construction of the MFOX units consists of ceramic circuit and printed wiring assemblies having low mass and extremely high natural frequencies, making them impervious to vibration loading. Any internal wiring routed near hardware or other chafing surfaces were strapped. Susceptibility of the pigtail termination of the opto-electronic module cases was eliminated by strain relief provided at the outer case (see paragraph 3.3.1.3.3).

3.2.2.8.6 Shock

Shock testing of the MFOX units consisted of a two meter drop onto all faces, edges and corners of the transit configuration (26 drops). Protection is provided by the transit packing

design. The units are restrained inside a box with urethane foam. This cushion has a natural frequency several orders of magnitude below those characteristic of the internal MFOX unit construction. Also, the shipping box is made of ductile cardboard which absorbs much of the impact energy.

3.3 Design Description

3.3.1 Level 1 Transmitter and Receiver ADMs

3.3.1.1 System Link Description

The Level 1 Transmitter and Level 1 Receiver comprise the Level 1 System. Four types of interconnections between the Level 1 System and the user's host system must be provided to fully operate and monitor a fiber optic link.

- o Power Inputs from Host System
- o Data Interface Control (Select) Inputs
- o Data Signals to/from the Selected Interface
- o Alarm (Test Point) Outputs Monitored by Host System

A working link therefore includes power from the host system, programming of the select bits to activate the proper data interface, data connections to the selected interface and the monitoring of the alarm test points to detect a "failed link" condition.

3.3.1.1.1 Optical Considerations

System Level 1 is capable of transmitting digital data through up to 4Km of optical fiber. A sample link is shown in the 3.3.1.2 figure. The link capability calculations must take into account the specifications of the MFOX transmitter and receiver, the optical fiber and the optical connectors. An evaluation of the link (assuming 4 Km of tactical cable) pictured in 3.3.1.2 is provided in Figure

3.3.1.1.1-1. The total cable and connector losses are subtracted from the transmitter best and worst case power output and compared to the receiver sensitivity and dynamic range. A positive margin not greater than 15 dB indicates the link will successfully pass data at the rates and formats specified.

	For Minimum Signal (Worst Case Transmission)	For Maximum Signal (Best Case Transmission)
Connector Loss (Assume 1.5dB per connector at 4 connectors)	6dB	6dB
Cable Loss (1.5 dB/Km over 4Km)	<u>6dB</u>	<u>6dB</u>
Total	12dB	12dB
Transmitter Optical Output	-19dBm	-16dBm
Optical Input to Receiver	-31dBm	-28dBm
Receiver Sensitivity	<u>-34dBm</u>	<u>-34dBm</u>
Margin	3dB	6dB
Receiver Dynamic Range	15dB	15dB

Figure 3.3.1.1.1-1 4Km System Link Power Budget

In this example the margin is both positive and less than 15dB, indicating a successful link. Note that although the transmitter optical output is given in terms of 50% duty cycle average power, the link will work with arbitrary data formats. The average optical output is given so that a relevant comparison can be made to the receiver sensitivity which is specified in terms of average power as well. Also, only four connectors are considered in the link because receiver sensitivity is specified at the receiver pigtail's fiber optic connector.

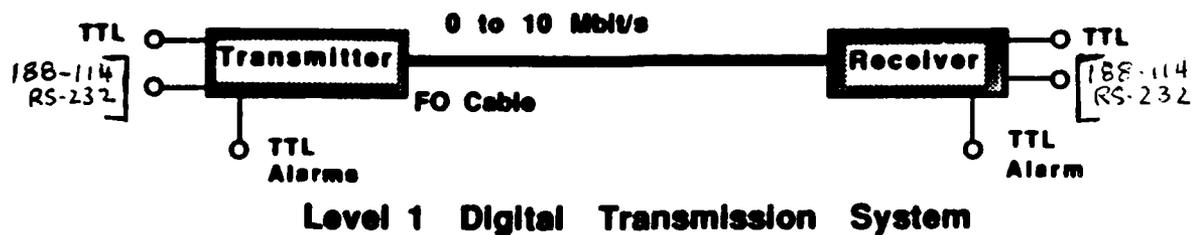
3.3.1.1.2 Alarm Considerations

Four alarm signals are made available to the host system for the monitoring of the fiber optic link. The transmitter interface alarm, the transmitter LED alarm and the receiver alarm are TTL compatible active-low outputs. The transmitter combined alarm is a TTL compatible active-high output.

An active transmitter combined alarm indicates that either the interface alarm or the LED alarm is active. The interface alarm indicates a transmitter interface failure, either part failure induced or as the result of below specification data transmission from the host system. The LED alarm indicates an emitter open circuit failure. The Receiver alarm will activate if either of the transmitter alarms activate, if improper or no optical data is reaching the receiver or if the receiver's optical detection circuitry has failed.

Isolation of any fault to the transmitter, receiver or host system is feasible given these alarm criteria.

3.3.1.2 System Diagram



3.3.1.2.1 Transmitter Description and Diagram

The transmitter consists of the Interface hybrid, the LED Driver module and the LED module as shown in the block diagram of Figure 3.3.1.2.1-1. The Interface hybrid handles all alarm signals, provides filtered power to all transmitter circuits and transmits digital data through one of two selectable interfaces from the host system to the

LED driver module. The LED Driver module modulates the LED and monitors the LED status. The amplitude of the LED current is adjusted to insure that the LED power dissipation and optical output do not exceed specifications. The LED module contains the LED and the temperature and current biasing elements.

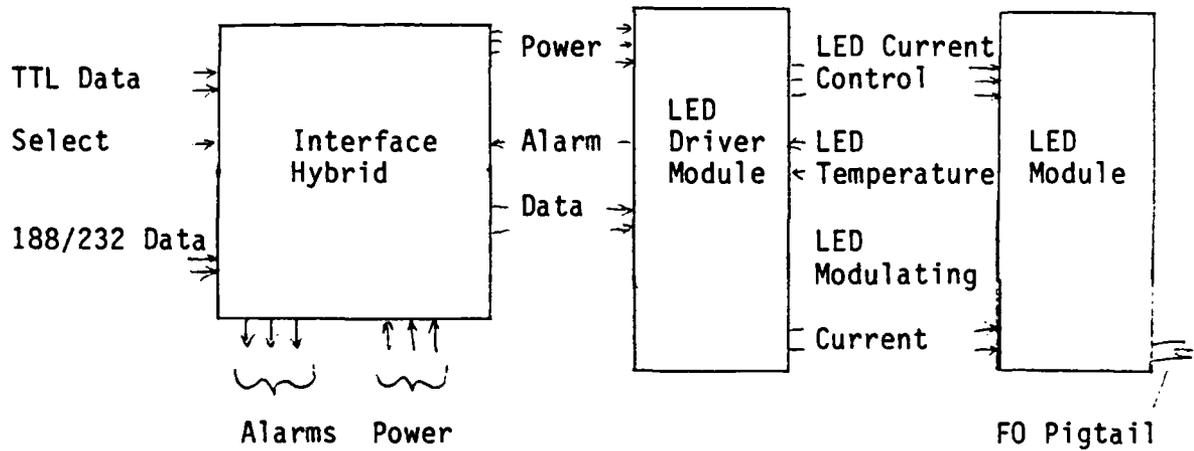


Figure 3.3.1.2.1-1 Transmitter Block Diagram

3.3.1.2.1.1 Driver and LED Assemblies

3.3.1.2.1.1.1 E/O Subsystem

3.3.1.2.1.1.1.1 Approach/Tradeoff

The initial design requirement for the Level 1 E/O subsystem was compromised in only one area. The only hard difference between the Level 1 LED driver unit and the Level 2 LED driver unit was that the Level 1 unit was specified to require a TTL data input whereas the Level 2 unit was specified to require an ECL data input. In the interest of cost reduction and development expediency, it was agreed between RCA NPD and RCA CISD to standardize on an ECL data input for both levels. This permitted the development of only one driver unit (C30625E) with the capability to drive both Level 1 and Level 2 LED's.

The chosen emitter was a standard RCA C86013E edge-emitting LED with each one put through stringent selection to ensure suitability. Each LED was characterized at -46°C to check for good linearity of output power versus forward current and at $+63^{\circ}\text{C}$ to ensure sufficient absolute output power, these being the most severe test conditions.

To avoid the entire transmitter subsystem becoming unusable in the event of fiber breakage close to the LED, it was decided to employ two packages - one for the driver and another for the LED. The LED package also contains a temperature sensor and two set resistors which are necessary to tailor the current output of a driver to the requirements of that particular LED over temperature. In this way any LED can be mated with any LED driver. Since the LED package now contained three extra components, no suitable standard package was available, consequently custom packages were designed for both LED and driver. These are the design approaches which led to the development

of an innovative transmitter subsystem built to full military standards.

3.3.1.2.1.1.1.2 Functional Description

A list of features and performance data and block diagram of the transmitter subsystem is shown below:

MFOX LEVEL 1 TRANSMITTER SUBSYSTEM PERFORMANCE

Mechanical

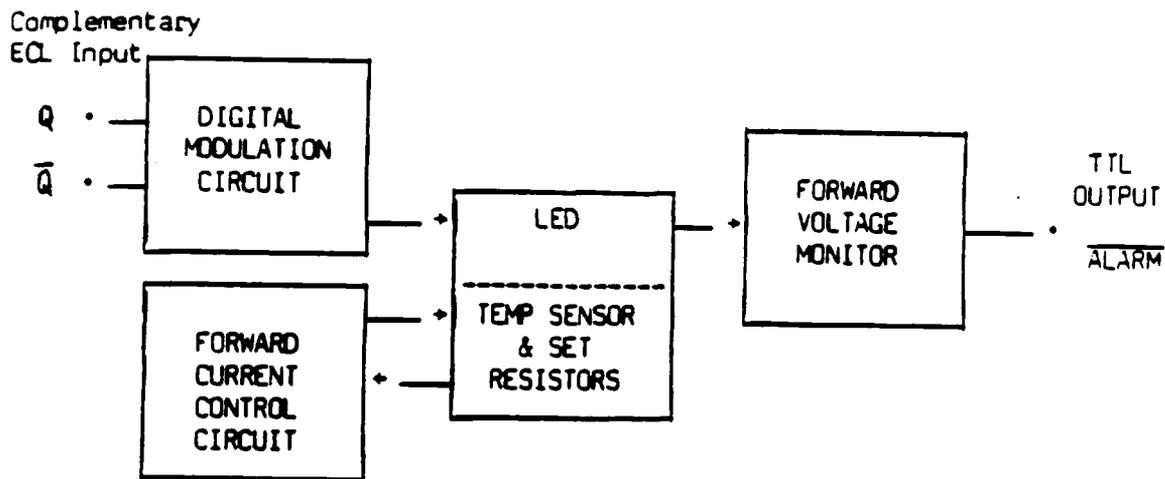
Operating Temperature Range:	-46°C to +52°C
Sealing:	Hermetic
Package Types:	Custom
Emitter:	Edge Emitting LED, RCA C86013E Chip
Fiber:	1m Pigtail of 50/125um Sumitomo EG-5/1304 or Siecor 104 fitted with Strain Relief Sleeve

Electrical

Supplies:	+5.0V @ 0.28A max/-5.2V @ 0.045A max.
Data Input:	Complementary ECL, no coding constraints, 1Kbps (NRZ) to 10Mbps (Manchester)
Alarm Output:	Triggered by open circuit emitter, TTL Compatible, active low

Optical

Peak Optical Power:	25uW min./50uW max. over operating temperature range
Wavelength:	Peak = 1300 +30nm FWHM = 60nm Typ.



The digital modulation circuit is essentially a fast level shifting circuit which converts the ECL data input to voltage levels which drive a GaAsfet, and it is this GaAsfet which turns the LED on and off. The GaAsfet operates in shunt regulation, in other words, it is connected in parallel with the LED so that switching the GaAsfet on deviates current from the LED thereby turning the LED off. Voltage across the GaAsfet when on is approximately 0.2V and appears across the LED. This is so low, however, that the LED cannot conduct and so is guaranteed to produce no light in the off state. Conversely, turning the GaAsfet off reroutes the current through the LED, and produces light. The GaAsfet switch is fast enough that on and off transitions occur in approximately 6ns which is more than fast enough for the transmission rate of the Level 1 subsystem.

The forward current control circuit is an analog circuit which takes three inputs from the LED package and defines the current flowing in the LED/GaAsfet circuit accordingly. One input is from a temperature sensor IC mounted adjacent to the LED chip and gives a

response proportional to the temperature of the chip. The other two inputs are from set resistors mounted inside the LED package. The value of these resistors is chosen during characterization of each LED so that any driver will respond to the forward current requirement of that LED as the temperature of the LED changes with environmental temperature. A knowledge of the temperature dependence of a LED is required in order to understand the operation of this circuit and this will be expanded in Section 3.3.1.2.1.1.2.

The alarm circuit has a voltage comparator as its heart and monitors the forward voltage of the LED. The output of the alarm is normally TTL high but when the forward voltage of the LED exceeds approximately 2V, indicating a damaged LED, the voltage comparator is triggered and the alarm output changes to TTL low.

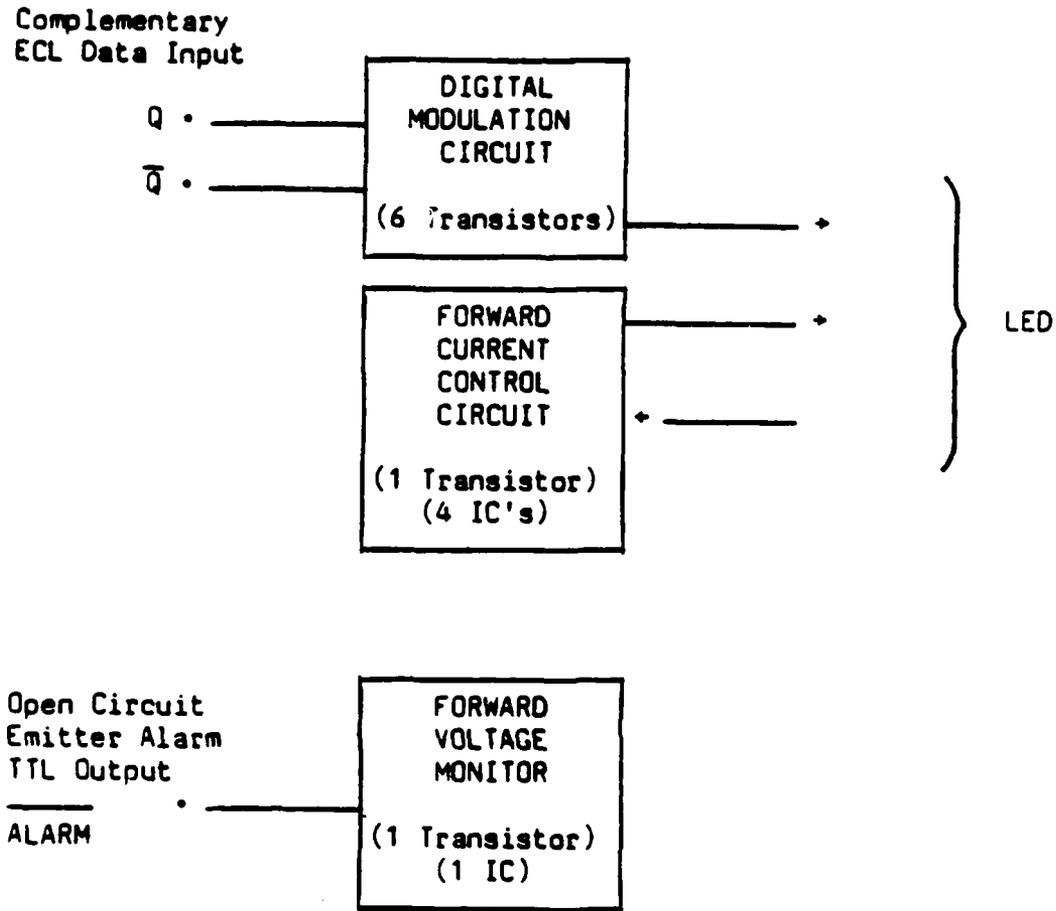
3.3.1.2.1.1.3 Special Considerations

Construction to military standards naturally required the use of high reliability components. These tend to be physically larger than the commercial equivalents and necessitated the use of larger packages than might otherwise have been the case. This, however, was accommodated with little difficulty.

Of more concern was the performance of the LED over the required temperature range. Extensive computer modelling was carried out in order to determine the operating temperature of the LED chip as a function of environmental temperature and electrical power dissipated in the chip. It was found that the chip itself would experience temperatures in the range of -46°C to $+63^{\circ}\text{C}$. The variation of LED forward current versus temperature to be applied by the driver was then designed to accommodate this temperature range.

3.3.1.2.1.1.2 Functional Description of Driver

3.3.1.2.1.1.2.1 Driver Block Diagram



3.3.1.2.1.1.2.2 Driver Function

An overall description of the digital modulation circuit has been given in 3.3.1.2.1.1.1.2, however, a few other properties are worth noting. The first stage of the modulation circuit is a long tailed pair which gives the driver some immunity to the possibility of slow transitions in the data input waveforms. The second useful property of the modulation circuit is that it is dc coupled. This extends the low end of the transmitter subsystem frequency response right down to dc which is eminently useful in both testing the subsystem and in making optical power measurements when installing the

subsystem. Lastly, the modulation circuit input stage is bipolar which, of course, makes it immune to electrostatic discharge.

The forward current control circuit is the most complex part of the subsystem and is required to stabilize the optical output power of the LED over its operating temperature range. When operated with a constant forward current, the optical power of an LED will vary with temperature as shown in Figure 3.3.1.2.1.1.2.2.1-1.

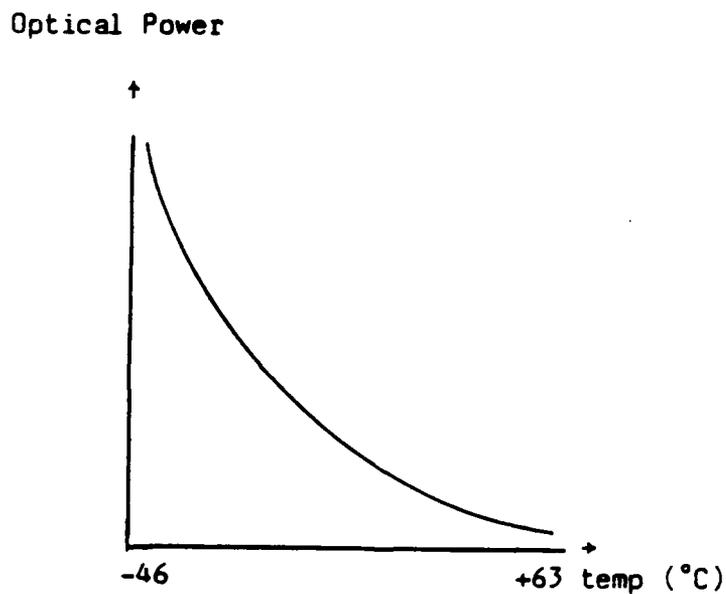


Figure 3.3.1.2.1.1.2.2-1

Or, depicted another way; to maintain a constant optical power, the forward current must be varied with temperature as shown in Figure 3.3.1.2.1.1.2.2-2.

Forward Current

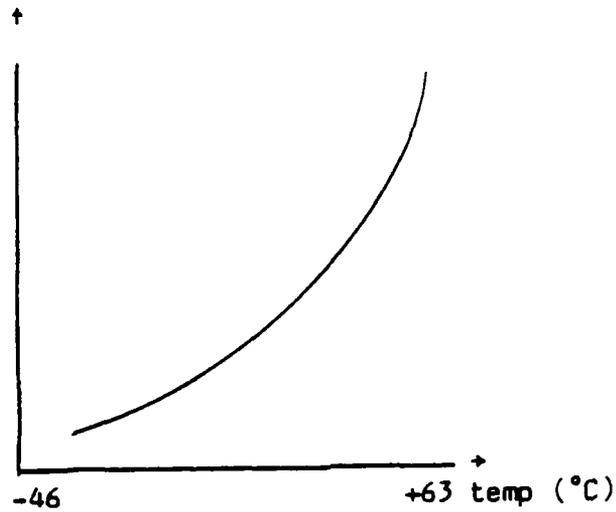


Figure 3.3.1.2.1.1.2.2-2

The curve shown in Figure 3.3.1.2.1.1.2.2-2 is rather oversimplified as it can be a complex curve and is different for each LED chip. The current control circuit performs first order stabilization by applying a linear current adjustment as shown by the broken line in Figure 3.3.1.2.1.1.2.2-3.

Forward Current

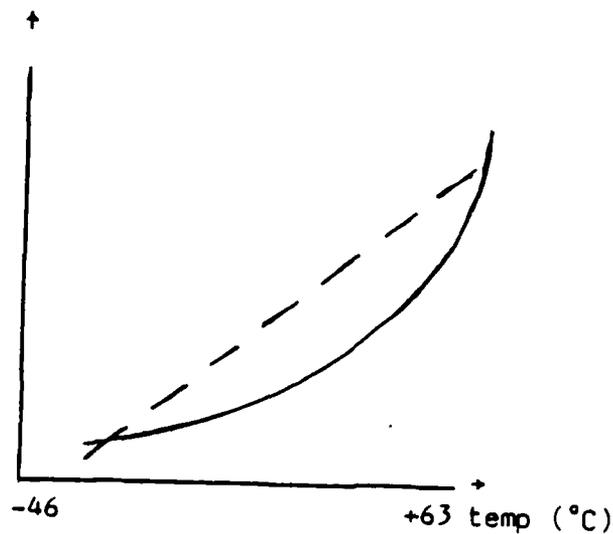


Figure 3.3.1.2.1.1.2.2-3

R_I alone defines the current as -45°C and its influence is independent of temperature as shown in Figure 3.3.1.2.1.1.2.2-5.

Forward Current

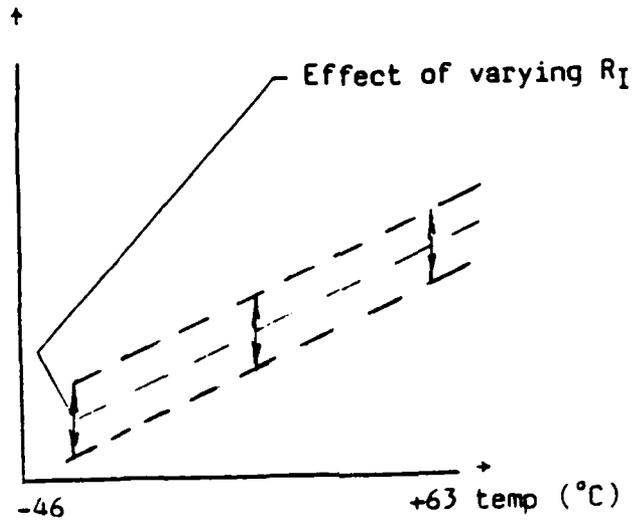


Figure 3.3.1.2.1.1.2.2-5

The effect that R_S has is to increase or decrease the temperature coefficient of the forward current as shown in Figure 3.3.1.2.1.1.2.2-6.

Forward Current

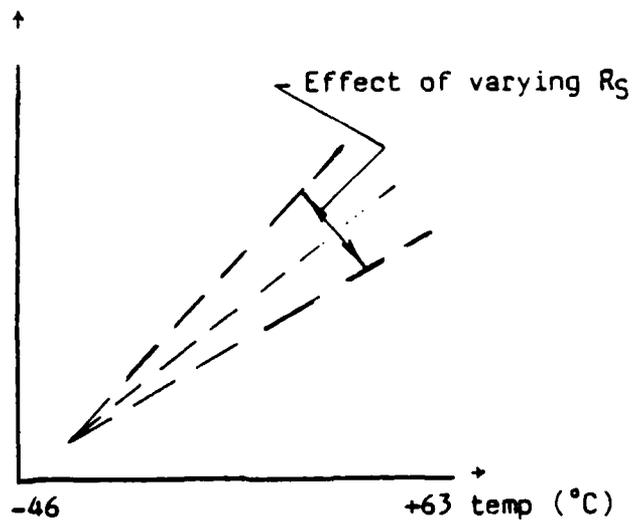


Figure 3.3.1.2.1.1.2-6

It will be seen that the compensation applied by the current control circuit under-drives the LED at the extreme of the temperature range and over-drives the LED in the middle of the range. This results in an optical power output which is not flat over temperature but one which is curved as shown in Figure 3.3.1.2.1.1.2.2-4.

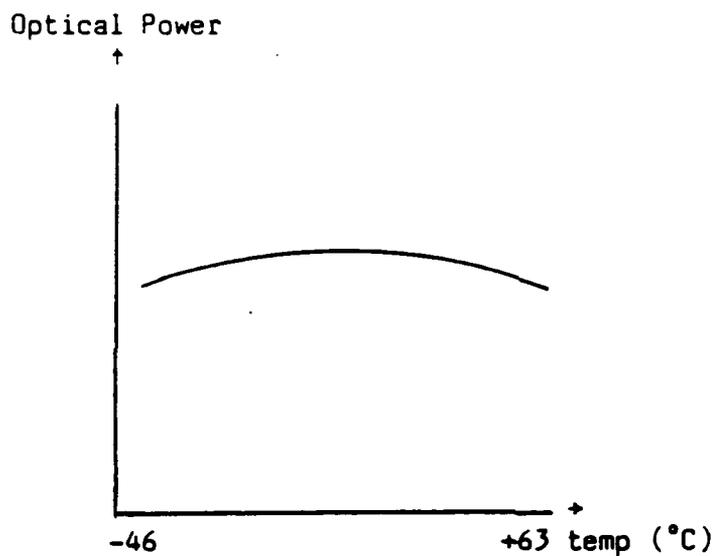


Figure 3.3.1.2.1.1.2.2-4

The two set resistors inside the LED package are selected to ensure that all of the above curve lies within the limits of 25 uW to 50 uW. These resistors, R_I and R_S , have different effects on the forward current as follows.

It is this technique which allows the optical power curve of Figure 3.3.1.2.1.1.2.2-4 to be moved up and down and to be pivoted which ensures it will lie between the required power limits.

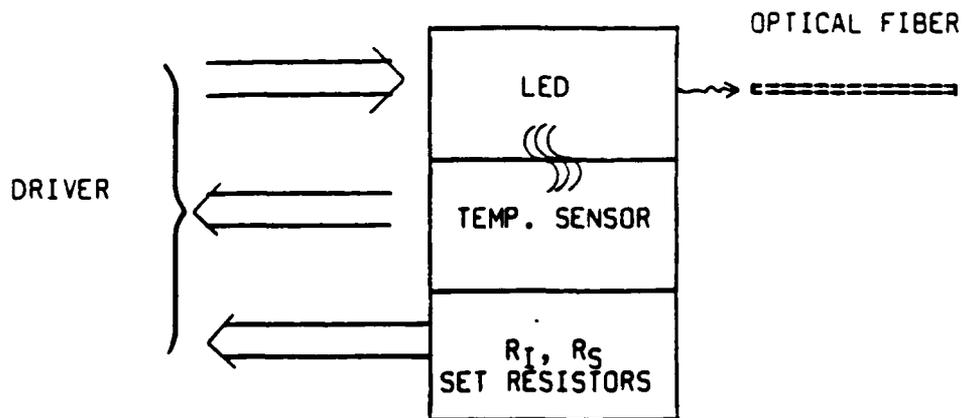
The forward voltage monitor is a simple circuit which has been described in Section 3.3.1.2.1.1.1.2. It has one unavoidable drawback however in that to register an unduly high forward voltage of the LED, the LED must obviously be on. This means that if the incoming data signal turns the LED off, the alarm output will not be triggered even if the LED is defective. This must be born in mind and the alarm output used accordingly.

3.3.1.2.1.1.2.3 Special Considerations

The driver proved to be somewhat inconvenient to test since it had to be held in a variable temperature environment, heatsunk since it can dissipate 1.6W, and accessed with various low frequency and high frequency connections. This was accommodated by constructing a special chamber with the required connections through which was passed dry air of the required temperature.

3.3.1.2.1.1.3 Functional Description of Level 1 LED

3.3.1.2.1.1.3.1 Block Diagram



3.3.1.2.1.1.3.2 LED Function

The most taxing part of the LED design and manufacture was to ensure mechanical rigidity between the LED chip and the optical fiber. The chip is mounted on a metal block inside the LED package which brings it to the optimum height for maximum light transfer into the fiber. Initially, rigidity was attempted by epoxying the end of the fiber to the metal block, however it proved to allow fiber movement during temperature cycling. This caused variation of the optical power traveling through the fiber in an unpredictable fashion and so had to be remedied. The adopted solution was to solder a very small metal sleeve over the end of the fiber and hold the sleeve to the metal block by a mechanical clamp arrangement. This gave good rigidity and also allowed micropositioning of the fiber during assembly for maximum light collection.

The temperature sensor is a two-terminal integrated circuit in a very small ceramic package. It is mounted close to the LED chip inside the LED package and gives an output to the driver of $1\mu\text{A}$ for every degree Kelvin of the LED chips' temperature.

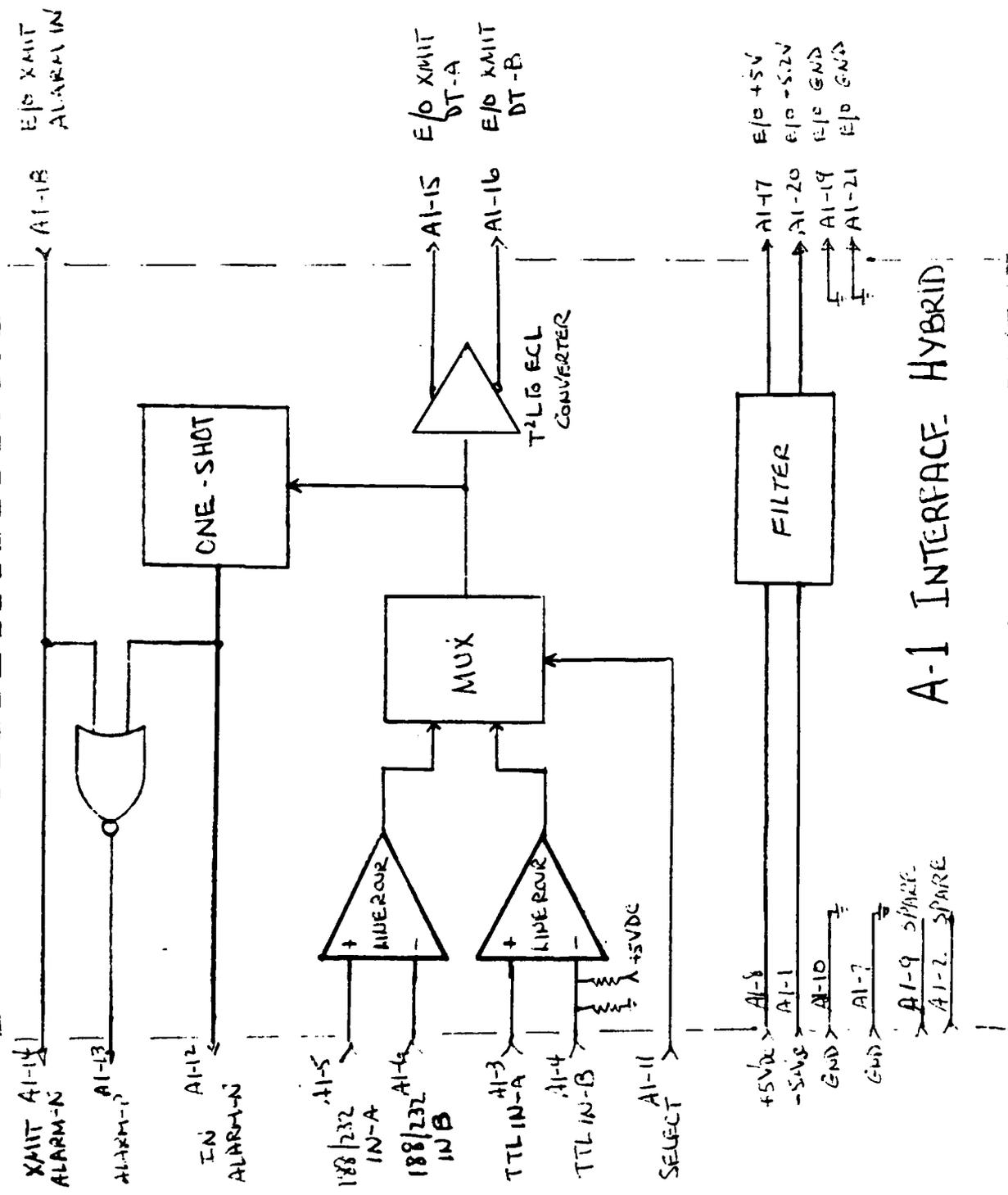
The two set resistors, R_I and R_S , are mounted in convenient locations inside of the LED package and control the driver as described in Sections 3.3.1.2.1.1.1.2 and 3.3.1.2.1.1.2.2.

3.3.1.2.1.1.3.3 Special Considerations

In order to maintain package hermeticity, the fiber/package interface had to be leak-proof. This was achieved by soldering the small metal tube over the fiber to the outlet ferrule in the LED package wall. The LED posed some of the same problems in testing conditions as did the driver. This was easily accommodated, however, by enclosing the LED in the environmental chamber designed for the driver. Selecting the set resistors for each LED was very time-consuming as this had to be checked at three different stages during manufacture. This was justified, though, by minimizing costly rework on LED's by accurately controlling the performance of the driver forward current control circuit.

3.3.1.2.1.2 Interface Assembly

3.3.1.2.1.2.1 Interface Assembly Block Diagram



3.3.1.2.1.2.2 Design and Tradeoffs

The Level 1 Transmitter Interface Assembly is designed for the following functions:

- o Selectively route TTL, MIL-STD-188-114 or RS-232C data from the host system to the Driver Module.
- o Provide Alarm test points detailing transmitter status to the host system.
- o Provide filtered power to all Level 1 Transmitter circuits.

3.3.1.2.1.2.2.1 Data Signal Paths

The Interface Assembly's TTL, MIL-STD-188-114 and RS-232C line receiver inputs are shown in the block diagram. One line receiver was selected that could meet all three MFOX interface specifications to minimize Interface Assembly size and power requirements. The AM26LS32B integrated circuit contains four line receivers, of which two are used.

One of the two line receivers handles balanced or unbalanced TTL data while the other handles balanced or unbalanced MIL-STD-188-114 or unbalanced RS-232C data. A comparison of line receiver characteristics to the MIL-STD-188-114 and RS-232C specifications is provided in 3.3.1.2.1.2.2.1-1.

<u>AM26LS32</u>	<u>Meets 188 Spec?</u>	<u>Meets RS 232C Spec?</u>
Voltage Threshold = 200mV max	yes (200mV max)	yes (3V max)
Voltage Threshold = 400mV max (with 500 OHMS in series with inputs)	yes (400mV max)	N/A
Common Mode Voltage = +15V max	yes (+7V max)	N/A
Input Voltage = 25V max	yes (10V max)	yes (25V max)
Input Resistance = 4K min	yes (4K min)	yes (3K min)
Data Rate = 10 Mbit/sec	yes (10 Mbit/sec Balanced max) 100 Kbit/sec un- balanced max	yes (20 Kbit/sec max)

Figure 3.3.1.2.1.2.2.1-1 Transmitter 188/232 Line Receiver
Specification Unbalanced Specification
Comparison

Unbalanced transmission of MIL-STD-188-114 or RS-232C data is accomplished by grounding the negative terminal of the line receiver and providing the data at the positive terminal. Balanced Transmission simply involves the connection of the balanced MIL-STD-188-114 source to the plus and minus terminals of the line receiver.

The AM26LS32B lends itself to balanced and unbalanced TTL transmission as well. A resistor voltage divider with an equivalent resistance of 1600 OHMS biases the negative terminal to approximately 1.3 volts for use as an unbalanced receiver. With this terminal floating, unbalanced TTL signals are routed through the positive terminal to the multiplexor. The voltage divider essentially raises the decision level of the line receiver from ground to 1.3V which is greater than a TTL logic 0 and less than a TTL logic 1 by wide margins. The relatively high impedance of 1600 OHMS was chosen so

that the biasing would not affect balanced TTL operation. A balanced TTL signal at the positive and negative terminals is relatively unaffected by the biasing of the negative input since any signal driving this input is isolated from +5V and from ground by the high resistances.

The balanced TTL and balanced MIL-STD-188-114 interfacing are designed to accommodate termination resistors to minimize signal distortion and reflection problems. Controlled impedance transmission methods such as twisted pair or simulated printed transmission lines with proper terminating resistors are recommended if signal rise times are short compared to transmission distances.

With the data properly connected to the TTL or 188/232 line receiver the multiplexor (see the block diagram of 3.3.1.2.1.2.1) is programmed to route the data to the one-shot timer (discussed in the Alarms section) and to the TTL to ECL converter. The MUX block is a SN54ALS157 two-to-one multiplexor programmed by shorting to ground or floating the Select bit. The Select input is TTL compatible and pulled up to +5V through a 10 K resistor. The ALS part was chosen to minimize power requirements, current spiking, and signal distortion. The TTL to ECL converter interfaces the Interface Assembly to the Driver Module.

3.3.1.2.1.2.2.2 Alarm Paths

The block labeled one-shot is actually a combination of two integrated circuits, the SN54LS122 retriggerable monostable multivibrator and the SN54LS10 triple three-input positive NAND gates. A schematic of the alarm logic is provided in Figure 3.3.1.2.1.2.2.2-1. The timer is triggered by rising edges of data output from the

multiplexor. The timer will time-out and its output will switch from a logic 0 to a logic 1 if the data output from the multiplexor ceases entirely or if the data pulse widths are longer than the timer's time-out interval. Since the system is specified at 1.0 Kbps minimum, data pulses have durations of at least 1.0 msec. The assumption was made that 10 consecutive identical bits constituted the longest interval with no data transitions during normal operation. The timer time-out interval is therefore designed to be longer than $2 \times 10 \times 1\text{msec}$, or 20 msec. The factor of two is added since the multiplexor is triggered by only the rising and not the falling edges of the data. The 150k resistor and 2.2uF capacitor yield values of typically 100 msec, which exceeds the requirement by a factor of five.

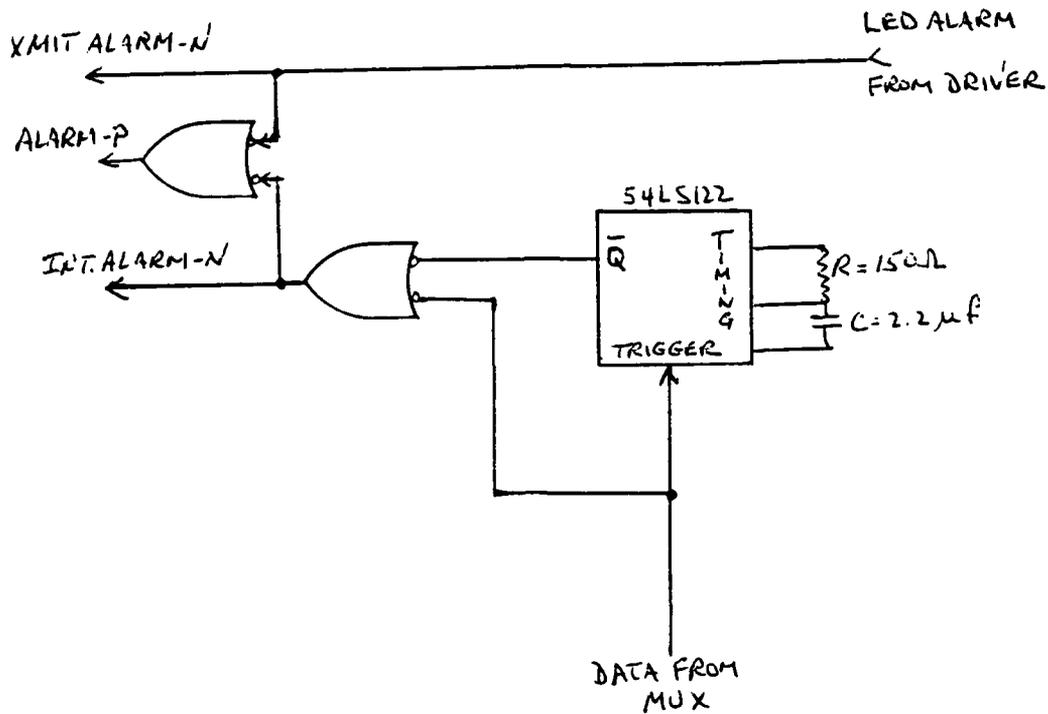


Figure 3.3.1.2.1.2.2.2-1

The output from the timer is sent to a NAND gate along with the data directly from the Mux. With these signals routed in this way, the NAND gate will switch from a logic 1 (non-alarmed state) to a logic 0 (alarmed-state) only if the timer times out and the data from the Mux is not a constant logic 0. This latter provision insures that when transmitting data asynchronously, long marking states such as those occurring during RS-232C inactive periods, will not trigger the alarm. In summary, the interface alarm is active low and detects faulty line receiver/multiplexor operation or below specification data transmission.

The LED alarm, explained in 3.3.1.2.1.1, is simply routed from the Driver, through the Interface Assembly, to the host system. This alarm is active low. The output of the second NAND gate pictured in

the schematic is provided as a single test point for convenience in detecting an alarm condition. This alarm is active high and is triggered by activation (logic 0 condition) of the interface and/or LED alarms.

3.3.1.2.1.2.2.3 Supply Filtering

The +5V and -5.2V supply inputs are filtered by the two-pole inductive capacitive filters described in 3.2.1.1.2. The filter component values are:

+5V Supply	C1 = 0.1uF
	C2 = 6.8uF
	L1 = 10uH

-5.2V Supply	C1 = 0.1uF
	C2 = 6.8uF
	L1 = 50uH

3.3.1.2.2 Receiver Description and Diagram

The receiver consists of a Threshold module, a Preamplifier module and a power supply filter mounted on a printed circuit board (PCB), and the Interface hybrid as shown in the block diagram of Figure 3.3.1.2.2-1. The Pre-amplifier module outputs an analog voltage to the Threshold module that is proportional to the incoming optical signal. The Threshold module converts the preamplifier output to a digital signal and passes this signal as well as alarm status information to the Interface hybrid. The Interface hybrid passes the alarm signal to the host system, transmits the digital data through one of two selectable interfaces to the host system and provides filtered power to all receiver circuits.

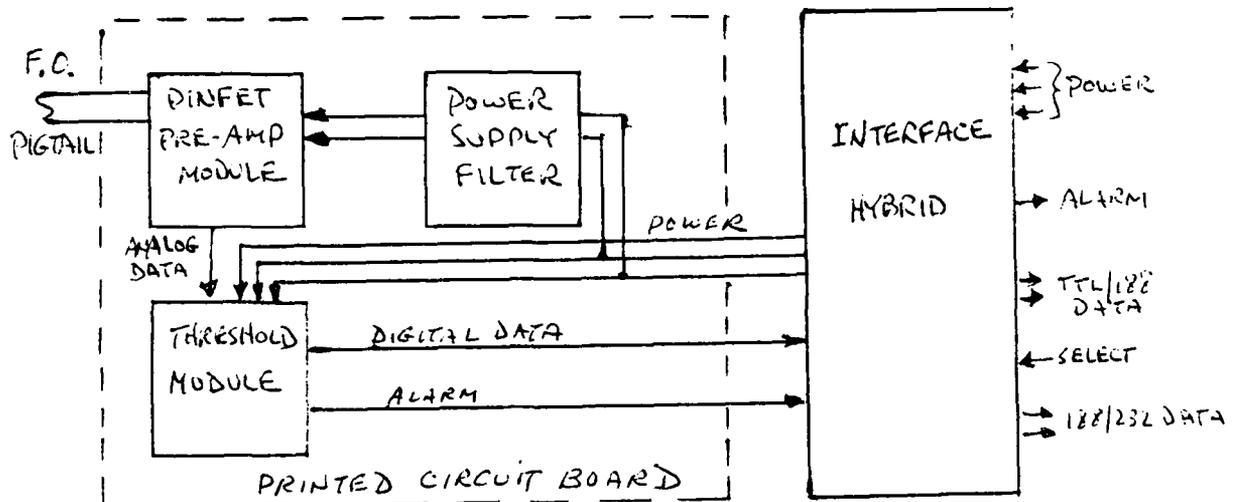


Figure 3.3.1.2.2-1

The Interface Assembly filter is described in 3.3.1.2.2.2. The printed circuit board mounted filters are simple one-pole resistive-capacitive filters designed to isolate the PINFET pre-amplifier +5V

and -5.2V supplies. The PINFET is a high-gain analog device, susceptible to supply transients that could cause receiver sensitivity degradation. This type of filter was chosen over the inductive-capacitive two-pole type for the following reasons:

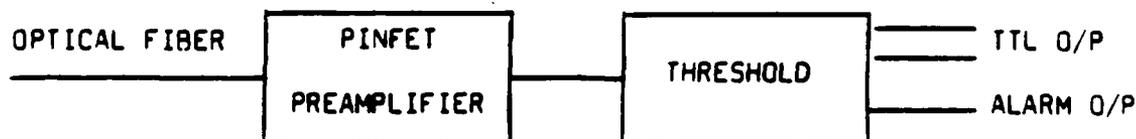
- o The resistor-capacitor filter does not exhibit resonant frequency peaking. Even a low "Q" inductive capacitive type filter exhibits an increased frequency response within the operating frequency range of 1Kbps to 10Mbps for practical inductor and capacitor values.
- o Because PINFET supply currents are low, the filter resistors induce a negligible voltage drop from Receiver circuit supplies to PINFET supplies, while acting as effective attenuators over a wide frequency range.

3.3.1.2.2.1 Threshold and PINFET Assemblies

3.3.1.2.2.1.1 E/O Subsystem

3.3.1.2.2.1.1.1 Description of the Subsystem

3.3.1.2.2.1.1.1.1 Level 1 E/O Subsystem Block Diagram



3.3.1.2.2.1.1.1.2 PINFET Function

The purpose of the pinfet is to transform the optical power coming out of the fiber cable into an electrical signal. The modules used were standard product from RCA - the C30986 series. This unit is

a transimpedance preamplifier module using a low noise GaAs FET front end, and a circuit configuration to minimize the input capacitance. The p-i-n photodiode (C30979) used in these devices is a high speed Indium Gallium Arsenide/Indium Phosphide photodiode providing high responsivity between 900 and 1700 nm.

3.3.1.2.2.1.1.1.3 Threshold

The purpose of the threshold units is to transform the analog output of the pinfet into a digital signal. The modules also provide an alarm signal which is activated when the optical power goes under a specified level.

3.3.1.2.2.1.1.2 Pinfet

3.3.1.2.2.1.1.2.1 Approach/Tradeoffs

The design work for the MFOX project consisted in selecting the appropriate feedback and internal gain resistors, in order to achieve the various system requirements.

In a transimpedance receiver the choice of the feedback resistor is extremely important since it will determine several characteristics of the module. The internal gain resistor is selected in conjunction with the feedback resistor. The internal gain adjustment is necessary to fine tune the frequency response, or put differently; the second order transfer function of the transimpedance is optimized by varying the open loop gain.

The following equations show the impact of the feedback resistor (R_F) on the module performance:

$$\text{Responsivity (R)} = 0.7 * 0.95 * R_F \quad \propto R_F$$

$$\text{Output spectral noise (N}_V) \quad \propto \sqrt{R_F}$$

$$\text{NEP} = \frac{N_V}{R} \quad \propto \frac{1}{\sqrt{R_F}}$$

$$\text{Bandwidth (BW)} = \frac{A_{in}}{2\pi C_{in} R_F} \quad \propto \frac{1}{\sqrt{R_F}}$$

$$\text{Sensitivity} = 10 \log \frac{6N_V \sqrt{BW}}{R} \quad \propto \log \frac{1}{\sqrt{R_F}}$$

$$\text{Overload point} = 10 \log \frac{V_{MAX}}{R} \quad \propto \log \frac{1}{\sqrt{R_F}}$$

These formulas show that with increasing R_F , we improve the responsivity, NEP and sensitivity figures. However, on the other hand we get reduced bandwidth as well as a lower overload point. Therefore, the choice of the feedback resistor will be governed by the respective system specifications.

3.3.1.2.2.1.1.2.2 Design Steps and System Requirements

Bit rate: 1Kbps (NRZ) to 10Mbps (Manchester) which gives a minimum bit time of 50ns (10Mbps in Manchester data format). The maximum rise time and minimum bandwidth are as follow:

$$\text{Rise time} = t_r < 0.7 * 50 \text{ ns} = 35 \text{ ns}$$

$$\text{Bandwidth} = BW > \frac{0.35}{t_r} = 10 \text{ MHz}$$

The sensitivity requirement is -36 dBm, but because of the hysteresis on the threshold module we subtract 8.2 dB, which gives -44.2 dBm. The dynamic range is 15dB, which gives an overload point of -21 dBm. With all these specifications in mind we can now go through the calculation to select the feedback resistor.

$$\text{Overload point} = -21 \text{ dBm} = 10 \log \left(\frac{V_{AVE-MAX}}{R_{MAX}} \right)$$

The maximum voltage at the output of the pinfet before saturation is 2.5V_{p-p}. For a 50% duty cycle signal, the maximum average voltage will then be 1.25 V.

$$-21 \text{ dBm} = 10 \log \frac{1.25}{R_{MAX}}$$

$$R_{MAX} = \text{Responsivity} = 157 \text{ Kv/W}$$

$$\text{Responsivity} = 0.7 * 0.95 * R_{F_{MAX}} = 157 \text{ Kv/W}$$

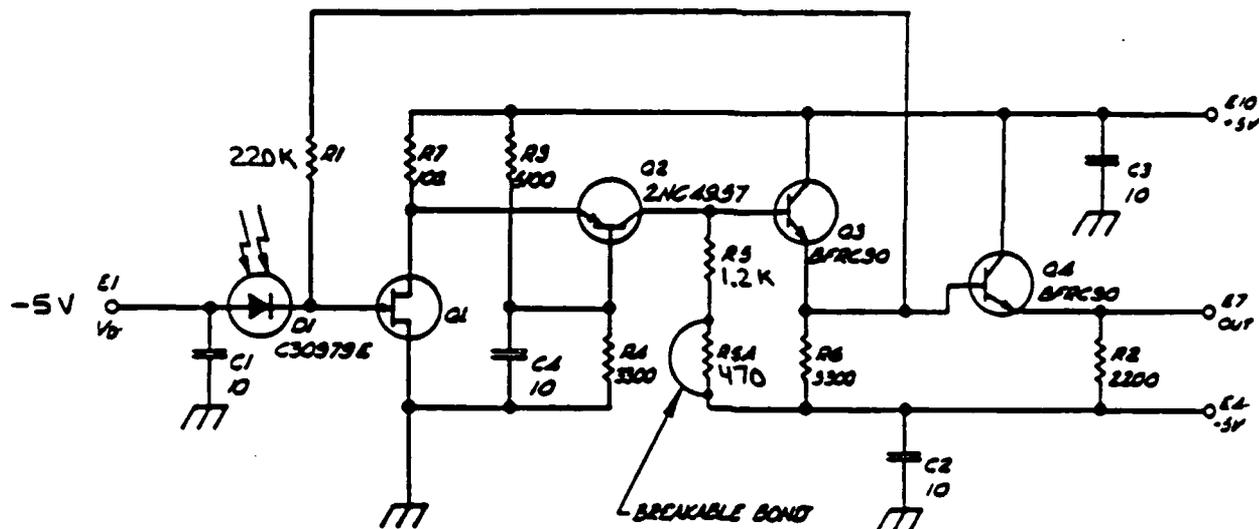
$$R_{F_{MAX}} = 236 \text{ K}\Omega$$

A feedback resistor of 220 K Ω will be selected at this point. A theoretical analysis of the output spectral noise voltage density gives a typical value of 80 nV/ Hz. And finally the projected sensitivity @ 10⁻⁹ BER is:

$$\text{Sensitivity} = 10 \log \frac{6 (80\text{nV}/\sqrt{\text{Hz}}) \sqrt{25 \text{ MHz}}}{157 \text{ Kv/W}} = -48 \text{ dBm}$$

Since all the system specifications are met, the choice of 220K Ω as the feedback resistor is adopted.

3.3.1.2.2.1.1.2.3 Pinfet Schematic



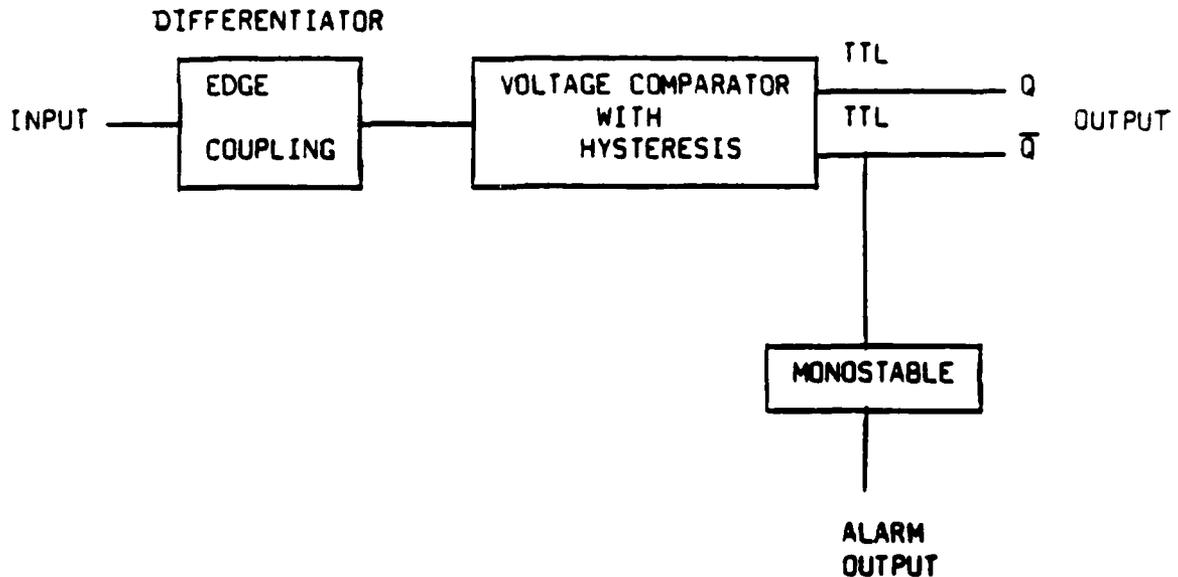
3.3.1.2.2.1.1.2.4 Pinfet Package

The pinfet is supplied in a hermetically sealed 14-pin dual in-line package. The package mechanical characteristics are described in RCA drawing #2545063-3.

The optical fiber is attached to the case using epoxy and torr seal. The alignment of the fiber is done by monitoring the photocurrent of the detector. For detailed description of the pigtailing steps consult RCA procedure P4122.

3.3.1.2.2.1.1.3 Threshold (C30614E)

3.3.1.2.2.1.1.3.1 Threshold Level 1 (C30614E) Block Diagram



3.3.1.2.2.1.1.3.2 Design and Tradeoffs

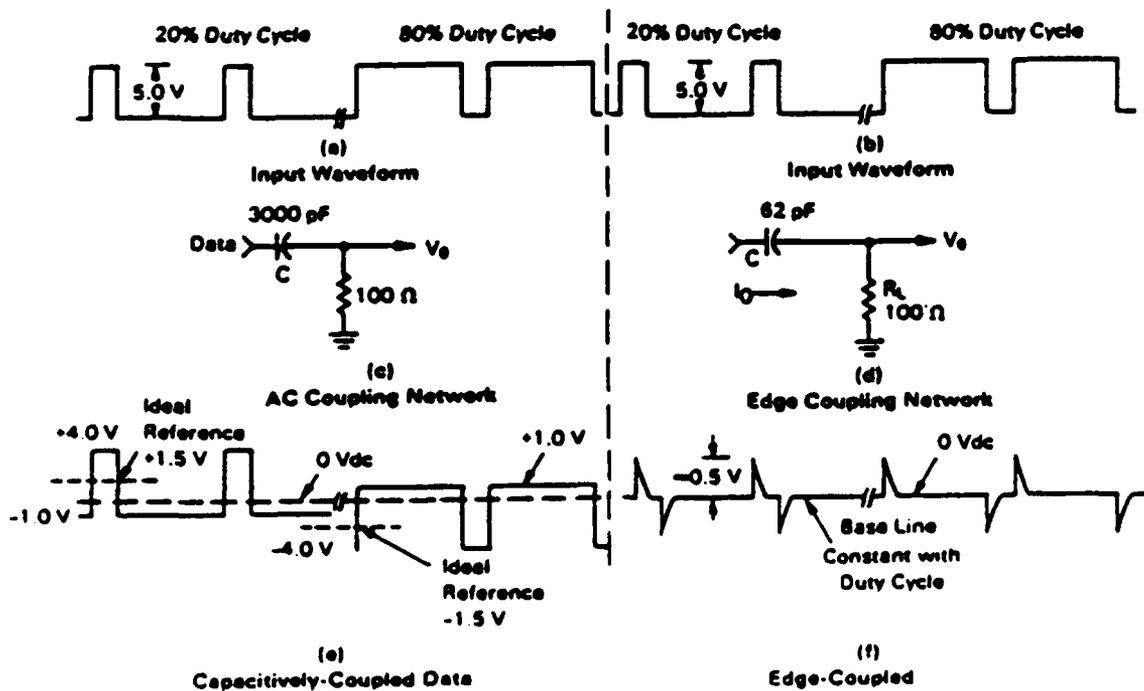
The following description of the C30614E will explain the design steps and tradeoffs that led us to the final configuration.

The first component in the block diagram of 3.3.1.2.2.1.1.3.1 is the differentiator or edge coupled receiver. The edge coupled receiver is used to strip off the base line variation with duty cycle from the data stream. Since the Level 1 system has to operate at an arbitrary duty cycle, without any coding constraints, the edge coupled receiver saves us from tracking base line variations which would occur with an AC coupled receiver, (see Figure 3.3.1.2.2.1.1.3.2-1).

On the schematic the differentiator is represented by C1 and R1. In selecting the values of these components we want to maximize the

voltage drop across R1 to provide maximum amplitude to the voltage comparator, the next stage in the module. To do so we have to maximize the RC time constant. However, there is a limit in increasing this time constant because the differentiator has to recover before the next bit.

The combination of 475 and 390 pf turned out to be the best compromise after some theoretical calculation and experimentation. Our first choice for C1 was 100 pf; this value permitted the differentiator to fully recover for the minimum bit time but was attenuating the signal too much. R1 was more or less a fixed value because it is used as a load resistor for the pinfet and as part of the hysteresis of the following stage. We preferred modifying the C1 value because of these factors.



COMPARISON OF DATA STREAM WAVEFORMS THROUGH AC COUPLED AND EDGE COUPLED SYSTEMS

Figure 3.3.1.2.2.1.1.3.2-1

The second component in the block diagram is the voltage comparator. The LM160 from National Semiconductor was chosen. The LM160 is a very high speed (20 ns) differential input, complementary TTL output voltage comparator. The electrical characteristics of this component satisfied the MFOX Level 1 requirements.

The voltage comparator is not used in an open loop configuration because we do not want the module to be continuously triggered by noise. In other words, our module should reject idle channel noise. This condition forces us to use a voltage comparator with hysteresis. The price to pay in using a single ended edge coupled receiver with hysteresis is a loss in sensitivity of 8.2 dB. This sacrifice in sensitivity buys us, as mentioned earlier, the freedom from idle channel noise and the simplicity of no base line variation with duty cycle. The duty cycle issue is particularly important because the Level 1 system uses NRZ coding. Moreover, since the Level 1 specification gives us enough room to spare 8.2 dB we naturally opted for that configuration.

The next step is to select the resistor values for the hysteresis (R1 to R4). To obtain noise rejection the hysteresis must be greater than the peak to peak noise riding on the data stream. The amplitude of that noise is found by looking at the pinfet spectral output noise voltage density value. For the Level 1 pinfet the worst case is:

$$V_n = 100 \text{ nV}/\sqrt{\text{Hz}}, \text{ BW} = 35 \text{ MHz}, V_o = 100 \frac{\text{nV}}{\sqrt{\text{Hz}}} \times \sqrt{35\text{M}} = 600 \text{ } \mu\text{V}$$

The required sensitivity of the Level 1 system being -36 dBm we can calculate what will be the minimum amplitude of the signal coming out

of the pinfet:

$$\text{Sensitivity} = -36 \text{ dBm} = 10 \log \frac{V_{AVE}}{\text{Responsivity}}$$

$$\text{where Responsivity} = 220 \text{ K}\Omega \cdot 0.7 \frac{\text{A}}{\text{W}} \cdot 0.9 = 1.4 \cdot 10^5 \text{ V/W}$$

$$\text{we get } V_{MIN} = 70 \text{ mV}_{p-p} \text{ (50\% duty cycle, } V_{AVE} = V_{p-p}/2)$$

This means that the hysteresis has to be set between the maximum noise output (600uVRMS) and the minimum signal to detect (70 mV_{p-p}). Here is how we calculate the hysteresis:

$$H = (V_{OHIGH} - V_{LOW}) \frac{R1}{R1+R4} = (3-0.25) \frac{475}{475+182K} = 7.2 \text{ mV}$$

As you can see we are well above the noise floor and we easily respect the sensitivity specification.

The last component in the block diagram is the monostable. The monostable controls the alarm output. As long as the voltage comparator sends data, the monostable is triggered and gives out a pulse of a certain duration. If no data are received for a period longer than the time constant (t_w) the alarm output changes state to signify a loss of communication. The time constant of the alarm signal (t_w) has been maximized in order to avoid false alarm on long strings of 0's and 1's.

$$t_w = 0.32 \cdot R10 \cdot C6 \left[1 + \frac{0.7}{R10} \right]$$

$$= 0.32 \cdot 182K\Omega \cdot 0.47 \mu\text{F} \left[1 + \frac{0.7}{182K\Omega} \right] = 27 \text{ mS}$$

3.3.1.2.2.1.1.3.4 Packaging

The Level 1 Threshold is supplied in a hermetically sealed 14-pin dual in-line package. The package mechanical characteristics are described in RCA drawing #2545063-7.

3.3.1.2.2.1.1.4 Test Results Vs. Acceptance Criteria

In order to show that the specifications were met by the pinfet, the threshold, and their combination (pinfet + threshold = receiver); here are some tables that compare actual test results with the original acceptance criteria.

3.3.1.2.2.1.1.4.1 Pinfet

@ 25°C	<u>ACCEPTANCE CRITERIA</u>			<u>TEST RESULTS</u>				<u>UNITS</u>
	<u>MINIMUM</u>	<u>TYPICAL</u>	<u>MAX</u>	<u>MINIMUM</u>	<u>MAXIMUM</u>	<u>MEAN</u>	<u>STD DEV</u>	
Responsivity @ 1.3 um	1.2x10 ⁵	1.5x10 ⁵	-	1.2x10 ⁵	1.7x10 ⁵	1.6x10 ⁵	0.15x10 ⁵	V/W
Output Spectral Noise Voltage Density Integrated Over the Bandwidth	---	80	100	66	99	89	9	nV/Hz
Bandwidth	25	35	-	29	44	37	5	MHz
Overload Point	-22	--	-	-21.7	-18.6	-20.7	1	dBm
Dark Current	---	15	30	3	27	10	8	nA
Sensitivity	-46	-47	-	-46.2	-49.0	-46.8	0.7	dBm

3.3.1.2.2.1.1.4.2 Threshold

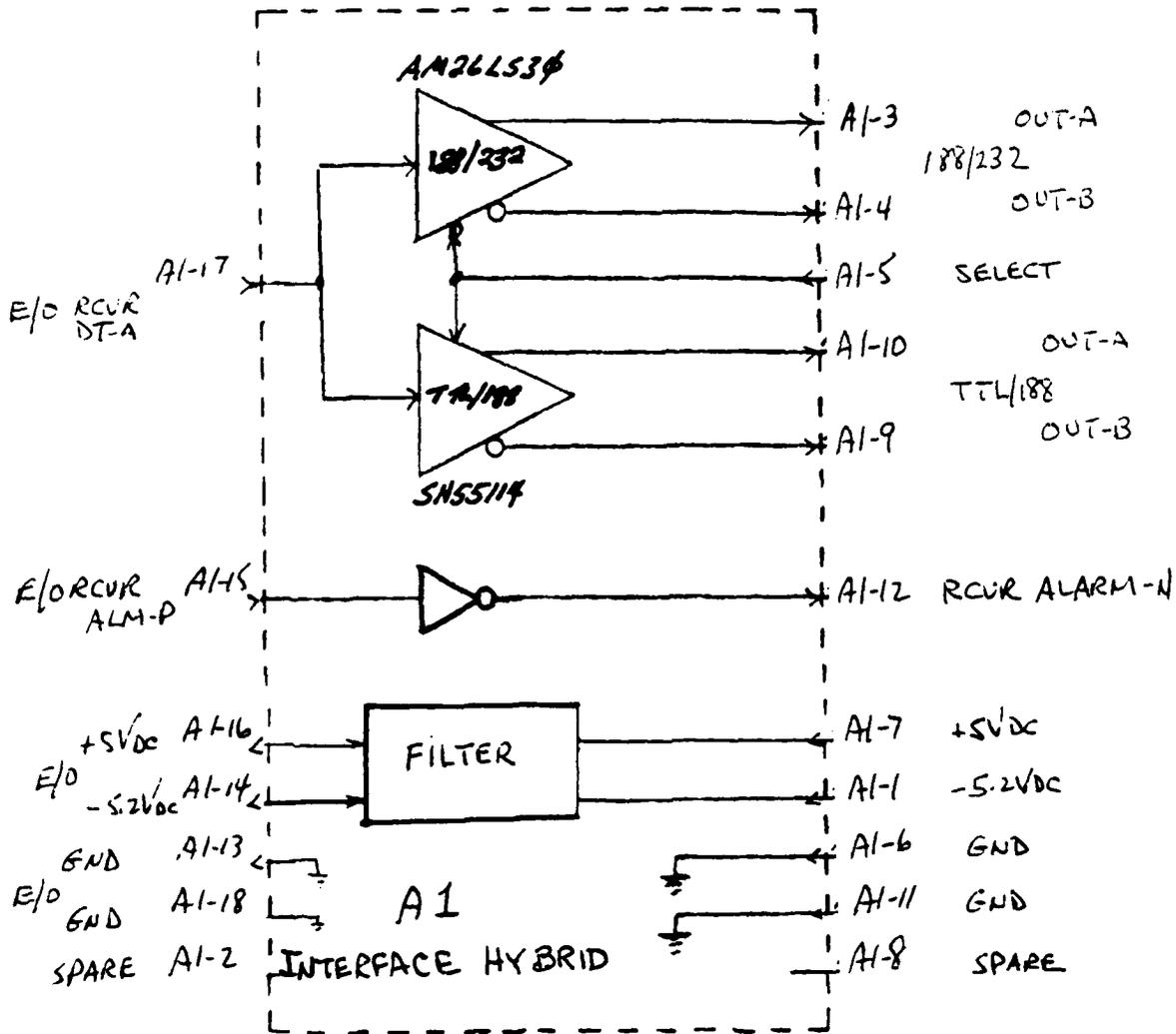
	<u>ACCEPTANCE CRITERIA</u>			<u>TEST RESULTS</u>				UNITS
	Min	Typ	Max	Min	Max	Mean	STD DEV	
Minimum Toggling Level @ 10 MHz (SQW)	-	50	70	12.2	14.8	12.8	1.4	mV _{p-p}
Minimum Data Rate (SQW) Before Alarm (Pin=-36dBm)	100	-	-	33	36	34	0.9	Hz
Power Consumption:								
I+	-	60	100	30	35	33	2	mA
I-	-	20	40	6.3	7	6.6	0.3	mA

3.3.1.2.2.1.1.4.3 Receiver

	<u>ACCEPTANCE CRITERIA</u>			<u>TEST RESULTS</u>				UNITS
	Min	Typ	Max	Min	Max	Mean	STD DEV	
Minimum Toggling Level @ 10 MHz (SQW)	-	50	70	7.9	10.8	9	1.6	mV _{p-p}
Minimum Data Rate (SQW) Before Alarm (Pin=-36dBm)	100	-	-	29	35	33	1.7	Hz
Power Consumption:								
I+	-	60	100	58	60	59	0.8	mA
I-	-	20	40	15	16	15	0.5	mA

3.3.1.2.2.2 Interface Assembly

3.3.1.2.2.2.1 Interface Assembly Block Diagram



3.3.1.2.2.2.2 Design and Tradeoffs

The Level 1 Receiver Interface Assembly is designed to perform the following functions.

- o Selectively route data from the Threshold module to TTL, MIL-STD-188-114 or RS-232C interfaces.

- o Pass the receiver alarm signal from the Threshold module to the host system.
- o Provide filtered power to all Level 1 Receiver circuits.

3.3.1.2.2.2.3 Data Paths

As shown in the Interface Assembly block diagram, data from the Threshold module is routed to two line driver circuits. Both line drivers can be enabled or disabled by the Select input. This input is TTL compatible and pulled up to +5V through a 10K resistor. Floating this input enables the TTL/188 driver and grounding this input enables the 188/232 driver. Only one driver is active at any time.

The SN55114 line driver is used as both the TTL interface and the balanced MIL-STD-188-114 interface. This is feasible since this line driver meets all TTL specifications and all balanced MIL-STD-188-114 specifications with only one exception. A comparison of the line driver specifications and the balanced MIL-STD-188-114 specifications are shown in Figure 3.3.1.2.2.2.3-1. Use of the SN55114 despite the output voltage offset discrepancy is justified on the following grounds: Any true MIL-STD-188-114 line receiver can handle common mode voltages up to ± 7 volts. Therefore, the 2 Volt common mode voltage typically induced by this line driver will present no problems provided the host system's line receiver meets MIL-STD-188-114 specifications.

<u>SN55114</u>	<u>Meets 188 SPEC?</u>
Open Circuit Output Voltage 6V TYP	Yes (6V max)
Output Resistance 100 ohms TYP	Yes (100 max)
Output Voltage Offset = 2V TYP	No (400mV max)
Short Circuit Current = 120 mA max	Yes (150mA max)
Leakage Current = 90uA max at 6V	Yes (100 uA at 6V)
Data Rate = 10 Mbit/sec	Yes (10 Mbit/sec)

Figure 3.3.1.2.2.3-1 Receiver Balanced MIL-STD-188-114 Line Driver Specification

At the time of the Receiver design an extensive search was made for an integrated circuit that could perform all MIL-STD-188-114 functions. No such part existed capable of meeting the output voltage and current requirements at rates to 10 Mbps. The only options were a discrete design, an off-the-shelf hybrid or the solution just discussed. The off-the-shelf hybrid met most MIL-STD-188-114 specifications but was a large, high current device not easily incorporated into the MFOX design. The discrete solution was also rejected because of size and power constraints.

The AM26LS30 does meet all MIL-STD-188-114 specifications with the exception of the data rate requirement of 10Mbps. This circuit is capable of the 100Kbit/sec requirement for unbalanced MIL-STD-188-114 transmission however. The SN55114 is not suitable for unbalanced transmission because of the positive and negative voltage signal switching requirements. The AM26LS30 then is used as a combination unbalanced MIL-STD-188-114 and RS-232C driver. A comparison of the AM26LS30 specifications with those interface requirements is provided

in Figure 3.3.1.2.2.3-2.

<u>AM26LS30</u>	<u>Meets 188 SPEC?</u>	<u>Meets RS-232C SPEC?</u>
Open Circuit Output Voltage = 4.0 min/6.0V max	Yes (6.0V max)	No $V_{oc} = 5.0V$ min
Output Resistance = 50 ohms max	Yes (50 max)	N/A
Short Circuit Current = 150 ohms max	Yes (150 mA max)	Yes
Leakage Current = 90 uA max at 6V	Yes (100 uA at 6V)	Yes (6mA at 2V)
Data Rate = 100 Kbit/sec	Yes (100Kbit/sec max)	Yes (20Kbit/sec max)

Figure 3.3.1.2.2.3-2 Receiver Unbalanced MIL-STD-188-114 and RS-232C Line Driver Specification Comparison

Use of the AM26LS30 as a RS-232C driver despite the 4 volt output minimum is justified on the following grounds: Any true RS-232C line receiver can detect input signals as low as 3.0 volts. Therefore, the guaranteed minimum of 4.0 volts output by this line driver will present no problems provided the host system line receiver meets RS-232C specifications.

The RS-232C output voltage amplitude issue is one that occurs for any RS-232C compatible driver selected for the MFOX system. The Level 1 Receiver is supplied from +5V and -5.2VDC voltages. A line driver output exceeding the +5V and -5V required by the RS-232C interface is clearly impossible. To minimize receiver size and current requirements the AM26LS30 doubles as the driver for both unbalanced interfaces.

3.3.1.2.2.2.4 Alarm Path

The alarm signal from the Threshold module is described in 3.3.1.2.2.1. The Interface merely inverts and buffers this signal

before transmitting it to the host system. The alarm output is TTL compatible, active low.

3.3.1.2.2.2.5 Supply Filtering

The +5V and -5.2V supply inputs are filtered by the two-pole inductive capacitive filters described in 3.2.1.1.2. The Filter component values are:

+5V Supply	C1 = 0.1uF
	C2 = 6.8uF
	L1 = 50uH
-5.2V Supply	C1 = 0.1uF
	C2 = 6.8uF
	L1 = 50uH

3.3.1.3 Special Considerations

3.3.1.3.1 Threshold Assembly Alarm

The first couple of threshold units we manufactured, had a problem with the alarm signal when using arbitrary duty cycle. This problem was caused by AC coupling the Q output of the voltage comparator, before going into the monostable. When working with high duty cycle, the base line was shifting upward and no more high level could be detected.

Since the monostable is activated by a rising edge, we simply solved the problem by DC coupling the alarm circuit.

3.3.1.3.2 PINFET Assembly Pigtail Attachment

The procedure for the attachment of the optical fiber to the pinfet module had to be modified. Indeed, after we tested the first samples, a high percentage of the fiber had fallen off. The standard procedure for pigtailling was using only ultra-violet epoxy. To reinforce the pigtail, we used in addition to the U.V. epoxy, a

substance called torr seal.

This new procedure greatly improved our yield. However, for future development we should look into a case with a permanent ferrule and soldered optical fiber. This assembly would free us from using epoxy, which softens and hardens with temperature variations, thus causing optical fiber disalignment.

3.3.1.3.C Pigtail Strain Relief

A special design concern for the transmitter and receiver was providing strain relief for the optical pigtails which are fed through the outer case. The pull strength of the pigtail termination at the LED and PINFET had to be supplemented to meet the goal of having a 50 N pull strength for the external optical cable. This was especially true for the PINFET which has an epoxy butt joint of the cable to component case. The LED termination is stronger because of a brazed tube construction. Strain relief is accomplished for copper conductors by applying a compressive force. This method cannot be employed for optical cable which suffers signal degradation when the compressive force approaches the strength limit of 300 N/cm. A simple, low cost solution was achieved by feeding the optical cable through a brazed tube on the outer case and applying adhesive lined semi-rigid shrink sleeving over the tube and cable. For the receivers which have the more fragile PINFET pigtail termination, the semi-rigid tubing is assisted by a high strength silicone potting compound which is injected inside the oversized feed-thru tube.

The thermal design of the transmitters was especially critical due to a temperature sensitive LED. Since the Level 2 transmitter LED ran hotter due to higher power dissipations, this issue is addressed

in Section 3.3.2.3.

3.3.1.3.4 PCB Filters

The original Level 1 Receiver printed circuit board mounted PINFET filter design called for a two-pole inductive capacitive filter for each supply. It was found that receiver sensitivity improved 1dB to 2dB when the filter was changed. This called into question the effectiveness of the inductor response and capacitor response at higher frequencies.

A 10 ohm resistor replaced the inductor and a ceramic capacitor replaced the tantalum capacitor. PINFET supply currents are low enough not to induce a significant voltage across 10 ohms and filter effectiveness was improved since the new components retain their filtering abilities over a wider frequency range.

3.3.2 Level 2 Transmitter, Receiver, Encoder and Decoder ADMs

3.3.2.1 System Link Description

The Level 2 System can be configured in either one of two ways. The Transmitter and Receiver can be operated in a standalone mode or can be operated with the encoder and decoder. In the standalone mode the following four types of interconnections between the Level 2 System and the user's host system must be provided to fully operate and monitor a fiber optic link.

- o Power Inputs from Host System
- o Data Interface Control (Select) Inputs
- o Data Signals to/from the Selected Interface
- o Alarm (Test Point) outputs monitored by Host System

A working standalone link therefore includes power from the host system, programming of the select bits to activate either the ECL, TTL

or MIL-STD-188-114 data interfaces, data connections to the selected interface and the monitoring of the Alarm test points to detect a failed link condition.

A Level 2 link that includes the encoder and decoder must provide the following four types of signals between the user's host system and the four Level 2 units:

- o Power inputs from Host System
- o NRZ Data and Clock Control (Select) Inputs
- o Encoder and Decoder Frequency Control Inputs
- o NRZ Data and Clock to/from the Selected Interface
- o Alarm (Test Point) Outputs Monitored by Host System

Furthermore, the following two types of connections must be provided between the encoder and transmitter and between the decoder and receiver:

- o NRZ Data and Clock
- o Manchester Encoded Data

A working transmitter/encoder, receiver/decoder link therefore includes power from the host system to each of the four units, programming of the transmitter and receiver select bits to activate either the TTL or MIL-STD-188-114 data and clock interfaces, programming of the encoder and decoder frequency controls for Manchester coding at the proper clock rate, data and clock connections to the selected transmitter and receiver interfaces, data, clock and Manchester connections between the encoder and transmitter and receiver and decoder and the monitoring of the Alarm Test points to determine a failed link condition.

The diagram of 3.3.2.2 illustrates the types of connections for both system configurations.

3.3.2.1.1 Optical Considerations

System Level 2 is capable of transmitting digital data through up to 8 Km of optical fiber. The link capability calculations must take into account the specifications of the optical fiber, optical connectors, transmitter, receiver and, if used, the encoder and decoder. The encoder and decoder adversely effect receiver sensitivity by 3 dB. Therefore, all link evaluations should assume a receiver sensitivity of -37 dBm rather than -40 dBm, when using the encoder and decoder. An evaluation of the link pictured in 3.3.2.2 in the standalone configuration assuming 8 Km of tactical cable is provided in Figure 3.3.2.1.1-1.

The total cable and connector losses are subtracted from the transmitter best and worst case power outputs and compared to the receiver sensitivity and dynamic range. A positive margin, not greater than 24 dB, indicates the link will successfully pass data at the rates and formats specified.

In this example, the margin is 4 dB indicating a succesful link with 4 dB safety margin. If the encoder and decoder are added, the safety margin is 1 dB. Fiber bandwidth must also be considered in the Level 2 System. Transmitter and Receiver optical bandwidth are specified at 100 MHz. Therefore the optical fiber's bandwidth must be sufficient to pass 100 MHz over the desired distance.

	For Minimum Signal (Worst Case Transmission)	For Maximum Signal (Best Case Terminal)
Connector Loss (Assume 1.5 dB Per Connector at 8 Connectors)	12dB	12dB
Cable Loss (1.0dB/Km over 8Km)	<u>8dB</u>	<u>8dB</u>
Total	20dB	20dB
Transmitter Optical Output	-16dBm	-13dBm
Optical Input to Receiver	-36dBm	-33dBm
Receiver Sensitivity	<u>-40dBm</u>	<u>-40dBm</u>
Margin	4dB	7dB
Receiver Dynamic Range	24dB	24dB

Figure 3.3.2.1.1-1 8 Km System Link Power Budget

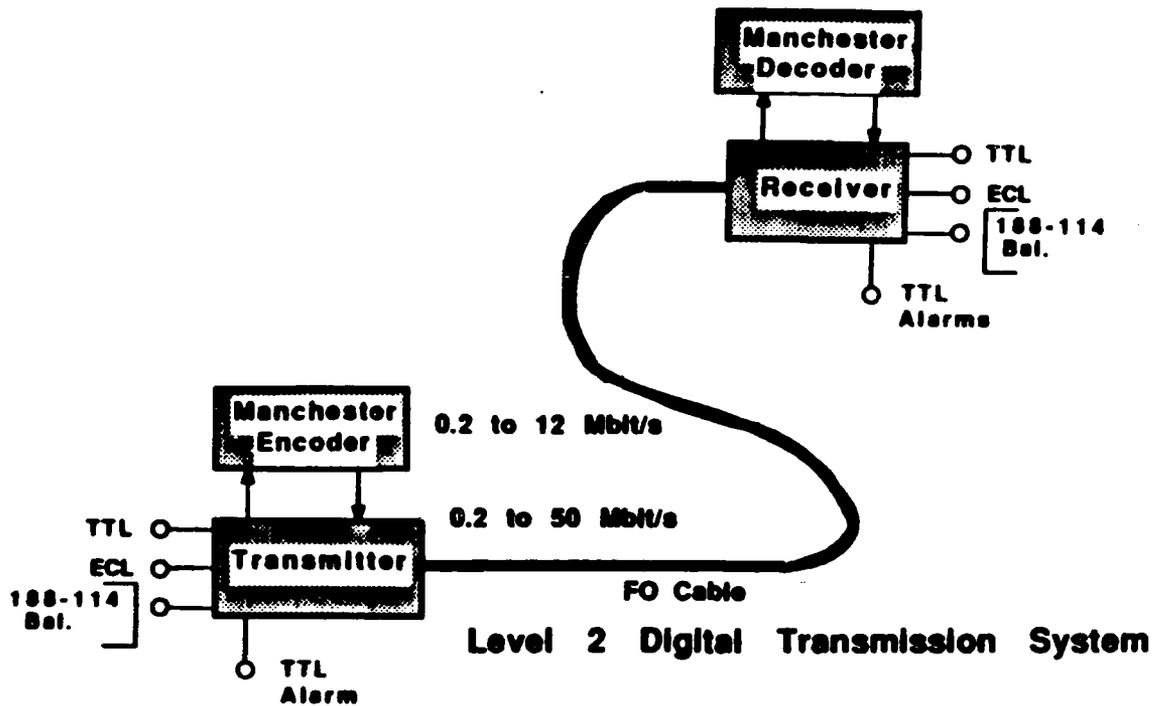
3.3.2.1.2 Alarm Considerations

Seven alarm signals are made available to the host system for the monitoring of the fiber optic link. All alarm test points reside in either the transmitter or the receiver, but fault isolation to the encoder and decoder is provided for.

The transmitter has four alarms. The first fault isolates the LED, the second the MIL-STD-188-114 and TTL interfaces, the third the ECL and Encoder interfaces while the fourth is a single test point for convenient monitoring of the other three.

The receiver has three alarms. The first fault isolates to the optical input, the second isolates the decoder while the third is a single test point for convenient monitoring of the other two.

3.3.2.2 System Diagram

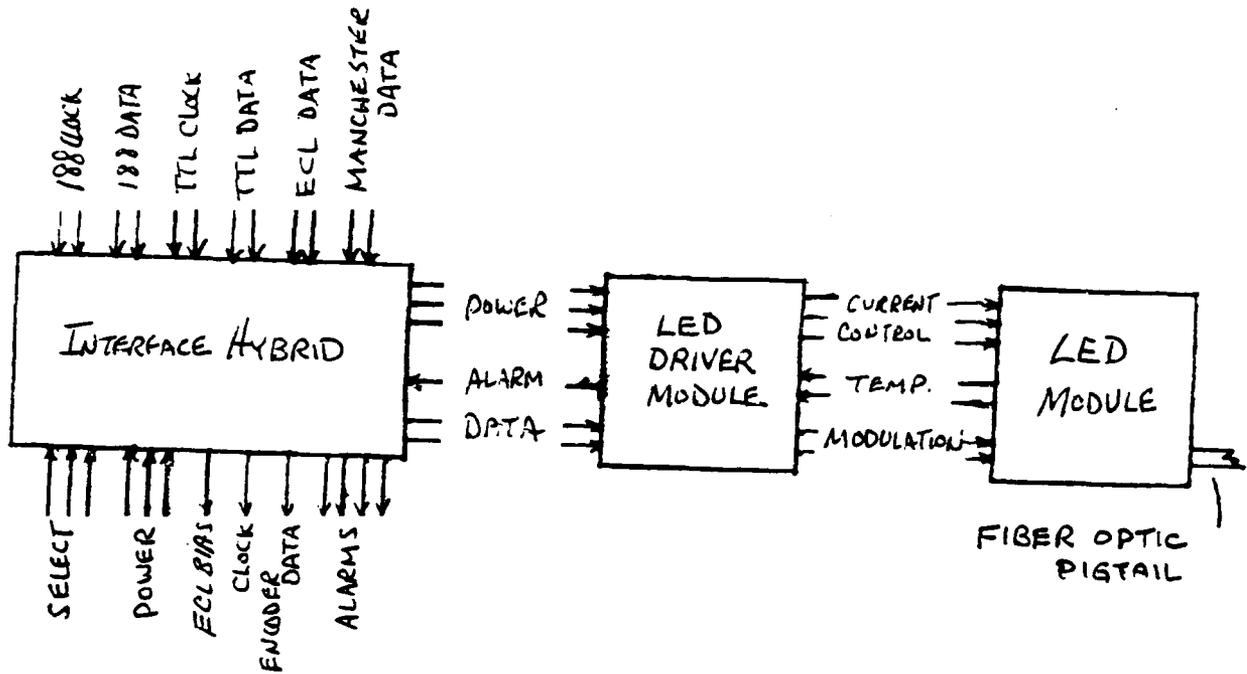


3.3.2.2.1 Transmitter Description and Diagram

The transmitter consists of the Interface hybrid, the LED Driver module and the LED module as shown in the block diagram of Figure 3.3.2.2.1-1.

3.3.2.2.1-1. The Interface hybrid handles all alarm signals, provides filtered power to all transmitter circuits and passes digital data from a host system, an encoder or a modulator to the LED driver module. The Select inputs determine which transmitter interfaces are active. The LED Driver module modulates the LED and monitors the LED status. The amplitude of the LED current is adjusted to insure that the LED power dissipation and optical output do not exceed specifications. The LED module contains the LED and the temperature sensing and current biasing elements.

Figure 3.3.2.2.1-1



3.3.2.2.1.1 Driver and LED Assemblies

A detailed description of the Level 2 transmitter driver and LED assemblies is unnecessary since they are identical to the Level 1 subsystem in every respect except data bit rates and optical output power limits. The Level 2 sheet below shows this, viz.

MFOX Level 2 Transmitter Subsystem Performance

Mechanical

Operating Temperature Range:	-46° to +52°C
Sealing:	Hermetic
Package Types:	Custom
Emitter:	Edge Emitting LED, RCA C86013E Chip
Fiber:	1m Pigtail of 50/125um Sumitomo EG-5/1304 or Siecor 104 fitted with Strain Relief Sleeve

Electrical

Supplies: +5.0V @ 0.28A max/-5.2V @
0.045A max.

Data Input: Complementary ECL, no coding
constraints, 0.2Mbps (NRZ) to
50Mbps (Manchester)

Alarm Output: Triggered by open circuit
emitter, TTL compatible, active low

Optical

Peak Optical Power: 50uW min./100uW max. over
operating temperature range

Wavelength: Peak = 1300 +30nm
FWHM = 60nm Typ.

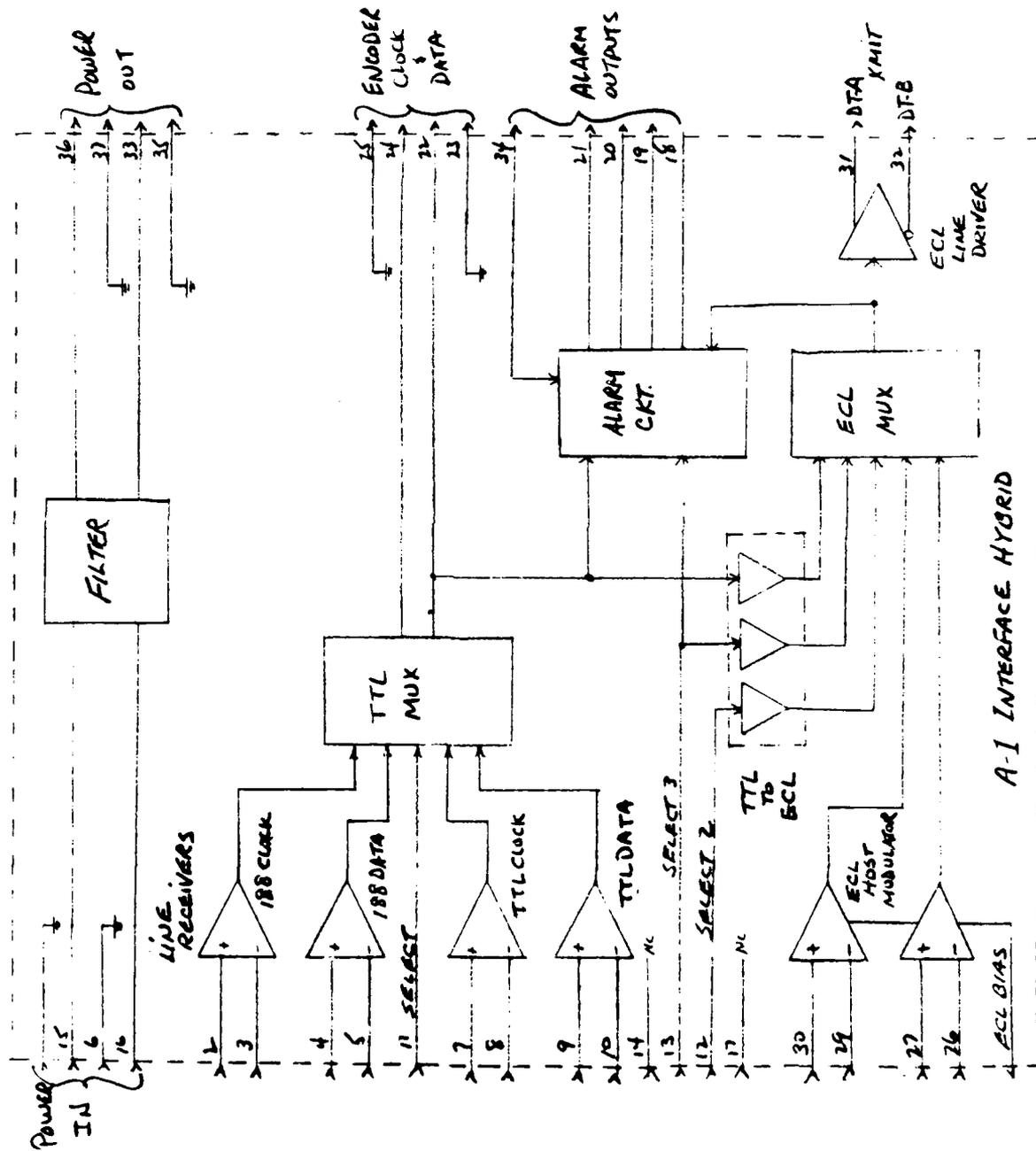
3.3.2.2.1.1.1 Level 2 Subsystem Observations

As described in Section 3.3.1.2.1.1.1.2, the optical output transitions occur in approximately 6ns which is theoretically not quite fast enough for best performance at the Level 2 maximum data rate. It was determined empirically on complete MFOX Level 2 transmission systems that this was indeed fast enough to give the transmission systems more than the required performance, however, and so was deemed to be acceptable.

Construction and testing of the Level 2 LED was identical to that of the Level 1 except that the LED chips were preselected to give the higher optical output power required.

3.3.2.2.1.2 Interface Assembly

3.3.2.2.1.2.1 Interface Assembly Block Diagram



3.3.2.2.1.2.2 Design and Tradeoffs

The Level 2 Transmitter Interface Assembly is designed for the following functions.

- o Route TTL, MIL-STD-188-114 or ECL data from the Host System to the Driver Assembly.
- o Route TTL or MIL-STD-188-114 Data and Clock from the Host System to the Encoder and ECL Manchester from the Encoder to the Driver Assembly.
- o Route frequency modulated ECL data from a modulator to the Driver Assembly.
- o Provide Alarm test points detailing transmitter, encoder or modulator status to the host system.
- o Provide filtered power to all transmitter circuits.

3.3.2.2.1.2.2.1 Data and Clock Signal Paths

The Interface Assembly's TTL and MIL-STD-118-114 line receiver inputs are shown in the block diagram. The data inputs only are used to transmit data directly from the host system to the fiber optic link while both the data and clock inputs are used to route NRZ data and clock to the encoder for Manchester formatting. One line receiver was selected that could meet both interface requirements to minimize Interface Assembly size and power requirements. The AM26LS32B integrated circuit, described previously in 3.3.1.2.1.2.2.1, contains the necessary four line receivers.

Data or Data and Clock is sent from these line receivers to the TTL multiplexor. This multiplexor is a SN54ALS157 programmed by shorting to ground or floating the Select 1 bit. The Select 1 input is TTL compatible and is pulled up to +5V through a 10K Ω resistor.

When operating with the encoder, the Mux data and clock outputs are available for connection to the encoder. In either case however, the Mux data output is monitored by an alarm circuit, described in 3.3.2.2.1.2.2.2, and is passed through the TTL to ECL converter to the ECL Mux.

The ECL Mux passes data from the TTL to ECL converter or data from one of the two ECL line receivers to the Alarm circuit and an ECL line driver. The ECL line driver interfaces to the Driver Assembly. The ECL Mux is programmed by the Select 2 and Select 3 inputs. These inputs have characteristics identical to the Select 1 input. They program the ECL Mux through the TTL to ECL converter.

One of the MC10116 ECL line receivers passes Manchester data from the encoder to the ECL Mux while the other passes Modulator or Host system data to the ECL Mux. Multiplexor programming determines the system configuration.

<u>Select 2</u>	<u>Select 3</u>	<u>ECL Multiplexor Output</u>
Grounded	Grounded	Modulator or Host ECL
Grounded	Floating	TTL or MIL-STD-188-114 Data from TTL to ECL Converter
Floating	Grounded	N/A
Floating	Floating	Encoder Manchester ECL
Select 1	TTL Multiplexor Output	
Grounded	MIL-STD-188-114	
Floating	TTL	

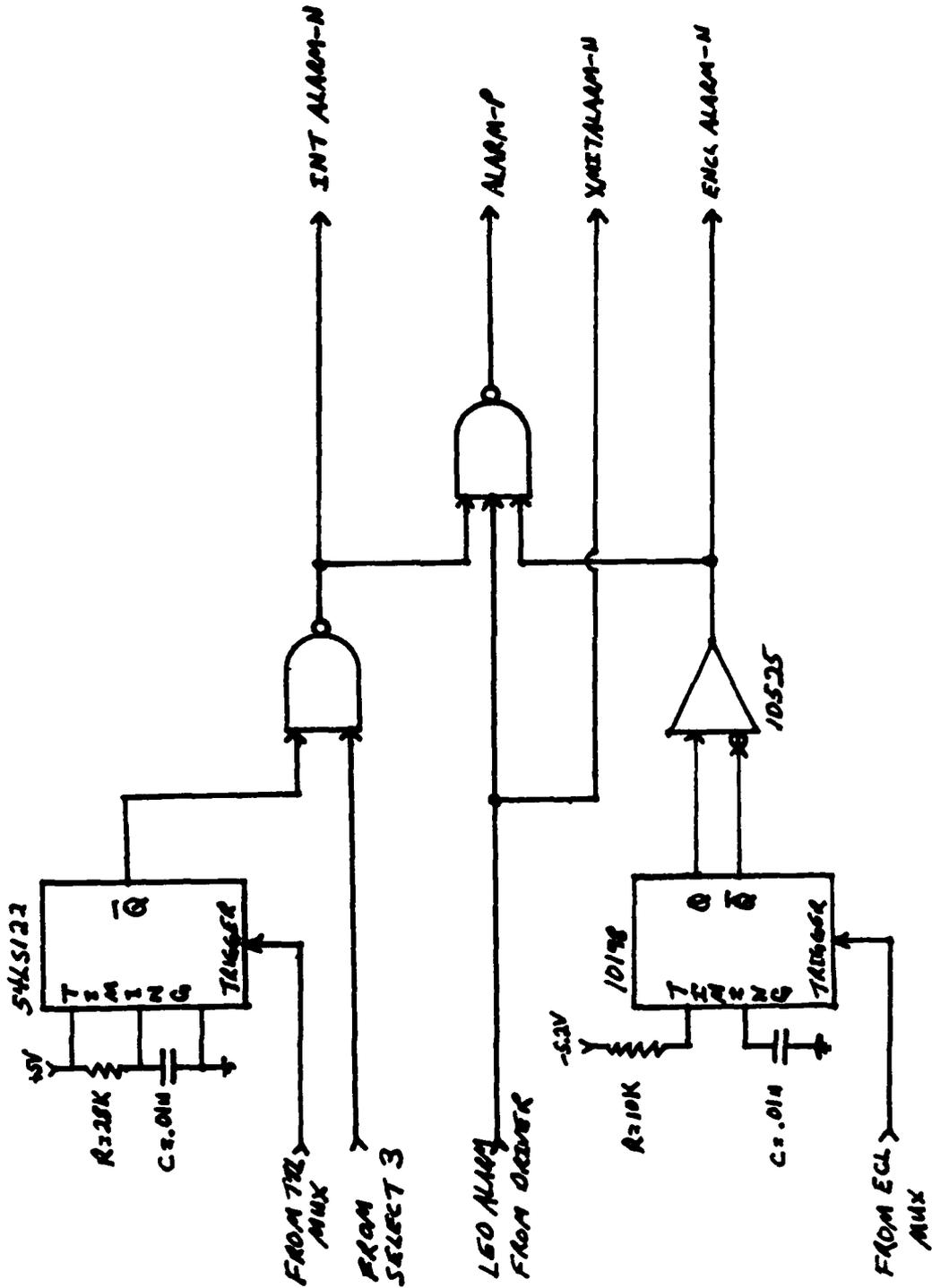
Therefore, to program the Interface Assembly to pass TTL data and clock to the encoder and Manchester data from the encoder to the Driver Assembly, all three Select inputs should be floated.

The Interface Assembly's encoder ECL line receiver input is terminated in 100 Ohms for balanced Manchester transmission. The other ECL line receiver passes balanced frequency modulated video from the modulator to the Driver Assembly or balanced or unbalanced ECL data from the host system to the Drive Assembly. Balanced interfacing should include a termination resistor equal to the characteristic impedance of the transmission line. Unbalanced transmissions should be terminated in 75 Ohms to -2V. The unused input is biased to the ECL switching threshold level of -1.29V by external connection the ECL Bias output.

3.3.2.2.1.2.2.2 Alarm Paths

The block labeled Alarm Circuit is actually a combination of several integrated circuits as shown in Figure 3.3.2.2.1.2.2.2-1.

Figure 3.3.2.2.1.2.2.2-1



The SN54LS122 timer monitors the output of the TTL Mux. If the TTL or MIL-STD-188-114 interfaces are unused (ECL from Modulator or ECL from host system interface active) the Select 3 input inhibits this alarm. The SN54LS122 monitors the rising edges of the data and has a typical time-out interval, determined by R and C of 100usec. Bit widths for the Level 2 transmission rate of 200 Kbps minimum are 5usec.

The MC10198 timer monitors all data routed to the Driver Assembly. This timer triggers on rising and falling data edges. The time-out interval is 100usec also. An ECL to TTL converter makes this alarm compatible with the other three.

The LED Alarm is merely routed from the Driver Assembly through the Interface Assembly. A combined alarm is offered for single-point fault monitoring.

3.3.2.2.1.2.2.3 Supply Filtering

The +5V and -5.2V supply inputs are filtered by the two-pole inductive-capacitive filters described in 3.2.1.1.2. The filter component values are:

+5V Supply: C1 = 0.1uF C2 = 6.8uF

L1 = 10uH

-5.2V Supply: C1 = 0.1uf

C2 = 6.8uF

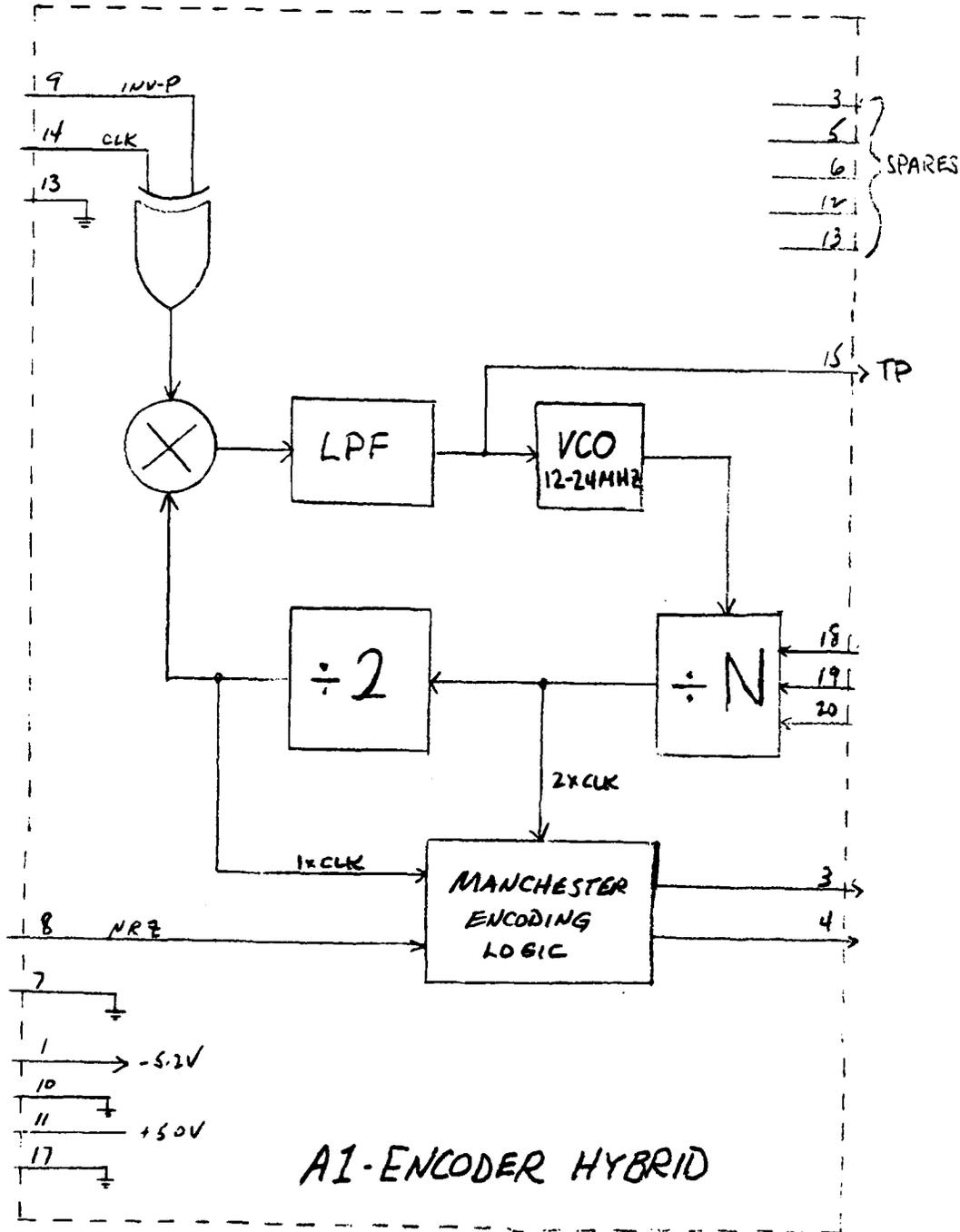
L1 = 10uH

3.3.2.2.2 Encoder Description and Diagram

The encoder is used as an optional companion unit with the transmitter to alter arbitrary NRZ data from the host system to

Manchester format. The encoder accepts clock and NRZ data fed through the transmitter from the host system and returns a Manchester encoded signal to the transmitter for optical transmission. There are four control inputs that are programmed to cover the input clock frequency range and clock-to-date phase relationship. The primary advantage of transmitting Manchester coded data over NRZ data is that Manchester's fifty percent average power optimizes the performance of the fiber optic receiver.

3.3.2.2.2.1 Encoder Block Diagram



3.3.2.2.2.2 Design and Tradeoffs

The encoder is made up primarily of the Manchester encode logic, a phase-locked loop and power supply filters.

The phase-locked loop is needed to produce the two-times clock necessary for the Manchester encoding of the NRZ data. Although the phase-locked loop is not the only method of frequency doubling, it was selected for the encoder because the same phase-locked loop circuit is needed in the decoder. This commonality between units simplifies design and manufacture. The reasons for the phase locked loop approach in the decoder are discussed in 3.3.2.2.4.

The phase-locked loop operates as follows. The clock from the host system and the phase control input are sent to an XOR gate. This gate assures the proper NRZ data to clock phase relationship. The phase control is grounded if the falling edge of the clock transition is occurring near the center of the data bit. It is floated if the rising edge occurs near the center of the data bit. The output of the XOR, which is sent to the PLL's phase detector, affects the phase of the recovered clock. The recovered clock and two times the recovered clock are used to clock in and Manchester encode the NRZ data. This phase determination feature increases the flexibility of the encoder when interfacing to a host system, since either clock-to-data phase relationship is easily accommodated.

The PLL itself consists of a phase detector, an amplifier/filter, a voltage controlled oscillator and an integer divisor. The PLL's function is to acquire the incoming clock, track it in frequency and maintain a constant output-to-input phase relationship. The phase detector compares the host system clock to

the PLL's feedback clock and generates an error voltage to maintain coincident edges. This error voltage is filtered and amplified. Filter values were chosen to optimize loop bandwidth, capture time and transient response. The PLL is designed to track input frequency variations smoothly and lock on to the initial clock input quickly.

The output of the filter/amplifier drives the voltage controlled oscillator. The VCO is programmed such that the amplified and filtered error voltage is sufficient to vary the VCO's output over a 12 MHz to 24 MHz range. This output is then divided down to two-times and one times the clock frequency. The two-times clock is used to encode the NRZ data. The one-times clock is sent to the phase detector for comparison to the host system clock. This recovered one times clock also is used to gate in the NRZ data.

The integer divisor circuitry provides a practical means of operating the PLL over a 0.2 Mbps to 12 Mbps or 60 to 1 range. The PLL itself must only be capable of little better than 24 MHz to 12 MHz or two to one, since the divisor circuitry can divide the VCO's output to any clock frequency over the operating range. This is accomplished by two D Flip Flops, a binary counter and a multiplexor. The first Flip-Flop and the counter automatically divide the VCO output as follows:

N	PLL Frequency Range
2	6 to 12 MHz
4	3 to 6 MHz
8	1.5 to 3 MHz
16	0.75 to 1.5 MHz
32	0.375 to 0.75 MHz

The output from each of these five ranges plus the direct 12 to 24 MHz VCO output is passed to the multiplexor. Three frequency select controls are then grounded and floated in the following combinations to determine the multiplexor output frequency range:

<u>Multiplexor Output</u>	<u>Frequency Rate Select</u>		
Frequency Range	A	B	C
12 to 24 MHz	Gnd	Gnd	Gnd
6 to 12 MHz	Float	Gnd	Gnd
3 to 6 MHz	Gnd	Float	Gnd
1.5 to 3 MHz	Float	Float	Gnd
0.75 to 1.5 MHz	Gnd	Gnd	Float
0.375 to 0.75 MHz	Float	Gnd	Float

The multiplexor output is the two-times clock. The one-times clock is generated by directing the two-times clock into the second FLIP-FLOP. The FLIP-FLOP output is the recovered clock. The three frequency select controls are therefore programmed as follows for the expected input clock frequency:

<u>BAUD Rate</u>	<u>Frequency</u>	<u>Rate</u>	<u>Select</u>
<u>Mbps</u>	<u>A</u>	<u>B</u>	<u>C</u>
6 to 12	Gnd	Gnd	Gnd
3 to 6	Float	Gnd	Gnd
1.5 to 3	Gnd	Float	Gnd
0.75 to 1.5	Float	Float	Gnd
0.375 to 0.75	Gnd	Gnd	Float
0.2 to 0.375	Float	Gnd	Float

This covers the entire encoder specified operating frequency range.

The Manchester encode logic and timing diagram is shown in

3.3.2.2.2.2-1. Inverted one-times clock gates the NRZ data into a D Flip-Flop. The Q output is now synchronized with the non-inverted recovered clock. Both are routed to an XOR for Manchester encoding. The XOR output is converted to ECL and is input to an ECL D Flip-Flop. The two-times clock re-clocks the Manchester data to the Flip-Flop Q and \bar{Q} outputs. This is the balanced ECL to be sent to transmitter for optical transmission over the fiber optic link. Balanced ECL was chosen for its low pulse distortion characteristics.

The +5V and -5.2V supply inputs are filtered by the two-pole inductive-capacitive filters discussed in 3.2.1.2.2. The filter component values are:

+5V Supply	C1 = 0.1uF
	C2 = 6.8uF
	L1 = 50uH

-5.2V Supply	C1 = 0.1uF
	C2 = 6.8uF
	L1 = 50uH

3.3.2.2.3 Receiver Description and Diagram

The receiver consists of a Threshold module, a Preamplifier module and a power supply filter mounted on a printed circuit board (PCB), and the Interface hybrid as shown in the block diagram of Figure 3.3.2.2.3-1. The Preamplifier module outputs an analog voltage to the Threshold module that is proportional to the incoming optical signal. The Threshold module converts the preamplifier output to a digital signal and passes this signal as well as alarm status

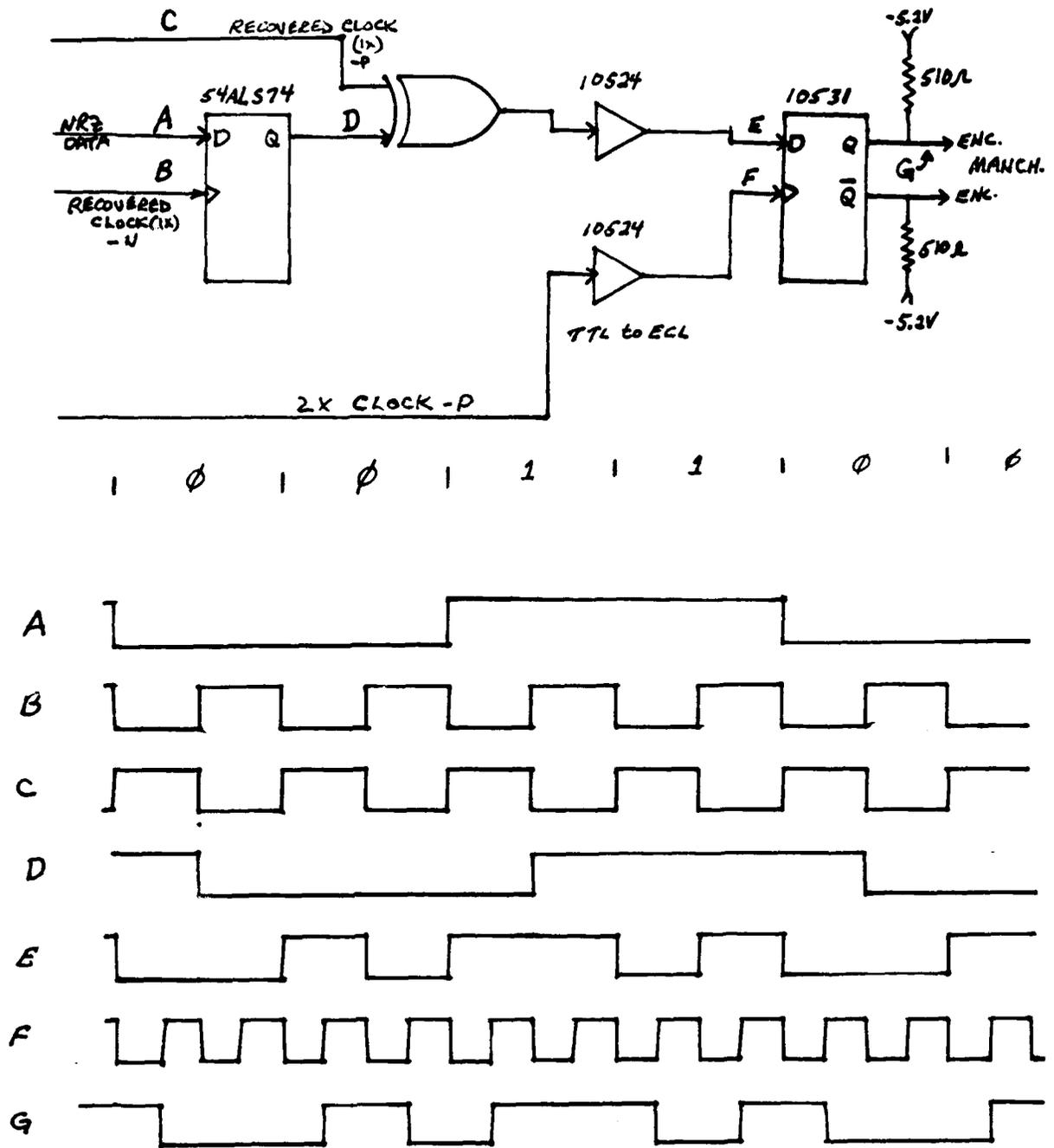


Figure 3.3.2.2.2.2-1

information to the Interface hybrid. The Interface hybrid handles all alarm signals, passes the digital data to the host system, a decoder or a demodulator and provides filtered power to all receiver circuits.

The Interface Assembly filter is described in 3.3.2.2.3.2. The printed circuit board mounted filters are simple one-pole resistive-capacitive types designed to isolate the PINFET pre-amplifier +5V and -5.2V supplies. The PINFET is a high gain analog device, susceptible to supply transients that could cause sensitivity degradation. This type of filter was chosen over the inductive-capacitive type because it exhibits no resonant frequency peaking and the filter resistors induce negligible voltage drops while operating effectively over a wide frequency range.

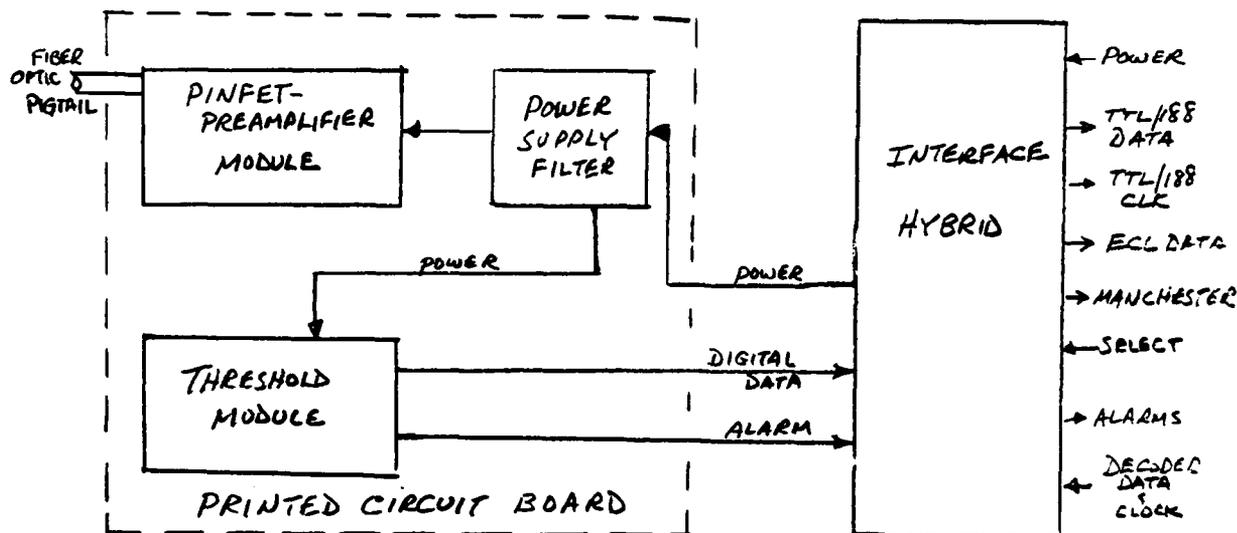


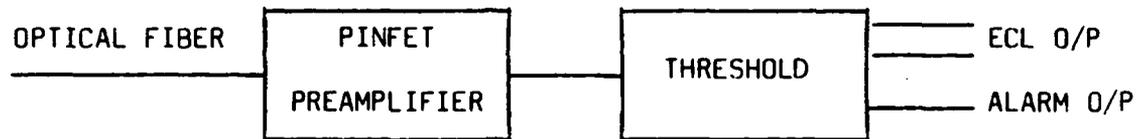
Figure 3.3.2.2.3-1

3.3.2.2.3.1 Threshold and PINFET Assemblies

3.3.2.2.3.1.1 E/O Subsystem

3.3.2.2.3.1.1.1 Description of the Subsystem

3.3.2.2.3.1.1.1.1 Level 2 E/O Subsystem Block Diagram



3.3.2.2.3.1.1.1.2 PINFET Function

The purpose of the pinfet is to transform the optical power coming out of the fiber cable into an electrical signal. The modules used were standard product from RCA - the C30986 series. This unit is a transimpedance preamplifier module using a low noise GaAs FET front end, and a cascade configuration to minimize the input capacitance. The p-i-n photodiode (C30979) used in these devices is a high speed Indium Gallium Arsenide/Indium Phosphide providing high responsivity between 900 and 1700 nm.

3.3.2.2.3.1.1.1.3 Threshold Function

The purpose of the threshold units is to transform the analog output of the pinfet into a digital signal. The modules also provide an alarm signal which is activated when the optical power goes under a specified level.

3.3.2.2.3.1.1.2 Pinfet

3.3.2.2.3.1.1.2.1 Approach/Tradeoffs

The design work for the MFOX project consisted of selecting the appropriate feedback and internal gain resistors, in order to achieve the various system requirements.

In a transimpedance receiver the choice of the feedback resistor is extremely important since it will determine several characteristics

of the module. The internal gain resistor is selected in conjunction with the feedback resistor. The internal gain adjustment is necessary to fine tune the frequency response, or put differently; the second order transfer function of the transimpedance is optimized by varying the open loop gain.

The following equations show the impact of the feedback resistor (R_F) on the module performances:

$$\text{Responsivity (R)} = 0.7 * 0.95 * R_F \quad \propto R_F$$

$$\text{Output spectral noise (N}_V) \quad \propto \sqrt{R_F}$$

$$\text{NEP} = \frac{N_V}{R} \quad \propto \frac{1}{\sqrt{R_F}}$$

$$\text{Bandwidth (BW)} = \frac{A_{in}}{2\pi C_{in} R_F} \quad \propto \frac{1}{\sqrt{R_F}}$$

$$\text{Sensitivity} = 10 \log \frac{6N_V \sqrt{BW}}{R} \quad \propto \log \frac{1}{\sqrt{R_F}}$$

$$\text{Overload point} = 10 \log \frac{V_{MAX}}{R} \quad \propto \log \frac{1}{\sqrt{R_F}}$$

These formulas show that with increasing R_F , we improve the responsivity, NEP and sensitivity figures. However, on the other hand we get reduced bandwidth as well as a lower overload point.

Therefore, the choice of the feedback resistor will be governed by the respective system specifications.

3.3.2.2.3.1.1.2.2 Design Steps and System Requirements

Bit rate = 0.2 Mbps (NRZ) to 50 Mbps (Manchester) which gives a minimum bit time of 10 ns (50 Mbps in Manchester data format). The

maximum rise and minimum bandwidth are as follows:

$$\text{Rise time} = t_r < 0.7 * 10 \text{ ns} = 7\text{ns}$$

$$\text{Bandwidth} = \text{BW} > \frac{0.35}{t_r} = 50 \text{ MHz}$$

The sensitivity requirement is -41 dBm and the dynamic range is 24 dB; for an overload point of -17 dBm. Again, keeping these specifications in mind, we will go through the feedback resistor calculation.

$$\text{Overload point} = -17 \text{ dBm} = 10 \log \frac{V_{AVE\text{max}}}{R_{\text{max}}}$$

The maximum voltage at the output of the pinfet before saturation is 2.5 V_{p-p}. For a 50% duty signal the maximum average voltage will then be 1.25 volts.

$$-17 \text{ dBm} = 10 \log \frac{1.25}{R_{\text{max}}}$$

$$R_{\text{max}} = \text{Responsivity} = 63 \text{ Kv/W}$$

$$\text{Responsivity} = 0.7 * 0.95 * R_{F\text{max}} = 63 \text{ Kv/W}$$

$$R_{F\text{max}} = 94 \text{ K}\Omega$$

For the Level 2 system, the maximum value of R_F could be limited by the bandwidth relation instead of the overload point; let's check:

$$\text{BW} = 50 \text{ MHz} = \frac{A_{\text{in}}}{2\pi C_{\text{in}} R_{F\text{max}}} = \frac{27 \text{ mS} * 1\text{K}\Omega}{2\pi (1.2\text{pf}) R_{F\text{max}}}$$

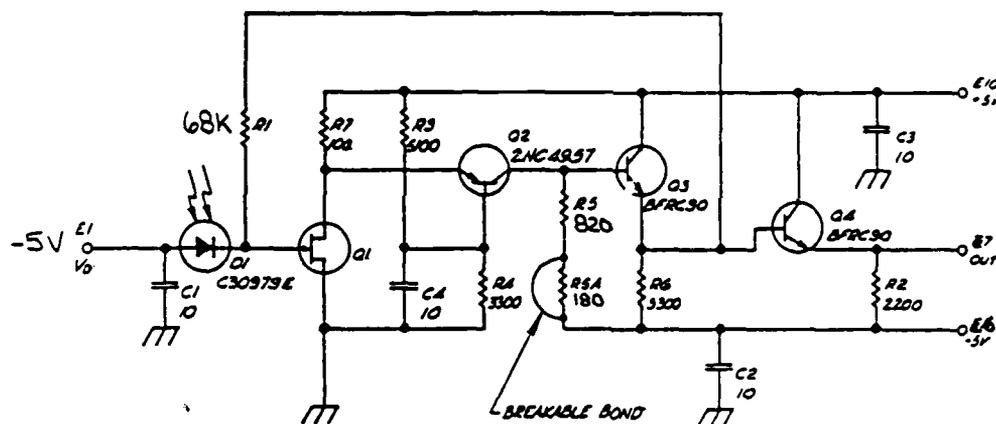
$$R_{F\text{max}} = 72 \text{ K}\Omega$$

As expected the limiting factor is the bandwidth. We will select a feedback resistor of 68K and determine the theoretical sensitivity. A theoretical analysis of the output spectral noise voltage density gives a typical value of 50 nV/ Hz. And finally the projected sensitivity at 10^{-9} BER is:

$$\text{Sensitivity} = 10 \log \frac{6 (50\text{nV}/\sqrt{\text{Hz}}) \sqrt{70 \text{ MHz}}}{68 \text{ K}\Omega * 0.95 * 0.7} = -42 \text{ dBm}$$

Since all the system specifications are met, the choice of 68K Ω as the feedback resistor, is adopted.

3.3.2.2.3.1.1.2.3 Pinfet Schematic

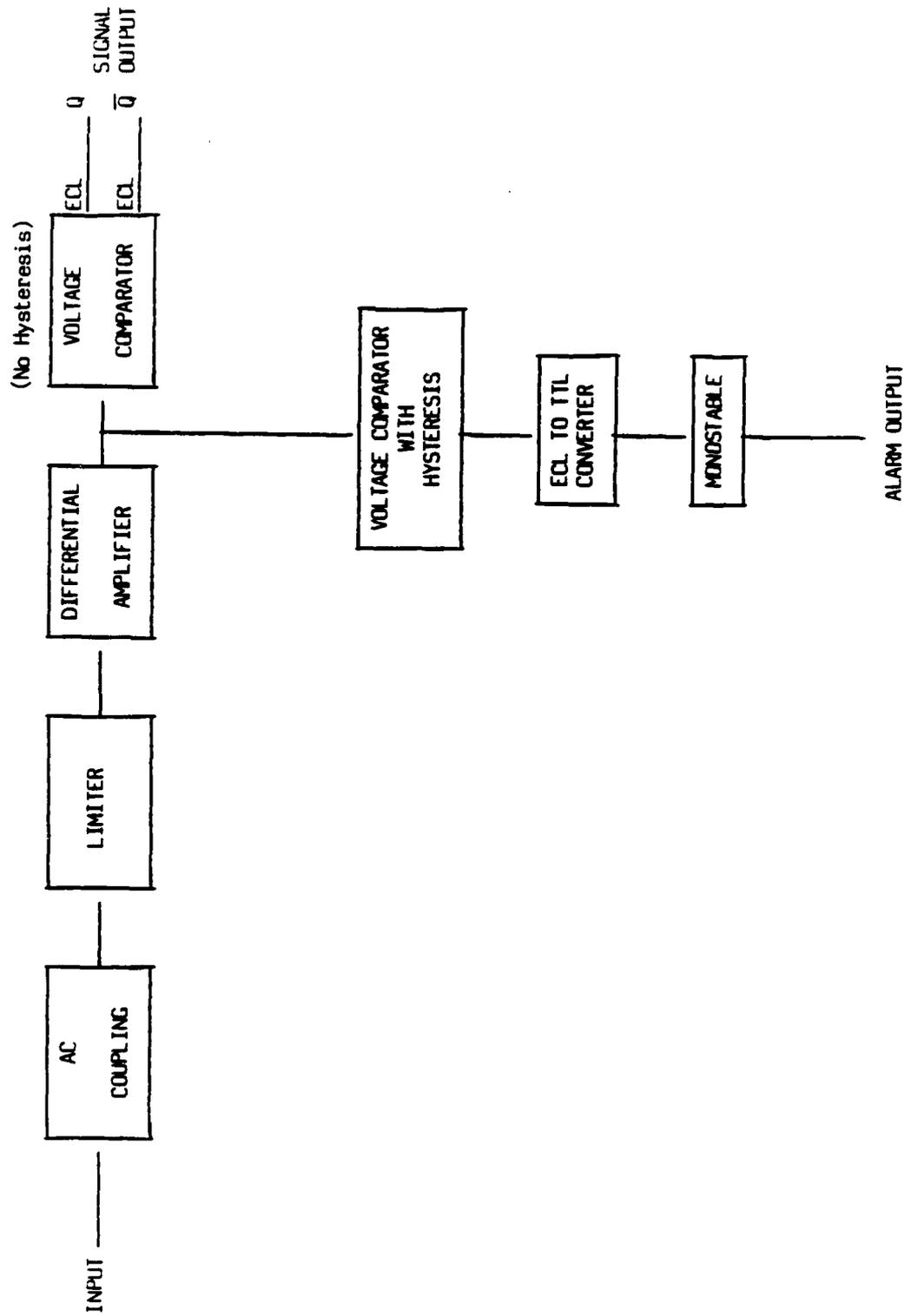


3.3.2.2.3.1.1.2.4 Pinfet Package

The pinfet is supplied in a hermetically sealed 14-pin dual in-line package. The package mechanical characteristics are described in RCA drawing #2545063-3.

The optical fiber is attached to the case using epoxy and torr seal. The alignment of the fiber is done by monitoring the photocurrent of the detector. For detailed description of the pigtailling steps consult RCA procedure P4122.

3.3.2.2.3.1.1.3.1 Threshold Level 2 Block Diagram



3.3.2.2.3.1.1.3.2 Design and Tradeoffs

The following description of the C30615E will explain the design steps and tradeoffs that led us to the final configuration. Figure 3.3.2.2.3.1.1.3.1 and RCA drawing #2580454 are the reference documents for this section.

The first component in the block diagram is the AC coupling. Since the Level 2 system is operated with 50% duty cycle data, it is permitted to use AC coupling without having to worry about base line variations.

After the coupling capacitor (C1) we find an amplitude limiter circuit, which is needed to cover the full 24 dB of dynamic range. The limiter consists of two back to back Schottky diodes. R7 is used as a current limiter when one of the diodes is turned on.

The sensitivity specification is -41 dBm, which represents at the output of the pinfet a signal of 6.8 mV_{p-p}. This very small signal should be amplified before being fed to the voltage comparator and the alarm circuit. This amplification is taken care of by a differential amplifier (Q1 and Q2) with a differential gain of 10.

$$(1) \text{ Sensitivity} = -41 \text{ dBm} = 10 \log \frac{V_{\text{min-p}}/2}{\text{Responsivity}}$$

$$\text{where responsivity} = 68 \text{ K}\Omega \cdot 0.7 \frac{\text{A}}{\text{W}} \cdot 0.9 = 43 \text{ kV/W}$$

$$\text{we get } V_{\text{min}} = 6.8 \text{ mV}_{\text{p-p}}$$

(2) Differential amplifier gain:

$$\frac{V_o}{V_{\text{in}}} = \frac{R_2}{R_3 + \frac{26 \text{ mV}}{I_{C_1}}} = \frac{510}{33 + \frac{26 \text{ mV}}{1.5 \text{ mA}}} = 10$$

The outputs of the differential amplifier are fed into two buffers, represented by Q3 and Q4. These buffers are necessary in order to get a precise gain from the amplifier.

At the emitters of Q3 and Q4 there are two signal paths; one to a voltage comparator, and the other to the alarm circuit. Let's take the first one. The combination of C7-R12 or C6-R11 make a high pass filter whose low frequency cut off must be below 50 KHz (acceptance criteria).

$$f_c = \frac{1}{2\pi C6 \cdot (R11 \parallel R_{IN})} = \frac{1}{2\pi \cdot 68nf \cdot (4.75K \parallel 6K)} = 883 \text{ Hz}$$

It is important to note that C6 and C7 are necessary to cancel the DC offset that could be present at the output of the differential amplifier.

The next block is the voltage comparator. Because the maximum frequency of operation is 50 MHz we needed a high performance voltage comparator, preferably with ECL output. The AM685 from Advance Micro Devices respected all our requirements (speed 6.5 ns and complementary ECL output). This voltage comparator is used in an open loop configuration because we couldn't afford to lose any sensitivity with a hysteresis. This means that when no signal is present the comparator will be randomly switched by noise. Finally the AM685 provides the complementary ECL output to the user.

Now, going back to the emitters of Q3 and Q4, we will take the alarm path. As mentioned in the previous paragraph, we couldn't afford to have a hysteresis on the signal path. However, in order to differentiate signal from noise, the alarm circuit needed a

hysteresis. The implication of this is an alarm circuit which is less sensitive than the ECL output. The calculation of the resistor values (R19, R20) is not trivial because the Q & \bar{Q} output do not have symmetrical swing due to the special loading of the Q output. This is why the value of the hysteresis was determined experimentally in order to obtain maximum sensitivity as well as good noise rejection.

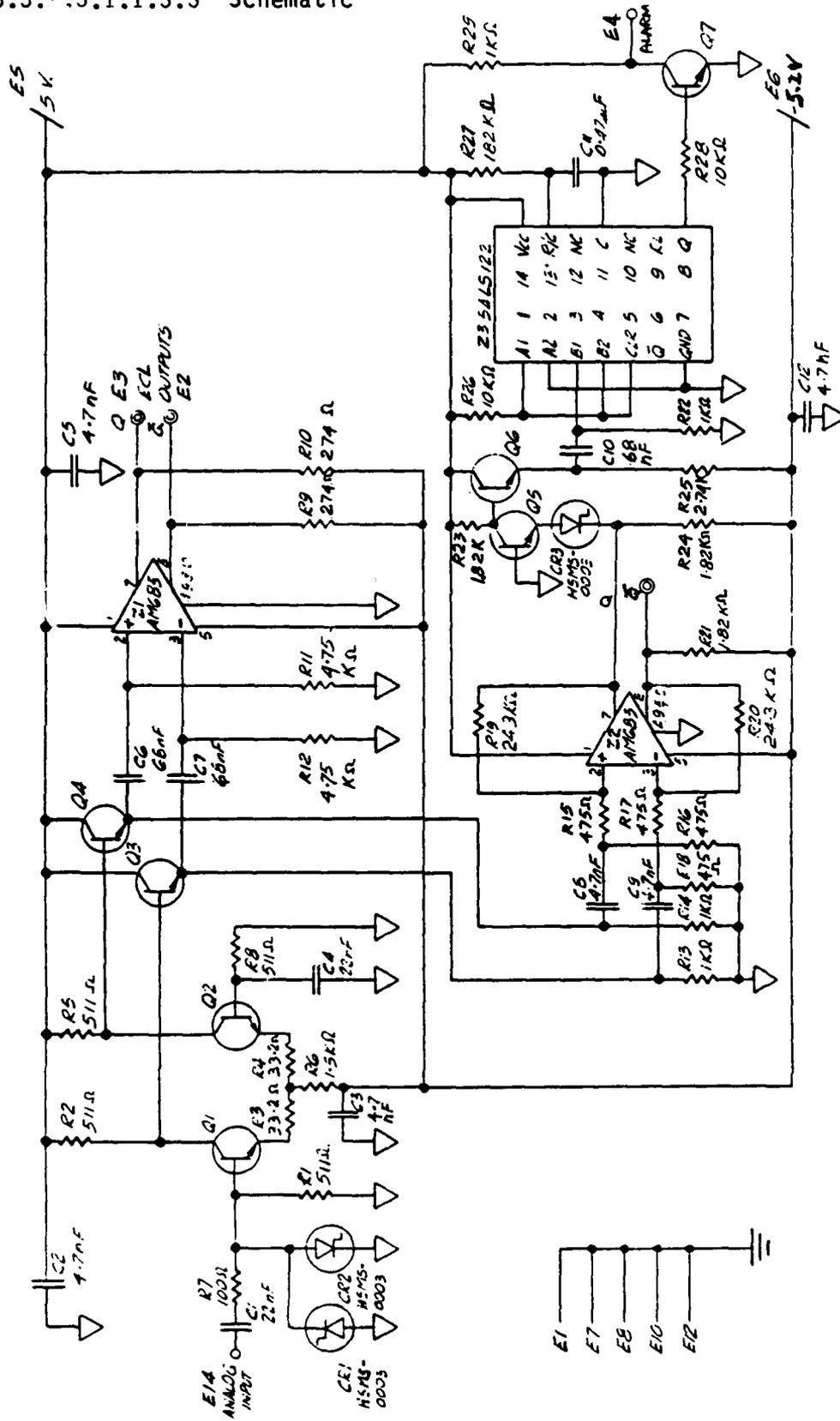
The next block in line is the ECL to TTL converter. This component is necessary since the monostable works only with TTL logic levels. The conversion is done by switching transistor Q5 at the appropriate levels, with the help of Schottky diode CR3.

Finally, the last component in the block diagram is the monostable. The monostable controls the alarm output. As long as the voltage comparator sends data, the monostable is triggered and gives out a pulse of a certain duration. If no data are received for a period longer than the time constant (t_w) the alarm output changes state to signify a loss of communication. The time constant of the alarm signal (t_w) has been maximized in order to avoid false alarm at low data rate.

$$t_w = 0.32 * R10 * C6 \left[1 + \frac{0.7}{R10} \right]$$

$$= 0.32 * 182K\Omega * 0.47 \mu F \left[1 + \frac{0.7}{R10} \right] = 27 \text{ mS}$$

3.3.2.3.1.1.3.3 Schematic



NOTE: TRANSISTOR Q1 TO Q7 ARE 2N2857

3.3.2.2.3.1.1.3.4 Packaging

The Level 2 threshold is supplied in a hermetically sealed 14-pin dual in-line package. The package mechanical characteristics are described in RCA drawing 2580474.

3.3.2.2.3.1.1.4 Test Result Vs. Acceptance Criteria

In order to show that the specifications were met by the pinfet, the threshold, and their combination (pinfet + threshold = receiver; here are some tables that compare actual test results with the acceptance criteria.

3.3.2.2.3.1.1.4.1 Pinfet

@ 25°C	Acceptance Criteria			Test Results				Units
	Minimum	Typical	Max	Minimum	Maximum	Mean	STD DEV	
Responsivity @ 1.3 um	4x10 ⁴	5x10 ⁴	---	4.5x10 ⁴	5.4x10 ⁴	5x10 ⁴	0.27x10 ⁴	V/W
Output Spectral Noise Voltage Density Integrated Over the Bandwidth	---	50	70	44	57	48	4	nV/ Hz
Bandwidth	70	90	---	90	100	93	3	MHz
Overload Point	-17	--	---	-16.3	-14.7	-15.4	0.4	dBm
Dark Current	---	15	30	3	16	7	3	nA
Sensitivity	-41.5	-43	---	-41.5	-43.0	-42.4	0.4	dBm

3.3.2.2.3.1.1.4.2 Threshold

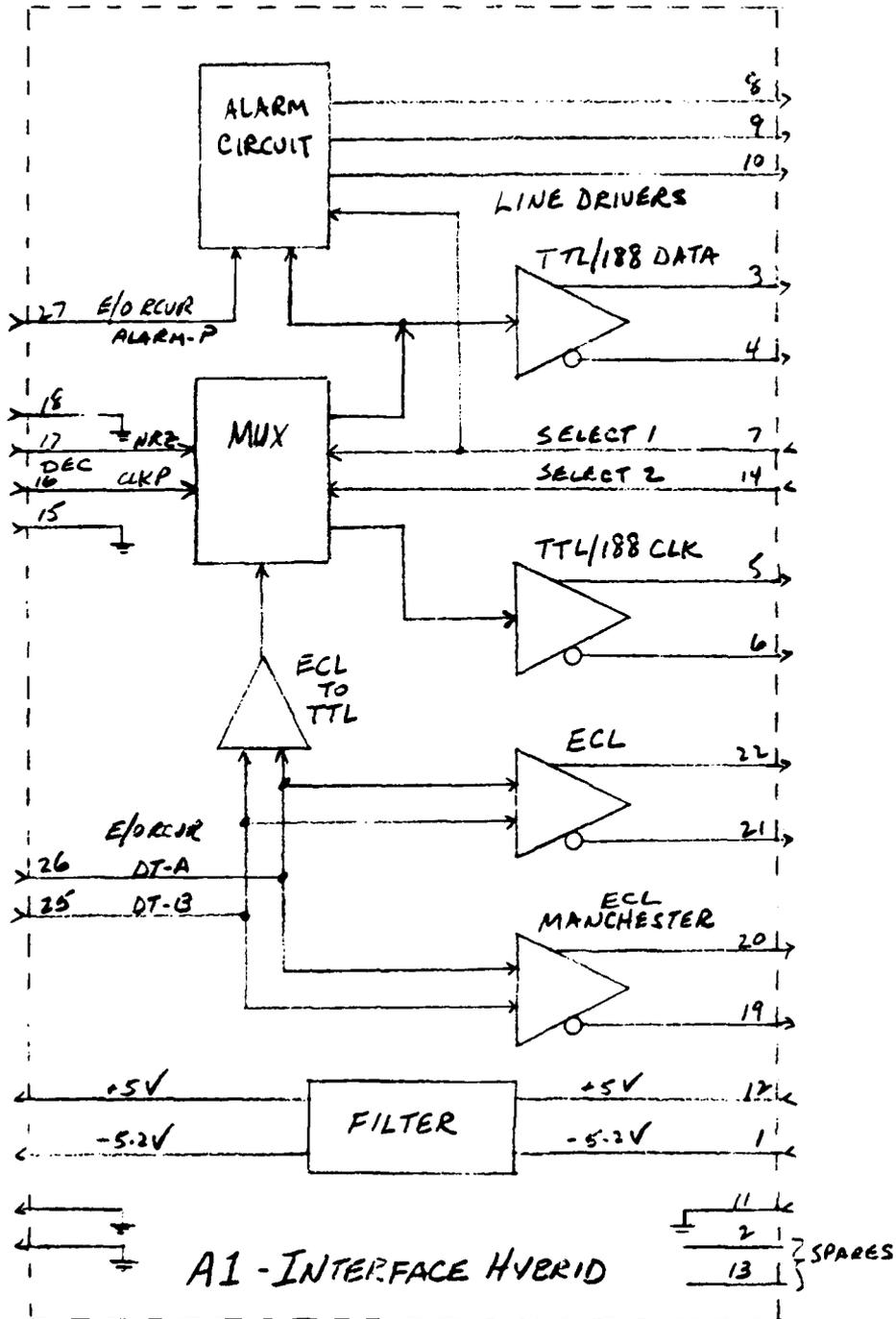
	<u>Acceptance Criteria</u>			<u>Test Results</u>				Units
	Min	Typ	Max	Min	Max	Mean	STD DEV	
<u>Alarm</u>								
- Minimum Toggling Level @ 50 MHz (SQW)	-	-	-	13.7	16.0	14.5	0.7	mV _{p-p}
- Minimum Data Rate (SQW), Pin = -41 dBm	50	-	-	27	32	28	2	KHz
<u>ECL O/P</u>								
- Minimum Toggling Level @ 50 MHz (SQW)	-	5.0	6.8	3.7	6.7	4.5	1	mV _{p-p}
- Minimum Data Rate (SQW), Pin = -41 dBm	50	-	-	13	17	16	0.9	KHz
Power Consumption:								
I ⁺	-	85	130	54	59	56	1.4	mA
I ⁻	-	93	130	78	81	79	0.75	mA

3.3.2.2.3.1.1.4.3 Receiver

	<u>Acceptance Criteria</u>			<u>Test Results</u>				Units
	Min	Typ	Max	Min	Max	Mean	STD DEV	
- Minimum Toggling Level @ 50 MHz (SQW)	-	-	-	8.7	13.0	11.2	1.3	mV _{p-p}
- Minimum Data Rate (SQW), Pin = -14 dBm	50	-	-	35	152	81	36	KHz
<u>ECL O/P</u>								
- Minimum Toggling Level @ 50 MHz (SQW)	-	5.0	6.8	3.4	6.5	5.2	1.1	mV _{p-p}
- Minimum Data Rate (SQW), Pin = -41 dBm	50	-	-	11	32	19	5.3	KHz
Power Consumption:								
I ⁺	-	85	130	81	85	82	1.4	mA
I ⁻	-	93	130	87	90	89	1.2	mA

3.3.2.2.3.2 Interface Assembly

3.3.2.2.3.2.1 Interface Assembly Block Diagram



3.3.2.2.3.2.2 Design and Tradeoffs

The Level 2 Receiver Interface Assembly is designed to perform the following functions:

- o Route data from the Threshold Assembly to TTL, balanced MIL-STD-188-114, or ECL interfaces.
- o Route ECL Manchester from the Threshold Assembly to the Decoder and Data and Clock from the Decoder to TTL or MIL-STD-188-114 interface.
- o Route frequency modulated ECL data to the Demodulator.
- o Provide alarm test points for receiver, decoder and demodulator troubleshooting.
- o Provide filtered power to all receiver circuits.

3.3.2.2.3.2.2.1 Signal Paths

The Threshold Assembly's balanced ECL data output is sent to three separate Interface Assembly line receivers. Two of these receivers are contained in the MC10116 line receiver integrated circuit. These line receivers are able to drive balanced or unbalanced ECL transmission lines, and are employed as the ECL interfaces from the receiver to the decoder, demodulator and host system. One line receiver is dedicated to interfacing Manchester data to the Decoder. The other doubles as the host system 0.2 to 50 Mbps data interface as well as the Demodulator interface. These interfaces are always active and are non-selectable. To interface ECL to the host system, decoder or demodulator, the connections are made and no select programming is necessary, other than for the purposes of disabling the TTL/188 line drivers in the case of host ECL or demodulator interfacing or enabling the decoder NRZ data and clock

interfaces in the case of decoder operation. The ECL interfaces do not have a disable feature because the increase in circuit complexity and overall receiver size was not justifiable for the limited benefits gained.

The third line receiver interfaced to the Threshold Assembly is the ECL to TTL converter. The converter output and the decoder TTL NRZ data and clock interfaces are directed to the multiplexor.

This multiplexor, programmed by two select bits, routes either the converted ECL data or the decoder data and clock to the combination TTL/MIL-STD-188-114 line drivers.

The select bits are TTL compatible and pulled up to +5V through 10K resistors. As such programming of the Mux is accomplished through various combinations of grounding and floating these select inputs as follows:

<u>Select 1</u>	<u>Select 2</u>	<u>Multiplexor Output</u>
Grounded	Grounded	Data from ECL to TTL Conv.
Grounded	Floating	Disabled
Floating	Grounded	NRZ Data and Clock from Decoder
Floating	Floating	N/A

The select inputs should never both be floating. Floating the Select 1 input enables the decoder alarm circuitry as explained in 3.3.2.2.3.2.2.2. Since no decoder data or clock can pass through the Mux when both selects are floated, the alarm will always be activated. With this in mind compare the following recommended interface programming to the Mux programming.

<u>Select 1</u>	<u>Select 2</u>	<u>Interface Recommendations</u>
Grounded	Grounded	Optical Input to TTL/188 Data Driver
Grounded	Floating	Optical Input to Host/Demod ECL Driver
Floating	Grounded	Optical Input to Decoder ECL Driver and Decoder Data and Clock to TTL/188 Drivers
Floating	Floating	None

The combination TTL/188 line drivers are SN55114's the same as those used in the Level 1 Receiver. Their characteristics are described in 3.3.1.2.2.2.3.

3.3.2.2.3.2.2.2 Alarm Paths

The alarm circuit details are shown in Figure 3.3.2.2.3.2.2.2-1.

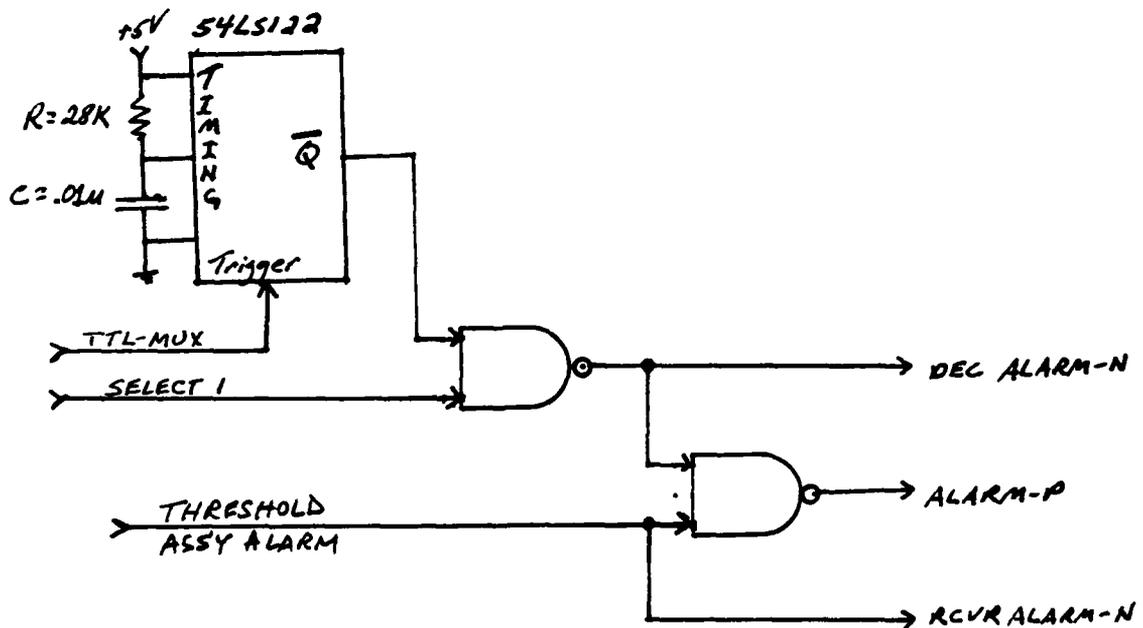


Figure 3.3.2.2.3.2.2.2-1

The timer output is low when triggered by incoming NRZ data from the decoder. The timer is triggered only by the rising edges of the data and has a time-out interval averaging 100 usec. Data pulses or runs of identical data pulses cannot be longer than 100 usec if the alarm is to operate properly. At a 0.2 Mbps minimum NRZ data rate, pulse widths are 5 usec. The timer will therefore not time-out for normal data transmission. This timer monitors data from the decoder and alerts the user to a fault by switching its output from a Logic 0 to a Logic 1. A NAND gate, enabled by the floating Select 1 input inverts and passes this signal to the user.

Select 1 is always floating when the receiver is used in conjunction with the decoder and is grounded otherwise. When grounded the NAND gate outputs a constant Logic 1 or non-alarmed condition.

The alarm from the Threshold Assembly is described in 3.3.2.2.3.1. It is merely routed through the Interface Assembly to the host system. A second NAND gate monitors this alarm and the decoder alarm for convenience in fault monitoring.

3.3.2.2.3.2.2.3 Supply Filtering

The +5V and -5.2V supply inputs are filtered by the two-pole inductive-capacitive filters described in 3.2.1.1.2. The filtered component values are:

+5V Supply: C1 = 0.1uF

C2 = 6.8uF

L1 = 50uH

-5.2V Supply: C1 = 0.1uF

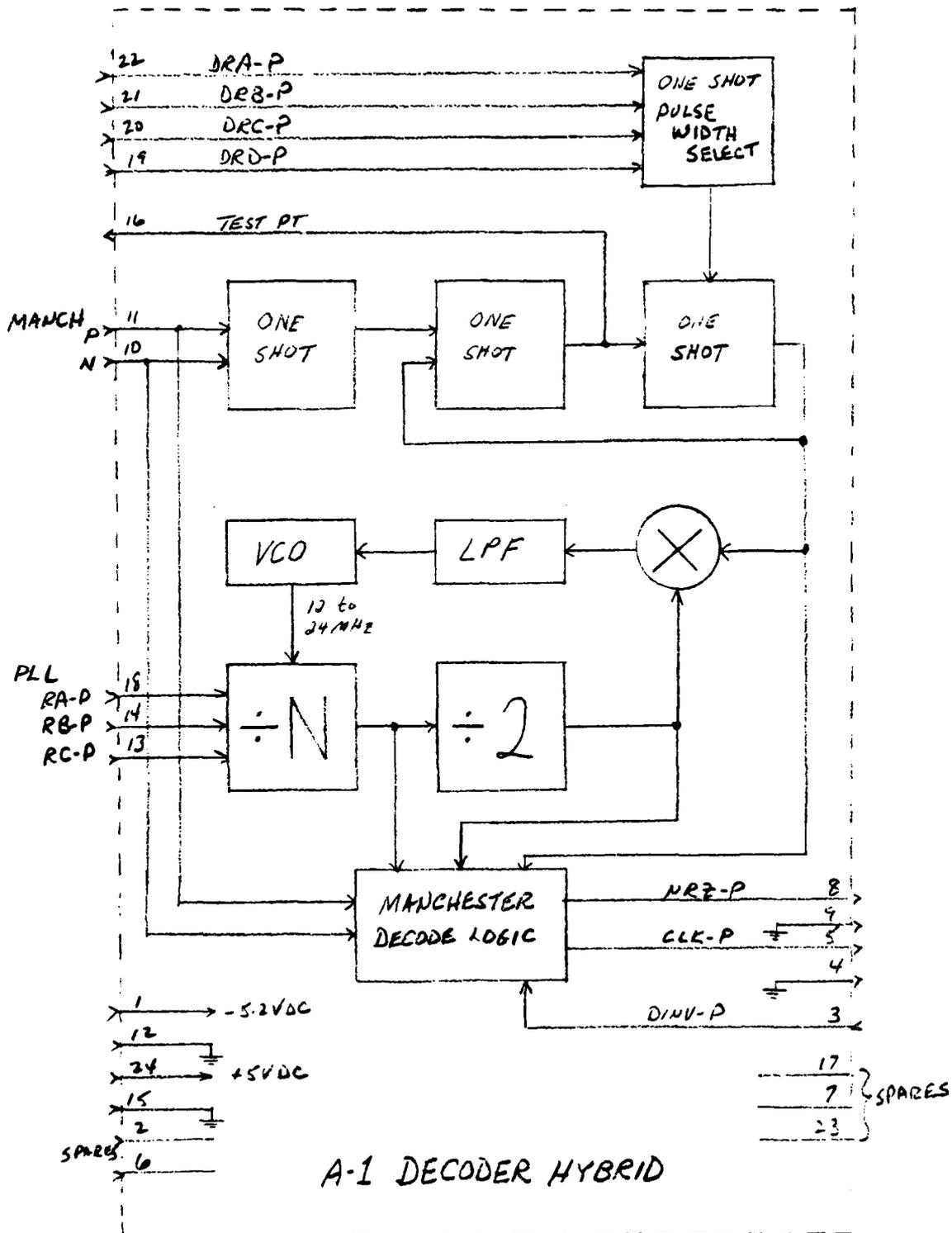
C2 = 6.8uF

L1 = 50uH

3.3.2.2.4 Decoder Description and Diagram

The decoder is used as an optional companion unit with the receiver to alter Manchester data to arbitrary NRZ data and clock. The decoder accepts Manchester data from the receiver and returns NRZ data and clock through the receiver to the host system. There are eight control inputs that are programmed to cover the output clock frequency range and clock-to-data phase relationship.

3.3.2.2.4.1 Decoder Block Diagram



3.3.2.2.4.2 Design and Tradeoffs

The decoder is made up primarily of the Manchester decode logic, a phase-locked loop, a preliminary signal processor and power supply filters. The preliminary signal processor extracts the fundamental frequency component from the Manchester data. The phase-locked loop locks on to this component and produces the one-times clock necessary for the Manchester decode logic's conversion of Manchester to NRZ data and clock.

3.3.2.2.4.2.1 Preliminary Signal Processing

Manchester data provides no distinct fundamental frequency component without pre-processing. The phase-locked loop requires such a component for reliable acquisition and tracking. Unprocessed Manchester data, passed directly to a phase-locked loop's input causes unreliable loop operation. The PLL could lock on to the wrong component or slew from one frequency component to the next, never recovering the clock.

The pre-processing circuitry strengthens the fundamental clock frequency of the Manchester data in relation to all other components. A detail of the pre-processing circuitry is shown in Figure 3.3.2.2.4.2.1-1. A 20 nsec pulse is generated for each edge transition of the incoming Manchester as shown in line A of the timing diagram.

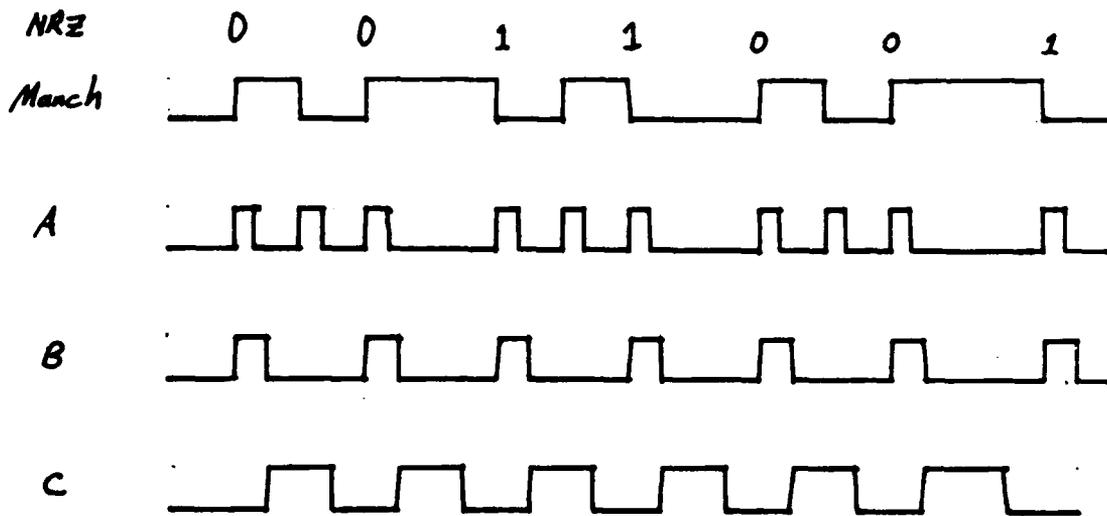
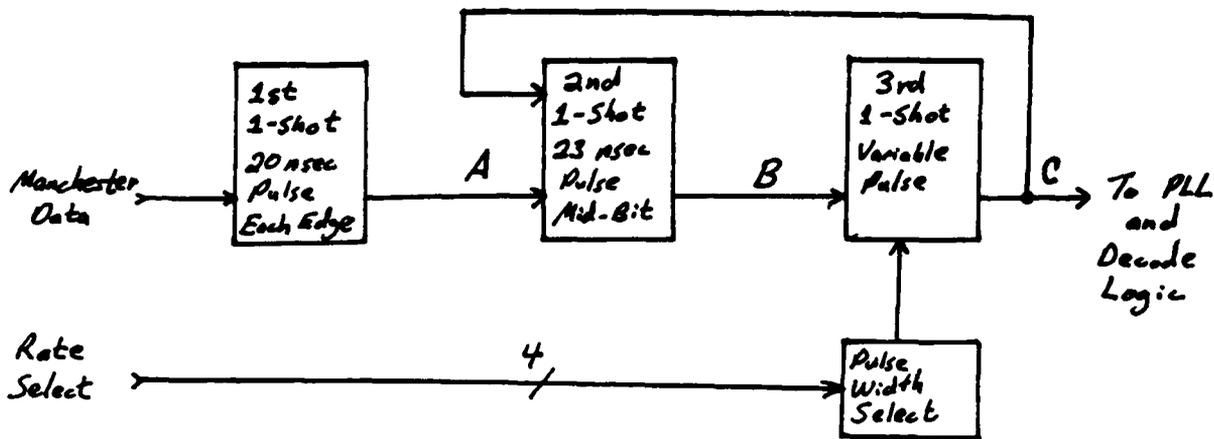


Figure 3.3.2.2.4.2.1-1

This pulse triggers a second one-shot timer, provided the second one-shot is enabled by yet a third timer. The second timer's pulse width is 23 nsec, while the third's is set by four rate select bits. These bits program the pulse interval to greater than the minimum Manchester pulse width, yet less than the Manchester bit width. The minimum Manchester pulse width is one-half the bit width. As an example 10 Mbps Manchester data has bit widths of 100 nsec, minimum pulse widths of 50 nsec and maximum pulse widths of 100 nsec.

When the third one-shot is triggered, the second one-shot is disabled for an interval longer than one minimum Manchester pulse duration as shown in lines B and C of the timing diagram. This ensures that the second one-shot is only triggered by mid-bit transitions which carry the one-times clock fundamental. The third one-shot, being triggered by the second one-shot, therefore also outputs a signal with this strong fundamental. This signal is converted from ECL to TTL and sent to the phase-locked loop's phase detectors.

The four rate select bits are TTL compatible but do not have pull-up resistors. They can be programmed low by grounding them but are programmed high only by external TTL Logic 1 voltage levels. They are programmed as follows:

<u>Manchester Data Rate Mbps</u>	<u>Minimum Pulse Width</u>	<u>Bit Width</u>	<u>Rate Select A B C D</u>	<u>Nominal Third One-Shot Interval</u>
9.133 to 12.000	41-55ns	93-109ns	1 1 1 1	46nsec
6.952 to 9.133	55-72ns	109-144ns	0 1 1 1	68nsec
5.291 to 6.952	72-95ns	144-189ns	1 0 1 1	97ns
4.027 to 5.291	95-124ns	189-248ns	0 0 1 1	134ns
3.065 to 4.027	124-163ns	248-326ns	1 1 0 1	183ns
2.333 to 3.065	163-214ns	326-429ns	0 1 0 1	208ns
1.776 to 2.333	214-281ns	429-563ns	1 0 0 1	332ns
1.352 to 1.776	281-370ns	563-739ns	0 0 0 1	444ns
1.029 to 1.352	370-486ns	739-972ns	1 1 1 0	590ns
0.738 to 1.029	0.486-0.639us	0.972-1.277us	0 1 1 0	783ns
0.596 to 0.738	0.639-0.839us	1.277-1.678us	1 0 1 0	1.035us
0.454 to 0.596	0.839-1.101us	1.678-2.203us	0 0 1 0	1.367us
0.345 to 0.454	1.101-1.449us	2.203-2.899us	1 1 0 0	1.803us
0.263 to 0.345	1.449-1.901us	2.899-3.802us	0 1 0 0	2.377us
0.200 to 0.263	1.901-2.500us	3.802-5.000us	1 0 0 0	3.128us

For optimum processing of the Manchester data, the combined pulse intervals of the second and third one-shots should sum to an interval mid-way between the longest minimum pulse width and the shortest bit-width of the Manchester Data rate range. The 23 nsec time-out of the second one-shot is added to the final column third one-shot pulse width for a total delay that splits the Manchester longest pulse width and Manchester minimum bit width times. For example, the combined delay of the two one-shot timers when operating in the 9.133 to 12.000 Mbps range is:

$$\begin{aligned} & \text{second one-shot interval} + \text{third one-shot interval} = \\ & \quad 23 \text{ nsec} \quad + \quad 46 \text{ nsec} = \\ & \quad = 69 \text{ nsec total interval} \end{aligned}$$

This total interval cannot be shorter than the 9.133 Mbps data rate minimum pulse width of 55 nsec or the edge bit transitions will be passed to the PLL along with the mid-bit transitions, resulting in no clear fundamental frequency component. Conversely, the total interval cannot be longer than the 12 Mbps data rate bit-width or some mid-bit transitions will not be passed to the PLL, again resulting in no clear fundamental component. The data rate ranges and timing interval were selected to provide some overlapping between ranges as insurance against one-shot timing tolerances and any pulse distortion or jitters of the Manchester data during transmission. The above example has a built in 14 nsec, or 20%, safety margin. All ranges have this 20% safety margin built in, resulting in a decoder that is somewhat forgiving of pulse distortion and jitter.

3.3.2.2.4.2.2 Phase-Locked Loop

Several methods exist for generating the clock necessary for decoding the Manchester data. The phase-locked loop was chosen for the following reasons:

- o Digital techniques require clock rates of 16 to 32 times the maximum clock rate (192 MHz or 384 MHz). A clock frequency this high was deemed impractical.
- o One-shot or delay line techniques are only usable at fixed frequencies, not the continuously variable MFOX frequency range.
- o The phase-locked loop is continuously variable over a wide frequency range.

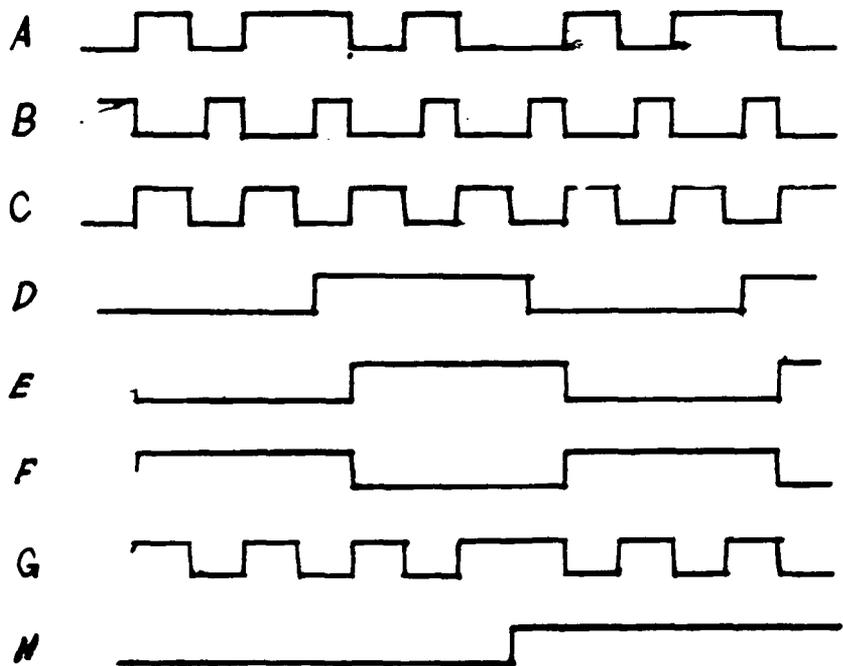
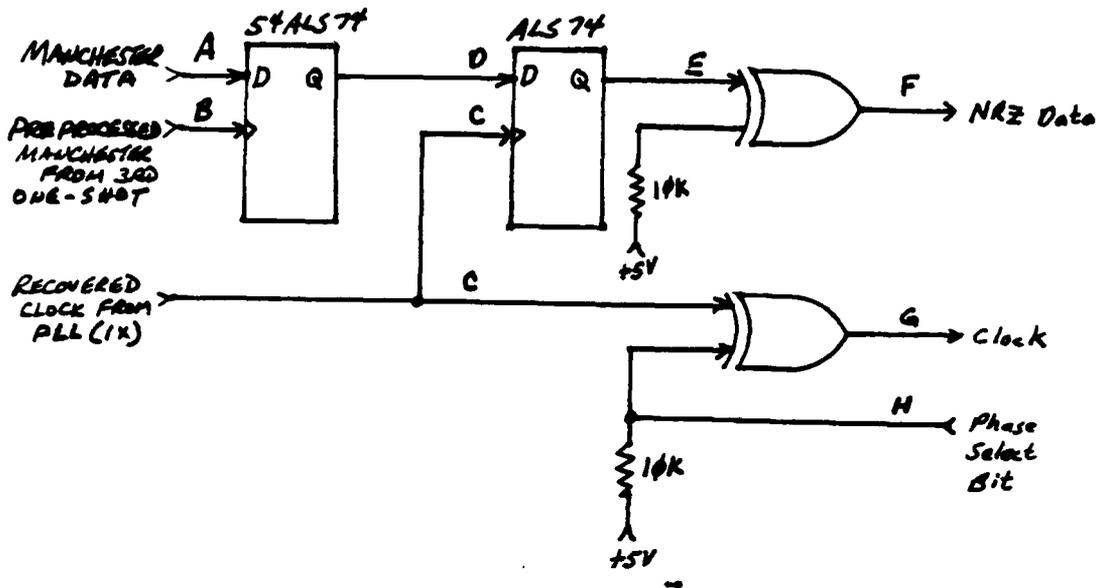
The phase-locked loop used in the decoder is identical to that in the encoder and is described in 3.3.2.2.2. The four pulse width selection programming bits and the three phase-locked loop frequency select bits are combined into one table for programming the decoder over a twenty interval range as shown on the following page.

Decoder Interfaces To User

Step #	Baud Rate Mb/s	One-Shot Interval Select				PLL Select		
		<u>D</u>	<u>C</u>	<u>B</u>	<u>A</u>	<u>A</u>	<u>B</u>	<u>C</u>
1	9.133 to 12.000	1	1	1	1	0	0	0
2	6.952 to 9.133	1	1	1	0	0	0	0
3	6.000 to 6.952	1	1	0	1	0	0	0
4	5.291 to 6.000	1	1	0	1	0	0	1
5	4.027 to 5.291	1	1	0	0	0	0	1
6	3.065 to 4.027	1	0	1	1	0	0	1
7	3.000 to 3.065	1	0	1	0	0	0	1
8	2.333 to 3.000	1	0	1	0	0	1	0
9	1.776 to 2.333	1	0	0	1	0	1	0
10	1.500 to 1.776	1	0	0	0	0	1	0
11	1.352 to 1.500	1	0	0	0	0	1	1
12	1.029 to 1.352	0	1	1	1	0	1	1
13	0.783 to 1.029	0	1	1	0	0	1	1
14	0.750 to 0.783	0	1	0	1	0	1	1
15	0.596 to 0.750	0	1	0	1	1	0	0
16	0.454 to 0.596	0	1	0	0	1	0	0
17	0.375 to 0.454	0	0	1	1	1	0	0
18	0.345 to 0.375	0	0	1	1	1	0	1
19	0.263 to 0.345	0	0	1	0	1	0	1
20	0.200 to 0.263	0	0	0	1	1	0	1

3.3.2.2.4.2.3 Manchester Decode Logic

The Manchester decode logic and timing diagram is shown in Figure 3.3.2.2.4.2.3-1



The pre-processed Manchester from the third one-shot timer gates the true Manchester data into a D Flip-Flop. The output of the Flip-Flop is the recovered NRZ data. A second Flip-Flop synchronizes the data with the recovered clock from the PLL. The recovered clock and NRZ data are buffered by two XOR gates for transmission to the Level 2 Receiver. A phase select bit determines the clock to NRZ data phase relationship as shown in the timing diagram. This feature simplifies interfacing to the host system.

3.3.2.2.4.2.4 Supply Filtering

The +5.2V supply inputs are filtered by the two-pole inductive-capacitive filters described in 3.2.1.1.2. The filter component values are:

+5V Supply	C1 = 0.1uF
	C2 = 6.8uF
	L1 = 50uH

-5.2V Supply	C1 = 0.1uF
	C2 = 6.8uF
	L1 = 10uH

3.3.2.3 Special Considerations

3.3.2.3.1 Problems and Solutions

3.3.2.3.1.1 Transmitter Pigtail Connectorization and LED Cooling

The MFOX units are designed to operate in a maximum ambient temperature of 52°C. This temperature is not typically a concern with the low power dissipations of the MFOX units, but 52°C does approach the allowable operating limit for the LED module in the transmitters. The LED chip die experiences optical power degradation as the

temperature rises. This is compensated for by a circuit which increases the current to the die as the temperature increases. This however, can lead to a thermal runaway situation as the LED die temperature rises when the current is increased. Based on the characteristics of the compensation circuit and the thermal resistance from the junction to case, the New Products Division determined the temperature must be limited to 64°C to meet optical output requirements and avoid a thermal runaway situation. A Peltier thermo-electric device would provide active cooling but required high current, low voltage power which would be difficult to supply in many potential MFOX applications. Preferably, the packaging design could provide a sufficiently low thermal impedance path to ambient. This goal was accomplished by addressing thermal considerations in a number of packaging design decisions. The LED chip inside the case was eutectically attached to a copper heat sink brazed to the LED case. A flatpack with provisions for bolted mounting was chosen for the LED case configuration. The LED case which is at +5V potential was mounted to an aluminum spacer having an anodize hardcoat finish. The LED assembly is then bolted to the outer case made of aluminum. The outer case in turn has a bolted interface to its mounting surface. A high resolution thermal finite difference analysis of the Level 2 Transmitter was performed and showed the above packaging design would sufficiently limit the temperature of the LED case at high temperature. This analysis was verified later by successful confidence and Qual testing.

A problem was encountered with the Level 2 Transmitter optical connector termination during burn-in temperature cycling. The bond

between the glass optical fiber and stainless steel connector cavity failed under cyclic thermal stressing. The bond failure resulted in pistoning or breakage of the fiber. The problem was only being experienced with the Level 2 LEDs which employ an epoxy free alignment mechanism of the LED die to fiber. The fiber is eutectically secured inside a brass tube clamped to the LED die heat sink. During the manufacture of the LED, the tube is mechanically deformed until optimum alignment of the LED die to fiber is achieved. The main benefit of this alignment mechanism is that it avoids the use of epoxy for fiber retention, which experiences much distortion during temperature variations. Fiber retention inside the brass tube requires a metallic deposition onto the termination area of the glass fiber. The processed fiber was only available from a single supplier who used a fiber having a heat cured silicone primary buffer. This silicone is extremely difficult to remove compared with the ultra-violet cured silicone or acrylate buffer materials generally used. Failure to remove the buffer weakens the epoxy bond inside the optical connector and can result in the failures that were experienced during temperature cycling. As a corrective action, the buffer stripping process for the Level 2 LEDs was changed from casual wiping with acetone to immersing the stripped fiber in hot sulfuric acid, followed by a rinse in de-ionized water and an alcohol wipe.

In addition, the entire connector was backfilled with epoxy to increase the effective length of the bond. The metallized fiber can now be obtained with a ultra-violet cured silicone, which will make this rigorous corrective stripping process unnecessary for future build.

Other special design considerations for the Level 2 units are discussed in previous sections of the report;

- transmitter and receiver optical pigtail strain relief, Section 3.3.1.3.3
- Ceramic substrate micro-cracking Section 3.2.2.8.1.

3.3.2.3.1.2 Receiver Pigtail Attachment

The procedure for the attachment of the optical fiber to the pinfet module had to be modified. Indeed, after we tested the first samples, a high percentage of the fiber had fallen off. The standard procedure for pigtailling was using only ultra-violet epoxy. To reinforce the pigtail, we used in addition to the U.V. epoxy, a substance called torr seal.

This new procedure greatly improved our yield. However, for future development we should look into a case with a permanent ferrule and soldered optical fiber. This assembly would free us from using epoxy, which softens and hardens with temperature variations, thus causing optical fiber disalignment.

3.3.2.3.1.3 Receiver Alarm Sensitivity

The original design of the C30615E alarm circuit provided an alarm signal for a signal level very close to the maximum sensitivity of the ECL output (-41 dBm or 6.8 mV_{p-p} at the pinfet output). This design concept caused a problem in practice, because the hysteresis of the alarm circuit could not consistently differentiate signal from noise. This means that in the absence of signal, the alarm circuit would randomly trigger on the noise. This behavior would also show with temperature variations. The cause of this problem was obviously an overly sensitive hysteresis; the signal to noise ratio at -41 dBm

was too poor to accept a hysteresis at this level.

The solution to this problem was to reduce the sensitivity of the alarm to a level clearly above the noise level. We had to determine experimentally the value of the hysteresis in order to obtain optimum performances. The end result is an alarm signal which is activated slightly (see test results) before we lose the ECL outputs.

3.3.2.3.1.4 Receiver Oscillation

After assembly of the first-piece unit, an oscillation problem was discovered.

With no optical signal present, a 100 MHz oscillation of the Threshold detector's Q and \bar{Q} data outputs was observed and the Threshold alarm output remained in a non-alarmed state. The alarm could not distinguish between oscillation and real data and therefore did not function properly.

After an extensive investigation the source of the oscillations was determined.

The Threshold's ECL comparator is very sensitive to output loading. Since in the original design, the PCB to Interface hybrid connection was an unterminated, uncontrolled impedance, the reflections seen at the signal source were large enough to cause this sensitive circuit to oscillate. A variety of series damping resistors and clamping diodes were tried at the signal source to dampen these reflections. As further insurance against possible oscillation, all unused ECL line receiver inputs on the interface hybrid were tied off. The ECL line receivers are high gain comparators so clamping their inputs and outputs to DC levels eliminated another possible source of

oscillation. These modifications necessitated white wire changes to the receiver Interface Assembly and the addition of two damping resistors and two clamping diodes to the PCB.

These changes resulted in a Level 2 Receiver with a working alarm and no oscillations. Sensitivity and data rate met specifications. The inductive elements of the PCB PINFET filters were changed to 10 Ohm resistors as an additional preventative measure. It was felt that the resistors were better attenuators at 100 MHz than the inductors, due to possible capacitances between inductor coils.

3.3.2.3.1.5 Encoder and Decoder Jitter

First-piece encoder and decoder units experienced severe jitter problems. Encoder Manchester output and decoder data and clock output pulse widths varied considerably. The problem was traced to the phase-locked loops of both units.

Portions of the PLL's contain sensitive, high impedance analog circuitry. The analog circuit interconnections were distorted by nearby fast-switching, high-amplitude digital circuitry. Crosstalk, probably capacitive in nature, between the digital and analog circuit elements caused the jitter.

An analysis of the analog and digital circuit traces was made and possible sources of crosstalk were noted. Digital traces running parallel to analog traces were particularly noted. All suspicious digital traces were cut and white wires were added as jumpers. The coupling between the white wires and the analog circuitry was considered negligible compared to the interactions between the digital traces and the analog circuitry. Marked improvements were made and all units underwent white-wire changes.

Although the jitter was greatly reduced (down to just a few nanoseconds), waveform distortion could still exceed 5% of the pulse width at the highest operating frequency of 12 Mbps (42 nsec minimum pulse width). Layout of future units should address this problem. Isolation of the analog circuitry through ground and/or voltage planes and routing all digital signals as far from the analog circuitry as possible should go a long way toward eliminating this problem.

3.3.3 Level 4 Modulator and Demodulator with Level 2 Transmitter and Receiver ADMs

3.3.3.1 System Link Description

The Level 4 Modulator and Demodulator provide a means to send wideband analog signals over a fiber optic link using the Level 2 transmitter and receiver which usually carry digital data.

The modulator and demodulator were designed to give the best possible performance consistent with size and reliability requirements. This meant that several design techniques used in high performance FM systems were not used because the small performance improvements could not justify the increased size and complexity and corresponding reduction in reliability.

For example, the FM modulation technique where two high frequency oscillators are modulated at a low percentage deviation (for high linearity), then heterodyned to a lower frequency with a high percentage deviation, was not used because a voltage controlled multivibrator was found to provide adequate linearity. Carrier frequency feedback stabilization was not needed because being a single carrier system, there are no other carriers to cause interference or be interfered with. Also, the type of demodulator selected can accept

wide range of carrier frequencies. Bandpass filters were not used in the demodulator for the following reasons:

1. No separation of carriers is required because this is a single carrier system.
2. The signal to noise improvement would only occur near threshold and with the transmitter and receiver operating with a digital BER of 10^{-9} they are operating well above threshold.
3. The filters would have to be located in the Level 2 receiver ahead of the limiter or if located in the demodulator, a low level linear output from the receiver would be required, complicating the receiver-demodulator interface. A limiter would have to be added in the demodulator leaving the one already in the receiver unutilized.

3.3.3.1.1 Carrier Frequency and Deviation

The requirements of the Level 4 system are that it transmit 10 MHz bandwidth analog data using the Level 2 transmitter and receiver. The analog data is transmitted via a frequency modulated square wave because it is the only means compatible with the Level 2 system's linearity and data rate.

The three main factors affecting the selection of carrier frequency and deviation are:

1. The upper edge of the spectrum must fit well within the bandwidth of the Level 2 transmitter and receiver.
2. The lower edge of the FM spectrum must be sufficiently above the video bandwidth so that residual carrier does not appear in the modulator output.

3. The deviation should be as wide as possible within constraints 1 and 2 to achieve the best signal to noise ratio. The greater than 50 MHz Level 2 system's bandwidth and 10 MHz analog bandwidth leads to a carrier frequency selection of 30 MHz. With a peak deviation of 10 MHz, most of the FM spectrum energy is between 20 and 40 MHz leaving a 10 MHz band on each side for the remaining sidebands in the Carson bandwidth.

3.3.3.1.2 Pre-emphasis

Television signals are more tolerant of high frequency noise than low frequency noise, so the use of pre-emphasis for improving signal-to noise ratio in FM systems is not required. It does, however, improve system linearity. Good linearity is especially important in systems where one or more subcarriers are used, such as in composite color television systems and some radar video systems.

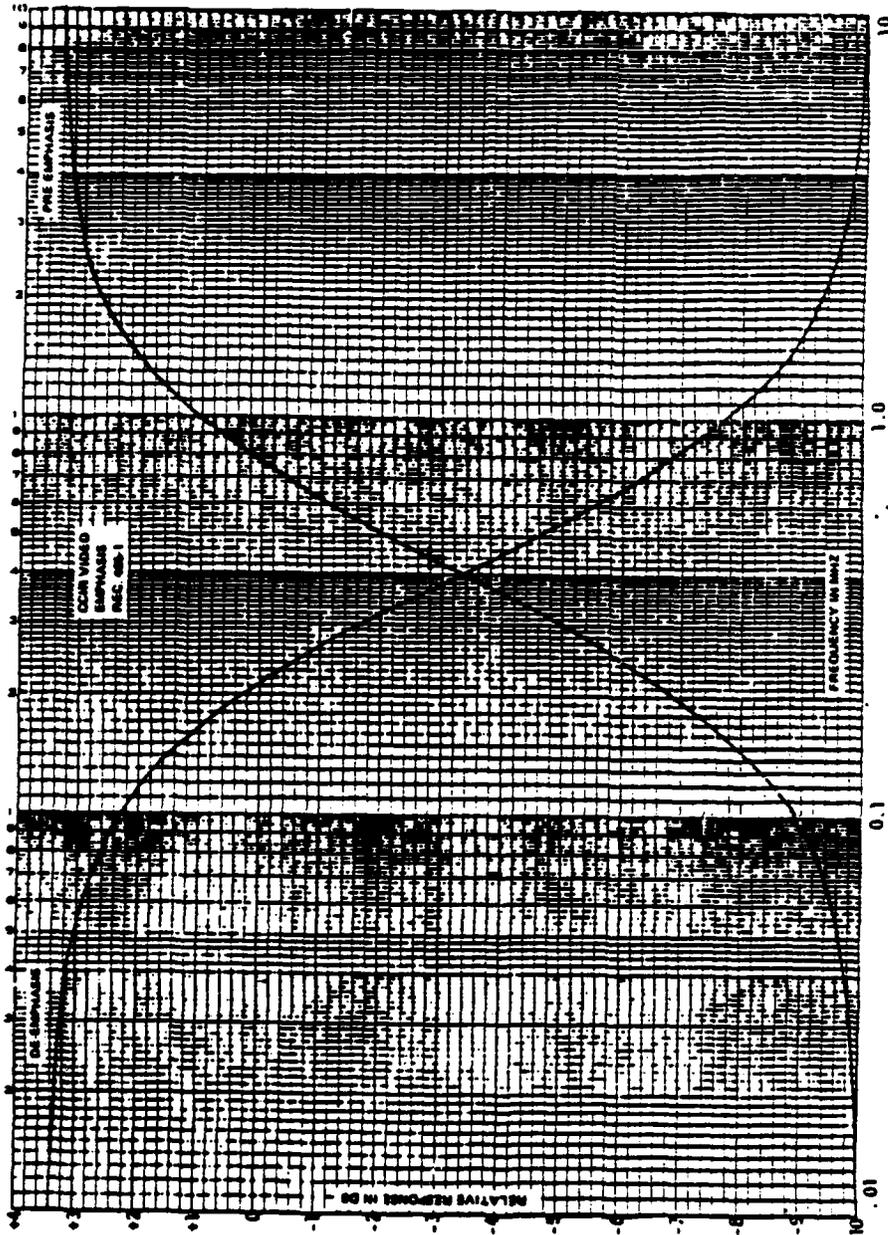
The CCIR 405-1 pre-emphasis standard was selected for the Level 4 system. This standard is used by most satellite and terrestrial microwave television transmission systems. The pre-emphasis and de-emphasis frequency response curves are shown in Figure 3.3.3.1.2-1. The maximum high frequency boost is only 3.4 db, so it is anticipated that pre-emphasis can be used in nearly all applications and its use is recommended to improve the system's linearity.

Never the less, its use is optional, and can be disabled externally. The deviation at low frequencies should be increased by 10 db if pre-emphasis is not used and this requires an adjustment inside the modulator and demodulator.

Figure 3.3.3.1.2-2 is a chart that relates signal voltage levels to the FM spectrum, with and without emphasis. The chart also shows how pre-emphasis reduces the FM excursions for low frequency luminance information and increases the excursions for high frequency information, in this example of the color subcarrier, thus reducing the interaction between each.

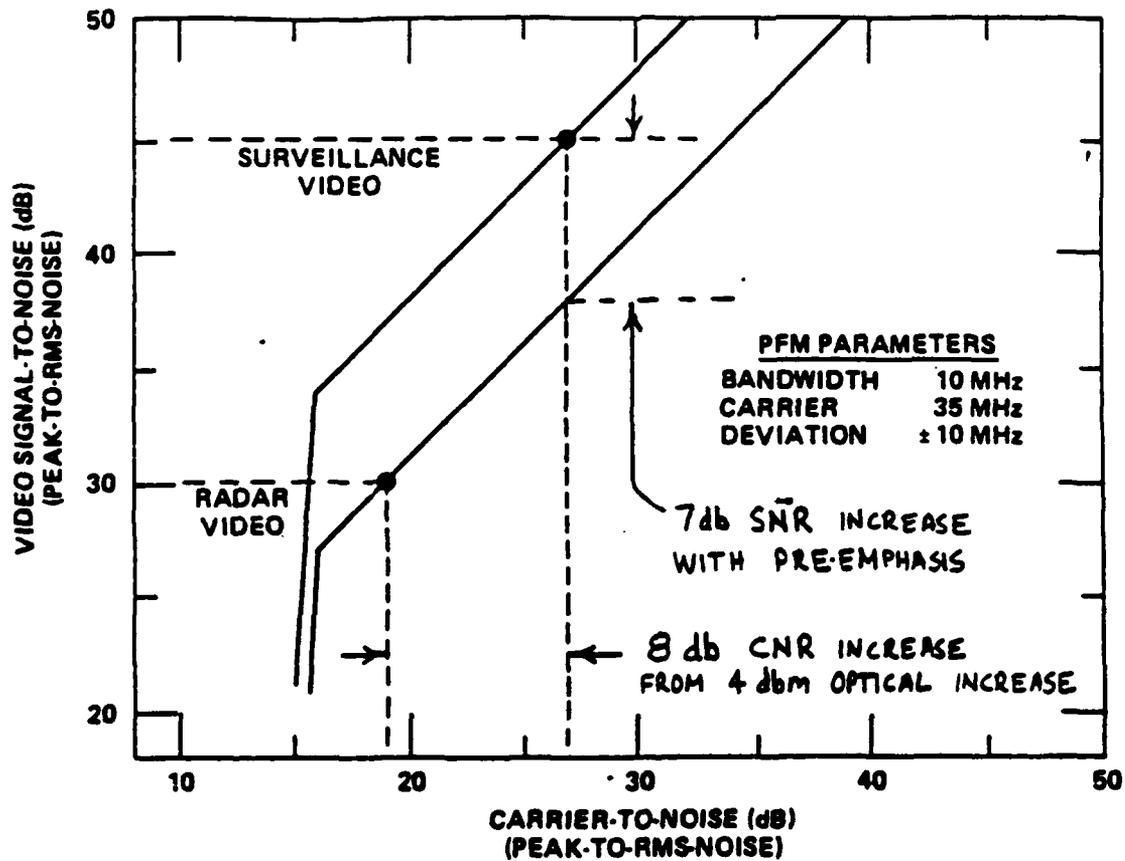
3.3.3.1.3 Signal-To-Noise-Ratio

The Level 4 system configuration requires that the video signal-to-noise ratio, SNR, be 30 db minimum for a Level 2 receiver optical input of -40 dbm. Additionally, the SNR should be 45 db minimum for an optical input of -36 dbm. This apparent 15 db SNR improvement for only a 4 db optical power increase requires an explanation. The specified SNRs appear in a graph, Figure 2-48 on pages 2-88 of the MFOX proposal that is reproduced here with additional notations as Figure 3.3.3.1.3-1. One convenient way of calculating processing gain was shown by S.J. Cowan in a paper entitled, "Fiber Optic Video Transmission Systems Employing Pulse Frequency Modulation." This paper appeared in the IEEE, Proceedings of Oceans, September 1979. The processing gain expressed as a voltage or current ratio is,



Pre-Emphasis And De-Emphasis
Amplitude Response

Figure 3.3.3.1.2-1



Video PFM Performance

Figure 3.3.3.1.3-1

$$G_{ss} = \frac{1.15 \Delta F \left(1 + \frac{\Delta F^2}{f_c^2}\right) B_{rf}}{\sqrt{f_c} B_{bb}^{1.5}} = 3.69 \text{ or } 11.34 \text{ db}$$

where F = peak frequency deviation = 10 MHz for 1.5 vp-p input.

f_c = carrier frequency = 30 MHz

B_{rf} = predetection bandwidth = 50 MHz

B_{bb} = post detection bandwidth = 10 MHz

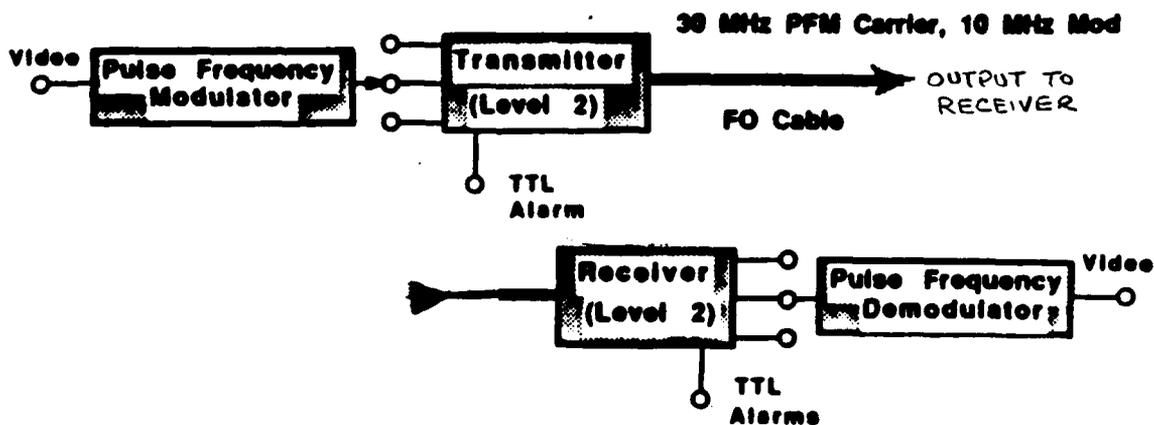
The lower specification point shown in Figure 3.3.3.1.3-1 applies to the radar video application where an optical power input of -40 dbm gives a carrier-to-noise ratio, CNR, of 19 db which with an 11 db processing gain provides a 30 db SNR. The higher specification point applies to the surveillance video application where 4 db more optical power will increase the carrier level and thus CNR by 8 db. (The receiver is a square law device whose output signal current or voltage is directly proportional to optical power input.) An additional 7 db SNR improvement comes from the use of pre-emphasis for the surveillance video application. It was assumed that pre-emphasis could not be used for the radar video application because the video is frequently accompanied by one or more subcarriers which could cause overdeviation if pre-emphasized. Also a SNR greater than 30 db is not required from the radar video application. As discussed earlier, improved linearity is the primary purpose of the type of pre-emphasis selected for this system during the design phase. While it does provide some SNR improvement, it is usually only about 2 db in a 4.2 MHz bandwidth system. This should be somewhat higher in the MFOX system with its 10 MHz bandwidth. Breadboard measurements, discussed

later, indicate that pre-emphasis improves the SNR by 3.6 to 4.2 db. While the SNR improvement originally expected from pre-emphasis is not fully realized, another factor relevant to television SNR measurements, noise weighting, needs to be considered.

The picture impairment caused by noise is also a function of its frequency as well as its amplitude. Noise weighting is used so that the SNRs of television systems with differing noise versus frequency characteristics can be compared. High frequency noise is less objectionable than low frequency noise of the same amplitude. In FM systems, the noise power per unit of bandwidth increases with frequency, so there is more noise at high frequencies than low frequencies. So, it is important that a noise weighting filter be used to more accurately reflect the picture impairment caused by noise. The noise weighting factor for the weighting filter specified in EIA standard RS-250-B is 12.2 db for a 5.0 MHz base bandwidth FM system with a triangular shaped noise spectrum. This factor is higher for higher base bandwidth systems and breadboard measurements indicate that it is on the order of 20 db for the MFOX system.

3.3.3.2 System Diagram

Level 4 Analog Transmission System

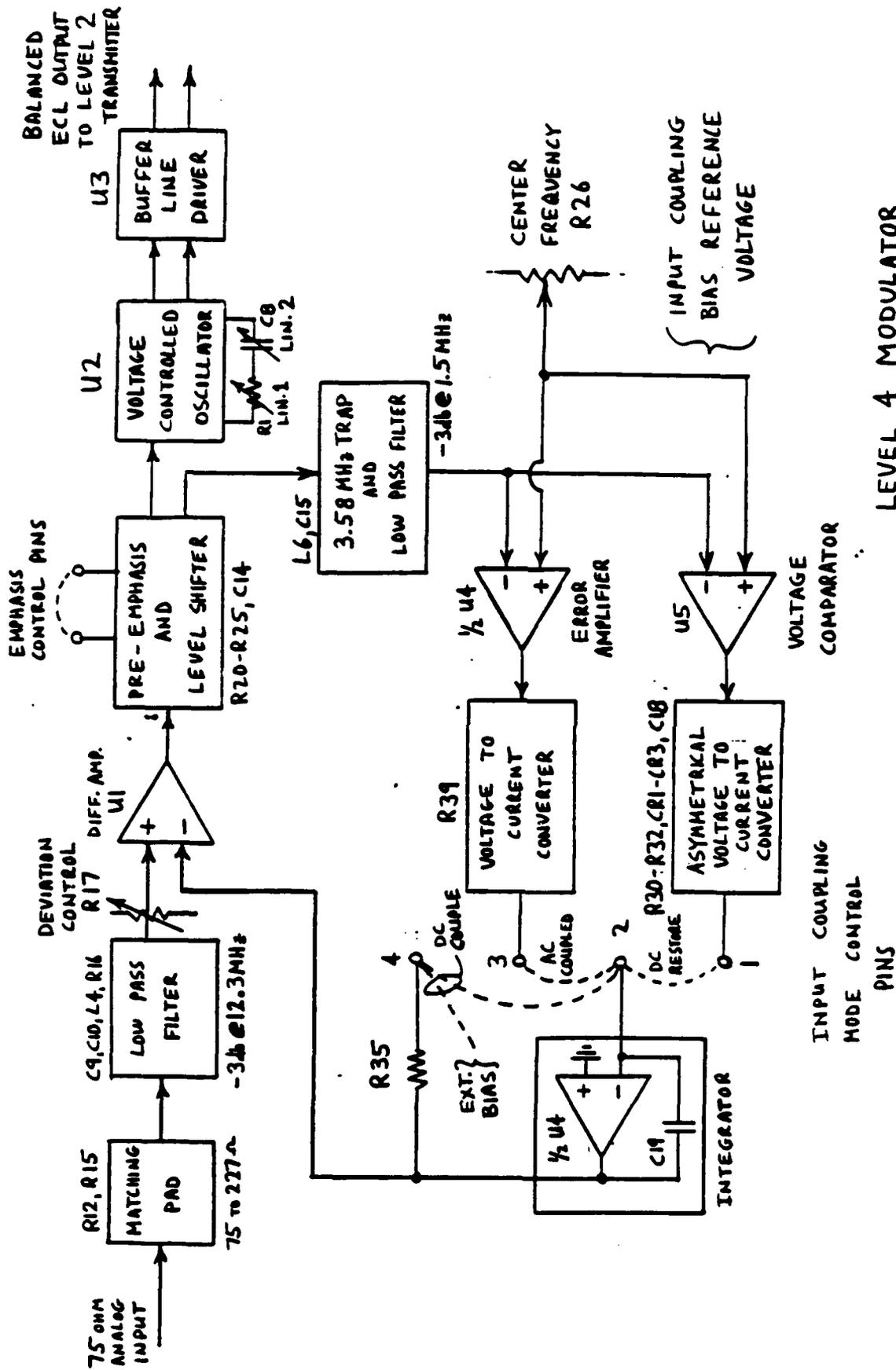


3.3.3.2.1 Modulator Circuit Description

Figure 3.3.3.2.1-1 is the block diagram and Figure 3.3.3.2.1-2 is the detailed schematic of the modulator. The input signal passes through a matching pad and low pass filter. The low pass filter's 12 MHz bandwidth rejects any out of band signals that could cause interference if they got inside the modulator. The matching pad matches the filter to the 75 ohm input and isolates the filter reactance from the input, providing high input return loss well beyond the system's analog bandwidth. R17 is the only gain control in the modulator and is used to set the frequency deviation. It is also part of the filter termination.

Differential amplifier U1 provides gain needed for pre-emphasis and also adds a D.C. control signal with the input signal as part of the input coupling and bias system. U1 drives two identical resistor networks, R20 to R22 and R23 to R25. The first network level shifts the analog signal negative to be within the proper range of the control input of U2, the voltage controlled oscillator (VCO). This allows U1 to operate in the middle of its output swing range. The first network is also the resistive part of the pre-emphasis network. When pre-emphasis is desired, module pins P13 and P14 are connected, placing C14 across R20, thus providing less attenuation for high frequencies than low frequencies. The second network supplies a signal to the input coupling and bias circuitry that is identical to the signal going to the VCO except without pre-emphasis.

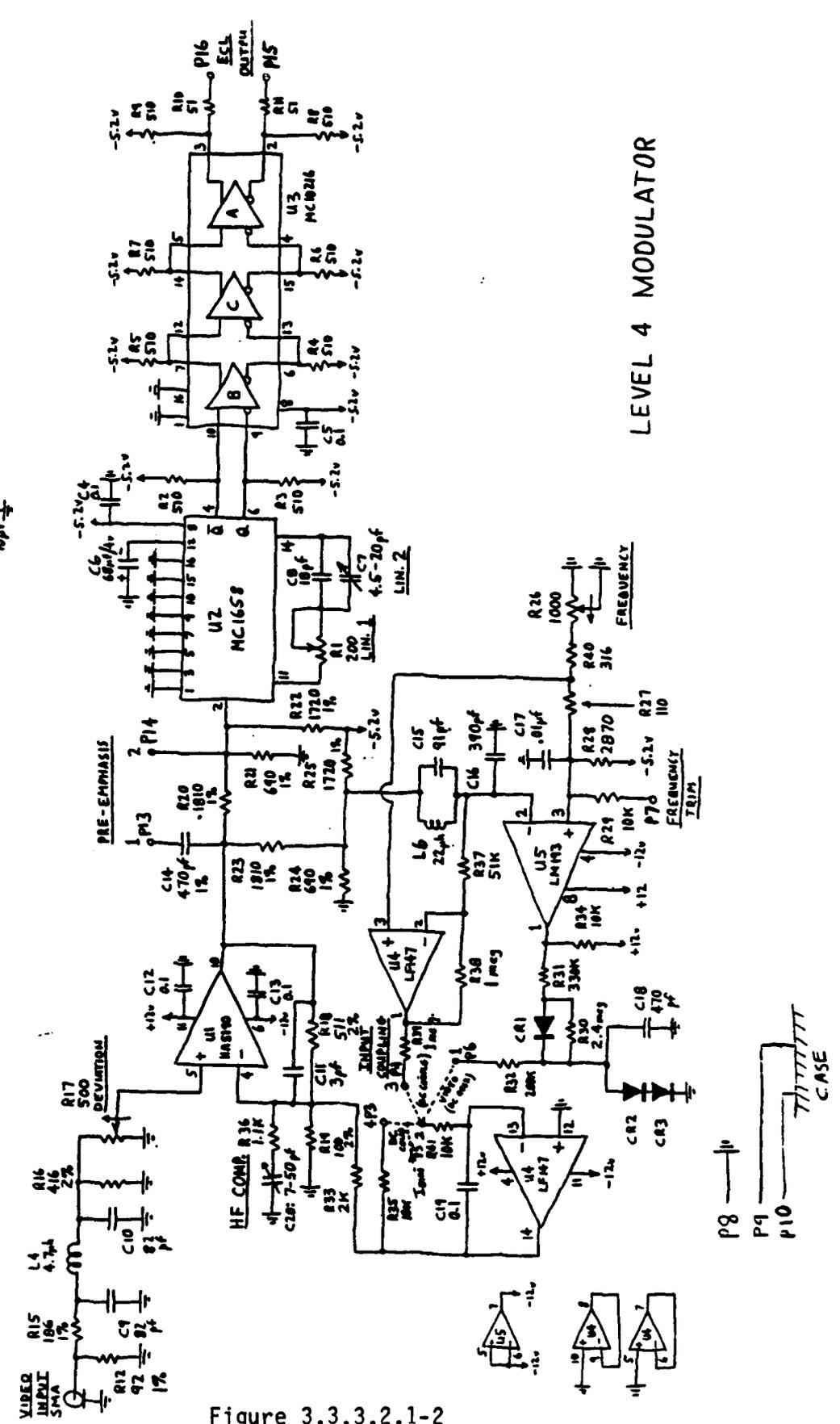
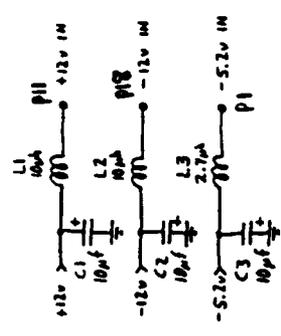
VCO U2 is a voltage controlled multivibrator. The linearity of the control voltage input versus frequency output transfer function of



LEVEL 4 MODULATOR

BLOCK DIAGRAM

Figure 3.3.3.2.1-1



LEVEL 4 MODULATOR

Figure 3.3.3.2.1-2

U2 is improved if there is some resistance, R1, in series with the timing capacitor between pins 11 and 14. The center frequency, deviation, and linearity are all interdependent functions of R1, C2 and the control voltage. Optimum adjustment of these controls requires a special procedure and test fixture. Therefore, once R1 and C7 have been set by the procedure, they should not be used for center frequency or deviation adjustment; only R26 and R17 (or the external Frequency Trim input, P7) should be used for these adjustments.

The output of U2 is a frequency modulated square wave at balanced ECL levels. These signals are buffered by U3 to provide isolation between U2 and the modulator output which is connected to the Level 2 transmitter using balanced twisted pair transmission line.

As mentioned previously, resistor network R23-R25 supplies a level shifted analog signal that has not been pre-emphasized to the input coupling and bias circuitry. L6, C15, and C16, along with the source impedance of the resistor network, form a low pass filter and 3.58 MHz trap to prevent high frequencies and color television subcarrier, if present, from getting into the input coupling and bias circuit. This circuit has three operating modes to optimize system operation for different types of analog signals. For unsymmetrical pulse type signals such as surveillance and radar video, the DC restore mode should be used. To operate in this mode, Input Coupling pins 1 and 2 (module pins P5 and P6) must be connected.

The DC restorer circuit adjusts the DC level of the input signal so that the signal swing at the VCO input is always within its linear range, regardless of the actual DC level of the input signal. (Note that the DC restorer only adjusts the DC level or bias of the input

signal; it does not affect the peak-to-peak amplitude of the input signal.) To set the input signal to the proper level, the circuit finds a certain part of the input waveform that has a known relationship to the signal extremes. The circuit then forces this part of the signal waveform to always be at the same absolute voltage when it goes into the VCO. The part of a television waveform that the circuit finds and uses as a reference is the video blanking level. In all conventional television formats, the signal waveform has to be at a blanking level a certain percentage of the time or duty cycle. The circuit finds blanking level by using a voltage comparator to "slice" a replica of the signal at various levels until it finds the proper duty cycle and then a feedback loop forces the part of the waveform to the desired voltage level. Although this operation is described in the context of the television video waveform, this method of DC restoration was selected because it will operate with very low duty cycle waveforms without distortion, such as with radar video. Another advantage is that it does not require any keying or clamp pulse.

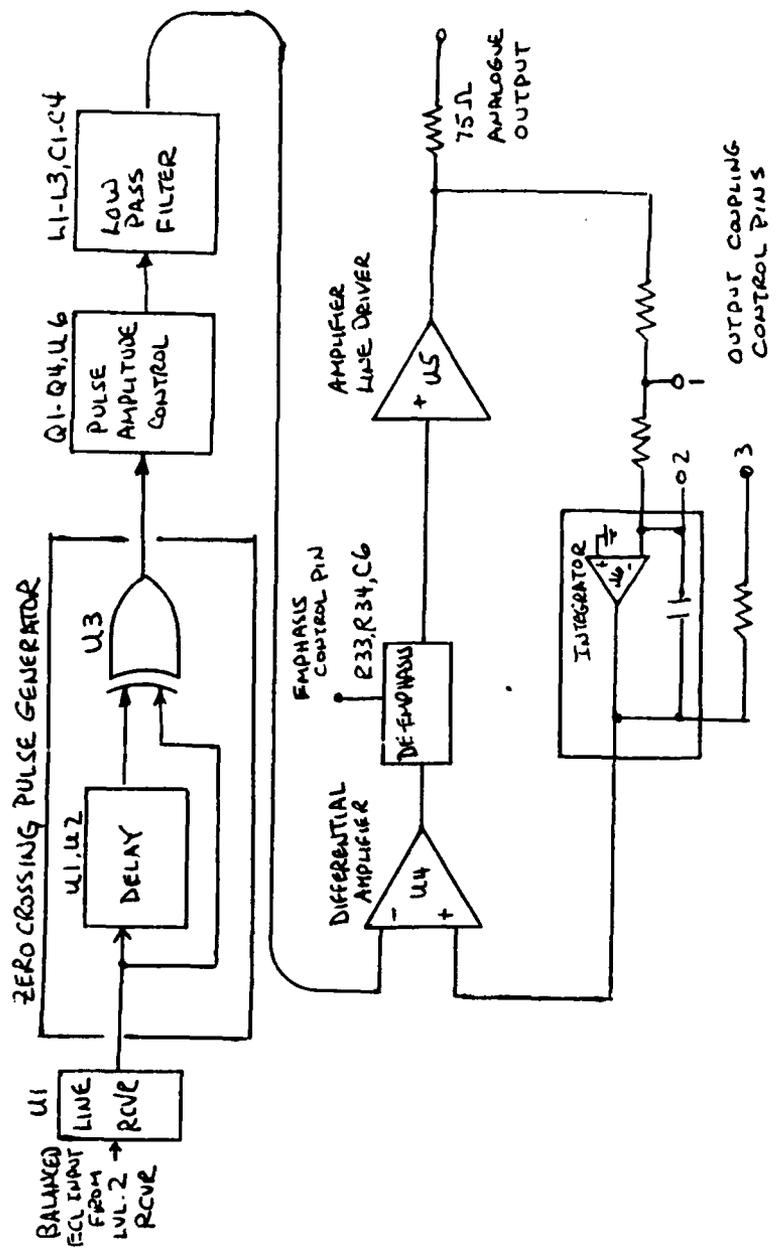
A replica of the input signal that has not been pre-emphasized is supplied by the level shift and filter network R23-R25, L6, C15, and C16 to voltage comparator, U5. This comparator "slices" the signal as part of the process to find the blanking level part of the waveform. The comparator's output is a rectangular wave with a variable duty cycle that is a function of how much of the input signal replica is above the DC reference voltage at U5 pin 3. The duty cycle will change as the DC level of the input signal replica changes. The comparator's output voltage which swings from nearly +12 volts to nearly -12 volts is converted to unequal positive and negative

currents by R30-R32 and CR1. (RC2, CR3 and C18 are not fundamental to the operation of the DC restorer. Their purpose is to reduce a disturbance caused by vertical sync.) The unequal currents are integrated by U4, a general purpose operational amplifier and C19. The output of the integrator is a DC voltage that is added to the input signal by U1 via R33. The feedback loop thus formed shifts the DC level of the input signal going to the VCO and its replica going to the voltage comparator, U5 pin 2, until the average current into the integrator U4 and C19, is zero. The average current is zero when the duty cycle of the comparator's output voltage is near +12 volts 13% of the time because of the unsymmetrical conversion of voltage to current by R30-R32 and CR1. The only place where a standard television signal can be "sliced" and get a 13% duty cycle is at blanking level because synchronizing pulses have a duty cycle of 8.5% and composite blanking (including sync) has a duty cycle of at least 22%. Thus, the circuit adds a DC bias to the input signal until the blanking level portion of the input signal is at the same absolute voltage as the reference input of the voltage comparator U5 pin 3.

In addition to the surveillance television and radar video, the DC restore mode may be the preferred mode for other unsymmetrical pulse type signals that have a baseline or reference level that needs to be controlled so as to obtain maximum linearity through the system. Using the DC restore mode to control the DC level of a baseline or reference level is especially important if pre-emphasis is not used. The DC restore circuitry will work with signals that are more positive than the baseline no more than 80% of the time and more negative than the baseline no more than 10% of the time. The linear signal swing

range is greater on the positive side of the baseline than on the negative side by about 2:1, although this ratio can be changed by adjusting the Frequency control, R26. The ratio can also be changed externally by connecting a bias voltage to the Frequency Trim input, module pin P7. The circuitry will work even if there are no negative excursions below the baseline, for example, video without synchronizing pulses. However, the circuitry will not work properly with inverted television video, for example, while negative going, because the negative signal excursion would exceed a 10% duty cycle. If inverted video needs to be transmitted, the AC coupled mode should be used.

The AC coupled mode should be used for sinusoidal signals that swing equally positive and negative from their average values. For example, audio and multiple subcarrier signals would fit in this category. The AC coupled mode is selected by connecting Input Coupling pins 2 and 3 (module pins P5 and P4). In this mode, one section of U4 functions as an error amplifier and its output is integrated by the U4, C19 integrator referred to earlier. As with the DC restorer, the integrator's output is a DC bias that is added to the input signal by U1. The integrator functions as a low pass filter for the error signal that is the difference between the DC level of the input signal replica at the output of network R23-R25, L6, C15 and C16 and the reference voltage set by the Frequency control, R26, and U4 pin 3. This negative feedback path around U1's forward gain for very low frequencies, less than 1 Hz, to be near zero and its gain for higher frequencies set by R18 and R19. Thus, the effect of AC coupling is achieved without actually having a coupling capacitor in



Level 4 Demodulator
Block Diagram

Figure 3.3.3.2.2-1

the main signal path.

The DC coupled mode should be used only for signals where the DC component of the signal must be maintained. This mode requires an external adjustable resistance to set the modulator's carrier frequency so that the frequency deviation remains within the range that was optimized for linearity. This mode is selected by connecting Input Coupling pins 2 and 4 (module pins P5 and P3.) This connection converts integrator U4 into an inverting op amp. A DC bias current into the junction of Input Coupling pins 2 and 4 is used to set the modulator's carrier frequency. With this connection, there is no bias controlling feedback around U1.

3.3.3.2.2 Demodulator Circuit Description

Figure 3.3.3.2.2-1 is the block diagram and Figure 3.3.3.2.2-2 is the detailed schematic of the demodulator. The demodulator is a pulse counting type of FM discriminator. A narrow pulse is generated for each zero crossing of the input carrier by delayed and undelayed replicas of the carrier to an Exclusive or gate. The pulse width is a function of the delay and not the input frequency. The pulse train is low pass filtered to allow only the average value of the pulses, which contains the modulating signal, to the succeeding stages.

The demodulator's input is a frequency modulated square wave at balanced ECL logic levels that comes from the Level 2 Receiver. R1 terminates the balanced twisted pair line which is connected to the differential input of the first section of U1, a triple line receiver. The signal out of the first section goes directly to the Exclusive OR gate, U3, and also through five additional line receiver stages, to provide delay, then to the other input of the Exclusive OR gate. The

balanced output of the EX-OR gate drives a differential transistor pair, Q1 and Q2. The output of Q1 are current pulses whose amplitudes are directly proportional to the collector current of transistor Q3. The collector current of Q3 is regulated by regulating the current of another transistor of the same type, Q4. Since Q3 and Q4 have the same base drive and equal emitter resistors, their currents are approximately equal and will not change as the base emitter voltages changes with temperature. One section of operational amplifier U6 compares the voltage developed by Q4's collector current through R24 with a reference voltage developed by R25, R26, R43, and voltage regulator CR1. Variable resistor R25 is used to set the demodulator output amplitude. The output amplitude can also be adjusted using an external bias to the Output Amplitude Trim input, module pin P3. Diode CR2 protects Q3 and Q4 from base emitter breakdown should an improper voltage be connected to the Output Amplitude Trim input and cause U6 to drive the bases towards -12 volts.

The current pulses from Q1 are low pass filtered by L1 to L3 and C1 to C4. The filter removes all carrier components leaving only the original modulating signal. From the filter, the signal goes through two stages of amplification, video operational amplifiers U4 and U5. Between the two stages is the de-emphasis network R33, R34 and C6. When de-emphasis is not used, the pin is left open and the signal passes through the network without attenuation. CR3 and CR4 protect U5 from differential input voltage over stress which could occur if the Output Coupling terminals were connected improperly or to excessive voltages.

The demodulator has AC and DC output coupling modes. The DC

restore mode is not needed because equipment receiving the video, such as monitors, are designed to accept AC coupled signals and do their own DC restoration. The bias feedback loop operation is similar to that used in the modulator, but the method of selecting modes is different. The AC coupled mode should be used for all signals, symmetrical and asymmetrical, including surveillance and radar video. The DC coupled mode should be used only if the DC component of the signal at the modulator input must be preserved. The AC coupled mode is selected by leaving all OUTPUT COUPLING terminals, module pins P5, P6, P7, open. In this mode, an integrator comprised of R39, R42, C7 and U6 provide high negative DC feedback and negligible AC feedback around the two video gain stages U4 and U5. This causes the forward DC gain of U4 and U5 to be near zero, thus effectively AC coupled. The AC forward gain of U4 and U5 is determined only by their individual feedback components R31, R32, and R35, R36 respectively.

To operate in the direct coupled mode, Output Coupling terminal 1, module pin P7, is grounded. This shorts out the feedback from the demodulator's output. Also, Output Coupling terminals 2 and 3, module pins P6 and P5, must be connected together and a bias current supplied to the junction. This connection converts U6 from an integrator to an inverting amplifier. The demodulator's output DC level is controlled by the bias current supplied to the junction of module pins P5 and P6.

4.0 ADM Test Program

4.1 Description

The MFOX Level 1, 2 and 4 ADMs were subjected to test procedures delineated in the CDRL B013 Test Plan and Procedures and the test results were analyzed in the CRDL B014 Test Report. Testing was

performed per these CDRLs to determine compliance with contractual requirements. Testing is summarized in paragraphs 4.1.1 thru 4.1.5. The test procedure list is reprinted from the test plan on the following pages.

Preliminary Acceptance Tests

LEVEL 1

- 1.1.1 Transmitter Static Test
- 1.1.2 Transmitter Dynamic Test
- 1.1.3 Receiver Line Driver and Activity Sensor Tests
- 1.1.4 Receiver Dynamic (BER) Tests
- 1.1.5 LED Driver Open LED Alarm Test
- 1.1.6 Un-Assigned
- 1.1.7 Un-Assigned
- 1.1.8 LED Output Power Characterization
- 1.1.9 Un-Assigned
- 1.1.10 Un-Assigned

LEVEL 2

- 1.2.1 Transmitter Static Test
- 1.2.2 Transmitter Dynamic Test
- 1.2.3 Receiver Line Driver and Activity Sensor Tests
- 1.2.4 Receiver Dynamic (BER) Tests
- 1.2.5 LED Driver Open LED Alarm Test
- 1.2.6 Un-Assigned
- 1.2.7 Un-Assigned
- 1.2.8 LED Output Power Characterization
- 1.2.9 Un-Assigned
- 1.2.10 Un-Assigned
- 1.2.11 Encoder Data Rate/Format Tests
- 1.2.12 Decoder Rate/Format Tests

LEVEL 4

- 1.4.1 Modulator Acceptance Tests
- 1.4.2 Demodulator Acceptance Tests

Design Verification Tests

LEVEL 1

2.1.1	Transmitter Static Test
2.1.2	Transmitter Dynamic Test
2.1.3	Receiver Line Driver and Activity Sensor Test
2.1.4	Receiver Dynamic (BER) Test
2.1.5	Long FO Cable Link Test
2.1.6	LED Wavelength/Spectral Width Test
2.1.7	LED Frequency Response
2.1.8	Size and Weight
2.1.9	Maintainability

LEVEL 2

2.2.1	Transmitter Static Test
2.2.2	Transmitter Dynamic Test
2.2.3	Receiver Line Driver and Activity Sensor Test
2.2.4	Receiver Dynamic (BER) Test
2.2.5	Long FO Cable Link Test
2.2.6	Size and Weight
2.2.7	Maintainability
2.2.8	Encoder Data Rate
2.2.9	Decoder Data Rate
2.2.10	LED Frequency Response

LEVEL 4

2.4.1	End-To-End Signal to Noise Ratio Tests
2.4.2	Mod/Demod Size and Weight
2.4.3	Mod/Demod Maintainability

OTHER TESTS

2.0.4.2.6-1	Burn-in
2.0.4.2.6-1	Burn-in Confidence Test
2.0.4.2.7	Environmental Qualification Tests
2.0.4.2.7.1	Environmental/EMI System Reference Test
2.0.4.2.7.2	Environmental/EMI System Monitor Test
2.0.4.2.8	EMI Tests

4.1.1 Acceptance Test Procedures

These tests are verification that a specific requirement is met by the exercising of the applicable unit(s) appropriate conditions in accordance with test procedures. PAT tests are tests that are conducted on every unit.

All units passed all relevant acceptance tests with but one exception. One Level 2 Receiver experienced an alarm failure that was traced to a printed wiring assembly component failure. The PWA was replaced and the receiver was successfully retested. Since all units are acceptance tested, the results can be summarized as one failure for 51 units tested.

4.1.2 Design Verification Test

For those requirements not tested by a PAT on each unit, each unit type was subjected to a design verification test.

The tests referred to in this paragraph apply only to the extensive room ambient electrical and optical tests and not the EMI, Environmental, Maintainability and Reliability tests described in 4.1.3 thru 4.1.5.

All DVT performance requirements were met or exceeded with the exception of the Level 2 Receiver Dynamic Range requirement of 27 dB. The MFOX design guarantees a 24 dB dynamic range; a 3 dB short fall. The only practical consequence of this is the necessity of an optical attenuator when the transmitter and receiver are connected back-to-back or over very short distances. Since the purpose of the system is communication over a distance, this drawback is negligible. In summary all design verification testing was in compliance with contractual requirements with the above solitary exception.

4.1.3 Environmental Qualification Test

The Environmental Qualification Test Program included natural and induced environmental tests and some electrical performance tests.

The tests were tailored to demonstrate the compliance of the equipment with the applicable requirements of the equipment specifications. The environmental performance was established by introducing the required environment and by testing and inspecting before, during, and after each test to the appropriate electrical and mechanical parameters.

The MFOX ADMs passed all of the environmental qualification test requirements and are in compliance with the appropriate specifications.

A summary of the test results is provided below:

High Temperature	Passed without incident.
Low Temperature	Passed with retest. During the performance test, Level 1 Transmitter S/N 005 failed due to a manufacturing defect. Level 4 Modulator S/N 006 was inoperative because of a blown fuse on the test equipment. Level 1 Transmitter S/N 005 was replaced with S/N 004, and the fuse on the test equipment was replaced. The test sequence was repeated on the Level 1 Transmitter S/N 004 and the Level 4 Modulator S/N 006 and passed without incident.
Humidity	Passed. During the post-test reference test, Level 1 Transmitter S/N 001 failed. Upon investigation, the LED driver had a low output due to a non-humidity related random part failure and was replaced. The test sequence was repeated on Level 1 Transmitter S/N 004 and passed without incident.
Altitude	Passed without incident.

Vibration Passed without incident.

Shock, Drop Passed without incident.

4.1.4 EMI

The following tests were performed on the MFOX units as directed in the test plan to evaluate the UUT in accordance with the requirements of MIL-STD-461B, and MIL-STD-462, Notice 2.

- a. CE01 - Conducted Emissions, Power Leads, 30 Hz to 15 KHz
- b. CE03 - Conducted Emissions, Power Leads, 15 kHz to 25 MHz
- c. CS01 - Conducted Susceptibility, Power Leads, 30 Hz to 50 kHz
- d. CS02 - Conducted Susceptibility, Power Leads, 50 kHz to 25 MHz
- e. CS06 - Conducted Susceptibility, Spikes, Power Leads
- f. RE02 - Radiated Emissions, Electric Field, 14 kHz to 10 GHz
- g. RS03 - Radiated Susceptibility, Electric Field, 14 kHz to 10 GHz

4.1.4.1 Conducted Emissions

Conducted Emissions levels were above specified limits at select frequencies. The source of the emissions was traced to the clock and its lower harmonics and to the direct spectrum of the transmitted data. These are intentional signals and their imprint on the power supply and ground plane is within expectations.

It was demonstrated for levels 2 and 4 that the emissions can be controlled at the MFOX/host interface with the addition of capacitance. The same applies to level 1 except that given the better baseline results obtained in this mode, less capacitance would be required.

The MFOX units are components and not stand alone units. The

power lines are secondary in nature and therefore emissions will be attenuated by the primary power supply in the host unit, so that their impact on the host unit's power source is minimized.

4.1.4.2 Conducted Susceptibility

The purpose of the conducted susceptibility tests as specified in the MFOX development specification was for information only in order to define interface requirements for the host units. In general, the susceptibility responses were not major disruptions (the system linkup remained intact) but caused minor degradations in the transmitted information.

4.1.4.3 Radiated Emissions

The test results should be considered worst case since up to six modules were tested at one time depending on the system level. Emissions in Level 1 fully complied with the test plan. Level 2 was investigated since it was the worst case and the same conclusions should apply for level 4. With Level 4, the amount by which the emissions exceeded the test limits was close to the 3 dB accuracy of the detection system.

The Level 2 investigation indicated that the primary source of the radiated emissions was the exposed electrical mounting pins. To a lesser extent leakage was also detected emanating from the top cover seams of the modules. With the encoder operating by itself, the levels were compliant when its pins were shielded.

For applications where the host equipment does not provide adequate attenuation of radiated emissions, optional case designs could be made available which provide feed-thru pin shielding. Further improvements could be achieved if an EMI gasket is used to

shield the top cover seam.

4.1.4.4 Radiated Susceptibility

The primary entry point for the radiated interference is suspected to be the exposed module pins. This does not appear to be a major problem since the host unit or installation could afford additional shielding effectiveness. The units did not lose sync nor were bit error rate failures detected. All susceptibility responses were aesthetic in nature, that is, slightly distorted waveforms on the oscilloscope and hash or horizontal lines on the video test pattern monitor.

4.1.5 Reliability and Maintainability

4.1.5.1 Reliability

The MFOX Reliability requirement was verified by collecting and analyzing all operating test hours and failures for all MFOX system testing. The observed MTBF was compared to the required MTBF to determine an accept/reject decision.

The MTBF requirement for a Level 1, Level 2 and Level 4 system was calculated and a composite system MTBF of 5,886 hours was determined. The MFOX systems were tested a total of 1525 hours with one relevant failure. The upper and lower MTBF values were calculated based on 1525 hours and one failure.

The demonstrated MTBF at an 80% confidence level is 392 hours lower MTBF and 14,474 hours upper MTBF which covers the required 5,886 hours. The necessary MTBF was demonstrated even through the relatively stringent qualification testing.

4.1.5.2 Maintainability

The objective of Maintainability Demonstration Test was to

verify compliance of Level 1, Level 2 and Level 4 configurations to the specified Maintainability requirements. The specification is a mean-corrective-maintenance time of no greater than 1.0 hours (95th percentile) at the organizational level of maintenance.

The Maintainability Demonstration Tests were performed in accordance with MIL-STD-471A, Notice 1, Test Method 9 and the procedures called out in the Test Plan. A total of 50 simulated faults were randomly induced and a repair time was noted for each fault.

The MFOX units met or exceeded the Maintainability requirement by wide margins in every case. The time taken to isolate the fault, remove and replace the unit and verify the repair was an order of magnitude less than the mean-corrective-maintenance of 0.5 hour.

5. Conclusions

This MFOX program phase has demonstrated the feasibility of a family of MFOX fiber optic modules to address ground based tactical communication needs.

The Advanced Development Models (ADM's) of MFOX Levels 1, 2 and 4 have demonstrated feasibility to address current needs and it is recommended the next programatic step be implemented. An Engineering Development Model phase to prepare for and to include appropriate production quantities is suggested to encourage broader usage of the modules.

The Experimental Models of MFOX Levels 3 and 5 have demonstrated the performance necessary to proceed from the Experimental Model phase to the next programatic step - namely the Advanced Development Model (ADM) stage.

The MFOX family concept has been demonstrably strengthened by the building, testing, delivery and demonstration of the hardware provided by this phase of the MFOX program. The favorable results strongly suggest continuation of the evolutionary aspects of the MFOX Family Concept - namely progressing to the next programatic stages as previously described in this section.