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The feasibility of this approach has been clearly demonstrated in the Phase I research effort, in which successful selective deposition of GaAs films on patterned Si wafers was achieved and the deposited films were characterized by a number of techniques. Preliminary results clearly indicate the effectiveness of this approach to eliminate wafer bow, minimize film cracking, and improve the quality of the heteroepitaxial films. A new deposition technique for GaAs-on-Si by Atomic Layer Epitaxy (ALE) has been introduced which has the potential of producing superior quality GaAs-on-Si films.

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A Final Report for:

SELECTIVE AREA EPITAXY OF GALLIUM ARSENIDE ON SILICON

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SUMMARY

The proposed research program was to investigate selective-area epitaxy of GaAs-on-Si by Metal Organic Chemical Vapor Deposition (MOCVD) as a means of reducing the thermal expansion mismatch effects, hence, improving the deposited film quality, wafer bow, and eliminating film cracking. This has been achieved by MOCVD of GaAs through openings patterned in the silicon dioxide coated wafers. The object of this research program was to develop the technology that will yield device quality GaAs-on-Si and a process applicable for monolithic integration of the high speed and/or optical communication capabilities of GaAs with the sophistication of the Si VLSI technology.

The feasibility of this approach has been clearly demonstrated in the Phase I research effort, in which successful selective deposition of GaAs films on patterned Si wafers was achieved and the deposited films were characterized by a number of techniques. Preliminary results clearly indicate the effectiveness of this approach to eliminate wafer bow, minimize film cracking, and improve the quality of the heteroepitaxial films. A new deposition technique for GaAs-on-Si by Atomic Layer Epitaxy (ALE) has been introduced which has the potential of producing superior quality GaAs-on-Si films.

This research and development program may lead to a technology with several important benefits. One such benefit is the replacement of GaAs bulk substrates, which are fragile, of low thermal conductivity, available in relatively small diameters and quite expensive, with Si substrates which have advantages in all the aforementioned categories. Another benefit of selective epitaxy is the feasibility of trans- and inter-chip optical interconnects which are immune to crosstalk and interference and have much faster data transmission rates compared to conventional wire interconnects. The successful completion of these research efforts will result in the development of a new generation of MOCVD reactors capable of efficient epitaxial growth in the conventional MOCVD and ALE modes.

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1.0 INTRODUCTION

This report describes the results of a Phase I SBIR program entitled "Selective Area Epitaxy of Gallium Arsenide on Silicon." The objective of this project was to investigate selective epitaxy by Metalorganic Chemical Vapor Deposition (MOCVD) process as a means of reducing the thermal expansion mismatch effects in GaAs-on-Si and hence minimizing wafer bow and film cracking. Another objective is to demonstrate the feasibility of selectively depositing high quality GaAs on the patterned Si wafers.

1.1 Background

The epitaxial growth of GaAs and its alloys on Si has recently been attracting strong interest.[1,2] Some of the reasons for this are that Si is a low cost, lightweight substrate with high mechanical strength, excellent crystalline quality, and high thermal conductivity. Si is also available as a large area substrate. Overall, the most significant reason for growing GaAs based semiconductors on Si is for the Monolithic integration of GaAs and Si (MGS) devices, thus combining the high speed and/or optical communication capabilities of GaAs with the sophistication of the Si VLSI technology.

In the past few years, exciting progress has been realized in the area of GaAs-on-Si. Growth has been reported on Si substrates up to six inches in diameter with thickness uniformity $\pm$ 4% and properties equivalent to those of smaller diameter wafers.[2] Majority-carrier devices, MESFETs and MODFETs, have been fabricated with DC and microwave characteristics equal to those fabricated on GaAs substrates.[4] On the other hand, minority-carrier devices are more adversely affected by the high dislocation density present in GaAs-on-Si films (typically $\cong 10^8$ cm^{-2}) than are the majority-carrier devices. However, lasers,[5,6] LEDs,[7] and solar cells[8] have been successfully fabricated in GaAs-on-Si structures. The performance of these devices can approach those fabricated in GaAs substrates if the defect density is reduced by two to three orders of magnitude.

The heteroepitaxial growth of GaAs-on-Si faces several problems including the polar/nonpolar interface, the large thermal expansion coefficient difference, and a 4.1% lattice mismatch between GaAs and Si. The deposition of a polar semiconductor (GaAs) on a nonpolar substrate (Si) results in Antiphase Domain Disorder (APD). The approach of

using Si substrates which are tilted from the (001) orientation by 2° to 4° towards the [110] has been implemented to solve this problem. The apparent reason for tilting the substrate off orientation is that this causes the formation of an even number of atomic steps in the Si surface which prevents APD formation.

The two main obstacles to overcome before the full potential of the GaAs-on-Si technology can be realized are:

1. **Thermal Expansion Mismatch** - The thermal expansion coefficient (α) mismatch between GaAs and Si ($5.73 \times 10^{-6}°C^{-1}$ and $2.6 \times 10^{-6}°C^{-1}$ respectively) results in biaxial tensile stresses in the GaAs epi-layer which can lead to film cracking and wafer bowing during the cooling down period from the growth temperature. This has been a serious problem with the growth of GaAs-on-Si. Cracks have been reported in films thicker than a few microns and wafer bowing has been found to interfere with the photolithographic processes.[9]

2. **Lattice Mismatch** - The substantial lattice mismatch between GaAs and Si (4.1%) leads to a high density of threading dislocations. This reduces the diffusion length in minority-carrier devices which adversely affects their characteristics.[10]

1.2 Proposed Approach

The proposed solution to address the thermal expansion mismatch problem has been the employment of selective-area epitaxy of GaAs-on-Si where the GaAs is deposited by MOCVD through openings patterned in the silicon dioxide (SiO_2) coated wafers. The strengths of this approach are discussed below.

1.2.1 Advantages of Selective Epitaxy (SE)

The advantages of selective epitaxy of GaAs-on-Si by MOCVD includes the following:

1. **Monolithic Integration** - The selective epitaxy of GaAs-on-Si would allow the monolithic integration of the optoelectronic and high-speed capabilities of GaAs with the complex circuitry of Si VLSI technology.

2. **Stress Relief** - In the present selective epitaxy approach, the GaAs coverage is limited to 20% of a two-inch Si wafer which implies a significant reduction in the tensile stresses in the film, thereby reducing substrate bow and film cracking. Complete stress relief has been reported in pattern etched GaAs-on-Si wafers for island sizes below 10 microns.[11]

3. **Wafer Flatness** - While the thermal expansion coefficient of SiO_2 ($\alpha = 0.5 \times 10^{-6} °C^{-1}$) is less than that of Si, α of GaAs is greater; hence, by balancing the SiO_2 layer thickness, the GaAs epilayer thickness, and the percentage of the wafer covered with GaAs, a flat wafer is easily achievable.

4. **Defect Reduction** - It is expected that the selectively deposited films will have less defects due to the stress relief associated with the smaller dimensions[11] and the defect reduction associated with lateral confinement.[12] Moreover, we have demonstrated that for conventional GaAs-on-Si, defect reduction can be achieved by the use of a strained layer superlattice buffer.[13,14] The threading dislocations generated at the GaAs/Si interface were found to bend at the SLS interface and propagate parallel to the interface for long distances. Coupling selective epitaxy with other defect-reduction techniques such as thermal annealing, SLS, and thermal cycle growth (TCG) can be the means for producing high quality, crack-free, and flat GaAs-on-Si wafers suitable for MGS devices.

5. **MOCVD** - The use of MOCVD is a good choice for this program since it produces GaAs-on-Si with excellent structural, electrical, and optical properties.[15] Moreover, MOCVD is a volume-amenable process where reactor capacities up to 1800 cm^2 per batch have been reported.[3]

1.2.2 Benefits of Si

The advantages of Si as a substrate for selective epitaxy of GaAs-on-Si includes:

1. **Large Area** - Si wafers are commercially available in up to eight-inch diameter sizes, while GaAs wafers only exist in diameters of up to four inches;

2. **Low Cost** - Si substrates are approximately 30 to 50 times less expensive than GaAs wafers of equal sizes;

3. **Light Weight** - The density of Si (2.3 gm/cm^2) is about half that of GaAs (5.3 gm/cm^3);

4. **Mechanical Strength** - Si wafers are much more rugged than GaAs. An indication of this property is the Knoop microhardness values, which are 1150 and 730 kgm/mm^2 for Si and GaAs, respectively;

5. **Thermal Conductivity** - Si has a thermal conductivity value (1.68W/cm K) that is more than twice that of GaAs (0.55W/cm K).

1.3 Literature Review

This section reviews the literature concerning selective epitaxy of GaAs on GaAs and Si with emphasis on reports that utilize the MOCVD technique.

Recently, the increased demand for high level integration and the emergence of new epitaxial techniques have generated renewed interest in selective-area epitaxy. Although the concept of GaAs selective epitaxy was initiated over 20 years ago using Vapor Phase Epitaxy (VPE),[16] many of its practical applications were precluded due to the difficulty encountered in growing Al compounds using this technique[17] and due to severe faceting formation resulting in distorted polygonal structures;[18] hence, serious investigating of selective epitaxy was not pursued at the time. Selective epitaxy of excellent quality homo-epitaxial films has been demonstrated using MOCVD[19,20] and MBE.[21] While SiO_2 has been the most commonly used mask material, other dielectrics including SiN_x, AlN, native oxide and shadow masks have also been used successfully.[19-22] Typically, epitaxial GaAs is deposited in the patterned window, while a polycrystalline film grows on the oxide. Since polycrystalline GaAs is highly resistive, it can be used for isolation and bridging in integrated circuits.[23] For other devices where the poly material is undesirable it is either etched off, as in the case for MBE and atmospheric pressure MOCVD, or its formation is prevented by the proper choice of growth parameters, as has been recently demonstrated in Japan using low pressure (LP) MOCVD.[20]

Another approach for selective homoepitaxy of GaAs is by atomic layer epitaxy (ALE).[24] In a typical ALE process, the substrate is sequentially exposed to fluxes of Groups III and V reactant species, with only one monolayer of each species remaining on the substrate surface after each exposure. For a review of this growth technique see reference 24a. The deposited film thickness is then determined by the number of deposition cycles and the lattice parameter of the material.[24] Recently, selective epitaxy on GaAs by ALE has been reported by a group at NEC in Japan using GaCl[24b] as well as DEGaCl[24c] and AsH_3 as precursors. GaAs deposition took place only on the unmasked portions of the substrate; no edge growth was observed, and the growth rate dependence on the island size was suppressed with sufficient purging prior to the AsH_3 flow step. This technique is very promising for accurate definition of structures and control over the deposited film thickness and composition.

Selective epitaxy of GaAs-on-Si has been the subject of growing interest in recent years[7,25-27] due to its potential for MGS devices and for improving the quality (i.e., reducing defects and stresses) of the deposited film. Recently, MIT Lincoln Labs has demonstrated the integration of a GaAs/AlGaAs LED and a single Si MOSFET.[7a] Also, they have reported the integration of a LED with a Si-driver circuit composed of 10 MOSFETs. First, the fabrication of the Si MOSFET was done except for contact openings and metallization, then, the wafer was coated with successive layers of SiO_2 and Si_3N_4 to protect the MOSFET structure during the MBE growth of GaAs/AlGaAs. The LED structure was grown in the opening that was etched in the SiO_2/Si_3N_4 film to expose the Si surface. A 3.5 micron thick structure was deposited using MBE, and inside the etched opening single crystalline film was deposited. The polycrystalline material deposited on the mask was subsequently removed by photoresist masking and wet chemical etching. Although the wafer bow, crack density, and dislocation densities were not reported, successful modulation of the LED output has been accomplished at rates exceeding 100 MHz.

Another recent report on MGS by selective epitaxy came from Japan (Toyota Central Research)[25] where they also utilized MBE of GaAs-on-SiO_2-patterned Si wafers. They reported the possibility of eliminating wafer warpage using selective epitaxy. The high-resistivity polycrystalline GaAs film deposited on the mask was used for device isolation of MODFETs.

Embedded growth of GaAs-on-Si where GaAs is epitaxially deposited in Si recesses has been recently reported[26,27] in an attempt to reach a co-planar GaAs-on-Si structure for high resolution metallization. Preliminary promising results have been reported by a research group from Belgium demonstrating 1.25 micron wide Au lines on a nearly planar GaAs/Si structure.[27] However, more serious defect problems are generated in the etched grooves.

Although MOCVD is the technique of choice for production of MGS by selective epitaxy, active research in this field has only been reported in Japan[28] and Europe.[29] One laboratory in Japan has recently reported the use of selective epitaxy to deposit films up to 8 micron thick on Si with no cracks.[28a] More recently, NTT (Japan) has utilized

selective epitaxy to prevent cracks from propagating to the device area. They have demonstrated a high efficiency solar cell (18.3%, one sun AM0) by coupling selective epitaxy with other defect reduction techniques.[28b] Finally, University of Ghent-IMEC (Belgium) briefly reported on successful MGS by selective epitaxy using atmospheric pressure MOCVD where a nearly planar structure was produced. The growth rate of the poly-GaAs and the epitaxial film inside the patterned SiO_2 windows was nearly equal. There was no mention of the structural, optical, or electrical properties of the deposited film.

2.0 SUMMARY of PHASE I RESULTS

The goal of the Phase I effort was to investigate the use of MOCVD to selectively grow GaAs-on-Si through openings patterned in SiO_2 and to explore the effects of this technique on wafer warpage, film cracking, crystalline properties, and threading dislocations.

2.1 Experimental Procedure

In this section, we will discuss the mask design, wafer patterning, and the deposition techniques used for this study. The wafers used for this study were 25 mils thick, two-inch Si substrates oriented 2° off the (100) plane towards the ⟨110⟩.

2.1.1 Photolithographic Mask

The mask was designed so square openings of SiO_2 can be patterned exposing the underlying Si. Figure 2-1a is a pen plot of a single module designed to yield 20% coverage of the patterned area. Each module contained squares with dimensions of 10, 25, 50, 100, 250, 500, and 1000 microns per side. The modules were repeated throughout the wafer area. The mask was fabricated by Advanced Reproduction in North Andover, MA.

2.1.2 SiO_2 Coating and Patterning

Representative two-inch Si wafers were coated with SiO_2 (thermally) in pure oxygen (99.997%) at 1000°C to achieve thicknesses of 500, 1000, and 2000 angstrom films. The oxide thicknesses were verified using ellipsometry. Five additional wafers with 1000 angstroms of SiO_2 coating were further coated with 5000 angstroms of SiO_2 in

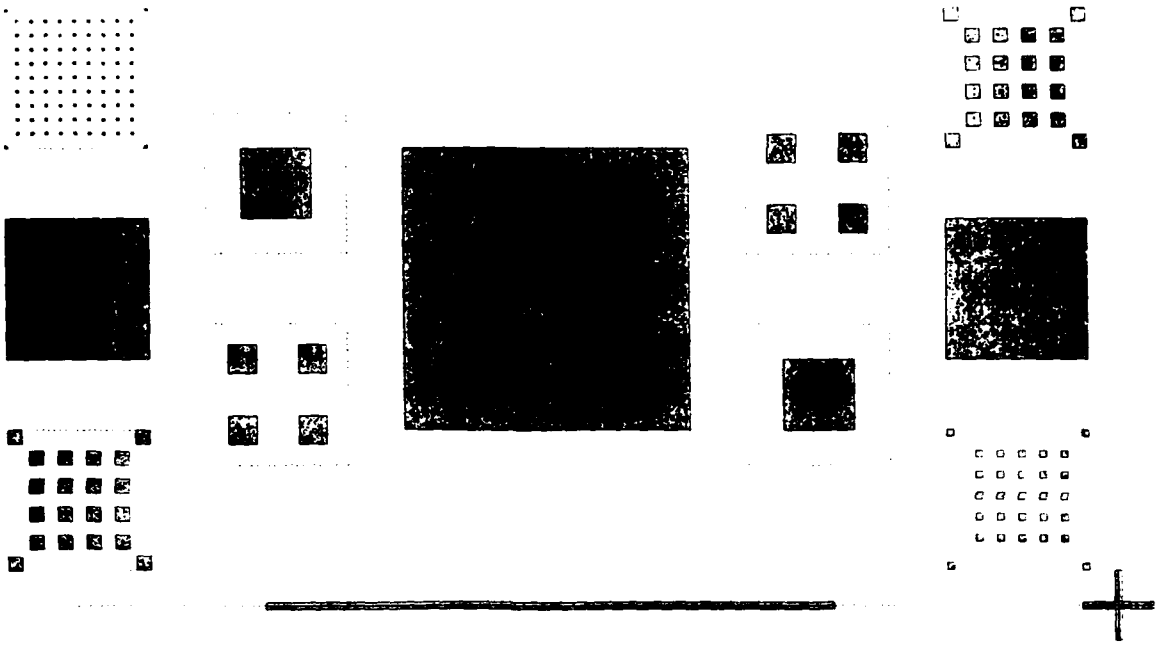

FIGURE 2-1a. PEN PLOT OF SINGLE MODULE.

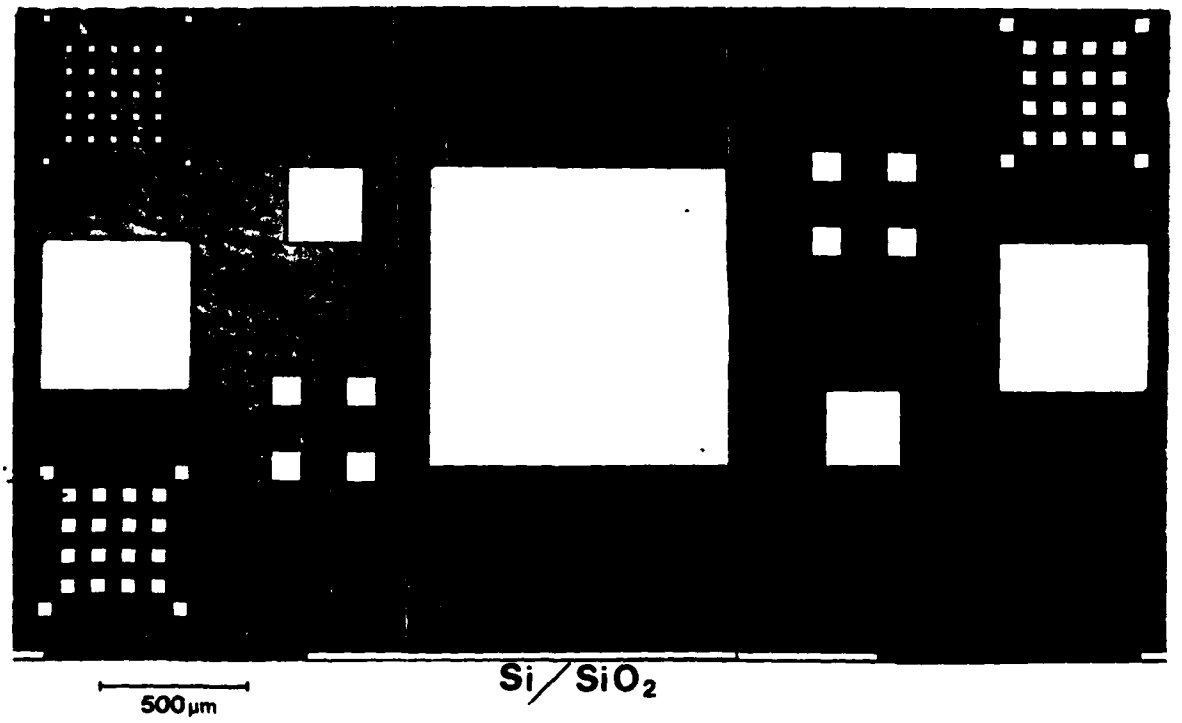

FIGURE 2-1b. OPTICAL MICROGRAPH OF A SINGLE MODULE ON A TWO-INCH SILICON WAFER WITH A 6000 angstrom SiO_2 COATING.

a pyrox reactor, thus creating a fourth group with 6000 angstrom thick oxide. This was done using SiH_4 (5% in N_2) in an oxygen atmosphere at 400°C and a growth rate of ~9 angstroms/sec.

The wafers were photolithographically patterned and etched using the following steps:

1. Positive resist spin-on;
2. Bake out at 90°C for 30 minutes in a N_2 atmosphere;
3. Resist exposure in a Cobilt contact mask aligner;
4. Resist developing;
5. Bake out at 120°C for 30 minutes in a N_2 atmosphere;
6. Pattern etching using buffered HF;
7. Standard RCA wafer clean.

Figure 2-1b is an optical micrograph of a single pattern module on silicon with a 6000 angstrom SiO_2 coating. The oxide thickness was checked with a microstylus Tencor α-step that confirmed the ellipsometry measurements. The buffered HF etch is a standard step for our conventional Si wafer preparation for GaAs-on-Si growth; hence, the patterning process is compatible with the current MGS technology. Figure 2-2 is an optical micrograph of a typical Si wafer after patterning.

2.1.3 Deposition of GaAs on Patterned SiO_2 on Si

Two different deposition techniques were employed for selective epitaxy of GaAs-on-Si. Depositions were carried out in a Spire SPI-MO CVD^{TM} 450 reactor; the precursors used were trimethyl gallium (TMG) and AsH_3 (10% in H_2) and the main carrier gas was H_2. The deposition techniques were conventional atmospheric pressure growth and GaAs-on-Si by ALE.

1. **Conventional GaAs-on-Si** - The basic GaAs-on-Si growth procedure developed in our laboratory is carried out at atmospheric pressure and consists of three steps:

   a. A high-temperature bakeout in H_2 for 30 to 60 minutes at approximately 1000°C;

   b. A low-temperature nucleation step in which ~200 angstroms of GaAs is deposited at 400°C;

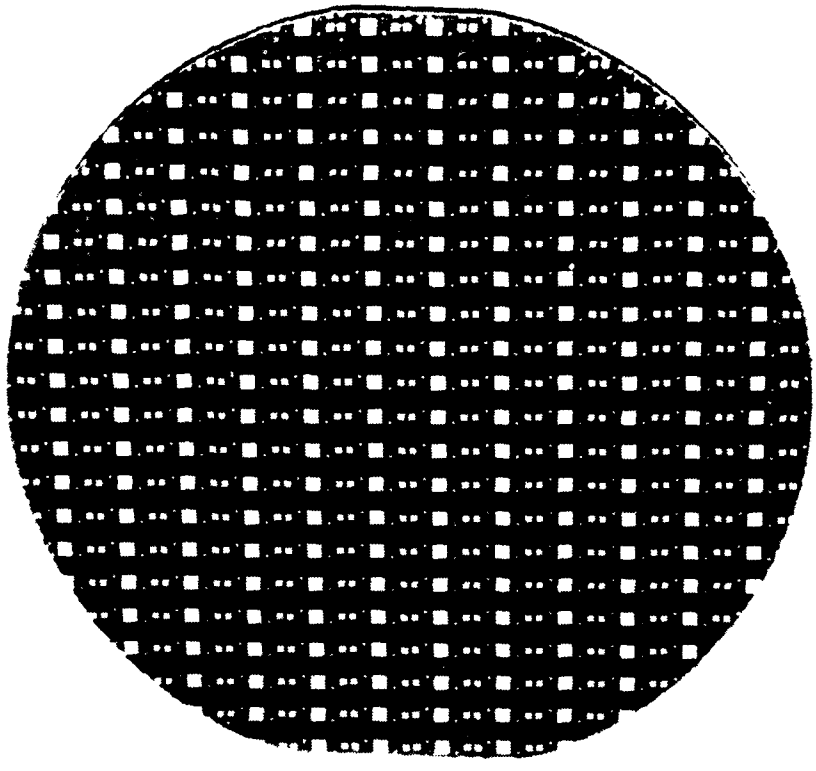

FIGURE 2-2. OPTICAL MICROGRAPH OF A 2-INCH SILICON WAFER AFTER A 1000 angstroms SiO_2 COATING AND PATTERNING.

c. A film-growth step in which GaAs is deposited at:

Temperature = 675°C
V/III ratio = 15
Growth Rate = 10 angstroms/sec

Excellent quality GaAs-on-Si is typically deposited using this technique. Figure 2-3a is a typical Nomarski optical micrograph of the as-grown surface morphology. Figure 2-4a is a bright field cross-sectional Transmission Electron Microscope (XTEM) image showing the types of defects typically present. For an as-grown 4 micron thick film the dislocation density measured by planview TEM is $\cong 2 \times 10^8$ cm^{-2} with a stacking fault and microtwin density of $\sim 10^7$ cm^{-2}.

2. MOCVD by ALE - This is a new deposition procedure recently developed at Spire for GaAs-on-Si and is still under further investigation for its potential in producing high quality films. The advantages of ALE have

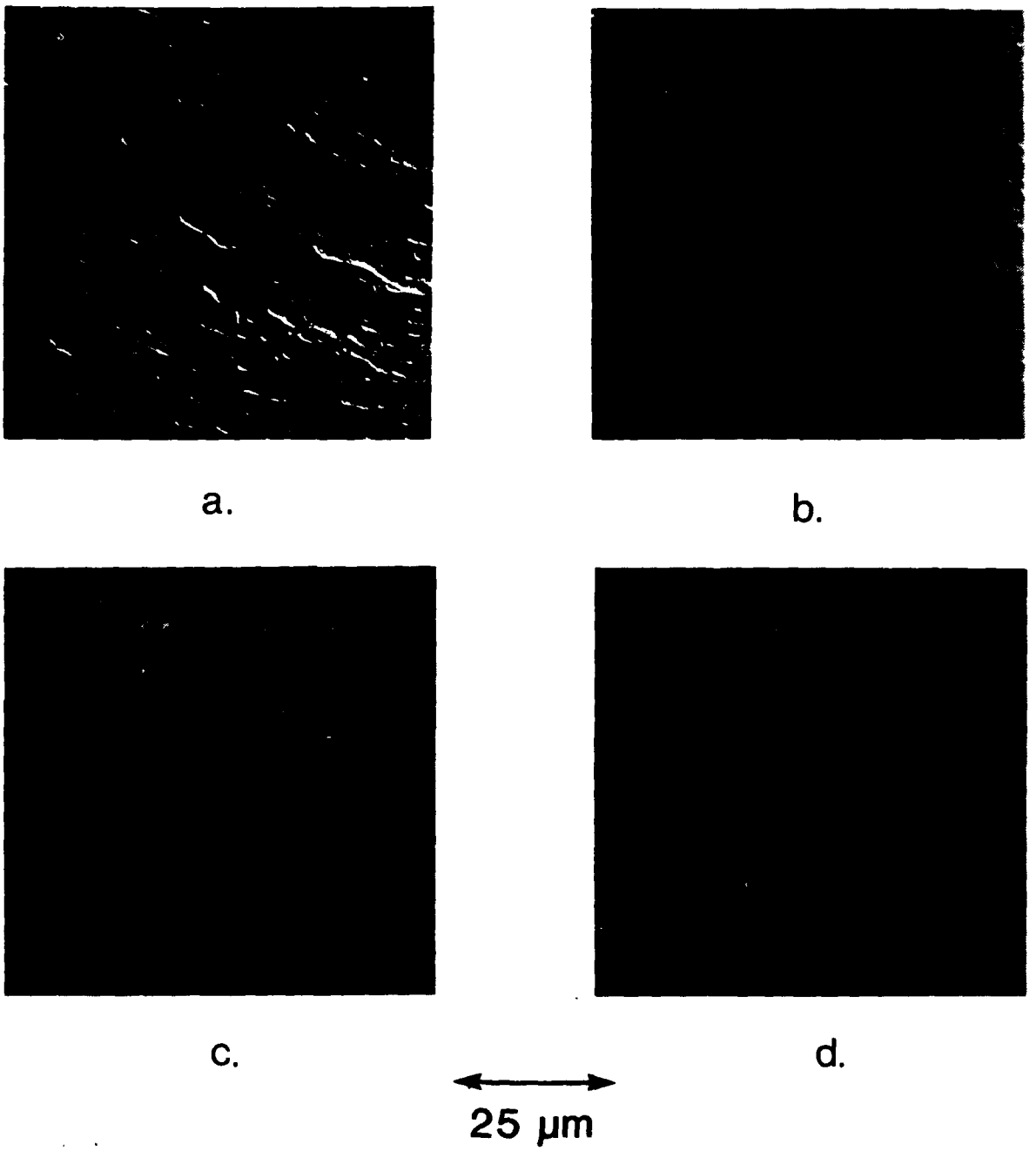

FIGURE 2-3. NOMARSKI OPTICAL MICROSCOPY OF GaAs DEPOSITED BY: (a) CONVENTIONAL TECHNIQUE; (b) ALE TECHNIQUE; (c) SELECTIVE EPITAXY CONVENTIONAL; (d) SELECTIVE EPITAXY BY ALE.

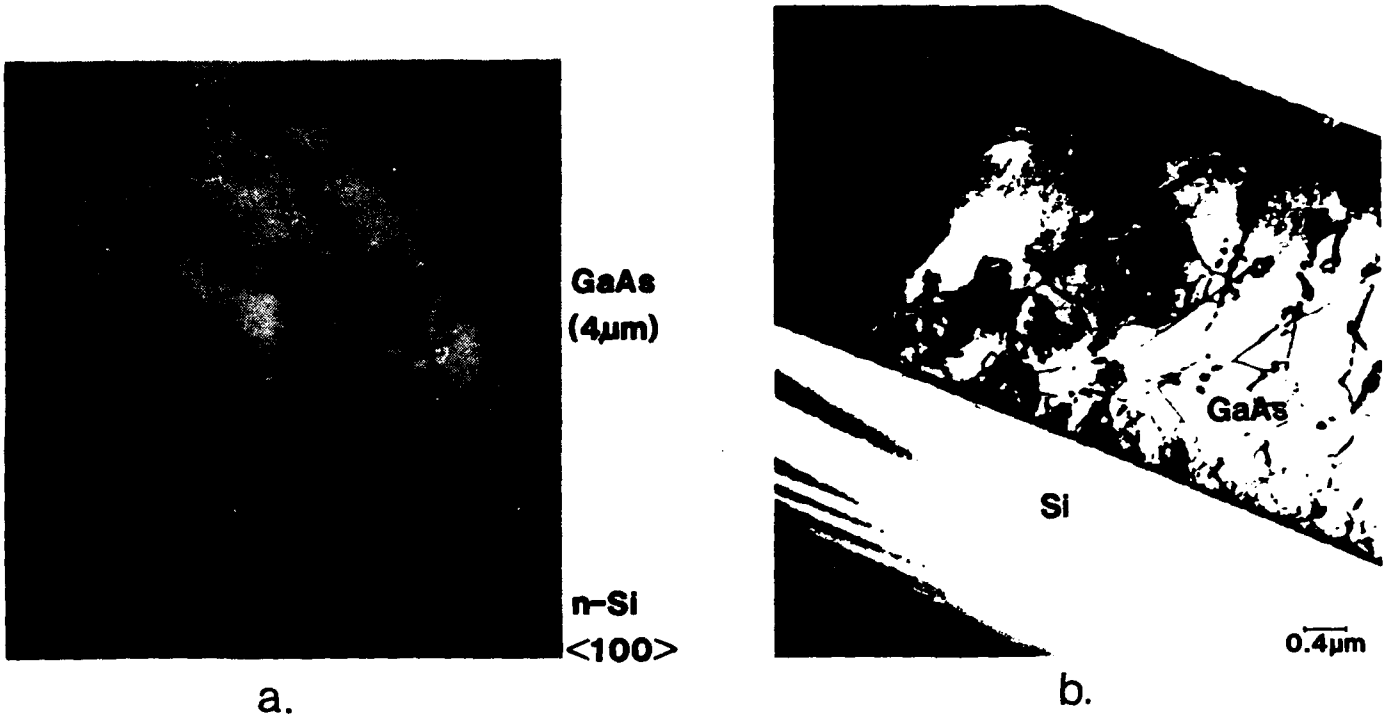

FIGURE 2-4. CROSS SECTIONAL TEM COMPARISON OF GaAs-on-Si DEPOSITED BY: (a) CONVENTIONAL TECHNIQUE and (b) ALE TECHNIQUE.

been discussed in the literature;[24] however, its main feature as mentioned in Section 1.3 is that only one monolayer (e.g., of GaAs) is deposited per ALE cycle in a self-limiting manner. The deposited thickness is determined by the number of ALE cycles and the lattice parameter of the material. The advantages of ALE for GaAs-on-Si include low temperature deposition, two-dimensional growth, suppression of three-dimensional growth, and elimination of anti-site defects (e.g., EL_2),[24] Spire has recently demonstrated the first GaAs-on-Si by ALE.[29] The deposition procedure includes:

a. A high temperature bake out in H_2 at 1000°C for 30 to 60 minutes to desorb the oxide (SiO_2) typically formed on the Si wafer;

b. A nucleation step by ALE in the temperature range 400 to 475°C, in which 100-200 angstroms of GaAs is deposited;

c. Film growth can proceed by either ALE or conventional L.P. MOCVD at:

Temperature = 675°C
V/III Ratio = 50
Growth Rate = 10 angstroms/sec
Pressure = 76 torr

For the present experiments Step c was carried out using LP MOCVD. This technique will be referred to as the ALE process. Figure 2-3 is a Nomarski optical micrograph of GaAs-on-Si by ALE showing a shiny, smooth surface morphology. Figure 2-4b is a bright field XTEM of GaAs-on-Si by ALE where the defects are typically shrunk to the interface with no microtwins. The use of ALE in the nucleation step (b) serves as a foundation for subsequent conventional GaAs deposition resulting in a film which appears to have less defects compared to the conventional two-step growth technique commonly employed for GaAs-on-Si.[1,2]

The distinctive advantages of ALE derive from the capability to deposit one monolayer and then to permit the substrate surface to equilibrate thermodynamically before the arrival of more atoms or molecules. This enforces 2-dimensional growth, circumvenitng the nucleation process that leads to the impingement and coalescence of 3-dimensional crystallites, with the concomitant introduction of dislocations and planar defects. It also minimizes formation of the point defects (vacancies, interstitials, antisite defects) that account for much of the degradation of the electronic properties of III-V compounds. A further benefit is that lower substrate temperatures can be used. In addition, it is not essential that the entire epitaxial structure be grown by ALE. Rather, a seed layer 10-30 nanometers thick is grown by ALE, and then growth is continued by conventional MOCVD at a deposition rate on the order of several micrometers per hour.

Both of these techniques, although non optimized for selective epitaxy, were successfully used for selective epitaxy of GaAs on the patterned wafers. In the proceeding section we will summarize the results of deposition experiments using these two techniques. Characterization tools including optical microscopy, TEM, X-ray diffraction Topography (XRT), surface profilometry, and photoluminescence (PL) have been utilized for this research effort.

2.2 Characterization Results

2.2.1 Surface Morphology

Figure 2-5 shows typical optical micrographs of selective epitaxy GaAs-on-Si by conventional (Figure 2-5a,c) and ALE (Figure 2-5b,d) processes. Selective epitaxy by conventional MOCVD typically has epitaxial GaAs deposited in the patterned windows, while the SiO_2 mask is covered with polycrystalline GaAs. This behavior is similar to that reported for selective homoepitaxy of GaAs[19] at atmospheric pressure, where the poly film on the mask is sparse for high deposition temperatures (T is greater than 750°C) and low V/III ratios, and is continuous for lower deposition temperatures (T is less than 650°C) and high V/III ratios. Figure 2-5 (a,c) also shows the surface-migration-induced depletion of the poly-growth around the peripheries of the patterned squares. This surface migration (diffusion) of the reactants is determined by the deposition temperature, pressure, and V/III ratio, and is independent of the square size. In fact if the surface diffusion length (SDL) is greater than the separation between squares, the mask surface will have very little or no poly-growth (Figure 2-6). However, these reactants that migrate onto the open squares are responsible for the edge growth and the growth rate enhancement which will be discussed later (Section 2.2.7).

Figure 2-5 (b,d) shows selective epitaxy by the ALE process where the poly-growth on the mask is completely suppressed. Elimination of the poly-growth on the mask may be of interest, since it eliminates the etching step for the poly-growth in MGS[7c] and opens the door for investigating the side walls as potential mirrors for optoelectronic integration. This phenomenon may be due to the relatively weak sticking coefficient of the Ga species to the oxide mask and the short residence time of the adsorbed reactants, especially at low pressures. Hence, after one ALE cycle a monolayer of GaAs is formed in the etched windows, while the weakly physisorbed species are purged off the oxide. Such a behavior has been reported for selective epitaxy of homoepitaxial GaAs by a Japanese group.[24] Moreover, poly-growth suppression has also recently been reported by a Japanese group using LP MOCVD at 10 torr.[20]

The surface morphology of the films deposited by either growth technique is nearly identical to those deposited on unpatterned wafers irrespective of the oxide thickness (see Figure 2-3c,d).

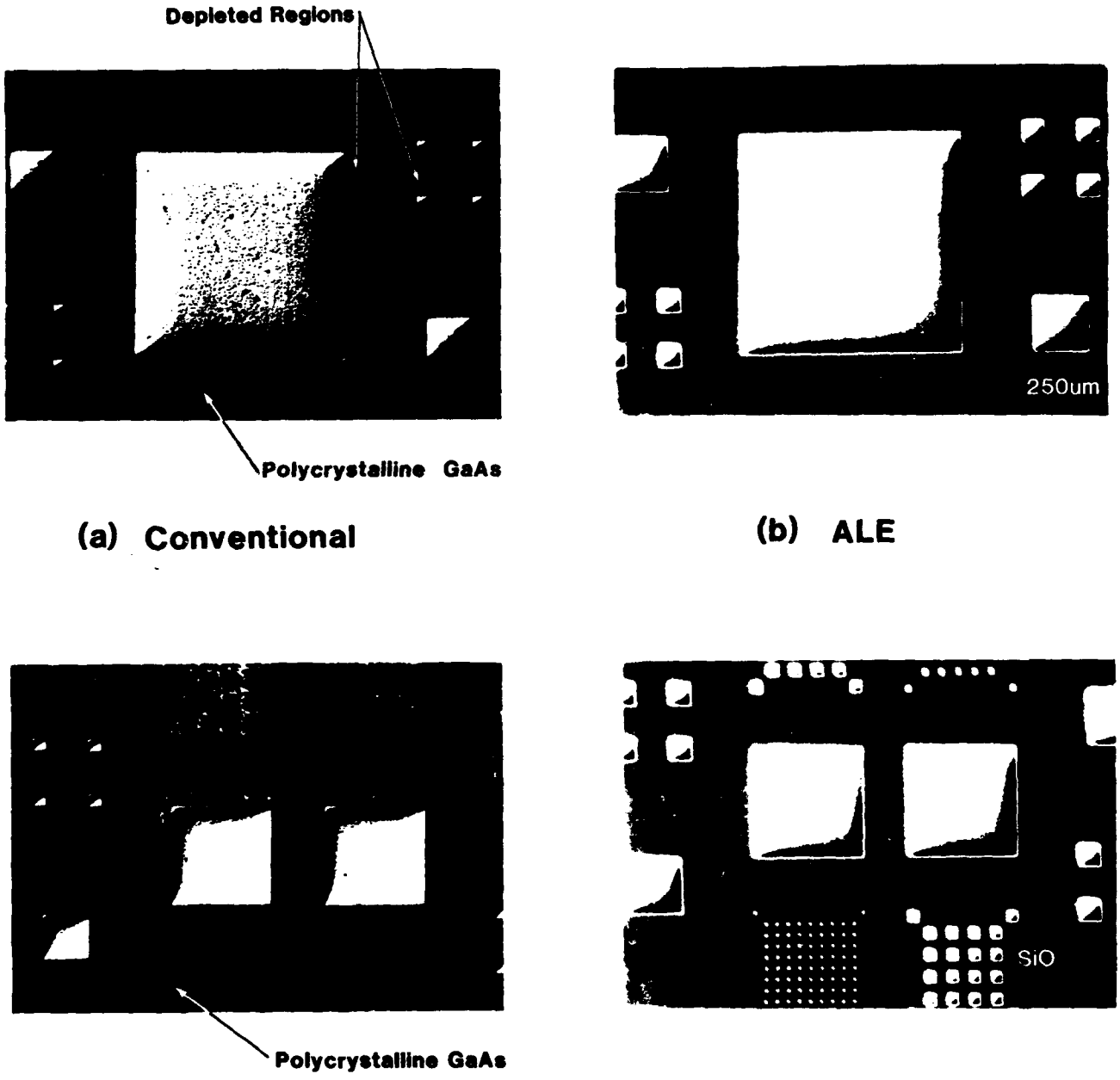

FIGURE 2-5. OPTICAL MICROGRAPH OF SELECTIVE EPITAXY OF GaAs-on-Si DEPOSITED BY: (a,c) CONVENTIONAL GROWTH AND (b,d) ALE NUCLEATION.

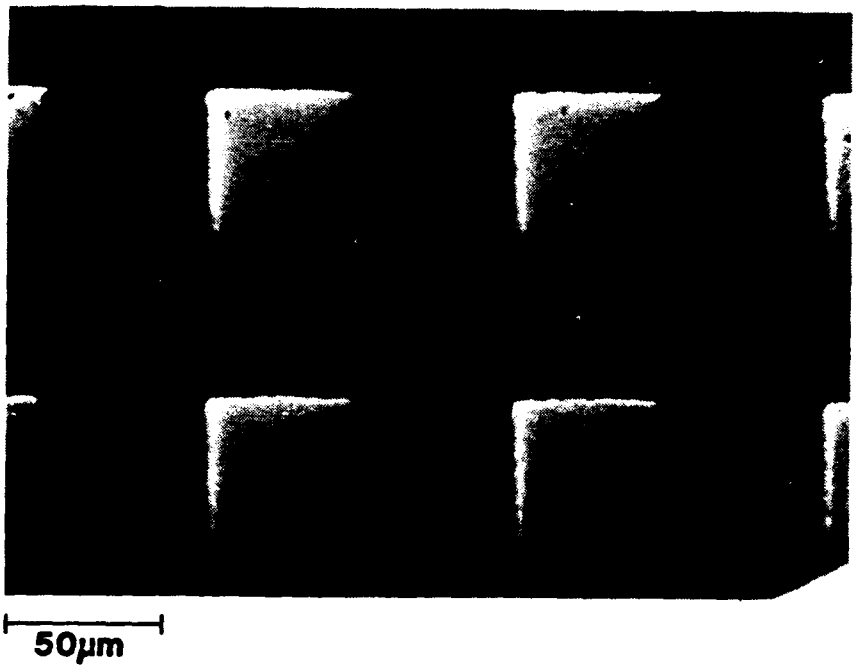

FIGURE 2-6. SELECTIVE AREA EPITAXY OF GaAs-on-Si BY CONVENTIONAL MOCVD SHOWING ABSENCE OF POLY-GROWTH ON THE OXIDE DUE TO SURFACE MIGRATION.

2.2.2 Transmission Electron Microscopy (TEM)

The selectively deposited films by conventional and ALE techniques have been characterized using XTEM and planview TEM at North Carolina State University (NCSU), courtesy of Prof. N.A. El-Masry. The types and nature of defects were found to be similar to their respective growth on unpatterned wafers. Figure 2-7a is a typical XTEM of selective epitaxy GaAs-on-Si by conventional MOCVD where microtwins, dislocations, and stacking faults have been identified (see Figure 2-4a for comparison). The dislocation density of a 4 micron thick film was determined by planview TEM (Figure 2-9a) to be $\sim 1\text{-}2 \times 10^{8}$ cm^{-2} which is comparable to MGS on unpatterned wafers. Figure 2-7b illustrates an occasional problem for small squares (10 micron) where incomplete removal of the SiO_2 from the window resulted in polycrystalline growth. This problem has been eliminated by using a defrothing reagent during the buffered HF etching of the windows.

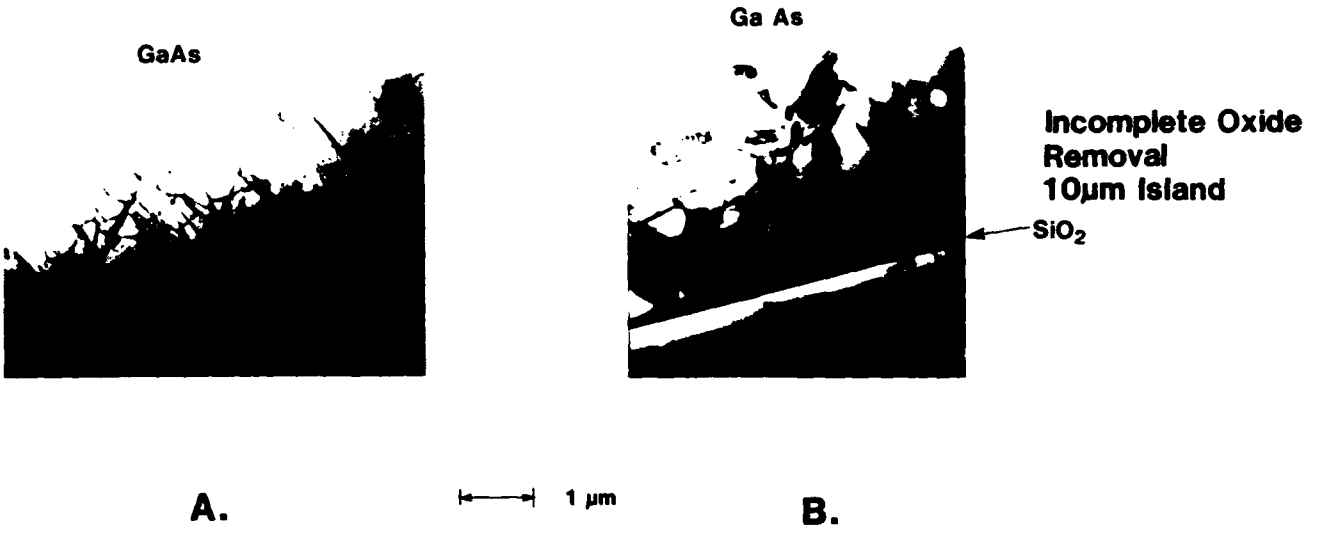

FIGURE 2-7. CROSS SECTIONAL TEM OF SELECTIVE EPITAXY GaAs-on-Si BY CONVENTIONAL MOCVD: (a) 50 micron SQUARE AND (b) OCCASIONAL INCOMPLETE OXIDE REMOVAL IN THE 10 micron SQUARES.

Figure 2-8 shows cross sectional TEM bright field images of selective epitaxy GaAs- on-Si by ALE for two squares with dimensions of (a) 1000 micron and (b) 100 micron per side. It is clear that the nature of the defects is completely different from the conventional MOCVD mode. There are no microtwins and the threading dislocation segments are very short, indicative of their propagation close to the foil normal. This may be advantageous since it may result in a net reduction in the dislocation density. Also the defects are shrunk to the GaAs/Si interface, a feature normally observed in conventional MGS samples after furnace annealing. The nature of these dislocations will be investigated in Phase II using g•b analysis where g is a vector representing the reflecting plane normal and b is the burger's vector. Figure 2-9b shows a planview TEM micrograph of a selective epitaxial film by ALE, indicating a dislocation density of 10^8 cm^{-2}.

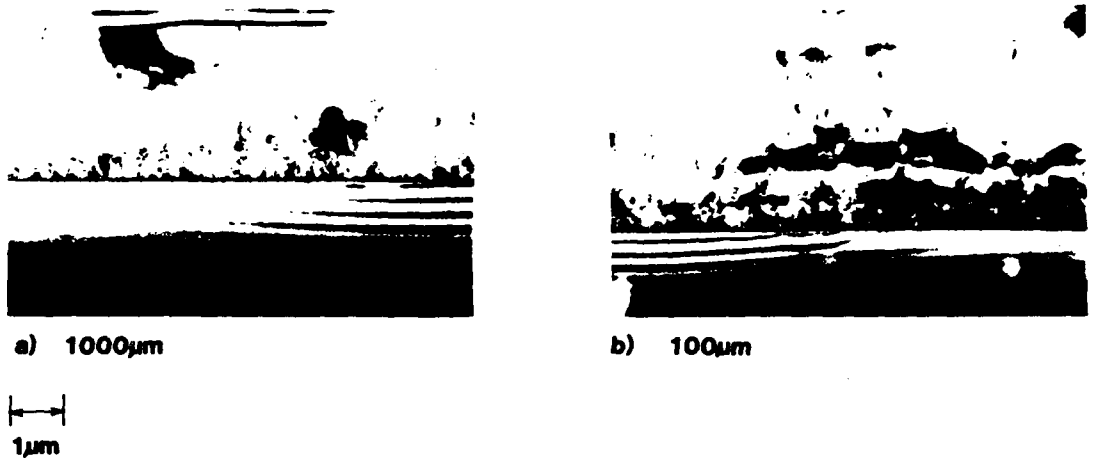

FIGURE 2-8. CROSS SECTIONAL TEM BRIGHT FIELD IMAGE OF SELECTIVE EPITAXY GaAs-on-Si BY ALE FOR TWO SQUARES: (a) 1000 micron and (b) 100 micron.

FIGURE 2-9. PLANVIEW TEM OF SELECTIVE EPITAXY GaAs-on-Si BY: (a) CONVENTIONAL MOCVD AND (b) ALE PROCESS.

2.2.3 X-ray Diffraction Topography (XRT)

There have been recent reports on stress relief associated with small dimension etch-patterned GaAs-on-Si samples measured by PL[11] and the effect of lateral confinement on defect reduction.[12] We, therefore, expect improvement in the structural properties of the selective epitaxy GaAs-on-Si films. Double crystal XRT in the reflection mode has been utilized for qualitative assessment of defect density in the selective epitaxy films as a function of square size. Figure 2-10 shows XRT, (g = 422) for the 1000, 500, 100, and 50 micron/side squares (a-d), respectively. The white-spot contrast represents the defects while the black represents the defect-free material. It is clear that as the square size decreases, the black contrast is more dominant, indicative of the improvement in the structural properties (defect reduction). The XRT analysis was performed at NCSU.

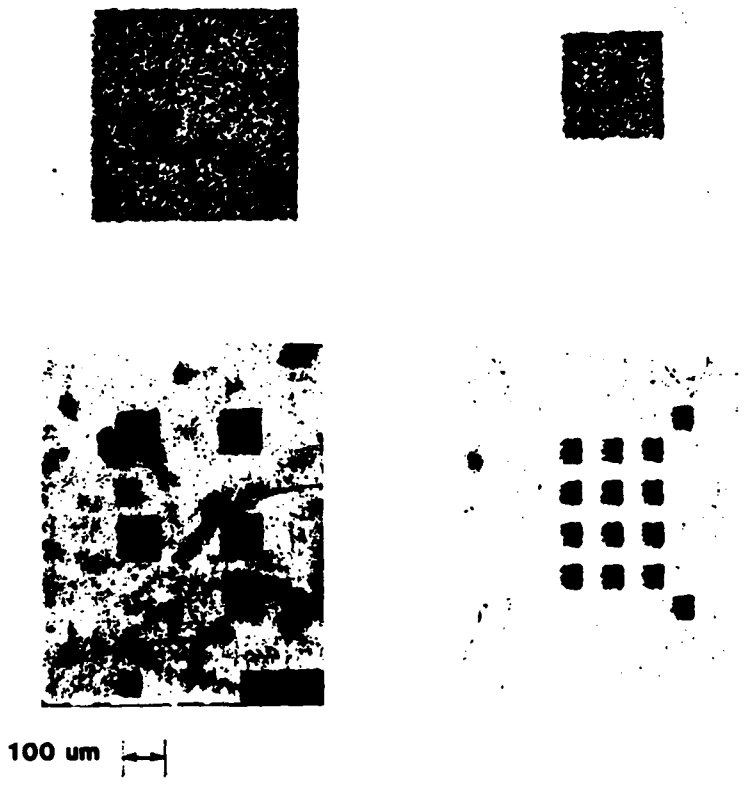

FIGURE 2-10. X-RAY TOPOGRAPHY (REFLECTION) (g = 422) OF SE GaAs-on-Si.

2.2.4 Photoluminescence (PL) Characterization

Preliminary low temperature PL (T=5K) was done at UCLA under supervision of Prof. Nancy Haegel. Figure 2-11 is a low temperature PL spectrum of a non-patterned sample (Figure 2-11a) compared to 1000 and 500 micron islands (Figure 2-11b and c, respectively). The main peak is identified as band-to-acceptor (carbon) transition. The shoulder at the high energy side is the band-to-band transition. Peak broadening is expected since the film was Si doped (5×10^{17} cm^{-3}). The relative peak intensity is approximately the same. The peak shift towards higher energy for the smaller size square indicates stress relief and the arrow in the figure represents the bandgap energy of homoepitaxial GaAs (zero stress). These results indicate the comparable optical properties of selective epitaxy and bulk GaAs-on-Si as well as an indication of stress relief for smaller squares. In Phase II, we plan to utilize a new PL mapping system recently installed at UCLA for studying the optical properties and stress relief associated with selective epitaxy.

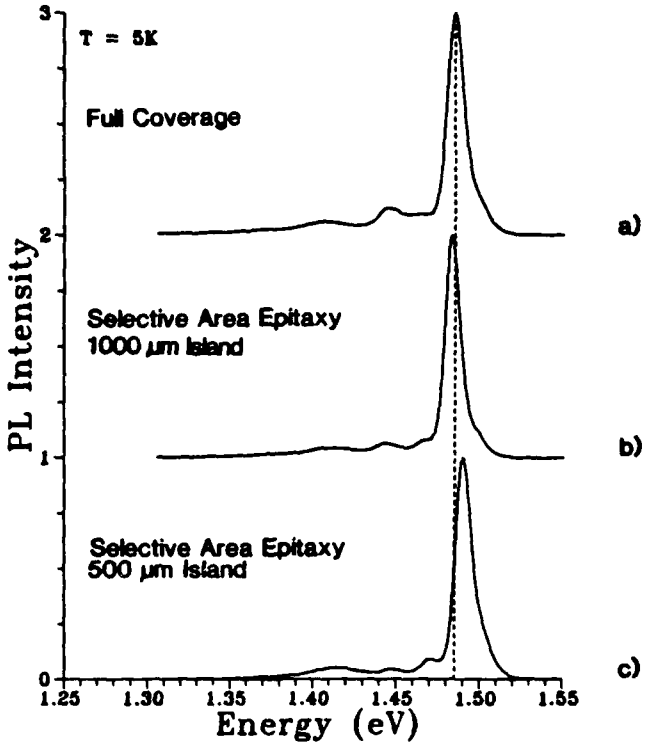

FIGURE 2-11. LOW TEMPERATURE (5K) PHOTOLUMINESCENCE CHARACTERIZATION OF GaAs-on-Si BY ALE.

2.2.5 Wafer Bow

The thermal expansion mismatch between GaAs and Si results in biaxial tensile stresses in the GaAs film as the wafer is cooled from the growth temperature (typically 600-700°C). This results in wafer bow and crack formation as mentioned earlier (Section 1.1). The present study shows that selective epitaxy can eliminate wafer bow. Figure 2-12b shows typical wafer bow as a function of GaAs epi-layer thickness for conventional unpatterned and conventional SE wafers measured using a Dektak profilometer. The 2-inch wafer (25 mils thick) bows approximately 27 micron (concave) for a 6 micron thick GaAs film. For fine line lithography, wafer bow should not exceed the range of 10 micron. The thermal expansion coefficient for SiO_2 ($0.5 \times 10^{-6} °C^{-1}$) is less than that of Si, hence the bow is convex for SiO_2-coated Si wafers and increases with the oxide thickness (Figure 2-12a) with the SiO_2 film being under biaxial compression. Hence, by balancing the tensile and compressive stress, which implies a balance between the SiO_2 thickness, the GaAs thickness, and the relative coverage of GaAs epi to oxide, a flat wafer is easily achievable. Wafer bow less than 10 microns has been achieved by both

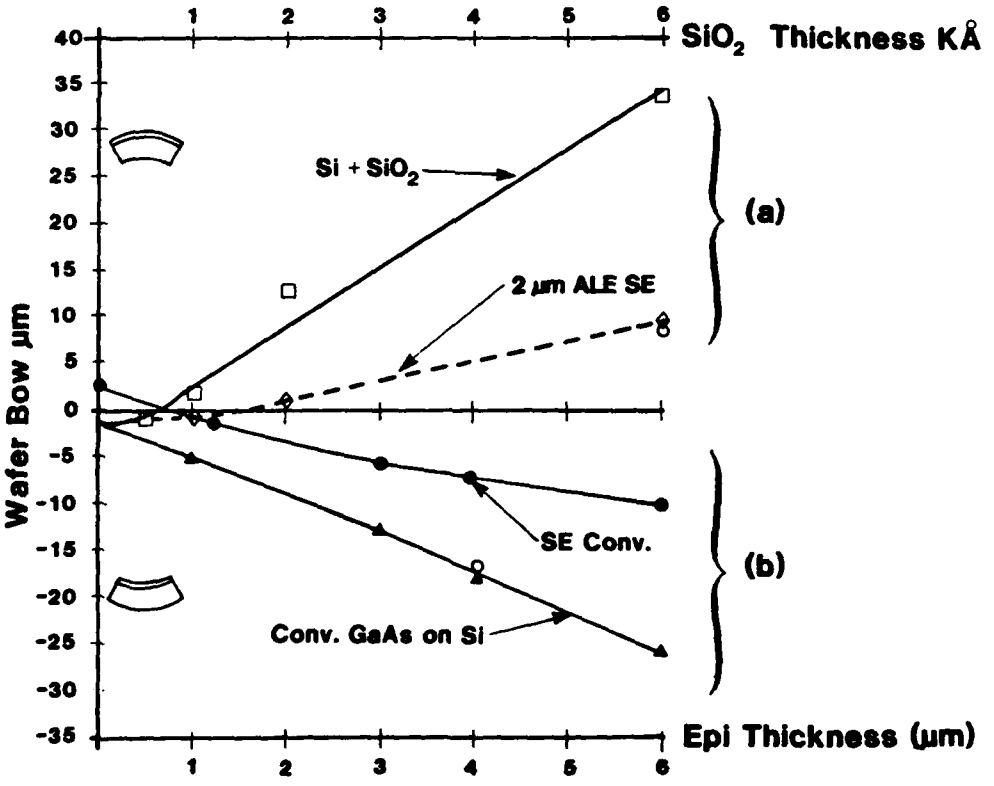

FIGURE 2-12. WAFER BOW VERSUS SiO_2 THICKNESS (a) AND GaAs THICKNESS (b).

conventional and ALE selective epitaxial techniques as shown in Figure 2-12. It is worth mentioning that the wafer bow does not change when the oxide is etched off after selective epitaxy by conventional or ALE growth. We believe that this is due to the permanent plastic deformation of the Si wafer during the cool down period from the growth temperature. This has been verified by measuring the warpage on a 4 micron thick GaAs film on an unpatterned wafer, then etching off the film completely. The wafer warpage was not affected as shown in Figure 2-12 (open circles).

Figure 2-13 shows the wafer bow for different SiO_2 thicknesses for selective epitaxy of GaAs (2 microns thick) on Si by ALE. This was done using a GCA/Tropel optical wafer flatness tester Model 9000 where each interference fringe was calibrated to 1 micron of bow. It is clear that the 1000 and 2000 angstrom-thick SiO_2-coated wafers are nearly flat while the 6000 angstrom-thick sample is bowed convexly.

FIGURE 2-13. WAFER BOW VERSUS SiO_2 THICKNESS FOR A 2 micron THICK GaAs-on-Si BY ALE.

2.2.6 Crack Density

Representative samples with different oxide thicknesses were used for crack-density measurements. A 4-micron-thick GaAs film was grown on the selectively-patterned wafers and an unpatterned wafer side-by-side using the conventional and ALE techniques. Cracks in the films were delineated using $NH_3OH:H_2O_2:H_2O$ etch and the density was measured using optical microscopy. For the unpatterned wafers there was no significant difference in the crack separation between the conventional and ALE deposition processes. Their average crack separation was ~110 microns. This is expected since the deposition temperature after nucleation was 675°C. The selective-epitaxy wafers showed a significant reduction in the crack density irrespective of the oxide film thickness or the deposition technique. Figure 2-14a shows the percentage of islands that are completely free of cracks versus island size. Islands that are 100 microns or less were found to be completely crack-free. As the islands size increased, the percentage of crack-free islands decreased. Figure 2-14b shows the average crack separation

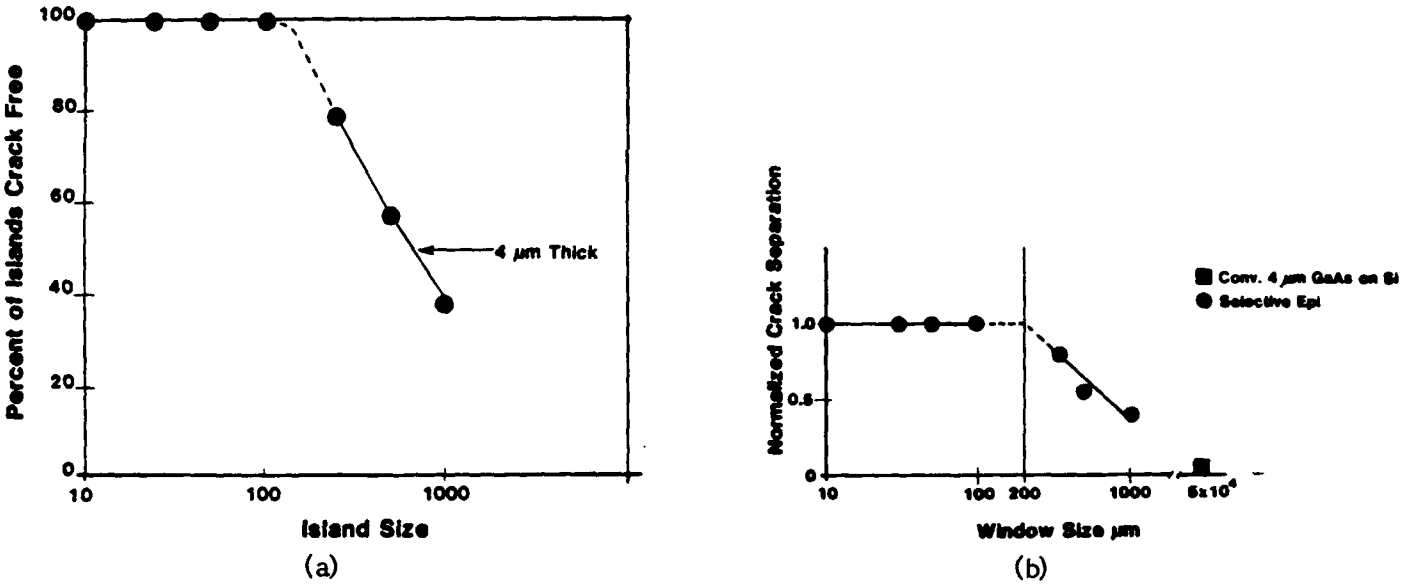

FIGURE 2-14. a) PERCENT CRACK-FREE ISLANDS AS A FUNCTION OF ISLAND SIZE.
b) NORMALIZED AVERAGE CRACK SEPARATION AS A FUNCTION OF ISLAND SIZE.

normalized to the island size for the different island sizes. Therefore, islands of 100 microns or less should show a normalized crack-separation value of 1.0. Although 40% of the largest islands (1000 microns) were crack-free, the average crack separation for the defective ones was found to be nearly three to four times that of the unpatterned wafers. Also by interpolation one can predict that islands up to 200 microns/side can be crack-free. These results are very encouraging and add to our confidence for the goals set for the Phase II program.

2.2.7 Selective Oxide Removal and Thickness Profile

The thickness profile of the selectively deposited films was measured using a micro-stylus (α-step Tencor) after the selective removal of SiO_2 and GaAs (poly).

1. **Selective Removal of SiO_2 and the Poly GaAs**

   For the case of selective epitaxy by ALE the procedure is simple, since there is no poly-growth on the oxide. A wafer dip in buffered HF for three seconds was sufficient to remove the oxide. On the other hand, for the case of selective epitaxy by conventional MOCVD two procedures were successfully employed:

   a. The formation of a continuous polycrystalline film makes it difficult for the buffered HF to attack the SiO_2 due to the small cross section exposed and the formation of stable bubbles that slow down the etching process. This problem was resolved by dipping the wafer for longer periods of time (20 to 30 minutes) in a buffered HF bath that is constantly agitated and contains a defrothing reagent.

   b. The second approach comprised photolithographically masking the GaAs islands using photoresist and etching the poly-GaAs with an isotropic etchant $HCl:H_2O_2:H_2O$ for five seconds, then stripping the resist. It is critical to etch for very short times since the etchant may attack existing cracks. Since the polycrystalline GaAs film has a high resistivity (10^5 ohm-cm) it is convenient to use it as an isolating film for some device applications.

2. **Thickness Profile Measurements**

   Figure 2-15 shows the thickness profiles for the selectively deposited films as a function of island size and deposition technique. The thickness profile for selective-epitaxy GaAs-on-Si by conventional MOCVD (Figure 2-15a) shows significant edge growth which could be a source of problems for device fabrication and metallization. As mentioned earlier (Section 2.2.1), this is caused by the surface migration (diffusion) of reactants resulting in a pile-up at the island edge that is determined by

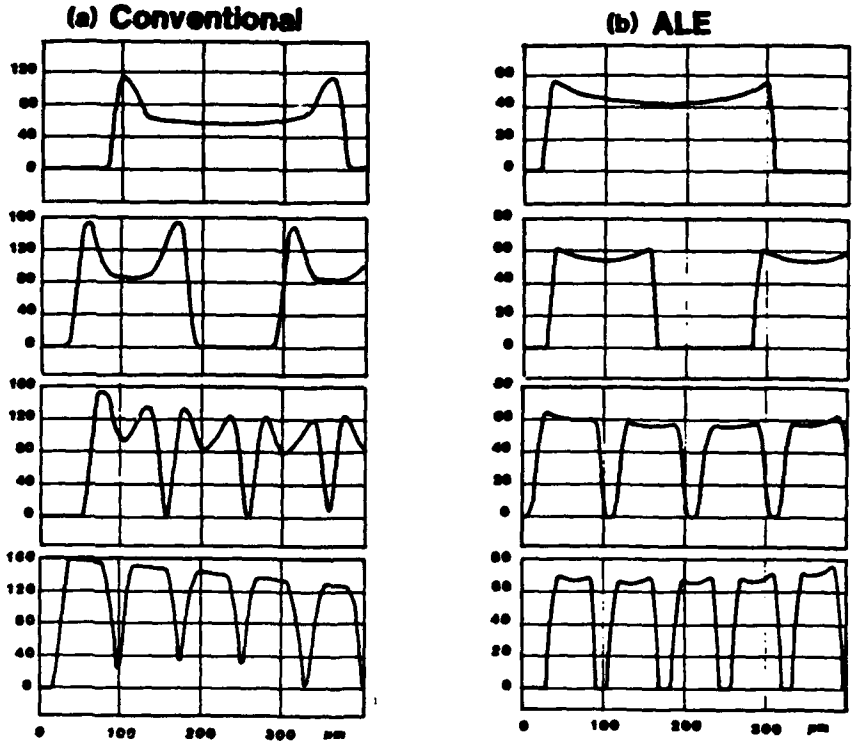

FIGURE 2-15. THICKNESS PROFILE COMPARISON FOR SELECTIVE EPITAXY OF GaAs-on-Si.

the SDL of the reactants and the relative oxide-to-window area ratio. It is energetically favorable for reactants deposited on the oxide areas directly adjacent to the islands to migrate to these islands. The distance they can migrate is determined by the deposition temperature (T), pressure (P), and the mole fraction of the reactants (V/III ratio). Judging by the thickness profile measurements, this length is approximately 50 micron. For small islands where the edge growth humps overlap, a flat top profile is achieved. A similar problem has been addressed for selective homoepitaxial growth of GaAs where the edge growth was suppressed by forming a continuous polycrystalline film on the oxide. This was achievable by deposition at lower temperatures and high V/III ratios. We will address this problem for selective epitaxy of GaAs-on-Si in Phase II.

Figure 2-15b shows the thickness profile achieved using the ALE process where the edge growth problem is less severe and nearly flat top islands are achievable. This is believed to be due to the longer SDL at lower deposition pressure (76 torr). We estimate the diffusion length at the employed growth conditions (Section 2.1.3) to be roughly 250 microns. In order to completely eliminate the edge growth and the island size dependence of the growth rate problems two approaches can be employed: (a) the first approach is to deposit at lower pressures (10 to 30 torr) and higher temperatures (700 to 750°C). This will prevent

nucleation on the oxide and will drastically increase the surface diffusion length. In addition it is also compatible with AlGaAs growth. Kamon et al. (Japan) recently demonstrated that LP MOCVD (10 torr) suppresses poly-growth on the oxide, edge growth, and growth-rate dependence of island size for selective epitaxy on GaAs.[20] Spire reactors can routinely operate at pressures as low as 15 torr. (b) The second approach is to employ ALE for the selective epitaxy of the entire structure rather than only for nucleation. Since only one monolayer can be deposited per ALE cycle,[24] the deposition will not be affected by surface migration and will be independent of the island size.

The facet formed during selective-epitaxy by the ALE process for the (011) and (01$\bar{1}$) cleavage planes have been identified (Figure 2-16). The facet formation on the two orthogonal planes are similar to those observed for selective epitaxy on GaAs.[2-19b]

3. Growth Rate/Island Size Dependence

Figure 2-17 shows the growth rate on the patterned wafers compared to that on unpatterned wafers. Note that the nominal growth rate has been adjusted to be similar for conventional MOCVD and LP MOCVD. The thicknesses were measured by a Tencor microstylus and the values reported were measured at the island center. The factors that affect the growth rate in the islands include the reactant flux (since the deposition is mass transport controlled), the nucleation/desorption rate on the oxide, the surface migration of the reactants and the relative areas of the island and the oxide surrounding it. Note that the oxide area that needs to be considered is only that within the SDL zone. Therefore conventional SE is expected to have a slower growth rate and a weaker island size dependence than that of the L.P. MOCVD technique. It is estimated that roughly 30% of the surface migrating reactants are incorporated and the rest desorbs. This is a rough estimation based on measurements of thickness profiles and the poly-GaAs-depleted area on the wafer.

3.0 SUMMARY

The results of Phase I program may be summarized as follows:

- Selective epitaxy of high quality GaAs-on-Si through openings patterned in SiO_2 mask has been successfully demonstrated by MOCVD.
- Selective deposition by the conventional GaAs-on-Si process resulted in single crystalline films inside the patterned openings and polycrystalline growth on the SiO_2 mask. The surface morphology and structural properties of the selectively deposited films are comparable to current state-of-the-art films deposited on unpatterned wafers.

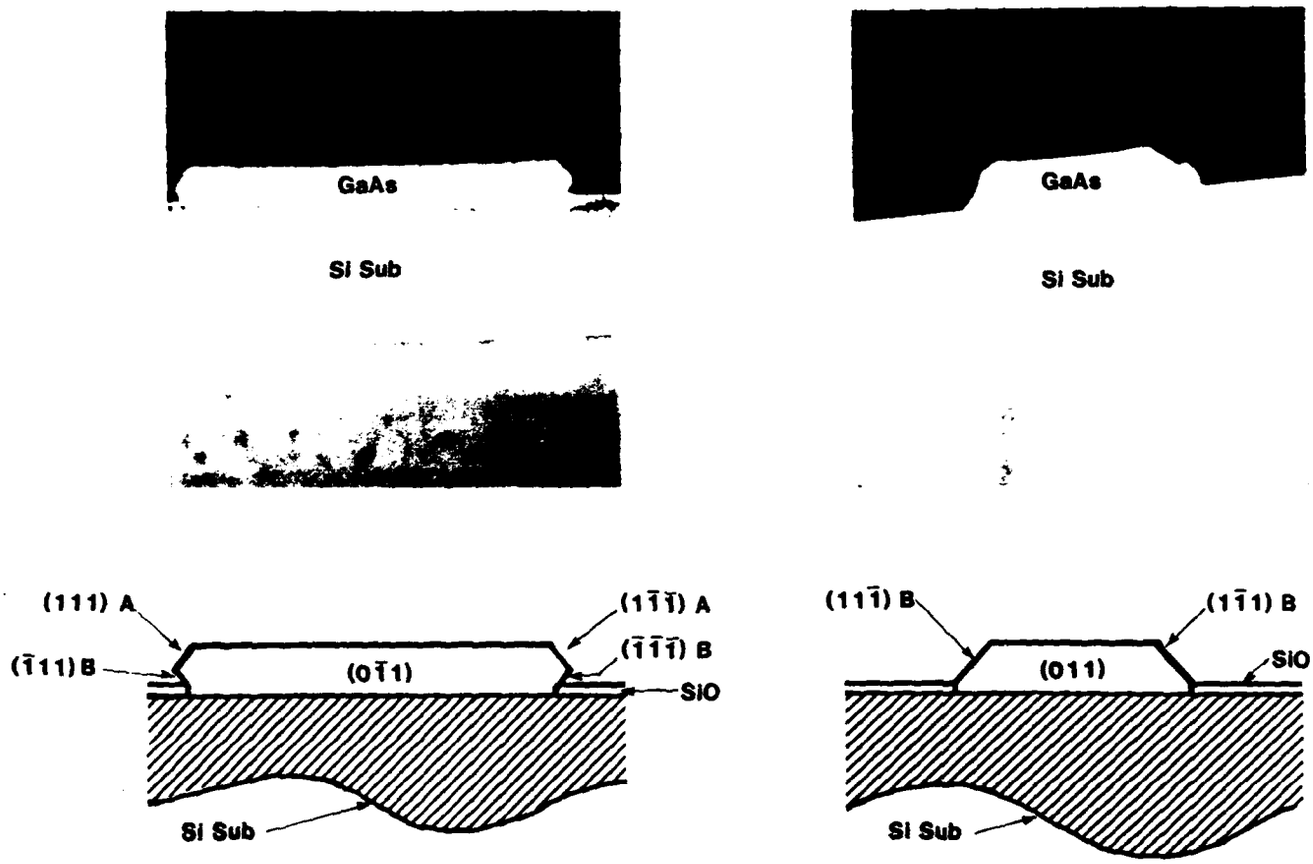

FIGURE 2-16. FACET FORMATION FOR SELECTIVE EPITAXY OF GaAs-on-Si: (a) (011) CLEAVAGE PLANE - (b) (011).

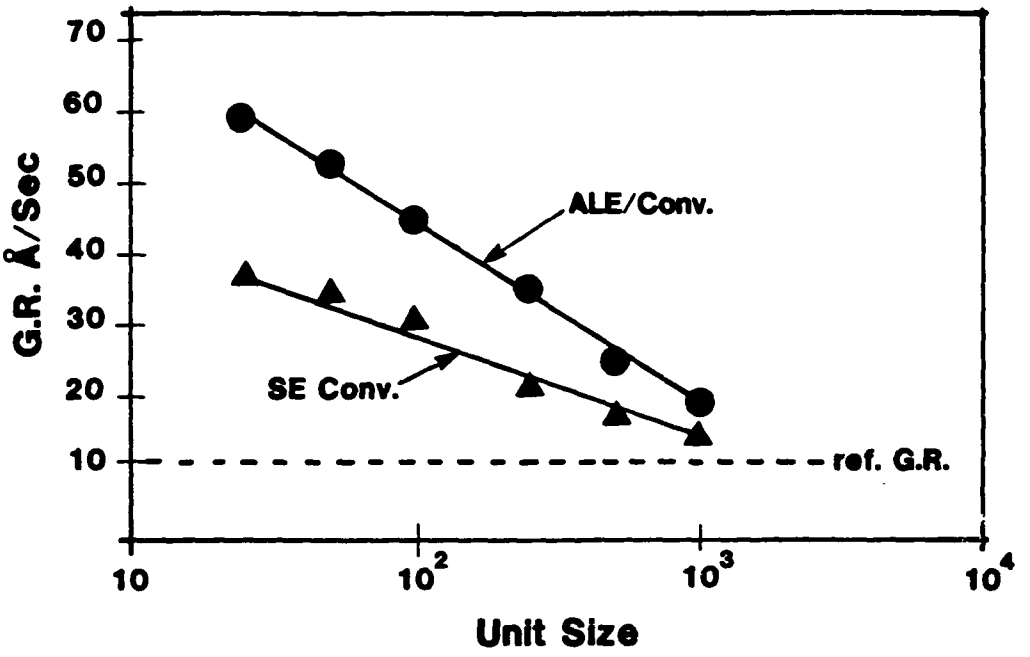

FIGURE 2-17. GROWTH RATE FOR DIFFERENT ISLAND SIZES.

- A new technique for depositing GaAs-on-Si by ALE has been introduced. Structural characterization (TEM) show that the ALE process can improve the quality of GaAs on Si.

- Selective epitaxy of GaAs-on-Si by the ALE process resulted in selective deposition of single crystalline films in the patterned openings and the suppression of polygrowth on the oxide mask. The surface morphology of the selectively deposited films are comparable to ALE deposition on unpatterned wafers.

- Selective epitaxy has been found effective in reducing wafer bow for GaAs-on-Si films as thick as 6 microns to levels suitable for high resolution photolithography. SE is potentially capable of eliminating wafer bow by carefully selecting the GaAs film thickness, the SiO_2 mask thickness, and the relative coverage of GaAs epi to oxide areas.

- Significant reduction in the film crack density has been achieved using SE-Islands with dimensions 100 microns/side or less were found completely crack-free. As the island size increased the percentage of crack-free islands decreased. The average crack separation for the largest size islands (1000 microns/side) was found to be three to four times that of the unpatterned wafers with comparable thicknesses.

- X-ray diffraction topography showed that the quality of the deposited films improved with reducing the island size.

- The optical properties of the selectively deposited films, measured by low temperature PL, were found comparable to those deposited on unpatterned wafers. Evidence of stress relief has been observed for smaller island sizes.

4.0 PHASE I CONCLUSIONS

The feasibility of selectively depositing GaAs-on-Si through openings patterned in SiO_2 has clearly been demonstrated. Preliminary results show that this technique may be effective in eliminating wafer bow, reducing film cracking, and possibly improving the quality of GaAs-on-Si for MGS devices. We have also introduced a new technique for depositing GaAs-on-Si by ALE. It is believed that these techniques when optimized can lead to the selective deposition of device quality films that are crack-free on perfectly flat wafers. Many parameters remain to be studied and a great deal of optimization in the growth procedure is possible and necessary. The proposed Phase II program will address the optimization issues and seek to demonstrate the growth of superior quality films suitable for MGS devices.

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