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Technical Document 1532
April 1989

DARPA Review on EHF Devices

Defense Advanced Research Projects Agency Joint Contractor Review

Held at Naval Ocean Systems Center
San Diego, California 92152-5000 on
24–25 January 1989

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NAVAL OCEAN SYSTEMS CENTER
San Diego, California 92152-5000

E. G. SCHWEIZER, CAPT, USN
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ADMINISTRATIVE INFORMATION

This document is a compilation of the papers delivered at the Defense Advanced Research Projects Agency (DARPA) Review of EHF Devices. This review was held at the Naval Ocean Systems Center, San Diego, California, on 24 and 25 January 1989.

Released by
L. J. Messick
Material and Device
Technology Branch

Under authority of
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FS

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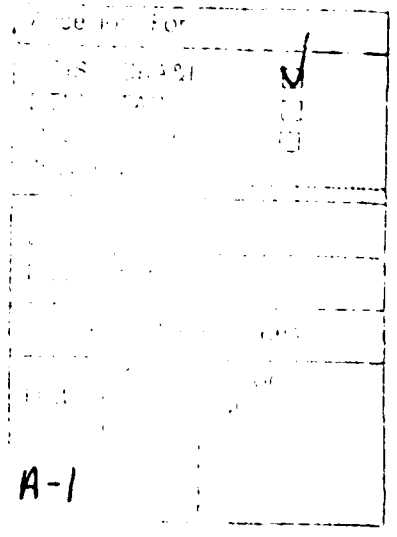

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AGENDA

DARPA REVIEW ON EHF DEVICES

NOSC Meeting Coordinator
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Louis Messick
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TUESDAY, 24 JANUARY

0745	Late Registration at the LaJolla Village Inn, Torry & Sorrento Rooms	
0815	Introductory Remarks	JAMES MURPHY DARPA
0830	Requirements for 94 GHz 3-Terminal Circuit Technology	JOHN ARMATA Army LABCOM
0910	Ballistic Transport in the Vertical and Laterial Dimension s	MORDEHI HEIBLUM IBM
0950	Break	
1010	Permeable Base and Vertical Transistors	MARK HOLLIS MIT Lincoln Lab
1050	Transport Considerations in EHF Devices	HAL GRUBIN Scientific Research Associates
1130	GaAlAs/GaAs HBTs for mm-Wave Applications	PETER ASBECK Rockwell Interna'l
1215	Lunch in University Room	
1330	Heterojunction Power FET Technology	BUMAN KIM Texas Instruments
1410	Resonant Tunnelling Structures	JAMES HARRIS Stanford University
1450	Array Applications	JAMES BALLINGAL General Electric
1530	Break	
1550	mm-Wave Phased Array Antennas	CHARLES LIECHTI Rockwell Interna'l
1630	Round Table Discussion: Promising Directions in mm-Wave Device Technology for Phased Array Applications	
1830	Buffet Dinner	

WEDNESDAY, 25 JANUARY

0800	Materials Engineering for Ballistic Transport and Drift Devices	S. KRISHNAMURPHY SRI International
0840	mm-Wave Performance of InGaAs/InAlAs HEMT	UMESH MISHRA North Carolina State University
0920	Break	
0940	Measurement of Response of High Speed Tunneling Devices	TOM MCGILL Cal. Tech.
1020	EHF HBT Development	B. BAYRAKTAROGLU Texas Instruments
1100	On Wafer Characterization of High Speed Circuits	DAVID BLOOM Stanford University
1140	End Review	

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Overview of Millimeter Wave Components and Systems for Army Military Applications

and

Requirements for 94 GHz Phased Arrays

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and

Thomas Koscica

U.S. Army Electronics Technology & Devices Laboratory
Ft. Monmouth, NJ

US ARMY
LABORATORY COMMAND

ELECTRONICS TECHNOLOGY and DEVICES LABORATORY

OVERVIEW OF MILLIMETER WAVE COMPONENTS AND SYSTEMS FOR ARMY MILITARY APPLICATIONS AND REQUIREMENTS FOR 94 GHz PHASED ARRAYS

JOHN F. ARMATA, JR.

and

THOMAS KOSCICA

U.S. ARMY ELECTRONICS TECHNOLOGY AND DEVICES LABORATORY
FORT MONMOUTH, NEW JERSEY

JCOV#52

AGENDA

US ARMY
LABORATORY COMMAND

ELECTRONICS TECHNOLOGY and DEVICES LABORATORY

RADAR COMPONENTS DEVELOPED UNDER FORT MONMOUTH SPONSORSHIP

6 REVIEW OF SOME SYSTEM APPLICATIONS AND REQUIREMENTS

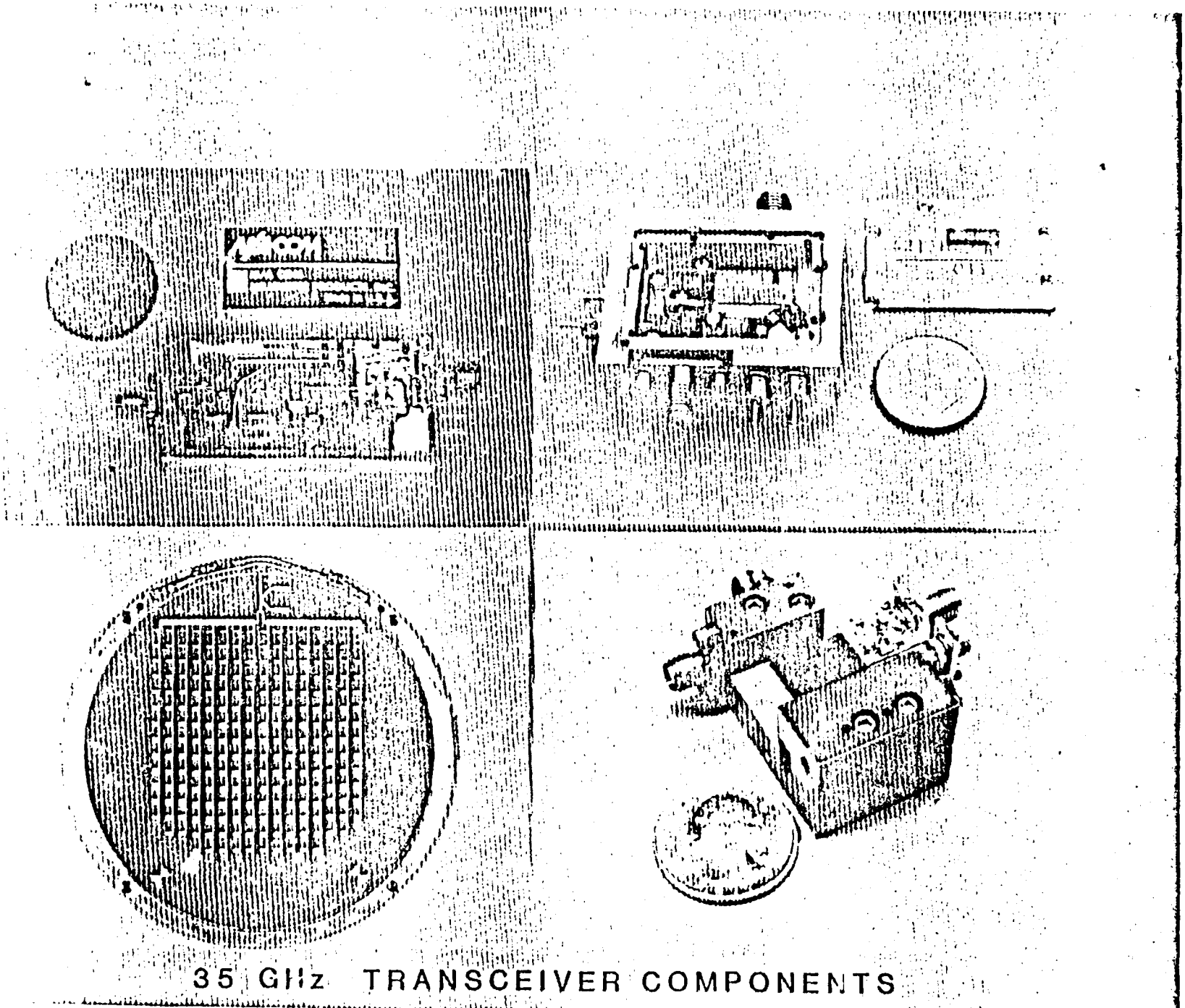
SADARM

SCOTT

MLRS-TGW

ACTIVE TANK DEFENSE

AGENDA\1-20-89\EPS\196\#52\SP



35 GHz TRANSCEIVER COMPONENTS

Ka-BAND MICROSTRIP VCO CIRCUIT

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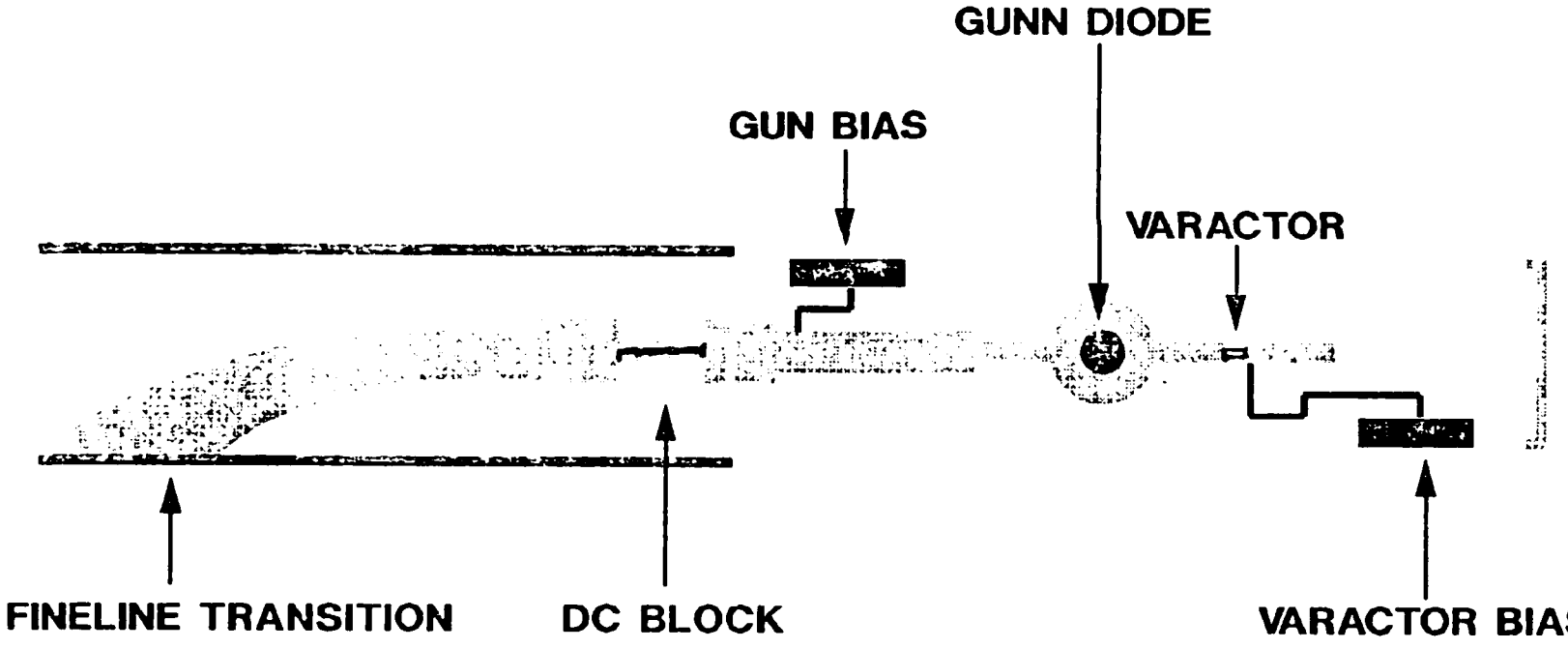
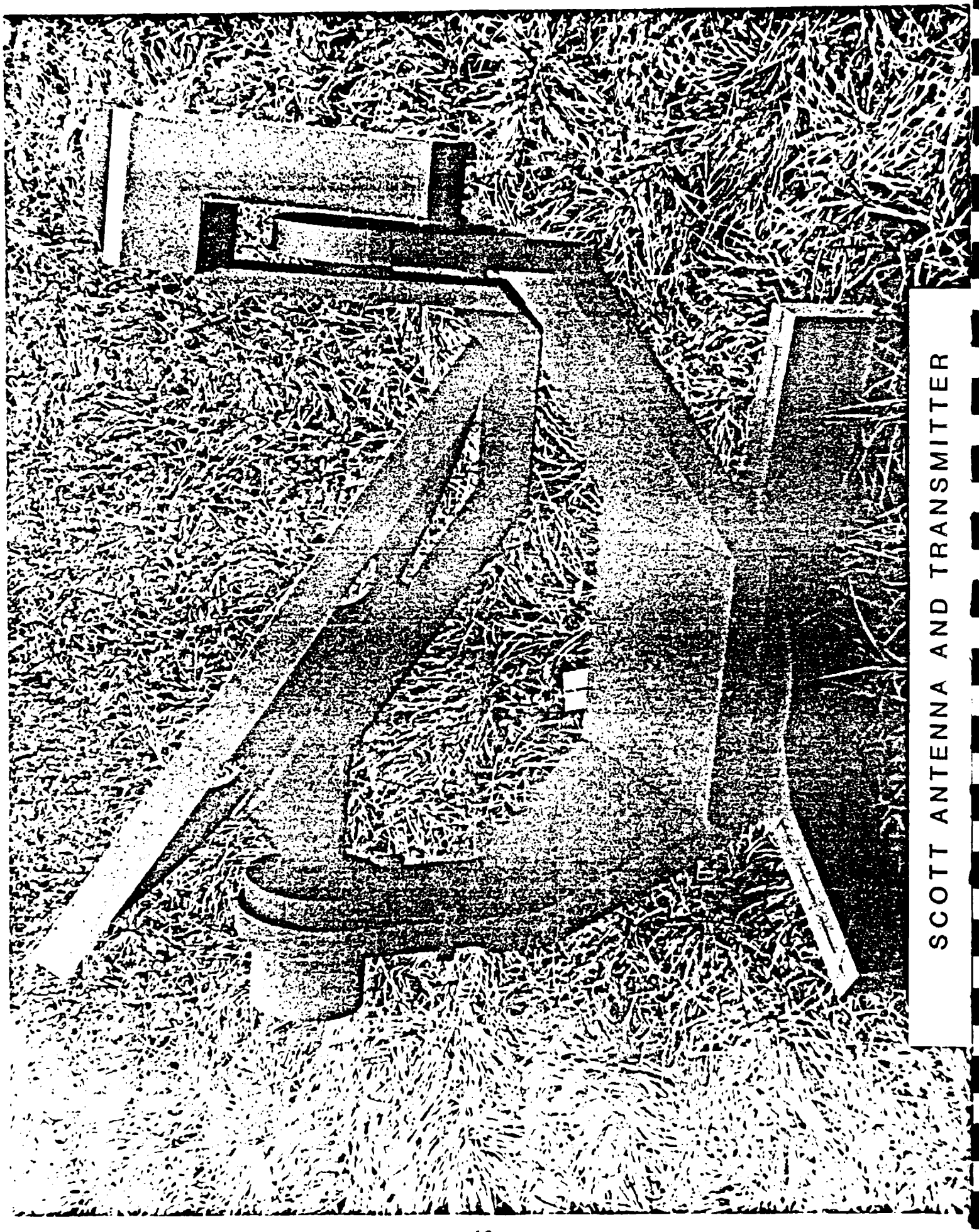
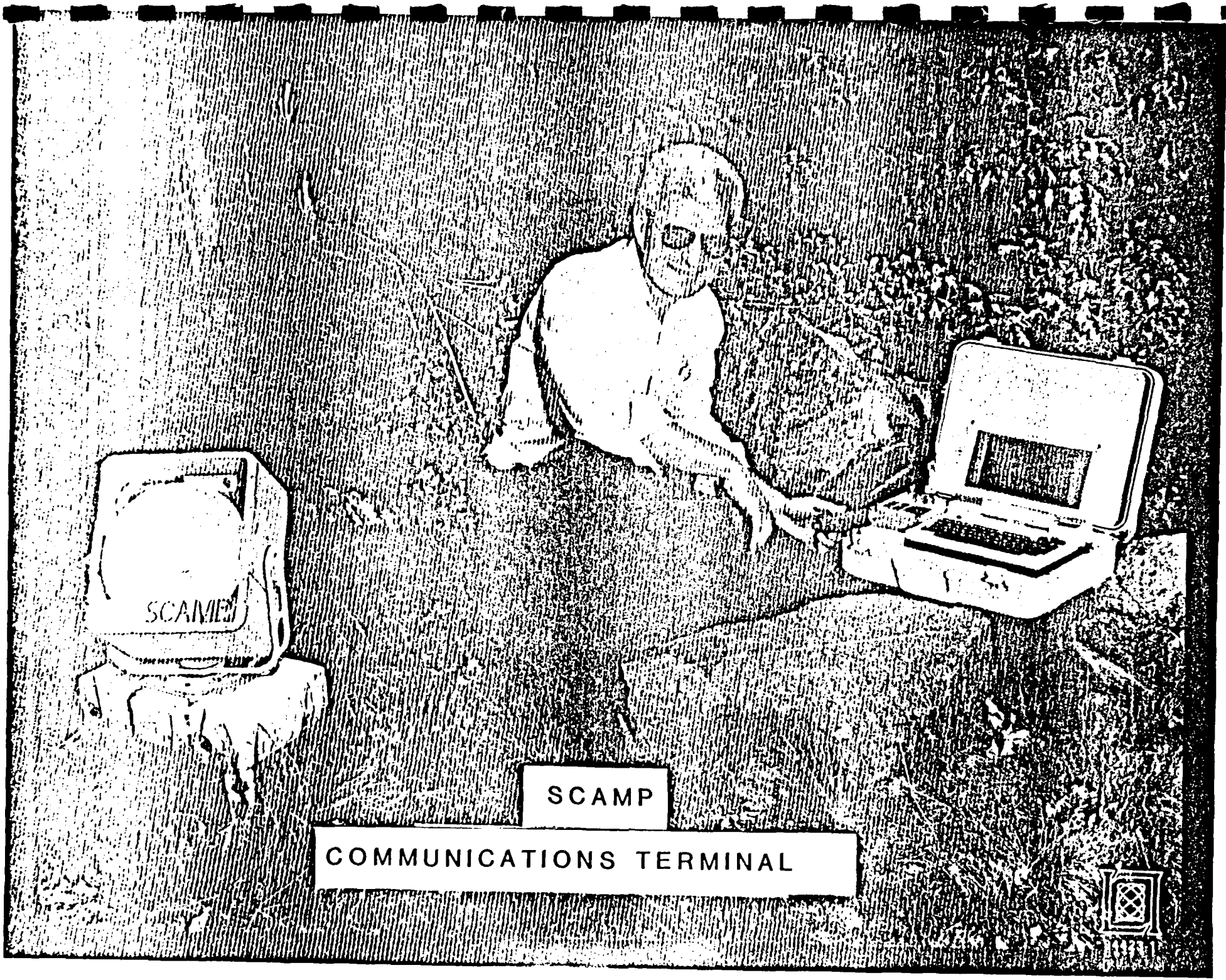
ELECTRONICS TECHNOLOGY and DEVICES LABORATORY



KaBANDMVCO\1-20-89\EPS\196\e52\SP

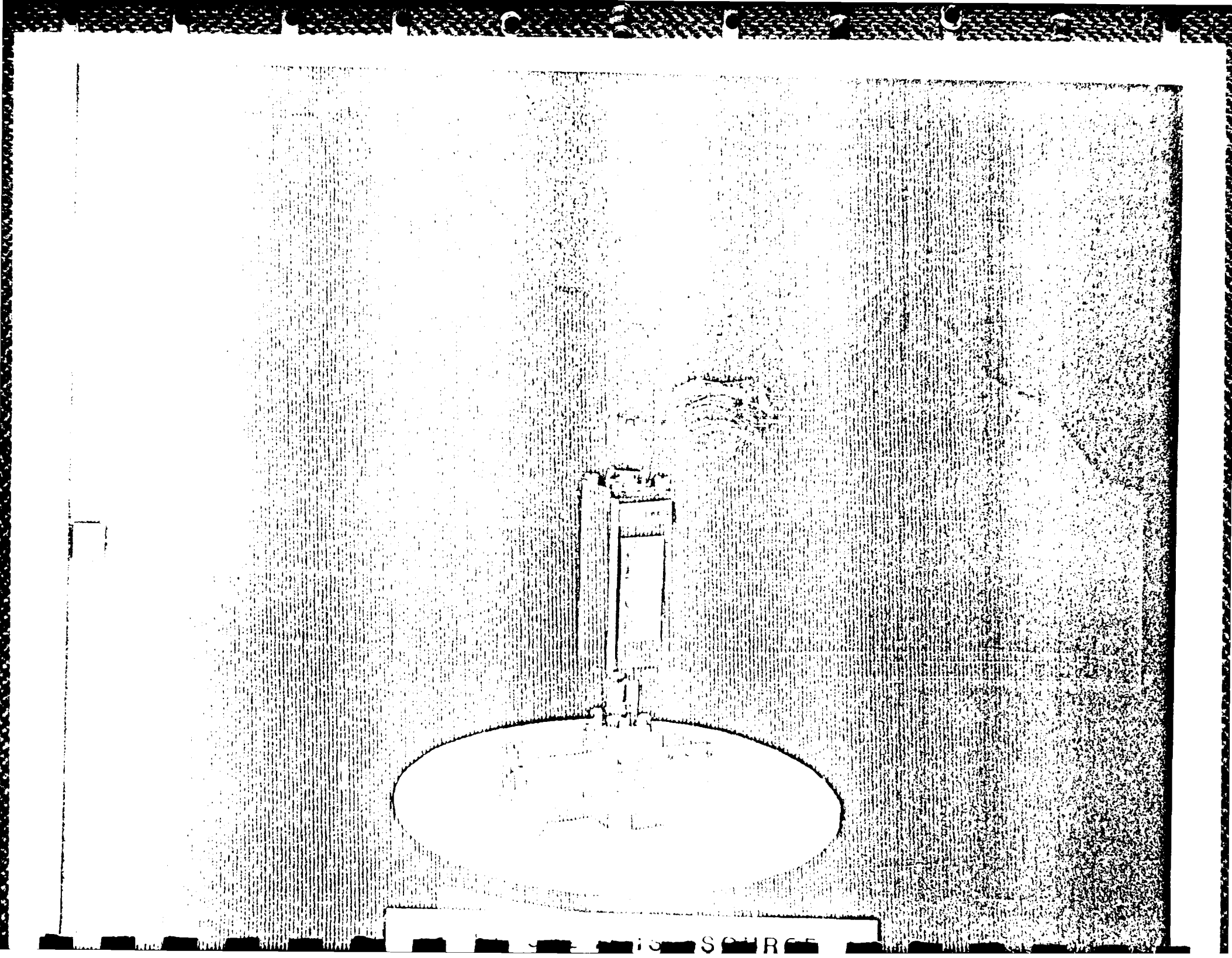


SCOTT ANTENNA AND TRANSMITTER


SCAMP
COMMUNICATIONS TERMINAL

44 GHZ HIGH POWER SOLID STATE TRANSMITTER

1
2
3
3
2
1



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ENR (DB) VS. FREQUENCY

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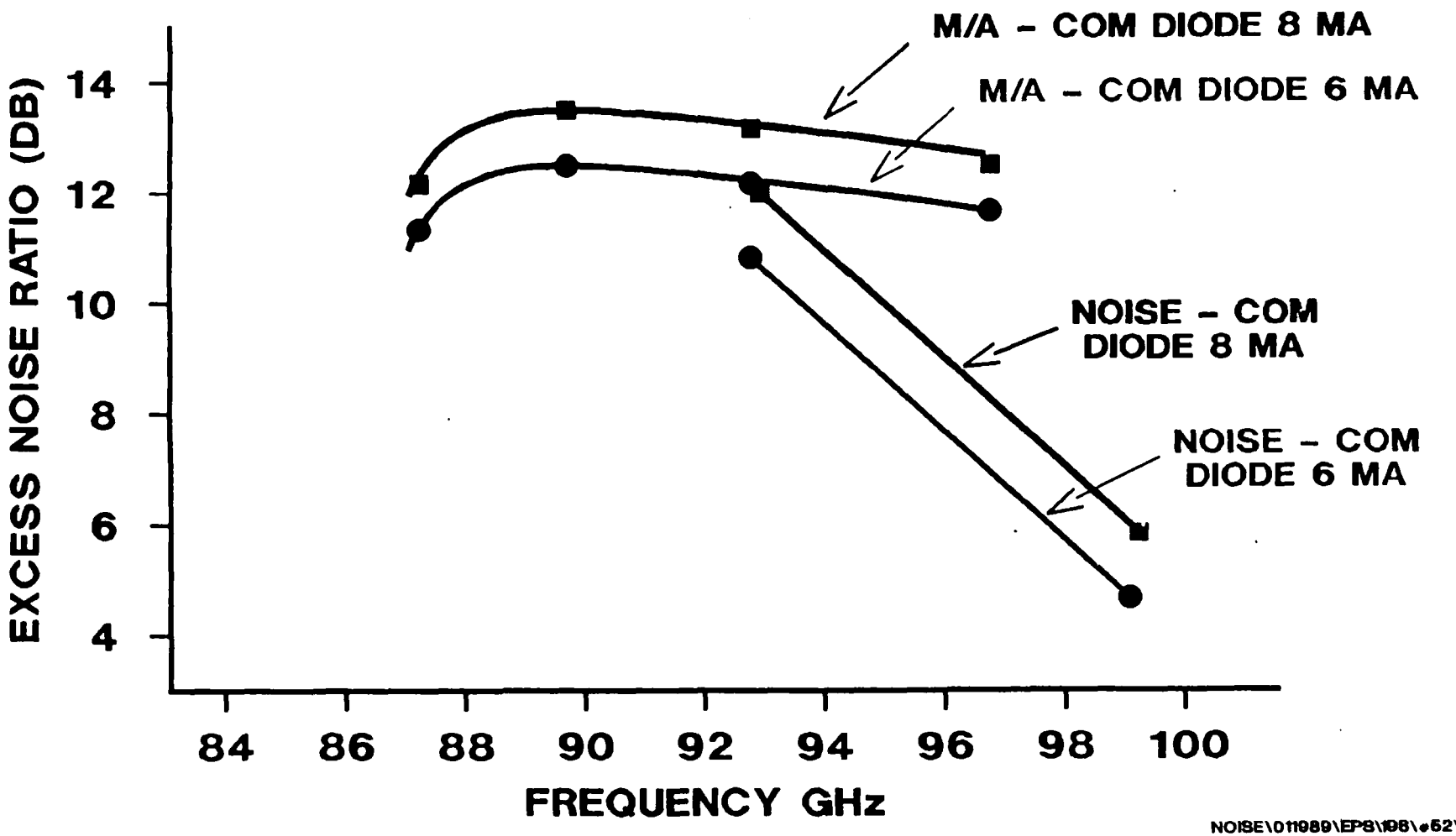
ELECTRONICS TECHNOLOGY and DEVICES LABORATORY



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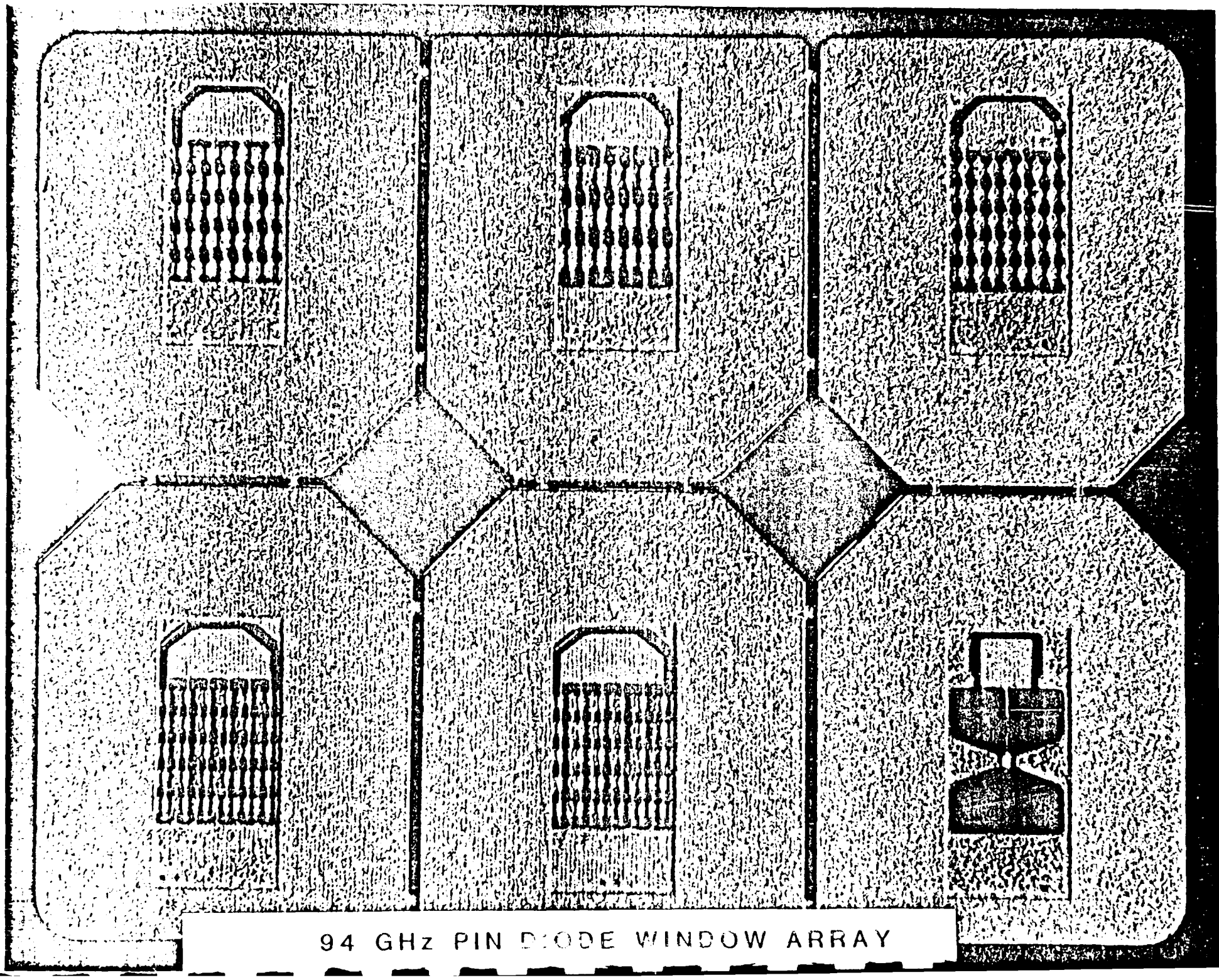
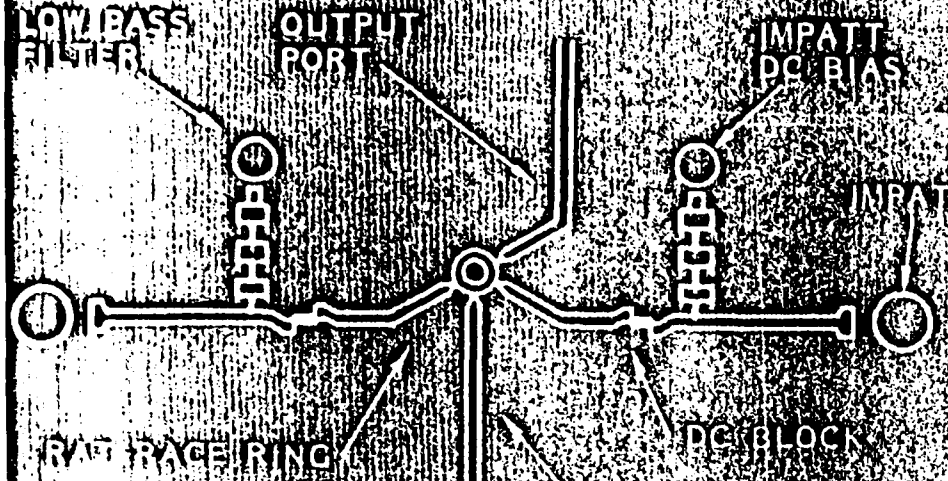
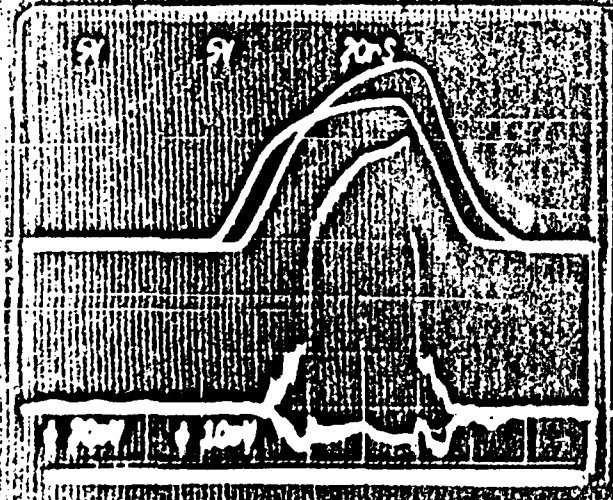


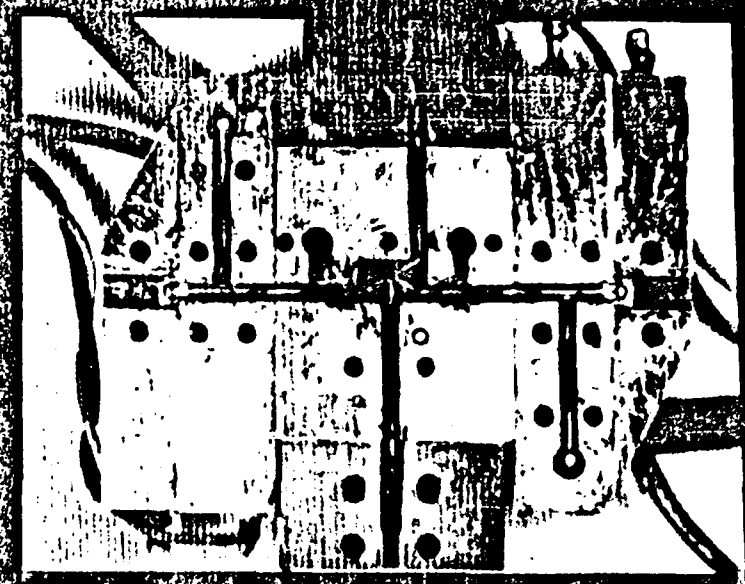
94 GHz PIN DIODE WINDOW ARRAY

W-Band MIC High Power Pulse Combiner



Transmission Type Rat-Race Combiner





MIC Short Pulse Rat-Race Combiner

FEATURES

- RAT-RACE RING HYBRID POWER COMBINER
- 20 W PEAK PULSED POWER NEAR 96 GHz
- 150 MHz FREQUENCY CHIRPING
- OVER 80% COMBINING EFFICIENCY
- ISOLATION BETWEEN INPUT AND OUTPUT PORTS IS ≥ 18 dB
- MICROSTRIP CONSTRUCTION LENDS ITSELF TO SMALL SIZE, LOW COST, AND COMPATIBILITY WITH MONOLITHIC IMPLEMENTATION

PROBLEMS WITH IMPATT AMPLIFIERS FOR 44 GHz

US ARMY
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ELECTRONICS TECHNOLOGY and DEVICES LABORATORY

1. COMPLEX CIRCUITRY

2. LARGE PHYSICAL SIZE

3. LOW EFFICIENCY (APPROXIMATELY 5-6%)

4. DIODE SELECTION PROBLEMS

5. IMPATTs OPERATE AT HIGH TEMPERATURES (RELIABILITY)

6. COSTLY

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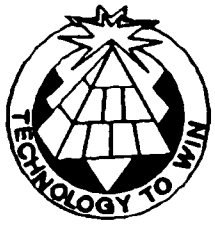

PROBLEMS WITH PRESENT MLRS-TGW RADAR

US ARMY
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ELECTRONICS TECHNOLOGY and DEVICES LABORATORY

POWER, GIMBAL ANTENNA

WAVEGUIDE AND MICROSTRIP LOSS

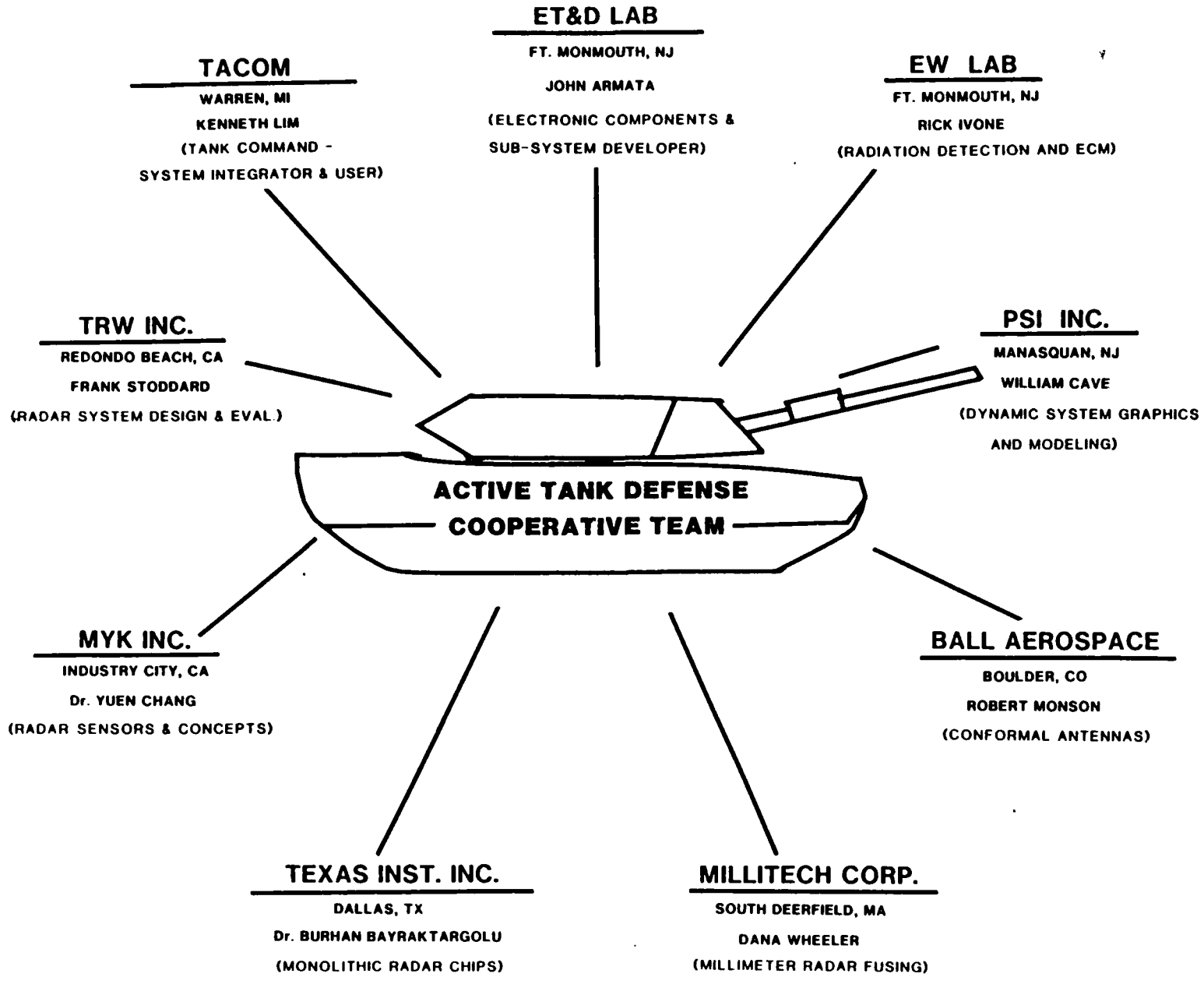
21

LOSSY COMPARATOR, FREQUENCY STABILITY

HIGH COST, HIGH NOISE FIGURE

LARGE VOLUME REQUIREMENTS

PWP\1-20-89\EPS\196\#52\SP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TRW INC.
REDONDO BEACH, CA
FRANK STODDARD
(RADAR SYSTEM DESIGN & EVAL.)
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MANASQUAN, NJ
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ACTIVE TANK DEFENSE
COOPERATIVE TEAM
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(RADAR SENSORS & CONCEPTS)
BALL AEROSPACE
BOULDER, CO
ROBERT MONSON
(CONFORMAL ANTENNAS)
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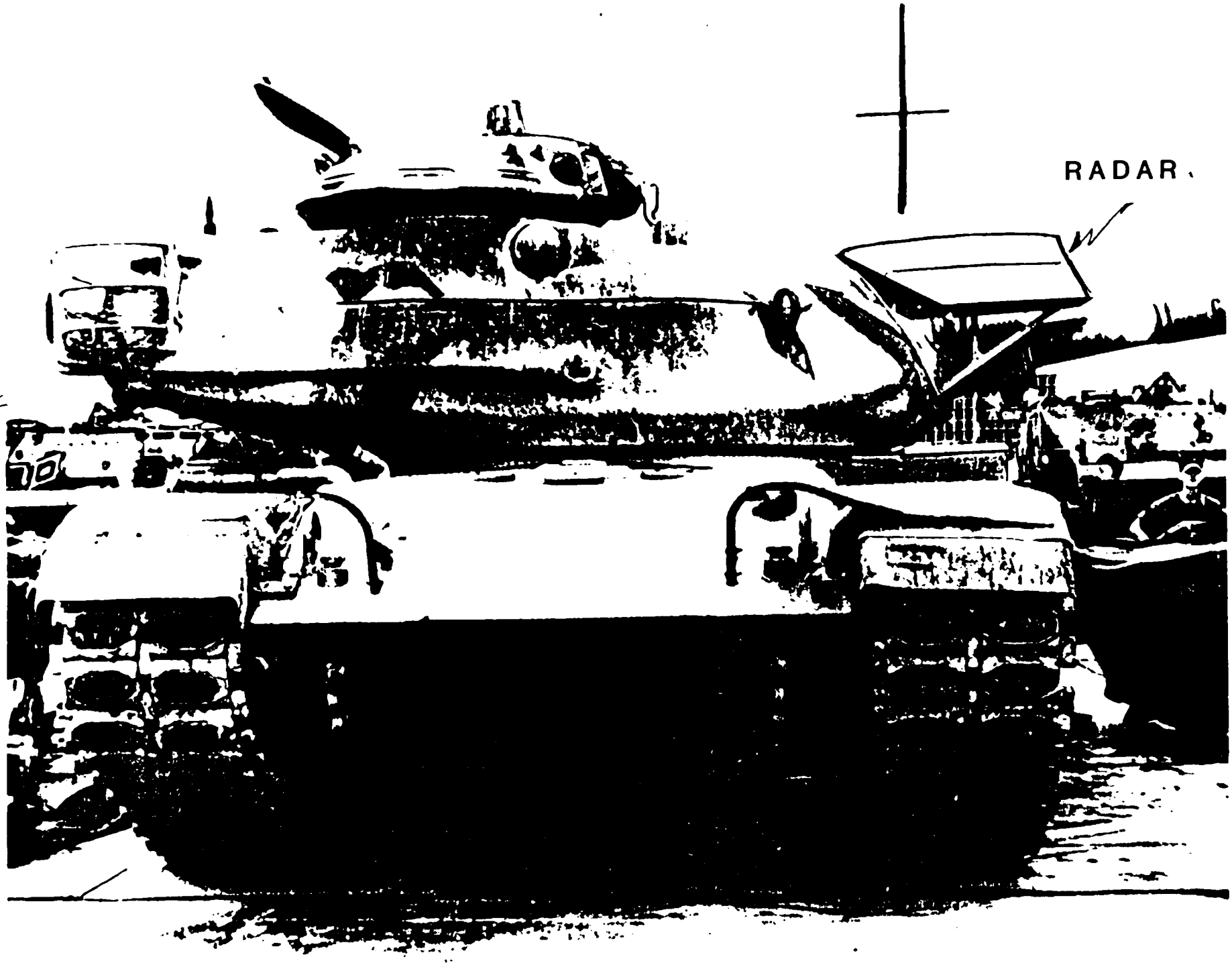
DALLAS, TX
Dr. BURHAN BAYRAKTARGOLU
(MONOLITHIC RADAR CHIPS)
MILLITECH CORP.
SOUTH DEERFIELD, MA
DANA WHEELER
(MILLIMETER RADAR FUSING)

▲ *One countermeasure, reactive armour, reduces penetration by exploding outward when hit*



EARLY VERSION OF MMW TARGET ACQUISITION RADAR FOR TANKS

SAMPLE TANK THREATS

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ELECTRONICS TECHNOLOGY and DEVICES LABORATORY

TYPE	SAMPLE SYSTEM	RADAR CROSS-SECTION	SPEED
OVERHEAD ATTACK	SADARM, MERLIN	MEDIUM	LOW
GUIDED MISSILE	TOW	LARGE	MEDIUM
HOMING MISSILE	MLRS, HELLFIRE	MEDIUM	MEDIUM
HEAT SEEKING MISSILE	HELLFIRE, STINGER	MEDIUM	MEDIUM
HEAT ROUND	GUN FIRED (105-135 MM)	SMALL	HIGH
LONG ROD PENETRATOR	GUN FIRED (105-135 MM)	V. SMALL	V. HIGH

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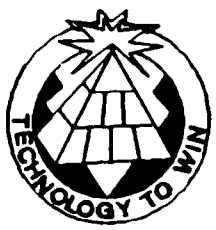


WHAT MAKES SENSE

US ARMY
LABORATORY COMMAND

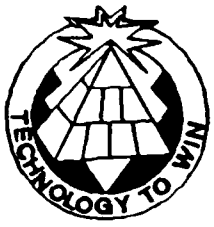
ELECTRONICS TECHNOLOGY and DEVICES LABORATORY

SURVIVABILITY OF TANK AND ARMORED PERSONNEL CARRIER CAN NO LONGER DEPEND ON HEAVIER COMPLEX ARMOR.

PROBLEMS: COST, WEIGHT, LOSS OF SPEED, FUEL REQUIREMENTS, ETC.

SOLUTION: REQUIRES NEW LEVEL OF ELECTRONIC TECHNOLOGY TO PROVIDE THE DEGREE OF PROTECTION REQUIRED IN BATTLEFIELD OF THE FUTURE.

WMS\1-20-89\EPS\196\#52\BP



MAJOR TANK DEFENSE PHASED ARRAY REQUIREMENTS

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ELECTRONICS TECHNOLOGY and DEVICES LABORATORY

- HIGH RESOLUTION
- MULTIPLE BEAM
- HEMISPHERICAL COVERAGE
- COVERTNESS
- HIGH ANGULAR RESOLUTION
- LOW TO MEDIUM POWER
- HIGH BEAM SCAN
- LOW SIDELOBES
- CONFORMAL
- AFFORDABLE

MTD\011989\EPS\096\062\MJR

POTENTIAL MILITARY SYSTEMS CANDIDATES FOR PHASED ARRAYS

US ARMY
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ELECTRONICS TECHNOLOGY and DEVICES LABORATORY

● 60GHz	SPACE COMMUNICATIONS, SDI	SABIR
● 35, 60, 94 GHz	SMART MUNITIONS	MLRS, HELLFIRE
● 94 GHz	ACQUISITION RADAR	ETAS (STARTLE) TACTICAL AIR
● 44, 60 GHz	COMMUNICATIONS	SPACE, HELICOPTER, TANKS
● 60, 94 GHz	TANK DEFENSE	DETECTION OF MISSILE & GUN FIRED PROJECTILES

PMS\011989\EPS\196\#52\MJR

THE KEY ELEMENT FOR CRITICAL FUTURE MILITARY SYSTEMS

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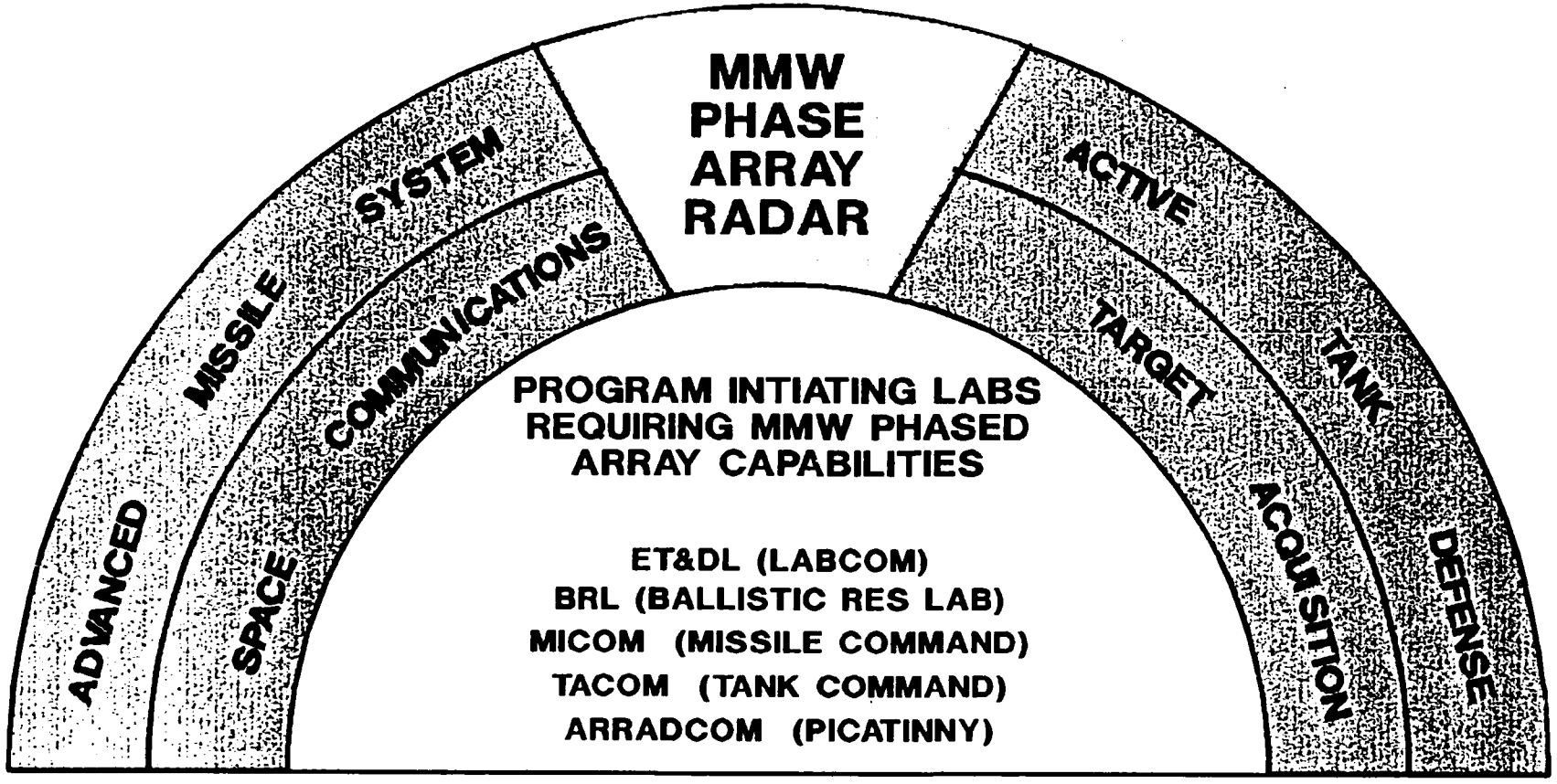


KEYSTONE\1-20-89\EPS\196\#52\SP

CRITICAL KEY AREAS FOR R&D

US ARMY
LABORATORY COMMAND

ELECTRONICS TECHNOLOGY and DEVICES LABORATORY

60-94 GHz COMPONENT TECHNOLOGY

HEMTs, PBTs, HBTs

MMW MONOLITHICS

DIRECT SURFACE RADIATION

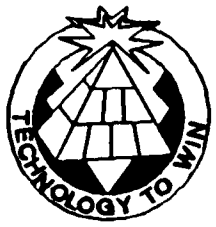
THERMAL DESIGN,& OTHERS

(AT 44 GHz EHF ARRAY PROGRAM HAS MADE A SIGNIGICANT IMPACT.)

REQUIRE ANOTHER CONCENTRATED EFFORT TO DESIGN AND DEVELOP A NEW GENERATION OF DEVICES AND CIRCUITS FOR 94 GHz TO MEET DOD NEEDS.

(MIMIC PROGRAM WILL NOT ADDRESS THESE AREAS)

CKAFR&D\1-20-89\EPS\196\s53\SP



POTENTIAL CANDIDATES 3-TERMINAL DEVICES FOR MILLIMETER WAVE PHASED ARRAY CIRCUIT ELEMENTS

US ARMY
LABORATORY COMMAND

ELECTRONICS TECHNOLOGY and DEVICES LABORATORY

- MESFETS
- PSEUDOMORPHIC HEMTS
- HETEROJUNCTION BIPOLAR
- PERMEABLE BASE TRANSISTOR
- INDIUM PHOSPHIDE FETs

PCT\011989\EPS\196\#52\MJR

FORT MONMOUTH PROGRAMS

US ARMY
LABORATORY COMMAND

ELECTRONICS TECHNOLOGY and DEVICES LABORATORY

1. PSEUDOMORPHIC HEMT (POWER) FOR SCOTT

   FUNDED ≈ 175 IN FY89 TOTAL ≈ 900K

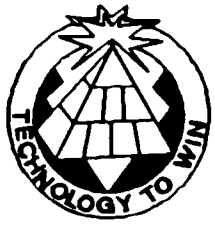
2. HBT FOR POWER AND EFFICIENCY (MMW)

3. MULTI BEAM PHASED ARRAY

   STUDY FOR TANK DEFENSE

} POTENTIAL NEW STARTS FOR FY89 IF FUNDING IS AVAILABLE AT THE PRESENT TIME.

PROGS\1-20-89\EPS\196\#52\SP



EHF DARPA ARRAY PROGRAM IMPACT

US ARMY
LABORATORY COMMAND

ELECTRONICS TECHNOLOGY and DEVICES LABORATORY

- LEADING THE DEVELOPMENT OF MILLIMETER WAVE DEAVICES FOR HIGHER POWERS.

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- HEMTs, HBTs, PBTs ARE ALL POTENTIAL CANDIDATES FOR REPLACEMENTS IN NEAR FUTURE.

- * PRESENTLY, Ft. MONMOUTH HAS A PROGRAM TO DEVELOP A 44 GHz 1/2 WATT DEVICE AND A 1 WATT MODULE TO REPLACE THE IMPATT BASED AMPLIFIER.

- PROJECT THAT WITHIN 3 YEARS–USING POWER DEVICE, THE IMPATT AMPLIFIER WILL BE REPLACED WITH MMW TRANSISTOR WHICH WILL ALLOW SMALL, EFFICIENT, COST EFFECTIVE AMPLIFIER.

Ballistic Transport in the Vertical and Lateral Domains

Mordehai Heiblum

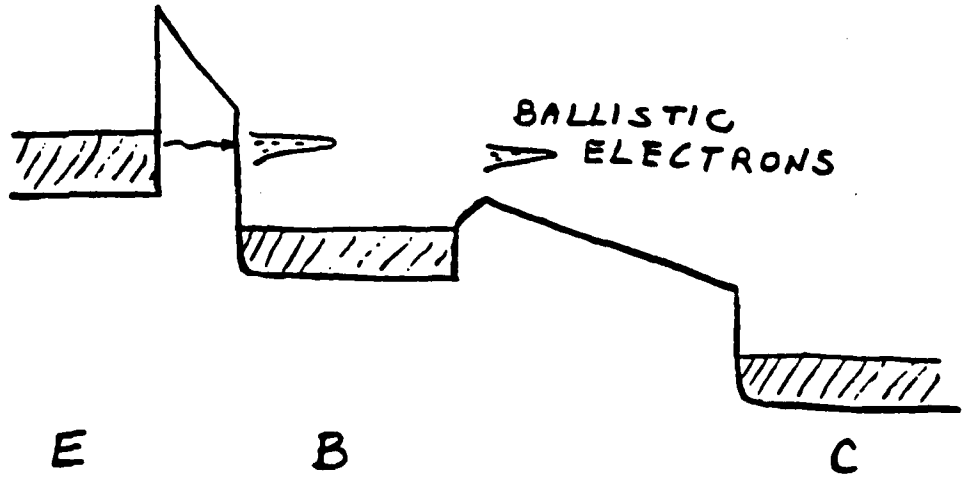
IBM
Yorktown Heights, NY

BALLISTIC TRANSPORT IN THE VERTICAL AND LATERAL DOMAINS

M. Heiblum

K. Seo, A. Palevski, C. Umbach, M. Weckwerth, D. Galbi, L. Osterling, C. Knoedler, and P. Bhattacharya

- Making High Gain THETA Devices
  1. All GaAs Device
  2. Strained Base Device
- A Lateral Ballistic Device
- Physics of Ballistic Transport: Single Phonon Emission

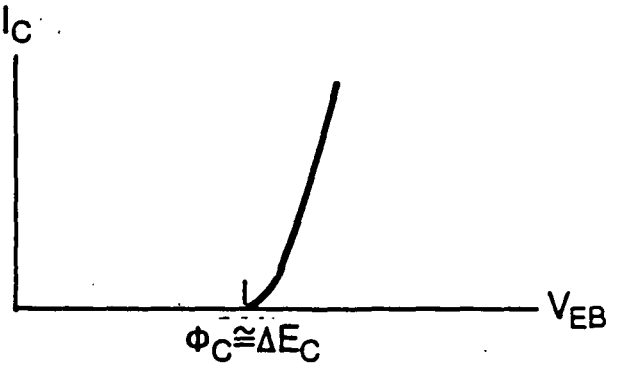


DEVICE POTENTIAL

- **No Minority Carriers Storage Effects**

- **Threshold Type Device**

  Threshold Determined by AlAs Mole–Fraction



- **Transit Time is < 0.2 pS**

For $J \cong 10^5$ A/cm^2
0.25 μm Geometry
$\Delta V = 0.1V$
} $\Delta t < 1ps$

TECHNOLOGICAL PROBLEMS WITH THE THETA DEVICE

- Low Gain
- Low Current Density
- High Base Resistance
- Poor Ohmic Contact to Base

Low Gain.....Is it an inherent problem in Ballistic Devices ?

CURRENT GAIN IN GaAs THETA DEVICES

Record Value Achieved for Base Doping of 8×10^{17} cm^{-3} :

α=0.9

β=9 at 77 K

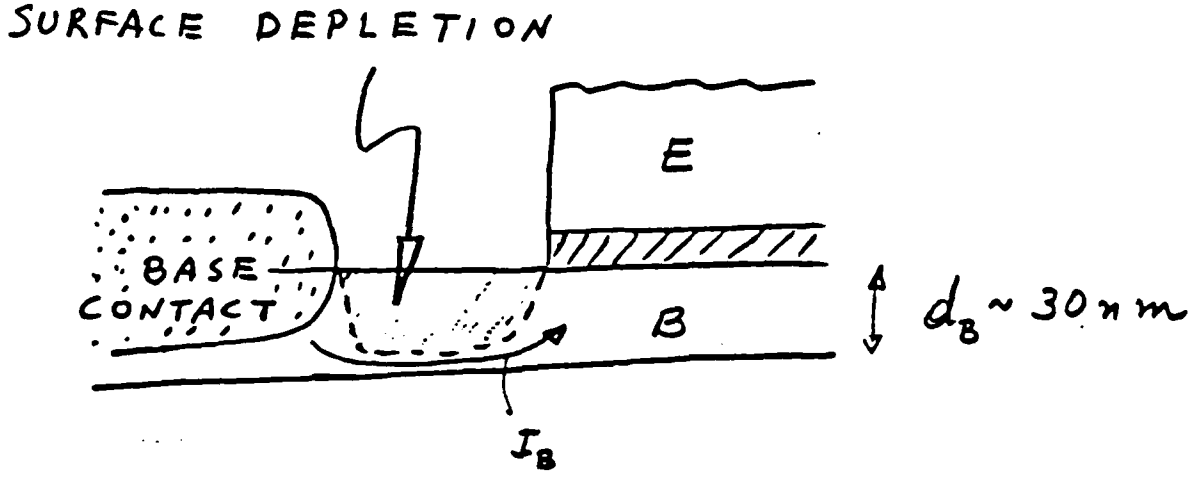
Questions Asked:

- What is the Ultimate Gain in GaAs Base Devices?
- Can the Gain be Increased with Different Base Materials?

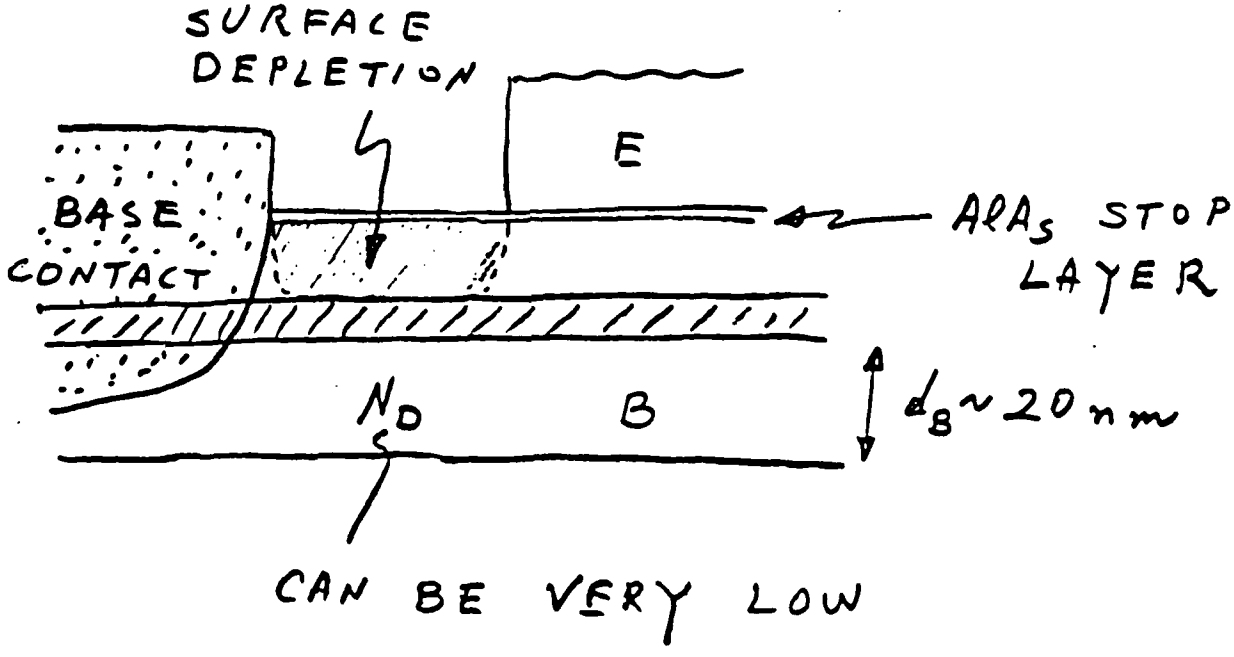
FACT : As the Doping Decreases the Gain Goes up !

The Base Depletion Problem

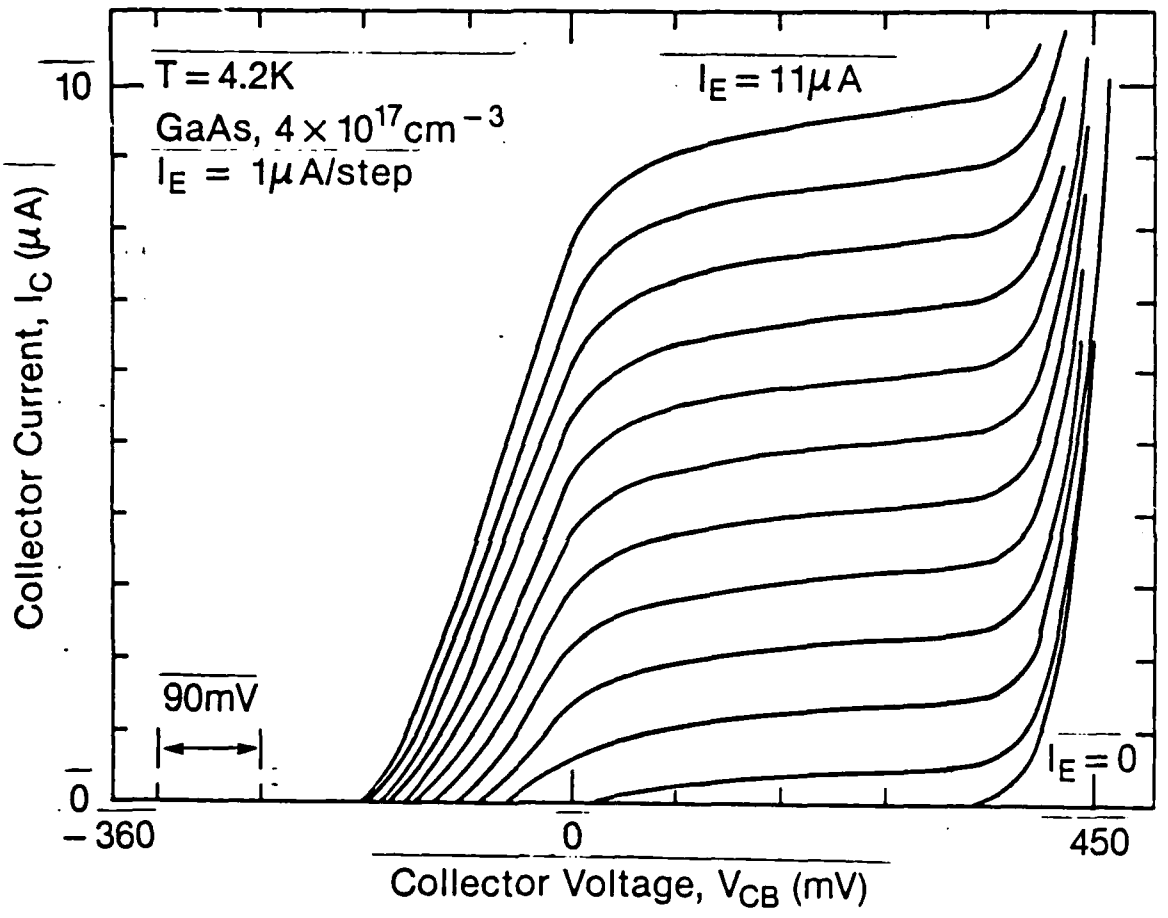
For $N_D = 4 \times 10^{17}\ cm^{-3}$



A Modified Design to Prevent Base Depletion

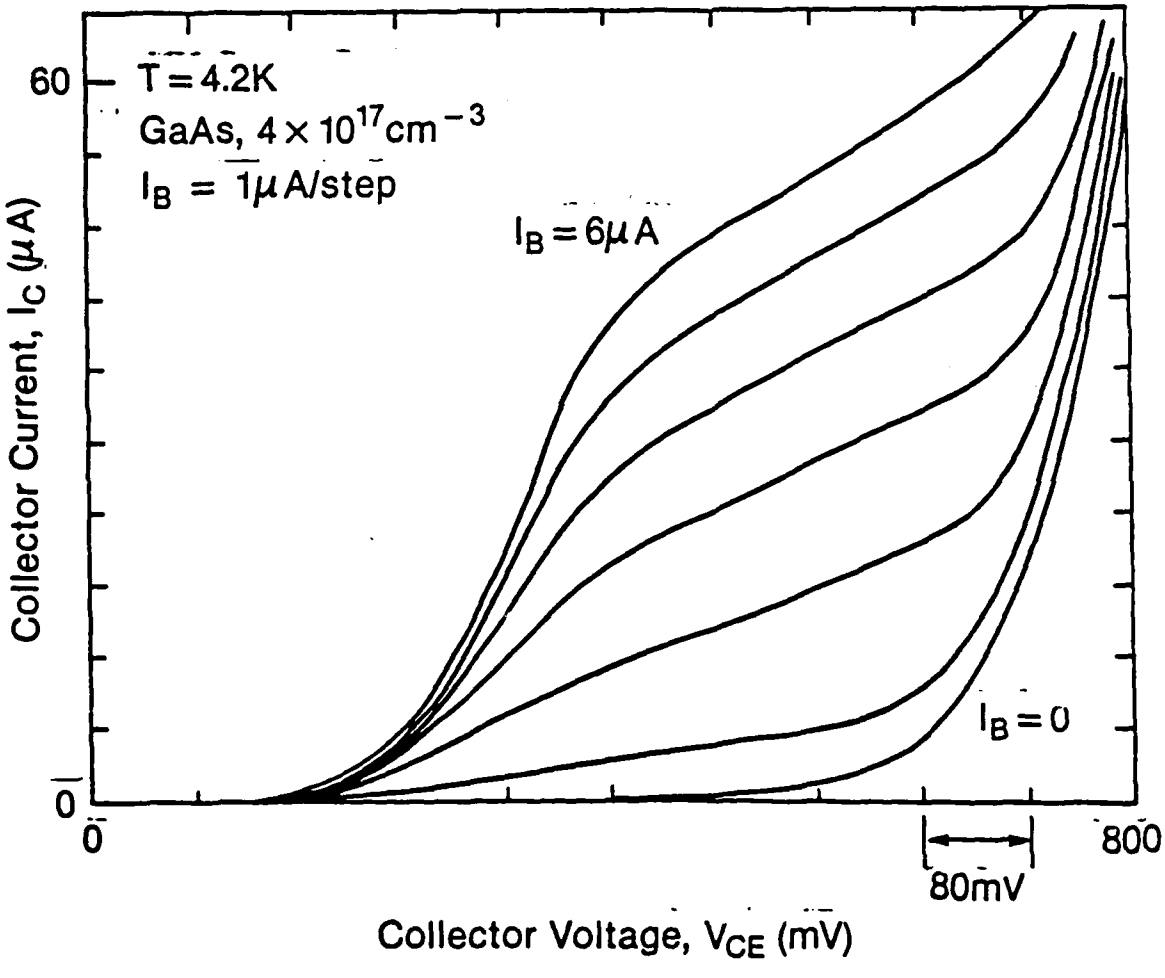


Common Base Characteristics



27

Common Emitter Configuration

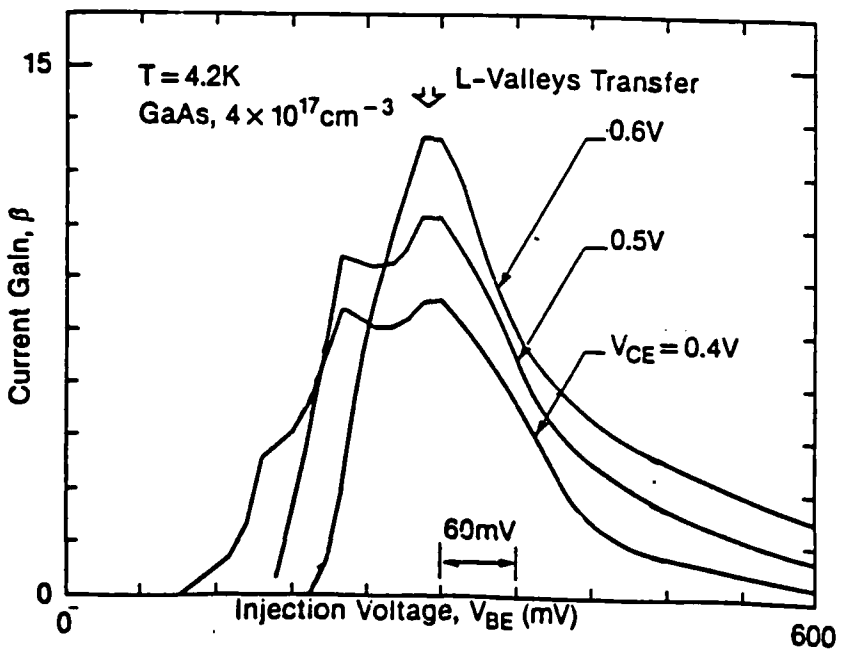


HIGHER GAIN RESULTS

$\alpha_{max} = 0.93$

$\beta_{max} = 13$ at 77 K

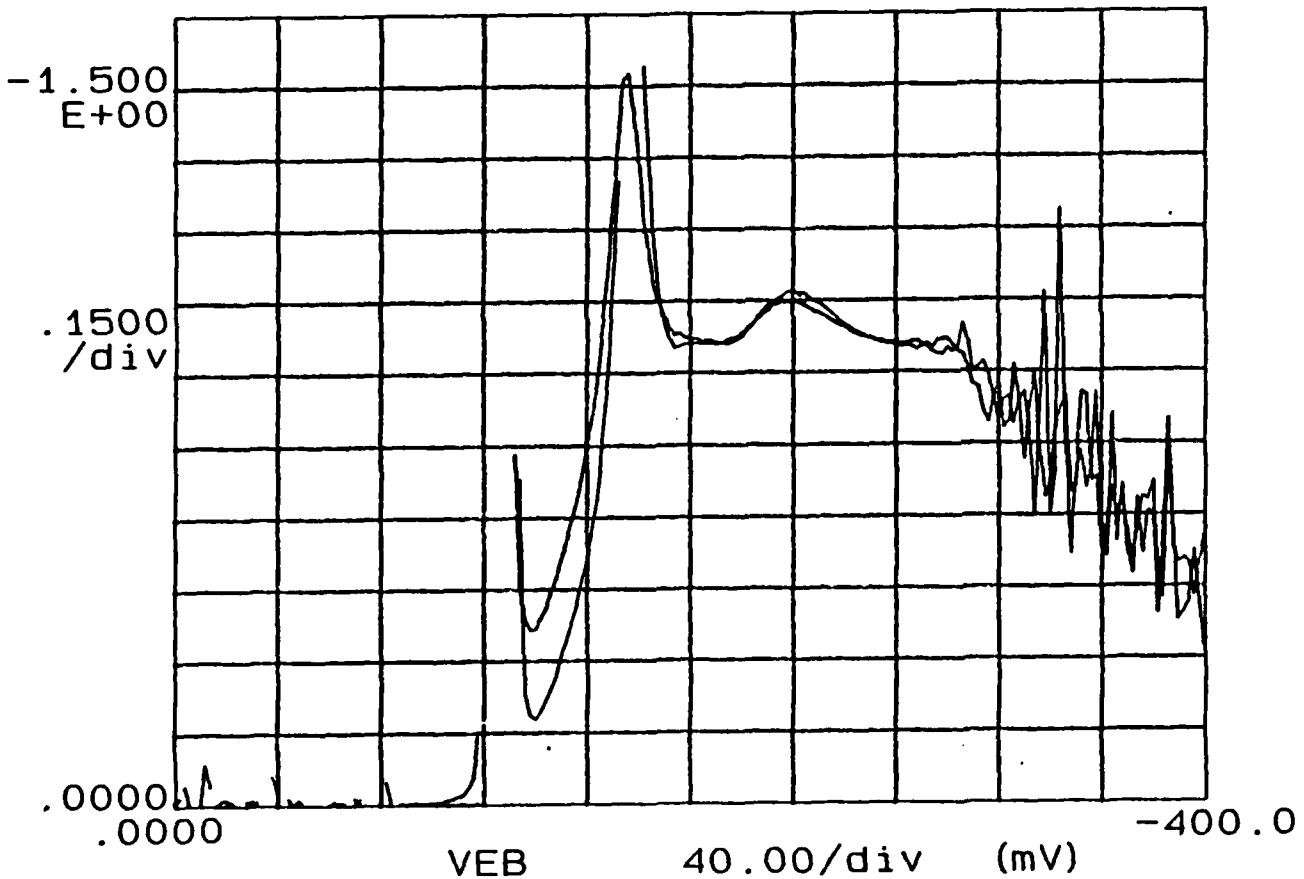
$l_{mfp} > 300$ nm



The Limiting Factor is L Valleys Transfer !

****** GRAPHICS PLOT ******

843



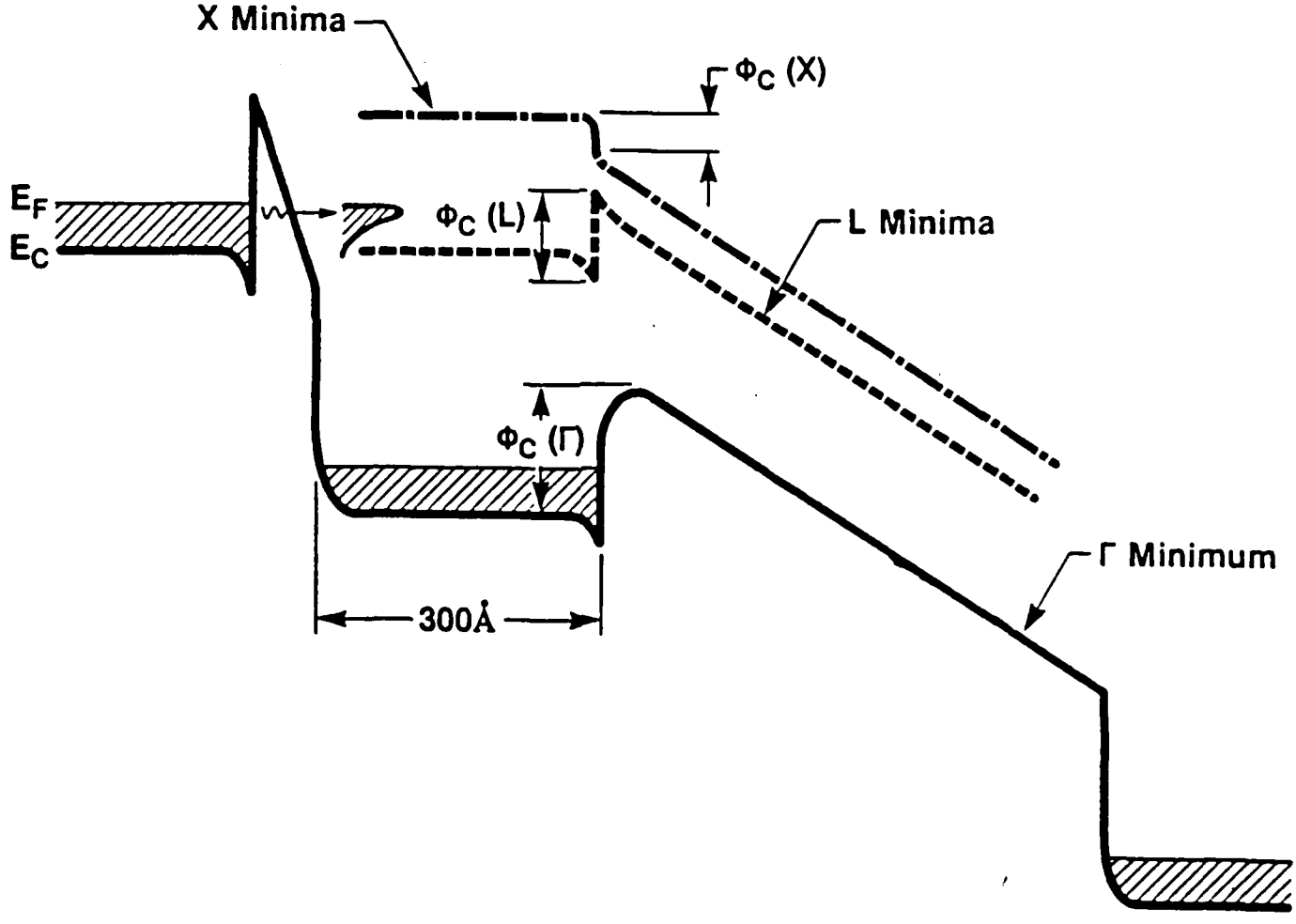
Variable1:
VEB -Ch1
Linear sweep
Start .0000V
Stop - .4000V
Step - .0020V

Variable2:
VCB -Ch3
Start .3000V
Stop .2990V
Step .1000V

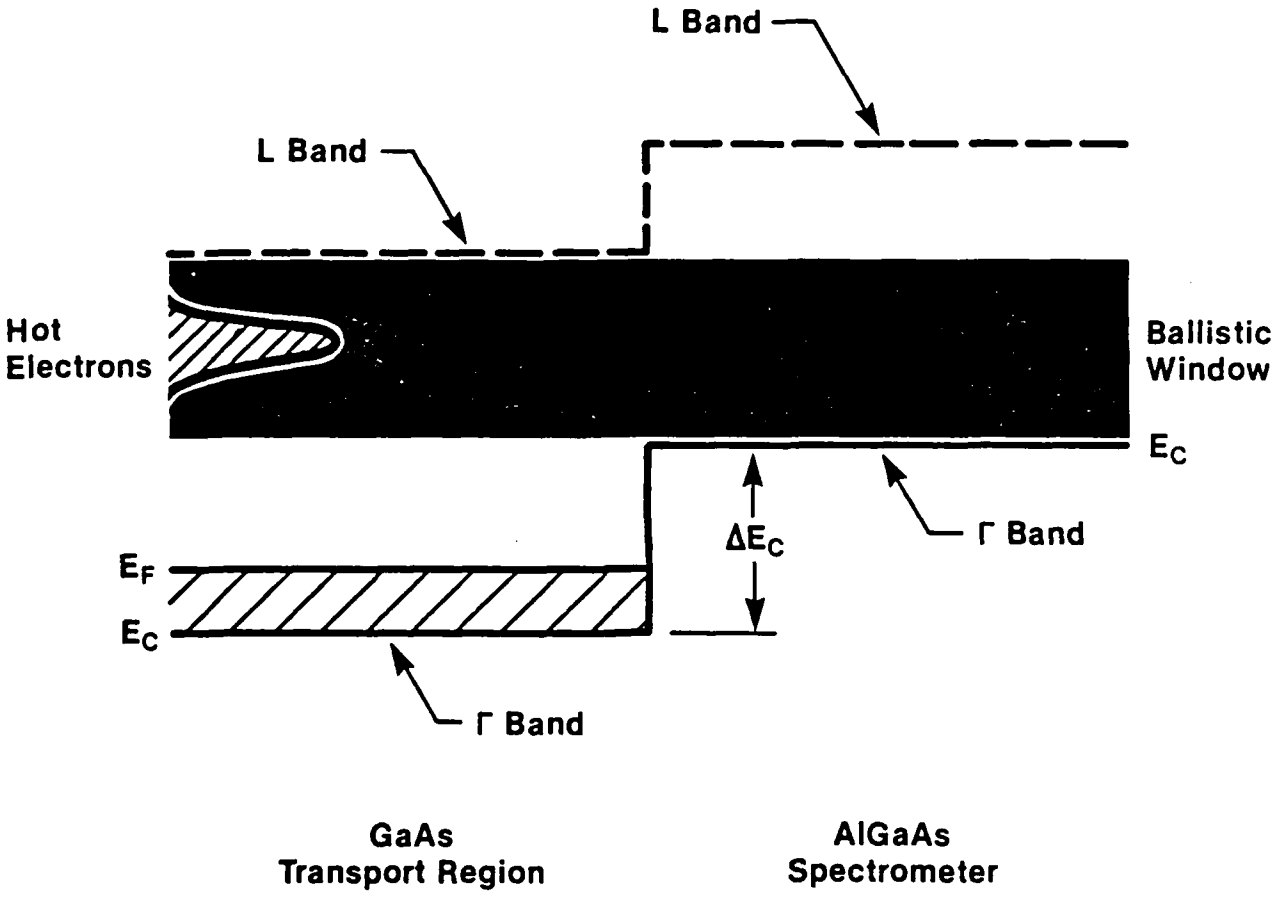
Constants:
VB1 -Ch2 .0000V
VB2 -Ch4 .0000V

AL ( ) = ΔIC/ΔIE
SAL ( ) = IC/IE

THE PROBLEM OF L VALLEYS TRANSFER



Window for Ballistic Transport



InGaAs PSEUDOMORPHIC BASE THETA DEVICE

(A) The Γ - L Separation in InAs is $E_{\Gamma L} = 1.16$ eV

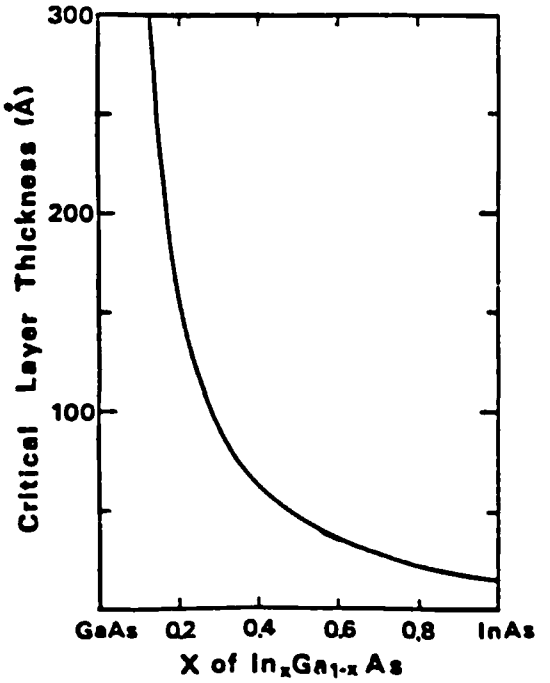
In InGaAs: $0.29 \text{ eV} < E_{\Gamma L} < 1.16 \text{ eV}$

(B) There is a band discontinuity ΔE_C to GaAs

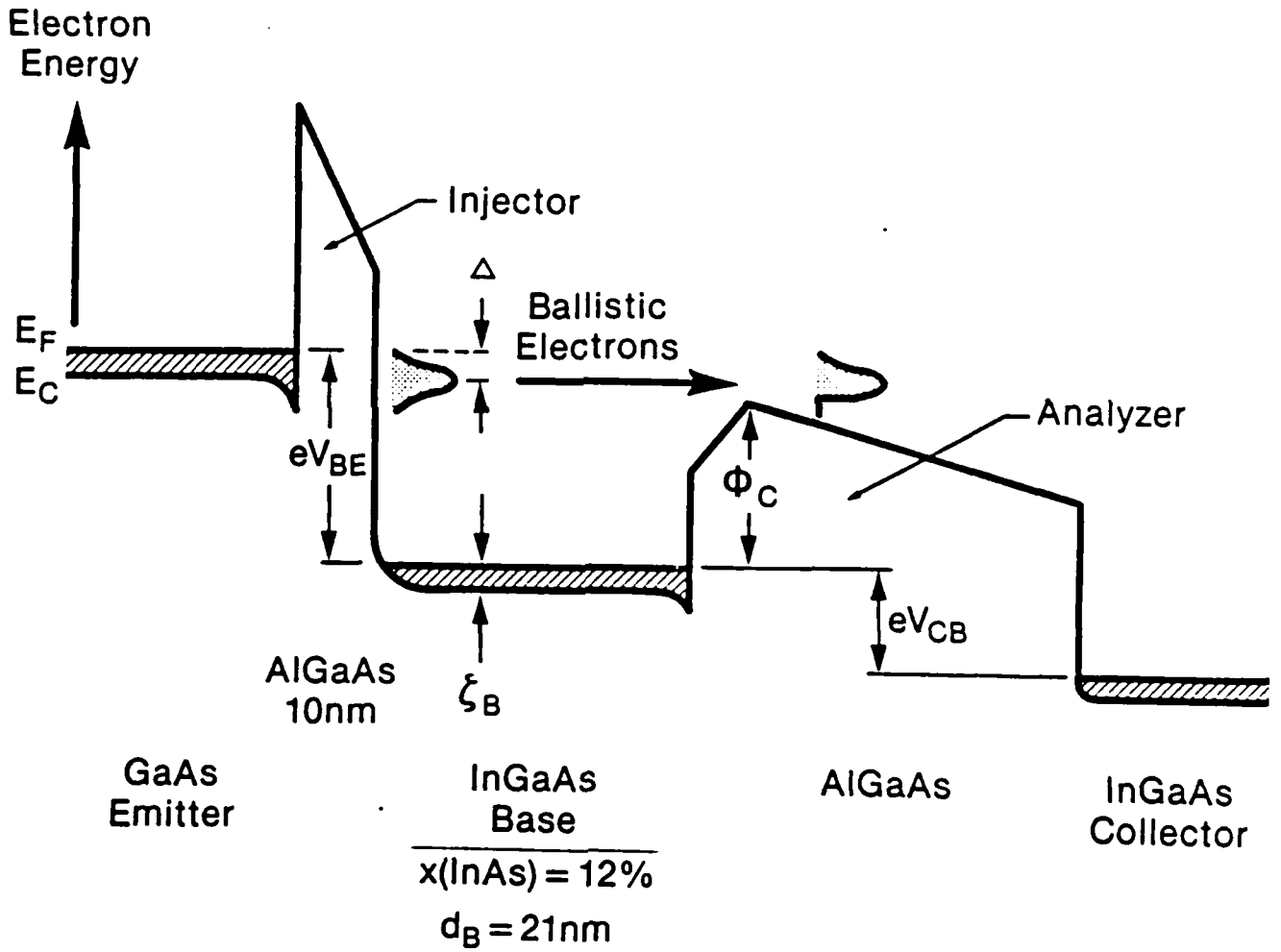
(C) InAs has a lattice constant 7% larger than GaAs.

For $In_xGa_{1-x}As$, x=14%, 1% Lattice Mismatch

CRITICAL THICKNESS for each InAs mole fraction. Below the CT Layers Can Grow PSEUDOMORPHIC

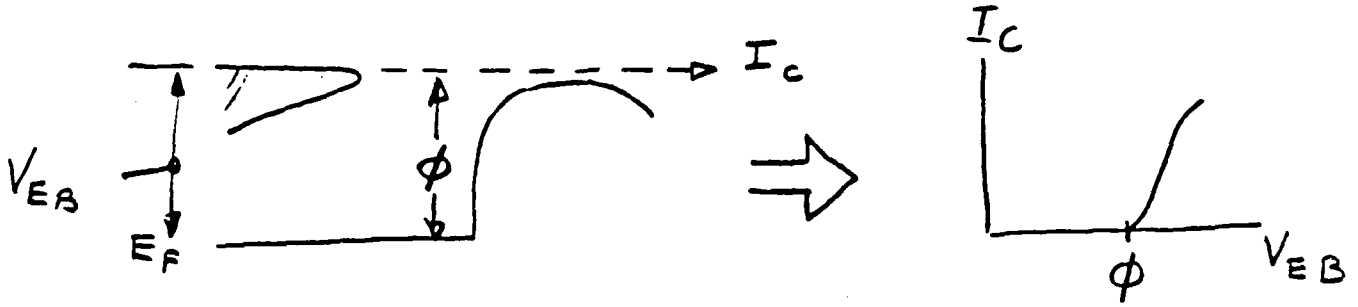


Pseudomorphic Base THETA



CHARACTERISTICS OF InGaAs BASE DEVICE

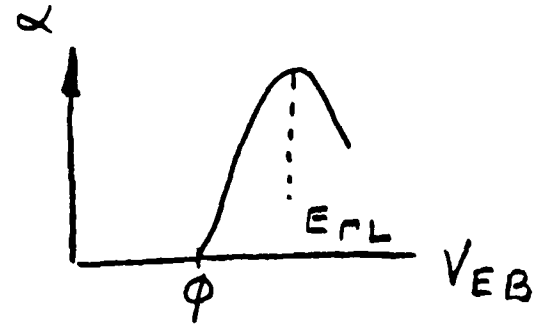
The Extra Band Discontinuity



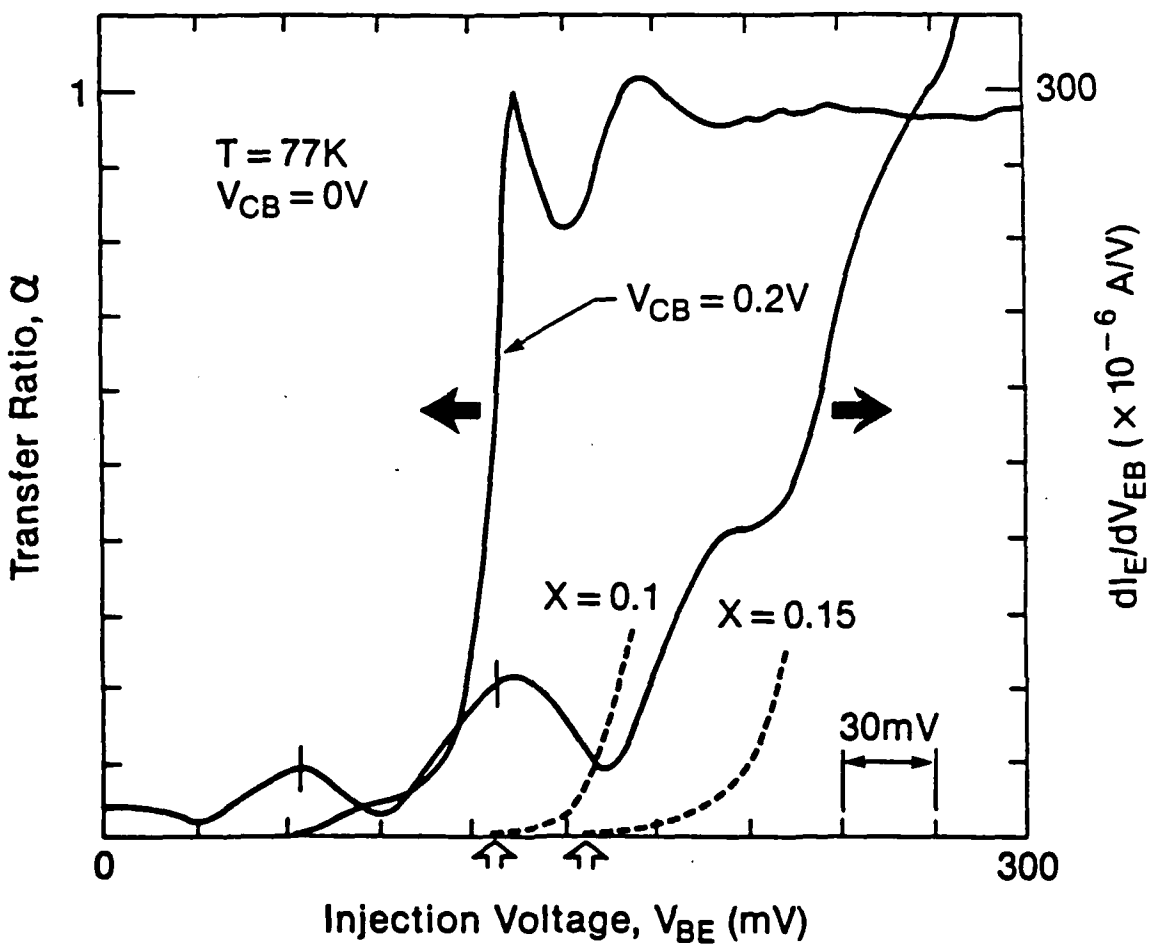
$\Delta E_C(GaAs - In_xGa_{1-x}As) = 7.5\ meV/1\%$

For x=15%.....ΔE_C=110 meV

$E_{\Gamma L}$

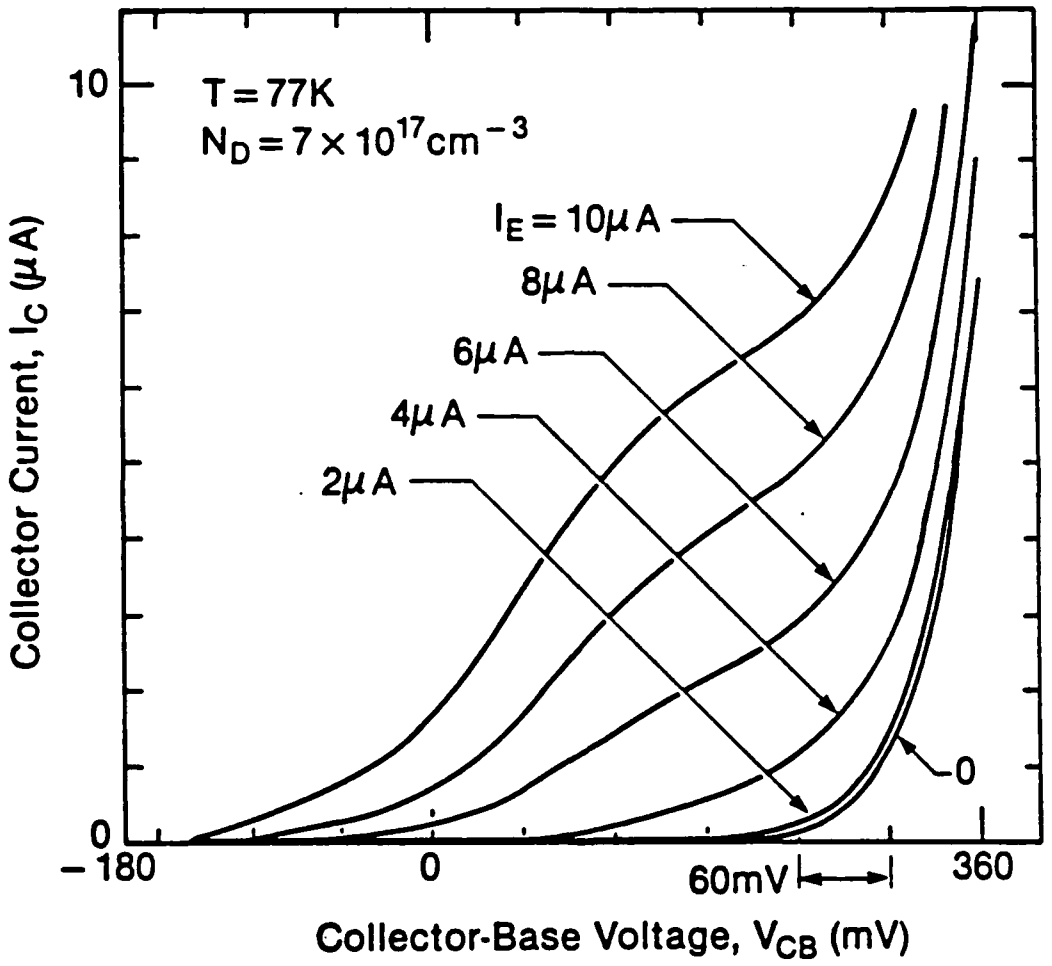


x=0 .....$E_{\Gamma L}$=0.29 eV
x=0.12.....$E_{\Gamma L}$=0.38 eV
x=0.15.....$E_{\Gamma L}$=0.41 eV


1
300
T = 77K
V_{CB} = 0V
V_{CB} = 0.2V
X = 0.1
X = 0.15
30mV
0
300
Transfer Ratio, α
dI_E/dV_{EB} ($\times 10^{-6}$ A/V)
Injection Voltage, V_{BE} (mV)

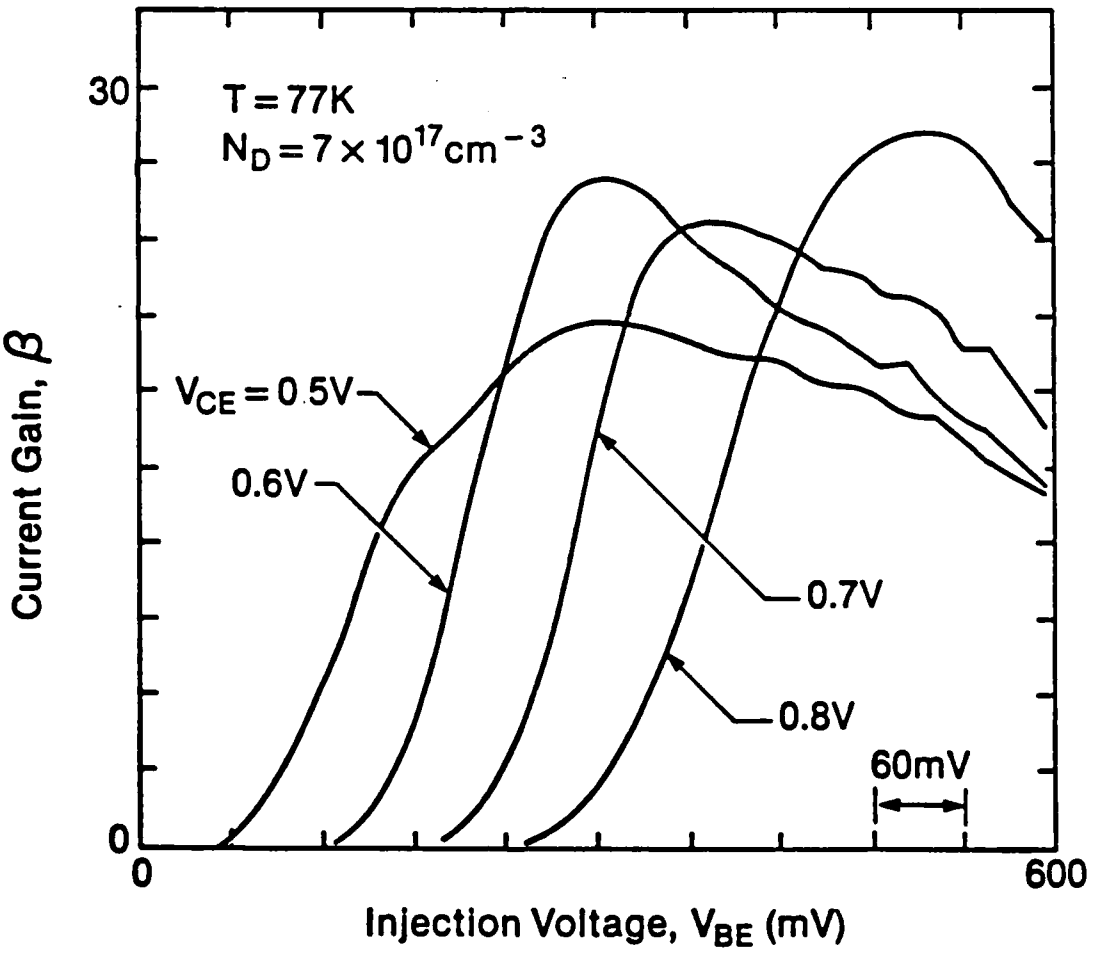
(b)

InGaAs Base, CBC



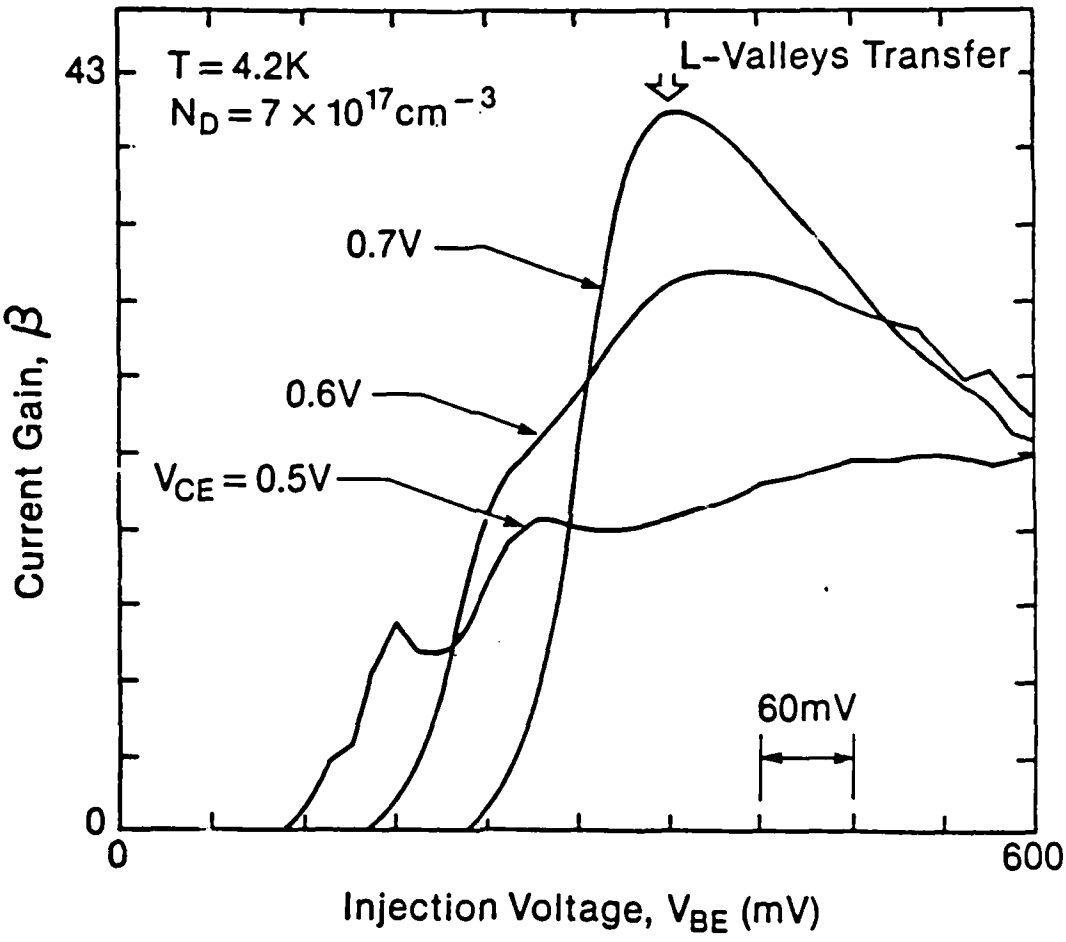
InGaAs Base

CEC, Current Gain at 77K



InGaAs Base

CEC, Current Gain at 4.2K



$\alpha_{max} = 0.975$

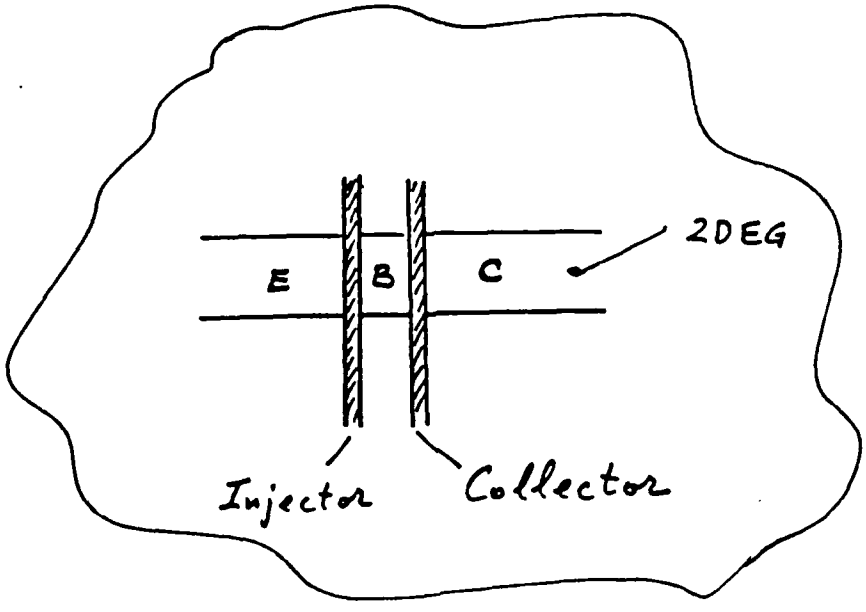
$L_{mfp} > 800$ nm

Device Achievements

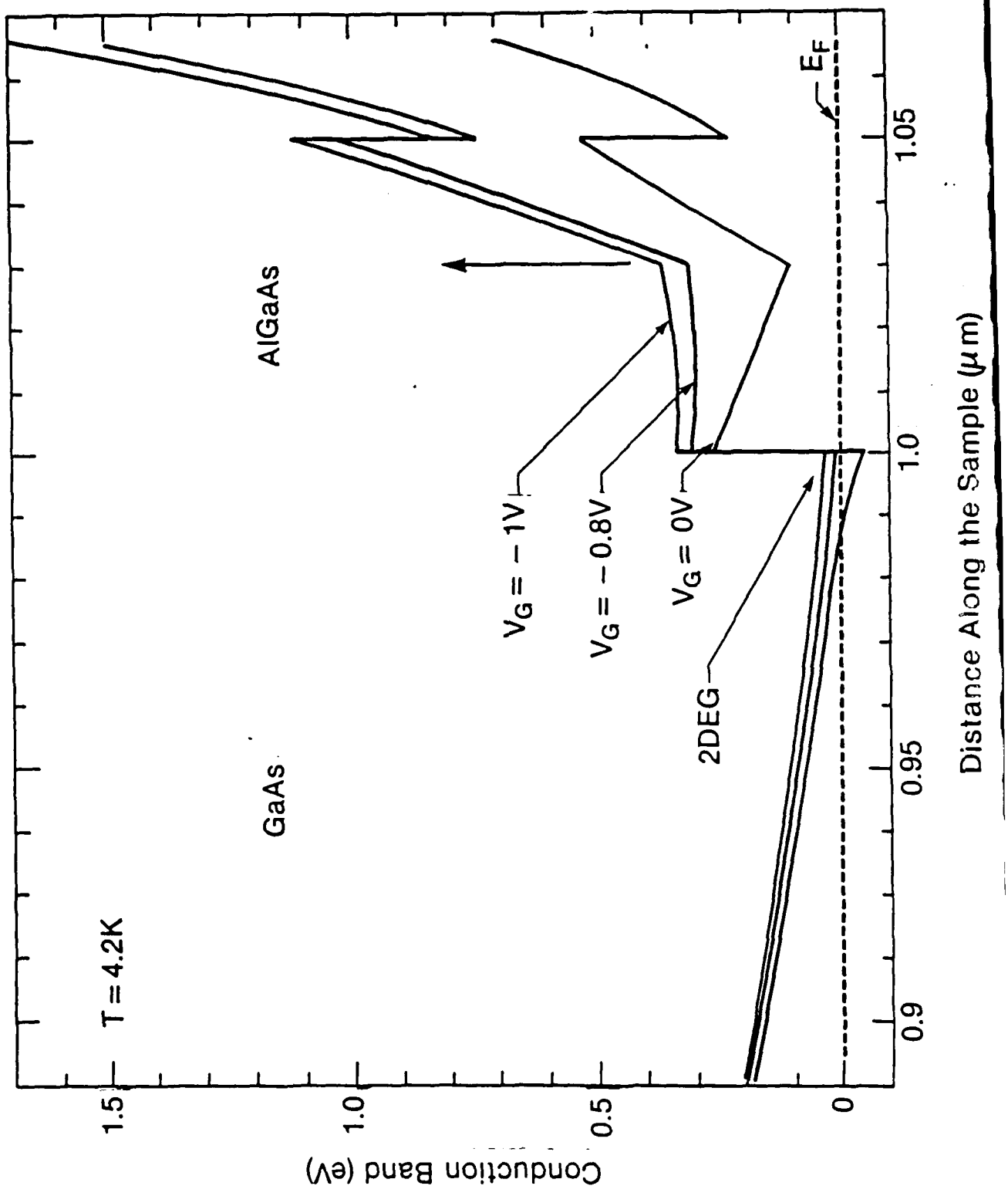
- Until Recently : $\beta_{max} \cong 9$
- Reduced Base Doping $\rightarrow 4 \times 10^{17} cm^{-3}$
  $d_B \cong 250 Å$
  $\beta_{max} \cong 13$ (4.2K)
- Increase Γ-L Valleys Separation by an InGaAs Pseudomorphic Base
  $\beta_{max} \cong 40$ (4.2K)
  $\beta_{max} \cong 30$ (77K)

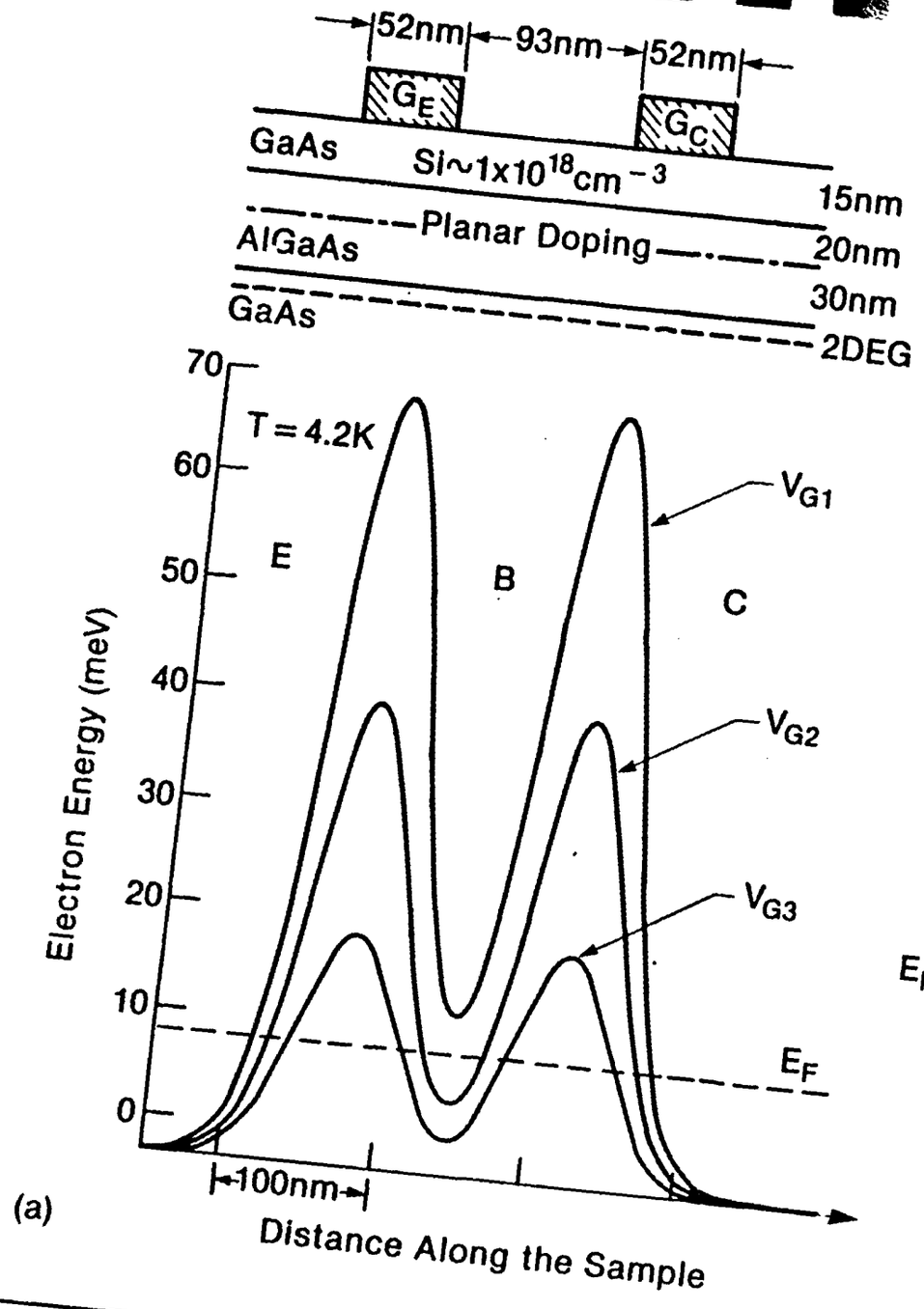
A LATERAL BALLISTIC DEVICE

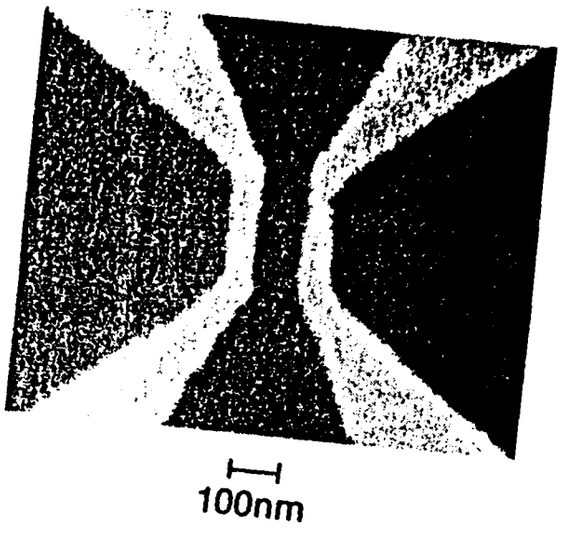
- Easy Contacting to Regions of the Device
- Using 2DEG as the Medium for Transport - Long Ballistic mfp
- An Added Lateral Dimension - Possibility of Stirring Electrons in the Plane

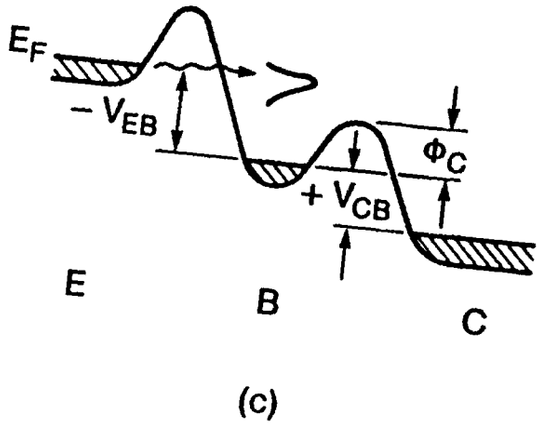


Biasing a 2DEG with a Gate



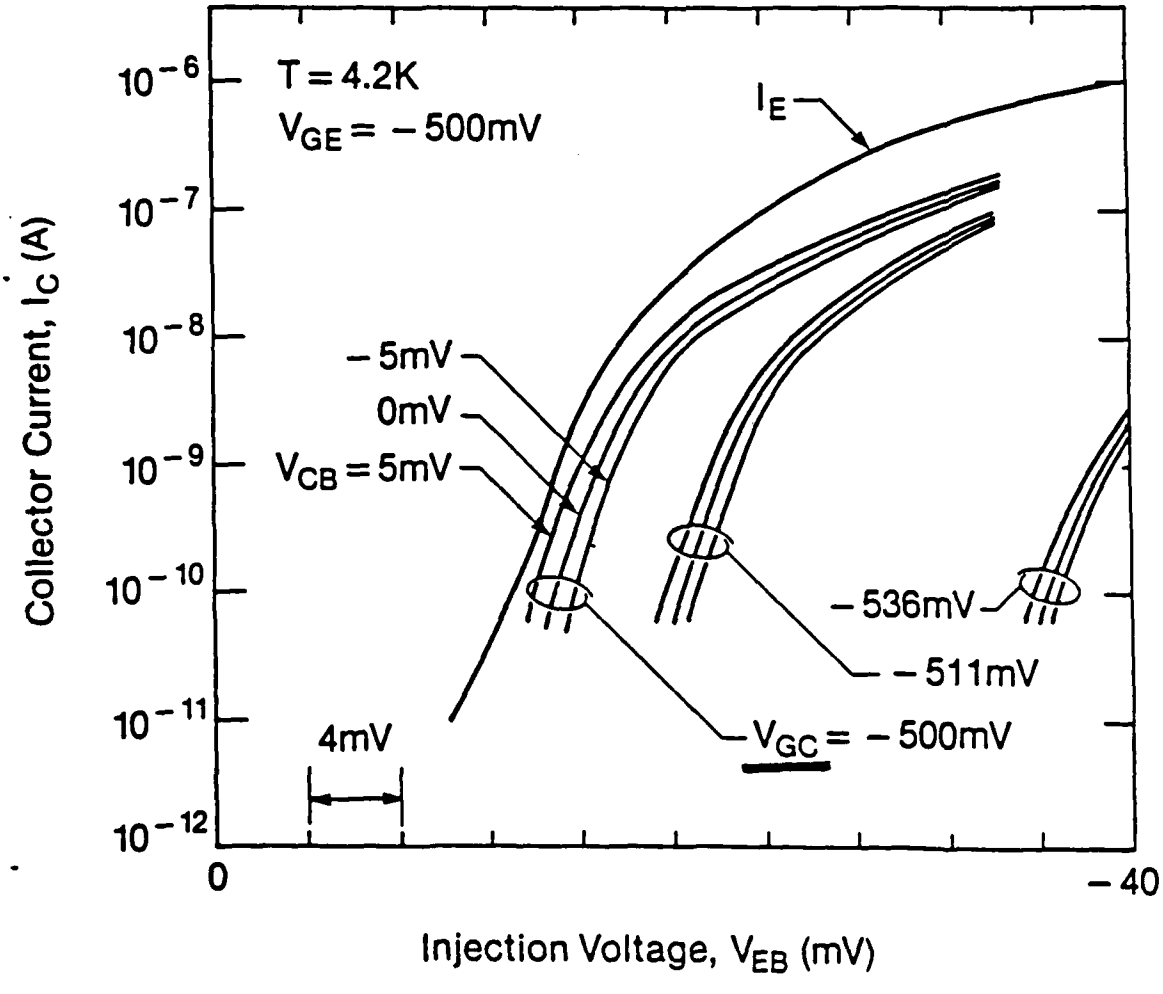

52nm
93nm
52nm
G_E
G_C
GaAs
Si~1x10^{18}cm^{-3}
15nm
Planar Doping
20nm
AlGaAs
30nm
GaAs
2DEG
T = 4.2K
V_{G1}
V_{G2}
V_{G3}
E
B
C
E_F
Electron Energy (meV)
70
60
50
40
30
20
10
0
100nm
Distance Along the Sample
(a)

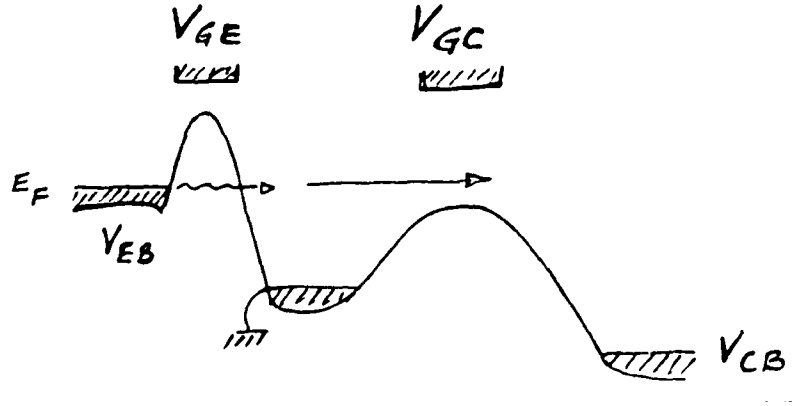

100nm
(b)


E_F
$-V_{EB}$
Φ_C
$+V_{CB}$
E
B
C
(c)

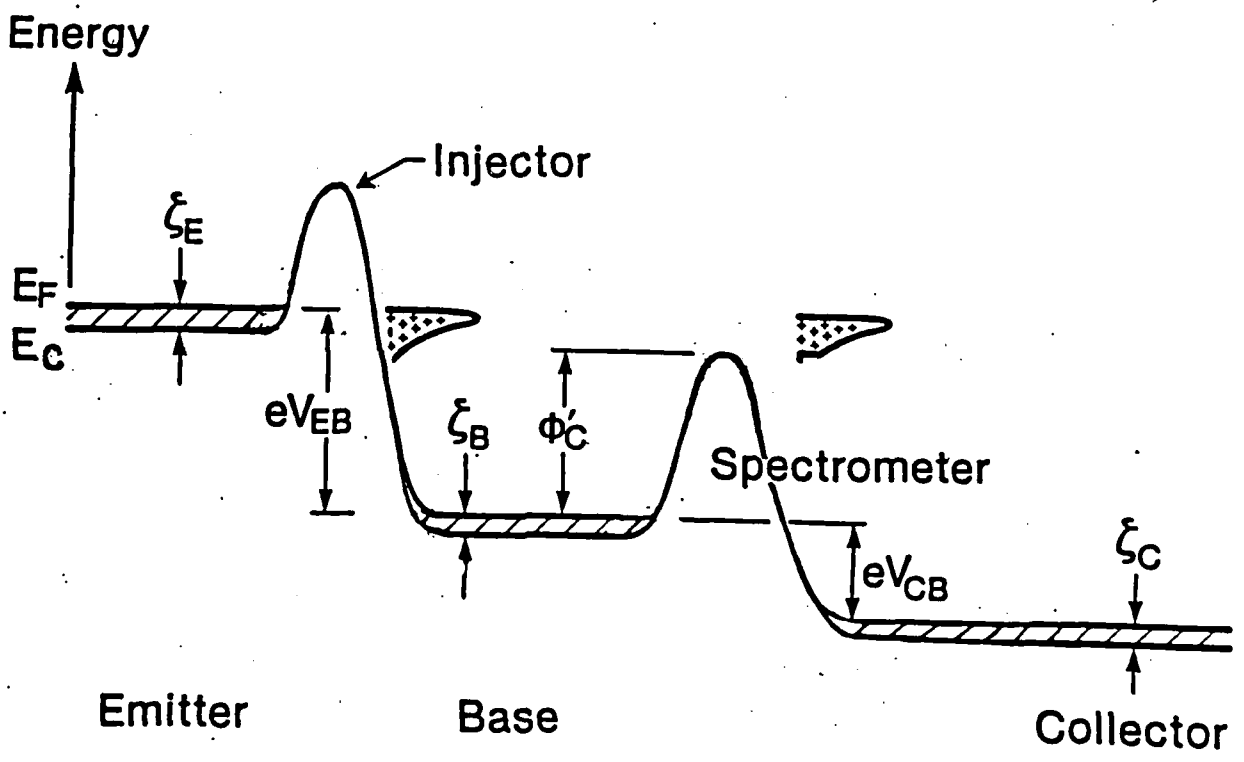
Collector Current Onset Changes

PROOF OF ELASTIC TUNNELING

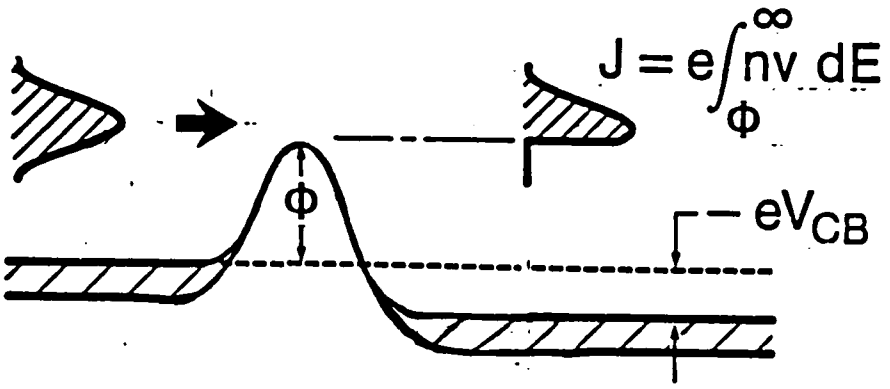




Ballistic Transport and Spectroscopy in Lateral THETA Device



Spectroscopy of Ballistic Electrons

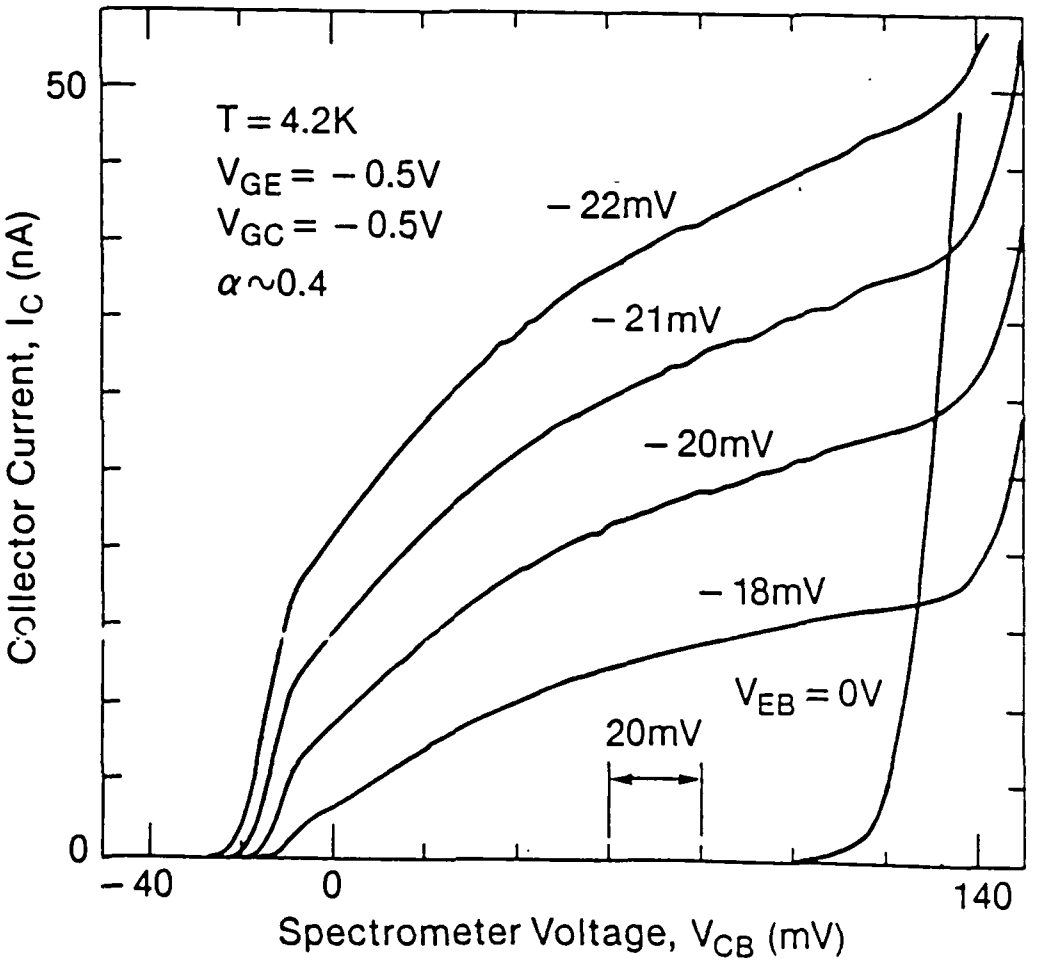


Base Barrier Collector

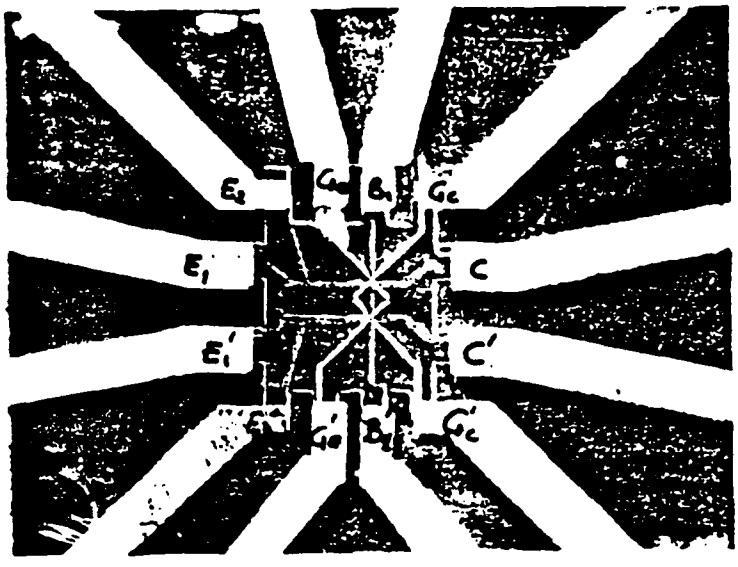
$$nv \sim \frac{dJ}{d\Phi} = \frac{dJ}{dV_{CB}} \Big/ \frac{d\Phi}{dV_{CB}}$$

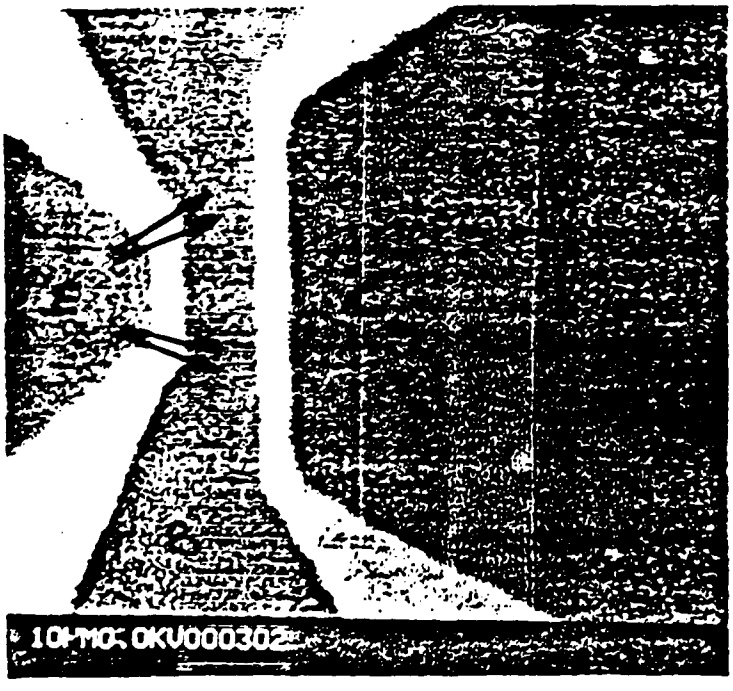
Measured

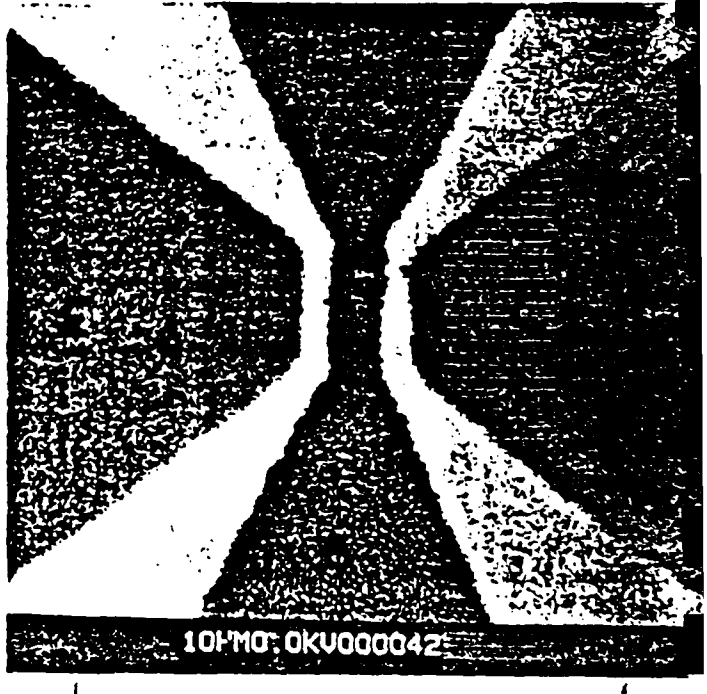
Output Characteristics in a Common Base Configuration



Geometry of the Gates and Formation of Ohmic Contact to a Base.

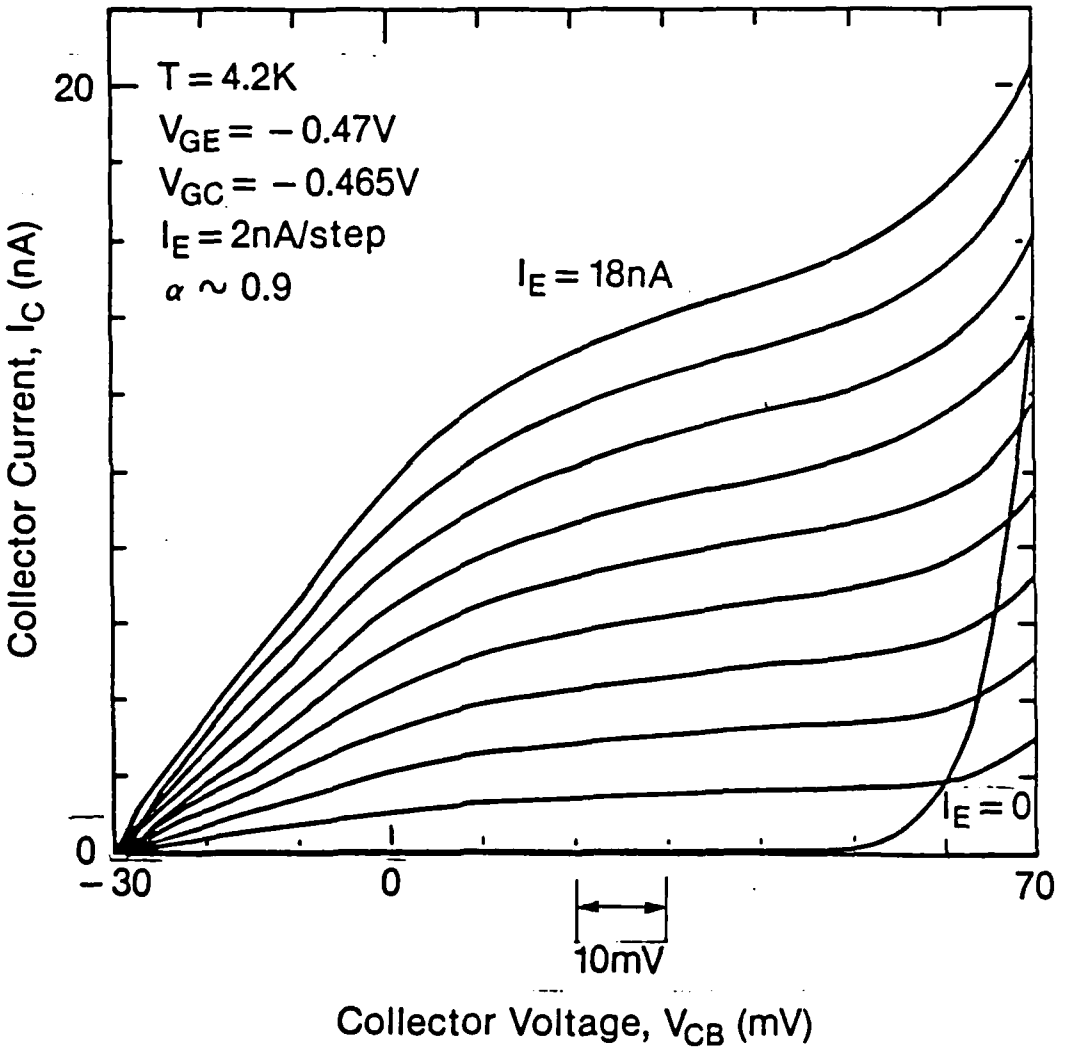




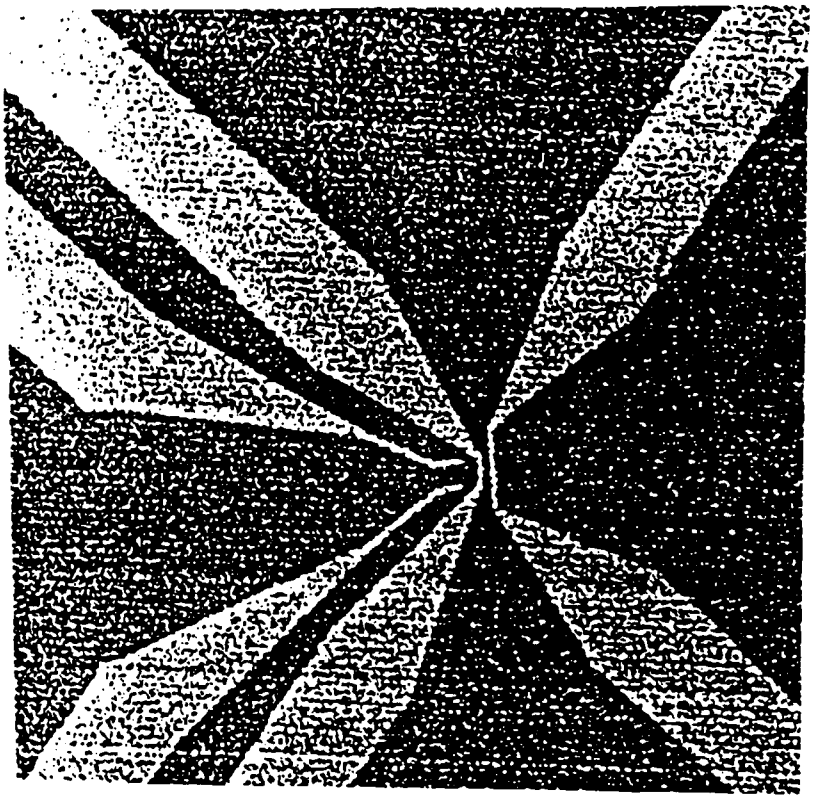


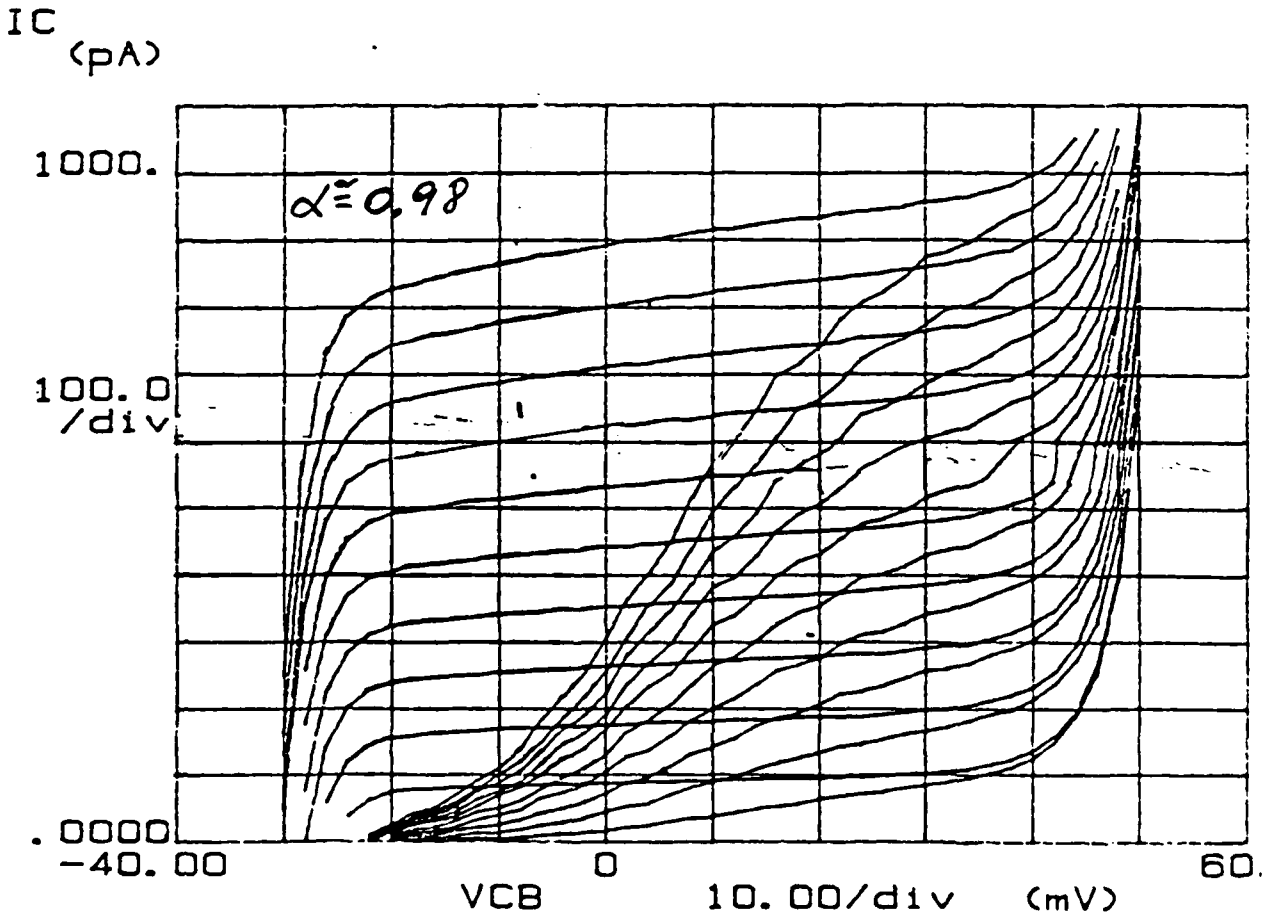
Common Base Configuration

LATERAL THETA



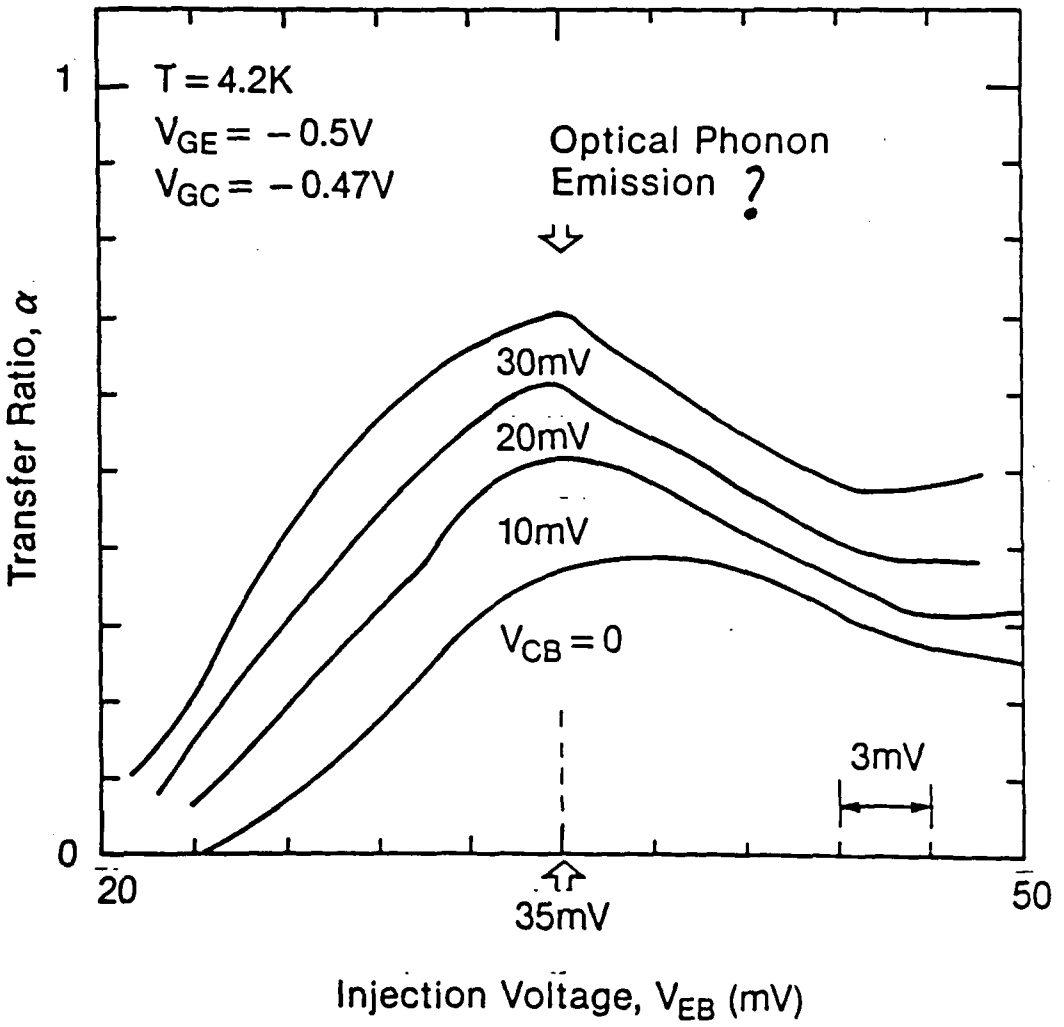
$\alpha \cong 0.9$




IC
(pA)
1000.
α≅0.98
100.0
/div
.0000
-40.00
0
60.
VCB
10.00/div
(mV)

XI

Optical Phonon Emission



$\alpha = \exp\left(-\frac{d_B}{\lambda}\right) = .7$

$\lambda \simeq 480$ nm

Conclusions

- Proof of Lateral Tunneling through a Wide Barrier
- Proof of Lateral Ballistic Transport with a Long Mean Free Path
- Possible High Gain THETA device.
- New Experimental Tool for Studying Quantum Properties of Electron Transport

PHYSICS WITH THE THETA DEVICE

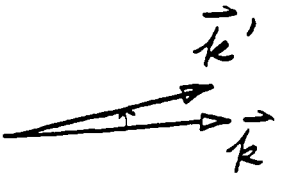
- Observation of Ballistic Transport (Electrons and Holes)
- Observation of Quantum Interference Effects (Electrons and Holes)
- Observation of L Valleys Transfer
- Measuring Band Discontinuities
- Observation of a Single Phonon Emission

PHONON EMISSION

- Dominant Phonon Scattering is due to LO Phonons in GaAs.

- Scattering ~ $|\vec{k} - \vec{k}'|^{-2}$,

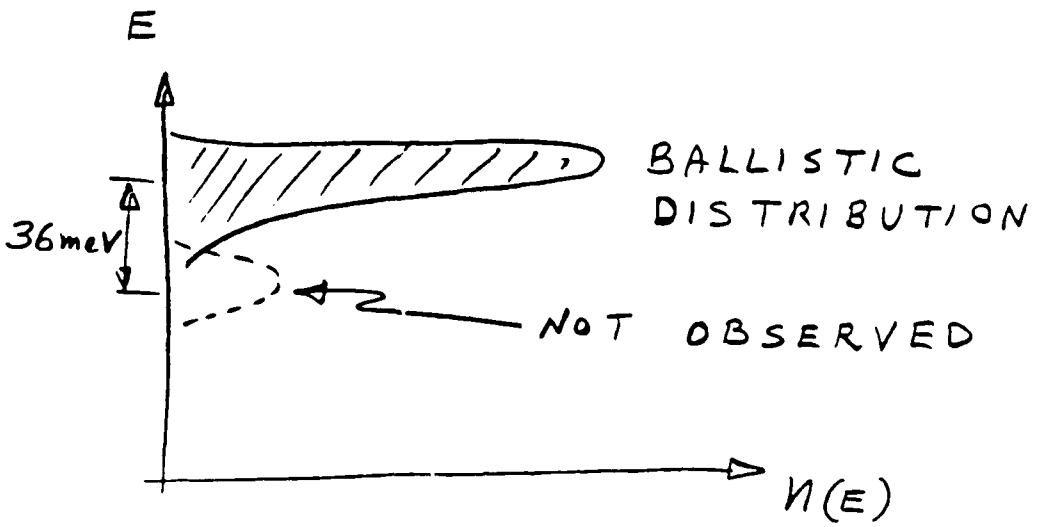
  Small Angle Scattering is Preferred



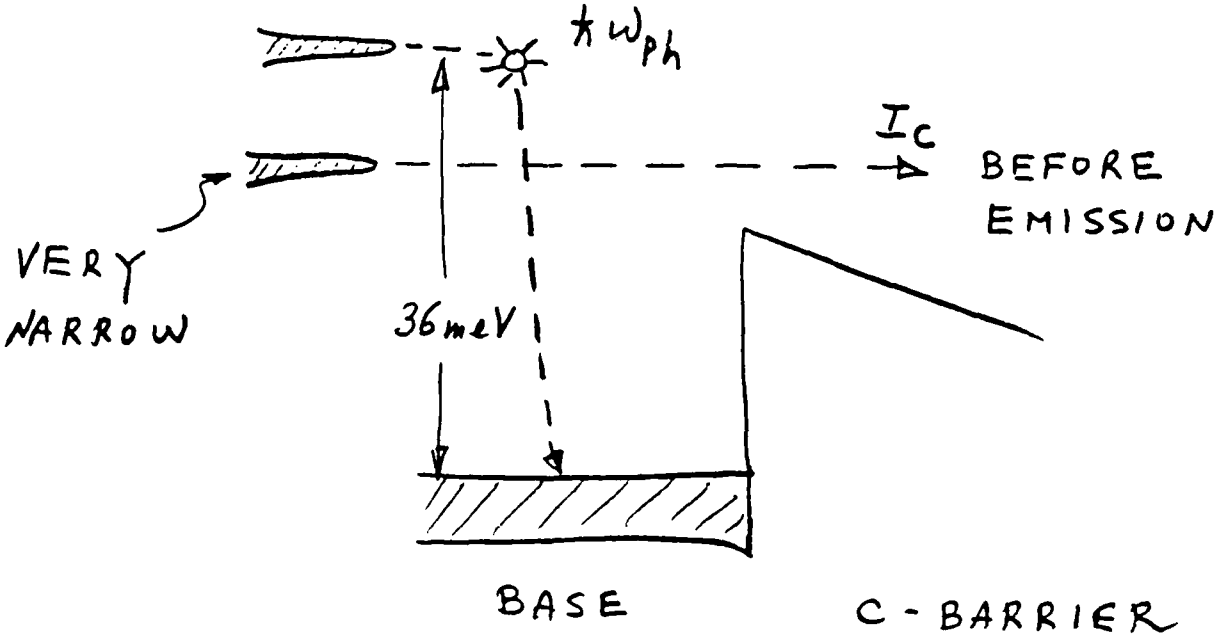
- Phonon Energy in Unscreened GaAs, $\hbar\omega_{LO}$=36 meV

- At Low Temperatures Only Phonon Emission Dominates

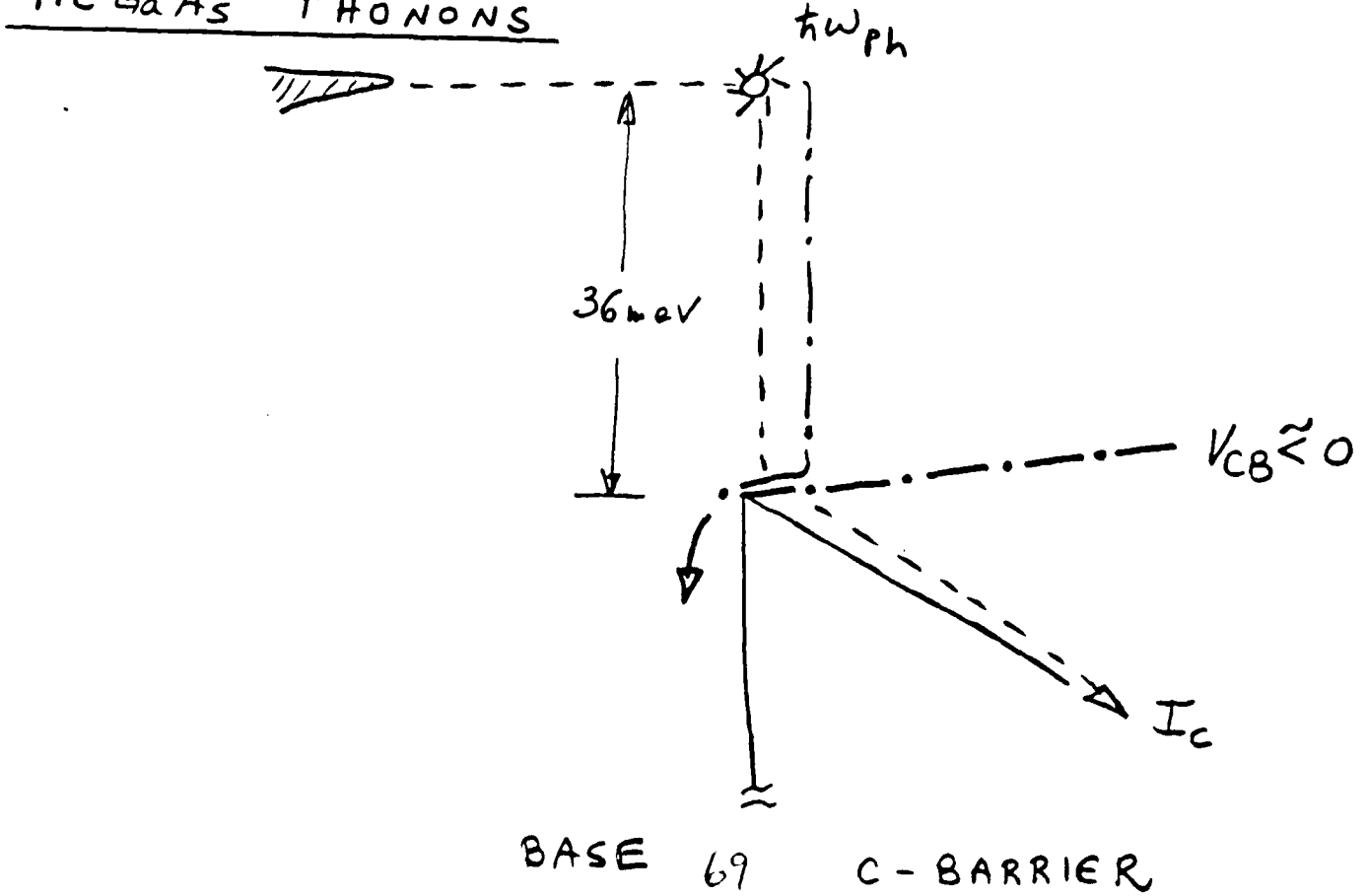
<u>Experimentally: We did not Observe Phonon Emission via Spectroscopy</u>



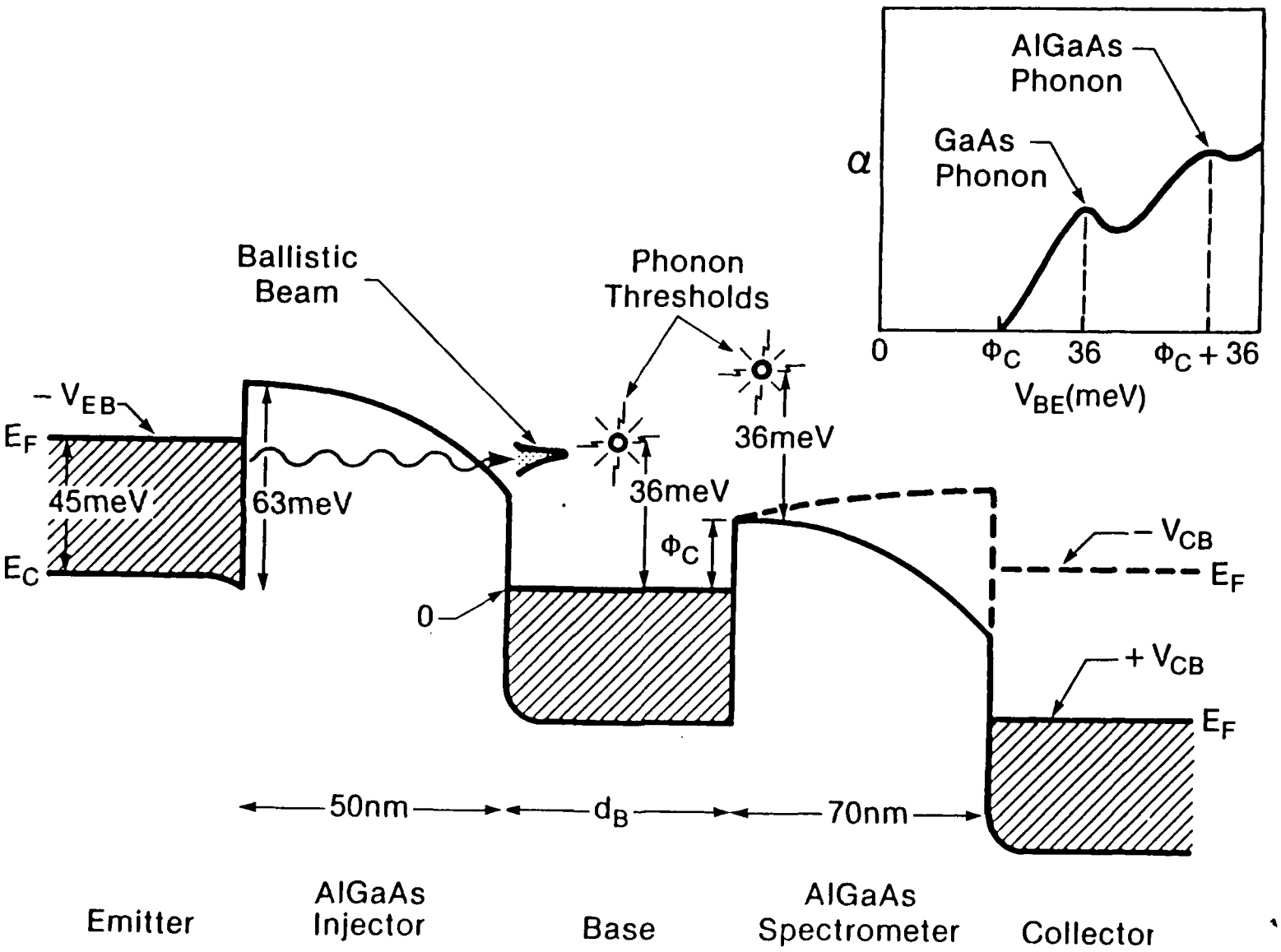
GaAs PHONONS



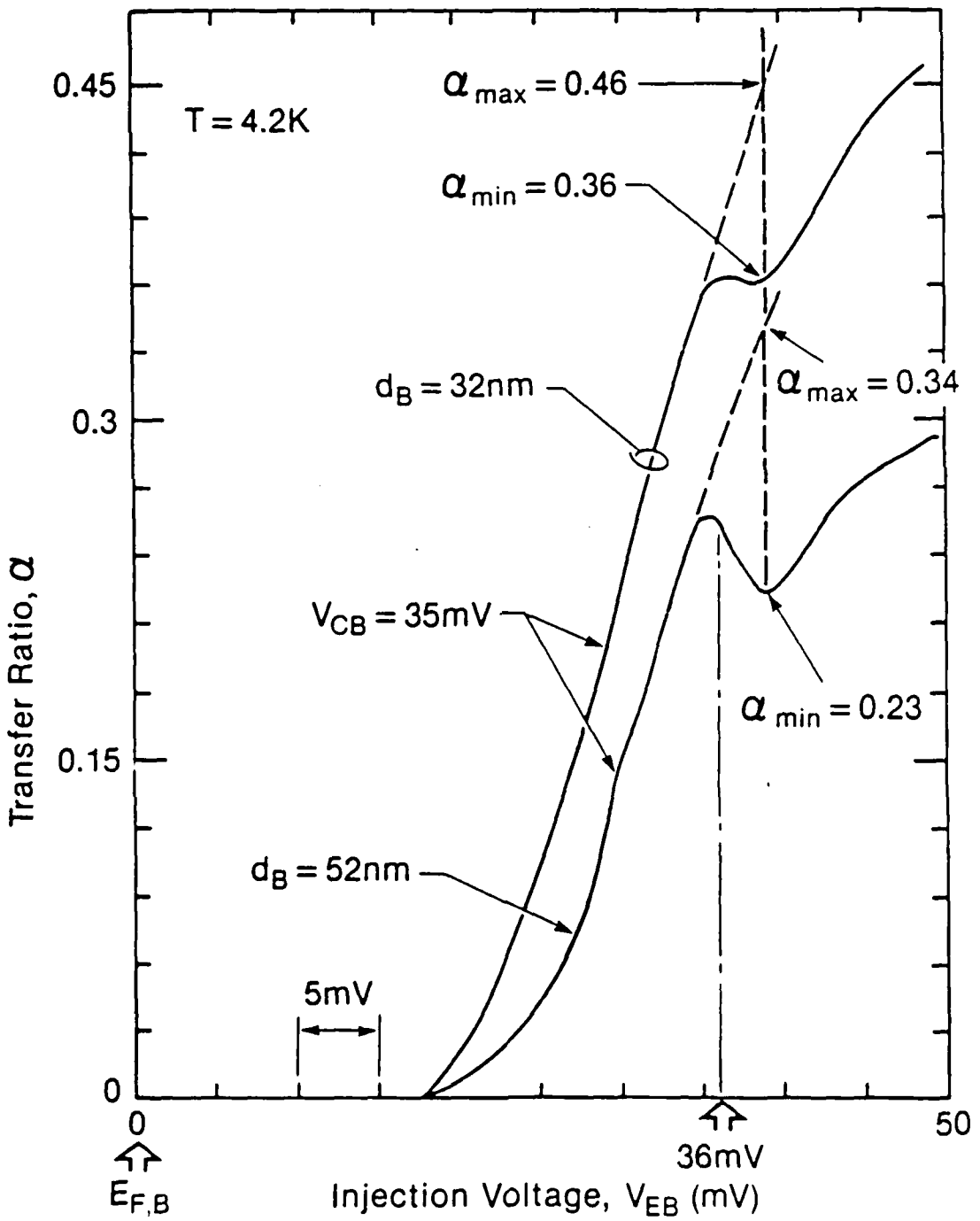
AlGaAs PHONONS



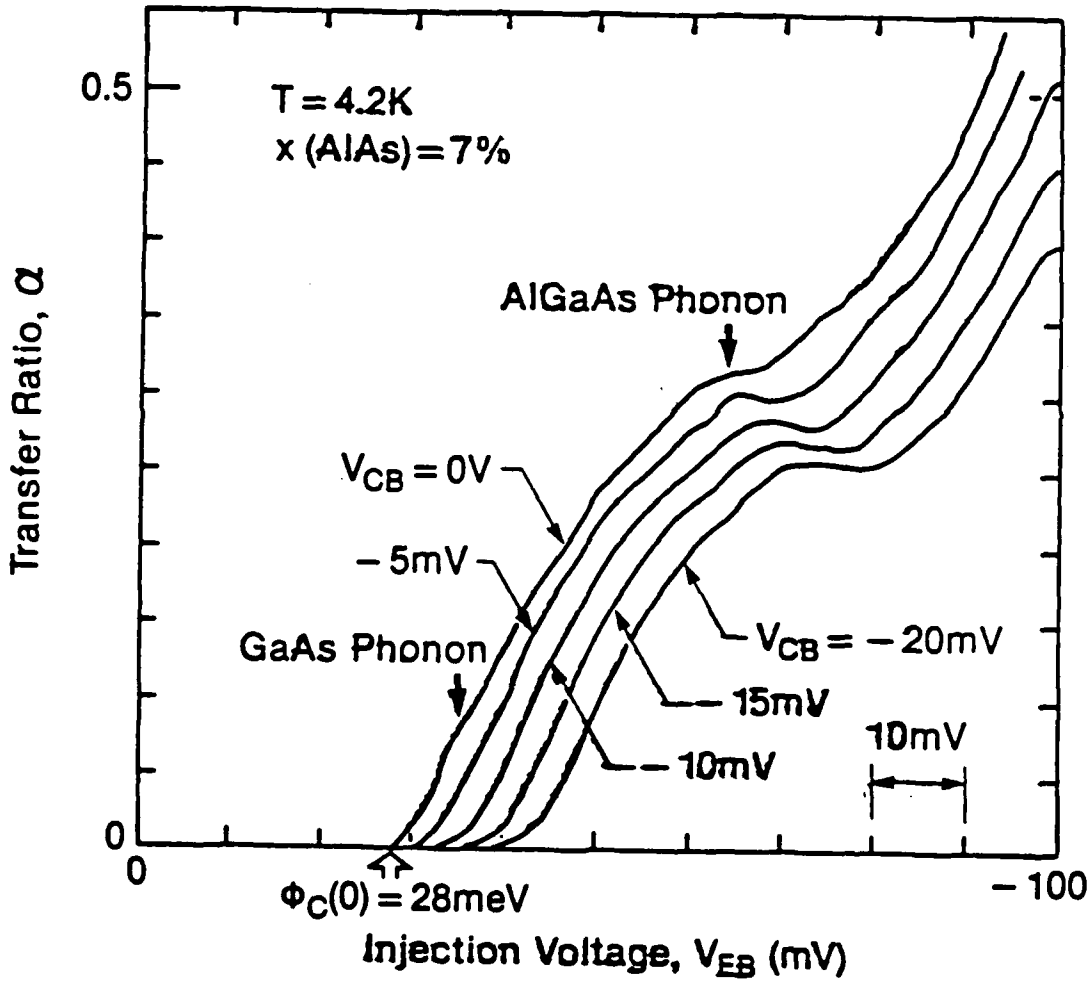
Ballistic Electrons Emitting Phonons



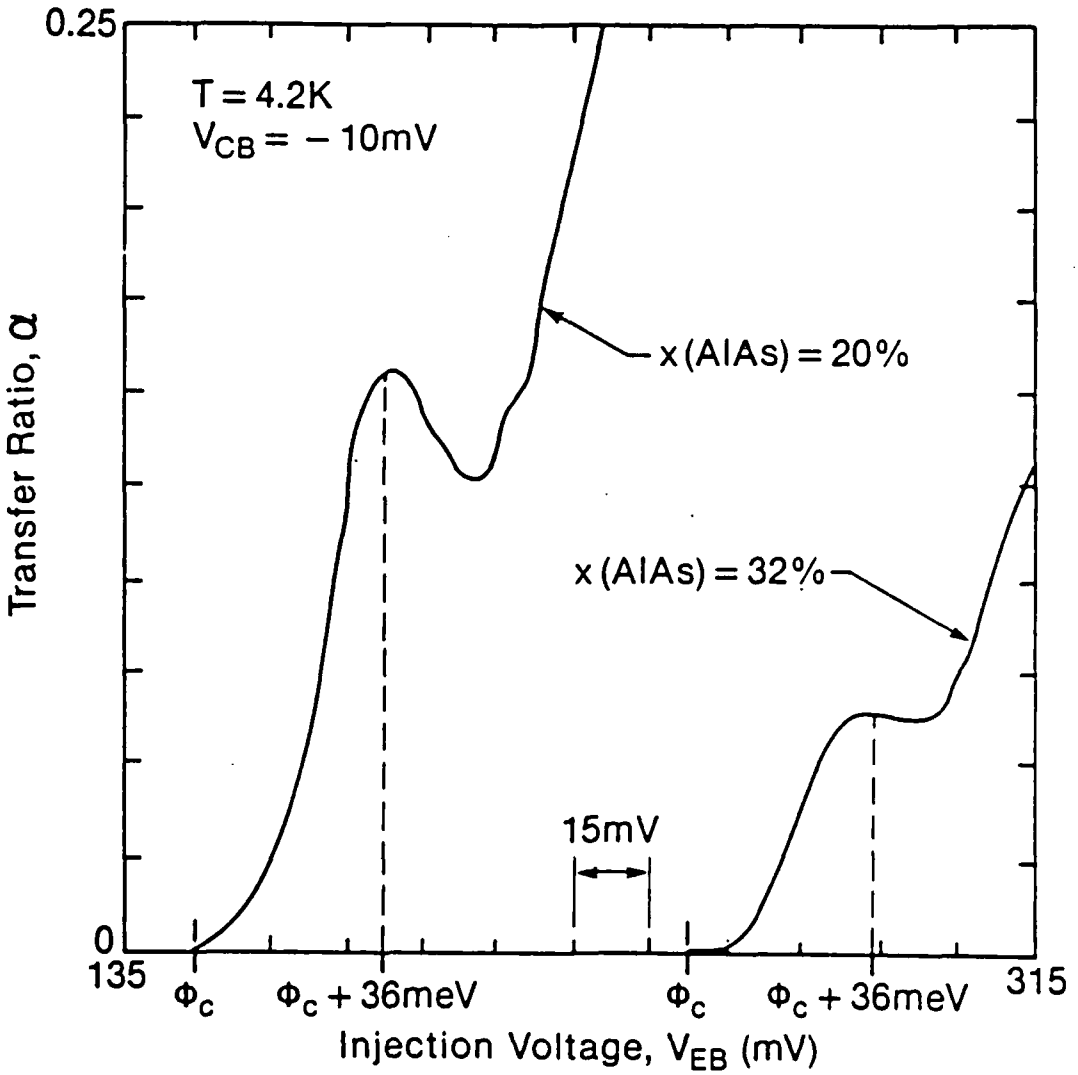
Observation of Single Phonon Emission in GaAs



$\ell_{mfp} \cong 130\ nm$


T = 4.2K
x (AlAs) = 7%
0.5
0
0
AlGaAs Phonon
GaAs Phonon
V_{CB} = 0V
– 5mV
– 10mV
– 15mV
V_{CB} = – 20mV
10mV
$\Phi_C(0)$ = 28meV
– 100
Transfer Ratio, α
Injection Voltage, V_{EB} (mV)

Observation of Single Phonon Emission in AlGaAs



Permeable Base Transistor and Regrowth FET Development

Mark A. Hollis

MIT Lincoln Laboratory
Lexington, MA

PBT AND REGROWTH FET DEVELOPMENT

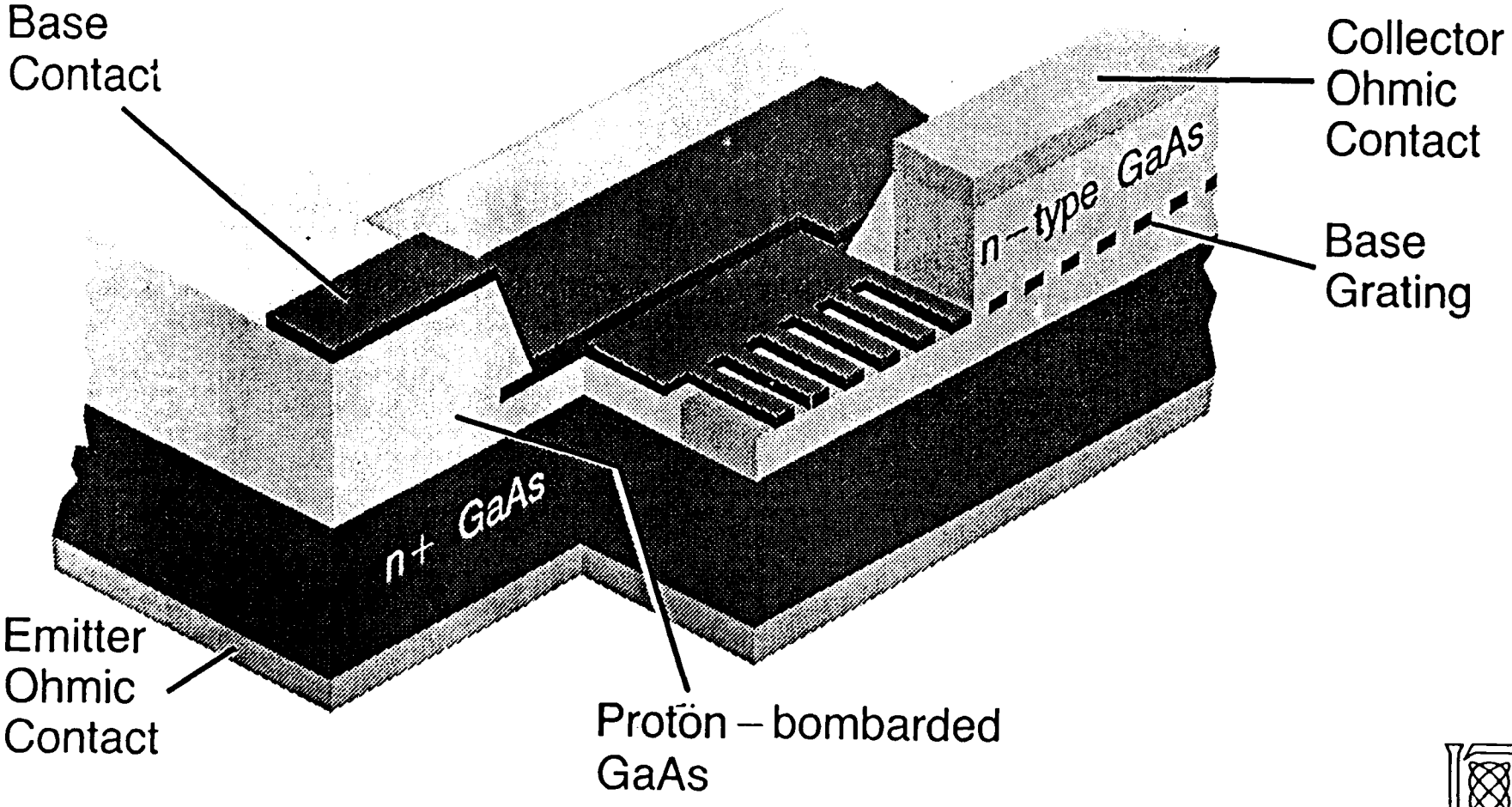
MARK A. HOLLIS

MIT LINCOLN LABORATORY

- PERMEABLE BASE TRANSISTOR
  - -- 94 GHz PERFORMANCE
  - -- PBTs ON SEMI-INSULATING SUBSTRATES
  - -- REDUCED-PERIODICITY PBT
  - -- PBT PERFORMANCE DATA
  - -- YIELD AND MANUFACTURABILITY
  - -- SUMMARY

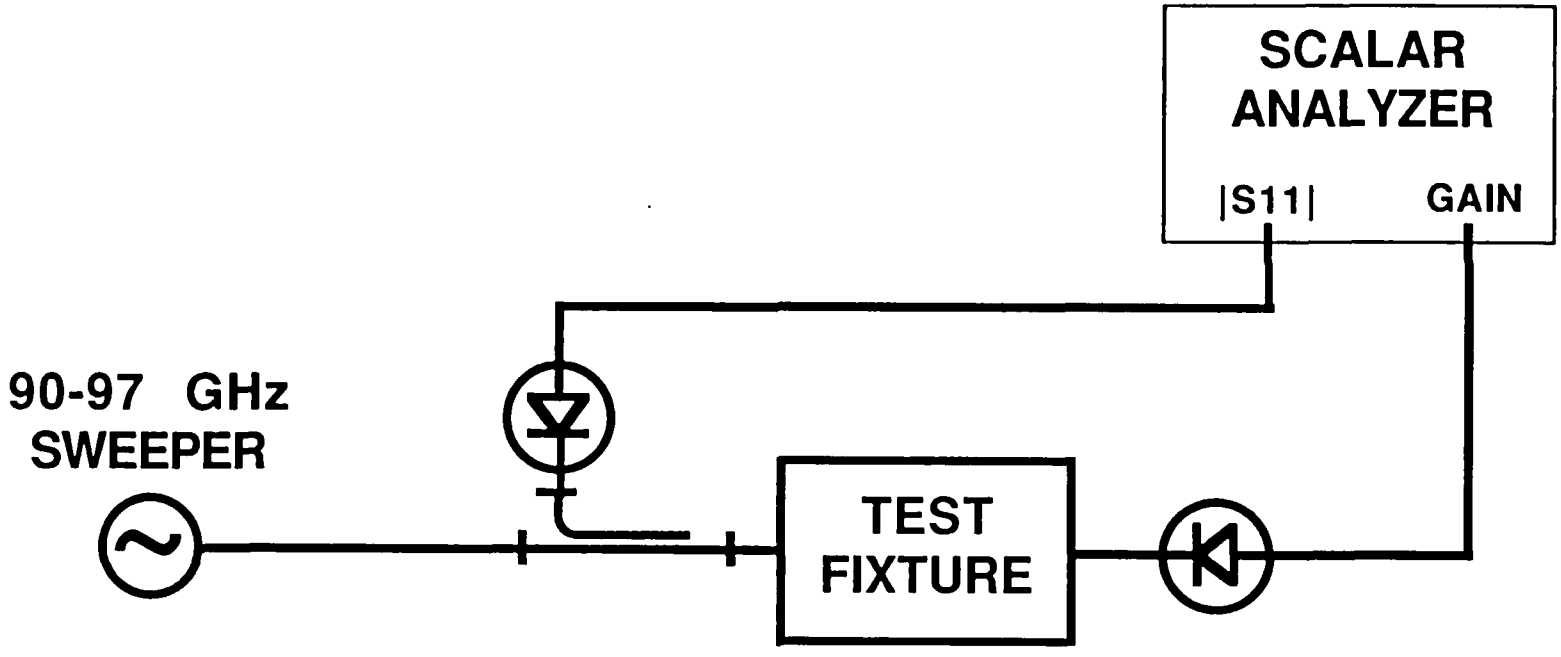
- REGROWTH FIELD-EFFECT TRANSISTOR
  - -- BASIC STRUCTURE
  - -- FABRICATION SEQUENCE
  - -- PROCESS DEVELOPMENT
  - -- SUMMARY

PERMEABLE BASE TRANSISTOR

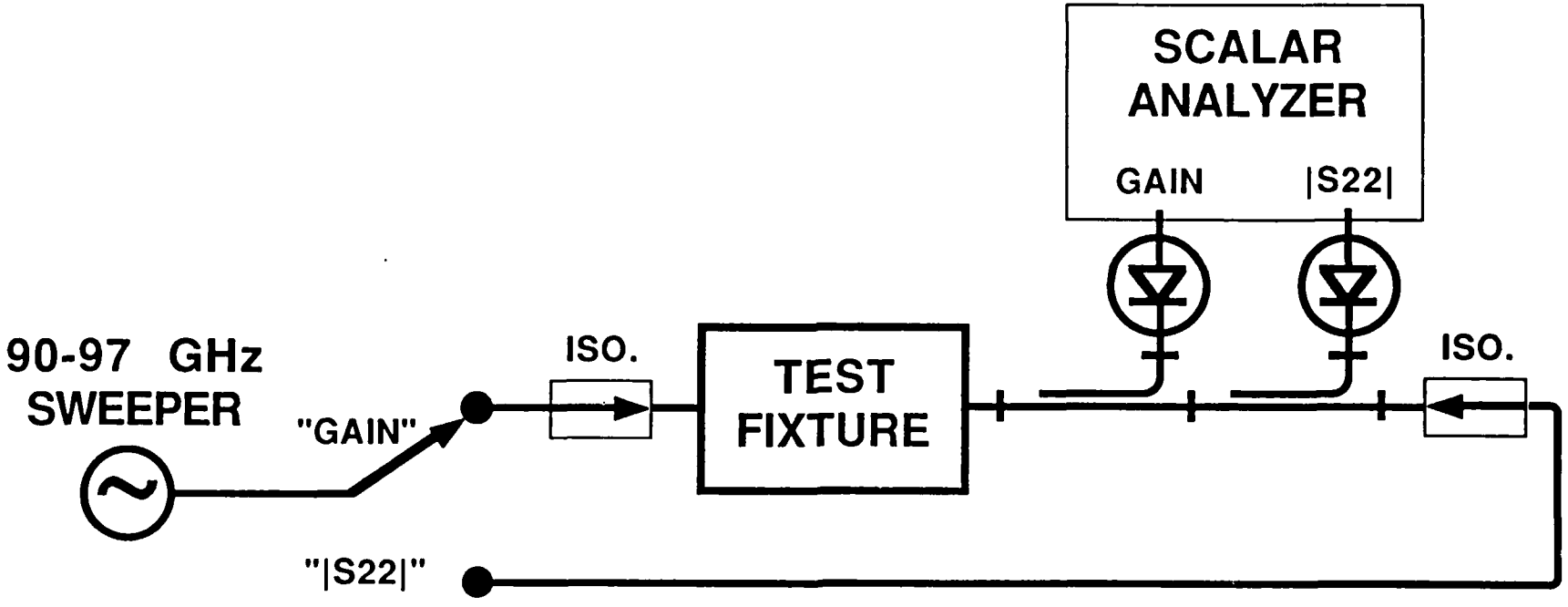


87 – 0766A

90-97 GHz Scalar Test Set

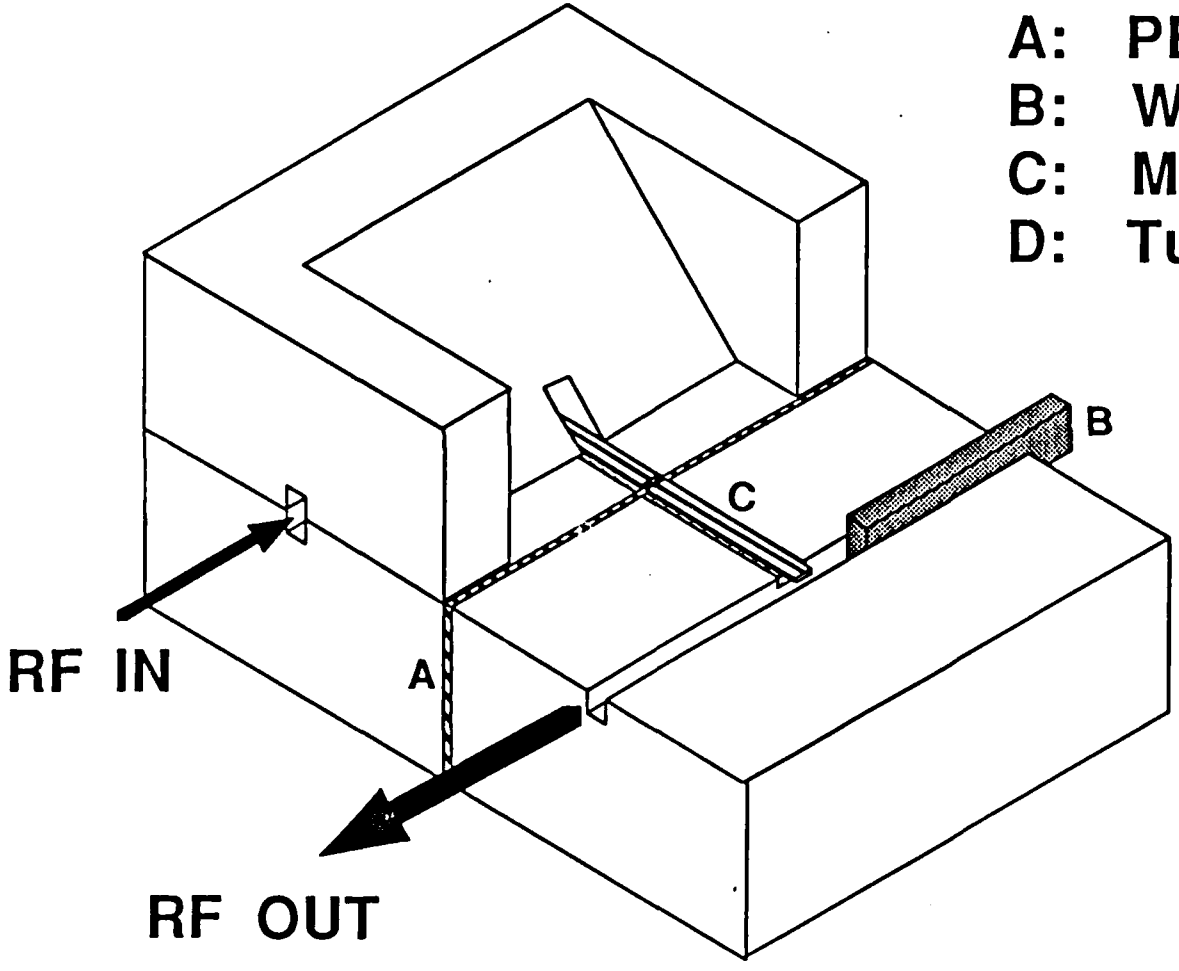


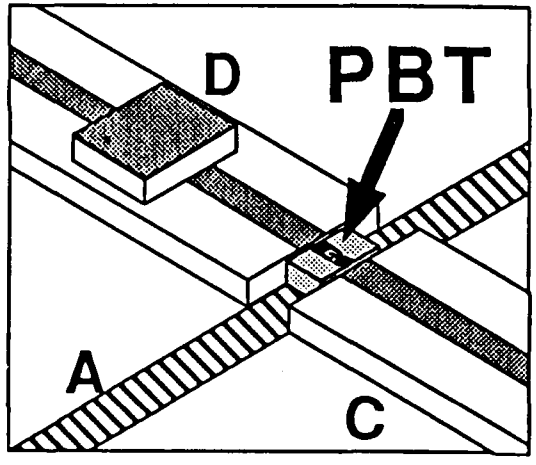
90-97 GHz Scalar Test Set

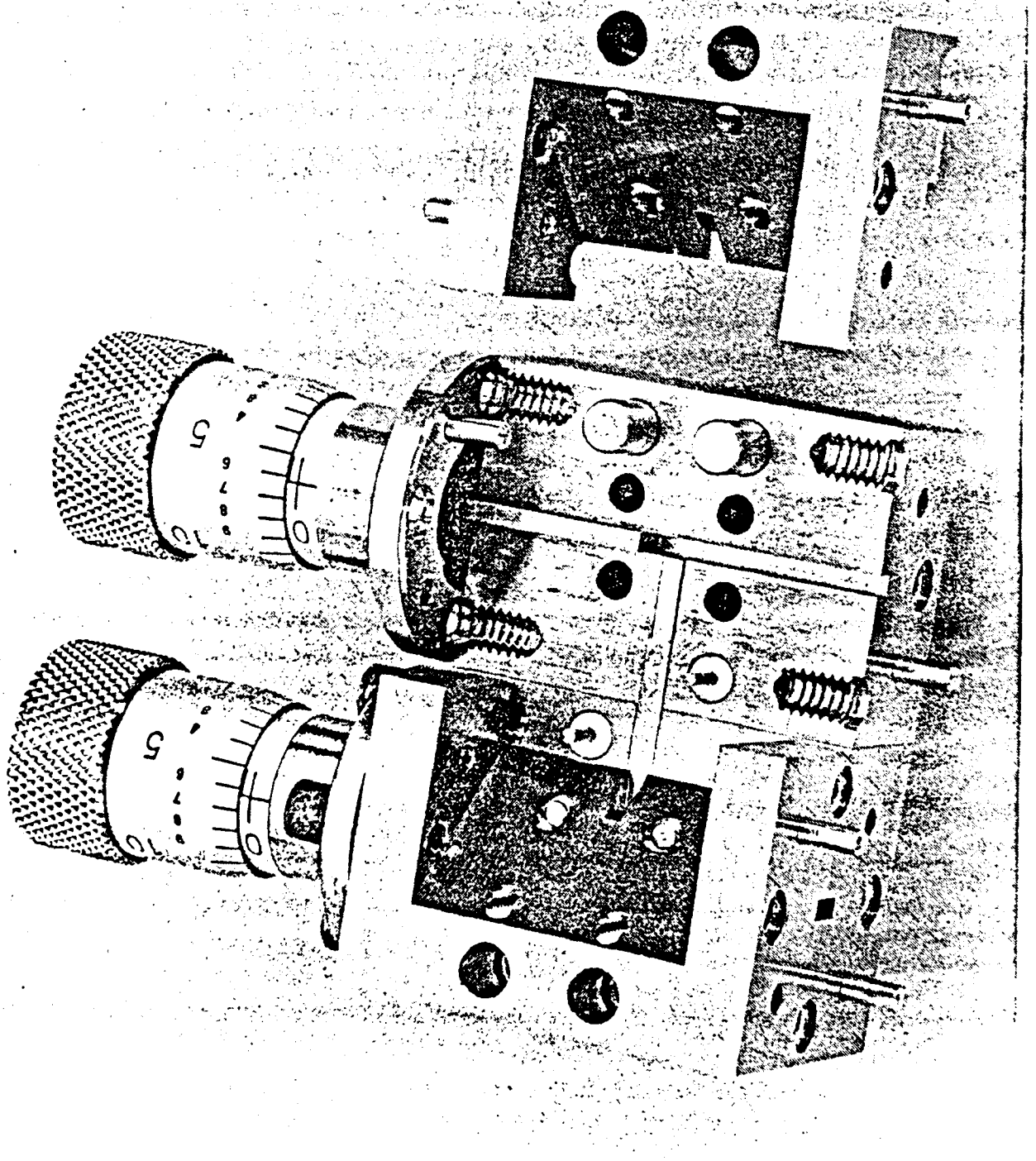


94-GHz Test Fixture

A: PBT Carrier
B: Waveguide Short
C: Microstrip Carrier
D: Tuning Chip

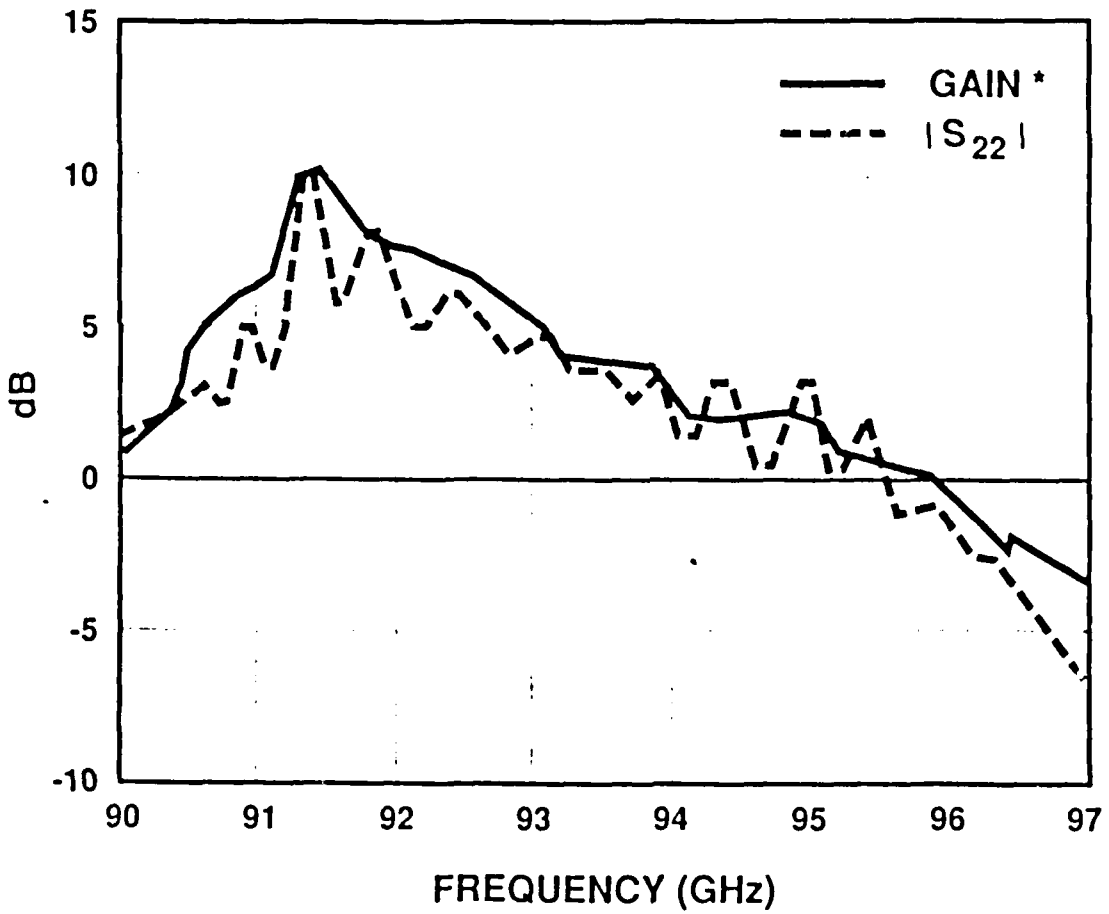






PBT SINGLE-STAGE HYBRID AMPLIFIER

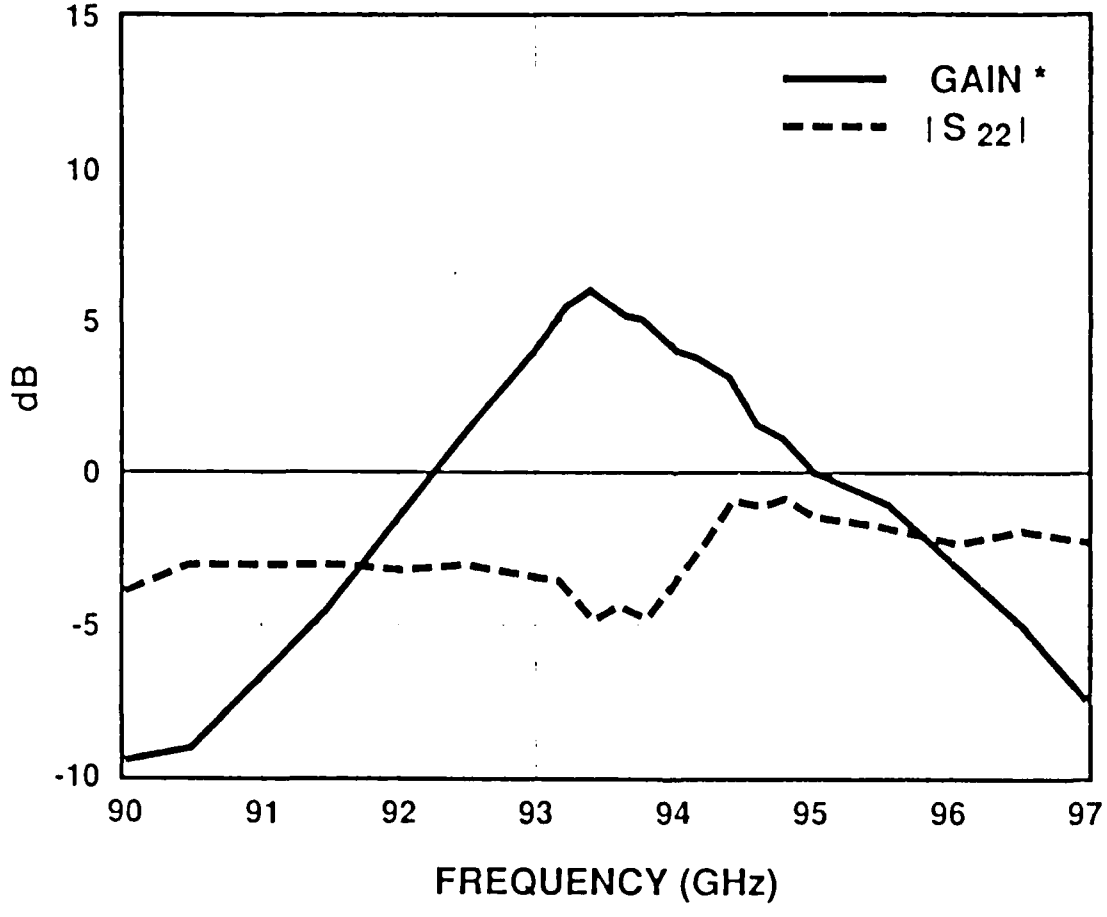
REGENERATIVE TUNING



* CORRECTED FOR FIXTURE LOSSES

PBT SINGLE-STAGE HYBRID AMPLIFIER

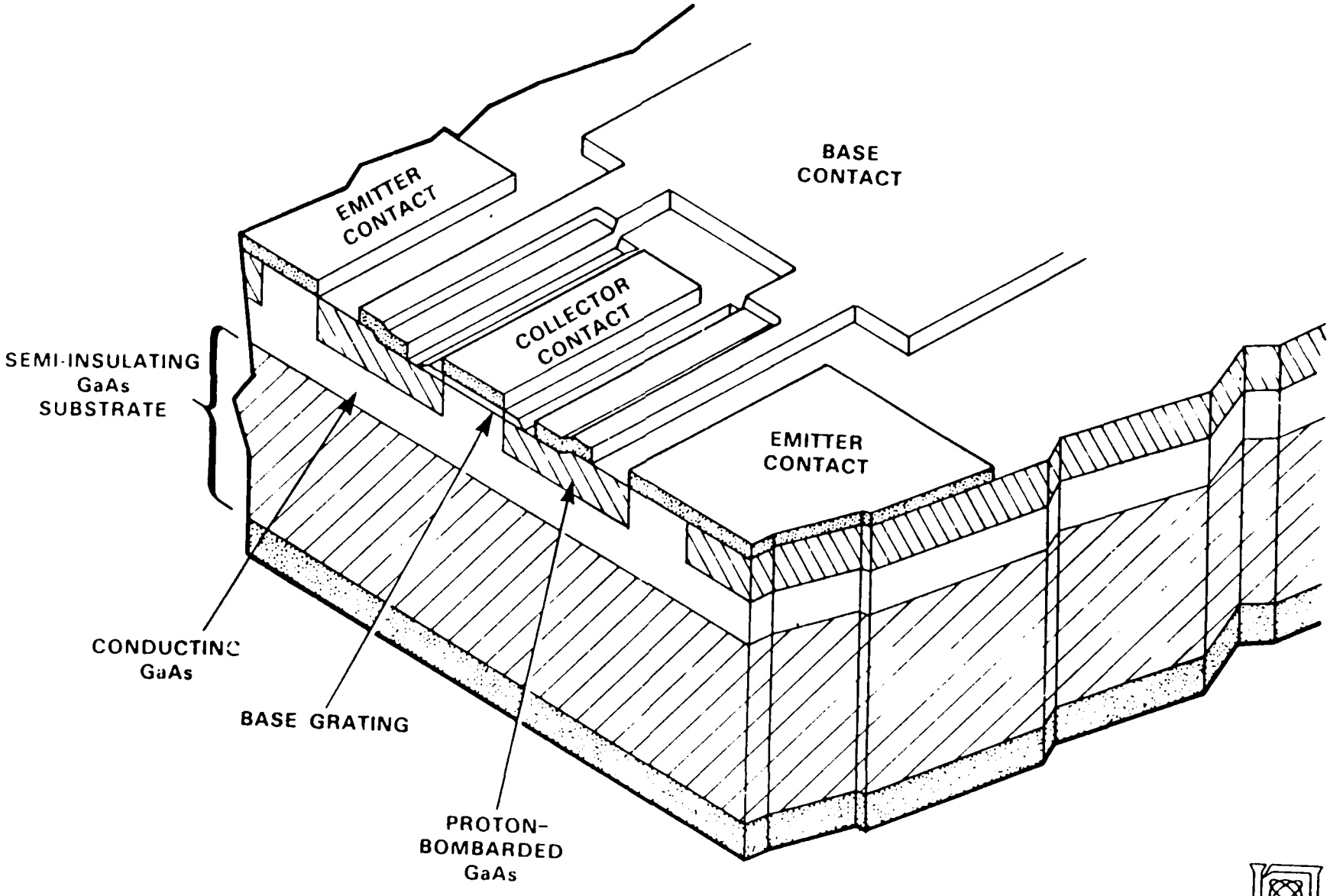
NON-REGENERATIVE TUNING



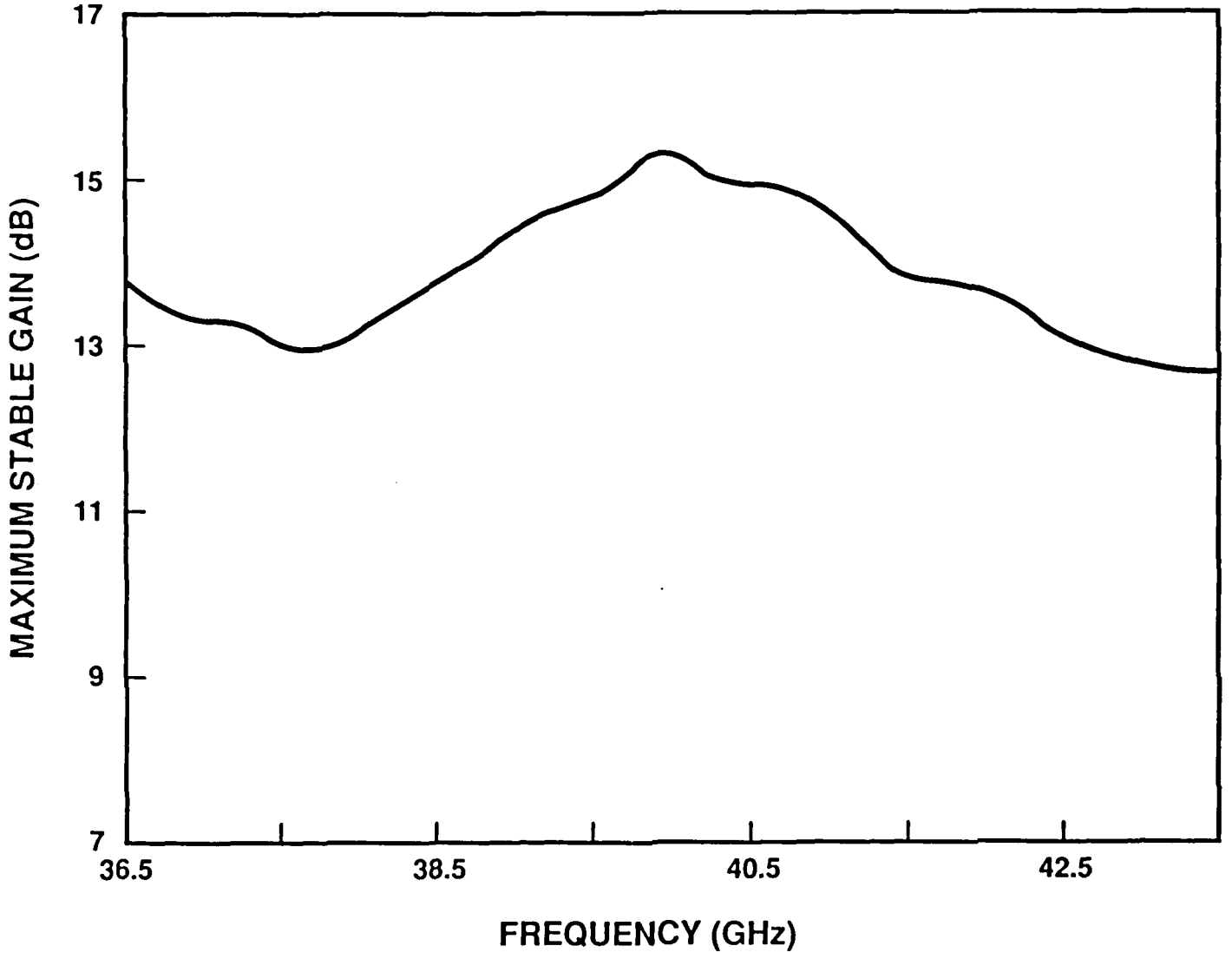
* CORRECTED FOR FIXTURE LOSSES

110930-2

PBT ON SEMI-INSULATING SUBSTRATE

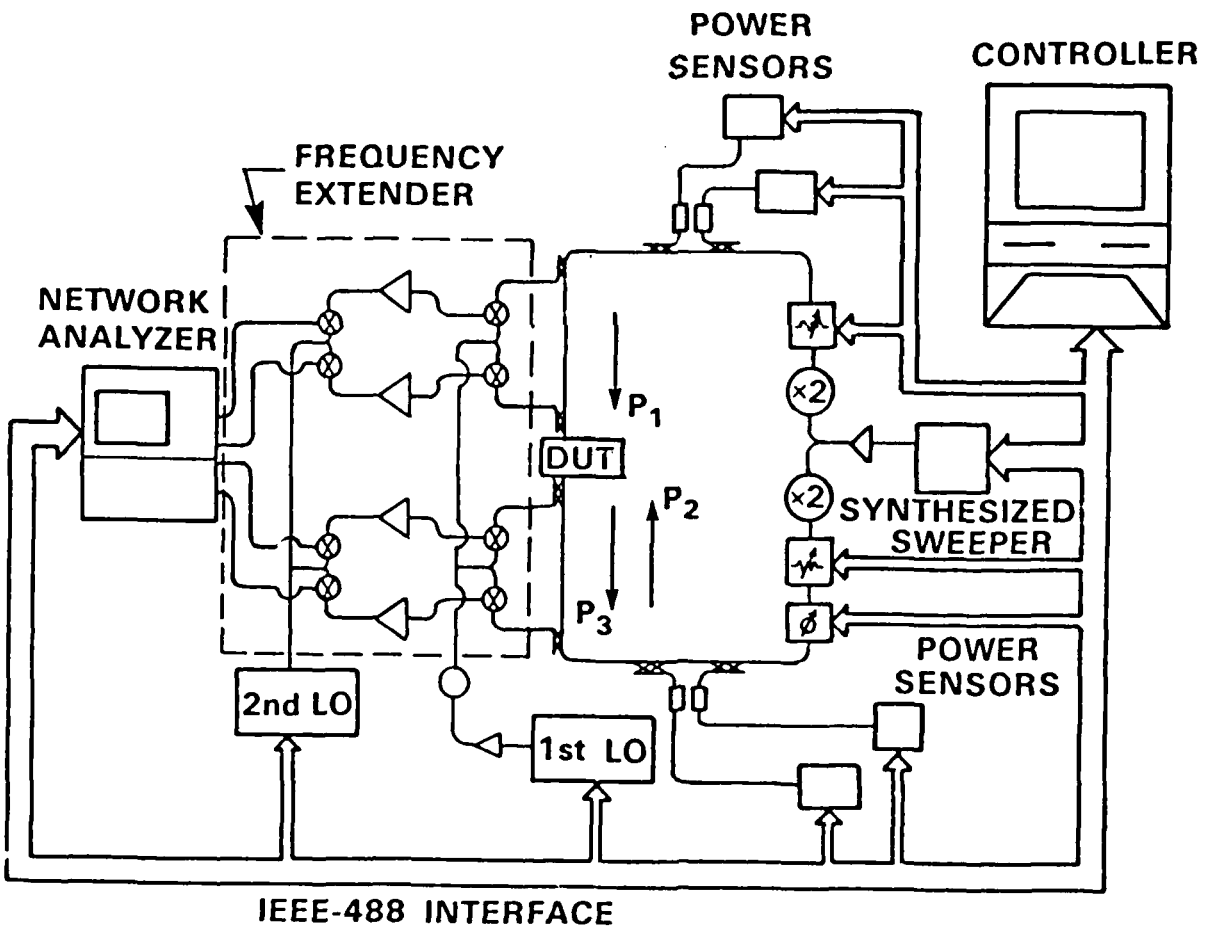


GAIN OF PBT ON SEMI-INSULATING SUBSTRATE



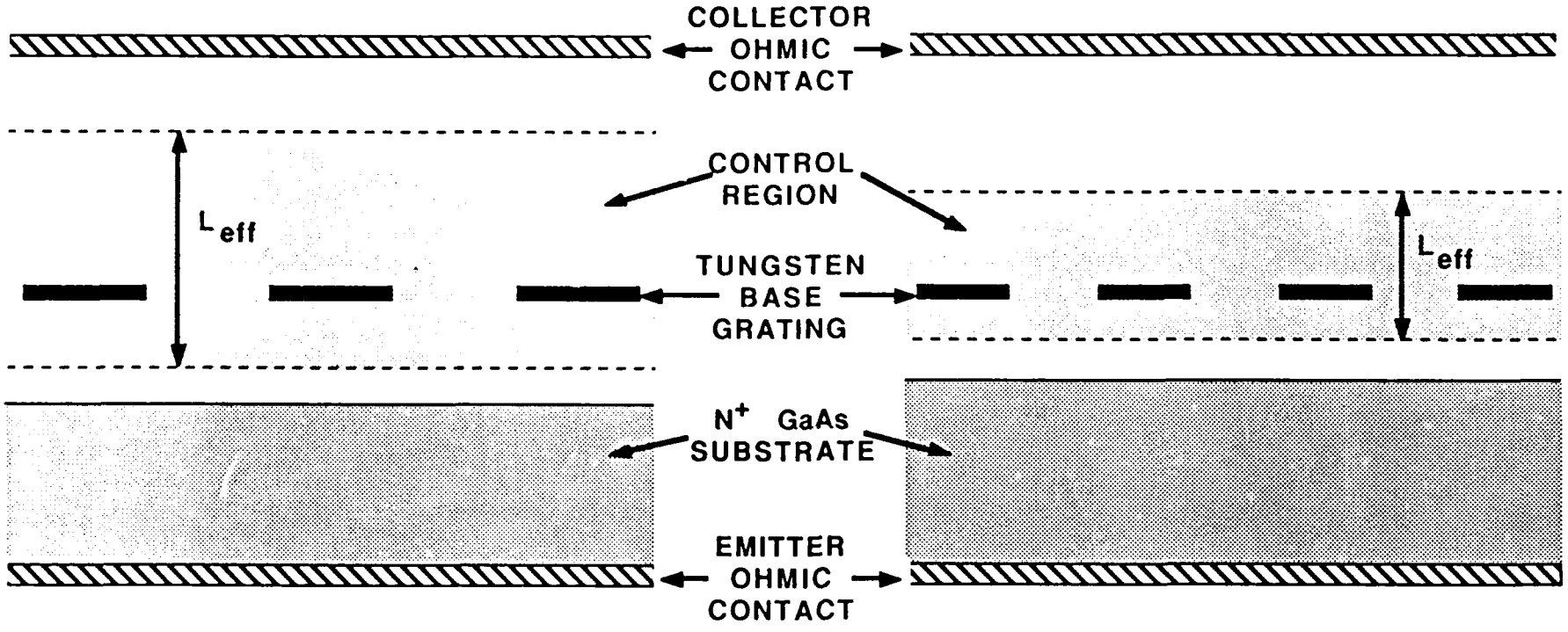
115426-1

EHF ACTIVE LOAD-PULL MEASUREMENT SYSTEM



109035-1

BENEFITS OF REDUCED-PERIODICITY GaAs PBT



STANDARD-PERIODICITY PBT

REDUCED-PERIODICITY PBT

$$f_T = \frac{g_m}{2\pi (C_{BE} + C_{BC})} = \frac{\langle v \rangle}{2\pi L_{eff}}$$

$$f_{max} = \frac{f_T}{2\sqrt{\frac{R_B + R_E}{R_O} + \frac{R_B g_m C_{BC}}{C_{BE} + C_{BC}}}}$$

PBT PERFORMANCE

- 7.5 dB GAIN AT 92 GHz IN A REGENERATIVELY TUNED AMPLIFIER
- 6 dB GAIN AT 93.5 GHz IN A NONREGENERATIVE AMPLIFIER
- 15 dB MAXIMUM STABLE GAIN AT 40 GHz FROM A PBT ON A SEMI-INSULATING SUBSTRATE
- 20.1 dB MAXIMUM STABLE GAIN AT 26.5 GHz
- EXTRAPOLATED f_{max} OF 265 GHz
- EXTRAPOLATED f_T OF 40 GHz
- 5-GHz SIGNAL SAMPLED WITH PBT TRACK-AND-HOLD CIRCUIT

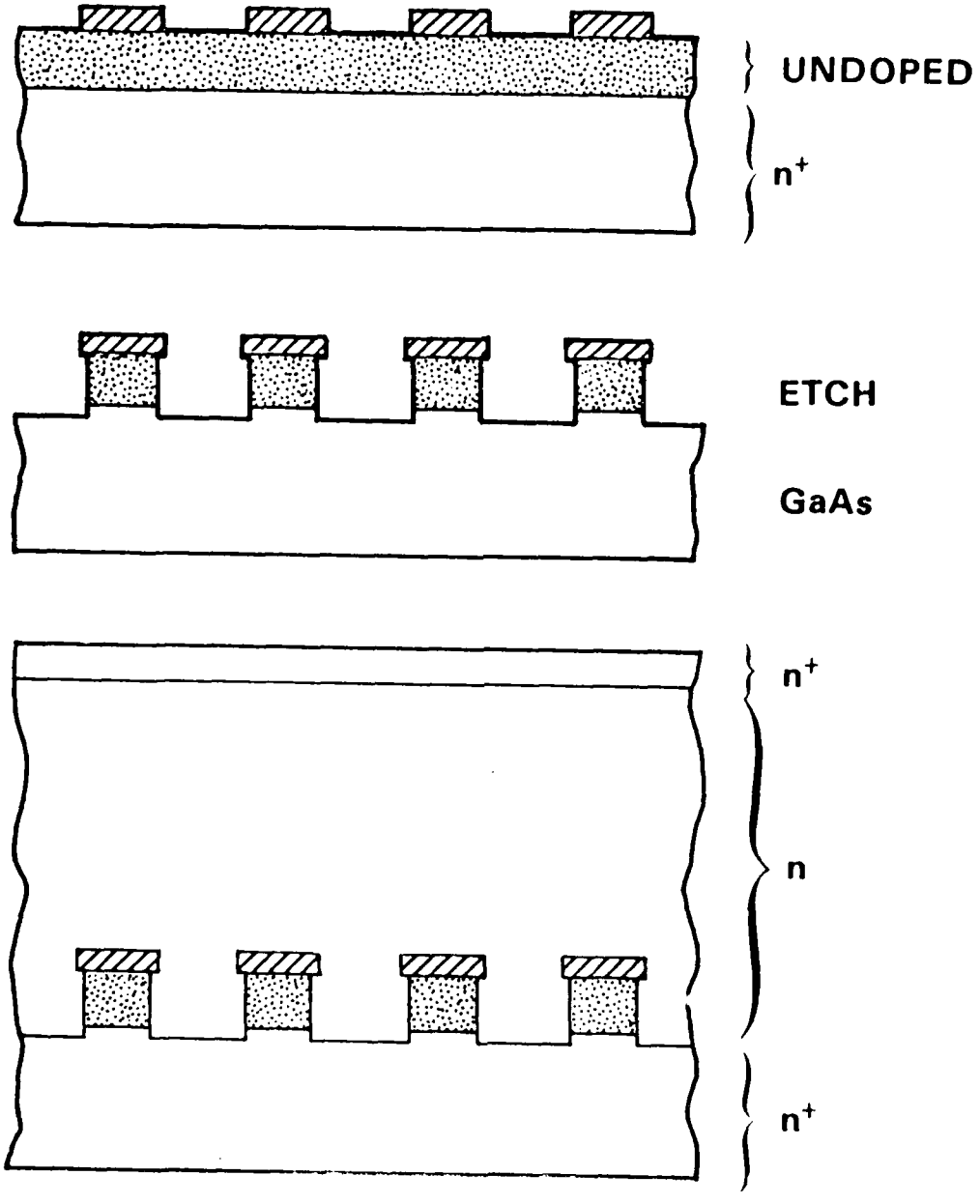
PBT POWER DATA

FREQUENCY (GHz)	1.3	1.3	22	22
POWER (mW)	100	1000	501	83
$\eta_{POWER-ADDED}$	66%	35%	30%	45%
GAIN (dB)	15	19	5.0	6.2
CLASS	AB	A	AB	AB

ADVANCED STRUCTURES

- PBTs HAVE DEMONSTRATED f_{max}/f_T ratios of 7:1
  - -- LOW PARASITICS, HIGH OUTPUT IMPEDANCE
  - -- DOUBLING $f_T \Rightarrow f_{max} \geq 500$ GHz
- STRUCTURES FOR ENHANCED f_T:
  - -- ETCHED-EMITTER PBT
  - -- REDUCED-PERIODICITY PBT
  - -- MODIFIED STRUCTURES AND DOPING PROFILES
  - -- REGROWTH FET

PBT WITH MODIFIED PROFILE

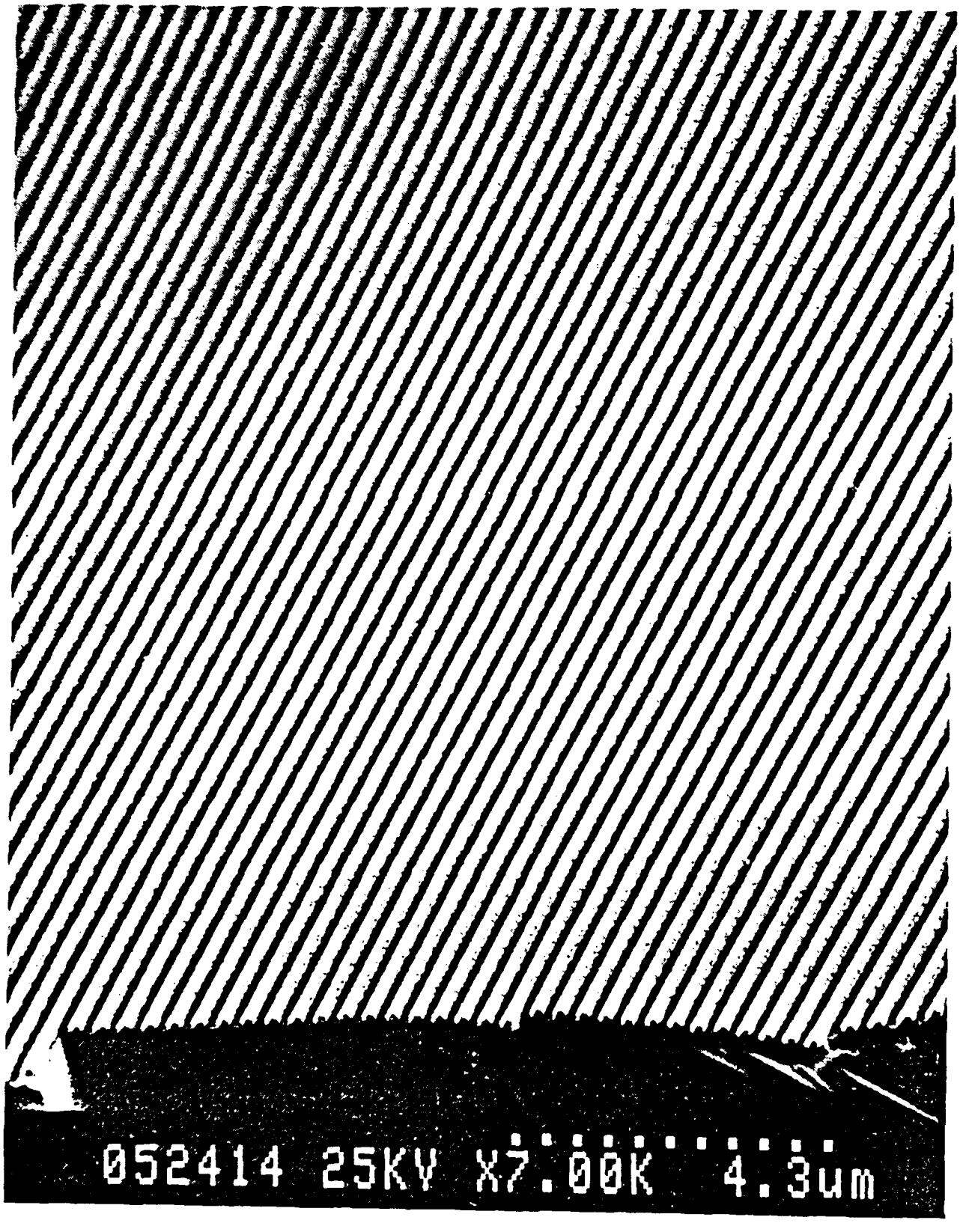


95694 2

PBT DEVICE YIELD

Wafer	YIELD (ALL BUT SHORTS & OPENS)	σ (I_{DSS})	σ (g_m)
VC2	89 %	21 %	14.4 %
SP1	93 %	17.6 %	21 %

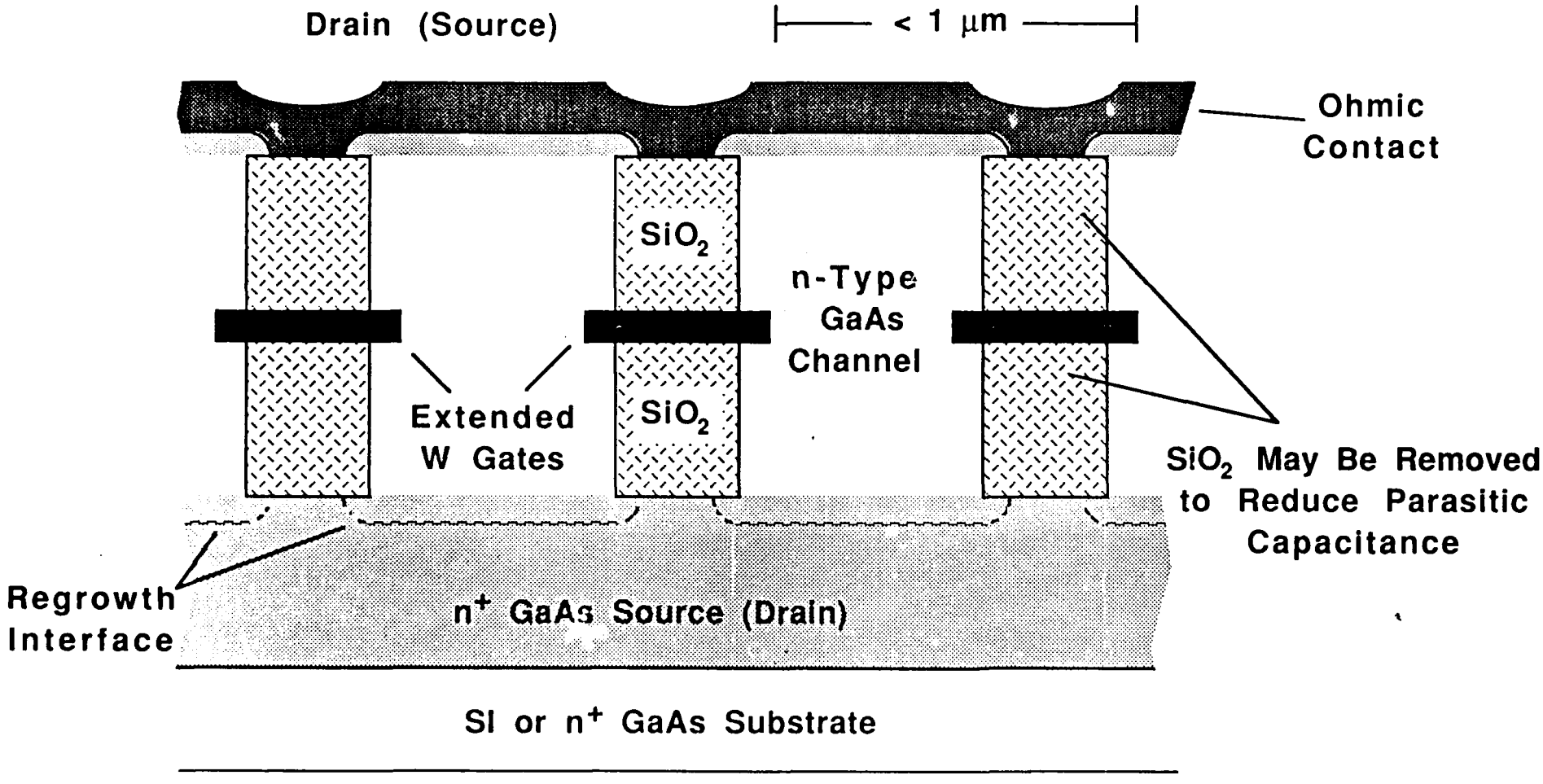
Wafer	YIELD (ALL WITHIN 10 % OF $\overline{I_{DSS}}$, $\overline{g_m}$)	σ (I_{DSS})	σ (g_m)
VC2	57 %	5.4 %	6 %
SP1	45.6 %	7.9 %	6.7 %


052414 25KV X7.00K 4.3um

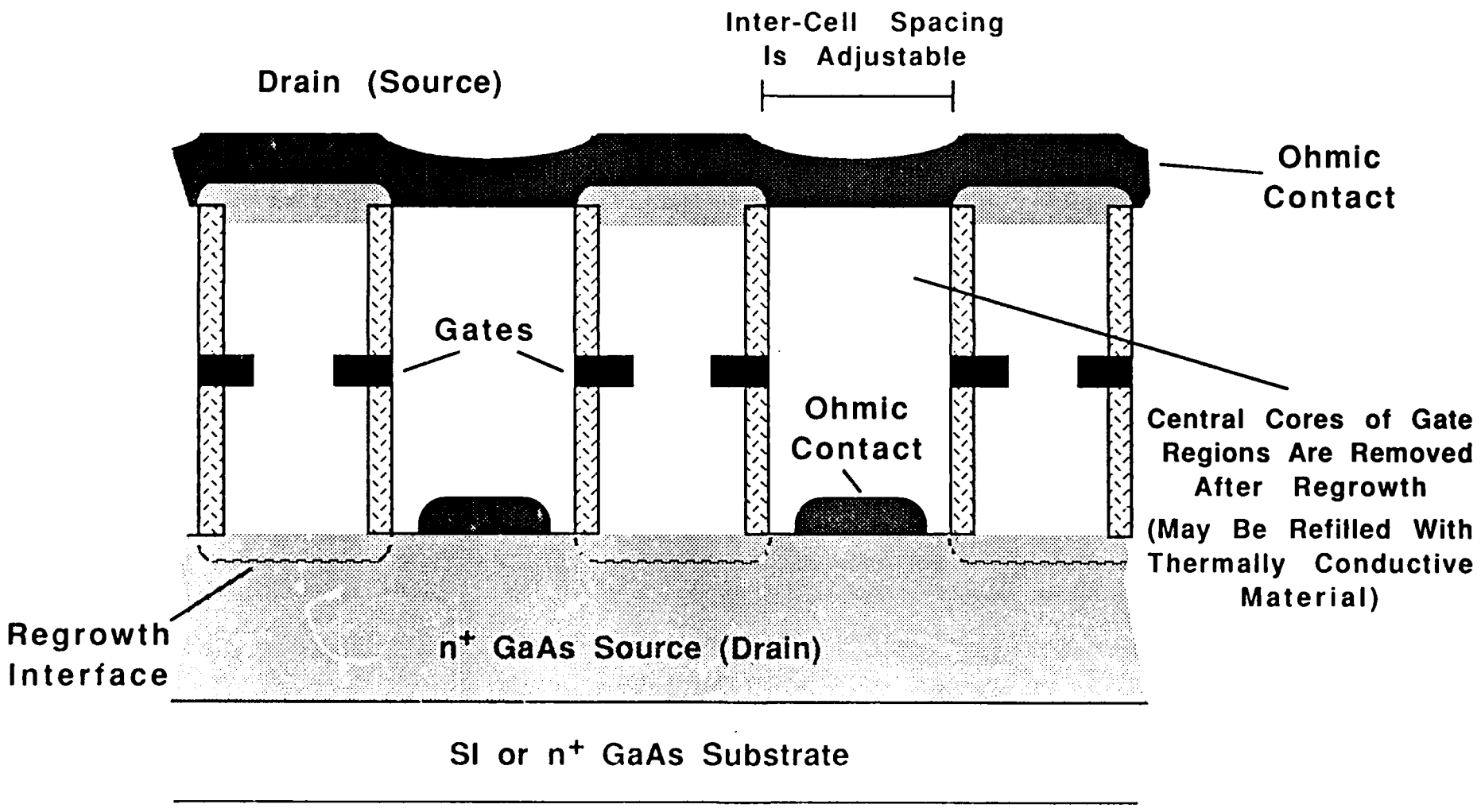
PBT SUMMARY

- PBTs HAVE DEMONSTRATED HIGH PERFORMANCE AT EHF
- HIGH-PERFORMANCE PBTs HAVE BEEN FABRICATED ON SEMI-INSULATING GaAs SUBSTRATES
- PBTs CAN BE FABRICATED ACROSS A FULL GaAs WAFER BY A HiGH-YIELD MANUFACTURING PROCESS
- ONGOING CIRCUIT EFFORTS AT
  - -- 22 GHz
  - -- 40 GHz
  - -- 94 GHz
- ADVANCED STRUCTURES

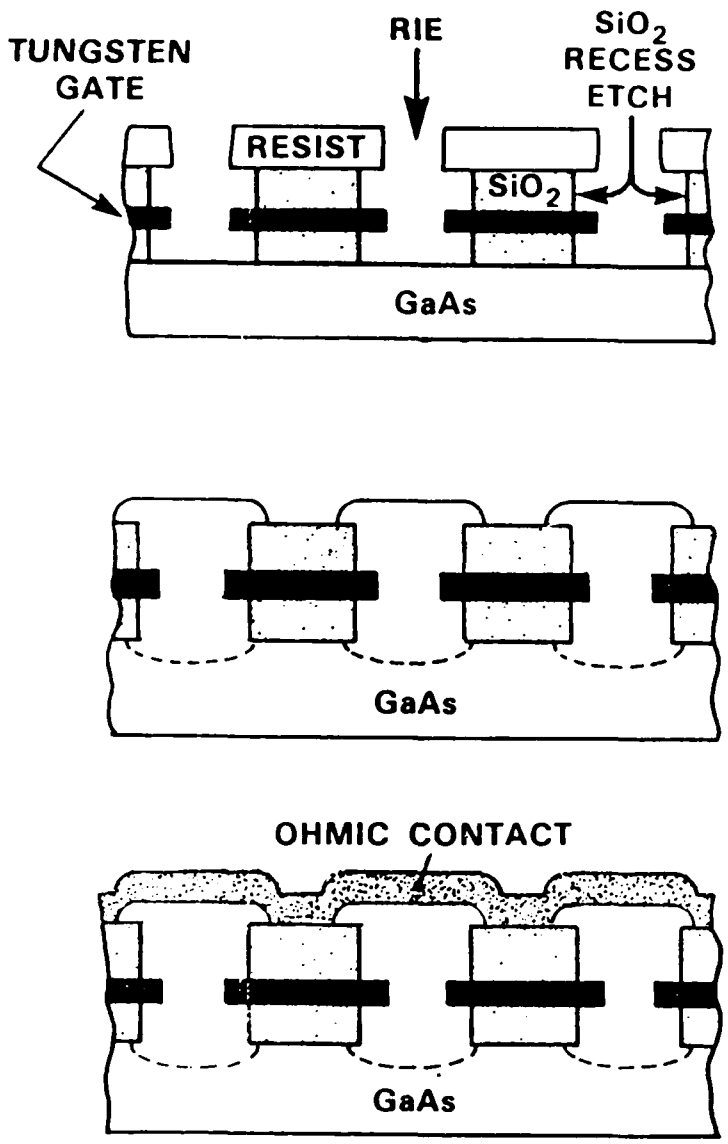
REGROWTH FET
(STANDARD DESIGN)



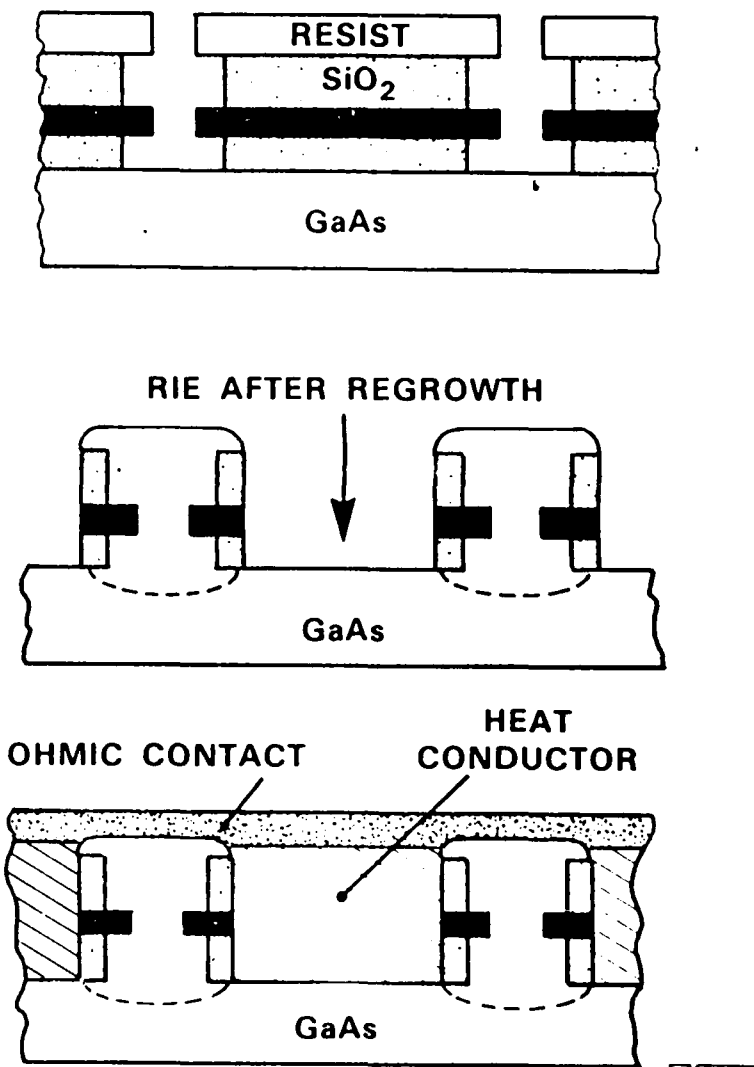
REGROWTH FET
(THERMAL DESIGN)



METHODS OF FABRICATING REGROWTH FET



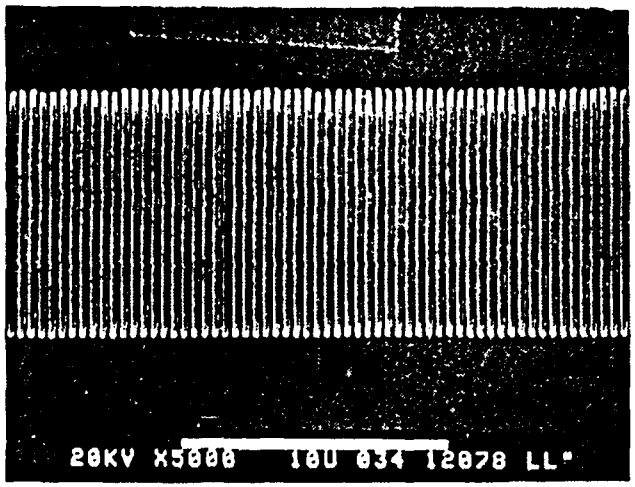
STANDARD DESIGN

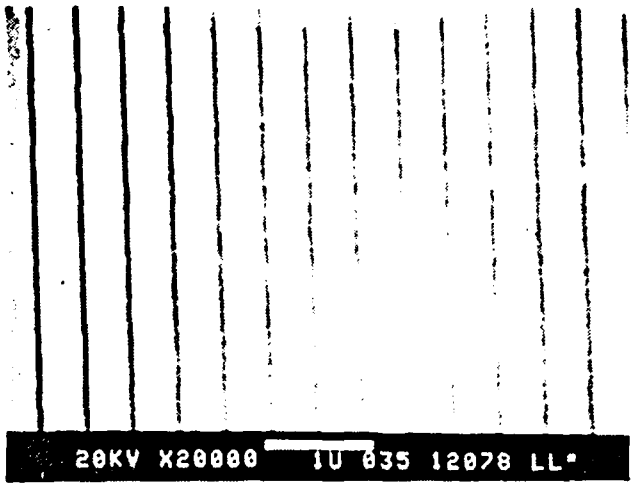


THERMAL DESIGN

95947-1

RFET GRATINGS FABRICATED USING ELECTRON-BEAM LITHOGRAPHY





115553-1

RFET AFTER SiO_2 RECESS ETCH

115665-1

REGROWTH FET SUMMARY

- REGROWTH FET ADVANTAGES:
  - -- HIGH SPEED
  - -- DESIGN FLEXIBILITY
  - -- THERMAL MANAGEMENT $\Rightarrow$ HIGH POWER
- PROTRUDING-GATE PROCESS FULLY DEVELOPED
- VIABILITY OF ELECTRON-BEAM LITHOGRAPHY SHOWN
- STUDY OF GaAs CRYSTAL GROWTH AROUND PROTRUDING GATES UNDERWAY
- DEVICE WAFERS FABRICATED USING PBT CRYSTAL GROWTH PARAMETERS

Transport Considerations for EHF Devices

H. L. Grubin

Scientific Research Associates
Glastonbury, CT

TRANSPORT CONSIDERATIONS FOR EHF DEVICES
SCIENTIFIC RESEARCH ASSOCIATES

PROGRAM OBJECTIVE

- USE NUMERICAL SIMULATION TO ASSIST IN THE DESIGN OF HIGH FREQUENCY AND HIGH SPEED SEMICONDUCTOR DEVICES
- DETERMINE REALISTIC GOALS FOR HIGH SPEED APPLICATIONS

PROGRAM APPROACH

- NUMERICALLY SOLVE TRANSIENT SEMICONDUCTOR DRIFT AND DIFFUSION EQUATIONS
- NUMERICALLY SOLVE MOMENTS OF BOLTZMANN EQUATION FOR SUBMICRON DEVICES
- NUMERICALLY IMPLEMENT MONTE CARLO PROCEDURES FOR MATERIAL CHARACTERIZATION
- ONGOING INTERACTION WITH DEVICE DESIGNERS

PROGRAM STATUS

- ACHIEVED LARGE SIGNAL PBT GAIN IN EXCESS OF 7 db AT 40 GHz AND 11 db AT 20 GHz
- ACHIEVED INDIUM BASED HBT GAINS SIGNIFICANTLY LARGER THAN GALLIUM ARSENIDE BASED HBT'S

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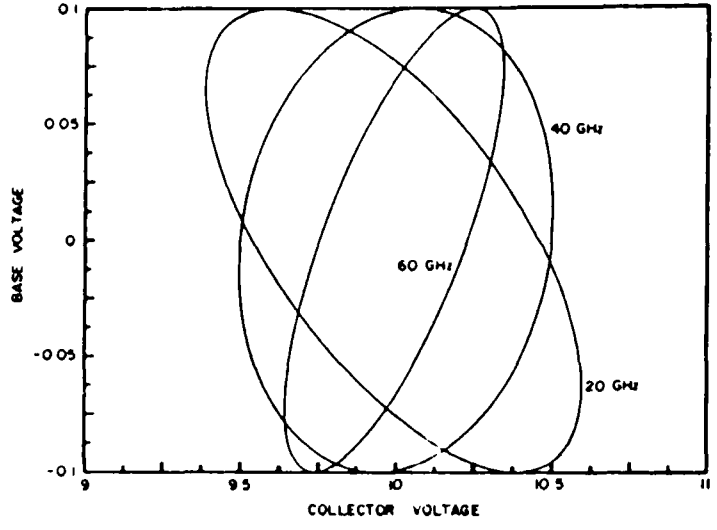
BASE vs. COLLECTOR VOLTAGE LISSAJOUS



CONTRIBUTORS

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MEYYA MEYYAPPAN

BEVERLY MORRISON

MOHAMED OSMAN

HAROLD GRUBIN

Scientific Research Associates

- DESIGN OF GaAs PBT's

- DESIGN OF COMPOUND SEMICONDUCTOR HBT'S

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PBT STUDIES

DESIGN PBT STRUCTURES FOR

- HIGH POWER
- HIGH GAIN
- HIGH POWER ADDED EFFICIENCY

NEED LARGE SIGNAL CALCULATIONS

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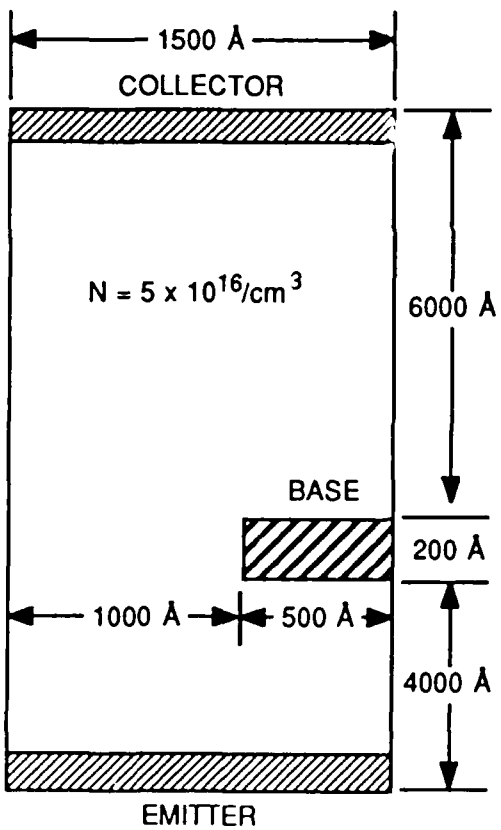
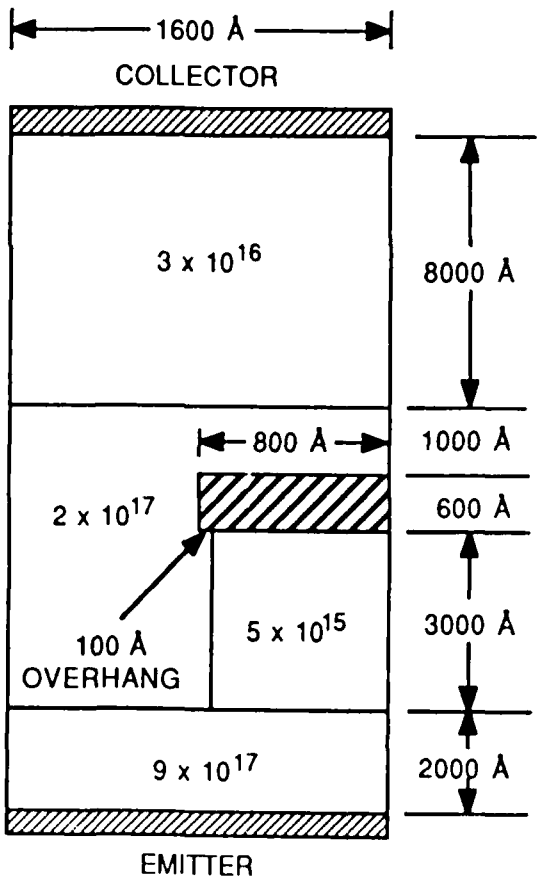
PBT STRUCTURES

UNIFORM DOPING



NONUNIFORM DOPING



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WHAT IS THE RELATIONSHIP BETWEEN LARGE AND SMALL SIGNAL CALCULATIONS AND BY SMALL SIGNAL WE MEAN THAT SUCH QUANTITIES AS THE CUT-OFF FREQUENCY AND f_{max} ARE RELEVANT.

- OUR LATEST CALCULATIONS INDICATE THAT ANY CONNECTION BETWEEN CUT-OFF FREQUENCY AND LARGE SIGNAL OPERATION MAY BE COINCIDENTAL.

- THIS IMPLIES THAT THE DESIGN OF A DEVICE FOR HIGH CUT-OFF FREQUENCY OPERATION WILL NOT NECESSARILY YIELD SATISFACTORY OR IMPROVED LARGE SIGNAL POWER OPERATION.

- RECALL THAT SMALL SIGNAL OPERATION IMPLIES SMALL PERTURBATIONS ABOUT A RECOGNIZABLE INPUT.

  THE NEXT TWO VIEWGRAPHS ILLUSTRATE THE EXTENT TO WHICH THIS ASSUMPTION IS VALID.

- THE APPROACH TAKEN IS TO ASSUME THAT THE PBT IS CONNECTED TO A DC COLLECTOR POWER SUPPLY THROUGH THE EXTERNAL CIRCUIT.

- THE CALCULATIONS ARE CONCERNED WITH DETERMINING THE POWER DELIVERED TO THIS EXTERNAL CIRCUIT.

- THE EXTERNAL CIRCUIT, BY CONTROLLING THE RELATIVE PHASE OF THE BASE AND COLLECTOR VOLTAGE, EXERTS FIRST-ORDER EFFECTS ON THE OUTPUT OF THE DEVICE.

- BASIC REQUIREMENT FOR POWER FETs AND PBTs IS THAT DECREASES IN BASE VOLTAGE SHOULD BE ACCOMPANIED BY LARGE INCREASES IN COLLECTOR VOLTAGE.

  THIS IS ALWAYS SATISFIED AT LOW FREQUENCY CONDITIONS BUT IS NOT SATISFIED, WITHOUT EXTERNAL ADJUSTMENTS AT HIGH FREQUENCIES.

- SUBSEQUENT CALCULATIONS REVEAL THESE FEATURES.

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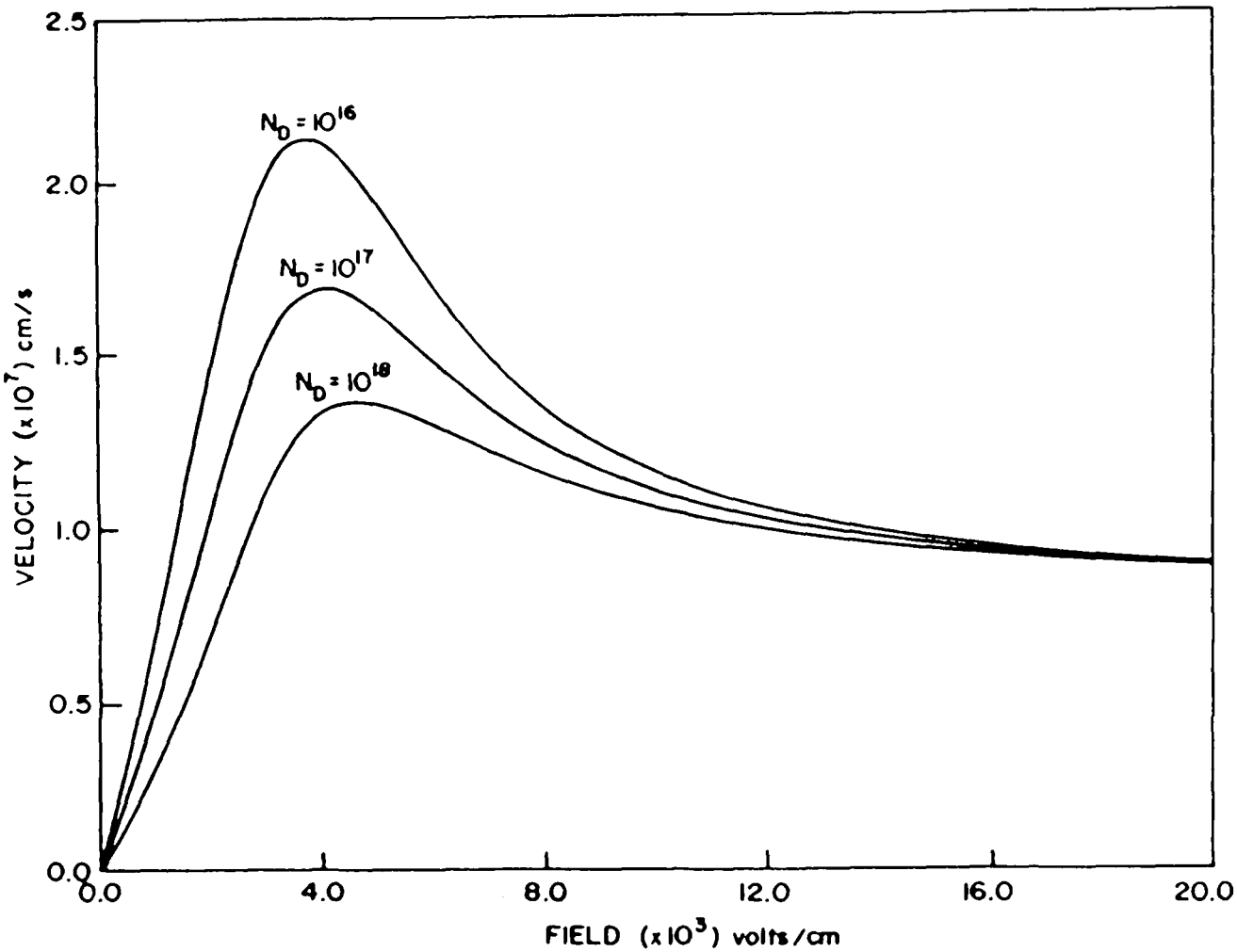
VELOCITY-FIELD CURVE FOR GaAs



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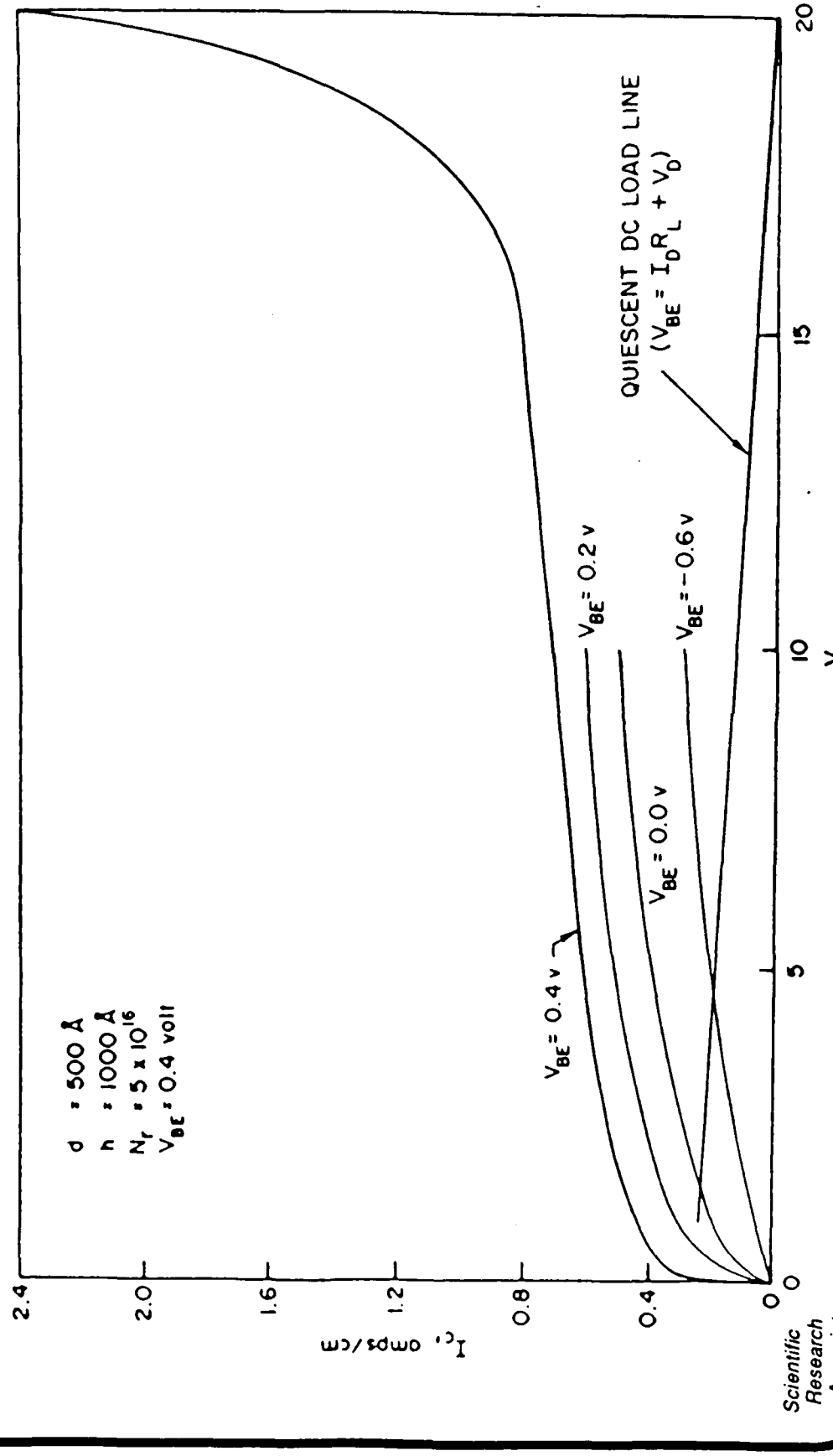
ORDER OF THE CALCULATIONS

- DC CALCULATIONS AND SMALL SIGNAL CHARACTERIZATION
- LARGE SIGNAL RESISTIVE CIRCUIT CALCULATIONS
- LARGE SIGNAL REACTIVE CIRCUIT CALCULATIONS WHERE THE CIRCUIT FREQUENCY IS BELOW AND ABOVE THE DRIVING FREQUENCY

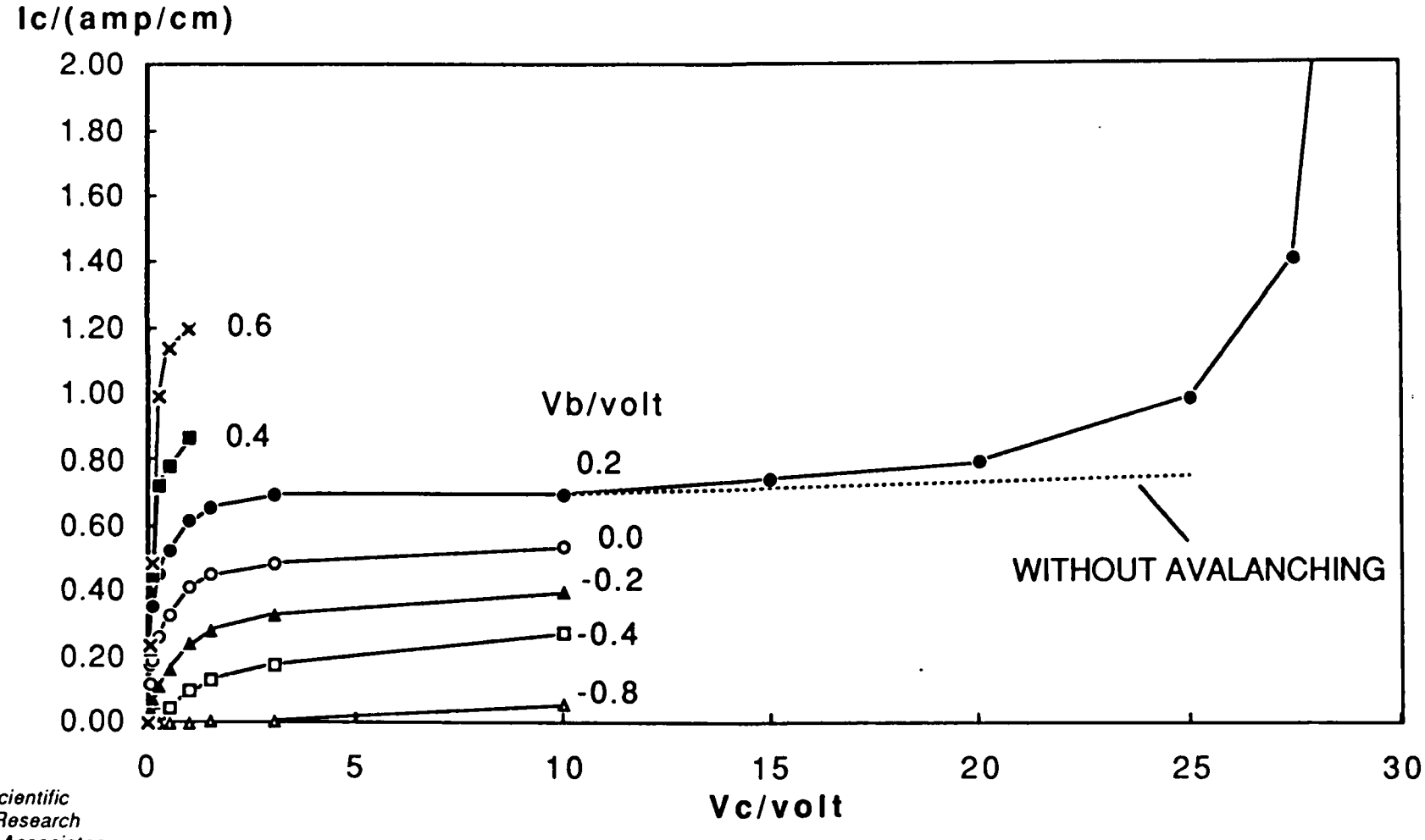
SELECT DC CHARACTERISTICS / BREAKDOWN CURVE

UNIFORMLY DOPED PBT



SELECT DC CHARACTERISTICS / BREAKDOWN CURVE

NONUNIFORMLY DOPED PBT



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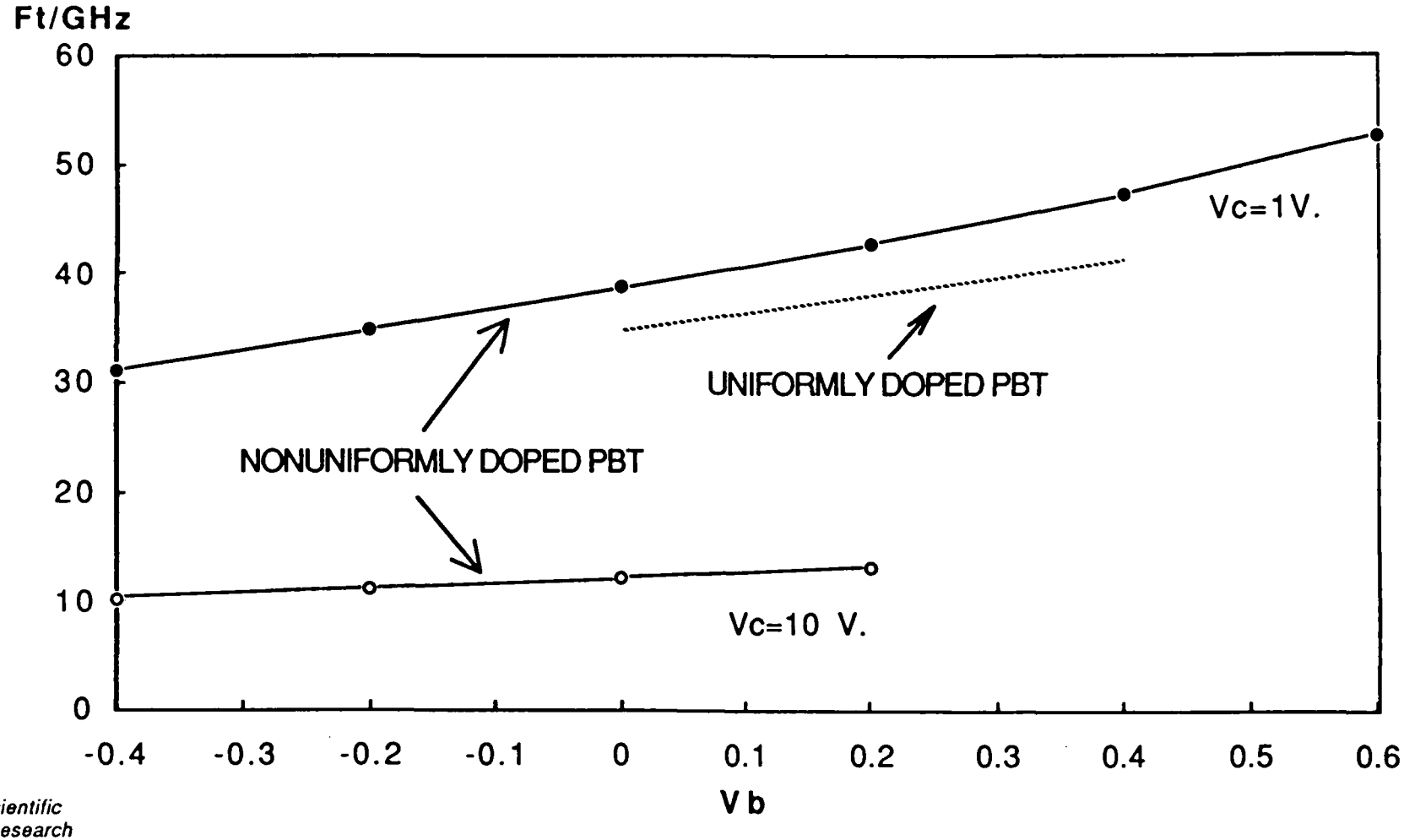
f_T DEPENDENCE ON BIAS



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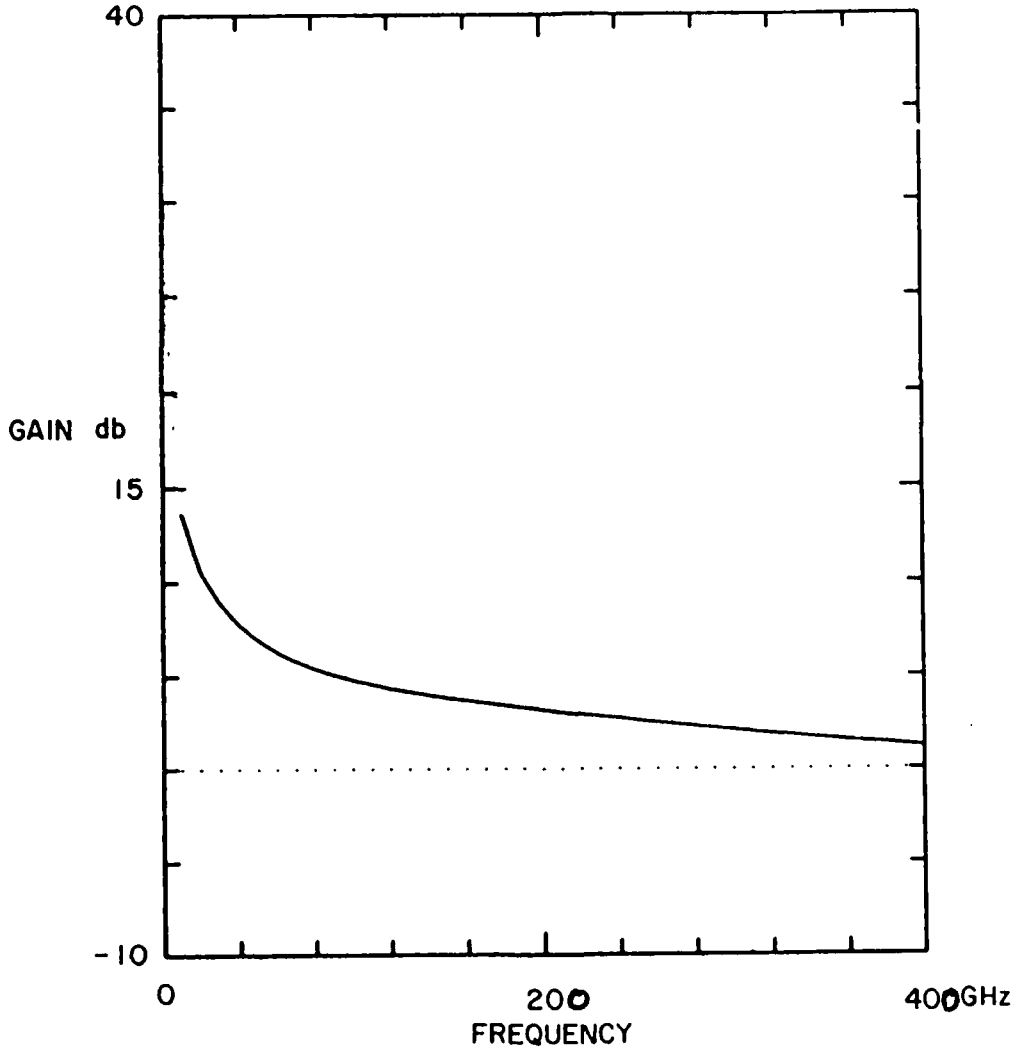
MAXIMUM STABLE GAIN
NONUNIFORM PBT $V_C = 1.0, V_B = 0.2$



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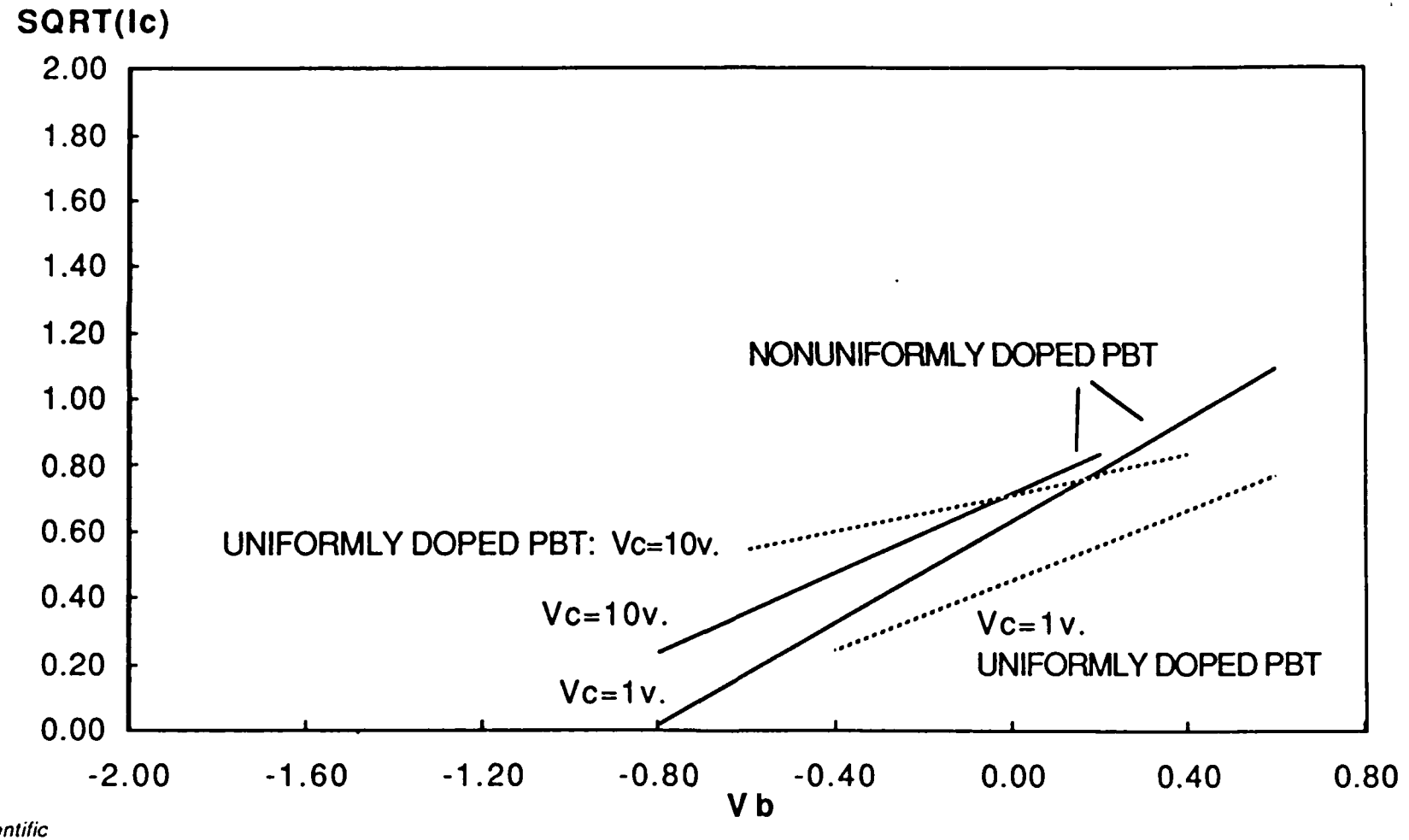
THRESHOLD VOLTAGE DEPENDENCE ON BIAS



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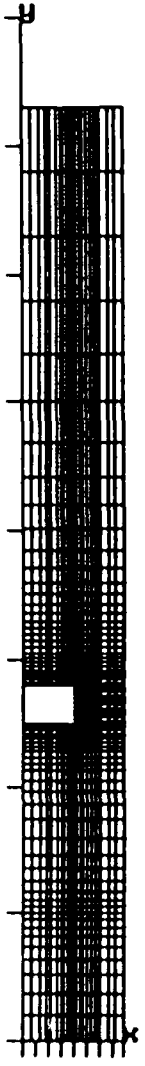
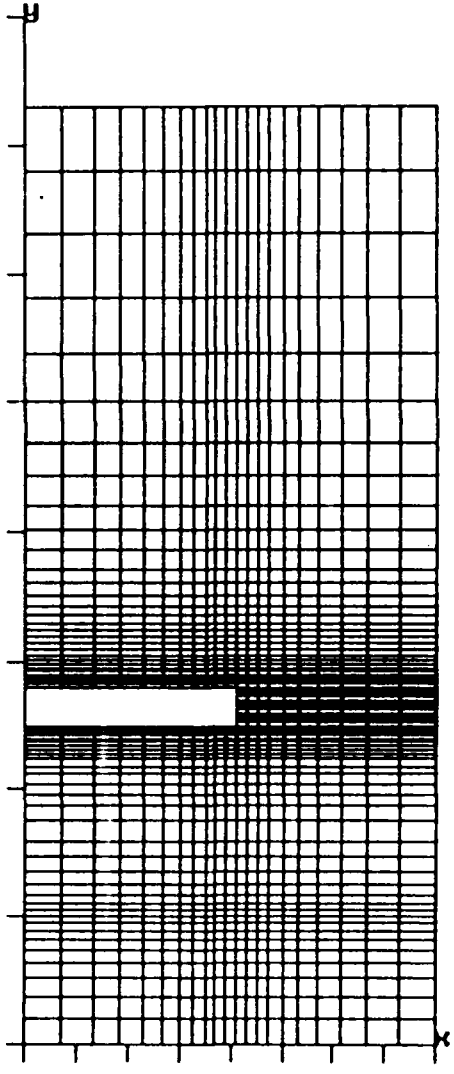
ACTUAL SHAPE

GRID 22 x 80



SHAPE USED IN CONTOUR PLOTS



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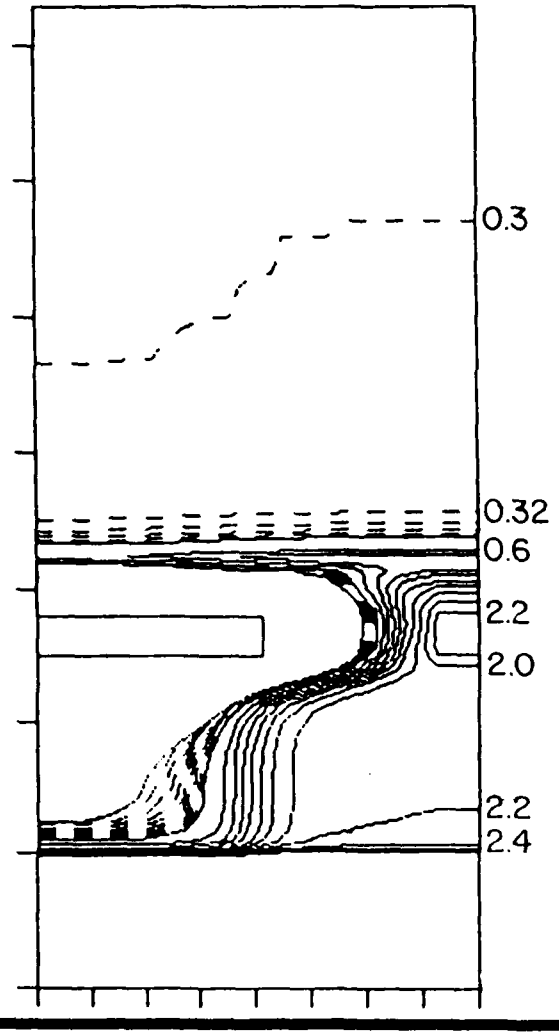
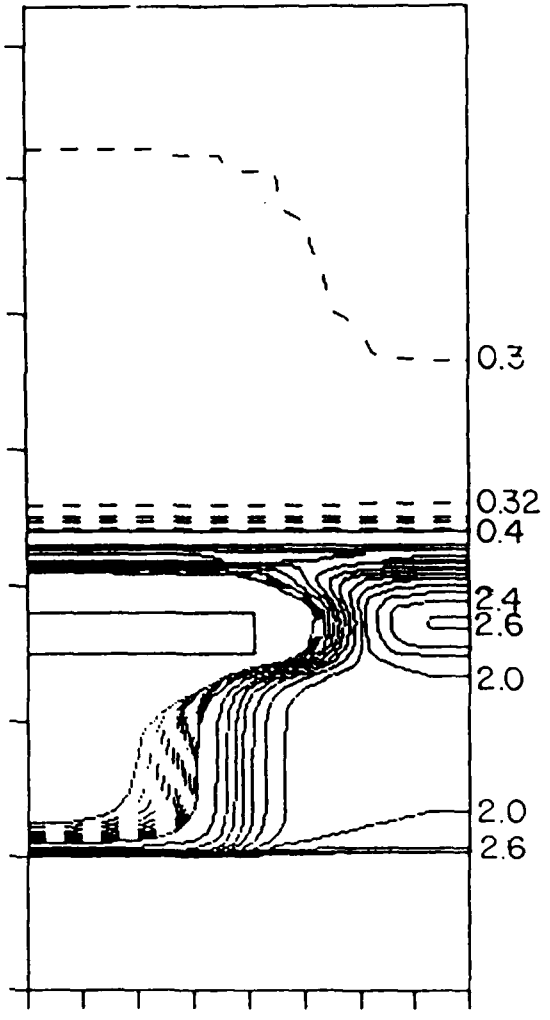
CARRIER DENSITY DISPLAYS (SMALL SIGNAL ?)

$V_c = 1.0,\ V_b = 0.2$



$V_c = 1.0,\ V_b = 0.6$



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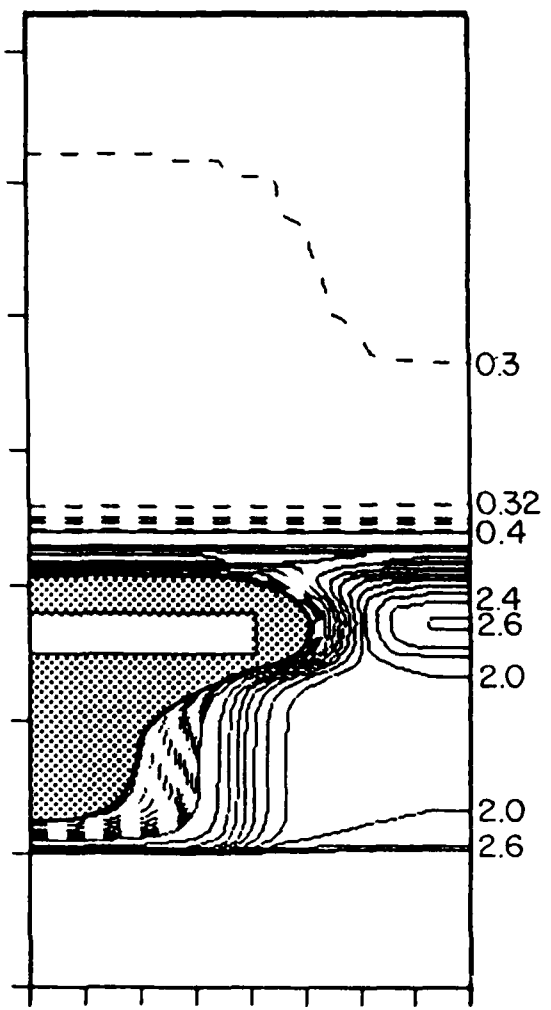
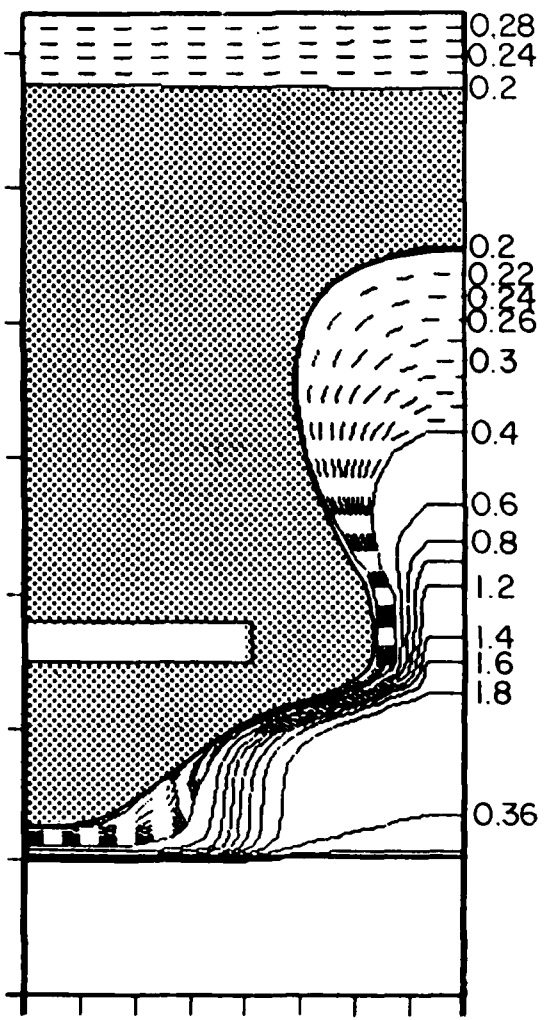
CARRIER DENSITY DISPLAYS (LARGE SIGNAL)

$V_c = 1.0,\ V_b = 0.6$



$V_c = 10.0,\ V_b = -0.4$



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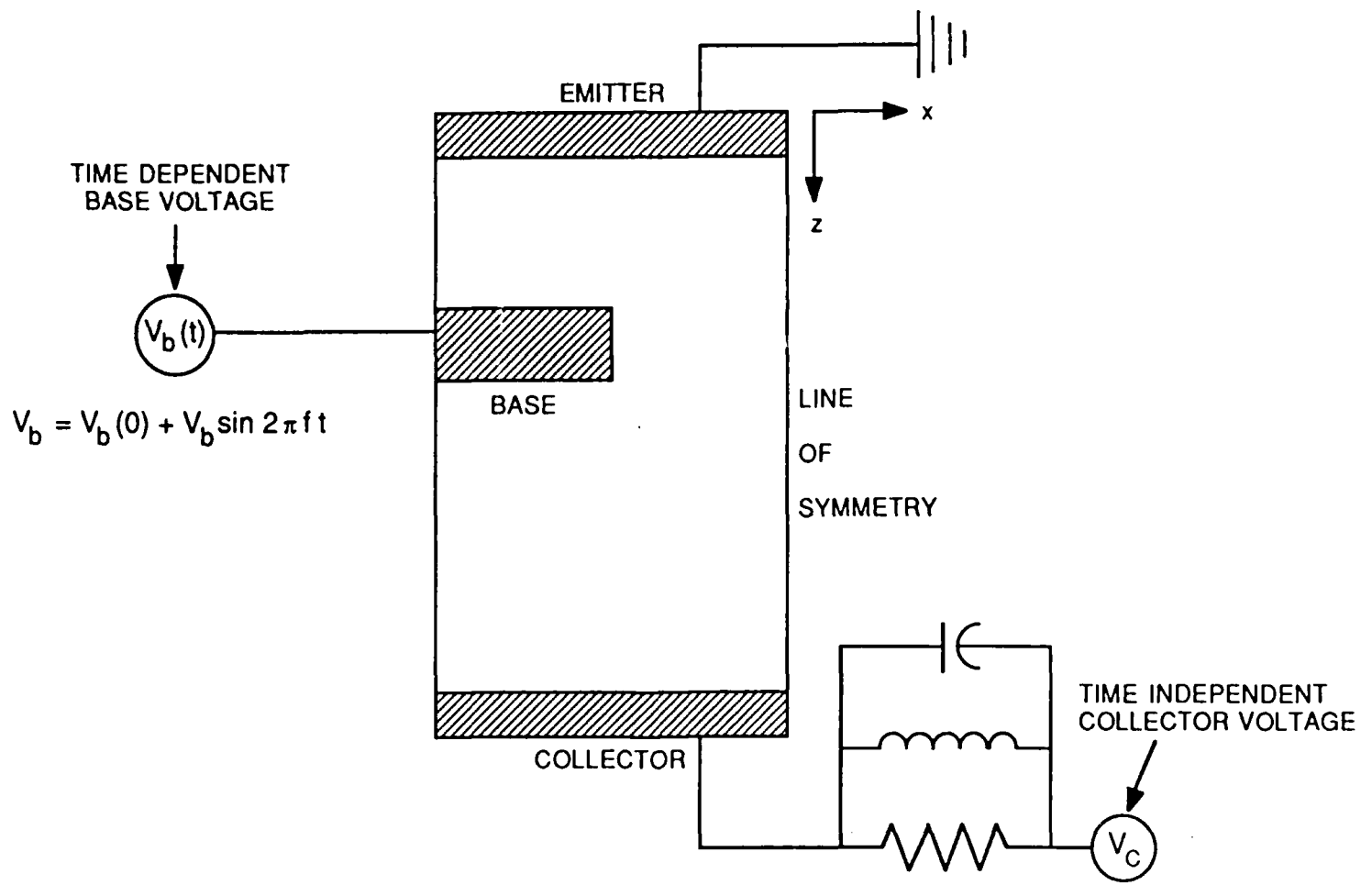
LARGE SIGNAL POWER CALCULATION

ASSUME 25 μm DEPTH AND 150 FINGERS (7mm)

LARGE SIGNAL PBT - CIRCUIT CONFIGURATION
TIME DEPENDENT BASE AND COLLECTOR PERTURBATION



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QUESTIONS

- HOW DO WE CHARACTERIZE THE LARGE SIGNAL BEHAVIOR OF THE PBT?

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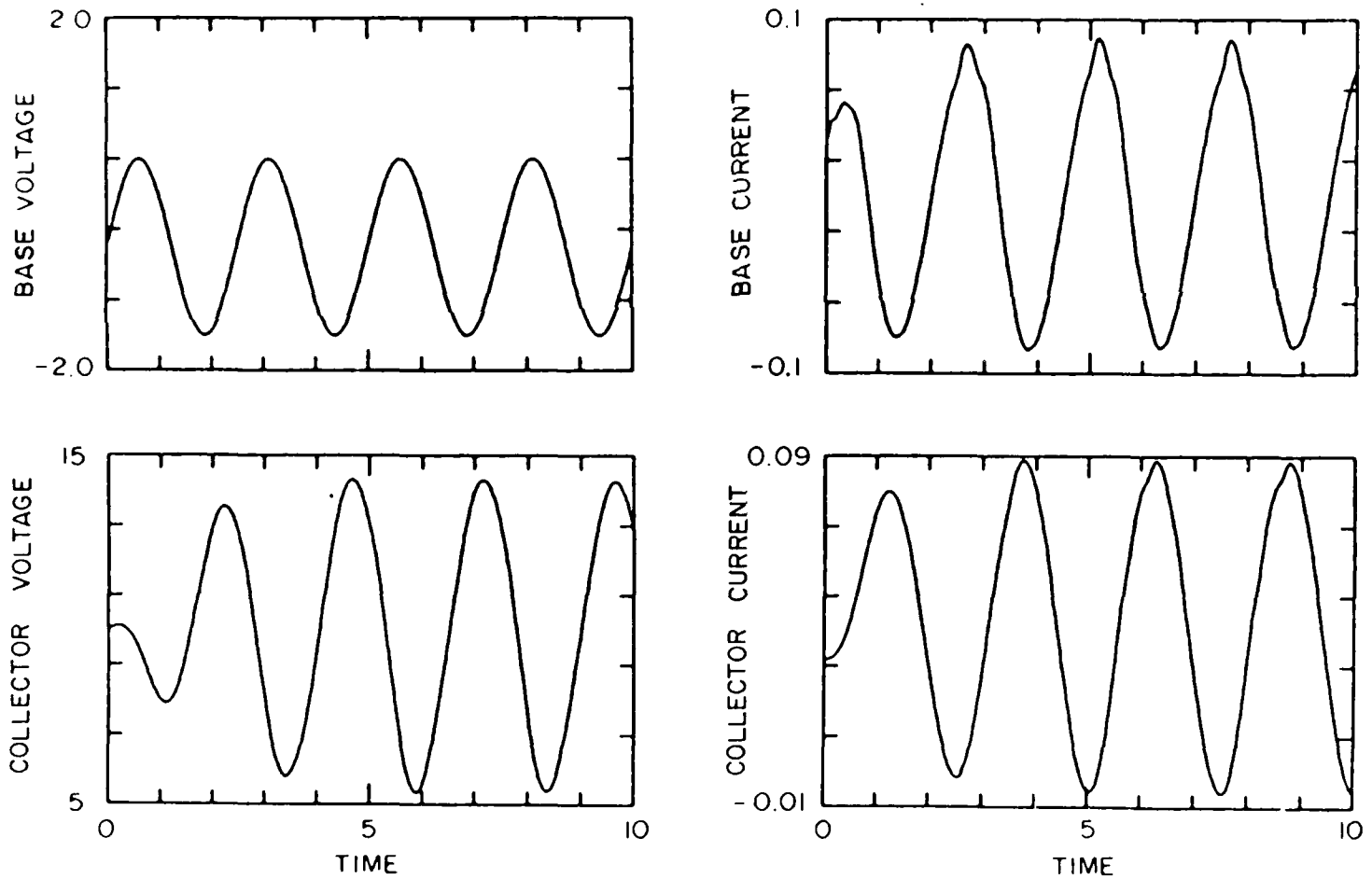
TIME DEPENDENT CURRENT AND VOLTAGE THROUGH BASE AND COLLECTOR



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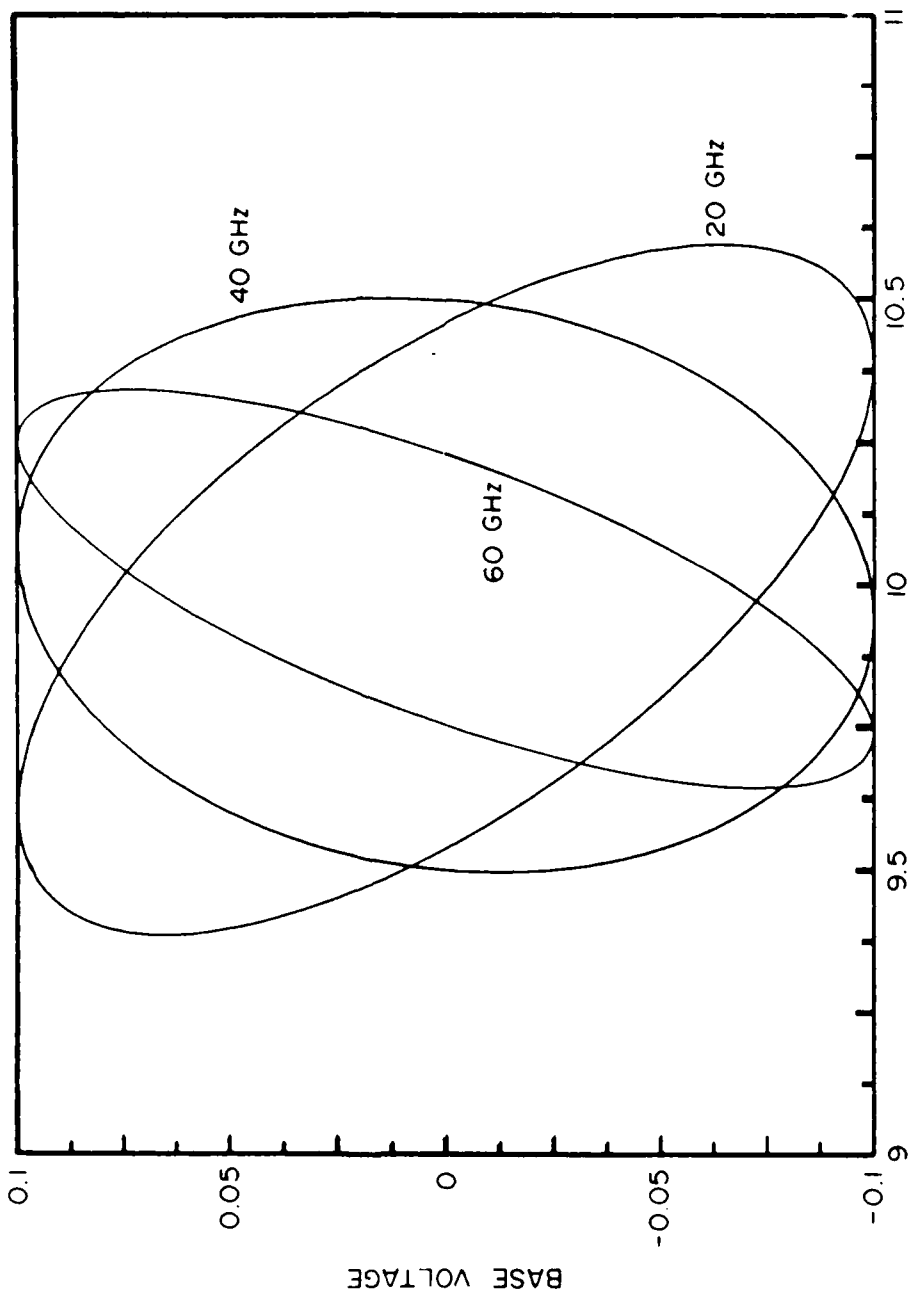
V_b vs. V_c LISSAJOUS



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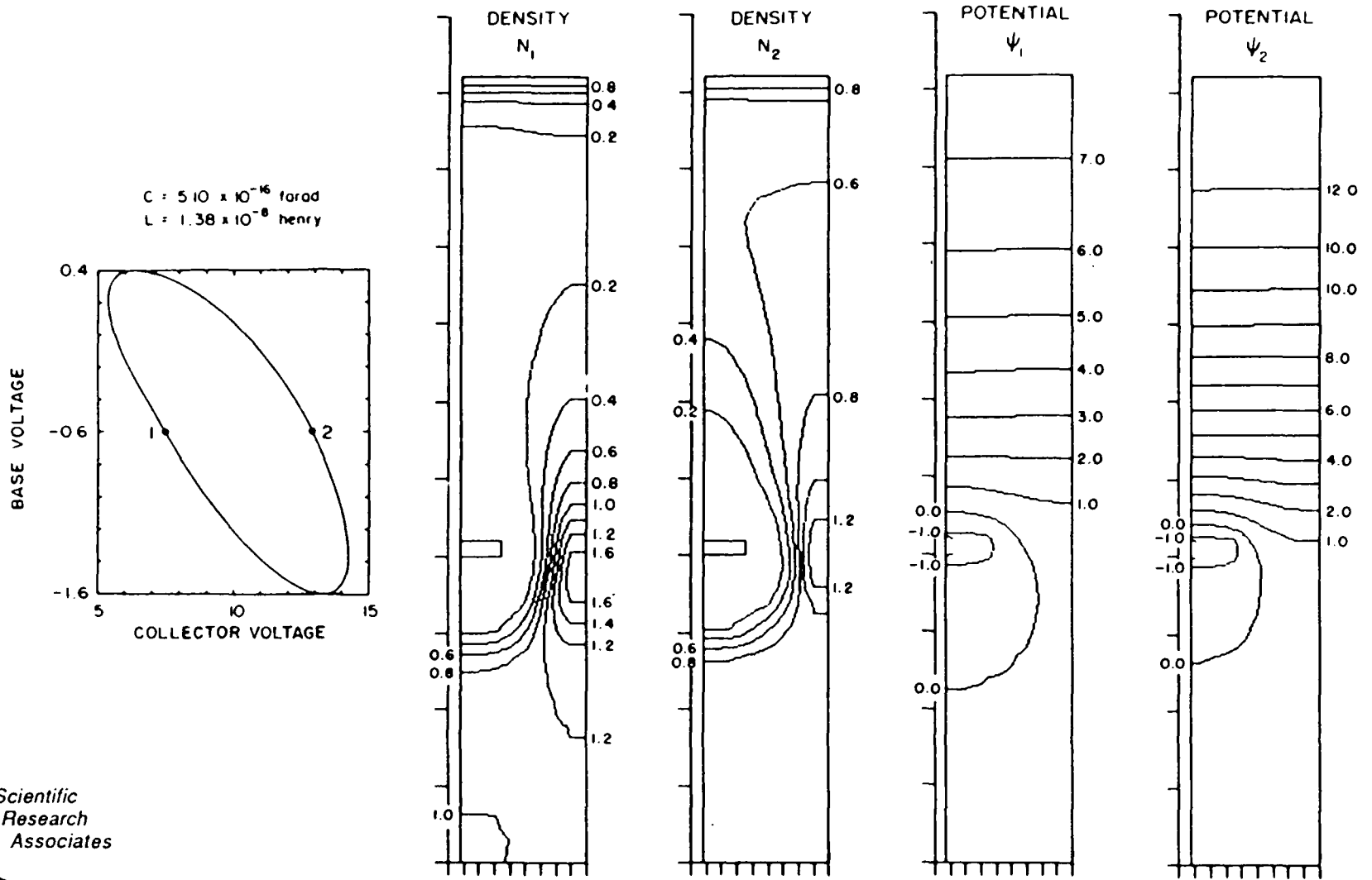
DENSITY AND POTENTIAL CONTOURS FOR $V_b(0) = -0.6$, $V_b = 1.0$

CIRCUIT FREQUENCY = 60 GHz AND DRIVE FREQUENCY = 40 GHz



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COMMENT ON THE RESISTIVE CIRCUIT CALCULATIONS

- AT THE LOWEST FREQUENCY OSCILLATION THE ELECTRONS HAVE AMPLE TIME TO RESPOND TO CHANGES IN THE BASE VOLTAGE.

  DECREASES IN BASE VOLTAGE ARE ACCOMPANIED BY INCREASES IN COLLECTOR VOLTAGE.

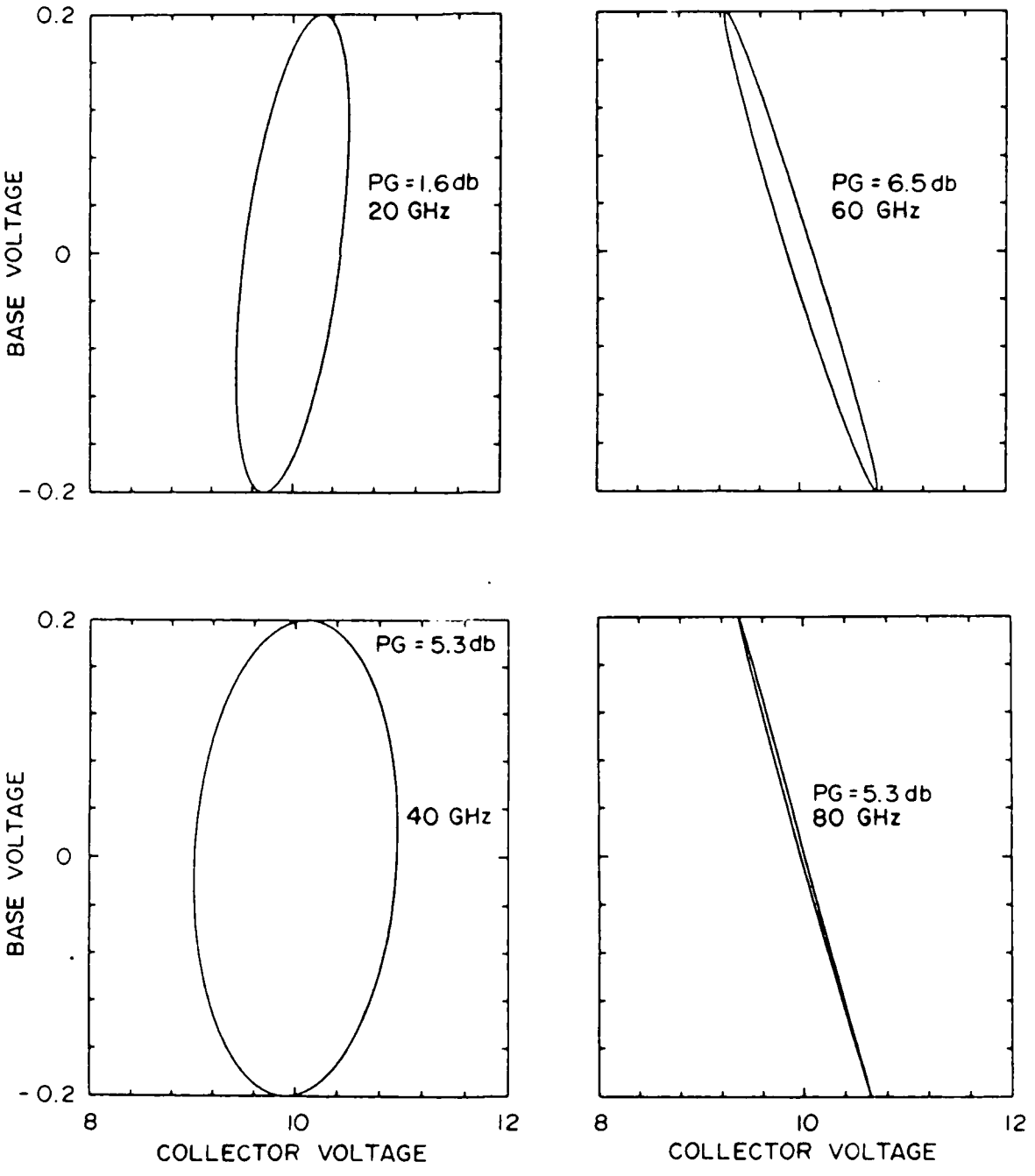
- AS THE FREQUENCY INCREASES ELECTRONS DO NOT HAVE SUFFICIENT TIME TO RESPOND TO THE CHANGE IN BASE VOLTAGE.

  DECREASES IN BASE POTENTIAL ARE NOT NECESSARILY ACCOMPANIED BY INCREASES IN COLLECTIVE POTENTIAL.

  THIS IS AN UNSATISFACTORY SITUATION.

V_B - V_C LISSAJOUS FOR $V_b(0) = 0.0$, $V_b = 0.2$

DRIVE FREQUENCY = 40 GHz, CIRCUIT FREQUENCY INDICATED



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COMMENTS ON REACTIVE CIRCUIT CALCULATIONS

- THE CIRCUIT USED IS A SIMPLE REACTIVE ELEMENT CIRCUIT.

  THE PHASE RELATIONSHIP BETWEEN THE REACTIVE CIRCUIT AND THE COLLECTOR CURRENT IS EASILY OBTAINED AND DEMONSTRATES THAT AT CIRCUIT FREQUENCIES ABOVE THE DRIVING FREQUENCY, IT IS POSSIBLE TO RESTORE A SUITABLE PHASE RELATIONSHIP SUCH THAT DECREASES IN BASE VOLTAGE ARE ACCOMPANIED BY INCREASES IN COLLECTOR VOLTAGE.

- SINCE CIRCUIT DESIGNERS CAN EXPERIMENTALLY OBTAIN LISSAJOUS FIGURES, THE LISSAJOUS IS AN IMPORTANT DESIGN PARAMETERS .

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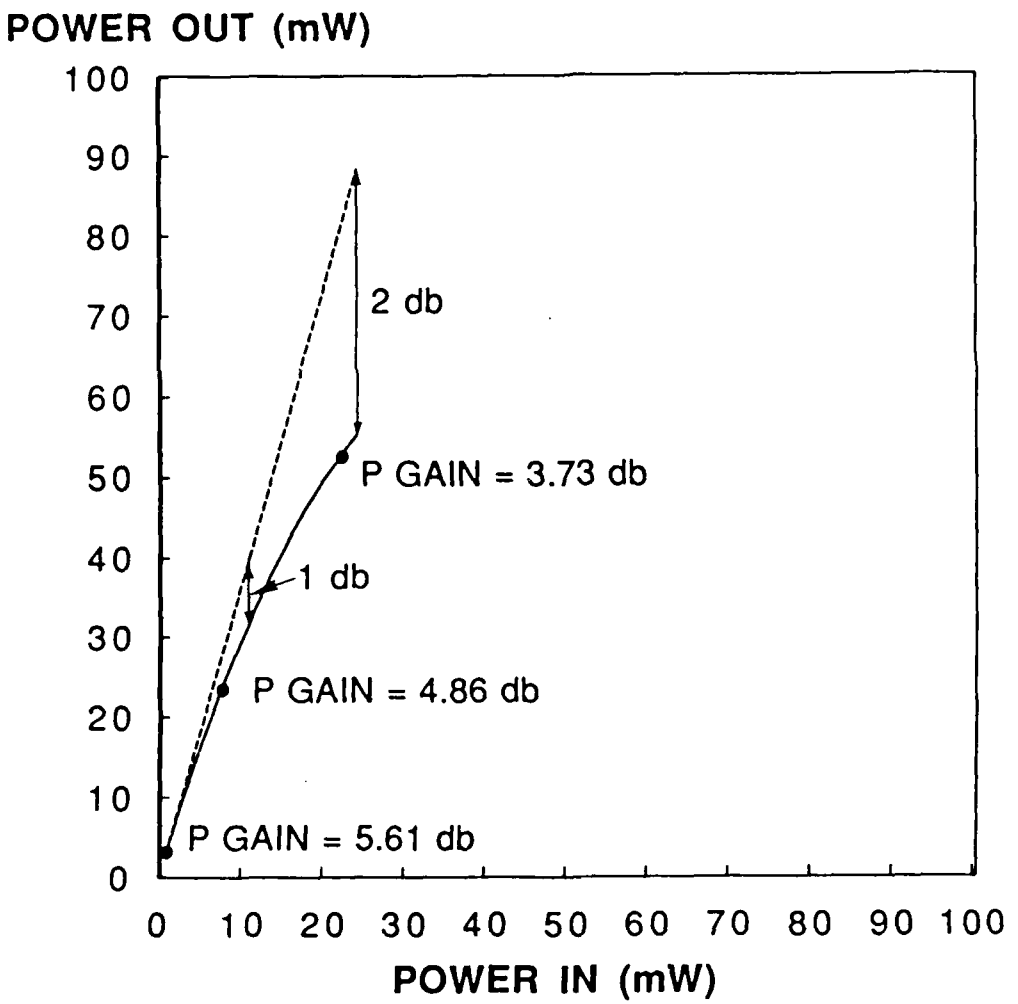
POWER (NEW DESIGN)



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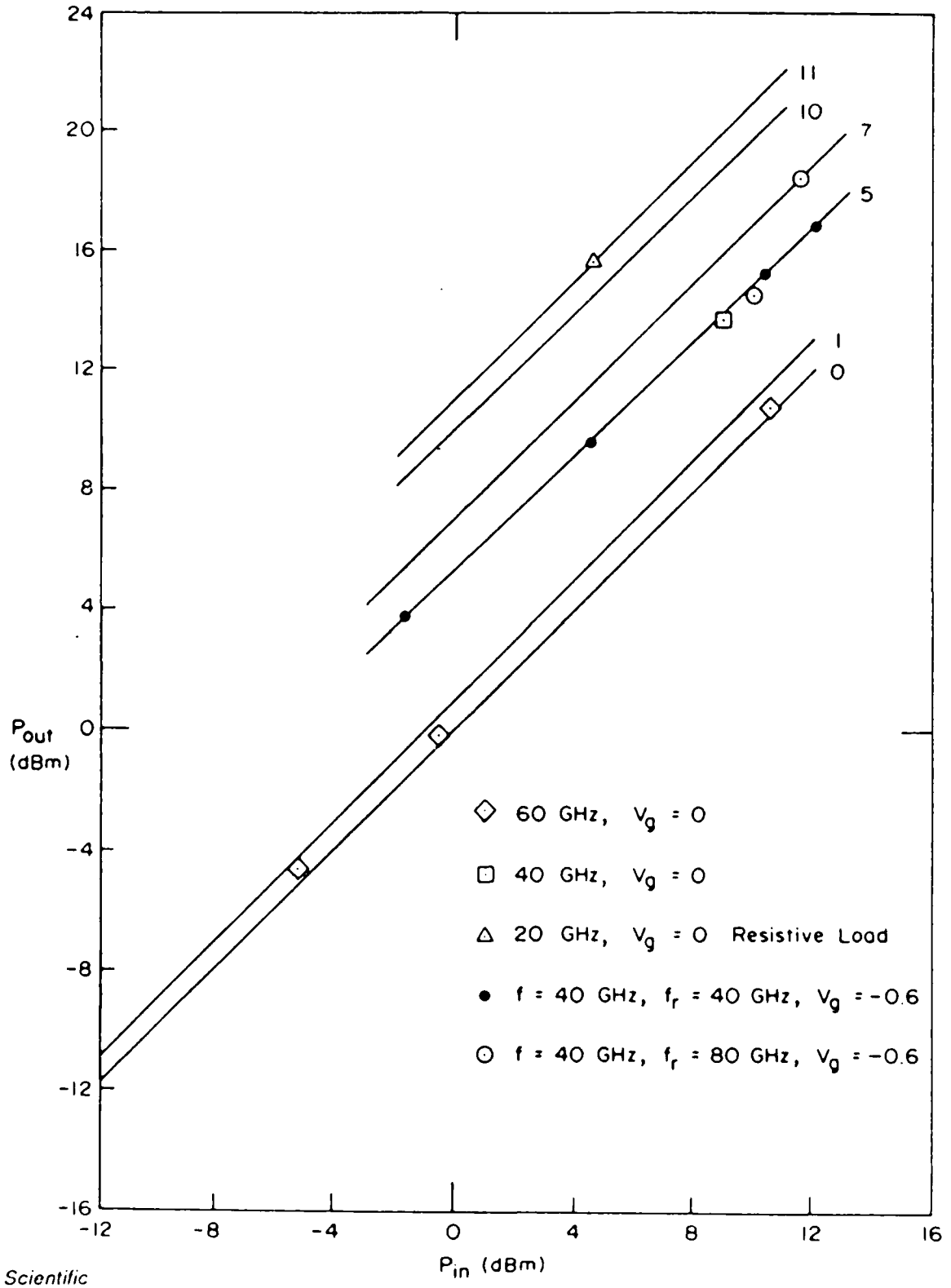
POWER (UNIFORM DOPING)



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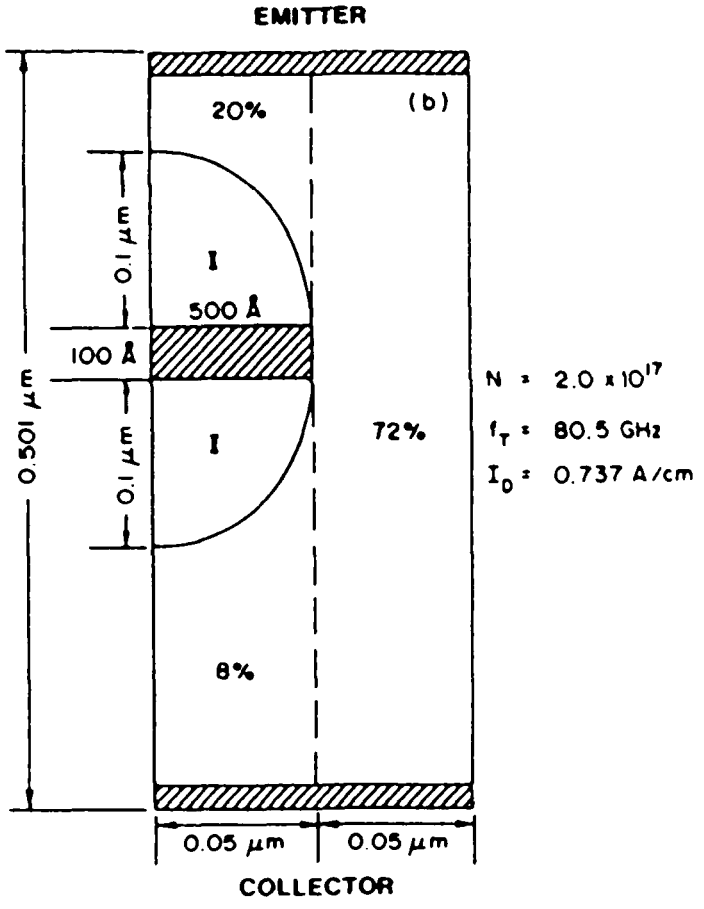
SRA



$N = 2.0 \times 10^{17}$

$f_T = 80.5$ GHz

$I_D = 0.737$ A/cm

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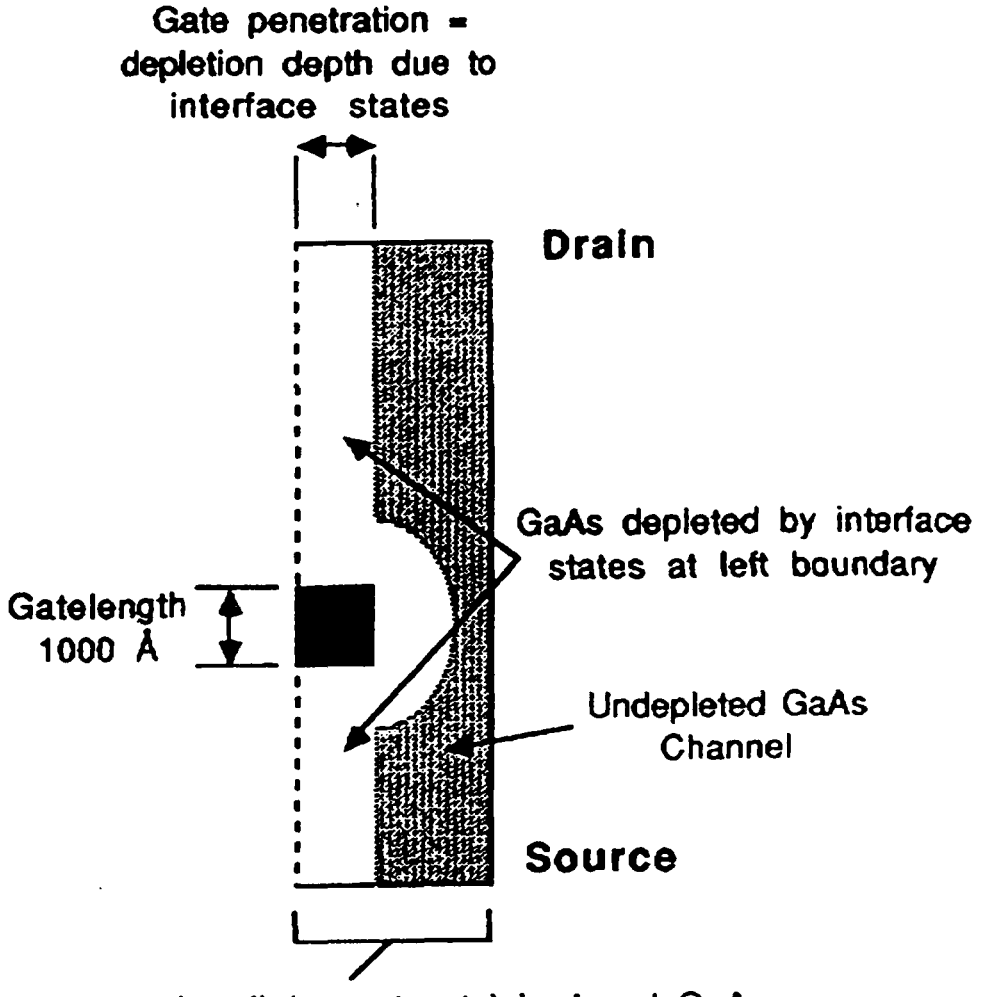
REGROWTH FET WITH 1000 Å GATELENGTH



SRA STRUCTURE

- MEYYAPPAN et al., JOURNAL OF APPLIED PHYSICS VOL. 64(9), p. 4733, NOVEMBER 1988

- MOTIVATION
  - CAPACITANCE SURROUNDING THE BASE IN CONVENTIONAL PBT LARGELY PARASITIC
  - REGION OF SI GaAs PROVIDES A CONTOURED BARRIER REDUCING UNWANTED STORED CHARGE
  - INCREASE IN f_T DEMONSTRATED

NEW WORK

- CONTINUE POWER CHARACTERIZATION OF NONUNIFORMLY DOPED PBT
- STUDY NONUNIFORMLY DOPED PBT WITH REDUCED BASE PENETRATION
- STUDY PBT / REGROWTH FET

PBT SUMMARY

- LARGE SIGNAL PBT DC CALCULATIONS DEMONSTRATE VERY HIGH BREAKDOWN VOLTAGES FOR DEVICES
- UNIFORM STRUCTURES AT 5 x 10^{16} /cm^3 OFFER OUTPUT POWERS AND LINEAR GAINS IN EXCESS OF 50 mW
- SCALING TO A DENSITY OF 2 x 10^{17} /cm^3 AND A FOURFOLD INCREASE IN CROSS-SECTIONAL AREA SUGGEST THE POSSIBILITY OF 3/4 WATT OF POWER AT 40 GHz

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InP/InGaAs HETEROSTRUCTURE BIPOLAR TRANSISTORS

SCIENTIFIC RESEARCH ASSOCIATES, INC.
GLASTONBURY, CT

Scientific Research Associates

InP / InGaAs HBT's

ADVANTAGES

- BETTER ELECTRON INJECTION DUE TO SMALLER CONDUCTION BAND-SPIKE THAN AlGaAs/GaAs SYSTEM
- EFFECTIVE BLOCKING OF HOLES DUE TO HIGHER ΔE_V THAN AlGaAs/GaAs SYSTEM

- LOWER RECOMBINATION (100 ns InP/InGaAs, 1 ns AlGaAs/GaAs)

- SELECTIVE TRANSPORT PROPERTIES SUPERIOR TO GaAs
  - HIGHER DRIFT VELOCITY OF InP (COLLECTOR REGION)
  - HIGHER ELECTRON MOBILITY OF InGaAs (BASE REGION)

- COMPATIBILITY WITH OPTOELECTRONIC IC's

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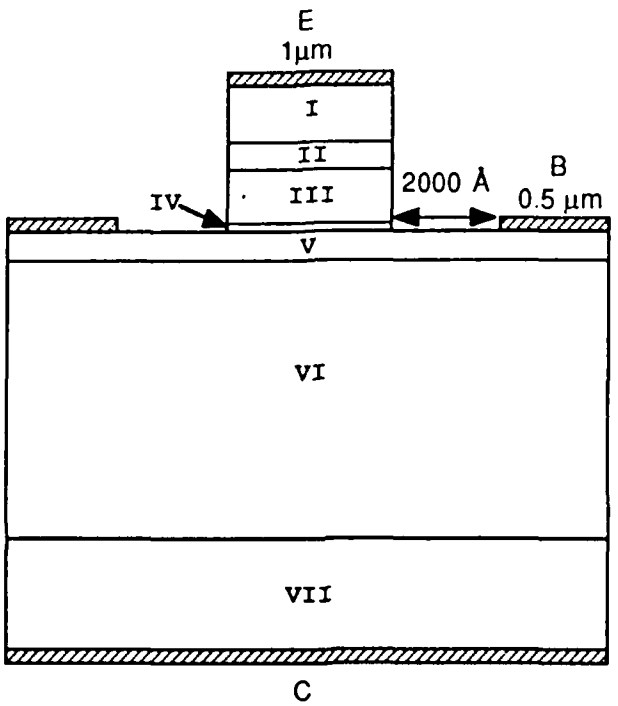

I	EMITTER CAP	$In_{0.53}Ga_{0.47}As$	1000 Å	5×10^{18} N^+
II	GRADED LAYER	InGaAs → InP	500 Å	5×10^{18} N^+
III	EMITTER	InP	1000 Å	2×10^{17} N
IV	GRADED LAYER	InP → InGaAs	100 Å	2×10^{17} N
V	BASE	BANDGAP GRADING $In_{0.53}Ga_{0.47}As$	500 Å	5×10^{18} P^+
VI	COLLECTOR	InP	5000 Å	1×10^{17} N
VII	SUBCOLLECTOR	$In_{0.53}Ga_{0.47}As$	2000 Å	5×10^{18} N^+

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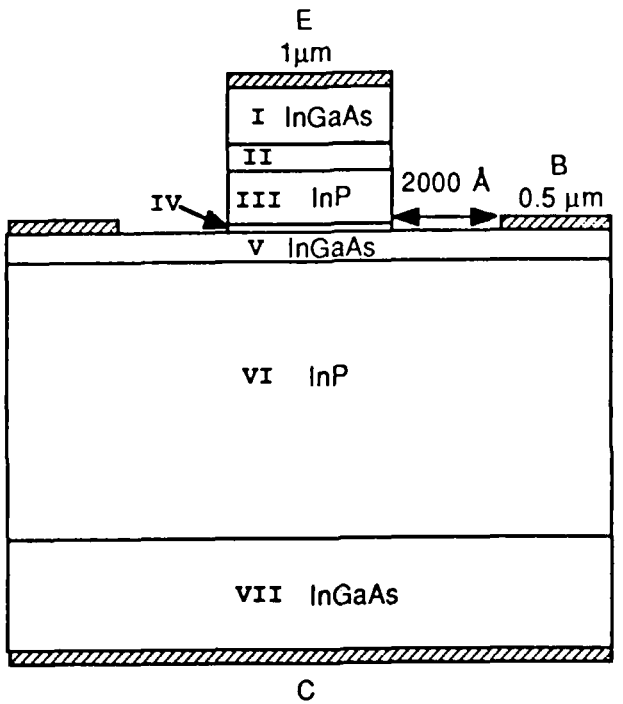
DOUBLE HETEROSTRUCTURE, InP/InGaAs/InP



I	EMITTER CAP	$In_{0.53}Ga_{0.47}As$	1000 Å	5×10^{18} N^+
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III	EMITTER	InP	1000 Å	2×10^{17} N
IV	GRADED LAYER	InP → InGaAs	100 Å	2×10^{17} N
V	BASE	BANDGAP GRADING $In_{0.53}Ga_{0.47}As$	500 Å	5×10^{18} P^+
VI	COLLECTOR	InP	5000 Å	1×10^{17} N
VII	SUBCOLLECTOR	$In_{0.53}Ga_{0.47}As$	2000 Å	5×10^{18} N^+

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CRITICAL DEVICE FEATURES

- SELF-ALIGNED STRUCTURE
- 500 Å BASE, BAND-GAP GRADING EMPLOYED
- 5000 Å COLLECTOR DOPED, 10^{17} N
- 1 μm STRIPE-WIDTH FOR EMITTER

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GOVERNING EQUATIONS

- POISSON'S EQUATION

$$\nabla \cdot (\varepsilon \nabla \psi) = +e\,(n - p - C)$$

- DRIFT AND DIFFUSION EQUATIONS

$$\partial n / \partial t = \nabla \cdot J_n / e - R_n$$

$$\partial p / \partial t = \nabla \cdot J_p / e - R_p$$

$$J_n = e(n\mu_n F_n - n\mu_n \nabla\psi - D_n \nabla n)$$

$$J_p = -\,e(p\mu_p F_p + p\mu_p \nabla\psi + D_p \nabla p)$$

$$F_n = \nabla (\chi / e + (kT / e) \ln N_c)$$

$$F_p = \nabla (\chi / e + E_g / e - (kT / e) \ln N_v)$$

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GOVERNING EQUATIONS (continued)

- RECOMBINATION

$$R_{SRH} = R_n = R_p + [pn - n_i^2] / [\tau_p(n + n_i) + \tau_n(p + p_i)]$$

$$R_{Aug} = r\,(n + p)\,(np - ni^2)$$

- TRANSPORT PROPERTIES

$$\mu = \frac{V}{F} \qquad \text{WHERE} \quad F = -\nabla\psi - F_n \text{ FOR ELECTRONS}$$

$$F = -\nabla\psi - F_p \text{ FOR HOLES}$$

$$D = \frac{kT}{q}\,\mu \qquad \text{(EINSTEIN RELATION)}$$

- BOUNDARY CONDITION AT THE OHMIC CONTACTS

$$\psi = \psi_{applied} - \frac{kT}{e} \ln \frac{N_c}{N_D} - \chi / e$$

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TRANSPORT PROPERTIES

- VELOCITY-FIELD CHARACTERISTICS, LOW-FIELD MOBILITY
- EVALUATED FOR BOTH InP AND $In_{0.53}Ga_{0.47}As$ AT VARIOUS DOPING LEVELS USING A MONTE-CARLO PROCEDURE

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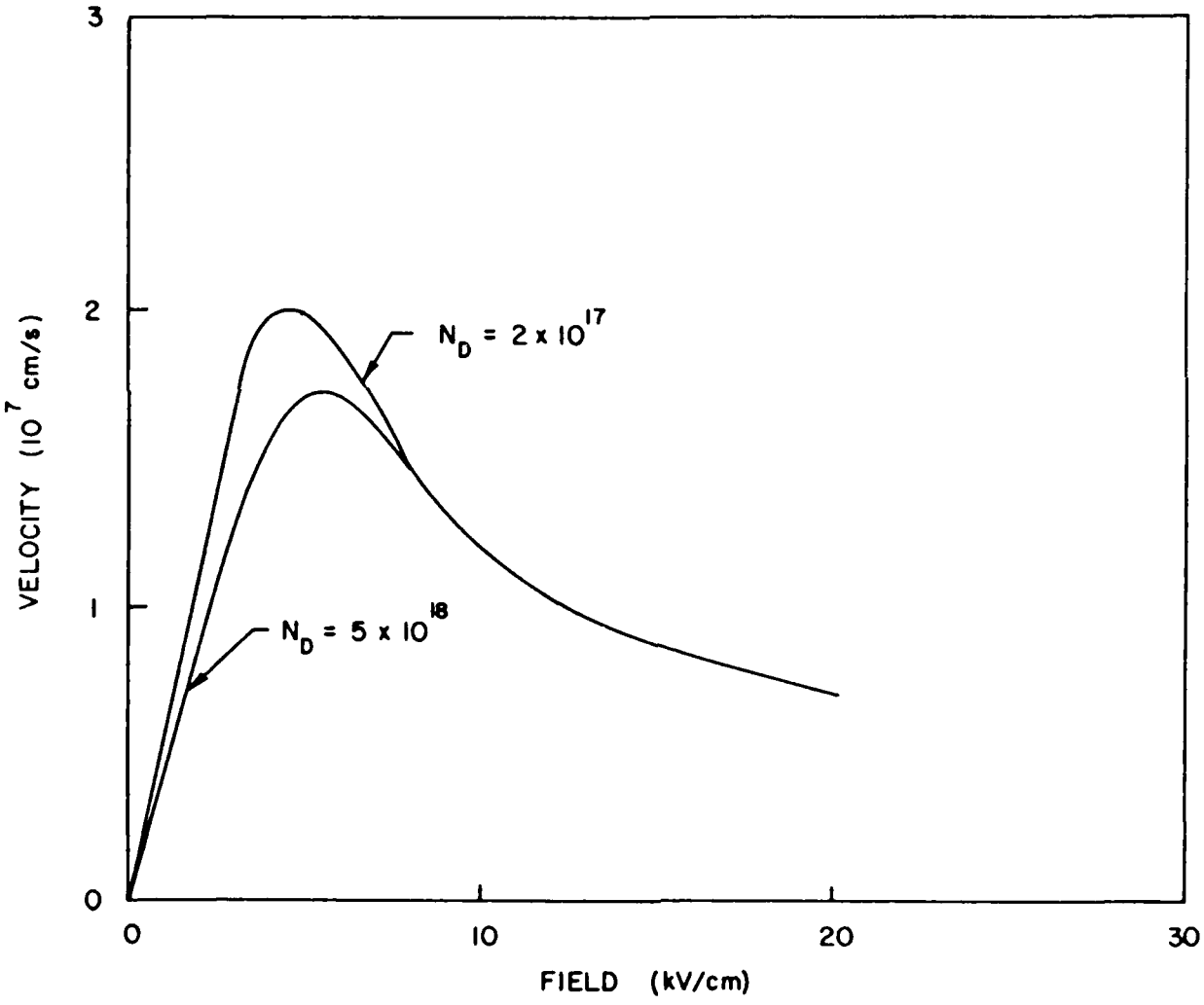
VELOCITY-FIELD CHARACTERISTICS: $In_{0.53}Ga_{0.47}As$



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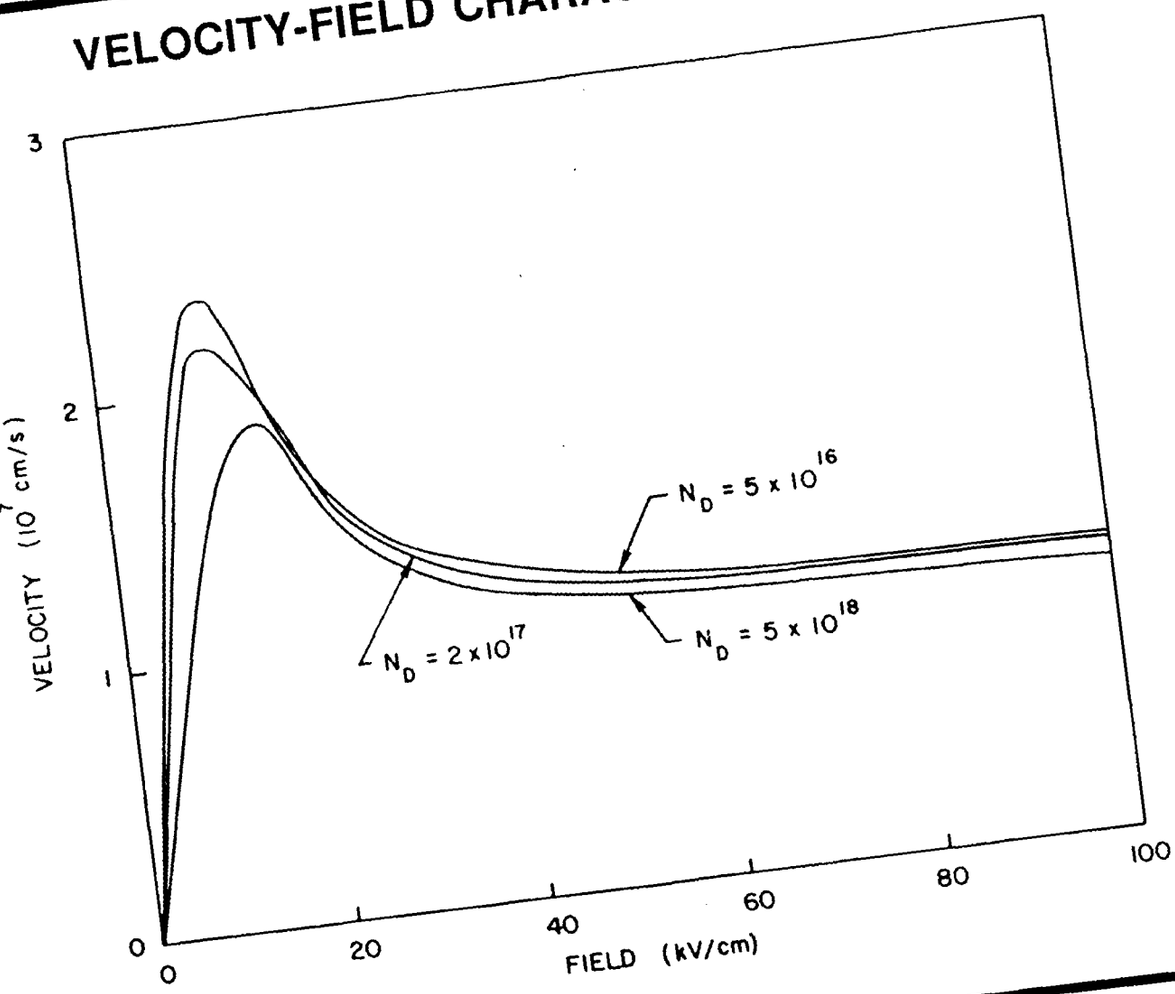
VELOCITY-FIELD CHARACTERISTICS: InP



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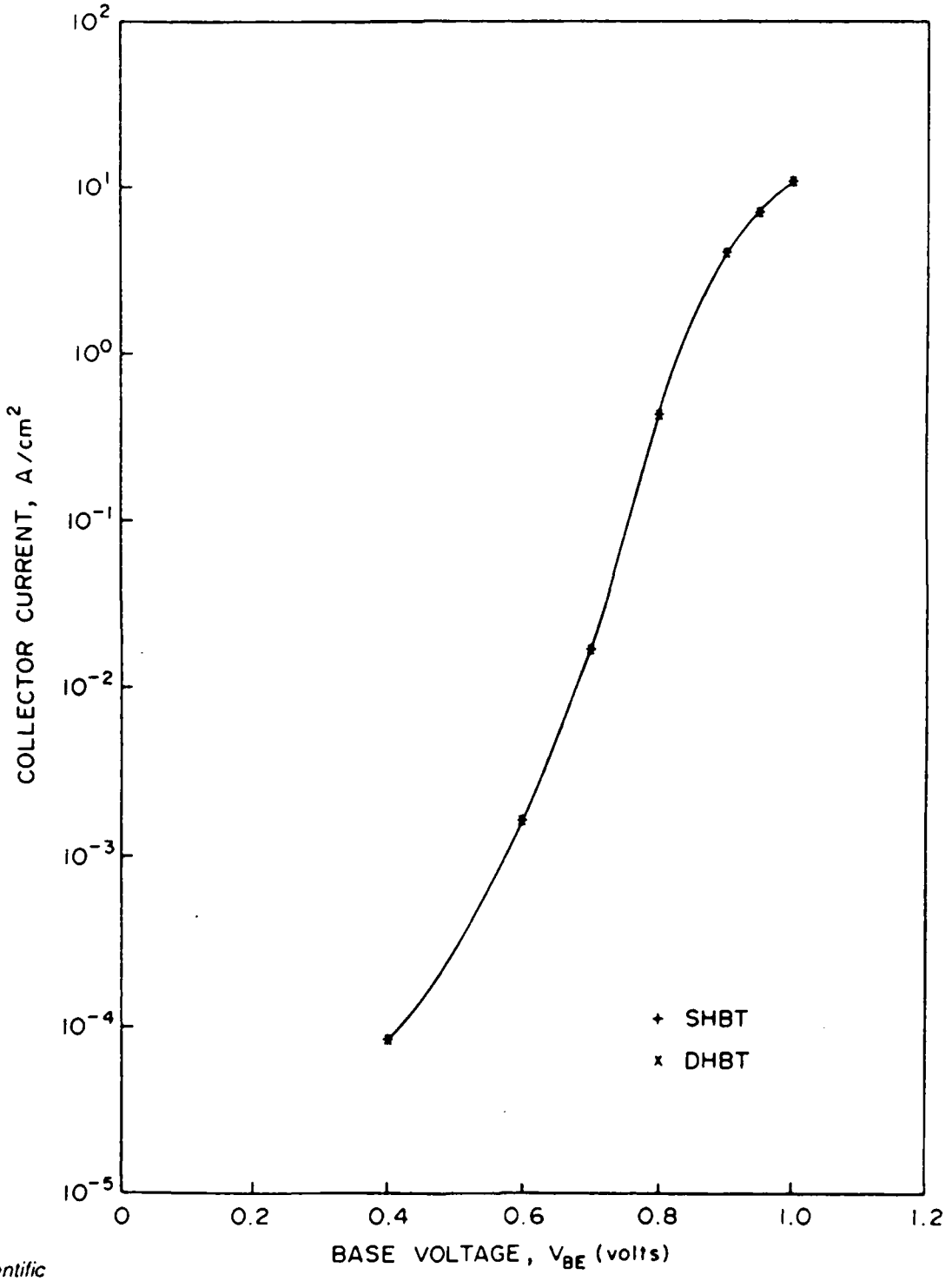
COLLECTOR CURRENT vs. V_{BE} FOR InP/InGaAs DHBT AND SHBT



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- VARIATION OF I_C WITH V_{BE} IDENTICAL FOR SHBT AND DHBT
  - CURRENT LIMITED BY EMITTER INJECTION: EMITTER / BASE DESIGN SAME IN BOTH CASES
  - COLLECTOR TRANSPORT DETERMINED BY SATURATION VELOCITY
  - $V_{sat,\ InP} / V_{sat,\ InGaAs} \approx 3$
  - CARRIER DENSITY IN THE COLLECTOR ADJUSTS $n_{InP} / n_{InGaAs} \sim 1/3$

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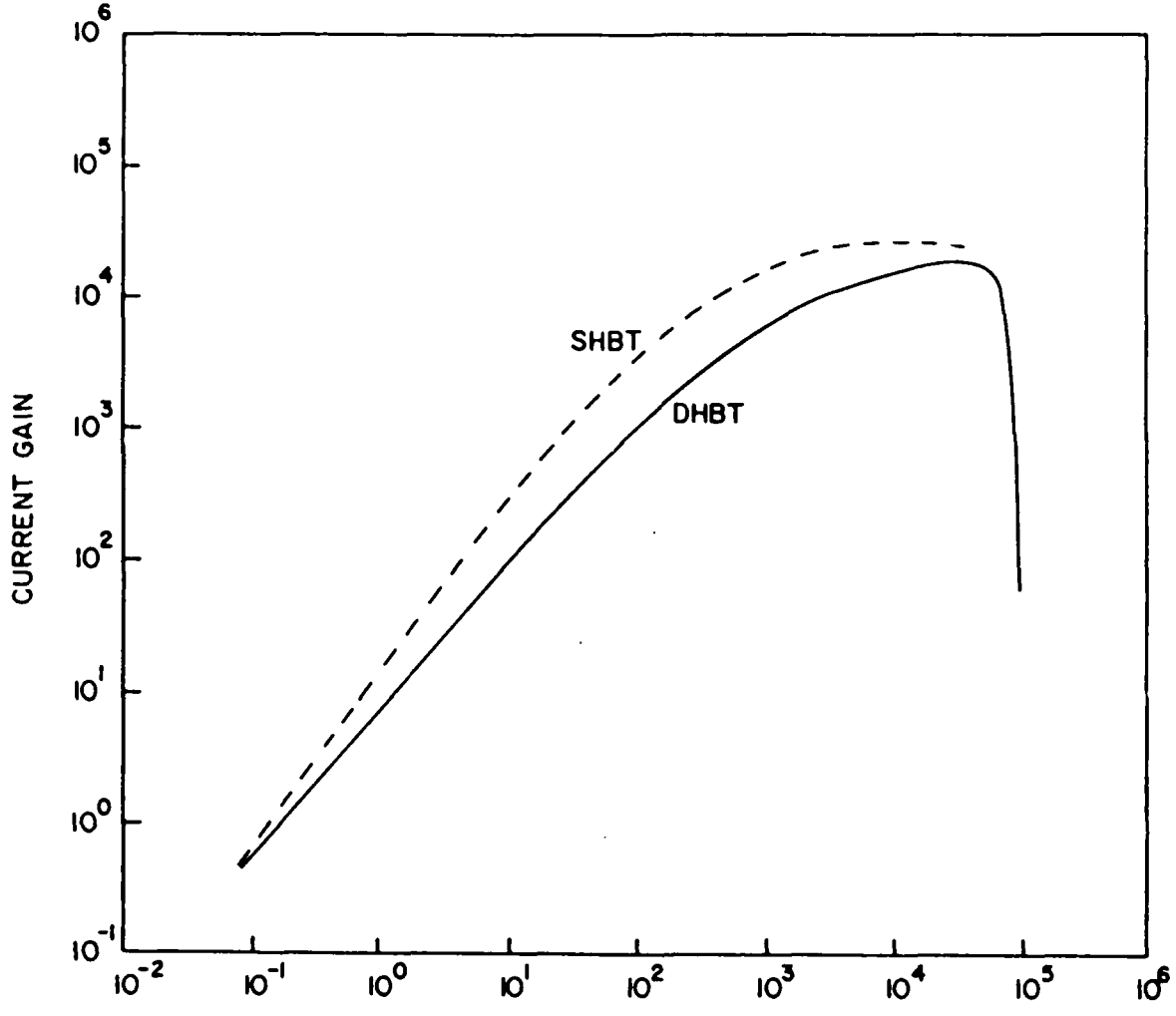
CURRENT GAIN vs. COLLECTOR CURRENT



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CONCLUSIONS

- HIGHER CUT-OFF FREQUENCY POSSIBLE WITH InP/InGaAs THAN THE AlGaAs/GaAs SYSTEM
- HIGHER CURRENT GAIN POSSIBLE WITH InP/InGaAs THAN THE AlGaAs/GaAs SYSTEM
- FURTHER CALCULATIONS NEEDED TO OPTIMIZE InP/InGaAs/InP HBT

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COMPARISON AGAINST EXPERIMENTAL RESULTS

- NOTTENBURG et al.: JANUARY 1989

  STRUCTURE WITH 3000 Å COLLECTOR, $N_D = 2 \times 10^{16}$

  650 Å BASE DOPED $N_A = 5 \times 10^{19}$

  3000 Å EMITTER $N_D = 5 \times 10^{17}$

  HIGHEST f_T = 110 GHz

  f_{max} = 58 GHz

  CURRENT GAIN = 11000

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FIGURES-OF-MERIT

- CURRENT GAIN 2.63×10^4 FOR DHBT
  vs. 2.55×10^4 FOR SHBT

- CUT-OFF FREQUENCY 78.6 GHz AT $I_c = 5.5 \times 10^4$ A/cm^2
  FOR DHBT vs. 46.9 GHz AT $I_c = 3.6 \times 10^4$ A/cm^2

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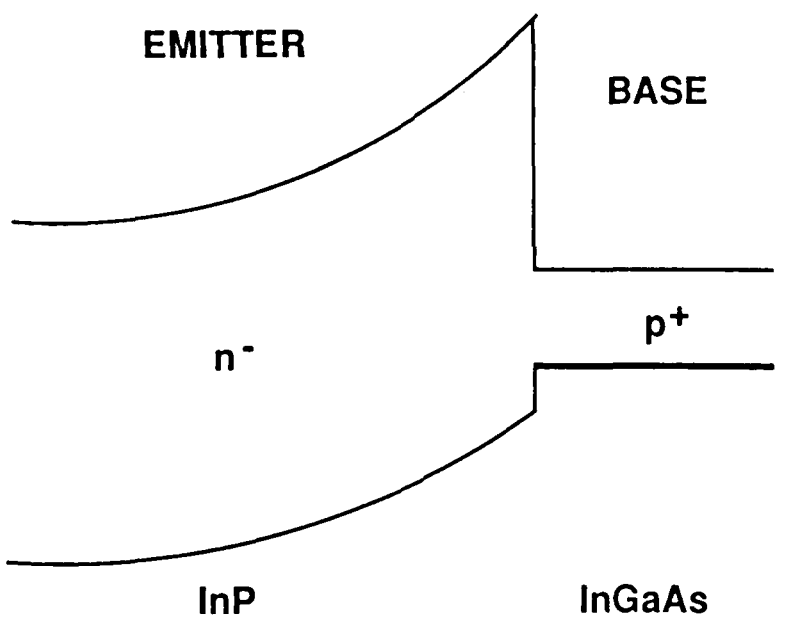
BAND DIAGRAM



$\Delta E_c = 0.22$ ev

$\Delta E_v = 0.37$ ev

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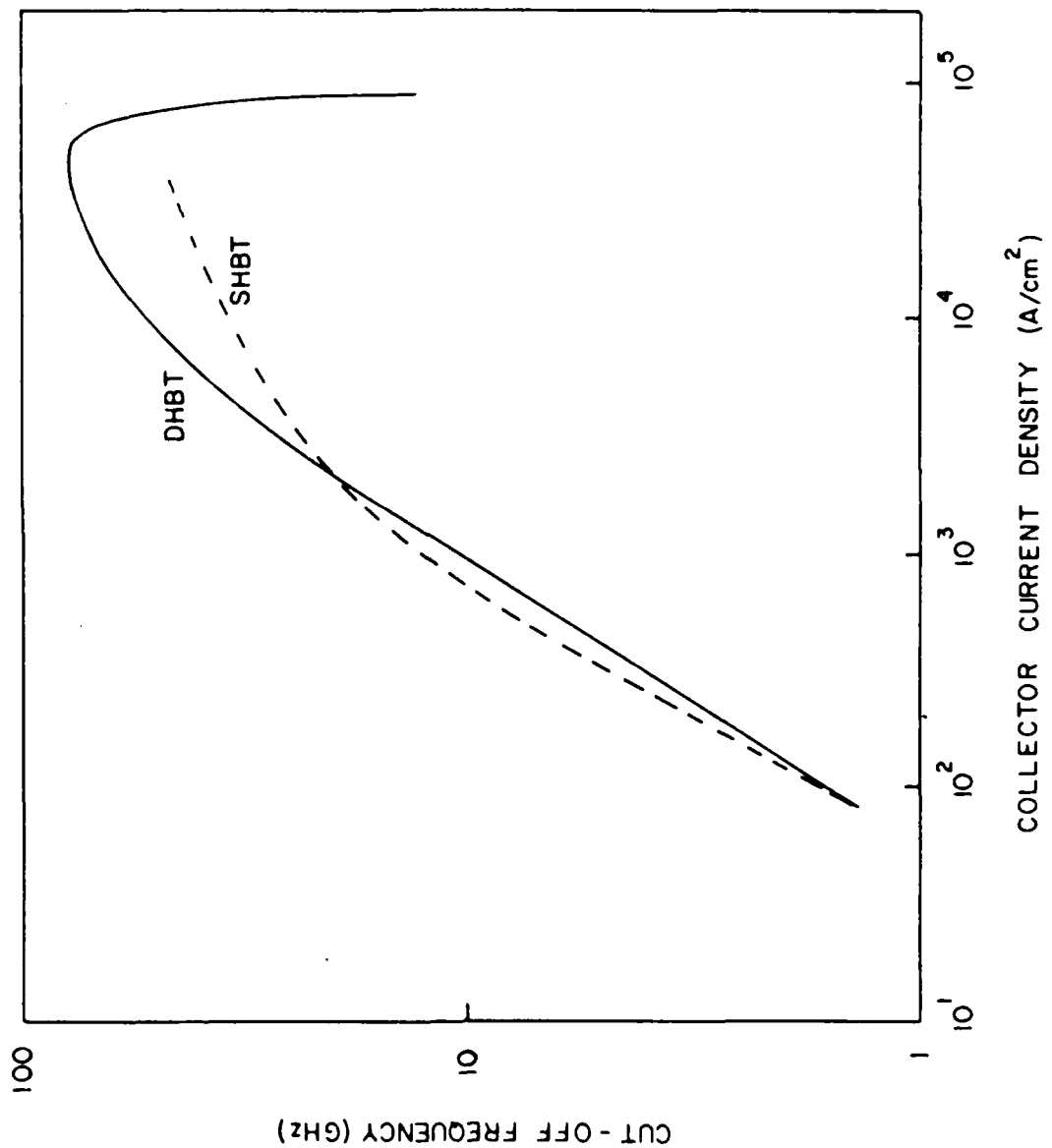
CUT-OFF FREQUENCY vs. COLLECTOR CURRENT



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FUTURE WORK

- INCREASE BASE DOPING TO REDUCE SHEET RESISTANCE AND INCREASE f_{max}
- REDUCE COLLECTOR WIDTH TO DECREASE COLLECTOR TRANSIT TIME
- OPTIMIZE EMITTER DIMENSIONS FOR POWER
- PERFORM TRANSIENT ACCURATE, SMALL SIGNAL CALCULATIONS
- PNP STRUCTURES FOR COMPLEMENTARY DEVICE CIRCUITS

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FUTURE WORK (cont.)

LARGE SIGNAL SWITCHING:

- SWITCHING FROM "OFF" TO A HIGH CONDUCTION STATE BY IMPOSING A STEP CHANGE IN BASE VOLTAGE KEEPING COLLECTOR BIAS FIXED
- COMPUTING DEVICE RESPONSE TIME THROUGH TRANSIENT ACCURATE CALCULATIONS

SMALL SIGNAL AMPLIFICATION:

- IMPOSE A SINUSOIDAL SIGNAL ON THE BASE CONTACT, KEEPING COLLECTOR BIAS FIXED
- FOURIER ANALYZE THE RESULTS TO COMPUTE f_{max} AND POWER

MATERIAL AND TRANSPORT PROPERTIES

E_g: $Al_{0.3}GaAs$ (1.8 ev) > GaAs (1.424 ev) > InP (1.34 ev) > $In_{0.53}GaAs$ (0.75 ev)

x : $In_{0.53}GaAs$ (4.6 ev) > InP (4.38 ev) > GaAs (4.07 ev) > $Al_{0.3}GaAs$ (3.752 ev)

V_{sat}: 10^7 cm/s FOR InP
7.5×10^6 cm/s FOR GaAs
5×10^6 cm/s FOR $Al_{0.3}GaAs$
3.5×10^6 cm/s FOR $In_{0.53}GaAs$

ΔE_c: 0.22 ev FOR InP/InGaAs vs. 0.318 ev FOR AlGaAs/GaAs

ΔE_v: 0.37 ev FOR InP/InGaAs vs. 0.057 ev FOR AlGaAs/GaAs

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CURRENT GAIN

- TWO ORDERS OF MAGNITUDE HIGHER THAN AlGaAs/GaAs SYSTEM
  - DUE TO LONGER CARRIER LIFE-TIME (100 ns vs. 1 ns)
  - NEGLIGIBLE SURFACE RECOMBINATION
  - LARGE VALENCE BAND DISCONTINUITY ($\Delta E_v = 0.37$ ev) TO PREVENT HOLE INJECTION INTO EMITTER (COMPARE 0.059 FOR AlGaAs/GaAs SYSTEM)
  - CONDUCTION BAND DISCONTINUITY 0.22 v FOR ELECTRON INJECTION (COMPARE 0.318 FOR AlGaAs/GaAs SYSTEM)

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GaAlAs/GaAs Heterojunction Bipolar Transistors for mm-Wave Applications

Peter Asbeck

Rockwell International, Science Center
Thousand Oaks, CA

GaAlAs/GaAs HETEROJUNCTION BIPOLAR TRANSISTORS FOR mm-WAVE APPLICATIONS

CONTRACT N00014-86-C-0078
MONITORED BY ONR

ROCKWELL INTERNATIONAL, SCIENCE CENTER
THOUSAND OAKS, CA

GaAlAs/GaAs HETEROJUNCTION BIPOLAR TRANSISTOR DEVELOPMENT

ROCKWELL INTERNATIONAL

SC44039

OBJECTIVE

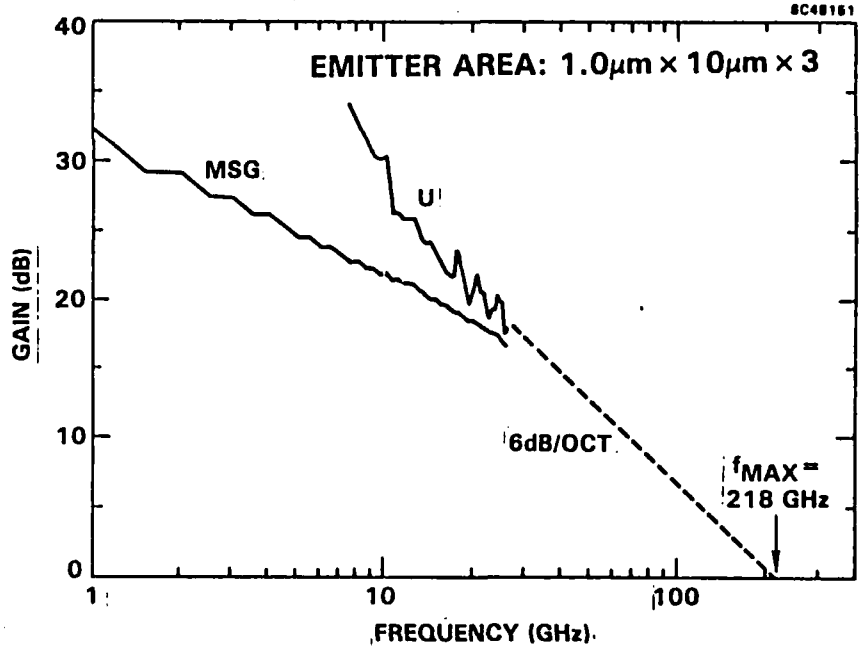
DEVELOP TRANSISTORS WITH SUPERIOR GAIN AND POWER HANDLING CAPABILITY AT 60 GHz AND 94 GHz

APPROACH

UTILIZE GaAlAs/GaAs MULTILAYER STRUCTURES TO OPTIMIZE THE PERFORMANCE OF BIPOLAR TRANSISTORS

STATUS

- FIRST HIGH PERFORMANCE, MM-WAVE COLLECTOR UP HBTs DEMONSTRATED- FMAX = 100 GHz
- FMAX OF EMITTER-UP HBTs INCREASED TO 215 GHz
- MMIC COMPATIBLE TECHNOLOGY DEMONSTRATED
- AMPLIFIER BEHAVIOR AT 94 GHz MODELED



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MM-WAVE HBT TEAM

MBE	PROCESS	CHARACTERIZATION & MODELING
G. Sullivan	F. Chang	N.H. Sheng
M. Szwed	W.J. Ho	P. Asbeck
	R. Anderson	J.A. Higgins
	R. Pierson	E. Sovero
	K. Steckbauer	K.C. Wang
		D. Deakin

SPONSOR

J. MURPHY

WHY HBTs FOR mm-WAVE OPERATION?

- VERTICAL STRUCTURE

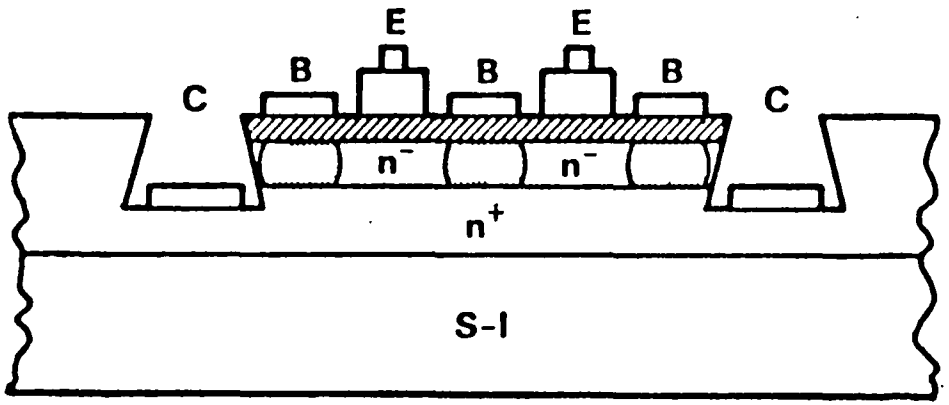
  CONTROLLABLE SHORT DIMENSIONS
  EASE OF VARYING COMPOSITION PROFILE
  HIGH POWER DENSITY
  NO SUBSTRATE LEAKAGE

- ROBUST FABRICATION WITH SIMPLE LITHOGRAPHY

- LOW OUTPUT CONDUCTANCE

- CONTROLLABLE BREAKDOWN VOLTAGE

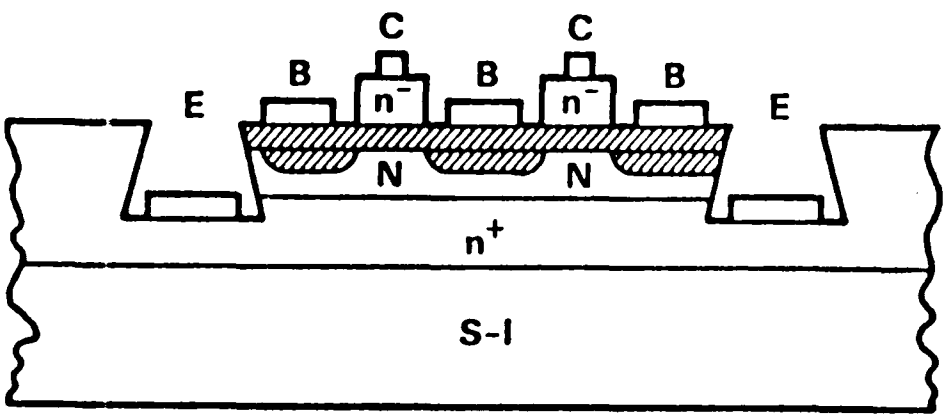
EMITTER-Up mm-WAVE HBT



- SIMPLER FABRICATION
- LOWER EMITTER RESISTANCE

COLLECTOR-Up mm-WAVE HBT

$$f_{max} = \sqrt{\frac{ft}{8\pi R_B C_{BC}}}$$



- LOWER BASE-COLLECTOR CAPACITANCE
- LOWER EMITTER INDUCTANCE

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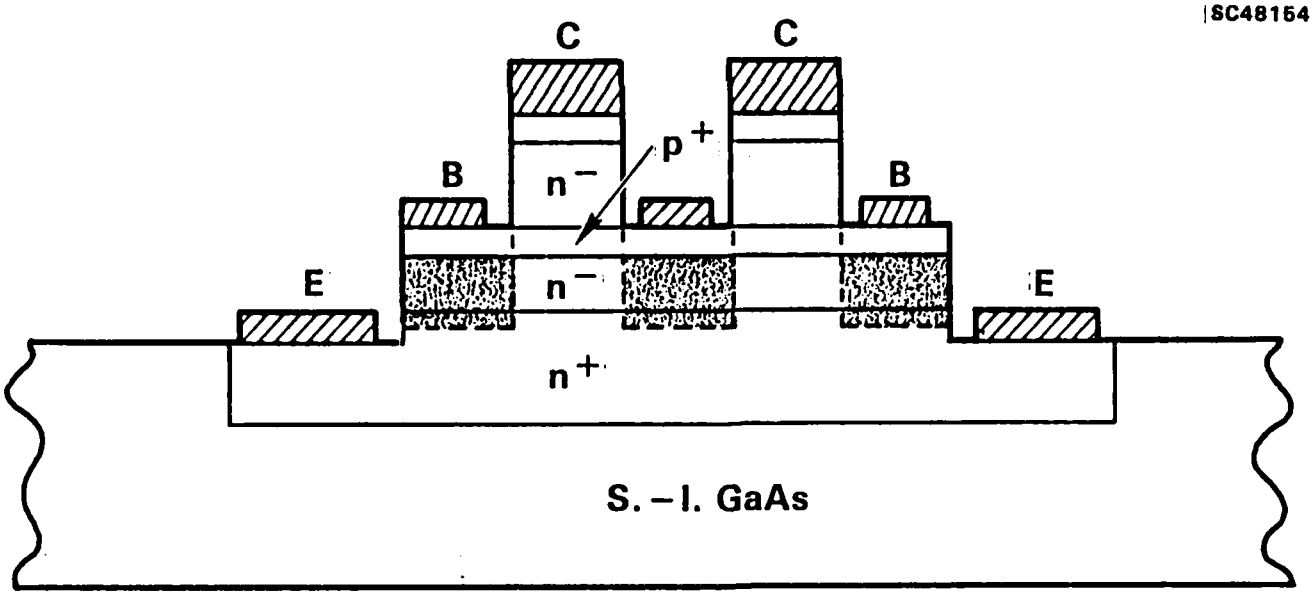
OUTLINE

- COLLECTOR-UP FABRICATION AND RESULTS
- EMITTER-UP FABRICATION AND RESULTS
- DEVICE AND CIRCUIT MODELING
- HBT PROGRESS AT LOWER FREQUENCIES

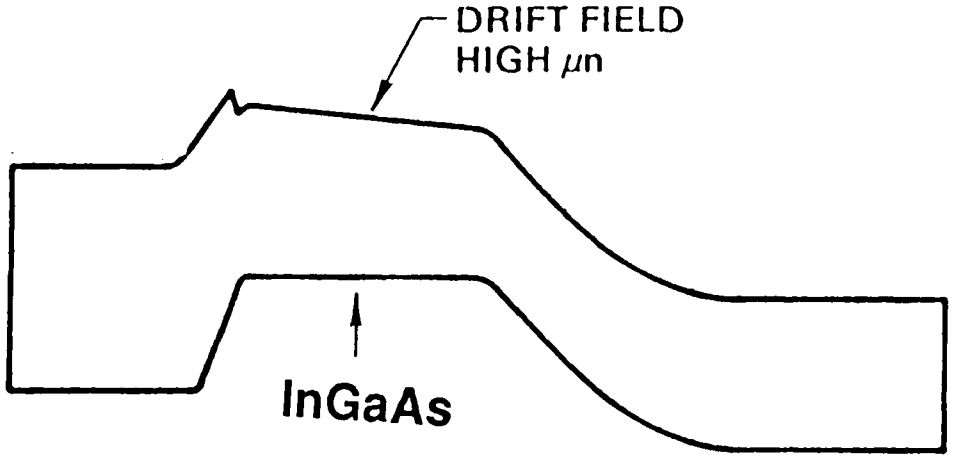
C-UP HBT FABRICATION CHALLENGES

- ETCHING OF COLLECTOR MATERIAL IN BASE CONTACT AREAS
- SUPPRESSION OF EMITTER INJECTION UNDER BASE CONTACTS

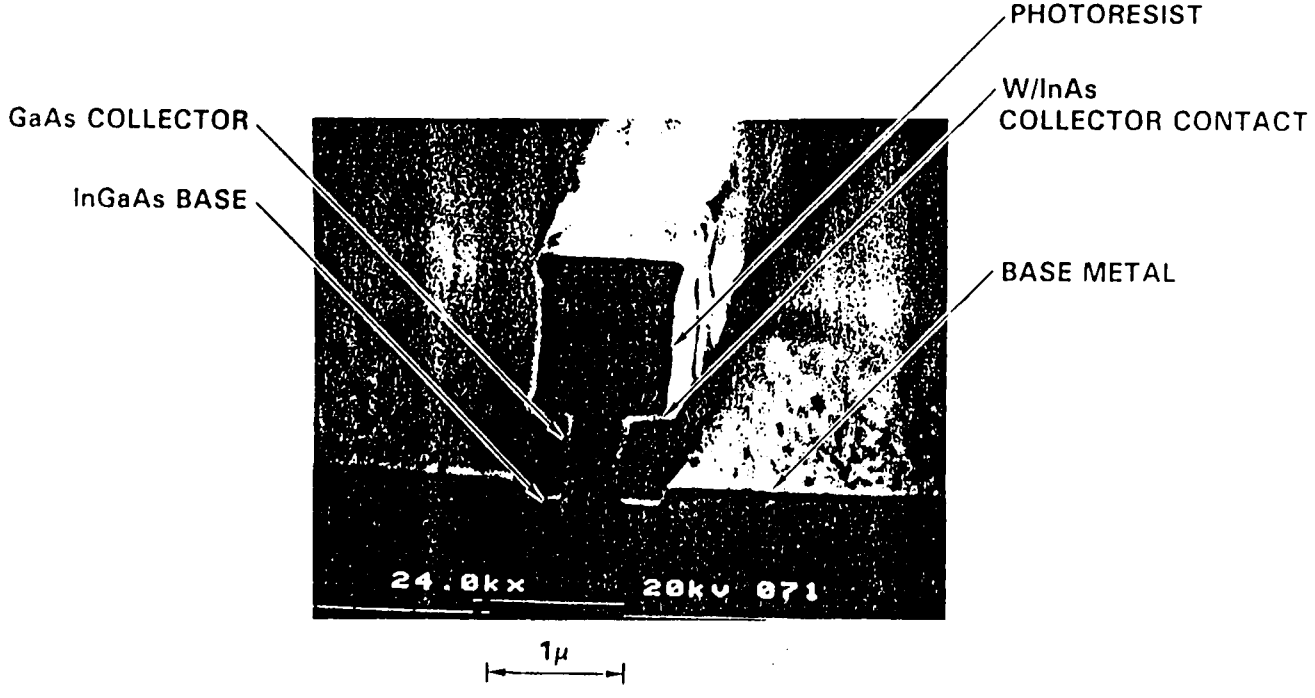


APPROACH TO BASE ETCH

InGaAs IS ETCH STOP FOR RIE

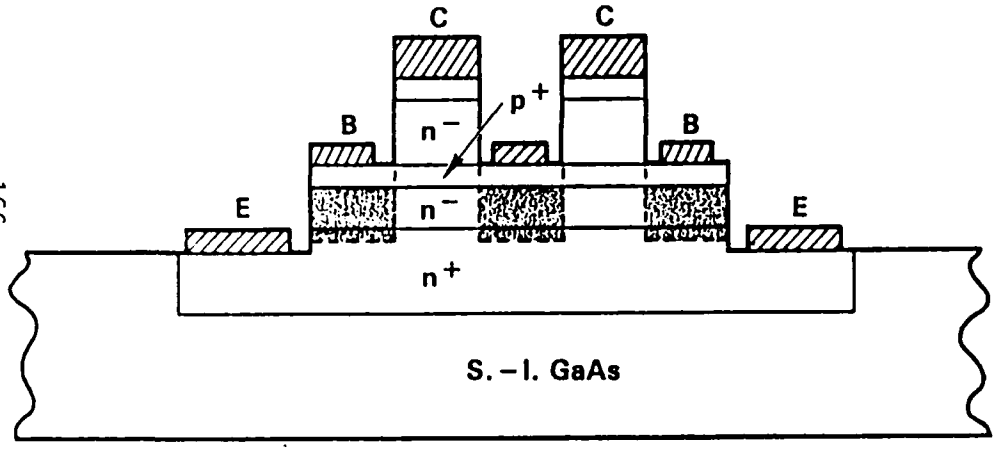


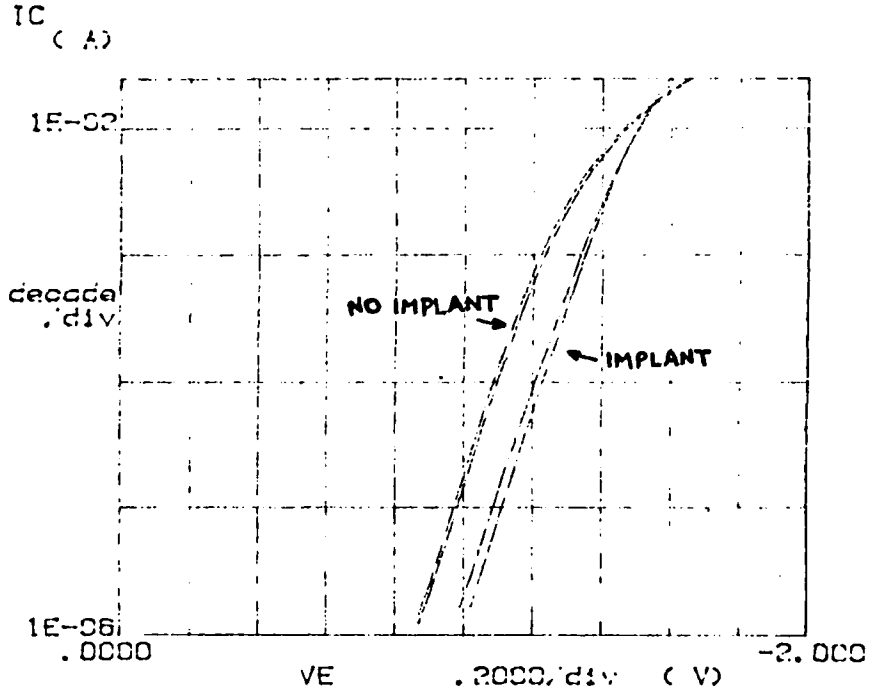
SC41684



APPROACH TO SUPPRESS INJECTION UNDER CONTACTS

SELF-ALIGNED PROTON BOMBARDMENT REDUCES INJECTION BY x10



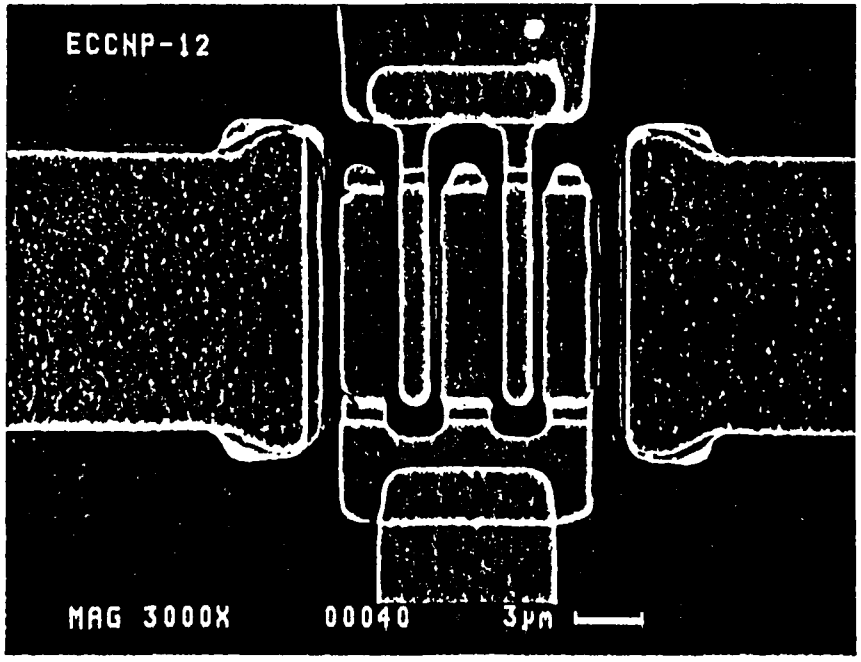


I-V Characteristics of Test B-E Diodes

COLLECTOR-UP HBT

SC48142

C



E E

B

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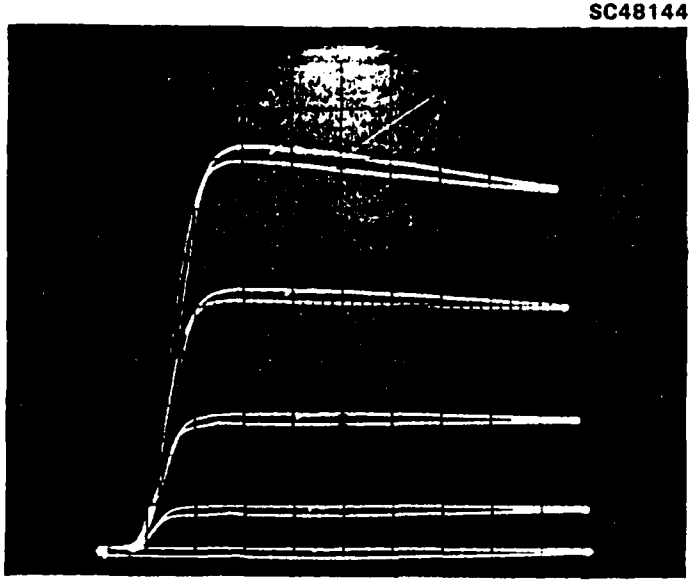
COLLECTOR-UP HBT — I-V CHARACTERISTICS

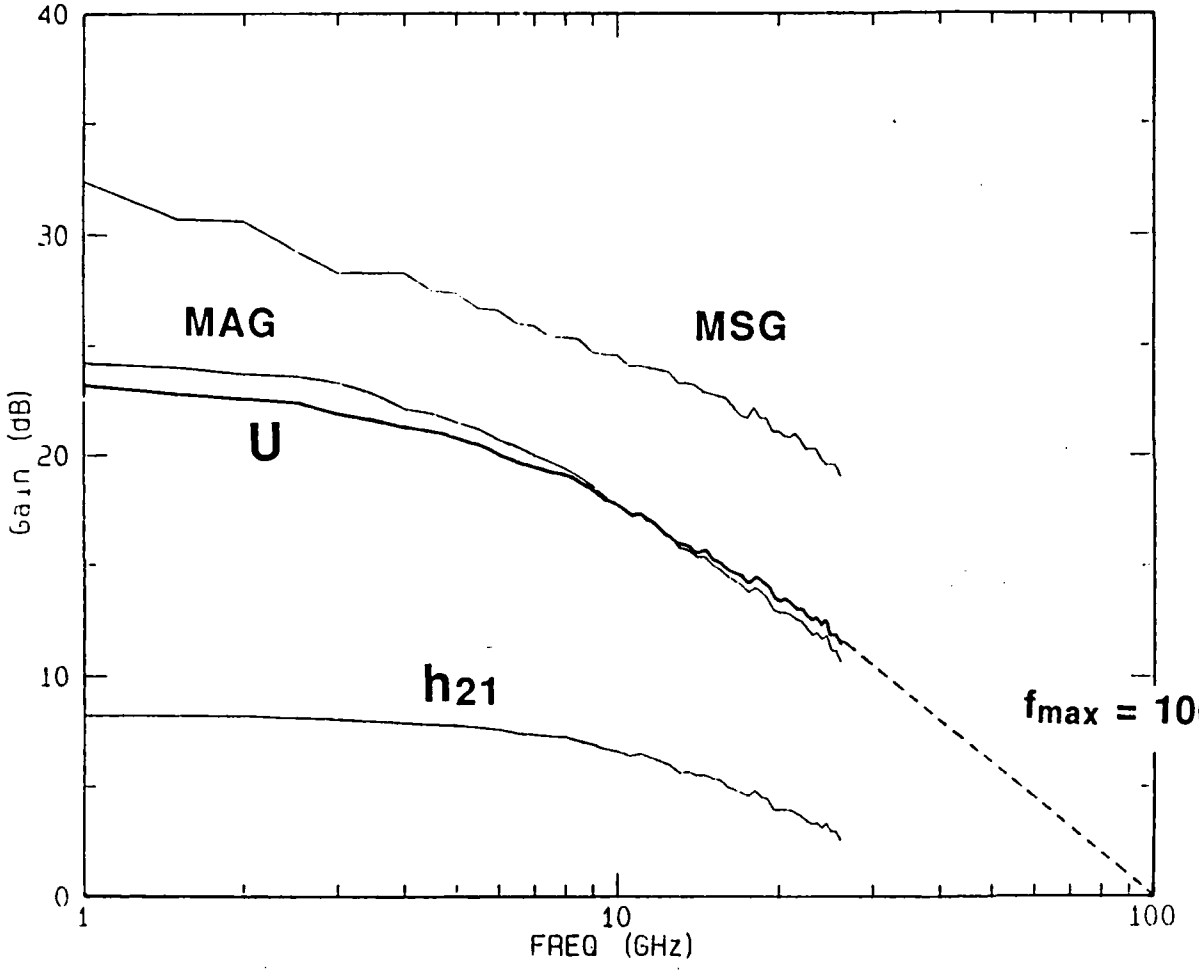
COLLECTOR AREA: 2μm × 10μm × 2

SC48144



I_C : 2mA/DIV
V_{CE} : 0.5 V/DIV
I_B : 0.5 mA/STEP

COLLECTOR - UP HBT
RF GAIN

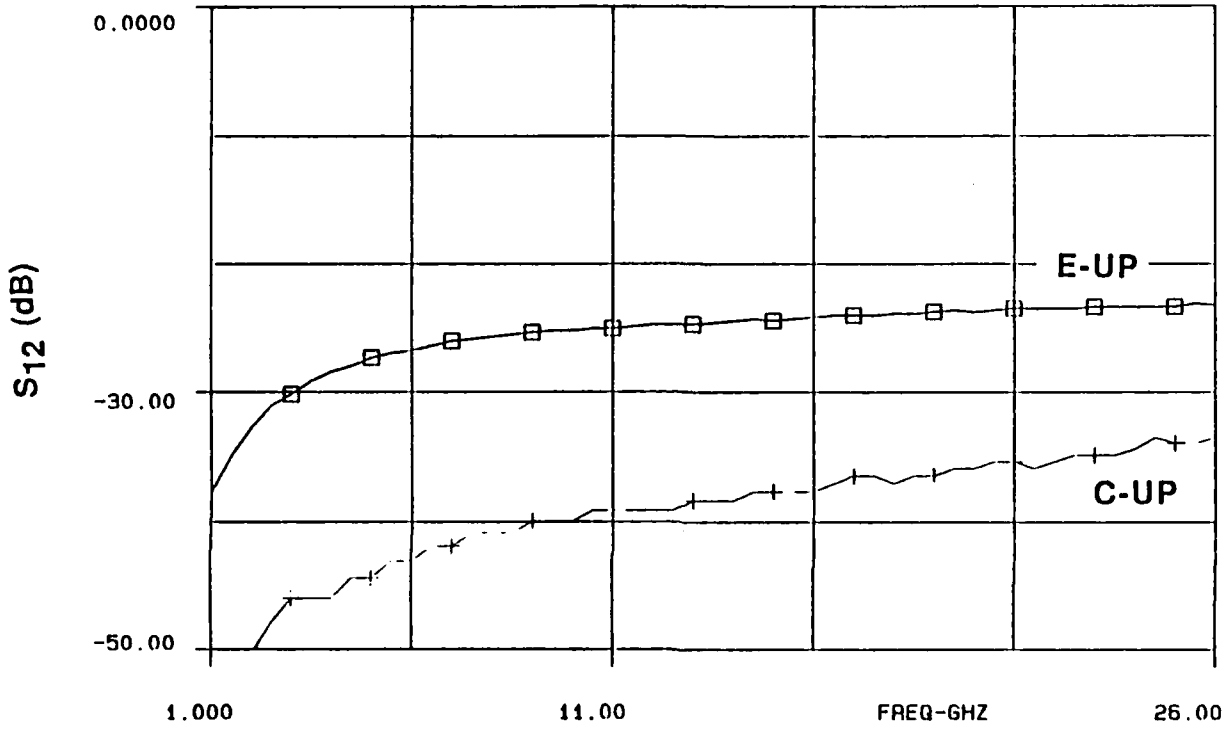


f_{max} = 100 GHz

HIGHEST fmax: 100 GHz
(ft > 35 GHz)

HIGHEST ft: 65 GHz
(fmax ~ 52 GHz)

COMPARISON OF S_{12} IN C-UP AND E-UP HBTs



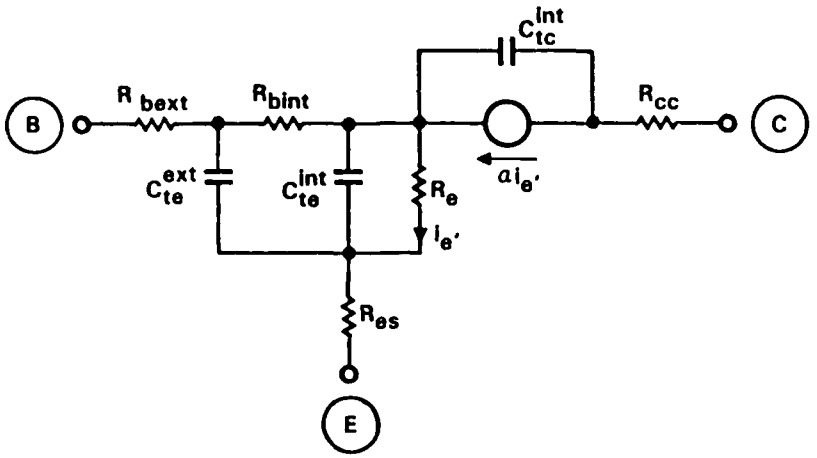
UNILATERAL FIGURE-OF-MERIT

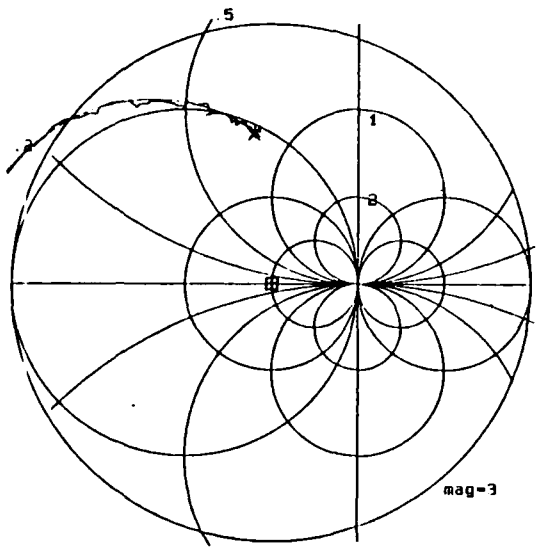
$$\mu = \frac{|S_{11}\, S_{12}\, S_{21}\, S_{22}|}{(1 - |S_{11}|^2)(1 - |S_{22}|^2)}$$

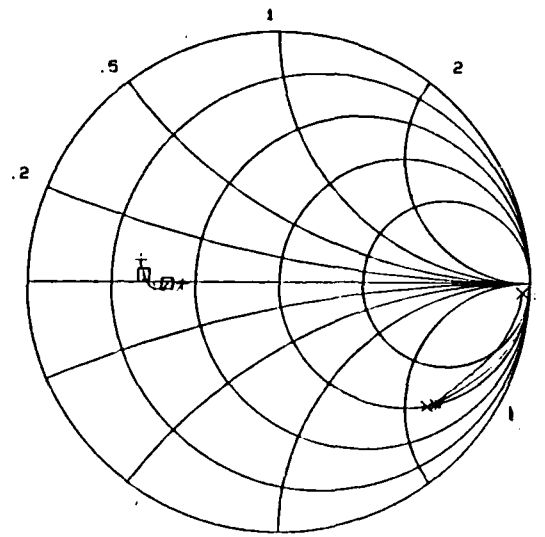
		μ @ 20 GHz
HEMT	f_{max} = 100 GHz	0.46
E-UP	HBT	0.12
C-UP	HBT	0.06

(want small μ for best isolation)

C-UP HBT MODEL



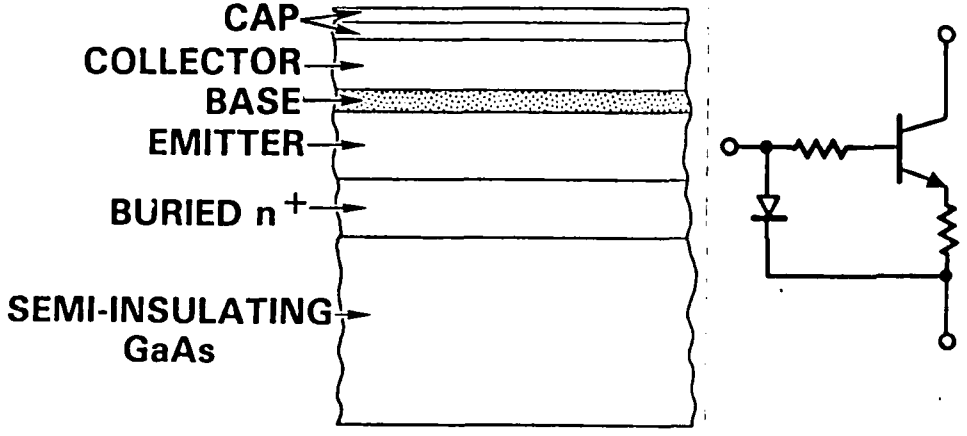


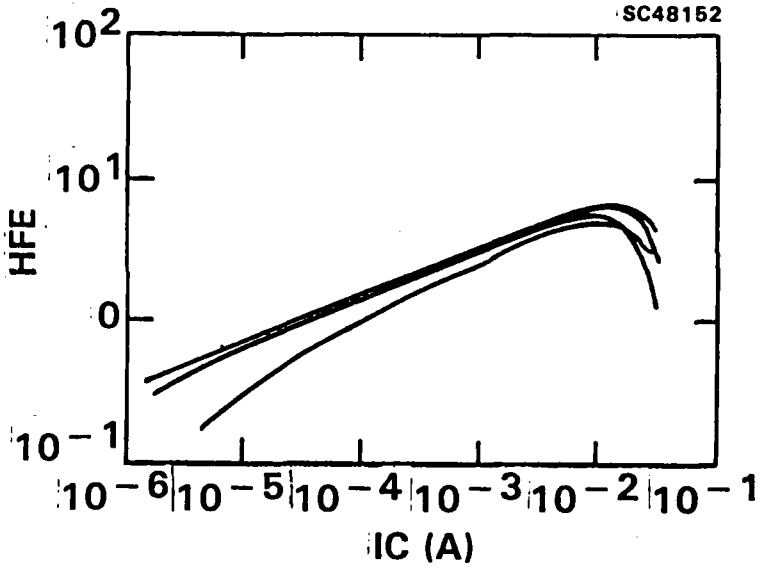


C_{TC}	=	14 fF	α_o	=	0.7
C_{TEi}	=	240 fF	T_B	=	1.8 pS
C_{TEe}	=	22 fF	T_C	=	0.6 pS
R_{vext}	=	6.3	L_e	=	5 pH
R_{bint}	=	4.2	L_b	=	26 pH
R_{es}	=	1.2	L_c	=	20 pH
R_{cc}	=	4.5			

REMAINING ISSUE

EMITTER STRUCTURE DESIGN TO DECREASE R_E





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THE FUTURE OF C-UP HBT TECHNOLOGY

1. BASE DOPING CAN BE INCREASED SIGNIFICANTLY (GROWTH ORDER FAVORS LOW T GROWTH)

2. EMITTER LAYER STRUCTURE CAN BE IMPROVED SIGNIFICANTLY ==> HIGHER H_{21}, lower R_E

3. SELF-ALIGNED COLLECTOR AND EMITTER CONTACTS CAN BE IMPLEMENTED

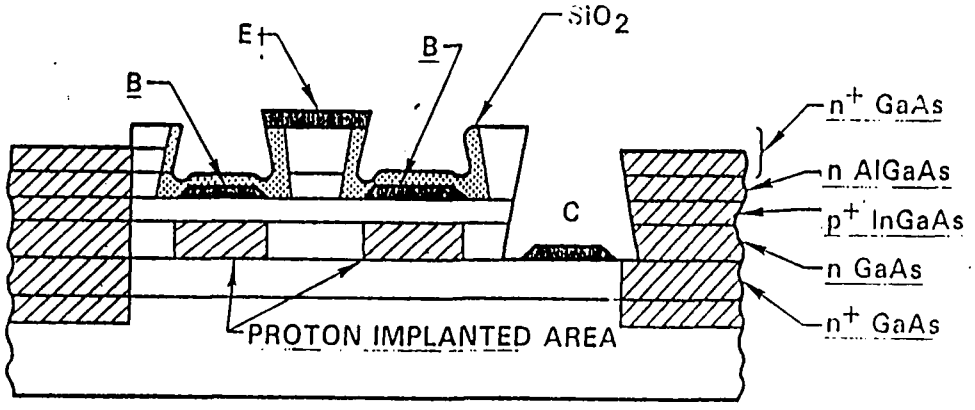
EXPECT f_{max} > 300 GHz WITH 1 μm DIMENSIONS

E-UP FABRICATION CHALLENGES

- MINIMIZE BASE RESISTANCE
- MINIMIZE BASE-COLLECTOR CAPACITANCE

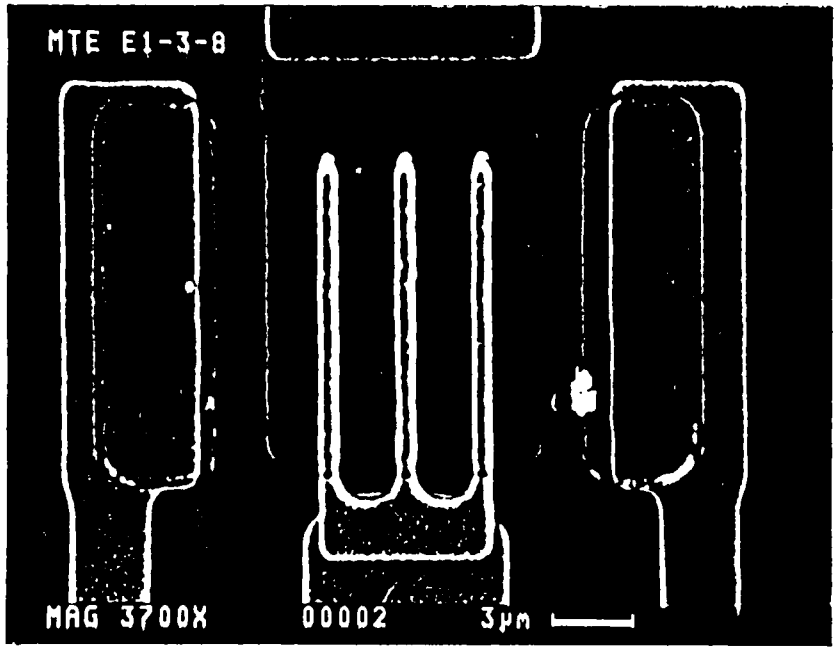
APPROACH

- ULTRAHIGH BASE DOPING (1 X 10^{20} CM^{-3})
- FULLY SELF-ALIGNED PROCESS
- PROTON-IMPLANTS IN EXTRINSIC COLLECTOR

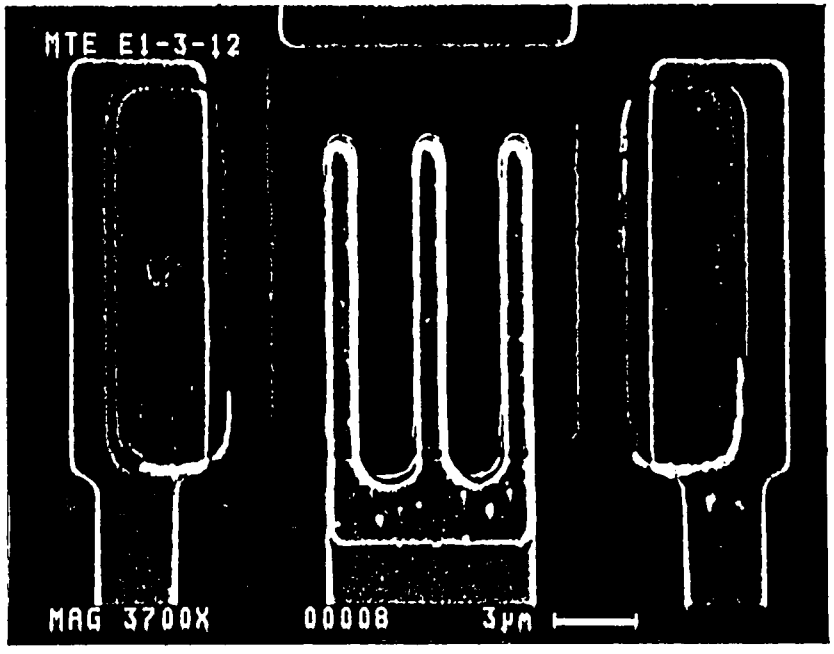


MASK SET MB1
PROJECTION OPTICAL LITHOGRAPHY

SC48146



$W_E = 0.8\mu m$



$W_E = 1.2\mu m$

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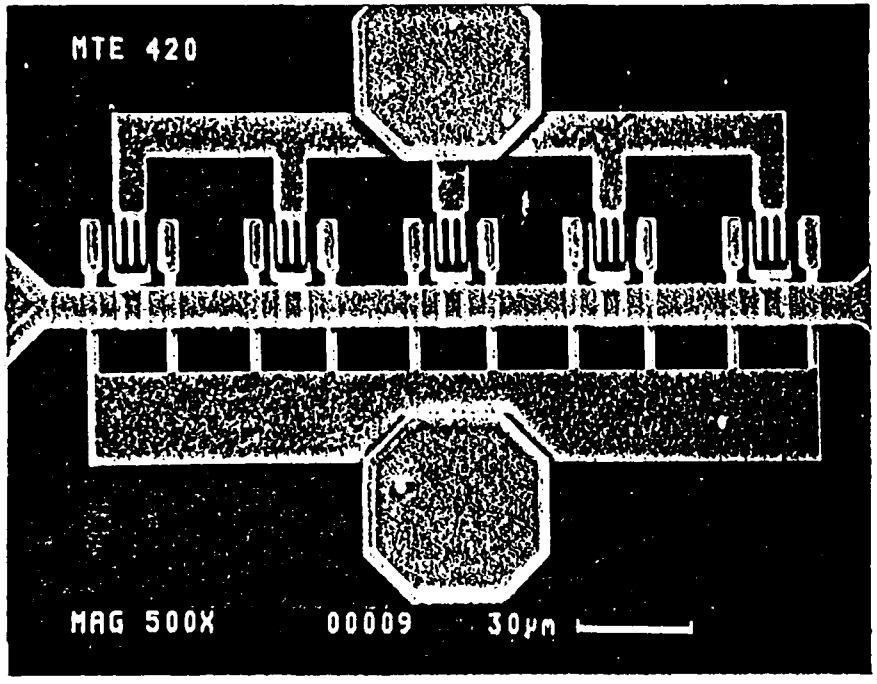
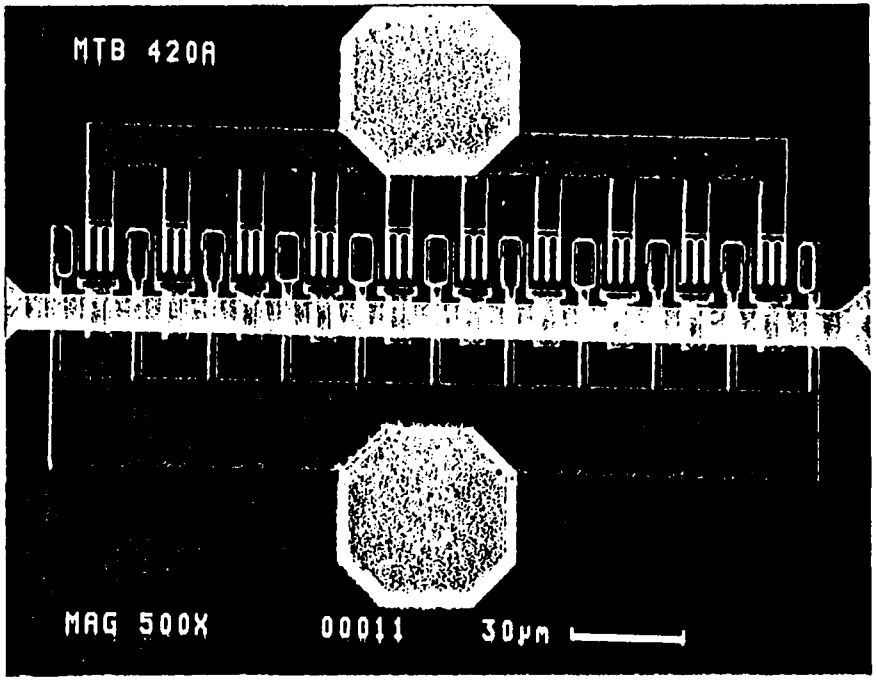
EXPERIMENTAL VARIATIONS

SC48145

COMMON EMITTER — COMMON BASE
MULTIPLE CELLS
VARIATIONS IN SPACING





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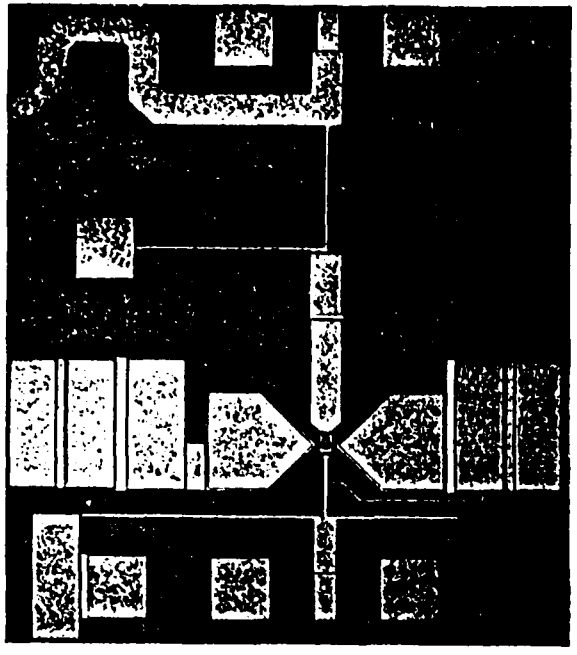
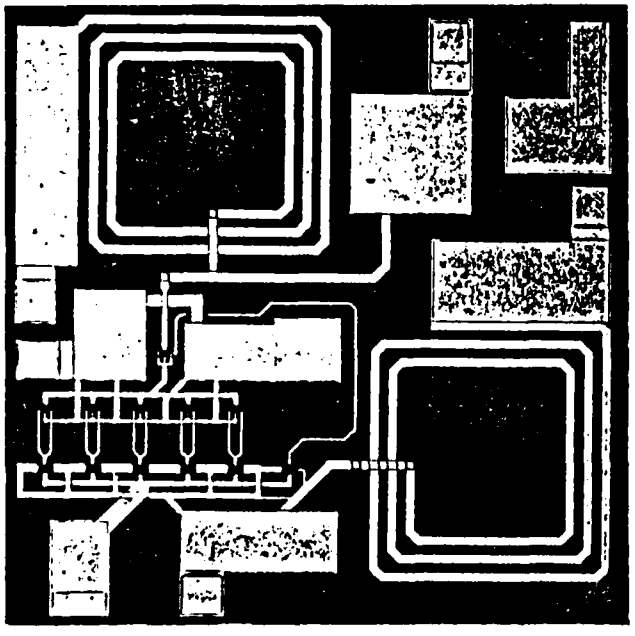
HBT MMIC TECHNOLOGY

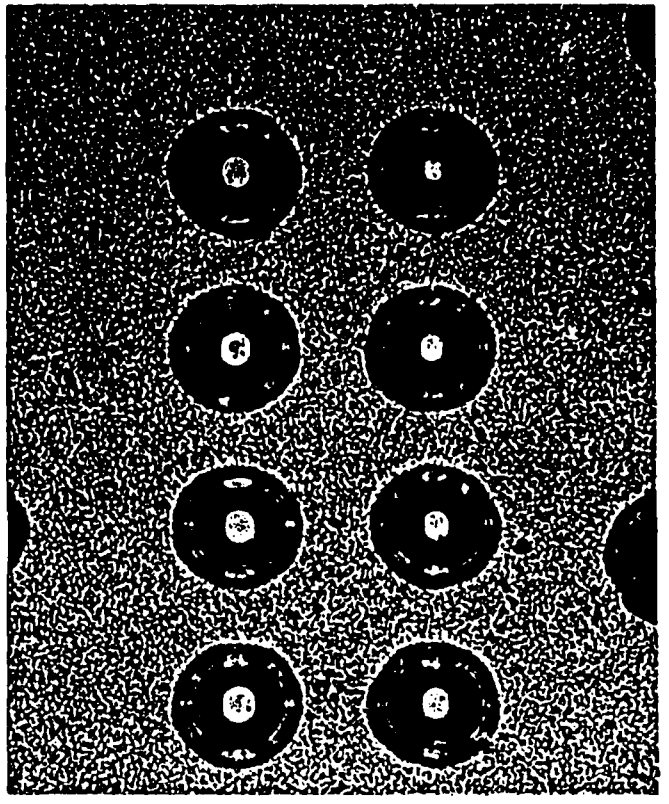


22 GHz
AMPLIFIER



10 GHz
AMPLIFIER

SC48143



THROUGH-SUBSTRATE
VIA HOLES

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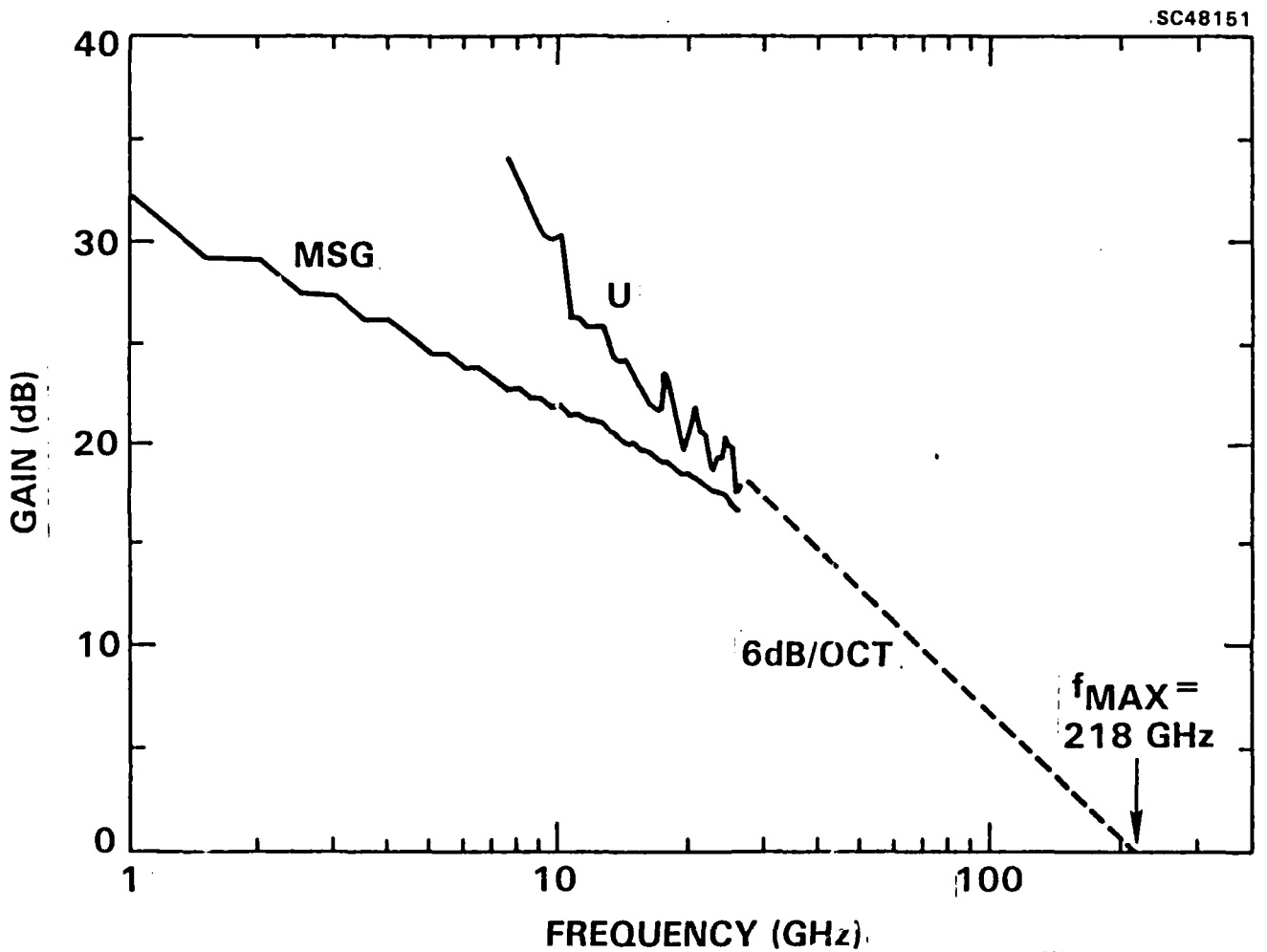
GAIN VS FREQUENCY — COMMON-BASE HBT

EMITTER AREA: $1.0\mu m \times 10\mu m \times 3$, $I_C = 20mA$, $V_{CB} = 0V$



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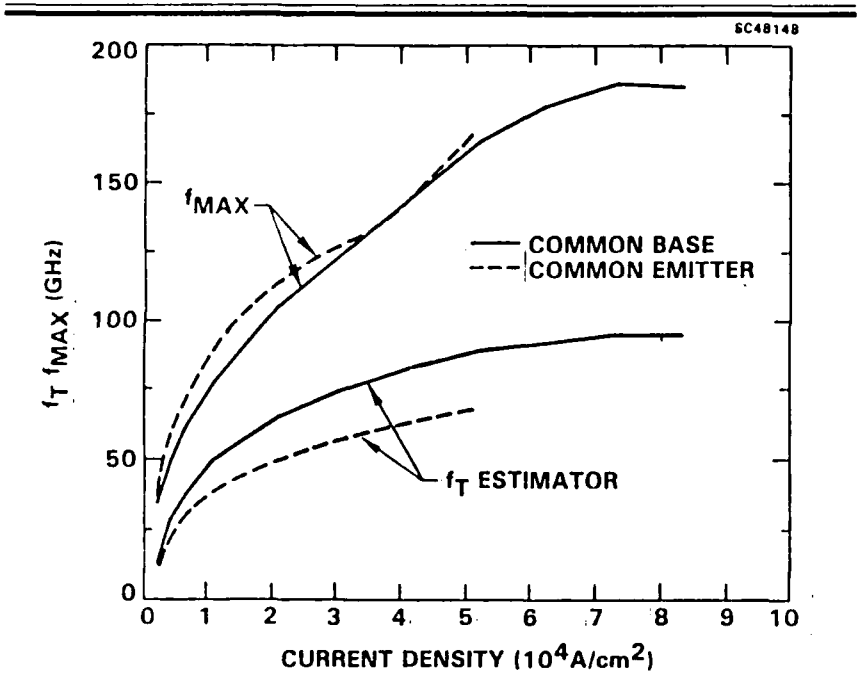
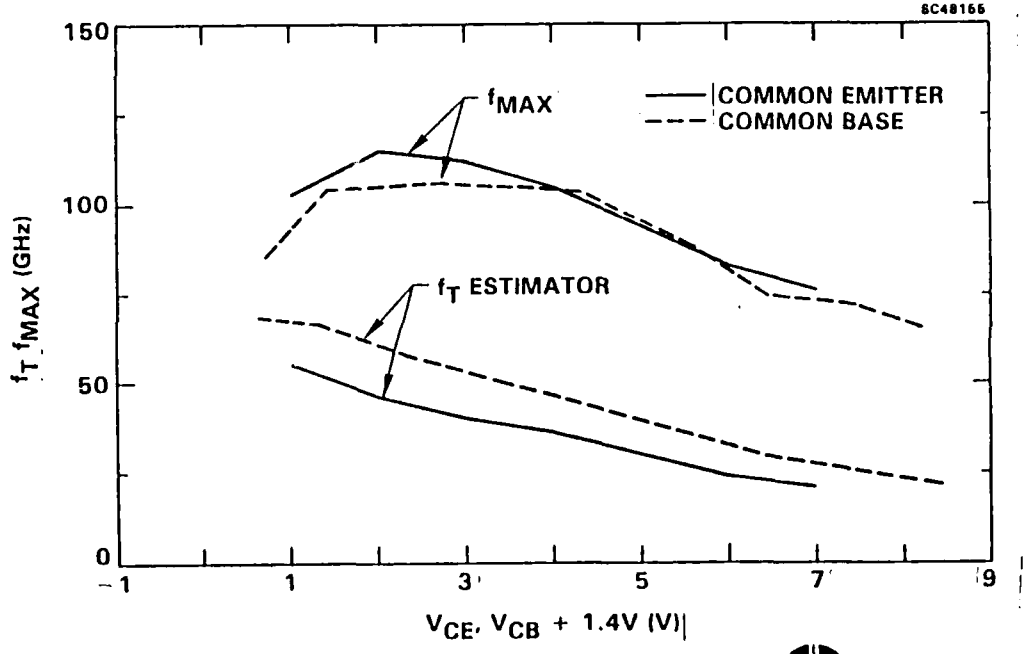
VARIATION OF GAIN WITH J_C





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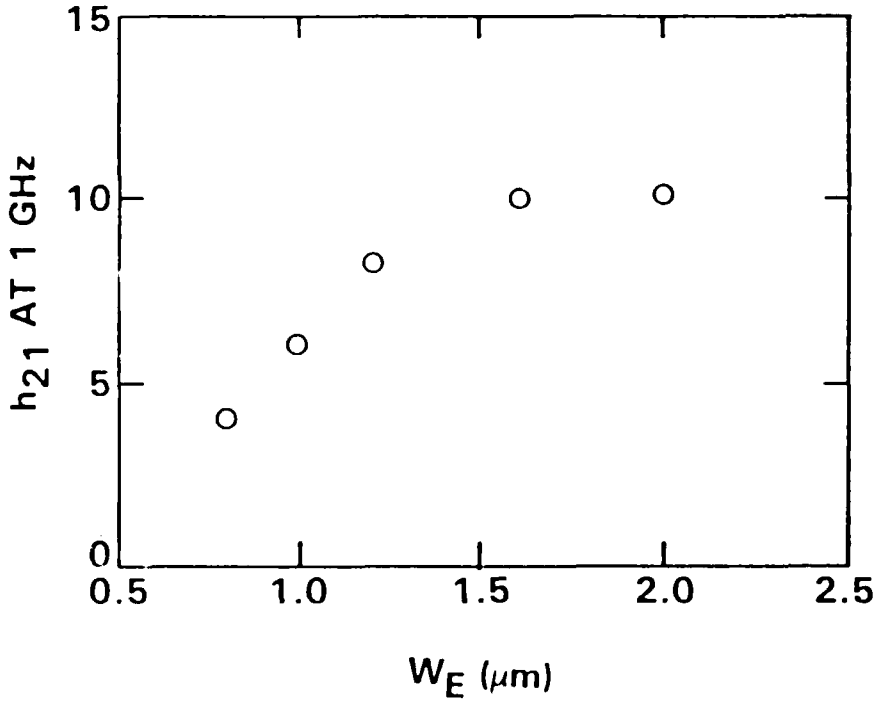
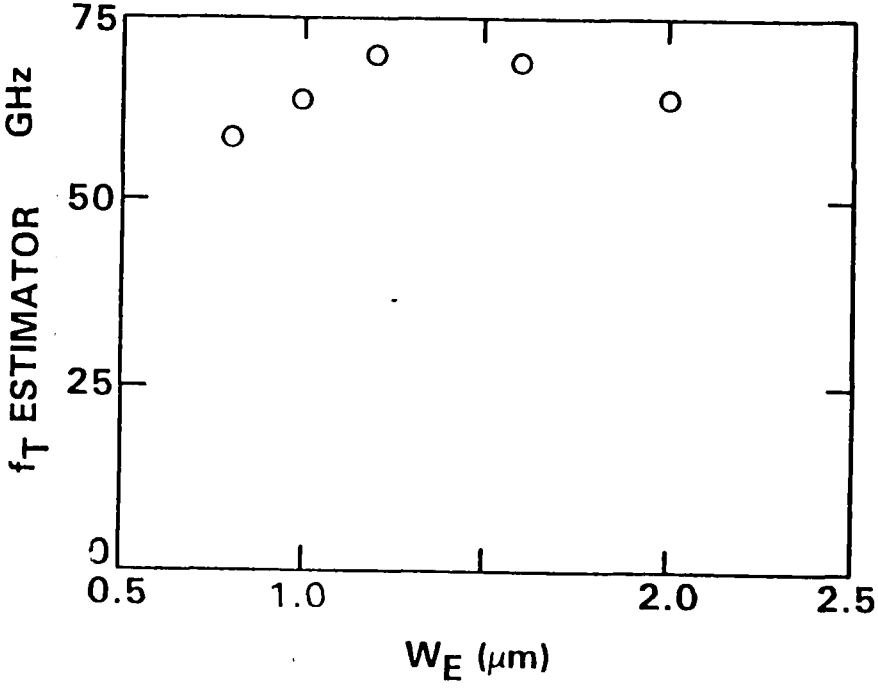
GAIN VS EMITTER WIDTH

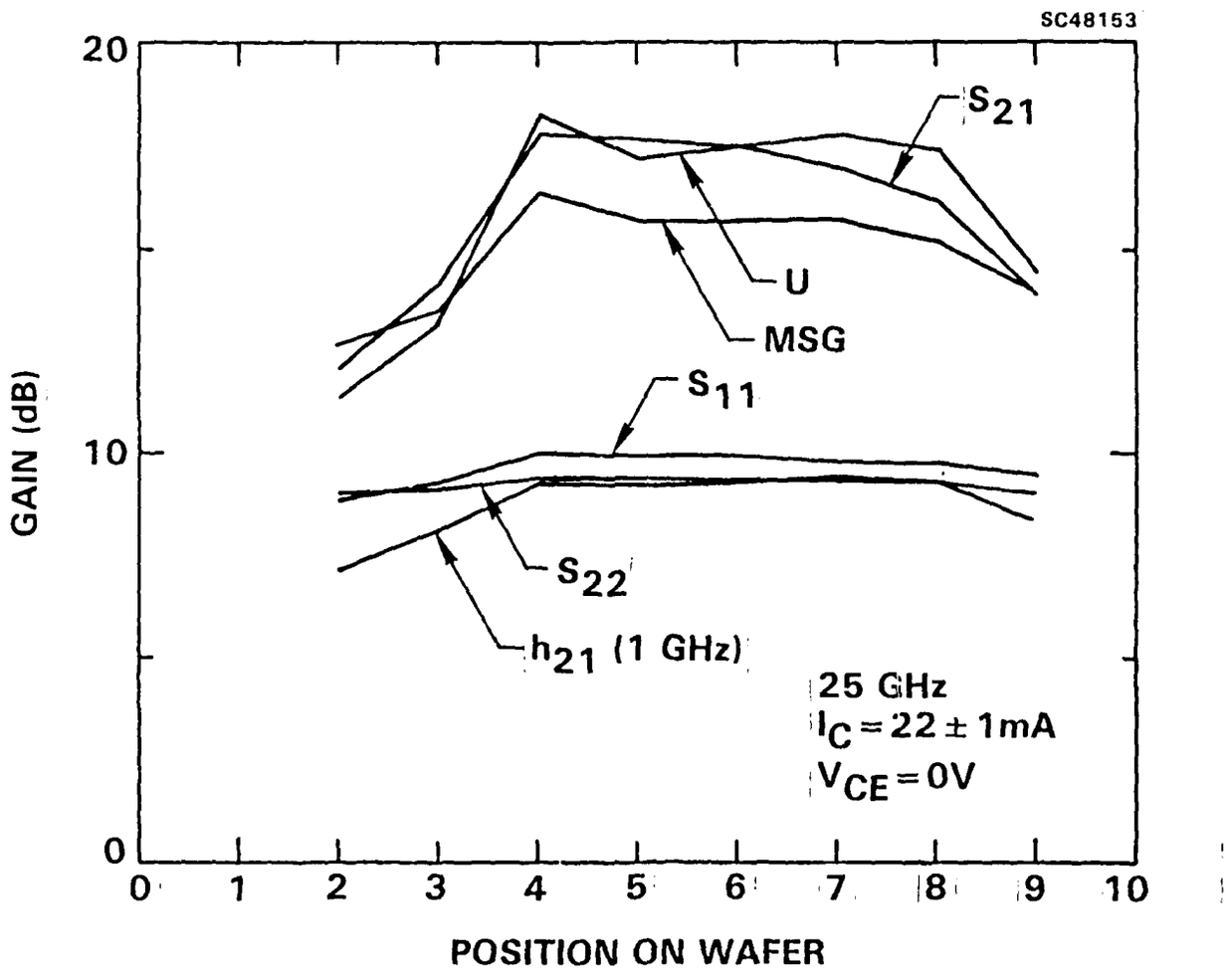
SMALLER EMITTER WIDTH

- LOWERS R_b, INCREASES f_{max}
- DECREASES dc CURRENT GAIN (MAKING EXTRAPOLATION TO 26 GHz LESS RELIABLE)
- MAKES PAD CAPACITANCE PROPORTIONALLY MORE IMPORTANT
- (2 UNIT CELLS GIVE f_t, f_{max} HIGHER THAN ONE CELL)





VARIATION OF GAIN ACROSS A WAFER



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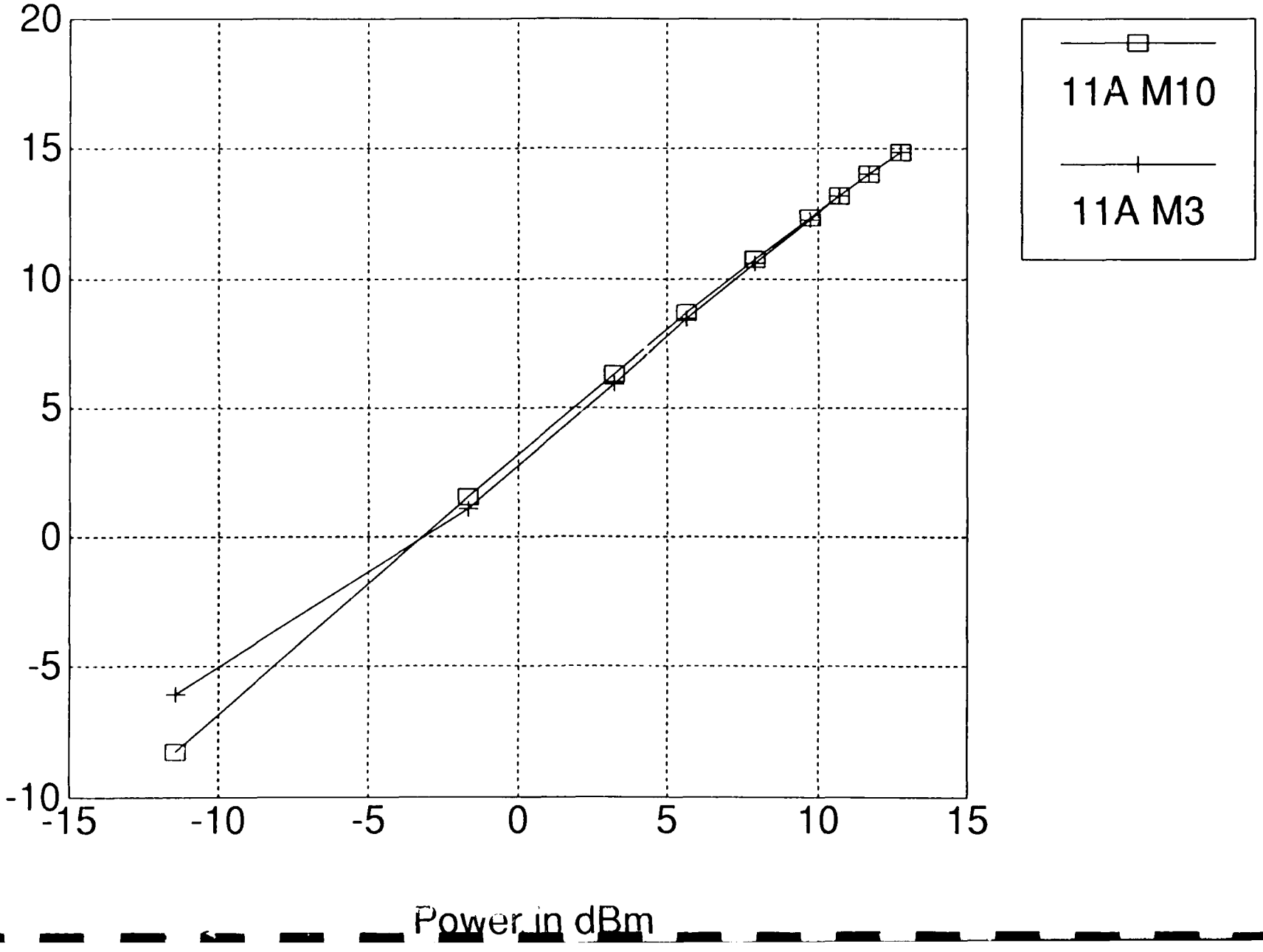
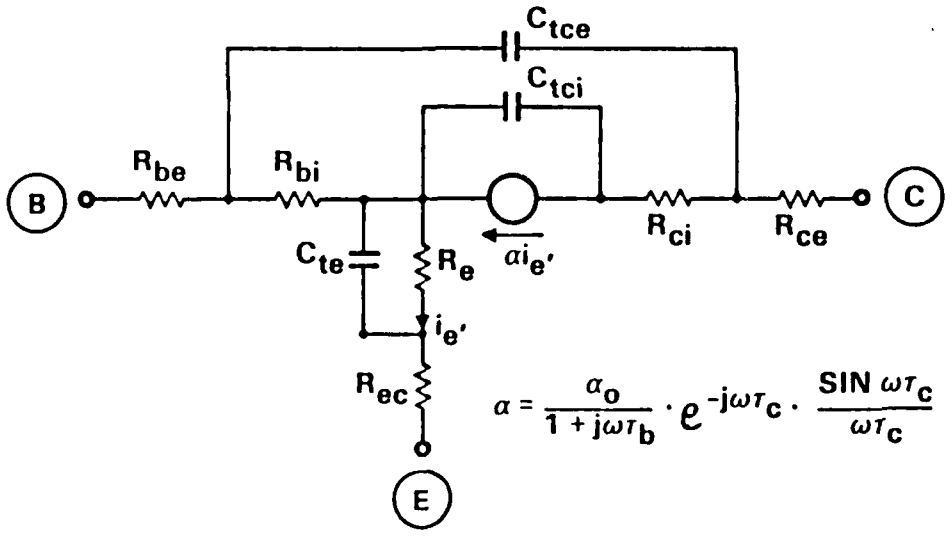
58.5 GHZ HBT

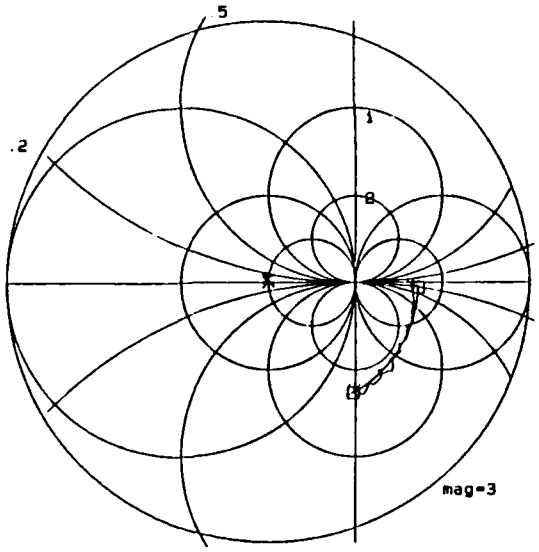

20
15
10
5
0
-5
-10
-15
-10
-5
0
5
10
15
Power OUT dBm
Power in dBm
11A M10
11A M3

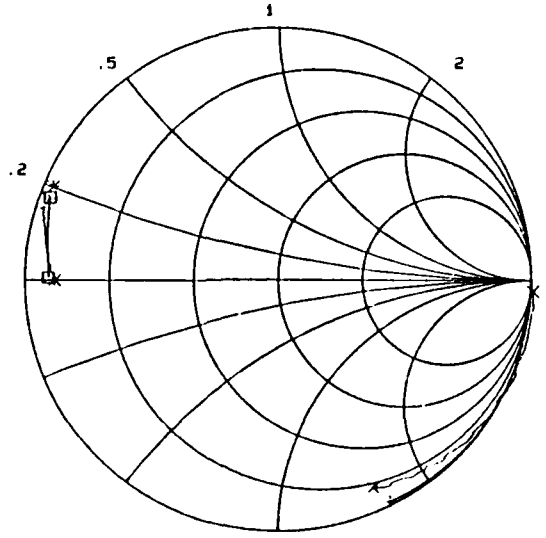
CM
0
1
2
3
4
5
6
7
8
9
10

HBT MODEL



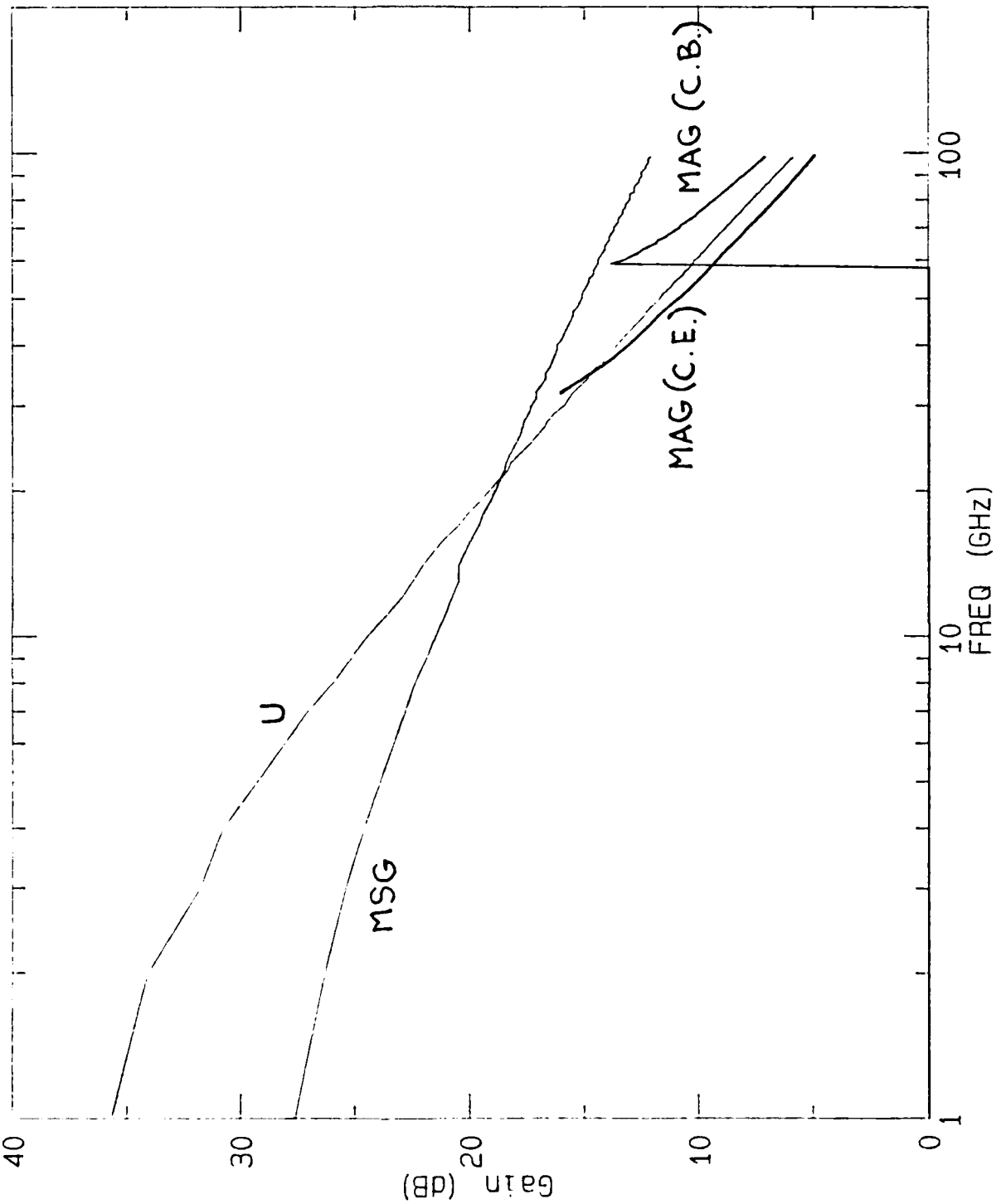
$$\alpha = \frac{\alpha_o}{1 + j\omega\tau_b} \cdot e^{-j\omega\tau_c} \cdot \frac{\text{SIN}\ \omega\tau_c}{\omega\tau_c}$$





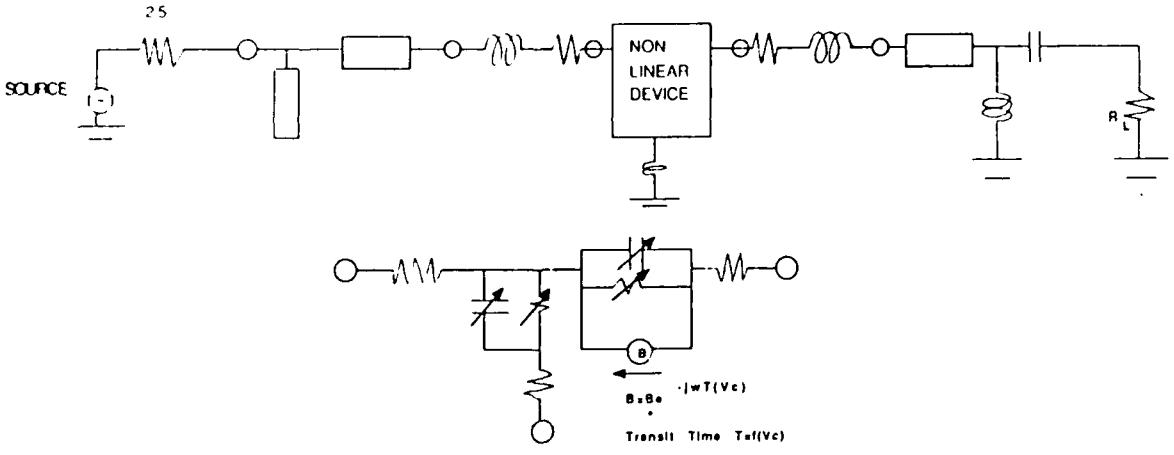
C_{TE}	=	150 fF	α_o	=	0.9
C_{TCi}	=	8 fF	T_b	=	0.4 pS
C_{TCe}	=	29 fF	T_c	=	0.4 pS
R_{bext}	=	1.9	R_{es}	=	0.8
R_{bint}	=	1.8	R_{cc}	=	12

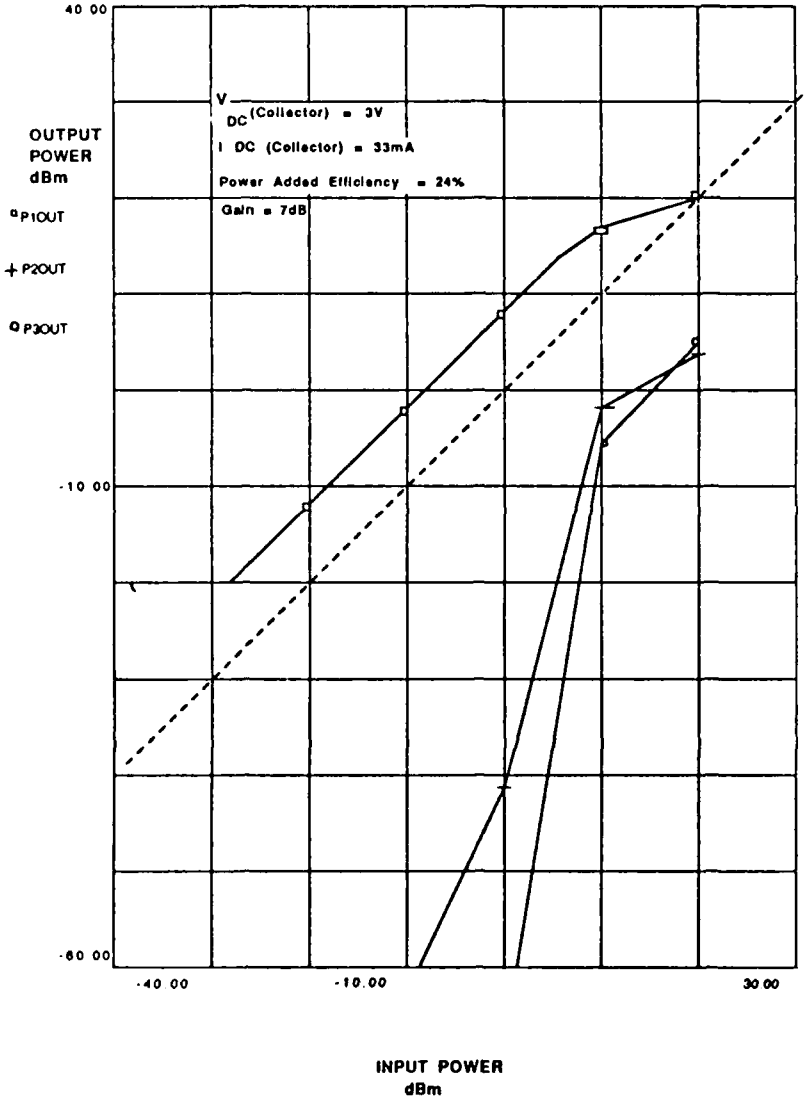
HIGH FREQUENCY MODELING



AMPLIFIER MODELLING

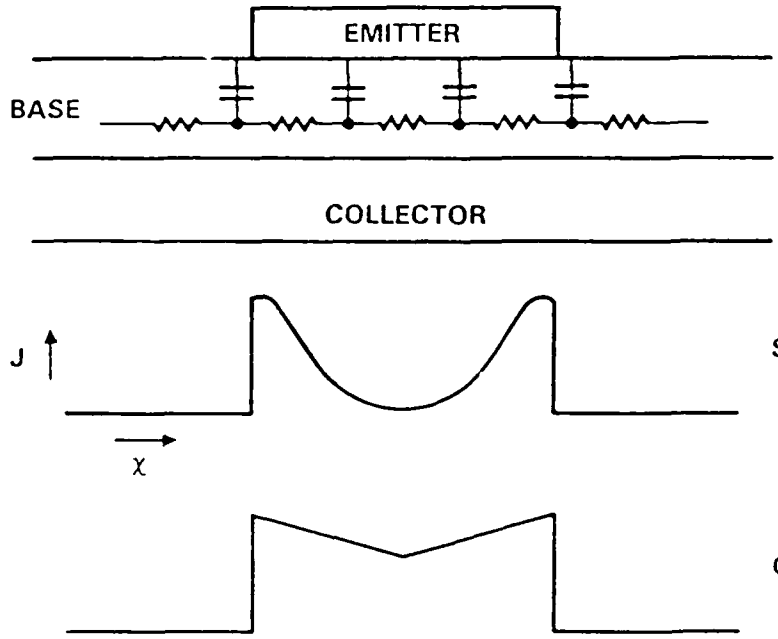
NONLINEAR HBT MODEL

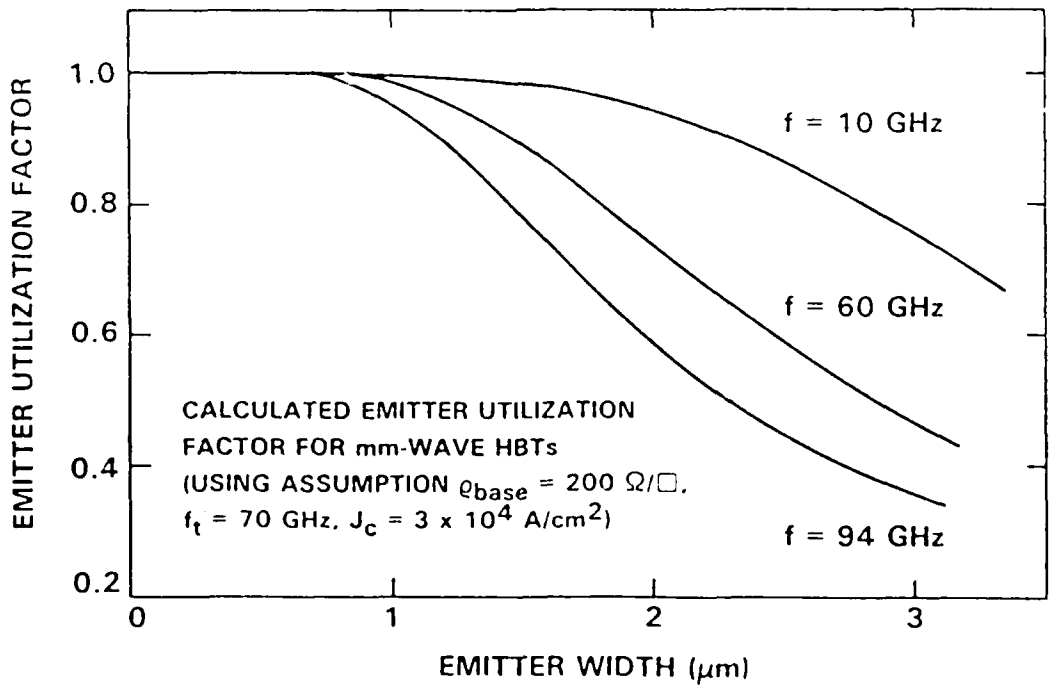




EMITTER UTILIZATION FACTORS

SC47338





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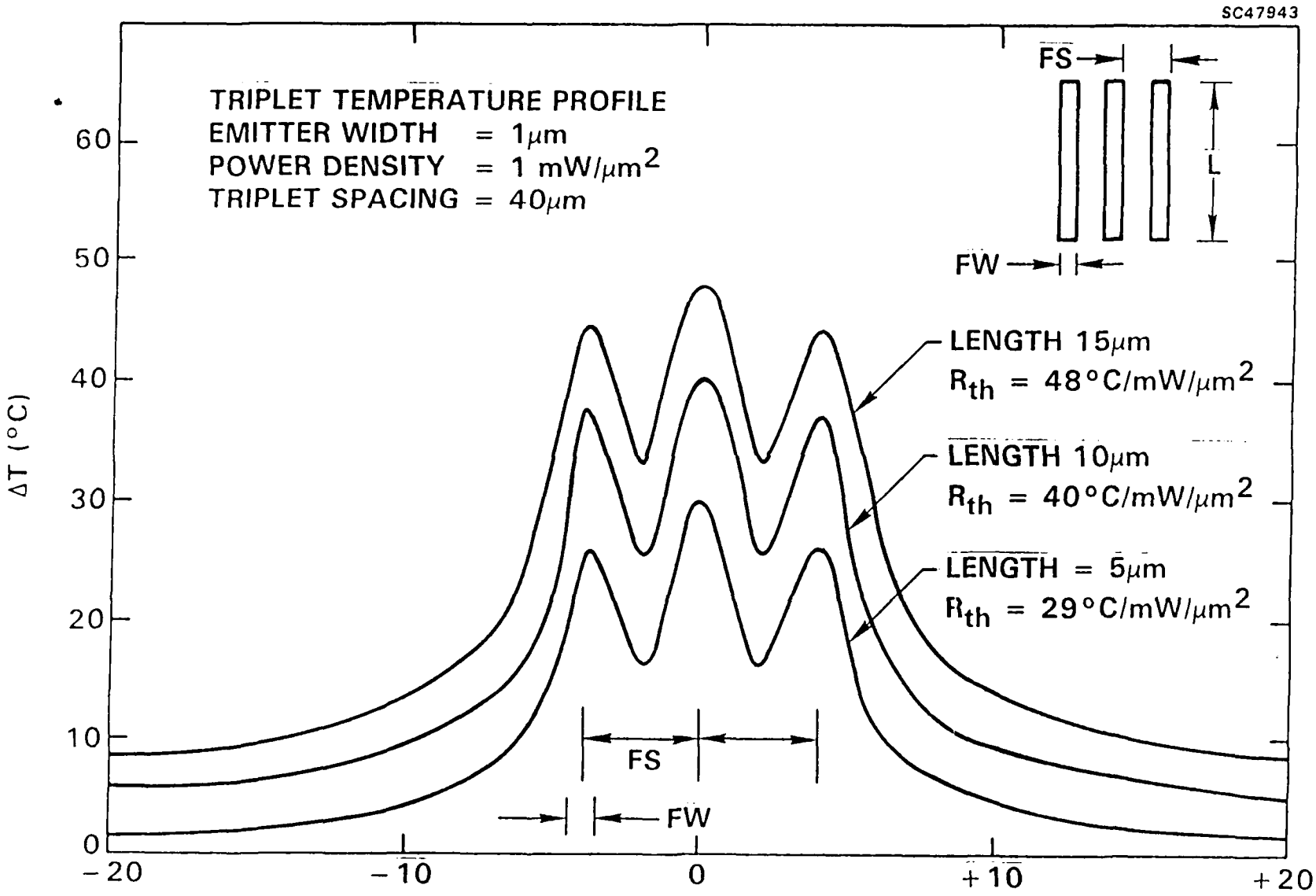

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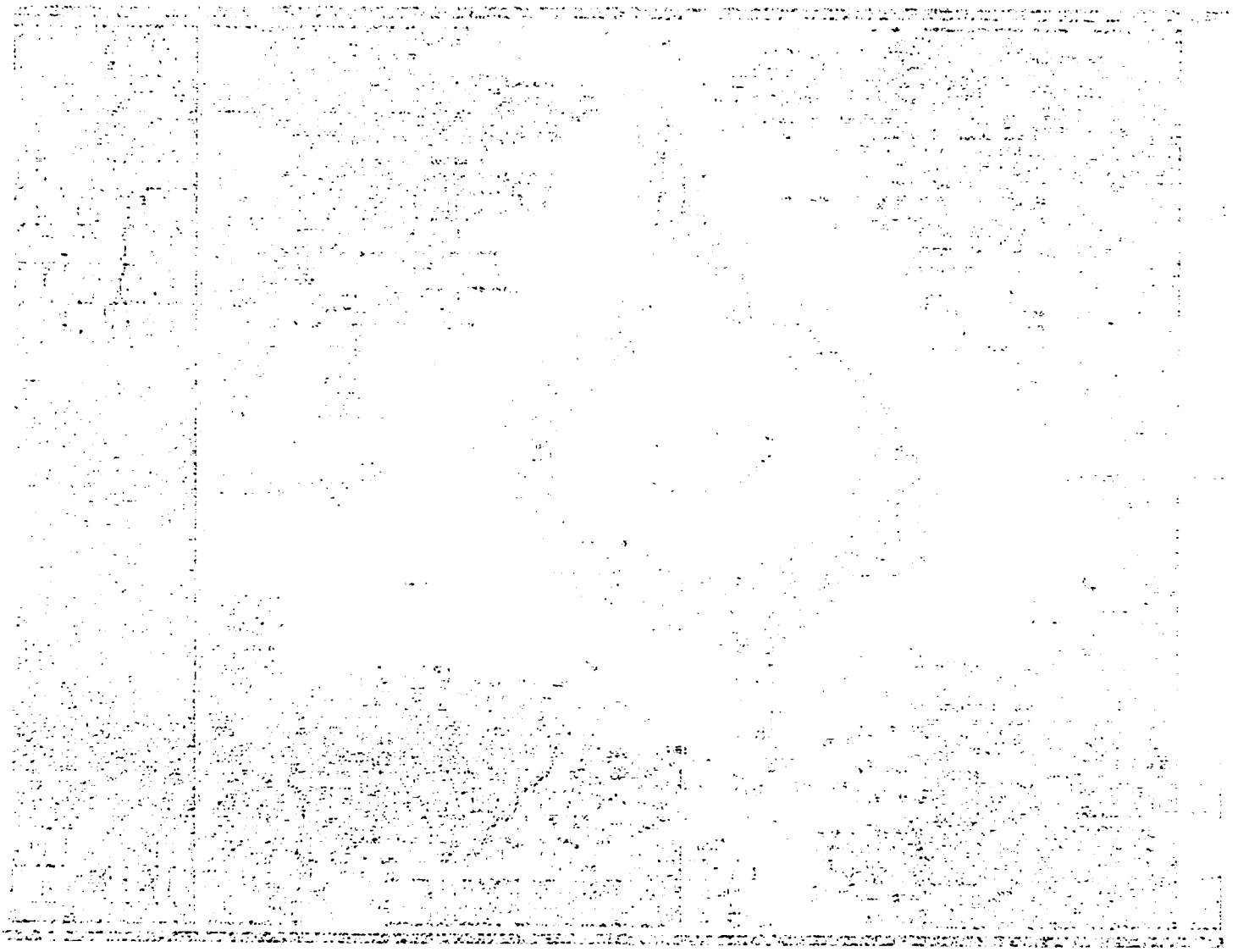
THERMAL IMAGE PROFILE



SEELINK TECHNOLOGY

DEVICE: 17D/5 (Coated) 40x magn.

CONDITIONS:

Base Temperature: 83.6 °C

Power : .1 W

6106 Del Canto dr., SAN JOSE CA-95119

ANALYSIS

EXPERIMENT (THERMAL IMAGING): $31 \pm 5°C\ \mu m^2/mW$

SIMULATION (15 μm SPOT SIZED ASSUMED): $60°C\ \mu m^2/mW$

DISCREPANCY MAY BE DUE TO SURFACE COOLING FROM METALLIZATIONS

PROJECTIONS FOR MM-WAVE OPERATION

FOR BIAS CONDITIONS: $V_{CE} = 4V$, $J_c = 5 \times 10^4\ A/cm^2$

$P_{dc} = 2\ mW/\mu m^2$, $P_{diss} = P_{dc}\ (1-\eta_{add})$

WORST-CASE PROJECTED: $\Delta T = 40°C\ \mu m^2/mW \times 2\ mW/\mu m^2 = 80°C$

PROGRESS SUMMARY

- FIRST HIGH PERFORMANCE MM-WAVE COLLECTOR-UP HBTs DEMONSTRATED - f_{max} = 100 GHz
- EMITTER-UP HBTs IMPROVED TO FMAX = 218 GHz
- MMIC-COMPATIBLE HBT TECHNOLOGY DEMONSTRATED
- PROJECTION OPTICAL LITHOGRAPHY USED
- HIGH FREQUENCY MODELING AND THERMAL MODELING DONE

PLANS

- COLLECTOR-UP HBT IMPROVEMENT:

  HIGHER BASE DOPING — Expect
  IMPROVED EMITTER DESIGN ==> f_{max} > 300 GHz
  FULLY SELF-ALIGNED

- EMITTER-UP HBT IMPROVEMENT:

  HIGHER BASE DOPING: C-SOURCE IN MBE, GROWTH VARIATIONS
  GRADED COMPOSITION BASE — Expect
  VELOCITY OVERSHOOT STRUCTURES ==> f_{max} > 270GHz

- CHARACTERIZATION:

  ADDITIONAL 60 AND 94 GHz RESULTS
  TEST LARGER STRUCTURES
  COLLABORATION WITH STANFORD UNIVERSITY

- AMPLIFIER MODELING:

  REFINE NONLINEAR MODELS FOR HARMONIC BALANCE ANALYSIS

MMW HBT TECHNOLOGY

- EFFICIENT 3-TERMINAL SOLID STATE DEVICES
  - COMMUNICATION SYSTEMS/SEEKERS/PHASE ARRAYS
  - FLEXIBLE CONFIGURATION (E-UP, C-UP, CLASS A, AB, ETC.)
- MANUFACTURABLE, HIGH YIELD TECHNOLOGY
  - BIPOLAR TRANSISTOR TECHNOLOGY
  - STANDARD OPTICAL LITHOGRAPHY
  - COMPATIBILITY WITH GaAs PILOT LINE
- RAPID PROGRESS/CLEAR PATH FOR FUTURE
  - MBE TECHNOLOGY MATURING
  - f_{max} = 215 GHz WITH 1 μm LITHOGRAPHY, f_{max} > 300 GHz EXPECTED

Heterojunction Power FET Technology

Buman Kim

Texas Instruments
Dallas, TX

HETEROJUNCTION POWER FET TECHNOLOGY

OBJECTIVE

DEVELOP A HIGH EFFICIENCY HETEROSTRUCTURE POWER FETs AND AMPLIFIERS FOR OPERATION AT 60 AND 94 GHz

APPROACH

QUANTUM WELL FETs

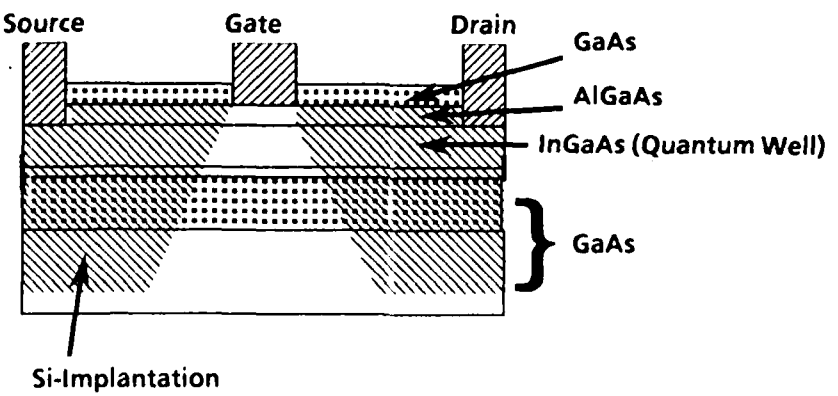
- -- QUANTUM WELL FOR GOOD CHARGE CONFINEMENT
- -- HIGH SHEET CARRIER DENSITY IN A THIN LAYER
- -- UNDOPED AlGaAs LAYER FOR HIGH BREAKDOWN VOLTAGE

STATUS

A 0.25 μm FET at 60 GHz

POWER DENSITY (W/mm)	EFFICIENCY (%)	GAIN (dB)	f_t (GHz)
1.0	27	3.2	120

QUANTUM WELL FET STRUCTURE



HETEROJUNCTION POWER FET TECHNOLOGY

OBJECTIVE

DEVELOP A HIGH EFFICIENCY HETEROSTRUCTURE POWER FETs AND AMPLIFIERS FOR OPERATION AT 60 AND 94 GHz

APPROACH

QUANTUM WELL FETs

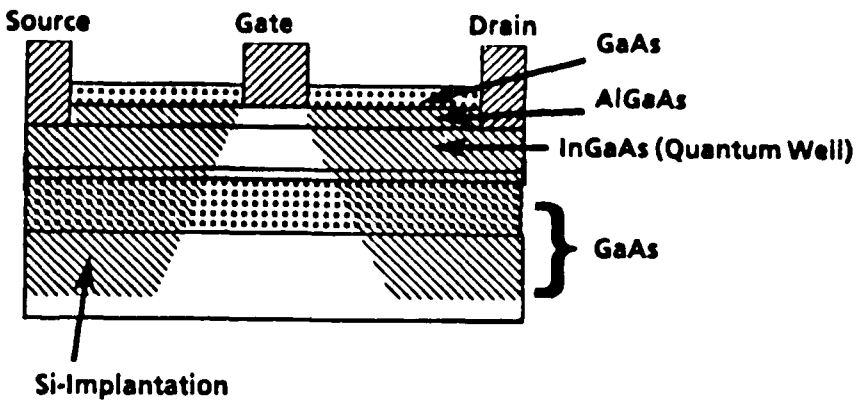
- QUANTUM WELL FOR GOOD CHARGE CONFINEMENT
- HIGH SHEET CARRIER DENSITY IN A THIN LAYER
- UNDOPED AlGaAs LAYER FOR HIGH BREAKDOWN VOLTAGE

STATUS

A 0.25 μm FET at 60 GHz

POWER DENSITY (W/mm)	EFFICIENCY (%)	GAIN (dB)	f_t (GHz)
1.0	27	3.2	120

QUANTUM WELL FET STRUCTURE



HETEROJUNCTION POWER FET TECHNOLOGY

Texas Instruments
Dallas, Texas

Contract No. N66001-86-C-0211

Contract Monitors: Jim Zeidler (NOSC)
Jim Murphy (DARPA)

AGENDA

- Introduction
- Device Design
- Device Performance
  - -- Undoped well
  - -- Doped well
- Summary

OBJECTIVE

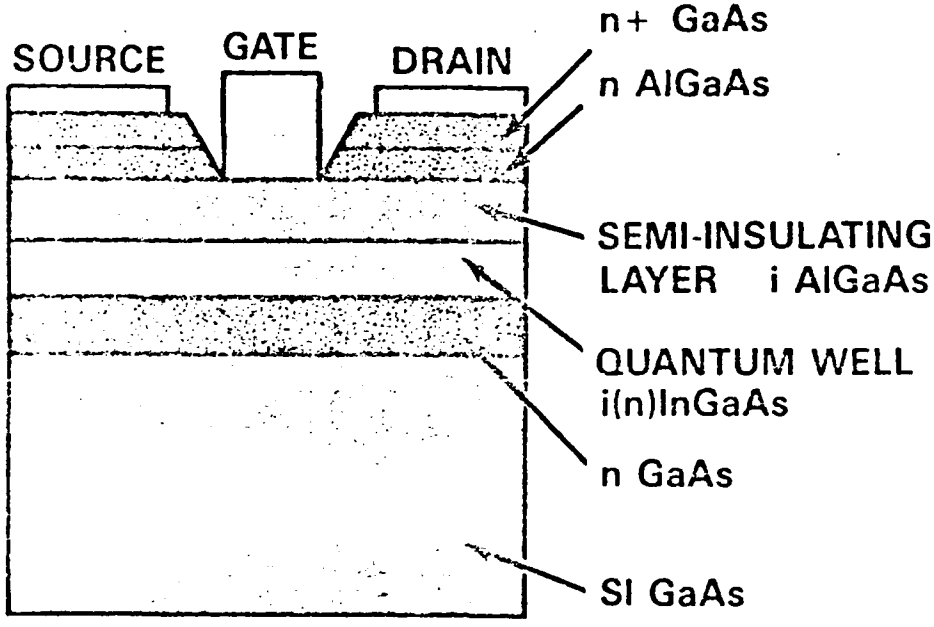
- Develop heterojunction power FETs at 60 GHz and 94 GHz
- Develop amplifiers at 60 GHz and 94 GHz

Frequency (GHz)	60	94	94
Output power (mW)	200	30	100
Efficiency (%)	20	30	20

ISSUES

- CARRIER TRANSIT TIME
  - QUARTER μm OR SUB-QUARTER μm GATES
  - REDUCE PARASITICS
  - BETTER MATERIAL (InGaAs CHANNEL) ←
- SHORT CHANNEL EFFECTS
  - THIN ACTIVE LAYER (UNDER 500 Å)
  - CHARGE CONFINEMENT USING POTENTIAL WELL ← (HETEROINTERFACE)
- POWER DENSITY
  - HIGH SHEET CARRIER DENSITY ←
  - HIGH BREAKDOWN VOLTAGE (MISFET) ←

MILLIMETER-WAVE QUANTUM-WELL MISFET

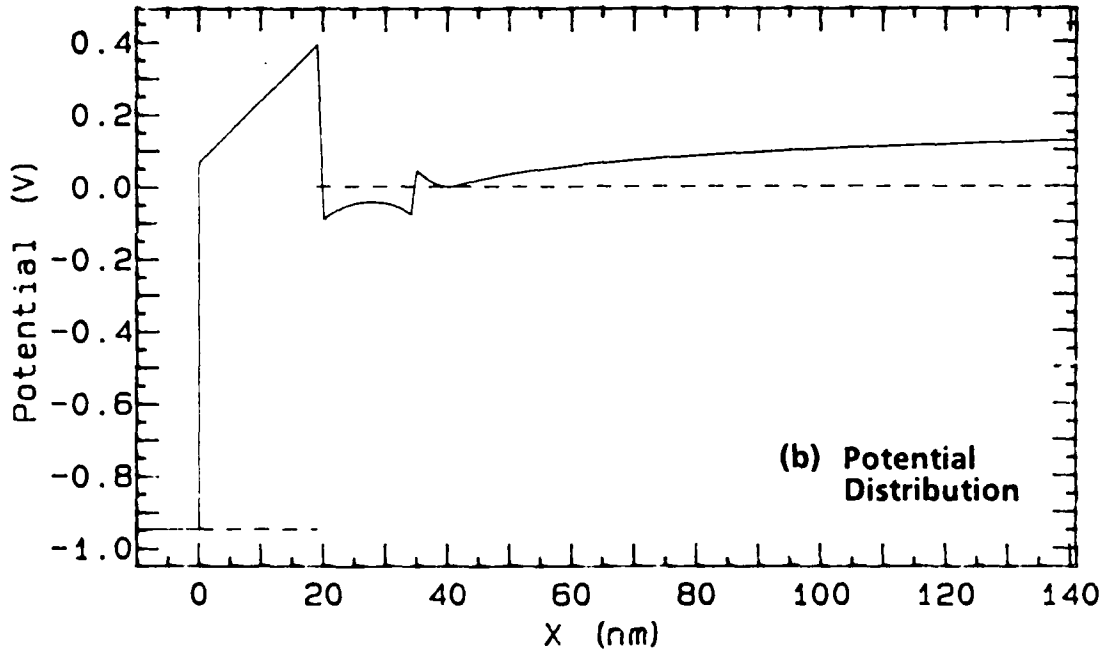


ADVANTAGE

- HIGH BREAKDOWN VOLTAGE
- CHARGE ACCUMULATION
- EXCELLENT CHARGE MODULATION
- SELF-ALIGNED GATE
- SELECTIVE ETCH FOR GATE RECESS

(a) Material Structure

Thickness	Composition	Doping	Electron Density
20 nm	$Al_{0.40}Ga_{0.60}As$	1.0×10^{10} cm^{-3}	3.11×10^{4} cm^{-2}
15 nm	$In_{0.15}Ga_{0.85}As$	1.0×10^{10} cm^{-3}	2.18×10^{12} cm^{-2}
2 nm	GaAs	1.0×10^{10} cm^{-3}	2.05×10^{10} cm^{-2}
5 nm	GaAs	3.0×10^{18} cm^{-3}	1.53×10^{11} cm^{-2}
100 nm	GaAs	1.0×10^{13} cm^{-3}	3.31×10^{11} cm^{-2}



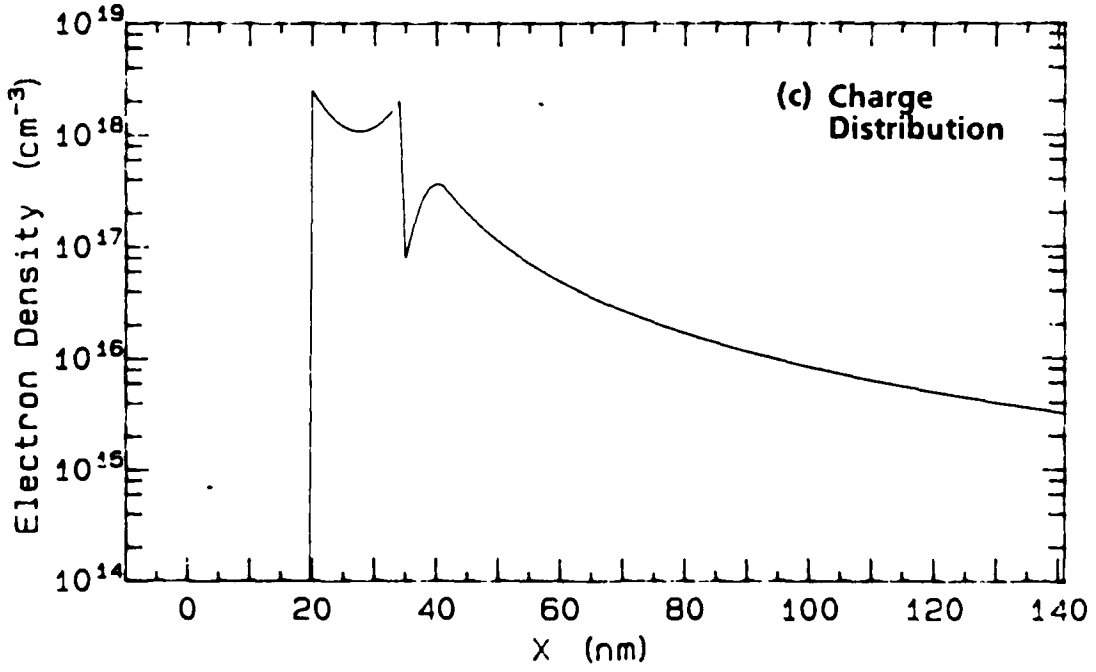
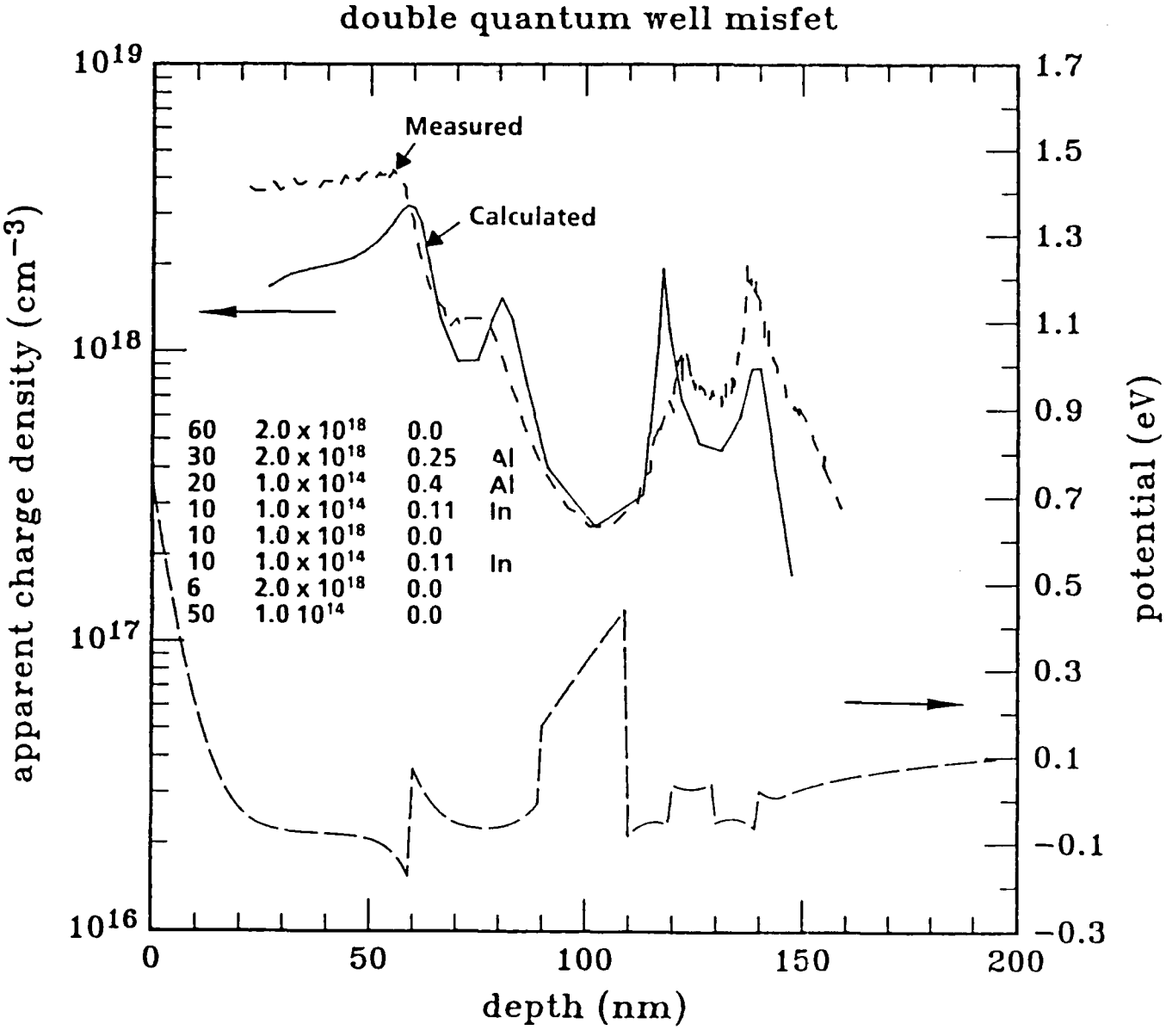
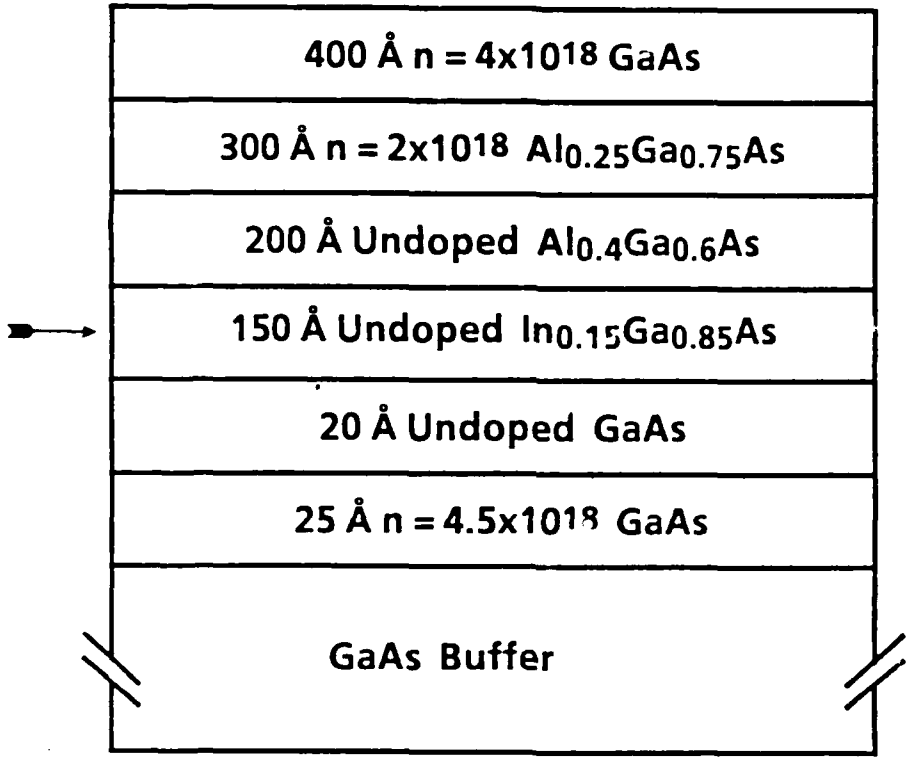


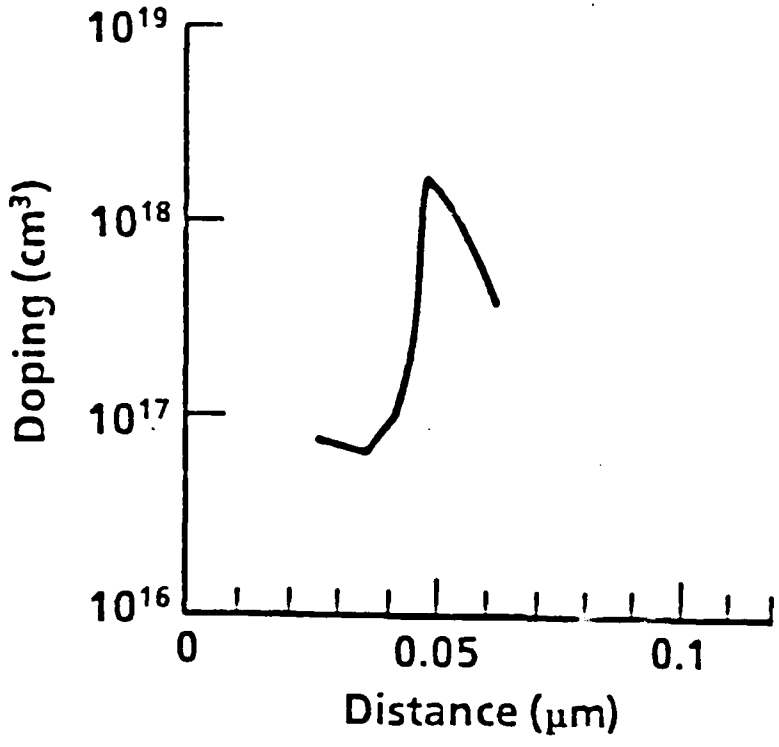
Figure 1. Quantum well MISFET with normal structure. (a) Material structure; (b) potential distribution; (c) charge distribution.


double quantum well misfet
Measured
Calculated
60 2.0 x 10^18 0.0
30 2.0 x 10^18 0.25 Al
20 1.0 x 10^14 0.4 Al
10 1.0 x 10^14 0.11 In
10 1.0 x 10^18 0.0
10 1.0 x 10^14 0.11 In
6 2.0 x 10^18 0.0
50 1.0 10^14 0.0
apparent charge density (cm^-3)
potential (eV)
depth (nm)
10^19
10^18
10^17
10^16
1.7
1.5
1.3
1.1
0.9
0.7
0.5
0.3
0.1
-0.1
-0.3
0
50
100
150
200

Quantum Well MiSFET with Undoped Channel

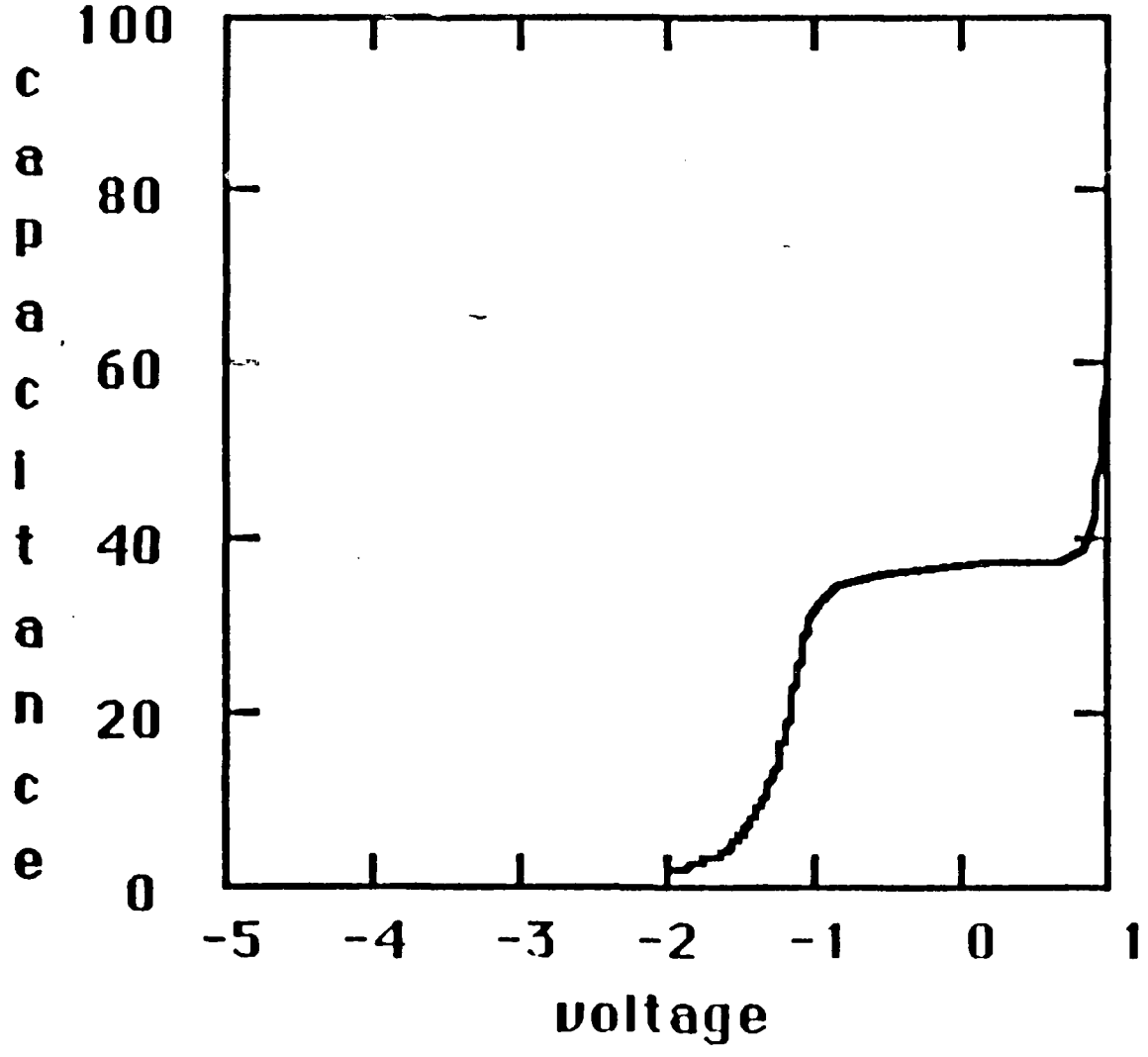


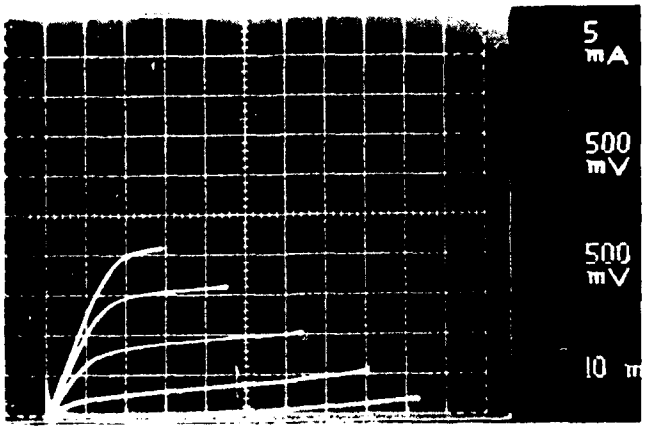
Material Structure



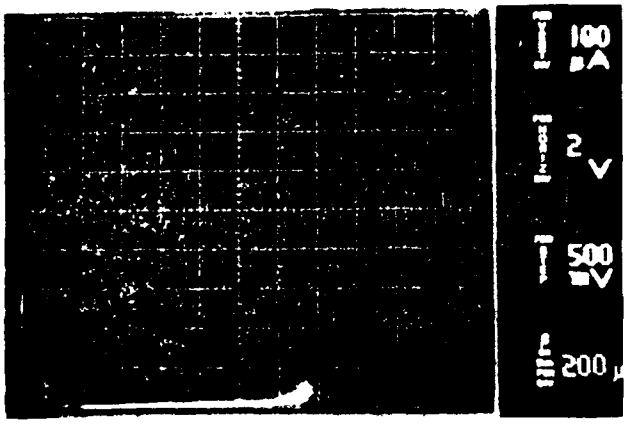
Charge Carrier Profile

GATE CAPACITANCE vs GATE VOLTAGE OF A QUANTUM WELL MISFET

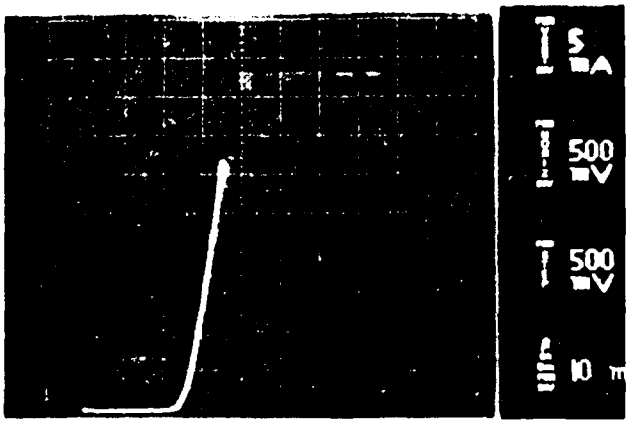




(a) I-V Curve



(b) Gate-Drain Breakdown Curve



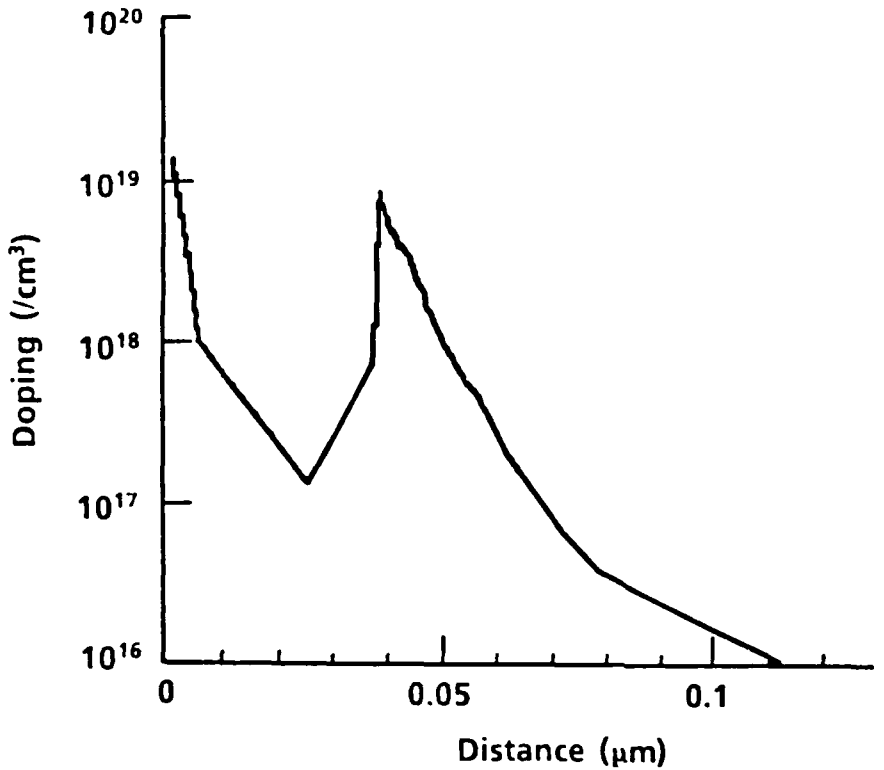
(c) Gate Forward Characteristic

Figure 22. Dc characteristics of quantum well MISFETS. (a) I-V curve; (b) gate-drain breakdown curve; (c) gate forward characteristic.

Quantum-Well MISFET with Doped Well

GaAs	400 Å	$n = 4 \times 10^{18}$
$Al_{0.2}Ga_{0.8}As$	300Å	$n = 2 \times 10^{18}$
$Al_{0.34}Ga_{0.66}As$	200 Å	Undoped
→ $In_{0.15}Ga_{.0.85}As$	120 Å	$n = 3 \times 10^{18}$
GaAs	80 Å	$n = 2 \times 10^{18}$

Material Structure

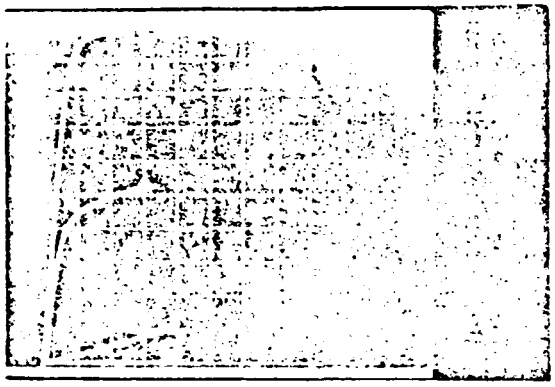


Charge Density Profile

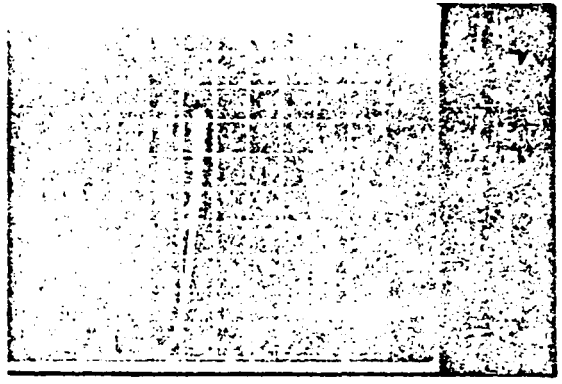
CENTRAL RESEARCH LABORATORIES

TEXAS INSTRUMENTS

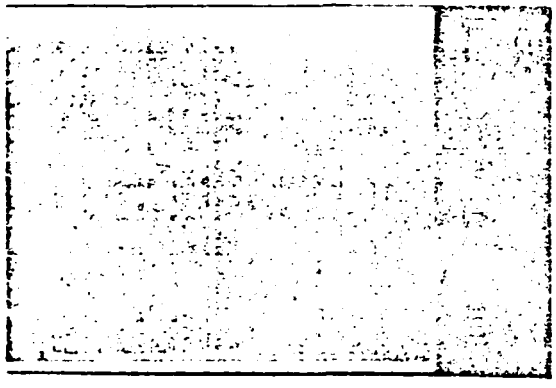
CHARACTERISTICS OF QUANTUM WELL MISFET WITH DOPED CHANNEL (0.25μm × 50μm)



I-V CURVE



SCHOTTKY PROPERTIES



GATE-DRAIN BREAKDOWN

DC

- TRANSCONDUCTANCE
  500 mS/mm
- I_{max} 1000 mA/mm
- SCHOTTKY BARRIER 1.4 V

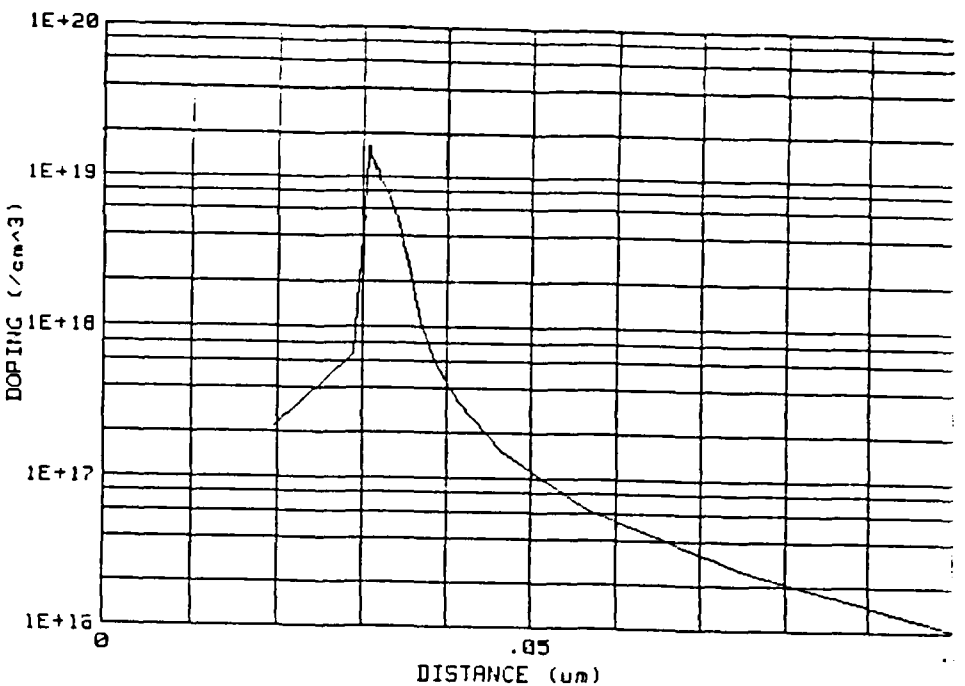
RF

60 GHz
0.95 W/mm, 24% EFFICIENCY
3dB GAIN

Quantum well MISFET

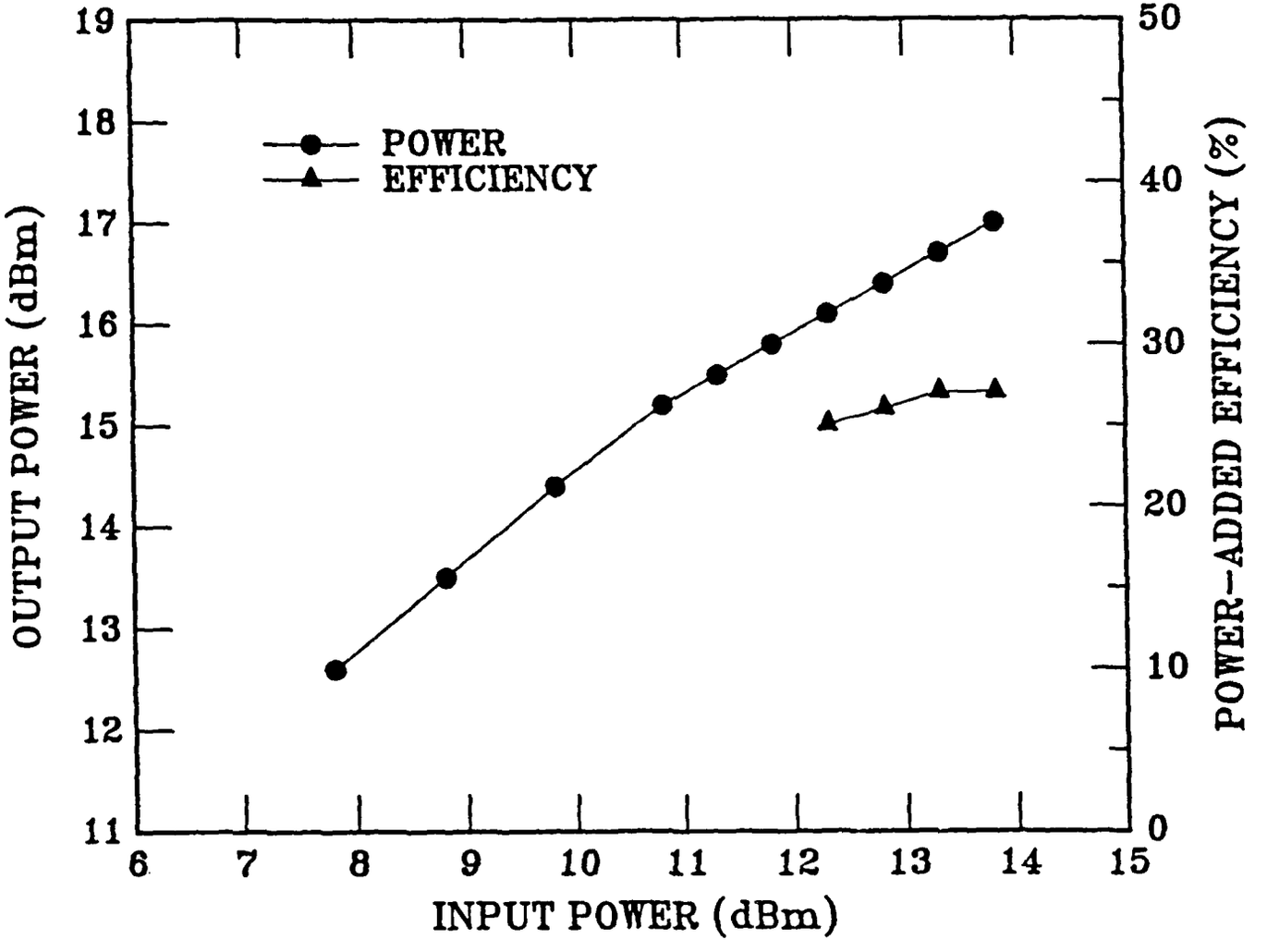
GaAs	4 x 10^{18}/cm^3	400 Å
$Al_{0.25}Ga_{0.75}As$	2 x 10^{18}/cm^3	400 Å
$Al_{0.4}Ga_{0.6}As$	Undoped	200 Å
$In_{0.18}Ga_{0.82}As$	6 x 10^{18}/cm^3	100 Å
GaAs Buffer		

Material Structure

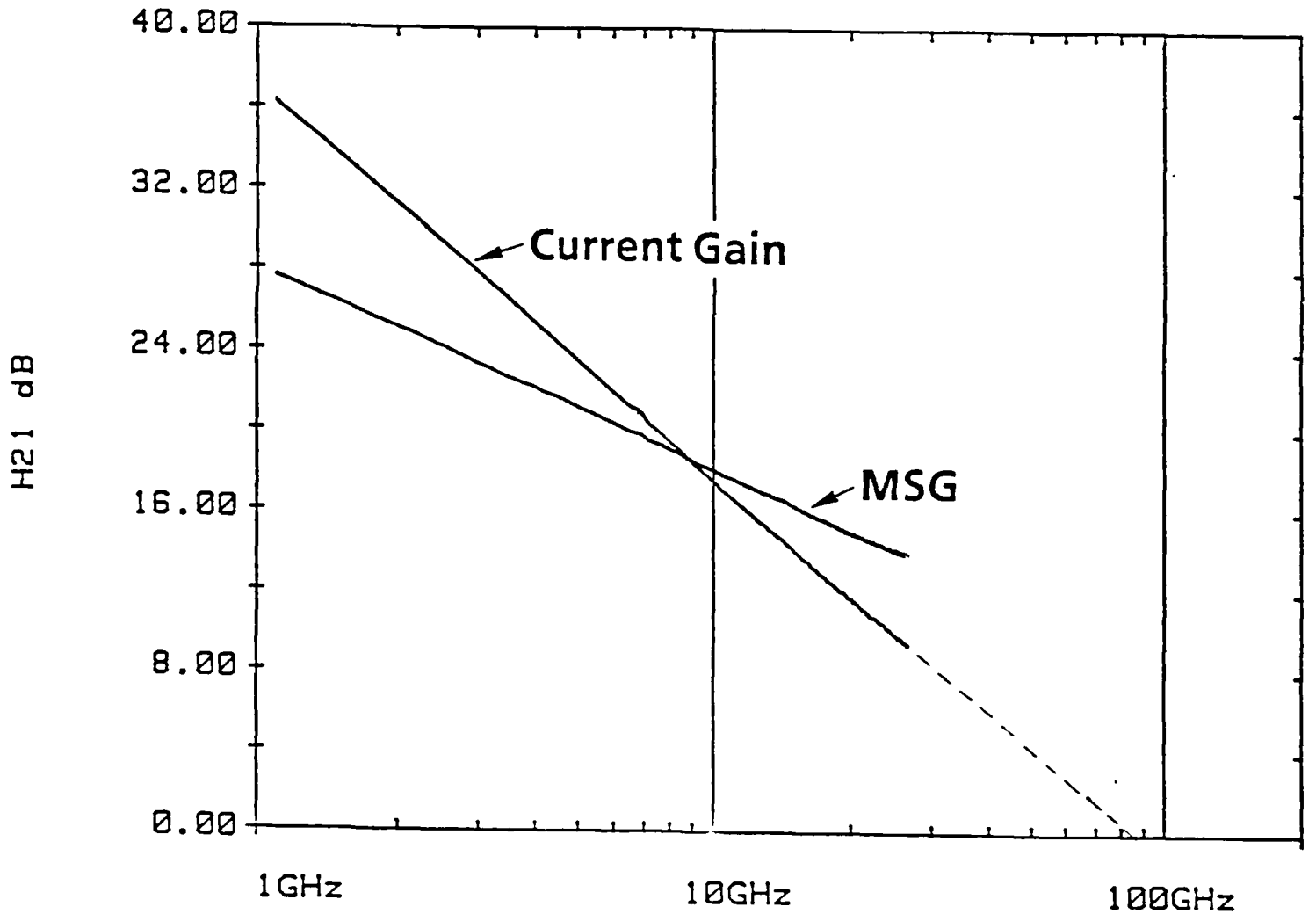


Charge Carrier Profile

PERFORMANCE OF 50 μm x 0.25 μm MISFET AT 60 GHz



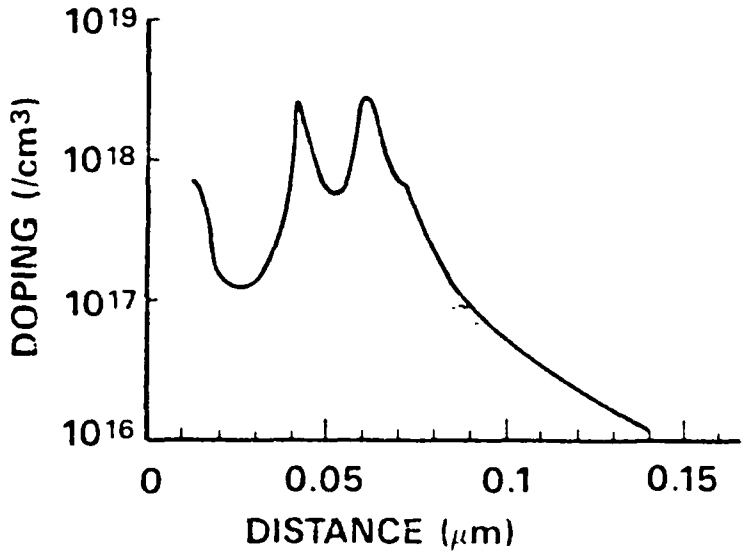
Current Gain and Maximum Stable Gain of QW MISFET



DOUBLE QUANTUM WELL MISFET

n = 4 × 10^{18}	GaAs	500 Å
n = 2 × 10^{18}	$Al_{0.25}Ga_{0.75}As$	300 Å
UNDOPED	$Al_{0.4}Ga_{0.6}As$	200 Å
n = 1 × 10^{18}	$In_{0.15}Ga_{0.85}As$	120 Å
n = 1.5 × 10^{18}	GaAs	100 Å
n = 1 × 10^{18}	$In_{0.15}Ga_{0.85}As$	120 Å
n = 2 X 10^{18}	GaAs	80 Å
GaAs BUFFER (1μm)		

MATERIAL STRUCTURE

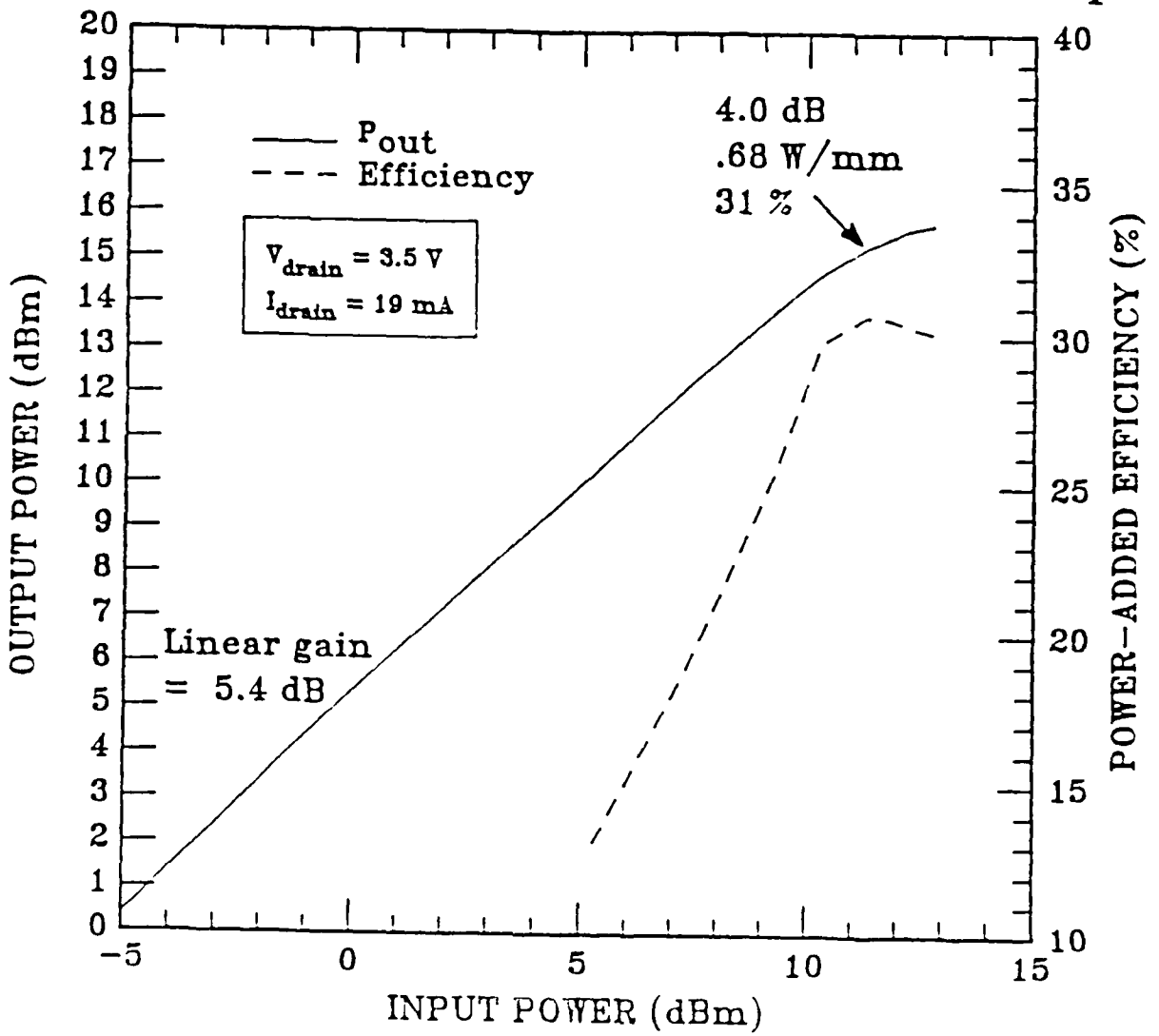


CHARGE DENSITY PROFILE

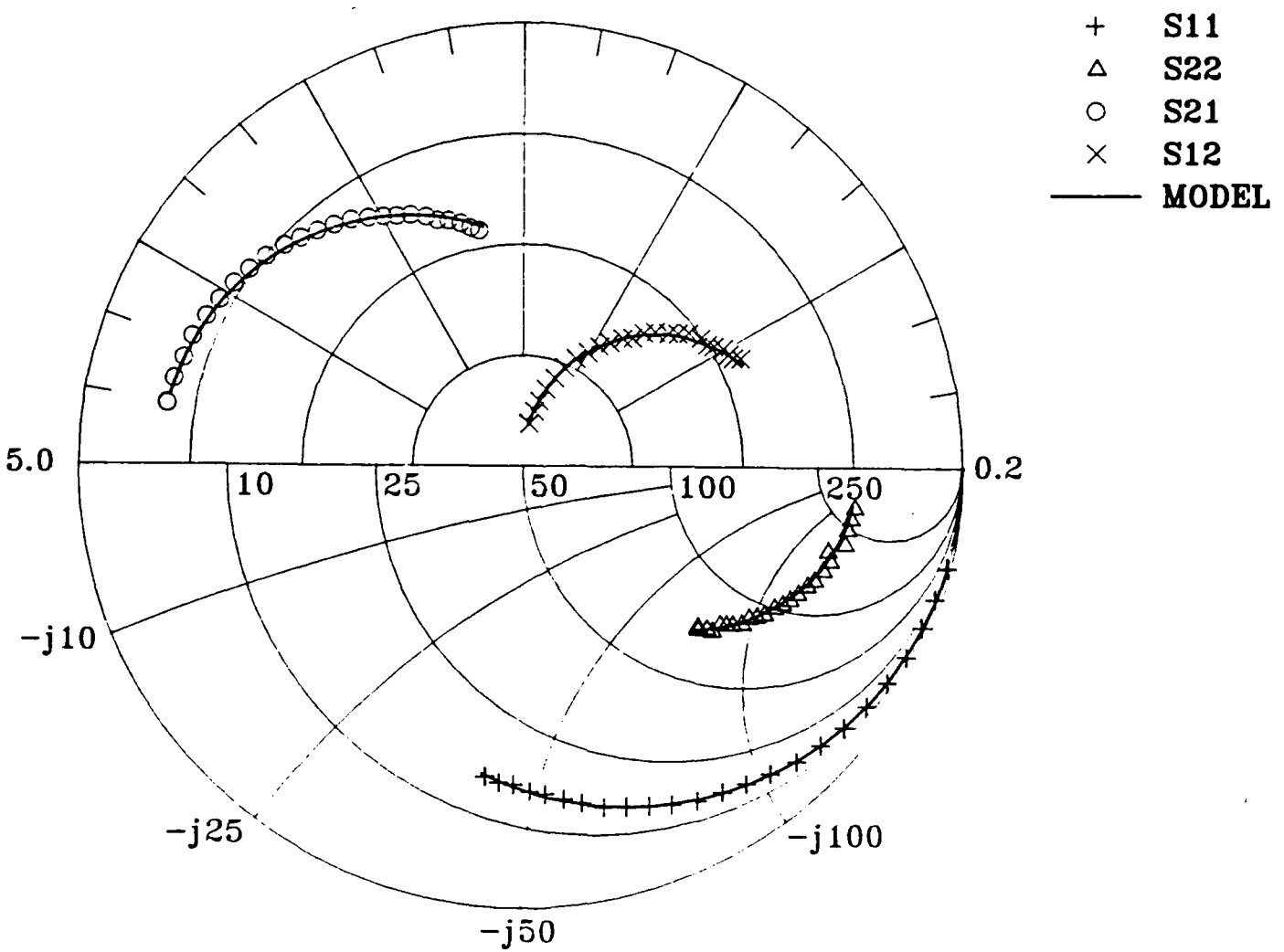
Performance of a 0.25 x 50 μm Double Quantum Well MISFET

FREQUENCY (GHZ)	POWER DENSITY (W/mm)	GAIN (DB)	EFFICIENCY (%)
55	0.68	4.0	31
55	0.89	3.7	26
55	0.96	3.0	24
60	0.6	3.4	20

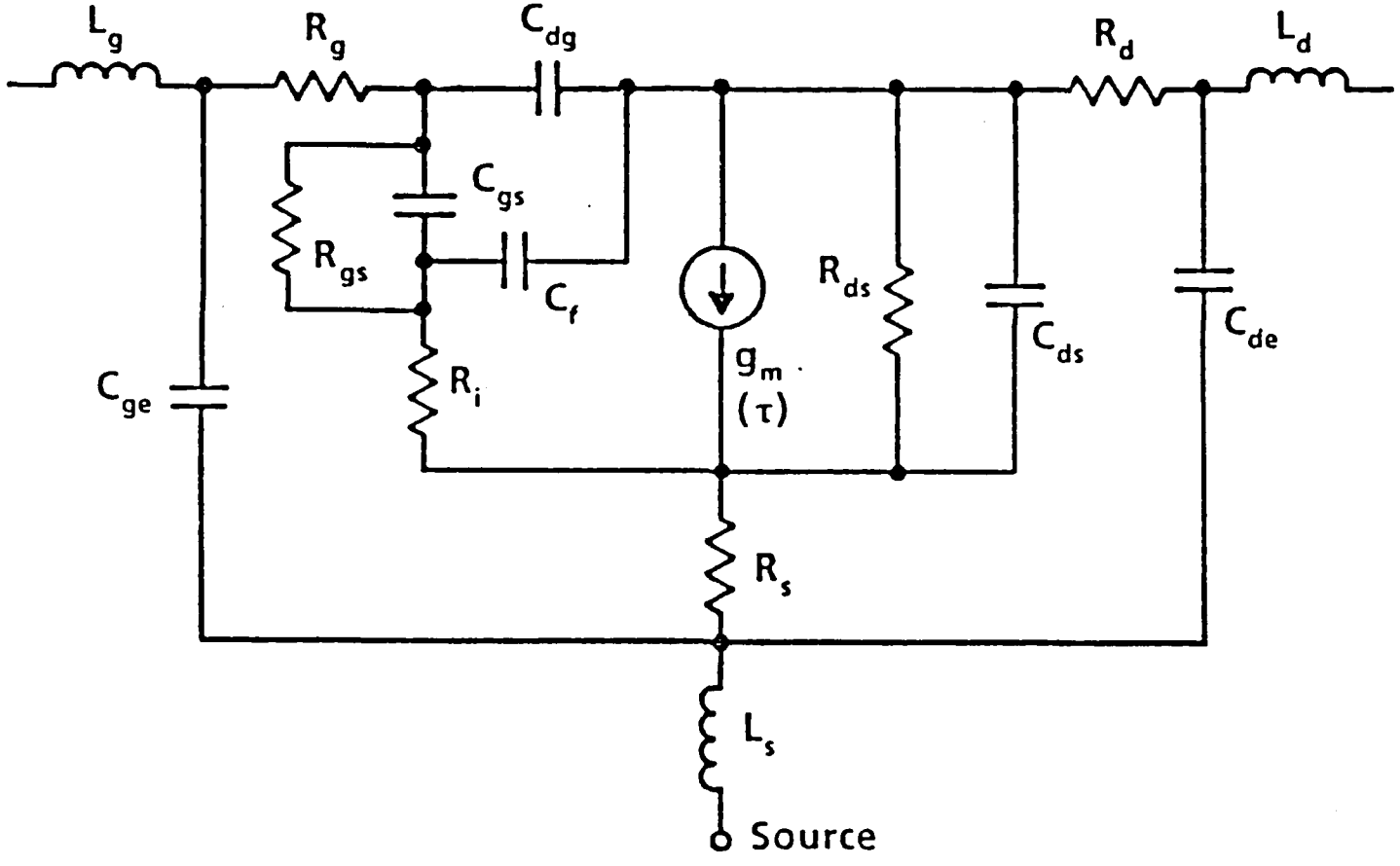
Performance of a Double Quantum Well MISFET at 55 GHz (0.25 x 50μm)



QW MISFET

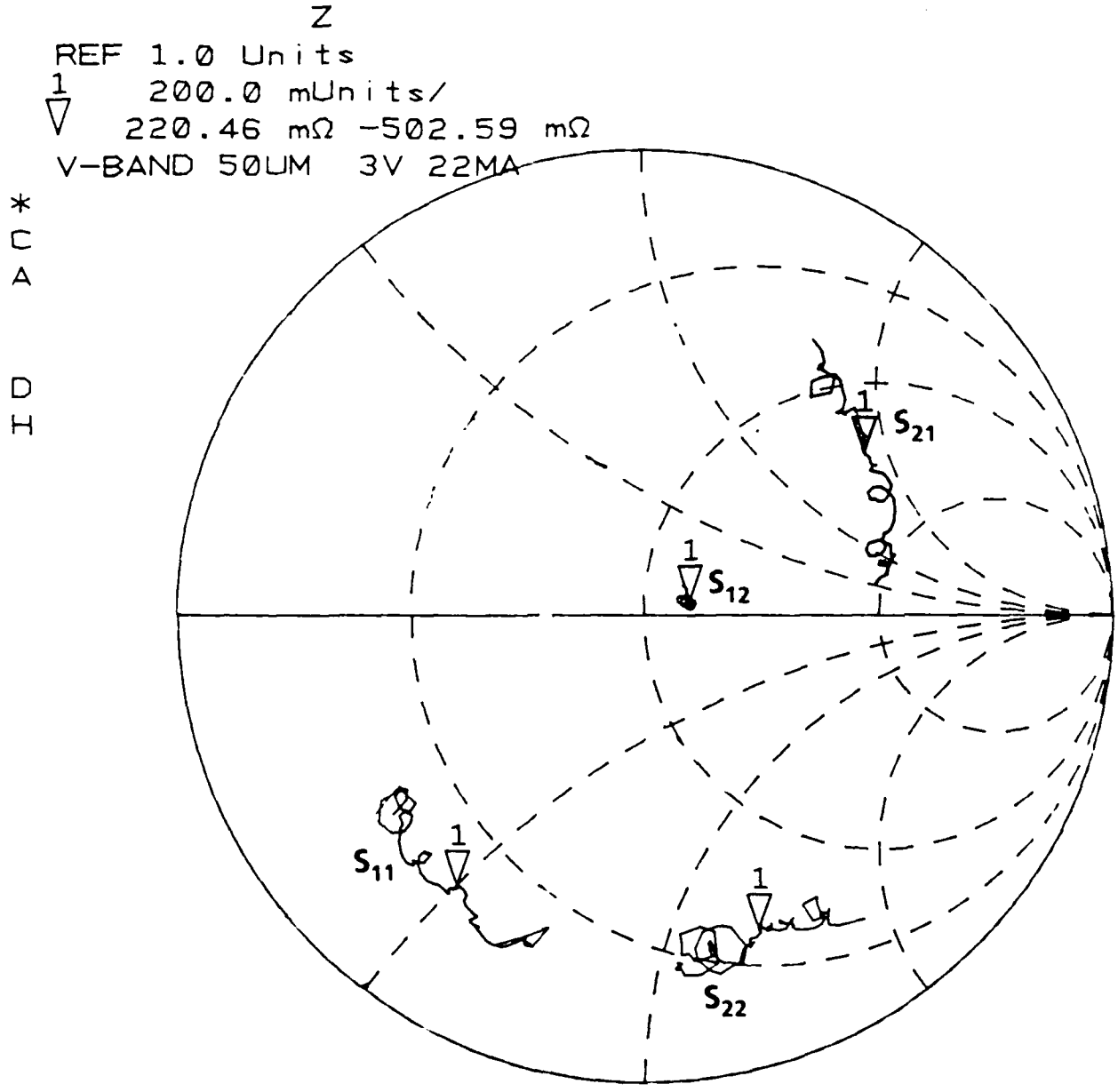


EQUIVALENT CIRCUIT MODEL OF FET

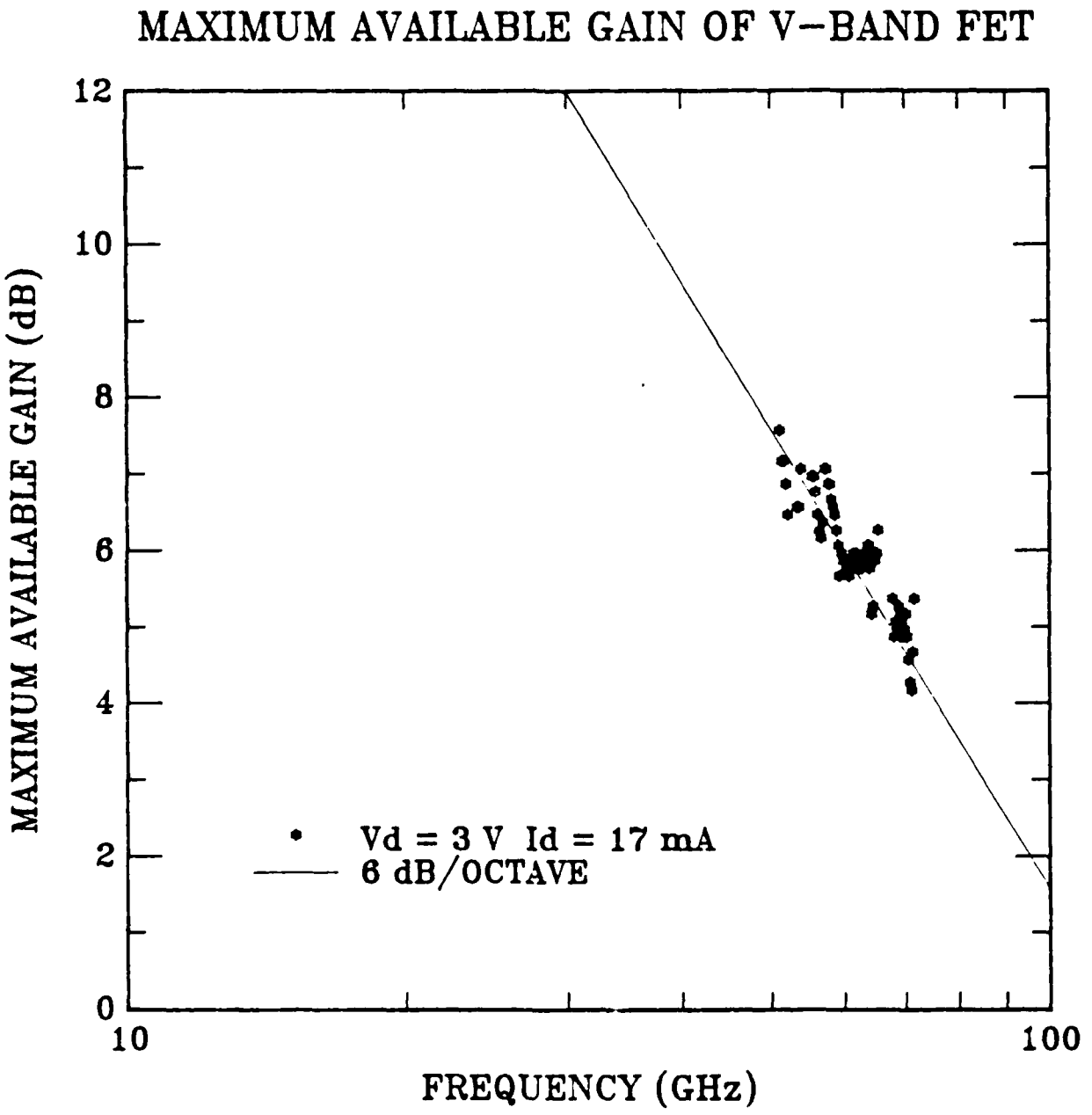


Equivalent Circuit Parameters of 0.25 x 50 μm Quantum Well MISFETs

Parameter	Undoped-Well	Doped-Well	Double-Wells
C_{gs} (pF)	0.074	0.04	0.05
g_m (mS)	20.5	37.5	26.6
C_{dg} (pF)	0.008	0.008	0.008
R_{ds} (Ω)	980	504	622
f_t (GHz)	40	120	72



S-Parameters at V-band (50-75 GHz)


MAXIMUM AVAILABLE GAIN OF V-BAND FET
MAXIMUM AVAILABLE GAIN (dB)
12
10
8
6
4
2
0
10
100
FREQUENCY (GHz)
Vd = 3 V Id = 17 mA
6 dB/OCTAVE

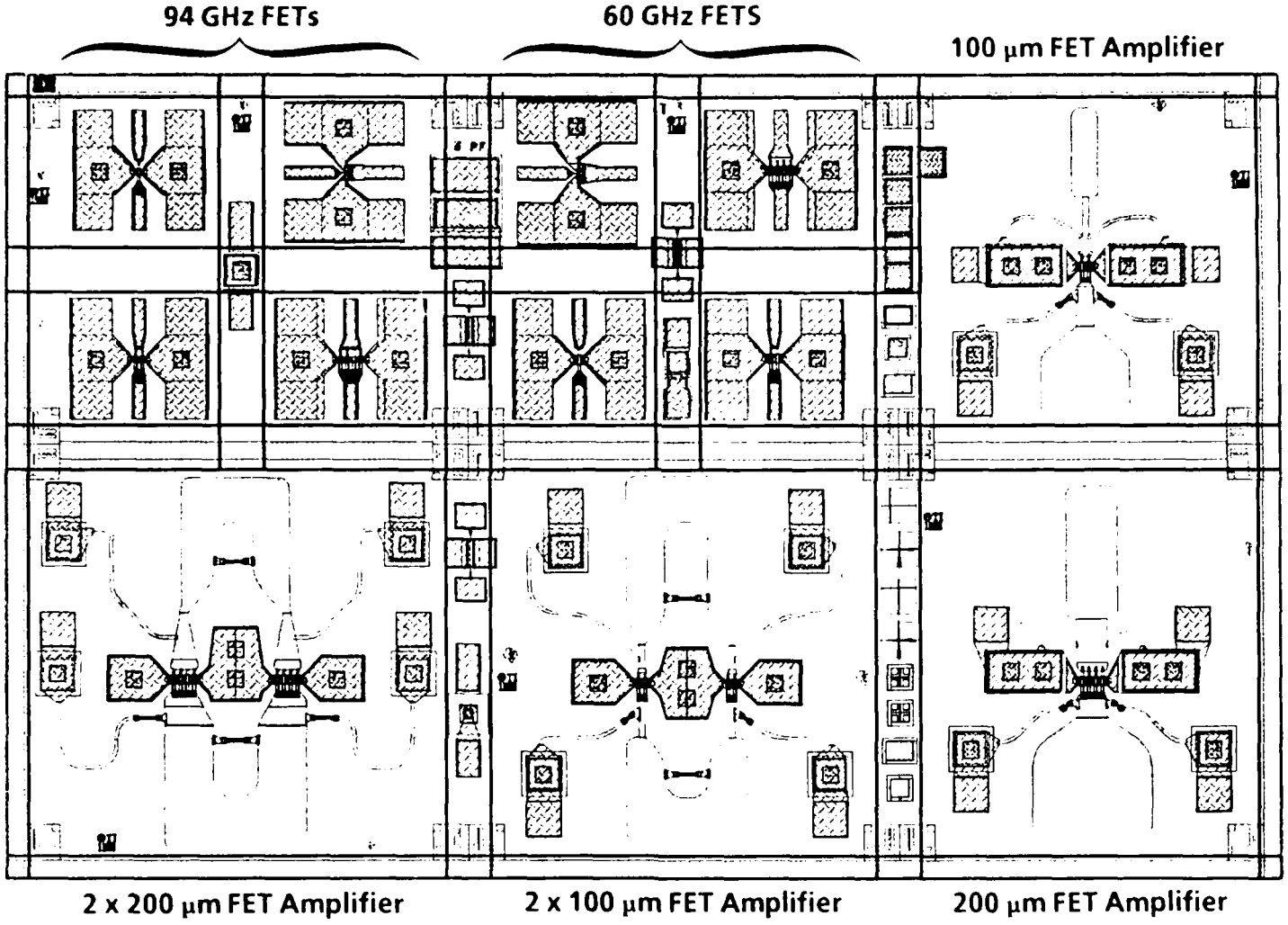
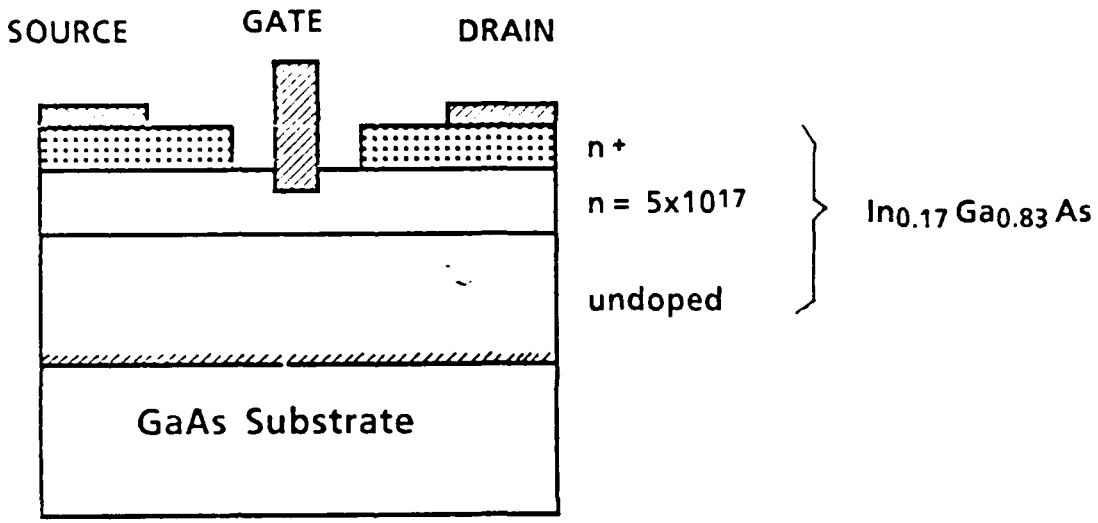


Figure 32. Mask layout.

InGaAs MESFET



- Good Transport Properties of InGaAs
- Heteroepitaxy Growth
- mm-Wave MISFET

Device Performance

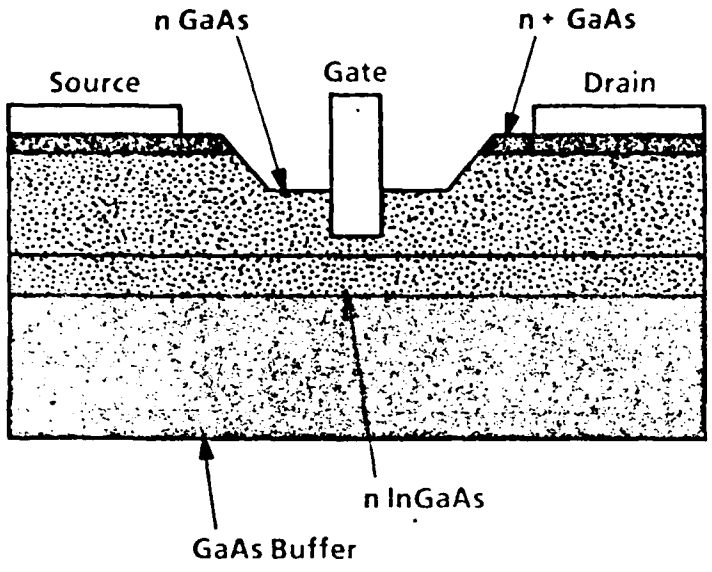
At 60 GHz

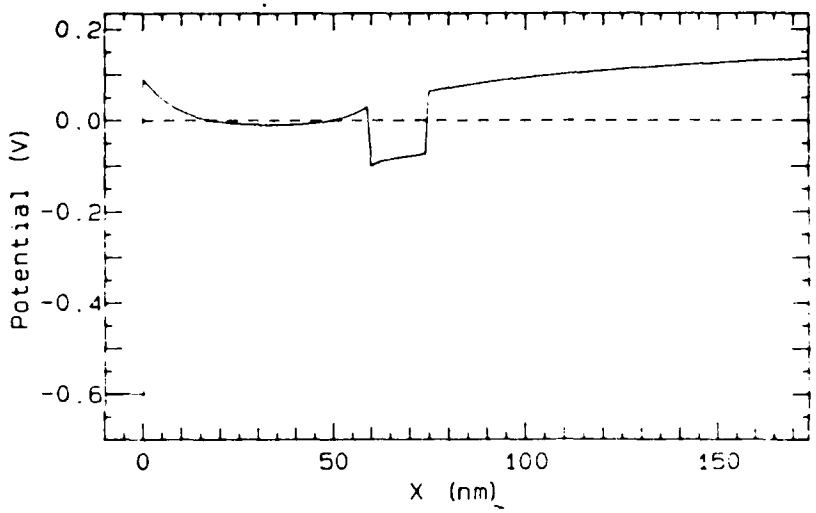
Power Density = 0.5 w/mm with 4dB gain and 20% Efficiency

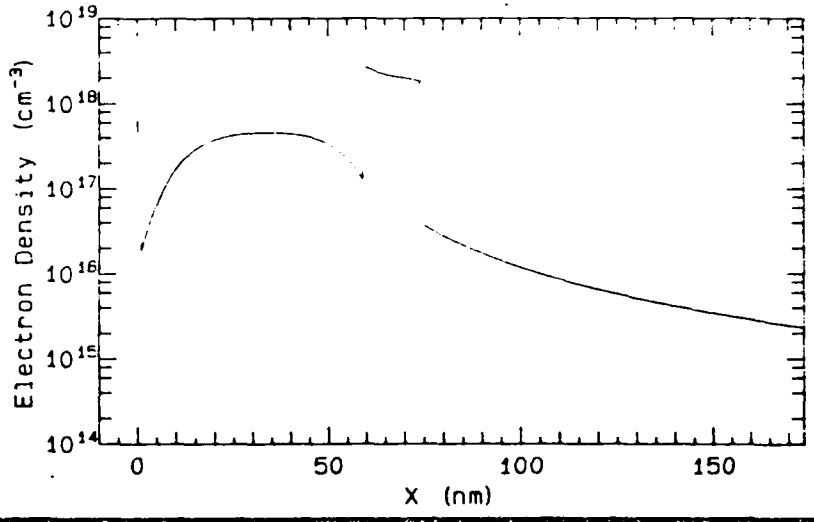
f_t = 65 GHz for 0.25 μm gate

TEXAS INSTRUMENTS

InGaAs PULSE-DOPED MESFET



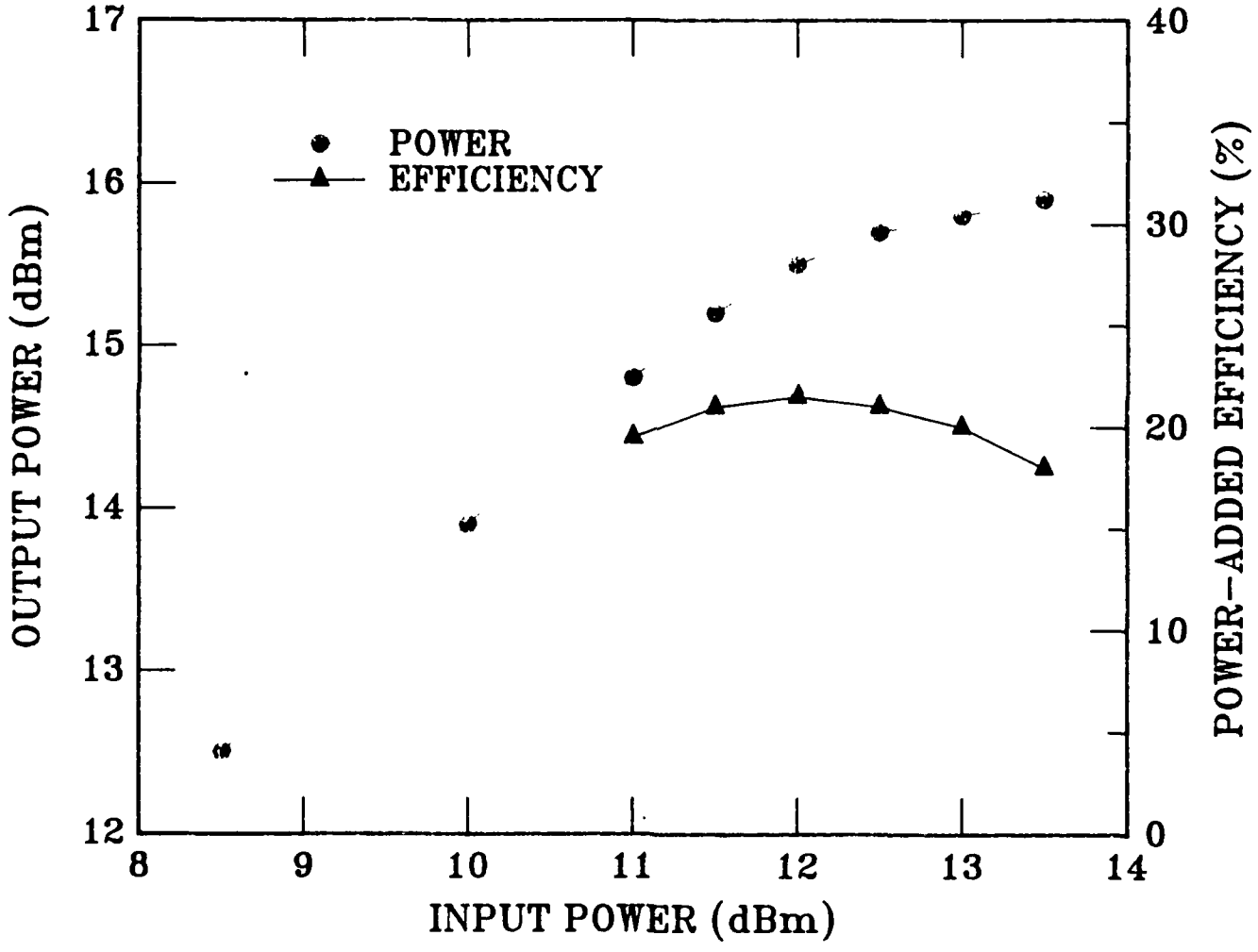




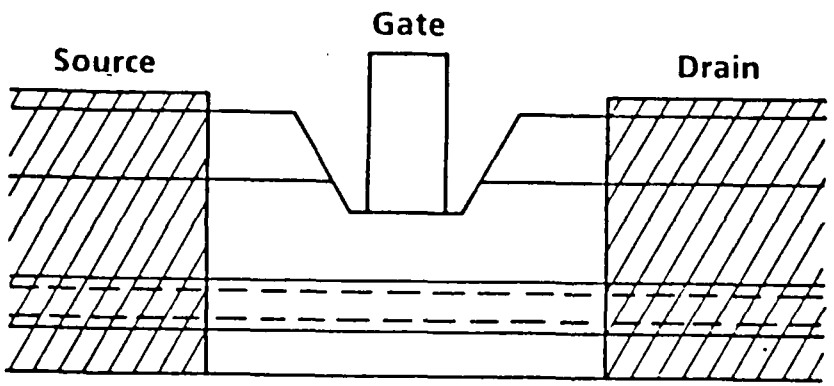
Advantages

- Better Transport Properties
- High Carrier Density
- Tight Electron Confinement
- Easy of Manufacturing

PERFORMANCE OF 0.25μm InGaAs PULSE–DOPED FET AT 60 GHz



MATERIAL STRUCTURE OF DOUBLE CHANNEL PSEUDOMORPHIC HEMTs



Cap Layer

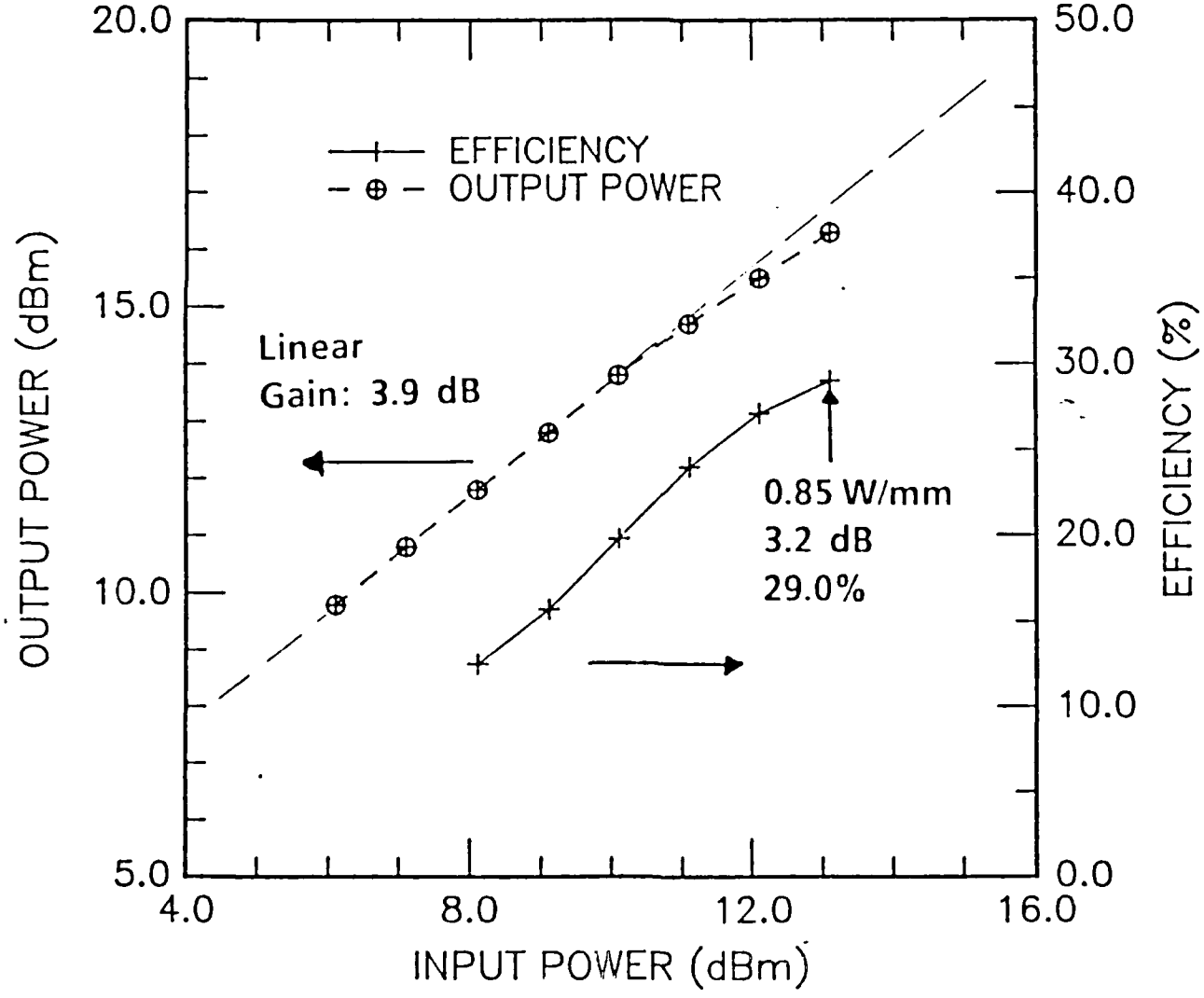
AlGaAs, 500 Å, 2×10^{18}

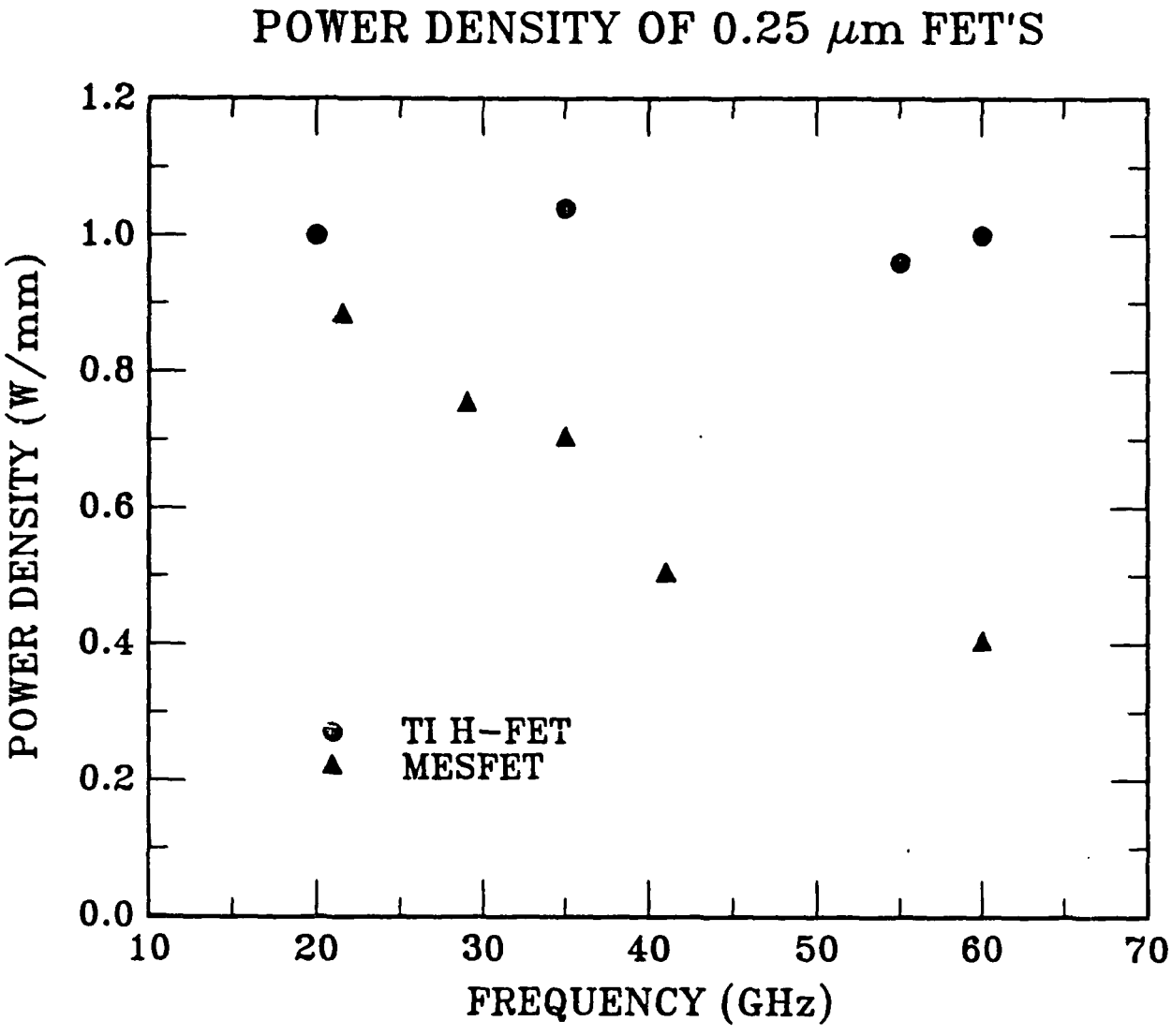
InGaAs, 100 Å, 2×10^{18}

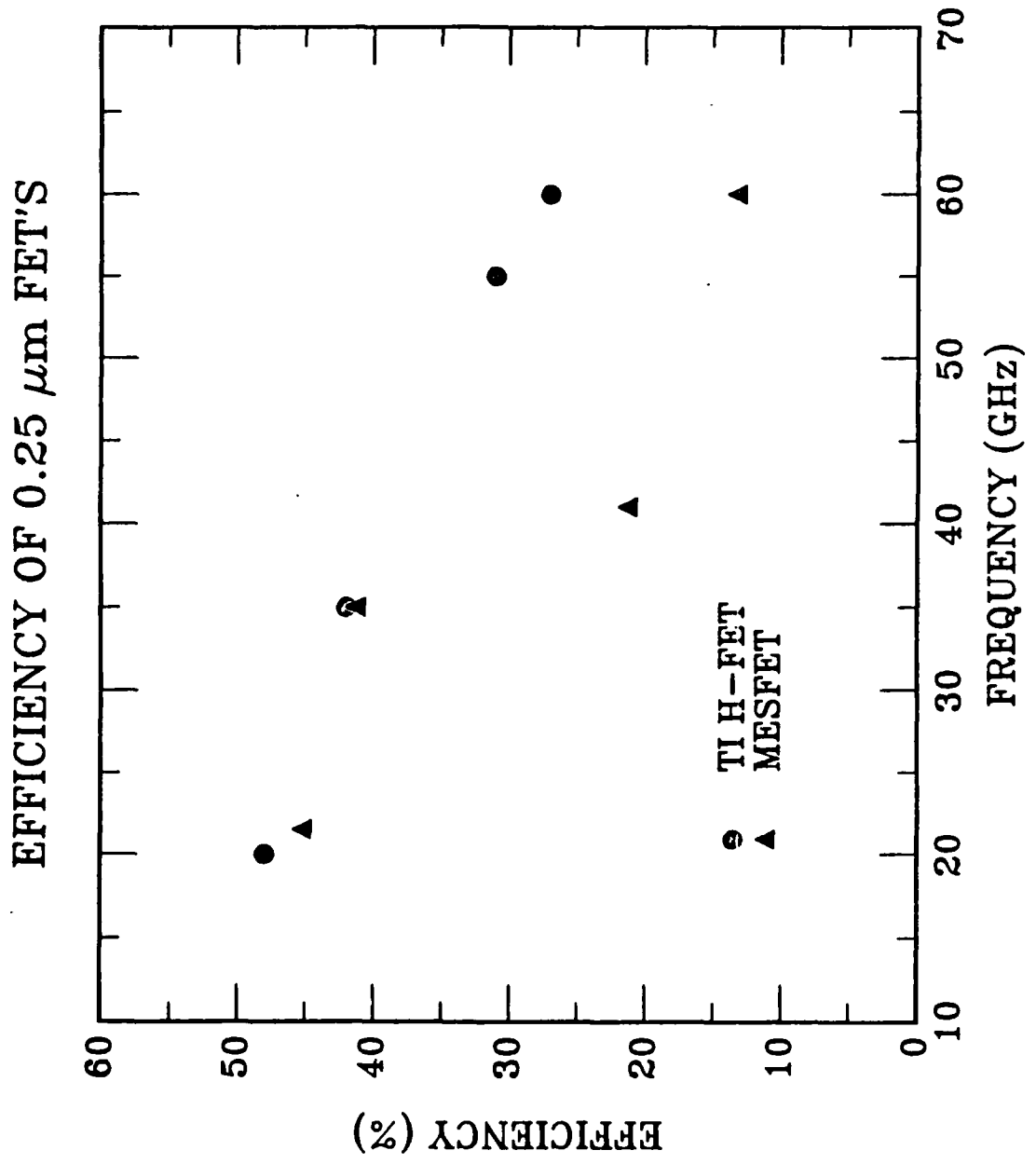
GaAs, 80 Å, 2×10^{18}

GaAs Buffer, 1 μm

POWER PERFORMANCE OF DOUBLE CHANNEL PSEUDOMORPHIC HEMTs




POWER DENSITY OF 0.25 μm FET'S
POWER DENSITY (W/mm)
1.2
1.0
0.8
0.6
0.4
0.2
0.0
10
20
30
40
50
60
70
FREQUENCY (GHz)
TI H-FET
MESFET


EFFICIENCY OF 0.25 μm FET'S
EFFICIENCY (%)
FREQUENCY (GHz)
TI H-FET
MESFET
0
10
20
30
40
50
60
10
20
30
40
50
60
70

SUMMARY

- Developed quantum well power MISFET at mm-wave frequencies
- Improved device performance by doping the well
- Achieved 1 W/mm with 3.2 dB gain and 27% efficiency at 60 GHz
- Designed monolithic power amplifiers

Molecular Beam Epitaxy and Resonant Tunneling Devices

J. S. Harris

Stanford University
Stanford, CA

MOLECULAR BEAM EPITAXY AND RESONANT TUNNELING DEVICES

J. S. Harris
Solid State Electronics Laboratory
Stanford University
(415)723-9775

DARPA EHF Monolithic Materials
Devices and Arrays Review
January 24-25, 1989
San Diego, CA

OUTLINE

- Oval Defects in MBE
- Resonant Tunneling Studies
  - Modeling
  - Double Barrier Structures
  - Lateral Barrier Structures

MOTIVATION

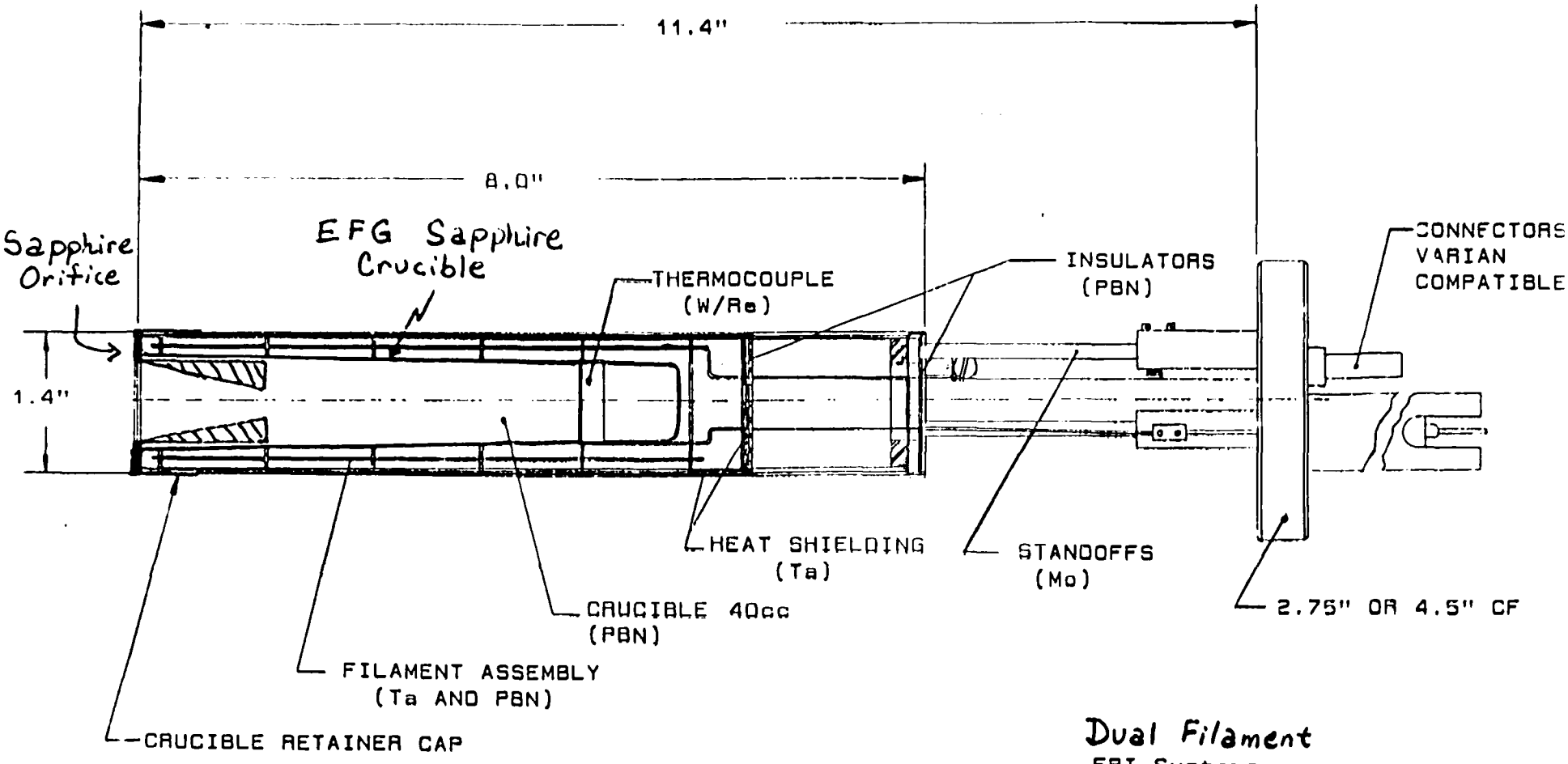
(CBE & GSMBE too)

* MOMBE has no gallium-related oval defects

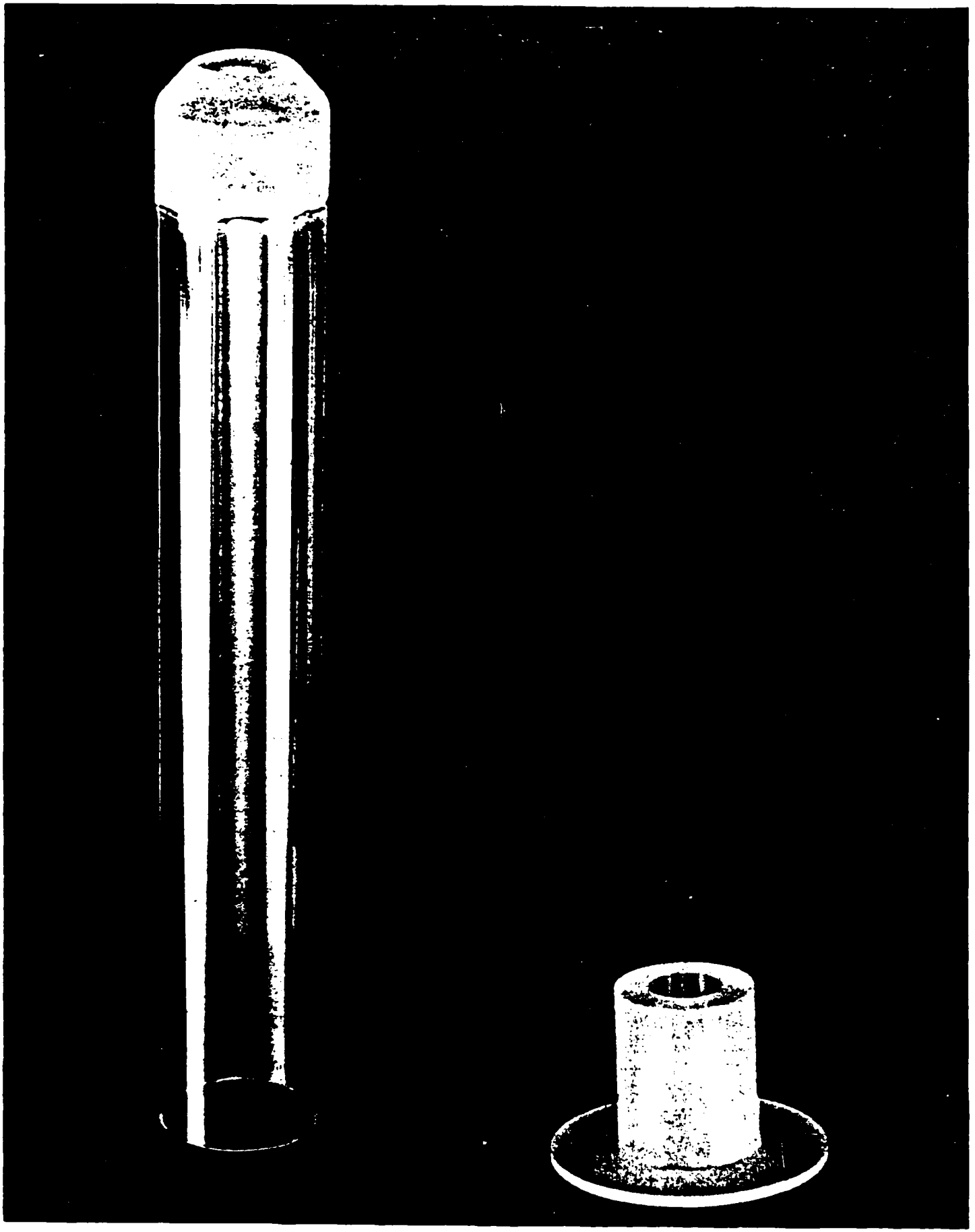
* Overheating gallium cell increases gallium-related oval defects

* Aluminum addition (add ~.1% after system bakeout) helps (Woodall), but we still see gallium-related oval defects.

* Gallium "spitting" / Ga_2O_3 oval defect cause not resolved (maybe both at work)



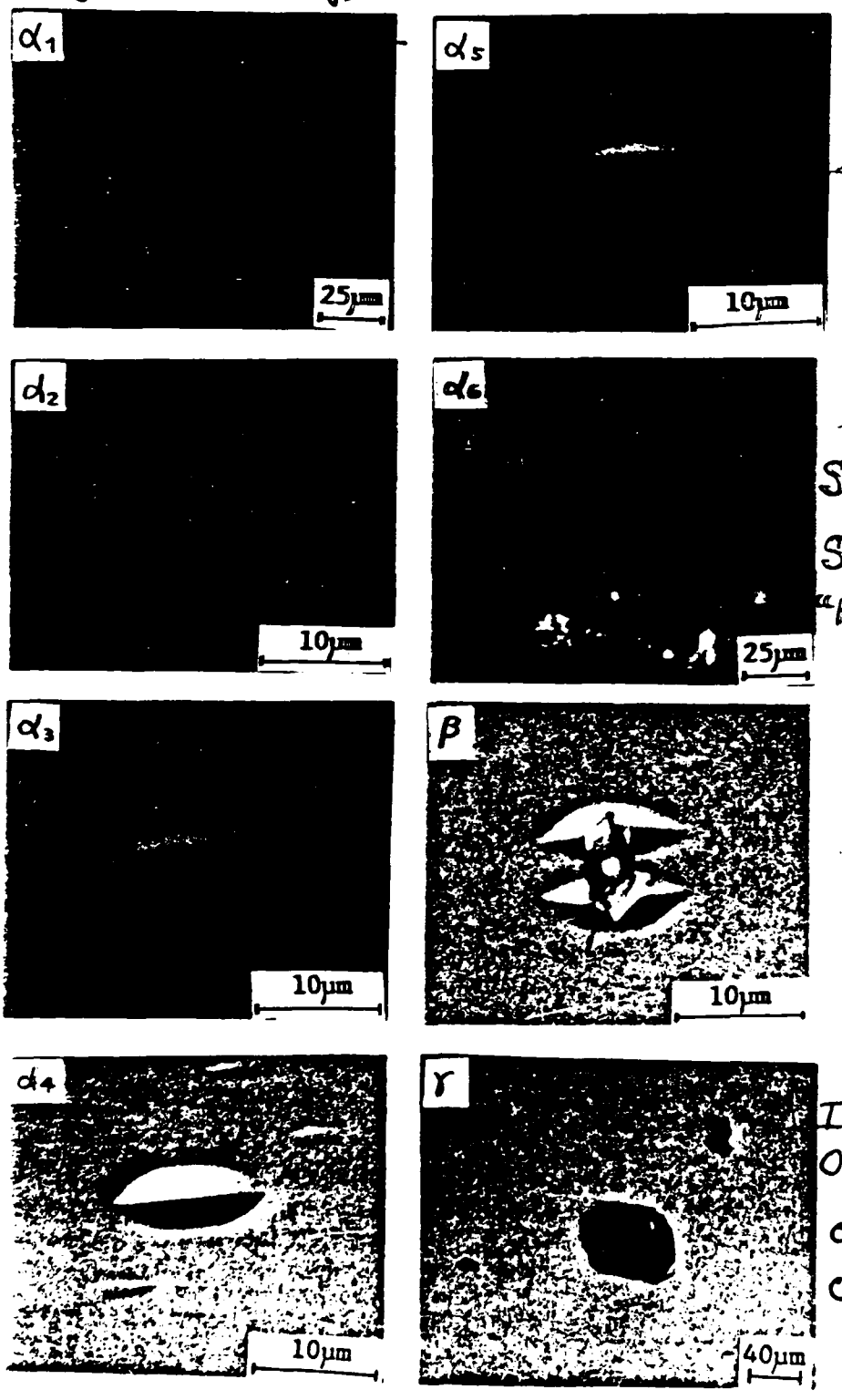
Dual Filament
EPI Systems
Model VA-40
Effusion Cell
June 1987



THE MANY "OVAL DEFECTS"

From: K. Fujiwara, K. Kanamoto, Y. N. Ohta, Y. Tokuda, & T. Nakayama (Mitsubishi)

Cause: As_2O_3 Octahedra? (Ploog) Carbon? (Mitsubishi)



Sulfur on Substrate "Pair Defect" (Varian)

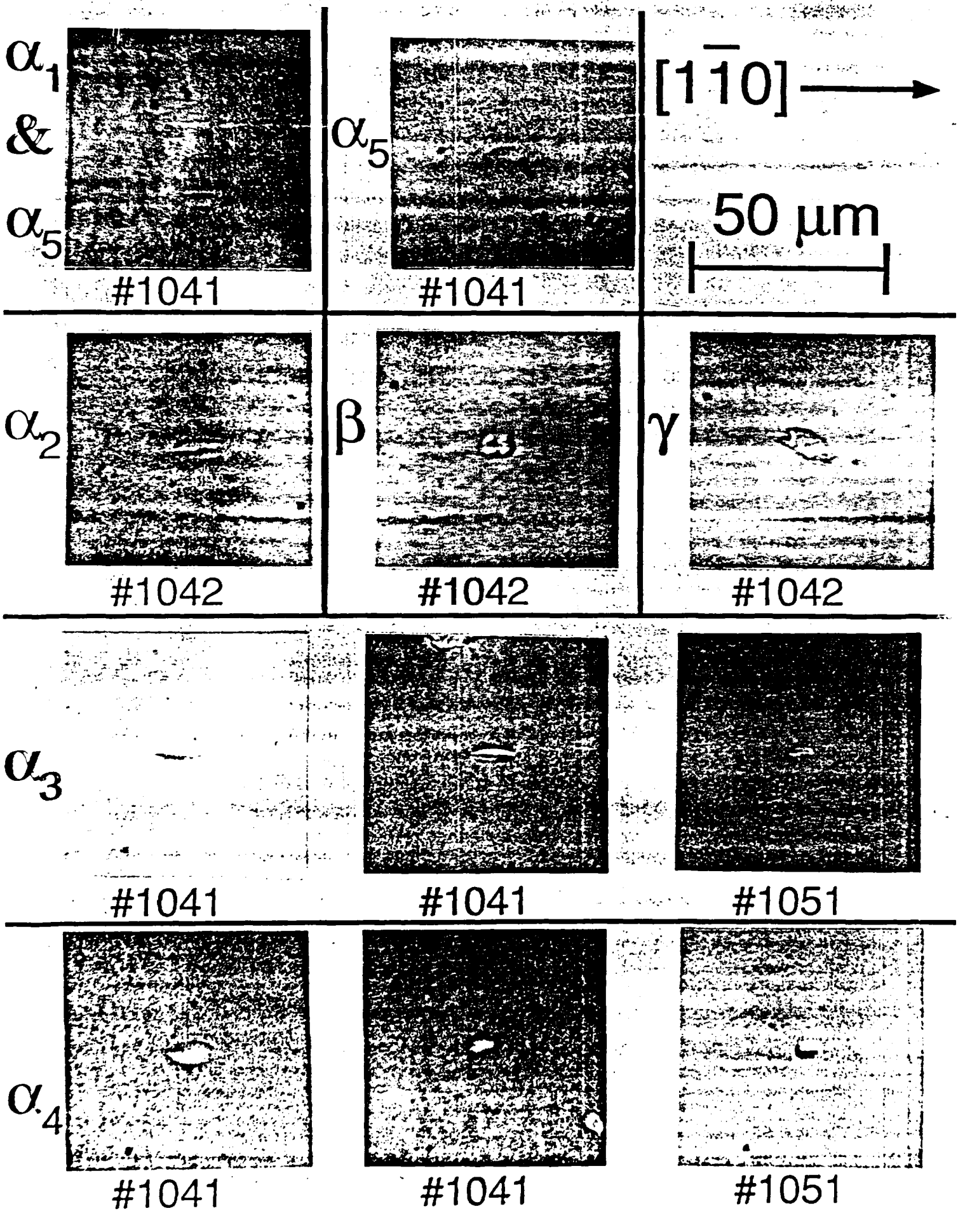
Flat Facet Along Center

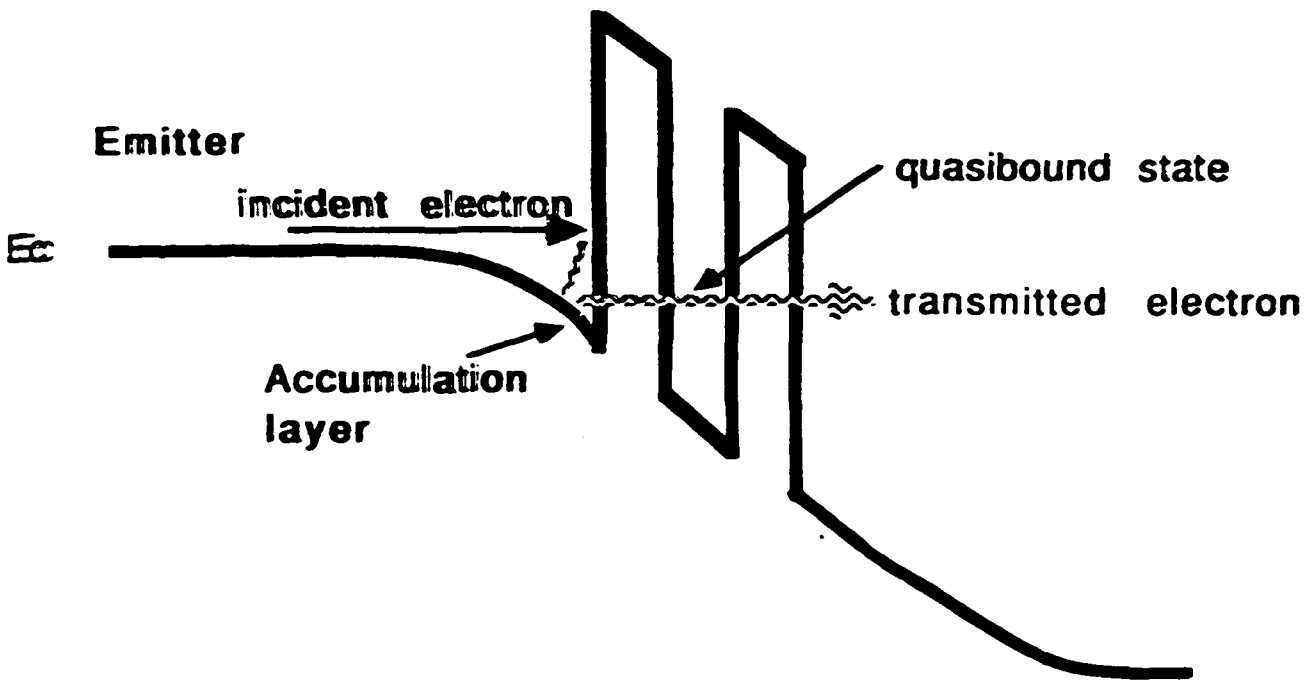
Gallium Source Related

Ga Rich? (Fujitsu)

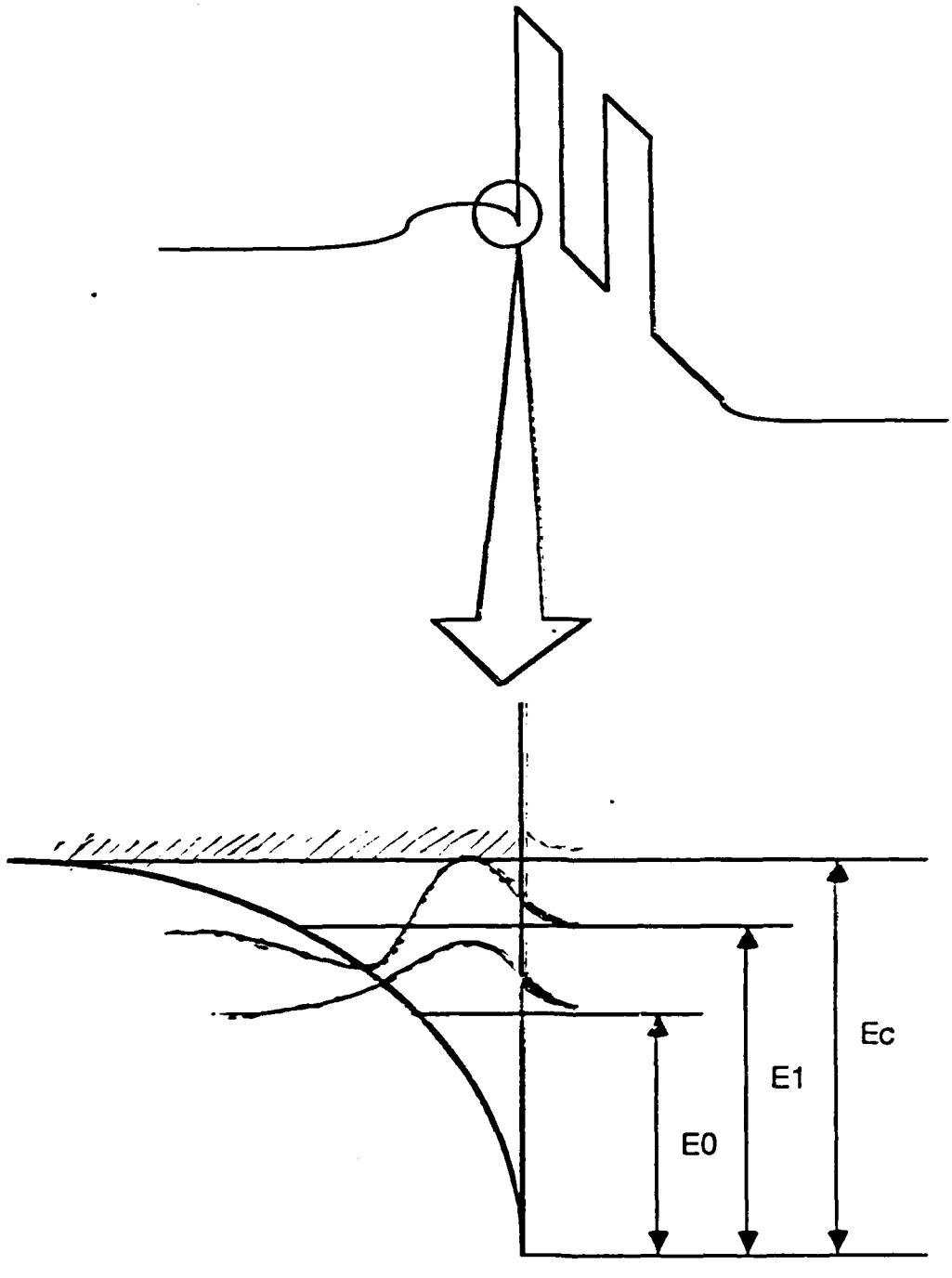
Insufficient Outgassing of Furnace or Shutters

Fig. 1. Nomarski phase-contrast micrographs of seven types of GaAs oval defects and an irregular surface defect.

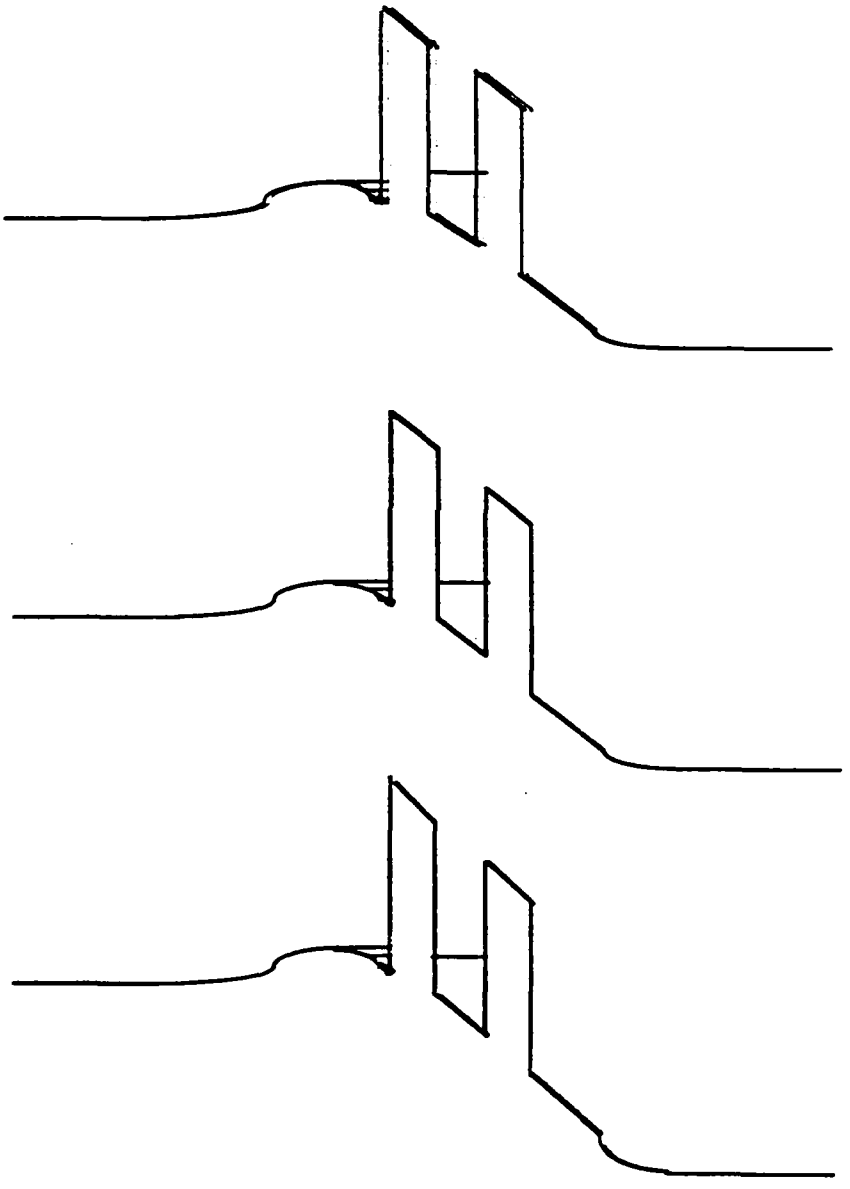

α1
&
α5
#1041
α5
#1041
[1$\bar{1}$0]
50 μm
α2
#1042
β
#1042
γ
#1042
α3
#1041
#1041
#1051
α4
#1041
#1041
#1051

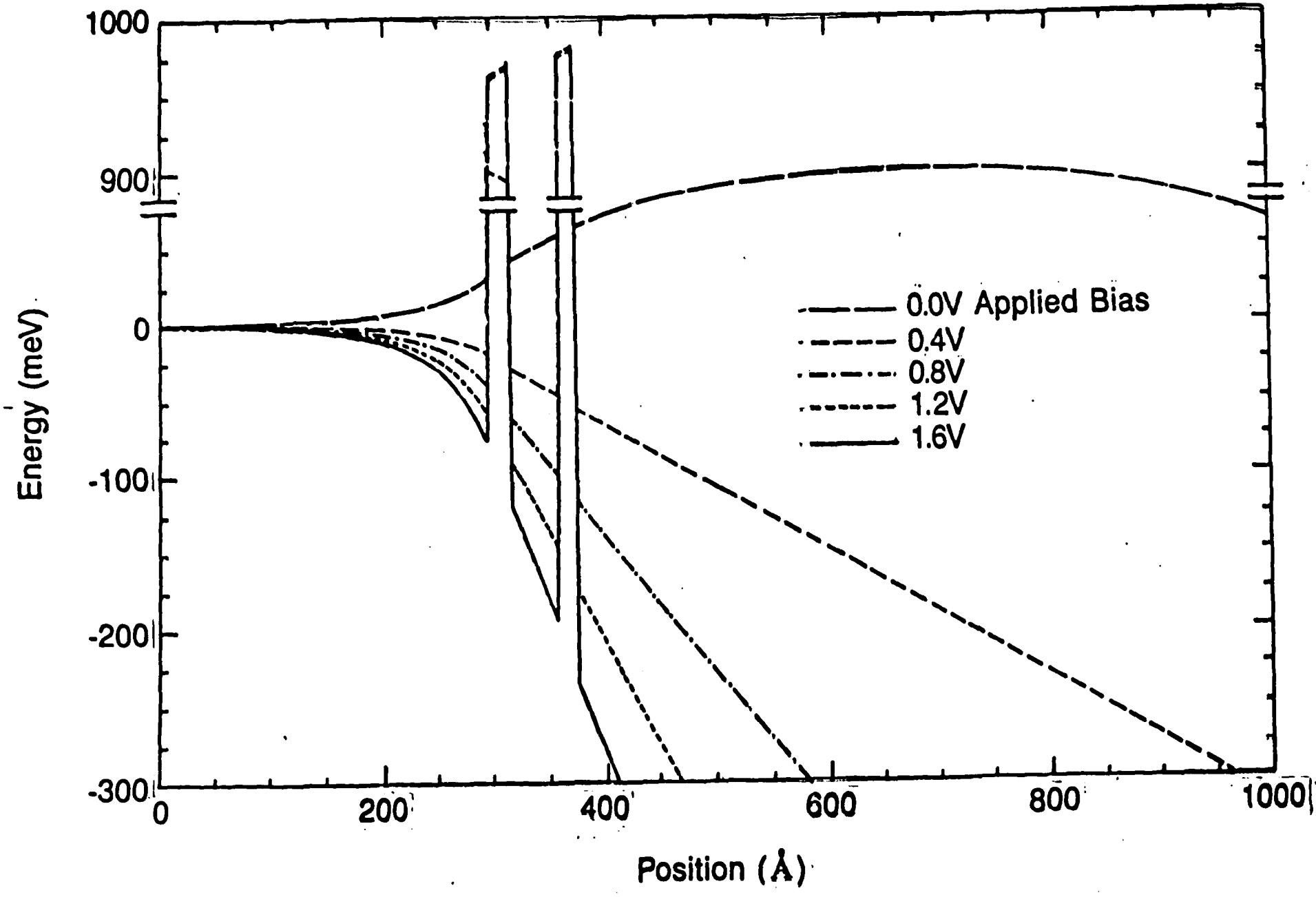

Emitter
incident electron
Ec
quasibound state
transmitted electron
Accumulation
layer

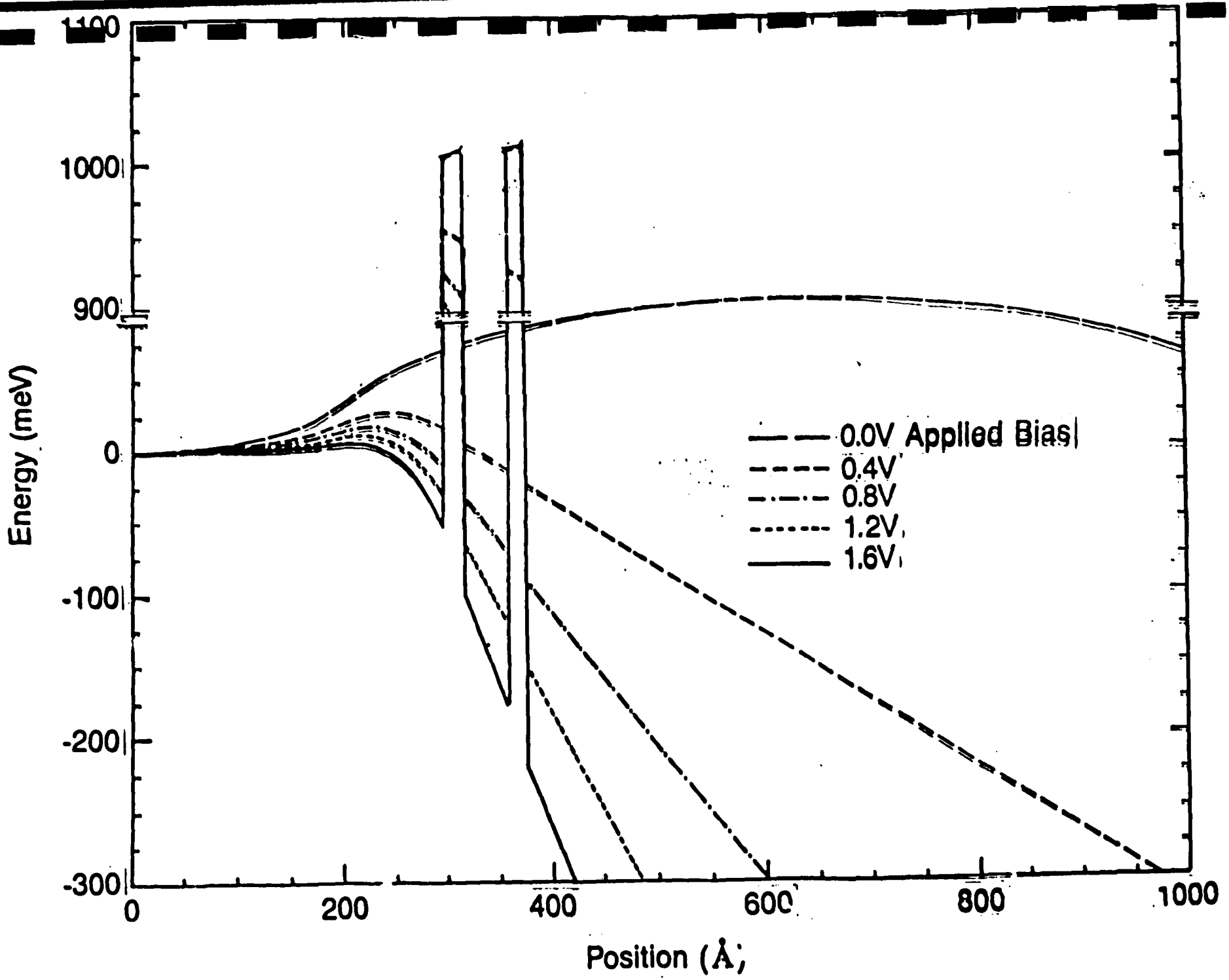
Quasi-Bound States in the Accumulation Layer



Finding the Bias Voltage for the Peak Current

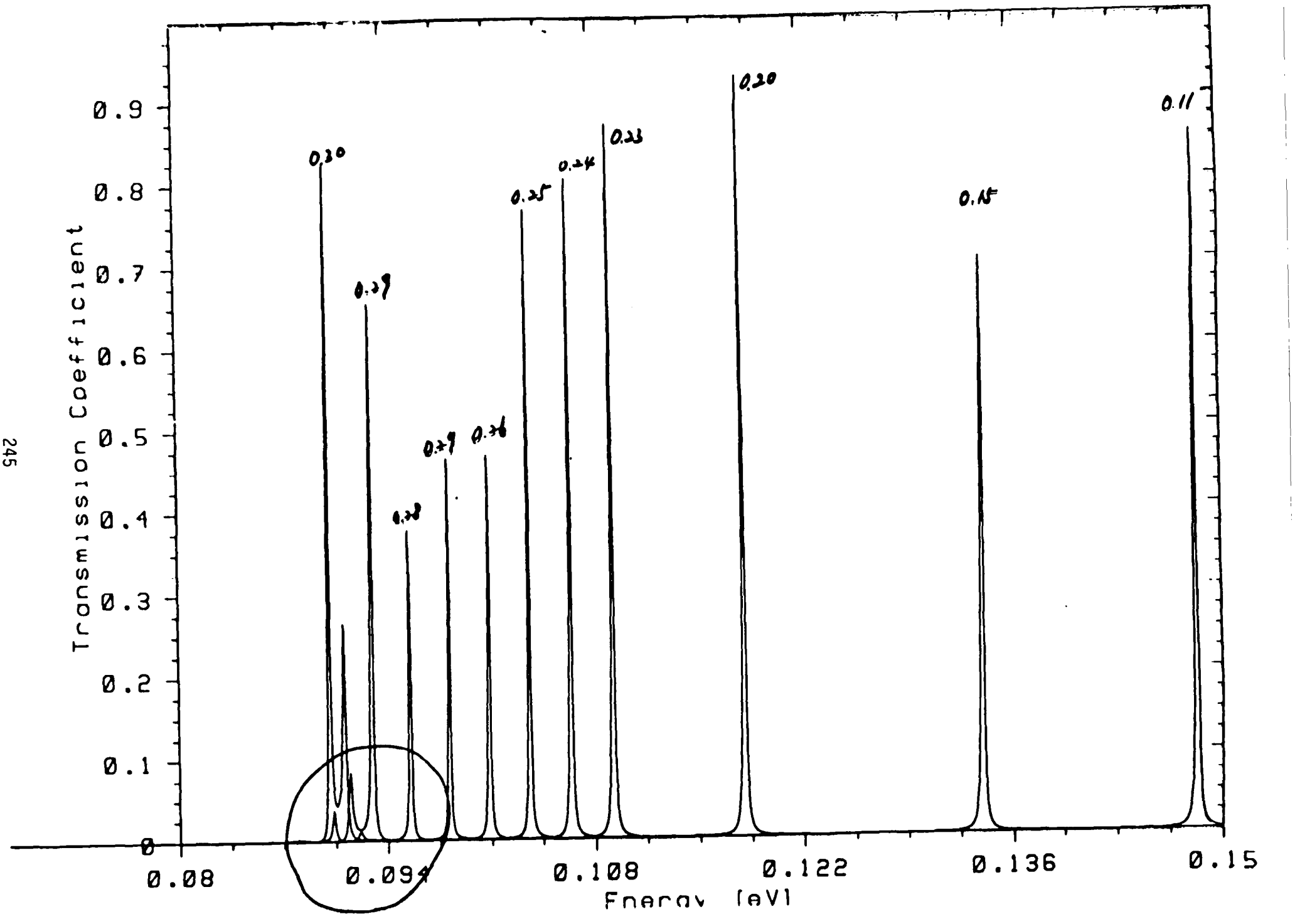


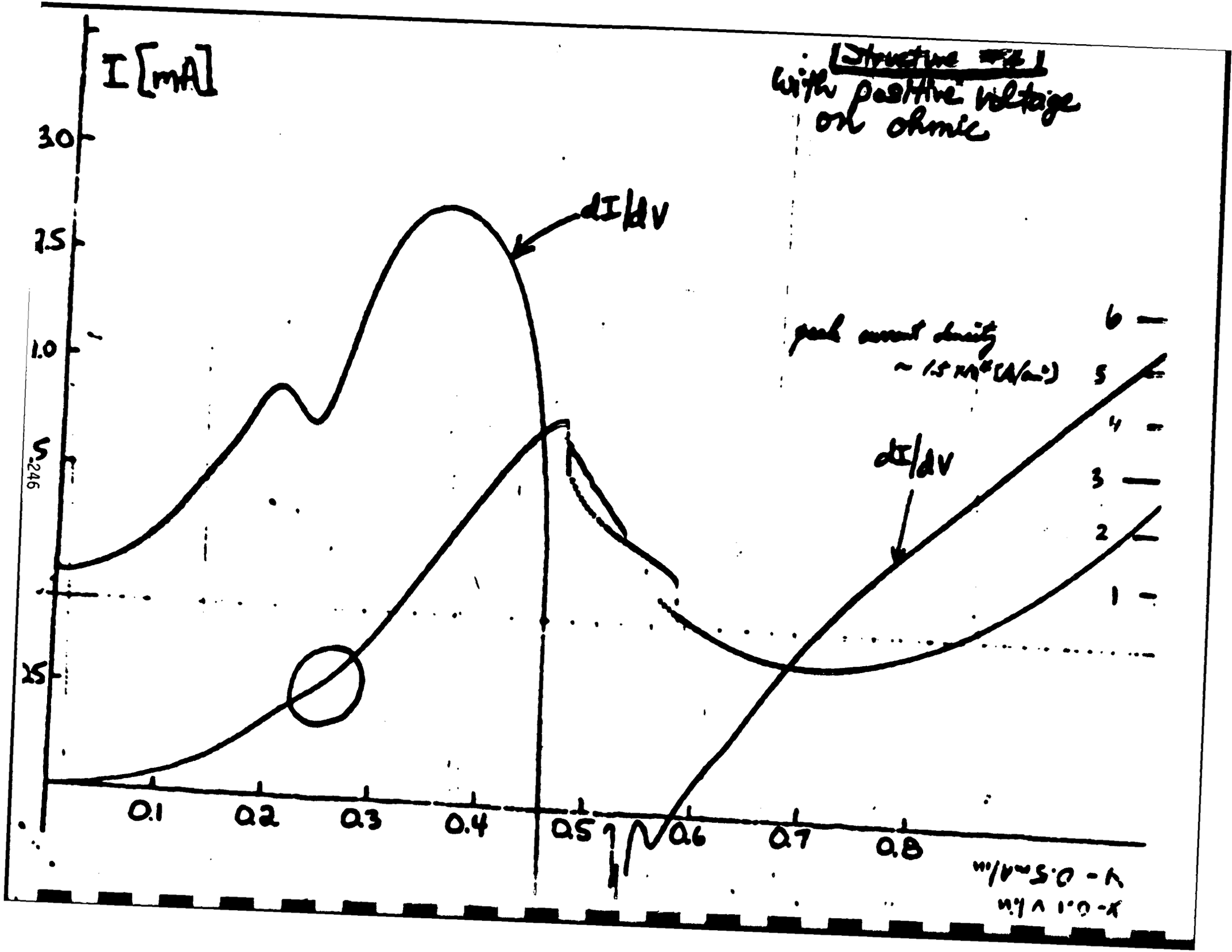

1000
900
0
-100
-200
-300
Energy (meV)
0
200
400
600
800
1000
Position (Å)
0.0V Applied Bias
0.4V
0.8V
1.2V
1.6V


1100
1000
900
0
-100
-200
-300
Energy (meV)
0
200
400
600
800
1000
Position (Å)
0.0V Applied Bias
0.4V
0.8V
1.2V
1.6V

RESONANT TUNNELING DIODE DESIGN TRADEOFFS

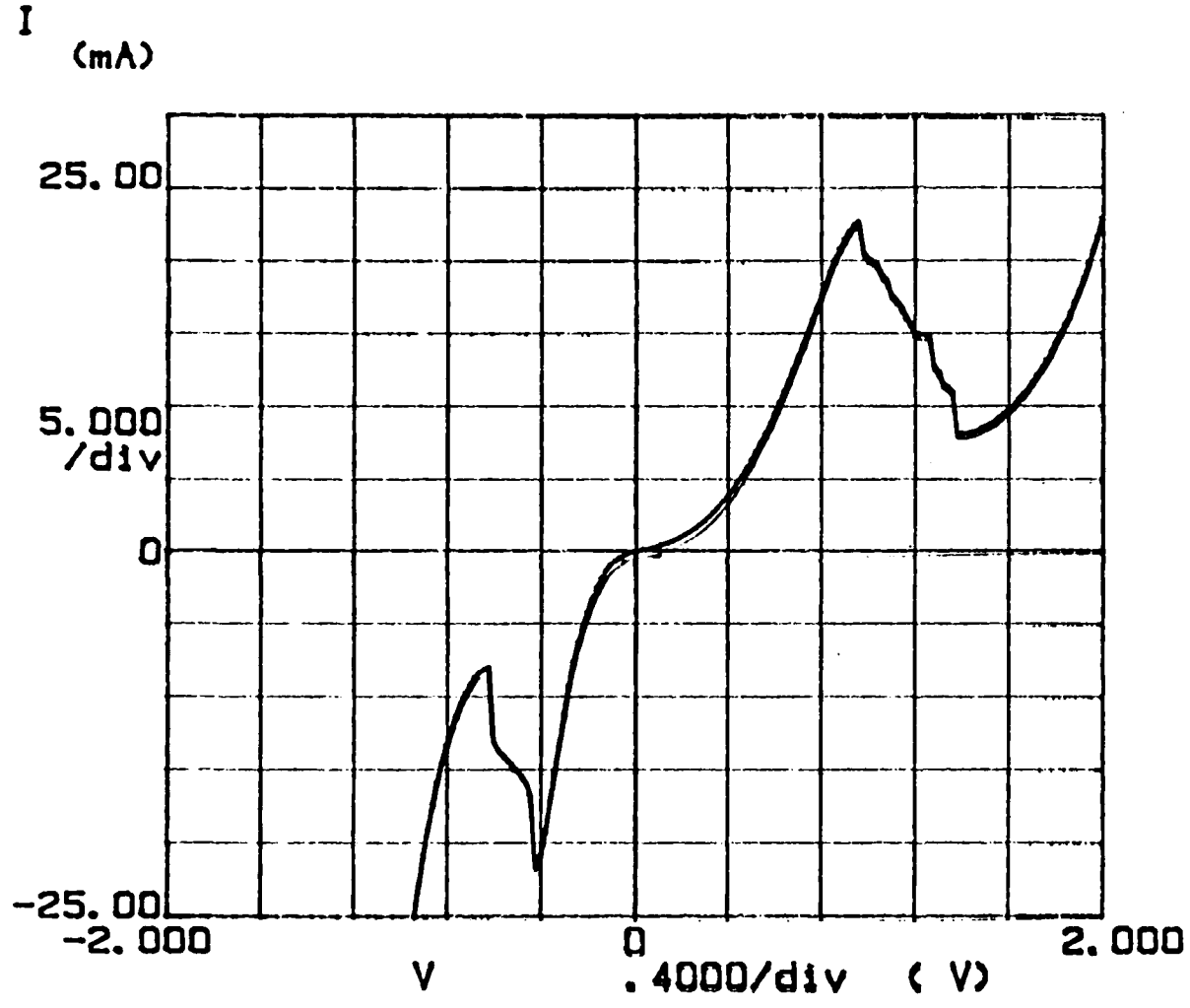
High Current Density	High Peak to Valley Ratio
- Transparent Barriers	- Less transparent barriers
- High Contact Doping	- Lower contact doping.
- Large difference in electron occupation at resonance.	- Undoped spacer layers.
	- Good interfaces and crystal quality.


Transmission Coefficient
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0.08
0.094
0.108
0.122
0.136
0.15
Energy (eV)
0.30
0.29
0.28
0.27
0.26
0.25
0.24
0.23
0.20
0.15
0.11


I [mA]
Structure #2
with positive voltage
on ohmic
dI/dV
peak current density
~ 1.5 kA/cm²
dI/dV
3.0
2.5
1.0
0.5
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
6
5
4
3
2
1
V - 0.5 V/div
V - 0.1 V/div

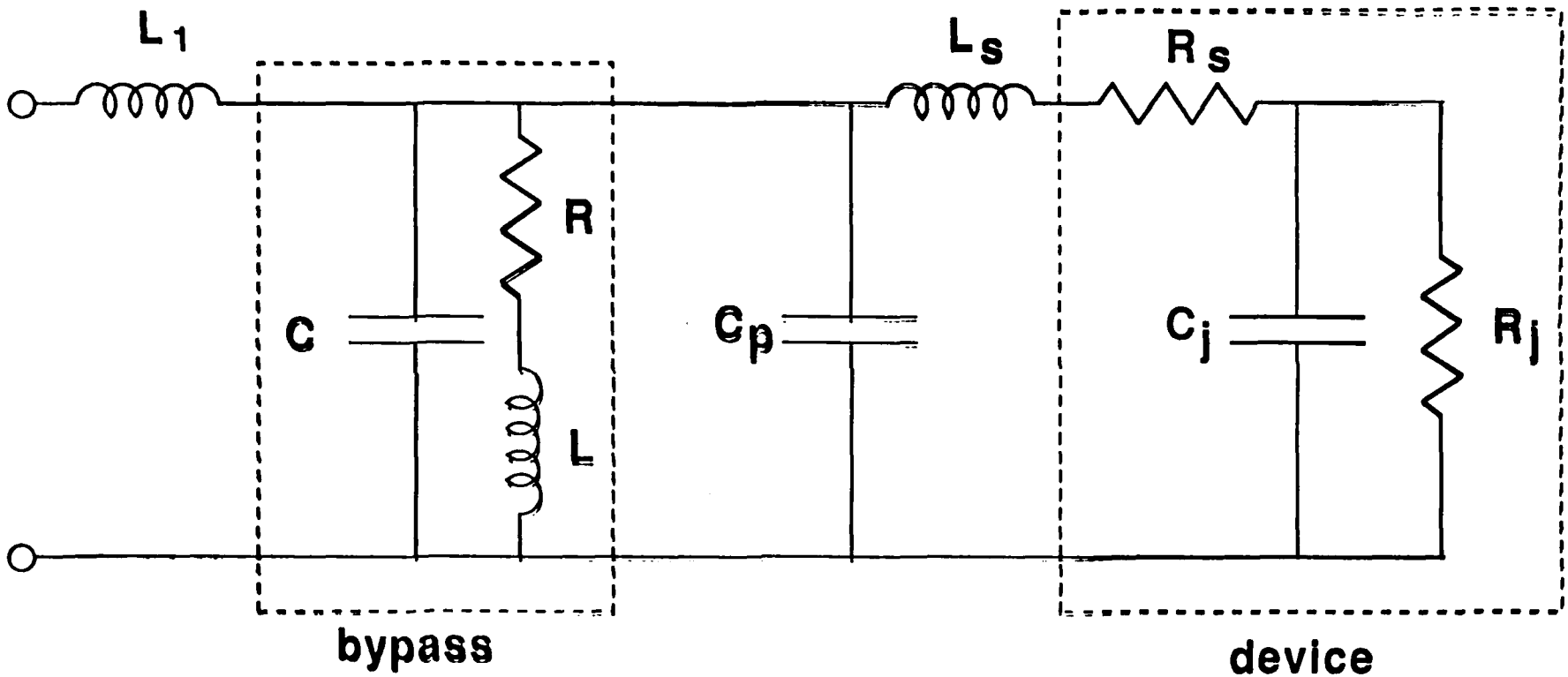
****** GRAPHICS PLOT ******

1071A-E3(P) 14um DIA 300K

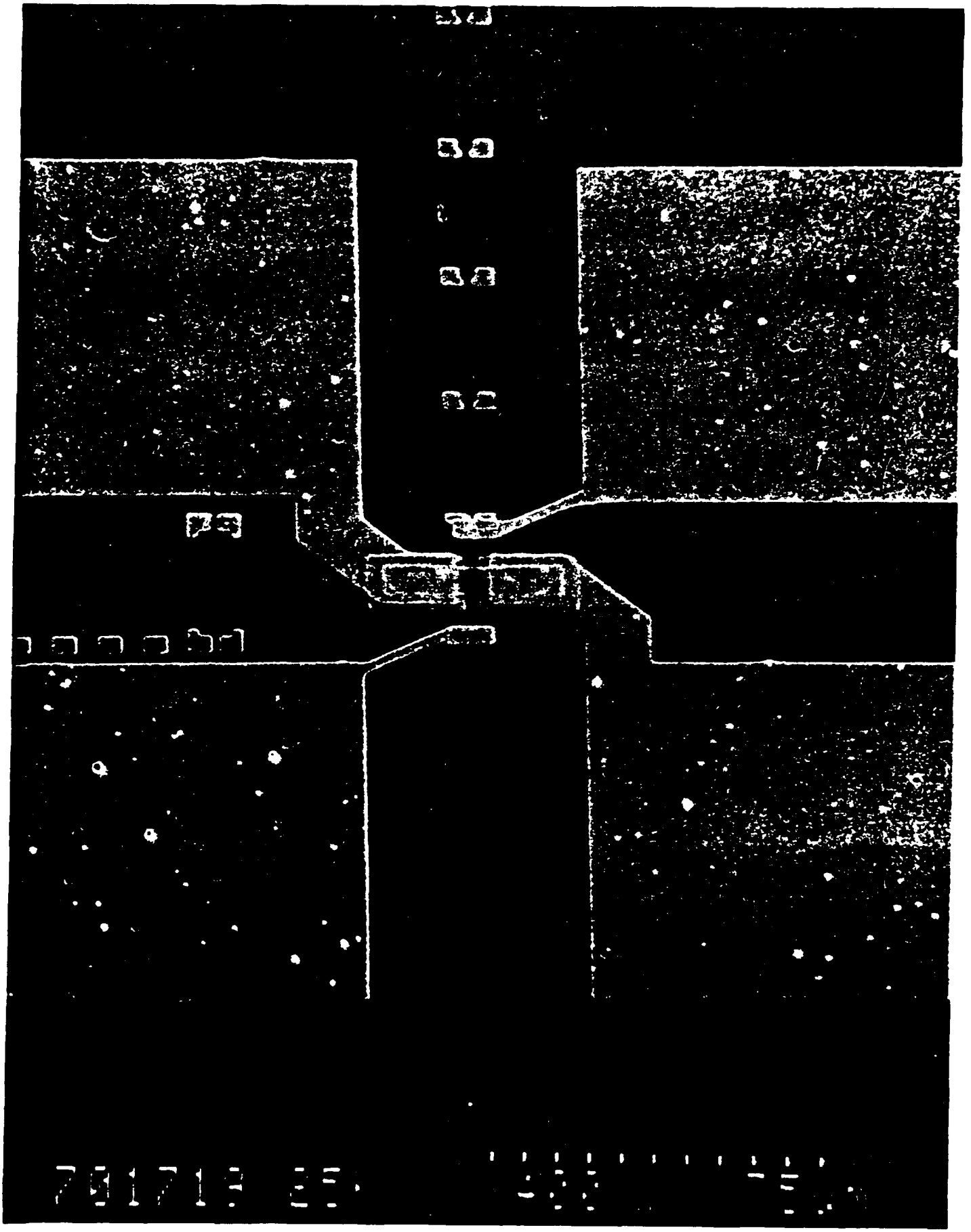


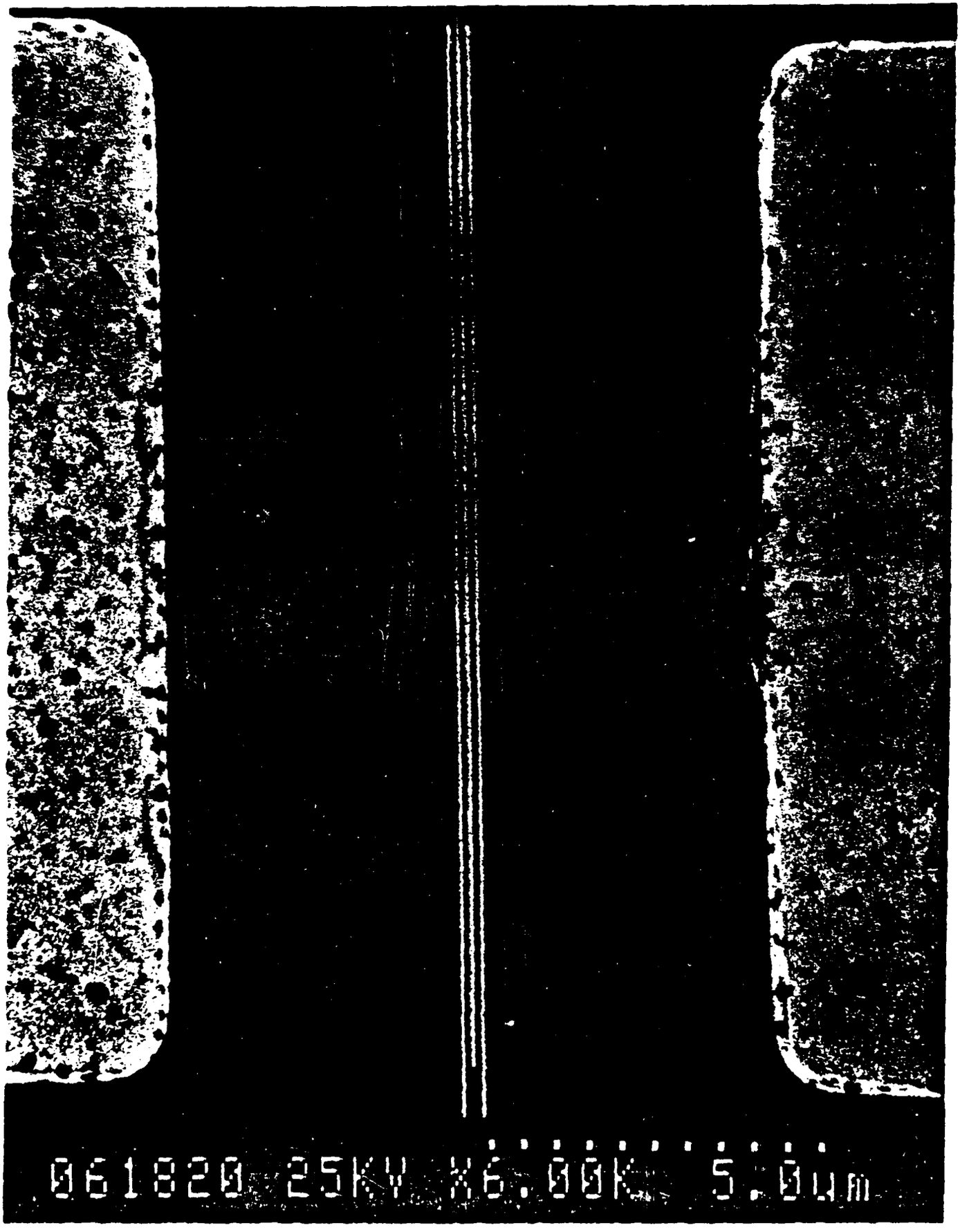
G (S) = ΔI/ΔV
R (Ω) = V/I

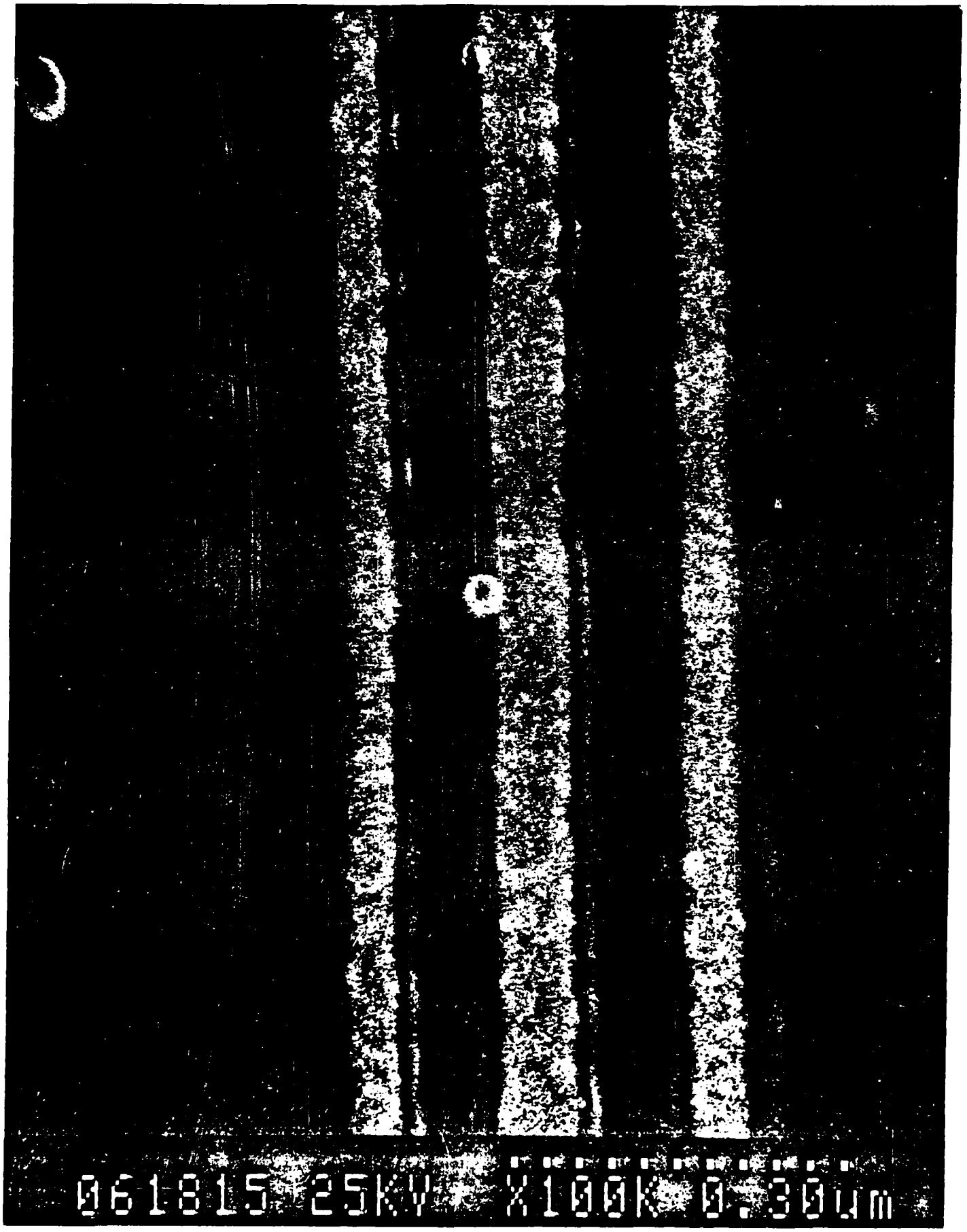
Equivalent Circuit for RTD and test fixture



L1=.65nH, L=.6nH, C=.2pF, R=10Ω, Cp=.28pF, Ls=.5nH, Rs=10Ω,
Cj=.68pF, Rj=200Ω (V=0v.) or Cj=.75pF, Rj=140Ω (V=1v.)

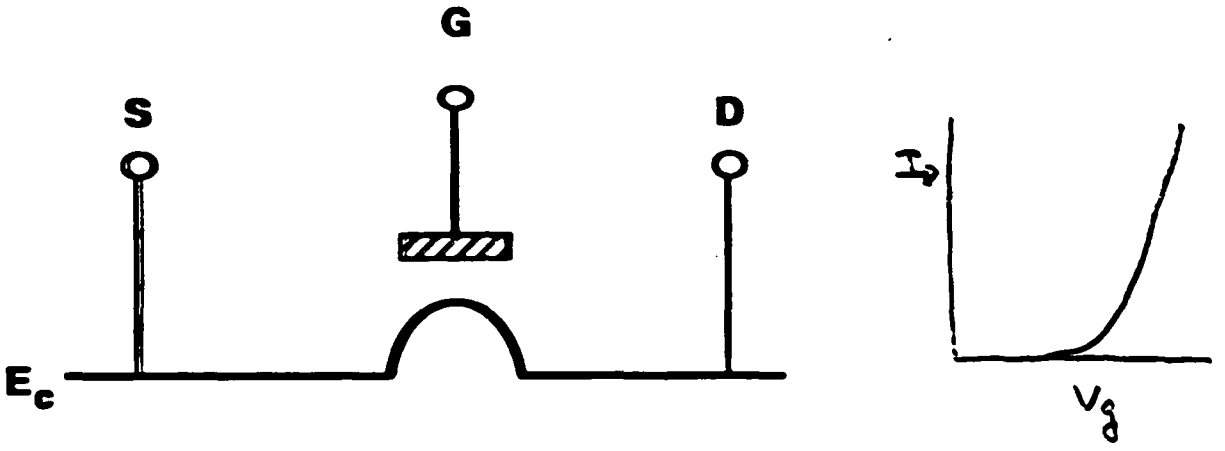


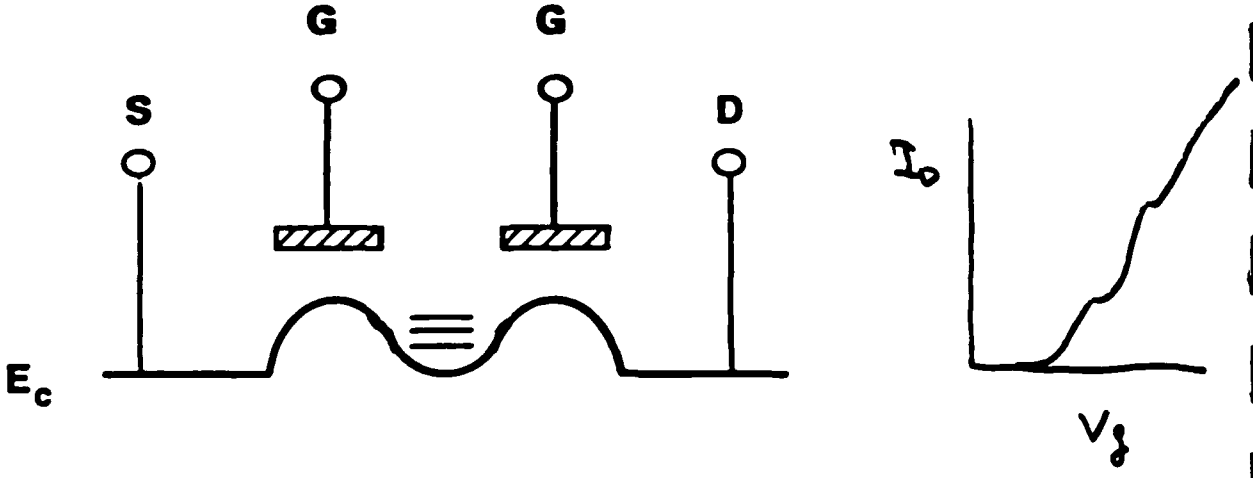

061820 25KV X6.00K 5.0um


061815 25KV X100K 0.30um

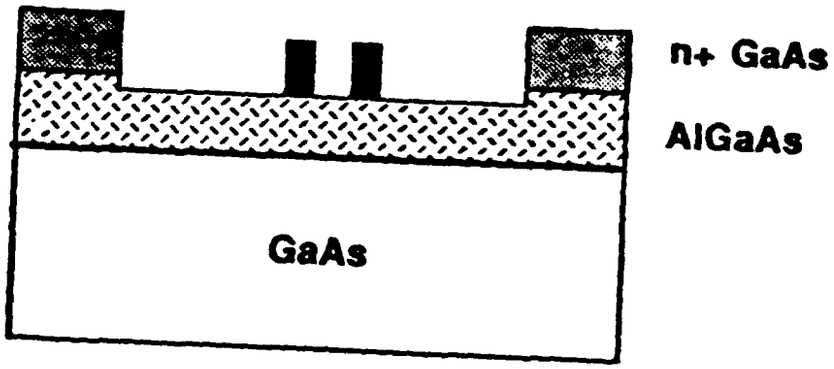
Operation Mode 1:

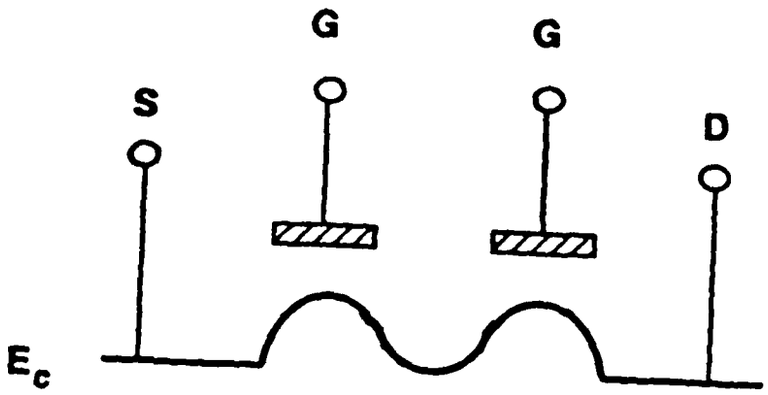
Fix Vds, Vary Vg.

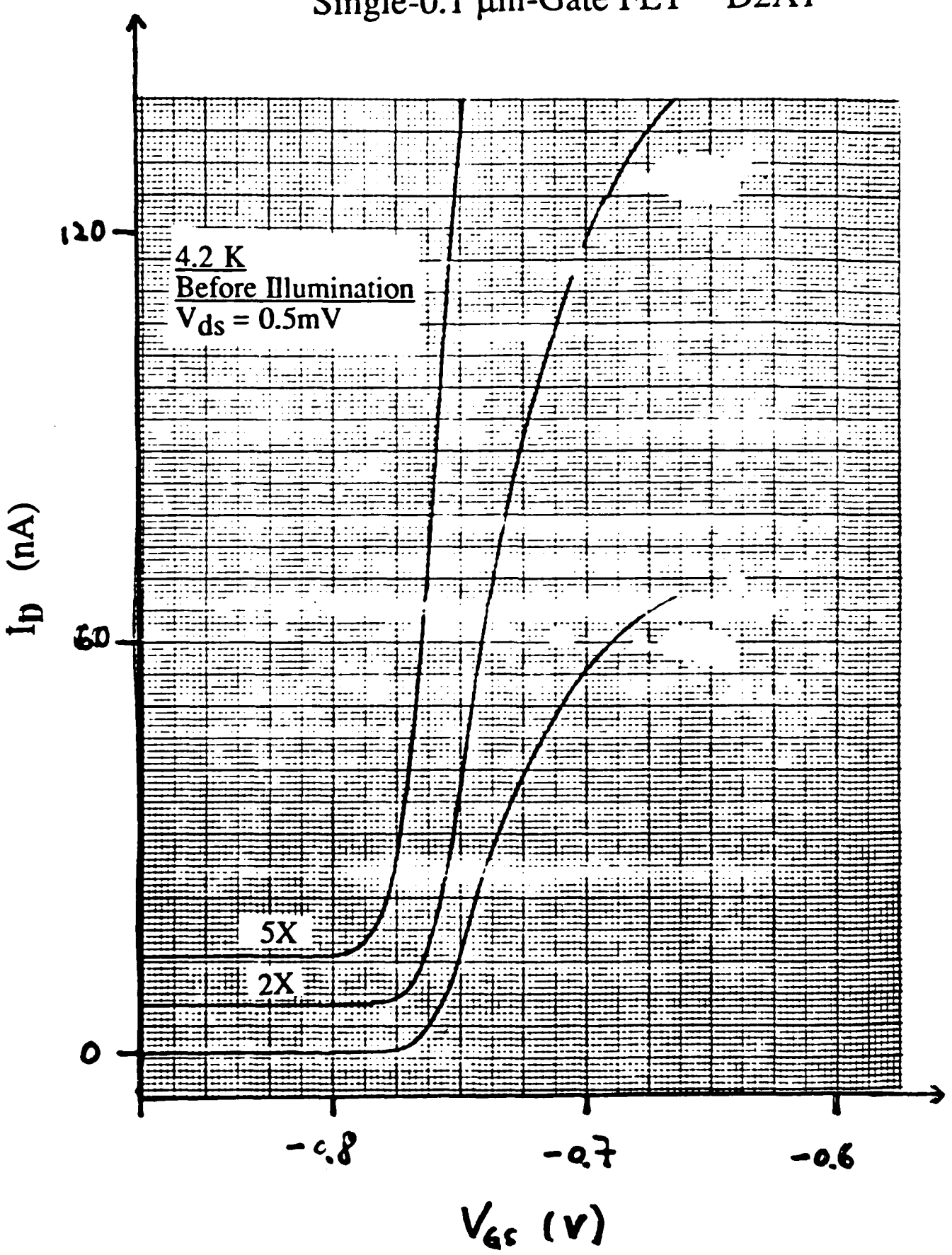




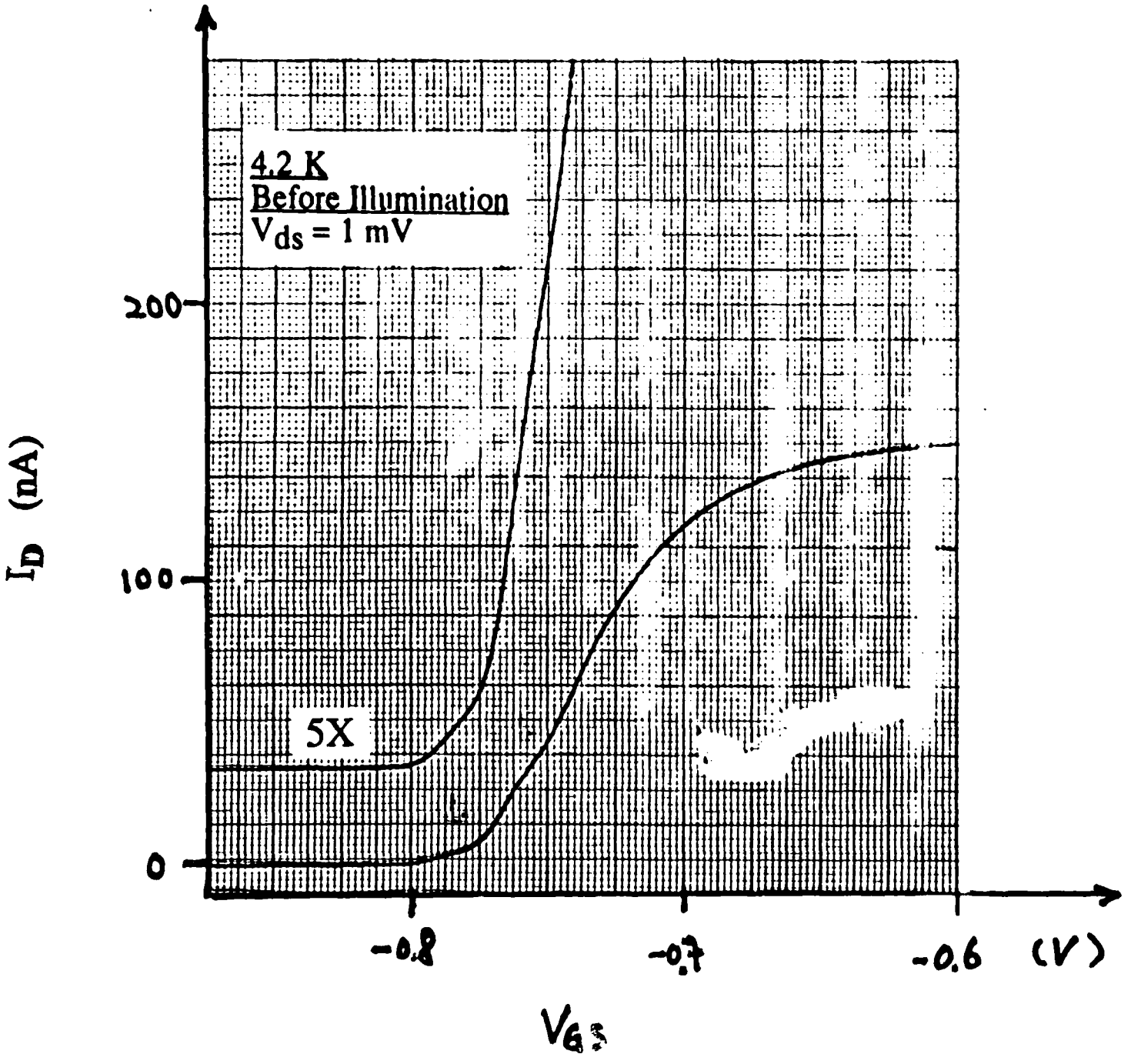
Dual-Gate LRTFET





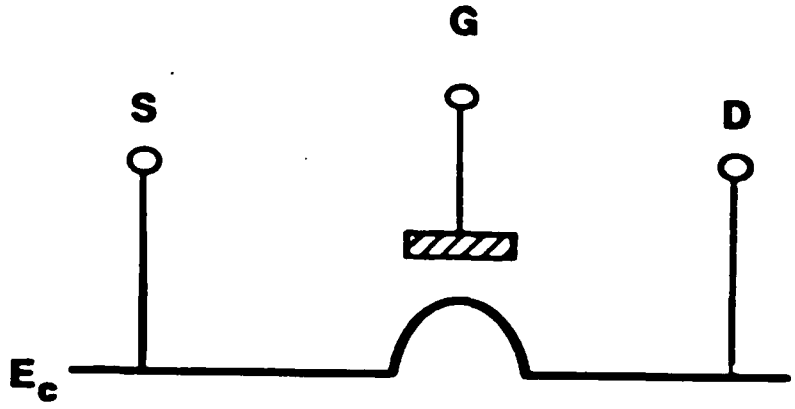

Single-0.1 μm-Gate FET D2A1
4.2 K
Before Illumination
V_{ds} = 0.5mV
120
60
0
I_D (nA)
5X
2X
-0.8
-0.7
-0.6
V_{GS} (V)

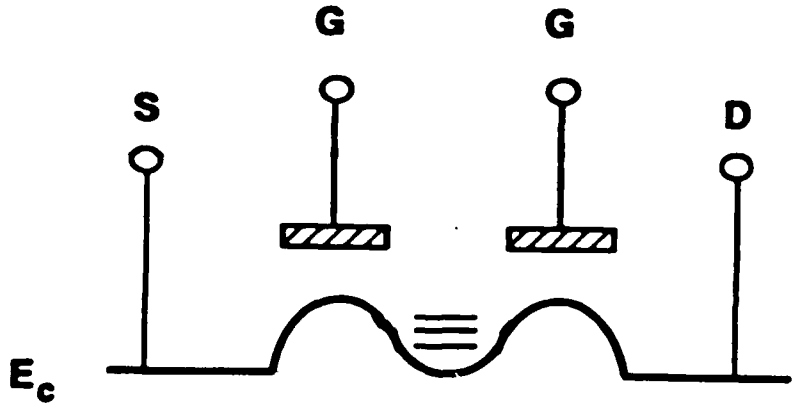
Dual-0.1 μm-Gates FET (Gate Spacing 0.1μm) D2A2



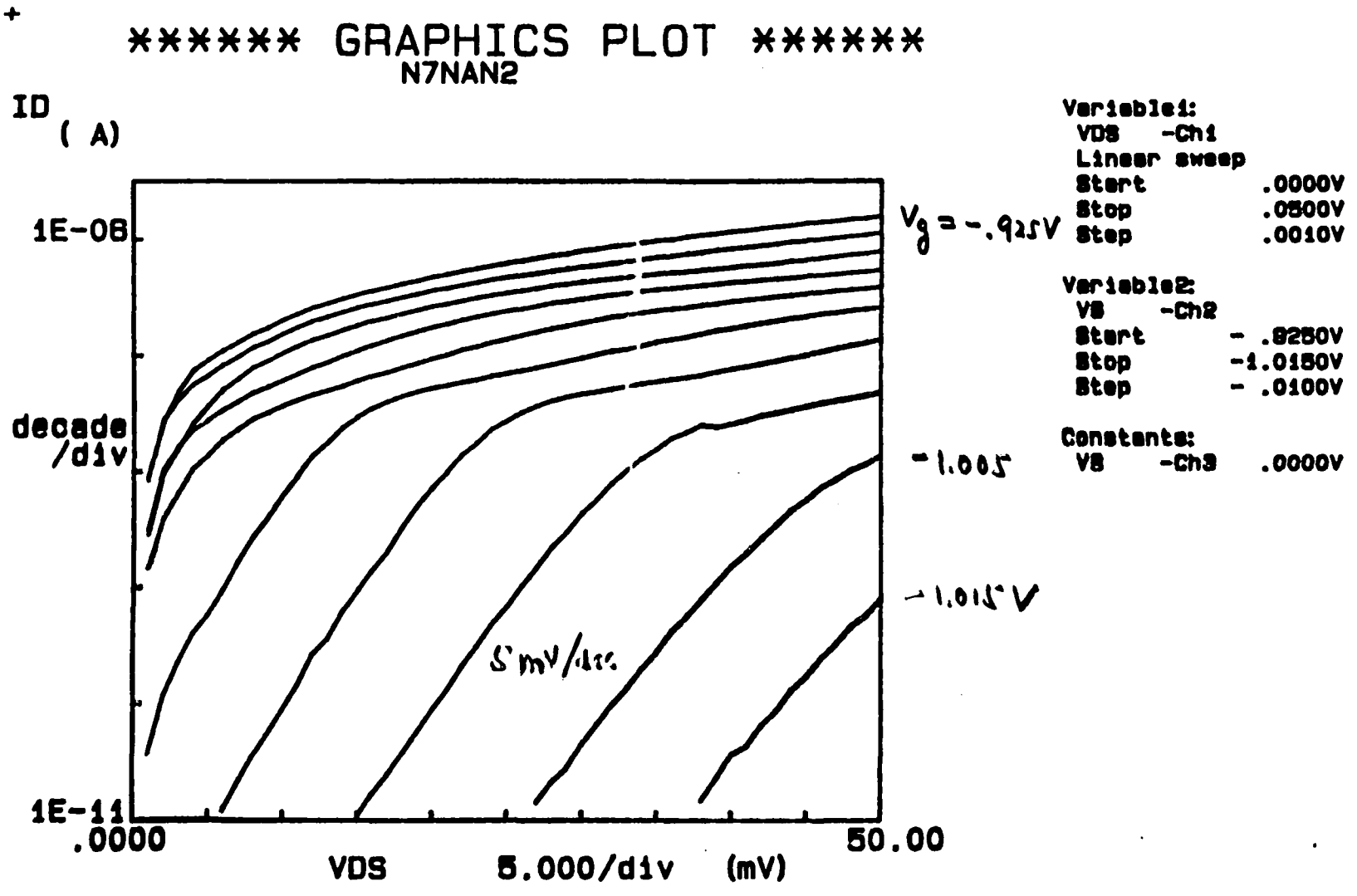
Operation Mode 2:

Fix Vg, Vary Vds.

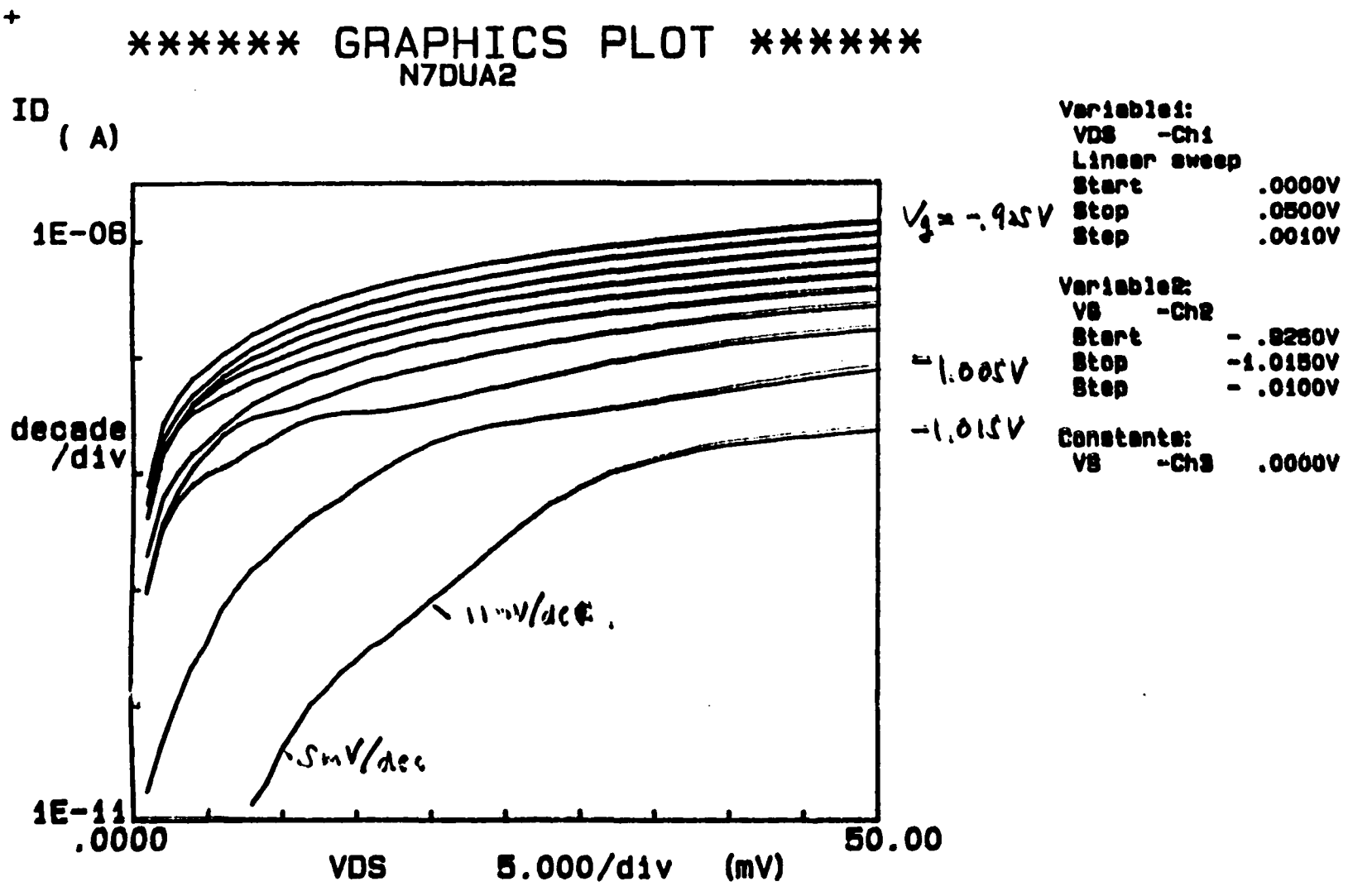




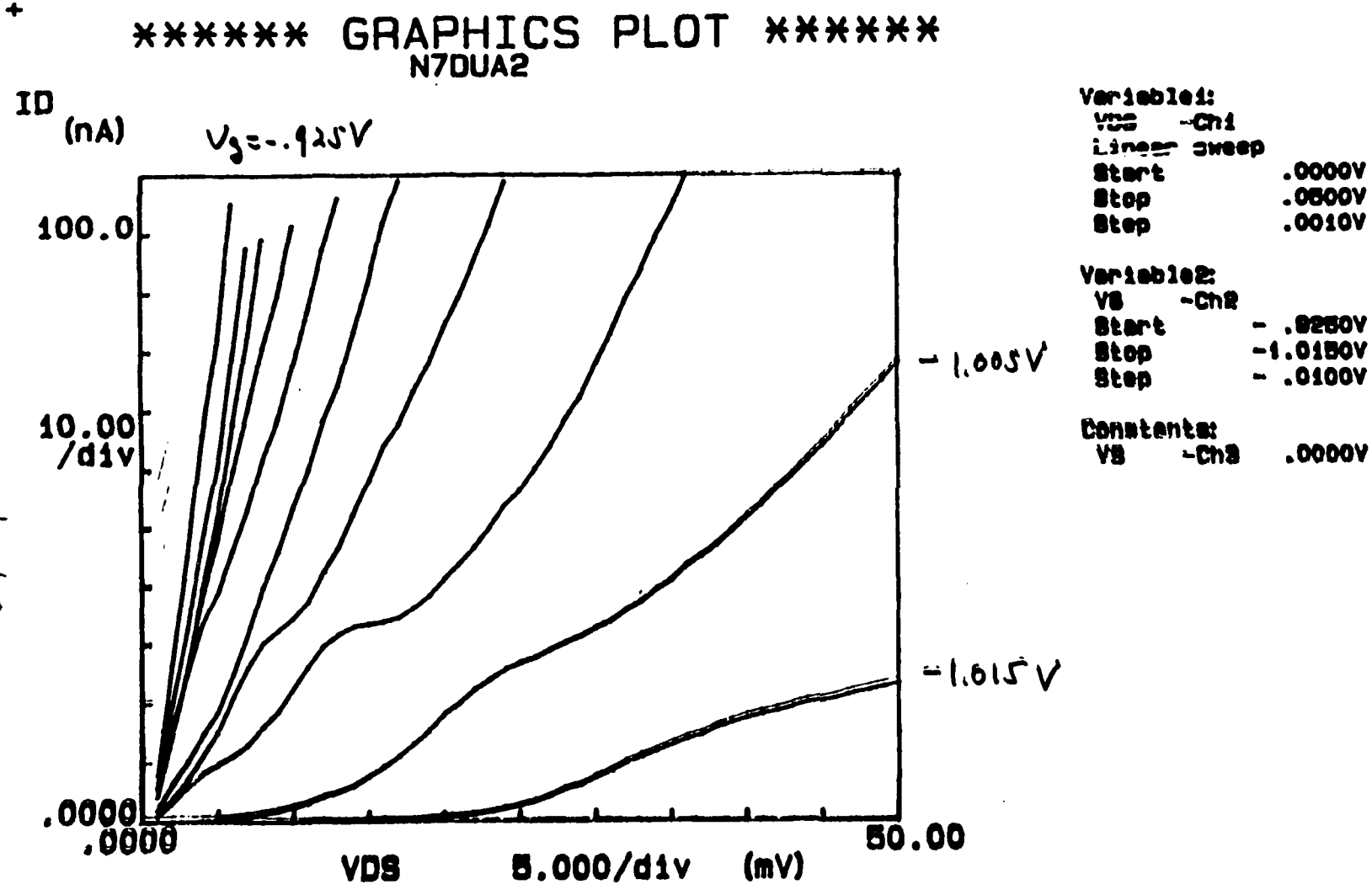
Single 0.1 μm gate FGT.



Dual 0.1 μm-gate LRTFET



Dual 0.1 μm-gate LRTFET.



259/260

Array Applications

Phillip M. Smith

General Electronics
Syracuse, NY

ARRAY APPLICATIONS

Phillip Smith
GE Electronics Laboratory
Syracuse, NY

Collaborators: P.C. Chao, J.M. Ballingall, K.H. Duh, L.F. Lester, P. Ho, B. Lee, R.P. Smith, D.W. Ferguson, A.A. Jabra, W. Kopp, A. Tessmer, M. Kao, D.A. Bates

Outline

- **Phased Arrays**
  - MMW Applications
  - GE V-Band Array Development
- **Device Technology for MMW Phased Arrays**
  - InGaAs Pseudomorphic Power HEMT
  - Low Noise HEMT
  - 0.1μm Pseudomorphic HEMT
  - InP-Based HEMT

Millimeter-Wave Applications

(From R. Sudbury)

FREQUENCY	APPLICATION
20 GHz	Communications
30 GHz	* Communications
32 GHz	* Deep Space Communications
35 GHz	Seekers Guidance Communications
44 GHz	* Communications
60 GHz	* Inter Satellite Communication Short Range Covert Communication * Space Based Radar
94 GHz	Fuze Projectiles Radar Smart Munitions

*Contracts using GE HEMTs

Why Solid State Phased Array?

- Agile Beam
- Efficient Power Combining in Space
- Solid-State Reliability
- Graceful Degradation

ISSUES FOR MMW PHASED ARRAYS	SOLUTION
Cost of Large Number of Elements	MMICs
Generation of Sufficient Power Per Element	Pseudomorphic HEMTs
Power Consumption/Thermal Loading	High Efficiency

60 GHz Communication Arrays

Satellite Crossfink Application

Principal Advantages

- Small Size Circuitry
- Light Weight
- Resistance to Ground Based Jamming
- High Agility/Reconfigurable

Module Technology Status

- Pseudomorphic HEMT (High Power, Low Noise, and Phase Shifter)
  - 7 dB Gain, 1.8 dB NF
  - 100 mW Power, 22% Efficiency
  - (DSCS HESSA Amp is Approximately 25%)
  - AFWAL 60 GHz LNA Contract Shutting Down
  - 60 GHz LNA Being Process on AFWAL LNA Contracts (AFWAL Shutting Down)

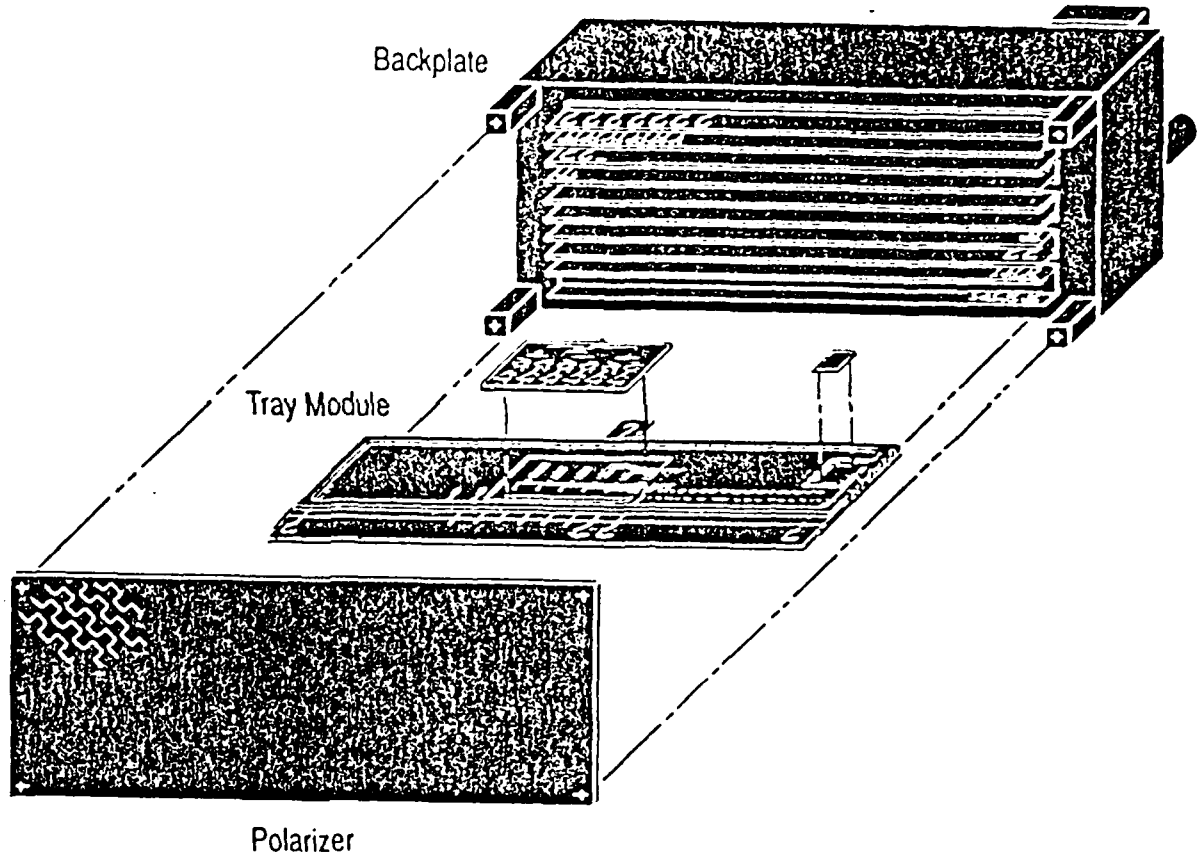
Resulting Hardware Capability

- Tx Array - EIRP 50 dBW, Approximately 4" x 4", 3 lbs (100 WRF)
- Rx Array - Gain 30dB, 4dB NF, 4" x 4", 3 lbs (5 dB/Degree K)

Communication Array Technology

Key Technologies

- Array Construct
- HEMT MMICs
- Low Cost Tray Module
- Backplate Construction
- Circular Polarizer

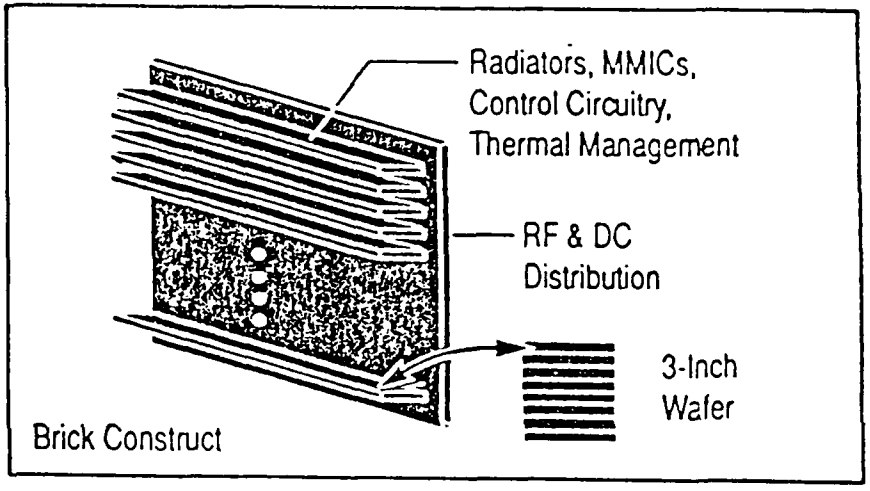


V-Band Phased Array Antenna Technology

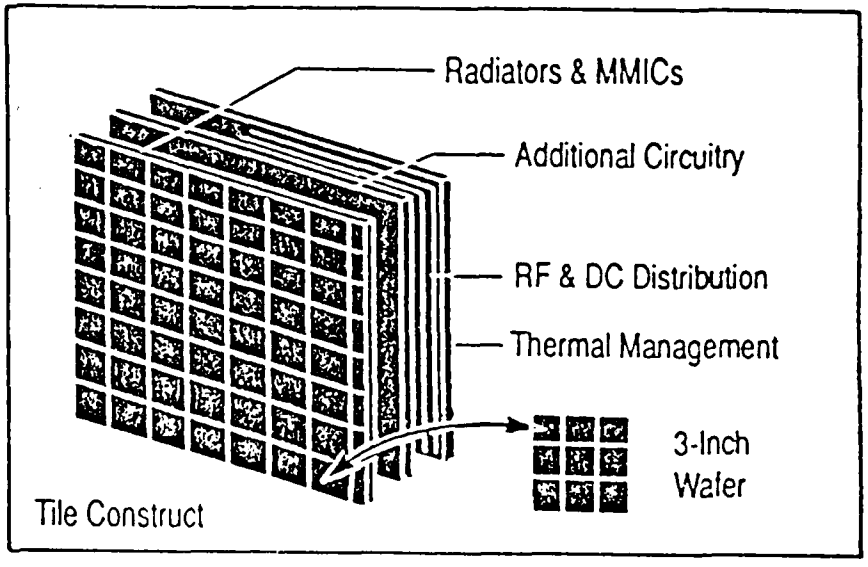
Brick Construct Advantages

- Modular Design With Tray Module.
- Depth Dimension Relaxes Size Restriction on MMICs Imposed by Element Pitch.
- Replaceable Tray Modules for Repairability/Maintainability.
- Array Design Not Constrained by MMIC Processing Yield.
- Accommodates Interleaved Thermal Cooling Channel and Tray Modules.
- Allows Hermetic Sealing and Shielding of Critical Circuitry.
- Applies to Both Transmit and Receive Arrays.

GE Approach

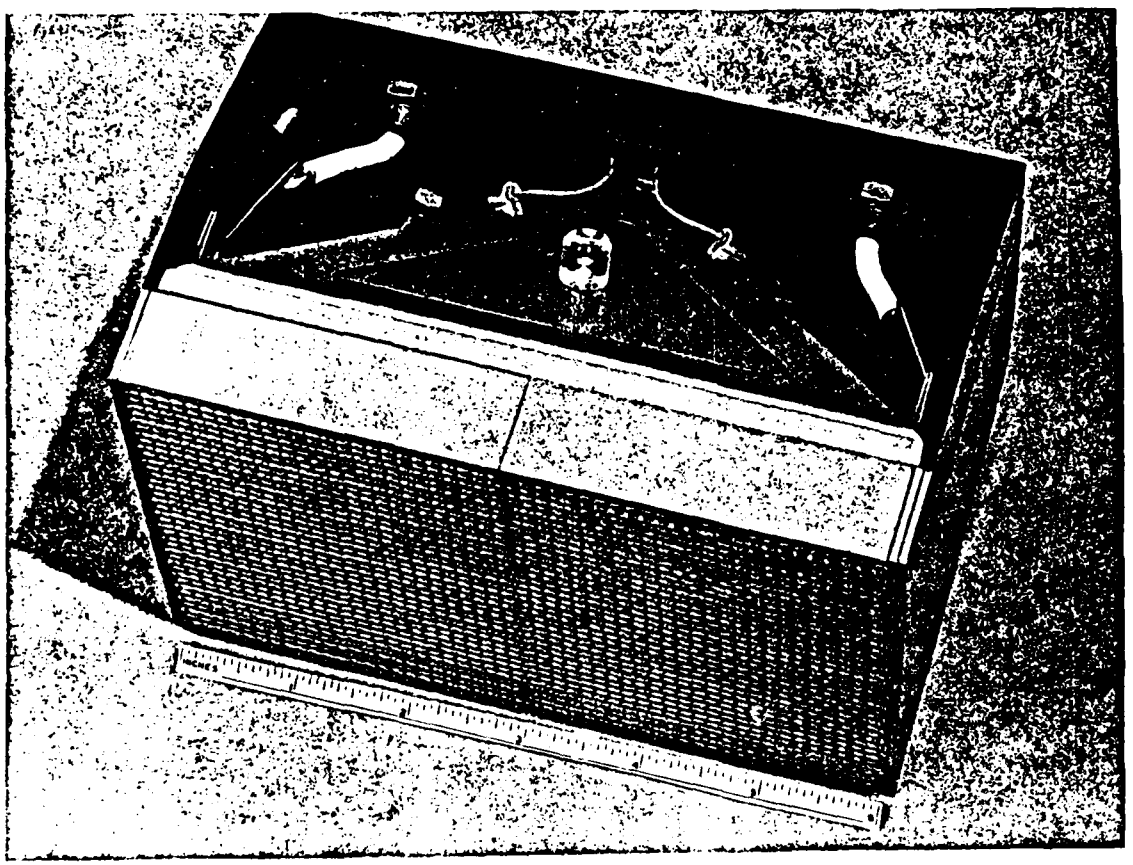


"Conventional" Approach



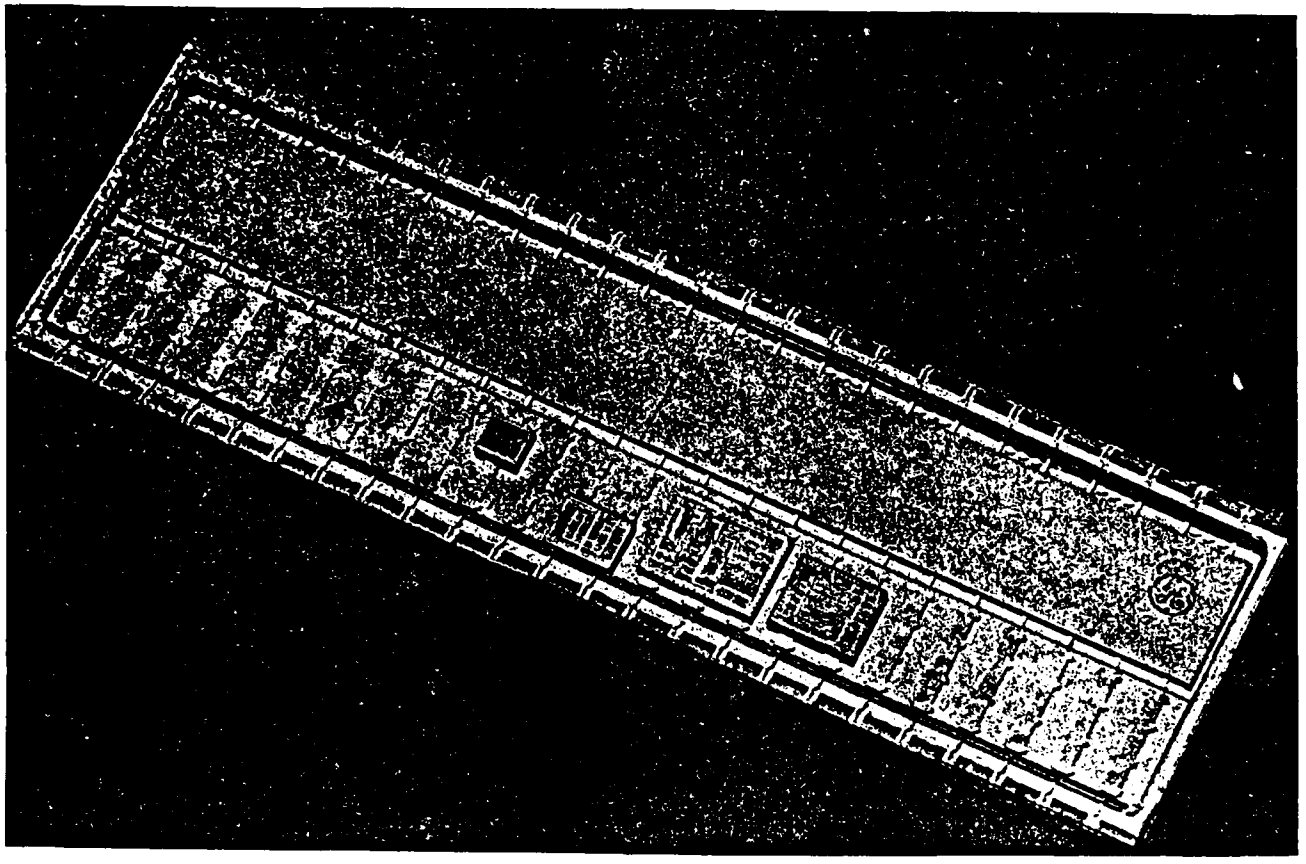
Model of 60 GHz Phased Array

GE Aerospace



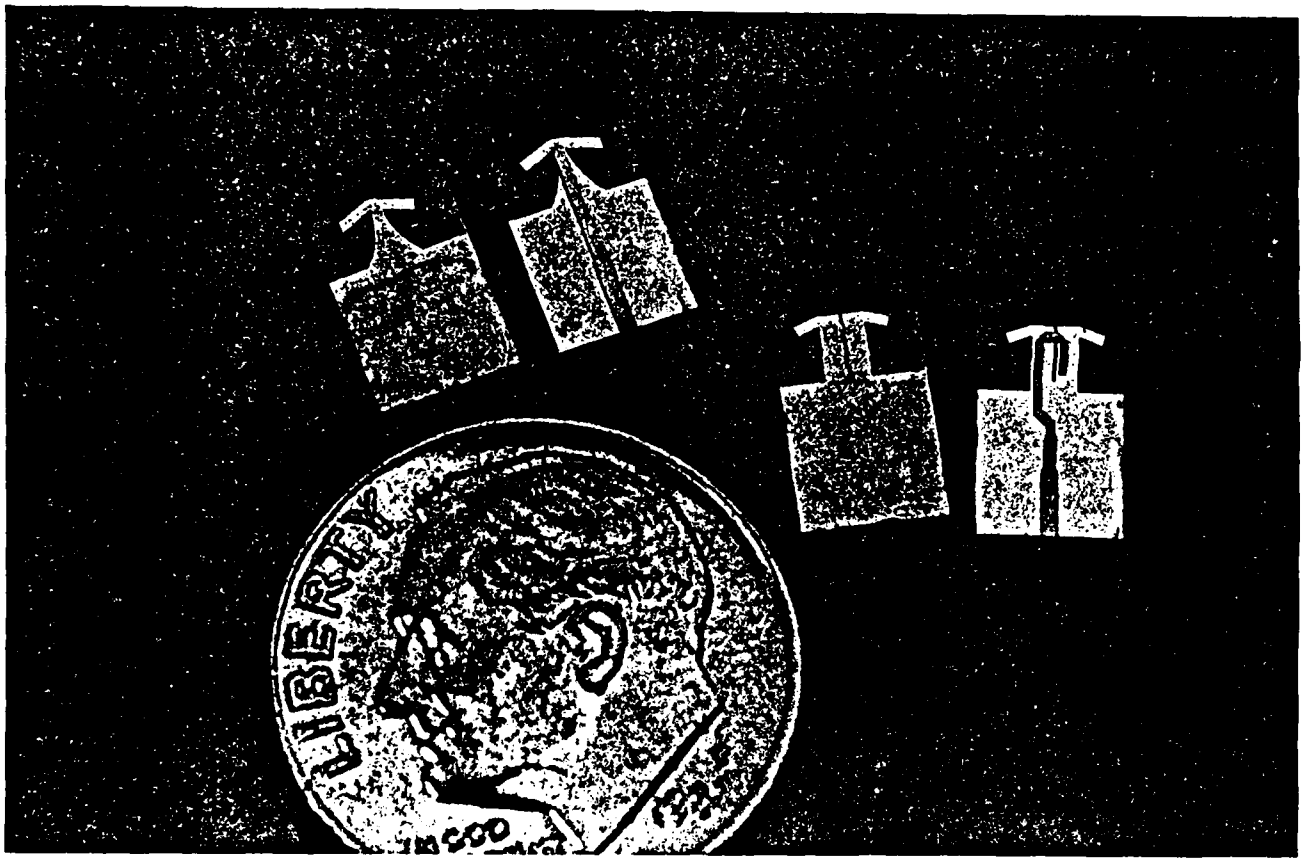
24 Element Tray Assembly - 60 GHz Phased Array

GE Aerospace



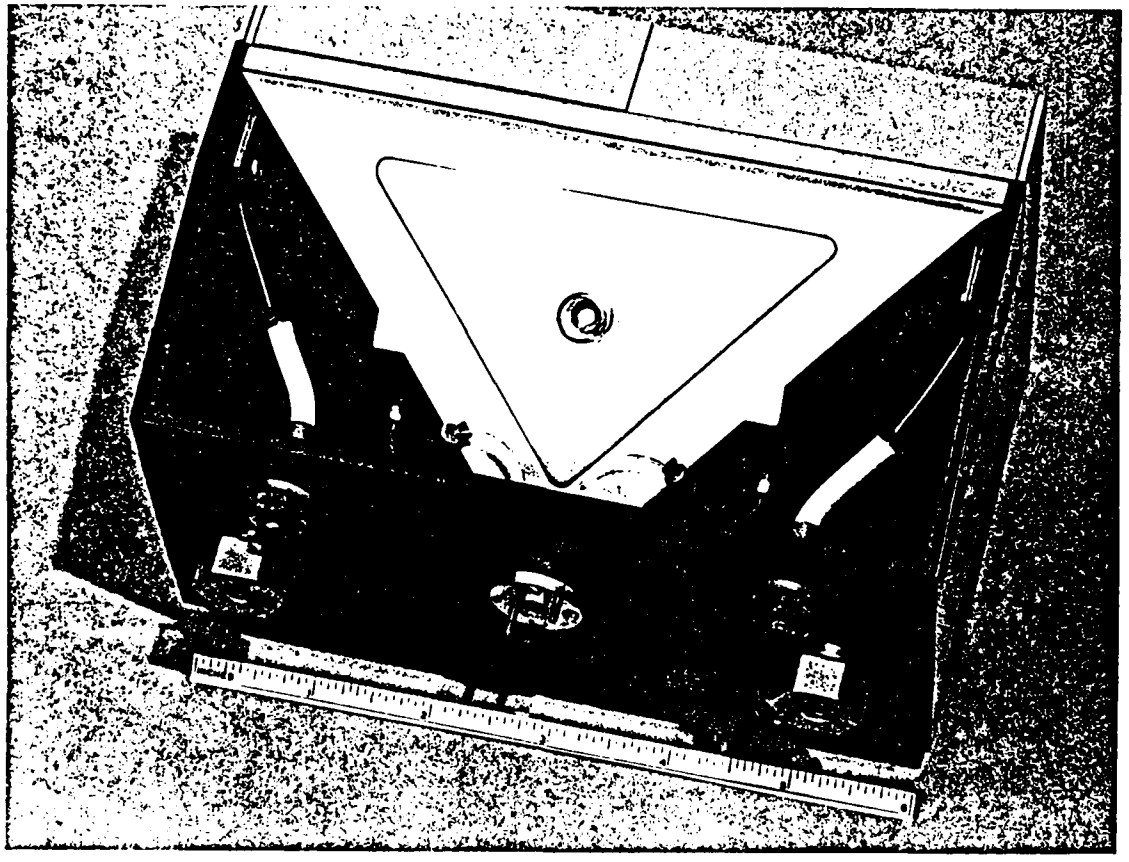
60 GHz Dipole Radiating Elements

GE Aerospace



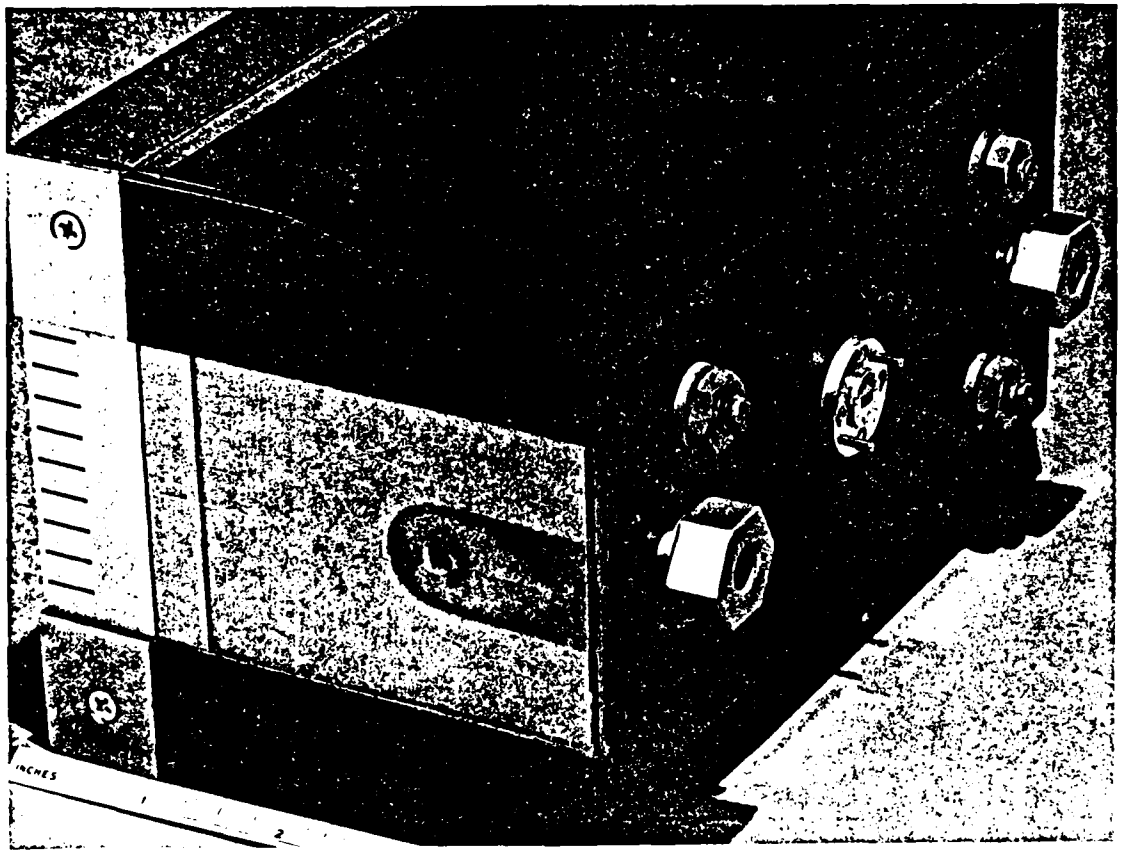
60 GHz Phased Array - Rear View

GE Aerospace



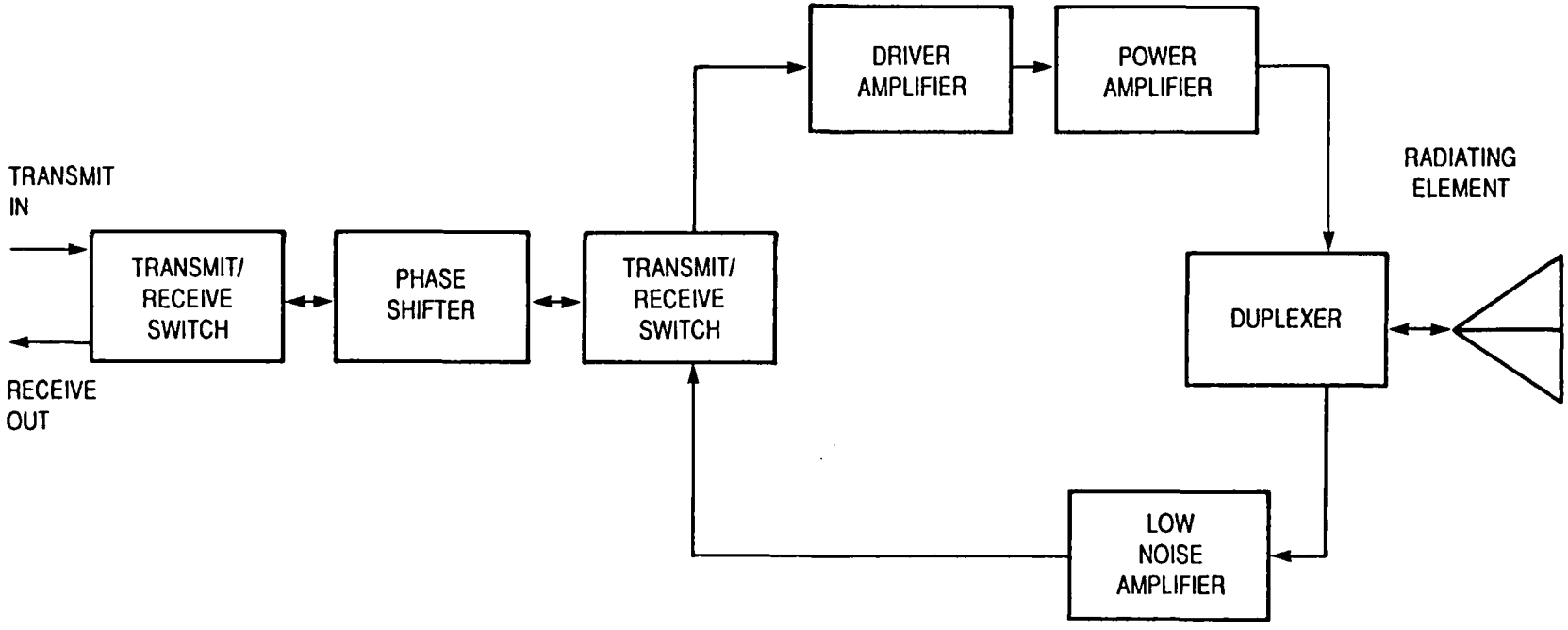
60 GHz Phased Array - Side View

GE Aerospace



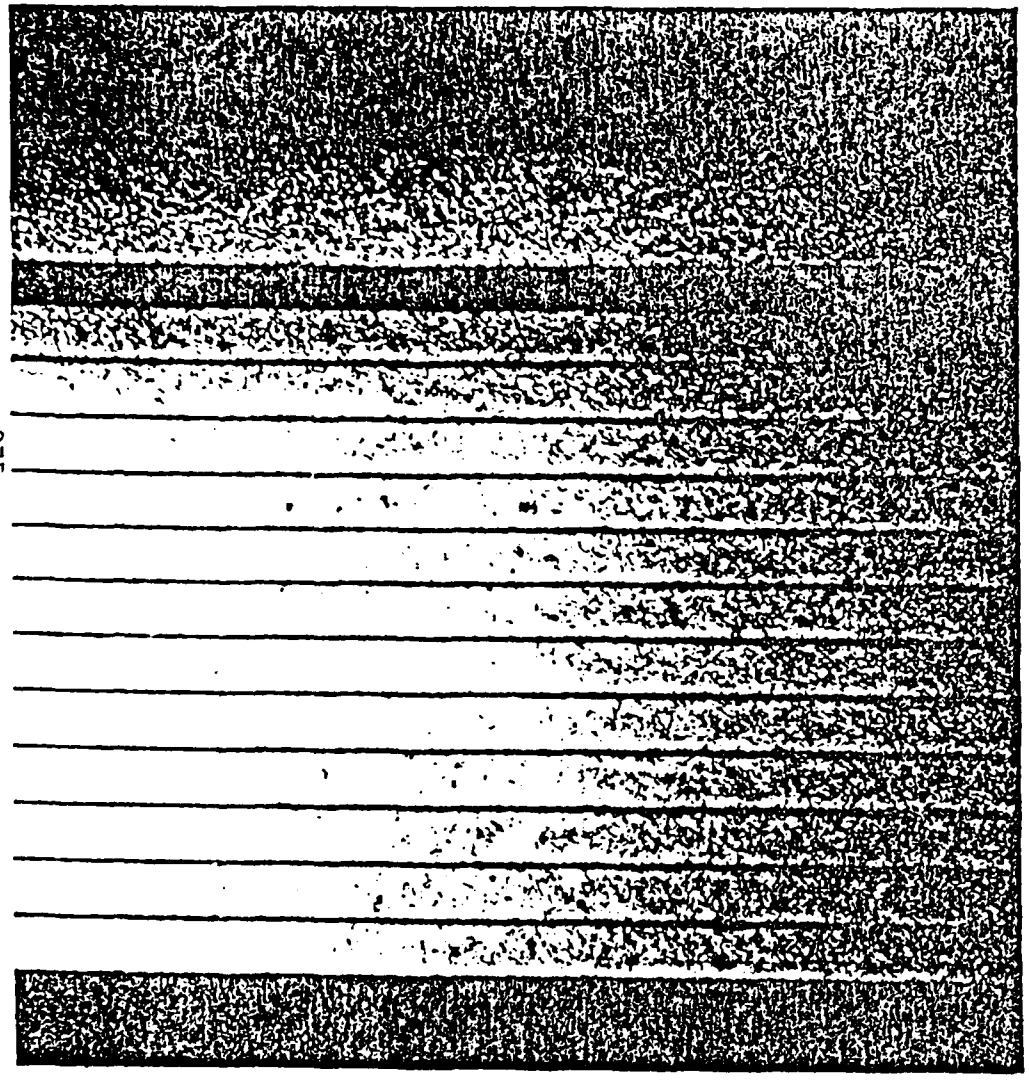
Transmit/Receive Module

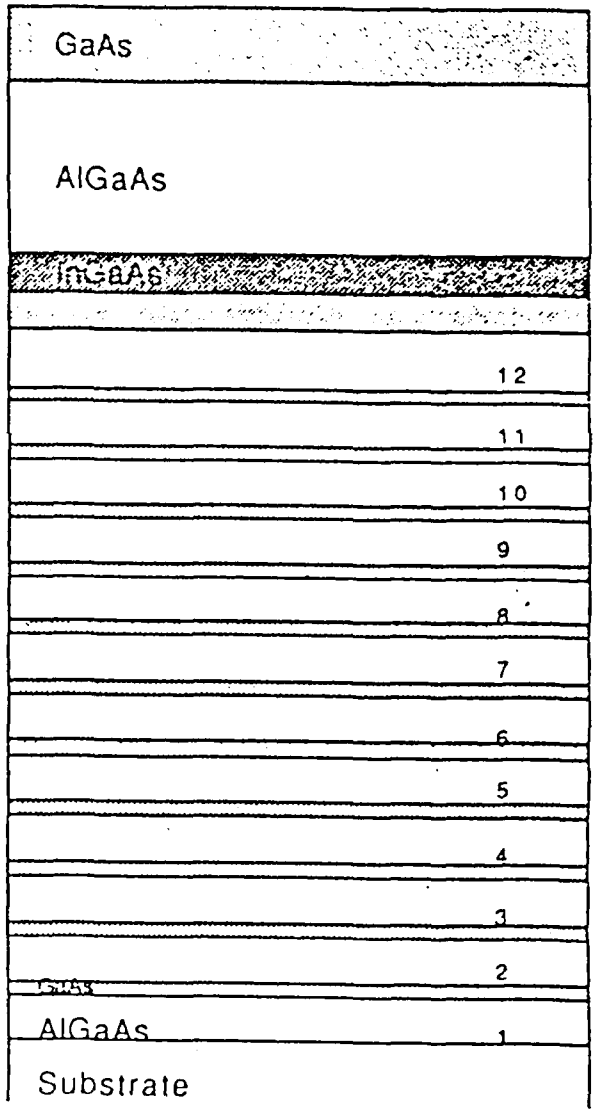
(From R. Sudbury)



TEM Cross Section of Pseudomorphic HEMT

GE Aerospace Laboratories

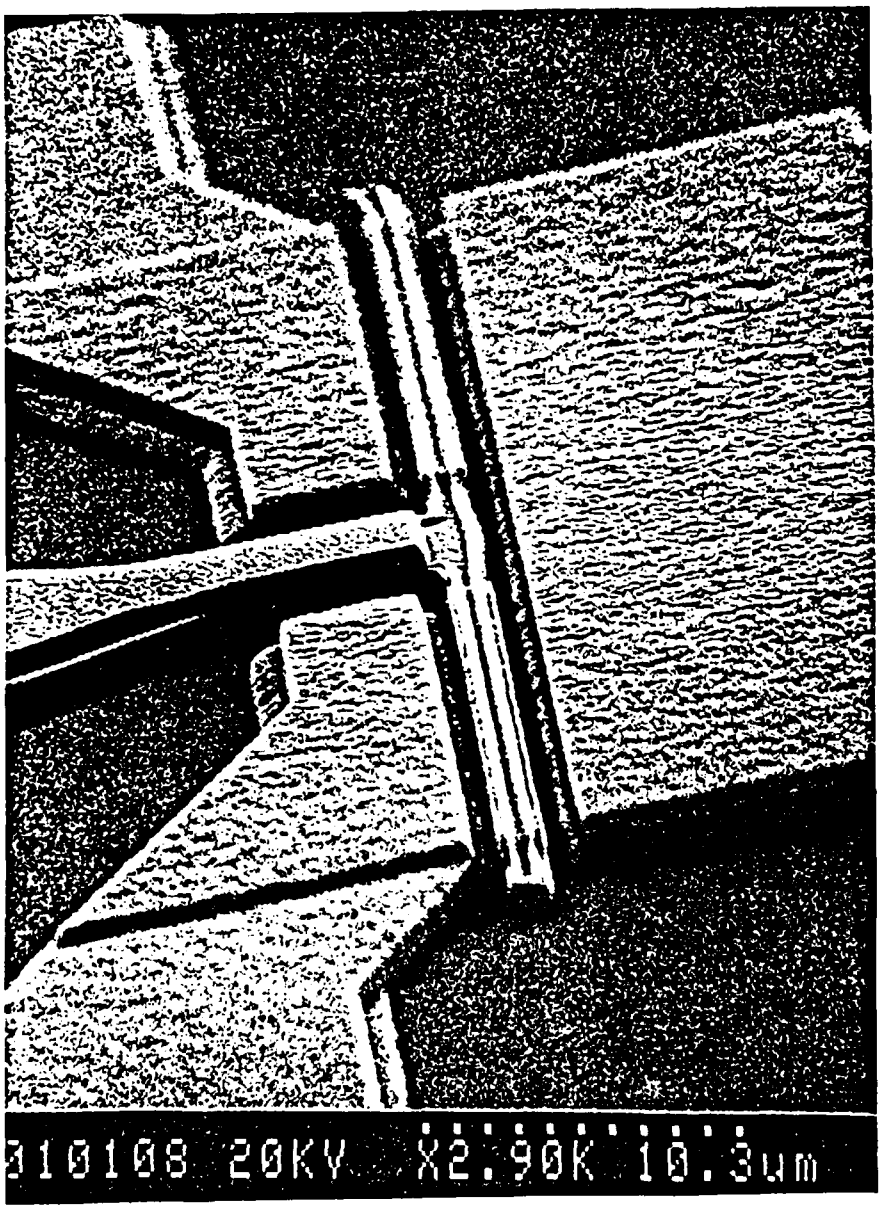




Layer	Thickness, Å
GaAs	319
AlGaAs	439
InGaAs	99
	51
12	195
	11
11	195
	11
10	
9	
8	
7	
6	
5	
4	
3	
2	195
	11
AlGaAs 1	195
Substrate	
Total:	3369

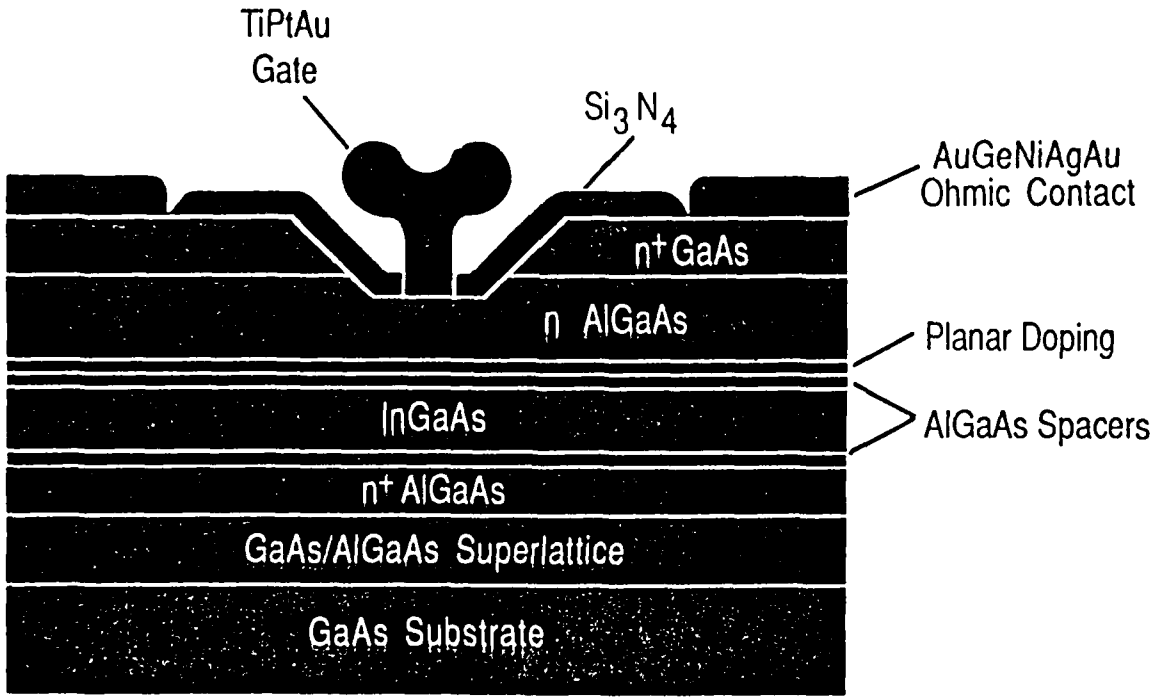
HEMT With 0.25μm T-Shaped Gate

GE Aerospace

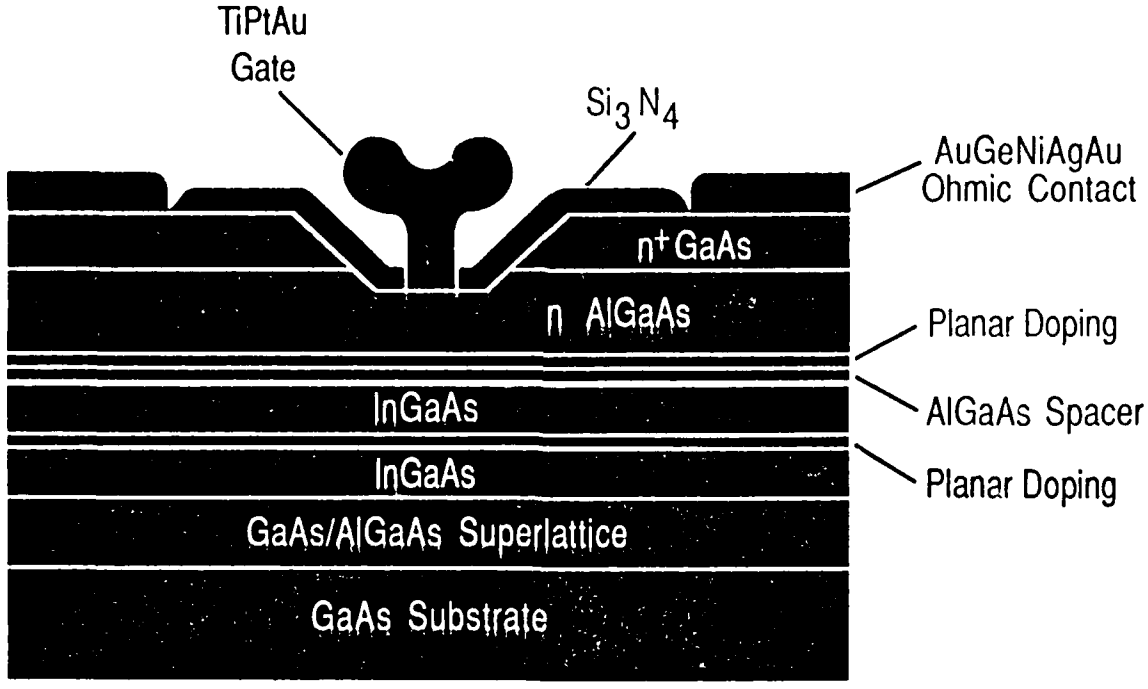


Double Heterojunction Pseudomorphic HEMT

GE Aerospace



Doped Channel Pseudomorphic HFET



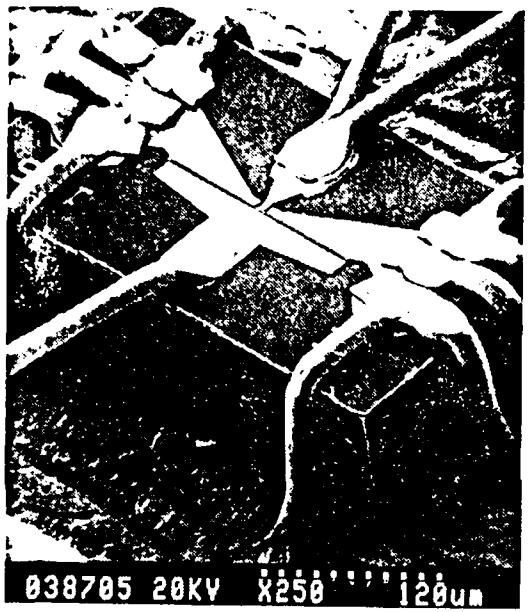
Comparison of Pseudomorphic Device Structures

GE Aerospace

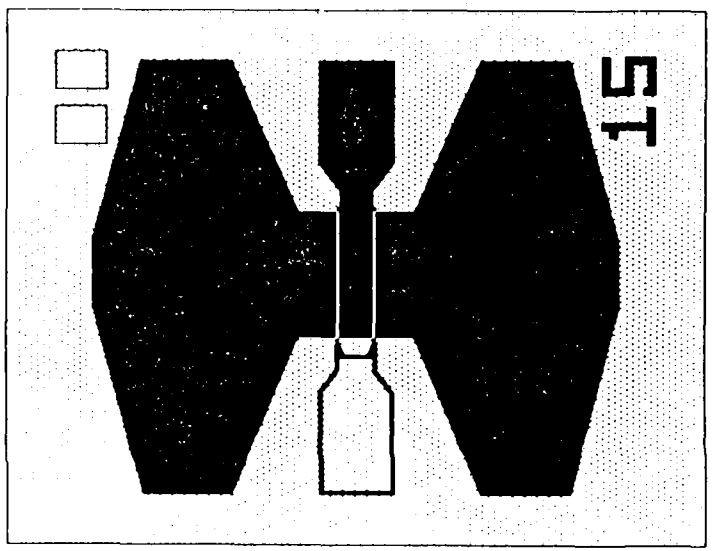
		DOUBLE HETEROJUNCTION	DOPED CHANNEL
	μ_{77K} (cm^2/V-sec)	20,000	5,000
	$n_{s\ 77K}$ (cm^{-2})	3.6×10^{12}	3.6×10^{12}
	g_m (mS/mm)	600	600
$L_g = 0.25\mu m$	I_f (mA/mm)	600	600
	V_{gdb} (V)	8	8
$L_g = 0.1 - 0.15\mu m$	g_m (mS/mm)	700	700
	I_f (mA/mm)	750	720
	V_{gdb} (V)	5	5

Effect of Source Inductance

GE Aerospace



0.25 x 150μm HEMT



0.25 x 150μm HEMT with
Via-Hole Source Grounding

35GHz Performance

VIAS	V_{ds} (V)	I_{ds} (mA)	OUTPUT POWER (mW)	POWER DENSITY (W/mm)	POWER-ADDED EFFICIENCY (%)	GAIN (dB)
No	4.3	37	93	0.62	43	6.0
Yes	4.3	38	92	0.61	48	7.9

- 0.25 x 150μm Double Heterojunction Pseudomorphic HEMT
- Via Holes Increase Gain at Maximum Efficiency by ~2dB

35 and 44 GHz Pseudomorphic Device Power Results

GE Aerospace

– 0.25 x 150μm Double Heterojunction HEMTs

FREQUENCY (GHz)	SOURCE VIAS	POWER DENSITY (W/mm)	POWER-ADDED EFFICIENCY (%)	GAIN (dB)
35	YES	0.44	50*	8.6
	NO	0.97*	35	5.0
44	YES	0.63	48*	6.6
	NO	1.01*	32	4.1

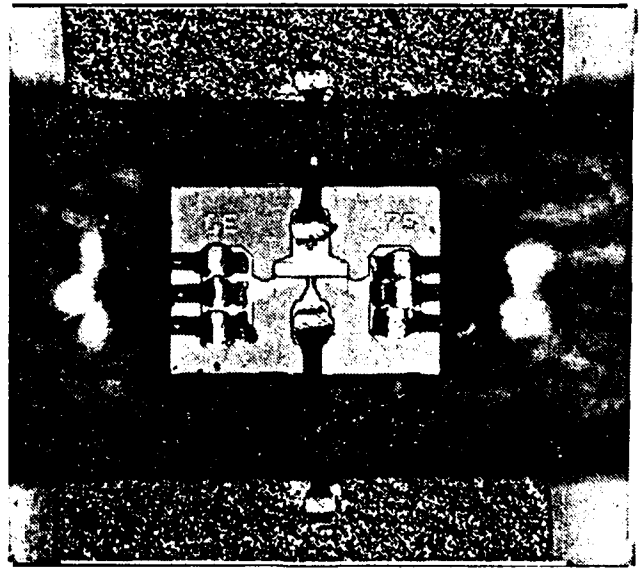
*maximum

~ 1 W/mm Power Density and ~50% Power-Added Efficiency Demonstrated at 35 and 44 GHz

0.25μm Doped Channel Pseudomorphic HFET – 60 GHz Power Performance

GE Aerospace

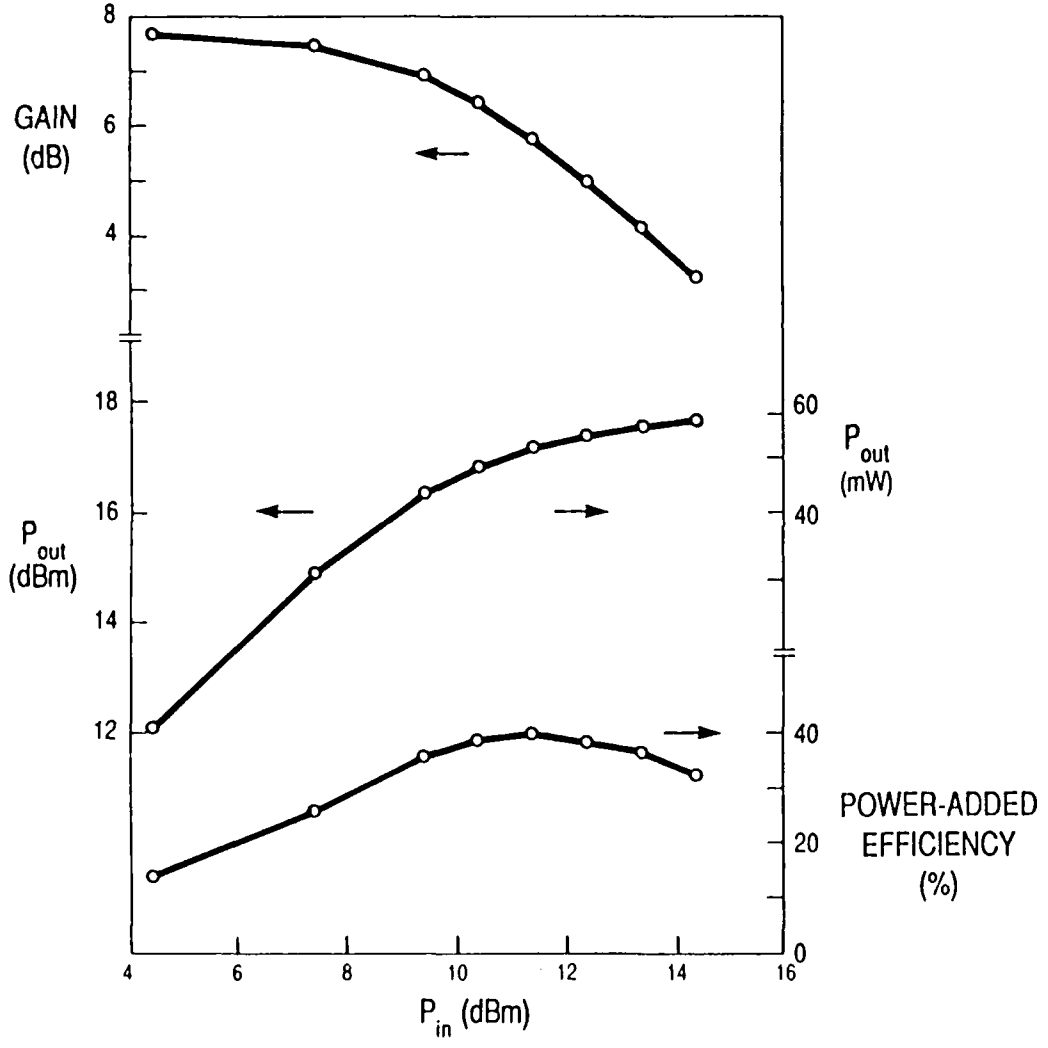
OUTPUT POWER (mW)	POWER DENSITY (W/mm)	POWER-ADDED EFFICIENCY (%)	GAIN (dB)
52	0.69	40	5.8
68	0.91	38	6.0
75	1.00	36	4.4



75μm Gate Width Device

60 GHz Power Data – Doped Channel Pseudomorphic HFET

GE Aerospace



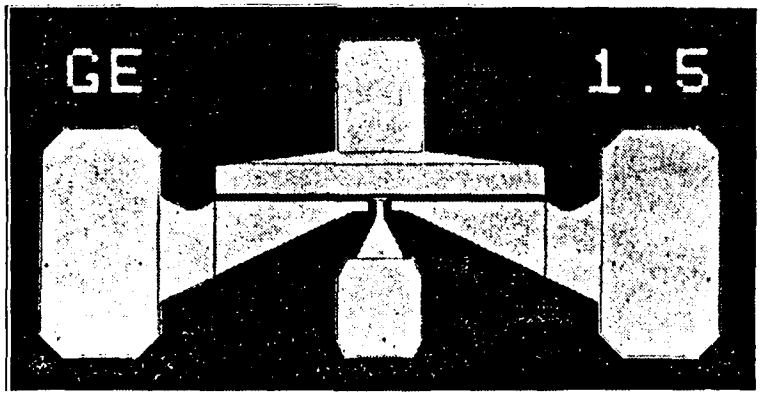
- 0.25 x 75μm Device

GAIN (dB)	POWER (mW)	EFFICIENCY (%)
5.8	52	40
6.4	48	39
7.0	43	36
7.5	31	26

0.15μm Double Heterojunction Pseudomorphic HEMT – 60 GHz Power Performance

GE Aerospace

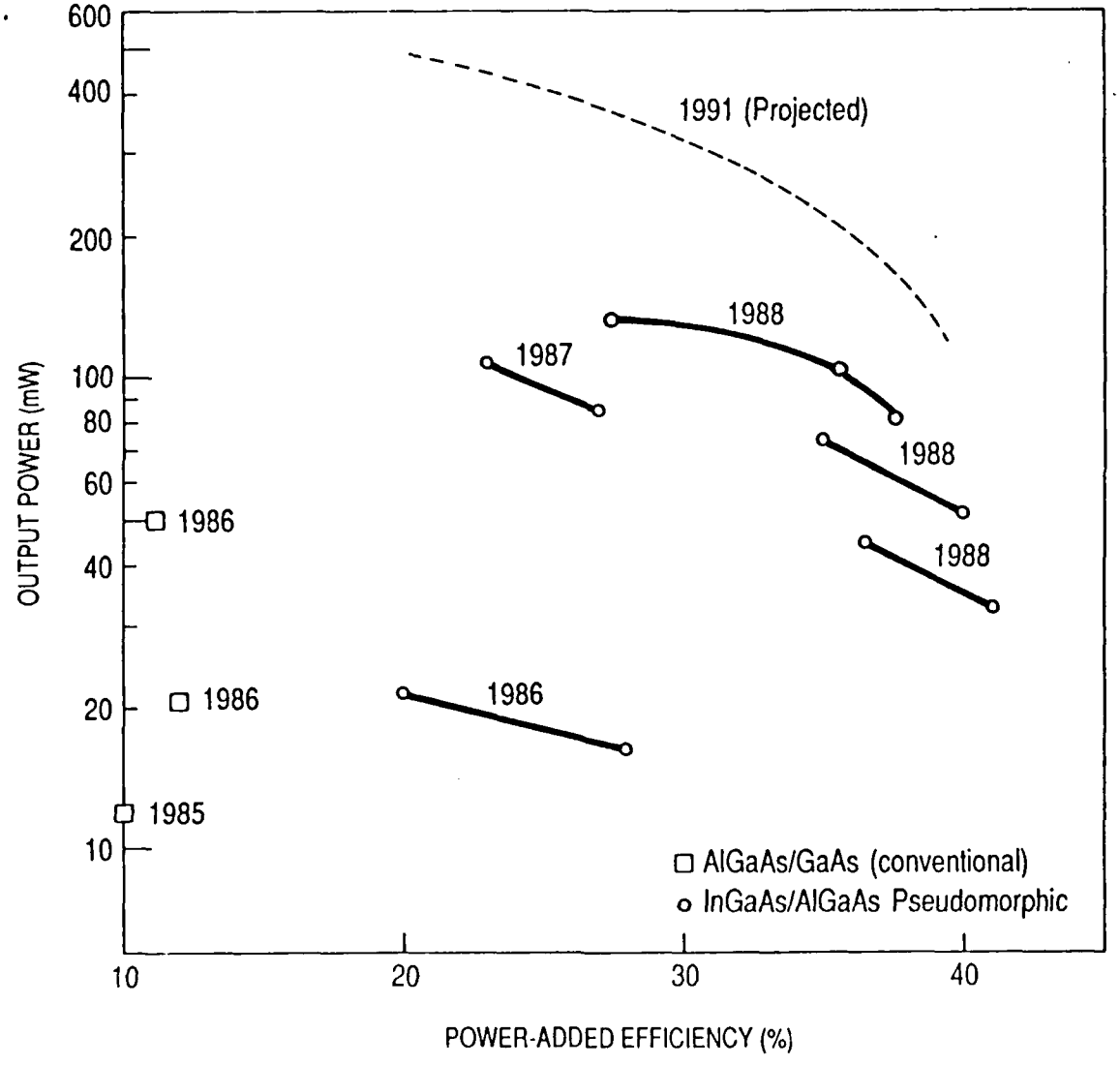
GATE WIDTH (μm)	OUTPUT POWER (mW)	POWER DENSITY (W/mm)	POWER-ADDED EFFICIENCY (%)	GAIN (dB)
50	33	0.66	41	5.8
	42	0.84	37	5.9
	47	0.94	30	3.3
150	82	0.55	38	4.7
	125	0.83	32	4.5
	139	0.93	28	3.0



150μm Gate Width HEMT

60 GHz Performance of GE Power HEMTs

GE Aerospace



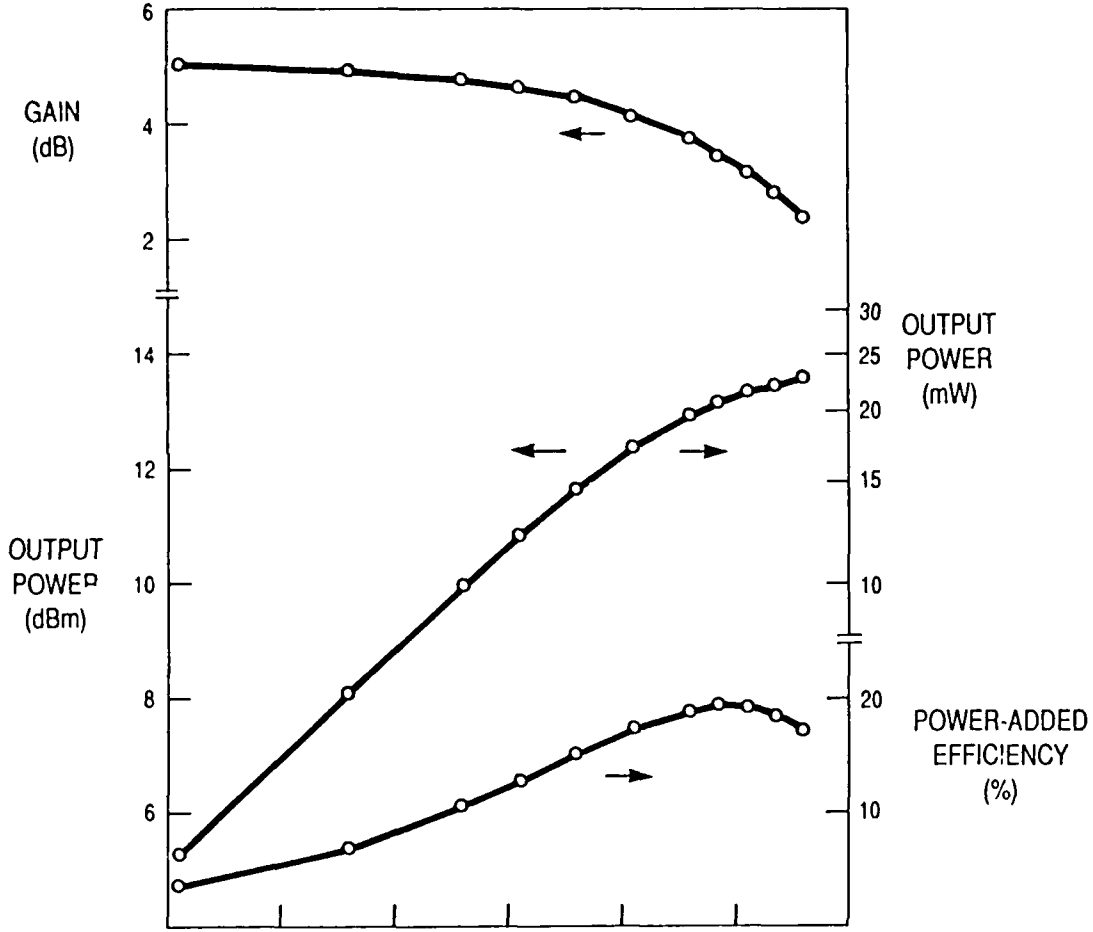
94 GHz Pseudomorphic HEMT Power Performance

- 0.15 x 50μm Gate Dimensions
- Double Heterojunction Pseudomorphic HEMT

OUTPUT POWER (mW)	POWER DENSITY (W/mm)	POWER-ADDED EFFICENCY (%)	GAIN (dB)
18	0.36	23	3.3
22	0.43	19	3.2

94 GHz Power Data – 0.15μm Pseudomorphic HEMT

GE Aerospace



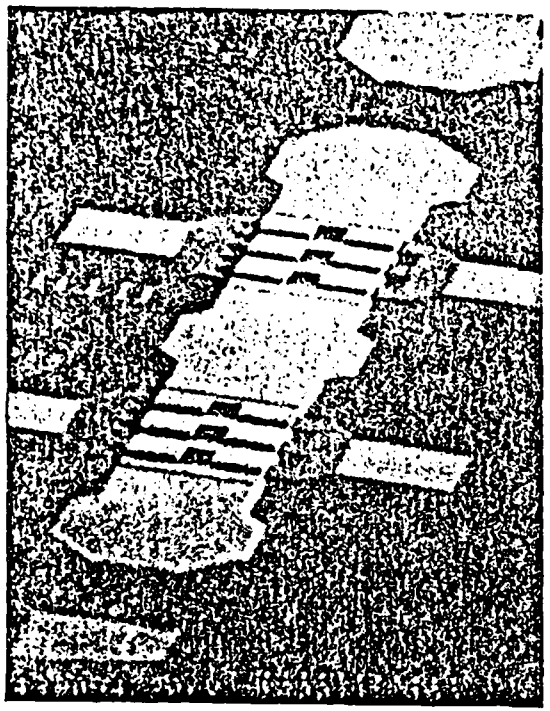
GAIN (dB)	POWER (mW)	EFFICIENCY (%)
3.2	22	19
3.7	20	19
4.2	17	18
4.5	15	15
4.8	10	11

Editorial Comment/Observations

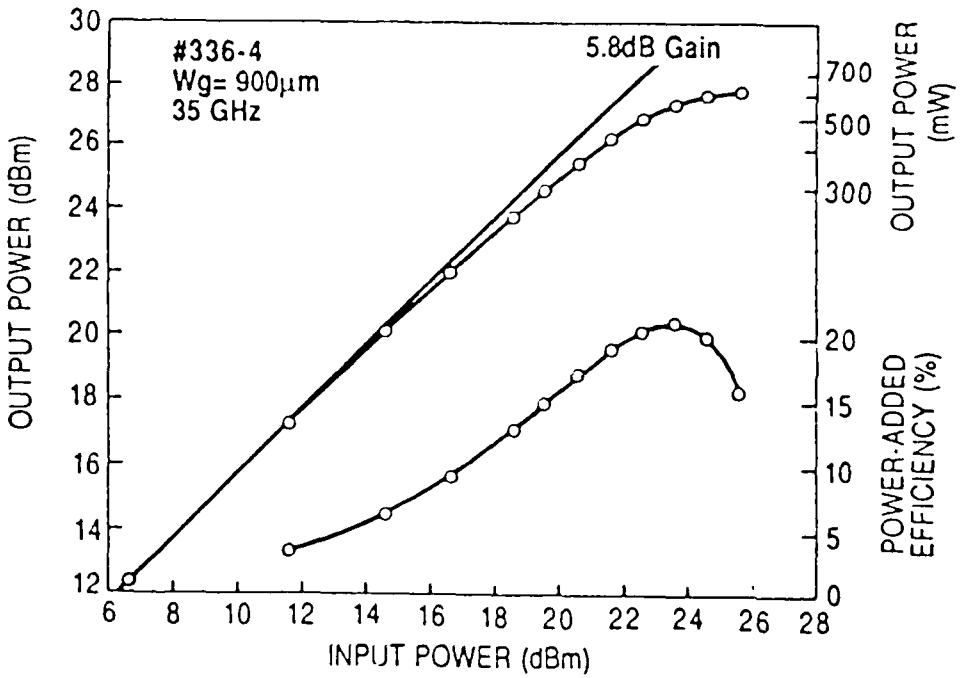
- **Not Valid to Compare Power Density for Different Device Types**
- **Universal Figures of Merit for Power Device are Output Power and Efficiency**
- **Compact Size is not an Advantage for Power Device – High Dissipated Power/Area → High Junction Temperature → Poor Reliability/RF Performance Degradation**
- **Power Density of HEMTs at 60 GHz is High Enough: 1 W/mm**
  - For High Efficiency/High Reliability, GaAs FETs Normally Operated at 0.3-0.5 W/mm
  - Higher Power Density Only Acceptable With Improved Thermal Resistance – Geometry, Substrate Thickness, Substrate Thermal Conductivity (InP)
- **Power HEMT Performance Degrades with Increasing Gate Width**
  - Source Inductance
  - Gate Resistance/Gate Line Attenuation
- **Need to Increase Output Power by Increasing Gate Width Without Sacrificing Too Much Gain and Efficiency**
  - Interdigitated Geometries
  - Low Resistance T-Gates
  - Via Holes

High Power Pseudomorphic HEMT

GE Aerospace Laboratories

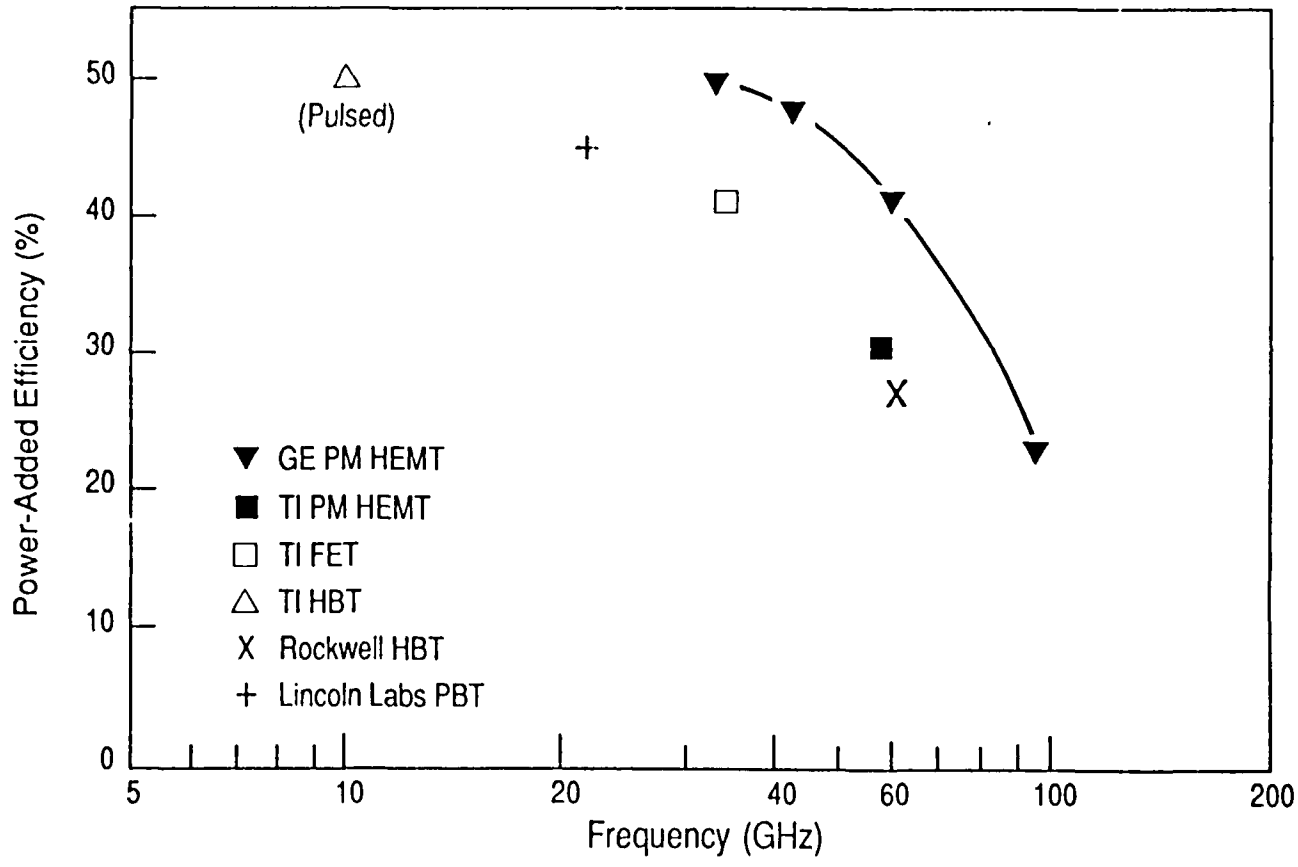


0.25μm Gate Length
900μm Gate Width
2 Cells

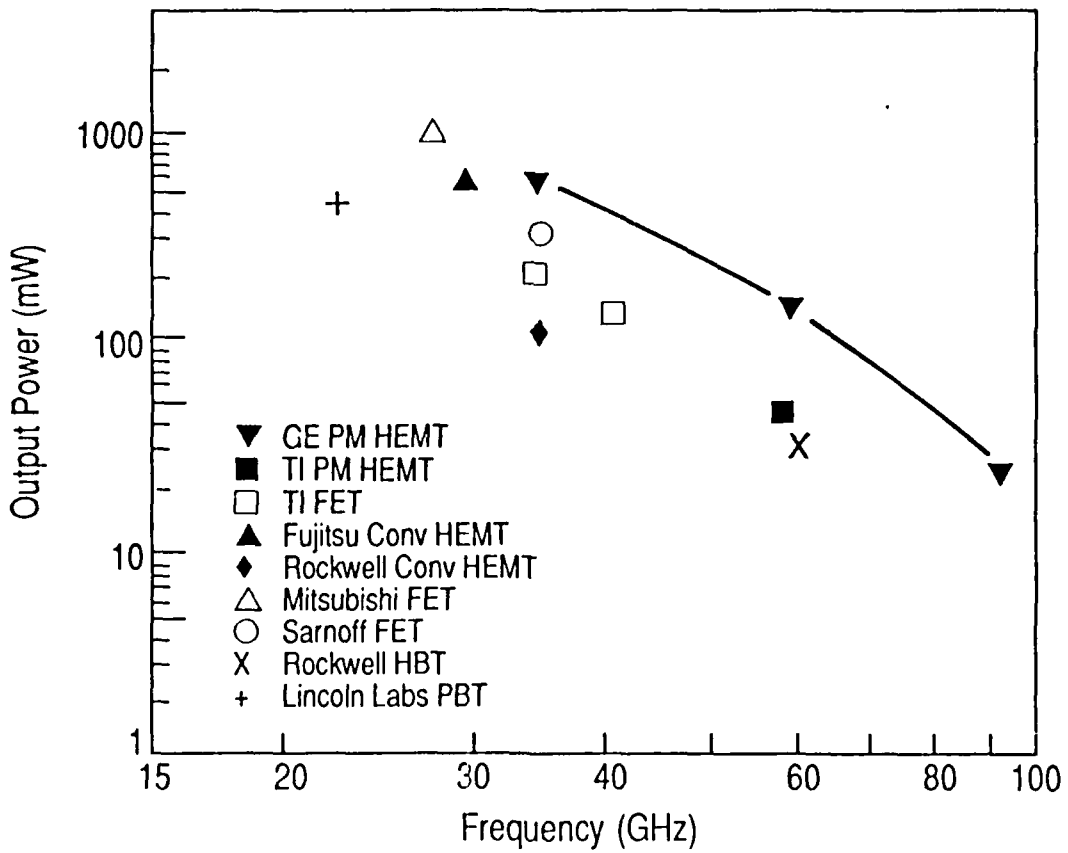


35GHz: 550mW Output Power With 3.8dB Gain, 21% Power-Added Efficiency

State-of-the-Art: Efficiency

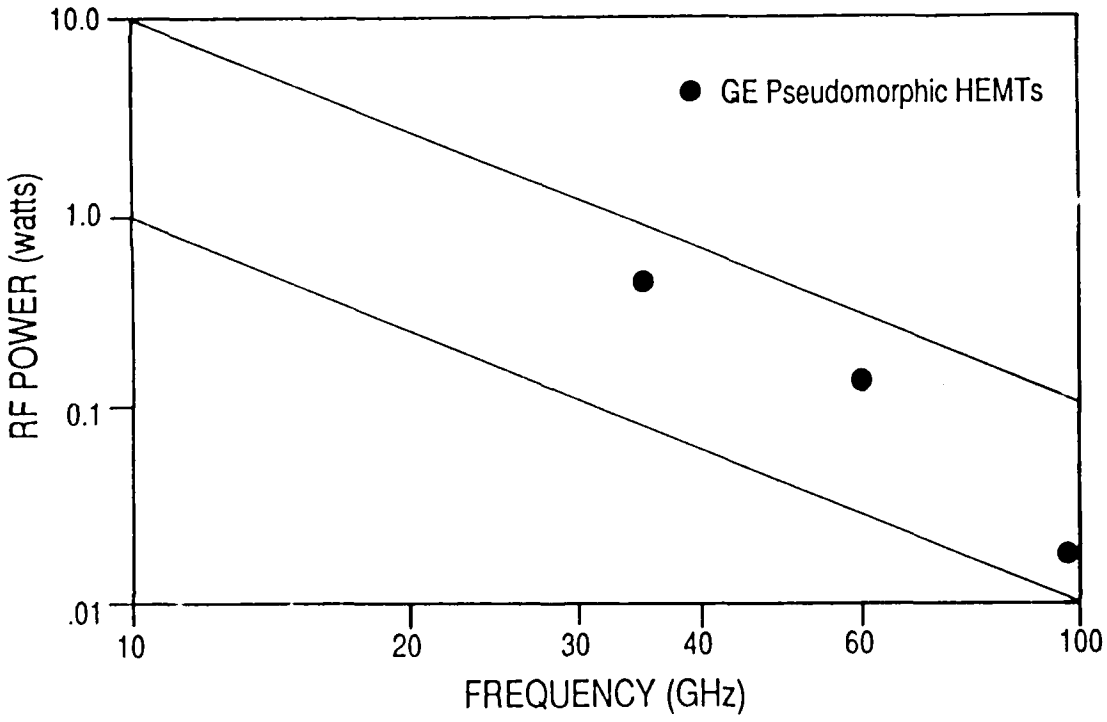


State-of-the-Art: Output Power



Typical Radiated Power/Element Requirements for Solid State Arrays

GE Aerospace



OUTPUT POWER OF CURRENT TRANSISTORS ADEQUATE FOR SOME MMW PHASED ARRAYS

0.15μm Double Heterojunction Pseudomorphic HEMT

GE Aerospace

Excellent Power Performance

60 GHz: 41% Maximum Efficiency with 5.8 dB Gain, 0.66 W/mm Power Density

Excellent Noise Performance

18 GHz: 0.6dB NF with 14.5 dB Ga

60 GHz (Projected): 1.7 dB NF with 7 dB Ga

Same Device Structure Suitable for Both Low Noise and Power Amplification

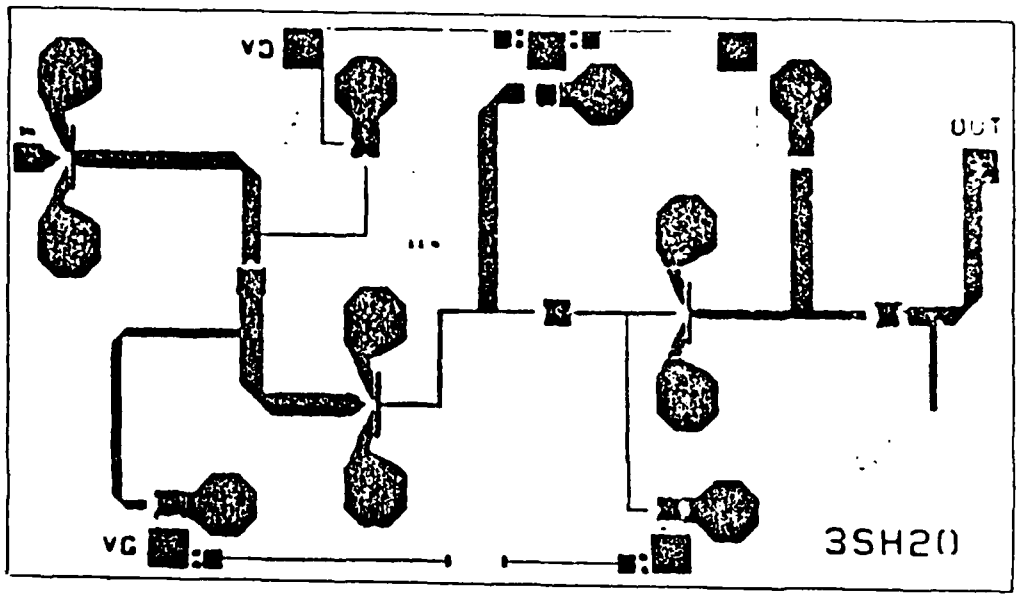
- Possible to Integrate LNA and Power Amplifier on Same GaAs Chip (Single-Chip T/R Module)

OR

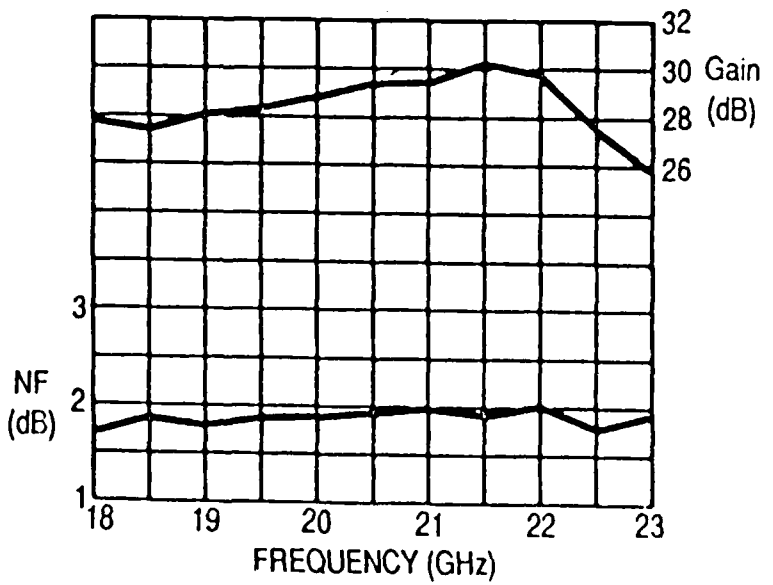
- Possible to Develop Generic Amplifier MMIC that can Serve as LNA or Power Amplifier

20 GHz 3-Stage HEMT MMIC LNA

GE Aerospace Laboratories



- 0.25μM HEMTs
- Input Match Off-Chip for Lowest Noise Figure
- 20.2-21.2 GHz Design Band

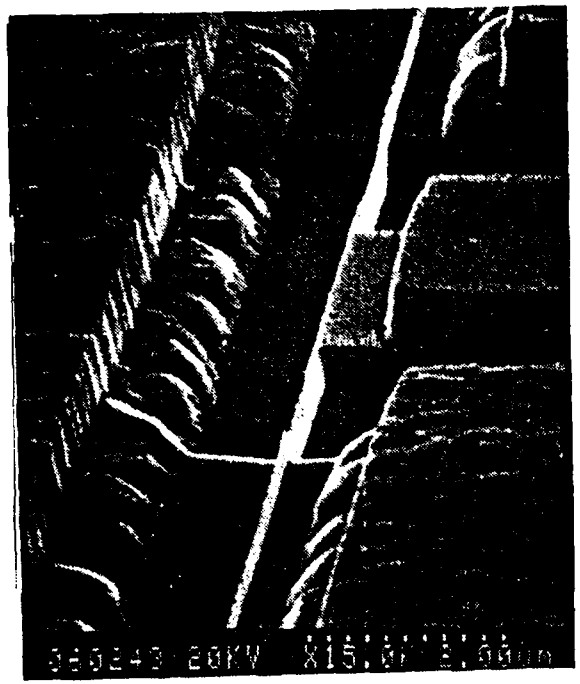


Performance: 20.2-21.2 GHz

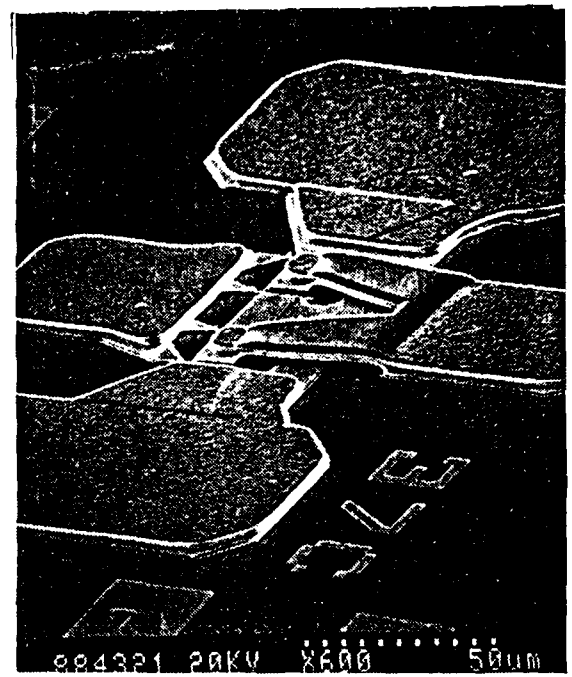
- Gain = 29.4 ± 0.4 dB
- NF ≤ 2.0 dB

0.1μm Pseudomorphic HEMT

GE Aerospace



Channel Region



50μm Gate Width Device Geometry

- Planar-Doped Pseudomorphic Structure for High Aspect Ratio
- 4-Finger Air-Bridged Geometry to Reduce R_g
- DC g_m = 930 mS/mm
- Excellent Noise Figure, High Gain Despite High R_g:

FREQUENCY (GHz)	NOISE FIGURE (dB)	GAIN (dB)
60	1.9	9.2
94	3.0	5.1

0.25μm InAlAs/InGaAs/InP HEMT

Noise

FREQUENCY (GHz)	NOISE FIGURE (dB)	GAIN (dB)
18	0.5	15.2
60	1.2	8.5
94	2.1	6.4

Power

- 150μm Gate Width HEMT Tested at 35 GHz
- At V_{ds} = 3.6 V, Output Power = 66mW
  Power Density = 0.44 W/mm
  Power-Added Efficiency = 38%
  Gain = 6.5 dB

Gain

- Maximum Small-Signal Gain:

FREQUENCY (GHz)	GAIN (dB)
63	15.5
95	12.0

- Extrapolated f_{max} = 380 GHz

Summary

- **Potential Array Applications at 35, 44, 60 and 94 GHz Demand High Performance Devices and Circuits**
- **Current HEMTs Offer Useable Device Performance for Arrays up to 60 GHz**
  - V-Band Subarray Demonstration Contract Using Present 0.25μm HEMT Technology
- **HEMTs Exhibit Excellent Noise Performance to 94GHz (1-2 db NF @ 60 GHz, 2-3 dB NF @ 94 GHz)**
- **Significant Progress was made in 60 and 94 GHz Pseudomorphic Power HEMTs with Double Heterojunction and Doped Channel Devices:**

  60 GHz
  - Power Gain of 6-7 dB with 40% Efficiency, 0.6-0.7 W/mm Power Density for Small Devices (50, 75μm Gate Width)
  - Output Power of 125 mW with 32% Efficiency, 4.5 dB Gain.
    Gain, Efficiency of 150μm Device will be Improved with Vias
  - Power Density of 1 W/mm is High Enough
  - Output Power can be Increased to 0.5 Watt

  94 GHz
  - 22mW Output Power, 23% Peak Efficiency, ~3 dB Power Gain
  - Higher Gain, Power Desirable for Applications

- **Low Noise and Power Pseudomorphic HEMTs Easily Integrate into GaAs MMICs**
- **New Devices for Improved Performance – 0.1μm Pseudomorphic HEMT, InP-Based HEMT**

mm-Wave Phased-Array Antenna Concepts

Charles A. Liechti

Rockwell International, Science Center
Thousand Oaks, CA

MM-WAVE PHASED-ARRAY ANTENNA CONCEPTS

Charles A. Liechti

ROCKWELL INTERNATIONAL
SCIENCE CENTER

OUTLINE

1. TECHNICAL GOALS AND DESIGN PARAMETERS
2. ARRAY CONSTRUCTION
3. PRINTED MICROSTRIP MM-WAVE RADIATORS
4. PROPOSED SPACE-FED SUB-ARRAY DESIGN
5. GaAs IC BLOCK DIAGRAM
6. CONCLUSIONS

PHASED-ARRAY TRANSMIT ANTENNA

FOR TELECOMMUNICATION

TECHNICAL GOALS

TRANSMIT ARRAY:

*	FREQUENCY	60 GHz	94 GHz
*	BANDWIDTH	2 GHz	3 GHz
*	SCAN ANGLE	60°	60°
*	POLARIZATION	CIRCULAR	CIRCULAR
*	POINTING ACCURACY	1/10 BEAMWIDTH	1/10 BEAMWIDTH
*	GAIN X POWER (EIRP)	50 dBW	50 dBW
*	BEAM SWITCHING TIME	<20 ns	<20 ns

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PHASED-ARRAY TRANSMIT ANTENNA
FOR TELECOMMUNICATION

DESIGN PARAMETERS ANTENNA

*	FREQUENCY	60 GHz	94 GHz
*	ELEMENT SPACING	2.5 mm	1.6 mm
*	NUMBER OF MODULES	1000	1500
*	TOTAL RF POWER OUTPUT	200 W	150 W
*	ANTENNA GAIN	31 dB	32 dB
*	BEAM WIDTH	3.4°	2.7°

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PHASED-ARRAY TRANSMIT ANTENNA
FOR TELECOMMUNICATION

DESIGN PARAMETERS
GaAs CHIPS

*	FREQUENCY	60 GHz	94 GHz
*	CW OUTPUT POWER PER MODULE	200 mW	100 mW
*	MODULE GAIN	20 dB	16 dB
*	INCREMENTAL PHASE SHIFT	45°	45°
*	MODULE SIZE ON GaAs Chip	2.5 x 6.7 mm	1.6 x 4.3 mm
*	NUMBER OF MODULES PER SUB-ARRAY (For demonstration of concept)	4 x 4	4 x 4
*	NUMBER OF CHIPS PER SUB-ARRAY	4	4
*	CHIP SIZE	10 x 6 mm	6.4 x 6 mm
*	POWER DISSIPATION PER CHIP	5 W	5 W

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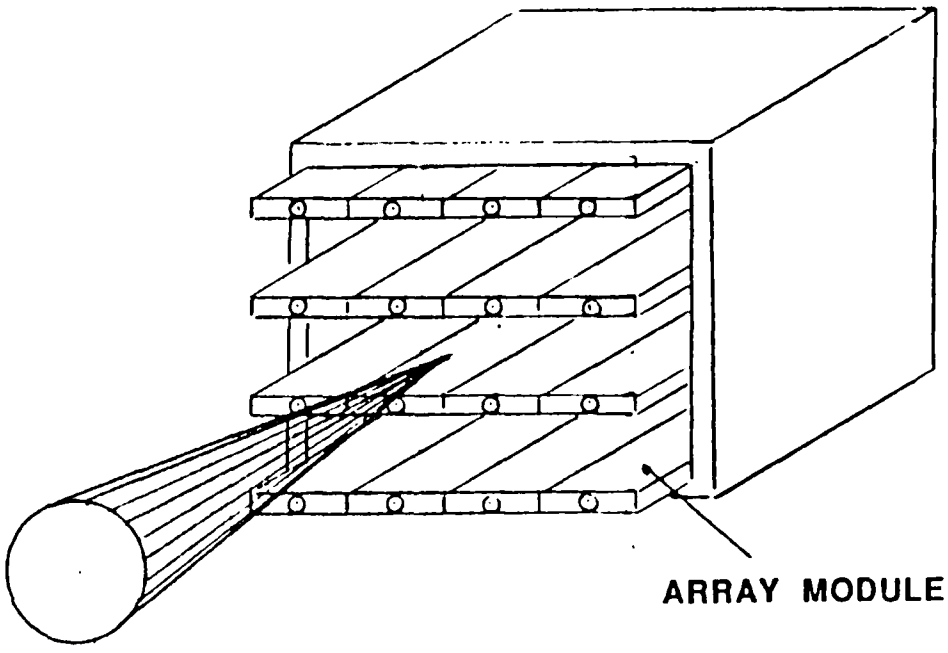
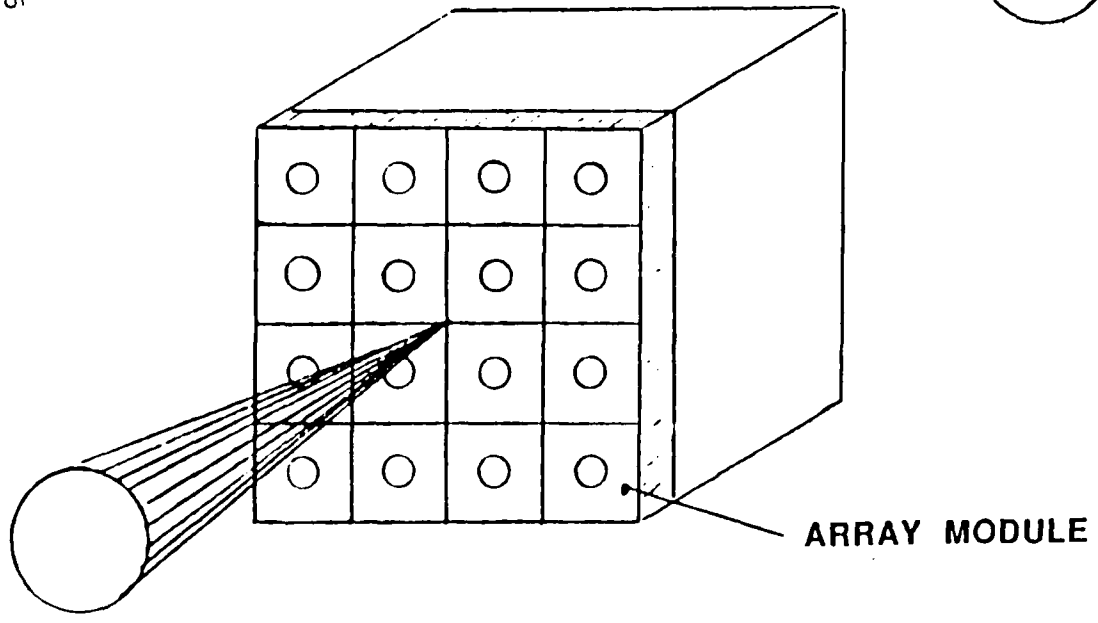
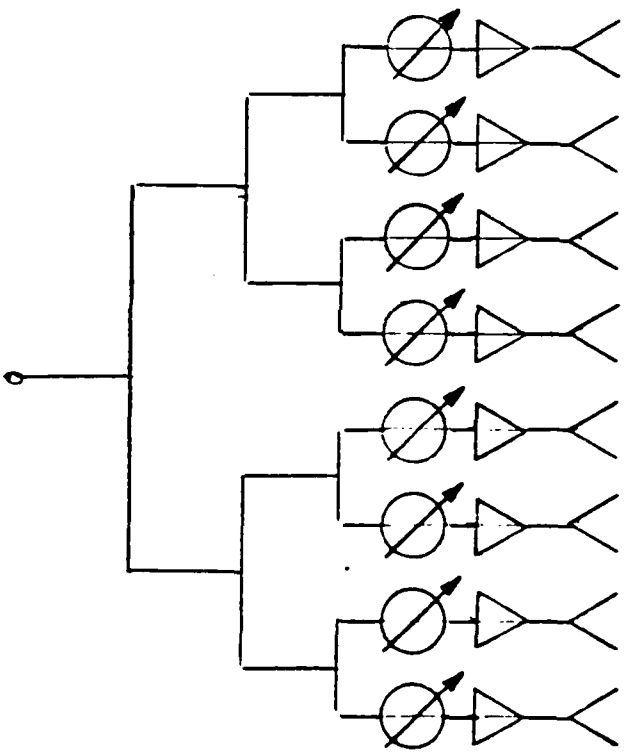
ARRAY CONSTRUCTION

ARRAY CONSTRUCTION ALTERNATIVES

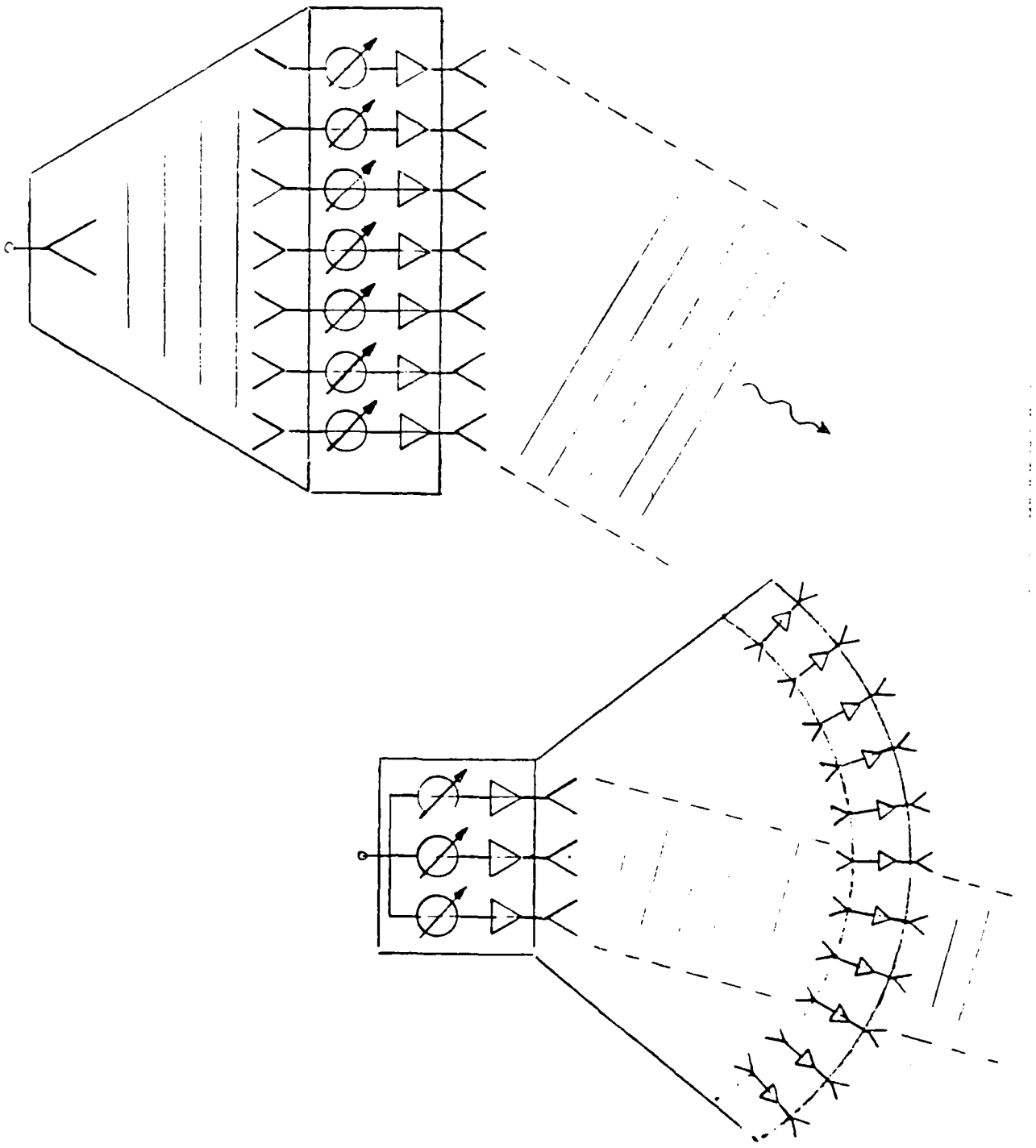




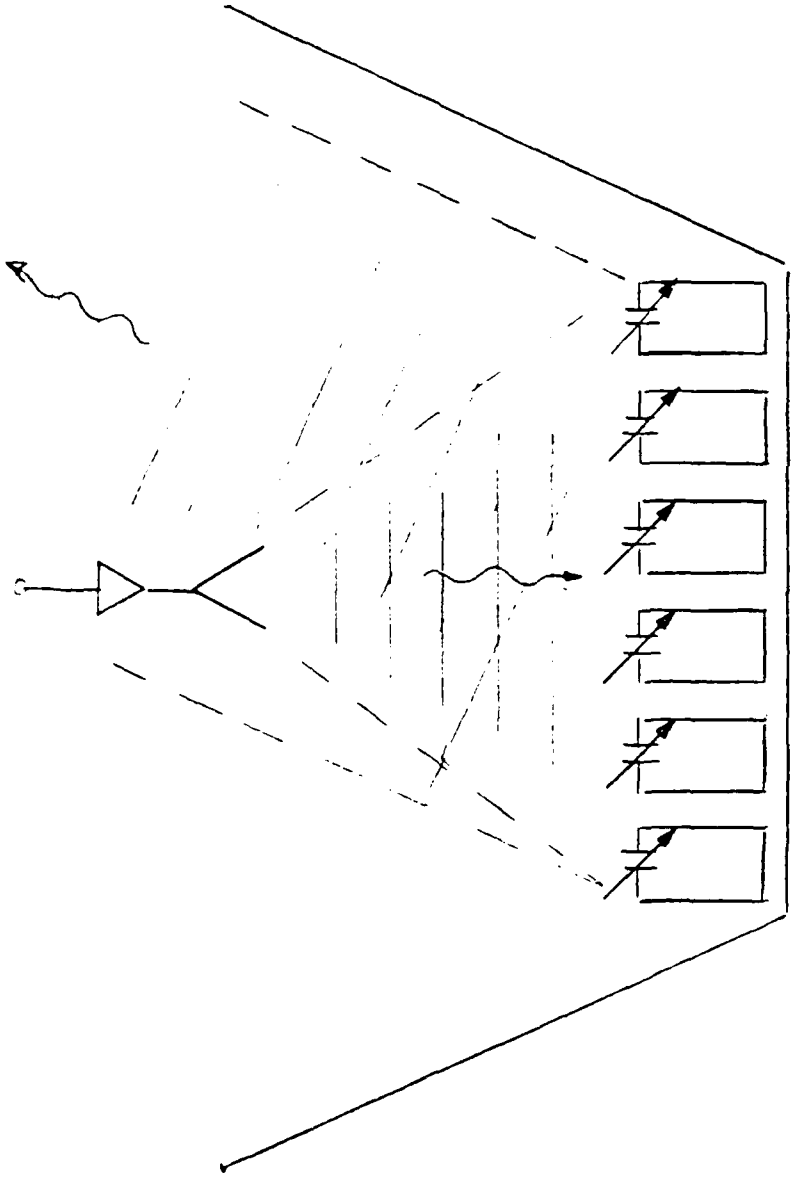
CORPORATE-FED ARRAY



SPACE-FED ARRAYS



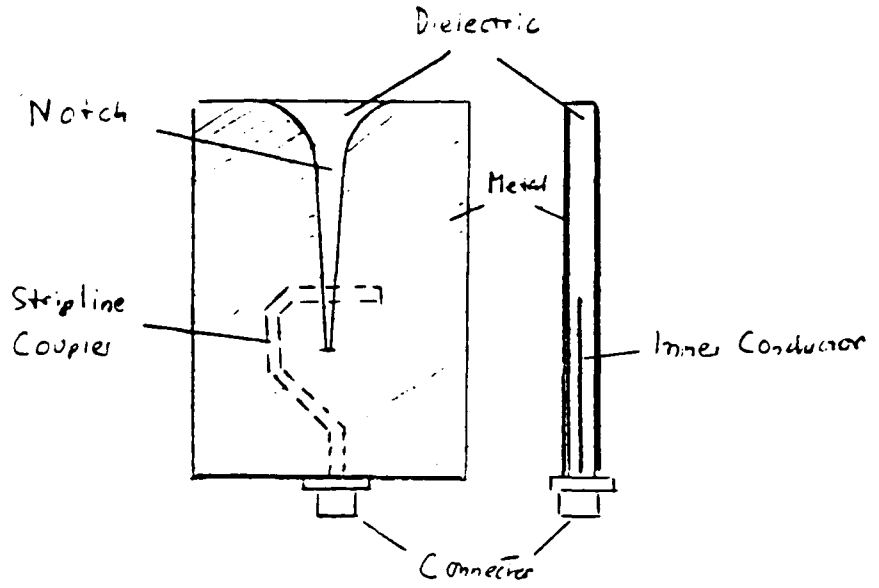
SPACE-FED REFLECTIVE ARRAYS



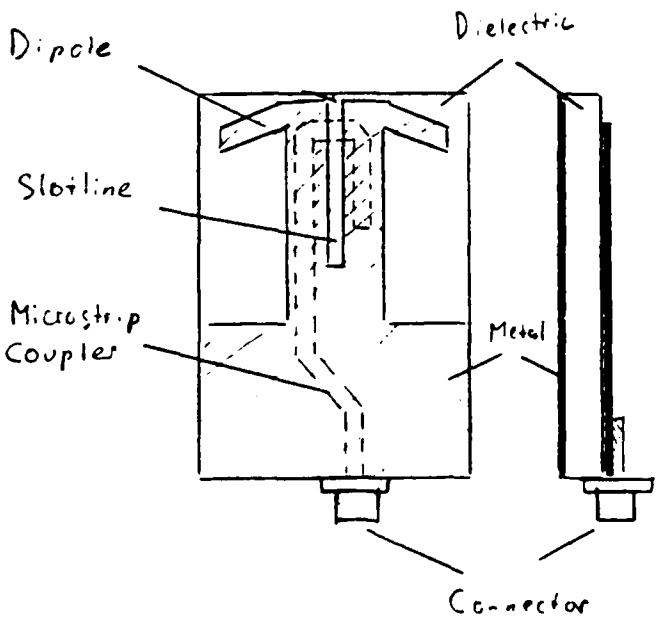
PRINTED MICROSTRIP

MM-WAVE RADIATORS

PRINTED MM-WAVE "END-FIRE" RADIATORS

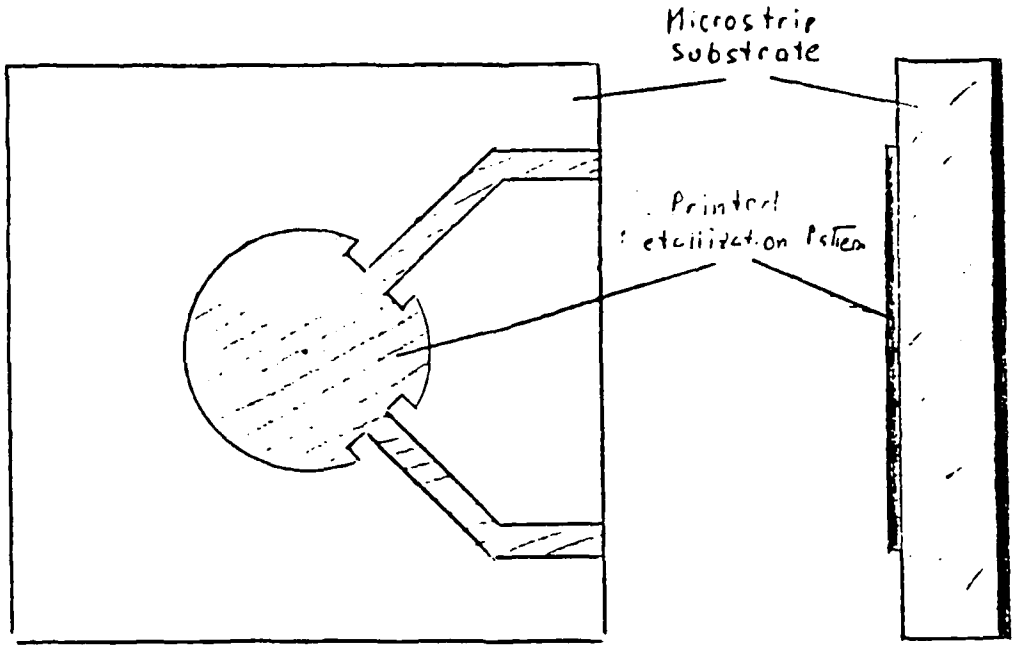


TAPERED-NOTCH RADIATING ELEMENT

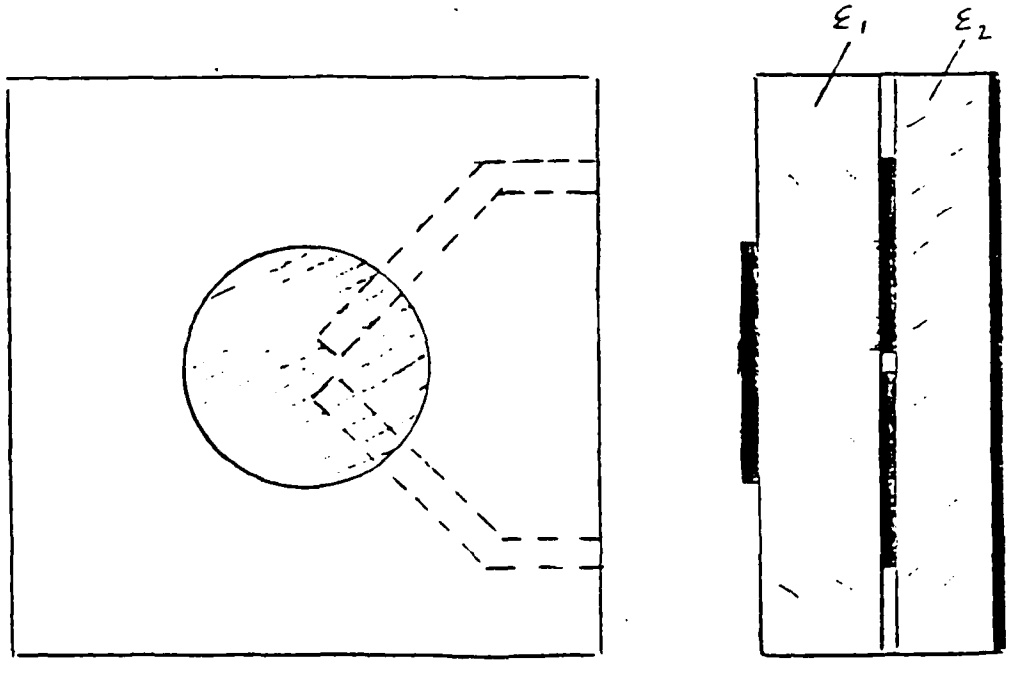


PRINTED DIPOLE RADIATING ELEMENT

PRINTED MM-WAVE "BROADSIDE-FIRED" RADIATORS

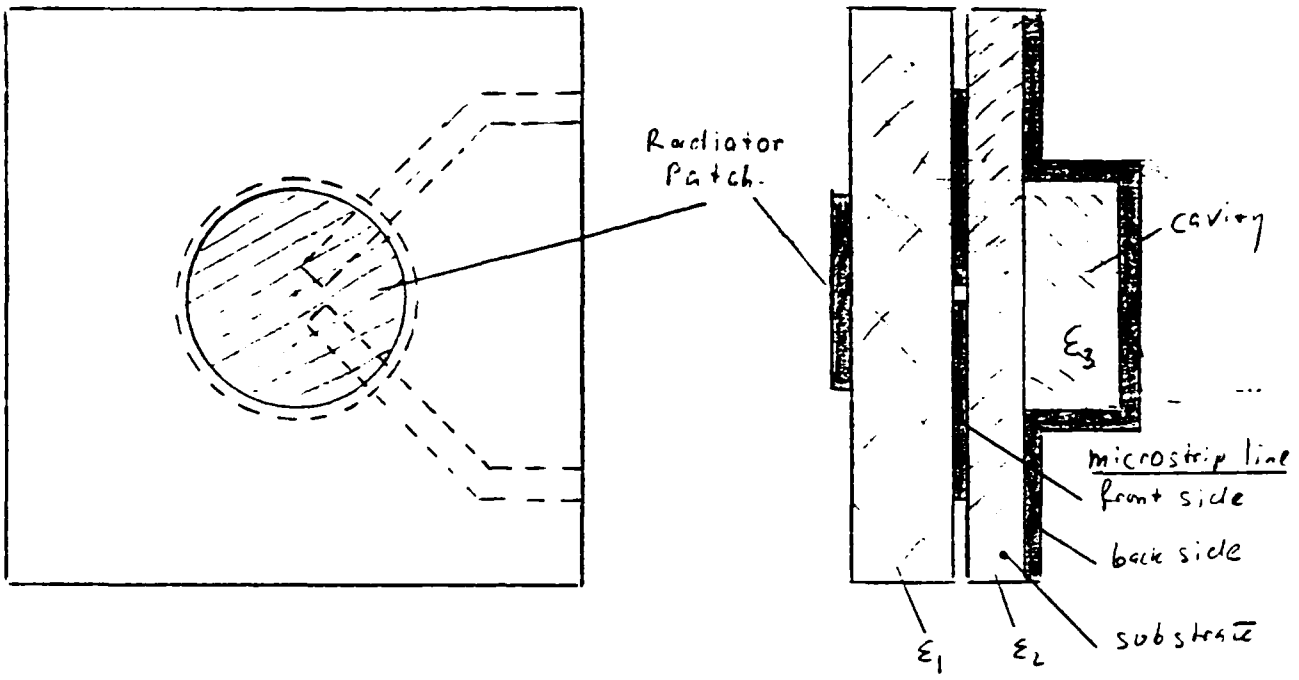


MICROSTRIP PATCH RADIATOR

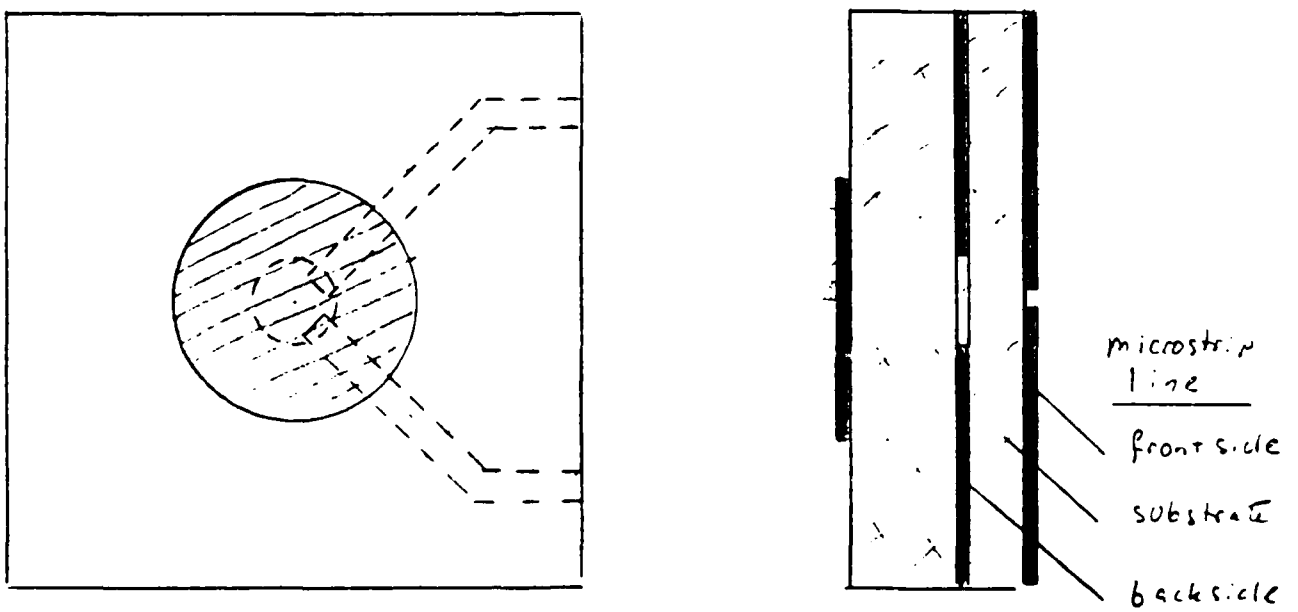


CAPACITIVELY-COUPLED MICROSTRIP RADIATOR

PRINTED MM-WAVE "BROADSIDE-FIRED" RADIATORS



CAPACITIVELY-COUPLED MICROSTRIP RADIATOR, CAVITY-BACKED



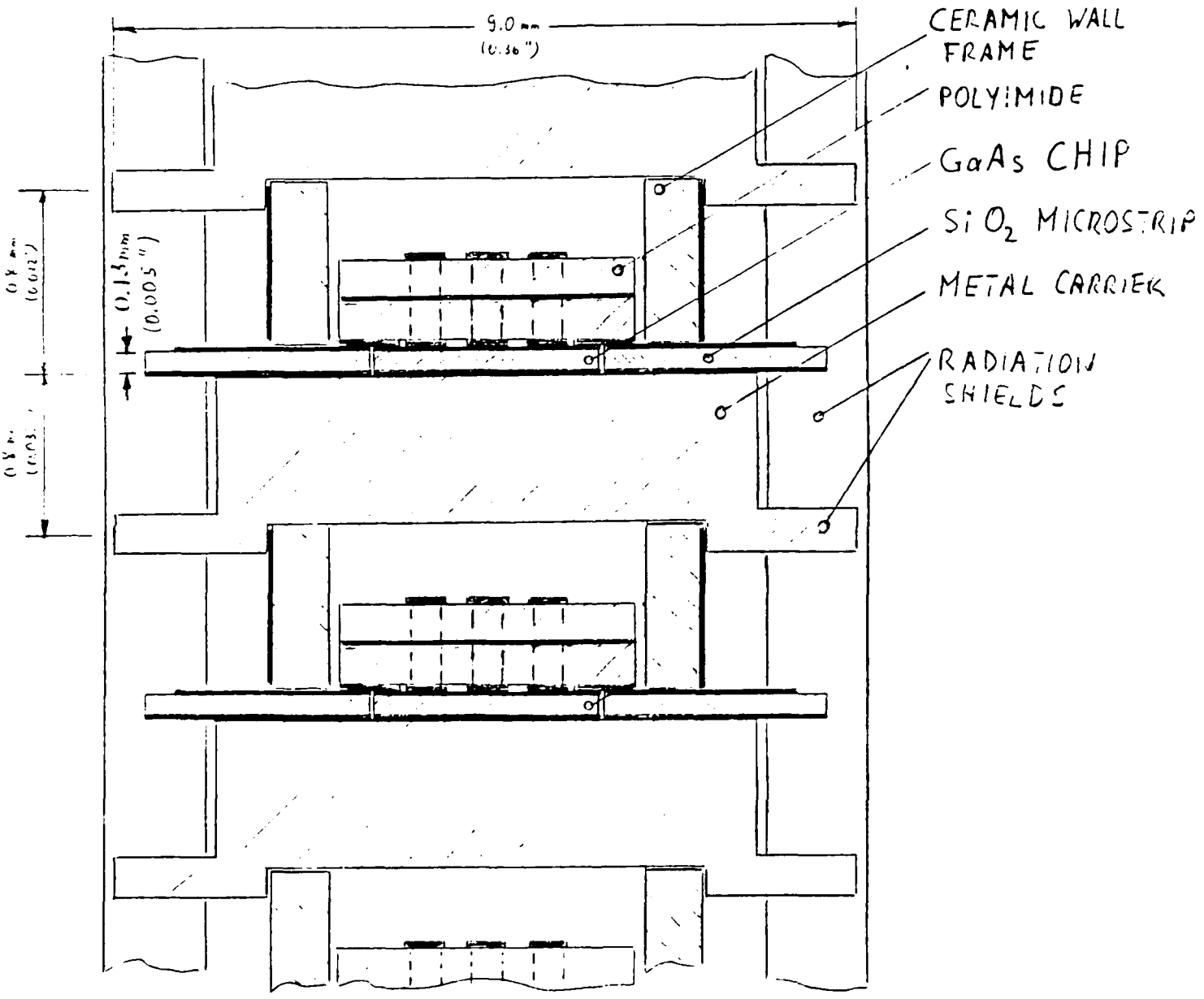
CAPACITIVELY-COUPLED MICROSTRIP RADIATOR, COUPLED THROUGH OPENING IN BACKSIDE METALLIZATION OF MICROSTRIP LINE

PROPOSED

SPACE-FED

SUBARRAY DESIGN

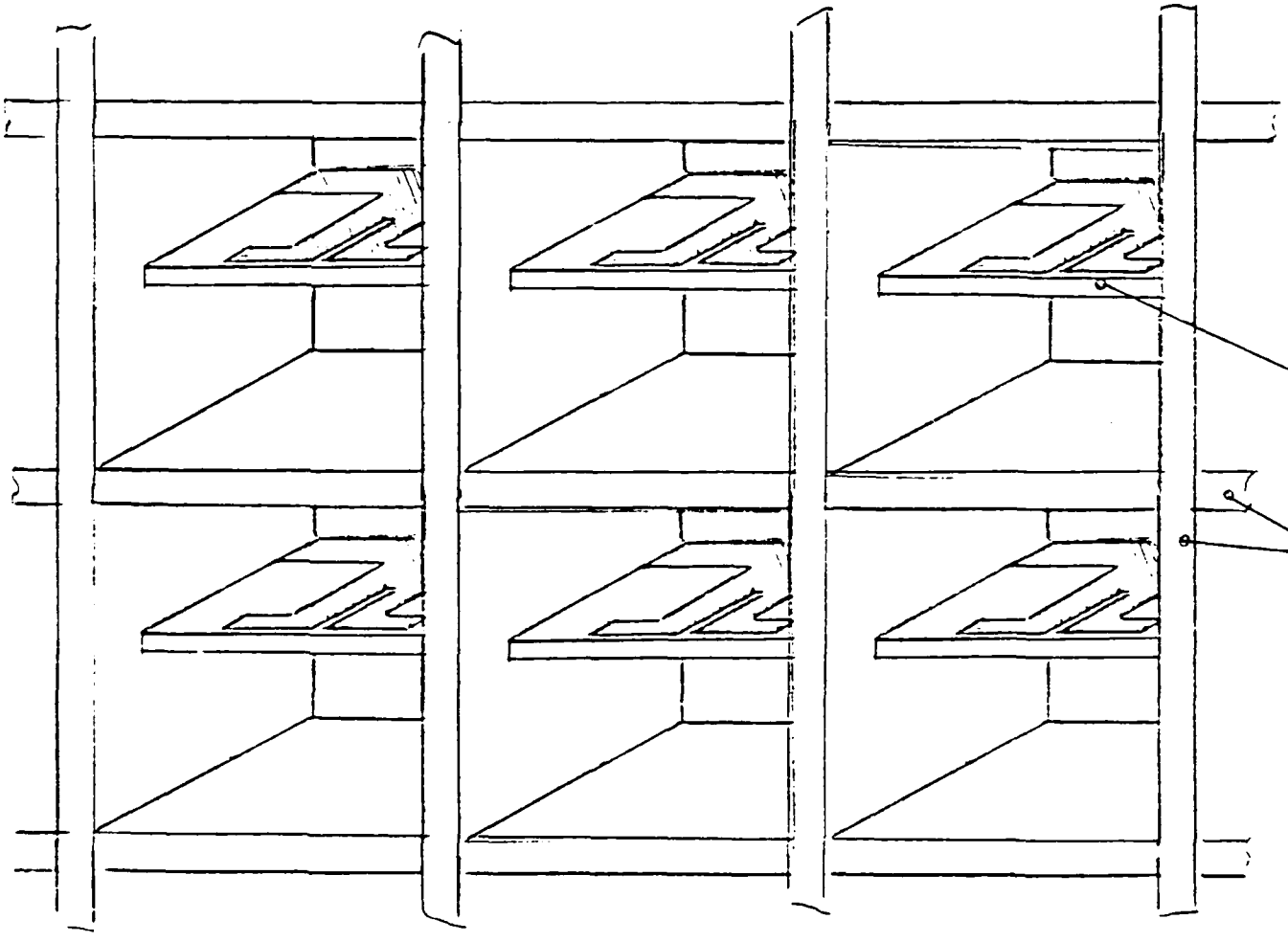
94 GHz PHASED ANTENNA SUBARRAY CROSS SECTION



C.A.L

APRIL 1988

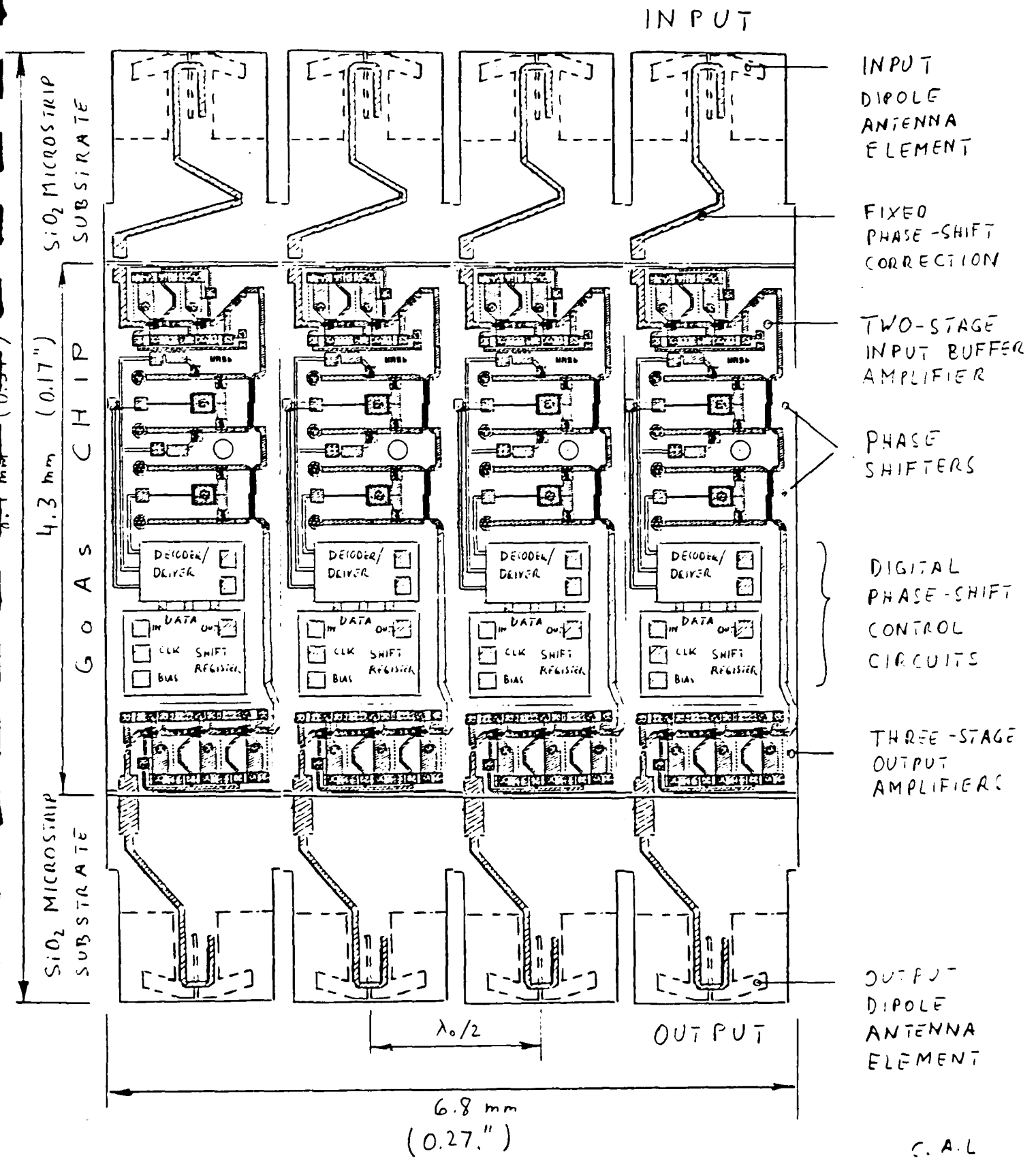
PHASED ANTENNA SUBARRAY VIEW OF ANTENNA FACE



CAL

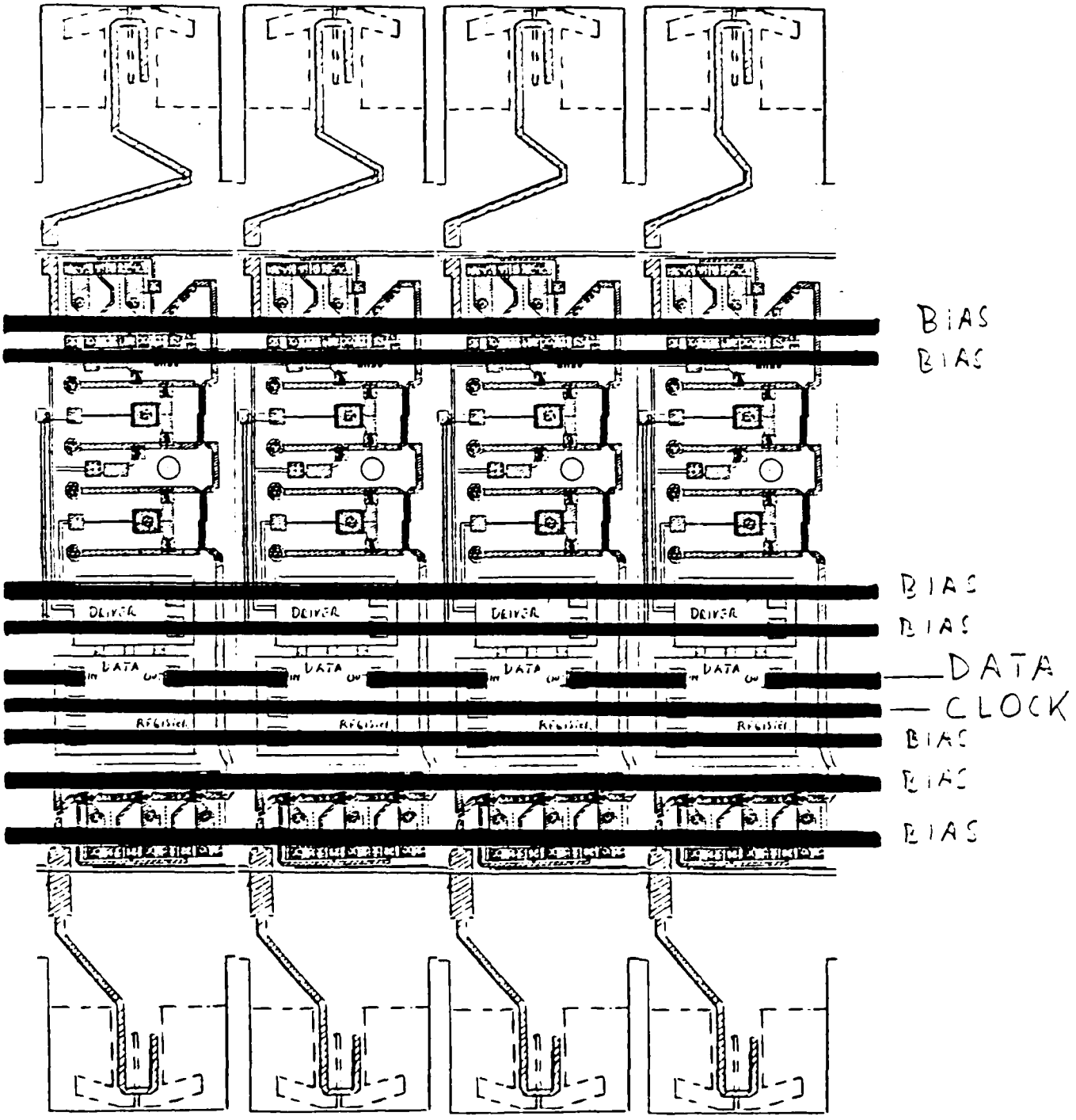
April 15th

94 GHz PHASED ANTENNA SUBARRAY



C.A.L
APRIL 1988

DC BIAS SUPPLY AND PHASE-SHIFT CONTROL INTERCONNECT LINES



C.A.L
APRIL 1988

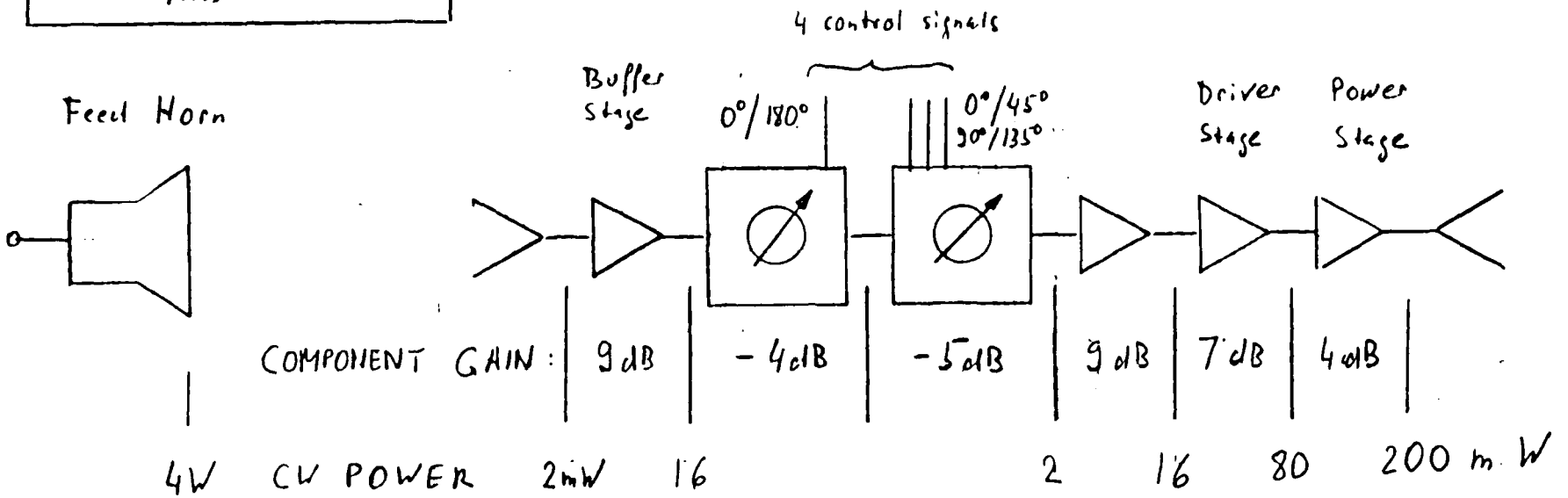
GaAs IC

BLOCK DIAGRAM

60 GHz PHASED-ARRAY TRANSMIT ANTENNA

TRANSMIT MODULE BLOCK DIAGRAM

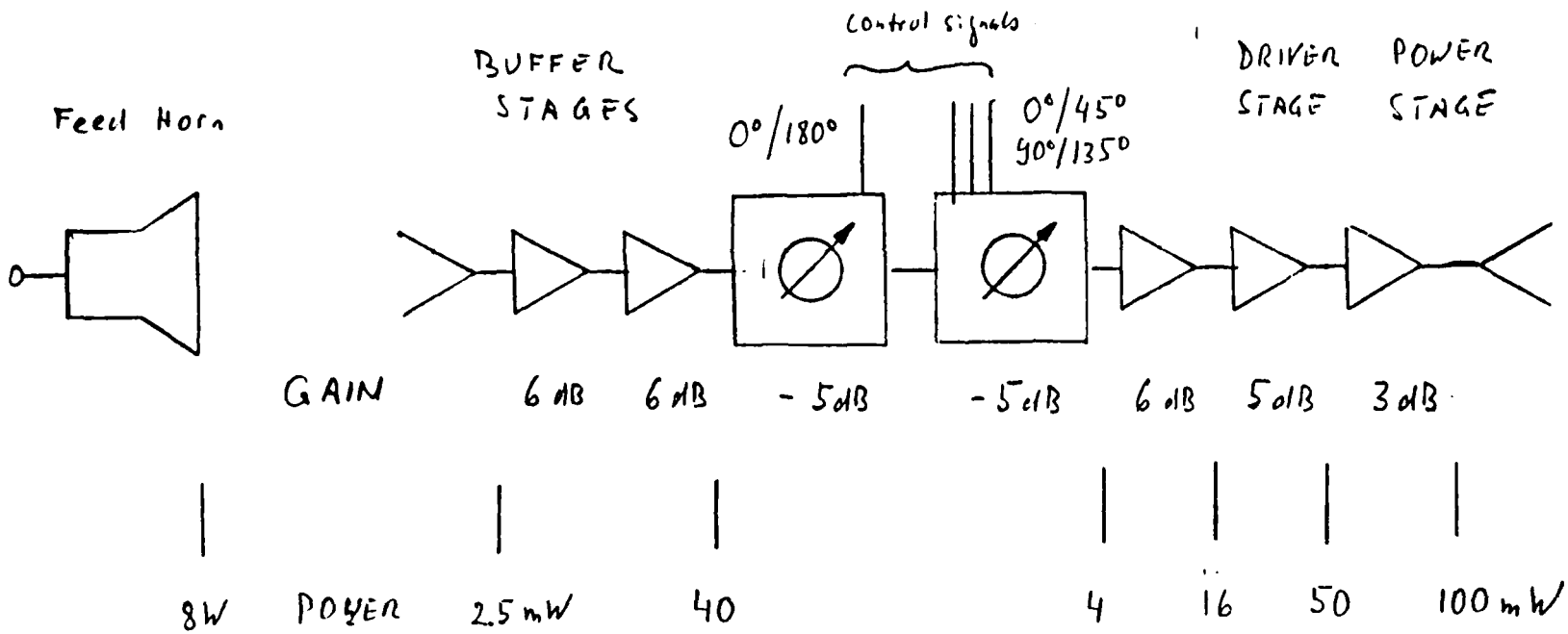
HBT f_{max} = 240 GHz



94 GHz PHASED-ARRAY TRANSMIT ANTENNA

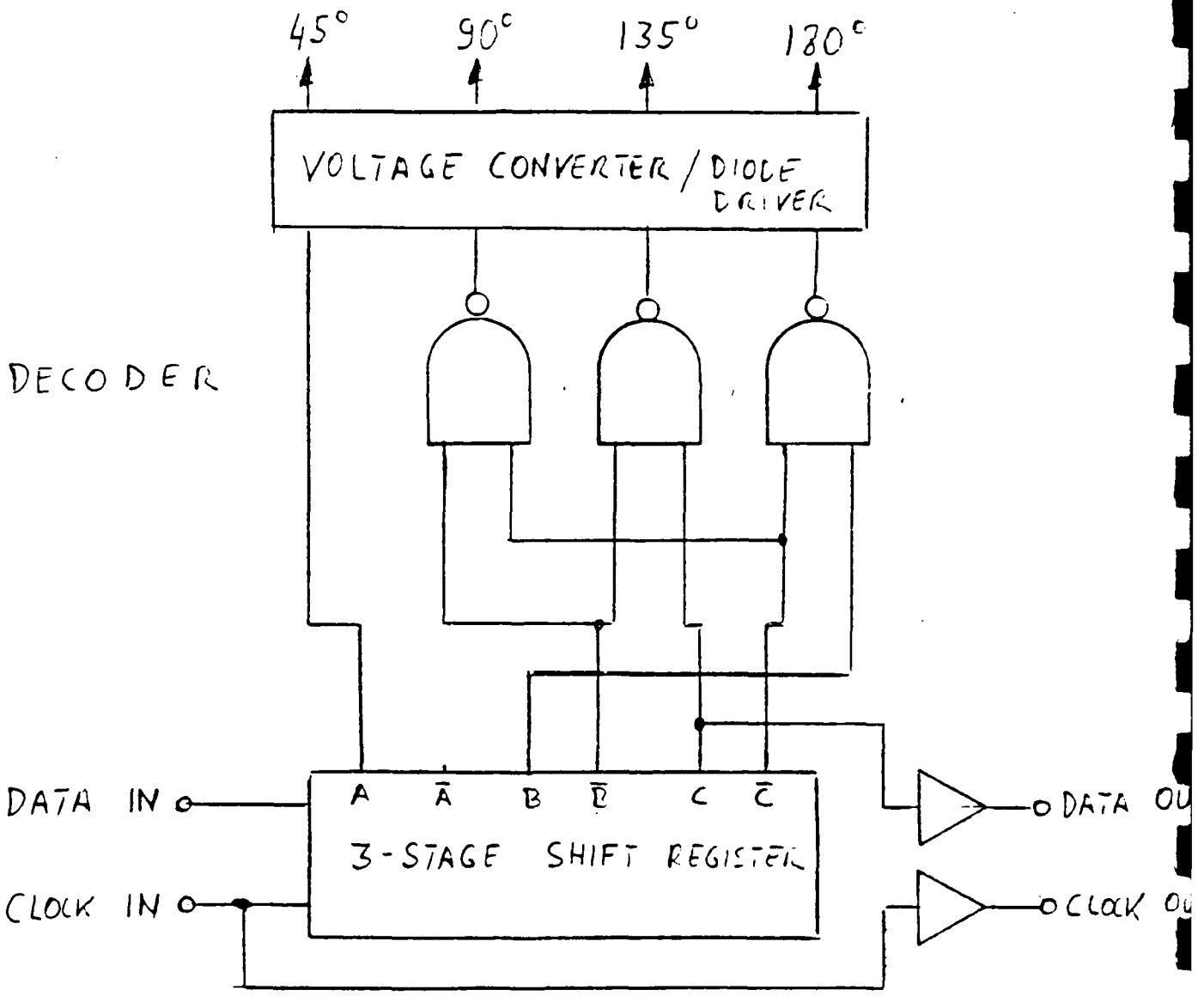
TRANSMIT MODULE BLOCK DIAGRAM

HBT f_{max} = 240 GHz

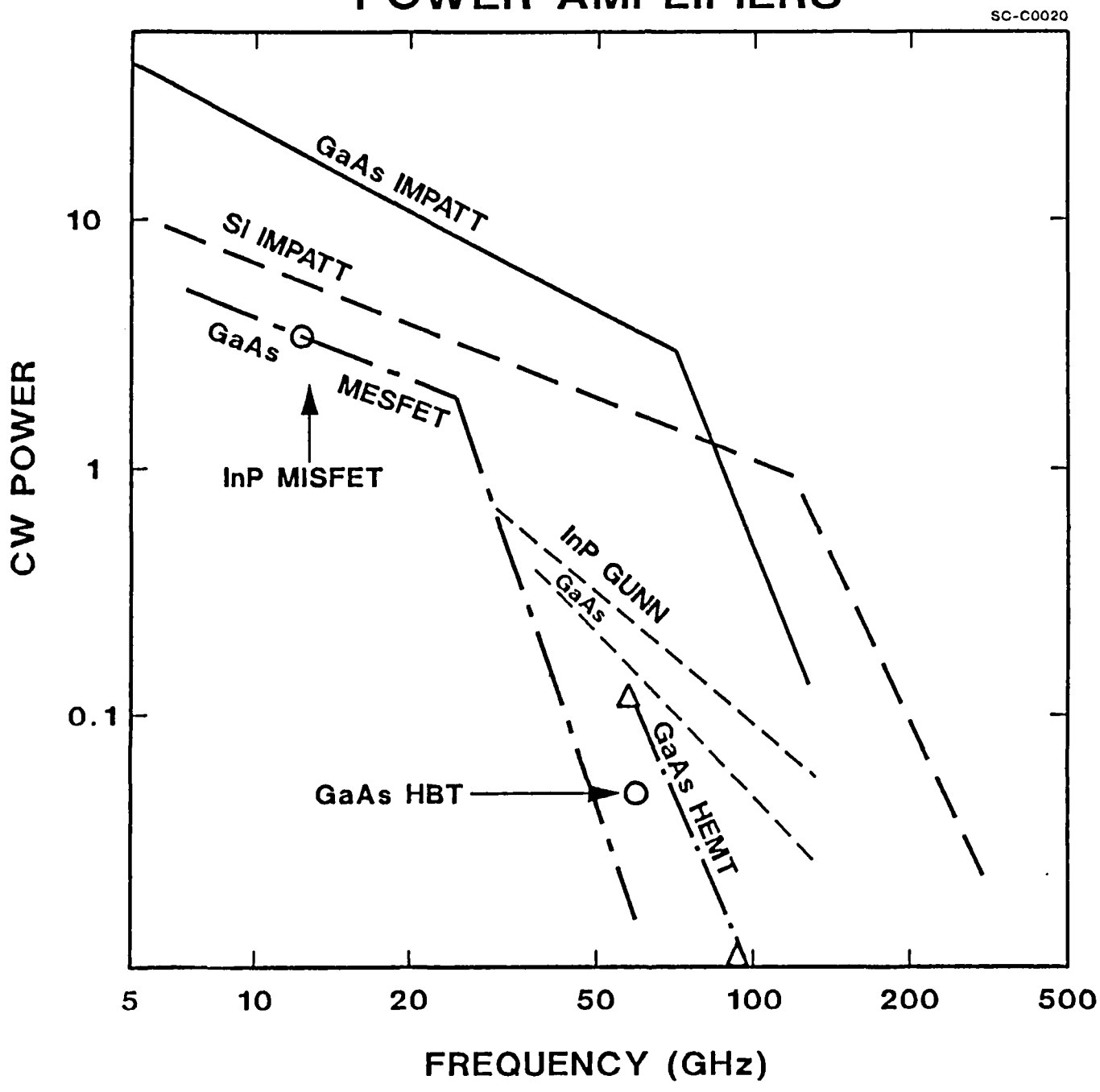


PHASED-ARRAY TRANSMIT ANTENNA

PHASE-SHIFT CONTROL UNIT



MICROWAVE AND MM-WAVE SOLID-STATE POWER AMPLIFIERS



CONCLUSIONS

CONCLUSIONS

* 94 GHz PHASED-ARRAY TRANSMIT ANTENNA (WITH EIRP OF 50 dBW AND 1500 MODULES) MIGHT BE FEASIBLE, PROVIDING THAT HBTs WITH f_{max} OF 240 GHz AND POWER-ADDED EFFICIENCY IN EXCESS OF 30% (AT 94 GHz) BECOME AVAILABLE

* AS A FIRST STEPPING STONE, A 60 GHz 4 X 4 ELEMENT SUBARRAY WITH "END FIRE" RADIATORS IS A SENSIBLE DEMONSTRATION VEHICLE

CONCLUSIONS (Cont.)

* FOR THE SUBARRAY, THE FOLLOWING KEY ISSUES MUST BE ADDRESSED:

  - POWER DISSIPATION
  - CHIP SIZE, COMPONENT PARAMETER UNIFORMITY, AND PROCESSING YIELD
  - SUBARRAY INTEGRATION
  - SURFACE WAVES, BLIND ANGLES AND CROSS-COUPLING WITHIN CIRCUITS AND BETWEEN RADIATORS
  - GENERATION OF HIGH QUALITY CIRCULAR POLARIZATION

Materials Choice for Ballistic and Drift Transport Devices

S. Krisnamurphy

SRI International
Menlo Park, CA

MATERIALS CHOICE FOR BALLISTIC AND DRIFT TRANSPORT DEVICES

S. KRISNAMURTHY, A. SHER AND A.-B. CHEN
SRI INTERNATIONAL
MENLO PARK, CA

AUBURN UNIVERSITY
AUBURN, AL

TOPICS:

- FACTORS THAT INFLUENCE MAT. SELECTION
- QUANTITATIVE ESTIMATION
- RELATIVE EVALUATION OF VARIOUS SEMICONDUCTORS COMPOUNDS & ALLOYS
- COMPARISON WITH EXPERIMENT
- FUTURE WORK

SEMICONDUCTOR ALLOY ENGINEERING FOR HIGH-SPEED DEVICES

PROJECT F49620-85-C-0103 SRI INTERNATIONAL

Objective

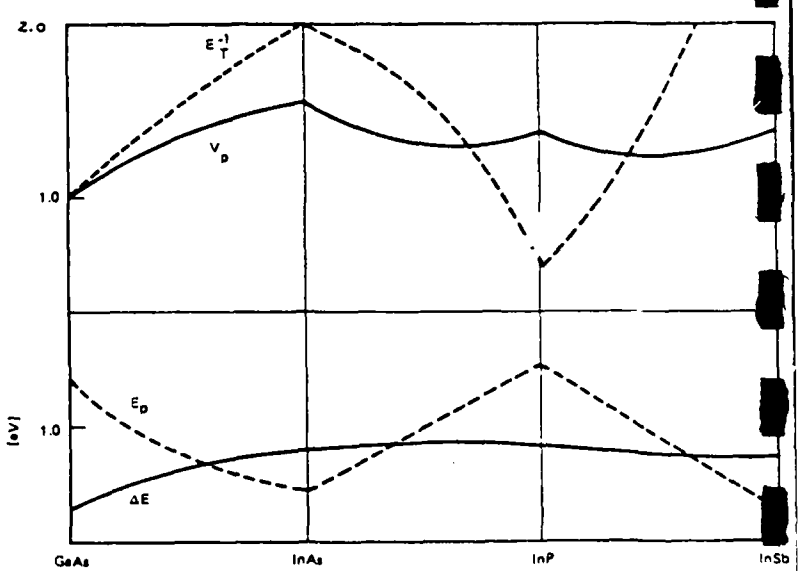
To develop a comprehensive theory of electronic transport properties of semiconductor materials with emphasis on optimal materials for High-speed devices

APPROACH

- Calculate computed band structure and scattering rate in the semi-conductor alloys incorporating diagnol and off-diagonal disorder in the coherent potential approx-imation (CPA)
- Using simple models, calculate peak velocity and threshold field to study trends
- Once candidates for high-speed devices are chosen, carry out detailed quantum transport calculations

STATUS

- Full band structure
- Free of transport related parameters
- Quantitative understand of various mechanisms
- Faster solution to Boltzmann Equation
- Optimum base materials for draft and quasi-ballistic transport



FACTORS

BALLISTIC MODE

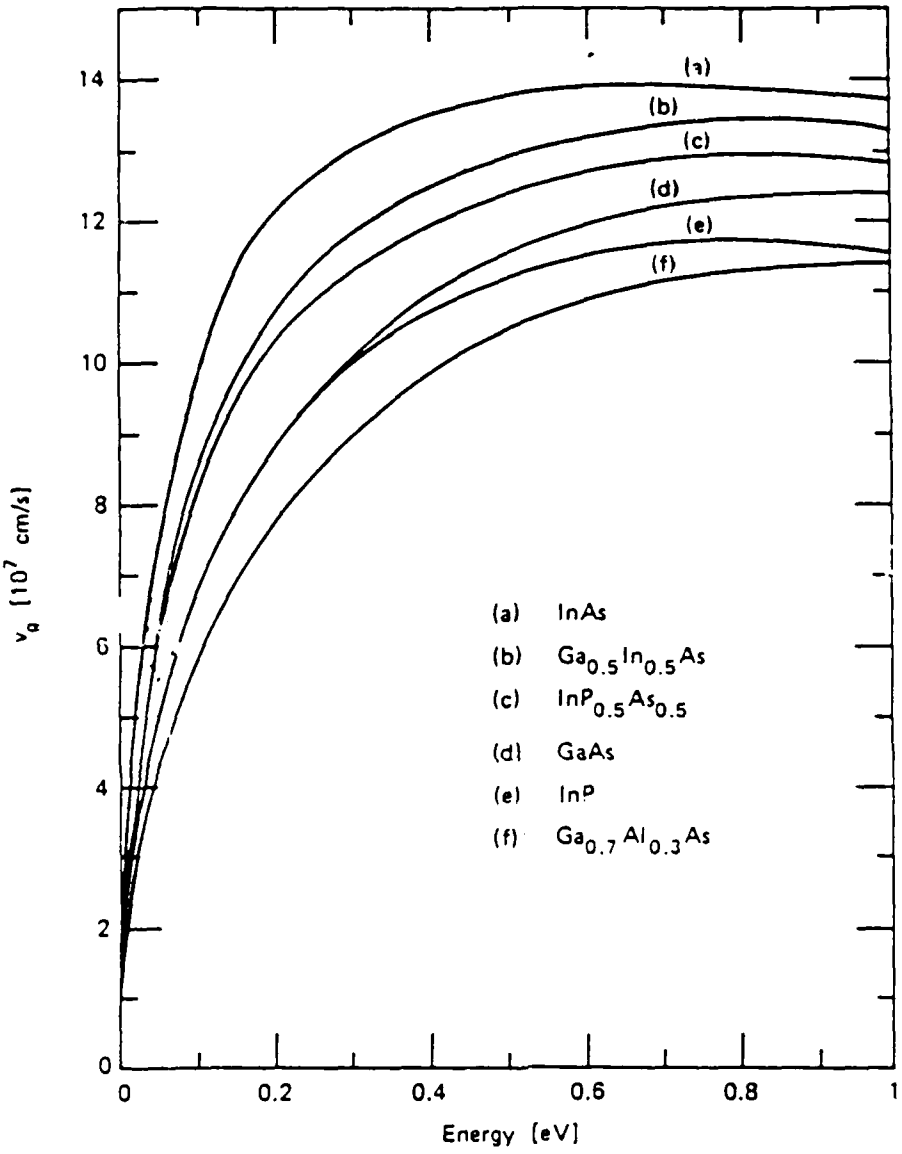
- BANDSTRUCTURE
- GROUP VELOCITY
- SCATTERING MECHANISMS
- INJECTION ENERGY
- INJECTION DIRECTION
- ELECTRIC FIELD
- VELOCITY MEAN FREE PATH

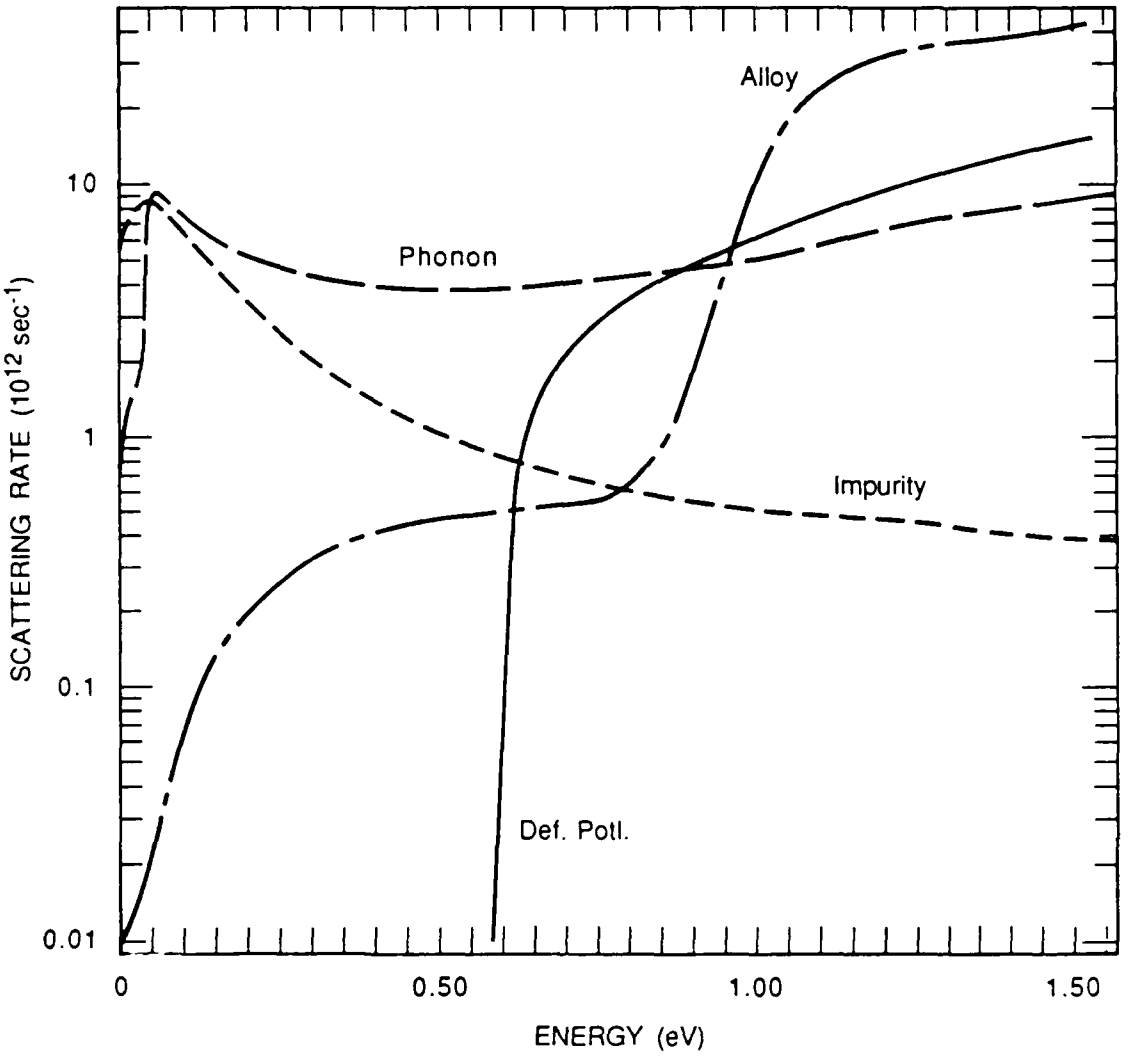
DRIFT MODE

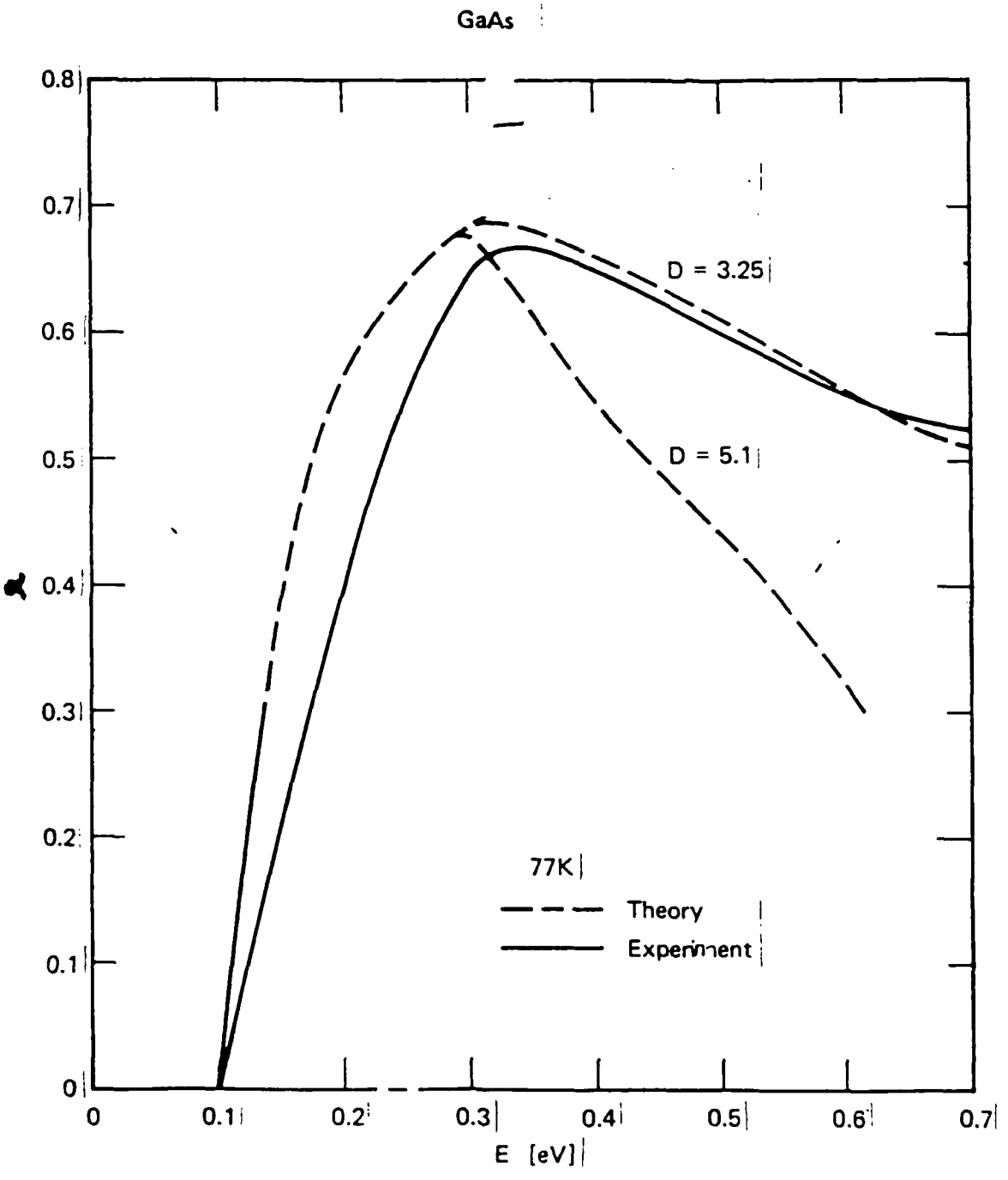
- BANDSTRUCTURE
- PEAK DRIFT VELOCITY
- THRESHOLD ELECTRIC FIELD
- SATURATED DRIFT VELOCITY
- Γ -L ENERGY SEPARATION
- ENERGY GAP
- SCATTERING MECHANISMS
- v-E CURVES

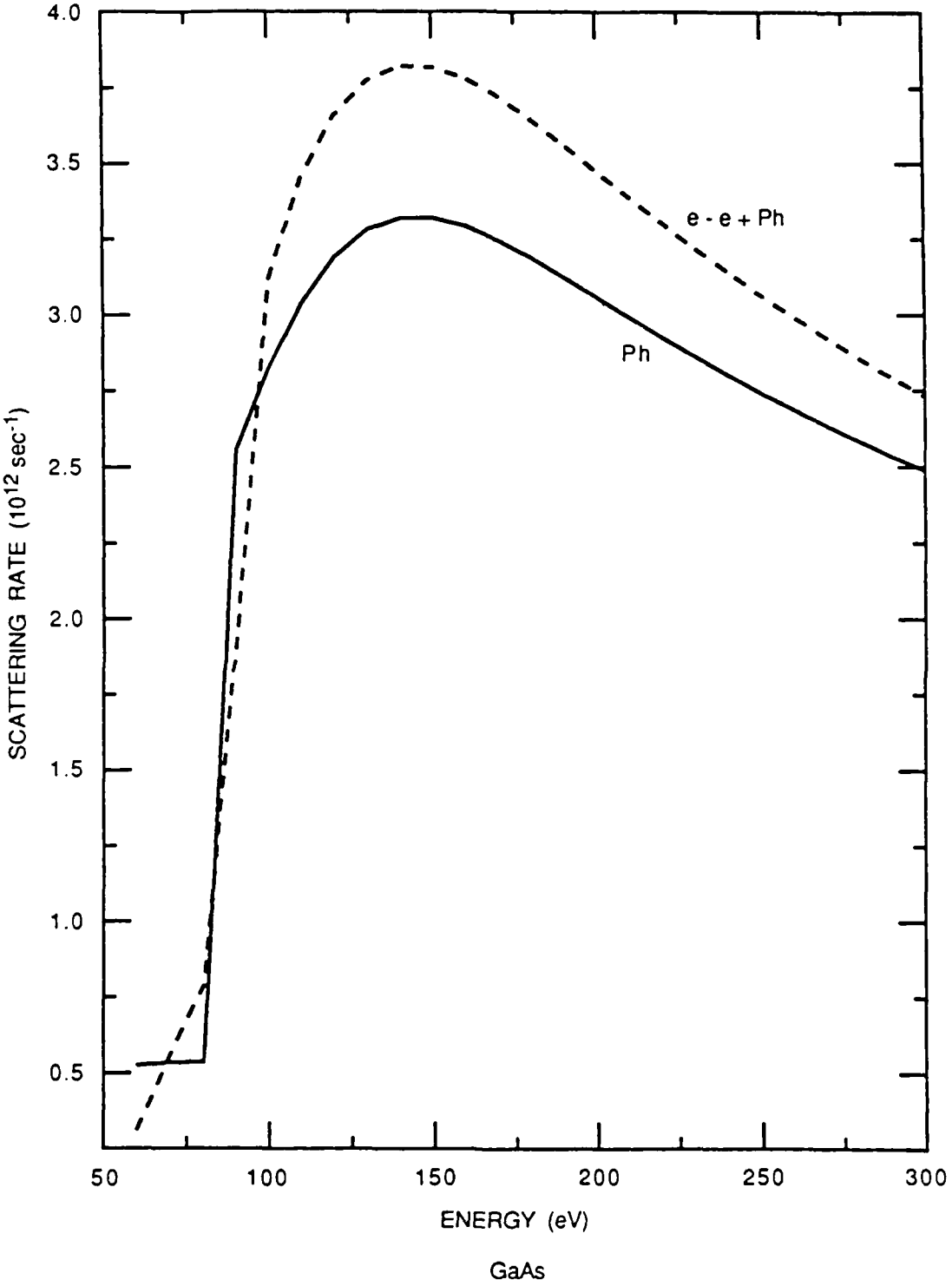
INTRA-and INTER-VALLEY SCATTERING MECHANISMS

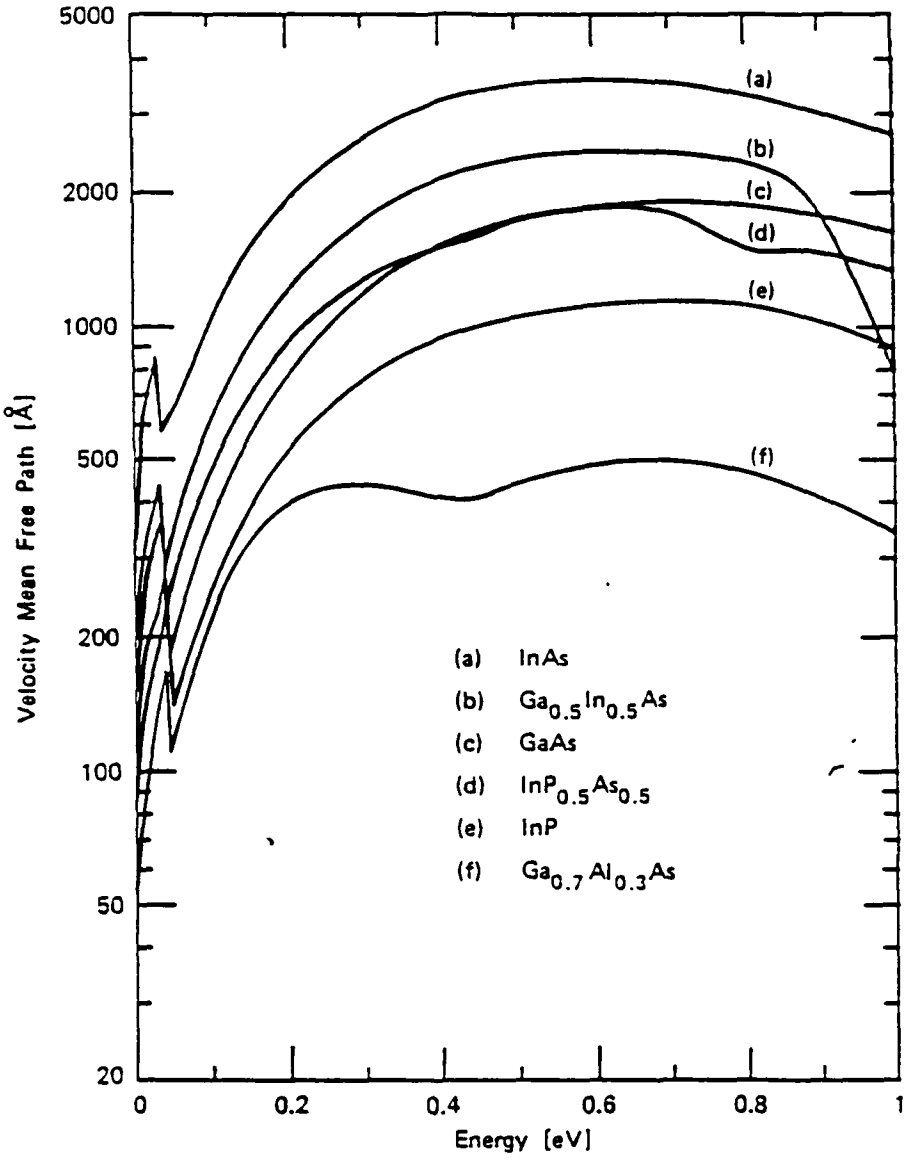
- IONIZED IMPURITIES
- PHONONS IN COMPOUNDS AND ALLOYS
  - TYPES
    - ACOUSTIC
    - OPTIC
  - COUPLING CONSTANTS
    - DEFORMATION POTENTIAL
    - POLAR
- ELECTRON-ELECTRON
- ALLOY DISORDER
- IMPACT IONIZATION

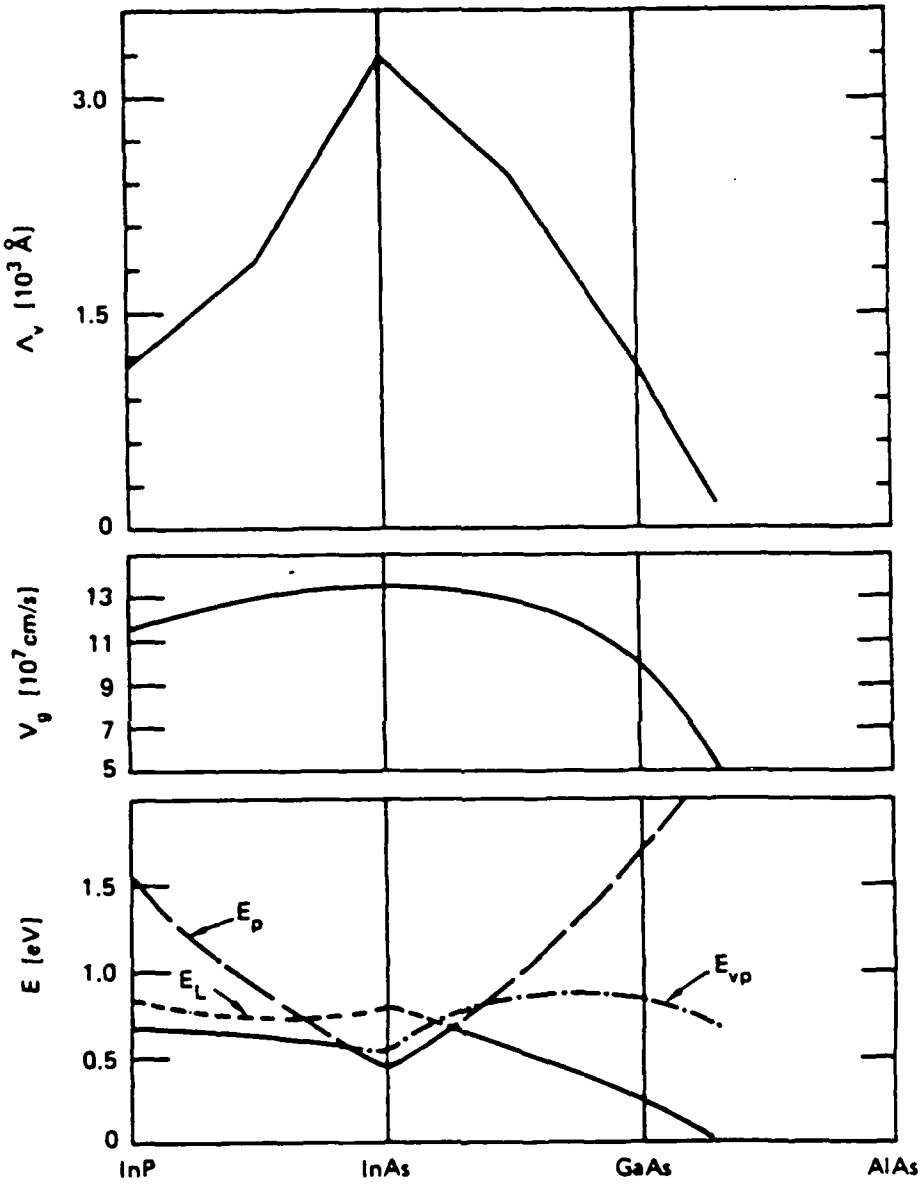

(a)
(b)
(c)
(d)
(e)
(f)
14
12
10
8
6
4
2
0
0
0.2
0.4
0.6
0.8
1
v_a [10^7 cm/s]
Energy [eV]
(a) InAs
(b) $Ga_{0.5}In_{0.5}As$
(c) $InP_{0.5}As_{0.5}$
(d) GaAs
(e) InP
(f) $Ga_{0.7}Al_{0.3}As$


Alloy
Phonon
Impurity
Def. Potl.
10
1
0.1
0.01
0
0.50
1.00
1.50
SCATTERING RATE (10^{12} sec^{-1})
ENERGY (eV)


GaAs
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
D = 3.25
D = 5.1
77K
Theory
Experiment
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
E [eV]


4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
SCATTERING RATE (10^{12} sec^{-1})
e - e + Ph
Ph
50
100
150
200
250
300
ENERGY (eV)
GaAs


5000
2000
1000
500
200
100
50
20
0
0.2
0.4
0.6
0.8
1
Velocity Mean Free Path [Å]
Energy [eV]
(a)
(b)
(c)
(d)
(e)
(f)
(a) InAs
(b) $Ga_{0.5}In_{0.5}As$
(c) GaAs
(d) $InP_{0.5}As_{0.5}$
(e) InP
(f) $Ga_{0.7}Al_{0.3}As$


3.0
1.5
0
Λ_v [10^3 Å]
13
11
9
7
5
V_g [10^7 cm/s]
1.5
1.0
0.5
0
E [eV]
E_p
E_L
E_{vp}
InP
InAs
GaAs
AlAs

DRIFT TRANSPORT

- **Solution to Boltzmann equation by eigen value method.**

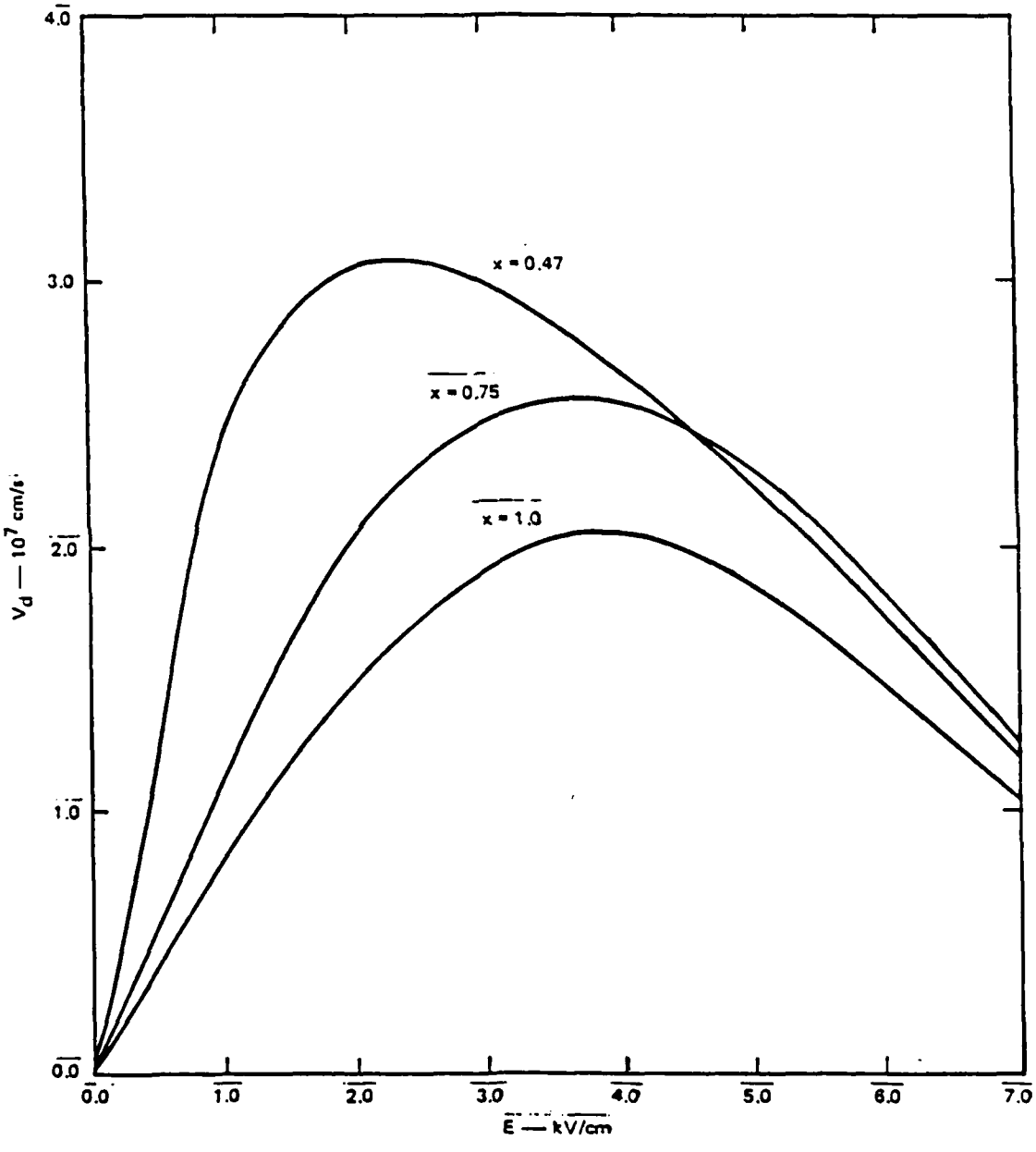
$$\frac{eE}{h}\frac{\partial}{\partial k_x} f(\vec{k}) - \sum_{k'} S(k,k') f(k') + \sum_{k'} S(k',k) f(k) = 0$$

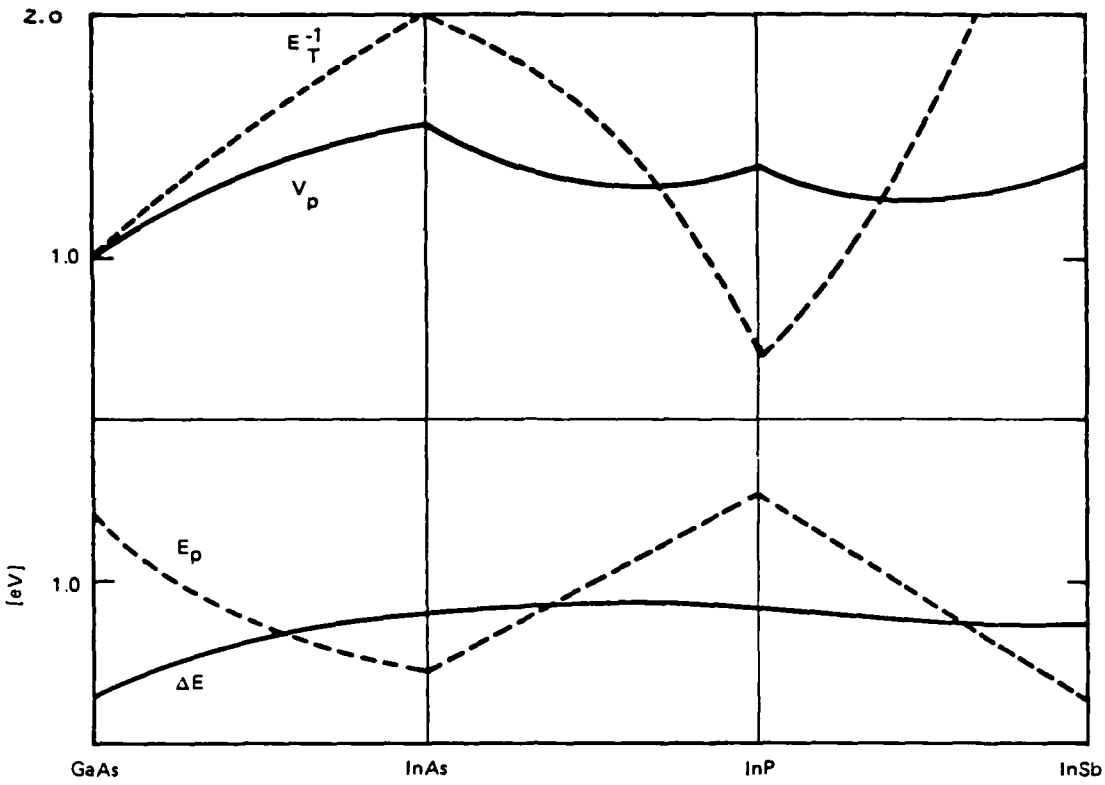
$$f(k) = \sum_{n} C_n \phi_n(k)$$

$$\Rightarrow \underline{M}C = 0$$

Eigen vector corresponding to zero eigen value gives the expansion coefficients C_n.

$Ga_xIn_{1-x}As$.


4.0
3.0
2.0
1.0
0.0
v_d — 10^7 cm/s
x = 0.47
x = 0.75
x = 1.0
0.0
1.0
2.0
3.0
4.0
5.0
6.0
7.0
E — kV/cm


2.0
1.0
E_T^{-1}
V_p
1.0
[eV]
E_p
ΔE
GaAs
InAs
InP
InSb

STATUS

- FULL BAND STRUCTURE
- FREE OF TRANSPORT RELATED PARAMETERS
- QUANTITATIVE UNDERSTANDING OF VARIOUS MECHANISMS
- FASTER SOLUTION TO BOLTZMANN EQUATION
- OPTIMUM BASE MATERIALS FOR DRAFT AND QUASI-BALLISTIC TRANSPORT

FUTURE WORK FOR DEVICE DESIGN

- EMITTER SIDE
  - INJECTION "BALLISTIC" DEVICES
  - INJECTION DRIFT DEVICES
  - INTERFACE
- COLLECTOR SIDE
  - REDUCE SCATTERING
  - INTERFACE
- LARGE CURRENTS
  - SPACE CHARGE
  - POTENTIAL VARIATION IN THE BASE
  - SELF CONSISTENT SOLUTION TO POISSON AND BOLTZMANN EQUATIONS

FUTURE WORK (contd.)

- 2D NATURE
  - ALLOY SEGREGATION
    - COMPOSITION DEPENDS ON LOCATION OF THE LAYER
    - ORDER/DISORDER TRANSITION
    - ELECTRONIC STRUCTURE AND TRANSPORT
  - EFFECTIVE MASS APPROXIMATION NOT VALID
  - QUANTUM TRANSPORT
    - MATCHING 2D BLOCK STATES
    - GREENS FUNCTION APPROACH
    - SCATTERING MECHANISM
    - WIGNER FUNCTIONS
- DEVICE CHARACTERISTICS
  - TRANSANDUCTANCE
  - CUT OFF FREQUENCY
  - FREQUENCY DEPENDENT CURRENT GAIN
  - POWER OUTPUT
  - SELECT MATERIALS AND GEOMETRIES TO OPTIMIZE DEVICE CHARACTERISTICS

AlInAs-GaInAs HEMTs FOR HIGH SPEED APPLICATIONS

U. K. Mishra

North Carolina State University
Raleigh, NC

AlInAs-GaInAs HEMTs

FOR HIGH SPEED APPLICATIONS

U.K. Mishra*, A.S. Brown**, and J.F. Jensen

* Now at N.C. State University, Raleigh, NC
** Now at Army Research Office, Durham, NC

RESEARCH LABORATORIES

ACKNOWLEDGEMENTS

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S. Rosenbaum
S. Vaughn
L. Larson

MANAGERMENT SUPPORT: M.J. Delaney, P.T. Greiling, C.F. Krumm

OUTLINE

HUGHES
RESEARCH LABORATORIES

- ADVANTAGES AND DISADVANTAGES OF AlInAs-GaInAs HEMTs AND HBTs.

- AlInAs-GaInAs HEMTS (RELATIVE TO GaAs BASED HEMTs)
  - DEVICE RESULTS
  - CIRCUIT RESULTS

- CONCLUSIONS

AlInAs-GaInAs HBTs

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ADVANGTAGES

- EXCELLENT THRESHOLD CONTROL
- COMPATIBLE WITH OTHER OPTO-ELECTRONIC ELEMENTS
- EXCELLENT DRIVE CAPABILITY
  ⇒ LOW FAN-OUT SENSITIVITY

DISADVANTAGES

- LOW COLLECTOR BREAKDOWN
- DIFFICULTY IN GROWING AlInAs
- LARGE NUMBER OF PROCESSING STEPS
- VERTICAL DEVICES ⇒ HIGH PARASITICS

AlInAs-GaInAs HEMTs

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RESEARCH LABORATORIES

ADVANGTAGES

- EXCELLENT LOW NOISE DEVICE
- SURFACE ORIENTED DEVICE
  - ⇒ Low Parasitics
- EXCELLENT DRIVE CAPABILITY
  - ⇒ Low Fan-Out Sensitivity in Circuits
- EXCELLENT HIGH FREQUENCY CHARACTERISTICS
- FEW MASK LEVELS

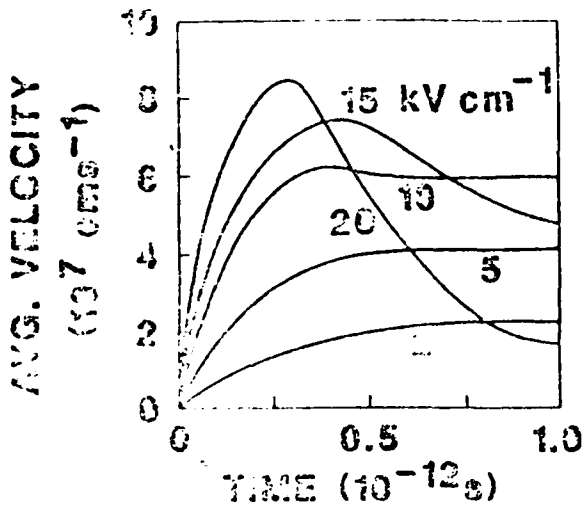
DISADVANTAGES

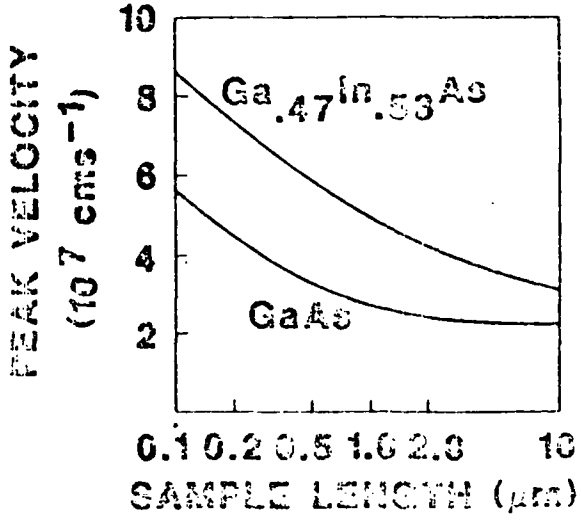
- LOW GATE BREAKDOWN
- POOR THRESHOLD CONTROL
- DIFFICULTY IN GROWING AlInAs

ADVANTAGES OF $Ga_{.47}In_{.53}As$ TRANSISTORS

18435-2

- HIGH ELECTRON MOBILITY
  - $n_S\downarrow$, $R_D\downarrow$
  - $\left[\mu(Ga_{.47}In_{.53}As) = 13{,}000\ cm^2V^{-1}s^{-1}\right.$
  - $\left.\mu(GaAs) = 8{,}000\ cm^2V^{-1}s^{-1}\right]$
- LARGE Γ–L VALLEY SEPARATION
  - $\left[\Delta\Gamma\text{–}L(Ga_{.47}In_{.53}As) = 0.55eV\right.$
  - $\left.\Delta\Gamma\text{–}L(GaAs) = 0.31eV\right]$
- HIGH PEAK VELOCITY
  - $g_m\uparrow$, $f_T\uparrow$
  - $\left[V_p(Ga_{.47}In_{.53}As) = 2.7 \times 10^7 cms^{-1}\right.$
  - $\left.V_p(GaAs) = 2\times10^7 cms^{-1}\right]$
- STRONGER VELOCITY OVERSHOOT
  - $g_m\uparrow$, $f_T\uparrow$





(NAG, et., al.)

AUGUST 1978

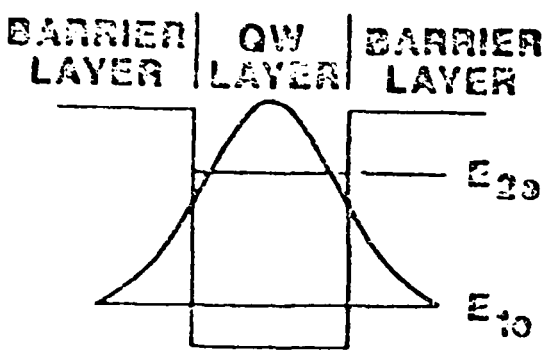
DIFFICULTIES IN GROWING AlInAs

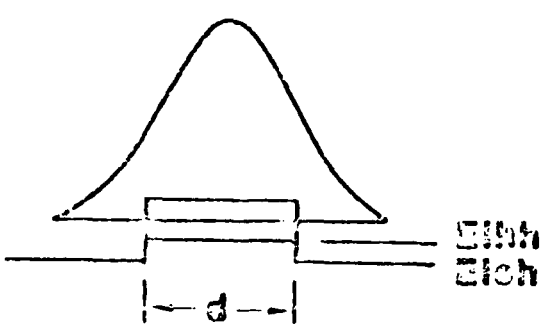
HUGHES

- Al-Al and In-In bonds have widely different bond strengths
- High As_4 overpressure is needed to prevent In desorption (reduces cation mobility)
- Low growth temperature to prevent In desorption (reduces cation mobility)
- Alloy tends to cluster into component binaries

PHOTOLUMINESCENCE CHARACTERIZATION OF QUANTUM WELLS

ROUGH





RECOMBINATION EMISSION ENERGY DETERMINED BY ΔE_g AND d

FULL WIDTH HALF MAXIMUM (FWHM) DETERMINES:

- QUALITY OF WELL (d > 100 Å)

  QUALITY OF INTERFACE (20 < d < 100 Å)

- QUALITY OF BARRIER (d < 20 Å)
- ASSUMING THE EXITON RADIUS (~200 Å) IS ≤ ½ (THE ISLAND SIZE)

MATERIAL QUALITY

18430-10

GaInAs

11 K PL LINEWIDTH OF 2.5 meV

$N_d - N_a = 2 \times 10^{15}$ cm^{-3}

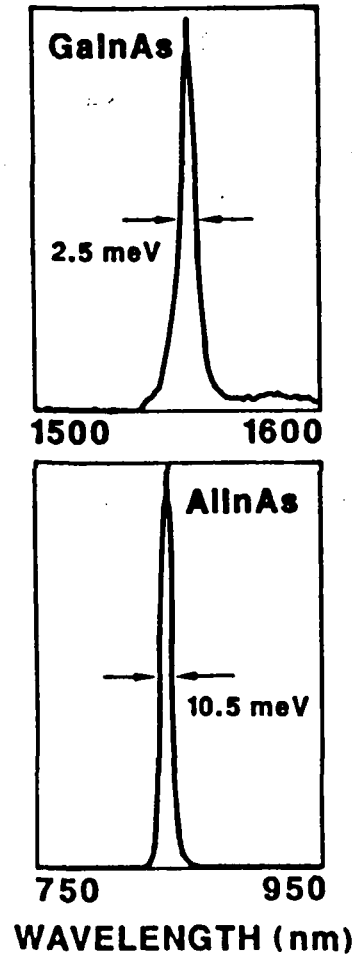
μ(300 K) = 8000 – 10000 cm^2/V•s

AlInAs

11 K PL LINEWIDTH OF 10.5 meV

$N_d - N_a = 1 \times 10^{15}$ cm^{-3}

μ(300 K) = 1600 cm^2/V•s



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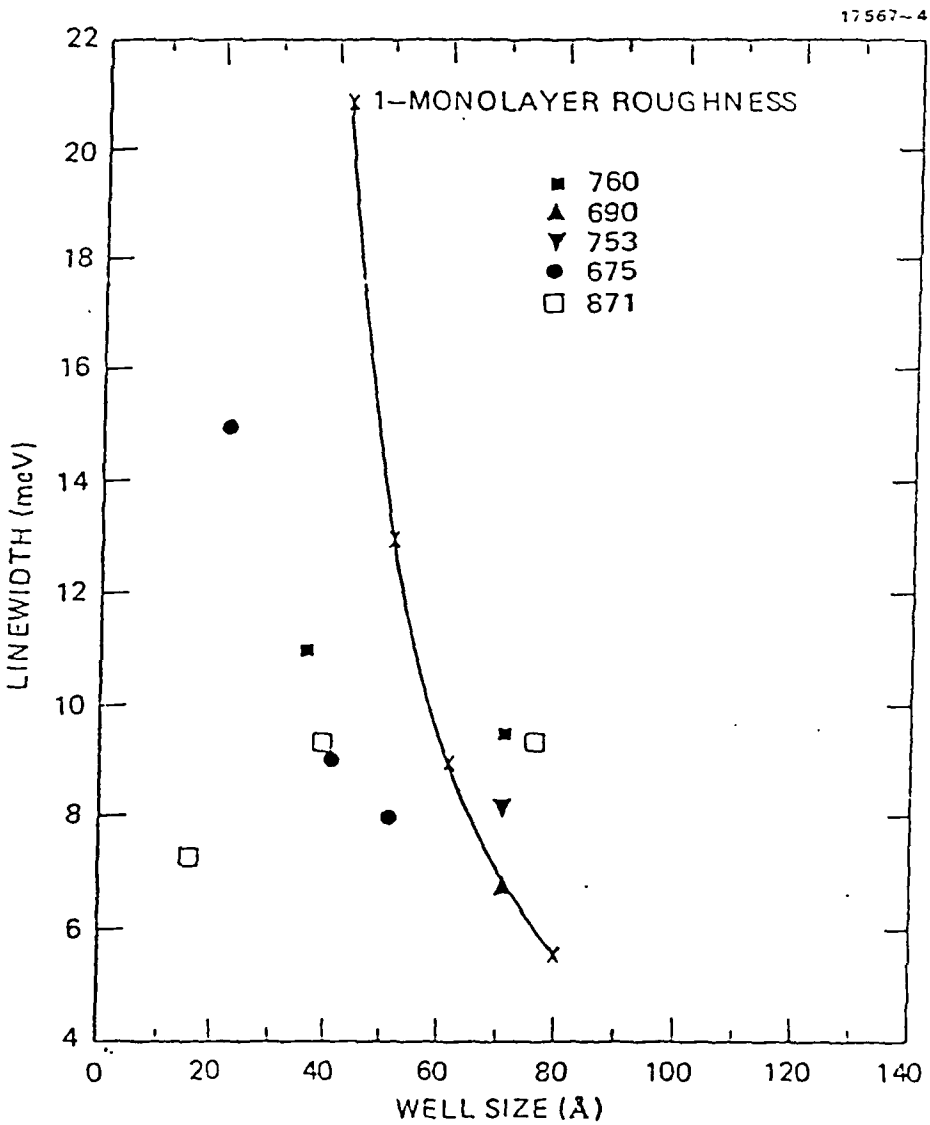
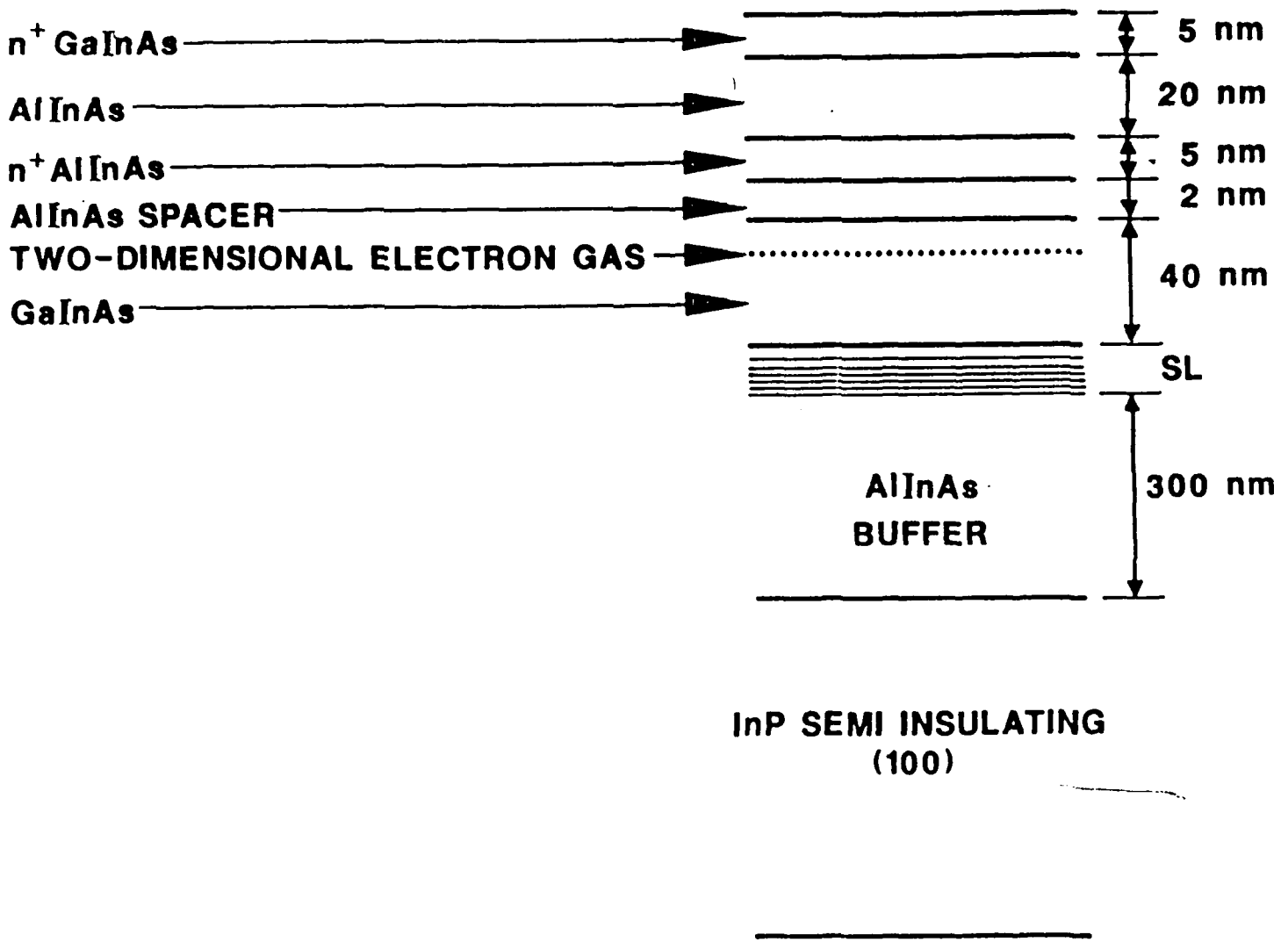

17567-4
1-MONOLAYER ROUGHNESS
760
690
753
675
871
LINEWIDTH (meV)
WELL SIZE (Å)
22
20
18
16
14
12
10
8
6
4
0
20
40
60
80
100
120
140

GaInAs/AlInAs HEMT LAYERED STRUCTURE

PROJECT 59

HUGHES

18430-33



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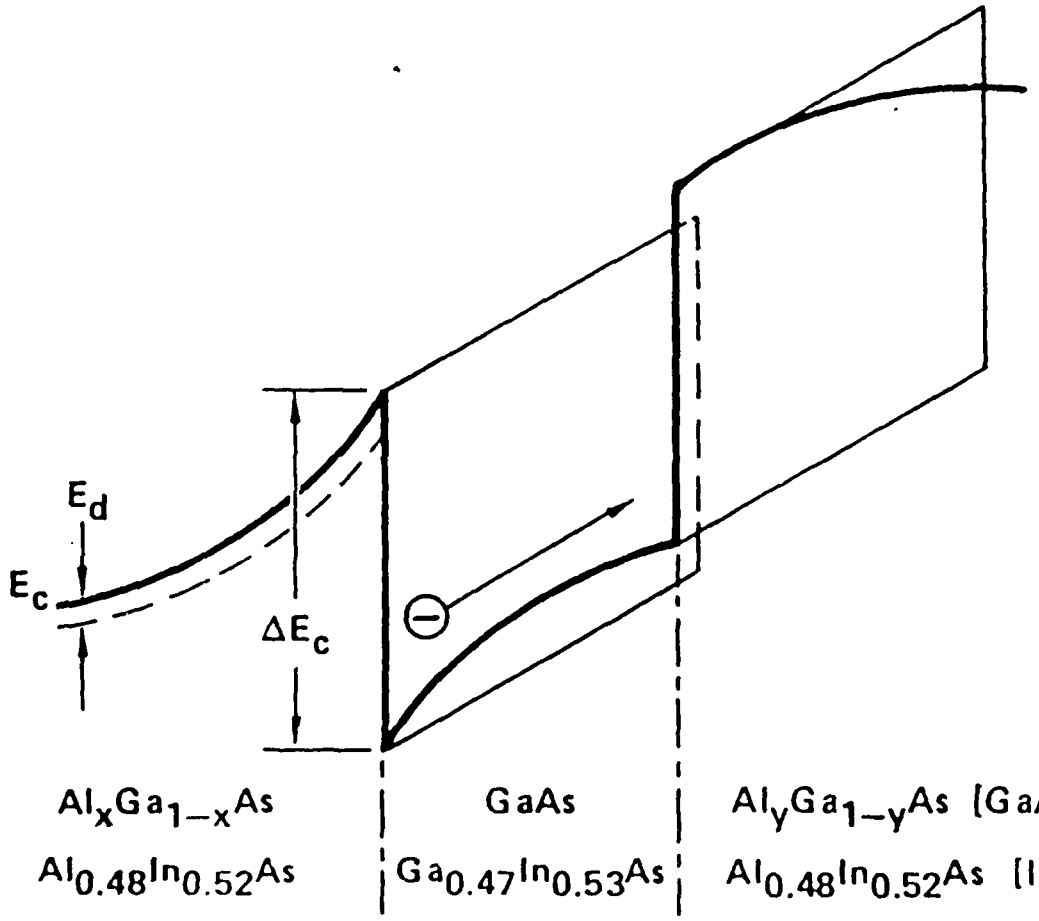
COMPARISON OF AlGaAs–GaAs AND AlInAs–GaInAs HETEROSTRUCTURES

17778-1



AlGaAs–GaAs

- $\Delta E_c = 0.25$ eV
- $n_s = 1x10^{12}$ cm^{-2}
- $\mu = 7000$ cm^2 V^{-1}s^{-1}
- $v_s = (1–2)x10^7$ cms^{-1}
- v_p (0.25 μm) = $(3–4)x10^7$ cms^{-1}

AlInAs–GaInAs

- $\Delta E_c = 0.55$ eV
- $n_s > 3x10^{12}$ cm^{-2}
- $\mu = 10{,}000$ cm^2 V^{-1}s^{-1}
- $v_s = (1–2)x10^7$ cms^{-1}
- v_p (0.25 μm) = $(6–7)x10^7$ cms^{-1}

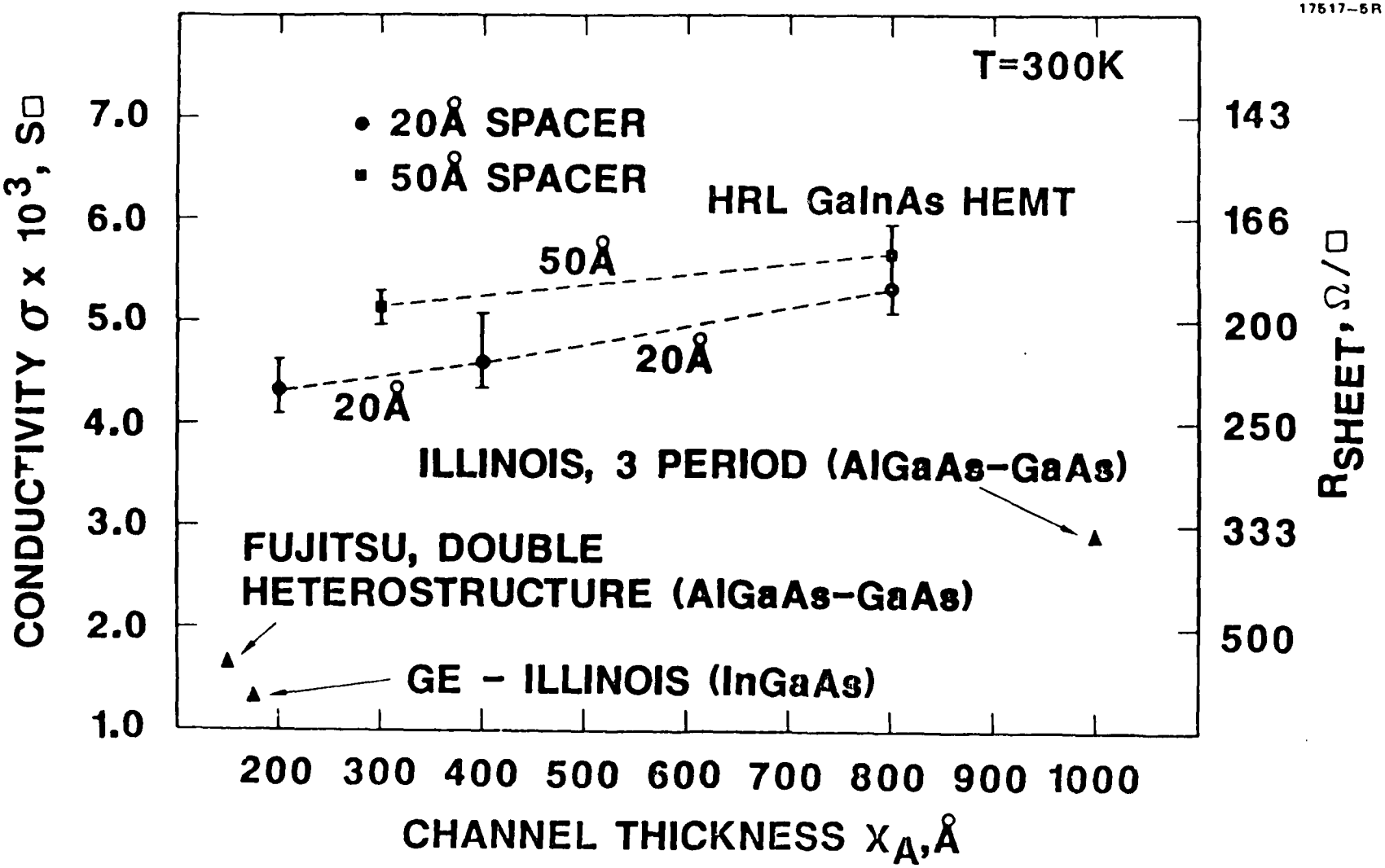
AUGUST 1988

PROJECT 59

CONDUCTIVITY vs. CHANNEL THICKNESS

HUGHES

17517-5R1



AUGUST 1987

STRAINED GaInAs HEMT

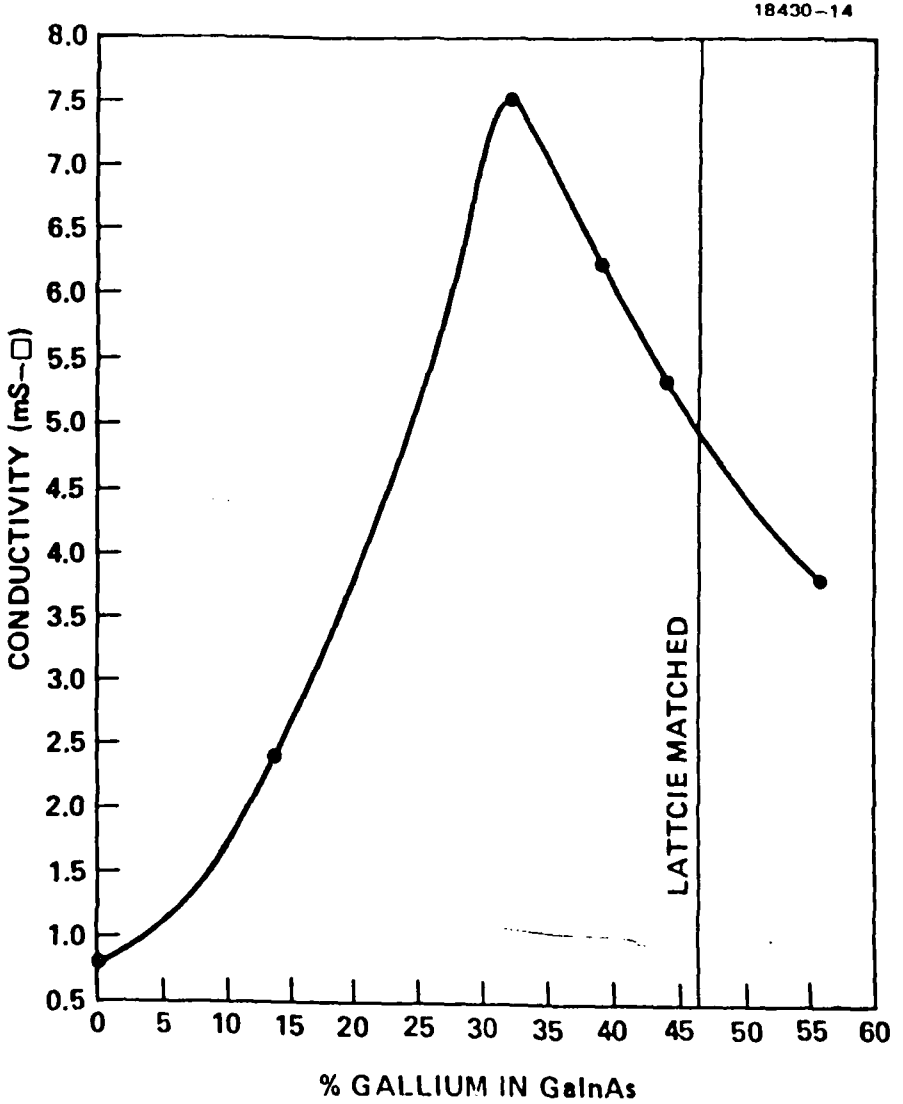
PROJECT 59

HUGHES

18430-14

STRAINED GaInAs-AlInAs HEMT

$Ga_{.47-y}In_{.53+y}As$ CONTACT	$n=2x10^{18}$	100A
$Al_{.48+u}In_{.52-u}As$ SCHOTTKY		200A
$Al_{.48+u}In_{.52-u}As$ DONOR	$n=4x10^{18}$	125A
$Al_{.48+u}In_{.52-u}As$ SPACER		20A
$Ga_{.47-y}In_{.53+y}As$ CHANNEL		400A
$Al_{.48}In_{.52}As$ BUFFER		2500A
InP	SEMI-INSULATING SUBSTRATE	



AUG 1988

WHY THE AlInAs-GaInAs HEMT FOR mm-WAVE LOW NOISE APPLICATIONS

C18309-2R1

- $F_{min} = 1 + K_f \frac{f}{f_T}\sqrt{g_m(R_g+R_s)}$
- LARGE $\Gamma - L$ SEPARATION IN $Ga_{.47}\ In_{.53}\ As$ ($\Delta\Gamma - L = 0.55$ eV) LEADS TO LOW INTERVALLEY NOISE ($K_F \downarrow$)
- LOW SHEET RESISTANCE OF THE TWO DIMENSIONAL ELECTRON GAS ($\varrho \cong 150\ \Omega/\square$) REDUCES THERMAL NOISE
- HIGH ELECTRON VELOCITY IN SHORT CHANNELS GaInAs (V_P ~6-7x10 ^{7} cm-s^{-1}) ($f_T \uparrow$, $g_m \uparrow$)

EPITAXIAL LAYER DESIGN OF $Al_{.48}In_{.52}As$ / $Ga_{.47}In_{.53}As$ AND $Al_{.48}In_{.52}As$ / $Ga_{.38}In_{.62}As$ HEMTs

$Ga_{.47}In_{.53}As$	CONTACT	(n = 5 x 10^{18})	70Å
$Al_{.48}In_{.52}As$	SCHOTTKY		315Å
$Al_{.48}In_{.52}As$	DONOR	(n = 5 x 10^{18})	80Å
$Al_{.48}In_{.52}As$	SPACER		15Å
$Ga_{.47}In_{.53}As$	CHANNEL		360Å
	SUPERLATTICE		360Å
AlInAs	BUFFER		2250Å
	InP:Fe		

μ (300K) = 9300 $cm^2V^{-1}S^{-1}$
$n_s \geq 3 \times 10^{12}$ cm^{-2}

$Ga_{.47}In_{.53}As$	CONTACT	(n = 5 x 10^{18})cm^{-3}	70Å
$Al_{.48}In_{.52}As$	SCHOTTKY		200Å
$Al_{.48}In_{.52}As$	DONOR	(n = 5 x 10^{18})cm^{-3}	75Å
$Al_{.48}In_{.52}As$	SPACER		15Å
$Ga_{.38}In_{.62}As$	CHANNEL		270Å
	SUPERLATTICE		360Å
$Al_{.48}In_{.52}As$	BUFFER		2250Å
InP	SEMI-INSULATING SUBSTRATE		

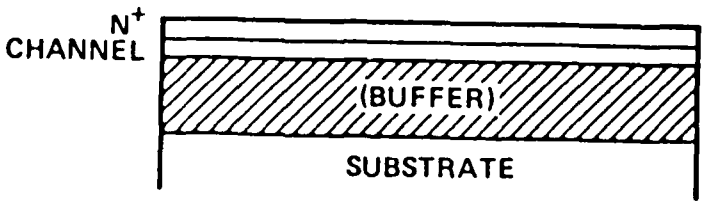
μ (300K) = 10,000 $cm^2V^{-1}S^{-1}$
$n_s \geq 4 \times 10^{12}$ cm^{-2}

SUPERFET: PROCESS OUTLINE

HUGHES

14754-3

1. MBE LAYER GROWTHS – MULTI-EPI OR HEMT



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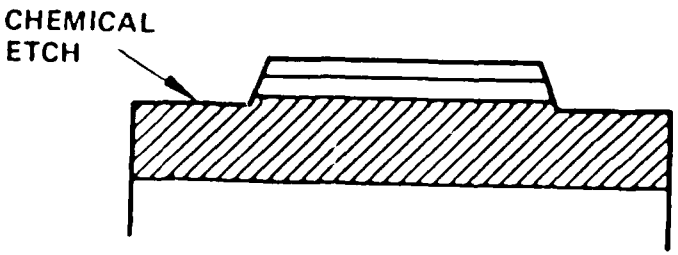
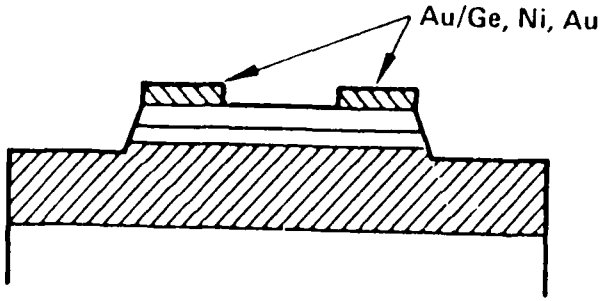
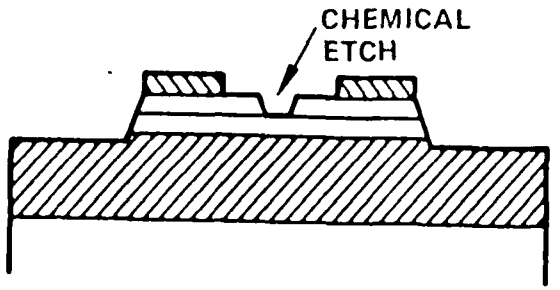


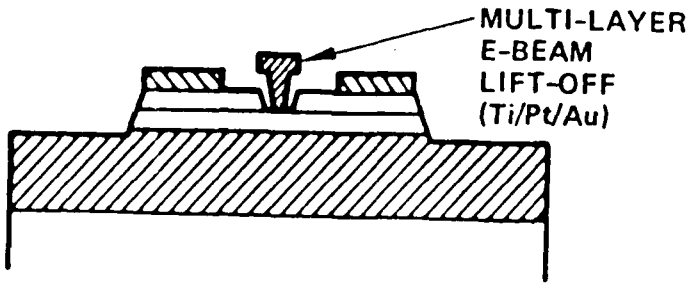
3. OHMIC CONTACTS



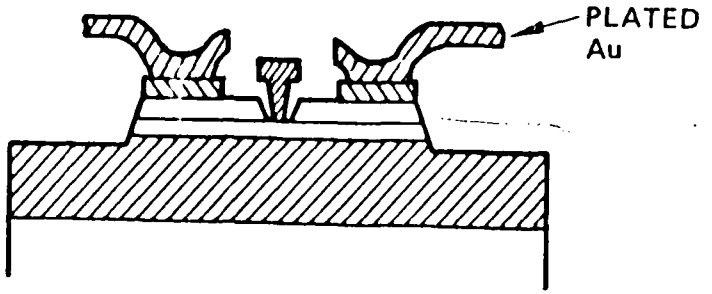
4. E-BEAM GATE RECESS – ESTABLISHES V_{PO}



5. E-BEAM T-GATE FABRICATION



6. AIRBRIDGE FABRICATION



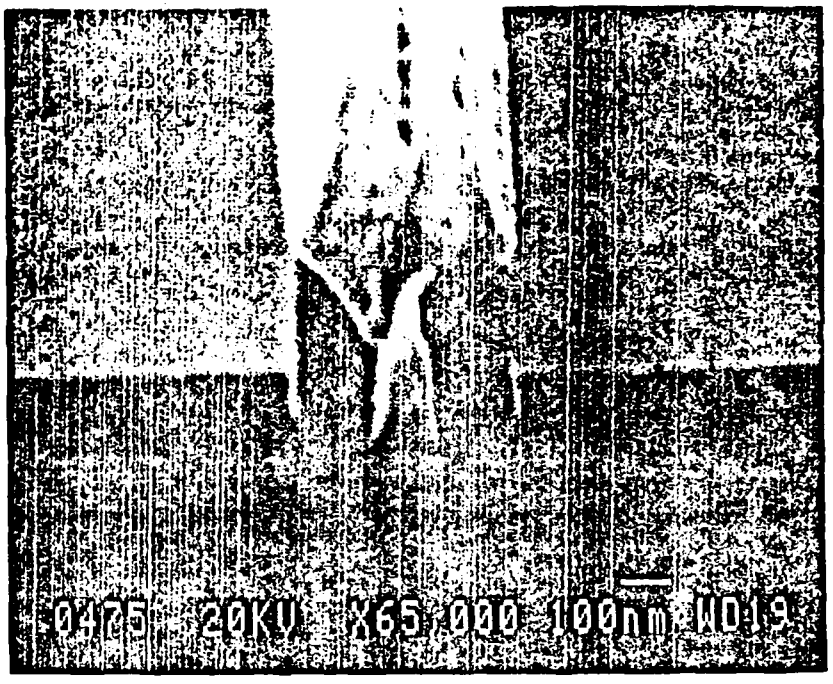
JANUARY 1985

0.1 μm T-GATE PROCESS

HUGHES

17564-11R1

- 4570 Å Ti-Pt-Au METALIZATION
- 0.1 μm T-GATE
- 7.5 INCREASE IN GATE CROSS-SECTIONAL AREA



OCTOBER 1987

13844A CS JUN 85

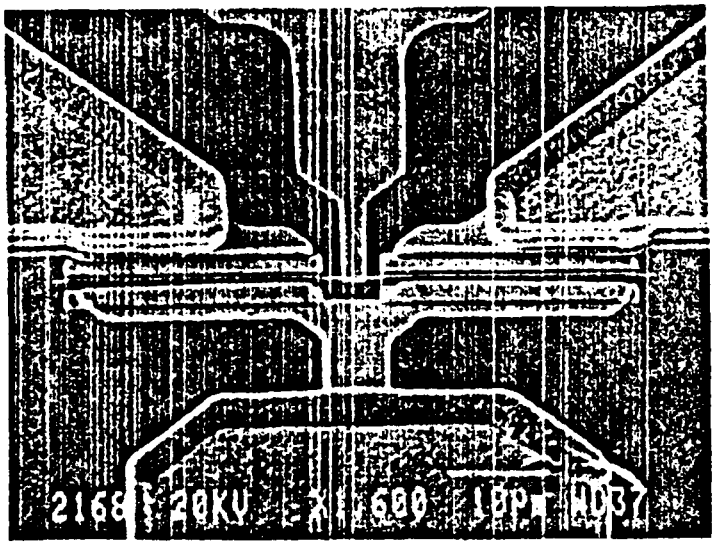
CLASSIFICATION

GaInAs HEMT V-BAND DEVICE DESIGN

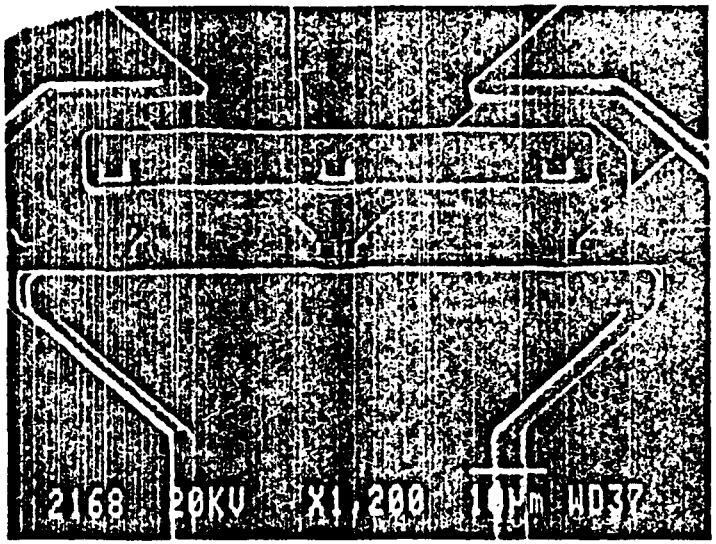
PROJECT 59

HUGHES

18430-18



50 µm WIDE DEVICE
T GATE FEED

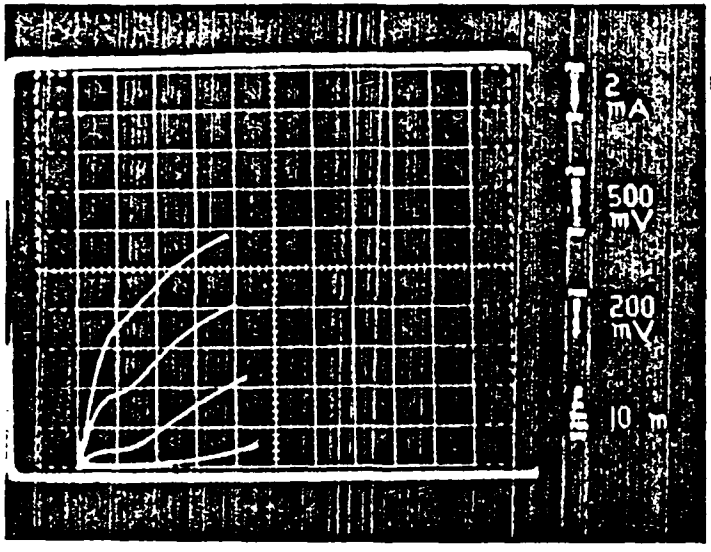


75 µm WIDE DEVICE
πGATE FEED

AUG 1988

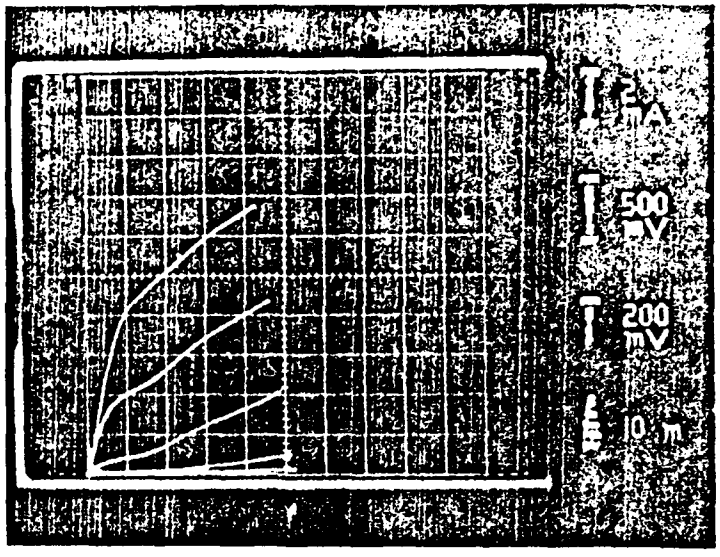
DC I–V CHARACTERISTICS OF 0.2 μm AND 0.1 μm GATE LENGTH HEMTs

18309--7R1



gm = 800 mS/mm

W = 25 μm

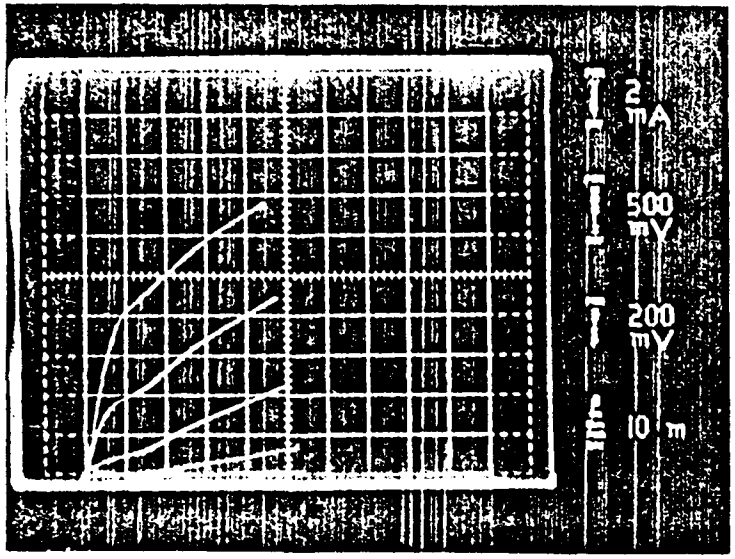


gm = 1080 mS/mm

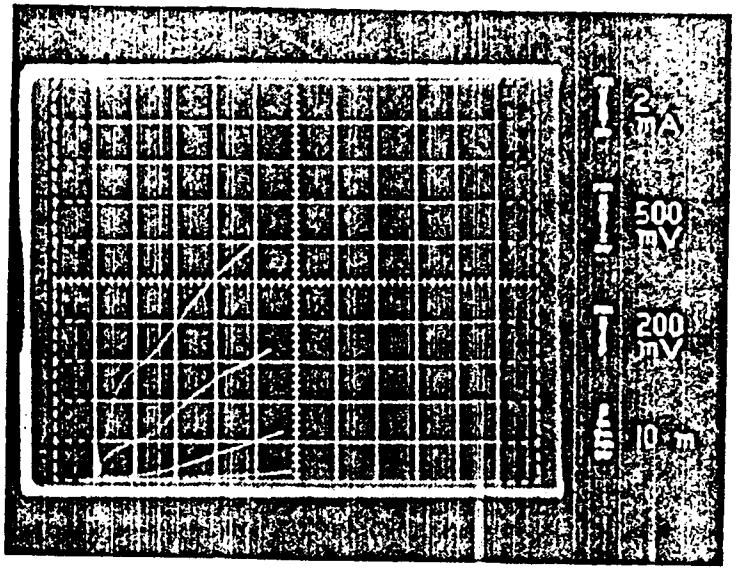
W = 25 μm

AUGUST 1988

DC I-V CHARACTERISTICS OF 0.1 μm GATE LENGTH $Al_{.48}In_{.52}As$ / $Ga_{.47}In_{.53}As$ & $Al_{.48}In_{.52}As$ / $Ga_{.38}In_{.62}As$ HEMTs



g_m = 1000 mS/μm
V_{FB} = 0.4 V
W = 25 μm

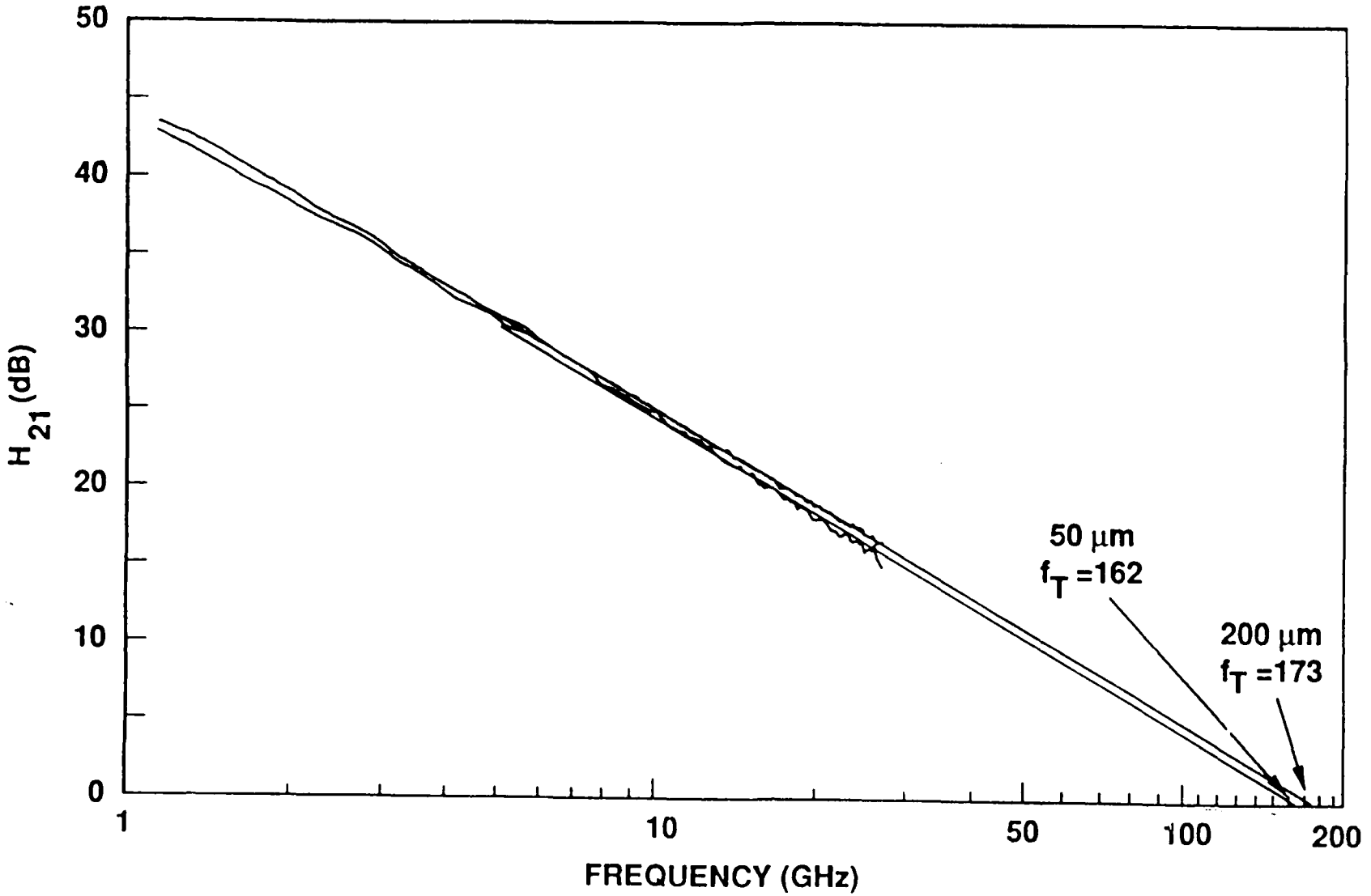


g_m = 1160 mS/μm
V_{FB} = 0.28 V
W = 25 μm

0.1 μm LATTICE MATCHED HEMT
$Al_{.48}In_{.52}As/Ga_{.47}In_{.53}As$

HUGHES

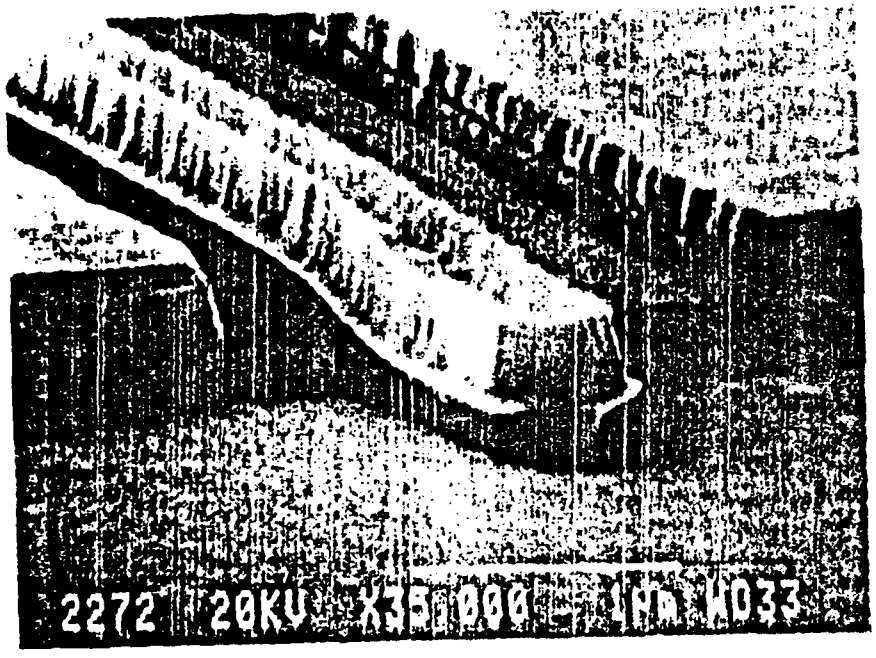
C8852-05-02

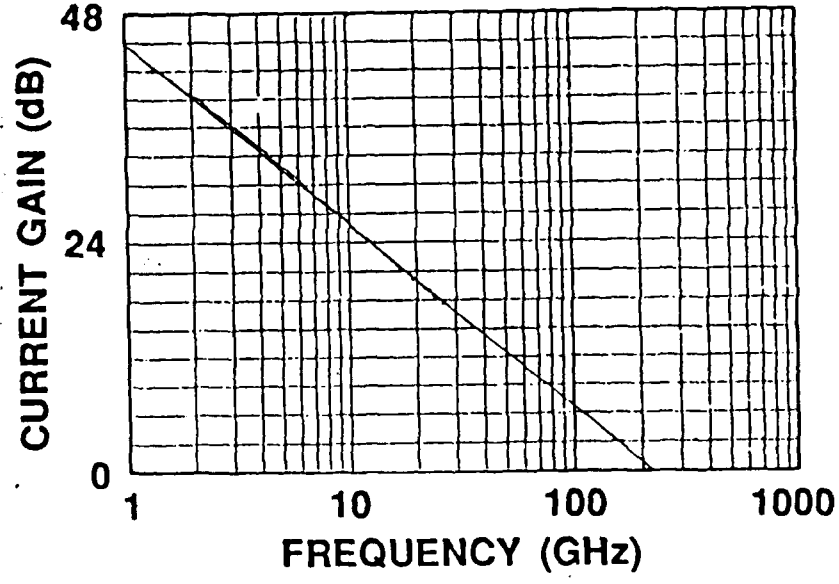


GaInAs HEMT 0.1 μm T-GATE

HUGHES

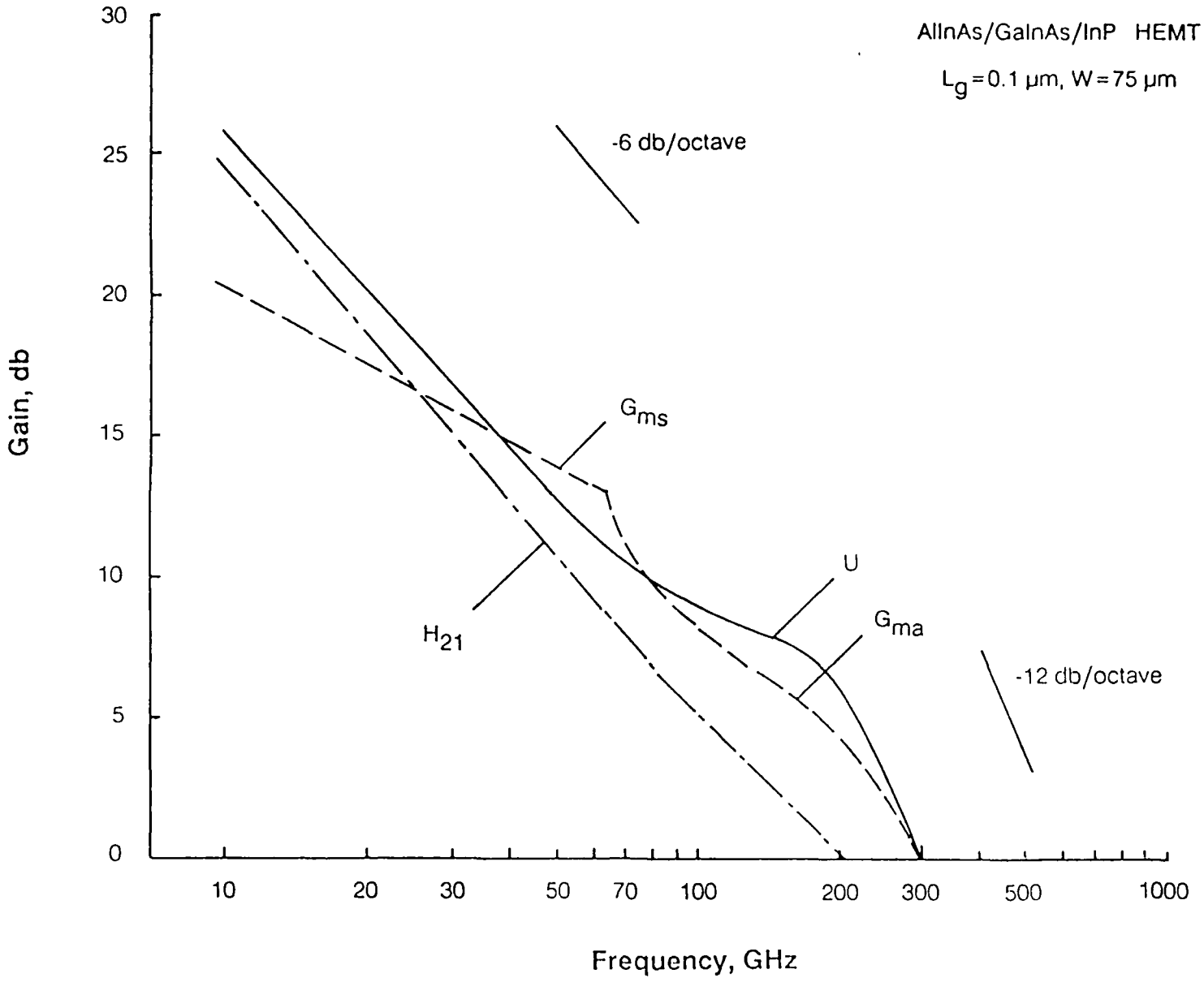
18335-1

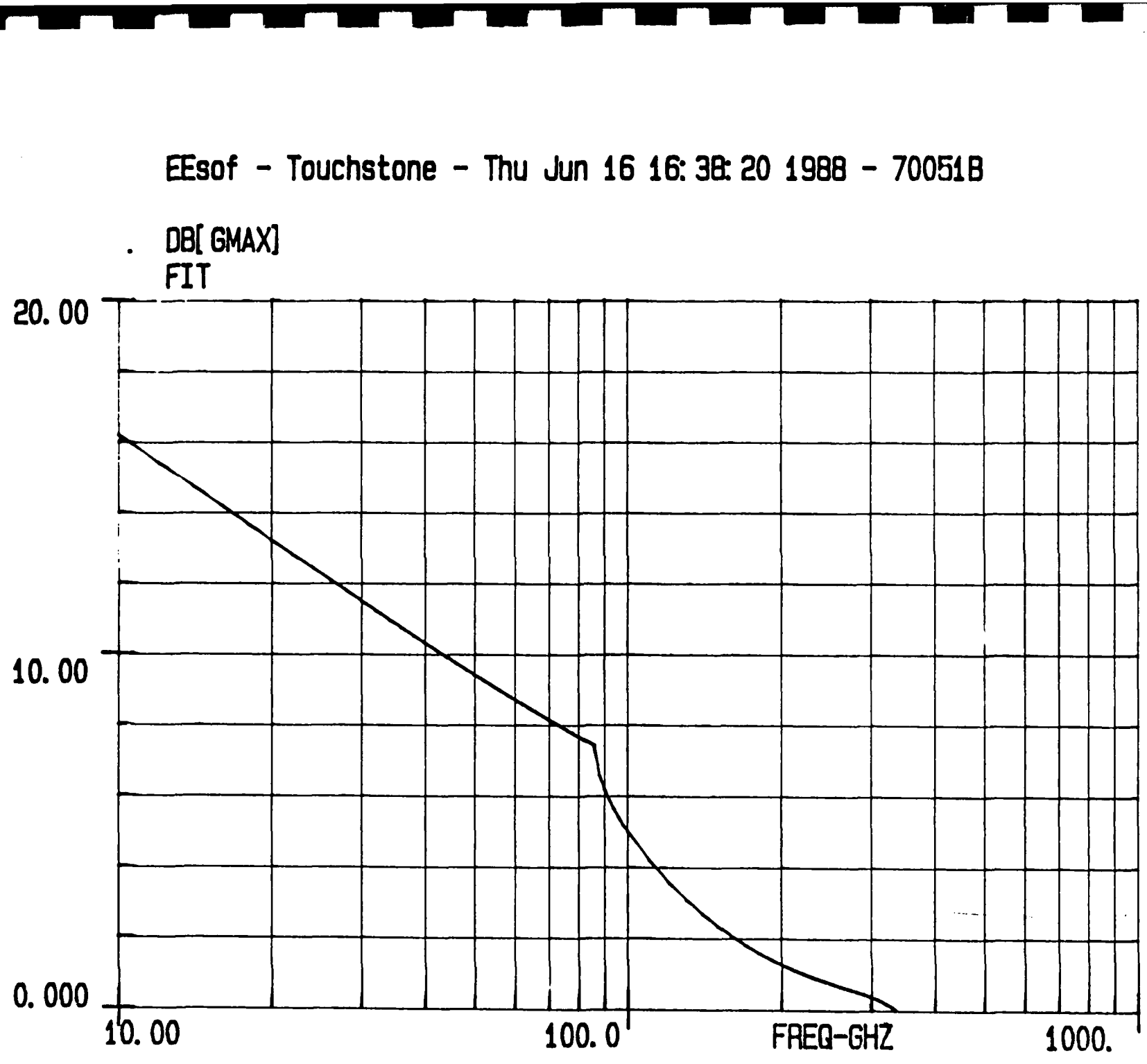




g_m = 1160 mS/mm

f_t = 210 GHz


AlInAs/GaInAs/InP HEMT
L_g = 0.1 μm, W = 75 μm
-6 db/octave
-12 db/octave
G_{ms}
U
G_{ma}
H_{21}
Gain, db
Frequency, GHz
30
25
20
15
10
5
0
10
20
30
50
70
100
200
300
500
1000

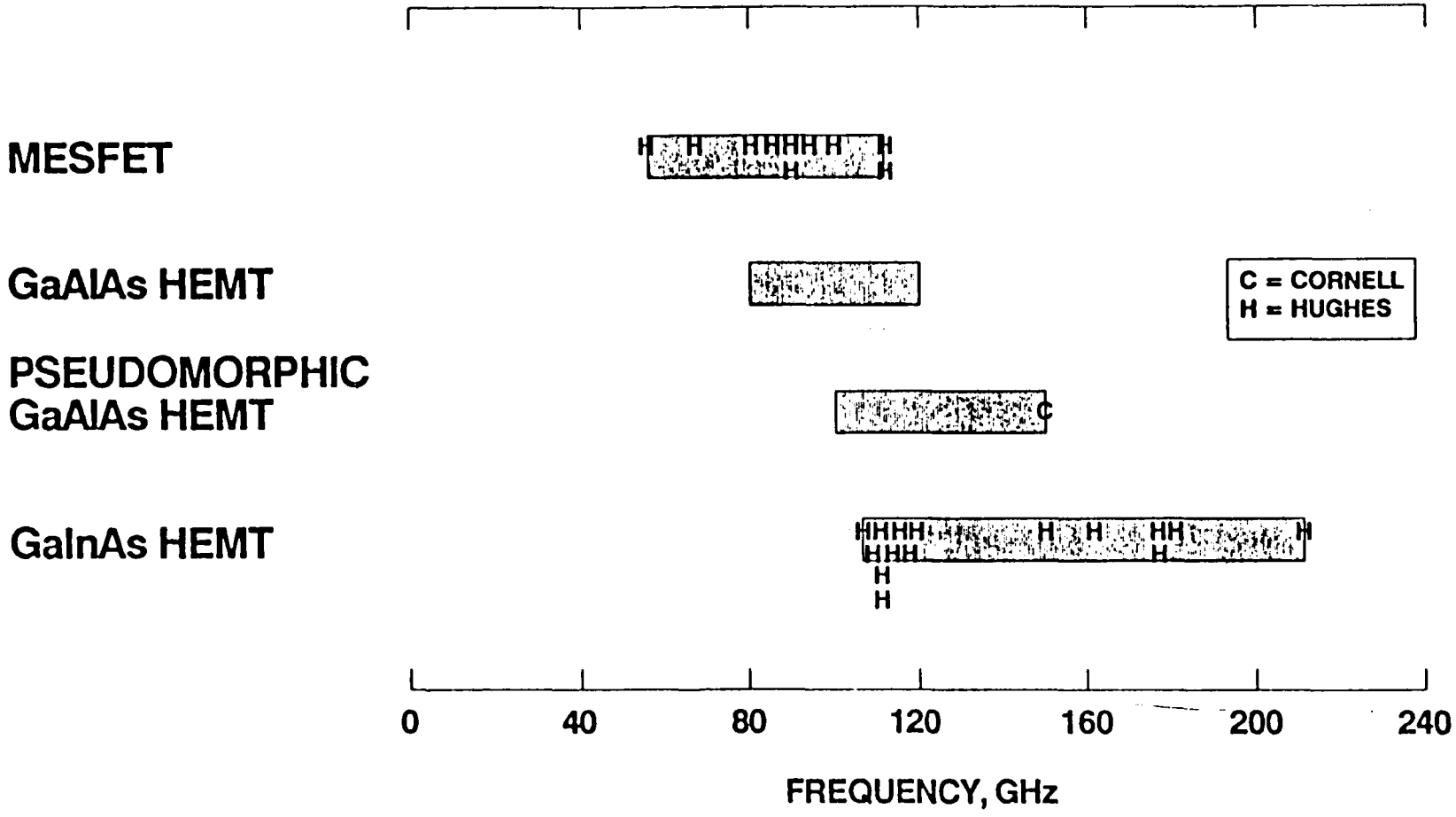

EEsof - Touchstone - Thu Jun 16 16:38:20 1988 - 70051B
DB[GMAX]
FIT
20.00
10.00
0.000
10.00
100.0
1000.
FREQ-GHZ

EXPERIMENTALLY MEASURED GAIN-BANDWIDTH PRODUCTS, F_t

HUGHES

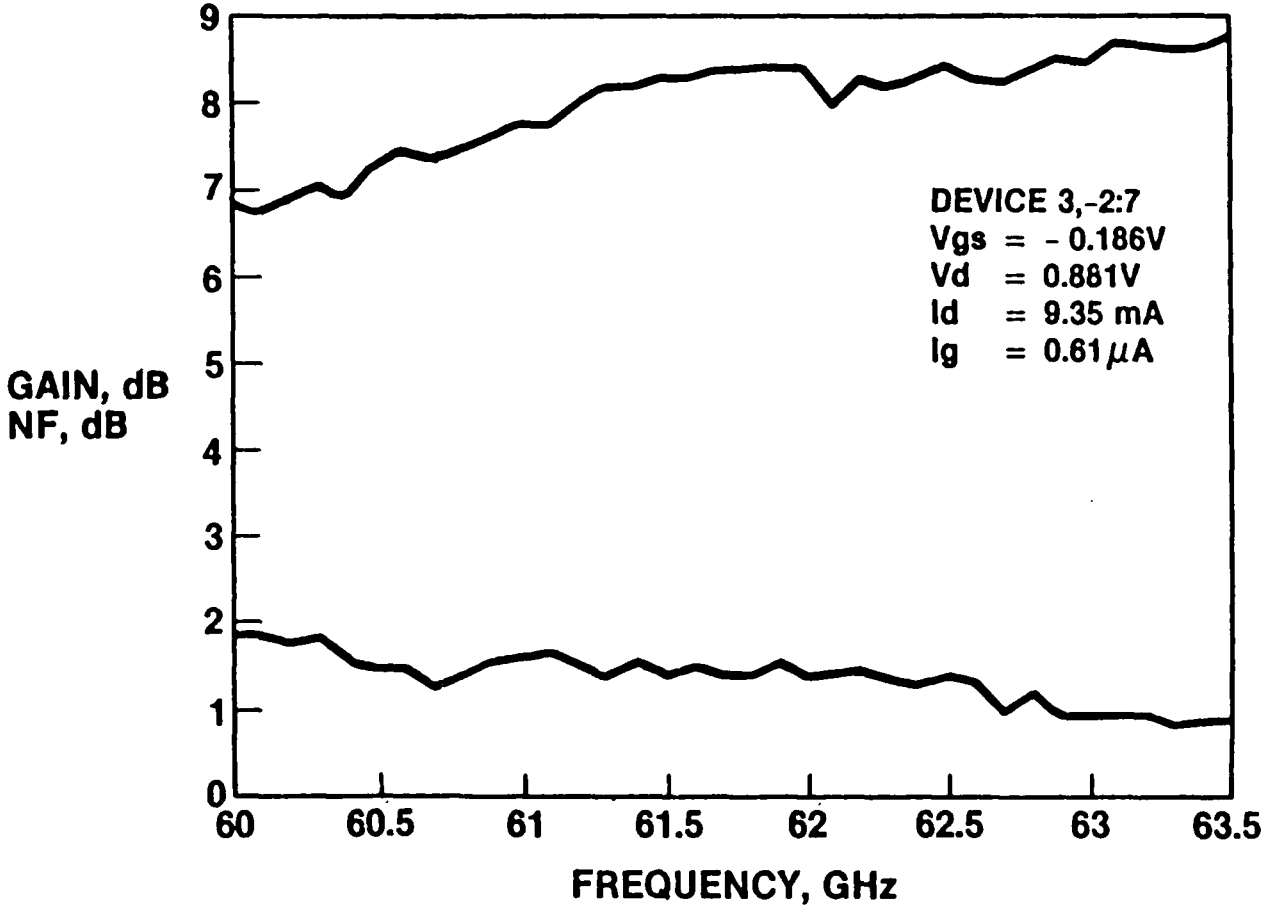
C8852-02-02

0.1 - 0.2 MICROMETER GATELENGTH



OCTOBER 1988

V-BAND AlInAs-GaInAs HEMT AMPLIFIER NOISE AND GAIN PERFORMANCE



Lg = 0.2μm

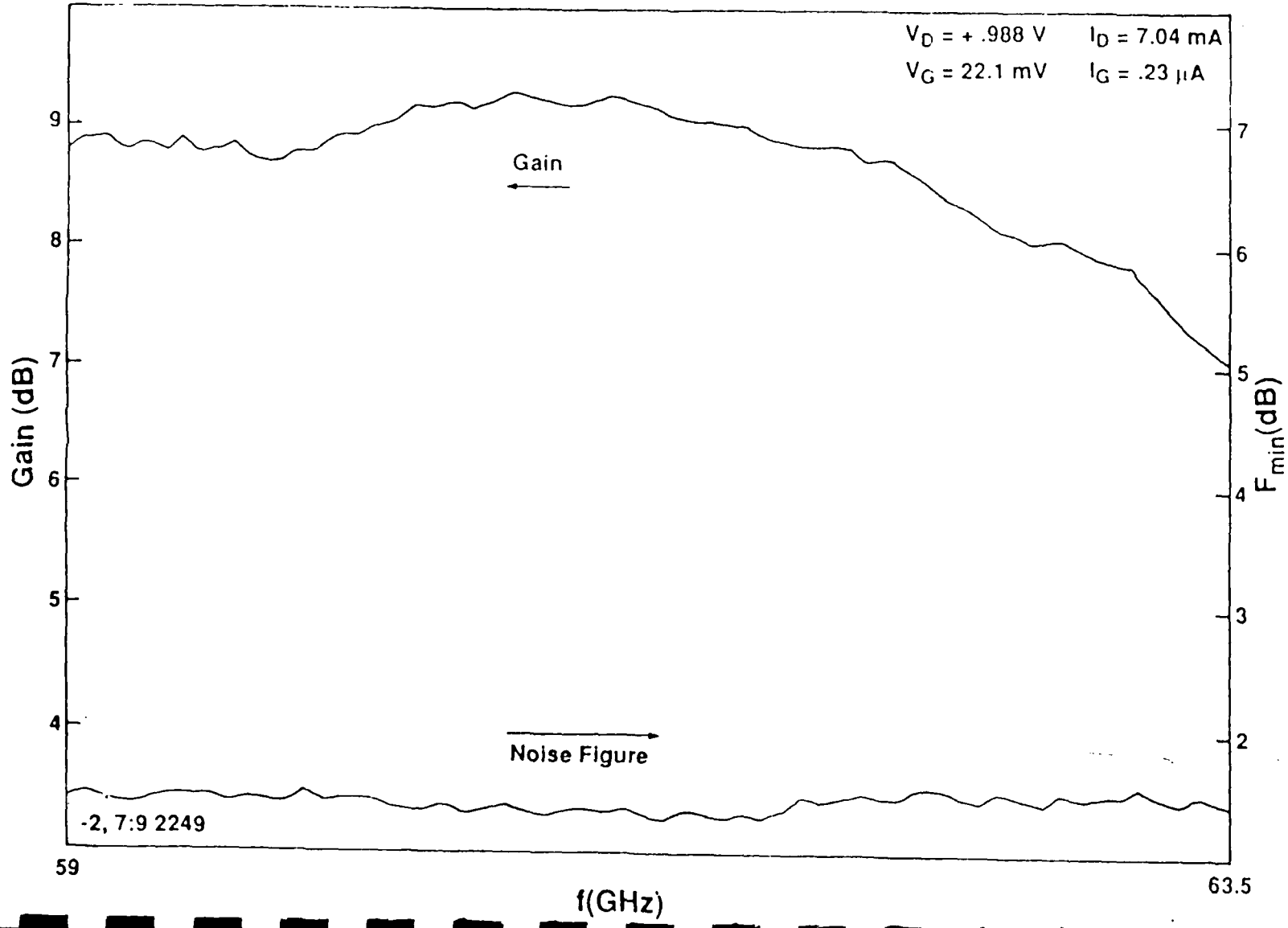
gm = 800 mS/mm

f_T = 130 GHz

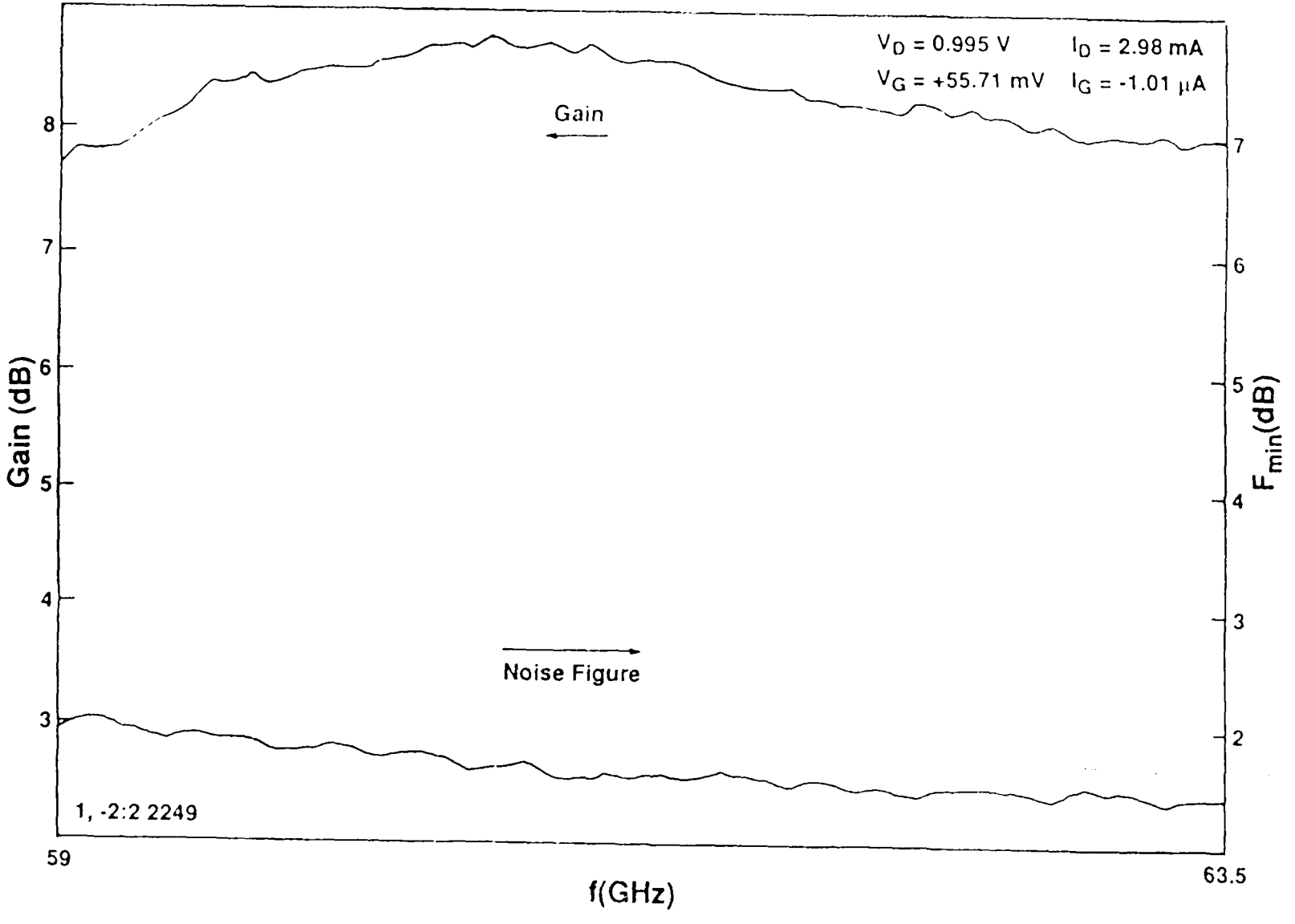
W = 50μm

AUGUST 1988

V-BAND NOISE PERFORMANCE OF LATTICE MATCHED $Al_{.48}In_{.52}As$ / $Ga_{.47}In_{.53}As$ HEMT AMPLIFIER



V-BAND NOISE PERFORMANCE OF PSEUDOMORPHIC $Al_{.48}In_{.52}As$ / $Ga_{.38}In_{.62}As$ HEMT AMPLIFIER



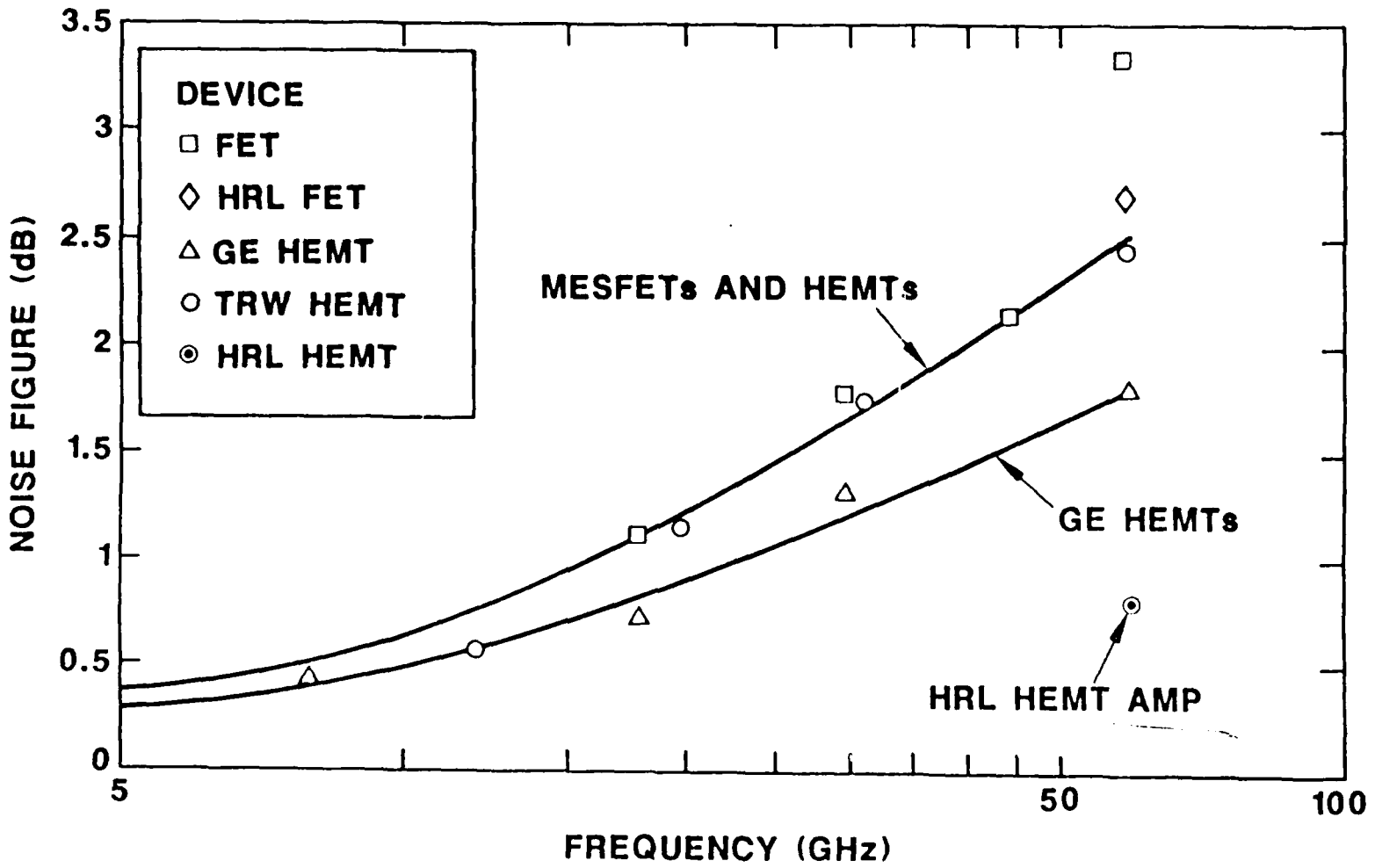
PROJECT 59

GaInAs HEMT LOW NOISE AMPLIFIER

HUGHES

18430-46

COMPARISON TO COMPETITION-1988



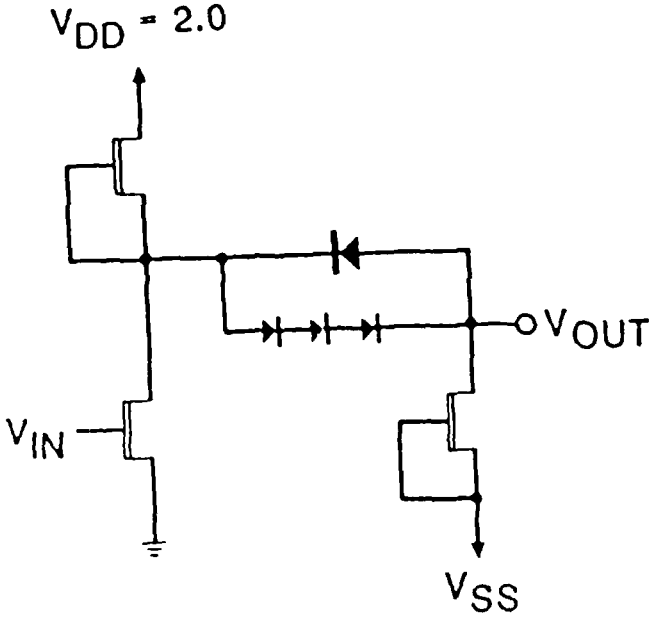
AUG 1988

CAPACITIVELY ENHANCED LOGIC INVERTER AND RING OSCILLATOR

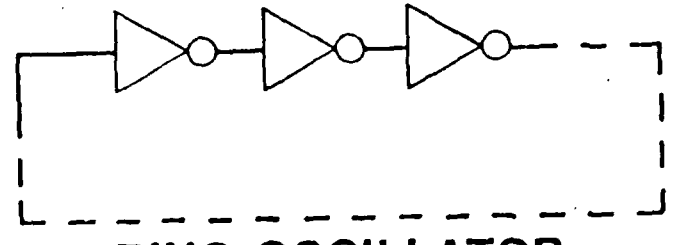
HUGHES

17772-3

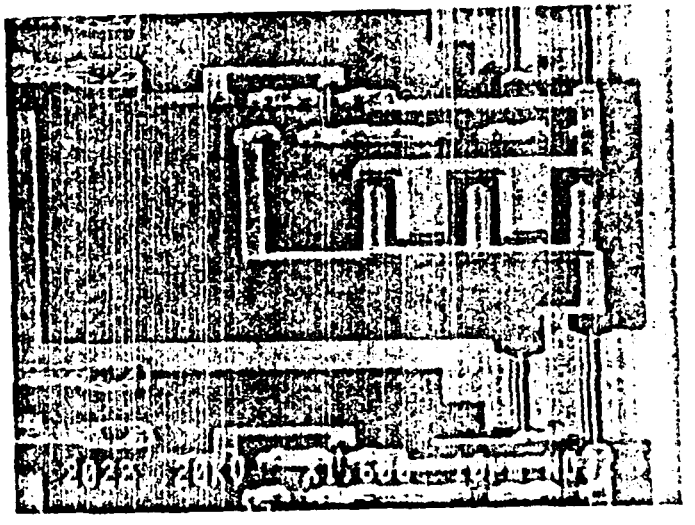
15392 2R58

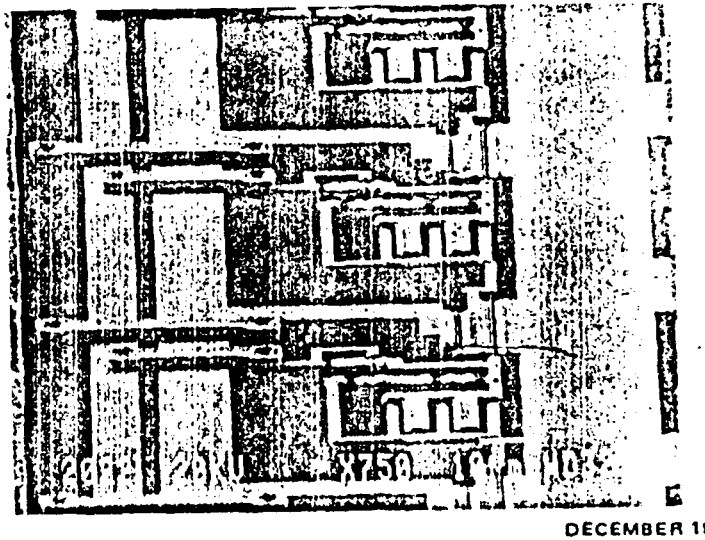


CEL INVERTER



RING OSCILLATOR



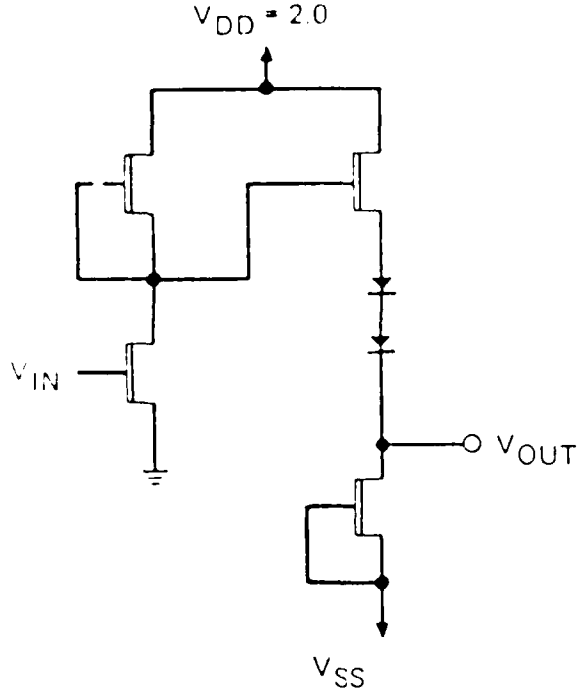


DECEMBER 1987

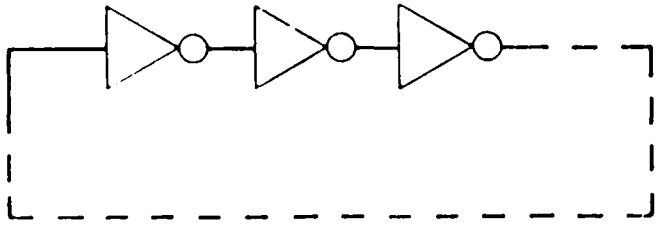
BUFFERED FET LOGIC INVERTER AND RING OSCILLATOR

HUGHES

15392 2R6A

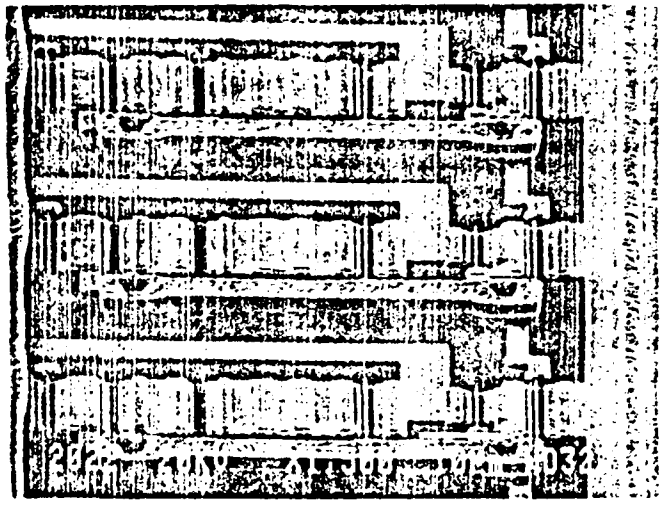


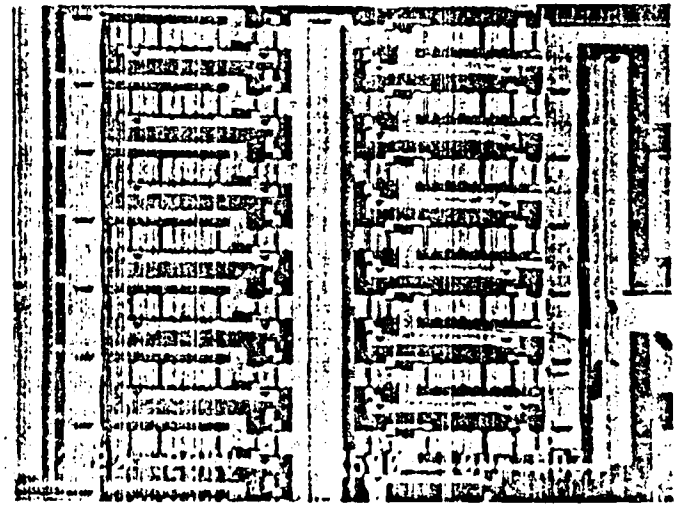
BFL INVERTER



RING OSCILLATOR

17772-2



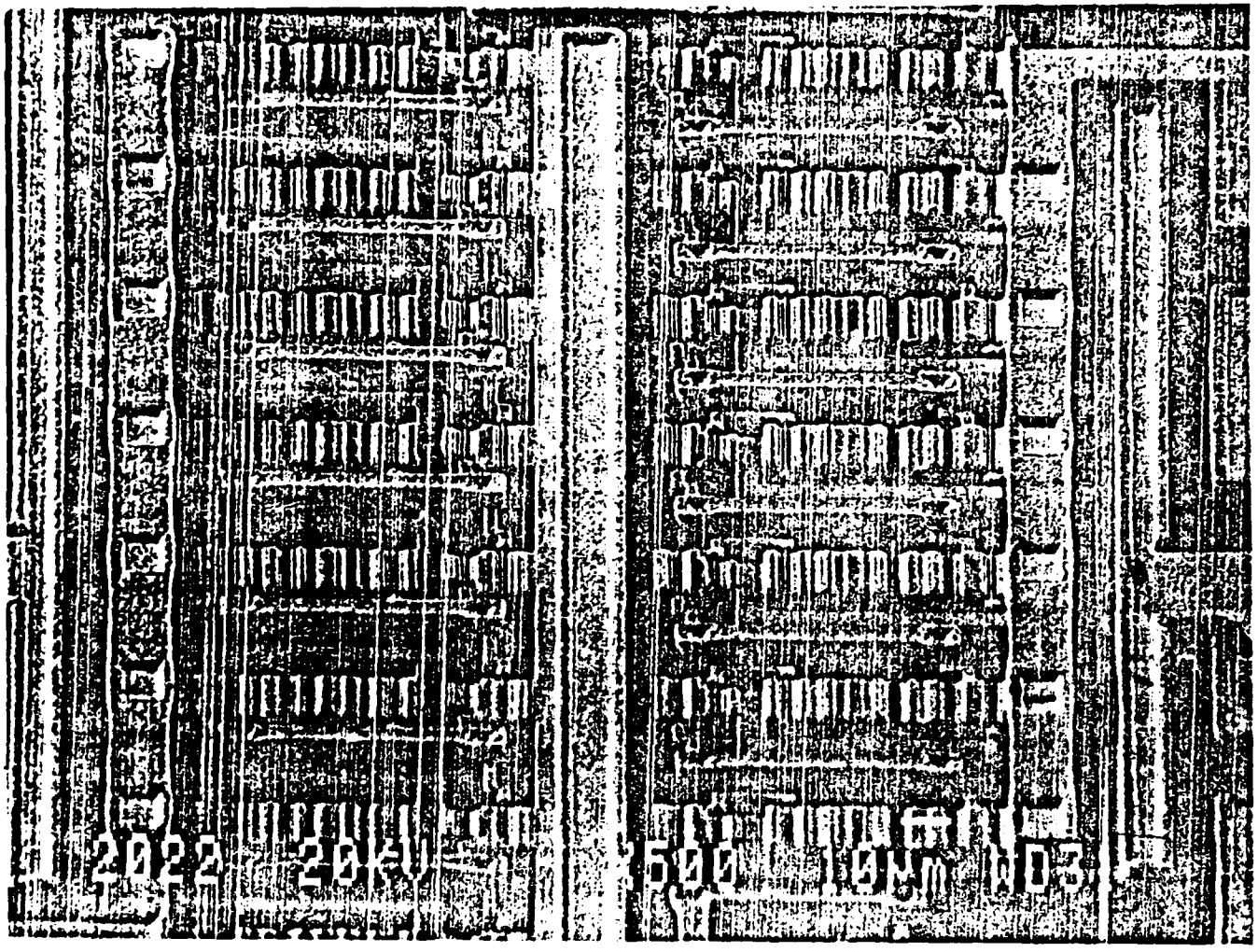


DECEMBER 1987

15 STAGE BFL RING OSCILLATOR IN 0.2 μm AlInAs–GaInAs HEMT TECHNOLOGY

HUGHES

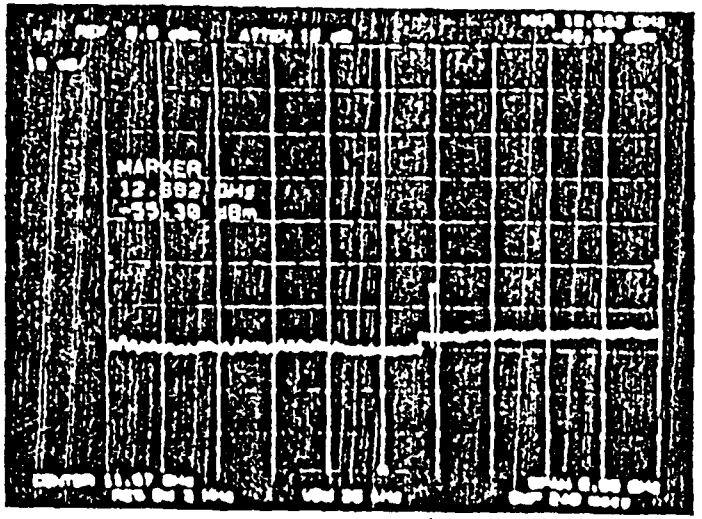
17772–1



DECEMBER 1987

AlInAs-GaInAs HEMT IC PERFORMANCE

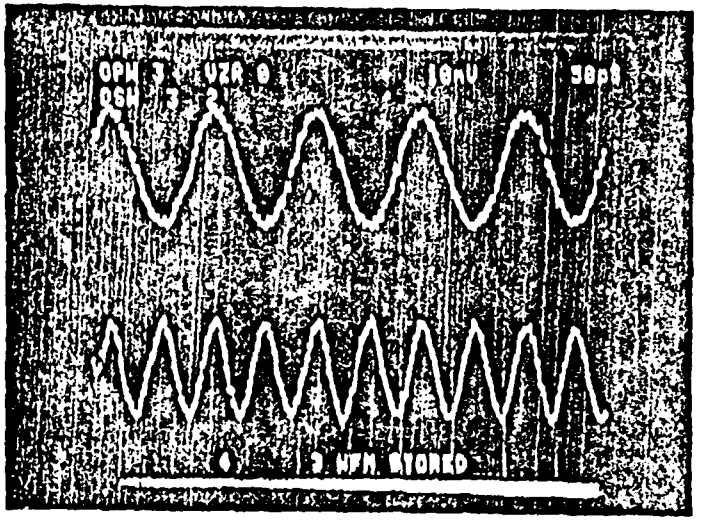
25.4 GHz OPERATION



$f_{ck/2}$ = 12.69 GHz

20 GHz OPERATION

C17902-9



CEL DIVIDER

F_{max} = 25.4 GHz

P_D = 63.8 mW

BFL DIVIDER

F_{max} = 25.2 GHz

P_D = 450 mW

RING OSCILLATOR RESULTS*

BFL τ_g = 9.26 ps @ 66.7 mW/GATE

CEL τ_g = 7.21 ps @ 24.5 mW/GATE

*REPORTED AT IEDM 1987

FEBRUARY 1988

FAN-OUT SENSITIVITY 1.4 ps/gate [BFL]

2.5 ps/gate [CEL]

CONCLUSIONS

- Pseudomorphic $Al_{.48}In_{.52}As$-$Ga_{.38}In_{.62}As$ HEMTs have demonstrated an extrinsic f_T of $>$ 200 GHz.

- Lattice matched and pseudomorphic HEMTs have comparable noise performance.

- With optimized epitaxial layer design an f_T of $>$ 250 GHz is expected.

- f_{max} is limited by device output conductance.

Measurement of Response of High Speed Tunneling Devices

T. C. McGill

California Institute of Technology
Pasadena, CA

MEASUREMENT OF RESPONSE OF HIGH SPEED TUNNLELING DEVICES

Principal Investigator: T. C. McGill, California Institute of Technology

DARPA ORDER 4833 ONR CONTRACT NO. N00014-84-C-0083

OBJECTIVE

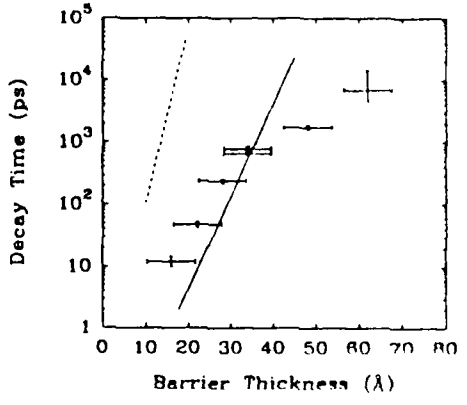
- Develop new and novel electronic devices
- Make appropriate measurements to characterize the high-speed device response

STATUS

- Fabricating tunnel device structures to order in MBE machine
- Perfected correlation technique for measuring decay of photoluminescence from quantum well
- Measured the response of photon-controlled electronic switches (PCE)
- Measured and reported the response of double barrier tunnel structures at speeds to 10ps
- Making measurements of bias dependence of decay of photoluminescence from quantum well
- Simulating the processes of making measurements

APPROACH

- Explore new phenomena potentially useful for making new devices
- Fabricate new device structures in MBE machine
- Develop and monitor techniques for measuring high speed devices
- Measure high-speed response using CPM laser with pulse width less than 300fs
- Simulate the measurement process



Decay times of the photoluminescence from a quantum well as a function of barrier thickness in double-barrier GaAs/AlAs tunnel structures. The solid line and dashed line are the theoretical values for the tunneling of electrons and heavy holes, respectively.

MEASUREMENTS OF RESPONSE OF HIGH SPEED TUNNELING DEVICES

by
T. C. McGill
California Institute of Technology
Pasadena, California 91125
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David Z. Ting *(Caltech)*

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A. T. Hunter *(Hughes Research Laboratories)*

R. B. Hammond *(Los Alamos National Laboratories)*

N. Politer *(Los Alamos National Laboratories)*

OUTLINE

I. WHAT AND WHY TUNNEL DEVICES?

   A. TWO-TERMINAL

   B. THREE-TERMINAL

II. SPEED OF TUNNEL DEVICES

III. PREVIOUS MEASUREMENTS

IV. OUR MEASUREMENTS

V. FUTURE PLANS

WHAT

AND

WHY

TUNNEL STRUCTURES

WHY TUNNEL DEVICES

A. HETEROJUNCTIONS VERSUS DOPING

- CHARACTERISTIC DIMENSIONS FOR DOPING CONTROL IS 1000Å
- HETEROJUNCTIONS GIVE SMALLER CHARACTERISTIC DIMENSIONS 10Å

B. POTENTIAL FOR VERY HIGH DENSITY WITH REASONABLE BIASES ETC.

C. SMALL CHARACTERISTIC DIMENSIONS OF TUNNEL DEVICES GIVE POTENTIAL FOR VERY HIGH SPEED

TWO-TERMINAL TUNNEL DEVICES

Negative Resistance in Double Barriers

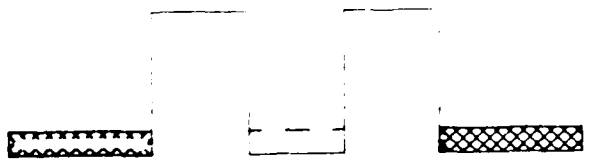
I. First approximation:

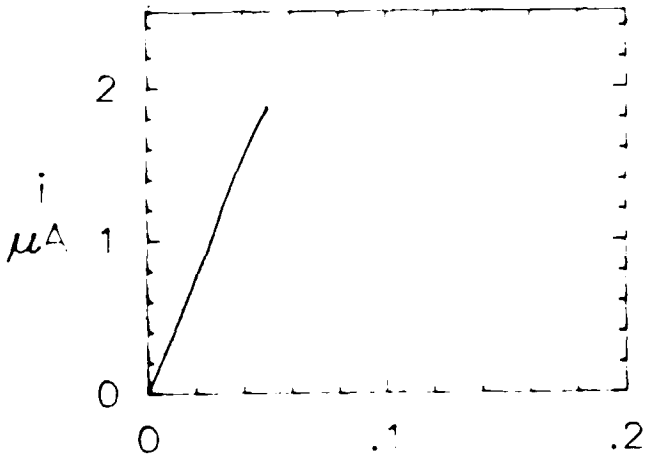
A. Energy conservation:

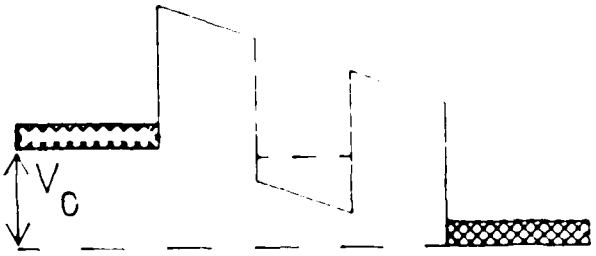
$$E = \hbar^2 k^2 / 2m$$

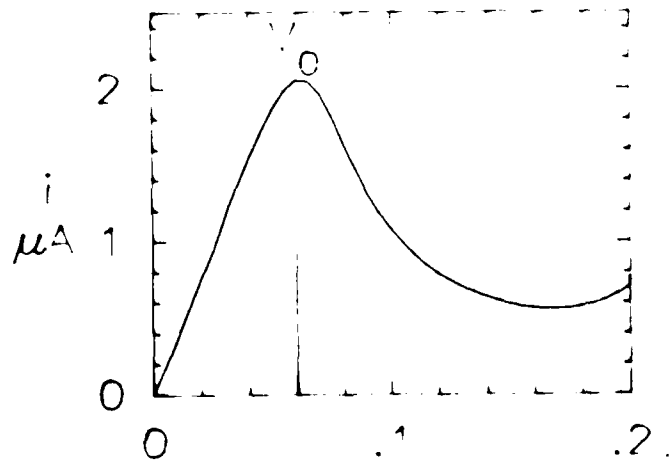
B. Parallel momentum ($k_{\parallel}$) conservation:

$$k = k_{\parallel} + k_{\perp}$$

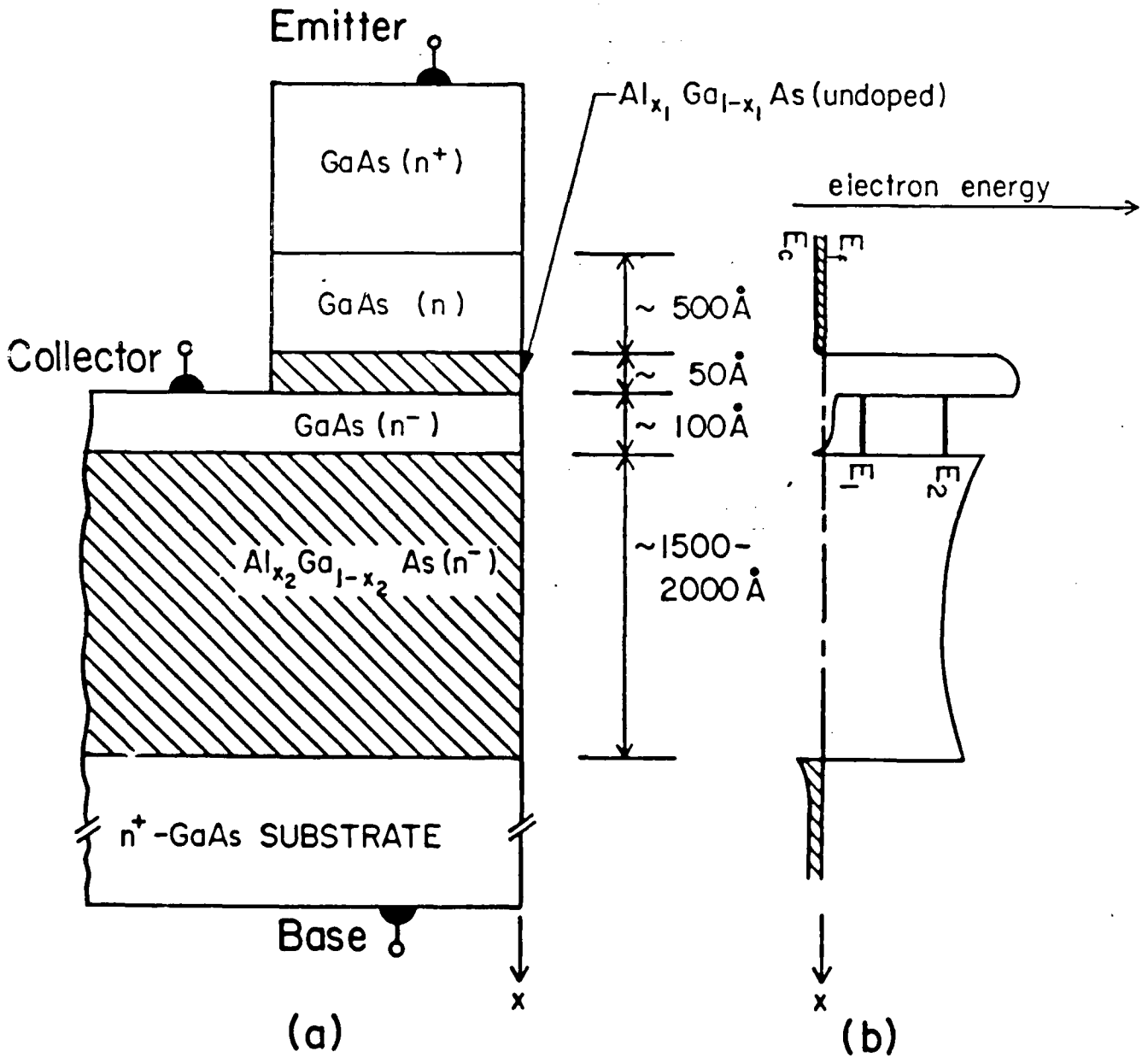








THREE-TERMINAL DEVICES


Emitter
GaAs (n+)
GaAs (n)
Collector
GaAs (n−)
Alx2Ga1−x2As (n−)
n+-GaAs SUBSTRATE
Base
x
(a)
Alx1 Ga1−x1 As (undoped)
~ 500Å
~ 50Å
~ 100Å
~1500-
2000 Å
electron energy
Ec
E1
E2
x
(b)

Inverted base-collector tunnel transistors

A. R. Bonnefoi, D. H. Chow, and T. C. McGill
T. J. Watson, Sr., Laboratory of Applied Physics, California Institute of Technology, Pasadena, California 91125

(Received 1 July 1985; accepted for publication 7 August 1985)

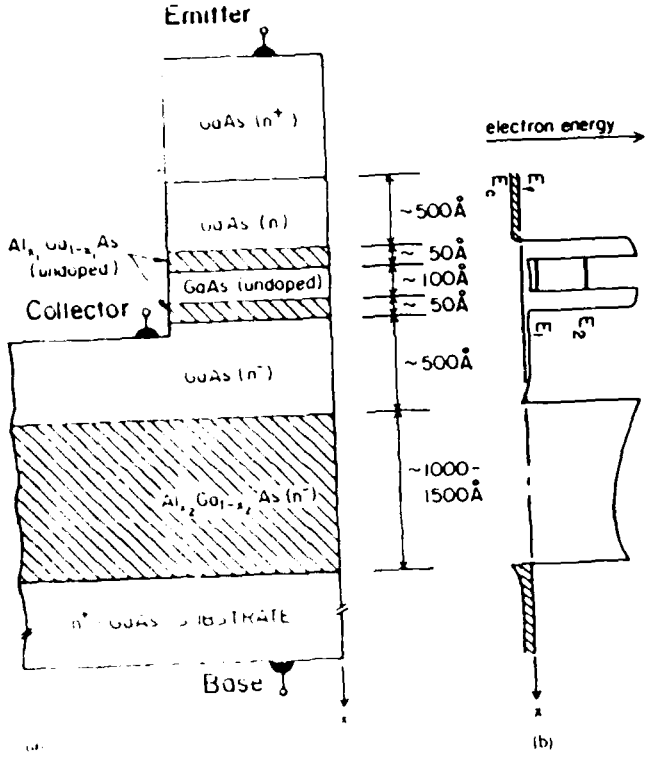


FIG. 3. Schematic diagrams (not to scale) of (a) a cross section of the proposed negative resistance Stark effect transistor (NERSET); (b) the conduction-band edge at equilibrium as a function of position in the x direction (perpendicular to the layers).

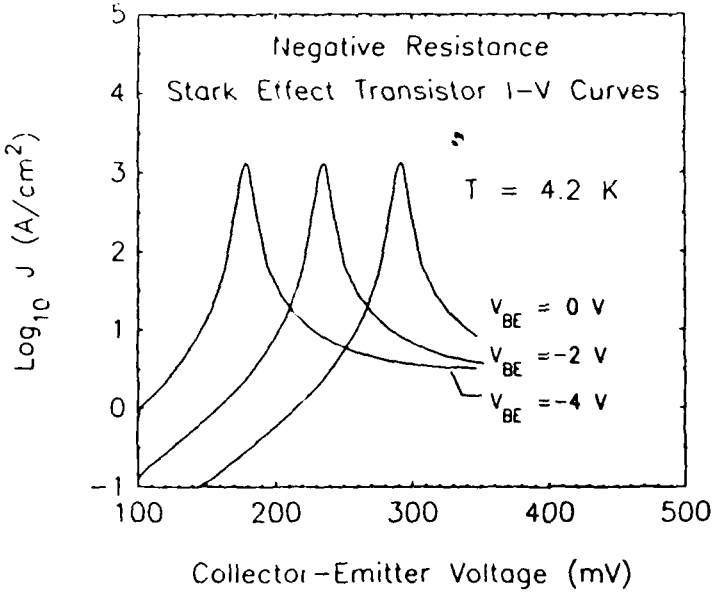


FIG. 4. Calculated current-voltage characteristics for the negative resistance Stark effect transistor (NERSET). The tunnel barriers are 20-Å-thick $Al_{0.6}Ga_{0.4}As$ layers and the well a 50-Å-thick GaAs layer. The conduction-band offset is taken to be 0.5 eV.

Inverted base-collector tunnel transistors

A. R. Bonnefoi, D. H. Chow, and T. C. McGill
T. J. Watson, Sr., Laboratory of Applied Physics, California Institute of Technology, Pasadena, California 91125

(Received 1 July 1985; accepted for publication 7 August 1985)

395

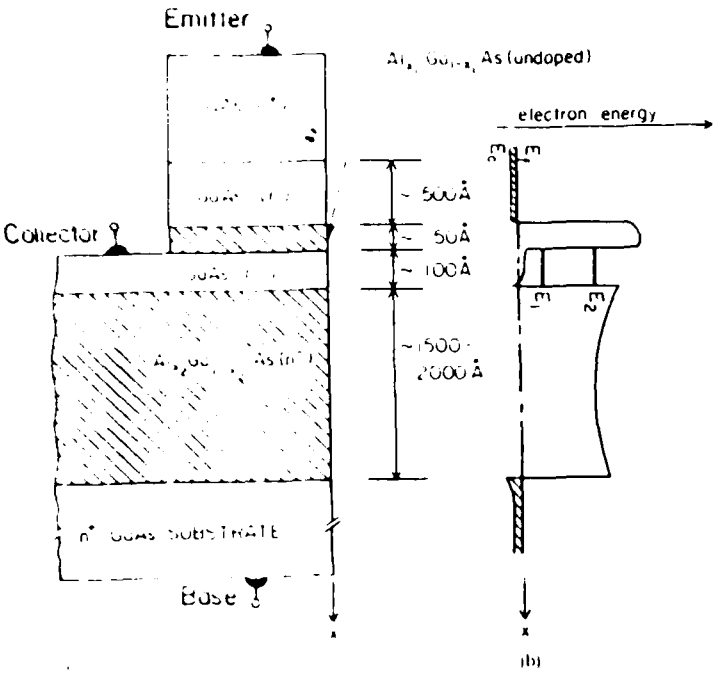


FIG. 1. Schematic diagrams (not to scale) of (a) a cross section of the proposed Stark effect transistor (SET); (b) the conduction-band edge at equilibrium as a function of position in the x direction (perpendicular to the layers).

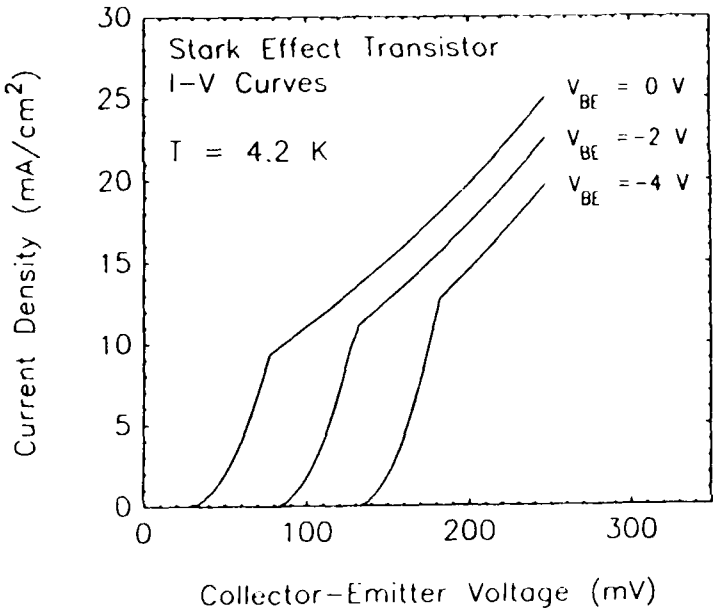


FIG. 2. Calculated current-voltage characteristics for the Stark effect transistor (SET). The barriers are pure AlAs, 50 and 1000 Å thick, respectively. The well is a 50-Å-thick GaAs layer. The conduction-band offset is taken to be 0.96 eV.

Negative transconductance via gating of the quantum well subbands in a resonant tunneling transistor

Fabio Beltram, Federico Capasso, Serge Luryi, Sung-Nee G. Chu, Alfred Y. Cho, and Deborah L. Sivco
AT&T Bell Laboratories, Murray Hill, New Jersey 07974

(Received 25 February 1988; accepted for publication 9 May 1988)

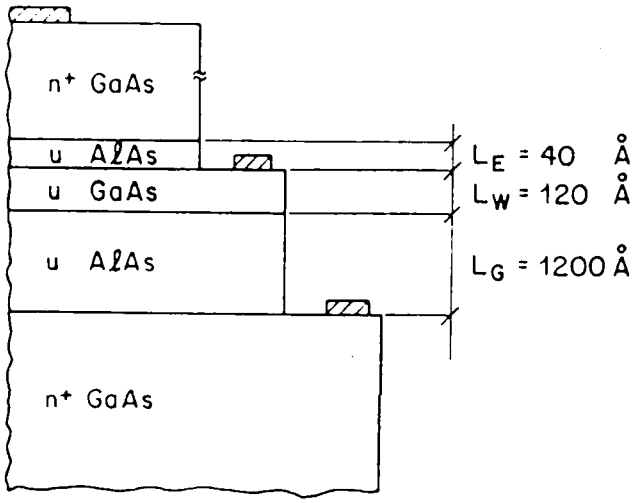


FIG. 1. Schematic cross section of the resonant tunneling transistor.

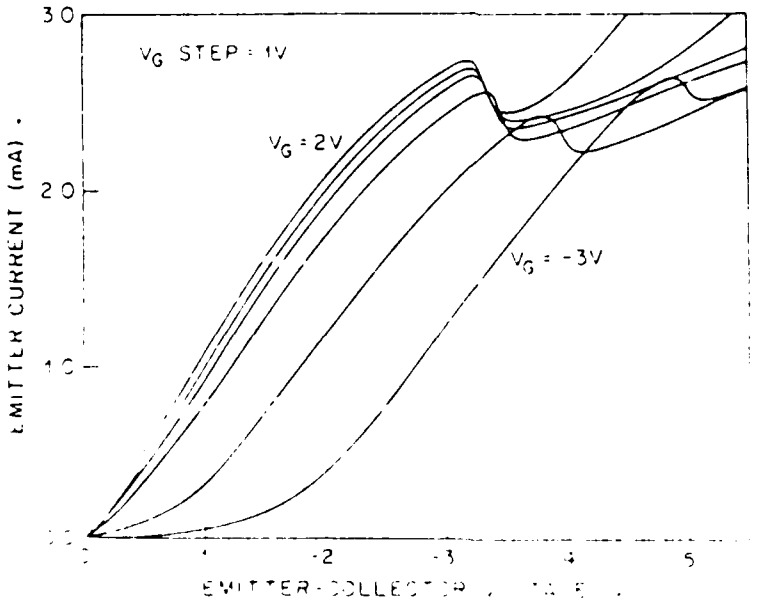
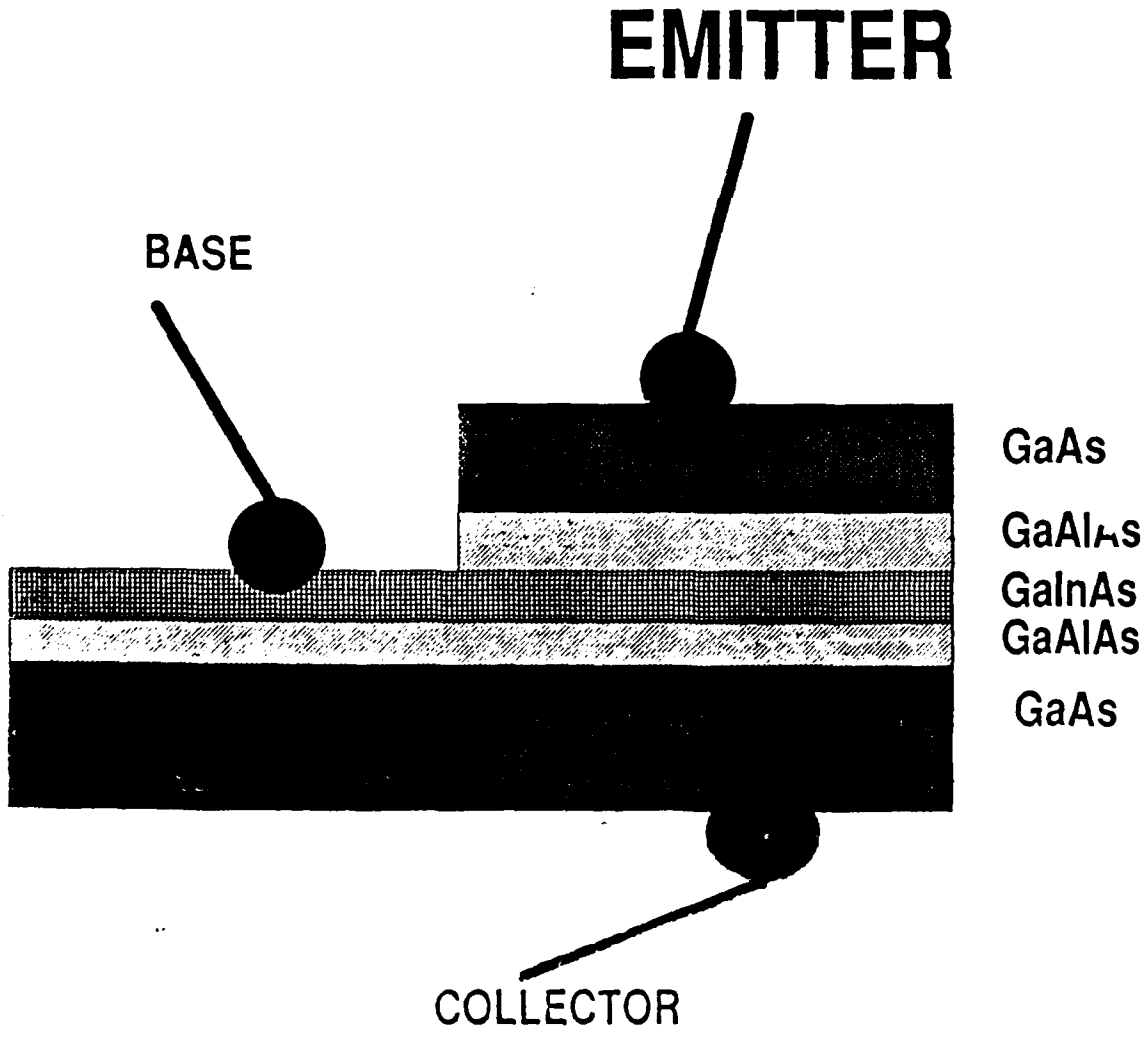


FIG. 2. Common-collector characteristics of the resonant tunneling transistor [illegible] measurements were performed at 4 K.

TEXAS INSTRUMENTS

THREE-TERMINAL DEVICE



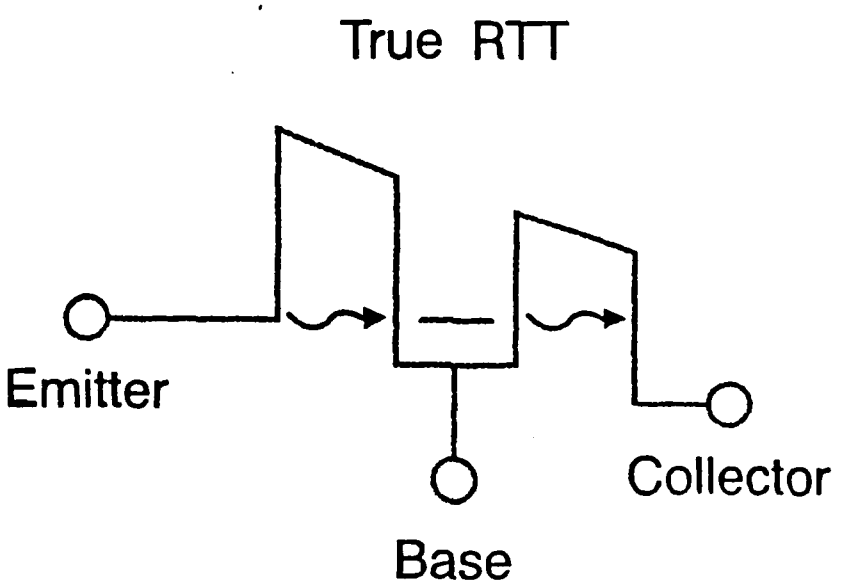
RESONANT TUNNELING TRANSISTORS (RTT)

Pseudo RTT

- Resonant tunneling diode structures
- Inserted in bipolar or FET devices
- Series combination
- Developed by others

True RTT

- Double barrier single well
- Direct contact to well for base
- Modulate resonance condition
- In development at TI
- Unipolar version needs no depletion layers
- Scalable well below 0.25μm geometries



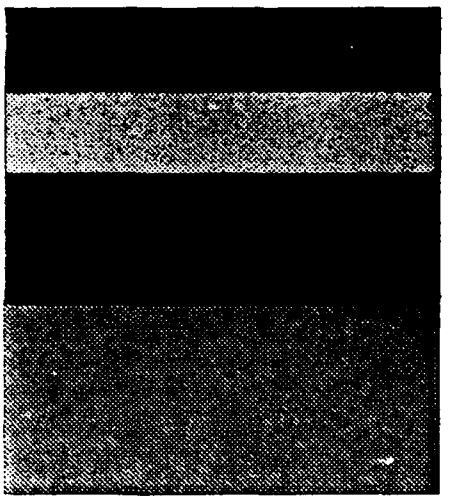
Si-Ge
HETEROJUNCTION
BIPOLAR TRANSISTOR

n-Si emitter

p-$Si_{0.85}Ge_{0.15}$base

n-Si collector

Si Substrate



- **Wide-bandgap emitter suppresses hole current**
- **Strain splitting of conduction bands in SiGe imporves electron transport in base**

HJBT
Beta= 400
F_T =100GHz

Standard Si
Beta=100
F_T=20GHz

SPEED OF TUNNELING DEVICES

A. TUNNELING DEVICES ARE VERY FAST-CHARACTERISTIC TIMES IN THE 100×10^{-15} SECOND RANGE

B. TUNNELING DEVICES ARE SLOWER WITH CHARACTERISTIC TIMES IN THE 10^{-12} SECOND RANGE

C. TUNNEL TIME OF ELECTRONS

TUNNELING TIMES

ON THE BASIS OF TWO OUT OF THREE "VOTES" IN FAVOR OF YOUR MANUSCRIPT, I AM INCLINED TO ACCEPT IT FOR PUBLICATION. BEFORE I DO SO, I WOULD LIKE TO HAVE YOUR ASSURANCE THAT YOU AND YOUR CO-AUTHORS HAVE CONSIDERED THE CRITICISMS CAREFULLY AND ARE SATISFIED THAT THEY ARE NOT VALID. I AWAIT YOUR REPLY WITH INTEREST.

F. E. Myers, Editor JAP December 8, 1966

K. K. Thornber, T. C. McGill, and C. A. Mead, J. Appl. Phys. **38**, 2384 (1967).

TUNNELING TIMES

τ_T

J. R. Barker's CLASSIFICATION

A. SCATTERING TIME GROUP

- DECAY OF METASTABLE STATES TIME INDEPENDENT PERTURBATION THEORY
- TUNNELING TIME VARIES INVERSELY AS TRANSITION MATRIX ELEMENT

$$\tau_T \sim \frac{1}{Transition\ Matrix\ Element}$$

- EQUIVALENT TO RC TIME CONSTANT

B. DWELL TIME GROUP

- PROBABILITY DENSITY IN TUNNELING REGION
- INCIDENT CURRENT FLUX
- TUNNELING TIME IS RATIO

$$\tau_T \sim \frac{PROBABILITY\ DENSITY}{INCIDENT\ CURRENT}$$

TUNNELING TIMES

(CONTINUED)

C. SEMI-CLASSICAL TIME GROUP

- PARTICLE IN BARRIER DESCRIBED BY AN IMAGINARY WAVE VECTOR

$$k_{IMAGINARY} = \sqrt{\frac{2m^* \Delta E}{\hbar^2}}$$

- TUNNELING TIME IS THE ASSOCIATED VELOCITY DIVIDED INTO BARRIER THICKNESS (D)

$$\tau_T = \frac{m^* D}{\hbar k_{IMAGINARY}}$$

D. PHASE TIME GROUP

- CONSIDER THE ENERGY DEPENDENCE OF PHASE SHIFT OF THE TRANSMISSION COEFFICIENT $\eta(E)$
- TUNNELING TIME IS DERIVATIVE OF THIS PHASE SHIFT WITH ENERGY

$$\tau_T = \hbar \frac{d\eta}{dE}$$

TUNNELING TIMES

J. R. Barker's CLASSIFICATION

A. SCATTERING TIME GROUP

B. DWELL TIME GROUP

C. SEMI-CLASSICAL TIME GROUP

D. PHASE TIME GROUP

PREVIOUS WORK

MEASUREMENTS OF TUNNEL RESPONSE ON TWO-TERMINAL DEVICES

A. MIXING EXPERIMENTS 2.5THz (SOLLNER)

B. PL DECAY EXPERIMENTS (SAKAKI AND CO-WORKERS)

C. ELECTRO-OPTIC TECHNIQUE (MOUROU AND CO-WORKERS)

Tunneling Escape Rate of Electrons From Quantum Well in Double-Barrier Heterostructures

M. Tsuchiya, T. Matsusue, and H. Sakaki

Institute of Industrial Science, University of Tokyo, Minato-ku, Tokyo 106, Japan

(Received 30 June 1987)

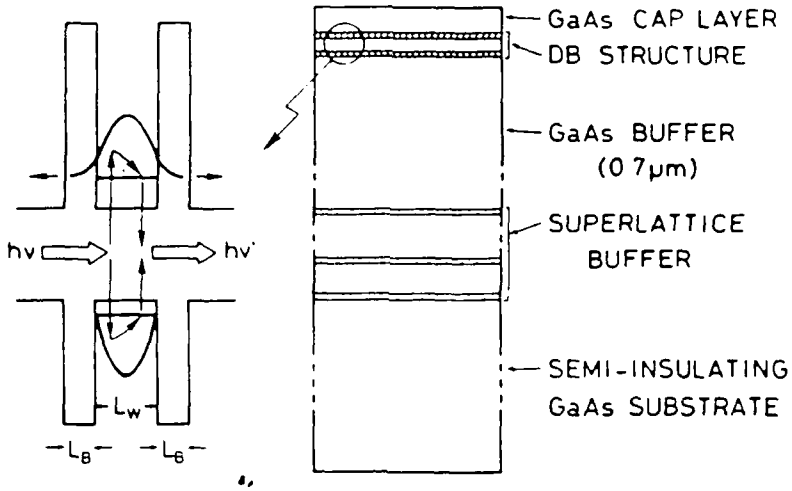


FIG. 1. Schematic structure of AlAs-GaAs-AlAs double-barrier samples used for the present study.

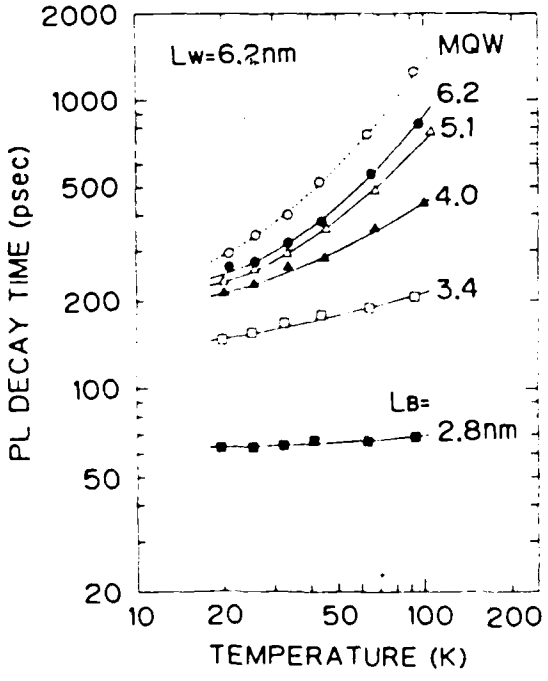


FIG. 4. The temperature dependence of PL decay time with arrier thickness as a parameter.

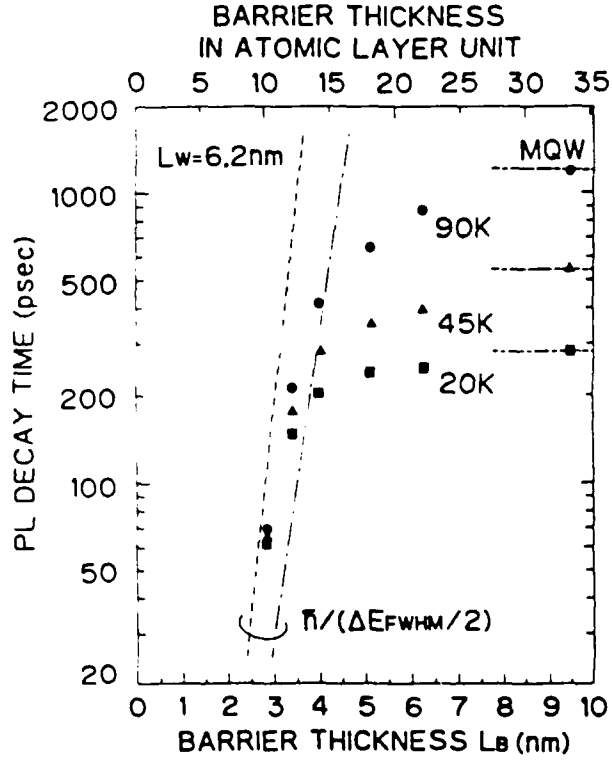


FIG. 5. PL decay times plotted as functions of barrier thickness L_B. When $L_B < 4$ nm, the tunneling escape process is dominant. Broken line and dot-dashed line are theoretical lifetimes calculated by $\hbar/(\Delta E_{FWHM}/2)$, with the assumption that the barrier heights are 1.36 and 0.96 eV, respectively.

PL DECAY EXPERIMENTS

A. TIME LIMITED TO 60ps IN THE SAKAKI EXPERIMENTS

B. MAJOR ERROR IN THE THEORETICAL EXPRESSION CLAIMED TO AGREE

C. DIFFICULTY IN INTERPRETING EXPERIMENT

- EXCITING LASER PRODUCES ELECTRONS AND HOLES
- ELECTRONS AND HOLES DECAY WITH VERY DIFFERENT TIMES
- CHARGING OF WELL DUE TO TUNNELING OF ELECTRON LEAVING HOLE BEHIND

Picosecond switching time measurement of a resonant tunneling diode

J. F. Whitaker and G. A. Mourou
Laboratory for Laser Energetics and Department of Electrical Engineering, University of Rochester, 250 East River Road, Rochester, New York 14623-1299

T. C. L. G. Sollner and W. D. Goodhue
Lincoln Laboratory, Massachusetts Institute of Technology, Lexington, Massachusetts 02173

(Received 7 March 1988; accepted for publication 1 June 1988)

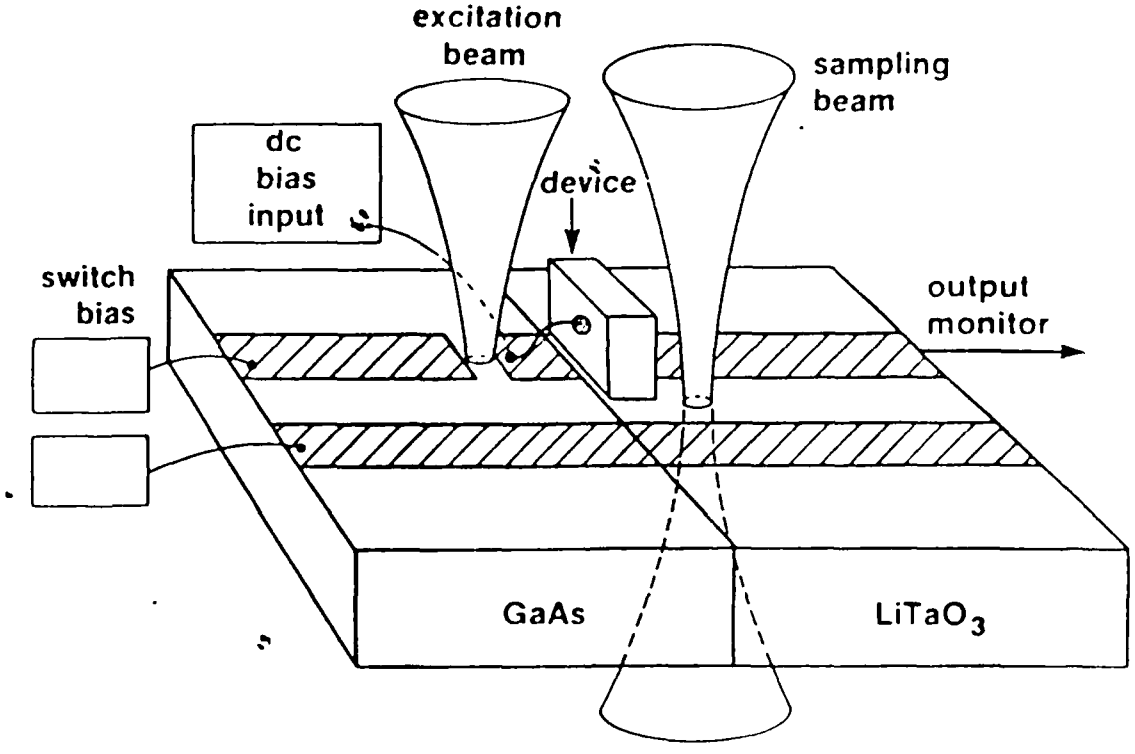


FIG. 1. Experimental configuration for electro-optic sampling of resonant-tunneling diode. A 12-μm-diam wire with a 1 μm tip contacts a mesa on the resonant-tunneling diode chip.

Picosecond switching time measurement of a resonant tunneling diode

J. F. Whitaker and G. A. Mourou
Laboratory for Laser Energetics and Department of Electrical Engineering, University of Rochester, 250 East River Road, Rochester, New York 14623-1299

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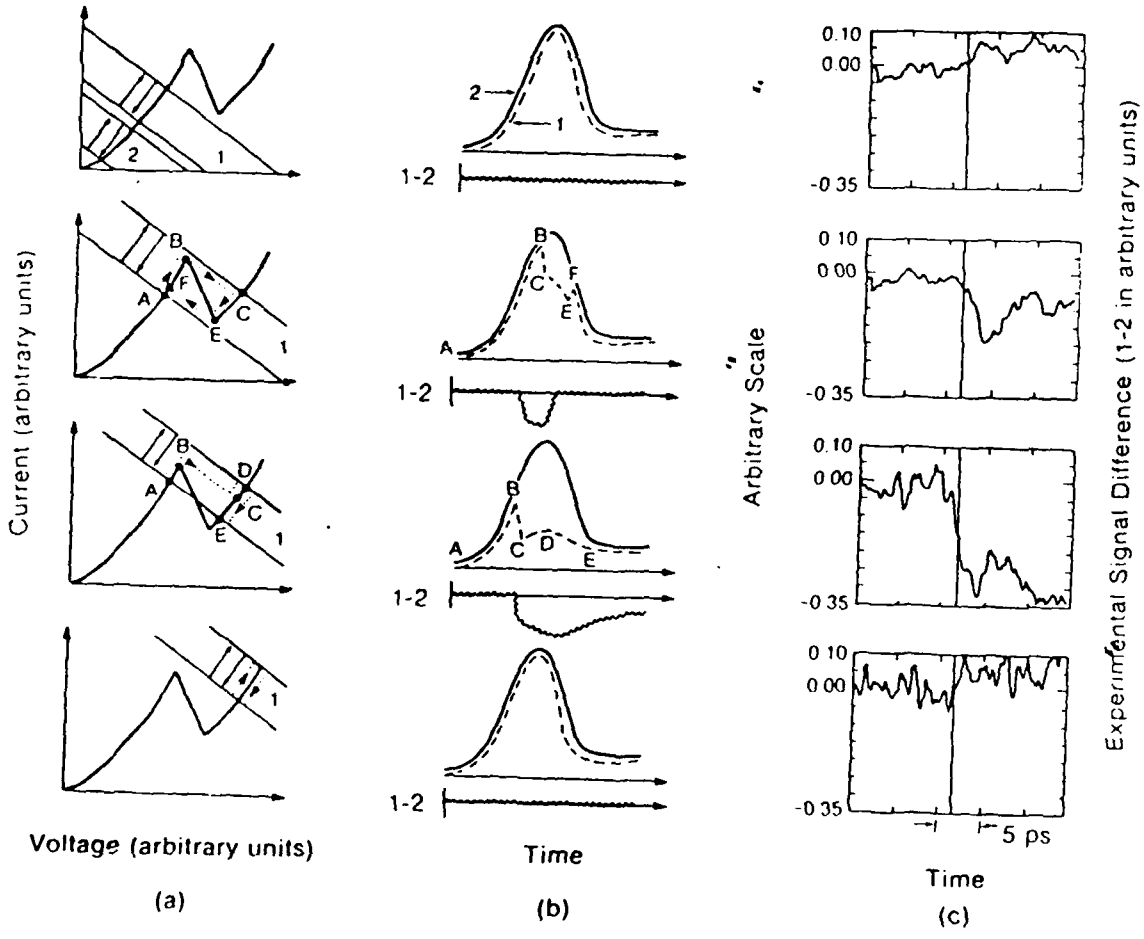


FIG. 3. Resonant-tunneling diode switching as a function of bias: (a) *I-V* curve with load lines, (b) analytic representation of waveforms resulting from movement of load lines in (a) and the difference of these waveforms, and (c) experimental signal difference.

ELECTRO-OPTIC TECHNIQUE

A. DIFFICULTY OF INTERPRETING DATA

B. NOISY SIGNAL

C. RESULTS IN DISAGREEMENT WITH SAKAKI

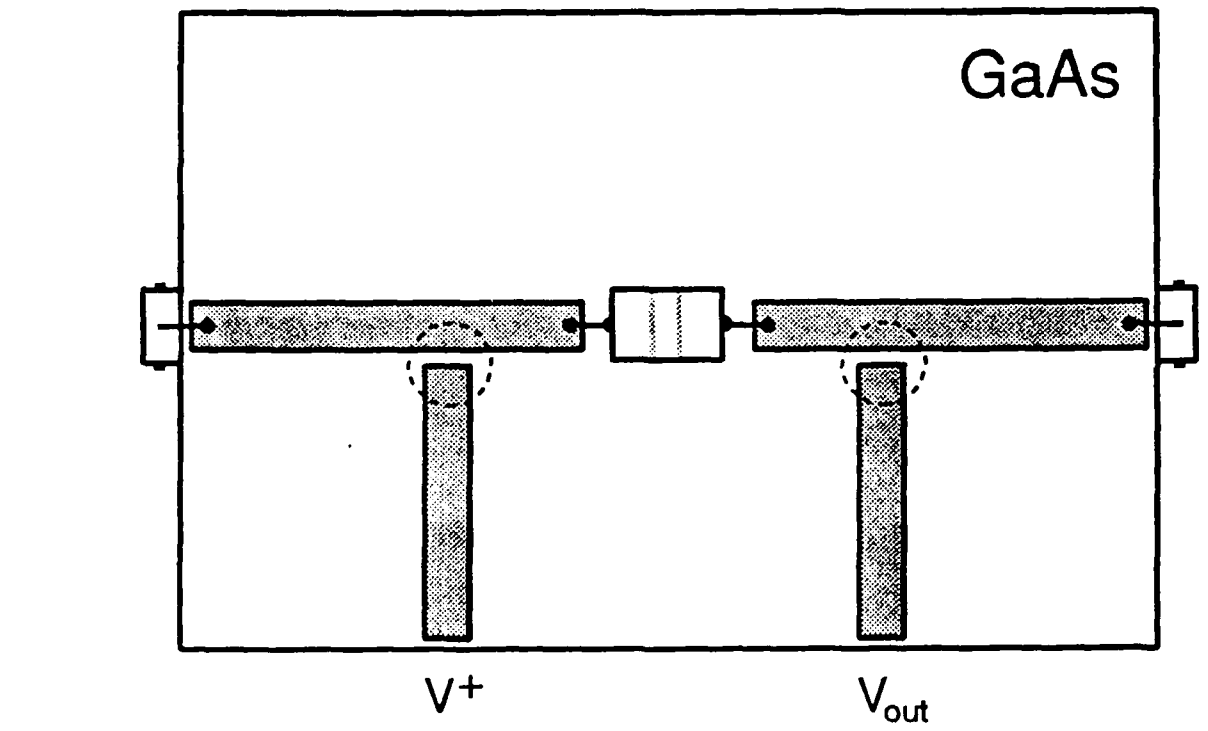
- SWITCHING TIME MEASURED 2ps
- SAKAKI DATA GIVES 8ps FOR THIS STRUCTURE

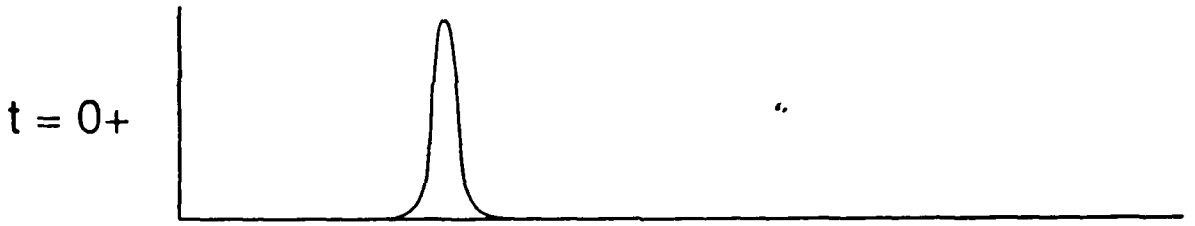
OUR WORK

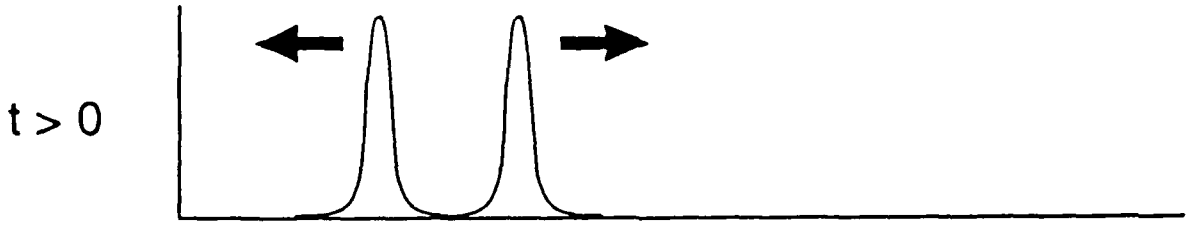
A. USE OF PCE'S FOR MEASUREMENTS

B. USE OF CORRELATION TECHNIQUE FOR MEASURING PL DECAY

- LIMITED BY LASER SPEED
- TIMES SUBSTANTIALLY BELOW 10ps


GaAs
V+
V_{out}


t = 0+

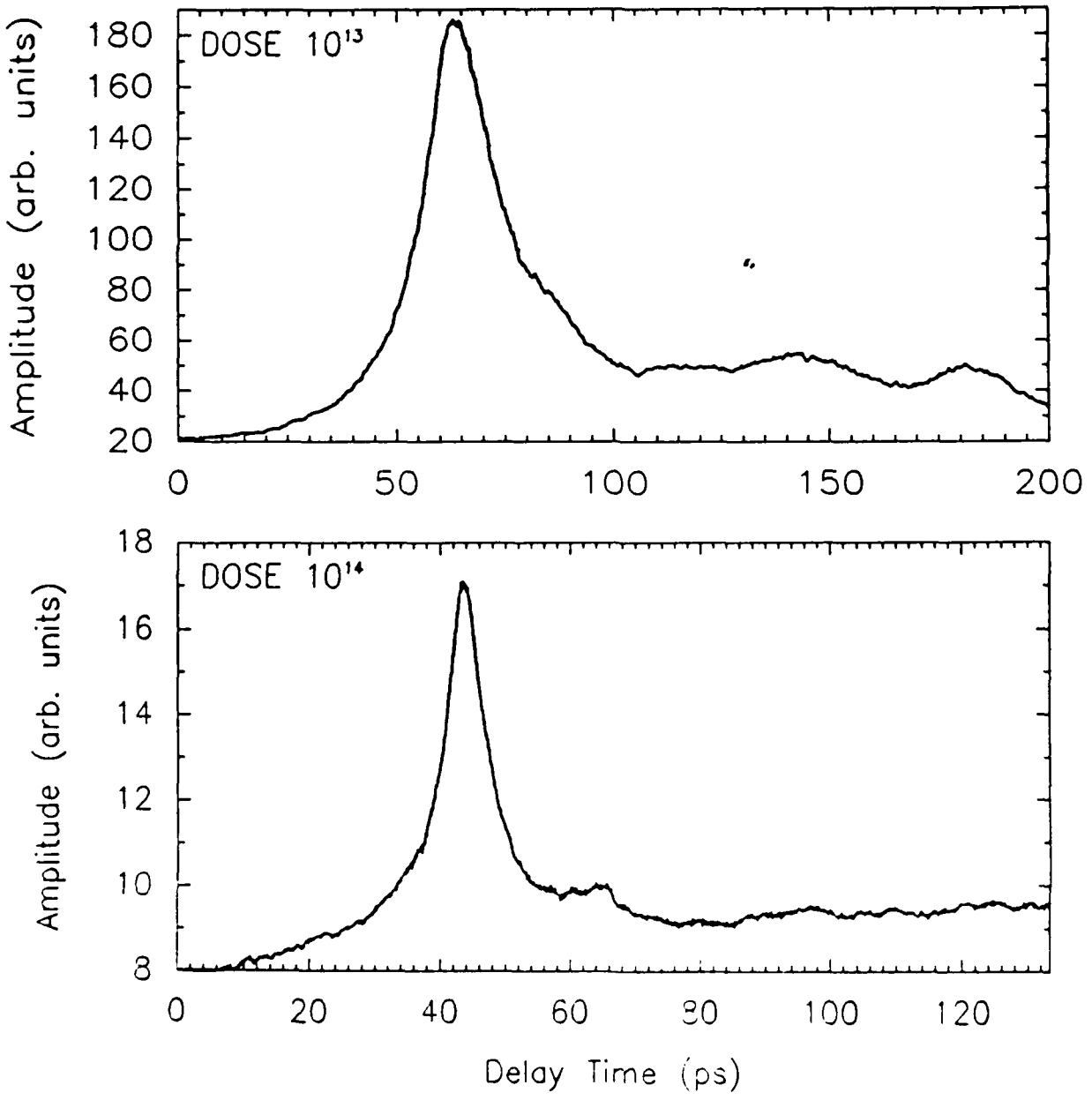

t > 0

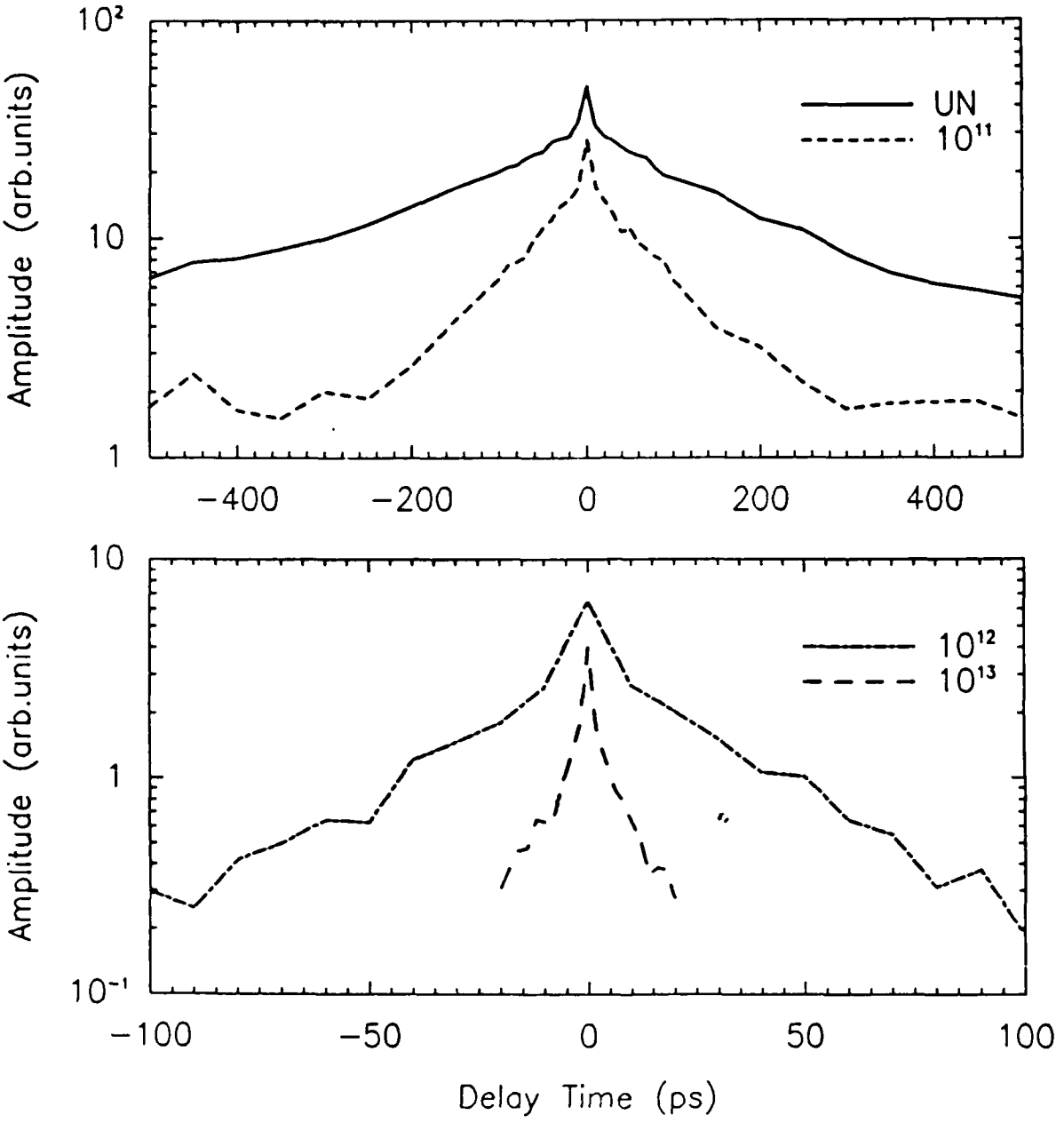
t >> 0

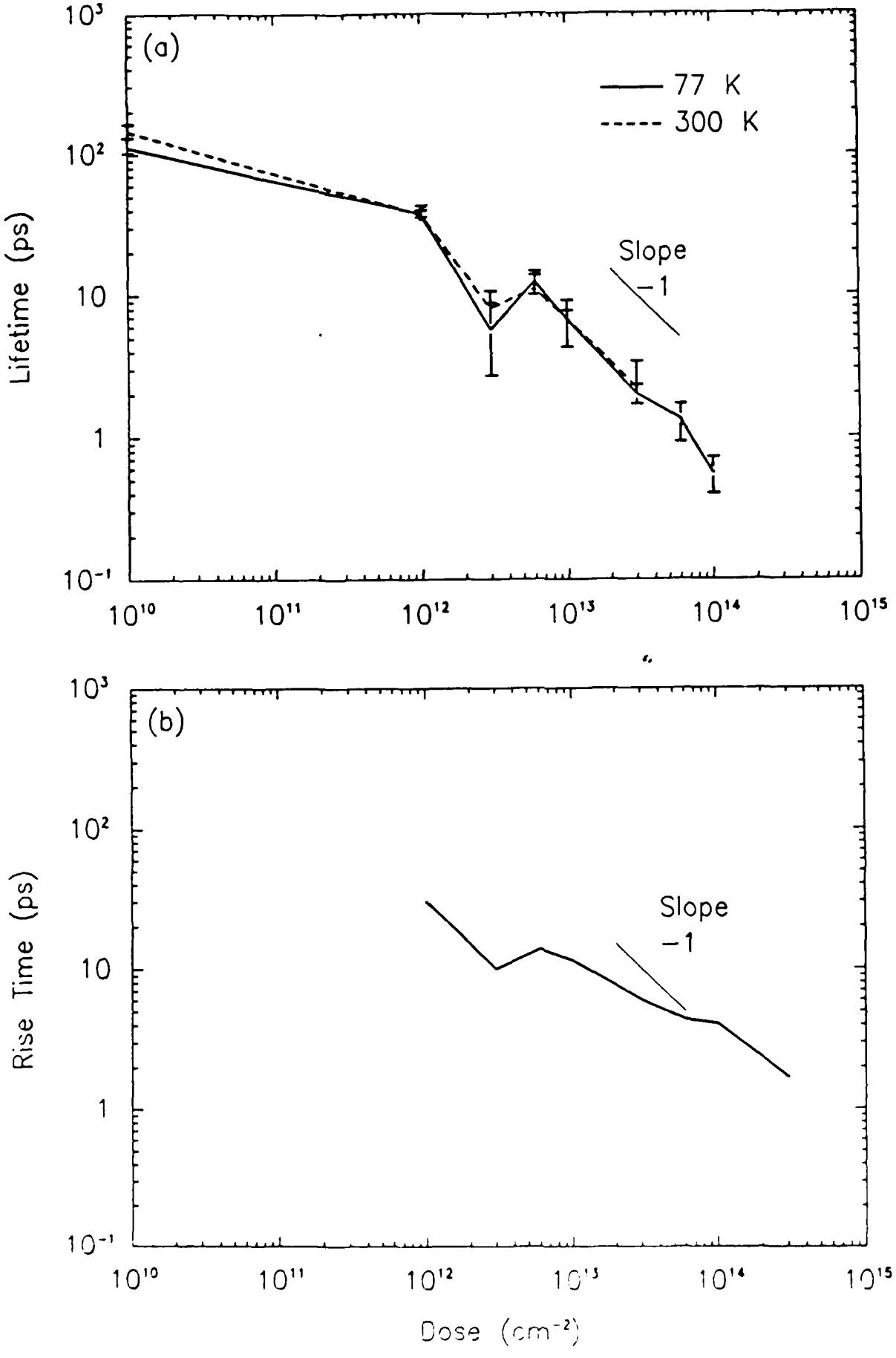
PCE MEASUREMENTS

A. DESIGNED STRUCTURES AND SIMULATED PROPAGATION OF HIGH-SPEED PULSE ON STRIP-LINES

B. CHARACTERIZED PCE MATERIAL


DOSE 10^{13}
Amplitude (arb. units)
180
160
140
120
100
80
60
40
20
0
50
100
150
200
DOSE 10^{14}
Amplitude (arb. units)
18
16
14
12
10
8
0
20
40
60
80
100
120
Delay Time (ps)

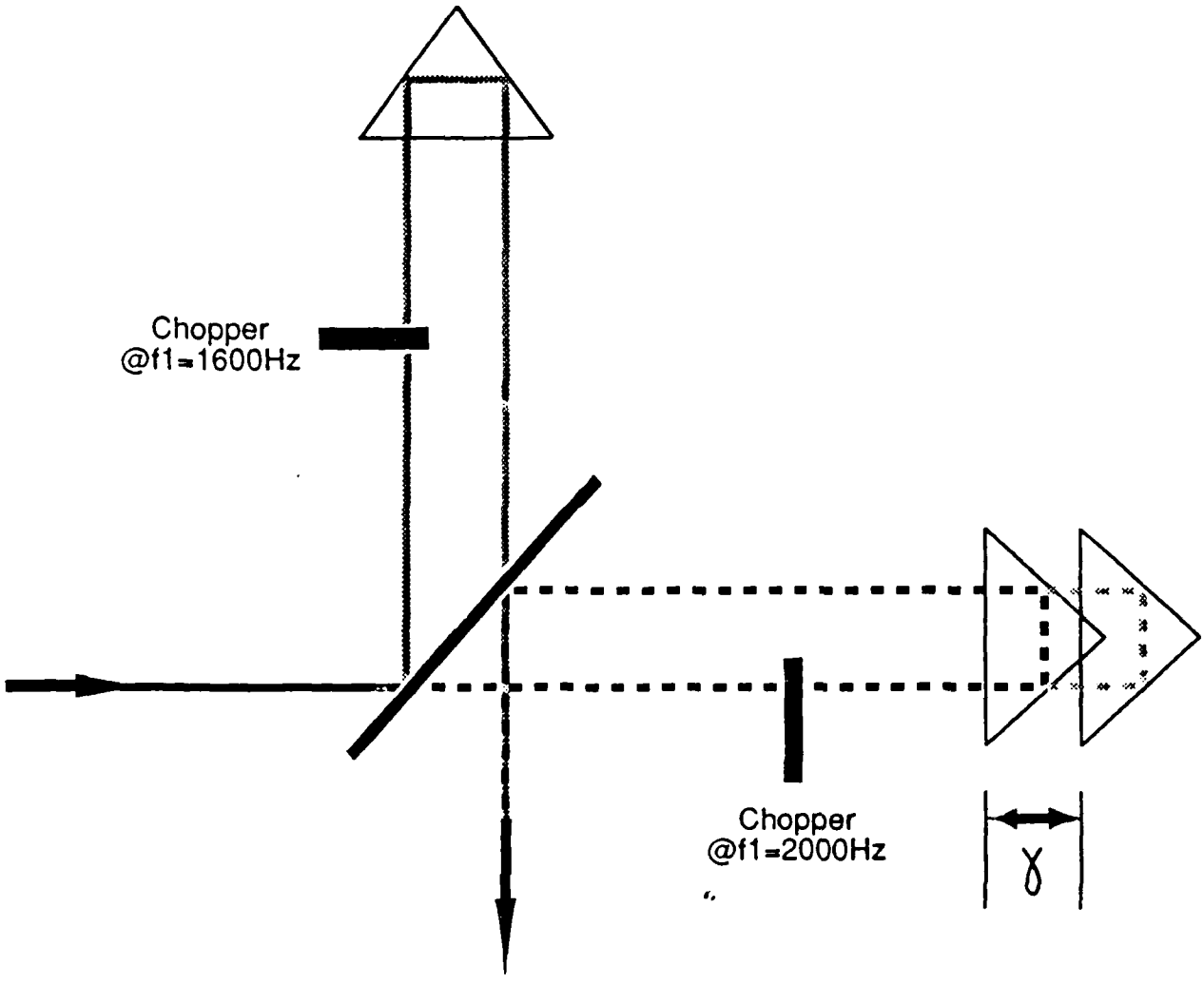

10^2
10
1
Amplitude (arb.units)
UN
10^{11}
−400
−200
0
200
400
10
1
10^{-1}
Amplitude (arb.units)
10^{12}
10^{13}
−100
−50
0
50
100
Delay Time (ps)


(a)
77 K
300 K
Slope
−1
Lifetime (ps)
10^3
10^2
10
1
10^{-1}
10^{10}
10^{11}
10^{12}
10^{13}
10^{14}
10^{15}
(b)
Slope
−1
Rise Time (ps)
Dose (cm^{-2})

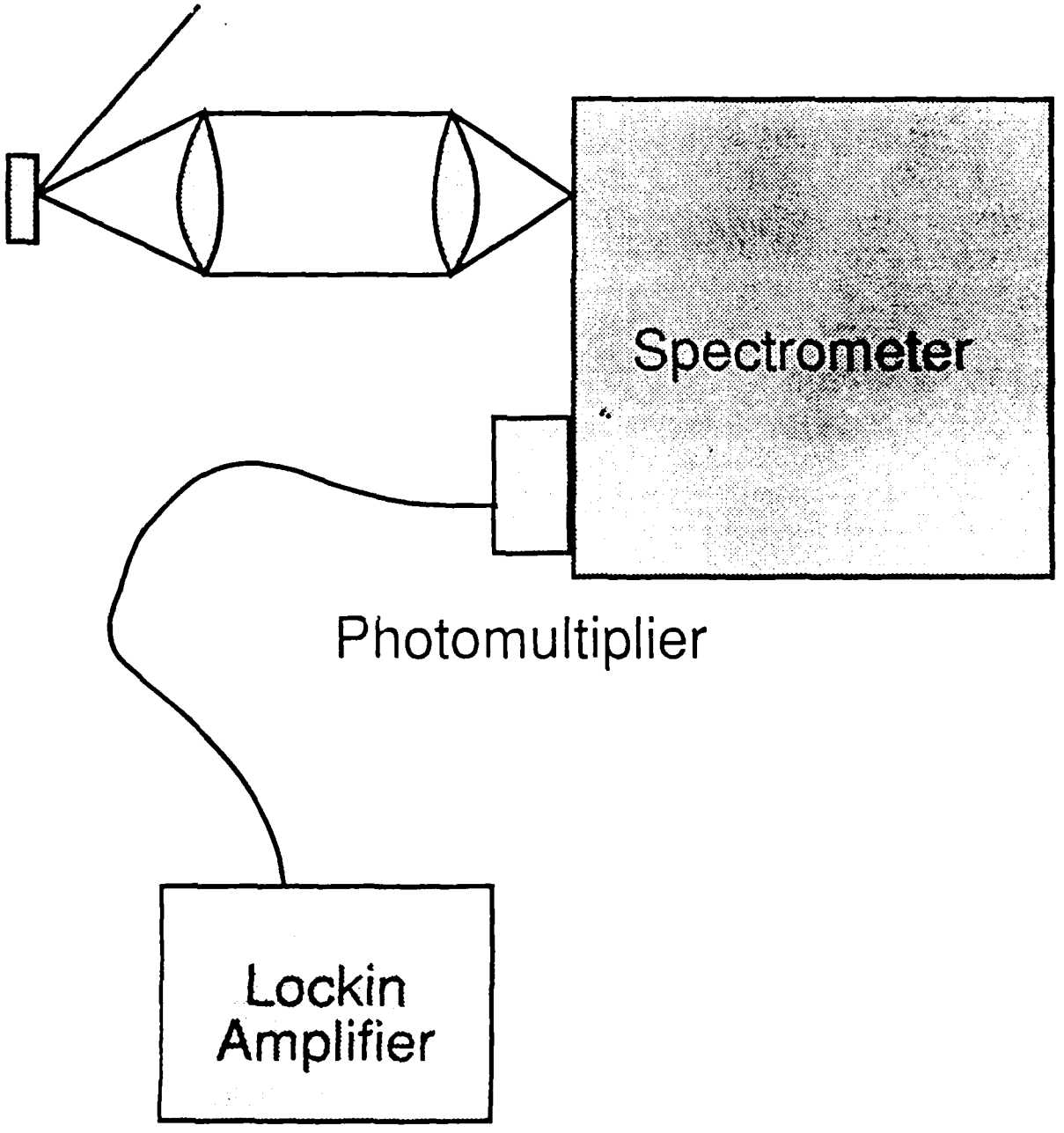
PL DECAY USING CORRELATION METHOD

A. THE METHOD

B. THE RESULTS



Time

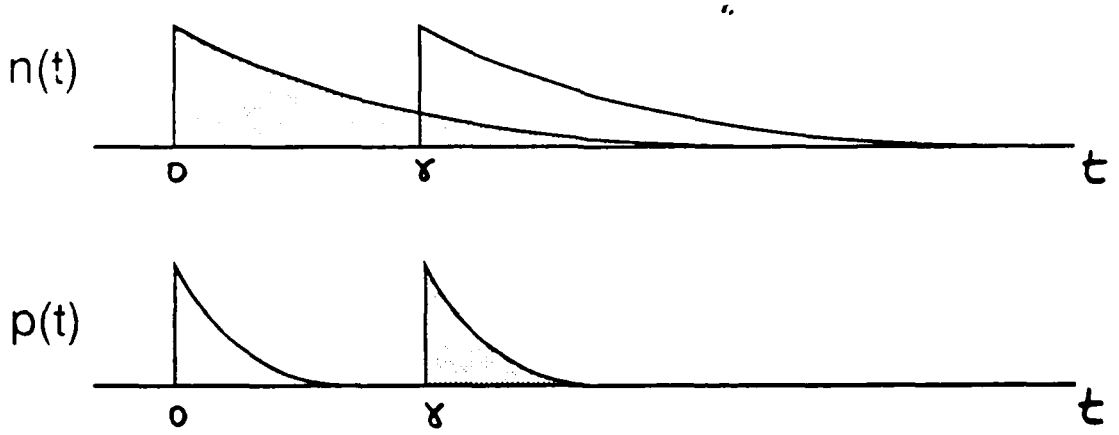

Spectrometer
Photomultiplier
Lockin
Amplifier

Photoluminescence Excitation Correlation Spectroscopy

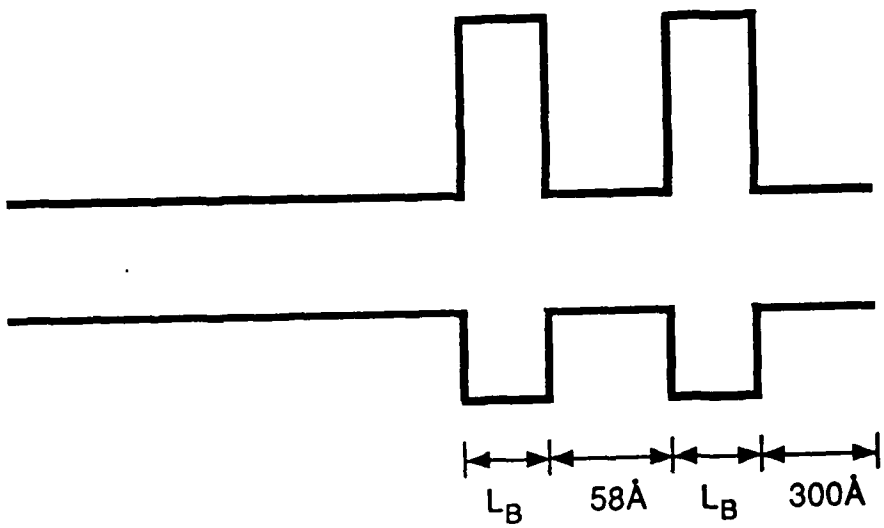
Detect at sum frequency

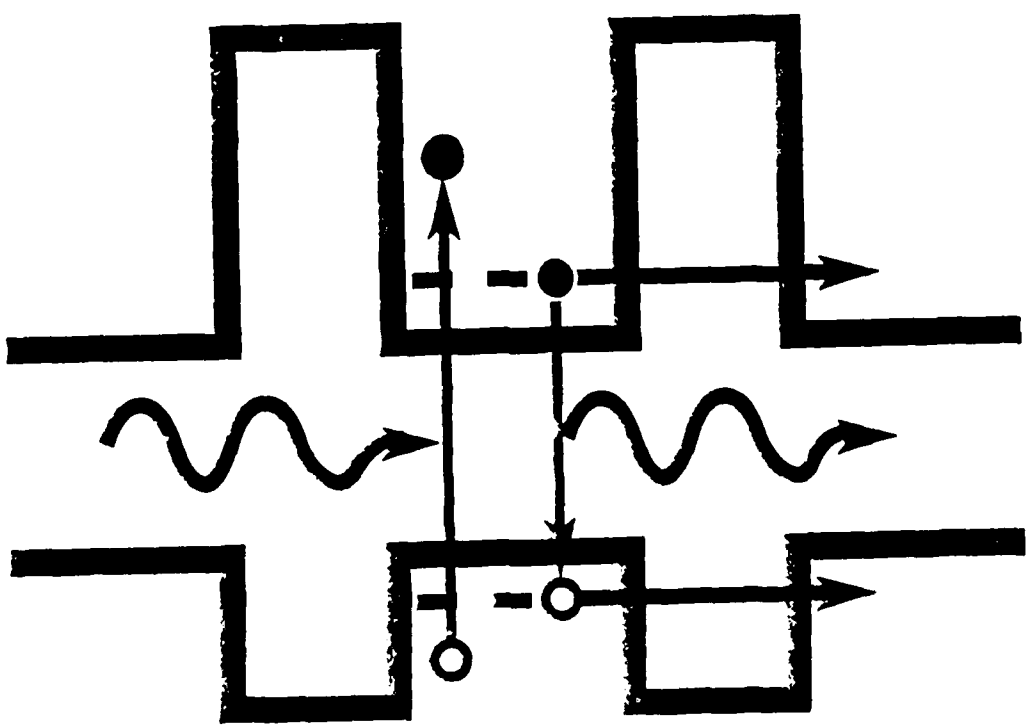
Cross correlation

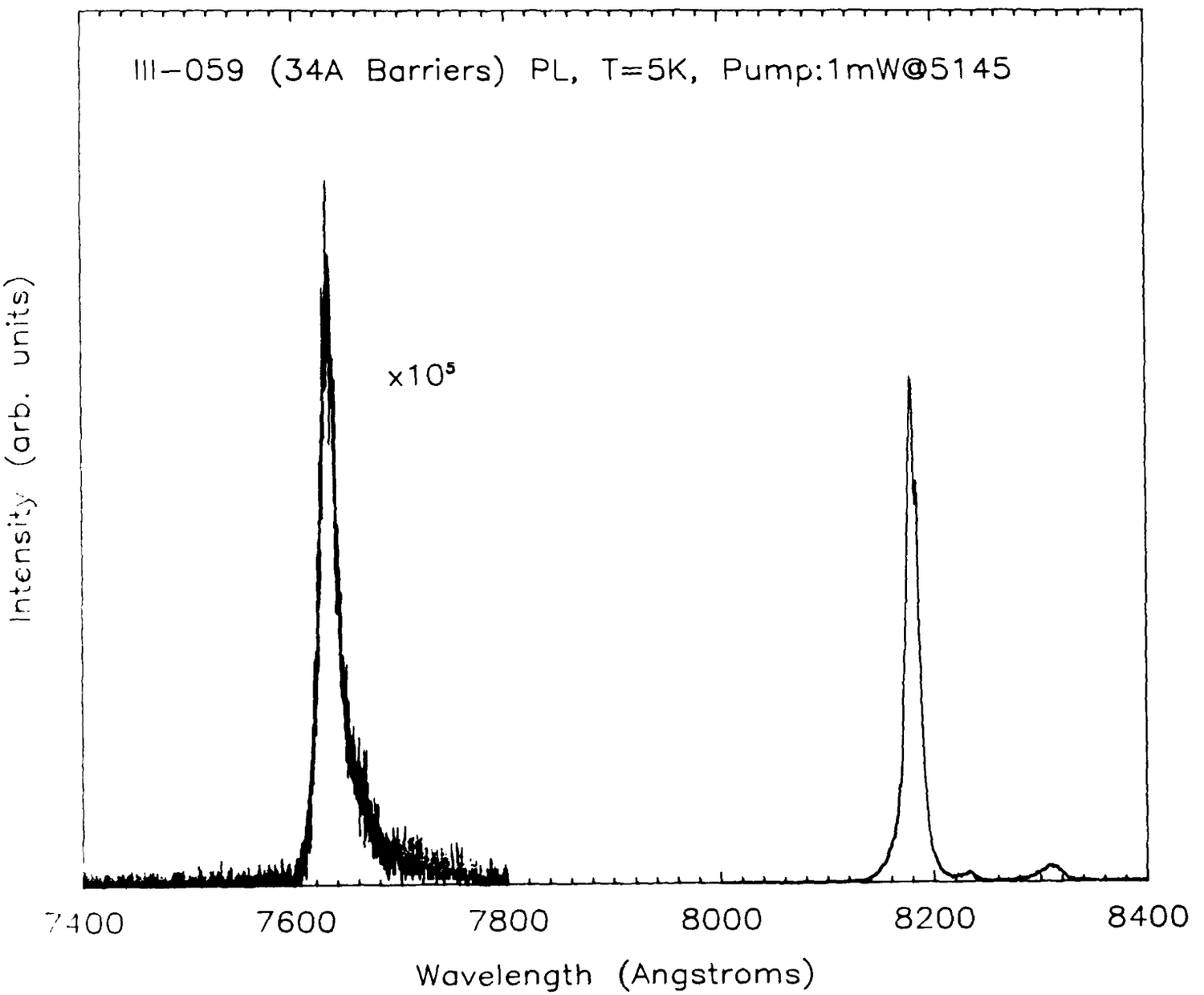
$$I_{SUM}(\gamma) \propto \int [n(t)\, p(t-\gamma) + n(t-\gamma)\, p(t)]\, dt$$

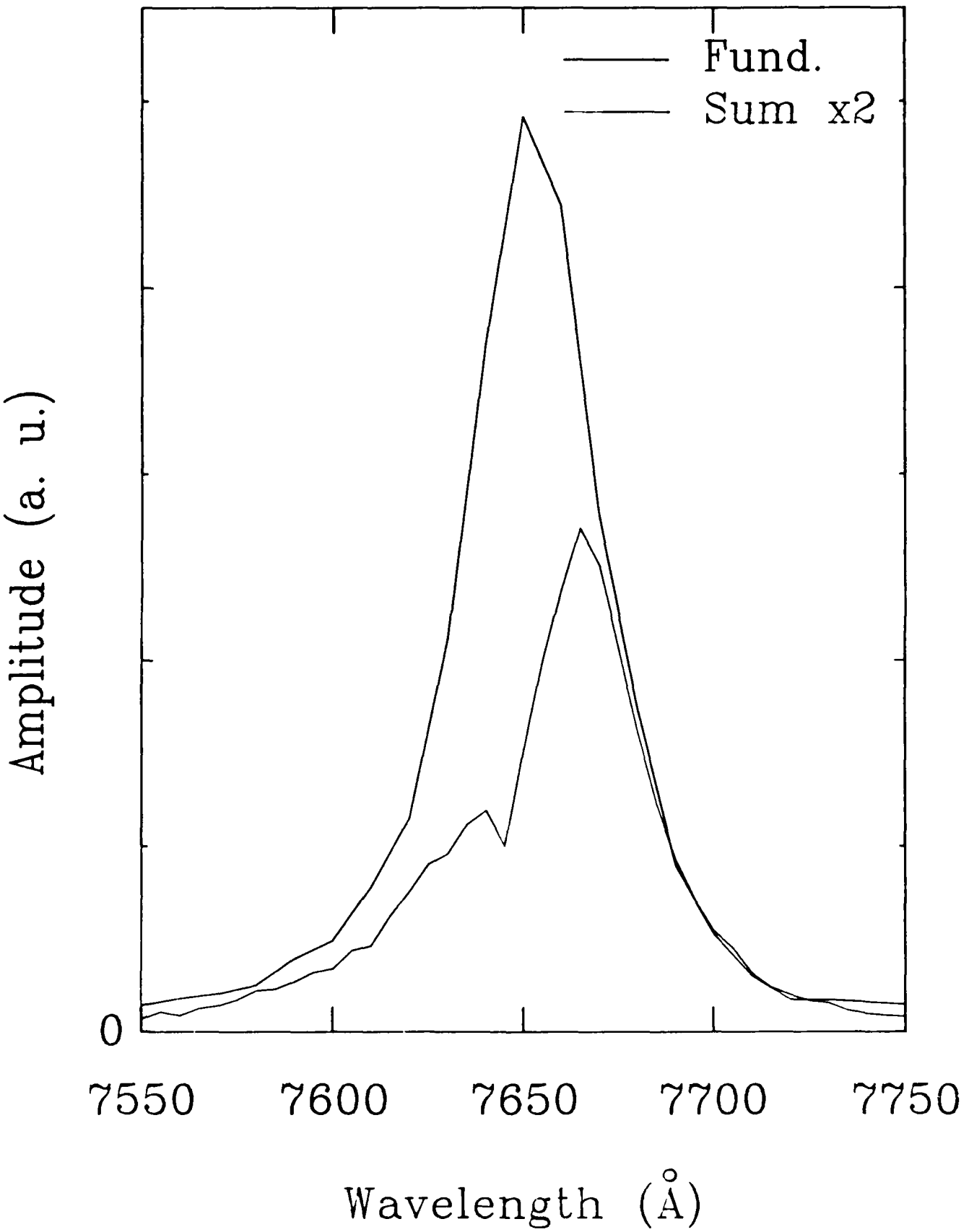


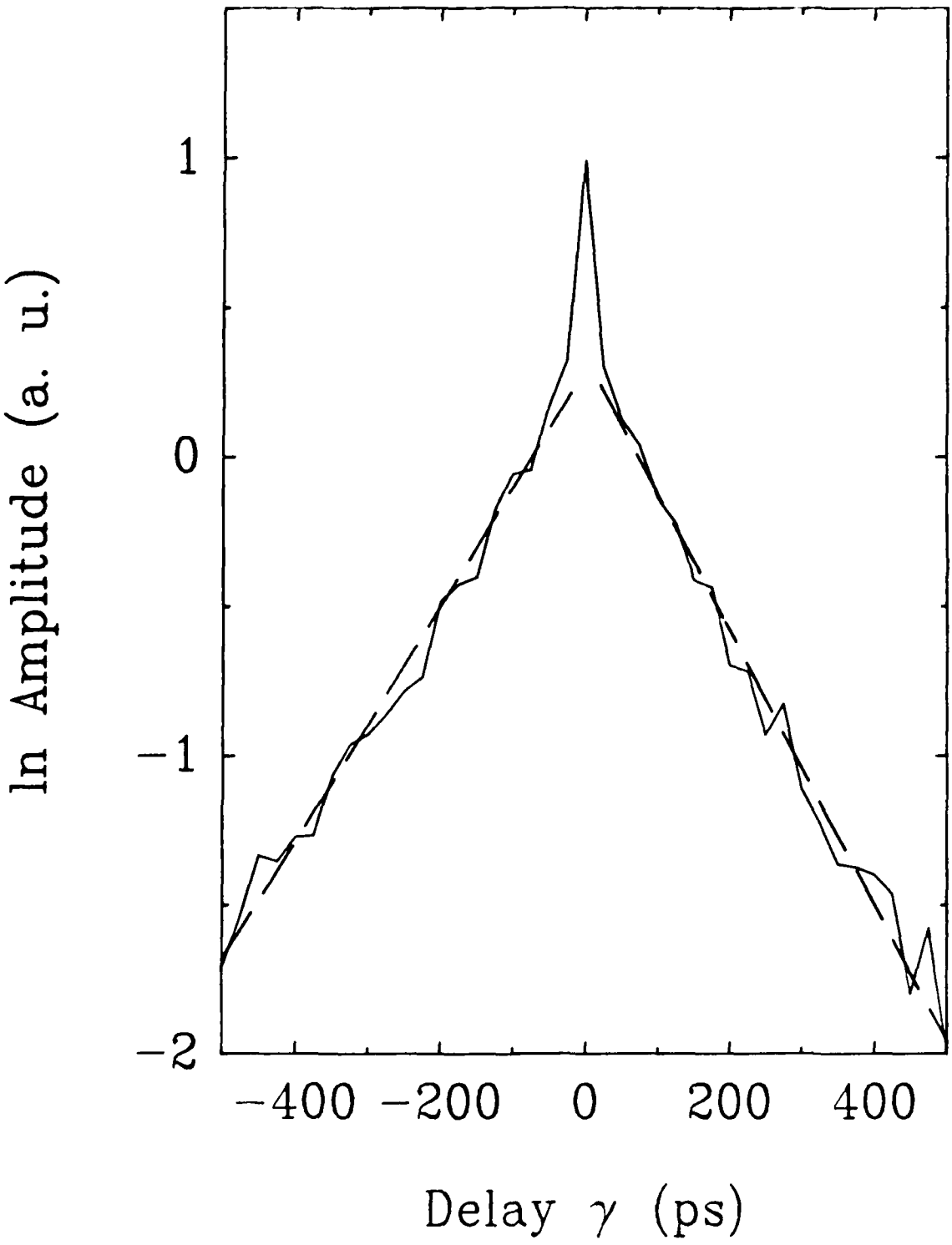
$$I_{sum}(\gamma) \propto \left[e^{-|\gamma|/\tau_1} + e^{-|\gamma|/\tau_2} \right]$$

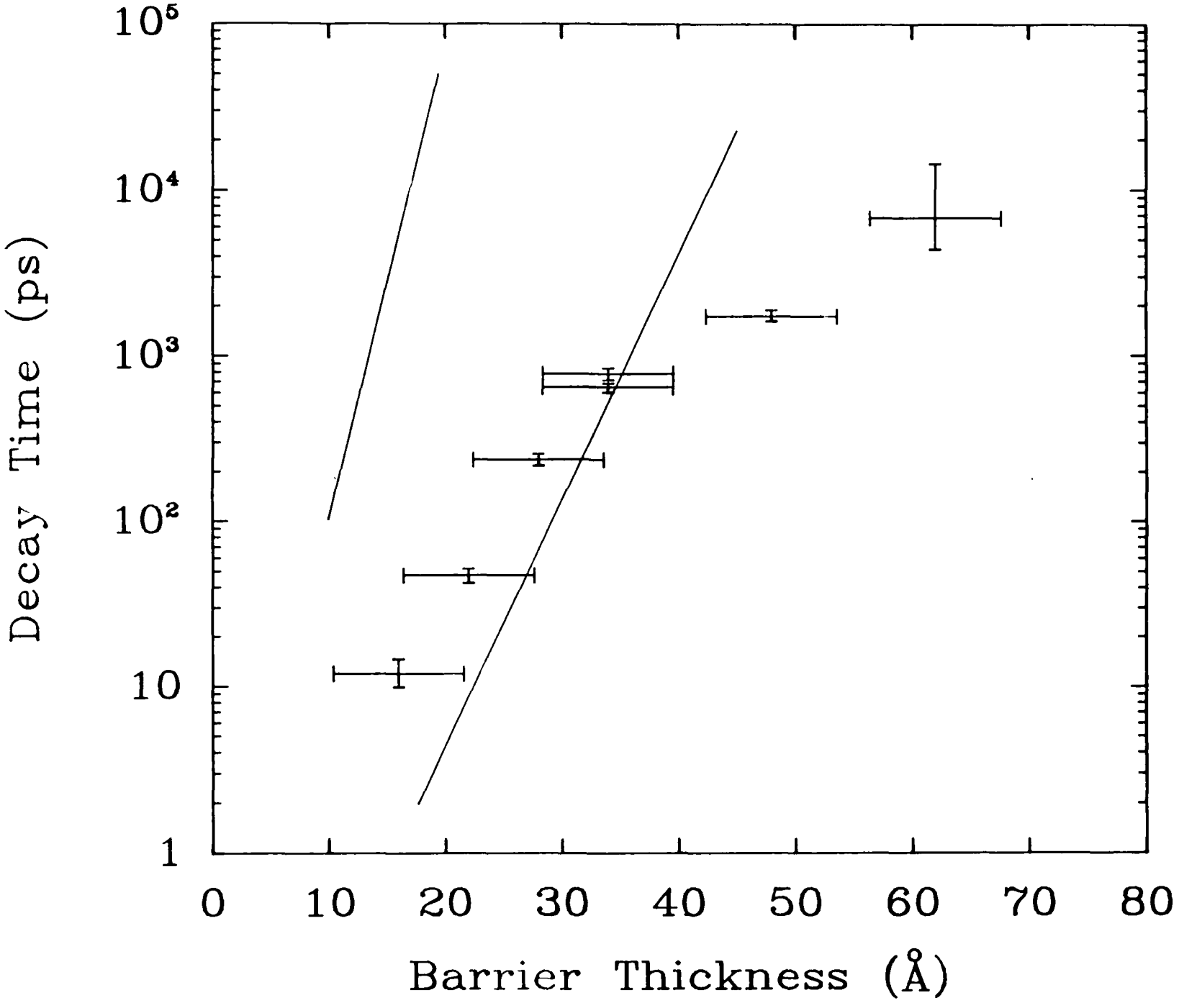

L_B
58Å
L_B
300Å

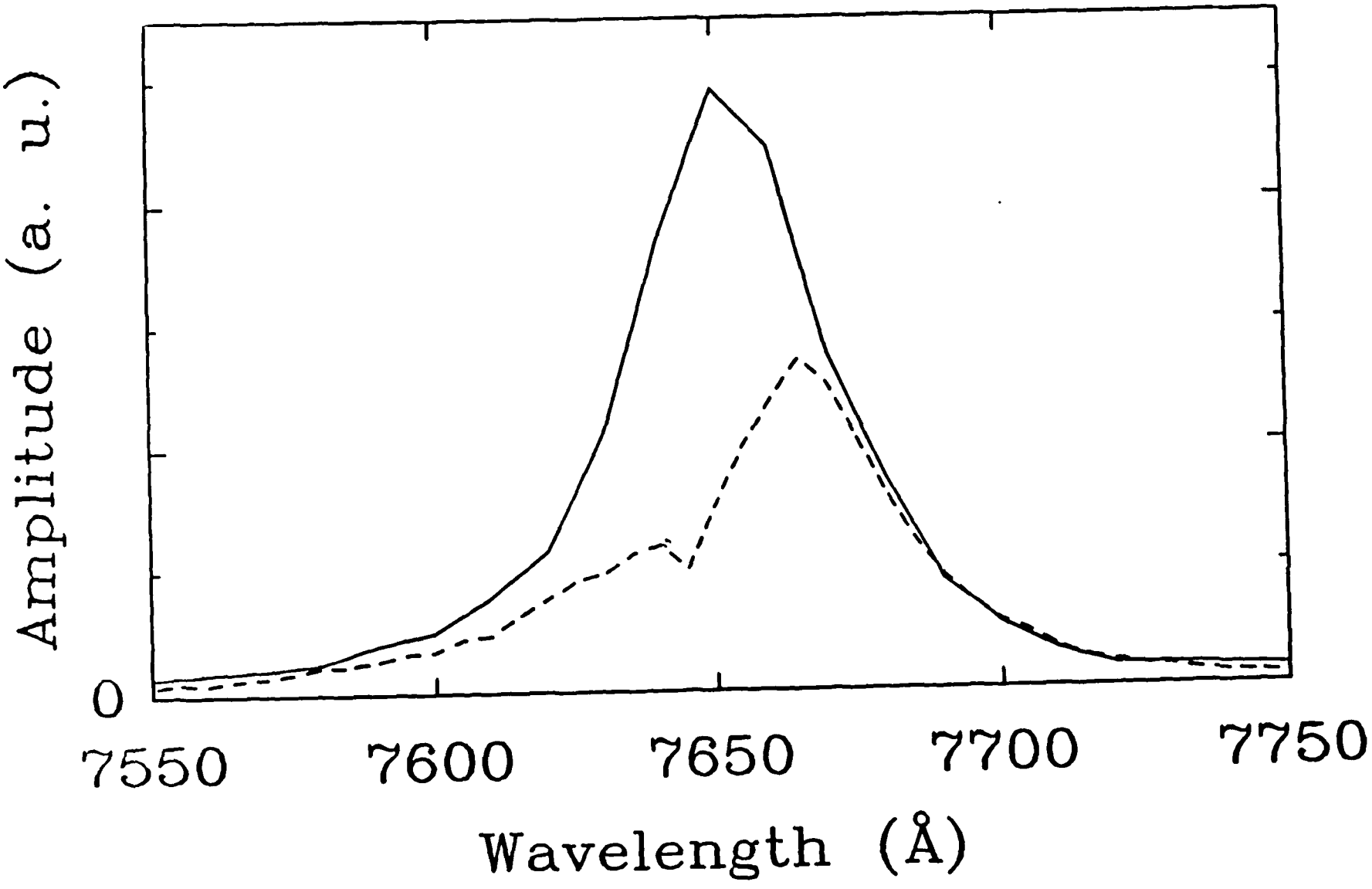


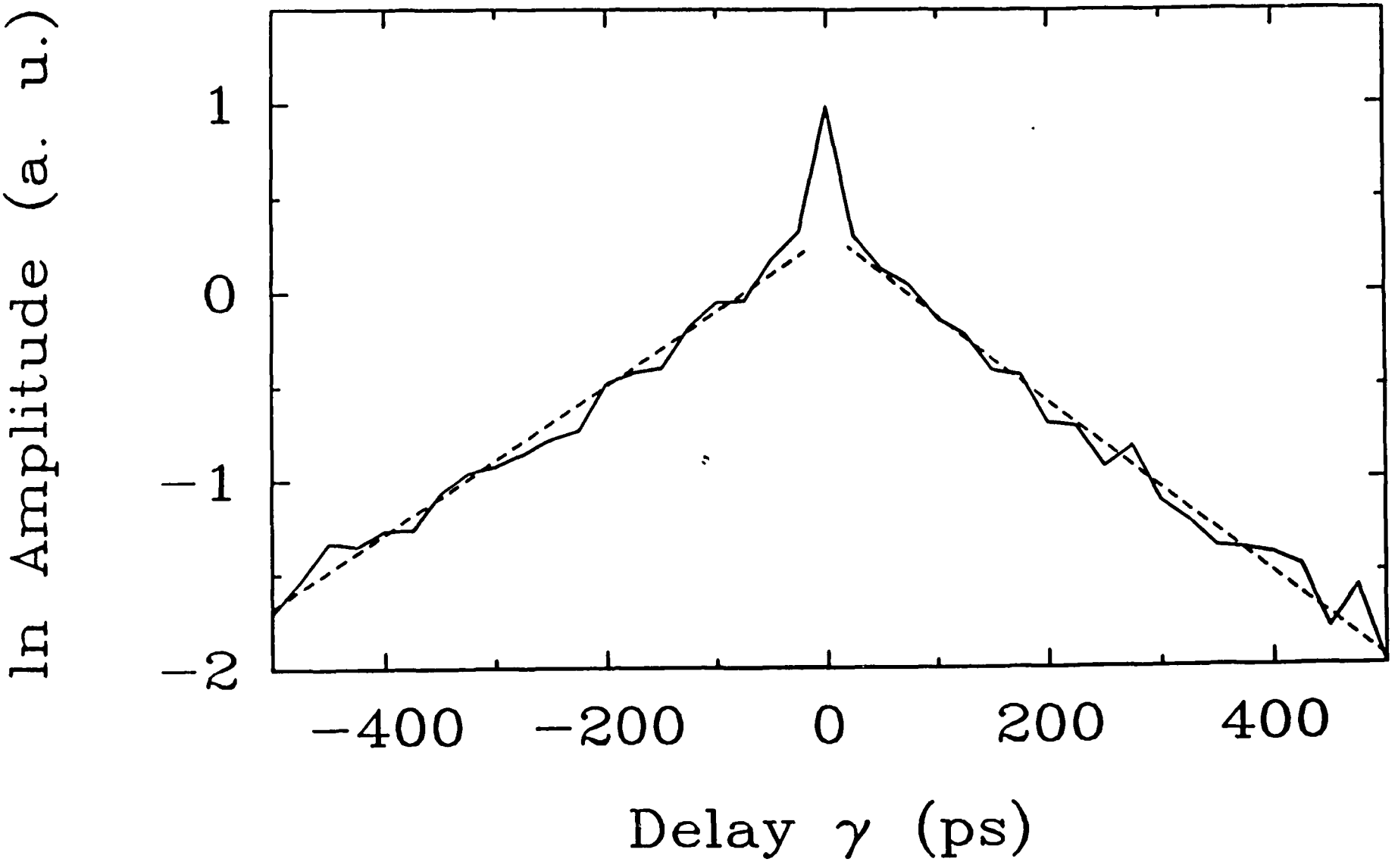

III-059 (34A Barriers) PL, T=5K, Pump:1mW@5145
x10⁵
Intensity (arb. units)
7400
7600
7800
8000
8200
8400
Wavelength (Angstroms)

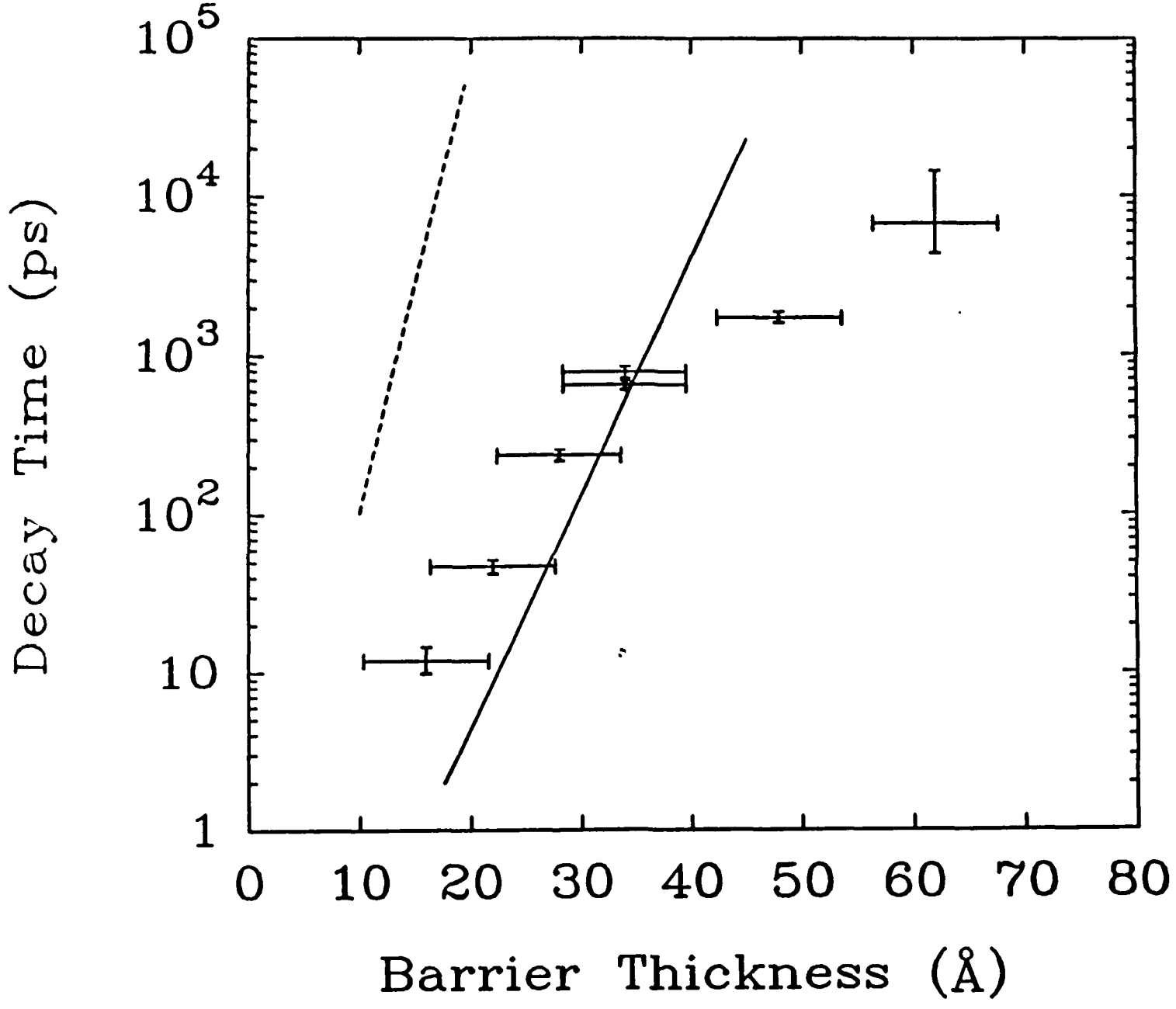

Fund.
Sum x2
Amplitude (a. u.)
0
7550
7600
7650
7700
7750
Wavelength (Å)


ln Amplitude (a. u.)
1
0
−1
−2
−400
−200
0
200
400
Delay γ (ps)

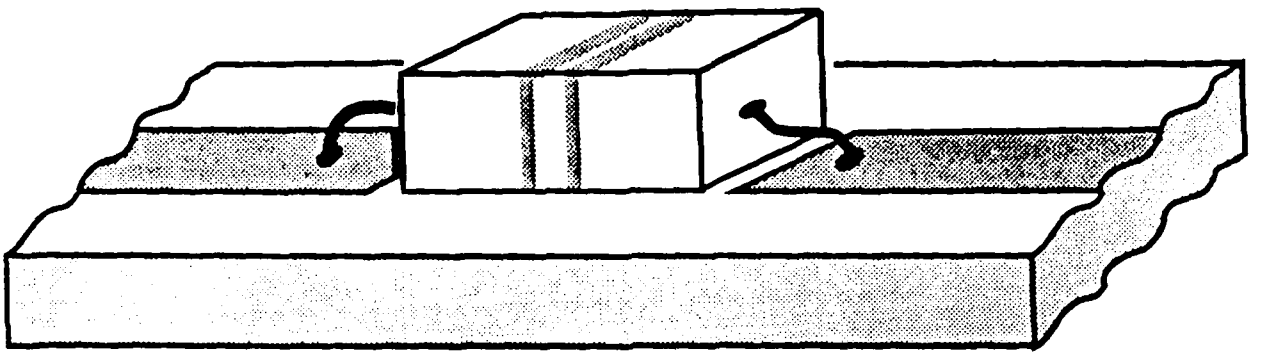

Decay Time (ps)
10⁵
10⁴
10³
10²
10
1
0
10
20
30
40
50
60
70
80
Barrier Thickness (Å)


Amplitude (a. u.)
0
7550
7600
7650
7700
7750
Wavelength (Å)

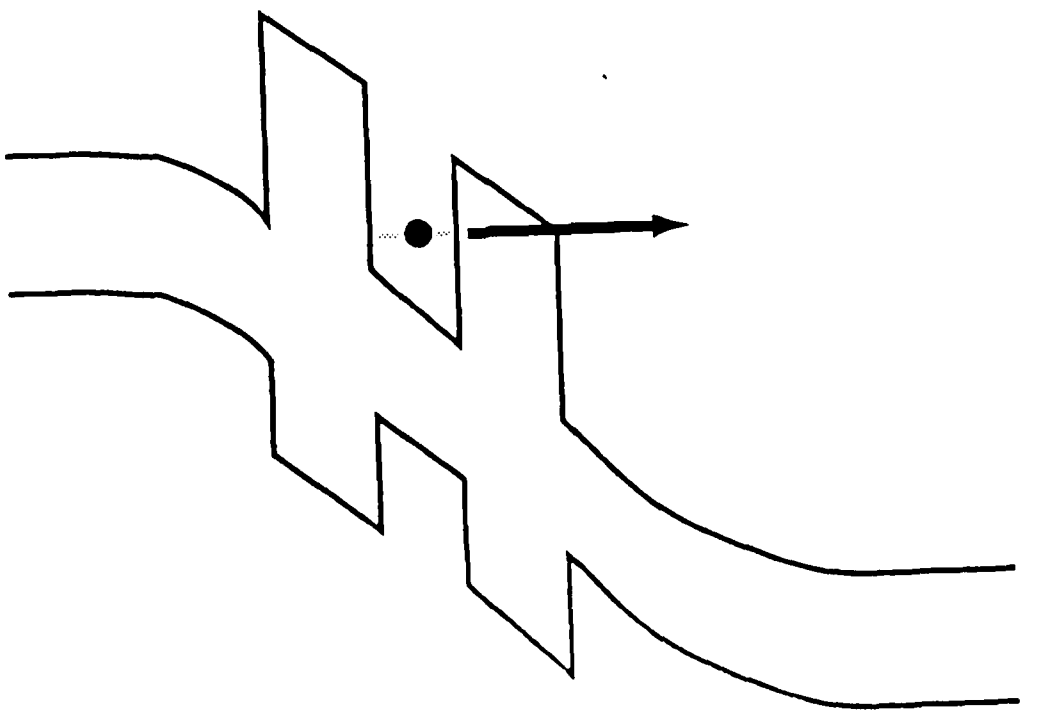

ln Amplitude (a. u.)
1
0
−1
−2
−400
−200
0
200
400
Delay γ (ps)

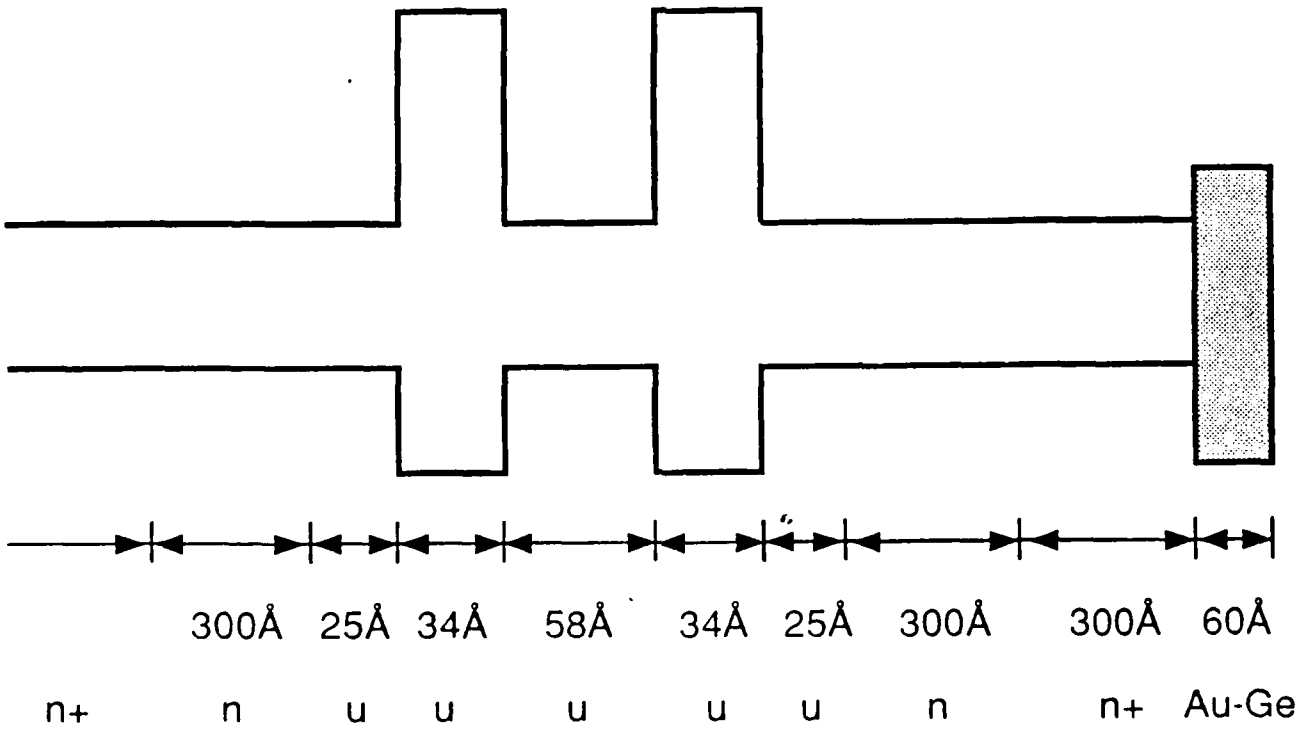

10^5
10^4
10^3
10^2
10
1
Decay Time (ps)
0
10
20
30
40
50
60
70
80
Barrier Thickness (Å)

Real Device



Effect




300Å 25Å 34Å 58Å 34Å 25Å 300Å 300Å 60Å
n+ n u u u u u n n+ Au-Ge

Resonant tunneling through quantum wells at frequencies up to 2.5 THz

T. C. L. G. Sollner, W. D. Goodhue, P. E. Tannenwald, C. D. Parker, and D. D. Peck
Lincoln Laboratory, Massachusetts Institute of Technology, Lexington, Massachusetts 02173

(Received 9 May 1983; accepted for publication 1 July 1983)

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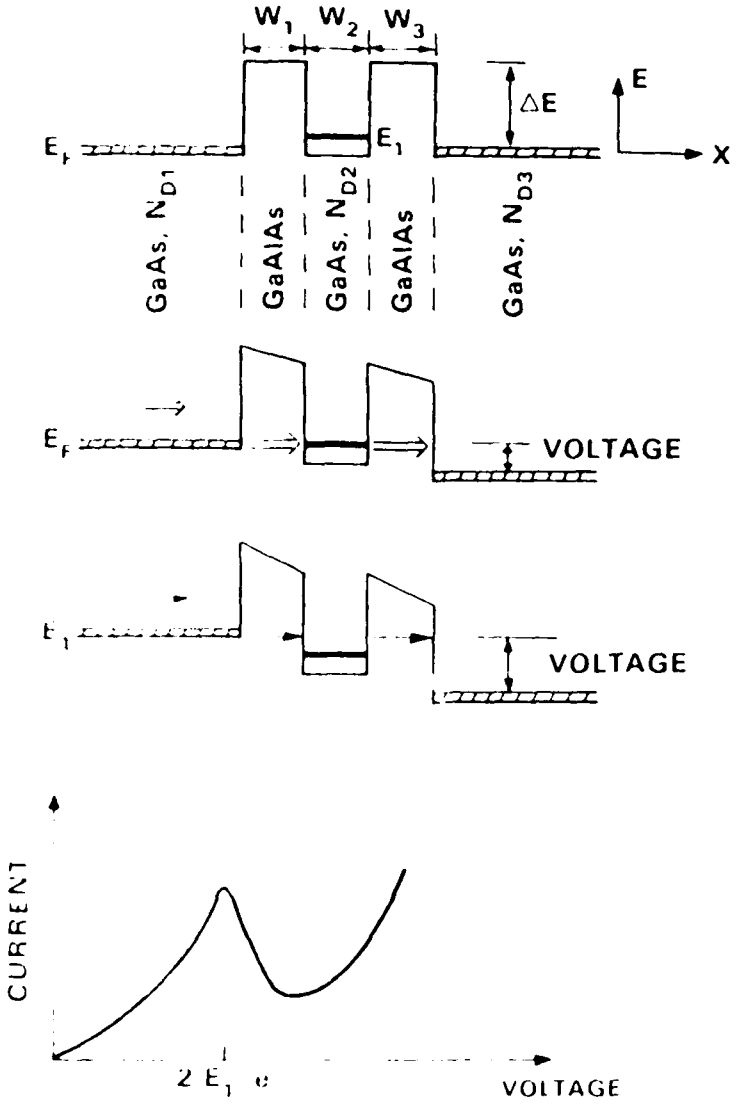


FIG. 1. Electron energy as a function of position in the quantum well structure. The parameters are $N_{D1} = N_{D3} = 10^{18}$ cm^{-3}, $N_{D2} = 10^{17}$ cm^{-3}, and $W_1 = W_2 = W_3 = 50$ Å. The doping level in the well center is an average value achieved by placing a layer of 10^{18} cm^{-3} material in the central 10% of the well. The energy level E_1 occurs above the bottom of the bulk conduction band because of confinement in the x direction. From the aluminum concentration (x = 25% - 30%) we estimate $\Delta E = 0.23$ eV.

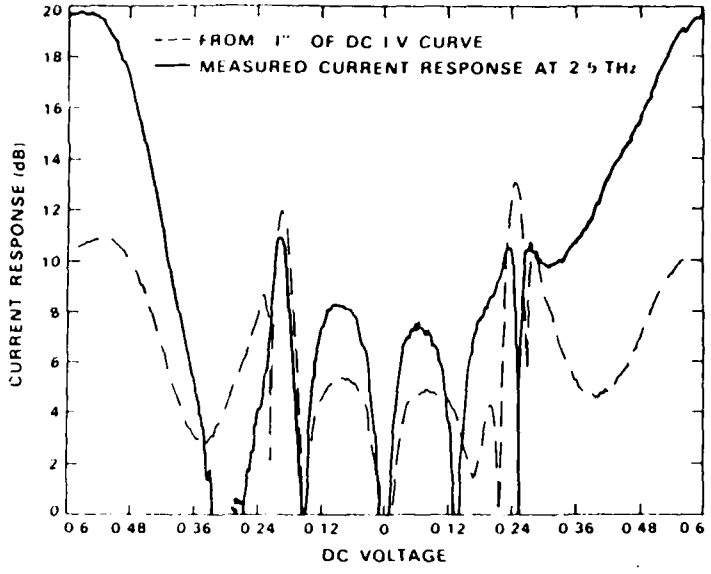
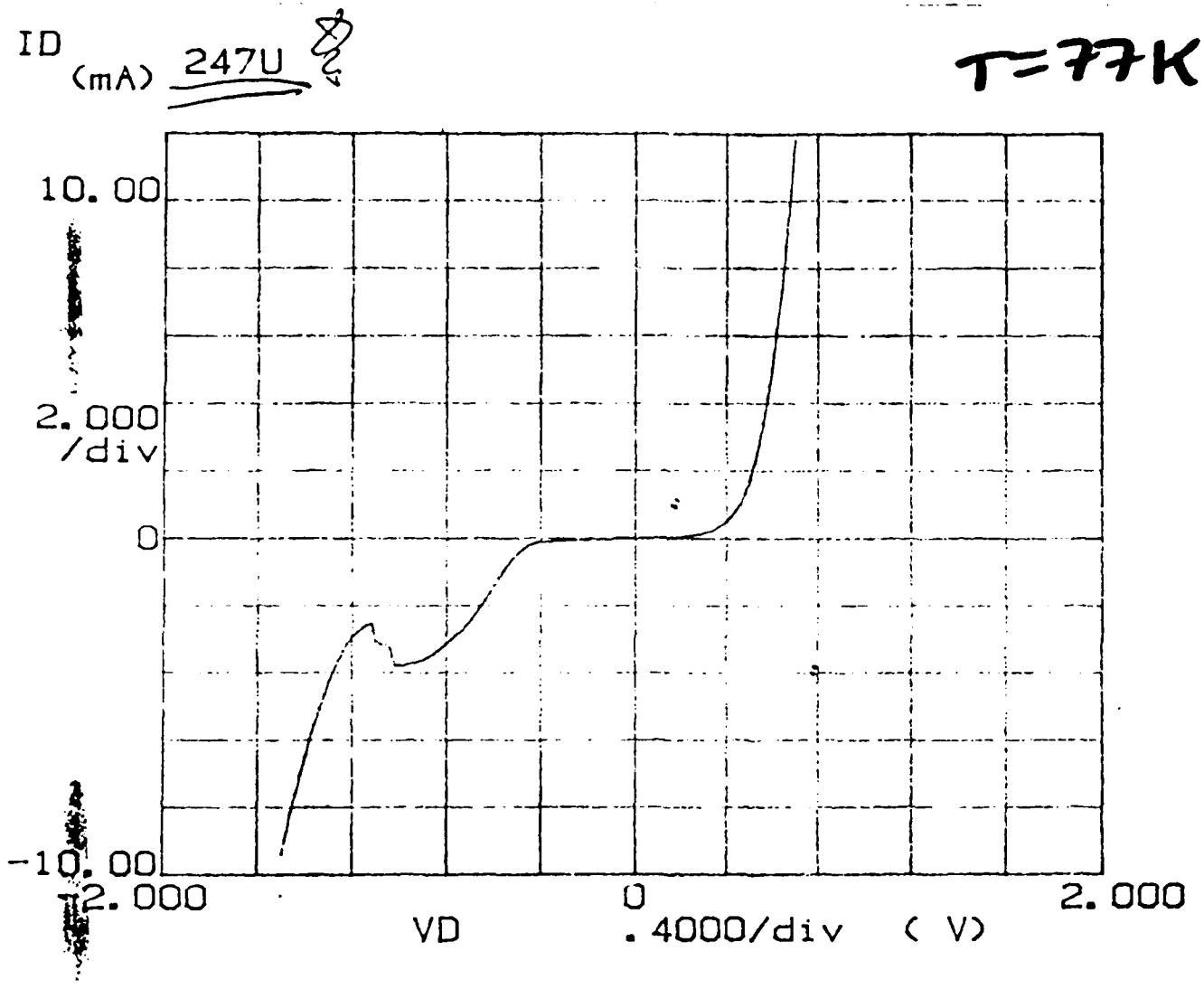


FIG. 3. Current response at 2.5 THz as a function of dc bias voltage. (Sample is at 25 K.) The dashed curve is calculated on the basis of the dc *I-V* curve. Zero decibels corresponds to 0.3 μA/W and 10 dB is 3 μA/W. The general agreement shows that the *I-V* curve at 2.5 THz is very similar to the dc curve, and thus the charge transport is fast.



250 μm device
60 Å AuGe

SUMMARY OF OUR MEASUREMENTS

A. CARRIED OUT PL DECAY MEASUREMENTS ON TUNNEL STRUCTURES

B. MEASUREMENTS TO SHORTER TIMES THAN SAKAKI TO 10ps

C. MEASURED A SINGLE DECAY TIME AT 80K

D. ROLE OF DIFFERENCES IN ELECTRON AND HOLE DECAY TIMES UNCLEAR

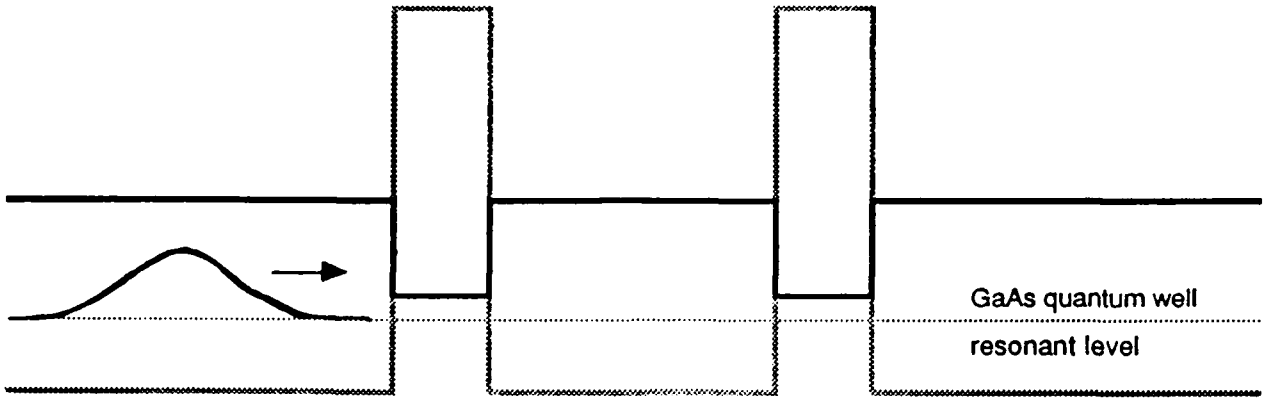
E. BEGINNING BIAS DEPENDENCE MEASUREMENTS

SUMMARY OF TUNNELING TIMES

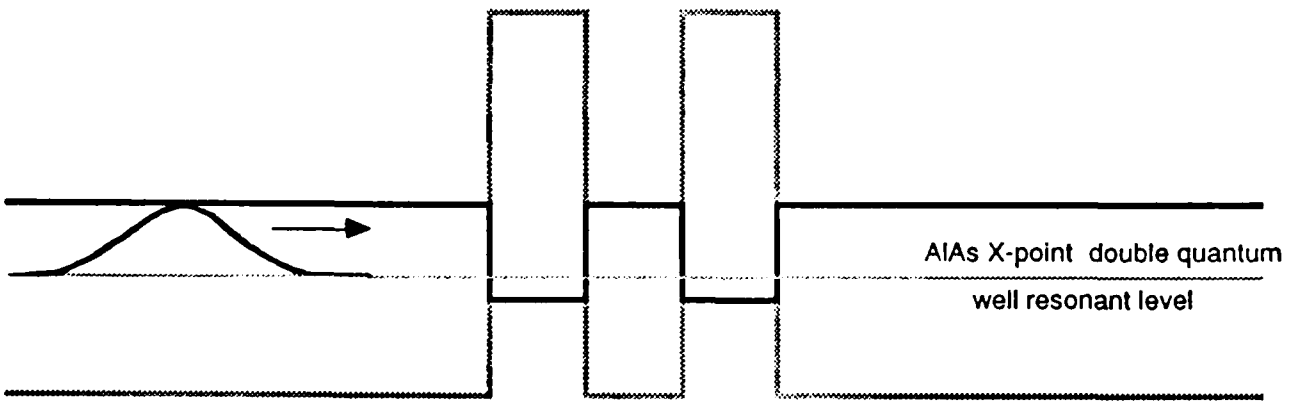
Source	Prediction for 16Å	Thickness for 2ps
Our Experiments; T=80K $\tau_T = 0.203e^{0.255L_B}$	12ps	9Å
2 Band Theory $\tau_T = 0.0047e^{0.342L_B}$	1.1ps	18Å
Sakaki and Co-workers: T=20K $\tau_T = 0.670e^{0.158L_B}$; T=90K $\tau_T = 0.229e^{0.201L_B}$	8.4ps (T=20K); 5.7ps (T=90K)	6.9Å(T=20K); 11Å(T=90K)

Resonant Tunneling

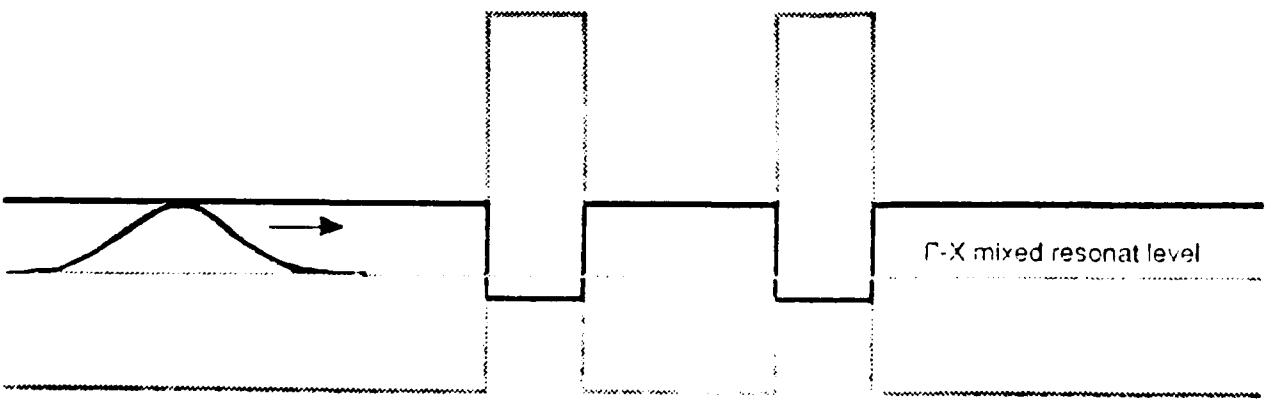
1. Γ-point resonant tunneling



2. X- point resonat tunneling



3. Resonant tunneling through Γ-X mixed state



Tunneling escape time of electrons from a quantum well under the influence of an electric field

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(Received 22 July 1988; accepted for publication 21 October 1988)

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p^+	$Al_xGa_{1-x}As$	2000 Å
i	$Al_xGa_{1-x}As$	2000 Å
i	GaAs	30 Å
i	$Al_xGa_{1-x}As$	b
i	GaAs	1000 Å
n^+	GaAs	1 μm

S.I. Substrate

FIG. 1. Structure of the single QW samples used in width b was varied to study the effect on the tunnel

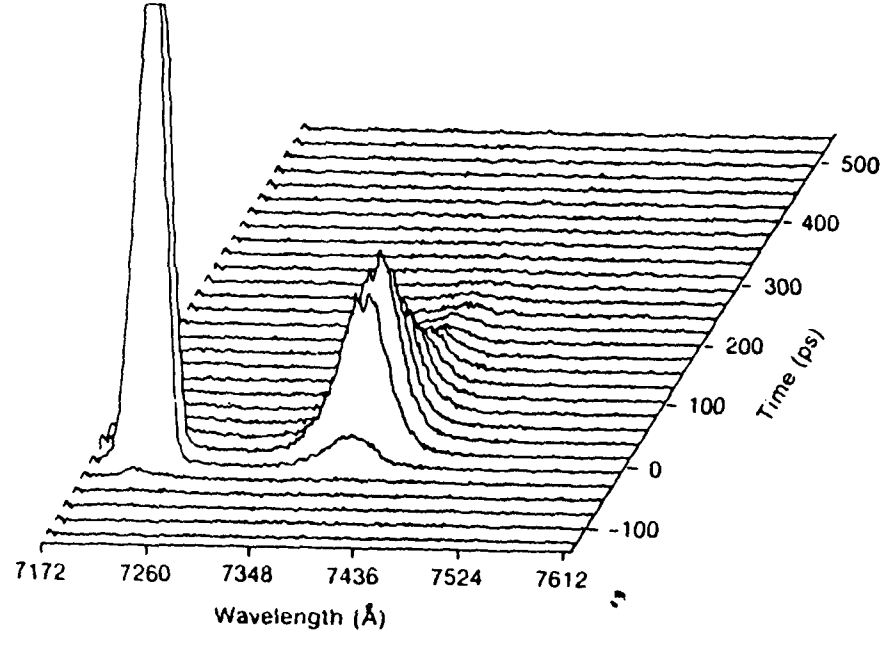
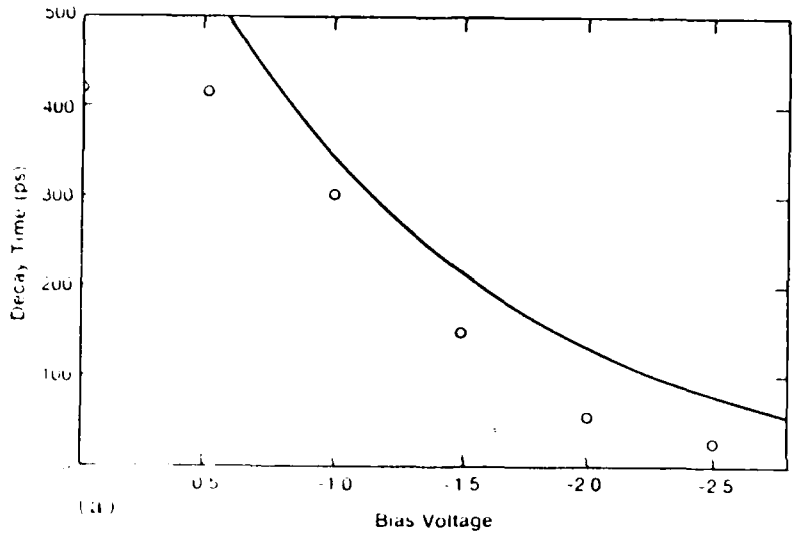
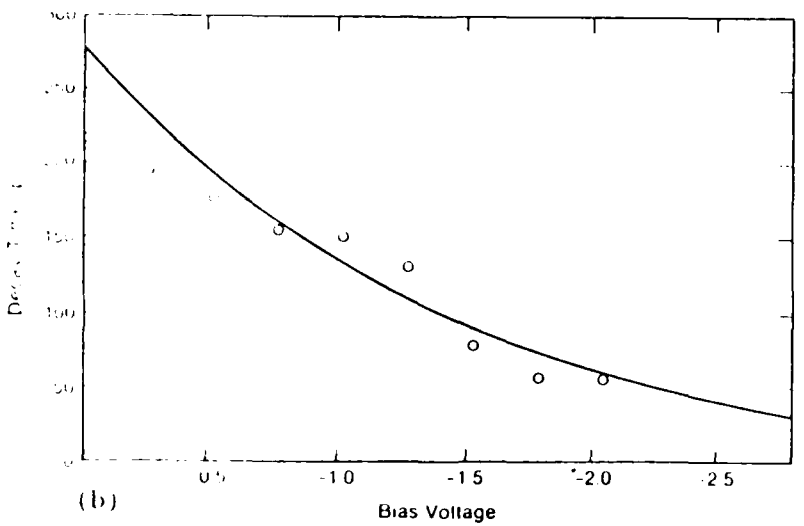


FIG. 2. Time-resolved PL spectrum from sample with $x = 30\%$, $b = 85$ Å at zero bias. The peak at 740 nm is the QW PL; the peak at 722 nm is scattered laser pump light.

Tunneling escape time of electrons from a quantum well under the influence of an electric field





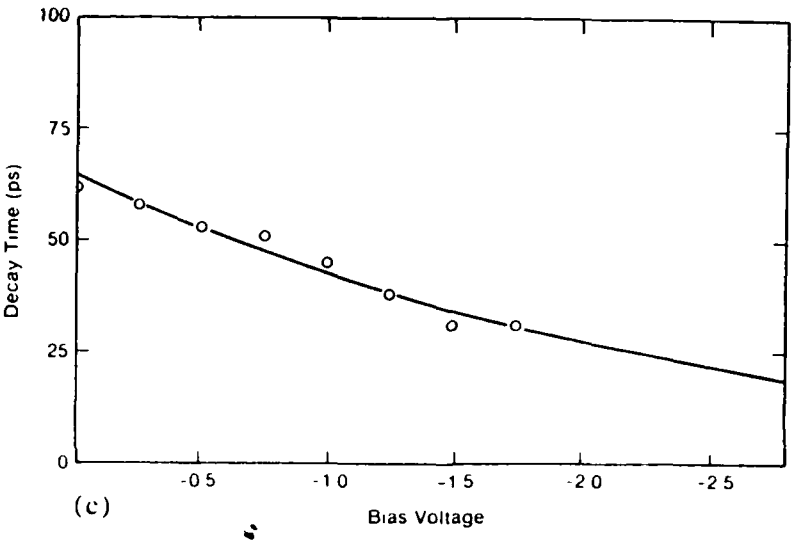


FIG. 3. PL decay rate vs applied bias. The QW width is 30 Å; the barrier Al composition x is 30%. The solid lines are the theoretical predictions from Eq. (2) in the text. (a) Barrier width $b = 121$ Å, (b) barrier width $b = 111$ Å, and (c) barrier width $b = 85$ Å.

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MEASUREMENTS OF BIAS DEPENDENCE OF PL DECAY

A. STRUCTURE NOT REALISTIC BARRIER WIDTH >85Å

B. DECAY TIMES MEASURED GREATER THAN 30-50ps

C. SUBSTANTIAL DISAGREEMENT BETWEEN THEORY AND EXPERIMENT FOR THINNER BARRIERS

FUTURE PLANS

A. MAKE BIAS DEPENDENCE MEASUREMENTS OF PL DECAY

B. MAKE SIMULATIONS OF MEASUREMENT

- DIFFERENCE IN BEHAVIOR OF ELECTRONS AND HOLES
- ROLE OF BANDSTRUCTURE
- COMPARE IN DETAIL THEORY AND EXPERIMENT

C. INVESTIGATE THE USE OF OTHER TECHNIQUES

- PCE STRIP LINE METHOD
- ELECTRO-OPTIC READOUT

D. MEASURE NEW TUNNEL STRUCTURES

EHF HBT Development

B. Bayraktaroglu

Texas Instruments
Dallas, TX

EHF HBT DEVELOPMENT

AGENDA

- PROGRAM GOALS
- APPROACH
- DEVICE STRUCTURE
- FABRICATION
- CHARACTERIZATION AND MODELING
- SUMMARY

EHF HETEROJUNCTION BIPOLAR TRANSISTOR

OBJECTIVE

DEVELOPMENT OF InGaAs/InP(InAlAs) HETEROJUNCTION BIPOLAR TRANSISTOR ON A GaAs SUBSTRATE FOR POWER AMPLIFICATION AT EHF BAND.

GOALS

FREQUENCY (GZ)	OUTPUT POWER (W)	GAIN (dB)	EFFICIENCY (%)
44	1.0	6	40
60	0.5	6	30
94	0.25	6	20

SCOPE

- DEVELOPMENT OF MATERIALS TECHNOLOGY TO PREPARE InGaAs/InP(InAlAs) HBT STRUCTURES ON GaAs SUBSTRATES BY MBE (MOMBE) AND MOCVD.

- DEVELOPMENT OF COMPLEMENTARY DEVICE STRUCTURES FOR HIGH POWER AND EFFICIENCY.

- SMALL AND LARGE SIGNAL DEVICE MODELING.

APPROACH

- PREPARE InGaAs/InAlAs HBT STRUCTURE ON InP SUBSTRATES BY MBE. OPTIMIZE DEVICE STRUCTURE.
- PREPARE InGaAs/InP HBT STRUCTURE ON InP SUBSTRATES BY MOCVD. OPTIMIZE DEVICE STRUCTURE
- GROW OPTIMIZED STRUCTURE ON GaAs SUBSTRATE BY MBE AND/OR MOCVD.
- USE 1 μm WIDTH EMITTER FINGERS AND SELF-ALIGNED EMITTER-BASE-COLLECTOR FABRICATION.
- OPTIMIZE npn AND pnp DEVICE PERFORMANCE ON SEPARATE SUBSTRATES. INTEGRATE OPTIMIZED STRUCTURES ON THE SAME SUBSTRATE.

Design: EHF–1

Emitter-up structure

LAYER	Doping (cm^{-3})	Thickness (μm)
n^+–InAs	1 x 10^{19}	0.05
Grading InP→ InAs	5 x 10^{18}	0.05
n–InP	2 x 10^{17}	0.1
Grading InP → InGaAs	2 x 10^{17}	0.01
p^+–$In_{.53}Ga_{.47}As$	1 x 10^{19}	0.1
Grading InGaAs → InP	5 x 10^{16}	0.01
n–InP	5 x 10^{16}	0.8
n^+–$In_{.53}Ga_{.47}As$	5 x 10^{18}	1.0
InP buffer	SI	2.0
GaAs SUBSTRATE	Undoped	500(nom.)

Initial HBT Structure on InP

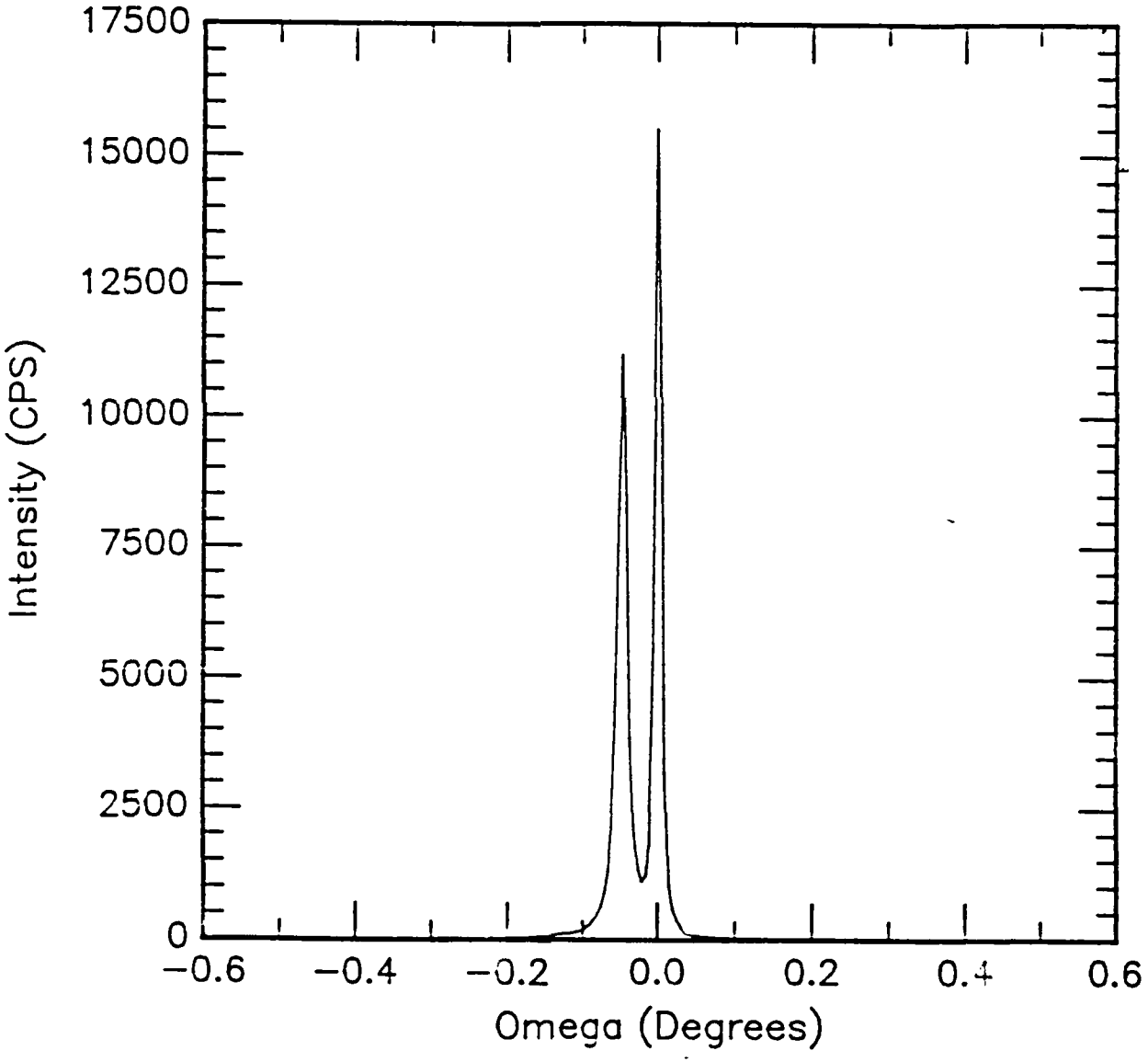
LAYER	Doping (cm^{-3})	Thickness (μm)
n^+–InAs	1 x 10^{19}	0.05
Grading InAs→ InAlAs	1 x 10^{19}	0.05
n–$In_{.52}Al_{.48}As$	2 x 10^{17}	0.1
Grading InAlAs → InGaAs	2 x 10^{17}	0.01
p^+–$In_{.53}Ga_{.47}As$	1 x 10^{19}	0.1
n–$In_{.53}Ga_{.47}As$	1 x 10^{17}	0.5
n^+–$In_{.53}Ga_{.47}As$	5 x 10^{18}	1.0
SI InP SUBSTRATE	Undoped	500(nom.)

Design: HBT–34

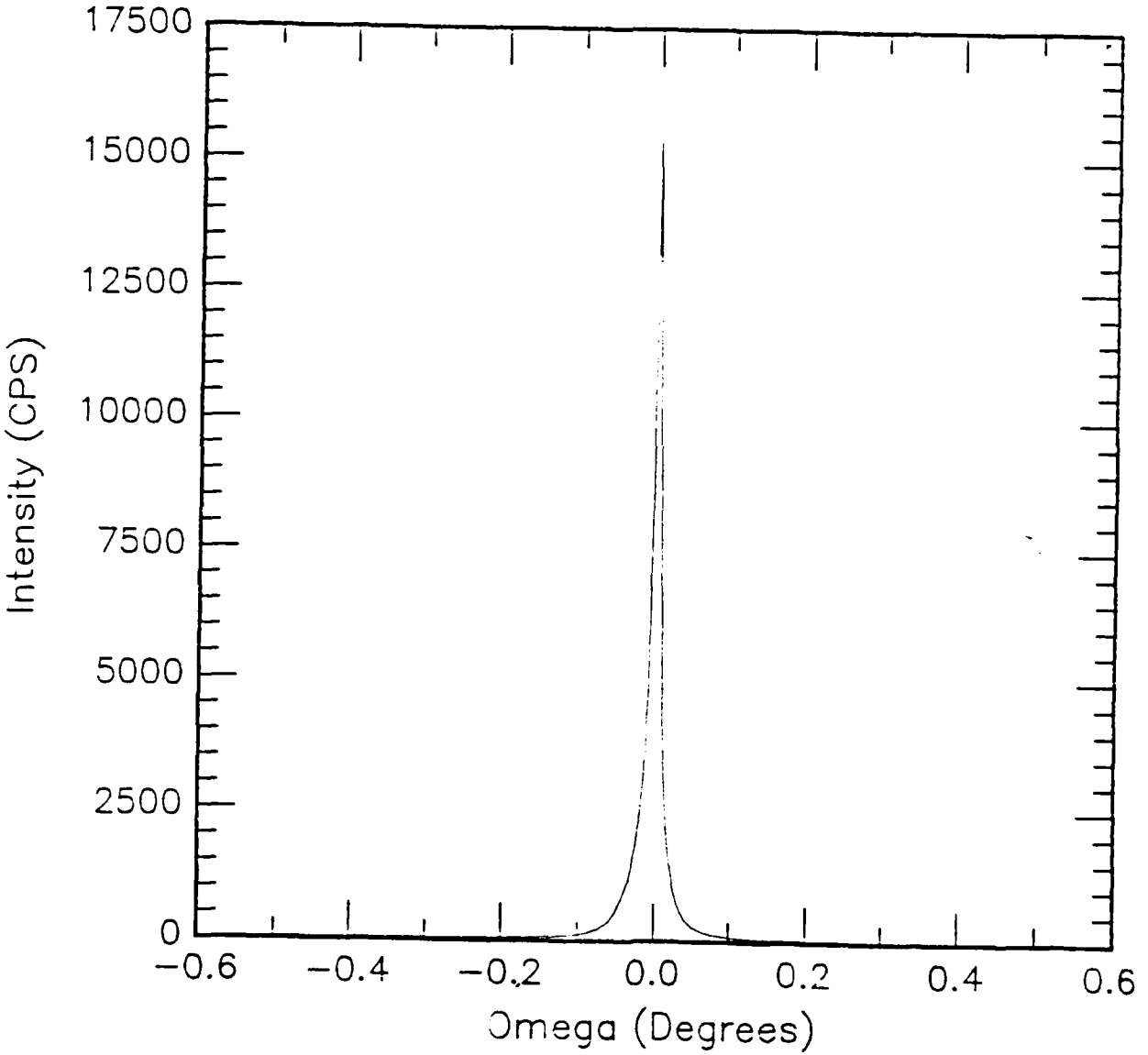
Strained-layer structure

LAYER	Doping (cm^{-3})	Thickness (μm)
n^+–InGaAs	5×10^{18}	0.02
n^+–GaAs	5×10^{18}	0.05
n–grading	1×10^{18}	0.03
n–$Al_{.3}Ga_{.7}As$	3×10^{17}	0.1
n–GaAs	1×10^{18}	0.01
p^+–$In_{.1}Ga_{.9}As$	1×10^{19}	0.02
p^+–GaAs	1×10^{19}	0.04
p^+–$In_{.1}Ga_{.9}As$	1×10^{19}	0.02
p^+–GaAs	1×10^{19}	0.04
n–GaAs	3×10^{16}	1.0
n^+–GaAs	5×10^{18}	0.5
SI SUBSTRATE	Undoped	500

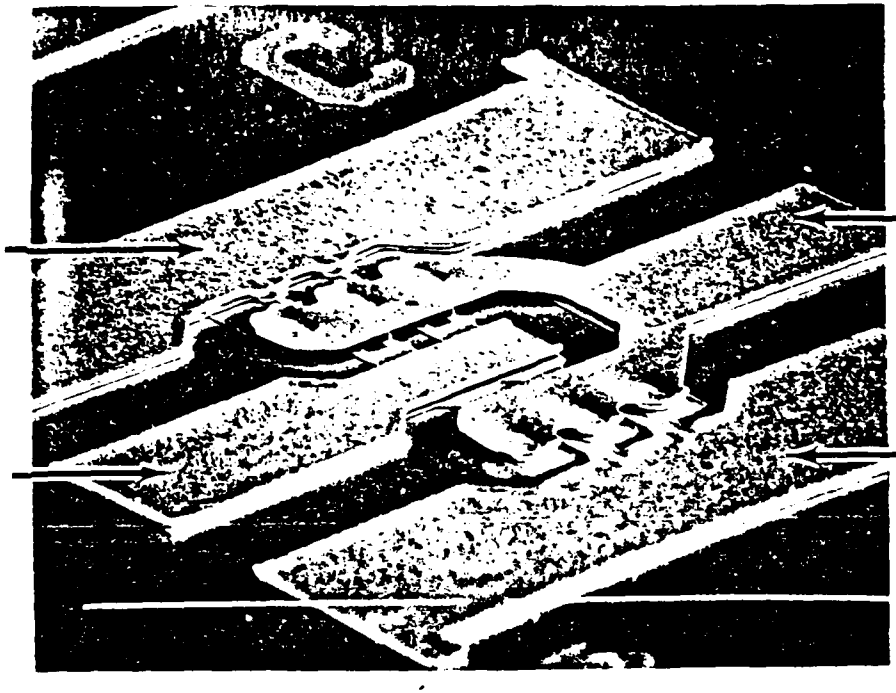
InGaAs ON InP WITH LATTICE MISMATCH



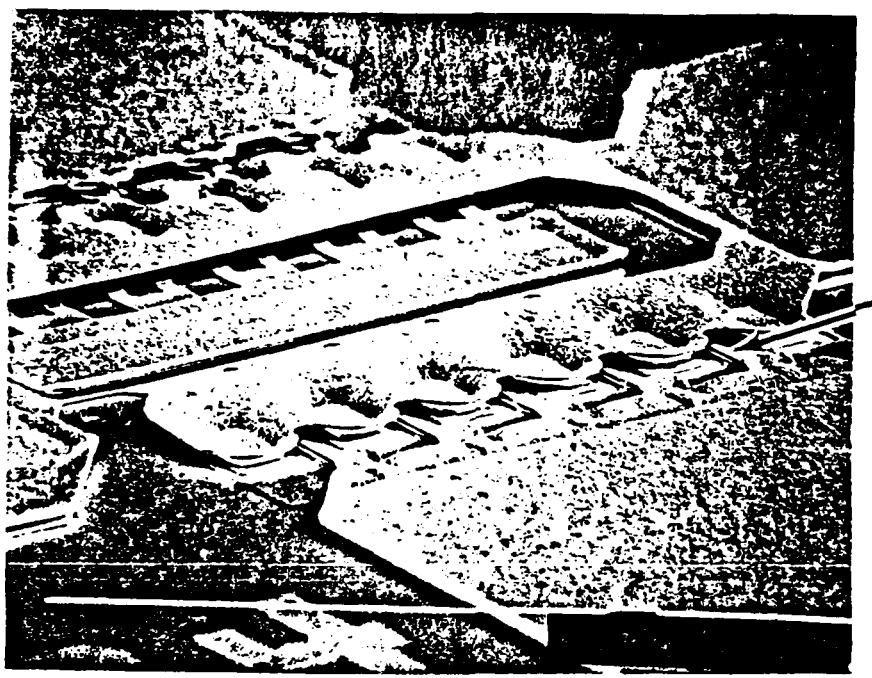
LATTICE MATCHED InGaAs ON InP



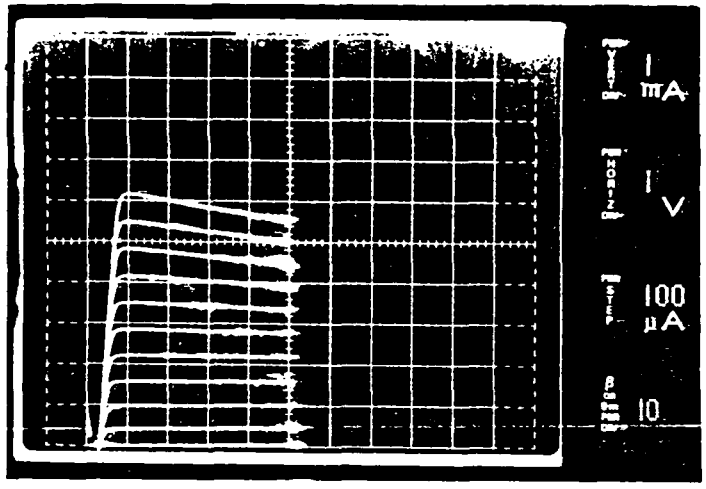
HETEROJUNCTION BIPOLAR TRANSISTOR
ON-WAFER PROBE CIRCUIT

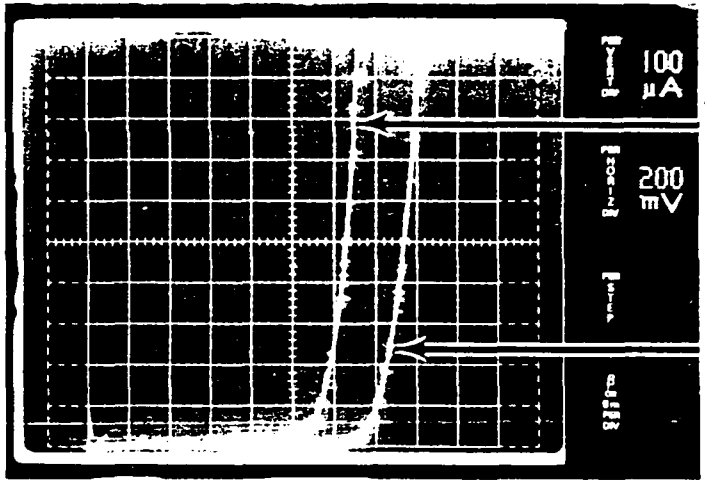


HETEROJUNCTION BIPOLAR TRANSISTOR
1 W CW UNIT CELL

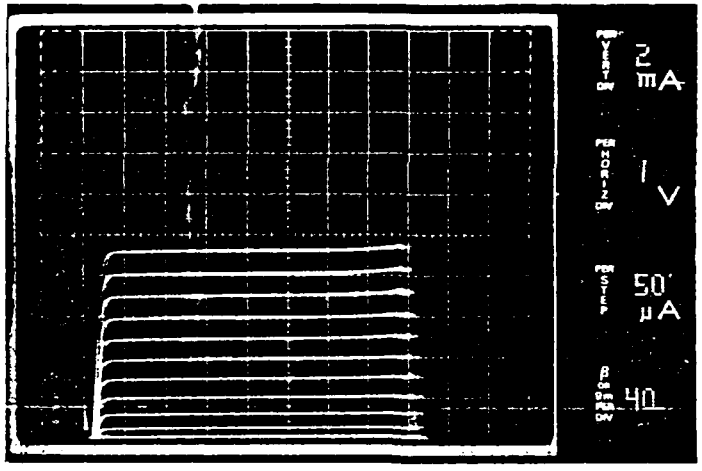


MBE GROWN STRUCTURE



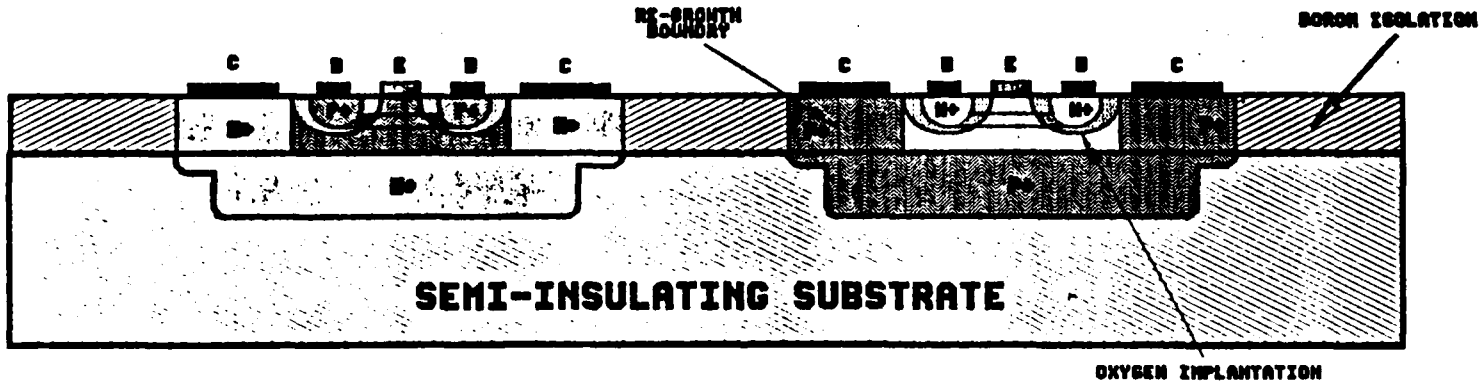


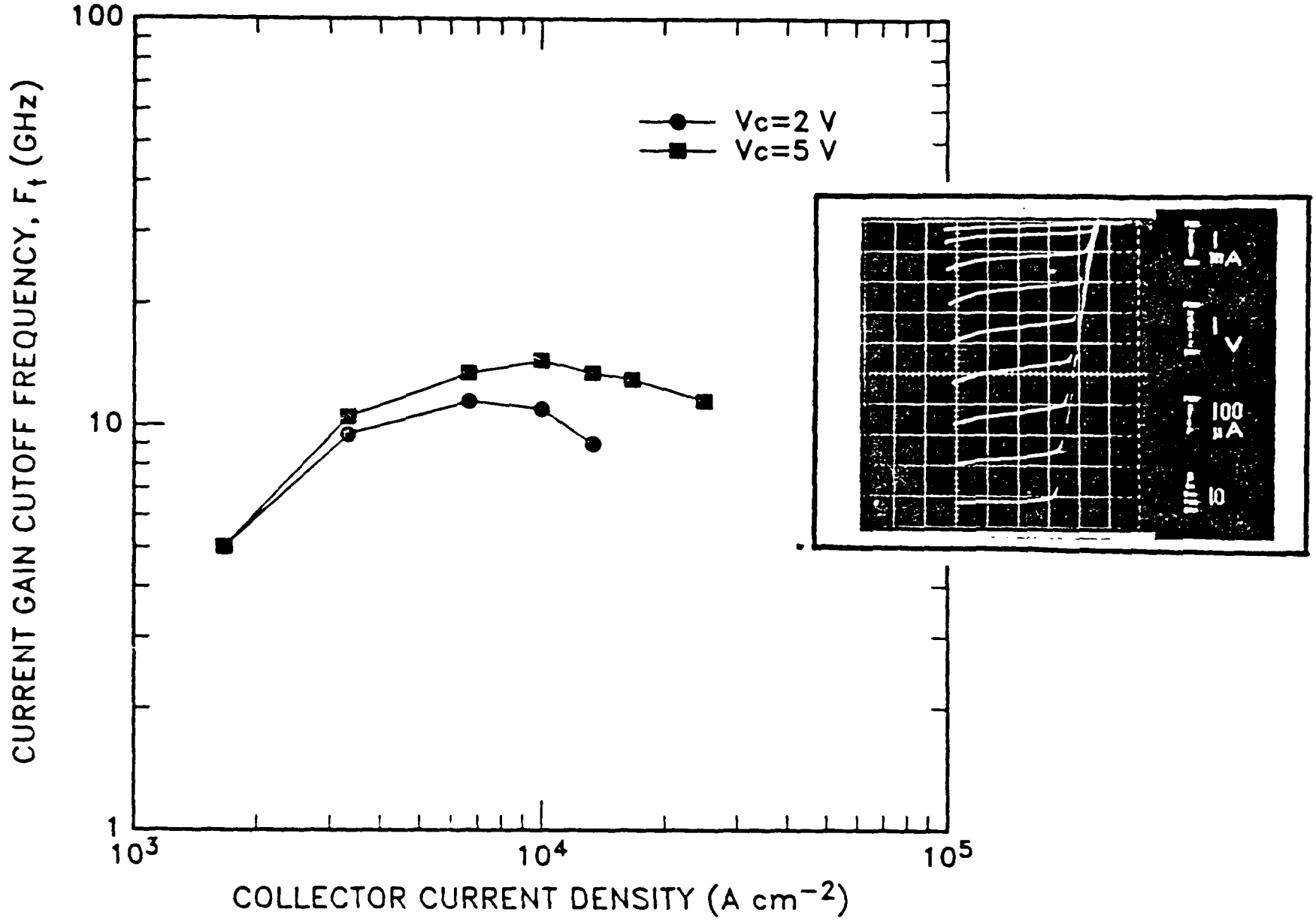
MOCVD GROWN STRUCTURE



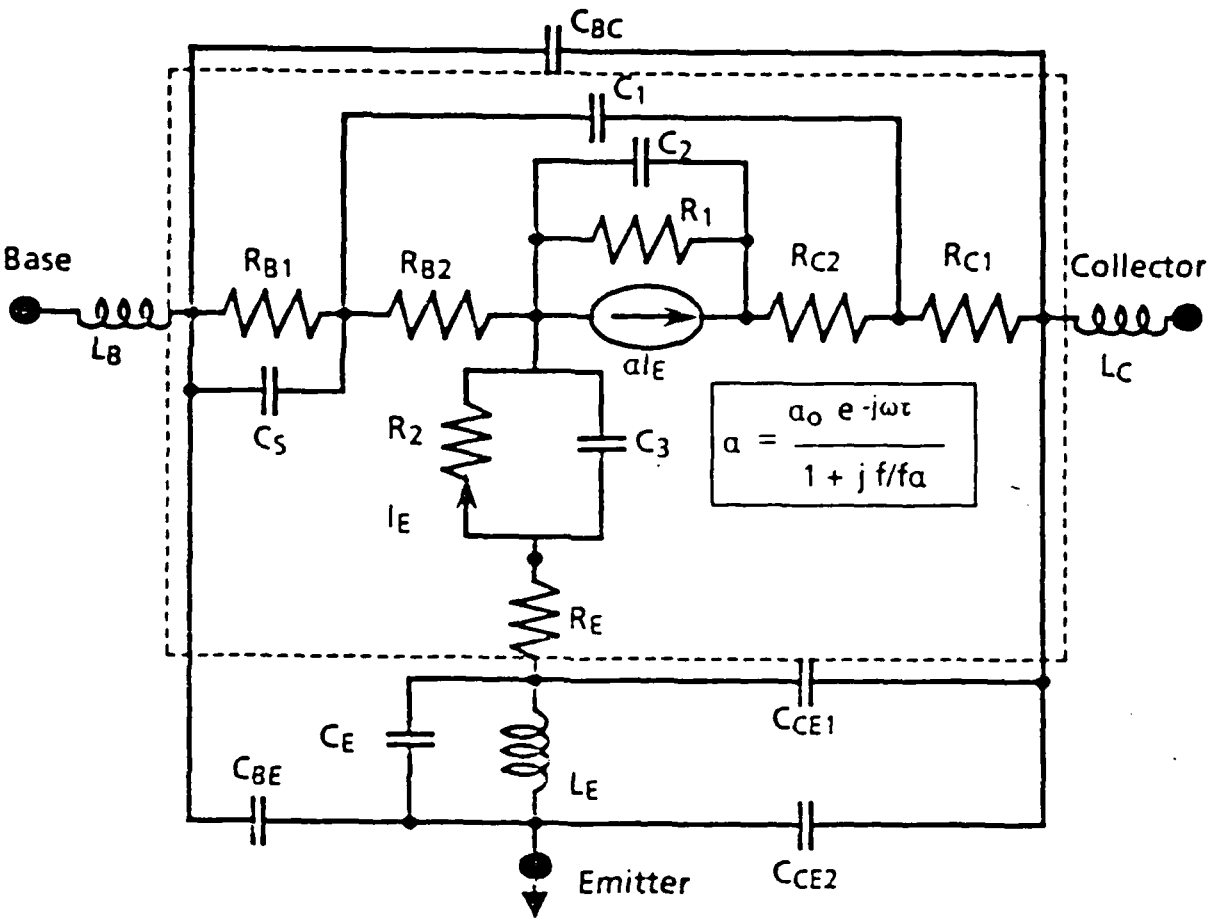
TEXAS INSTRUMENTS

PLANAR COMPLEMENTARY HBT STRUCTURE

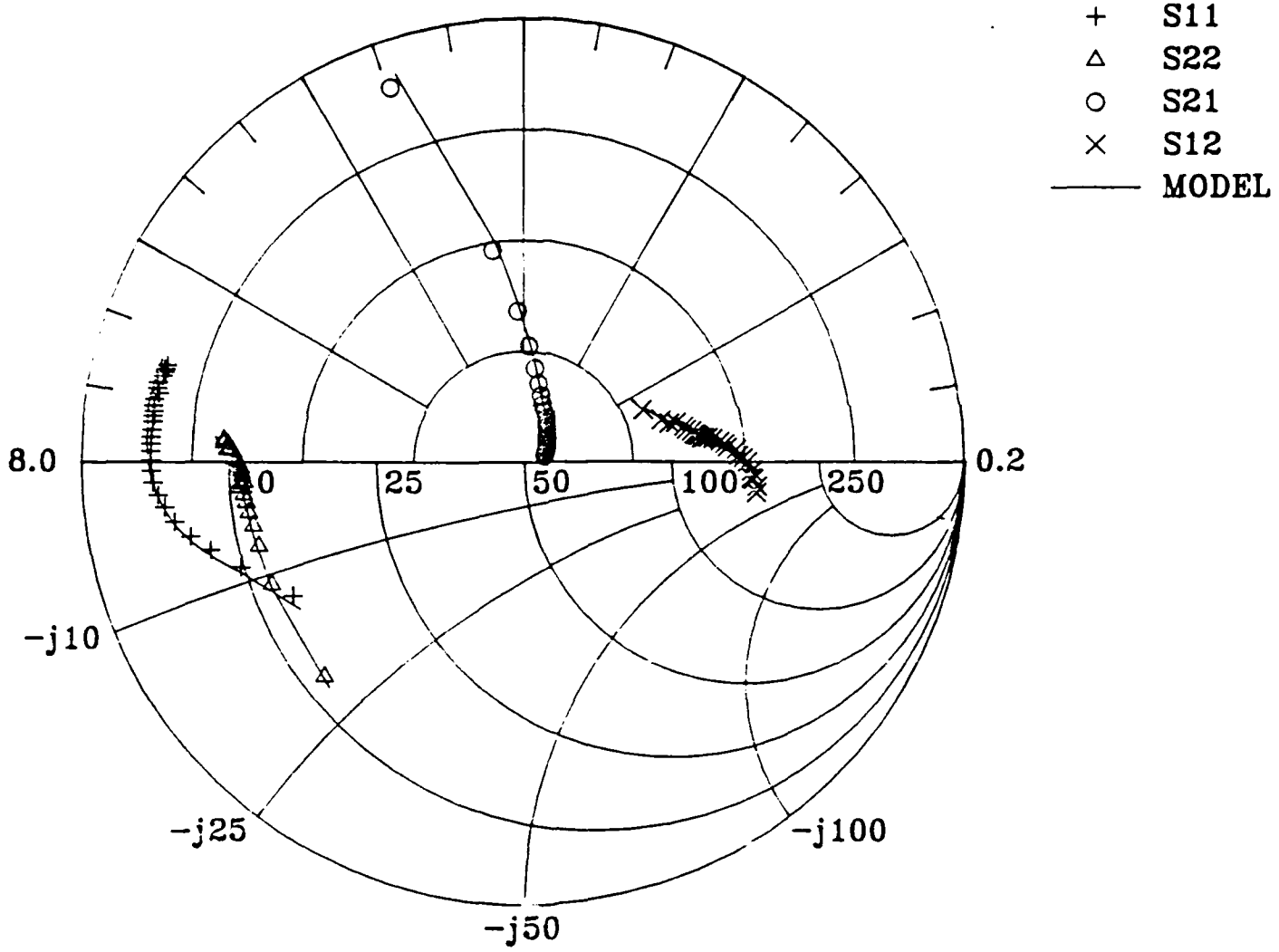



100
10
1
10^3
10^4
10^5
CURRENT GAIN CUTOFF FREQUENCY, F_t (GHz)
COLLECTOR CURRENT DENSITY (A cm^{-2})
Vc=2 V
Vc=5 V
1 mA
1 V
100 μA
10

THE EQUIVALENT CIRCUIT

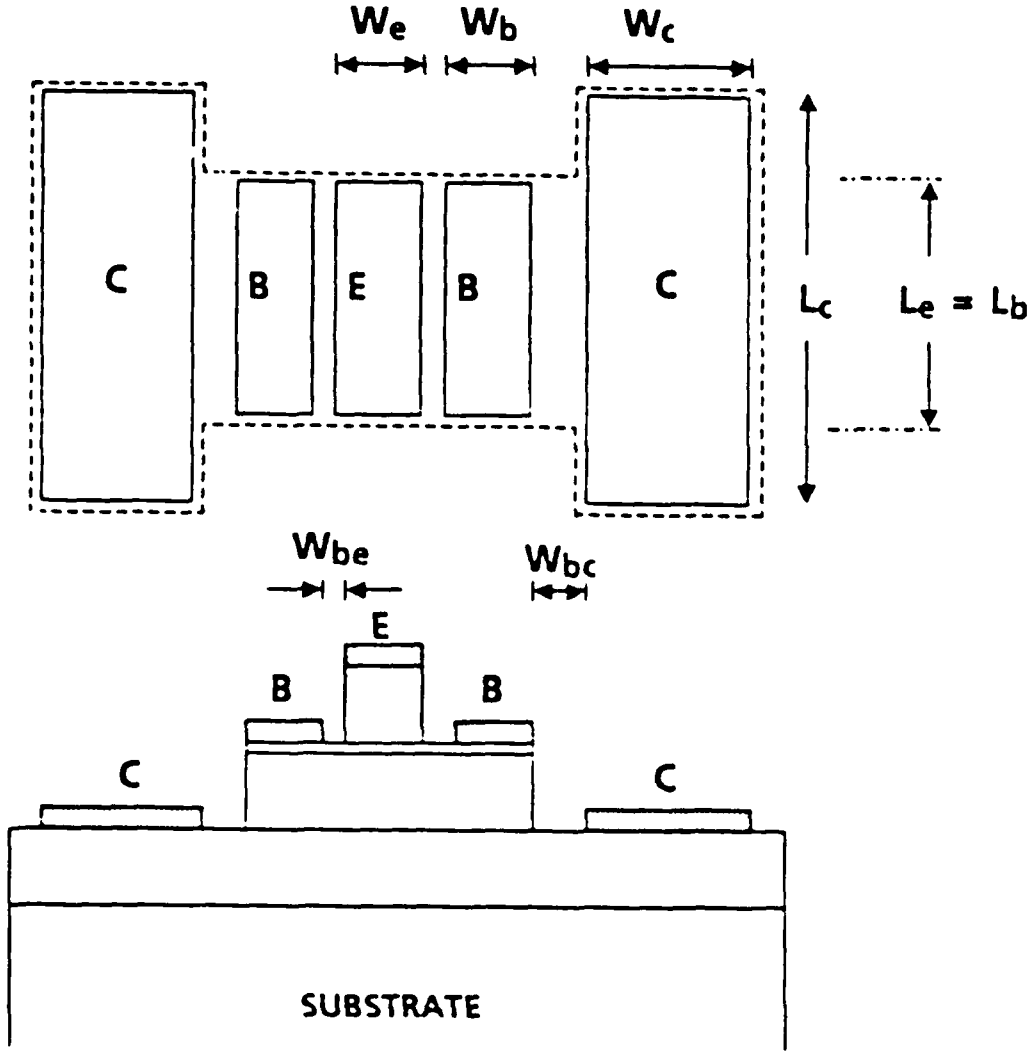


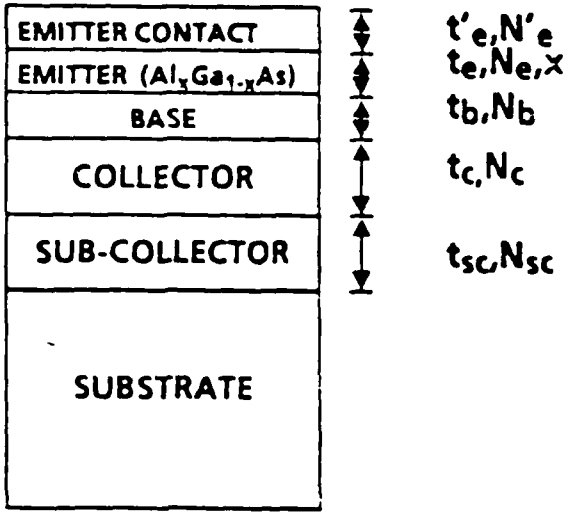
NPN HBT (138B-B5)



COMMON-EMITTER

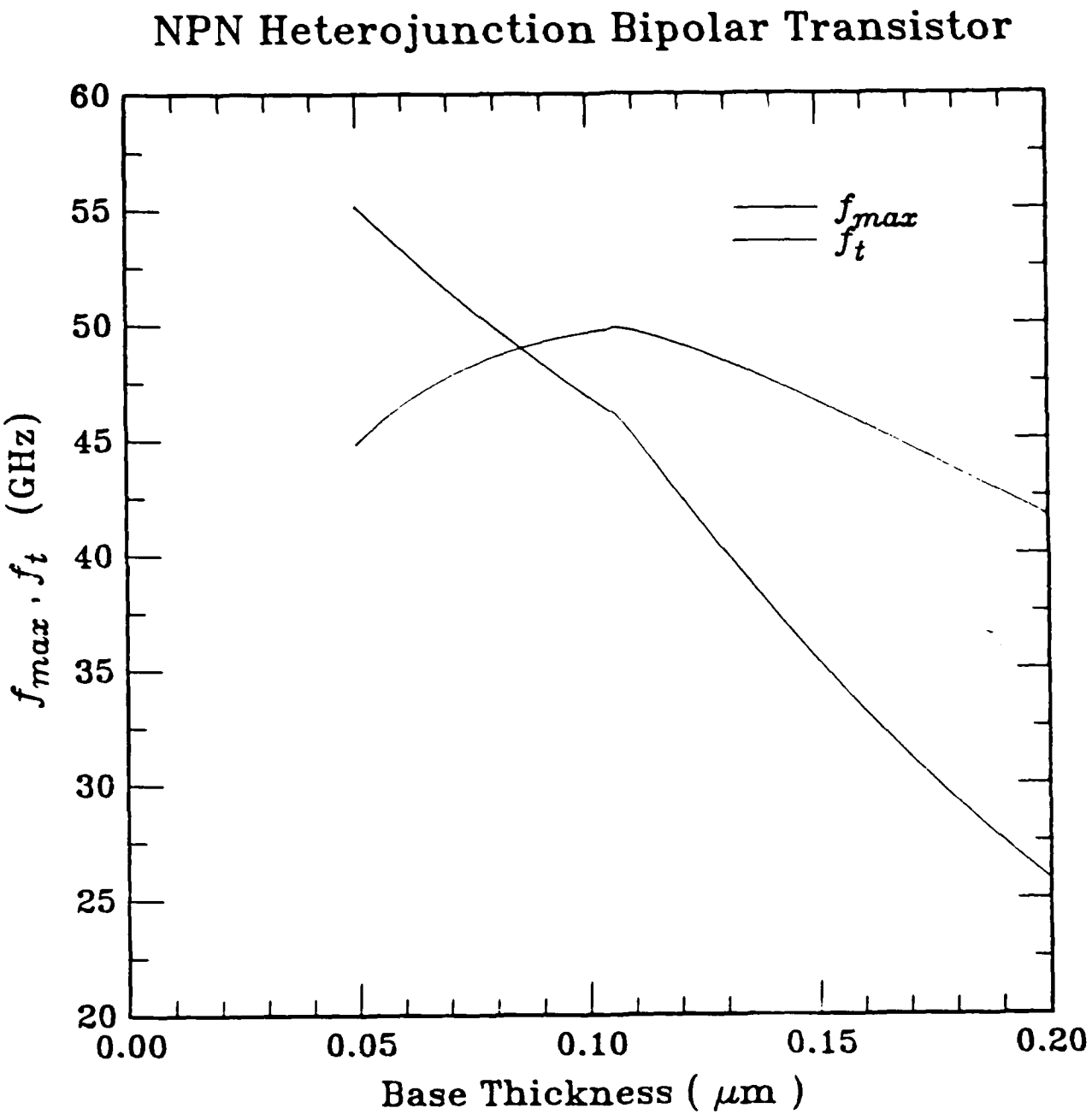
PARAMETERS FOR SMALL-SIGNAL HBT MODEL



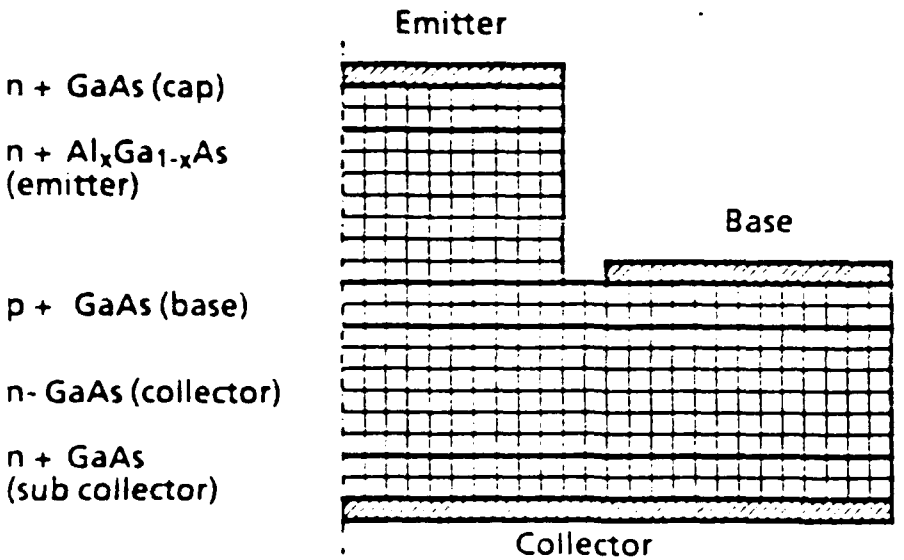


OTHER PARAMETERS

EMITTER CONTACT RESISTIVITY	$= \rho_e$
BASE CONTACT RESISTIVITY	$= \rho_b$
COLLECTOR CONTACT RESISTIVITY	$= \rho_c$
TEMPERATURE	$= T$
BIAS CONDITIONS	$= V_{bc}, I_c$


NPN Heterojunction Bipolar Transistor
60
55
50
45
40
35
30
25
20
f_{max}
f_t
f_{max} , f_t (GHz)
0.00
0.05
0.10
0.15
0.20
Base Thickness (μm)

TWO - DIMENSIONAL NUMERICAL HBT MODEL

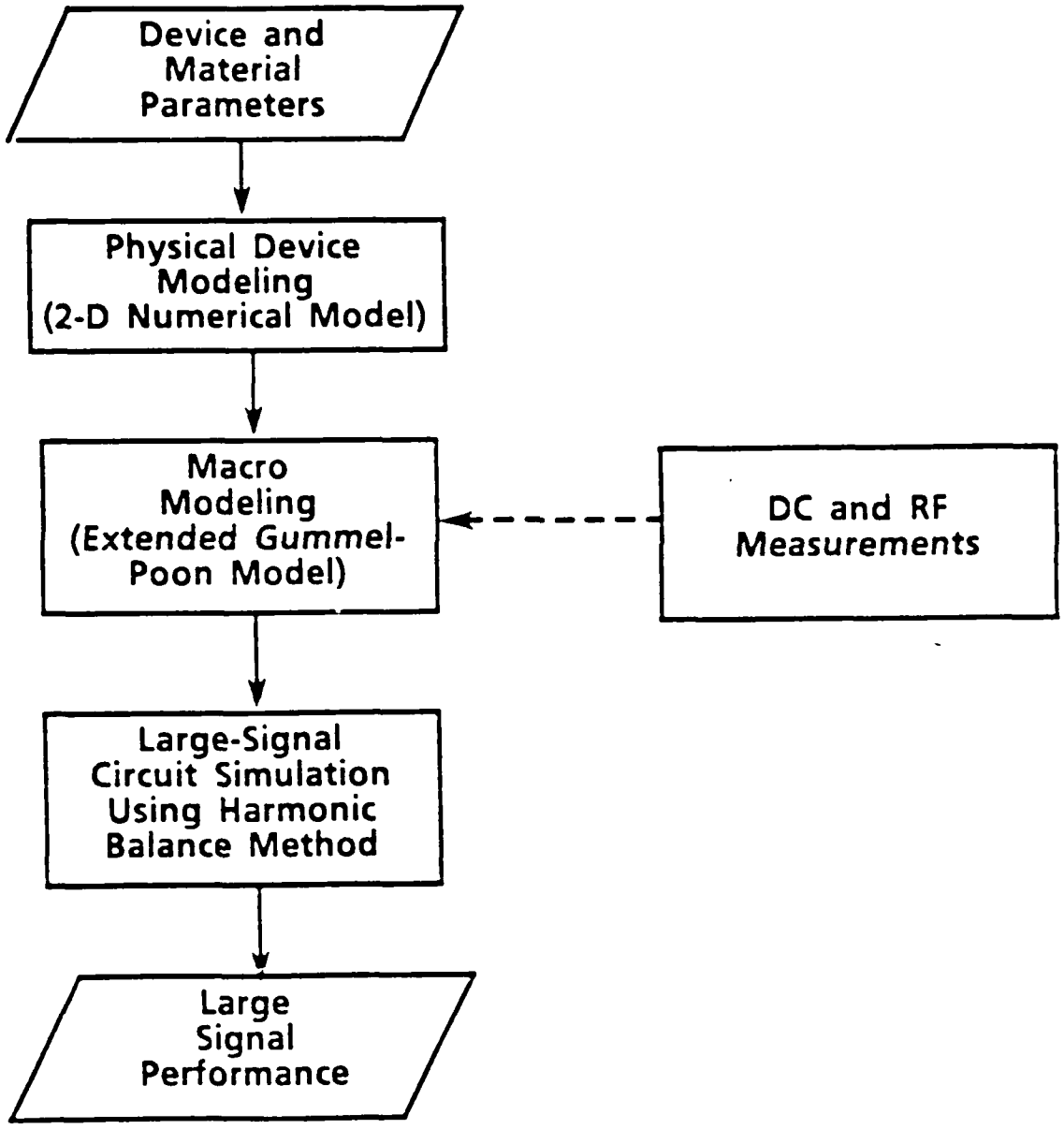


FEATURES:

- Finite difference model with variable mesh size.
- Drift and diffusion current transport model.
- Impact ionization generation and bulb and surface recombination considered.
- Arbitrary heterostructure layers (effects of bandgap grading in the base and at the base-emitter junction can be studied).

OUTPUT:

- Current and electric field distribution.
- Electrode currents and current gain (β).
- Breakdown voltage.
- Capacitances
- Transit time.
- Macromodel (Gummel-Poon) parameters for large signal circuit analysis.


Device and Material Parameters
Physical Device Modeling (2-D Numerical Model)
Macro Modeling (Extended Gummel-Poon Model)
DC and RF Measurements
Large-Signal Circuit Simulation Using Harmonic Balance Method
Large Signal Performance

SUMMARY

- STRAINED-LAYER GaAs/InGaAs/AlGaAs HBT STRUCTURES WERE GROWN BY MBE AND MOCVD. DEVICE PERFORMANCE WAS EVALUATED.
- InGaAs/InAlAs HBT STRUCTURE WAS GROWN ON InP SUBSTRATE
- A COMPREHENSIVE SMALL-SIGNAL DEVICE MODEL WAS DEVELOPED.

On Wafer Characterization of High Speed Circuits

D. M. Bloom

Stanford University
Stanford, CA

On Wafer Characterization of High Speed Circuits

D. M. Bloom
Edward L. Ginzton Laboratory
Stanford University

DARPA Joint Contractor Review of
EHF Monolithic Devices

January 25, 1989

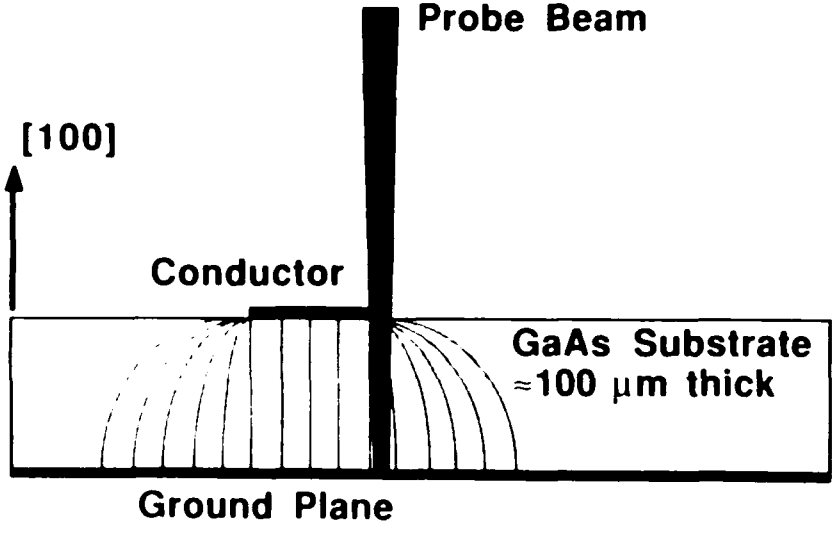
COST GOALS

MIMIC

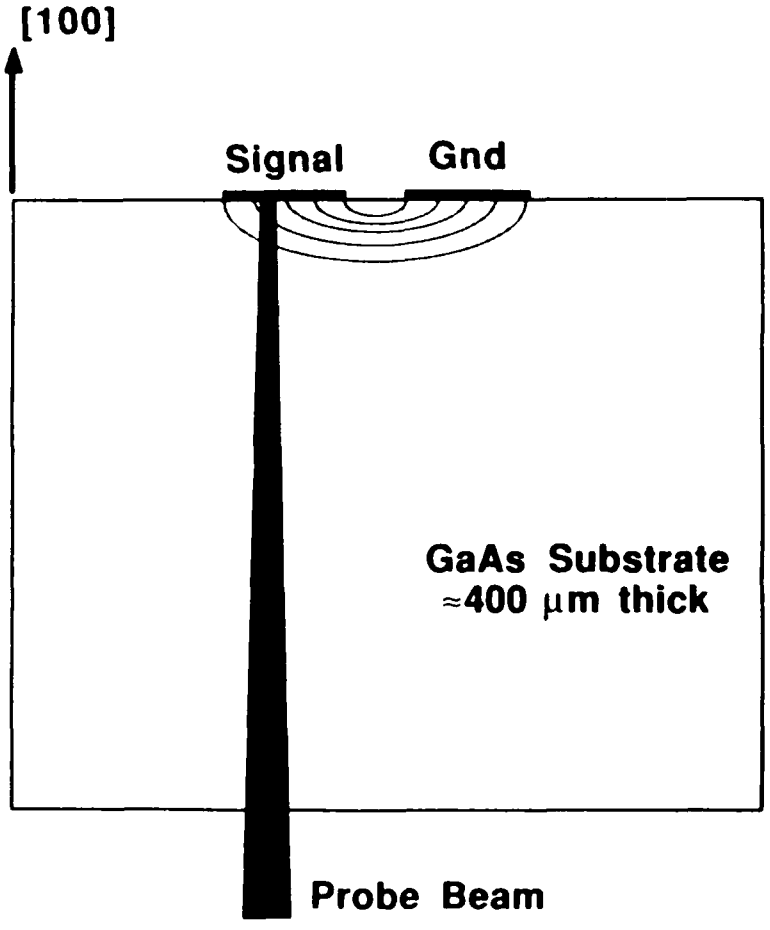
DEMONSTRATE THAT MONOLITHIC DEVICES CAN BE DELIVERED IN FUNCTIONAL MODULES AT:

- $2.50 CHIP COST, IN A
- $25 PACKAGE, WITH LESS THAN
- $250 OF TEST DATA

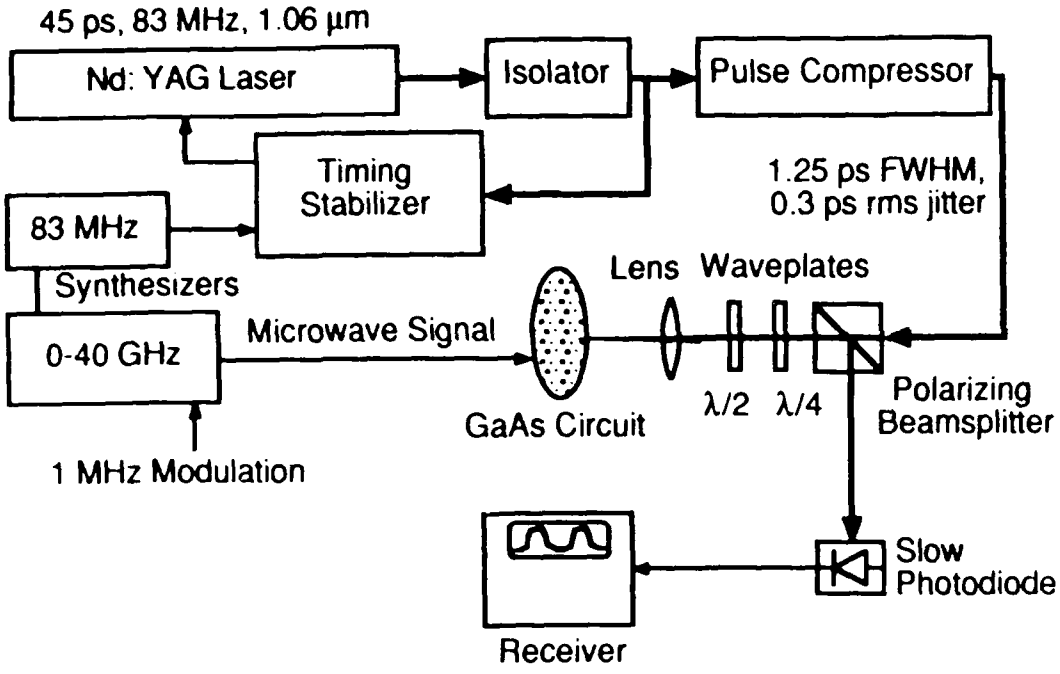
Frontside Probing

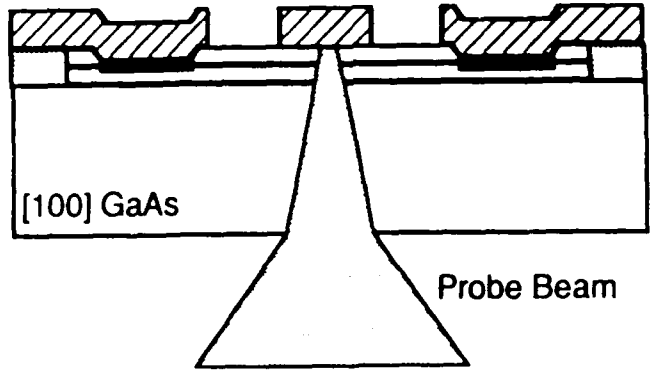


Backside Probing

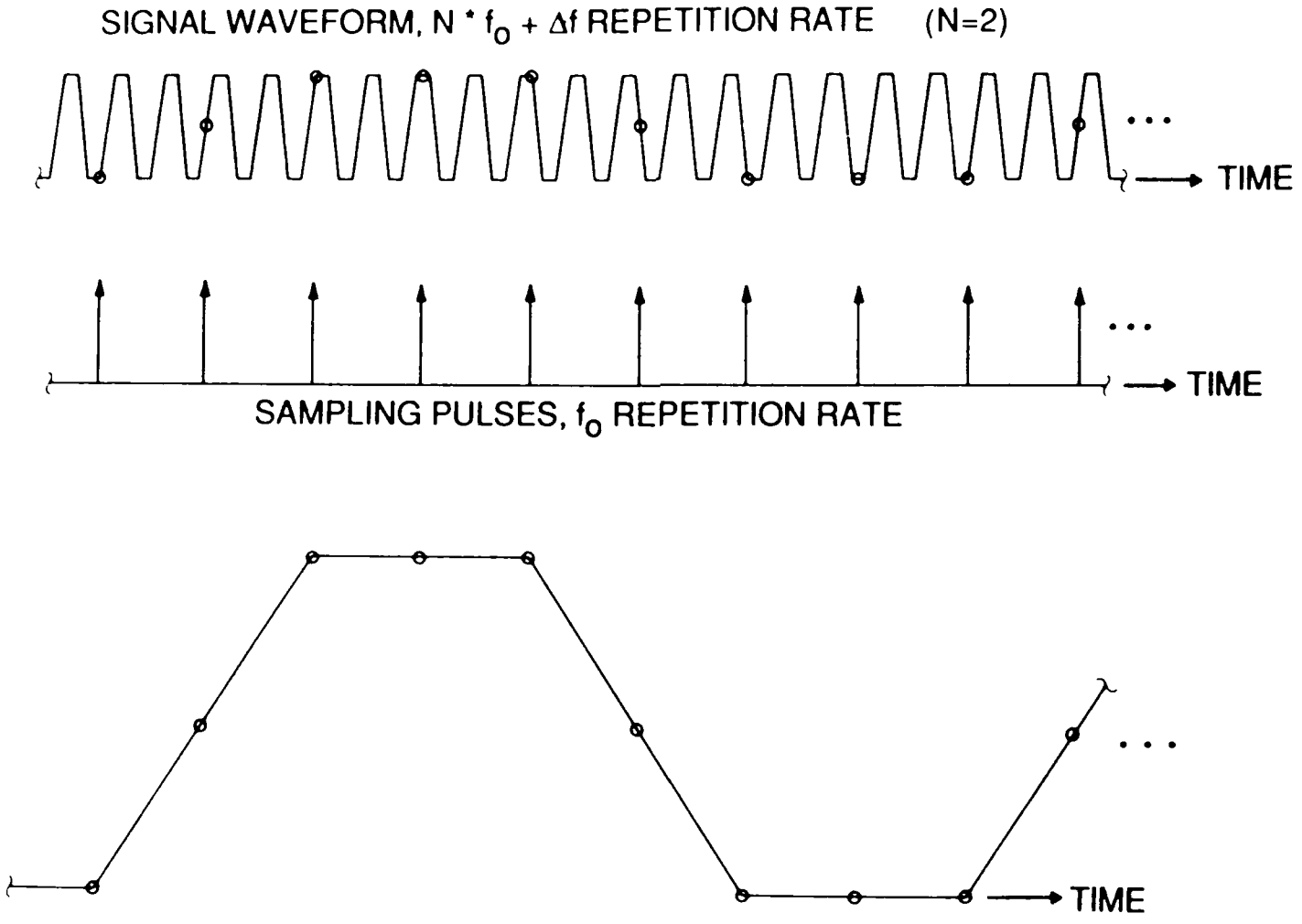


Electrooptic Sampling

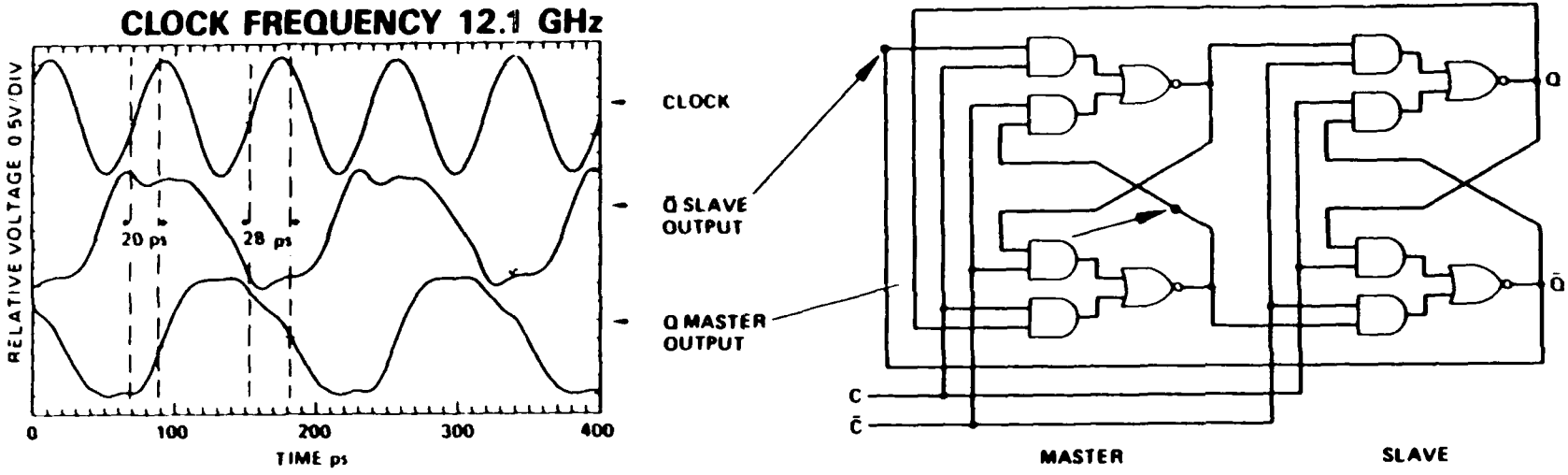




Equivalent-time sampling



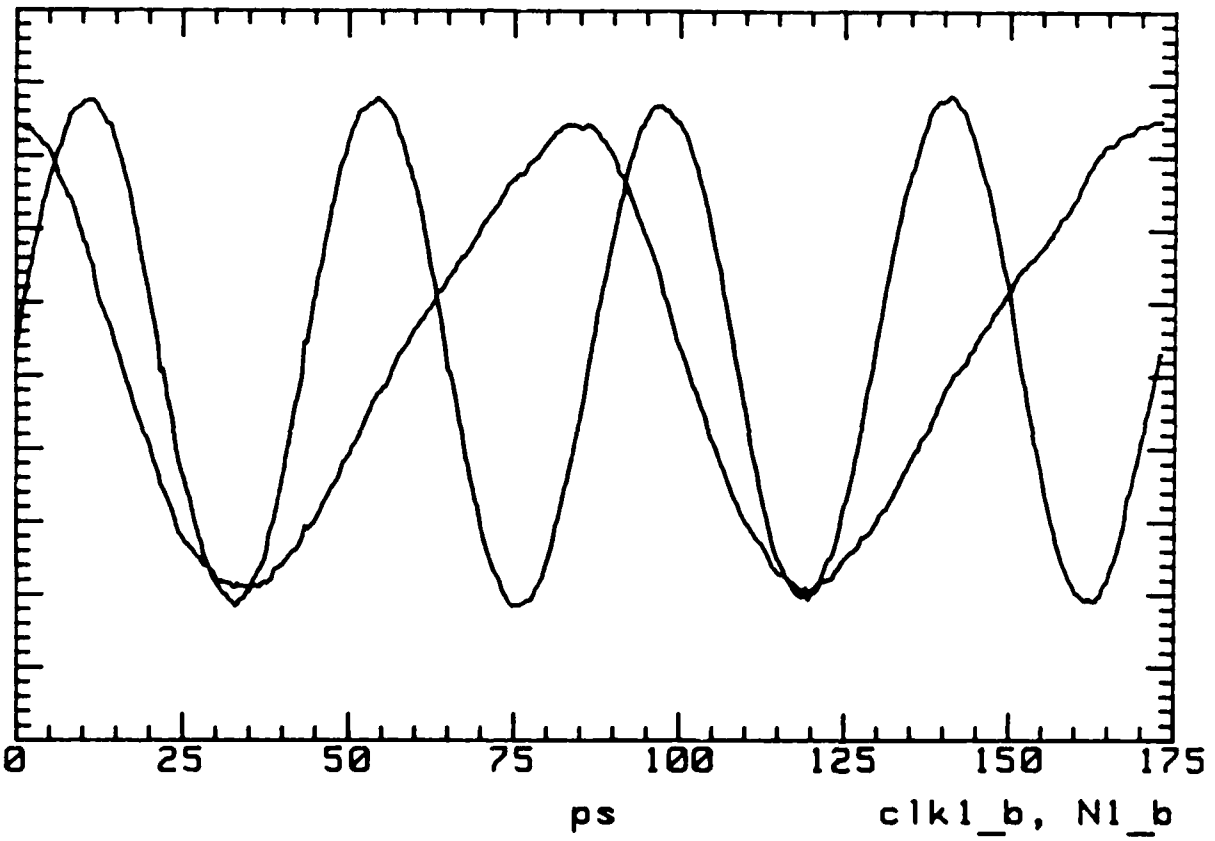
CEL DIVIDER ELECTROOPTIC SAMPLED WAVEFORMS



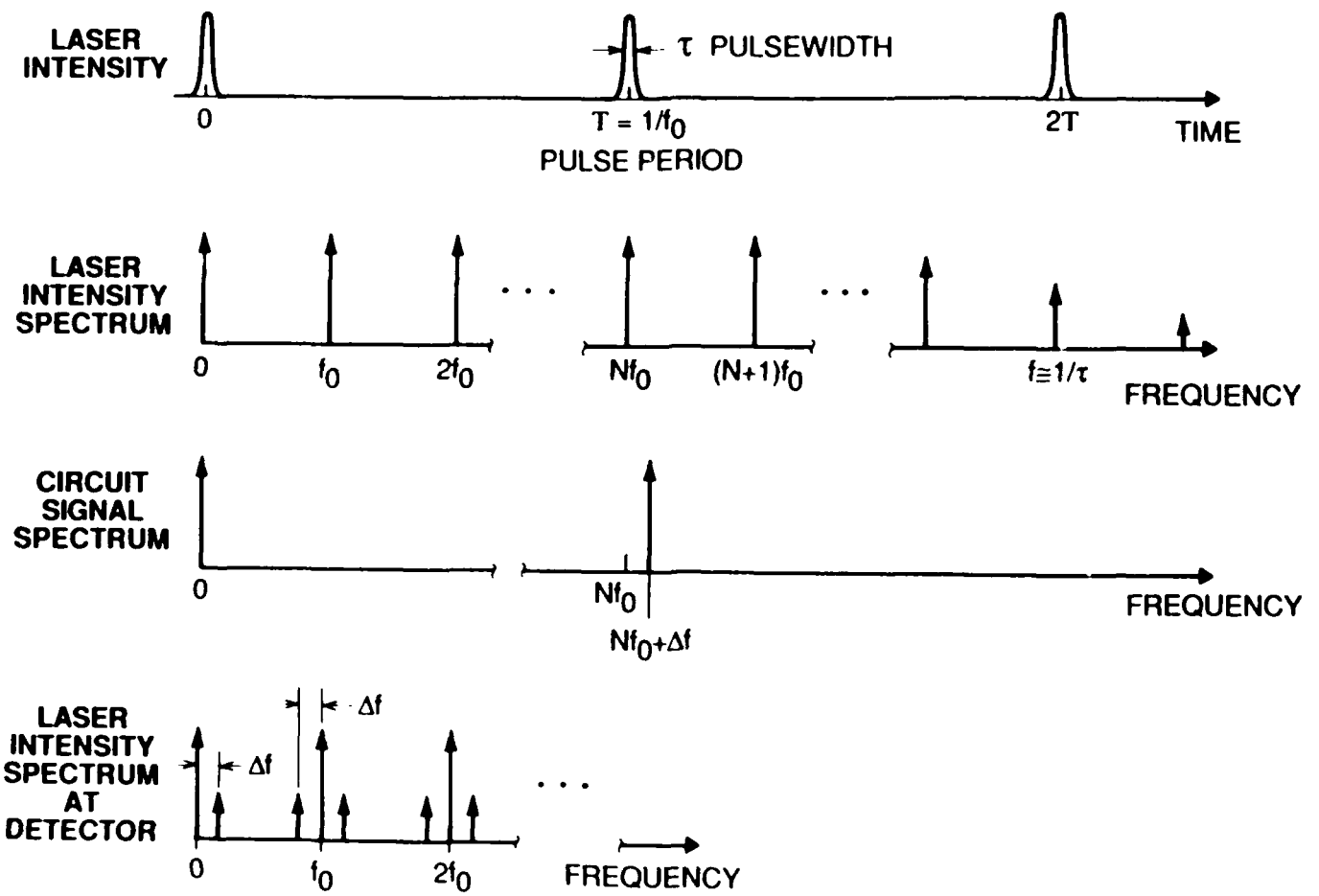
INDIRECT MEASUREMENT OF MAXIMUM CLOCK FREQUENCY = 17.9 GHz

ELECTROOPTIC MEASUREMENT PREDICTS MAXIMUM CLOCK FREQUENCY = 17.9 GHz

BFL dynamic divider, 23 GHz operation

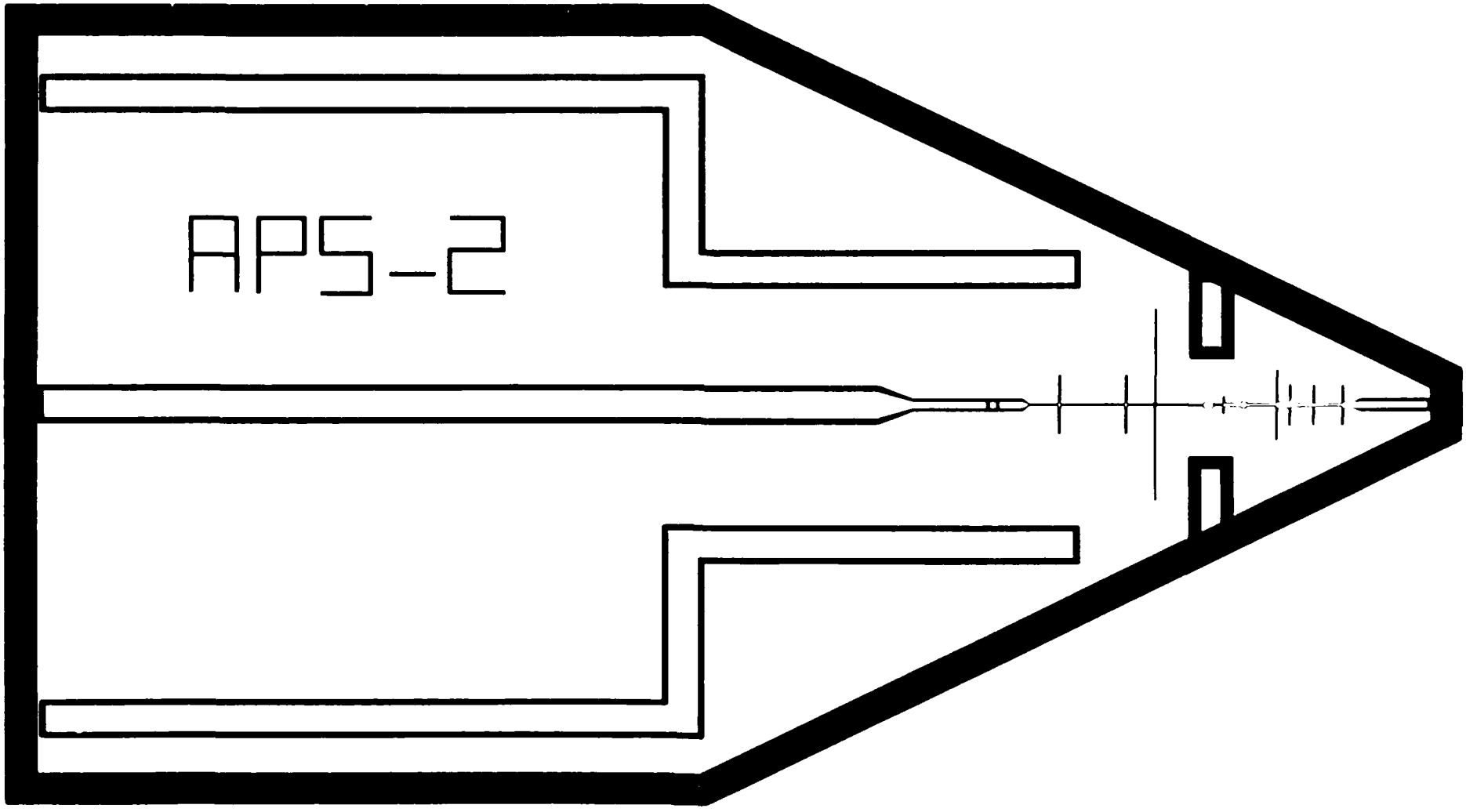


Harmonic mixing

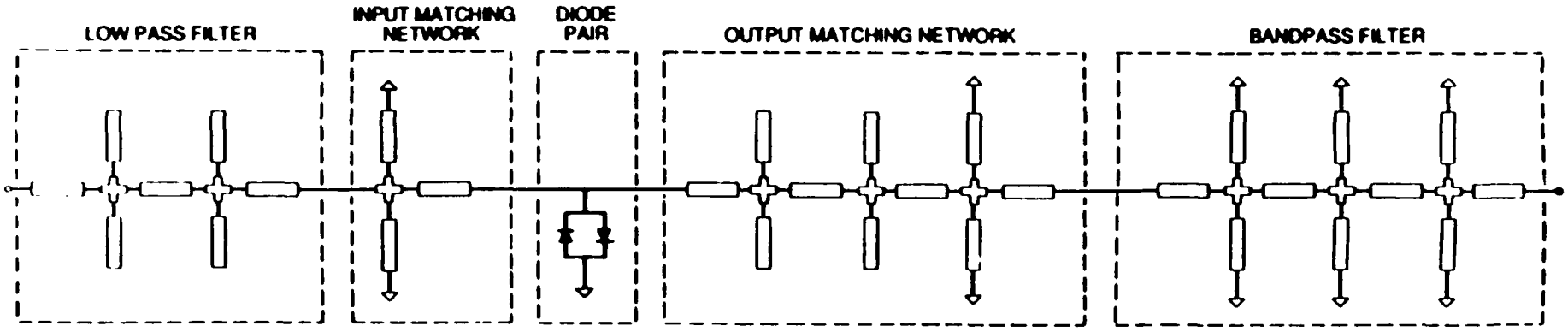


Millimeter-Wave Active Probe Quintupler

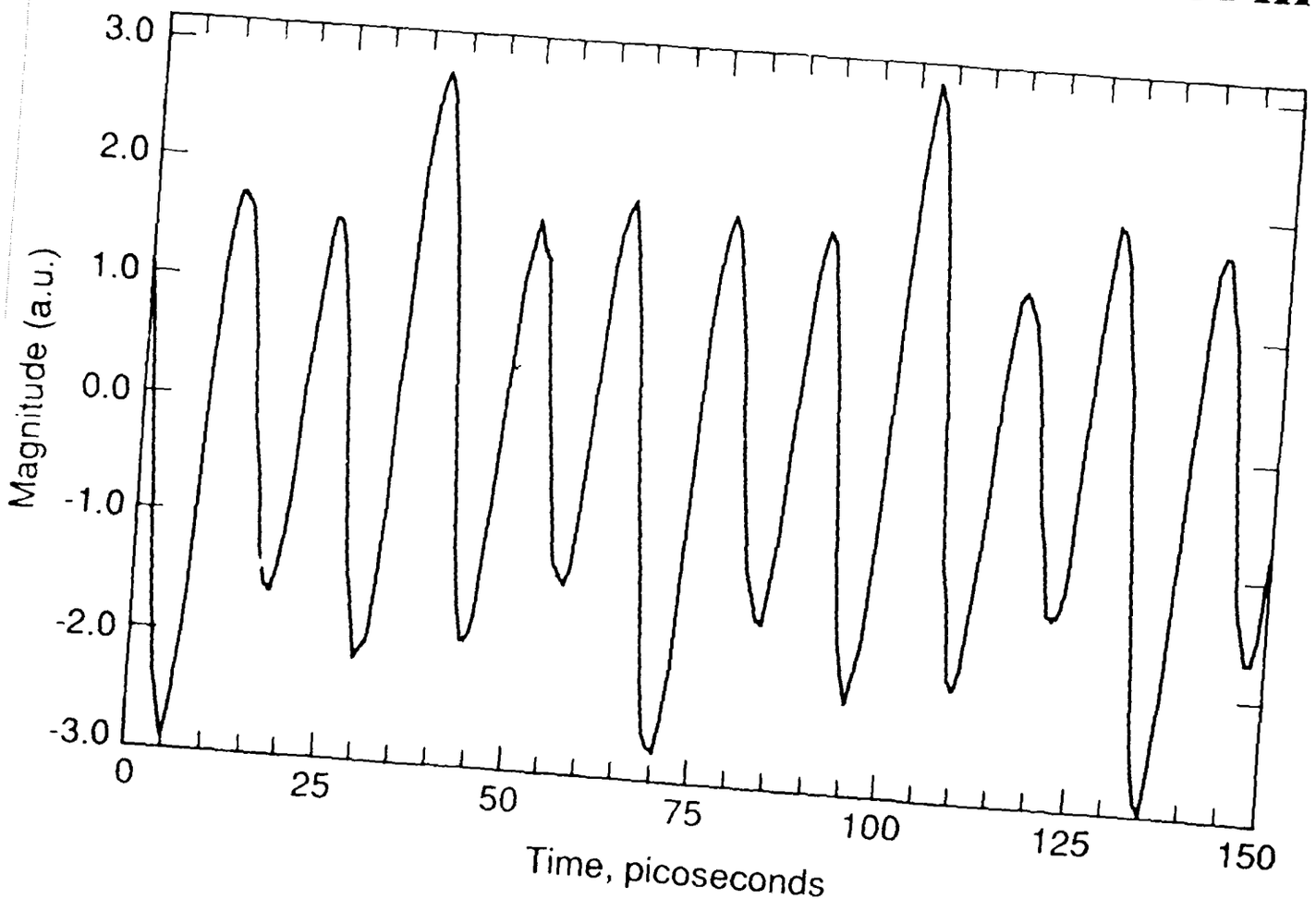
Output Frequency : 60-100 GHz



Active Probe Quintupler Schematic



77 GHz Active Probe Waveform



n + GaAs

n + Al_xGa
(emitter)

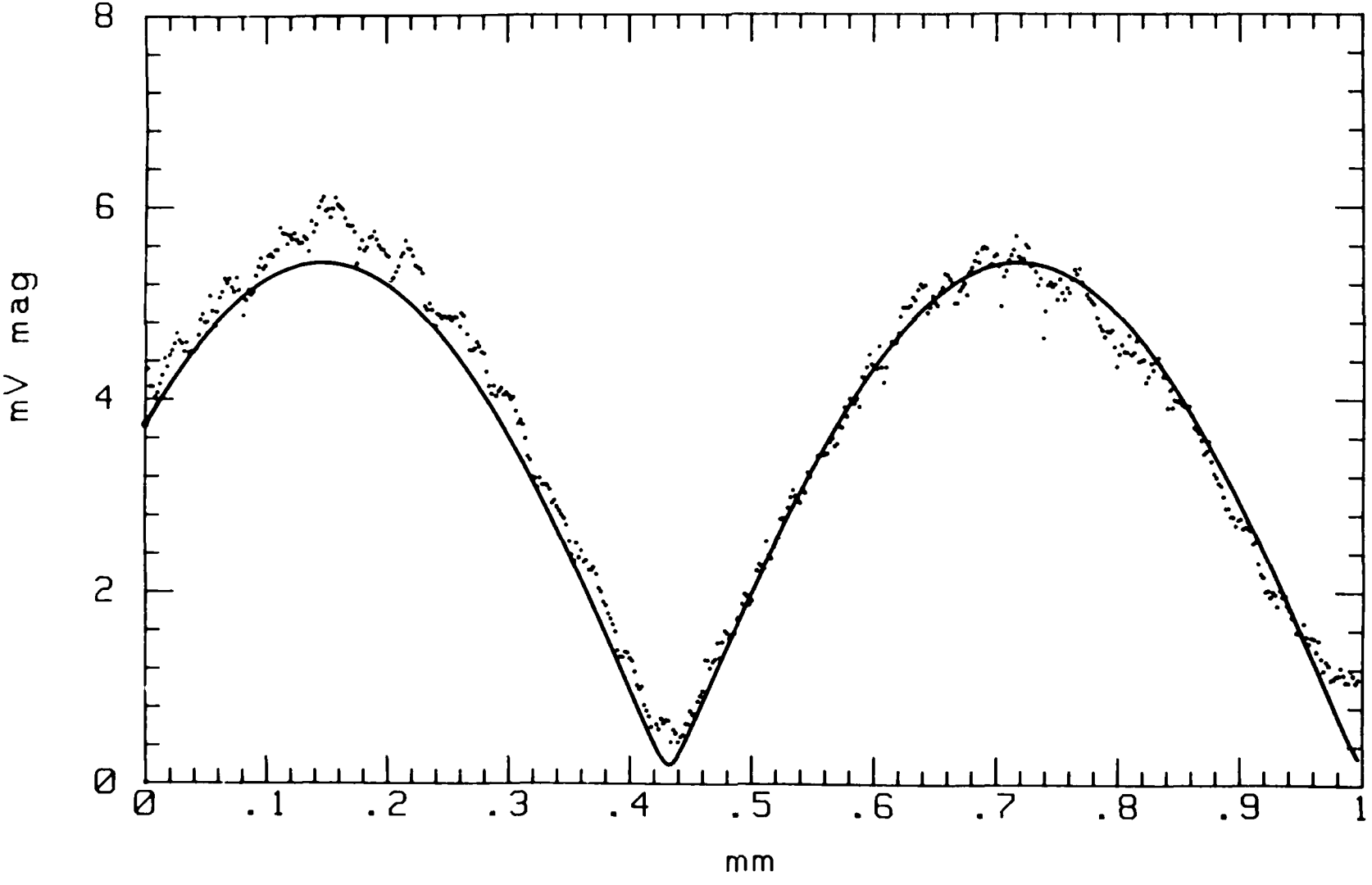
p + GaAs

n- GaAs (

n + GaAs
(sub colle

100 GHz CPW Standing Wave

Γ=0.93 @ -94°

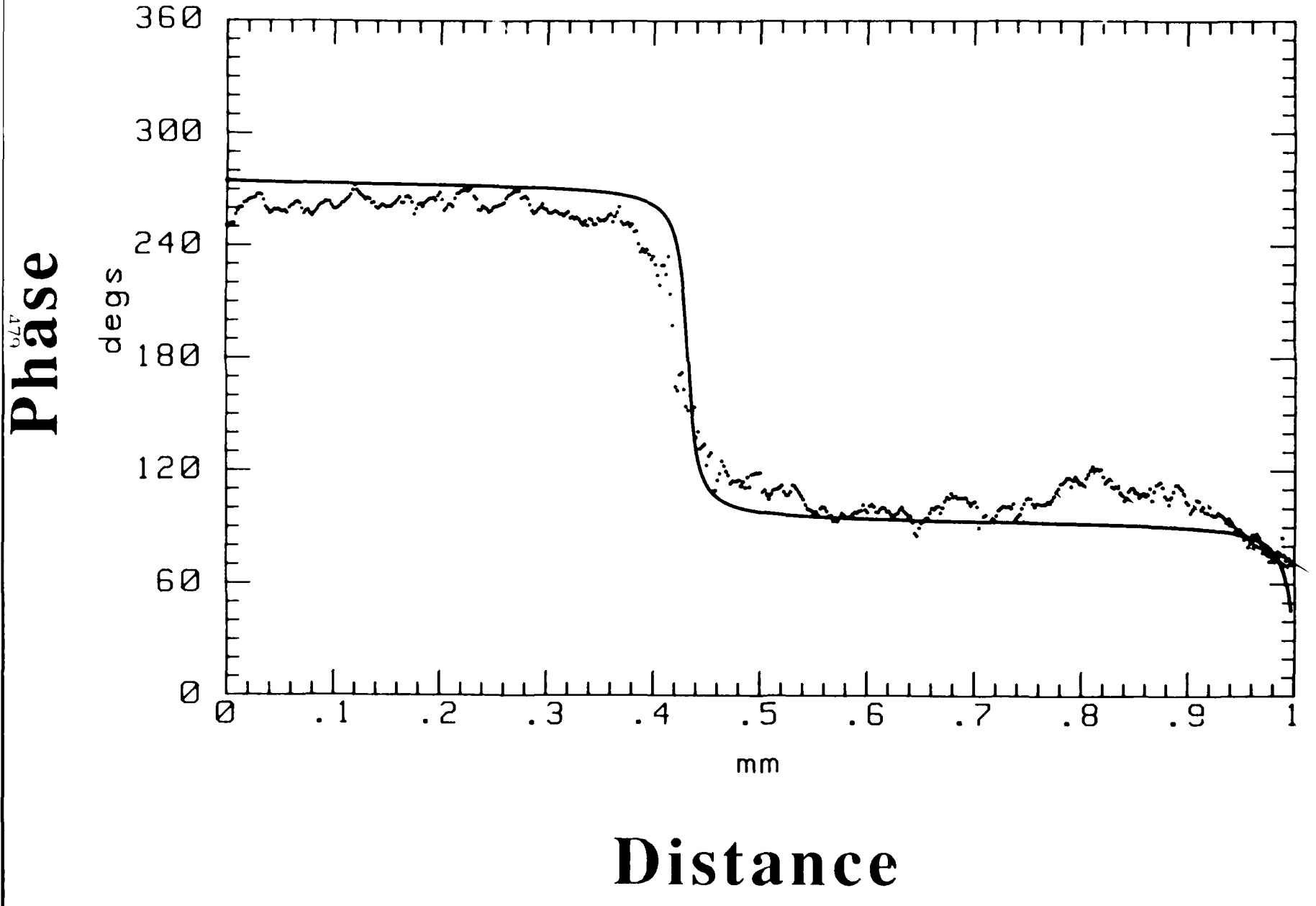


Magnitude

Distance

100 GHz CPW Standing Wave

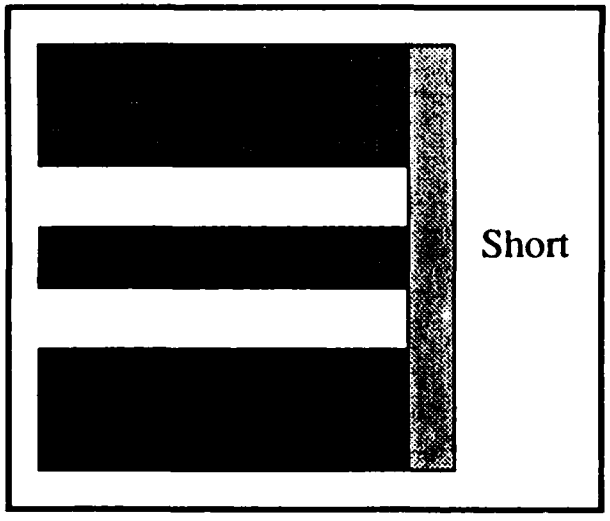
Γ=0.93 @ -94°

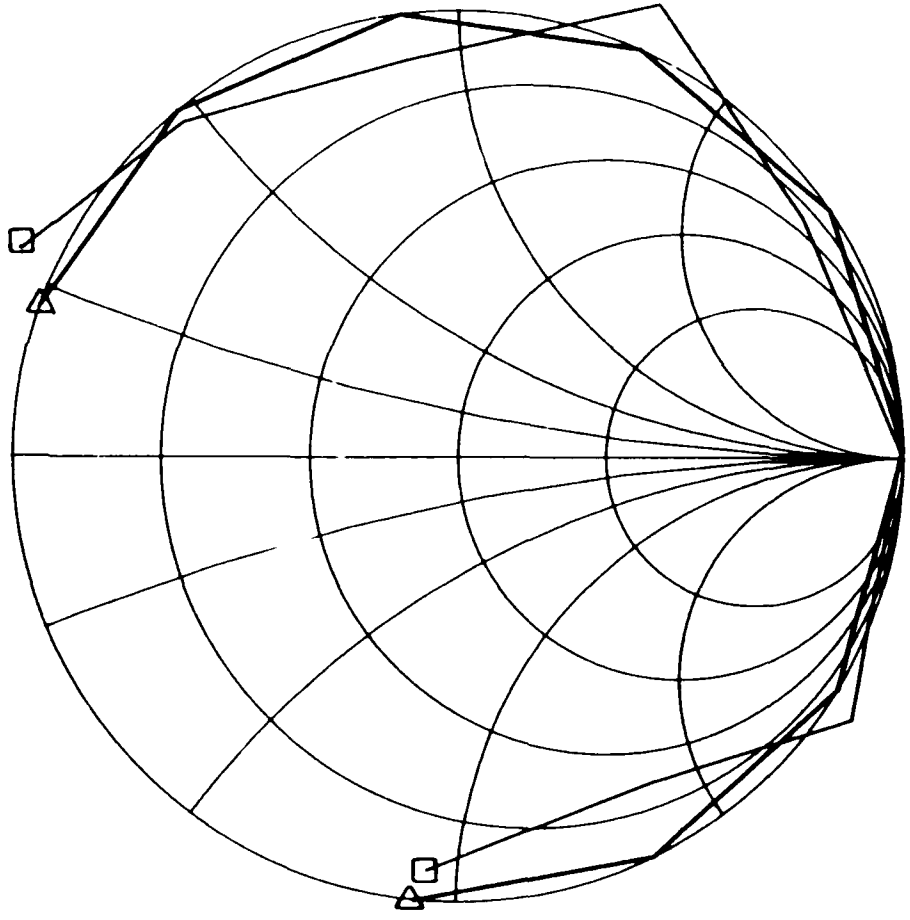


60-100 GHz S11 Measurements

△ S11
MODEL

□ S11
MEASURED



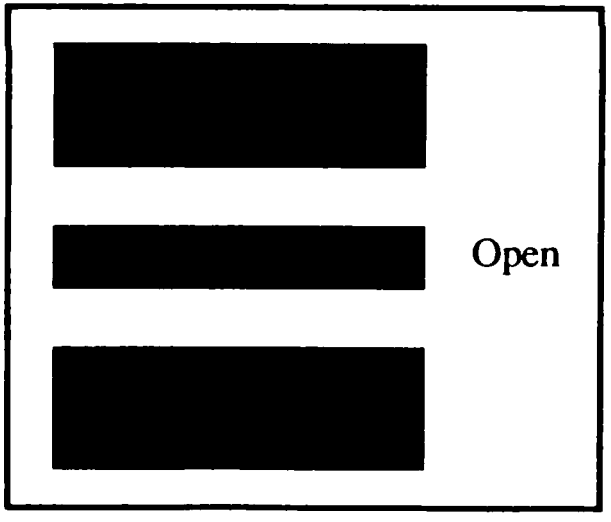


f1: 60.0000
f2: 100.000

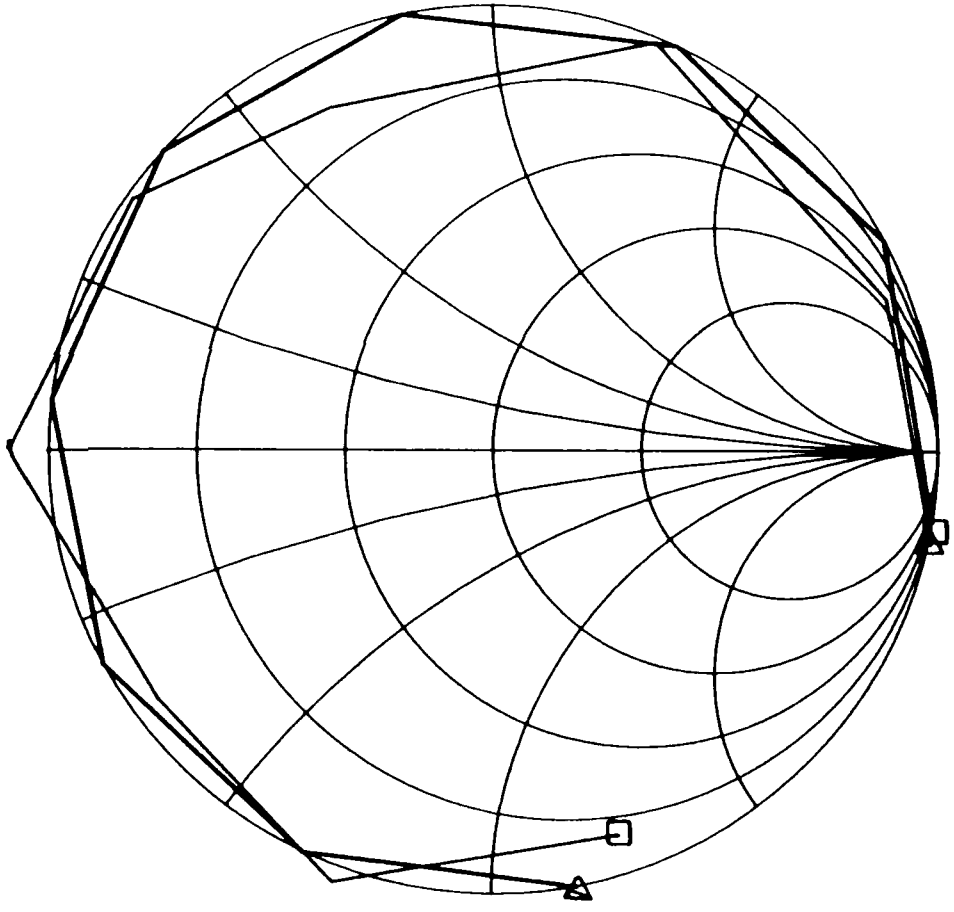
60-100 GHz S11 Measurements

△ S11
MODEL

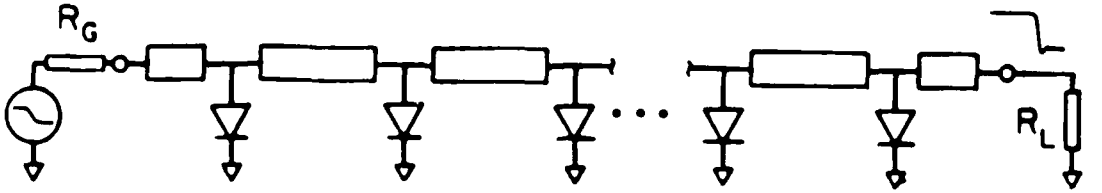
□ S11
MEASURED

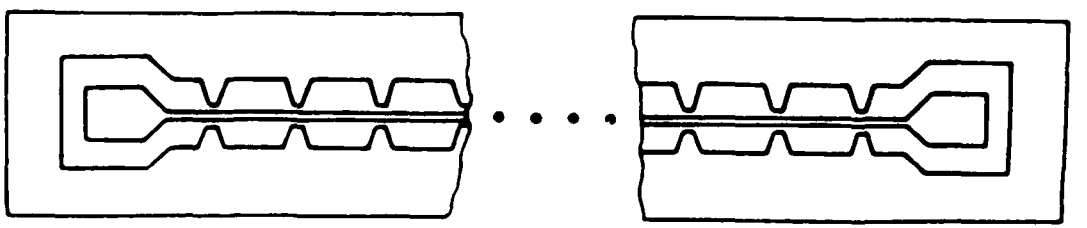


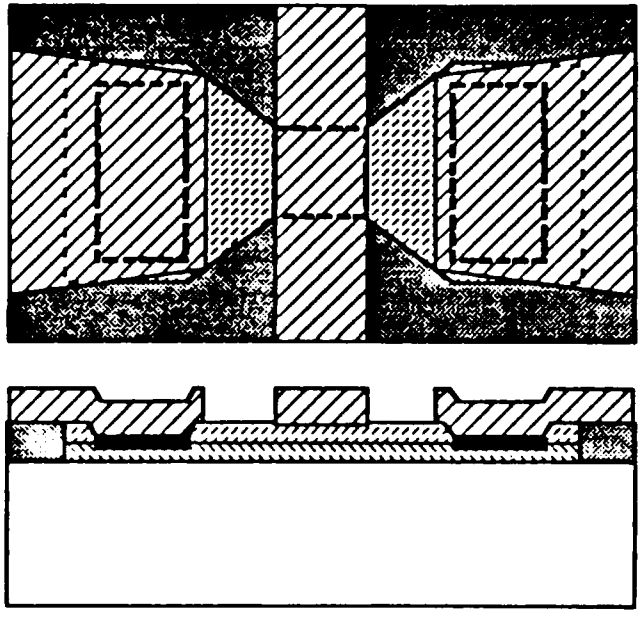
f1: 60.0000
f2: 100.000



Nonlinear Transmission Line







Schottky & Interconnect Metal

Ohmic Metal

N- Layer

N+ Layer

Semi-Insulating GaAs

Proton Isolation Implant

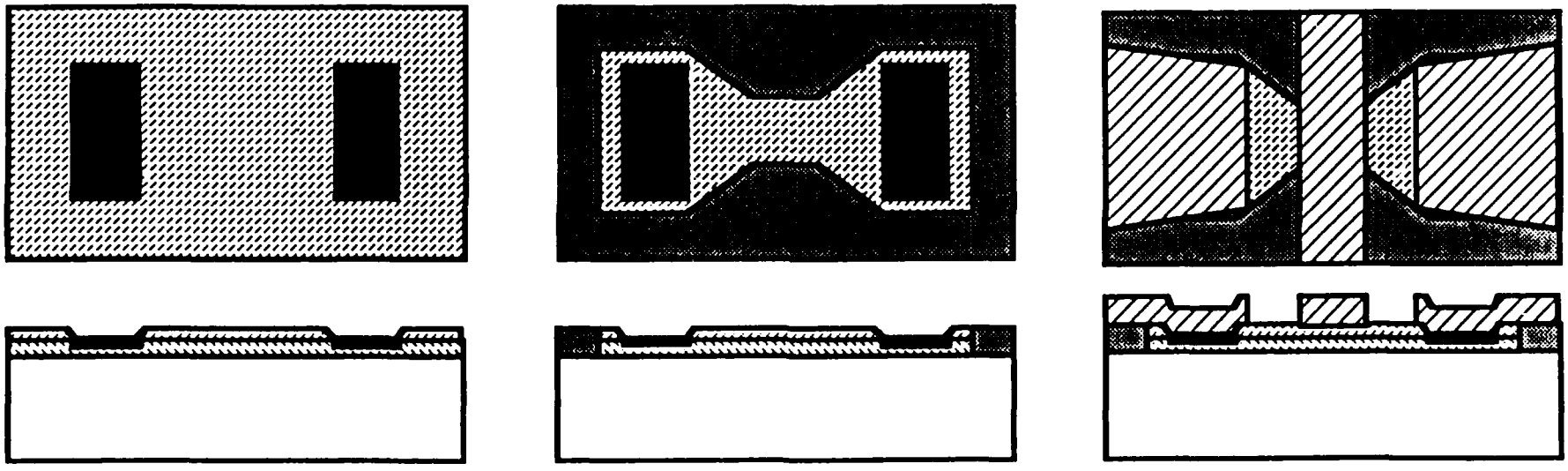
Schottky and Ohmic Contact Regions

Fabrication Sequence

Ohmic Contacts

Isolation

Schottky Contacts
and Interconnect Metal



Schottky & Interconnect Metal

Ohmic Metal

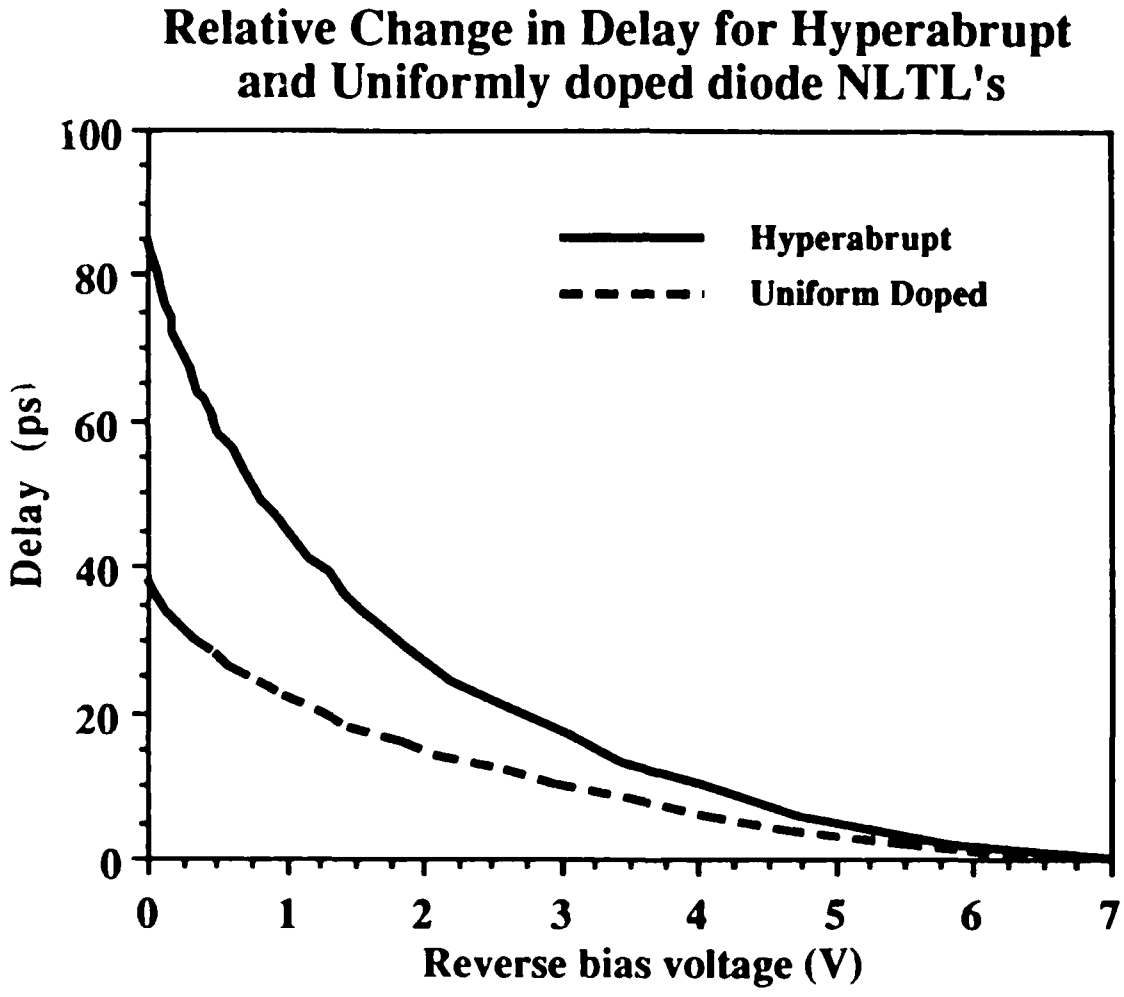
N- Layer

N+ Layer

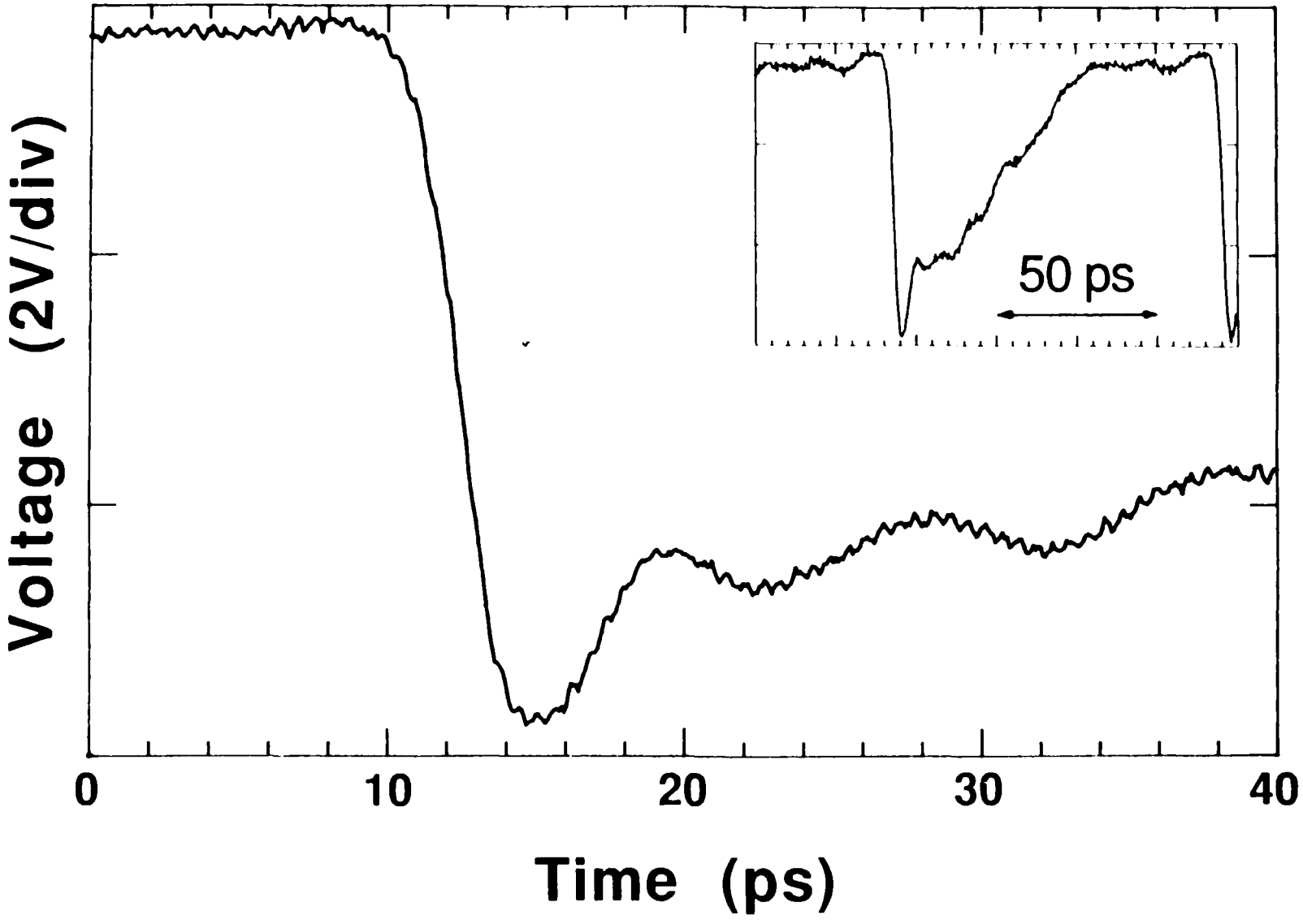
Semi-Insulating GaAs

Proton Isolation Implant

Falltime Compression with 2 Cascaded Lines
Input Signal, 2.0 Volt/div.
Output Signal, 0.5 Volt/div.
Input: 23 dBm, 8 GHz
(37 ps falltime)
Output: 3.5 ps falltime
0
10
20
30
40
50
60
70
80
90
100
Time, picoseconds


Relative Change in Delay for Hyperabrupt and Uniformly doped diode NLTL's
100
80
60
40
20
0
Delay (ps)
Hyperabrupt
Uniform Doped
0
1
2
3
4
5
6
7
Reverse bias voltage (V)

Shock wave on a hyperabrupt diode NLTL with sinusoidal drive



Nonlinear Transmission Line

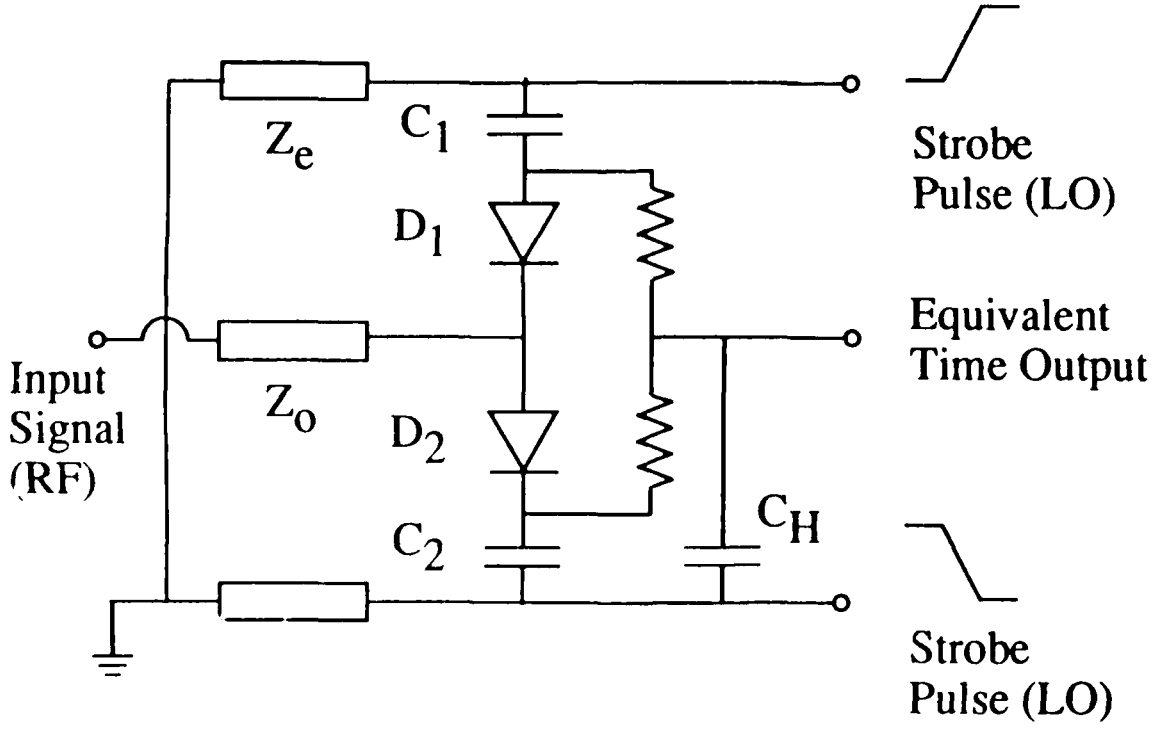
- Picosecond Shock-wave Generation
- Hyperabrupt Diode Design
  - 6 volt Signal Amplitude
  - Approx. 1.5 ps Falltime
- < 1 ps Output Falltime Possible in Future
  - Requires Improvement to Electrooptic Sampler
  - Investigate Circuit Applications

Prior Art in Threshold Devices and Pulsers

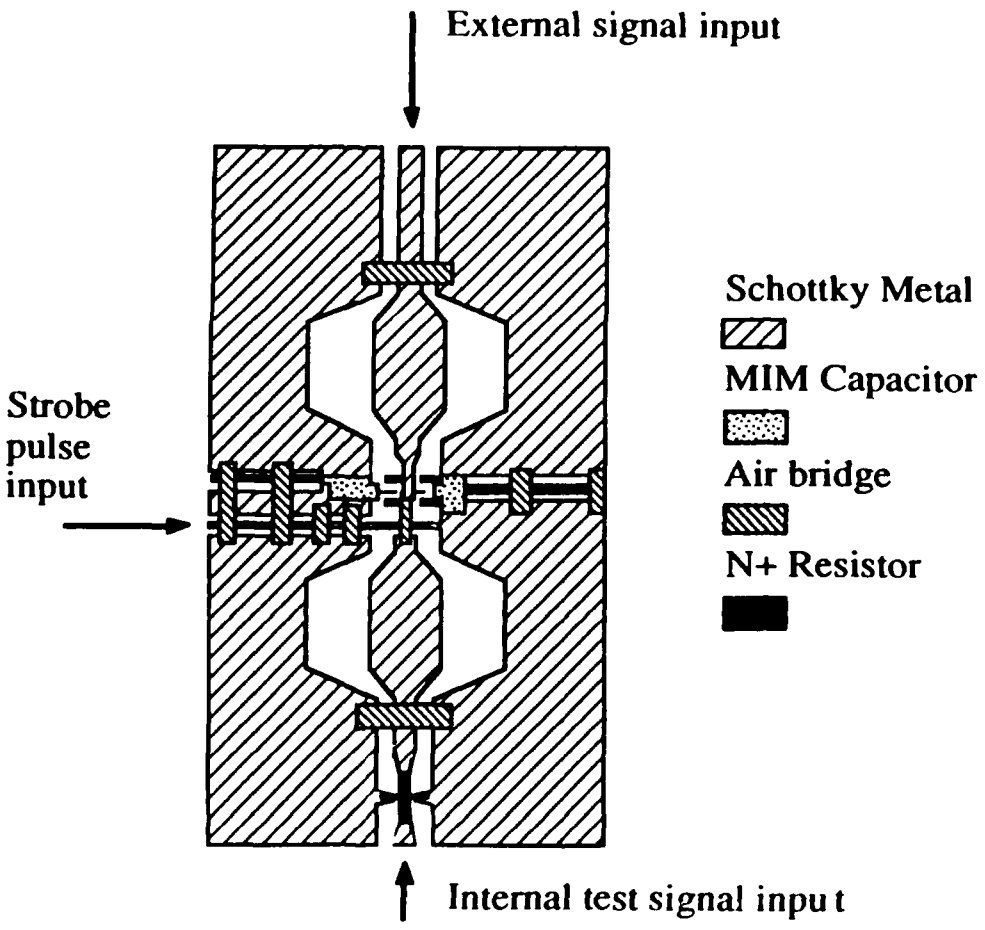
Threshold Device	Transition Time	Threshold
Josephson Junctions	2.1 ps	~ 5 mV
Schottky Diodes	0.2 ps	~ 800 mV

Pulser	Transition Time	Amplitude
Josephson Junctions	2.1 ps	~ 5 mV
Step Recovery Diodes	35 ps	10 V
Nonlinear Line	3.5 ps	2 V

Two Diode Sampling Bridge

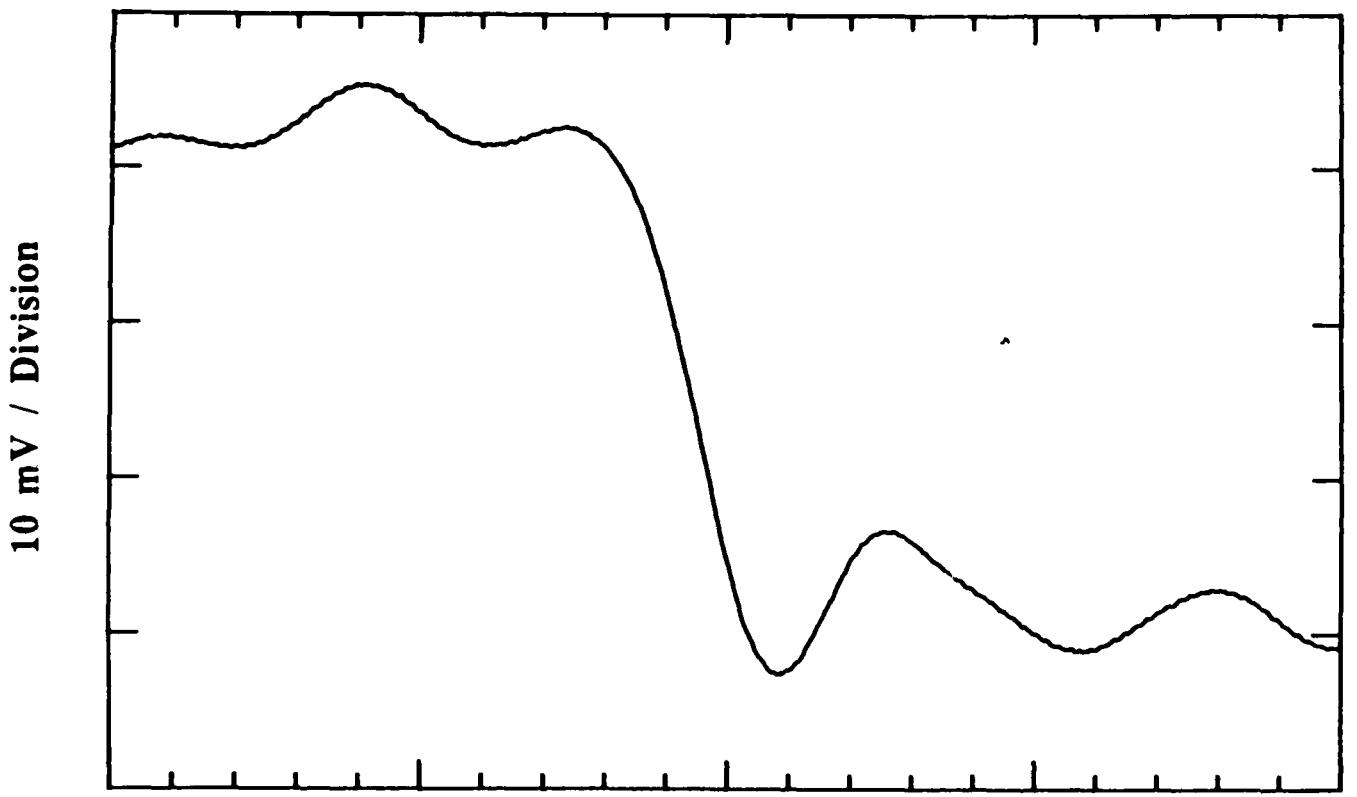


Layout of Diode Sampler

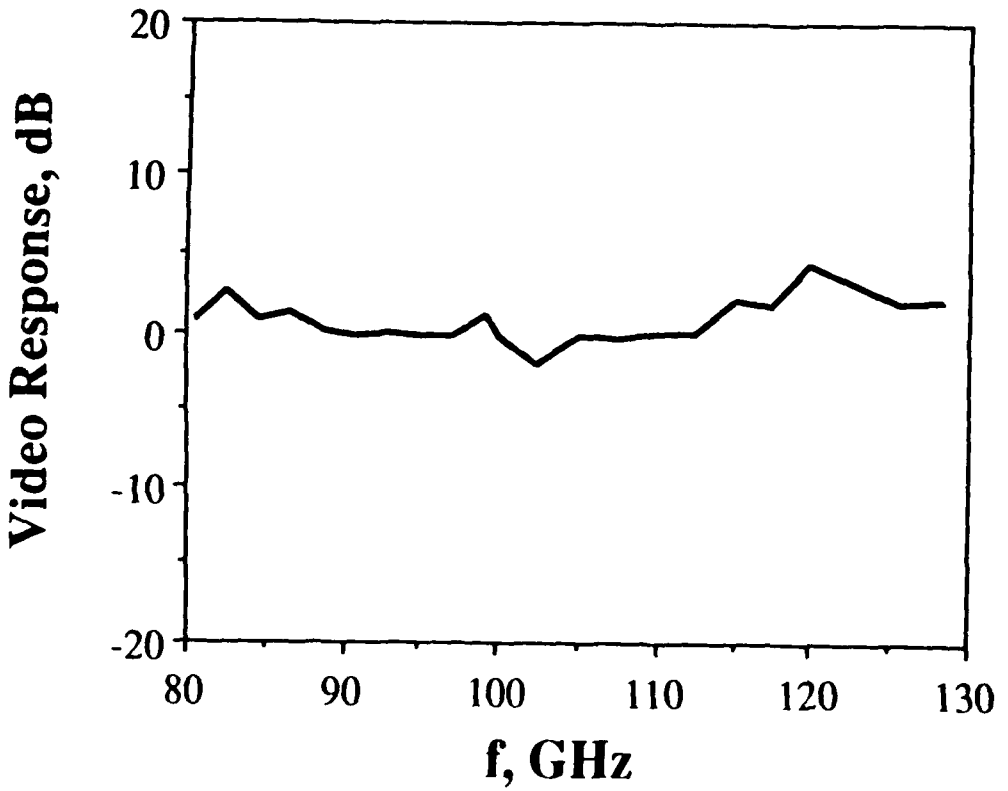


Balanced 4 ps FWHM Diode Gating Pulses
Voltage (a. u.)
0.0
10
20
30
40
50
Time (Picoseconds)

4.0 ps Falltime Measured with Diode Sampler



Frequency Response of Diode Sampling Bridge



Sampling Head Performance

RF Bandwidth		> 130 GHz
Estimated Rise Time		2.7 ps
Linearity to 400 mV		within 0.5%
Sensitivity		90 nV/$\sqrt{Hz}$
Isolation @ 5 GHz	LO to RF	68 dB
	RF to IF	55 dB
	LO to IF	63 dB