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A Compaq-286 Micro-Processor Based

High-Speed High-Density

Digital Data-Acquisition and Recording System

Volume I : System Overview

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A COMPAQ-286 MICRO-PROCESSOR BASED

HIGH-SPEED HIGH-DENSITY

DIGITAL DATA-ACQUISITION AND RECORDING SYSTEM

VOLUME I: SYSTEM OVERVIEW

DREP Technical Memorandum 88-23

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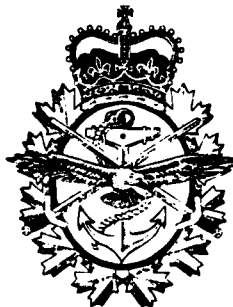
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ABSTRACT

A design is presented for a 'state-of-the-art' high-speed high-density data-acquisition system based on a commercially available COMPAQ-286 microcomputer. The system utilizes an 'in house' developed A/D board, capable of sampling 31 channels (expandable to 62) with 16-bit resolution, and with an aggregate sample rate of ~100 kbytes/sec. Data are logged on a Hewlett Packard 9144 digital cassette drive that uses 68 megabyte formatted cassettes. To achieve the required throughput, the software, written in 286-assembler, is interrupt-driven and uses direct memory access on output. The data-acquisition system is described in two volumes, the first giving a system overview, and the second providing sufficient software and hardware for the system to be reproduced. Keywords: Data processing; computer hardware, computer software; data storage; digital data; (KT)

1 <u>INTRODUCTION</u>

Many modern-day scientific experiments require the logging of
data for subsequent computer analysis, and consequently have a need for some
form of digital data-acquisition system.   Up until the present decade, for
applications where "off the shelf" mini-computer systems could not be used,
such as those requiring compactness and high data gathering rates, DREP
usually designed tailor-made acquisition systems for each particular
project.   Only then could the required speed and data throughput be
obtained, together with the compactness, low power consumption, and
reliability required for use in the field.   Such dedicated systems however,
although being optimum for the particular task in hand, had the disadvantage
that they could not be modified for alternative uses.

During the early 1980's, with the rapid advances in micro-
processor technology, micro-computers became commercially available that
utilized high-speed 16-bit devices and which almost met DREP's requirements.
In 1985, with the advent of the IBM AT-like micros, it was decided to
develop a data-acquisition system based on a COMPAQ 286.   In addition to
meeting both the data-acquisition requirements and allowing some capability
for real-time analysis, the 286 gave the potential for later detailed on-
site analysis of the data, as well as permitting easy modification of the
system for changing applications.

The description of the data-acquisition system is divided into
two volumes.   The first of these gives a system overview, and outlines its
development and the techniques required to meet the design objectives.   The
system has now been adopted by several groups and is well proven.   In this
first volume, Section 2 outlines the design objectives of the system, and
Sections 3 and 4 describe the hardware and software.   The second volume[1],
which essentially forms an appendix to the first, presents detailed circuit
diagrams and gives complete software listings.   In particular, circuit
diagrams are presented for the general-purpose A/D board designed for the
IBM AT-like computer, as well as for the daughter acquisition pod.   This
volume provides sufficient information for the acquisition system to be
reproduced.   Utility programs and diagnostic hardware are also discussed.

2 DESIGN OBJECTIVES

2.1 OVERALL SPECIFICATIONS

The initial target specifications for the acquisition system were to sample twelve channels of data, each at 1024 samples per second and with a resolution of 16 bits per sample (including sign). This corresponded to an aggregate sample rate of 24 kbytes/sec. At that sample rate the storage medium was to accomodate 30 minutes of data without change. In practice the system exceeded these specifications, digitizing 15 channels at 1024 samples/sec (30 kbytes/sec[I]), and logging 37 minutes of data without change.

The number of channels was to be variable up to a maximum of 31, and the sample rate was to be completely variable subject only to the constraints of the overall throughput specification. The digitization circuitry was to accomodate single-ended ±10-volt signals, and was to have a D/A monitoring capability for each channel. The final specifications achieved in practice are given in Section 5.

The physical considerations were that the system was to be highly reliable, small and portable, and that it make maximum use of commercially available units. The system, being personal-computer (PC) oriented, was to have the ability to read data back into the PC so as to permit the running of subsequent analysis programs, as well as the capability to off-load the data to a mini or main-frame computer for remote processing. The design was also expected to maximize the potential expected compatibility with future generations of PC.

2.2 HARDWARE CONSIDERATIONS

A survey of commercially available personal computers in 1985 indicated that products incorporating INTEL's 80286 or MOTOROLA's 68000 microprocessor had the required speed for the present application. As DREP

I. limited by the storage medium transfer rate

already owned several COMPAQ 286-based computers (an IBM AT equivalent), the 286 product was chosen for reasons of compatibility.

A study of the available digital 'mini' tape-decks showed few units to be capable of the 30-minute capacity at 24 kbytes/sec (ie. 34.2 megabytes). The best choice was found to be a Hewlett Packard 9144 drive which recorded on 68 megabyte-formatted cassettes, and which utilized IEEE input-output protocol. A Tecmar Corporation IEEE circuit board was used to interface the HP drive to the computer.

An evaluation of the existing data-acquisition boards for AT-like computers showed none to be suitable for the present project. Either the resolution was too low (12 or 14 bits), the sampling-rate was too low, or the number of channels that could be sampled simultaneously was inadequate. Furthermore, all of the commercially available units were designed for pre AT-generation computers and so used 8-bit transfers, thus negating the advantage of the 16-bit bus of the AT. Consequently, it was decided to design an A/D interface tailor-made for the AT.

The general design criterion of the board was to minimize the time required by the CPU for data-acquisition, and thus optimize the overall throughput by freeing the 286 to concentrate on data-logging and any in-memory data manipulation. Consequently the board was to be designed to use the 16-bit bus, was to be interrupt driven, and was to include a first-in/first-out (FIFO) buffer so as to avoid the need for immediate CPU response on completion of sample conversion. A direct memory access (DMA) capability was also to be included on the board, although this was not implemented in the present software. Sample and hold circuitry was to be included for each channel, as well as a D/A capability to permit verification of system performance. Finally, to further reduce the demands on the CPU, the sampling times were to be the responsibility of the board and not of the CPU.

2.3 SOFTWARE CONSIDERATIONS

The overall software considerations were to concentrate on speed of the program, and minimize CPU redundancy, hence maximizing the data-

acquisition and collection rate. All of the A/D handling routines were to
be interrupt driven, and DMA was to be used on output to the IEEE device.
Although the program was to be invoked under a standard operating system
such as MS-DOS, for reasons of efficiency no use was to be made of the DOS
software during time-critical stages of the acquisition. At all stages of
the development the aim was to decrease the number of machine instructions
required. In this way any free CPU time could be utilized later for real-
time display.

3 HARDWARE DESCRIPTION

The hardware of the data-acquisition system consists of three
main parts, an acquisition or "data pod", an adapter board, and the main
COMPAQ central processing unit (CPU) as shown functionally in Figure 1.
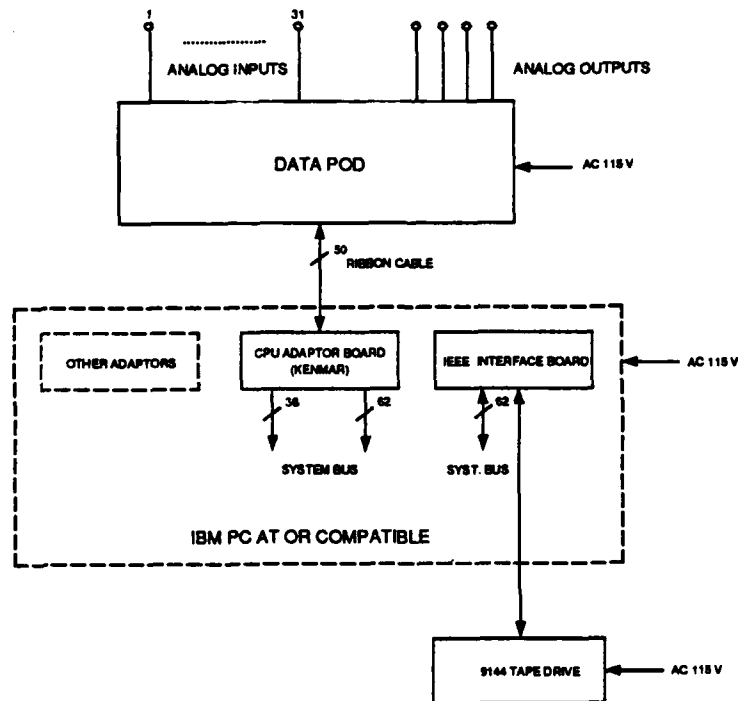
Figure 1. Functional sketch of system.

As indicated earlier, the principle design objectives were to obtain high
resolution (16-bits), a high sample-rate (50 kHz), a multi-channel
capability (31 channels), and a simultaneous sample and hold facility.
Complete circuit diagrams for the unit are given in Appendix 1.

3.1 THE DATA POD

The data pod was separated from the CPU and adapter board by an
umbilical cable to reduce digital interference and to allow convenient
front-end modification. It contained all of the analogue electronics such
as the sample-and-hold, multiplexing, A/D and D/A facilities.   A
functionality diagram is shown in Figures 2a and b.

ANALOG OUTPUTS

NOTE: · GROUP MONITOR SELECT
ALLOWS MONITORING ANY WINDOW
OF FOUR CHANNELS FROM 1 to 31

-ANALOG OUTPUTS FOR MONITORING ONLY

Figure 2a.   Functionality diagram of the data pod.

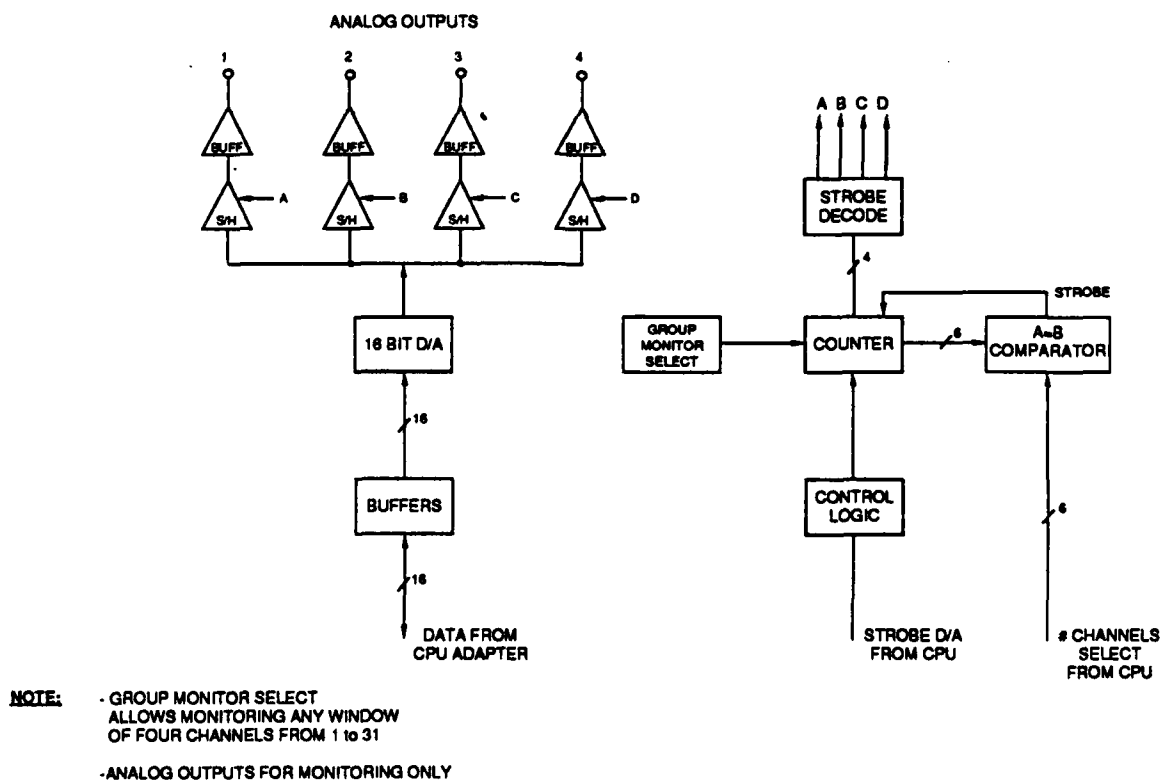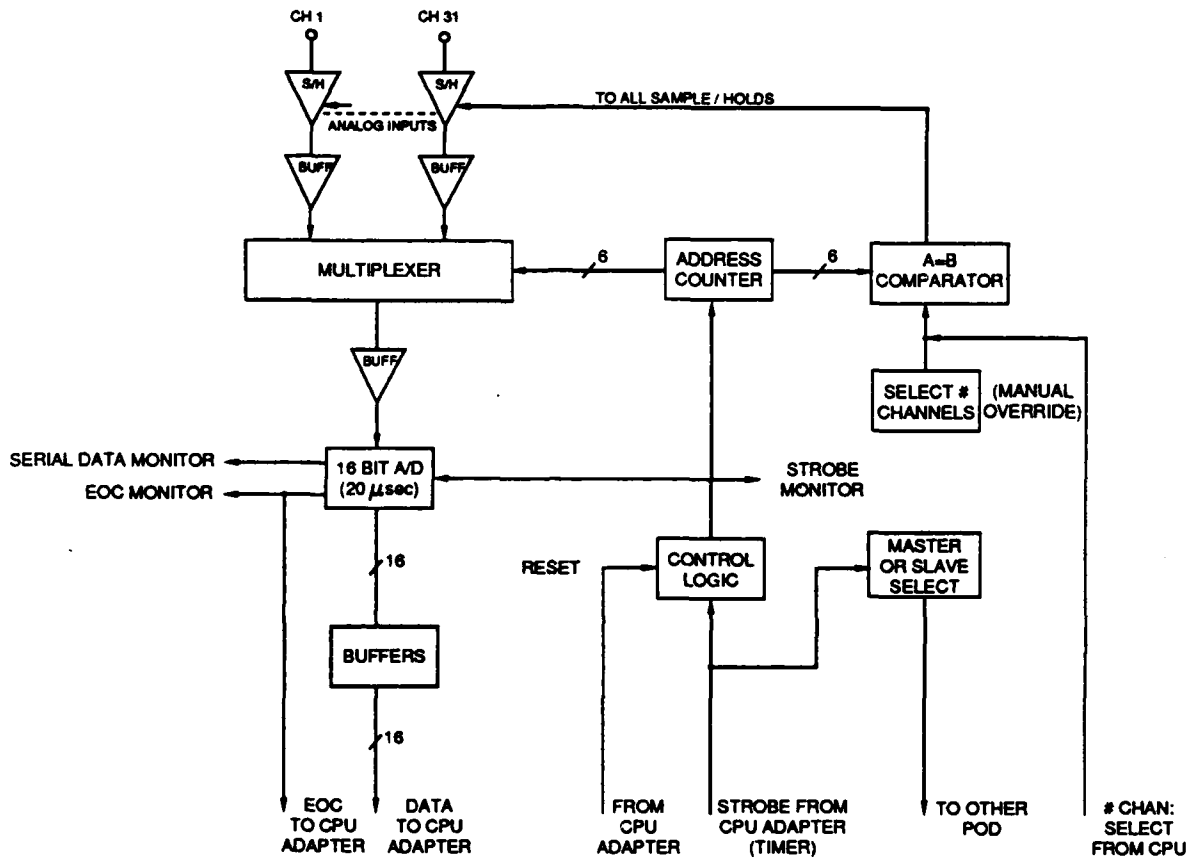Figure 2b.   Functionality diagram of the data pod.

A simultaneous sample-and-hold was implemented to permit phase coherent data-acquisition. Because of the high resolution (16 bit) of the pod, considerable care was needed to eliminate interchannel crosstalk. The sample and hold circuitry therefore used matched high-impedance LF398's, each with an offset adjustment and suitable buffering to eliminate reverse charge transfer from the previous analogue multiplexer channel. The sample-and-holds and multiplexing electronics were incorporated on two printed circuit cards each having 16-channel capability.

The analogue multiplexer was designed to sequence using an address counter that "rolled over" at the preselected number of channels. This avoided the need for the software to perform channel selection, thus freeing the CPU from unecessary work. The number of channels sampled before roll-over was CPU selectable.

The multiplexed analogue data were synchronously converted to digital form with a 16-bit A/D converter, and then transferred to the adapter board. Terminals were available to allow monitoring of the convert strobe, the sample/hold pulse (ie. roll-over), the serial data and end-of-conversion. A master/slave switch and suitable connector permitted coupling of two pods to allow expansion to 62 channels of simultaneous analogue input data.

A D/A capability was also included in the pod to permit monitoring of the integrity of the data passing from the analogue input into the CPU memory. This consisted of a 16-bit D/A converter, four sample-and-hold channels, and the associated timing and control logic. Because of the limitations in space and power, it was decided to use a switch selectable "window" which permitted the monitoring of all 31 channels, but in groups of four. The control and timing logic had to be independent from that of the A/D, because of the asynchronous nature of the CPU's burst mode input/output.

Considerable care was taken to minimize the effect of digital noise transmitted along the ground and data lines of the connecting cable, since this would produce inaccuracies in the analogue conversion. To aid in this, the conversion and data input/output was "interleaved" with the noise spikes produced by the asynchronous CPU and D/A data.

The inputs to the pod were purposely made single-ended for reasons of compatibility with existing analogue amplifiers and anti-aliasing filters.

The pod was packaged in a standard 3.5" rack-mount chasis, together with its power supply, 31 input connectors, D/A outputs, 50-pin shielded ribbon cable connector (to CPU) and master/slave connector and switch. Connectors to enable monitoring of the control signals were also added. A photograph of the pod layout is shown in Figure 3.
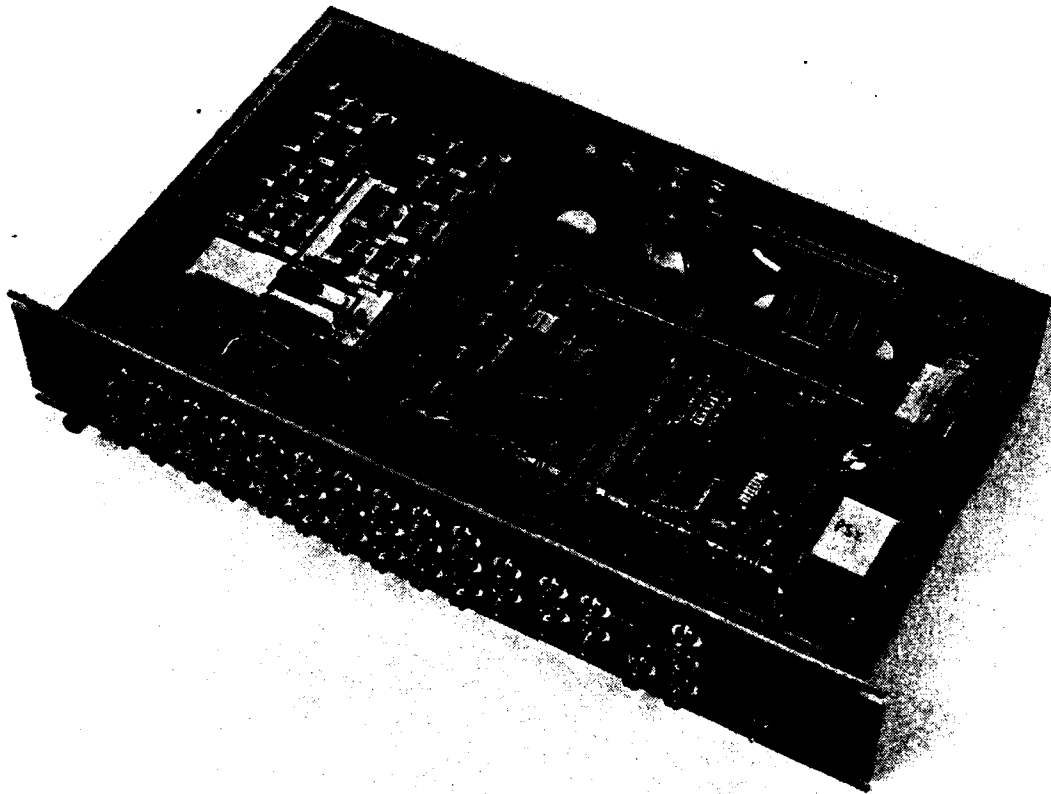
Figure 3.   Layout of the data pod.

3.2 THE ADAPTER BOARD

A functionality diagram for the adapter board is shown in Figure 4. The board was designed to operate in both the COMPAQ 286 and later 386
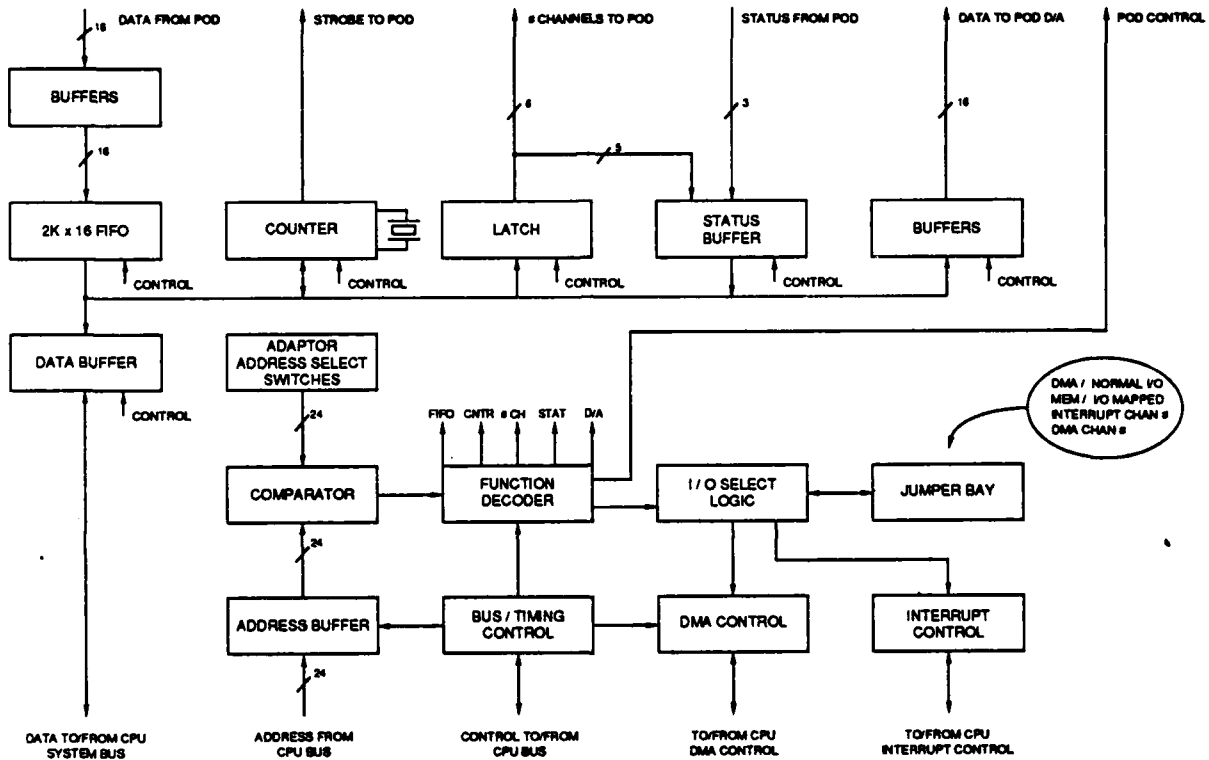
Figure 4.   Functionality diagram of the adapter board.

CPU's, with as much inherent flexibility of use as possible.   For this reason the switch selectable addressing encompassed the entire 32 megabyte addressability of the 286, and all available interrupts and DMA channels were selectable through onboard jumpers, together with a choice of either memory- or I/O-mapped useage.   All functions on the adapter board were addressable through 32 consecutive locations in the CPU address space.   By reading or writing to the board, various functions can be performed in either a handshake or autonomous mode.   Details of the control of the board are given in appendix A.5

The functions performed by the board are summarized in Table I, and although most are self-explanatory, several comments are necessary. Firstly, the start conversion function, once set, will continuously trigger data conversions without further CPU control. The frequency (aggregate) of conversion is selectable between 0.004 Hz and 250 kHz, and the number of channels (1 to 31) is latched on the adapter board, where it is sent to the pod and used for the automatic "roll-over" of the sample channel. Finally, the status word when read by the CPU, gives a means of confirming that the correct number of channels has been set up, and indicates whether a DATA READY, FIFO BUFFER FULL, or END OF CONVERSION has occurred.

Table I   Functions of the Adapter Board

Channel number selection
Sample rate generator/timer
First in, first out (FIFO) data buffer
Status register
CPU address select/decode
CPU signal buffering
Function decode/timing
Operation mode select
Start/stop conversion

To operate the adapter board the software must adhere to the following sequence:

1 Issue board reset;
2 Set number of channels;
3 Set aggregate sample frequency;
4 Start sampling;
5 Wait for DATA READY (by interrupt, DMA or polling);
6 Read immediately or wait until FIFO fills;
7 Transfer data to CPU memory;
8 Store on mass storage media if applicable;

9 Output to D/A for monitoring if applicable;

10 Loop to 5.

Once the timer has been started, the A/D converts each channel sequentially, and automatically stores the data in the 2k x 16 FIFO memory. The first two words loaded into the FIFO set an interrupt indicating DATA READY. If the CPU does not act on these interrupts, then the FIFO fills and another interrupt (FIFO FULL) is issued indicating an error condition to the CPU. Depending on the software design, the data can either be made to "fall through" the FIFO, or be transferred in "burst mode" to the CPU memory as fast as the interrupt handler will allow. If the DMA function is used, this "burst mode" rate can be as high as 650 kHz. It can be realized that data output to the D/A is only synchronous if the fall through mode is used in the FIFO. In burst mode, the data monitor outputs are delayed, reflecting the burst timing.

The prototype board was fabricated on a general purpose wire wrap card which led to difficulties with ground and signal noise problems that were overcome by careful lead routing and noise supression techniques. For subsequent units a ground plane printed circuit board was used. The layout of the adapter board is shown in Figure 5.
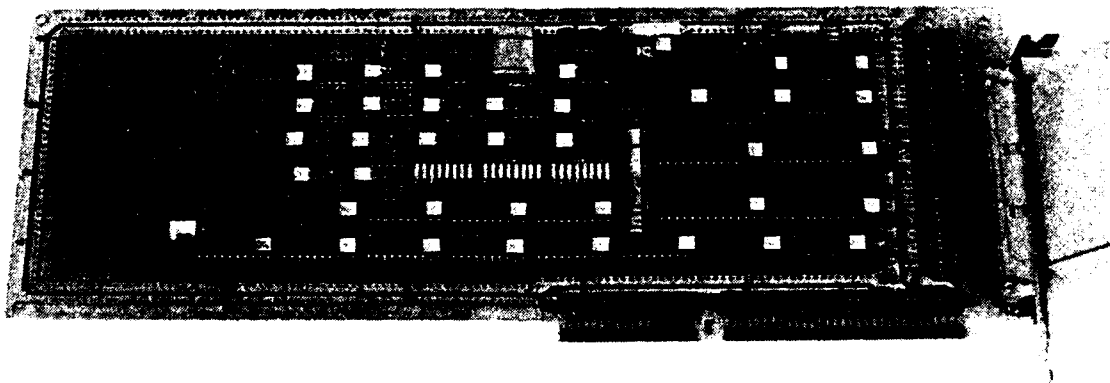

Figure 5.   Layout of the adapter board.

4 SOFTWARE DESCRIPTION

As mentioned previously the principal aim of the software design was to achieve maximum throughput and not have the data acquisition rate reduced by any software limitation. Consequently all of the programming was done in 286-assembler, DMA was used for transfer from the computer to the HP9144 tape drive, and the software was driven by hardware interrupts. Within the actual data collection loop, DOS calls were totally excluded since these are far too slow. In addition, DMA and keyboard access were performed at the chip level, again without any DOS system calls.

Modularity was an important consideration in the program design. The software was organized so that future hardware changes would require just a change in module, and not a complete rewrite of the program.

The program consists of 5 major sections, namely a control section and four interrupt handlers. Flowcharts of the sections are given in Figures 6 to 8, and complete program listings are given in the Appendix. A brief description of each of the sections follows.
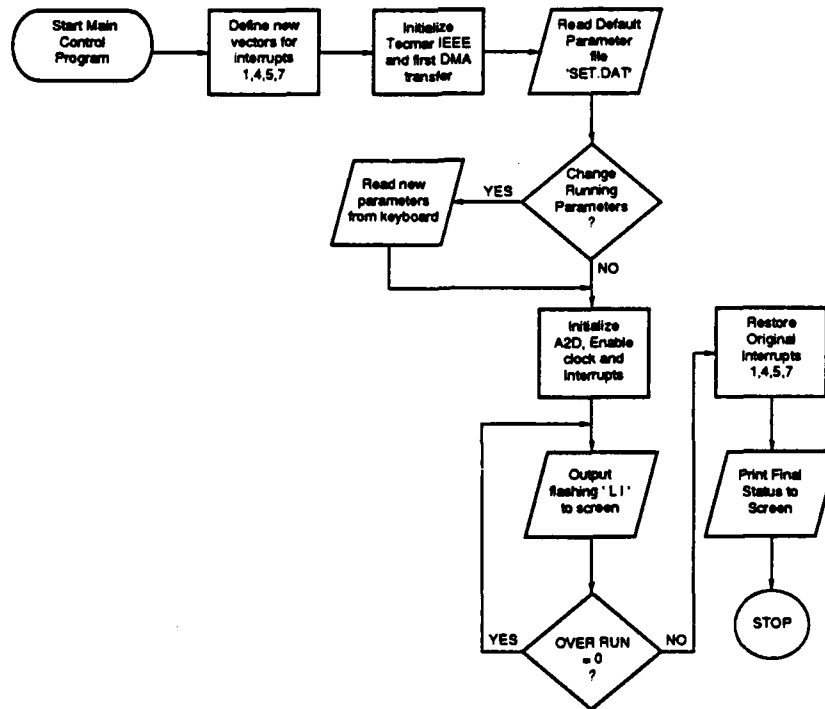
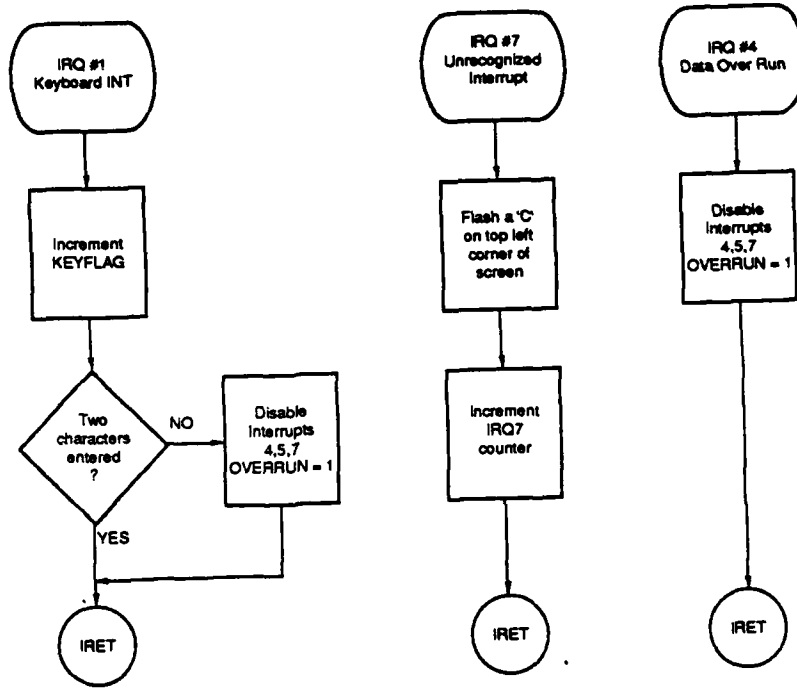Figure 6. Flow chart of the main acquisition program.
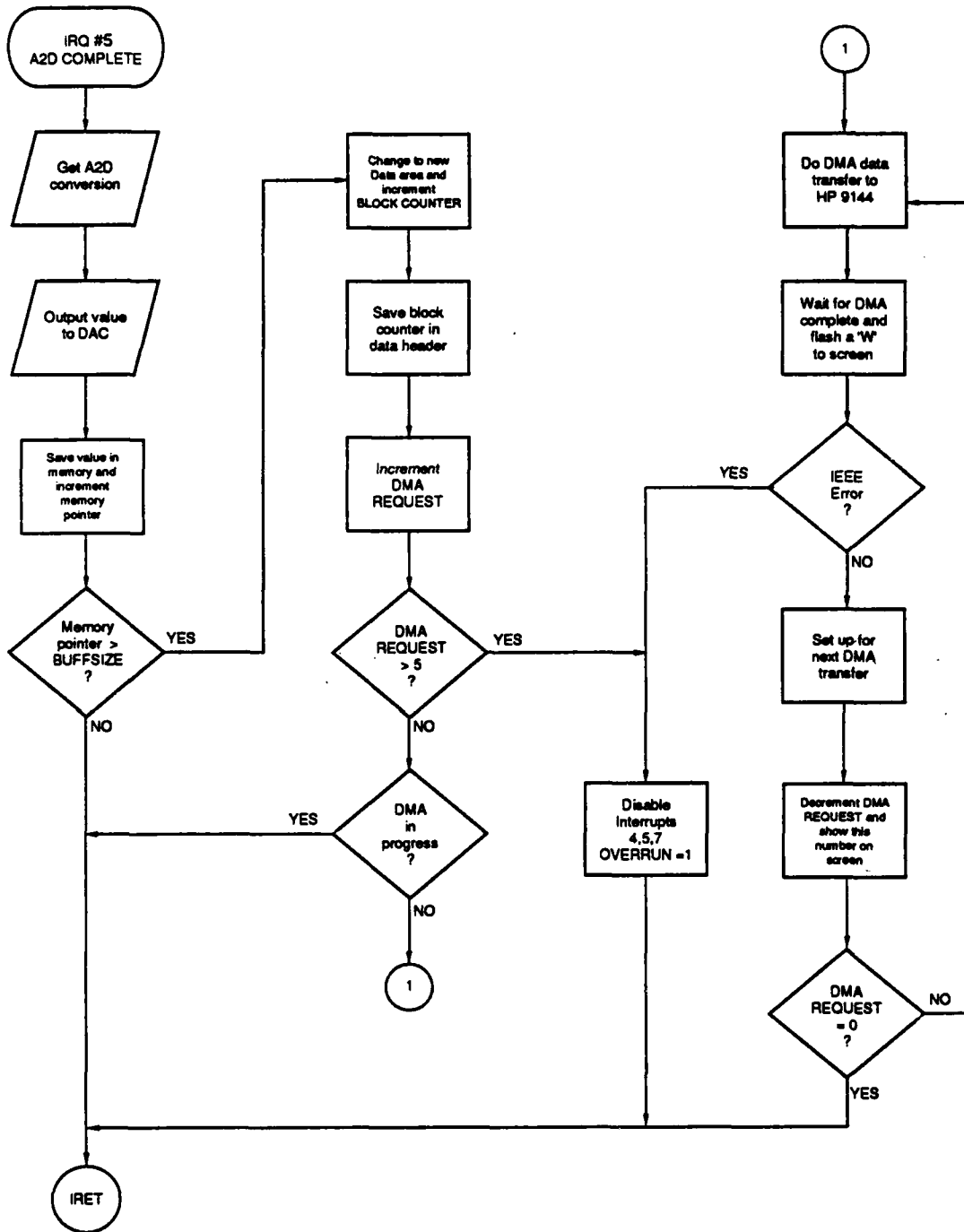
Figure 7. Flow chart of the interrupt structure.

Figure 8. Flow chart of the A/D module.

4.1 CONTROL PROGRAM

On start-up, interrupts 4, 5 and 7 are masked off and the new interrupt jump vectors are installed for IRQ#4 (overrun), IRQ#5 (A/D done), and IRQ#7 (unidentified interrupt). Several software variables and the Tecmar IEEE card are then initialized.

A default file that contains the sample rate and number of channels to digitize is read in. The user can either accept or change these defaults. The software buffer size (the number of 1024-byte packets sent to the HP9144) is also read from this default file. This is usually set at 63 kbytes, except for test purposes or for very slow sample rates.

A routine is called to initialize the A/D card, and the interrupt priority structure is changed so that the keyboard has the lowest priority, and data overrun the highest.

The DOS keyboard handler (IRQ#1) is then replaced by a simplified routine, and the DMA transfer channel is set up. After masking on the interrupts, the A/D clock is enabled and the program starts acquiring data.

The main program then goes into a loop during which the characters "L1" are flashed on the screen. The flashing characters give a visual confirmation that the program is working, and give an approximate idea of the free processor time available. While this looping is taking place, the data-acquisition and transfers to tape are taken care of by the interrupt handlers.

Any error condition or normal termination is sensed by a handler and an error flag set. This flag is detected by the looping main program which subsequently exits.

On exit the interrupt routines are restored to their original state, and a final status report is displayed on the screen.

4.2 INTERRUPT HANDLERS

4.2.1 INTERRUPT #1 - IRQ#1 - (KEYBOARD)

A simplified keyboard routine had to be written since the DOS handler was inappropriate. This routine simply increments a keyboard counter each time it is entered. When the counter reaches 4 the handler masks-off the hardware interrupts and passes an error flag back to the main program. As each key causes the routine to be entered twice, two presses on the keyboard terminate the data collection process.

4.2.2 INTERRUPT #4 - IRQ#4 - (DATA OVERRUN)

If the FIFO on the data acquisition board is filled up beyond its limit, the hardware will trigger the data overrun interrupt. This condition is fatal and indicates that either the computer or tape drive are not responding sufficiently fast for the desired sample speed.

The interrupts are disabled, and the error flag is passed back to the main program.

4.2.3 INTERRUPT #5 - IRQ#5 - (A/D DONE)

This interrupt is set each time the hardware FIFO has valid data that can be passed to the CPU. The handler inputs the converted word, and stores it in a memory location within a software buffer. The handler then outputs the word back to the DAC. This DAC output can be used to monitor the data or verify that the system is performing correctly. After each acquisition the memory pointer is incremented, and provided that the software buffer size is not exceeded, the interrupt routine is exited.

When the software buffer becomes full, the DMA section is entered. This section immediately changes the data storage area to a new

software buffer, and updates its information header. There are seven such buffers (each 63 kbytes) available to the program.

A DMA request counter is incremented which indicates the number of filled buffers that are awaiting transfer to the HP9144. If this counter ever exceeds 5, the program recognizes that all available buffers have been utilized, and the program is terminated. Under normal usage the counter varies between zero and one, rising to about 3 during a tape track change or "serpentine".

If the DMA is already active, the interrupt routine simply exits, and the latest filled buffer remains queued for transfer. If the DMA is not active the DMA transfer section of the handler is entered. After the DMA has commenced the program waits for a DMA complete status; during this state a flashing "Ww" is shown on the screen to indicate that the system is indeed logging data. At this point the handler has become reentrant, since conventional acquisition interrupt entries are still taking place. The DMA request counter is also displayed on the screen at this time.

On completion of the DMA, the IEEE status is checked. Any error is considered fatal and the program is terminated. Provided that there has been no error, the DMA is re-initialized for the next transfer and the DMA request counter is decremented. If the counter is non zero, a further DMA transfer is commenced. If no buffer transfers are outstanding, then the routine simply exits.

4.2.4 INTERRUPT #7 - IRQ#7 - (UNRECOGNIZED INTERRUPT)

Apart from a genuine signal being supplied to the IRQ#7 line (which is not used by the present acquisition hardware), this interrupt is triggered if the 286 interrupt handling chip (intel 8259A) is unable to recognize the origin of any interrupt. This condition is not considered fatal, but a "C" is displayed at the top left of the screen. A counter is updated and the total number of IRQ#7's printed out on program completion. The occurrence of IRQ#7's, however, should be reason for concern.

5 THE COMPLETE DATA-ACQUISITION SYSTEM AND ITS OPERATION

A photograph of the final data-acquisition system, which indicates its compactness, is shown in Figure 9. Although shown here with a portable-286 computer, the system has been successfully operated with a DESKPRO version, and more recently with 386-based products. The final specifications of the system are summarized in Table 2.
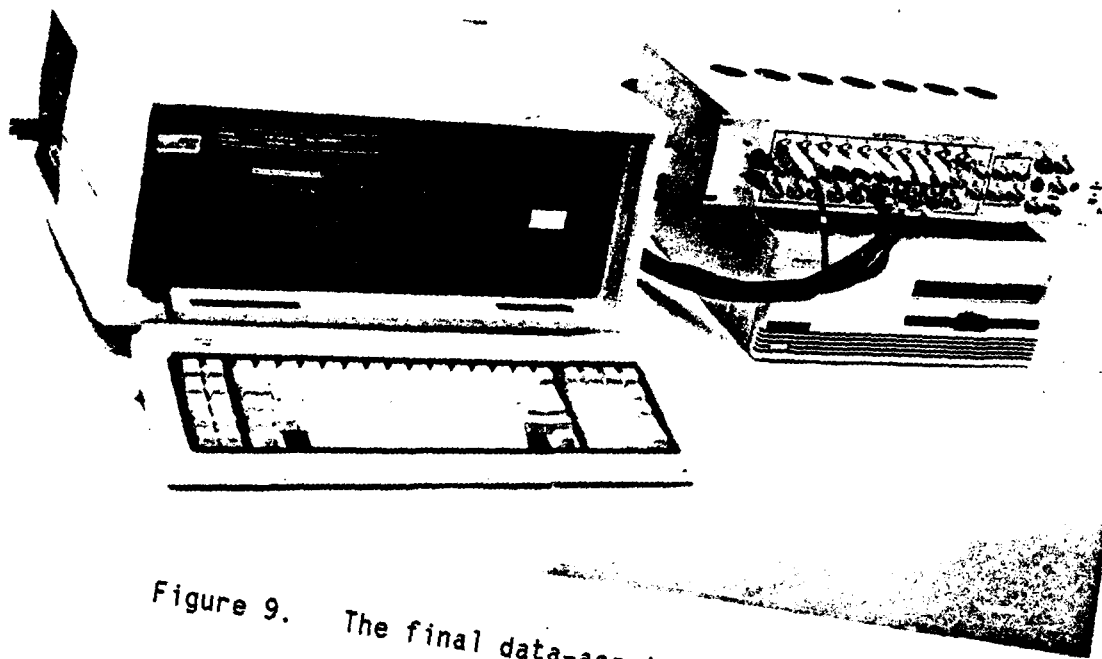
Figure 9. The final data-acquisition system

To install the software package, the main acquisition program MASTER.EXE, the utility programs STAT2.EXE and IEEEE.EXE (see section 6), and the defaults file SET.DAT must be installed on the COMPAQ. Although the three execution files are normally installed in the same directory, this is not mandatory provided the paths are appropriately set. MASTER.EXE and SET.DAT, however, must reside in the same directory.

To operate the system the following steps must be invoked:

1 Rewind the tape drive if needed   - invoke IEEEE
2 Run the status program   - invoke STAT2

3   Run the acquisition program   - invoke MASTER

Steps 2 and 3 are normally incorporated in a command file, whereas Step 1 is performed separately by running the rewind program (see Section 6.2.2).

Step 1 will depend on the user's intent, since if ommitted the acquisition will simply continue from the point at which the tape left off. Step 2 clears the IEEE circuitry, and if a new tape has been loaded, positions it at the first block.   Step 3 invokes the main data acquisition

<u>Table 2</u>   <u>System Specifications</u>

No. of channels (1 pod)	1 to 31 (expandable)
A/D resolution	16 bits
Dynamic range	90 dB
Maximum input level	±10v
Aggregate sample rate (excluding HP9144 transfer rate limitation)	100 kbytes/s (50 ksamp/s)
Aggregate sample rate (including tape storage transfer rate limitation)	
Continuous	~30 kbytes/s (15 ksamp/s)
Burst mode (until buffers filled)	100 Kbytes/s (50 ksamp/s)
System noise	1-2 bits
DMA transfer rate of adapter board	650 kbytes/s
D/A resolution	16 bits
Storage capability (of HP9144)	68 Mbytes
Addressing (32 locations)	anywhere up to 32 Mbyte
Interrupts	selectable to any CPU available
DMA channel	selectable to any CPU available
Power requirements	
Data pod 5v	30 mA
" " ±15v	±0.3 A
Adapter board 5v	0.5 A
Operating temperature	0 to 85C

```
frequency   :1000 hz    # of channels:5   total frequency:5000
block start :639         recording time:111 min.
```

Modify Run Parameters ? [Y/N/Q]:

Figure 10.   The video screen format.

program.   Defaults for the number of channels to be collected, together
with the sample rate, are read from a disk file SET.DAT[II] .   These defaults
are displayed on the screen and the user is prompted for any change.
Either, or both, of the defaults may be changed.   The screen, an example of
which is shown in Figure 10, also displays the current starting block of the
tape, the aggregate sample rate, and the time on tape remaining for this
sample rate.   As may be seen, the program can be aborted during this user
prompt stage.   In this event the tape position remains unchanged.

.Once commenced, and provided that no errors occur, the acqusition
program will run interrupted until either an end-of-tape (EOT) occurs or any
two entries are made on the keyboard.   At that time the acquisition is
terminated and an end of file written to the tape.   (An end-of-file is also
written for an error termination).   Provided that the EOT has not been
reached, the system is now ready for a further recording session.   If an
EOT is reached, or if a user wishes to terminate use of a particular tape,
the tape is unloaded by using the front panel control of the HP 9144.

II.The SET.DAT file also contains the length of each of the multiple buffers
   used in the acquisition in units of 1024 bytes (see Section 4.1).   As
   this parameter is rarely changed, it can only be modified by editing the
   file.   Note that the channel number and sample rate defaults are also
   changed by editing this file.   The format for the parameters NCHAN,
   SAMPLE RATE, and NBUFF in the file is a single line, with each field
   having 10 columns, and with each item left justified within the field.

6 DIAGNOSTIC AIDS AND UTILITY PROGRAMS

6.1 SYSTEM VERIFICATION HARDWARE

To verify system performance we developed a staircase generator that enabled a known pattern to be placed on tape. The generator outputs a 32-element triangle (see Figure 11), with the changes between levels being
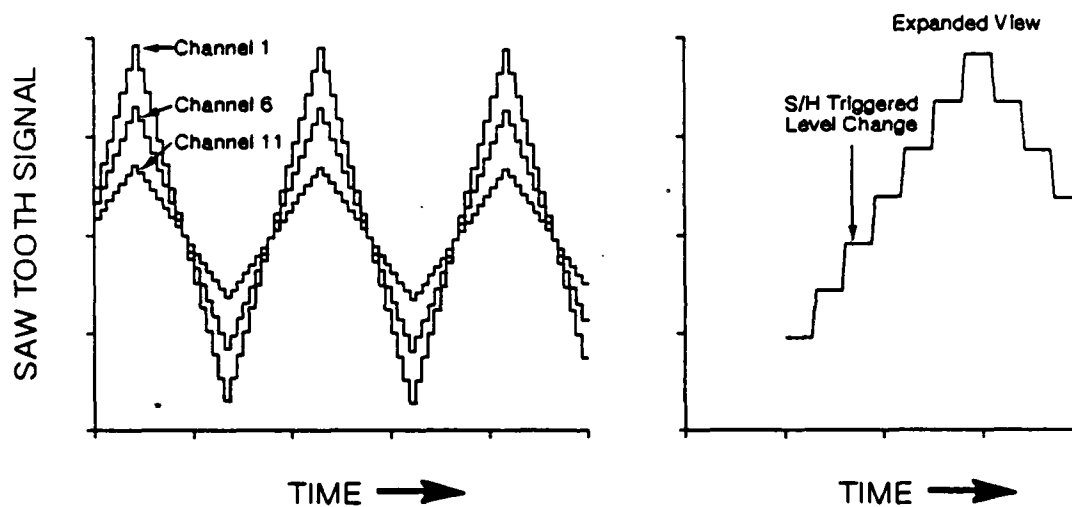
Figure 11.   The staircase generator sinewave.

controlled by the SAMPLE/HOLD (S/H) pulse of the data-acquisition system. In this manner a complete tape could be written with a pre-determined pattern that could later be checked for error. In practice, the tape writing and subsequent comparison were automated, and the process run for periods of days to look for any infrequent sources of error.

The circuit diagram for the generator is shown in appendix A.3.

6.2 SOFTWARE UTILITIES

Three utility programs, necessary for running the complete data-acquisition package, are discussed.

6.2.1 STATUS

The status program requests the status of the HP9144, while at the same time clearing the IEEE interface and the tape unit, thereby placing it in a known state. This program should always be run immediately prior to data-acquisition. A listing of the program is given in appendix A.4.1

6.2.2 MEDIA REWIND

This program, which is listed in appendix A.4.2., simply sends the appropriate commands to the HP9144 to rewind the tape.

6.2.3 DATA DEMULTIPLEX

Some form of demultiplex program is required to subsequently separate the data stored on tape into its constituent channels. Our own code is not presented, since the form of the program depends critically on the read-back computer being used. Information concerning the HP9144 tape storage format, sufficient to enable development of demultiplex code, is given in appendix A.4.3.

7 FUTURE DEVELOPMENTS

Several modifications are anticipated for the data-acquisition system. Firstly the DMA capability of the adapter board will be utilized to increase the throughput of the system. As considerable restructuring of the software will be necessary, this modification has not yet been attempted.

Secondly, following the recent introduction of Intel's 80386 products and the corresponding 80387 coprocessor, work has already begun on modifying the system to utilize a COMPAQ 386. Software changes will be needed to utilize 386-specific instructions, and thus fully exploit the speed of the 386. At the same time, the feasibility of developing a high capacity system incorporating either a 400-megabyte optical disk or 2-gigabyte 8-mm tape drive is being investigated, as is a self verification program which automatically checks all the features of the acquisition system. The first phase of these studies is complete[1], and the remainder will be reported elsewhere.

Finally, the program will be modified to incorporate real-time screen plotting of user selectable channels.

8 SUMMARY

A design, both hardware and software, has been presented for a high speed, high capacity data-acquisition system based on a COMPAQ-286 (IBM AT-like) computer and a Hewlett Packard 9144 digital cassette tape drive. The system enables 16-bit wide sampling of up to 31 channels of data, with an aggregate sample rate of ~30 kbytes/sec. The system has been run successfully with both COMPAQ-286 and 386 computers.

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