

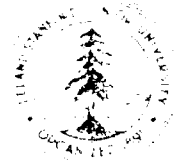
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SOLID STATE ELECTRONICS LABORATORY

STANFORD ELECTRONICS LABORATORIES
DEPARTMENT OF ELECTRICAL ENGINEERING
STANFORD UNIVERSITY · STANFORD, CA 94305



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JSEP ANNUAL REPORT

1 May, 1987 through 30 April, 1988

James S. Harris, Jr.
JSEP Principal Investigator
and Program Director

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Period of 1 May 1987 - 30 June 1988

**Department of Electrical Engineering
Stanford University
Stanford, CA 94305**

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Abstract

This is the annual report of the research conducted at the Stanford Electronics Laboratories under the sponsorship of the Joint Services Electronics Program from 1 May 1987 through 30 April 1988. This report summarizes the area of research, identifies the most significant results and lists the dissertations and publications sponsored by the contract DAAG29-85-K-0048.

Key Words and Phrases: None

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JSEP ANNUAL REPORT
April 1, 1987 - June 30, 1988

INTRODUCTION

The JSEP contract supports a program of unclassified basic research in electronics conducted by faculty members of the Electrical Engineering Department of Stanford University as a component of the research program of the Stanford Electronics Laboratories. The Stanford Electronics Lab JSEP Director and Principal Investigator is Professor James Harris. He is responsible for the selection of the best individual proposals, coordination between Stanford and the JSEP TCC and coordination between the selected areas of the JSEP Program. In planning the JSEP Program at SEL, a general objective is to develop new projects with 3-6 years of JSEP sponsorship, leading to transition to DoD or other agency program funding. This report covers the final year of our current 3 year cycle. During the second year, we started two new projects supporting newly appointed faculty, John Cioffi and Bruce Wooley. Near the end of the second year, the discovery of the high T_c superconductors provided an opportunity to quickly fund new projects in this area, long before more conventional sources of research funding could respond to this opportunity. This JSEP supported project has produced significant results and received considerable recognition, partially because we were able to get this project started before other institutions could get funded, thus truly demonstrating the value of the flexibility of JSEP funding.

Four program highlights achieved during the past year are summarized below. Following these highlights, the specific objectives and progress in each work unit are reported.

There are two well known methods of solving the minimum-mean-square filtering problem: the recursive least squares (RLS) algorithm and the least-mean-square (LMS) algorithm. The LMS algorithm is widely used because of its computational simplicity and robustness. Two groups of RLS algorithms, the fast transversal filter (FTF) have been introduced recently, but these have been plagued by exponential instability of the propagation of numerical

errors. We have now developed a stabilized FTF algorithm which is only 28% more computer expensive than the fastest, but unstable FTF algorithms.

The growth of high temperature superconductors by molecular beam epitaxy (MBE) has been instrumental in understanding the growth of in-situ, high T_C thin films. We have demonstrated that a reactive oxygen source is essential for any moderate vacuum deposition technique to produce in-situ superconducting films. We have also observed metastable phases that form by intentional layering of the films during growth by shuttering the fluxes in the same pattern as the layered superconducting unit cell. These metastable phases have not been observed by other deposition techniques. This result provides great incentive to continue this approach for investigation of the new, higher T_C Bi and Tl compounds, in which the value of T_C is related to the number of CuO layers in the unit cell.

A major factor in IC performance is interconnection delay. A careful analysis of the effect of reduced line resistance on the performance of CMOS circuits operated at liquid-nitrogen temperature has been completed. For a typical 0.8 micron CMOS technology, it has been found that the RC delay of the interconnect degrades performance for line lengths exceeding 1 cm at room temperature and 2.5 cm at liquid-nitrogen temperature. For typical circuits which use interconnects below these lengths, the delay is dominated by the RC delays associated with the source resistance and the improvement in performance achieved through operation at 77°K is close to a factor of two regardless of interconnect length. We conclude from these results that the use of lower resistance materials, such as high T_C superconductors, will not enhance circuit performance at 77°K.

We are examining the potential of heteroepitaxial GaAs on silicon at the circuit and system level to achieve significant performance advantages. Such integration would substantially reduce the performance limiting parasitics that typically exist at the interface between the receiver preamplifier and a discrete photodetector in an optical receiver. We have completed the

analysis, design and fabrication of both bipolar and CMOS versions of the amplifier in silicon and we have demonstrated the ability to grow local areas of GaAs into recessed trenches in the silicon substrates. These films have been used to implement a metal-semiconductor-metal photodiode of the type that is integrated for the fiber-optic receiver.

The technical knowledge developed under the JSEP contract is widely disseminated through sponsor reviews, presentations of papers at technical meetings, publications in the open literature, discussions with visitors to the laboratories, and publication of laboratory technical reports.

Unit: 1

TITLE: Molecular Beam Epitaxy of High Tc Superconductors

Principal Investigator: James S. Harris

Research Associate: Eric S. Hellman

Graduate Students: Darrell Schlom and Zong Jian Chen

SCIENTIFIC OBJECTIVE:

The discovery by Bednorz and Müller of a class of materials which exhibit superconductivity at unprecedented temperatures has opened new possibilities for the future of electronic devices. In these new materials, such as $\text{YBa}_2\text{Cu}_3\text{O}_{7-x}$ (YBCO), superconductivity occurs in copper-oxygen layers sandwiched between rare-earth or alkaline earth oxide layers. More recently discovered high temperature superconductors, such as in the Bi-Ca-Sr-Cu-O (BCSCO) and Tl-Ca-Ba-Cu-O systems, share this layered structure. However, the polycrystalline nature of the ceramic forms of these materials is likely to be unsuitable for electronics applications. In addition, the very short coherence lengths of these superconductors has made it difficult to prepare thin film tunnel junctions in the usual ways. The ideal form of these materials is thus likely to be that of epitaxial films, prepared in such a way that composition and structure can be controlled at the level of atomic layers. Recent work on the thallium system has shown that the transition temperature can depend on the number of copper-oxygen layers contained in the layered structures. Well connected thallium compounds have been synthesized with up to 3 copper-oxygen layers to obtain T_c s above 125°K. Up to 5 copper-oxygen layers have been seen by TEM in portions of the thallium samples. The compounds with larger number of layers in bulk form become progressively more difficult to synthesize. Clearly, an epitaxial process capable of controlling the layer structure on an atomic layer by atomic layer basis would be a boon both to science and technology. With these goals in mind, we have begun an investigation into the suitability of molecular beam epitaxy (MBE) for the preparation of high temperature superconductor thin films.

SUMMARY OF RESEARCH:

The MBE system used for this work is a modified Varian 360 system located at Varian Research Center in Palo Alto. The work described here is the product of a collaboration between the MBE groups at Stanford University and at Varian Research Center, and the High Tc Thin Film group at Stanford, under the auspices of the Thin Film Thrust at CMR. To improve the oxygen pumping capability of this system, a turbo-molecular pump and a titanium sublimation pump have been added to the usual configuration of the system. A precision leak valve introduces oxygen into a tube which terminates near the substrate. Copper, barium, and dysprosium beams are obtained from effusion cells with pyrolytic boron nitride (PBN) crucibles. Dysprosium (Dy) was selected in place of yttrium from among the elements which form high-Tc superconductors in the $\text{YBa}_2\text{Cu}_3\text{O}_{7-x}$ structure because of its high vapor pressure.

Thin film synthesis of the 90°K material, $\text{LnBa}_2\text{Cu}_3\text{O}_{7-x}$ (the "1-2-3" compound, where Ln = Y or a lanthanon other than Cs, Tb or Pr), by deposition and high temperature annealing has been demonstrated in many laboratories around the world. High critical currents in the high Tc superconductors^{1,2} were first obtained in thin films in which the constituent elements were first deposited by electron beam evaporation. The superconducting crystallites were then grown from the deposited film by solid phase epitaxy in an atmospheric pressure oxygen furnace. Such a process offers almost no control during the critical step when the superconductor is actually made, but has the virtue of simplicity during the deposition process. Subsequent to the e-beam evaporator work, many techniques³ including our own work on MBE, sputtering⁴ and laser ablation⁵ were found suitable for the deposition phase of the film synthesis. Since the superconducting phase is formed during the anneal for each of these processes, there are no advantages and many disadvantages for a technique like MBE compared to the other techniques. However, deposition of films which could be annealed into 90°K superconductors was essential as a first step on the road to monolayer epitaxy.

Although we have obtained superconducting films with zero resistance at 67K on $\{1\bar{1}02\}$ sapphire, and at 85°K on $\{100\}$ yttria stabilized cubic ZrO_2 , the best films have been obtained on $\{100\}$

SrTiO₃ substrates. These substrates also show the strongest tendency towards oriented epitaxy during deposition, based on observations of spots in RHEED (Reflection High Energy Electron Diffraction) patterns. Depositions of DyBa₂Cu₃O_{7-x} DBCO on SrTiO₃ have been made under a variety of growth conditions. At substrate temperatures below about 500°C deposition of DBCO results in a rapid disappearance of the diffraction pattern, indicating that the deposited film is amorphous. After the high temperature oxygen anneal, these films become superconductors of reasonably good quality if the overall film compositions are close to being stoichiometric. For substrate temperatures between 500°C and 720°C, a distinctive pattern of diffraction spots, is seen for the first few minutes of growth. These spots then give way to a ring pattern characteristic of polycrystalline growth, which diminishes in intensity through the deposition. We have identified this initial pattern as that of metallic copper, which forms in islands on the SrTiO₃. The islands are epitaxially aligned with the substrate, the interface plane being predominantly {110}Cu and some {100}Cu. The presence of unoxidized copper, at least in the initial phase of growth, suggests the existence of kinetic or thermodynamic barriers to oxidation of the copper. This suggested to us that the use of oxidants other than molecular oxygen, may be beneficial.

There are several obstacles to the attainment of epitaxy of YBCO in situ. In contrast to the simplicity of most of the material systems in which MBE has been successfully achieved, at least three pseudo-ternary and six pseudo-binary compounds of various crystal structures, in addition to the three oxides, exist in the equilibrium phase diagram. In experiments on bulk synthesis, the YBa₂Cu₃O_{7-x} structure (to be referred to here as the 123 structure) forms above 800°C, and undergoes a tetragonal to orthorhombic transition upon cooling to 700°C. In addition, oxygen can evolve from the material at temperatures as low as 200°C, transforming the material from a superconducting metal to a non-superconducting semiconductor or insulator. Thus, it may be unrealistic to expect to obtain superconductors directly from a high-temperature high-vacuum process with low oxygen pressures. However, the tetragonal YBa₂Cu₃O_{7-x} structure is stable with as few as 6 oxygens per unit cell ($x=1$), so most of the advantages of epitaxy may be preserved if this layered perovskite structure can be obtained during growth, requiring only a low temperature oxygen anneal to obtain the superconductor. Recent

work on BCSCO indicates that it is more stable with respect to oxygen content, suggesting that it may be significantly easier to form in situ. Excellent epitaxial films have recently been achieved in situ by techniques such as magnetron⁶ and ion beam sputtering⁷ which operate at relatively high oxygen pressures (1-20 mTorr) and generate more reactive forms of oxygen (ions, atoms, etc.). Even with the high oxygen pressures used in these techniques, the quality of the films which result is very sensitive to the details of the oxygen discharge. At present, these higher pressure techniques do not offer the flexibility or the monolayer control potentially achievable by MBE-like methods. In addition, lower pressures allow the use of surface analytical tools such as reflection high energy electron diffraction (RHEED), low energy electron diffraction (LEED), Auger electron spectroscopy, ultra-violet and x-ray photoemission spectroscopy (XPS) to study surface structure and bonding on an atomic scale. These tools may prove essential if atomic layer engineering is to be realized.

Several groups^{9,10,11} have been successful in obtaining epitaxial films which are superconducting as removed directly from a low-pressure deposition chamber by using oxygen ion beams⁸ or oxygen plasmas^{10,11} in conjunction with standard evaporation techniques and by raising the oxygen pressure in the chamber with the substrate still hot after the deposition is complete. The substrate temperatures used in these processes are well below the minimum temperature needed to form the superconductor in the standard deposit and anneal method. In these techniques, oxygen pressures at the substrate may exceed 10 mTorr during growth, close to the cross-over out of the molecular flow regime. With sufficient differential pumping, these conditions are compatible with many of the standard "high-vacuum" analysis techniques.

Our own group has used an oxygen plasma source in conjunction with atomic-layer shuttering of molecular beams to obtain high quality epitaxy of Dy-Ba-Cu-O layered compounds. However, the electrical and crystallographic properties of the films depend very sensitively on the deposition conditions, and in many respects appear to be different from the materials obtained by annealing at higher temperatures. RHEED patterns from the growing film are used to study the orientation and structure of the epitaxial film. In particular, we observe patterns

throughout the growth which indicate a tripling of the unit cell along a particular direction of the crystal. This phase has lattice constants close to those of the superconducting phase $\text{DyBa}_2\text{Cu}_3\text{O}_{7-x}$. Other, unidentified phases are observed to grow epitaxially when the film composition is different from that of the superconducting phase. Smooth epitaxial films which exhibit streaked RHEED patterns throughout growth are obtained by use of atomic layering. Superconducting films can be obtained directly from the chamber with resistive onsets as high as 70K at this early stage in this work.

During epitaxial growths using the oxygen plasma, the oxygen pressure at the substrate was typically in the mid 10^{-4} torr range, while remaining on the low 10^{-4} scale in the rest of the chamber due to differential pumping. The incident fluxes were set to give a growth rate corresponding to one c-axis unit cell height (of $\text{DyBa}_2\text{Cu}_3\text{O}_{7-x}$) every 18 seconds ($0.65 \text{ \AA}/\text{sec}$). During growth, the copper and oxygen fluxes were not interrupted, but the dysprosium and barium shutters were periodically shuttered in order to encourage the Dy-Ba-Ba-Dy-Ba-Ba-... layering of the desired $\text{Dy}_1\text{Ba}_2\text{Cu}_3\text{O}_{7-x}$ structure. The amount of time and relative phase of each dysprosium or barium burst could be changed during growth, as well as the total Dy-Ba-Ba cycle period. Two growths will be described in detail here. The first was performed with a 6 second open time for dysprosium immediately followed by 12 seconds of barium, at a substrate temperature of $530 - 560 \text{ }^\circ\text{C}$. The second growth was begun with identical shuttering conditions, but the shuttering period and dysprosium open time were lengthened during the growth. The substrate temperature was also raised from its initial value of $585 \text{ }^\circ\text{C}$ briefly up to $615 \text{ }^\circ\text{C}$ and then back to $600 \text{ }^\circ\text{C}$ for the duration of the growth. The affects of these changes were monitored by in situ RHEED.

Figures 1 and 2 show sequences of RHEED photographs during the growths of two samples with composition close to $\text{Dy}_1\text{Ba}_2\text{Cu}_3\text{O}_{7-x}$. The samples in Figs. 1 and 2 have average metal compositions of $\text{Dy}_{1.4}\text{Ba}_{3.4}\text{Cu}_{5.2}$ and $\text{Dy}_{1.6}\text{Ba}_{3.5}\text{Cu}_{4.9}$ by electron microprobe, respectively. Figure 1a shows the RHEED pattern along the $\langle 100 \rangle$ azimuth of a clean SrTiO_3 (100) substrate before growth. Figure 1b shows the same wafer after the growth of 490 Dy-Ba-Ba layers ($\approx 0.6 \mu\text{m}$) along the same azimuth. Figure 1c shows the wafer after 497

layers along the $\langle 110 \rangle$ SrTiO₃ azimuth. The presence of streaks indicates the growth of a smooth epitaxial Dy-Ba-Cu-O film. The streak spacing indicates in plane lattice constants close to, but slightly smaller than the SrTiO₃ (100) substrate ($a=b=3.80 \pm 0.05$ Å). Further, the in-plane lattice constants appear equal to within the resolution of our RHEED photos (± 0.05 Å), implying a tetragonal structure.

Figure 3 shows the RHEED pattern of another layer of similar composition that was grown without dysprosium and barium shuttering. It is also epitaxial, but the spots indicate that it has a much rougher surface than the shuttered sample. Note that its c-axis (three times as long as the SrTiO₃ subcell) is lying in the plane of the substrate, rather than perpendicular to it.

X-ray diffraction of the sample in Fig. 1 confirms that it is a highly oriented epitaxial layer. Further, it reveals two families of diffraction peaks, one with $c \approx 11.83$ Å and another with $c \approx 7.55$ Å, layered in the growth direction. The relative intensities of these two families of peaks vary across the sample with the latter structure more intense in the barium rich area. The existence of the two superstructure phases could arise from flux non-uniformity across the sample and/or to the total number of atoms in each flux burst or during each cycle not equalling precisely one "monolayer." This sample was not a superconductor as grown, and oxygen annealing only increased the resistivity.

The RHEED patterns of another growth that did produce a superconductor are shown in Fig. 2. Figure 2a shows the clean SrTiO₃ (100) substrate before growth viewed along the $\langle 110 \rangle$ azimuth. Figure 2b shows the same azimuth after the growth of about 50 Dy-Ba-Ba layers. The in-plane lattice constants ($a=b=4.15 \pm 0.05$ Å) are slightly greater than those of the SrTiO₃ (100) substrate. The presence of half-order streaks indicates a doubling of the unit cell (compare Fig. 2b with 2a and 1c). We have observed this same doubling in other copper poor samples. After increasing the total amount of incident copper per cycle (by lengthening the cycle period by 50%), increasing the dysprosium open time by 10%, and increasing the substrate temperature by 7 degrees, these half-order streaks became more faint as shown in Fig. 2c. The substrate temperature was briefly increased by another 25

degrees until RHEED showed polycrystalline growth (above ≈ 610 °C), then lowered to 600 °C for the duration of the growth. Figure 2d shows the RHEED pattern at the end of the growth. The presence of a superposition of rings and streaks indicates the presence of both epitaxial and polycrystalline material. The streak spacing indicates an in-plane lattice constant $a \approx 3.93 \pm 0.05$ Å, a lower value than earlier in the growth.

X-ray diffraction of the sample in Fig. 2 revealed that it was epitaxial with three families of diffraction peaks. One with $c \approx 11.83$ Å ($a \approx b \approx 3.86$ Å), the second with $c \approx 7.53$ Å and a third with $c \approx 4.04$ Å ($a \approx b \approx 4.09$ Å), layered in the growth direction. The 4.04 Å and 11.83 Å family of reflections had the greatest intensity. When rocked off the (100) SrTiO₃ substrate, the peaks were reduced to the same extent as the sample in Fig. 1, indicating that the majority of the film is epitaxially aligned to the plane of the substrate.

Figure 4 shows the resistivity versus temperature curve for the as grown sample of Fig. 2. The broad superconducting transition with onset near 60°K may be indicative of incomplete oxygen ordering in this metastable, apparently tetragonal, superconducting phase. However, the sample became insulating when annealed in oxygen up to 700 °C.

Direct evidence that the epitaxial growth mechanism is strongly affected by the shuttering of the barium and dysprosium fluxes is provided by the RHEED intensity oscillations. Figure 5 shows a plot of the diffracted RHEED beam intensity as a function of time while the barium and dysprosium beams are being shuttered during the growth of three samples. (Oscillations were observed but not recorded during the 123-like growth of VSC117.) These oscillations are relatively intense and are plainly visible to the naked eye. Before discussing the meaning of these oscillations, it is important to distinguish them from the RHEED oscillations often observed during molecular beam epitaxy of GaAs¹² as well as many other materials. In the case of GaAs, the oscillations arise from scattering intensity differences between complete and incomplete molecular layers which occur in a layer by layer growth mechanism. In our case, the composition of the incident flux is being modulated, so that the oscillations may result simply from modulation of the surface stoichiometry. Note the differences in

the shape of the oscillations for the two different runs. The variations in oscillation shapes are the subject of ongoing inquiry, but may signify the growth of different crystal structures.

Detailed crystallographic, structural and electrical characterization of the thin epitaxial films grown by oxygen plasma molecular beam epitaxy on strontium titanate substrates is in progress. A remarkable variety of structure is revealed, making clear both the possibilities and challenges for MBE as applied to the cuprate superconductors. The films are highly epitaxial, often with crystal structure similar to $\text{DyBa}_2\text{Cu}_3\text{O}_{7-x}$. These films can be superconducting, but are more often semiconducting or insulating, with lengthened c-axes, perhaps due to non-stoichiometry. The best conditions for epitaxy do not appear to be the best conditions for obtaining superconductivity; very nice epitaxial films have been grown with crystal structure very similar to that of the 90K superconductor, but which are not superconducting. Phases related to the $\text{DyBa}_3\text{Cu}_2\text{O}_x$ (the other perovskite¹³) also appear to be very important for epitaxial growth, and display distinctive signatures in the RHEED patterns. Preliminary evidence suggests that solid-solutions of this other-perovskite structure may exist metastably well outside its equilibrium range. Other epitaxial impurity phases including BaCuO_2 and possibly CuO have also been obtained. (The remarkable structure of BaCuO_2 ¹⁴ with its 360 atom unit cell, its 24-fold coordinated Ba and Cu_6O_{12} polyhedra would make it by far the largest and most complicated crystal structure ever grown epitaxially by MBE.) In studying a wide range of Dy-Ba-Cu-O films, from superconductors through insulators, all grown on SrTiO_3 by MBE, it is hoped that by understanding the nature of the films that can be grown under the present conditions, we can control what grows under different conditions.

We are currently studying epitaxy in the bismuth calcium strontium copper system. While some results have been encouraging, epitaxy of an in situ BCSCO superconductor phase has not been achieved. Insulating solid-solution bismuth oxide phases appear to dominate the epitaxy.

The amount that has been achieved in such a short time has been impressive. Still, much better knowledge of the structure and epitaxial characteristics of the impurity phases is needed to begin to understand

epitaxy of such a complicated system. Studies of surface structure and the RHEED oscillations will also be of great use. Much greater control over precise metal fluxes and oxygen plasma conditions in MBE must be achieved before the detailed mechanisms of growth in the dysprosium barium copper oxide system can be elucidated. The apparent metastability of the phases we have grown by MBE may be both a blessing and a curse. Although the metastable phases already made may have degraded superconducting properties compared to the stable target phases, the prospect that undiscovered metastable phases may have superior properties is enticing.

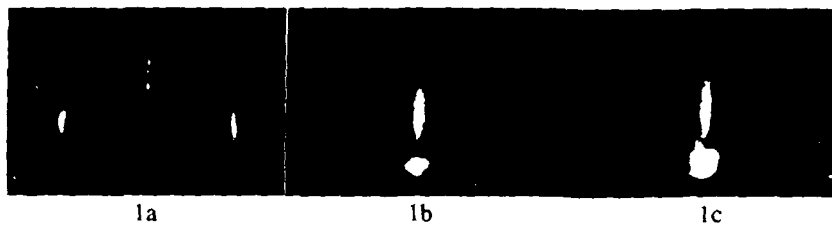


FIGURE 1

- (a) SrTiO_3 (100) substrate before growth, $\langle 100 \rangle$ azimuth, $T_{\text{sub}} \approx 540$ °C.
- (b) After 490 Dy-Ba-Ba layers (≈ 0.6 μm), $\langle 100 \rangle$ SrTiO_3 azimuth, $T_{\text{sub}} \approx 550$ °C.
- (c) After 497 Dy-Ba-Ba layers (≈ 0.6 μm), $\langle 110 \rangle$ SrTiO_3 azimuth, $T_{\text{sub}} \approx 550$ °C.

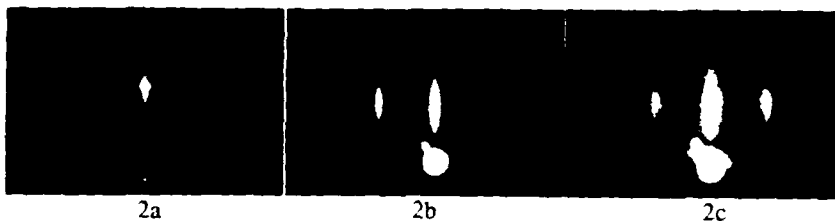


FIGURE 2

- (a) SrTiO_3 (100) substrate before growth, $\langle 110 \rangle$ azimuth.
- (b) After ≈ 50 Dy-Ba-Ba layers (≈ 600 Å), $\langle 110 \rangle$ SrTiO_3 azimuth, $T_{\text{sub}} \approx 583$ °C.
- (c) After 134 Dy-Ba-Ba layers (≈ 0.16 μm), $\langle 110 \rangle$ SrTiO_3 azimuth, $T_{\text{sub}} \approx 590$ °C.
- (d) After 313 Dy-Ba-Ba layers (≈ 0.37 μm), $\langle 100 \rangle$ SrTiO_3 azimuth, $T_{\text{sub}} \approx 600$ °C.

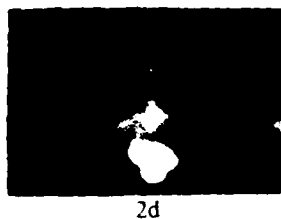




FIGURE 3
 (a) Unshuttered growth.
 $\approx \langle 110 \rangle$ SrTiO₃ azimuth.
 Composition Dy_{0.18}Ba_{0.33}Cu_{0.49}O_{7-x}.

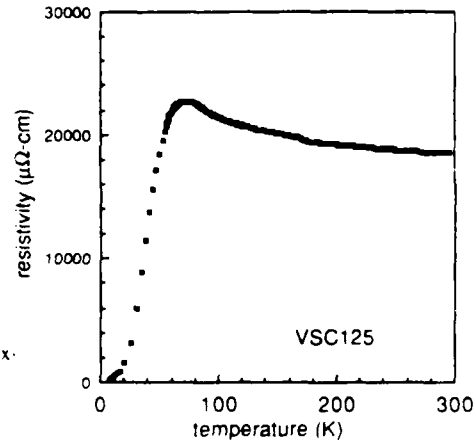


FIGURE 4

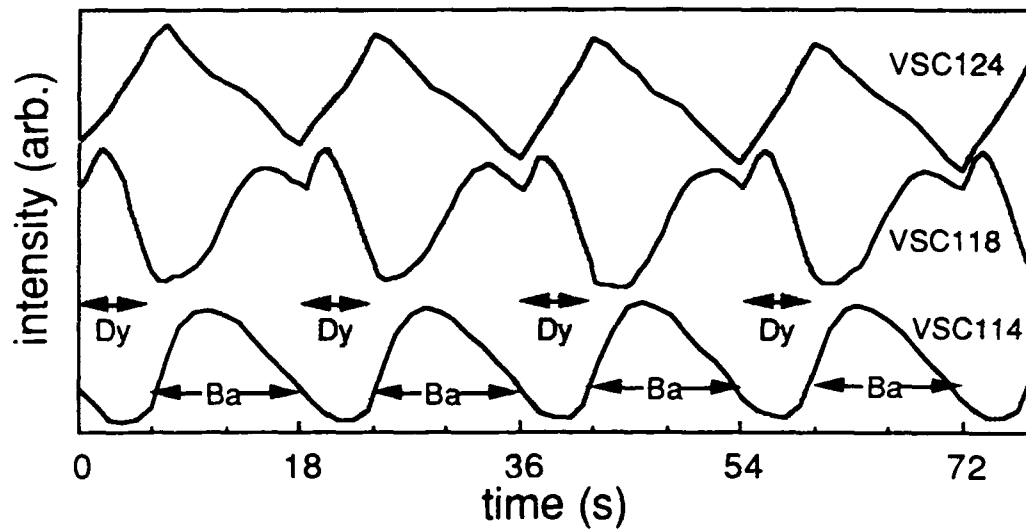


Figure 5 Diffracted RHEED beam intensity as a function of time (from an arbitrary starting point) while the barium and dysprosium beams are being shuttered during the growth of three samples. The shading indicates the periods where the Dy shutter is open and the Ba shutter is closed. The Cu shutter remains open throughout the growth.

JSEP SUPPORTED PUBLICATIONS

1. "Growth of High Tc Superconducting Thin Films Using Molecular Beam Epitaxy Techniques", C. Webb, S.-L. Weng, J. N. Eckstein, N. Missert, K. Char, D. G. Schlom, E.S.Hellman, M. R. Beasley, A. Kapitulnik, and J. S. Harris, Jr., *Appl. Phys. Lett.* 51, 1191 (1987).
2. "Molecular Beam Epitaxy and Deposition of High Tc Superconductors", E.S.Hellman., D. G. Schlom, N. Missert, K. Char, J. S. Harris, Jr., M. R. Beasley, A. Kapitulnik, T. H. Geballe, C. Webb, S.-L. Weng and J. N. Eckstein, *J. Vac. Sci. & Tech.* B6, 799 (1988).
3. "In-situ RHEED Characterization and Molecular Beam Epitaxy of DyBa₂Cu₃O_{7-x}", J. N. Eckstein, F. Turner, C. Webb, S.-L. Weng, D. G. Schlom, E.S.Hellman, N. Missert, J. S. Harris, Jr., M. R. Beasley and T. H. Geballe, *Bull. Am. Phys. Soc.* 33, 333 (1988).
4. "Molecular Beam Epitaxy of Layered Dy-Ba-Cu-O Compounds", D. G. Schlom, J. N. Eckstein, E.S.Hellman, F. Turner, C. Webb, J. S. Harris, Jr., M. R. Beasley and T. H. Geballe, *Extended Abstracts, High Temperature Superconductors II*, ed. by D. W. Capone, W. H. Butler, B. Batlogg and C. W. Chu (Materials Research Society, Pittsburg, 1988), 197.
5. "Molecular Beam Epitaxy of Layered Dy-Ba-Cu-O Compounds", D. G. Schlom, J. N. Eckstein, E.S. Hellman, S. K. Streiffer, J. S. Harris, Jr., M. R. Beasley, J. C. Bravman, T. H. Geballe, C. Webb, K. von Dessonneck, F. Turner, submitted to *Appl. Phys. Lett.*
6. "Characterization of Dysprosium Barium Copper Oxide Thin Films Grown on Strontium Titanate by Molecular Beam Epitaxy", E. S. Hellman, D. G. Schlom, A. F. Marshall, S. K. Streiffer, J. S. Harris, Jr., M. R. Beasley, J. C. Bravman and T. H. Geballe, unpublished.

JSEP SUPPORTED PRESENTATIONS:

1. "Molecular Beam Epitaxy and Deposition of High Tc Superconductors", E.S.Hellman., D. G. Schlom, N. Missert, K. Char, J. S. Harris, Jr., M. R. Beasley, A. Kapitulnik, T. H. Geballe, C. Webb, S.-L. Weng and J. N. Eckstein, presented at the 8th Workshop on Molecular Beam Epitaxy, Los Angeles, 9/87.
2. "In-situ RHEED Characterization and Molecular Beam Epitaxy of DyBa₂Cu₃O_{7-x}", J. N. Eckstein, F. Turner, C. Webb, S.-L. Weng, D. G. Schlom, E.S.Hellman, N. Missert, J. S. Harris, Jr., M. R. Beasley and T. H. Geballe, presented at American Physical Society March Meeting, New Orleans, 1988.

3. "Molecular Beam Epitaxy of Layered Dy-Ba-Cu-O Compounds", D. G. Schlom, J. N. Eckstein, E.S.Hellman, F. Turner, C. Webb, J. S. Harris, Jr., M. R. Beasley and T. H. Geballe, presented at the Spring Meeting of the Materials Research Society, Reno, 4/88.

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UNIT: 2

TITLE: Ultra-Submicron Devices

SENIOR PRINCIPAL INVESTIGATOR: R. F. W. Pease

RESEARCH ASSOCIATE: S. Y. Chou

GRADUATE STUDENT: D. R. Allee

SCIENTIFIC OBJECTIVE:

The objective of this project is to investigate heterojunction, quantum well and superlattice concepts and their application to new electronic devices with superior performance to devices based upon current semiconductor device principles. The small vertical dimensions which can now be readily achieved by molecular beam epitaxy (MBE) make it possible to fabricate superlattice structures which are dominated by quantum size effects^{1,2,3}. The long mean free path of the confined electrons in these structures makes it possible to fabricate lateral structures with a periodicity which is much less than a mean free path⁴. The properties of carrier transport and storage in various regions of these ultra-small, 3 dimensionally confined structures are not well understood and their application to an entirely new generation of electron devices is still in its infancy. The project will focus on new quantum mechanical and ultra-small 3-dimensional device concepts and techniques to define and realize such ultra small structures in both vertical and lateral dimensions

SUMMARY OF RESEARCH:

The development of molecular beam epitaxy (MBE) in the early 70's enabled the study of quantum size effects in tailored structures for the first time. Extensive investigation of AlGaAs/GaAs superlattice structures has uncovered a great deal of interesting physics. Novel electronic devices that are based on these quantum effects, such as the resonant tunneling diode, have been successfully fabricated. MBE however is a layer growth technology, and the quantum size effects demonstrated by MBE grown materials is necessarily perpendicular to the surface of the wafer. Electrons are limited to one-dimensional

confinement, that is confinement to a plane parallel to the wafer surface.

The potential to develop new electronic devices will be greatly enhanced if lateral electron confinement is a design option allowing the incorporation of lateral superlattices, quantum wires and quantum dots. There are two technologies capable of defining patterns laterally with sufficient resolution to observe quantum size effects: X-ray lithography and ultra-high resolution electron beam lithography (UHREBL). Using PMMA as the resist, UHREBL has a resolution limit of approximately 25nm structures on a 50nm period⁵. These dimensions are not as small as the layer thicknesses obtainable with MBE but are small enough to observe quantum effects at low temperatures.

We are primarily pursuing UHREBL as the lateral patterning technology of choice. An existing custom UHREBL has been adapted for device fabrication. These modifications include a stage that will hold 2 and 3 in. wafers for ease in later processing and a custom pattern generator that facilitates fine line lithography and has an alignment accuracy of 100nm.

As a precursor to the fabrication of quantum -well devices, a GaAs process sequence has been established by fabricating MESFETs and MODFETs with sub-tenth micron recessed gates on MBE grown wafers⁶. These MESFETs, with gate lengths down to 65 nm and transconductances as high as 330 S/m, are described in the attached publication⁷.

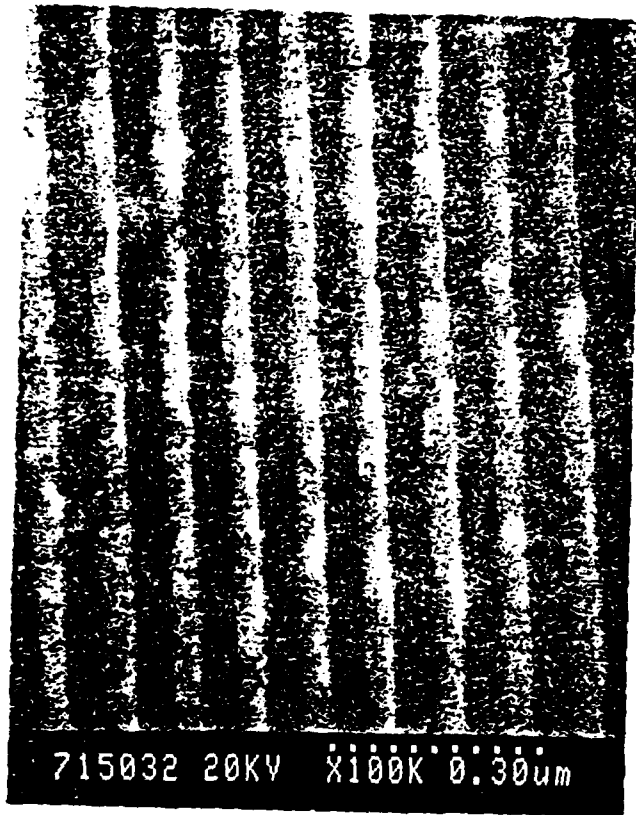
MODFETs with GaAs and InGaAs channels have been fabricated with gate lengths as small as 55 nm⁸. The GaAs channel MODFETs had transconductances as high as 415 S/m, and the InGaAs MODFETs had transconductances as high as 315 S/m. GaAs channel MODFETs were found to have a maximum effective saturation velocity of 1.95×10^7 cm/s at a gate length of 150 nm. The occurrence of this maximum effective saturation velocity near a gate length of 150 nm agrees with the predictions of Kizilyalli et. al. These devices were described in a paper delivered at WOCSEMAD (Monterey, Feb. 1988).

Work has continued on the fabrication of two lateral quantum

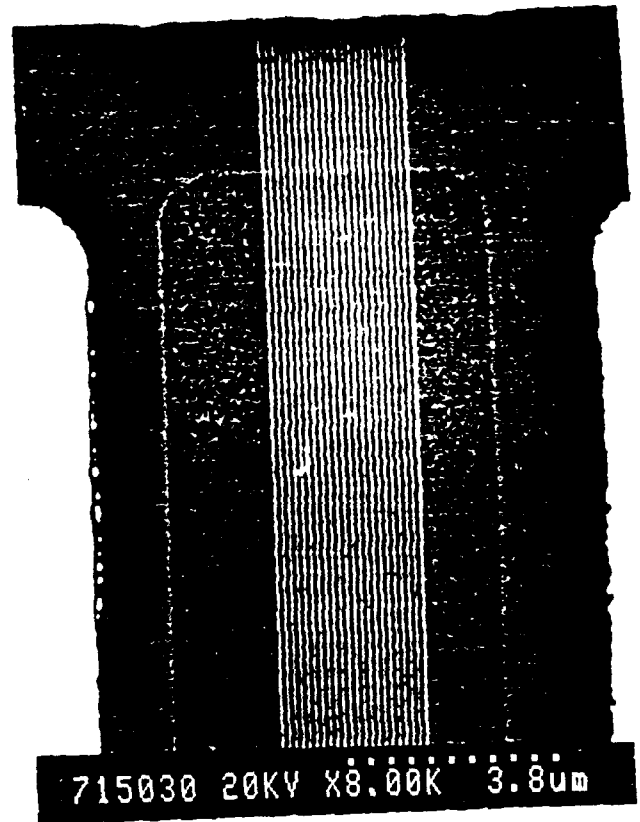
devices. The first is a lateral double barrier resonant tunneling MODFET in which the depth of the central well is tunable with a stacked gate configuration. The confinement and tunneling characteristics of the electrons in the central quantum wire will be studied as a function of temperature, electric and magnetic fields. This structure has device potential as a high speed three terminal resonant tunneling transistor. The second involving various combinations of grid and grating stacked gates in a MODFET. The possible device applications include tunable photon detectors, high frequency oscillators, and high speed switching transistors. There has been considerable progress in developing both the electron beam pattern generator in the metal structure of the gates and in the selective etching of the active region to assure device operation. Two photographs of device structures as shown in Fig. 1.

Much of the effort during the current reporting period has been to investigate potential improvements in electron beam lithography through the use of improved Monte Carlo analysis of the electron transport just following emission. In this region the electrons are initially emitted with a Maxwellian distribution of velocities but under certain conditions momentum transfer between the electrons results in a much broader energy spread^{10,11}. Such an increased spread leads to poor resolution. Our analysis employed an economical algorithm that allowed the use of a small computer (Apple Mac II) to describe graphically the developing energy distribution (Fig. 2) and, more importantly, indicated how unusual cathode structures such as those employs small-area, laser-induced emission¹² or semiconductor junction cathodes¹³ can deliver high brightness beams with energy spreads no greater than the Maxwellian distribution. Papers describing this work presented at the 1988 International Symposium on Electron Ion and Photon Beams and at the 1st International Conference on Vacuum Microelectronics; a journal article (manuscript attached) has been accepted for publication (J. Vac. Sci. Tech., Jan/Feb 1988).

In view of our need to concentrate on the fabrication and characterization of lateral quantum well devices alternative funding is being sought to resume the work on low energy-spread, high-brightness sources.

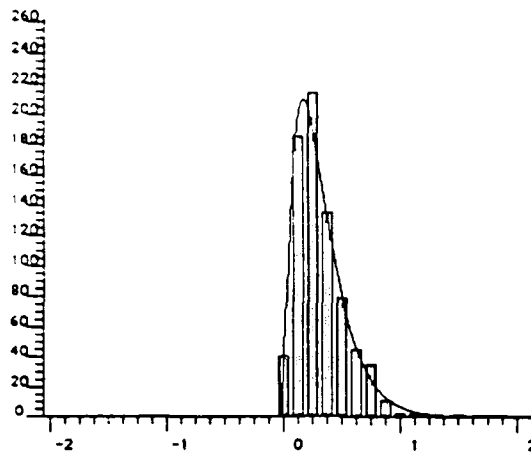


(a)

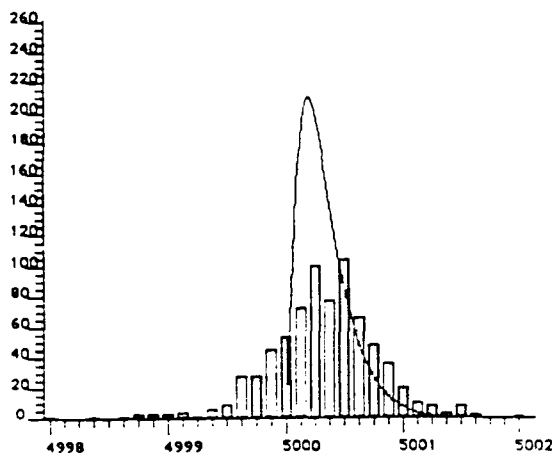


(b)

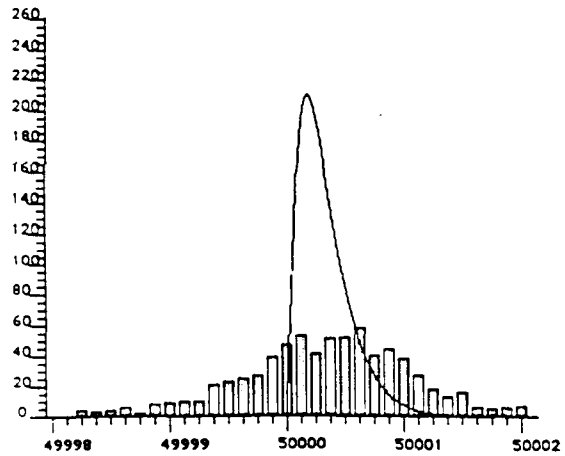
Fig. 1 Two lateral surface superlattice structures on MBE-grown GaAs/AlGaAs layered substrates. (a) shows 50nm wide Ti electrodes on 100nm centers (b) shows similar electrodes extending over an extended etched recess (channel) region of a MODFET type substrate.



(a)



(b)



(c)

Fig. 2 Number of particles vs. energy (eV) histograms for laser irradiated thermionic emission from lanthanum boride. The source current density is 20A/cm^2 , and the real source radius of 10m . The anode is 10mm away at 50kV . The solid line is the Maxwellian distribution for the source temperature. a) The energy distribution at the source. b) The energy distribution 1mm from the source. c) The energy distribution 10mm from the source. Roughly half the energy broadening occurs in the first 1mm .

JSEP SUPPORTED PUBLICATIONS AND PRESENTATIONS

1. D. R. Allee, J. D. Pehoushek, and R. F. W. Pease, "Novel Monte Carlo Simulation of Space Charge Effects in Laser Irradiated Thermionic and Photoemissive Electron Sources," presented at the 32nd International Symposium on Electron, Ion, and Photon Beams, Ft. Lauderdale, FL, May 1988.
2. D. R. Allee, P. R. de la Houssaye, D. G. Scholm, J. S. Harris and R. F. W. Pease, "Sub-100 nm Gate Length GaAs MESFETs and MODFETs Fabricated by a Combination of Molecular Beam Epitaxy and Electron Beam Lithography," in *Proceedings 31st International Symposium on Electron, Ion, and Photon Beams, Journal of Vacuum Science and Technology B*, 6(1), pp. 328-332, Jan./Feb. 1988.
3. D. R. Allee, P. R. de la Houssaye, D. G. Scholm, B. W. Langley, J. S. Harris, Jr., R. F. W. Pease, "Sub-100 nm Gate Length GaAs MESFET's Fabricated by Molecular Beam Epitaxy and Electron Beam Lithography," in *Proceedings IEEE/Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits*, Aug. 10-12, 1987, Ithaca, New York, pp. 190-198.

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 8. P. R. de la Houssaye, D. R. Allee, Y. -C. Pao, D. G. Scholm, J. S. Harris, Jr., and R. F. W. Pease, "Electron saturation velocity in MODFETs; InGaAs vs. GaAs channel devices; gate lengths to 500Å," WOCSEMMAd 1988, Monterey, CA, February 22,24, 1988.
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 11. D. R. Allee, J. D. Pehoushek, and R. F. W. Pease, "Novel Monte Carlo simulation of space-charge induced energy broadening in laser-irradiated cathodes," paper presented at International Symposium on Electron, Ion and Photon Beams, 1988, accepted for publication *J. Vac. Sci. Technol.*, Jan./Feb. 1989.
 12. A. M. E. Hoeberechts and G. G. P. van Gorkom, "Design technology and behavior of a silicon avalanche cathode", *J. Vac. Sci. Technol.* B4, Jan/Feb 1986, pp. 105-107.

Unit: 3

TITLE: GaAs on Si Integrated Circuits

PRINCIPAL INVESTIGATOR: B. A. Wooley

GRADUATE STUDENT: G. Nasserbakht

SCIENTIFIC OBJECTIVE:

The objective of this research is to investigate means by which newly emerging compound semiconductor technology, such as heteroepitaxial GaAs on Silicon, can be exploited at the circuit and system level. The emphasis of the program is on the application of GaAs/Si technology to optoelectronic circuits for broadband communication systems.

SUMMARY OF RESEARCH:

In optical fiber communication systems, where information is represented in both optical and electronic forms, the interface between the optical and electronic components often determines the overall system performance. At the receiving end of a fiber-optic channel this interface consists of a photodetecting device and the receiver electronics. The bandwidth and sensitivity of the overall system is typically limited by parasitic elements associated with the interconnection of the photodetector and the front-end preamplifier. The monolithic integration of these components would overcome this limitation by decreasing the parasitic interconnection capacitance. The main obstacle to achieving such integration is the necessary transition between two different semiconductor technologies at the interface. The optoelectronic properties of compound semiconductors make them the materials of choice for photodetectors, while silicon is often the preferred material for the front-end receiver and the subsequent VLSI circuitry used for data processing. Recent progress in the growth of epitaxial GaAs films on Si substrates has opened up the potential of merging these technologies in order to obtain substantial improvements in system performance.

In this research, we are pursuing the integration of a GaAs

photodetector with a silicon front-end preamplifier. The receiver amplifier has been designed in bipolar technology and successfully integrated at Hewlett-Packard. This amplifier is a transimpedance design using a shunt-series feedback architecture. A GaAs interdigitated MSM (metal-semiconductor-metal) photodetector is now being integrated on substrates containing the preamplifier. The overall circuit is expected to operate with a bandwidth of nearly 1GHZ and a transimpedance of 5KOHM.

To achieve the desired integration of the two technologies, a new fabrication process has been devised. An important feature of this process is its compatibility with Si processing. No special processing of the Si circuits is required other than they be fabricated on substrates with a special orientation. Following the fabrication of Si devices, an anisotropic KOH etch is used to form recessed trenches in Si, in which epitaxial GaAs is grown using an MBE process. After the completion of GaAs device fabrication, the wafer is metallized to form the Schottky barriers and establish the desired interconnections. The final topology is adequately planar, since GaAs is grown in recessed regions in Si. The input capacitance of the photodetector, including the diode capacitance and the interconnection stray capacitance is estimated to be about 0.2pf. This value competes favorably with even the lowest input capacitance values obtainable, using advanced packaging techniques, in a hybrid technology.

The fabrication of the Si circuits has been completed, and epitaxial GaAs has been grown on the wafer. Processing of the GaAs photodetector is currently in progress.

As part of this research, we are also investigating the integration of an NMOS preamplifier with a GaAs MSM photodetector. A transimpedance NMOS preamplifier has been designed and fabricated and further processing to fabricate the GaAs photodetector is in progress. The primary objective of this part of the research is to determine the extent to which fabrication of GaAs devices influences the characteristics of Si MOS devices and circuits.

Unit: 4

**TITLE: The Chemical and Electronic Structure of Refractory
Metal GaAs Interfaces**

**SENIOR PRINCIPAL INVESTIGATORS: C. R. Helms, I. Lindau and
W. E. Spicer**

GRADUATE STUDENTS: Margaret Kniffin and Carl McCants

SCIENTIFIC OBJECTIVES:

Refractory metals, particularly Ti, W, and Mo, are increasingly becoming the metallization of choice for the formation of Schottky barriers in GaAs devices. The objective of this work is to make a significant advancement in our level of knowledge of refractory metal-GaAs interfaces. This information will also contribute to a general understanding of GaAs Schottky barriers.

Having briefly described our general goals, more specific objectives of our experimental program are:

- To determine the effect of work function, metal electronic structure, interface intermixing, and chemical reactions on Schottky barrier height for refractory metal (especially Ti) GaAs interfaces.
- To quantitatively determine the effect of oxygen and GaAs surface defects on Schottky barrier height for Ti-GaAs interfaces.

SUMMARY OF RESEARCH:

Over the past year, we have continued to focus our attention on the changes that occur at the Ti/GaAs interface upon annealing for both clean (UHV cleaved) and oxide covered (chemically cleaned) substrates. A variety of surface spectroscopic techniques have been used to correlate changes in the interfacial chemistry to the electrical properties of the interface.

A. Electrical Properties

We have previously reported the effect of annealing on the

Schottky (SBH) of Ti diodes fabricated on chemically cleaned n-type (100) substrates^{1,2}. A 0.1 eV increase in the SBH was observed upon annealing to 350°C. The SBH then remained relatively constant up to 550°C. The change in barrier height was found to correlate with the onset of TiAs formation at the interface.

Electrical measurements (I-V) have also been performed on Ti/n-GaAs(110) diodes fabricated, annealed, and measured in situ in UHV. Figure 1 shows the n-type Schottky barrier height (SBH) as a function

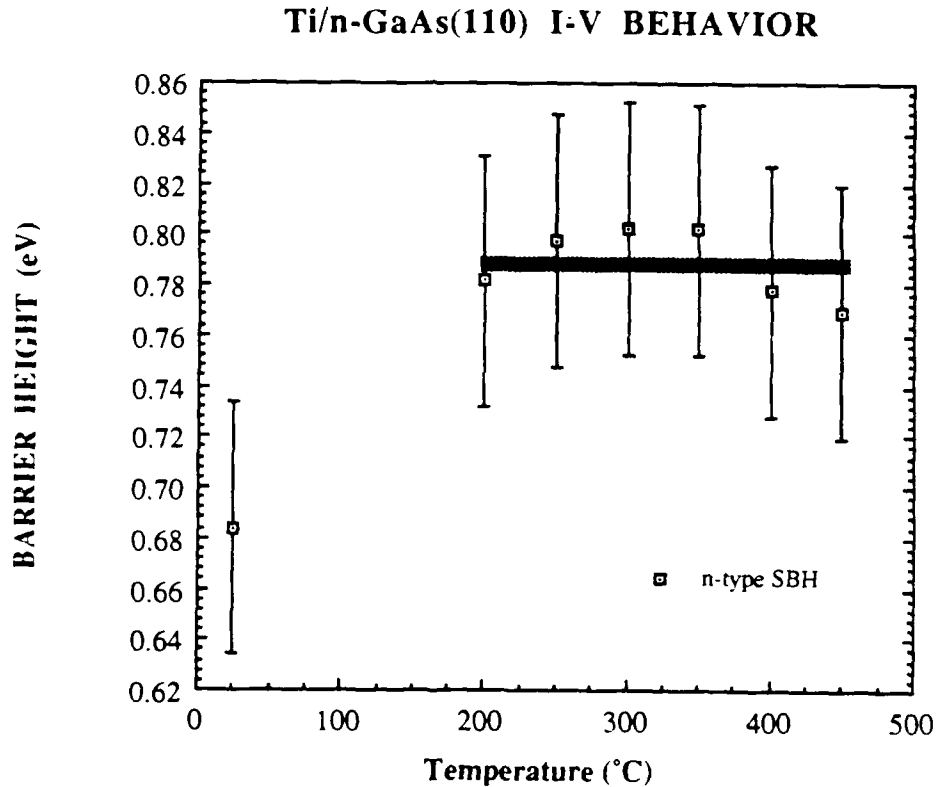


Figure 1 Plot of the Schottky Barrier Height (SBH) vs. annealing temperature for Ti/n-GaAs(110) diodes. The SBH increases by 0.1 eV at 200°C and remains relatively constant for temperatures up to 450°C.

of annealing temperature. We observe a 0.1 eV increase in the SBH after annealing to 200°C. This agrees well with prior work reported for similarly fabricated diodes annealed in situ at 320°C³ and also to those of the work described earlier on chemically cleaned GaAs (100) surfaces^{1,2}. We note, however, that the temperature at which we observe the change in barrier height is significantly lower than that at which the change is seen in the studies on the chemically cleaned (100) surface. We believe that this difference is due to the oxide layer present on chemically cleaned surfaces. This interfacial layer may retard interdiffusion and reaction between the Ti overlayer and GaAs substrate.

B. Interfacial Reactions

We have previously reported the effects of annealing, at temperatures below 500°C, on the morphology of the Ti/GaAs interface^{1,2,3}. Interfacial reactions were studied for thin (≈ 10 ml) coverages on UHV cleaved surfaces, as well as for thick (1000 Å) films deposited on chemically cleaned substrates. The Ti/UHV-cleaned GaAs study has been extended to include much thinner coverages. For the Ti/chemically cleaned samples some higher temperature results have been obtained. The results are summarized below.

1. Thin Films

For brevity we will discuss data from the 3.3 ML Ti study. Figure 2 shows the evolution of the Ga and As 3d core levels with increasing temperature for this thickness. The figure also shows the results of a curve fitting routine similar to what has been previously described⁴. All band bending shifts have been removed from the figures. The scale factors are in reference to the area and intensity of the appropriate as cleaved core level.

For the Ga 3d at RT, there is a significant reacted Ga component. However, we observe an intensity decrease of this reacted component with increasing temperature, with a dramatic decrease between RT and 315°C. There is only a slight shift to lower kinetic energy of the reacted Ga between 225 and 315°C; between 315 and 413 °C, the energy of the reacted Ga component shifts by ≈ 0.5 eV to lower kinetic energy. We note that at 475°C, emission from the reacted Ga component has become negligible. The steady increase in substrate intensity suggests

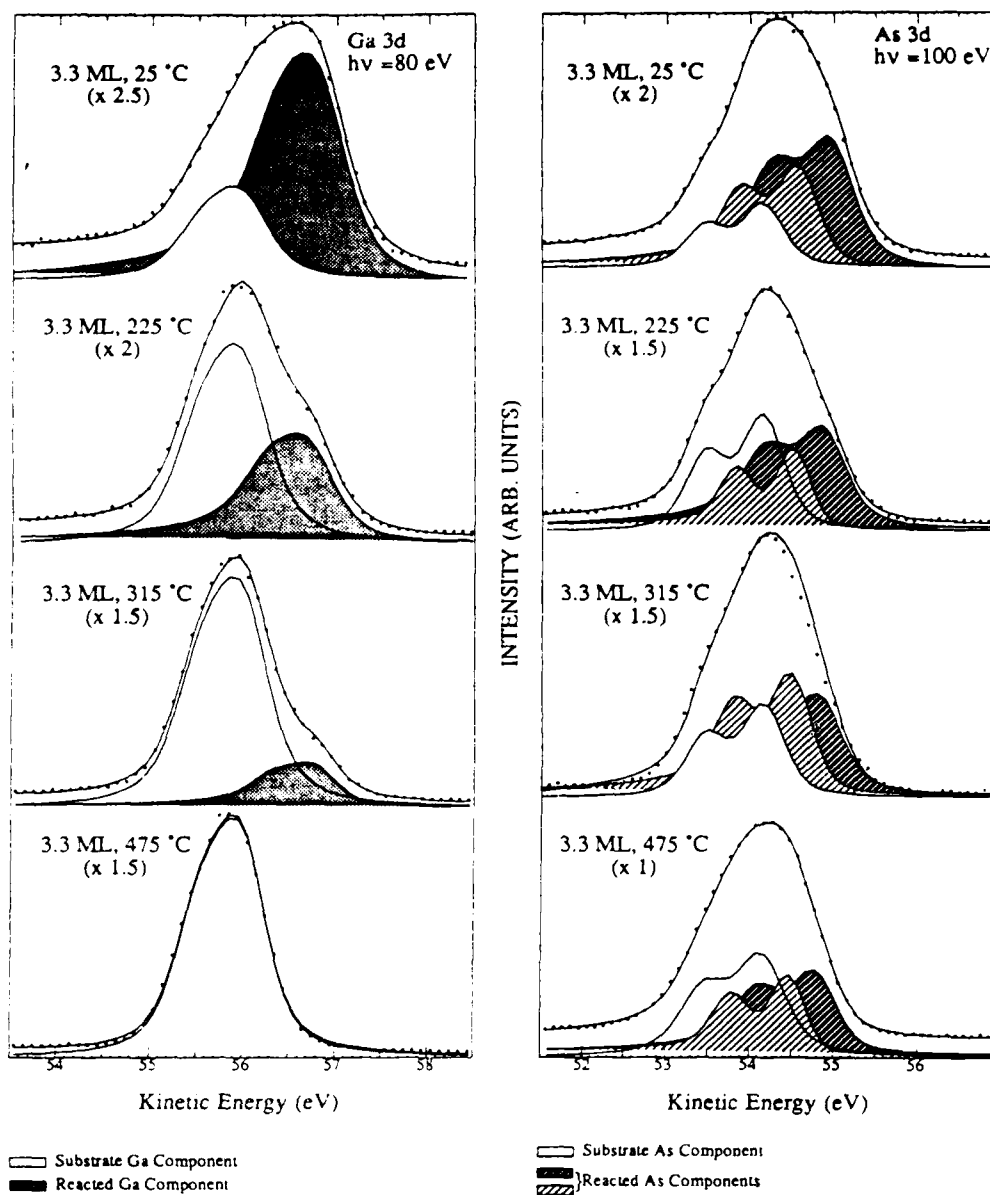


Figure 2 SXPS spectra of the Ga and As 3d core level for a Ti thickness of 3.3 ML taken at photon energies of 80 and 100 eV respectively. The shaded regions represent the reacted components of the Ga and As core levels. For the Ga, emission from the reacted component is negligible above 413°C, while the reacted As components remain over the entire range of annealing.

that the reacted Ga may be forming clusters of elemental Ga on the surface. Another possibility is that the Ga is evaporating at the highest temperatures.

The energies of the reacted As components remain stable over the entire range of annealing. There is an increase in the intensity of the substrate component between RT and 225°C, with only a slight change in intensity through the highest anneal temperature. The intensity ratio between the two reacted components changes between 225°C and 413°C, but at 475°C, is approximately the same as what is observed at RT. This suggests that the formation of a stable reacted As compound not only begins at RT for thicker layers, but this same stable compound is also formed at low coverages. What is striking, though, is that the intensity of the two reacted components does not decrease as we observed for the Ga. Instead, both reacted components are visible for the entire range of annealing, with only a slight change in the intensity of the substrate component. The change in scale factor does suggest that there is an increase in the amount of As near the interface.

The results from the Ga 3d core level decomposition indicate a marked difference from what is seen for thicker Ti overlayers, both at RT and after annealing. The RT energy position of the reacted Ga component is close to that for elemental Ga, rather than the dilute Ti-Ga alloy observed previously^{5,6}. When taken in context with the interfacial chemistry of the As, we suggest that the primary effect of annealing on the Ga is liberation from the substrate and a movement towards cluster formation on the overlayer surface. The data suggests that for these thin overlayers, the Ti layer becomes completely reacted. It has already been established that the Ti preferentially reacts with As at elevated temperatures³ and we have seen that this appears to be the case for thin overlayers as well. These observations imply that due to a limited amount of Ti, the Ga atoms move to the surface of the reacted Ti-As compound layer, where they either form clusters or evaporate. This may also provide an explanation for the sudden intensity decrease at temperatures $\geq 300^\circ\text{C}$ seen for Ti thicknesses of 6.7 and 10 ML⁷ on GaAs (110) and (100), respectively. As the reaction nears completion for these moderately thick overlayers, more and more of the Ti bonds with the As. Another important aspect of the GaAs(110) work previously reported³ is that

the width of the reacted Ga component changed very little with annealing. This again suggests that rather than a continuous change in stoichiometry from a Ti-Ga alloy to elemental Ga, what we observed was the effect of Ga atoms coalescing together, diminishing the effects of the dilution by the Ti.

In contrast to the Ga, the interfacial chemistry observed for the As is very similar to that seen for thicker overlayers. The reacted components remain relatively stable in energy over the range of annealing temperatures. What is significant is that emission from these components is visible for all annealing temperatures, which gives a further indication of the strength of the reaction between the Ti and As. At 1.3 ML, there is little change in the ratio between the substrate and reacted component areas between 215°C and 475°C, suggesting that the reaction has gone to completion. At 3.3 ML, the reaction does not appear to be complete until $T \geq 400^\circ\text{C}$. These results also have implications for understanding the properties of Ti interlayers used as diffusion barriers in GaAs device fabrication. Given the uniformity and stability of the Ti-As compound for Ti thicknesses as low as 1.3 ML, it seems that it is this compound, rather than pure Ti, which is responsible for the diffusion barrier properties.

As has been stated earlier and can be seen in Fig. 1, the Schottky barrier height changes at a temperature of 200°C. In a previous work, this change was correlated with the formation of a Ti-As layer contacting the GaAs substrate; it was suggested that the change in electronegativity of this layer with respect to Ti was the mechanism responsible for the change^{1,2}. In that study, though, no change in the interfacial reaction products were observed until a temperature of 350°C. In the PES studies for both "thin" and "thick" Ti overlayers, the amount of reacted As increases steadily over the entire range of annealing temperatures, with evidence of this reaction visible at temperatures $\sim 200^\circ\text{C}$. This would agree with the prediction of the AUDM which states that a decrease in anion antisite concentration should provide charge to pull the Fermi level towards the VBM and hence an increase in the n-type barrier height⁸.

2. Thick Films

A detailed examination of the interface morphology for contacts annealed up to 550°C has been described previously^{1,2}. In summary, the Ti was found to react with the substrate to form a uniform layered structure: Ti_{0.35}Ga_{0.65}/TiAs/GaAs. This structure was found to be both electrically and chemically stable up to 550°C. These results suggest that the Ti/GaAs system has the potential to form the basis of a good reacted contact metallization.

Current trends in GaAs device technology, however, are creating a demand for metallizations which can withstand processing temperatures up to 800 to 900°C. To address this issue, a preliminary investigation of the metallurgical stability of the Ti/GaAs system, in the temperature range 500 to 800°C was conducted.

Above 550°C the Ti:W cap, which was adequate for the low temperature annealing cycles, failed to prevent oxidation of the underlying titanium. The failure mechanism involved the outdiffusion of the Ti through the capping layer, where it was subsequently oxidized. After annealing at 800°C for 15 min., the Ti was completely consumed by the oxidation reaction, leaving the original cap in contact with the substrate. Similar behavior has been observed for other refractory metal/Ti/GaAs structures⁹.

This behavior is distinctly different from the behavior seen in refractory metal-titanium bilayers and multi-layers on silicon¹⁰. Currently it is not clear whether this stems from differences in the kinetics of these systems, or whether it arises from differences in the thermal stability of the relevant reaction products and their oxides. As most fabrication processes are carried out in oxygen containing ambient understanding what makes the Ti/GaAs system so much more susceptible to oxidation is an important issue.

Sputter-deposited WSi₂ caps were successful in inhibiting the oxidation reaction. Only a limited interfacial reaction between the silicide cap and Ti film was observed. Figure 3 shows the resulting microstructure for WSi₂ capped films annealed at 600 and 800°C for 30 min. The 600°C film has the Ti_xGa_{1-x}/TiAs/GaAs structure described in the previous section. Some segregation of the gallium to the

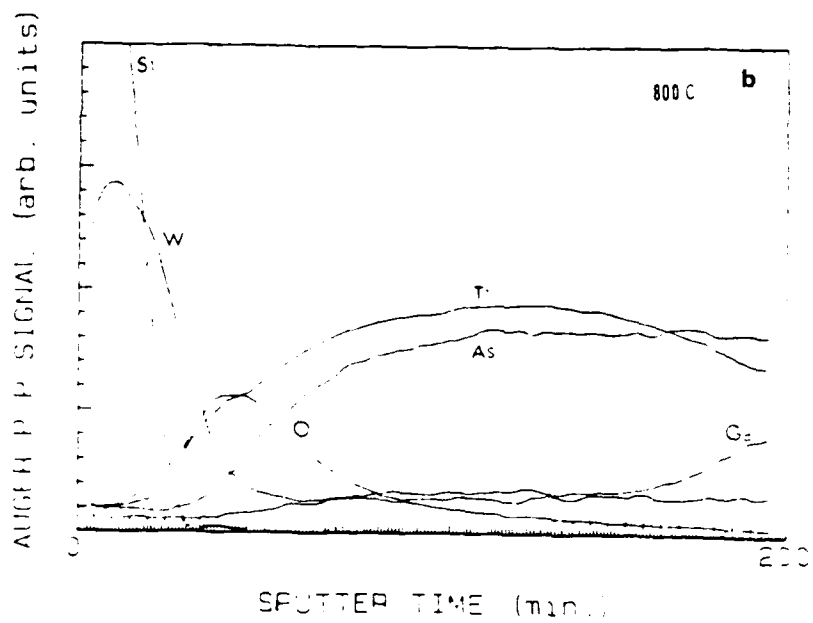
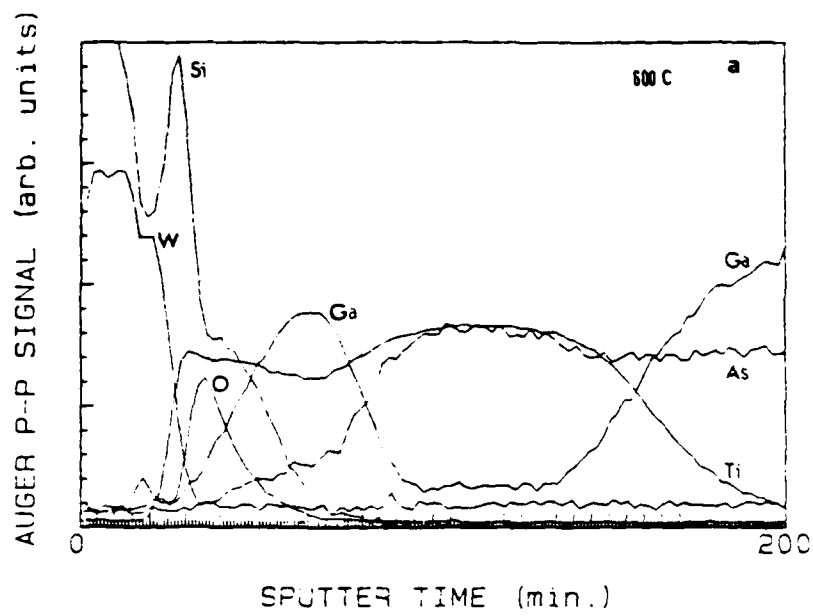


Figure 3 Auger profiles of WSi_2 capped samples annealed at (a) $600^\circ C$ and (b) $800^\circ C$ for 30 min.

Ti - Ga - As

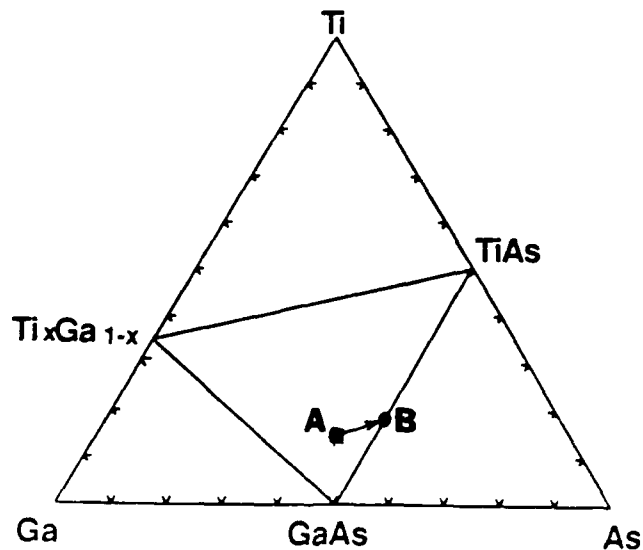


Figure 4 Partial Ti:Ga:As ternary phase diagram illustrating the shift in equilibrium from point A to B due to gallium outdiffusion.

surface and the WSi_2 interface was observed. At $800^\circ C$ however, a very different structure was formed. While the TiAs proved to be stable with respect to GaAs at these temperatures, it appears that rapid out diffusion and subsequent evaporation of the gallium has altered the system's equilibrium, as shown schematically in Fig. 4. Gallium loss seems to have moved the equilibrium point to the TiAs:GaAs tie line. Note that a substantially thicker TiAs film is formed as all the available Ti has been incorporated into this phase. A similar phenomenon was seen for the ultra-thin film studies and has been reported by Parker et al.¹¹, for thin TEM specimens annealed in situ. To our knowledge this is the first system for which formation of a single phase M:As film, due to gallium loss, has been observed. The formation of single phase Pd:Ga and Co:Ga films, due to As evaporation at high temperatures, has been reported, however^{12,13}.

Despite the relative instability of the Ti_xGa_{1-x} alloys, the TiAs/GaAs interface was, at least metallurgically, stable up to $800^\circ C$.

This suggests that metallizations based on this and other refractory metal arsenides may be suitable candidates for fabrication processes involving high temperature annealing cycles. We are currently investigating various means of fabricating TiAs/GaAs and other refractory metal arsenide/GaAs contacts.

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Unit: 5

**TITLE: The Study of Crystal Properties Using
Channeling Radiation**

SENIOR PRINCIPAL INVESTIGATOR: Richard H. Pantell

RESEARCH ASSOCIATE: Alan S. Fisher

GRADUATE STUDENTS: Charles Gary, Jae Kim, Xiaoyu Yang

SCIENTIFIC OBJECTIVE:

The purpose of the program is to investigate the properties of crystals in which relativistic electrons or positrons are channeled. In previous work, we used this technique to measure crystalline potentials, to observe the effect of nitrogen platelets on the diamond lattice, to observe and quantify electron-induced damage effects in certain materials, to determine thermal vibrational amplitudes, and to measure channeling lengths in III-V compounds, alloys and superlattices. Future research will involve studies of defects and properties of electronic semiconductors, investigations of strained superlattices, and observations of damage effects in semiconductors.

SUMMARY OF RESEARCH:

Last year's report described the new channeling-radiation beamline installed on the Mark III electron linear accelerator at Stanford University. Previous channeling experiments used a beamline at the Lawrence Livermore National Laboratory, but the Livermore accelerator is no longer operating. Furthermore, our move to the Mark III allows us to take advantage of its high average current. This effort has been funded primarily by the Air Force Office of Scientific Research, to obtain a source of hard x-rays from channeled electrons. The JSEP program has provided an important increment in funding to allow this considerable investment in capital equipment to be used for studies of electronic semiconductors.

During the past year, the new beamline has been used to measure channeling spectra at high currents for the first time. In addition, we

have installed, and are continuing to install, a number of improvements to our beamline, our x-ray monochromator, and our control and data-acquisition electronics. These efforts are discussed below.

At Livermore, channeling spectra were measured using time-average currents of ≈ 10 pA. Such low currents allowed spectra to be taken by analysis of the pulse height of individual x-ray photons in a solid-state detector. This method is relatively resistant to noise from high-energy background radiation, because the pulse height from high-energy photons is easily distinguished. However, the ≈ 10 - μ s processing time restricts the technique to fluxes of one photon per accelerator pulse, so that defect formation was measured in the past by comparing spectra taken before and after high-current bombardment.

To permit measurements with time-average currents of up to 10 μ A, our new beamline uses a Bragg monochromator instead of pulse-height analysis. With this method, Bragg diffraction selects an energy, and a scintillator and photomultiplier give a signal proportional to the number of photons collected in each accelerator pulse. Scanning the Bragg angle produces a spectrum. The disadvantage is a much greater sensitivity to the high-energy background, which is always present when a high-current beam strikes a target. The Bragg crystal is an excellent low-energy filter, but high-energy photons can still reach the scintillator by Compton scattering and other processes. We employ several methods to improve the signal-to-noise ratio, including massive concrete and lead shielding around the monochromator, stacks of lead and brass collimator slits before and after the Bragg crystal, and background subtraction (with the target crystal oriented so that no channeling occurs). For further improvement, we usually do not use a pure crystal, such as silicon, for our Bragg crystal, but instead use a graphite crystal with a mosaic spread of grain orientations to broaden the filter bandwidth and thereby increase the signal by a factor of 40. The lattice spacing of graphite is suitable for photon energies up to 30 keV; a LiF (422) crystal with a mosaic spread is now being tested for energies up to 60 keV.

To take these spectra, the Bragg crystal must be stepped through a sequence of angles, while the integrated signal, totaled over several accelerator macropulses (see below), is recorded for each. We have

developed a computerized system, using an IBM PC/XT and a CAMAC interface, to do this automatically. CAMAC modules control various stepping motors and monitor the beam current and the detectors. In addition to taking spectra, the system is also used to locate the planes of the target crystal. The target is mounted in a goniometer with three axes of rotation and one of translation. The crystal is rotated around one axis while an ionization chamber detects the x-ray flux at all energies. The signal peaks when a crystal plane is aligned with the beam. By taking several such scans while varying the other axes, a map can be built up to determine the crystal's orientation.

In the high-current experiments, we have channeled electrons through the (100) and (110) planes of silicon. Previous experiments have shown that defects form very slowly in silicon, and, despite hours in the high-current beam, our measured spectra [e.g., Fig. 1(a)] display the expected channeling peaks.

An important feature of this radiation is its time structure. In an rf linear accelerator, the electrons are tightly bunched at the peak of each microwave period. For the Mark III, these electron bunches (micropulses) are 0.5 to 2 ps long and are separated by 350 ps. This pattern continues over the 3- μ s duration of the klystron pulse (the macropulse), and these pulses repeat at 15 Hz. As a result, while the average current is microamperes, the peak current is typically 60 A. The peak photon flux per keV bandwidth at a typical spectral peak, the 32-keV peak of Fig. 1(a), is 2×10^{18} photons/(s.sr.keV). This is the only intense source of picosecond x-rays known (synchrotron radiation from storage rings has pulse durations from 0.1 to 2 ns), and, like synchrotron radiation, it is narrow band, tunable, and highly directional. We are now considering various experiments using this beam as a source, to take advantage of its unique features.

We are also now preparing to study channeling in a $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ strained superlattice. As last year's report explained the periodicity of the superlattice can combine with the transverse oscillations of the electrons in the channel to create new spectral peaks or enhance existing ones. We have obtained a superlattice sample with 425- \AA layer thicknesses and $x = 5.3\%$. The superlattice peak, at 59 keV, cannot be resolved with the graphite Bragg crystal and is awaiting the LiF. A second superlattice, with 850- \AA layers and $x = 5.3\%$, is now

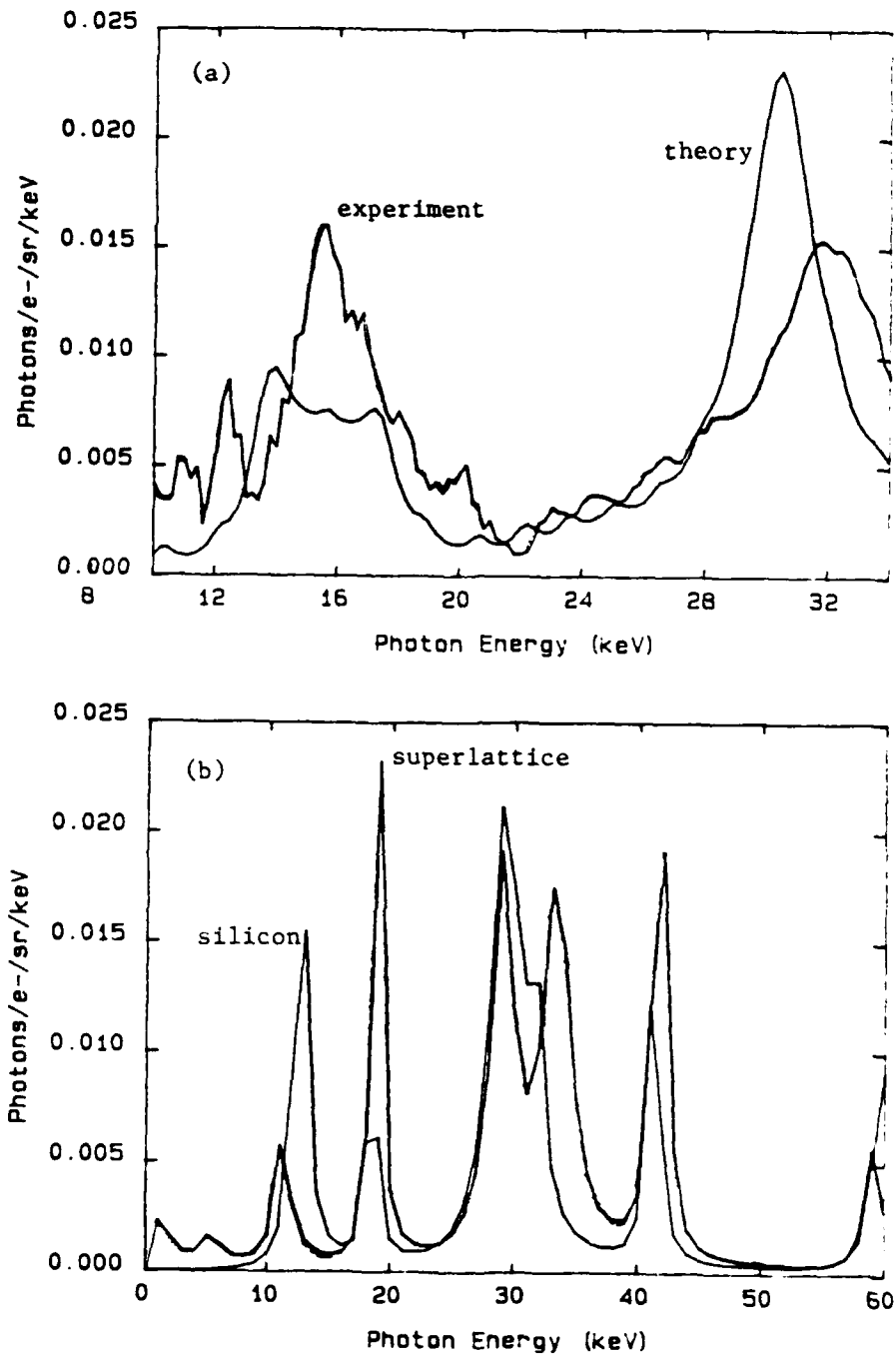


Figure 1. (a) Theoretical and experimental channeling spectra of 27.7-MeV electrons through Si (100). A Bragg-angle error of 0.25° , significant only at high energies, displaced the 30-keV peak by 2 keV. (b) Calculated (100) channeling spectrum of 27-MeV electrons through an 850-Å $\text{Si}_{.947}\text{Ge}_{.053}/\text{Si}$ superlattice, compared to pure Si. Note that the superlattice generates an extra peak at 33 keV and enhances other Si peaks.

being fabricated; its spectrum is shown in Fig. 1(b). Such spectra should prove useful for the study of superlattices and also as an easily tuned radiation source, since the effective period of the electron's motion due to the strain can be changed, while still channeling in the same plane, by varying the angle of incidence of the electron beam.

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Unit: 6

**TITLE: Complementary MOS Device and Material
Physics at 77°K**

PRINCIPAL INVESTIGATOR: J. D. Plummer and K. C Saraswat

**GRADUATE STUDENTS: A. Henning, J. Watt, T. Schreyer
and J. Woo**

SCIENTIFIC OBJECTIVES:

The overall objective of this work is to investigate the fundamental physics of operation and potential for VLSI circuits, of silicon CMOS devices operated at 77°K. Our work in this reporting period has concentrated on two areas: experimental measurement and modeling of MOS device characteristics at low temperature; and measurement and modeling of circuit interconnects at low temperature. Progress in each of these areas is described below. Our work on bipolar device physics and on hot carrier effects both at low temperatures, was completed at the beginning of this reporting period and resulted in two Ph.D. dissertations.

A. MOS DEVICE PHYSICS AT LN₂

Accurate predictions of CMOS circuit performance at room temperature and liquid nitrogen temperature are necessary to assess the viability of a cooled CMOS technology. Furthermore, an accurate modeling capability is essential to optimize device and circuit design for maximum performance. Since the performance of a circuit is determined by the MOS device characteristics as well as the properties of the load being driven, both of these areas have been addressed in this research.

During the past year, we have examined the theory and measurement of charge-voltage characteristics of MOS devices. The ac split CV technique has been used to measure the gate-channel capacitance of n- and p-channel MOSFETs with channel doping densities in the range $3E16-4E18$ cm⁻³ at both 295°K and 77°K. Comparison to simulation has revealed a stretch-out of the measured characteristics which can

be well modeled assuming a lateral threshold voltage nonuniformity with a Gaussian probability distribution. The standard deviation of the threshold voltage distribution varies from 25 mV to 375 mV as doping density increases with very little dependence on dopant type or temperature. The observed variance of the threshold voltage has been accurately predicted by a three-dimensional model based on the method of images which includes only the contribution from a random distribution of dopant ions in the depletion region.

In addition to affecting the charge-voltage characteristics, surface potential fluctuations also affect carrier transport in MOS devices by introducing potential barriers in the channel. The resulting thermally activated transport process causes a reduction in the effective carrier mobility at low inversion charge densities which has been characterized for both n- and p-channel devices at room and liquid-nitrogen temperature. While the mobility behavior of holes has been predicted by a simple barrier model, there is additional degradation in the case of electrons which may be due to ionized impurity scattering.

The results of this study clearly demonstrated the presence of surface potential fluctuations in MOS devices resulting from the random channel dopant ion distribution. While the effects of the surface potential fluctuations do not become significant until doping densities approach the 10^{18} cm⁻³ level at room temperature, measurable departures from simple theory occur over the entire doping density range studied. At liquid-nitrogen temperature the fluctuations induced by the channel dopant ions are substantial even at doping densities in the 10^{16} cm⁻³ range and must be considered to accurately model device behavior.

During the past year we have also extended earlier inversion layer mobility measurements to higher surface normal fields, higher levels of substrate doping and low temperature. It has been known for some time that a universal relationship exists between the effective mobility of electrons at room temperature and an effective field in the inversion layer. We have shown for the first time that similar relationships exist for holes at room temperature and both electrons and holes at liquid nitrogen temperature. Deviations from the universal curves occur in all cases at high levels of substrate doping as a result

of ionized impurity scattering. We have developed a new inversion layer mobility model based on the universal curves and included for the first time the effects of ionized impurity scattering from channel dopant ions.

The PISCES two-dimensional device simulator has been modified to include the new inversion layer mobility model. The addition of this model gives PISCES the capability to accurately predict the characteristics of small geometry MOS devices at both room temperature and liquid nitrogen temperature. The results of PISCES simulations have been compared to measurements of 1.25 micron NMOS device designed for operation at liquid-nitrogen temperature. The modified program has been used to accurately predict the short channel effects in the subthreshold region and the IV characteristics in the linear region. We have used PISCES to extract values for the saturated drift velocity of electrons at room temperature and liquid-nitrogen temperature by matching the experimental measurements to simulations. The values we have determined are $8.5e6$ cm/s at 295 K and $10.25E6$ cm/s at 77°K.

B. Interconnects and their Effect on Circuit Performance at Low Temperatures

Having examined the behavior of thin film metal resistance and of contact resistance at low temperature, it was determined that neither of these would be a problem at 77°K. Contacts to heavily doped silicon exhibit only a slight, if any, increase in resistance. Resistance of thin Al, Al-Si, and Al-Cu-Si films was also examined at low temperatures. These films showed a reduction in resistivity by a factor of 5-10, and bulk behavior was obtainable when clean deposition conditions were maintained.

This behavior seems very favorable to 77°K CMOS operation. But to understand the impact these effects will have on circuit speed, it is necessary to examine the behavior of actual interconnections, and determine how their performance depends on metal and contact resistance.

An analysis of the delays caused by interconnections in VLSI integrated circuits was undertaken. This analysis examined the effects metal resistance and silicon conduction have on signal propagation,

where the interconnection is modeled as a microstrip transmission line over a dual dielectric. The top of these two dielectrics, the oxide, is a perfect (lossless) insulator, while the other dielectric, the silicon, is conductive and lossy.

Because of the complexity of this type of problem, it is best to perform computations in the frequency domain, and then convert them to time domain using an inverse Laplace or Fourier transform. But this requires modeling the transistor driving the line as a linear device. A graphical technique which can determine the reflections generated at any non-linear device on a lossless (superconducting or ideal) transmission line was developed; use of this technique showed that it is possible to define an effective equivalent resistance and source voltage, which may be used to model the transistor in the frequency domain calculations. For CMOS circuits, the best model for the transistor is one which has a voltage source, with voltage equal to V_{DD} (for pull-up transistors) or zero (for pull-down transistors) in series with a resistance R_{eff} , where $R_{eff} = \frac{V_{ds}}{I_d} |_{V_{ds}=V_{DD}/2}$. This definition allows that the transistor will be matched to the transmission line if $R_{eff} = Z_0$, the characteristic impedance of the line.

Interconnection step responses were computed by solving the telegraphers' equations for microstrip transmission lines over Si | SiO₂ substrates in the frequency domain, and converting the solution to time domain via an inverse Laplace transform. Experimental data, was obtained from Time Domain Reflection (TDR) and Time Domain Transmission (TDT) measurements on similar lines. The computed responses show good agreement with the measurements, thus verifying the computer model. The computer model was then used to isolate and evaluate the impact metal and silicon losses have on interconnection response.

The results of this examination show that there are three possible modes of signal propagation in VLSI interconnections. This had previously been concluded for single frequency (or narrow bandwidth) signal transmission, but had not been determined for step (very broad bandwidth) signals. The propagation mode depends upon the geometry of the line and the resistivity of the substrate. The so-called slow wave mode, which has been assumed in previous analyses, is generally

NOT the predominant propagation mode at VLSI geometries.

Losses from the resistance of the interconnection metal may cause signal dispersion and slow interconnection response time, but this occurs only if the total (DC) resistance of the line is greater than its characteristic impedance. With aluminum interconnections operating at room temperature, this occurs only for line lengths of one centimeter or more. Therefore it may be concluded that only long lines made of silicide or polysilicon will exhibit resistive effects. Operating aluminum lines at 77°K, or replacing aluminum with a high T_c superconductor will not increase circuit speed appreciably.

JSEP SUPPORTED PUBLICATIONS:

1. J. T. Watt, B. J. Fishbein and J. D. Plummer, "A Low-Temperature NMOS Technology with Cesium-Implanted Load Devices," *IEEE Transactions on Electron Devices*, Vol. ED-34, No. 1, January 1987, p. 28.2. T. A. Schreyer, P. J. Wright and K. C. Saraswat, "The Effect of Superconducting Interconnect on Circuit Performance," presented at the IEEE 45th Annual Device Research Conference, Santa Barbara, CA, June 1987.
2. J. T. Watt and J. D. Plummer, "Universal Mobility-Field Curves for Electrons and Holes in MOS Inversion Layers," *Proceedings of 1987 Symposium on VLSI Technology*, Karuizawa, Japan, Paper IX-2, p. 81.
3. J. T. Watt and J. D. Plummer, "Efficient Numerical Simulation of the High Frequency MOS Capacitance," *IEEE Transactions on Electron Devices*, Vol. ED-34, No. 10, October 1987, p. 2214.
4. J. T. Watt and J. D. Plummer, "Effect of Interconnection Delay on Liquid Nitrogen Temperature CMOS Circuit Performance," *Proceedings of the International Electron Devices Meeting*, Washington, D. C., December 1987, Paper 16.4.
5. T. A. Schreyer, A. J. Bariya, J. P. McVittie and K. C. Saraswat, "Specific Contact Resistivity Measurements of Reactive Ion Etched Contacts," *J. Vac. Sci. Technol. A* 6 (3), May/June 1988, p. 1402.
6. T. A. Schreyer, Y. Nishi, K. C. Saraswat, "A Complete RLC Transmission Line Model of Interconnect Delay," in *Proceedings of 1988 Symposium on VLSI Technology*, San Diego, CA, May 1988, p. 95.

JSEP SUPPORTED PRESENTATIONS:

1. T. A. Schreyer, P. J. Wright and K. C. Saraswat, "The Effect of Superconducting Interconnect on Circuit Performance," presented at

the IEEE 45th Annual Device Research Conference, Santa Barbara, CA
June 1987.

2. J. T. Watt and J. D. Plummer, "Surface Potential Fluctuations in MOS Devices Induced by the Random Distribution of Channel Dopant Ions," presented at the 46th Annual Device Research Conference, Boulder, CO, June 1988, Paper IIA-4

JSEP SUPPORTED PhD DISSERTATIONS:

Albert Karl Henning, "Hot Carrier Effects In CMOS Field Effect Transistors At Cryogenic Temperatures," August 1987.

Jason C.S. Woo, "Operation Of MOS and Bipolar Transistors at Liquid Nitrogen Temperature," September 1987.

Unit: 7

TITLE: Coding for Spectrally Constrained Channels

PRINCIPAL INVESTIGATOR: J.M. Cioffi

**GRADUATE STUDENTS: J. Aslanis, G. Dudevoir, P. Fortier,
S. Kasturia and A. Ruiz**

SCIENTIFIC OBJECTIVES:

Our objective continues to be the design of codes for channels with severe intersymbol interference (ISI). This objective has been initially achieved through the invention of a method that we call "Vector Coding" (VC) [1],[2]. Our recent emphasis has been on a number of methods that can be used to improve the applicability of vector coding and to explain the large improvements that it displays with respect to previous coding and equalization methods for channels with severe ISI.

SUMMARY OF RESEARCH:

Our work for the past year can be decomposed into three main categories: analysis of VC, application of VC methods to the ISDN digital subscriber loop, and reduction of implementational complexity through the use of block equalization methods. Each of these categories will be subsequently summarized in more detail. Basically, we have been able to demonstrate that VC achieves the highest possible coding gain, on any linear gaussian noise channel, for finite complexity of implementation. We have also extended vector coding to the very important case where several digital communication channels are co-located and crosstalk interference dominates performance measures. Again, here, we can show that gains are as high as can be practically achieved. Additionally, we have developed a theory of block (as opposed to symbol) equalization that can be used to reduce implementation complexity to well within acceptable levels.

Analysis of Vector Coding

Vector Coding (VC) is best summarized in the two enclosed papers [1] and [2], currently under review for publication. VC is designed for

bandlimited channels with severe ISI - so severe that conventional equalization methods perform below acceptable thresholds. The basic concept has its roots in the fundamentals of detection theory, which generally dictate that optimal detectors for channels with severe ISI must observe an infinite time interval at the channel output before a decision can be made. Conventional equalization methods try to eliminate channel memory (ISI) so that an instantaneous decision (often called "symbol-by-symbol" detection) will suffice. VC methods can be used to eliminate channel memory only between successive blocks of symbols. Then, performance somewhere between optimal and symbol-by-symbol can be achieved. Even for channels with very severe ISI, the block length need not be excessively large to effectively obtain the performance that would be obtained by the optimal detector that spans an infinite time interval. However, a special coding method must be ascribed within the successive (independent) blocks in order to realize the largest possible gain. The combination of the elimination of block interference between successive blocks and the application of the associated code is what we term "Vector Coding".

The analysis of VC has proceeded along two avenues: showing that VC achieves the highest possible gain and determining this highest possible performance level for any particular channel.

The first objective has been obtained through an analysis of VC using the so-called "computational cut-off rate" parameter for channels with ISI, often denoted R_0 (for instance, see Gallager [8]). Basically, R_0 is a maximum rate that can be achieved on a digital communication channel with a finite amount (realizable in practice) of implementation complexity. In the enclosed invited paper to Milcom '88, we show that VC achieves R_0 for any ISI pattern and for any correlation of the additive gaussian noise. R_0 had only previously been achieved in a very limited sense for an **ISI-free** channel with additive **white** gaussian noise by the so-called "trellis coding" methods, originally introduced by Ungerboeck [9]. This performance level is illustrated in Figs. 1a and 1b for a typical digital subscriber loop channel and for the DC-blocking 1-D channel, respectively. The second objective has been achieved through the use of a single, though complicated, formula that is presented in both [1] and [2] (see formula (2), p. 26 of [1]). The formula conveniently summarizes two (often

opposing) effects in computing the gain of VC for a particular channel. The first term describes the coding gain that is due to the application of good coset codes [10] to the finite block channel through the partitioning of a particular block use of the channel via our VC method described in [1]. The second term represents an inevitable channel-dependent coding gain loss for the channel that increases with the severity of the ISI. Note that the fraction ("frac") of the Nyquist band used is critical to both terms in this formula. Figure 2 illustrates this dependence for the $(1+D)^2(1-D)$ partial response channel, and also illustrates that as available transmit power increases (more bits/T transmitted), the optimal (highest gain) fraction of bandwidth to be used approaches unity.

Application to the Digital Subscriber Loop:

There is increasingly intense interest in the application of VC methods to the ISDN digital subscriber loop. In particular, the American National Standards Institute, under committee T1E1.4 is now considering standardization of an 800kbps digital service over most twisted copper pairs of interest.¹ Of crucial importance in applying any coding method to twisted-copper-pair channels, as are of interest in this application, is the presence of crosstalk from adjacent channels. In this context, VC must be extended to allow the possibility that an adjacent (independent) transmitter may also be simultaneously using the same coding method to try and boost his rate to the highest possible level. This problem has been solved and was presented in a special invited presentation at the International Conference on Communications (ICC '88) [4] recently. Since then, Bellcore has produced a simplified version of VC [11], to be published, that achieves 800kbps in their laboratory tests. The reader is deferred to [4] for further details. Another special session at ICC '89 (June '89, Boston) has been organized, and our work has also been invited for presentation at this conference [5a,b]. Further, a journal paper on this subject is now under preparation and should be submitted shortly. Probably the most striking result, from this submission or from [5a,b] is shown in Fig. 3, where achievable data rate is plotted versus transmitter power. There we illustrate for a representative channel that 1.6 Mbps is just barely achievable on a single channel for reasonable transmitted power

¹Two such services would total 1.6 Mbps, allowing the transmission of one of the most important digital services in ISDN, the so-called "Primary Access" rate of 1.536 Mbps, which is also called H11 or T1 carrier.

even in the presence of absolute worst-case crosstalk. Further, we note in Fig. 3, that when crosstalk is considered, almost 12dB of improvement of VC with respect to conventional schemes at the ANSI-standard target rate of 800kbps.

Block Equalization and Complexity of Implementation:

The final category of study has been the use of block equalization methods to simplify the implementation of VC. The VC methods in [1] and [2] can require very long block lengths (several hundred), which can be unacceptable for implementation. These long block lengths can be reduced by an order of magnitude, without sacrificing gain, through the use of the Block Decision Feedback Equalizer (BDFE). We will introduce this concept in the enclosed Globecom '88 paper in December [6]. This technique will also appear in a Globecom '88 paper by Lechleider of Bellcore [12], although the Bellcore BDFE does perform a few dB worse than our method, as it does not use the best energy assignment on the associated code.

The basic concept is that trailing interference from previously transmitted blocks is subtracted (because it is already known) at the receiver. This method removes a considerable burden from the transmitter, which in the original VC, had to be designed such that successive transmitted blocks would be independent at the channel output. In the BDFE, subtracting the trailing ISI, removes this stringent constraint on the transmitter, thus enabling the use of much shorter block lengths. The reduction in block length is illustrated in Fig. 4.

Also, in [7], we will publish a brief analysis of computational requirements for the BDFE that show it requires less computation per unit of real time than conventional methods, and can also be pipelined easily, whereas conventional methods cannot.

CONCLUSIONS:

Vector Coding methods are beginning to prove themselves as practically feasible methods by which to optimize the performance of a wide class of communication channels. Our recent work has been to analyze the improvements, as well as to productively apply the technique to a particular application, the ISDN digital subscriber loop, where our methods (through Bellcore) are the leading candidates for

standardization. Continuing work focuses on a number of important and interesting problems in the design of signal constellations for VC, the capacity of distributed crosstalking communication networks, and VLSI realization of VC encoders and decoders at sampling rates of 400Khz and 800Khz.

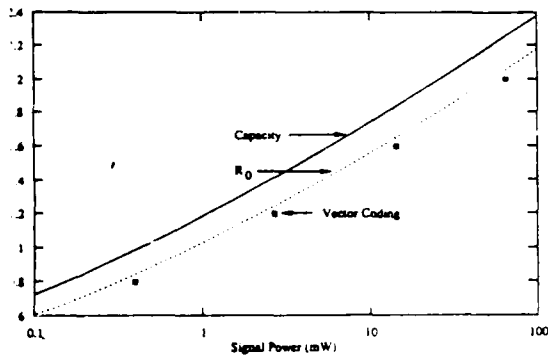


Figure 1a - R_0 for ISDN Subscriber Loop

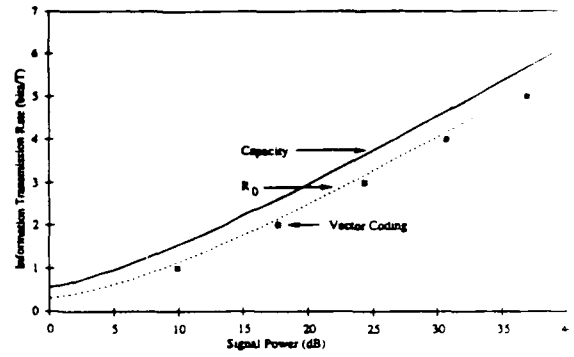


Figure 1b - R_0 for the 1-D channel

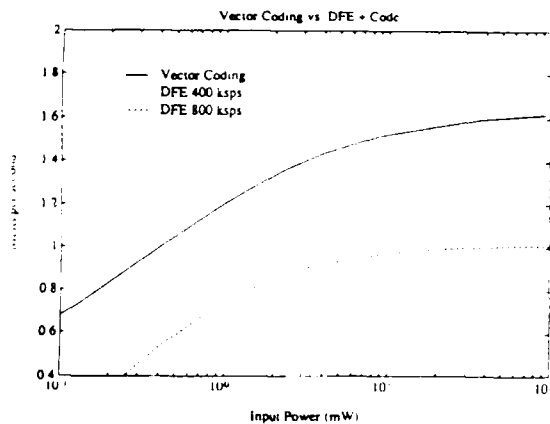


Figure 3 - Achievable Data Rate Comparison

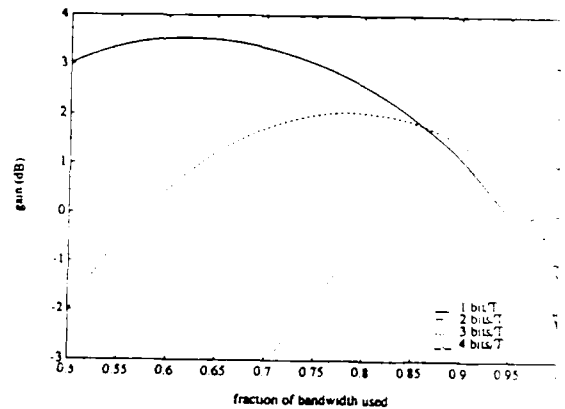


Figure 2 - Coding Gain vs. Fraction of 1/2

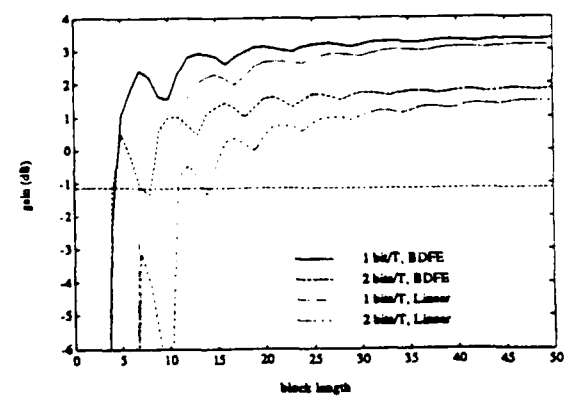


Figure 5 - Coding gain $:(1 - D)(1 + D)^2$

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Unit: 8

TITLE: Real Time Statistical Signal Processing

PRINCIPAL INVESTIGATOR: T. Kailath, J. M. Cioffi

VISITING PROFESSORS: V. U. Reddy and J. Chu

RESEARCH ASSOCIATE: R. Roy

GRADUATE STUDENTS: D. T. M. Slock

SCIENTIFIC OBJECTIVES:

The goals of this research program have been to study the direction-of-arrival (DOA) estimation and adaptive beamforming problems and in particular focus on innovative techniques that have computational and performance advantages over existing methods. Of special interest is the beamforming problem in the presence of "coherent" interference as can arise in "multipath" and "smart" jammer environments. Two signals are said to be coherent (or fully correlated) if one is a scaled and time-shifted version of the other. Another area of interest is to develop numerically robust fast algorithms for Recursive Least-Square adaptive filtering.

SUMMARY OF RESEARCH:

The list of publications gives a general idea of our research effort over the last reporting period. We will highlight a few key contributions below.

A. Spatial Smoothing to Combat Signal Coherency

The first step in high resolution "eigenstructure" or "subspace" techniques for DOA estimation and beamforming is to estimate the array covariance matrix from the array data, and then to determine the number of sources from the multiplicity of the minimum eigenvalue of the covariance matrix. With the number of sources known, signal and noise subspaces are estimated from the eigenvectors of the covariance matrix

and then the DOAs are determined by the intersections of the array manifold with the (estimated) signal subspace. However, in the presence of two or more coherent sources, this approach fails because of the collapse of the dimensionality of the signal subspace due to the full correlation between the sources. In previous reports, we have proposed a spatial smoothing (or subarray averaging) technique to restore the dimensionality of the signal subspace.

More recently, new insights in and refinements of this technique have been obtained. In [3], the question of testing the array covariance matrix to verify solvability has been addressed, as also the issues of determining the number of sources, intersource correlations, etc. A new concept was introduced, called the *smoothed rank profile* (SRP) defined as the rank profile of a telescoping series of matrices obtained by averaging smaller and smaller principal diagonal blocks of the original matrix. The SRP can be used to determine the *source coherency structure* in the presence of coherent signals. In the practical situation of limited observations, an information-theoretic criterion is proposed to determine the signal subspace dimensions.

Signal cancellation and interference rejection effects of the optimum beamformer in the presence of partially and fully correlated interfering sources are studied in [2]. Expressions are derived for the output power and the gain in the interference direction of the beamformer in terms of the source powers, correlation, and the sensor noise power. The penalties arising from increasing correlation in several scenarios are demonstrated quantitatively. Next, spatial smoothing is shown to progressively decorrelate the sources at a rate that depends on the spacing and directions of the sources. In this way, the degree of smoothing has been related to the improvement in signal cancellation and interference rejection behavior provided by spatial smoothing.

B. Optimum Beamforming for Coherent Signals

The performance deterioration of the optimum (Capon) beamformer in the presence of correlated interference arises because the minimization criterion employed in these beamformers uses the total array covariance matrix without explicitly accounting for the underlying signal model. Instead, the criterion should employ the signal-free covariance matrix in determining the optimum weight vector. Using this approach, two

different versions of an optimum linear beamformer were recently proposed (see [6]) that completely eliminate the signal cancellation phenomenon. Furthermore, in certain situations such as multipath propagation, the interferences are the signals arriving from different specular paths; rather than being cancelled they should be properly combined with the signal arriving via the direct path. In [6], a beamforming method is suggested where the desired signal and the interferences correlated with it are combined to yield maximum SINR (signal-to-interference-plus-noise ratio) at the output.

C. Abstract of Ph.D. Thesis

Richard Roy has completed his Ph.D. dissertation during this period entitled "ESPRIT-Estimation of Signal Parameters via Rotational Invariance Techniques." ESPRIT, a novel approach to the general problem of signal parameter estimation, has been introduced in a previous report. The abstract of the thesis follows.

High-resolution signal parameters estimation is a problem of significance in many signal processing applications, including *direction-of-arrival* estimation and time series analysis, where accurate parameter estimates are desired from observations of a sum of narrowband waveforms. This class high-resolution parameter estimation problems has come to be known as *high-resolution spectral analysis* since the introduction of the maximum entropy (MEM) method by Burg in 1967, and the *maximum-likelihood* (ML) method by Capon in 1969. These and other methods such as AR prediction techniques all claim to provide increased resolution and accuracy over their predecessors, but all suffer from *model mismatch*.

The development of the MUSIC algorithm by Schmidt in 1977 represented a significant breakthrough in that the underlying data model was correctly exploited in the geometric approach employed. The algorithm, which can be viewed as a generalization of the work of Prony (1795) and Pisarenko, reduced the highly nonlinear problem of multiple source parameter estimation using data received by an arbitrary sensor array to the problem of finding intersections between observed *signal subspaces* and known *array manifolds*. Through asymptotically unbiased and efficient, MUSIC has not been widely applied due to the significant computational burden and storage requirements that it imposes in many applications.

A new subspace approach (ESPRIT) to the estimation of parameters of signals observed in additive noise that mitigates these problems is described. ESPRIT exploits an underlying *rotational invariance* among signal subspaces induced by an array of sensors manifesting a particular invariance structure. The technique is most easily described in the context of direction-of-arrival estimation where the required array *invariance* structure takes the form of pairwise matched and aligned antenna element doublets. The new approach has several remarkable advantages over earlier techniques such as MUSIC, including elimination of massive data storage requirements, significant reductions in computational complexity, and decreased sensitivity to sensor array imperfections. Results of simulations indicate ESPRIT also yields finite-sample unbiased and asymptotically efficient parameter estimates. The performance of ESPRIT relative to that of the conventional MUSIC algorithm, the now popular root-MUSIC algorithm (applicable to the case of uniform linear arrays of omni-directional sensors), and a recently developed *multi-dimensional* MUSIC algorithm are presented.

D. RLS Adaptive Filtering

Research in the area of fast algorithms as applied to adaptive signal processing has continued during the last reporting period. Considerable breakthroughs have recently been achieved in the numerical stabilization of the family of fast recursive least-squares transversal filter (FTF) algorithms. These results have been presented at ICASSP 88. For a variety of reasons, the FTF algorithms are the preferable choice in the family of adaptive algorithms for signal processing, communications and control. However, numerical considerations (arising in practical implementations) have been disturbing this picture for a long time. FTF algorithms have been known to diverge in the presence of round-off errors. By introducing some redundancy in the FTF algorithms, an error-feedback mechanism can be implemented that effectively stabilizes the dynamics of the error propagation mechanism. These seemingly minor modifications have proved to yield a practical solution to the important problem of filter stability in real-world applications.

The technical details in the analysis of the conventional algorithms and the newly proposed solution have now been worked out fairly extensively. A journal paper has been submitted for publication based on this work.

Although a basic solution has been established, several finer details have arisen in the study of this problem and these are currently under ongoing investigation. It turns out that in practical implementations the problem to be solved can be extremely ill-conditioned or even ill-posed. Though this issue creates a problem for all existing adaptive algorithms, it is imperative to handle this complication in the context of the proposed stable FTF algorithms so as to allow for their widespread utilization. Current research is converging towards a solution that involves regularization of the problem to be solved. Also the use of adaptive control and the effect of normalization on the numerical behavior of the FTF algorithm are currently being investigated.

Many models in such diverse applications as system identification, adaptive control and decision-feedback equalizers for communications to name a few, involve multiple FIR filters and require the multichannel formulation of the FTF algorithm. These multichannel algorithms give rise to new aspects in the consideration of numerical properties, conditioning of the problem, multiprocessor implementations, etc. The implementation of the multichannel FTF algorithm on a modular architecture, corresponding to sequential updating for the contributions of the different channels, is being considered and the associated numerical issues will be investigated.

E. Summary of Results

- A formula for the minimum number of subarrays in spatial smoothing required to restore the dimensionality of the signal subspace.
- A detailed performance analysis of the (Capon) optimum beamformer in the presence of correlated sources and its behavior under spatial smoothing.
- Two new optimum beamforming techniques for coherent signal and interferences.
- A numerically stabilized version of the FTF algorithm for fast Recursive Least-Squares estimation in time series.

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Journal Papers

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JSEP SUPPORTED PH.D DISSERTATION

R. Roy, "ESPRIT - Estimation of Signal Parameters via Rotational Invariance Techniques," August 1987.