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DOPPLER TARGET SIGNAL GENERATOR

by

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ABSTRACT

The Threat Radar Simulator (TRS), utilized in DREO's ECM facility, is equipped with a Moving Target Indicator (MTI) processor used to detect the skin echo of moving targets. The MTI unit makes use of a doppler shift, associated with the moving target, to discriminate between the target and unwanted clutter. To facilitate the MTI's requirement for doppler shifts in the return pulses, a Doppler Target Signal Generator (DTSG) has been developed at DREO. The DTSG is an X-band programmable frequency synthesizer with three independent outputs. Two of the outputs are used in the generation of target returns and the third output provides a doppler shift to the clutter return signal.

RESUME

Le simulateur de menace radar utilisé dans le système de contremesures électroniques du CRDO comprend un indicateur de cibles mobiles pour la détection d'échos d'objets en mouvements. L'indicateur de cibles mobiles utilise l'effet Doppler des échos pour séparer les réflexions utiles des autres. Un générateur d'échos Doppler pour signaux a été développé au CRDO afin de produire des déplacements Doppler d'échos pour les besoins de l'indicateur de cibles mobiles. Le générateur d'échos Doppler est constitué d'un synthétiseur de fréquences opérant dans la bande X et produisant 3 sorties indépendantes. Deux des sorties sont utilisés pour la génération d'echos de cibles et la troisi me produit le déplacement Doppler de l'echo d'interference.

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1.0 INTRODUCTION

The Electronic Wafare Engagement Simulation Facility (EWESF) at DREO is comprised of an RF anechoic chamber, a Threat Radar Simulator (TRS), a Target/Jammer/Clutter (TJC) signal generator and an ECM Simulator computer. The inter modular connections are illustrated in Figure 1-1. Target return and jamming signals are generated from the TJC signal generator and transmitted through a dipole antenna array network located at one end of the chamber. The radiated signals are received at the opposite end by the radar's antenna, which processes the signals to produce range tracking, antenna steering, and display information. The TRS system is a noncoherent 2 channel monopulse radar equipped with various signal processing modules including a Moving Target Indicator (MTI). The MTI is a noise suppressing device used to help the radar distinguish moving targets from unwanted stationary objects or clutter. The MTI circuit consists of a digital high pass filter designed to accept doppler frequency shifts associated with moving targets and reject low or no doppler frequency shifts produced by clutter.

To facilitate the MTI's requirement for a doppler shifted signal, a Doppler Target Signal Generator (DTSG) was developed and implemented into the EWESF. The DTSG is a programmable frequency synthesizer with three independent outputs, two of which provide doppler shifts to individual target return signals and one which provides a doppler shift to the clutter signal. The DTSG obtains and processes, from the ECM simulator computer, the instantaneous velocity of a target relative to the radar's platform, to calculate the appropriate doppler frequency. The DTSG can produce positive and negative doppler frequency shifts to represent a target travelling towards or away from the radar respectively.

In addition to a doppler shift, the DTSG can produce frequency sidebands to simulate the complete spectral profile of a complex target. This feature is presently not required since the non-coherent MTI processor in the radar is insensitive to such narrow sidebands. This feature however will accommodate a coherent pulse doppler radar which makes full use of the target's doppler sidebands to discriminate against clutter returns.

The next section includes a theoretical discussion of the doppler frequency phenomenon. Mathematical equations which describe the doppler effect are brought to light to serve as the basis for the design of the DTSG. Also, a description of the EWESF's Target Signal Generator is provided with emphasis given on the DTSG's implementation. Finally, sections 3 and 4 provide an overview of the RF and digital designs of the DTSG respectively.

2.0 DESIGN CONSIDERATIONS FOR THE DTSG

2.1 Theory of Doppler Frequency

Targets are generally much larger than the carrier wavelength of the radar pulse and are usually of irregular shape. This combination causes the phase and amplitude of the echo to be a sensitive function of the carrier frequency and target orientation with respect to the radar boresight axis. Consequently, the phase and amplitude of the echo from a moving target are random processes in time. A brief discussion on these processes for the pulse radar, with and without frequency agility, is given. This provides the background for describing the hardware implementation of the Doppler Target Signal Generator (DTSG).

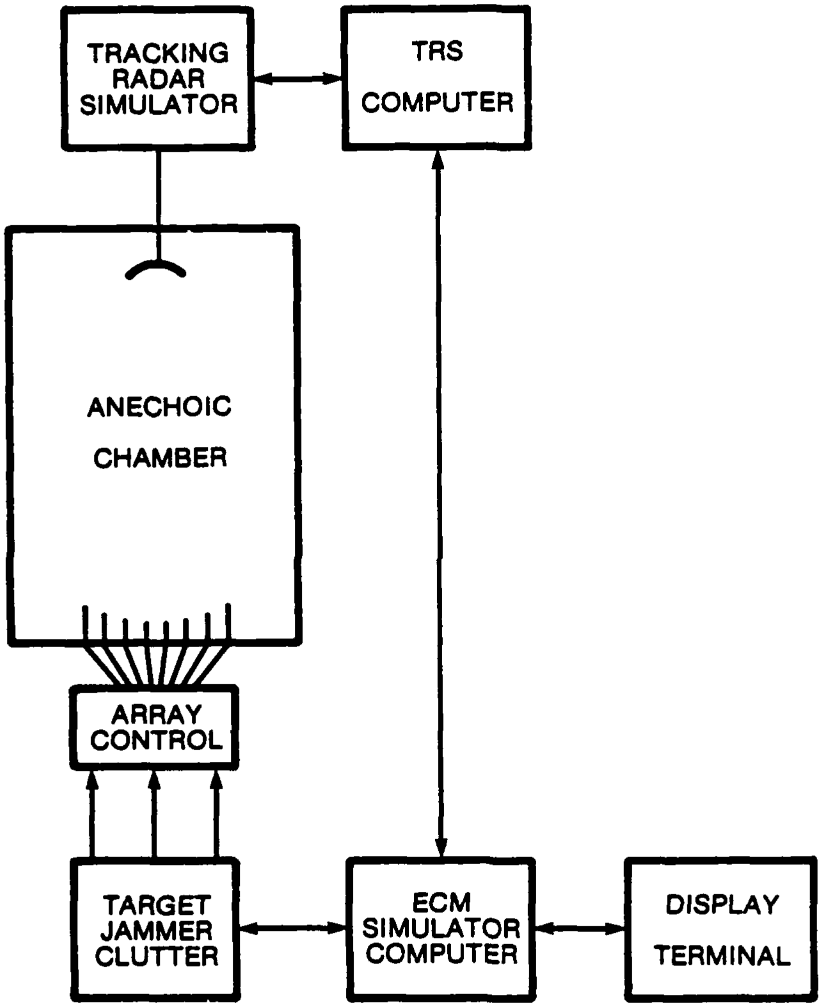


FIG. 1-1. Block Diagram of the Electronic Warfare Engagement Simulation Facility

The phase front of a point source excited by a CW radar is shown in Figure 2-1. The total angular displacement of the electromagnetic wave to and from the target is given by:

$$\Phi = \frac{4\pi r}{\lambda} \tag{2-1}$$

where

λ = RF carrier wavelength
r = radial distance from point source target to phase contour.

For a fixed distance r, the phase contours are concentric circles, exhibiting no amplitude fluctuation (scintillation) or angle variation (glint) for any radar viewing angle Θ. Thus the only requirement for simulating this target (assuming that it is in motion) is the doppler frequency which can be expressed as:

$$f_d = \frac{1}{2\pi} \frac{d\Phi}{dt} \tag{2-2}$$

From Eq. 2-1 and Eq. 2-2

$$f_d = \frac{4\pi}{2\pi\lambda} \frac{d\bar{R}}{dt} = \frac{2}{\lambda} \bar{v} \cos \Theta \tag{2-3}$$

where

$\bar{R}$ = position vector between the radar and point source
$\bar{v}$ = target velocity
Θ = angle between $\bar{R}$ and direction of target propagation (see Figure 2-1)

Modelling of real targets is complicated by the fact that they exhibit scintillation and glint, with changing aspect angle, resulting from the irregular shape of the target. The phenomenon of scintillation can be explained by considering a target modelled by two point sources. Figure 2-2 outlines the phase contours of such a target. The wrinkles on the contours are due to the interference of the two sources. Figure 2-3 illustrates the incidence of distorted phase contour on the radar antenna. The power flow or Poynting vector is always perpendicular to the phase front as indicated [1]. The tracking radar will align its boresight axis so that it is colinear with the Poynting vector resulting in a tracking angle error (Θ). Since the phase contours fluctuate with time due to the motion of the target, the tracking angle error will vary. This is denoted as the angle fluctuation or glint.

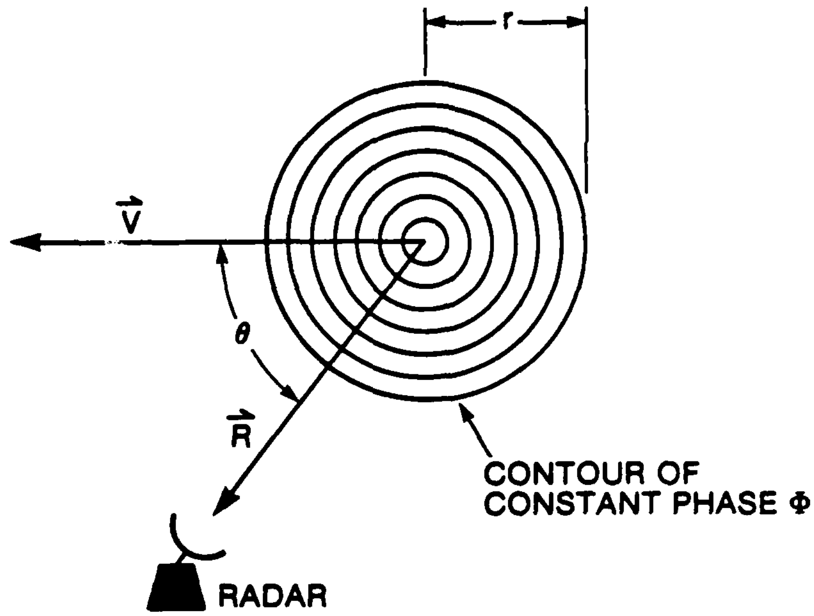


FIG. 2-1. Phase Front Radiating From a Point Source

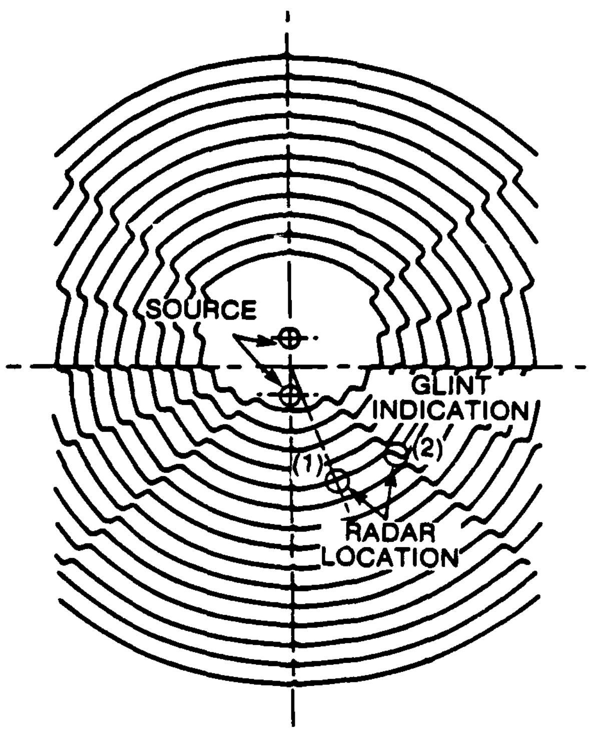


FIG. 2-2. Phase Front Radiated From a Two-Element Target

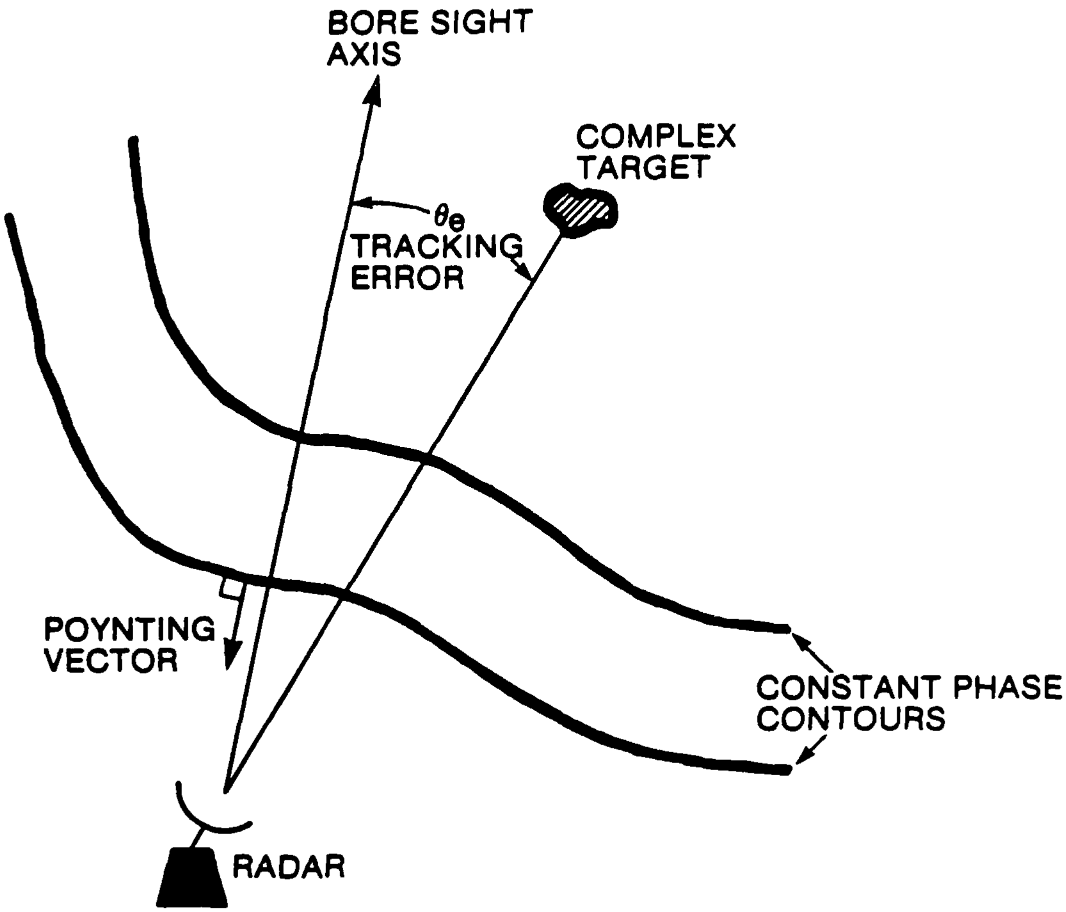


FIG. 2-3. Illustration of Angle Scintillation

Amplitude fluctuation is caused by the changing vector sum of the amplitudes of the two point sources as the target moves. There is an inverse relationship between the angle and amplitude perturbations, ie, large magnitudes of glint tend to occur in regions of small echo amplitude [2] (regions of destructive interference between point sources). For the fixed frequency pulse radar, amplitude scintillation is generally of little concern since it is suppressed by the AGC circuitry (provided the AGC bandwidth is sufficiently large).

Finally, considering the doppler frequency fluctuation, Eq. 2-2 can be rewritten to yield the expected value of the doppler frequency.

$$\langle f_d \rangle = \left\langle \frac{\Phi}{2\pi} \right\rangle \tag{2-4}$$

The probability density function, $P(f_d)$, based on the assumption that the scintillation component is Gaussian distributed, is:

$$P(fd) = \frac{1}{2\pi\sigma_\psi\sigma_t} K_o \left[\frac{f_d - \langle f_d \rangle}{2\pi\sigma_\psi\sigma_t} \right] \tag{2-5}$$

where

K_o = modified Hankel function of x
σ_ψ = standard deviation of angle scintillation
σ_t = standard deviation of yaw rate

The doppler frequency probability function of a Boeing 707 jet aircraft at X band is plotted in Figure 2-4 [1].

The effect of glint is reduced on a radar which utilizes frequency agility. The frequency change on every PRI is made large enough so that the target return will become uncorrelated from one PRI to the next. Consequently, since the angle tracking servo loop response time is much longer than the PRI, the glint effects are effectively integrated out. Thus glint effects are generally not significant for the frequency agile radar. In the case of a frequency agile pulse radar, it is not possible to discriminate between targets by using doppler frequencies. Therefore, adding a doppler frequency to the target return in this case is not necessary.

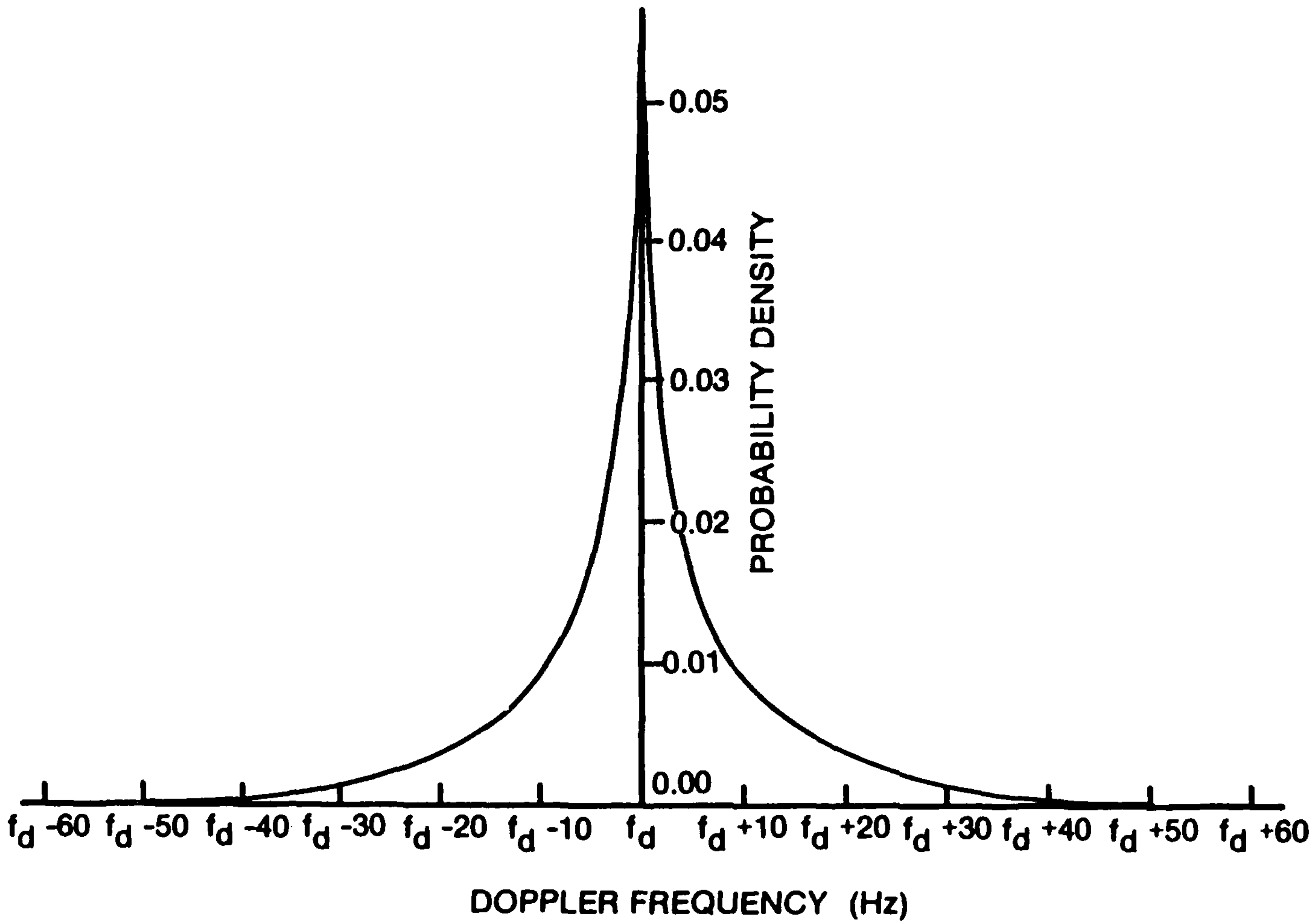


FIG. 2-4. Probability Density Distribution of a 707 Jet

In addition to the amplitude and angle fluctuations described above, there are also side bands produced by moving parts of the target such as the rotating propeller blades or turbines of an aircraft. Figs. 2-5 and 2-6 show a typical doppler spectrum of a propeller aircraft and jet aircraft respectively [3]. As shown, the side bands produced by the rotating parts of the aircraft have an RCS which is comparable to that of the fuselage. The Threat Radar Simulator (TRS) uses MTI filtering which is rather insensitive to side bands on the target doppler spectrum. Therefore it is not necessary to implement the circuitry which generates these side bands in the DTSG. However, should the TRS be modified to simulate a pulse doppler radar, which tracks the target's doppler component, then the doppler side bands must be included. This requires both phase and amplitude modulation of the DTSG output to produce the appropriate side band levels.

2.2 EWESF Target Signal Generator Implementation

In this section an outline of the basic implementation of the target signal generator used in the EW engagement simulation facility is given with emphasis on the DTSG.

A simplified block diagram of the target signal generator is shown in Figure 2-7. The box denoted as the scenario controller consists of a PDP 11/44 computer. The scenario controller defines the trajectory of the target and thus controls the parameters of the target echo. It uses the relative position, velocity, and acceleration parameters of the threat radar with respect to the target. The DTSG generates a CW microwave carrier signal with the required doppler shift as determined by the scenario controller. Phase noise is added to this signal to generate the phase scintillation and doppler side bands. The output CW signal from the DTSG is pulse modulated by the amplitude modulator shown. The modulating signal is determined from the displacement of the target to the threat radar and the envelope of the simulated target return pulse train. The resulting RF pulse is radiated by the antenna array which is controlled by the azimuth and elevation angles of the target generated by the scenario controller.

The scenario controller also generates parameters to produce glint and scintillation. Scintillation, which is dependent on the the radar's aspect viewing angle, is generated by randomly amplitude modulating the DTSG output. Glint, which is correlated with the scintillation, is produced by randomly changing the antenna element radiating the generated target signal in the antenna array. A complete description of the scenario controller and associated peripherals is contained in [4].

The DTSG consists of three channels and is shown, in simplified block diagram form, in Figure 2-8. Two channels are for target signal generation and

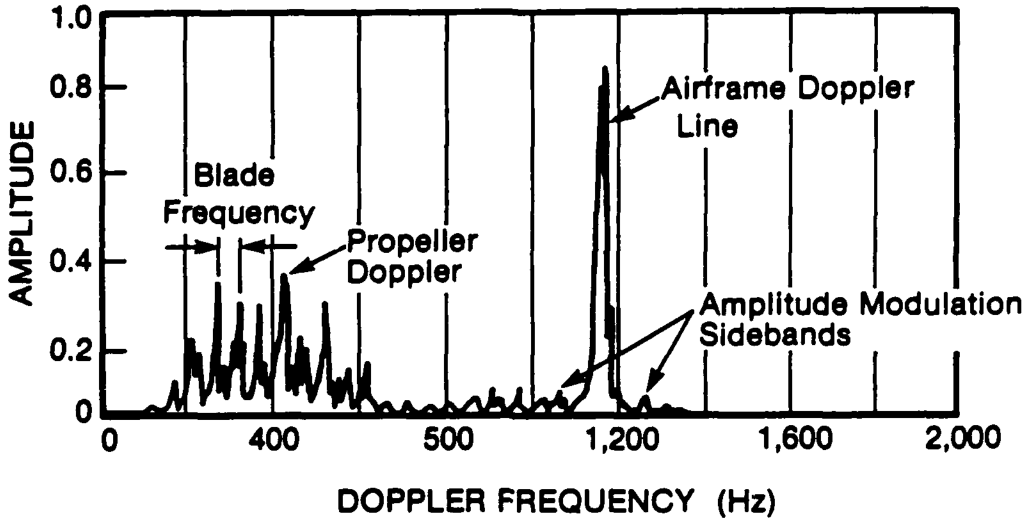


FIG. 2-5. Doppler Frequency Spectrum of a Propeller Driven Aircraft

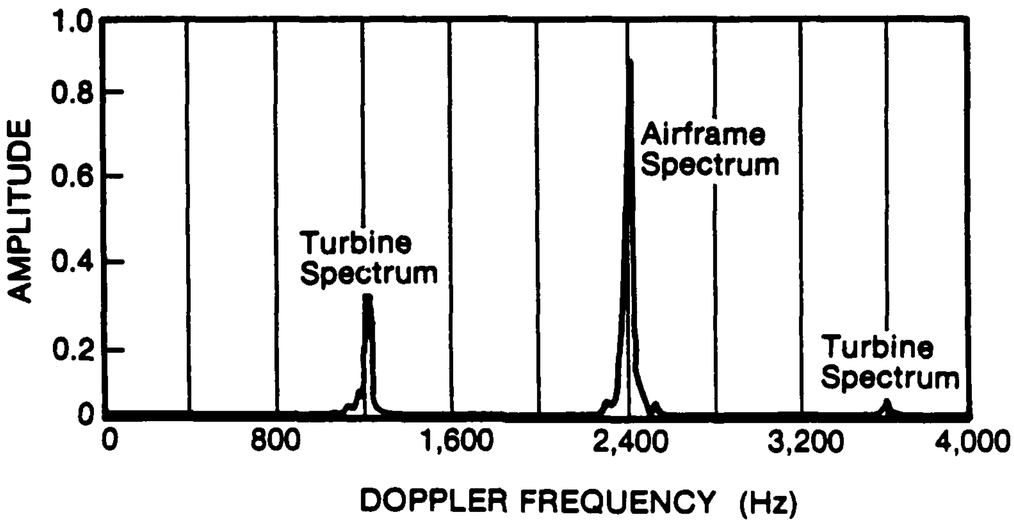


FIG. 2-6. Doppler Spectrum of an Approaching Single-Engine Turbojet Fighter Aircraft

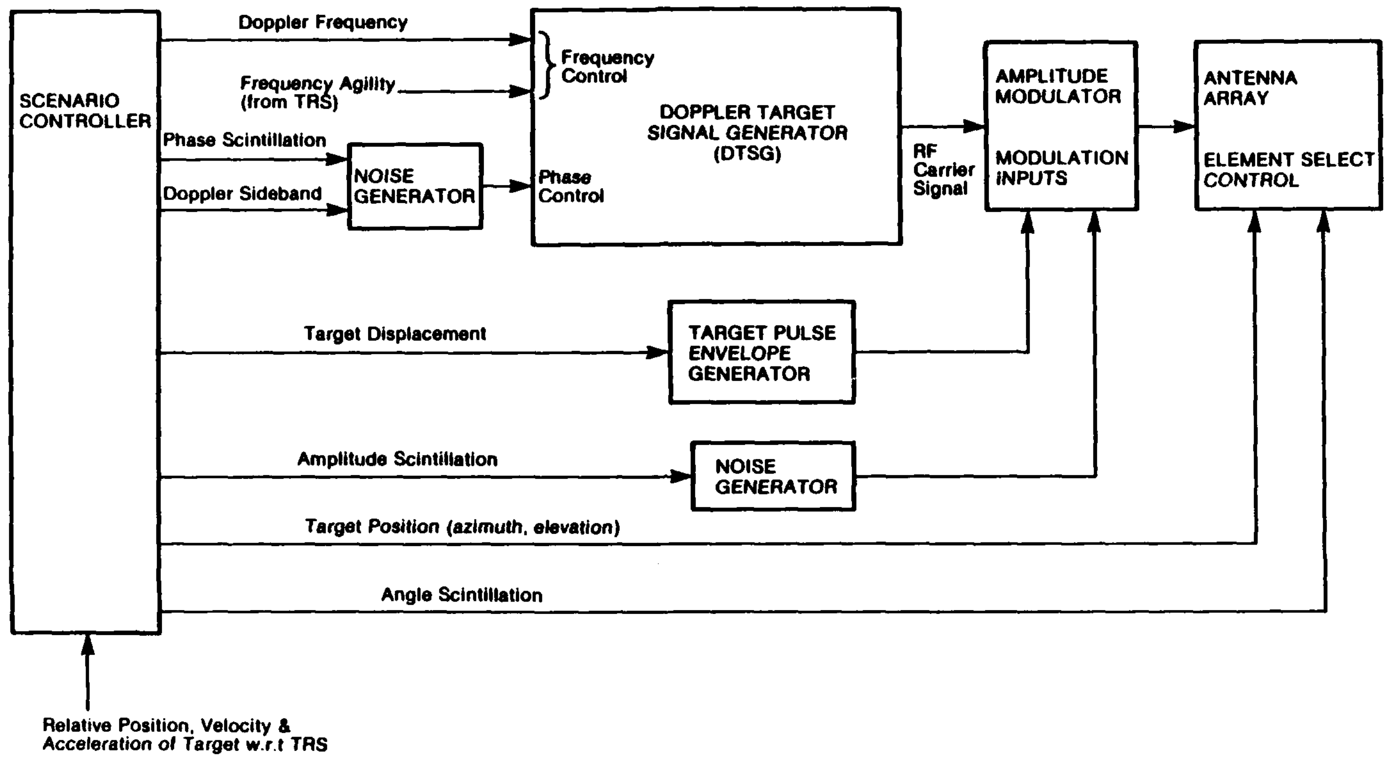


FIG. 2-7. Target Signal Generation

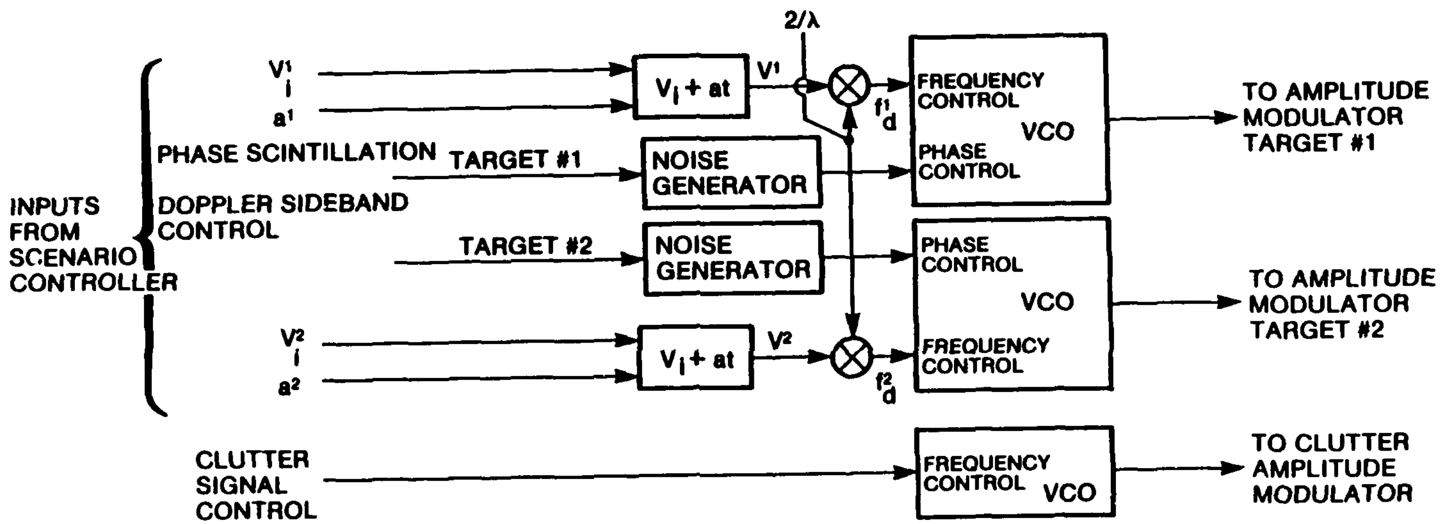


FIG. 2-8. Block Diagram of DTSG

the third channel is for adding a doppler shift to the clutter signal. For both target channels, the initial velocity (V_i) and acceleration (a) of the targets are downloaded into the DTSG. The DTSG computes the instantaneous velocity (v) by evaluating the expression:

$$v = V_i a t^2 \qquad (2\text{-}1)$$

where t is the time. The components V_i, v and a refer to the relative radial velocities and acceleration between the target and threat radar. The instantaneous velocity, v, is multiplied by $2/\lambda$, as given by equation 2-3, to obtain the doppler frequency f_d. Since the TRS has a frequency agile mode, the wavelength (λ) of the simulated radar carrier frequency is a function of time. The signals $f_d{}^1$ and $f_d{}^2$ control the frequency of two X band VCO's which feed into the amplitude modulators of Figure 2-7.

The glint signal from the scenario controller is fed to the noise generator which randomly modulates the phase of the VCO output as seen in Figure 2-8. To ensure that doppler shifts of a few kHz can be added to an X band carrier, an accurate control of the VCO output frequency is required. Figure 2-9 depicts a simplified block diagram of a circuit that achieves this control. A frequency synthesizer within the DTSG generates an X band carrier frequency at f_c. This signal is up converted to f_c + 60 MHz + f_d. The 60 MHz + f_d frequency originates from a VCXO which is tuned by an analog signal proportional to f_d. The up converted signal is AM modulated and then transmitted through an antenna array. The radiated signal is received by a radar antenna and down converted to 60 MHz + f_d, with the local oscillator set to a frequency of f_c. The two target signals and clutter signal are generated from a common local oscillator, thus preserving coherency throughout the system.

Single Side Band (SSB) modulators are inappropriate as up-converters because of the relatively broad bandwidth (400 MHz) of the TRS in frequency agile mode. Wideband SSB modulators do not have good suppression of unwanted side bands. When the local oscillator signal is mixed with the VCXO output at 60 MHz, side bands occur at multiples of 60 MHz above and below the local oscillator signal. This implies that the IF frequency in the TRS receiver is mapped with spurious components that cause distortion in the video signal and result in performance degradation of the TRS.

The performance inadequacy of the SSB technique was verified experimentally by measuring the level of the undesired sidebands of the Anaren model 90338-60SSB mixer. The RF carrier frequency was set for 9 GHz at 7 dBm and the 60 MHz modulating signal was set at 7.5 dBm. These power levels were adjusted for maximum suppression of the unwanted side bands. Figure 2-10 depicts the SSB spectrum for the upper and lower side band modulation case. As shown, the unwanted side bands are only 20 dB below the desired side band, which is unacceptable for radar simulation purposes.

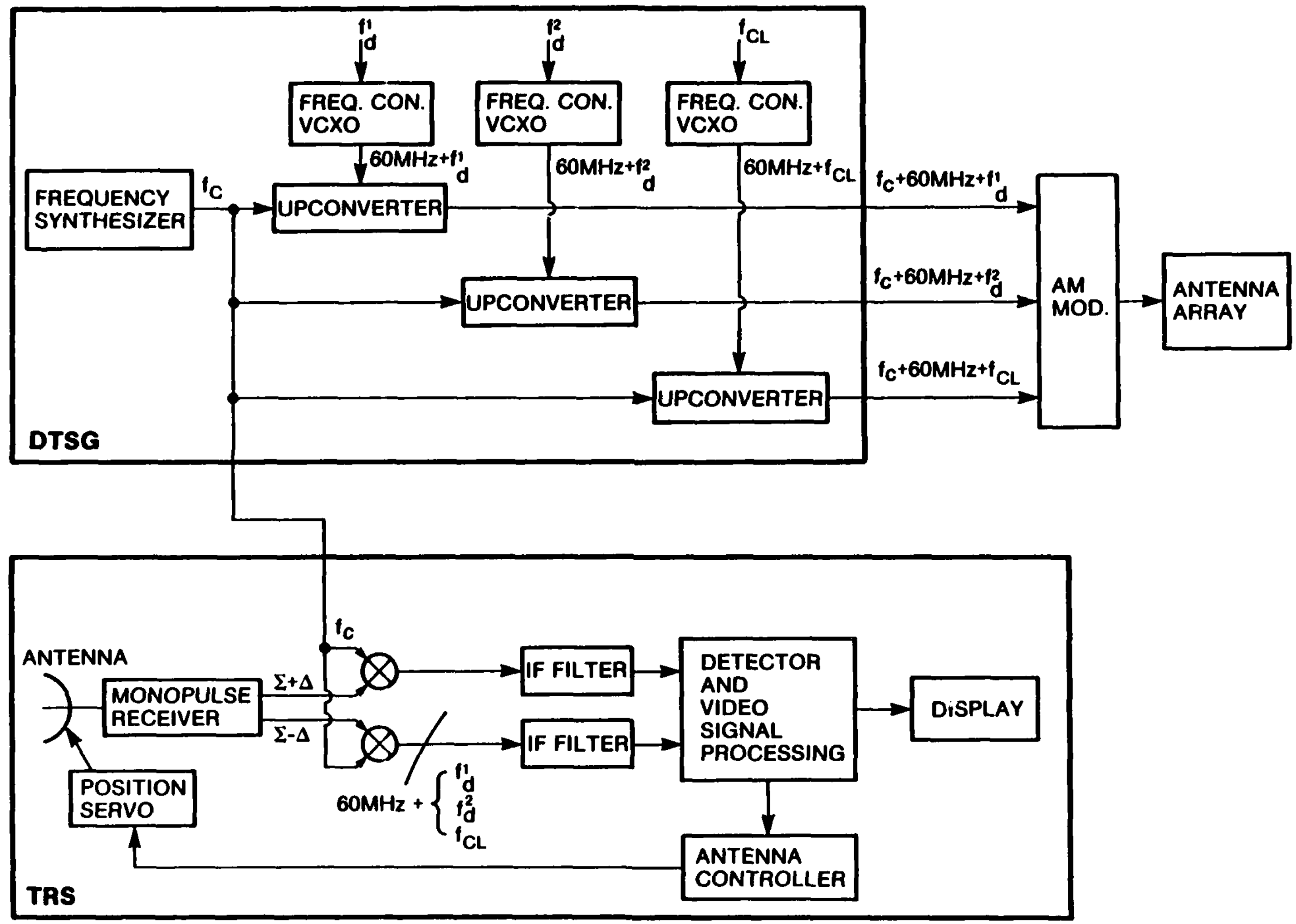
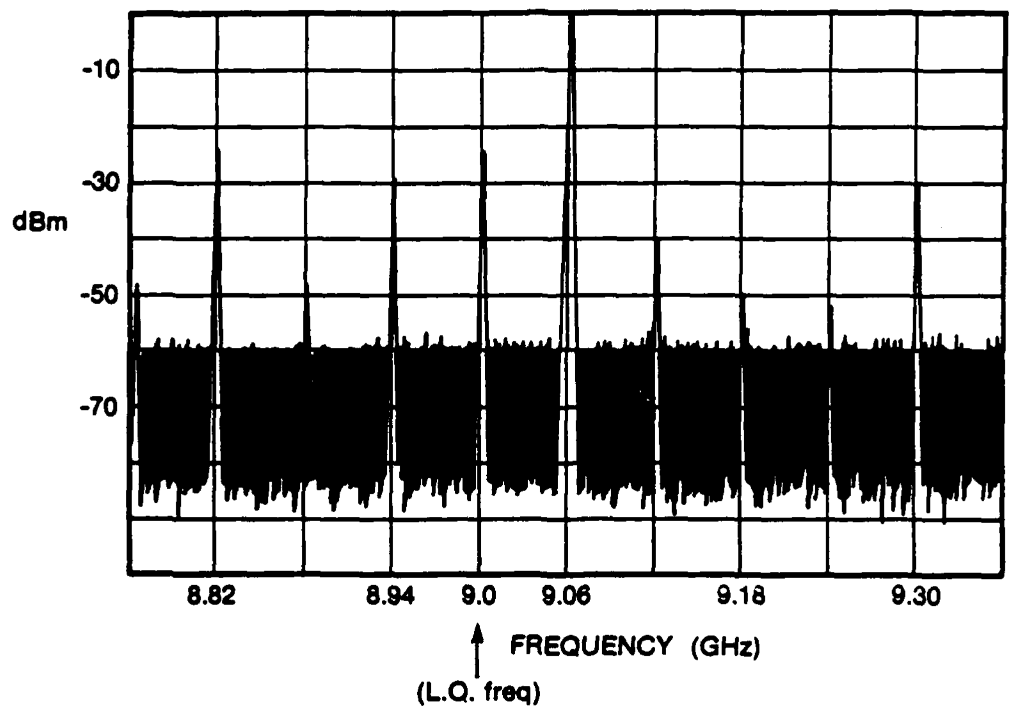
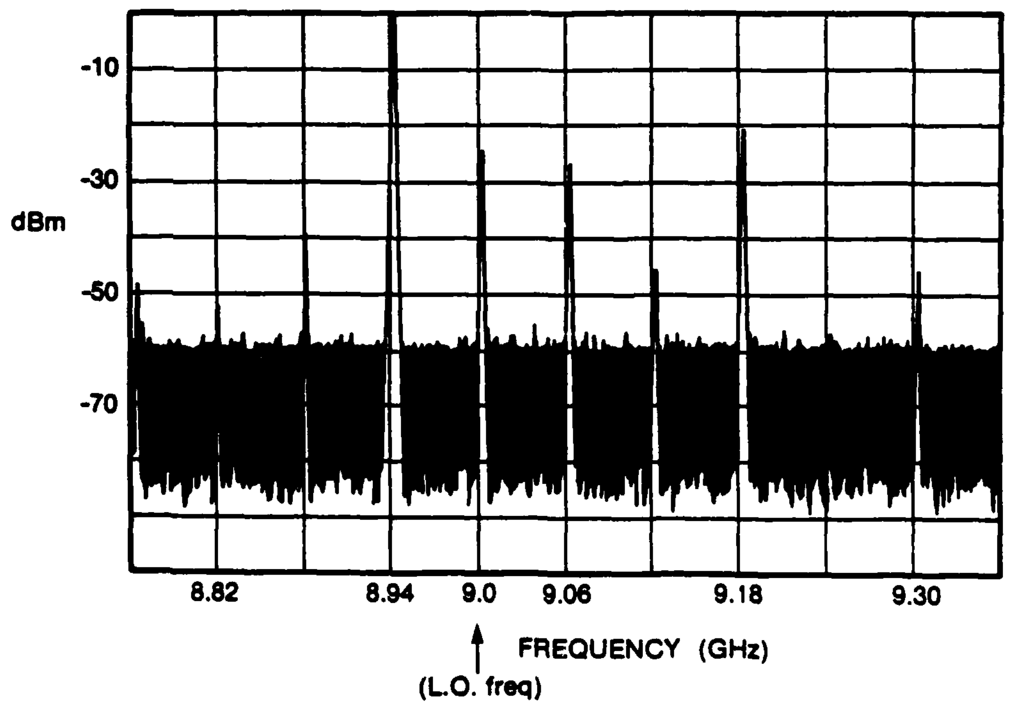


FIG. 2-9. Coherent Form of Target Signal Generation



(a)



(b)

FIG. 2-10. Output Spectra of SSB Modulator
a) UPPER SIDEBAND MODULATION
b) LOWER SIDEBAND MODULATION

To avoid problems with spurious side bands, the up-conversion stage was designed using a phase locked loop (PLL) approach. Figure 2-11 shows a block diagram of one of the three channels. A microwave VCO is phase locked to the sum frequency of a 5.6 GHz reference source and the VCXO output at 60 MHz + f_d. The resulting VCO output at 5.66 GHz + f_d is up-converted by a synthesizer, operating at 3.4 GHz + f_a, where f_a is the frequency agility component. The spurious components at the output of the VCO and synthesizer mixer are not mapped onto the 60 MHz IF, as was the problem with the SSB method. In the following section, details of the DTSG RF design are given.

3.0 DTSG RF Design

3.1 Introduction

The RF design of the DTSG is based on a phased lock loop (PLL) circuit which is shown in the block diagram of Figure 3-1. The PLL consists of a voltage control oscillator (VCO), a low pass loop filter, and two frequency mixers. The VCO output is down-converted to DC through mixers M1 and M2. The output of the second mixer, M2, is filtered and biased by the Loop filter which tunes the VCO to the required frequency of 5.66 GHz + f_d. This signal is up-converted by mixer M3 to produce the output signal of 9.06 GHz + f_a + f_d (where f_a is the frequency agility). The loop filter is described in further detail in section 3.2.

When the DTSG is not being utilized, i.e. prior to a trial run, the VCXO is stabilized to exactly 60 MHz by the *VCXO frequency stabilizer.* The stabilizer measures the voltage required to tune the VCXO to 60 MHz and uses it as an offset voltage for the VCXO during the trial run. Since trials last for no more than a few minutes, the frequency drift of the VCXO is negligible. The stabilizer is described in more detail in section 3.4.

The frequency counter, shown in Figure 3-1, provides immediate feedback for the operator calibrating the system. The circuitry is described in section 3.5.

3.2 Loop Filter Used in PLL

3.2.1 General

The system operates under two modes denoted as search and lock, which are briefly described below. A block diagram of the loop filter is shown in Figure 3-2.

Search Mode

The phase lock loops are unlocked when power is initially applied to the DTSG. To establish phase lock, the VCO frequency is scanned over a range of approximately 100 MHz. The scanned frequency range is adjusted so that the loop circuit locks onto the required upper side band of 5.6 GHz + 60 MHz + f_d (as opposed to the lower side band of 5.6 GHz - 60 MHz - f_d).

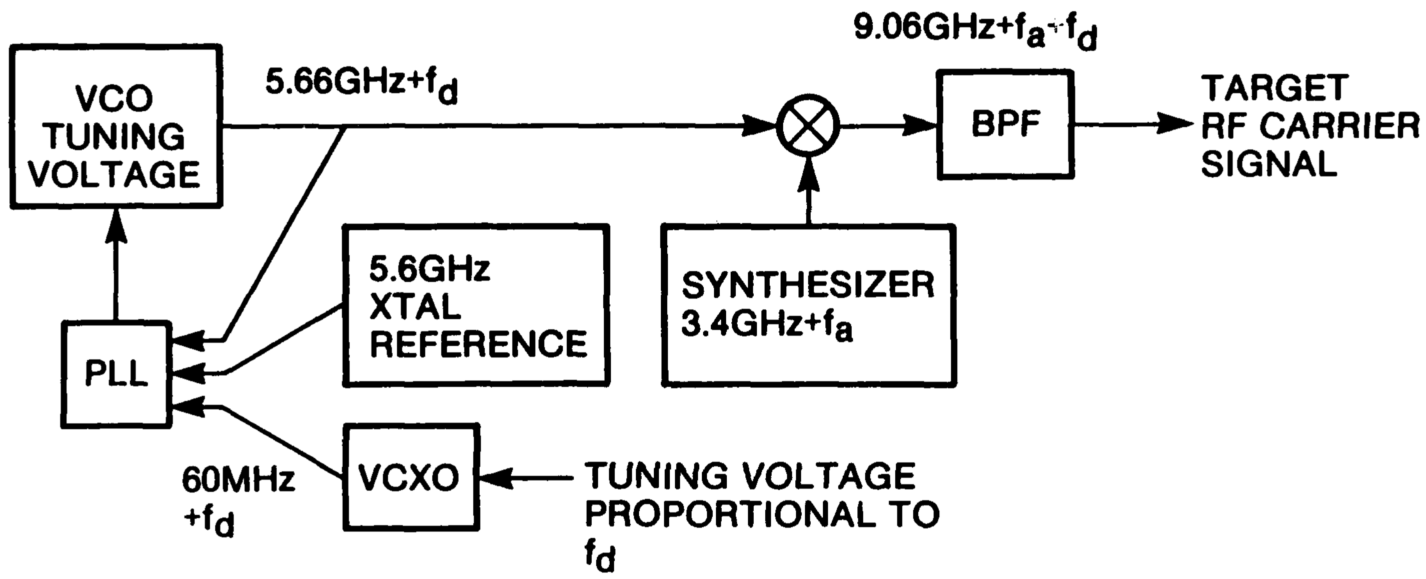


FIG. 2-11. Approach Using a Microwave PLL

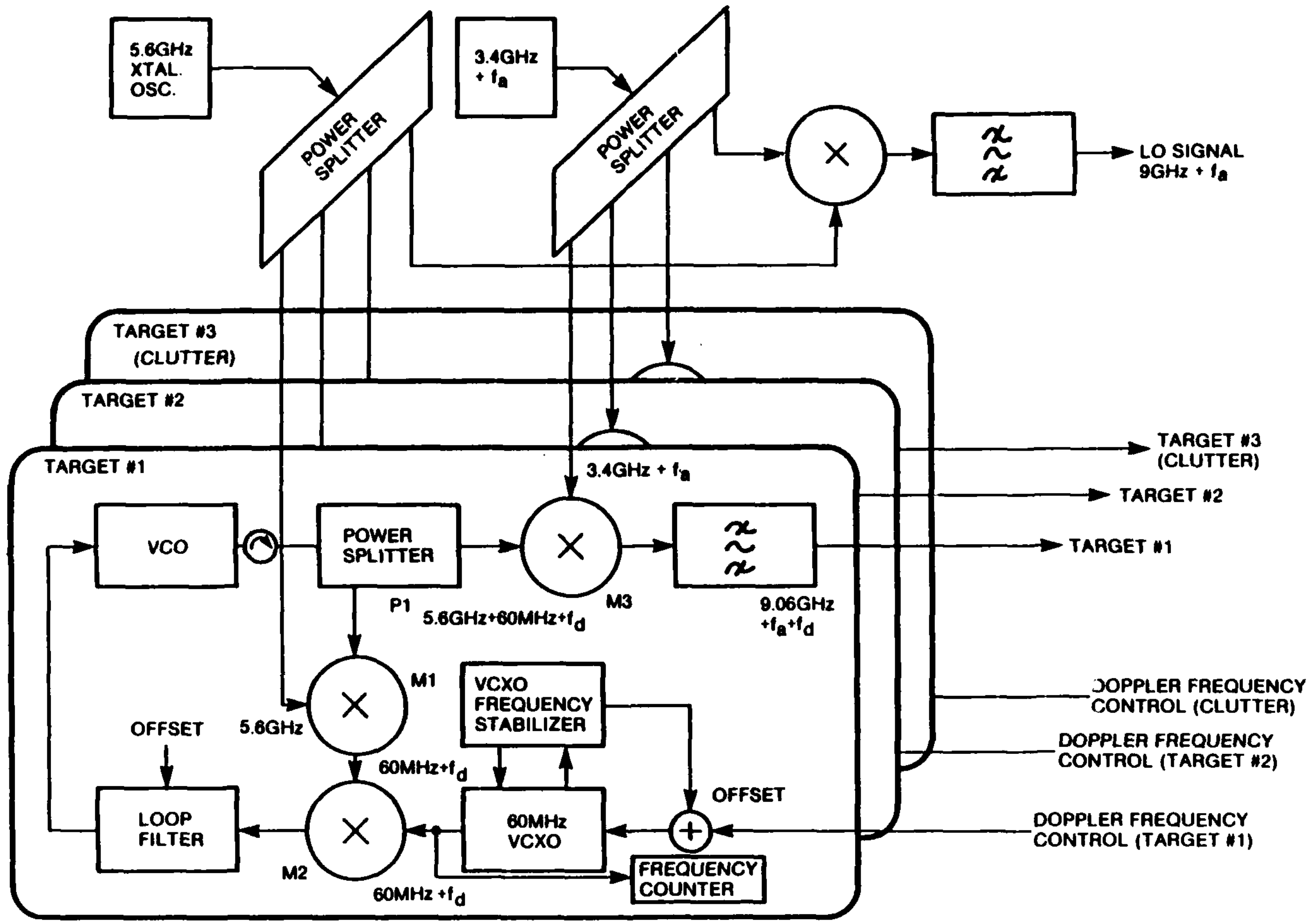


FIG. 3-1. RF Portion of Doppler Target Signal Generator

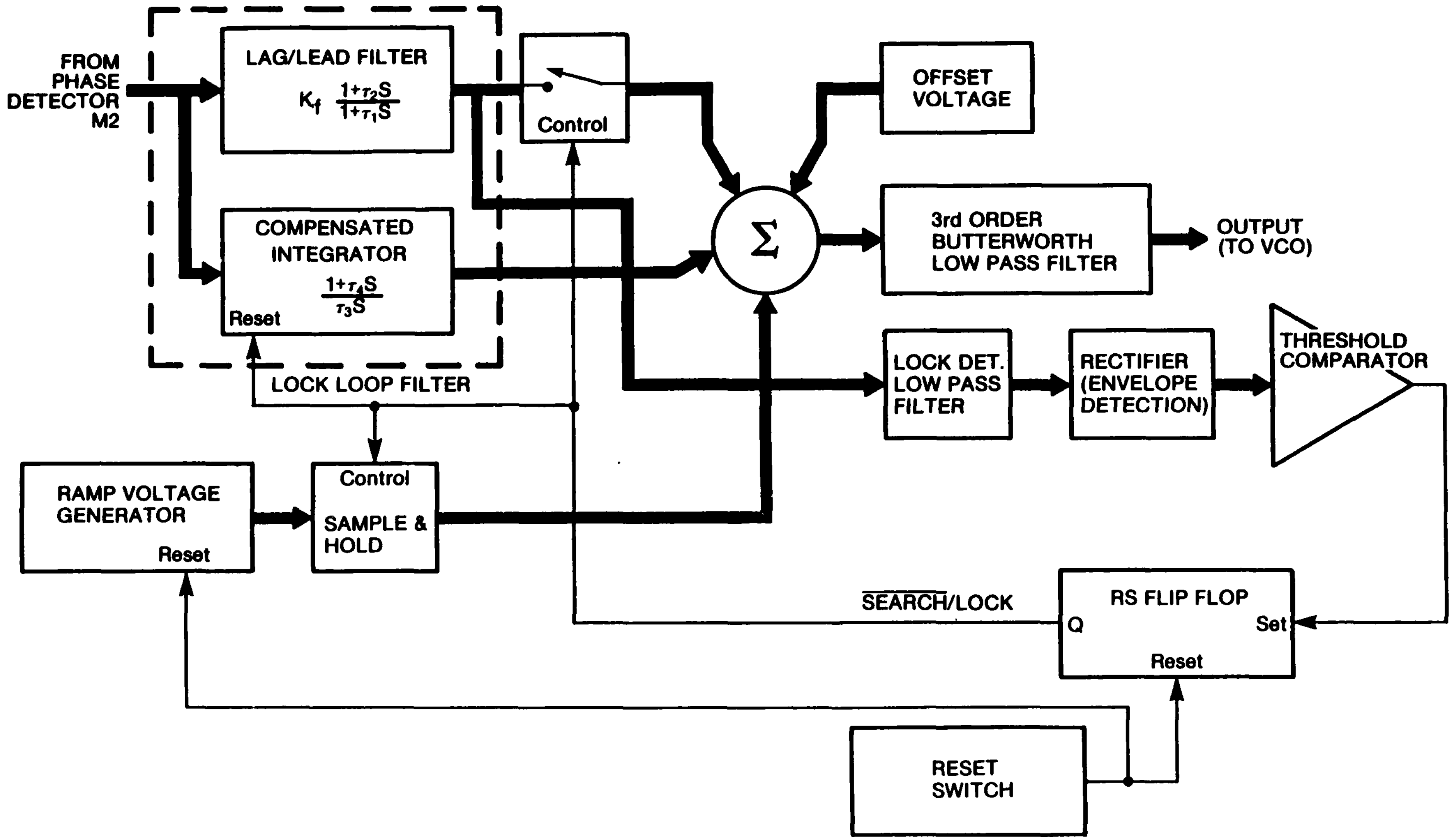


FIG. 3-2. Block Diagram of Loop Filter

Lock Mode

When the scanned frequency approaches the upper side band, the ramp signal is disabled and a loop filter is switched into the circuit which closes each PLL. The loop filter consists of a lag/lead filter with a 3 dB bandwidth of 100 Hz. The filter enables the PLL circuit to track the changes in the doppler frequency. This filter is in parallel with a compensated integrator filter which has a long time constant designed to compensate for drift in the VCO tuning voltage characteristics.

Detailed explanations of the hardware used to implement the two modes of operation are now given.

3.2.2 Search Mode

The circuit used to generate the search mode is illustrated in the block diagram of Figure 3-2. In search mode, the ramp signal from the ramp voltage generator is fed to the summer network via the sample and hold circuit. The remaining three inputs to the summer originate from the lock loop filter circuitry. The output of the summer drives the VCO frequency control through a 3rd order Butterworth low pass filter of 1 MHz bandwidth. It is inserted to reduce the high frequency noise and the 60 MHz spurious signals which leak through the lag/lead filter.

The ramp signal allows the VCO to be scanned over a frequency range of 100 MHz. An offset voltage is superimposed on this ramp voltage so that the center of the frequency scan is approximately 5.66 GHz.

When the VCO frequency is near 5.66 GHz + f_d, the frequency of the phase detector output will be within the passband of the lock detection low pass filter (see Figure 3-2). The envelope detection will then exceed a pre-determined threshold and set the RS flip flop, making the search/lock signal low. This signal causes the sample and hold circuit to hold the present value of the ramp signal which in turn will keep the tuning voltage of the VCO constant.

The time constant of the envelope detection circuit is about 10^{-3} sec and the bandwidth of the lock detection low pass filter is 100 kHz. Consequently, to ensure that the detection circuit will respond to the VCO as it scans through the frequency of 5.66 GHz, the scan time through a 200 kHz range (twice the filter bandwidth) should be sufficiently greater than 10^{-3} sec. A safe maximum scan rate chosen is 20 MHz/sec. The repetition period of the ramp signal is 5 seconds. Since the modulation sensitivity of the VCO is approximately 20 MHz/volt, the peak ramp signal is set at approximately 5 volts.

Figure 3-3 depicts the circuit used for lock detection in the PLL while Figure 3-4 illustrates the timing diagram for the lock up procedure. Listed below are the sequential steps of the lock up procedure.

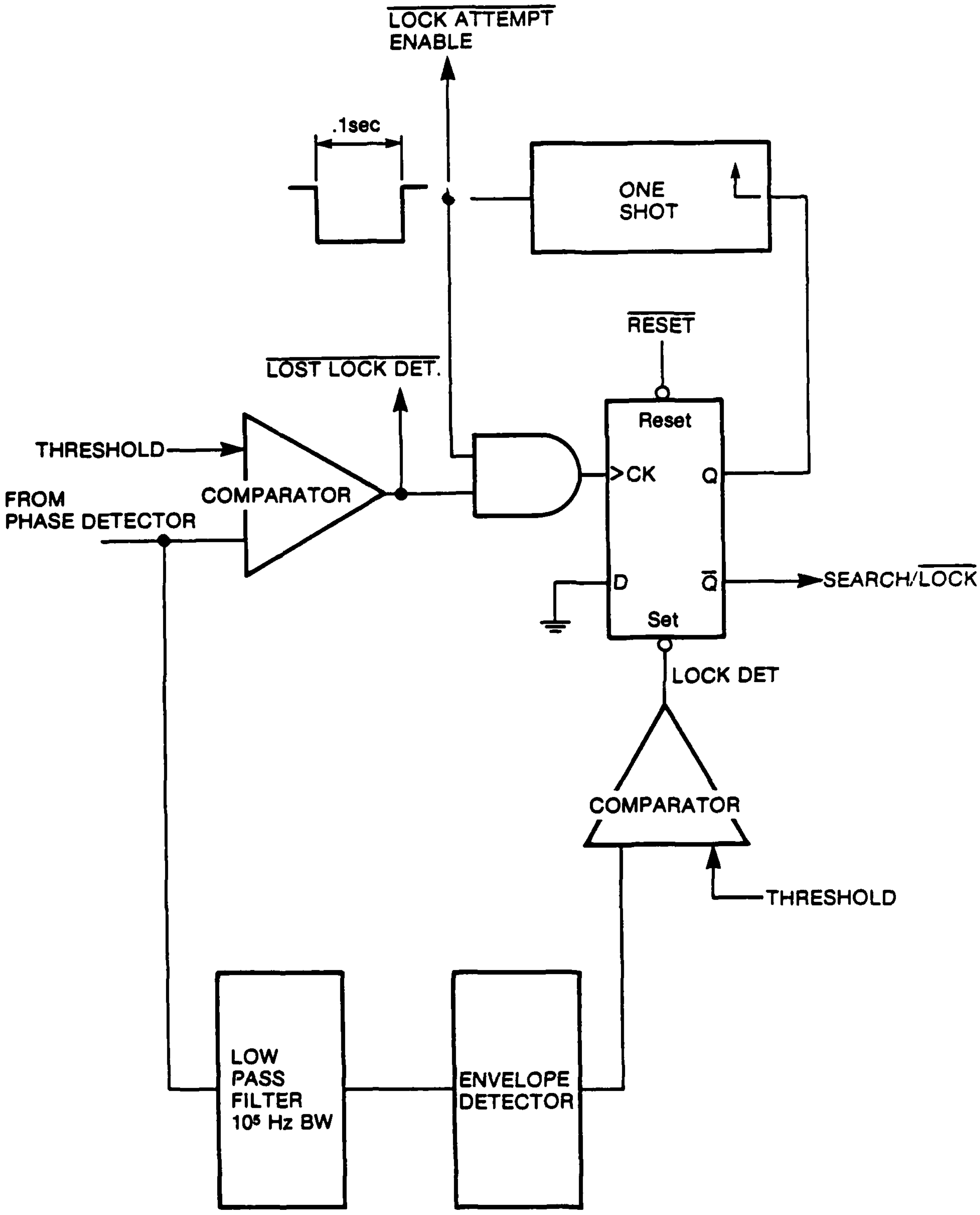


FIG. 3-3. Circuitry Used For Lock Detection

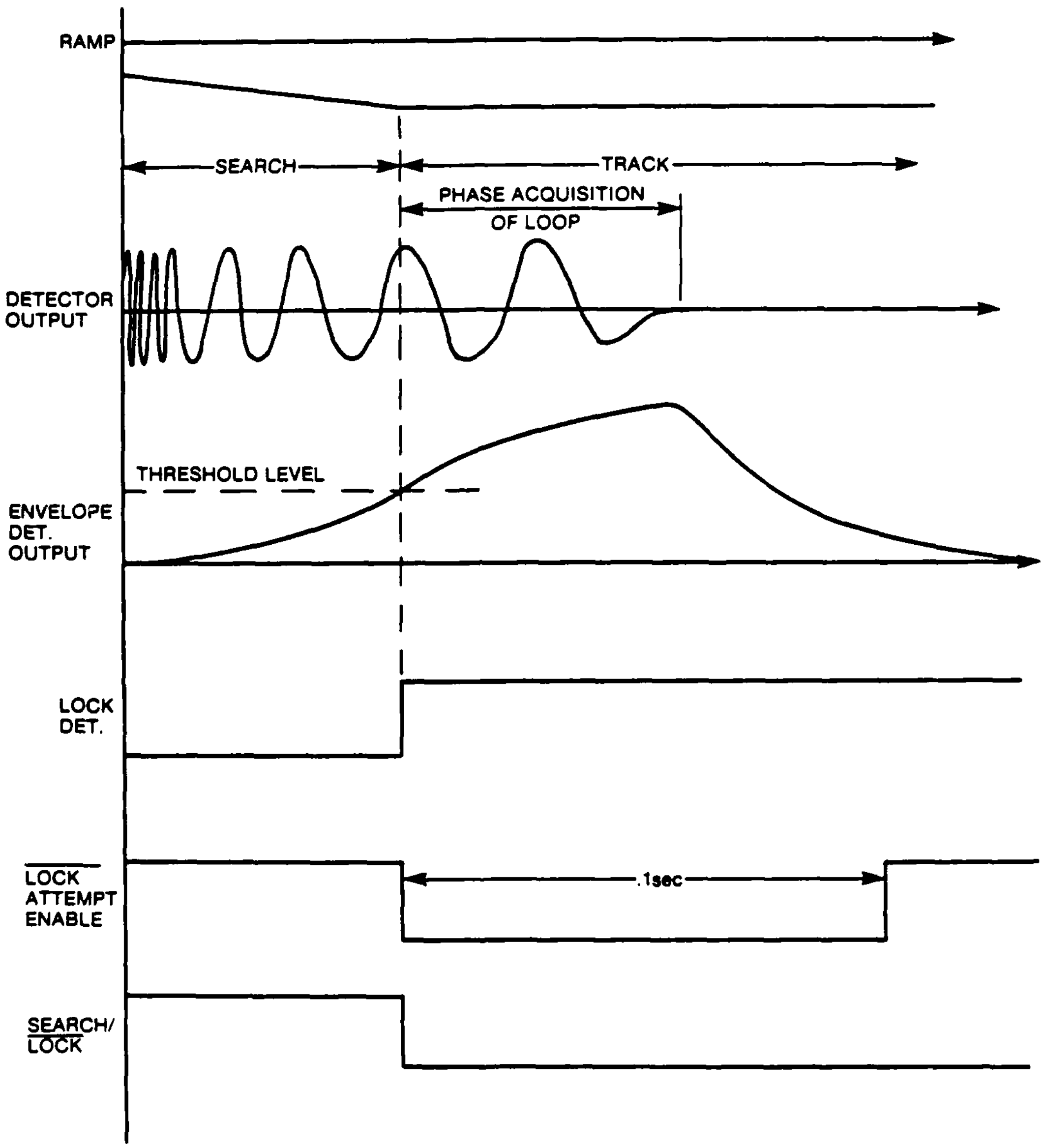


FIG. 3-4. Timing Diagram of Lock Up

1) Upon reset, the RAMP signal tunes the VCO toward the desired frequency of 5.66 GHz + f_d.

2) As the VCO frequency approaches 5.66 GHz + f_d, the frequency at the phase detector output decreases. When the VCO frequency is within 100 kHz of 5.66 GHz + f_d (i.e. within the bandwidth of the low pass filter), the envelope detector output begins to increase in amplitude.

3) The envelope detector output exceeds the threshold value when the VCO frequency is within a few tens of kHz from 5.66 GHz + f_d. At this time the LOCK DET signal goes high, causing the SEARCH/LOCK signal to go low.

4) Upon receiving a low SEARCH/LOCK signal, the sample and hold circuit samples the ramp voltage and holds it, keeping the VCO tuning voltage constant.

5) Finally, the Lock loop filter (see Figure 3-2) is switched into the circuit and the PLL locks up.

Should the attempt for lock up fail, the LOST LOCK DET signal will continue oscillating, thus resetting the search/lock flip flop. This will cause the search mode to be reactivated.

Since the PLL requires some time to lock up, the LOCK ATTEMPT ENABLE signal is activated for 0.1 second each time the PLL goes into Lock mode. This prevents the LOST LOCK DET signal from resetting the SEARCH/LOCK flip flop for 0.1 sec after the loop enters lock mode. Consequently the loop has 0.1 sec to attempt phase lock. If the lock up is successful then the LOST LOCK DET signal is not active.

The status of the SEARCH/LOCK signal is indicated by an LED on the front panel. It can also be read by the host computer through the computer interface. When the DTSG is powered up, the host computer strobes the RESET Line to initially start the loop filter in search mode.

3.2.3 Lock Mode

The lock mode is initiated when the SEARCH/LOCK signal goes low. As previously discussed, this engages the lock loop filter which closes the individual PLL circuits. As shown in Figure 3-2, the lock loop filter consists of a lag/lead network and an integrator with phase compensation.

The lag/lead filter has a 3 dB bandwidth of about 100 Hz. It is designed to respond to the required change in VCO frequency due to the changing doppler frequency. The frequency hold range provided by the lag/lead filter is approximately 4 MHz. Keeping the hold range small ensures that the VCO output has a high spectral purity and the PLL circuit maintains high stability. Difficulty arises in acquisition however if the hold range is made any smaller than 4 MHz*.

(*) Theoretically, the lower limit of the hold range is the doppler frequency range requirement of about 150 kHz.

Unfortunately, the tuning characteristics of the VCO are very sensitive to temperature fluctuations. For the models used in the DTSG, the deviation can be as high as 2 MHz/^{o}C. Since the frequency hold range of the lag/lead filter is only 4 MHz, a 2^{o}C change in temperature will cause the loop to lose lock. This drift is compensated by the compensated integrator circuit. The time constant of the compensated integrator is large enough so that it doesn't interfere with the operation of the lag/lead filter. The integrator network also compensates for the drop in the voltage of the holding capacitor used in the sample and hold circuitry (used to hold the ramp voltage on the search to lock transition).

As shown in Figure 3-2, the output of the loop filter passes through a 3rd order Butterworth low pass filter prior to entering the frequency control input of the 5.6 GHz VCO. The filter has a bandwidth of 2 MHz and is required to prevent the 60 MHz harmonic components, generated on the output of mixer M2 (see Figure 3-1), from propagating through the lock loop filter. Although the lock loop filter is essentially a low pass filter, it contains active components that have bandwidths of up to 60 MHz. Therefore, the extra low pass filter ensures that no spurious components (at 60 MHz multiples from the carrier) reach the VCO input. The frequency response of the filter is shown in Figure 3-5.

3.3 Performance of Microwave PLL

The spectrum of the VCO output, measured in the locked condition at 5.66 GHz with the VCXO adjusted to 60 MHz, is shown in Figure 3-6. Note that the spurious components, at multiples of 60 MHz from the carrier, are more than 50 dB below the carrier. This is a 30 dB improvement over the alternative method of SSB modulation that was discussed earlier. The spurious side bands are not produced by the VCO but by mixer M1 of Figure 3-1. To overcome this problem, an isolator was placed between the power splitter P1 and mixer M1.

As mentioned earlier, the 5.66 GHz signal is mixed with a 3.4 GHz source to produce a target output signal of 9.06 GHz. Over a frequency span of 50 MHz, the DTSG output, shown in Figure 3.7(a), contains spurious noise that is 50 dB below the main carrier. To measure this performance in terms of quality, the output of the DTSG is compared with that of a high precision HP8672A synthesizer. Set at 9.06 GHz, the HP8672A produces a noise floor that is 55 dB below the carrier, as indicated by Figure 3.7(b). The DTSG is generating a noise floor that is only 5 dB higher than that of the expensive and elaborate HP8672A synthesizer. Therefore, the DTSG is considered to be an ideal RF source for generating realistic target return signals for the Threat Radar Simulator.

A closer view of the spectral output of the DTSG, operating at zero doppler, is shown in Figure 3.8(a). The diagram confirms that no spectral noise exists within the target doppler band, which at X-band can range from 0 to 60 kHz, representing velocities of 0 to 1000m/sec respectively. In Figure 3.8(b), a doppler component of f_d=10kHz is added to the DTSG output to

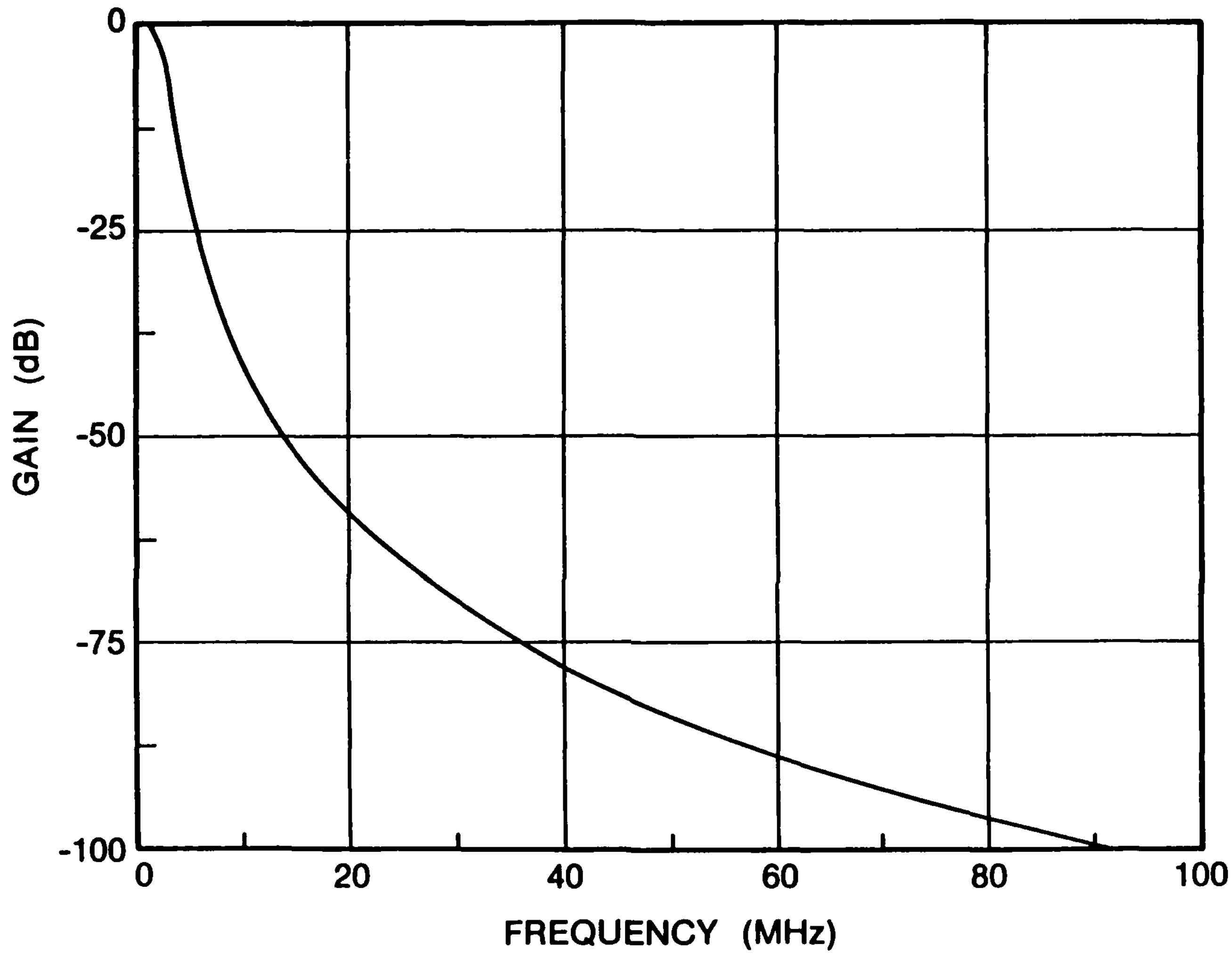


FIG. 3-5. Frequency Response of 3rd Order Butterworth LPF

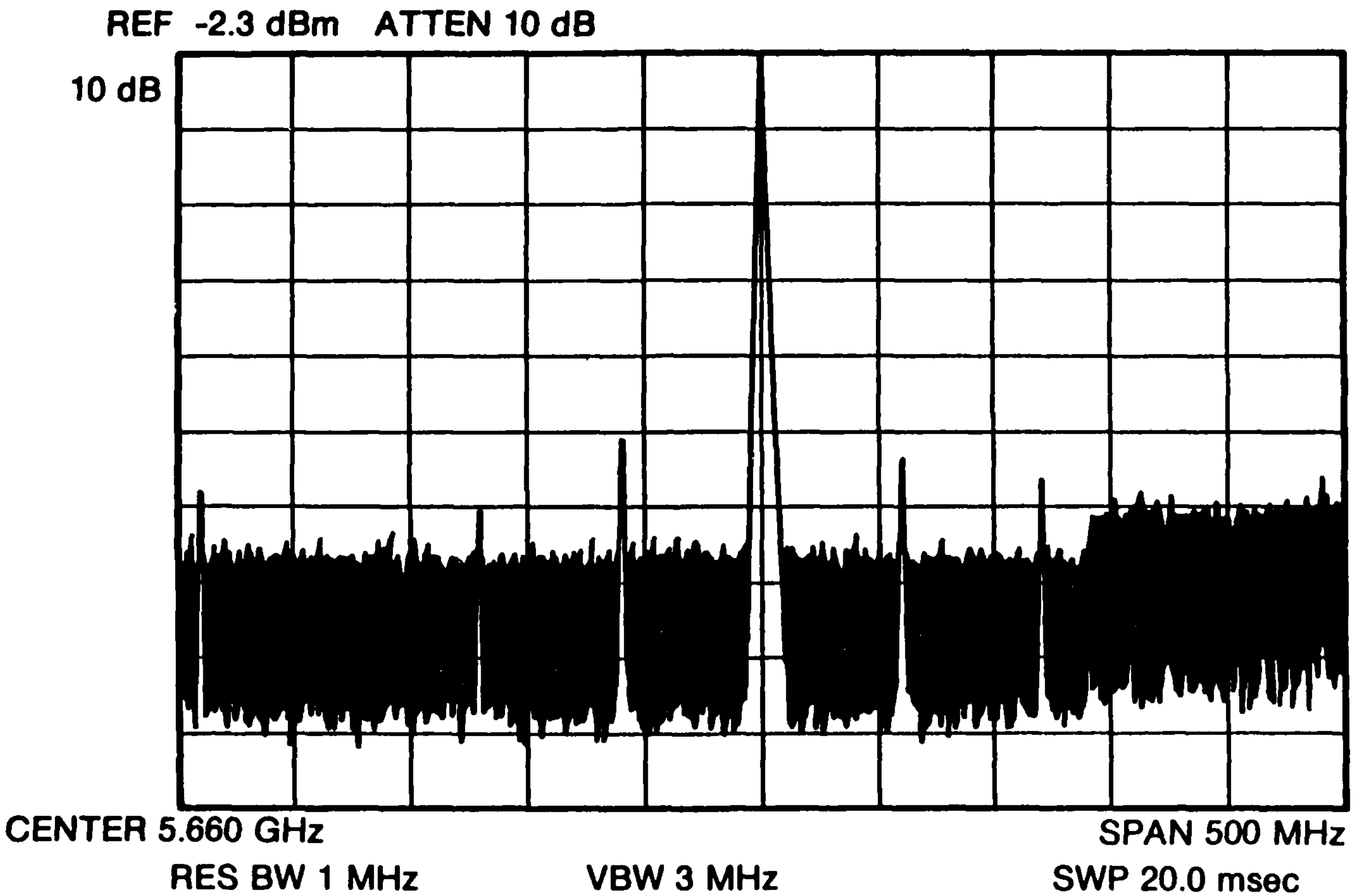
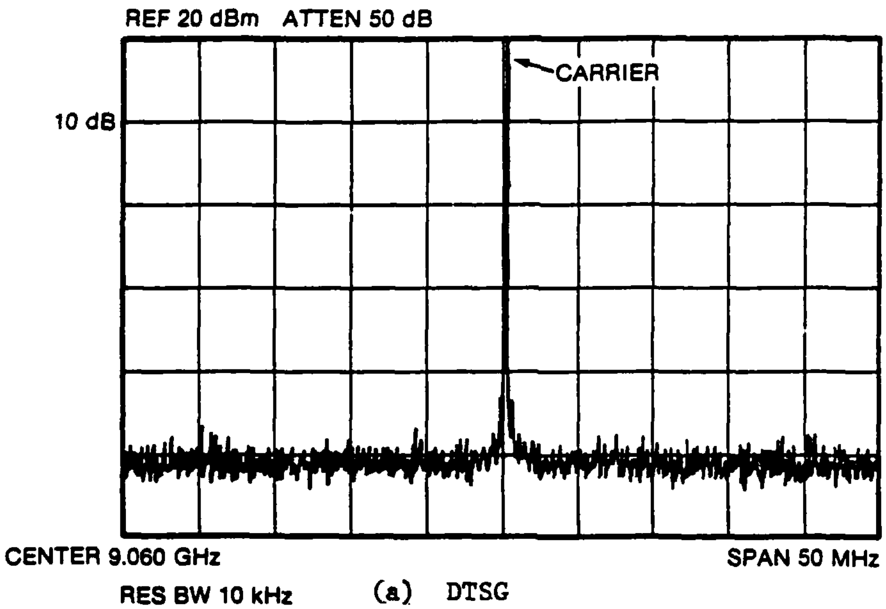
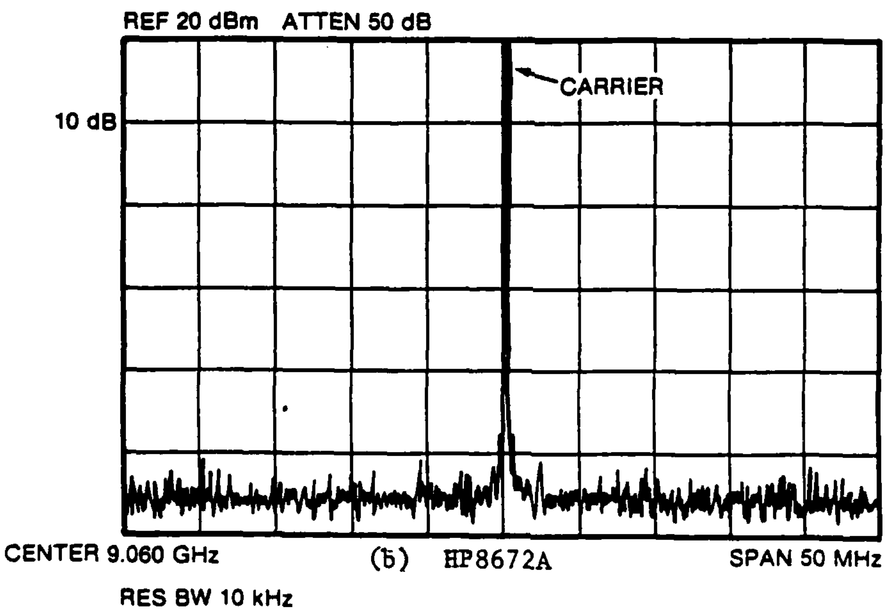


FIG. 3-6. Spectrum of VCO Output

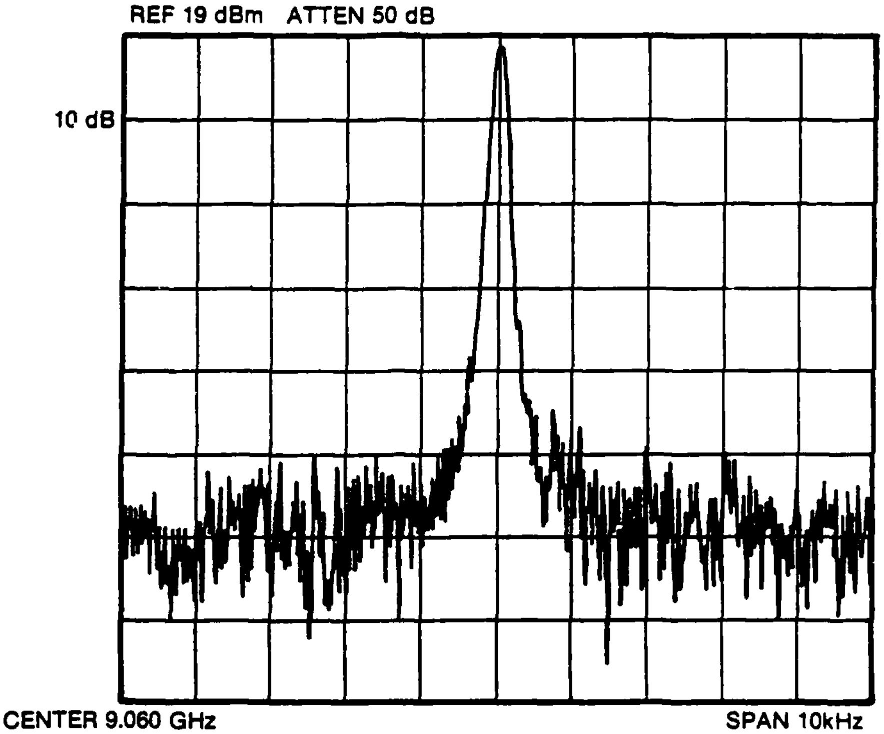


(a) DTSG

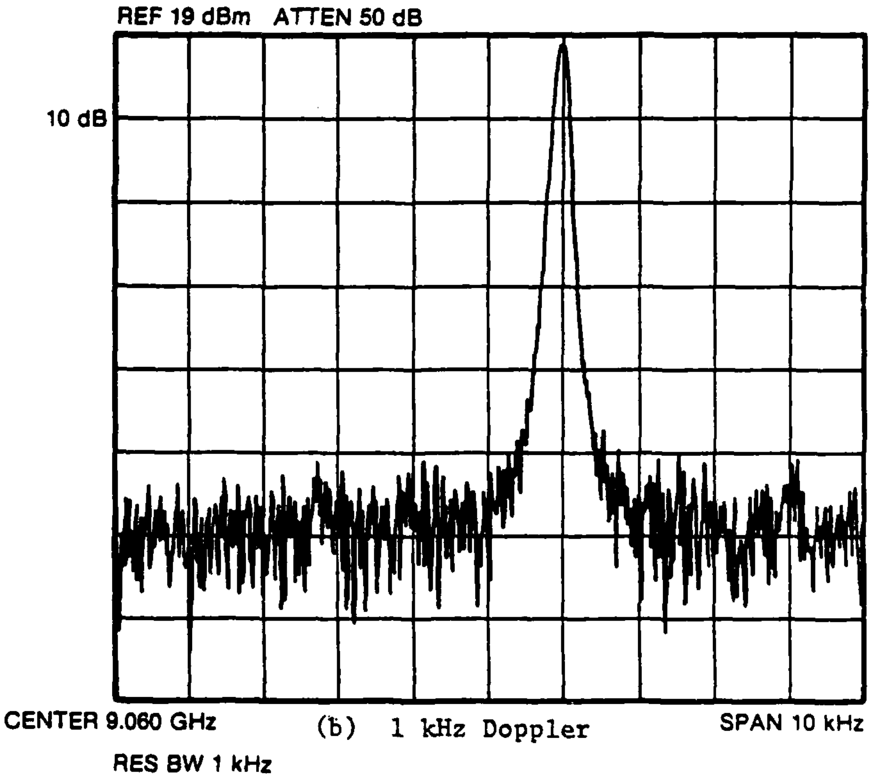


(b) HP8672A

FIG. 3-7. Comparing the Output Spectrum of the DTSG with an HP8672A Synthesizer set at 9.06 GHz



(a) Zero Doppler



(b) 1 kHz Doppler

FIG. 3-8. Output Spectra of DTSG With and Without Doppler represent a target travelling at 166m/sec. It is observed that the PLL process, used to mix the doppler signal with the 5.66 GHz source, does not alter the carrier signal or introduce spurious noise within the target doppler band. In contrast, the SSB technique introduces spurious components at multiples of the doppler frequency away from the carrier onto the output. This produces many false targets travelling at different velocities. Thus the DTSG, using the PLL circuit, is ideal for generating doppler components without affecting the target spectral profile or creating false targets.

3.4 VCXO Frequency Stabilization

VCXO's are generally very difficult to mechanically tune, and once set to the desired frequency, they tend to drift in time. To avoid these tuning problems, an automatic tuning circuit was implemented. The circuit is activated prior to running a scenario and locks the VCXO's to a 60 MHz reference frequency. The bias voltages required to tune the VCXO's are digitized. During run time, the bias voltage is added to the frequency tuning voltage from the VCXO driver. The short term drift of the VCXO is only $\pm$ 2Hz measured over several minutes, which is negligible.

A block diagram of the VCXO stabilization circuit is shown in Figure 3-9. The VCXO is initially locked to a 60 MHz reference immediately following the closing of SW1. The loop filter, which is a phase compensated integrator, provides the proper filtering at the output of the mixer. When SW2 is closed, the counter begins to count up or down, depending on the sign of the integrator output. The D/A converter output changes until the loop filter output is zero. When the run sequence begins, SW2 is opened causing the D/A output to remain locked at its present level. When SW1 is opened, the VCXO generates the correct doppler frequency proportional to the doppler control input.

SW1 and SW2 are controlled by the STAB command which originates from the host computer. Consequently, stabilization is achieved through software control.

3.5 Doppler Frequency Monitor

The doppler frequency monitor is a dual channel frequency counter which monitors the average doppler frequency of the two targets. The averaging is calculated over a 0.1 second or 1.0 second interval, as selected by the operator. An LED display indicates the doppler frequency of both channels.

The monitor determines the doppler sign (positive or negative) through I and Q channel demodulation of the VCXO signals. A block diagram of the monitor is shown in Figure 3-10. A brief explanation of its operation is now presented. Let the VCXO signal be denoted by s(t) and given by

$$s(t) = \cos(2\pi(f_{if} + f_d)t + \theta) \qquad (3\text{-}1)$$

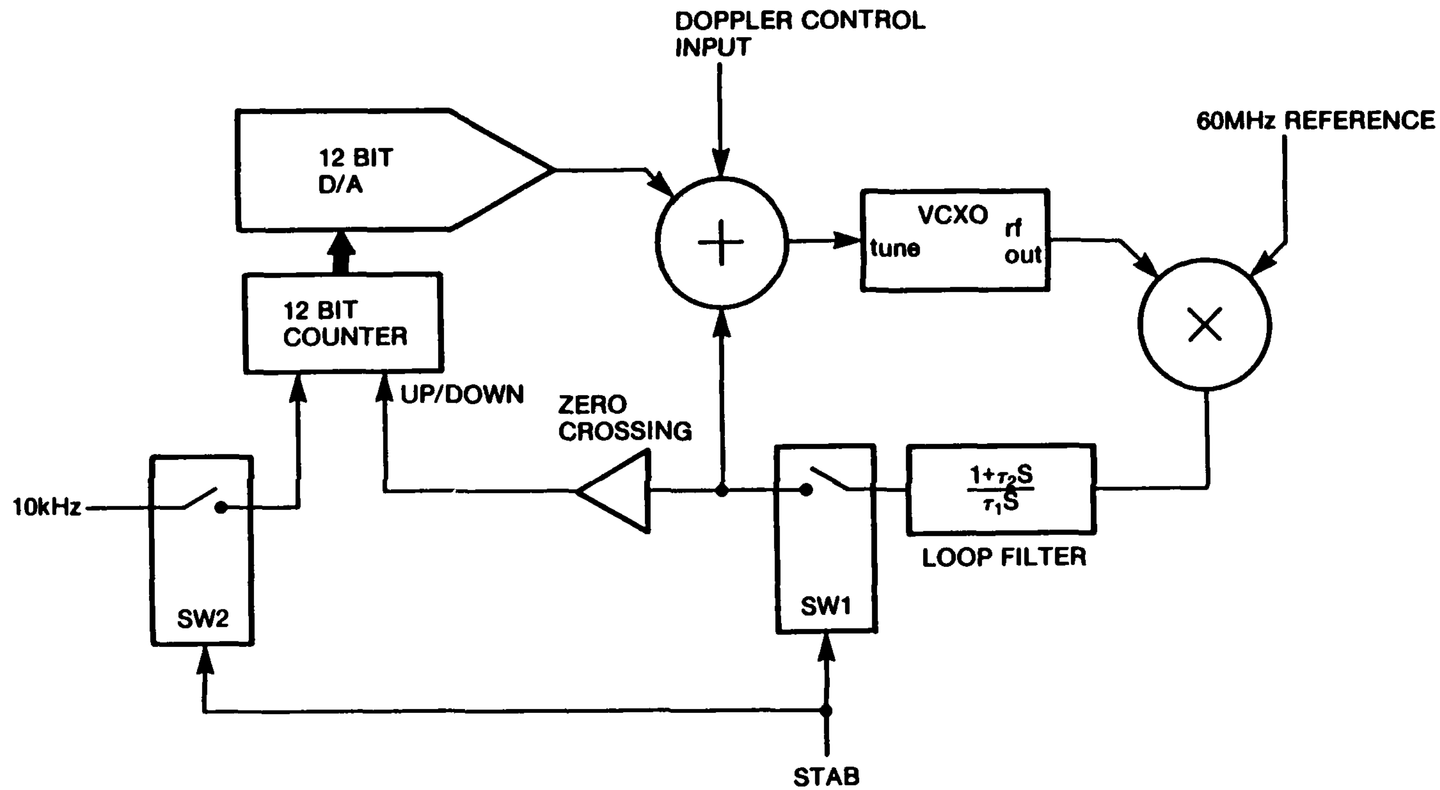


FIG. 3-9. VCXO Frequency Stabilization

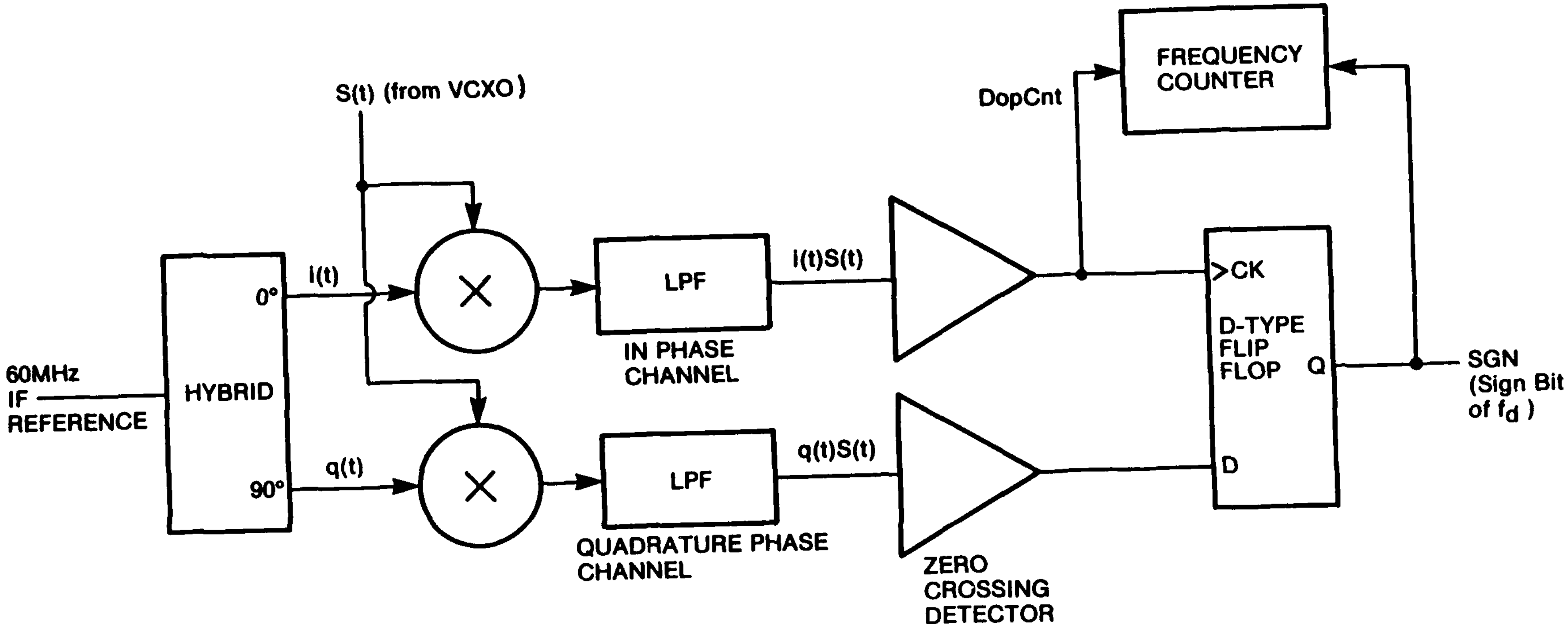


FIG. 3-10. Circuitry for Determining Sign Bit of the Doppler Frequency f_d

where

f_{if} - IF frequency of 60 MHz

f_d - Doppler frequency

Θ - Arbitrary phase constant

An IF reference signal at 60 MHz is used to provide two reference signals in time quadrature denoted as i(t) and q(t). They are given by:

$$i(t) = 2 \cos (2\pi f_{if} t) \qquad (3\text{-}2)$$

$$q(t) = 2 \sin (2\pi f_{if} t) \qquad (3\text{-}3)$$

The signal s(t) is multiplied by i(t) and q(t) and then filtered through low pass filters to form the products

$$s(t)\, i(t) = A \cos (2\pi f_d t + \Theta) \qquad (3\text{-}4)$$

$$s(t)\, q(t) = A \sin (2\pi f_d t + \Theta) \qquad (3\text{-}5)$$

It is seen from equation 3-4 and 3-5 that the sign of f_d is equivalent to the sign of s(t)q(t) at the instant of time that s(t)i(t) passes through zero on a positive transition. The D-type flip flop makes use of this fact to determine the sign of the doppler frequency. The s(t)i(t) signal is fed to the clock input of the flip-flop while the s(t)q(t) signal is fed to the D input. The output of the flip-flop, which represents the sign of f_d, takes on the sign of s(t)q(t) as s(t)i(t) makes a positive transition.

Only one counter circuit is used to monitor the frequency of the two target channels. Consequently, the two channels are multiplexed onto the same counter, as shown in Figure 3-11. The selection of the two channels is achieved by using two voltage controlled attenuators. The driving signals for the attenuators are EN1 and EN2 and are described below:

EN1 - Active high couples the output of VCXO1 into the power combiner.

EN2 - Active high couples the output of VCXO2 into the power combiner.

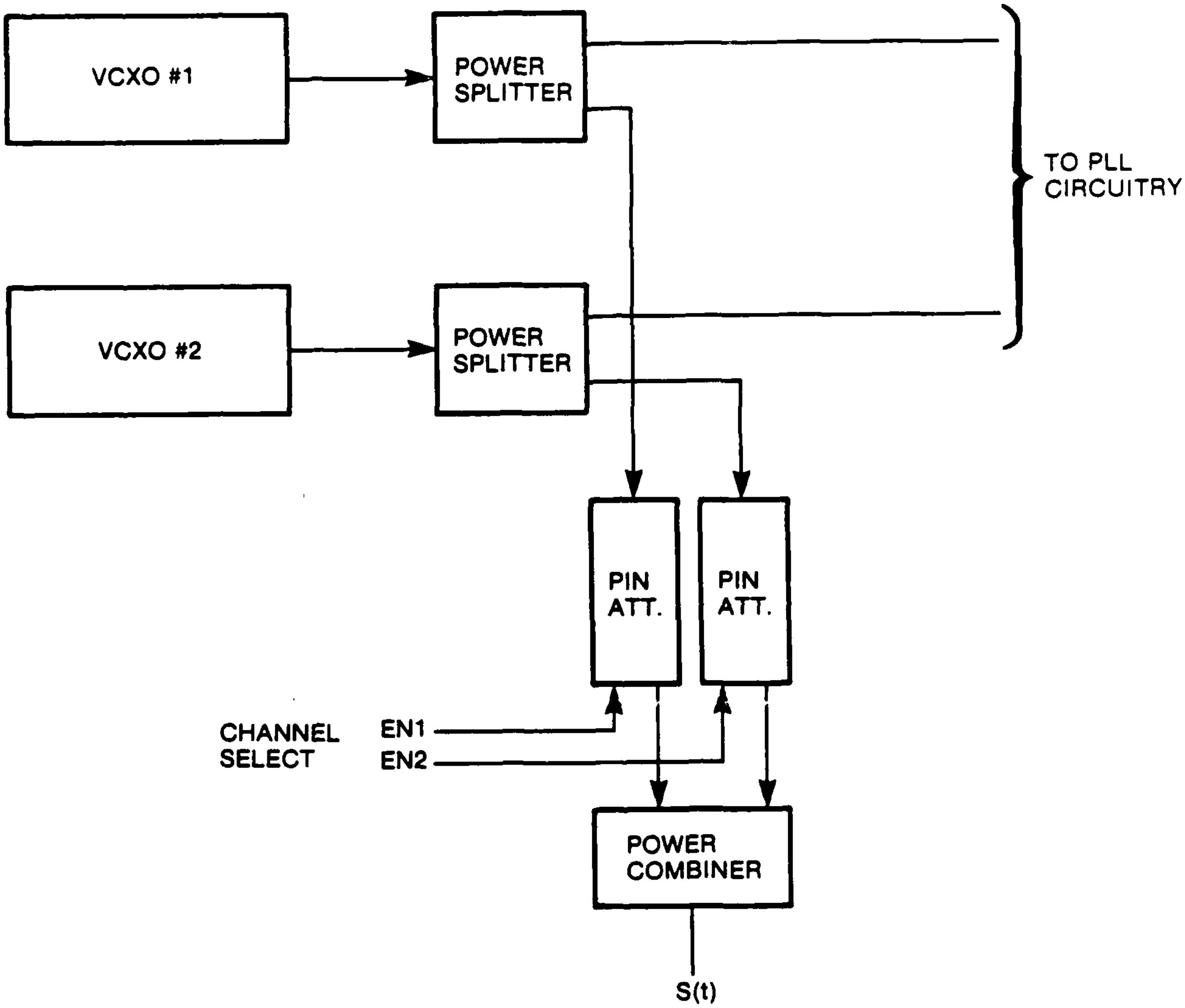


FIG. 3-11. Multiplexing VCXO Outputs into Frequency Counter

The signals passed to the frequency counter are (See Figure 3-10):

Dop Cnt - Zero detected form of i(t) in TTL compatible signal format.

SGN - Sign of the doppler frequency. SGN is high if the doppler frequency is positive.

A block diagram of the frequency counter is shown in Figure 3-12. A crystal oscillator based timer establishes the time interval for the counting. This interval can be selected, via a front panel switch, as 1 sec or .1 sec for 1 Hz or 10 Hz resolution respectively. A 5 digit BCD counter is used to count the doppler frequency during the timing interval. The counter output is latched using one of two 20 bit latches. The output of each latch is decoded and fed to an LED display.

4.0 DTSG CONTROL SECTION

The Doppler Target Signal Generator control section consists of three parts: The Computer Interface, the Digital Integrator, and the VCXO driver.The computer interface provides a link between the DTSG hardware and the host computer for the programming of doppler frequencies. The host computer periodically updates the target's radial velocity and acceleration from which the instantaneous velocity is calculated. The Digital Integrator is used to calculate the instantaneous velocity. This is accomplished by continually integrating the initial acceleration with time and adding the result to the initial velocity. The formula for this is shown below:

$$v_1 = V_{i1} + \int_o^t A_1 \, dt \tag{4-1}$$

$$v_2 = V_{i2} + \int_o^t A_2 \, dt \tag{4-2}$$

where

v_1 = Instantaneous velocity for target 1
v_2 = Instantaneous velocity for target 2
V_{i1} = Initial velocity for target 1
V_{i2} = Initial velocity for target 2
A_1 = Initial acceleration for target 1
A_2 = Initial acceleration for target 2

The VCXO driver consists of a digital to analog converter used to transform the instantaneous velocity into analog form to drive the 60 MHz VCXO. The doppler frequency generated is proportional to the voltage applied to the VCXO.

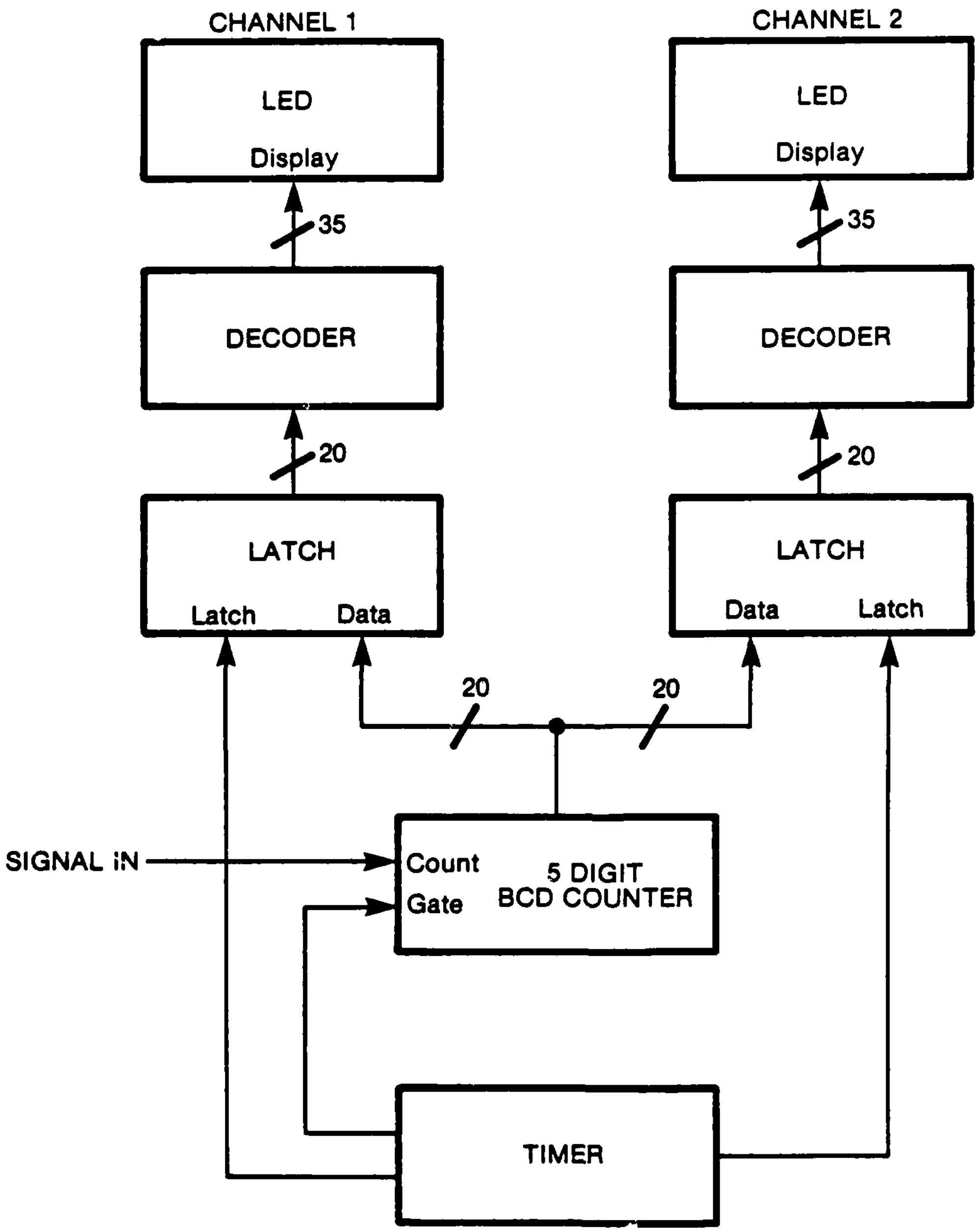


FIG. 3-12. Block Diagram of Frequency Counter

5.0 CONCLUSION

The Threat Radar Simulator (TRS) used in the Electronic Warfare Engagement Simulation Facility (EWESF) at DREO includes a Moving Target Indicator (MTI) processor. The MTI circuit makes use of the doppler frequency shift associated with moving targets to distinguish the target return from clutter. To provide the MTI processor with the necessary doppler frequency, a Doppler Target Signal Generator (DTSG) was developed at DREO. The DTSG can produce positive or negative doppler shifts to simulate targets that are travelling toward or away from the radar respectively. Although the Threat Radar Simulator at DREO is a non-coherent system, the DTSG is capable of providing phase perturbations that can be detected by a coherent radar. This is an important consideration since phase fluctuation in the pulse returns provides significant information to the radar about the target's spectral profile. Therefore in the event that the TRS should become coherent, the DTSG is capable of providing the necessary doppler side bands that are representative of real targets.

Due to the receiving sensitivity of the tracking radar, it is imperative that the DTSG produce doppler frequencies that contain very low spurious frequency components or unwanted side-bands at multiples of the IF frequency. For this reason, a phase lock loop (PLL) approach was used instead of the conventional Single Side Band technique for modulating the carrier frequency with the doppler frequency. Experimental results show that the PLL method provides up to 30 dB of spurious noise improvement over the SSB technique. This is an important consideration since it is essential that the tracking performance of the radar not be compromised due to poor target simulation.

6.0 REFERENCES

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(U) The Threat Radar Simulator (TRS), utilized in DREO's ECM facility, is equipped with a Moving Target Indicator (MTI) processor used to detect the skin echo of moving targets. The MTI unit makes use of a doppler shift, associated with the moving target, to discriminate between the target and unwanted clutter. To facilitate the MTI's requirement for doppler shifts in the return pulses, a Doppler Target Signal Generator (DTSG) has been developed at DREO. The DTSG is an X-band programmable frequency synthesizer with three independent outputs. Two of the outputs are used in the generation of target returns and the third output provides a doppler shift to the clutter return signal.

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Doppler Target Signal Generator
PLL
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TRS
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