





ROYAL SIGNALS AND RADAR ESTABLISHMENT

Test Report No 87/CC3/2

TITLE:	PERFORMANCE OF A RAPID CARRIER ACQUISITION CIRCUIT FOR SATELLITE GROUND TERMINAL MODEMS
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SUMMARY

The performance of a Rapid Carrier Acquisition circuit for low data rate satellite communications equipment is described. The results achieved for carrier acquisition at signal to noise ratios of 30 dBHz show that acquisition can be achieved in 300 milliseconds, giving two orders of magnitude improvement over currently implemented equipment. Details of performance with various modulation schemes and operation at signal to noise ratios as low as 25 dBHz are given.

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1. INTRODUCTION

The Rapid Carrier Acquisition circuit was designed as part of a satellite communications system, to find signals at low signal to noise ratios in a frequency uncertainty band of 12 KHz.

Existing PSK systems perform this task in around 40 seconds but the Rapid Carrier Acquisition circuit has been developed to improve on this and has demonstrated its ability to locate the signal in about 300 milliseconds; this having important implications for Low Data Rate satellite communications systems,

A detailed description of the working of this circuit can be found in Ref 1. This reference does not include details of the TMS 320 microprocessor control board, so the first section of this report is dedicated to providing an outline of the hardware/software designed for this critical part of the Rapid Carrier Acquisition circuit.

This report summarises the performance measurements taken when testing the circuit under the following conditions:

- a) Speed and accuracy in acquiring CW signals at various values of signal to noise ratio (C/kT) from 25 to 50 dBHz.
- b) Accuracy in acquiring PSK signals of differing data rates at various C/kT values.
- c) Accuracy in acquiring FSK signals of differing data rates at

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various C/kT values.

2. TMS320 MICROPROCESSOR BOARD

The results obtained from the circuit shown in Ref 1 were initially displayed as Argand (In Phase and Quadrative) diagrams on an oscilloscope for test purposes. This was achieved by connecting Digital to Analogue converters to the output latches on the Real (I) and Imaginary (Q) channels, and using them to drive the X and Y axes of the CRO. By selecting the relevant frequency bin (channel) on a set of seven DIL switches each bin could be examined in turn.

However, what was desired was a means of numerically showing which frequency bin held the largest signal, for feeding information to a demodulator circuit, and also to produce a "Spectrum Analyser" type of display of the 12 KHz band, for test purposes, on a CRO.

The requirement to store this data, integrate the contents of the frequency bins, perform arithmatic and then display the data was met by most microprocessors. However, due to availability and existing back-up facilities the TMS 32010 was chosen, (Figures 1, 2 and 3 show the circuit design).

The 12 KHz band was divided into 128 frequency bins each of 93 Hz width and since the TMS 32010 has 144 x 16 bits of on-board RAM it was ideal for this purpose. The basic operation of the circuit is as follows:

The microprocessor sends out the 7 bit address of the frequency bin to be sampled (intially bin 0). This is latched to the comparator on the Rapid

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Carrier Acquisition Board, which waits for the Real and Imaginary channel filters to reach and update the correct frequency bin store. When this occurs the data from these channels is latched through to the TMS 32010 via an EPROM. This EPROM takes the 8 bit values of the two channels and performs a sum of squares operation on them to produce a value of the power in the frequency bin. Within the TMS 32010, this value is then stored in the relevant on-board memory address and the next frequency bin address is sent to the Rapid Carrier Board. This process is repeated, so that all frequency bins are addressed in the following order: 0, 64, 1, 65, 2,66..... 63, 127, which is an efficient way of sampling. The TMS 32010 can easily process two frequency bins for each complete sweep (128 bins) by the filters.

In order to find the most powerful signal the location and size of the largest frequency bin is stored. As each frequency bin is sampled, it is compared with the value of the largest bin and replaces it if necessary.

Using the procedure outlined above, the program monitors all 128 frequency bins, and then checks are made to see if sufficient samples have been taken to identify the most powerful signal. One of the best ways of achieving this is to compare the value of the largest frequency bin with an average value of the rest of the frequency bins. When the difference exceeds a certain threshold, the sampling is stopped and the results are displayed. This threshold can be set, and thus optimised, on 8 DIL switches which are read at the beginning of the program.

When the microprocessor has decided that the signal has reached the threshold condition it drops into a continuous output-display loop. In this loop, the number of the frequency bin which contains the largest

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signal is displayed on seven LEDs and the contents of each frequency bin memory address is sent through a digital to analogue converter to the CRO for display. Each "frame" of 128 frequency bins sent to the CRO is preceeded by a sync pulse, to trigger the display. When incorporated in a modem, the Rapid Carrier Acquisition Processor Board will provide details of the frequency bin to the demodulator for signal demodulation. This will occur approximately every 300 milliseconds at 30 dBHz.

3. DESCRIPTION OF TEST SYSTEM

Figure 4 shows the system used to test the Rapid Carrier Acquisition circuit.

The carrier signal is generated by a synthesiser at 52.173 MHz ± 6 KHz and is fed into a satellite link simulator box. This produces signal plus noise at 70 MHz (± 25 MHz) and this combination enters the front-end stages of a standard manpack modem [See Ref 3]. After a series of down mixers and crystal filters, the signal emerges at 93 ± 6 KHz.

It is this noisy signal that is checked on the spectrum analyser to establish the signal to noise ratio before it is fed to the front-end circuits of the Rapid Carrier Acquisition Board. These components convert the signal to 0 to 12 KHz and hard-limit it to produce a square-wave which is sampled at 24 KHz by the main rapid acquisition circuits.

4. PERFORMANCE USING CW SIGNALS

4.1 ACCURACY

The main purpose of these tests was to check if the Rapid Carrier

Acquisition circuit could accurately indicate in which frequency bin the CW signals occured.

Measurements were taken at signal to noise ratios of 25, 27, 30, 35, 40 and 50 dBHz - these being typical values expected for various equipment and data rate types. The signal to noise ratio was measured at 93 \pm 6 KHz at the point where the signal was fed into the front-end circuits. The measurement was made on a Spectrum Analyser and the following correction factor was applied [See Ref 4].

Carrier Energy = S dBm Noise Energy = N dBm Resolution Bandwidth (of Analyser) = F Hz $C/kT = 10 \log (1.2 \times F) + S - (N+2.5) dBHz$

For each signal to noise value measurements were made at the following frequencies: 88.5 KHz, 90 KHz, 93 KHz, 96 KHz and 97.5 KHz. These correspond to frequency bin numbers of: 16, 32, 64, 96 and 112 respectively.

i. C/kT = 25 dBHz

Figures 5 to 9 show both the Spectrum Analyser display and the Rapid Carrier Acquisition Board display on the CRO.

Figure 5 shows the response with the signal at 88.5 KHz. The tailing off of the spectrum at the end is due to the cut-offs in the modem filters, but this does not affect the _RO display, which clearly shows the signal. The LED display indicated that the signal was in bin 15.

Figure 6 shows a 90 KHz signal. This again is seen clearly on the CRO and

the LEDs displayed bin number 31.

Figure 7 gives the response at 93 KHz. Here the bin number was 63.

Figure 8 shows a signal at 96 KHz. The corresponding frequency bin number was 96.

Finally, Figure 9 shows the signal at 97.5 KHz. The frequency bin number was 111.

ii. C/kT = 27 dBHz

Figure 10 shows a 27 dBHz signal at 88.5 KHz. Again the CRO display is clear and the frequency bin number displayed is 15.

In Figure 11, the signal is at 90 KHz and is found in bin 32.

Figur: 12 shows the 93 KHz signal. The Rapid Carrier Acquisition circuit identified this signal as being in bin 64.

Figures 13 and 14 shows signals at 96 KHz and 97.5 KHz. These were calculated to be in bins 95 and 111, respectively.

iii. C/kT = 30 dBHz

Figures 15 to 19 show signals at 30 dBHz. In the photographs of the CRO displays, the signals do not appear to be any taller than those at 25 dBHz. This is because the data lines from the TMS 32010 to the DAC were changed, in order to prevent the signal on the CRO display from becoming too large.

In Figure 15, the signal is at \$8.5 KHz and the frequency bin was found to be number 15.

In Figures 16 to 19, the signal frequencies were 90, 93, 96 and 97.5 KHz, whilst the frequency bin numbers were 31, 63, 95 and 111, respectively.

iv. C/kT = 35 dBHz

In Figures 20 to 24 the same group of frequencies was used, and again the frequency bin numbers were 15, 31, 63, 96 and 111 respectively.

v. C/kT = 40 dBHz and above

The Rapid Carrier Acquisition circuit was tested with signal to noise ratios of up to 50 dBHz. At these levels the circuit achieved the same results as at 35 dBHz, only in a shorter time.

4.2 ACQUISITION TIME

The most accurate way to measure the speed of the Rapid Carrier Acquisition circuit was to use a counter/timer. This was triggered when the TMS 32010 was reset and stopped when the first sync pulse was sent to the CRO. Thus giving an accurate response to the acquisition time.

Initially a signal to noise ratio of 25 dBHz was used, and the threshold number on the 8 DIL switches set to provide an unambiguous response at this ratio. Thereafter the number was unaltered for all measurements and found to be 0010 1010. Figure 25 shows the results obtained and looking at the graph in Figure 26 it can be seen that even at 25 dBHz, the acquisition time is no greater than 700 milliseconds.

At 30 dBHz, which is about the lowest signal to noise ratio at which existing modems operate and at which data can be transmitted at a BER of 10^{-4} at 50 bps, the time is only 300 milliseconds. This value falls to about 90 milliseconds at 50 dBHz.

One interesting observation, is that at values of C/kT below 30 dBHz, the times fall into two discrete bands. One band is around 300 to 400 milliseconds and the other is around 700 milliseconds. At 29 dBHz, most of the results are about 300 milliseconds. At 28 dBHz a few are at 700 milliseconds. As the signal to noise ratio falls to 25 dBHz, fewer results are at 300 milliseconds and more are at 700 milliseconds. As yet no explanation has been found for this anomaly, although it could be a feature of the threshold decision software, and does not seriously affect the performance of the circuit.

5. PERFORMANCE USING PSK SIGNALS OF VARIOUS DATA RATES

In order to test the Rapid Carrier Acquisition circuit with PSK signals a signal generator was used to provide a square wave to externally modulate the input signal in Fig 4. Having set the carrier frequency and a phase shift of about π radians, a signal at a frequency equal to half the data rate was set on the modulating signal generator.

The tests were performed with data rates of 50, 75, 300 and 2400 bits per second (typically used data rates), at signal to noise ratios of 30, 40 and 50 dBHz.

a) C/kT = 30 dBHz

Figures 27 and 28 show PSK signals at 93 kHz and data rates 50 and 75 bps. Both signals appear to look like CW signals on the CRO display due to the resolution limits imposed by the 93 Hz bin width. The LED display identifies the signal as being in frequency bin 64, in both cases.

The spectrum analyser trace of Figure 29 clearly shows the two peaks of the 300 bps PSK signal, this was identified as being in bin 63.

A 2.4 kbp/s signal was used in Figure 30. Here the peaks are 2.4 KHz apart and the frequency bin was identified as bin 51, which is 1.2 KHz lower than bin 64, but corresponds to one of the sidelobes of the PSK signal.

b) C/kT = 40 dBHz

In Figures 31 and 32, the signals are in bin 64 and can be clearly identified on the CRO display.

In Figure 33, the CRO display shows a slightly broader signal, with two peaks just visible. The highest energy in this 300 bps signal was found in frequency bin 63.

In Figure 34, the first lower sidelobe of the 2.4 kbps signal was again identified as being in bin 51. It is also possible to see the peaks of the other sidelobes starting to appear.

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c) C/kT = 50 dBHz

Figure 35 shows a 50 bps PSK signal at 50 dBHz, and again it is found in bin 64.

In Figure 36 the 300 bps signal produces a much broader image on the CRO display. Here the signal is identified as being in bin 62.

Figure 37 shows the 2.4 kbps signal. Here the CRO display shows all the sidebands and the carrier has reappeared. With this signal the microprocessor decided the upper sideband was the largest, and displayed bin 77.

6. PERFORMANCE USING FSK SIGNALS OF VARIOUS DATA RATES

To test the Rapid Carrier Acquisition circuit with FSK signals, the procedure was very similar to that using PSK. The carrier frequency and a frequency shift (of about twice the data rate) were set on the synthesiser. The signal generator then modulated the synthesiser with a square wave at a frequency equal to half the data rate. Thus for 75 bps, the frequency shift was 150 Hz and the signal generator frequency was about 37.5 Hz.

As with the PSK signals, data rates of 50, 75, 300 and 2400 bps were tested at signal to noise ratios of 30, 40 and 50 dBHz.

a) C/kT = 30 dBHz

Figure 38 shows a 50 bps FSK signal at 30 dBHz. Only a single peak can be

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seen on the CRO display, and this was in bin 64.

In Figure 39, two peaks can be observed, and the TMS 32010 decided that the 75 bps FSK signal was in bin 65 (the upper peak).

Two peaks can be seen clearly on the CRO display in Figure 40. This time the data rate was 300 bps and the frequency bin was number 62.

In Figure 41, the two peaks of the 2.4 kbps signal are again visible. This time the frequency bin displayed is number 39, which is 2.4 KHz from the carrier.

b) <u>C/kT 40 dBHz</u>

Figure 42 shows the 50 bps peak in bin 64.

Figure 43 shows the beginning of two peaks. The TMS 32010 located this signal in frequency bin 63.

The peaks of the 300 bps signal in Figure 44 broaden the signal in the CRO display, and this time the microprocessor decided that the signal was in bin 62.

The 2.4 kbps signal in Figure 45 caused multiple peaks, and most of these can be seen in the CRO display. The lower 'main' peak was in bin 39 and the upper 'main' peak in bin 90.

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c) C/kT = 50 dBHz

In Figures 46 and 47, the signals were in bins 64 and 61 respectively.

In figure 48 most of the peaks can be seen on the CRO display, and this time the signal was found to be in bin 39.

7. ALIASING

In the course of testing the Rapid Carrier Acquisition circuit it was found that certain carrier frequencies caused aliasing problems. In fact the first of these frequencies was found to be d.c. and the effect was observed when no signal or noise entered the Rapid Carrier front-end circuits.

Figure 49 shows the response to d.c., with an exponential decay and the biggest alias peak in about bin 85 (7.9 KHz or 94.9 KHz at the front end circuit).

Following this observation, calculations were made to determine all other possible aliasing frequencies. The result was that three pairs of frequencies were discovered and measurements confirmed their existance and exact position in the 12 KHz band. The first pair are shown in Figure 50. In both photographs a pure signal at about -15 dBm, with no noise, was used.

In photograph a), a signal was fed to the front end circuits at 89.4 KHz (bin 25) which produced an alias in bin 76/77. Photograph b) shows the reverse, when a signal at 94.2 KHz (bin 76/77) produced an alias in bin 25. Both these results confirmed the theoretical calculations.

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The second pair of frequencies are shown in Figure 51, using the same signal level, and no added noise. Photograph a) shows a 90 KHz (bin 32) signal with aliasing in bin 96, and photograph b) shows a 96 KHz (bin 96) signal with aliasing in bin 32. These results are also confirmed by theory.

The final pair of frequencies are shown in Figure 52, using the same method as above. Photograph a) shows a 91.8 KHz (bin 51) signal producing an alias in bin 102, and a 96.6 KHz (bin 102) signal giving an alias in bin 51. Again these results were predicted by the theory.

All the above measurements were made using a large signal and no noise. When noise was added and measurements taken with signal to noise ratios in the range 25 to 50 dBHz, the aliasing frequencies were too small in amplitude to be observed, hence having no effect on the performance of the Rapid Carrier Acquisition Circuit.

8. CONCLUSIONS

Existing modems operating a 50 bps data link, take up to 40 seconds to acquire a 30 dBHz signal and lock to it. The Rapid Carrier Acquisition circuit has clearly demonstrated its unfailing ability to acquire the same signal in about 300 milliseconds. When used in conjunction with the phase locked loop described by J. Pritchard in Ref 2, which is able to carrier lock and track in less than a second, this has significant consequences for future modems. The ability to lock onto a signal and start to demodulate it in about a second allows the use of simplex "PTT" operation. Since the transmitter is only switched on a second before passing data, the 'transmitter-on' time is drastically reduced compared to existing PSK satcom equipment with a corresponding reduction in vulnerability to detection. A reduction in 'transmitter-on' time helps conserve battery power - vital for man-portable communication systems. The Rapid Carrier Acquisition circuit has also demonstrated that various modulation schemes such as PSK and FSK, have no detrimental effect on its performance. The Rapid Carrier Acquisition circuit can identify a signal at low signal to ratios with an accuracy of ± 1 bin (93 Hz) - which is within the lock limits (\pm 180 Hz) of the PLL described in Ref 2.

REFERENCES

Ref 1 RSRE Memorandum No 3925.

'A compact digital communications system. Part 1: Rapid Carrier Acquisition'.

Authors: S P Luttrell and J A S Pritchard.

- <u>Ref 2</u> RSRE Memorandum No 4027. 'A compact digital communications system. Part 3: Generalising the phased locked loop'. Author: J A S Pritchard.
- <u>Ref 3</u> "A Manpack Satellite Communications Earth Station", C H Jones, The Radio and Electronic Engineer, Vol. 51, No 6, June 1981.

Ref 4 H.P. Application Note 150-4, April 1974.

FIG 1 BLOCK DIAGRAM OF INTERFACE BETWEEN RAPID CARRIER ACQUISITION CIRCUIT AND TMS320









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FIG 3b R.S.R.E. FAST SIGNAL ACQUISITION BOARD (1)



FIG 4 TEST SYSTEM FOR RAPID CARRIER ACQUISITION CIRCUIT



I/P TO FAST ACO. CCT AT 25 dB Hz 16 7/87. REF .0 dBm ATTEN 10 dB





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5 dB

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5 dB/

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MKR 96.12 kHz -31.25 dBm SPAN 12.00 kHz SWP 300 sec ATTACKAT TO ¥ AMA **MANA** VBW 1 Hz كريني يليل كمسيا معطيت التر مكالملك الملاميات إن المطالبات مكالم المالية والمناقب والمناقبة والمناق FIG 13 and a second and a second a CENTER 93:00 kHz RES BW 100 Hz •

I/P TO FAST ACQ. CCT. AT 27 dB Hz. 17/7/87. REF .0 dBm ATTEN 10 dB



5 dB/

Q





5 dB


F

I/P TO FAST ACO, CCT, AT 30 dB Hz, 1777'87. REF .0 dBm ATTEN 10 dB

MKR 96.05 kHz -28.65 dBm



5 dB

I/P TO FAST ACQ. CCT. AT 30 dB Hz 17/7/87. REF .0 dBm ATTEN 10 dB

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MKR 97.56 kHz -29.85 dBm





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5 dB/

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5 dB/

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C/kT (dB Hz)									Acqui	isition	Time	(sm)								
25	688	710	715	969	701	688	683	401	320	707	710	686	691	969	680	388	693	694	385	704
26	669	686	707	697	691	702	969	694	393	385	293	683	693	336	330	383	309	710	697	669
27	385	685	694	314	694	393	669	323	674	694	696	· 299	312	342	688	669	697	318	702	393
28	307	347	696	306	339	303	323	388	309	339	312	328	374	314	320	331	312	382	699	311
29	969	307	315	309	322	307	309	309	307	301	317	331	315	312	312	686	295	306	320	326
30	312	307	307	322	315	301	320	320	320	317	314	279	307	323	621	315	314	312	315	314
32	182	204	239	239	219	187	241	236	250	212										
34	121	239	206	204	225	168	190	193	166	190										
36	139	141	144	133	160	162	152	136	147	163										
38	117	120	128	119	122	133	128	133	127	141										
40	98	106	98	108	100	117	105	103	109	111										
45	95	87	6	92	89	6	96	89	85	87										
50	92	87	87	89	92	87	87	87	87	82										

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FIG 25 CARRIER ACQUISITION TIMES





75 bps PSK at 30 dB Hz. 21/7/87. REF .0 dBm ATTEN 10 dB

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5 dB/

SPAN 12.00 kHz SWP 300 sec VBW 1 Hz مهرمي معد علم معلمه معلمه من المعلم ركم المعصد والمعول المعالم والمعالم والمعار والمعالم معد المعلم مع المعالي ا 2.9.75 A. 1.1.7 P. ADDER PROVING - FIG 28 -CENTER 93.00 kHz RES BW 100 Hz



300 bps PSK at 30 dB Hz. 21/7/87. REF .0 dBm ATTEN 10 dB

2.4K bps PSK at 30 dB Hz - 21 7 87 REF - 0 dBm - ATTEN 10 dB

5 dB/

SPAN 12.00 kHz SWP 300 sec ومر بالمردان والإلار المراسلين and a second and a second a present of the property of the second of the VBW 1 Hz 5 _ FIG 30 _ Contraction and a second second CENTER 93.00 kHz RES BW 100 Hz



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5 dB.



2.4K bps PSK at 40 dB Hz 2177.87. REF 5.0 dBm ATTEN 20 dB

5 dB.



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300 bps PSK at 50 dB Hz _21 _367 REF 30.0 dBm = A11EN 40 dB



2.4K bps PSK at 50 dB Hz. 21/7/87. REF 30.0 dBm ATTEN 40 dB

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75 bps FSK at 30 dB Hz, 21/7/87. REF .0 dBm ATTEN 10 dB

300 bps FSK at 30 dB Hz. 21-7-87. REF .0 dBm ATTEN 10 dB



SPAN 12.00 kHz SWP 300 sec

CENTER 93.00 kHz DEC RW 100 Hz

VBW 1 Hz



2.4K bps FSK at 30 dB Hz. 21/7/87. REF .0 dBm ATTEN 10 dB

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2.4K bps FSK at 40 dB Hz. 21/7/87. REF 5.0 dBm ATTEN 20 dB



10 dB



10 dB/

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10 dB

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ALIASING WITH D.C.

FIG 49



ALIASING WITH SIGNAL AT 89.4 kHz



ALIASING WITH SIGNAL AT 94.2 kHz

FIG 50



ALIASING WITH SIGNAL AT 90 kHz



ALIASING WITH SIGNAL AT 96 kHz

FIG 51



ALIASING WITH SIGNAL AT 91.8 kHz



ALIASING WITH SIGNAL AT 96.6 kHz

FIG 52
DOCUMENT CONTROL SHEET

Overall security classification of sheet UNCLASSIFIED

(As far as possible this sheet should contain only unclassified information. If it is necessary to enter classified information, the box concerned must be marked to indicate the classification eq. (R) (C) or (S).)

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1. DRIC Reference (if known)	2. Originator's Reference TEST REPORT 87/CC3/2	3. Agency Reference	4. Report Si U/C	ecurity Classification
5. Originator's Code (if	6. Originator (Corporate Author) Name and Location			
known) 778400	RSRE, ST ANDREWS ROAD, MALVERN, WORCS WR14 3PS			
5a. Sponsoring Agency's Code (if known)	6a. Sponsoring Agency (Contract Authority) Name and Location			
7. Title	<u></u>			
PERFORMANCE OF A RAPI TERMINAL MODEMS	D CARRIER ACQUISITIO	N CIRCUIT FOR SATE	LLITE GROU	ND
7a. Title in Foreign Language	(in the case of translation	15)		
7b. Presented at (for conference napers) Title, place and date of conference				
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Abstract				
The performance of a l satellite communication carrier acquisition a acquisition can be ac	Rapid Carrier Acquis ons equipment is des t signal to noise ra	ition circuit for cribed. The resul tios of 30 dBHz sh	low data r ts achieve ow that	ate d for

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